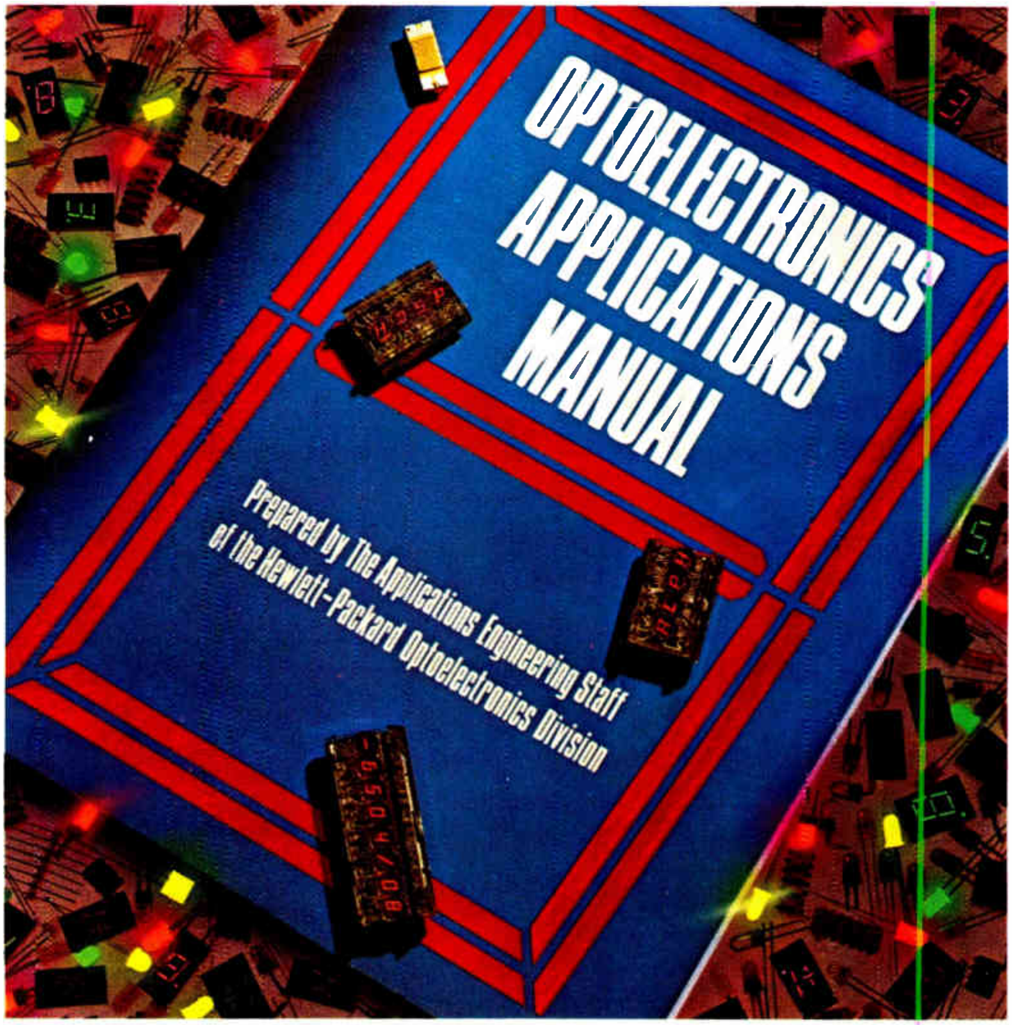
SURPRISE!



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FEBRUARY 2, 1978

WHAT THE CARTER BUDGET HOLDS FOR ELECTRONICS/73

Pitfalls in dynamic-RAM board design, and how to avoid them/104

Try forward converters for better switching power supplies/119

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097/47

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Electronics

The International Magazine of Electronics Technology

Vol. 51, No. 3 • February 2, 1978

Highlights

Cover: 6800 family grows, compatibly, 95
The 6800 microprocessor family is growing, with a two-chip version out and single-chip and high-performance versions in the works. The new models are software-compatible with the original processor, as will be the next-generation microcomputer family.

Cover designed and photographed by Art Director Fred Sklenar.

NATO, R&D are big budget items, 73
President Carter's first budget stresses tactical weapons, especially for the Army, as part of his strong support for the North Atlantic Treaty Organization. Also in for a boost are high-technology military and civilian research and development funds.

Microprocessors supervise mini's I/O, 104
A natural for supervising minicomputer input/output tasks is the dedicated microprocessor. Such distributed I/O processing will be a speedy, low-cost implementation.

Dynamic RAM systems can be painless, 109
Designing systems that use dynamic random-access memories need not be traumatic. The key principles to follow are adequate margins in power distribution and signal timing.

And in the next issue . . .
What the ISSCC presages for semiconductor devices . . . a 16-bit central processor joins the 8080 family . . . an improved tantalum capacitor has higher reliability.

Electronics

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Publisher's letter

Although microprocessors, memories, and other semiconductor devices always seem to steal center stage, there's still a lot of interest in such supporting-cast performers as power supplies—without which the show would not go on. On page 119 is an informative article about dc-dc converters that enable switching power supplies to handle 5 volts at a hefty 1 kilowatt, a noteworthy feat. A comparison of two recent circuits with the widely used push-pull converter is presented by Kees van Velthooven and Hugo Koppe from the semiconductor lab of the Dutch company Philips, who each have tapped more than a decade's worth of experience in power-control design in writing this article.

The Federal budget, like the proverbial New Year's resolution, is full of good intentions. Although it paints a picture of what a President would like to see accomplished, what finally emerges from the debates and compromises of the congressional process is always somewhat different.

Still, the budget serves to show the broad outlines of the impact of Federal spending—and nonspending—in the near future. Thus, our detailed report on what the budget proposes has become an early-year tradition with us.

This year's edition was compiled by our Washington bureau manager, Ray Connolly, after a weekend round of press briefings and long hours of research into the thousands of pages that make up the budget documents. For the first time, though, the New York expeditionary force sent down to help in putting the report together did not make it. The worst snowstorm to hit the East Coast in a decade closed the airports and stalled the trains. So Ray had to handle the time-consuming digging, sifting, and questioning alone. You'll find his report starting on page 73.

As we do every year, we have compiled an annual index of the news stories, technical articles, newsletters, and new products that have appeared in *Electronics*. If you would like a copy of the 1977 index, circle number 340 on the reader service card and send it in.

February 2, 1978 Volume 51, Number 3 96,121 copies of this issue printed

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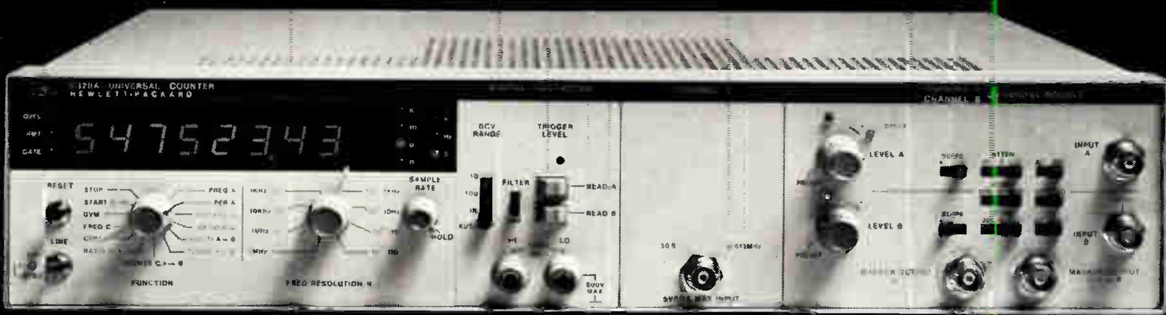
HP 5328A Universal Counter. The Right Performance At The Right Price.



If you're looking for a medium priced universal counter with the capability to do just about any counting job and the versatility demanded by tough systems applications, look no further.

For only $1300* the HP 5328A Universal Counter is a basic 100 MHz/100ns instrument that expands to meet your needs. Optional modules let you expand its capabilities to 512 or 1300 MHz and 10 ns time interval.

You can select an optional built-in DVM (single-ended or full floating, 10 μv to 1000v) for accurate determination of trigger levels and for external digital voltage measurements. Only HP offers it.

Other options let you make use of an ultra-stable time base and HP Interface Bus Operation including full remote control of the counter and the DVM.

Sound good?

There's more information available for you on the HP 5328A Universal Counter and the full line of sophisticated HP electronic counters.

Just call your nearby HP field office or write for our new electronic counter brochure.

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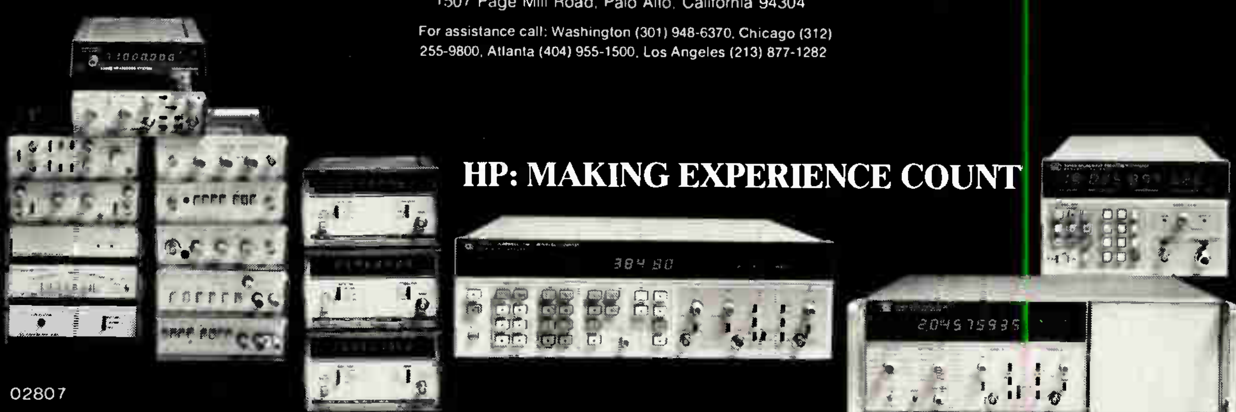

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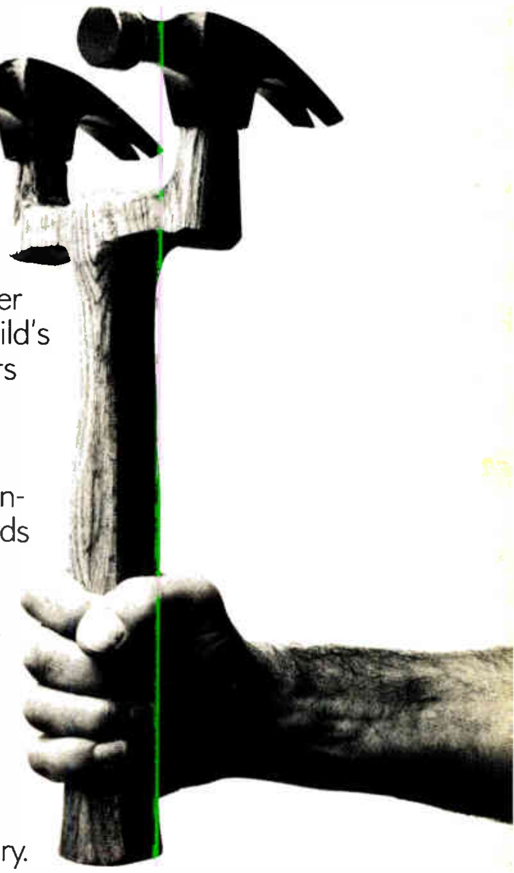


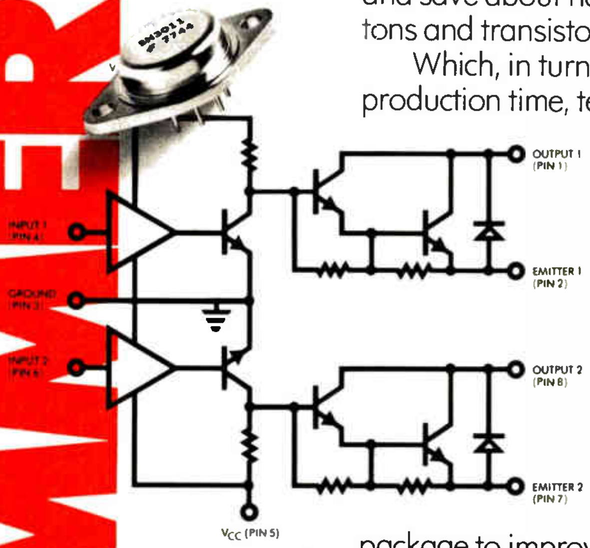
If you're looking for higher current and higher voltage without paying higher prices, Fairchild's new SH3011 Dual 5-amp Hammer Driver hits the nail on the head.

BIG SAVINGS.

Our new dual hammer driver was designed as an alternative to 2½" x 2½" circuit boards that end up costing you a small fortune in time and parts.

So now whenever you need high-power for driving impact printer heads, solenoids or motor controls, you can plug in a SH3011 and save about half the TTL gates, darlingtons and transistors you'd need otherwise.

Which, in turn, saves you insertion time, production time, test time, labor and inventory.



And all those savings added together can greatly reduce your overall system cost.

BIG PERFORMANCE.

Each of the SH3011's two independent hammers is capable of sinking 5-amps of current. Each output is designed to withstand 80 volts between the collector and emitter. And each driver is TTL compatible.

The SH3011 comes compactly and hermetically sealed in a steel, 8 lead TO-3 package to improve reliability and eliminate heat sink.

For details on our newest Hybrid (or other Hybrid products), just contact your Fairchild distributor or representative. For more immediate results call your nearest Fairchild sales office.

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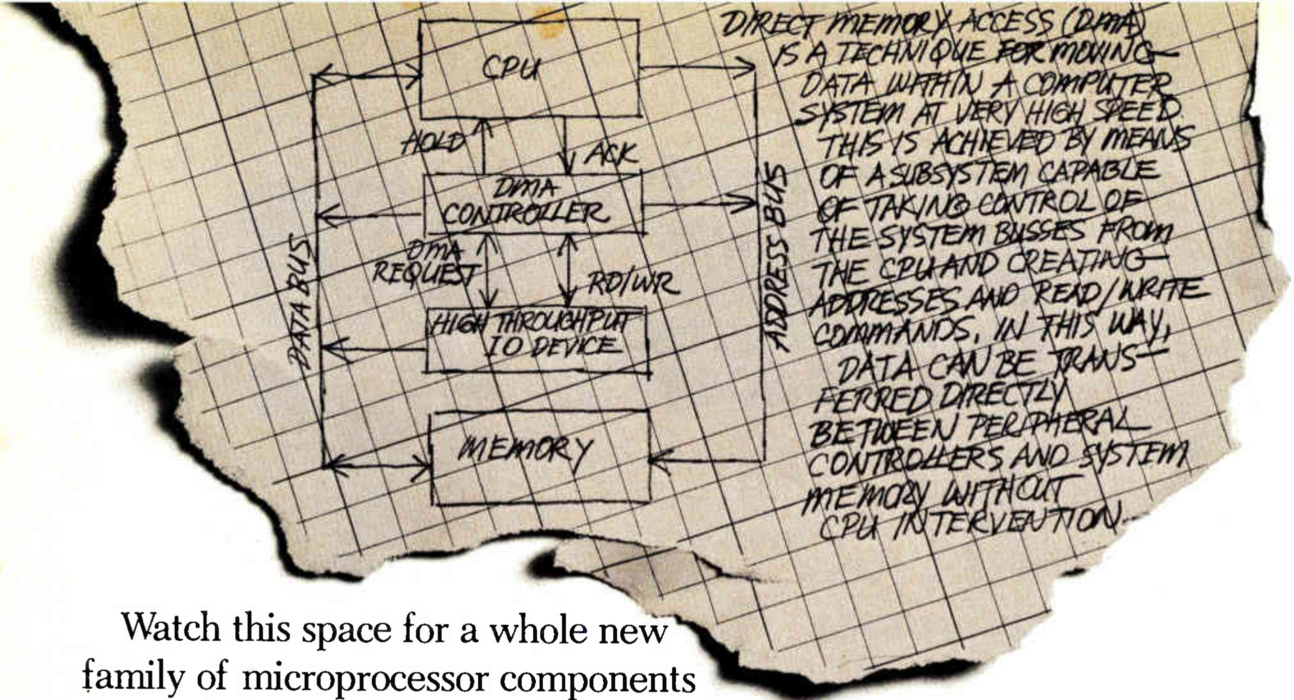

Watch this space for a whole new family of microprocessor components designed by Advanced Micro Devices.

They're built from your side of the board. They're microprocessor-based solutions from a system viewpoint.

For example:

DMA WITH EVERYTHING ON IT.

Advanced Micro Devices' new Am9517. It's a multimode DMA controller that lets you transfer information directly

MOS MICROPROCESSING: WE'RE ON YOUR SIDE.

How 36 trigger points can simplify analysis of your microprocessor-based systems.

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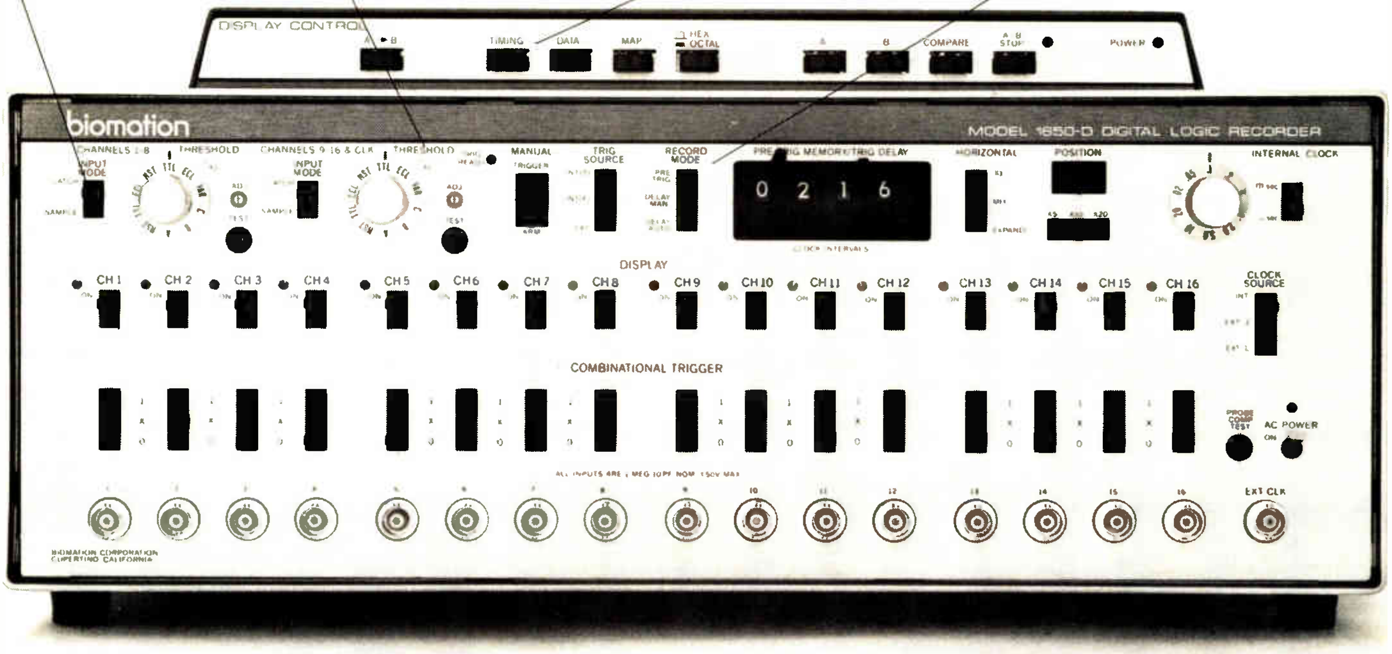
Mixed Logic Thresholds. Select one threshold voltage for channels 1-8, another for 9-16. Dial in ECL, TTL, MST, any of three user-preset values or continuously variable level.

Display Control. Select timing diagram, data domain logic state display or map mode dot pattern of system operation, using the accessory 116 Display Control. Memory feature permits comparison of current and stored system characteristics.

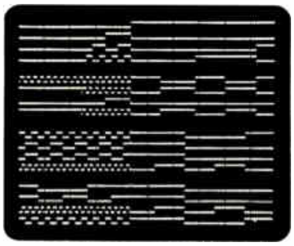
Precise Memory Control. Pretrigger recording enables you to split the 512-word memory to capture data on both sides of the trigger event. Or, with Delay Mode, start of recording can be delayed as long as 9999 clock intervals after the trigger.



Designing a microprocessor-based system? There's no better way to get a precise, detailed look at both 8-bit and 16-bit microprocessor system operation than our 16-channel, 50 MHz logic analyzer.

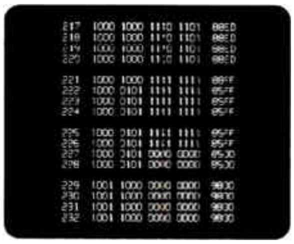
Plug in two of our 10-TC active probe pods and the 1650-D's combinational trigger capability is expanded to trigger on words up to 36 bits long. That gives you the power to record and analyze up to 16 digital signals triggering from up to 20 additional locations. Now, with the 1650-D, you can trigger on word lengths that you just couldn't detect before.

Versatility is the key to the 1650-D's popularity with designers working on microprocessor system development, instrumentation interfacing or analysis of real-time digital circuits. With the 116 Display Control, the 1650-D gives you the capability to analyze both timing and logic state displays. That's the key to simplified hardware/software debugging and integration.



Time Domain. Timing diagram lets you see the sequential and simultaneous relationship between digital signals, to simplify hardware troubleshooting.

A Latch Mode on the input signal enables the 1650-D to detect and record glitches or pulses as narrow as 5ns — vital information when trouble-shooting the operation of digital circuits. Or, for data analysis, Sample Mode ignores synchronous glitches not coincident with the data clock.



Data Domain. Display logic states (1's and 0's) with hex or octal translation. That's essential information for troubleshooting software and firmware.

There's not space here to give you all the details on how our 1650-D, with 10-TC probe pods and 36-bit trigger, can simplify your task. But we'll gladly send you detailed information on the 1650-D and our entire line of logic analyzers, from the budget-priced 920-D to the ultra-fast, 200 MHz 8200. And, at your convenience, we'll arrange a demonstration of Biomation's logic analyzers in your lab, capturing and displaying the data you work with.

Map Mode. Each digital word can be translated into a singularly positioned dot in this graphic representation of recorded data. Especially useful for spotting illogical or illegal memory addresses.

Write, call or use the reader service card. Biomation, 10411 Bubb Road, Cupertino, CA 95014. (408) 255-9500. TWX: 910-338-0226.

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Circle 13 for information

Precision quad op amps. *Precision.*

PMI's new OP-09 and OP-11 are pin-compatible with the un-precision quads now on the market.

The quad op amp has finally come of age. With the introduction of the OP-09 and OP-11, PMI has made it a truly workable reality. Consider:

Low V_{OS} and other goodies.

Since quads can't be nulled—there aren't enough pins available—the user is at the mercy of whatever input offset voltage (V_{OS}) he happens to get. PMI refined the manufacturing process to get V_{OS} under control. We came up with the lowest V_{OS} of any quad op amp made today.

At the same time, we gave the OP-09 and OP-11 the highest gain and the lowest drift of any quad op amp. We expanded bandwidth, reduced offset and supply current, and increased the slew rate. Here it is in black and white:

OP-09/OP-11 Features

	TYP.	MIN./MAX.
• Low V_{OS}	0.30 mV	0.5 mV MAX.
• Low offset current	8.0 nA	20 nA MAX.
• Low supply current (Total for all 4)	3.5 mA	6 mA MAX.
• Voltage gain	250K	100K MIN.
• Slew rate	1.0 V/µS	0.7 V/µS MIN.
• Matched positive and negative slew rate for low distortion.		
• Bandwidth		2.0 MHz MIN.

We make them match.

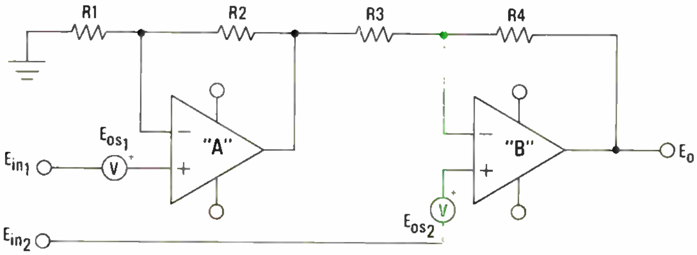
Another important advantage: we guarantee that all four op amps will match in terms of V_{OS} and CMRR. Here's how we specify them:

Matching Characteristics

		OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage Match	ΔV_{OS}	–	0.5	0.75	–	0.8	2.0	mV
Common Mode Rejection	ΔCMRR	–	1.0	20	–	1.0	20	µV/V
Ratio Match		94	120	–	94	120	–	dB

(Match exists between all four amplifiers)

DUAL INSTRUMENTATION AMPLIFIER 2 OP AMP DESIGN
(1/2 CIRCUIT SHOWN)



These matching dc characteristics should interest you. They reduce distortion, improve system performance, and simplify your design. But that's not all.

We've given all four op amps symmetrical positive and negative slew rates—an important thing to keep in mind for audio system design.

It's fair to say that the OP-09 and OP-11 are the most accurate, most advanced and the only precision quad op amps on the market. And they are on the market—available now, today.

Like to check one out? Be our guest. Just drop us a line on your company's stationery, telling us if you'd prefer an OP-09 (4136 pinout) or an OP-11 (148/4741 pinout). We'll be glad to send literature and a sample.

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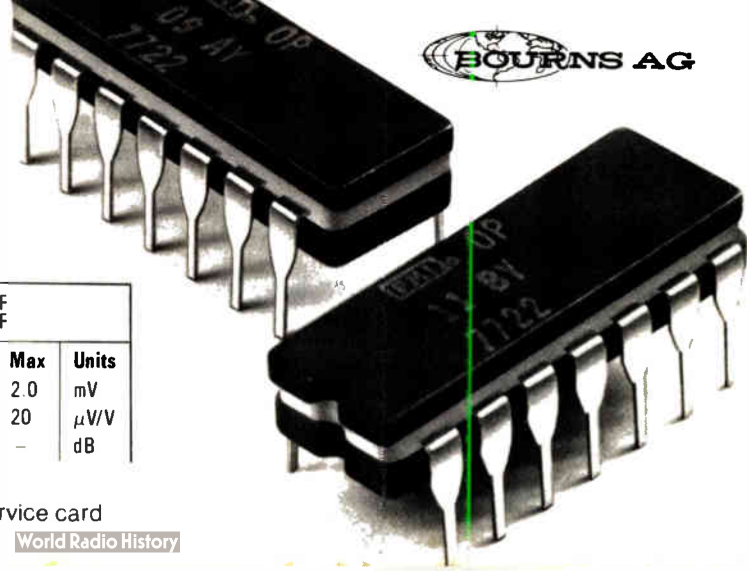

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Associates Inc., Gloucester, Mass.

The division has a license to use Bell Labs' electron-beam exposure technology, has sold at least one production machine to make masks, and is building two more. And Extrion engineers are hard at work on direct wafer exposure. The division is also the leading producer of ion-implantation equipment for semiconductor processing.

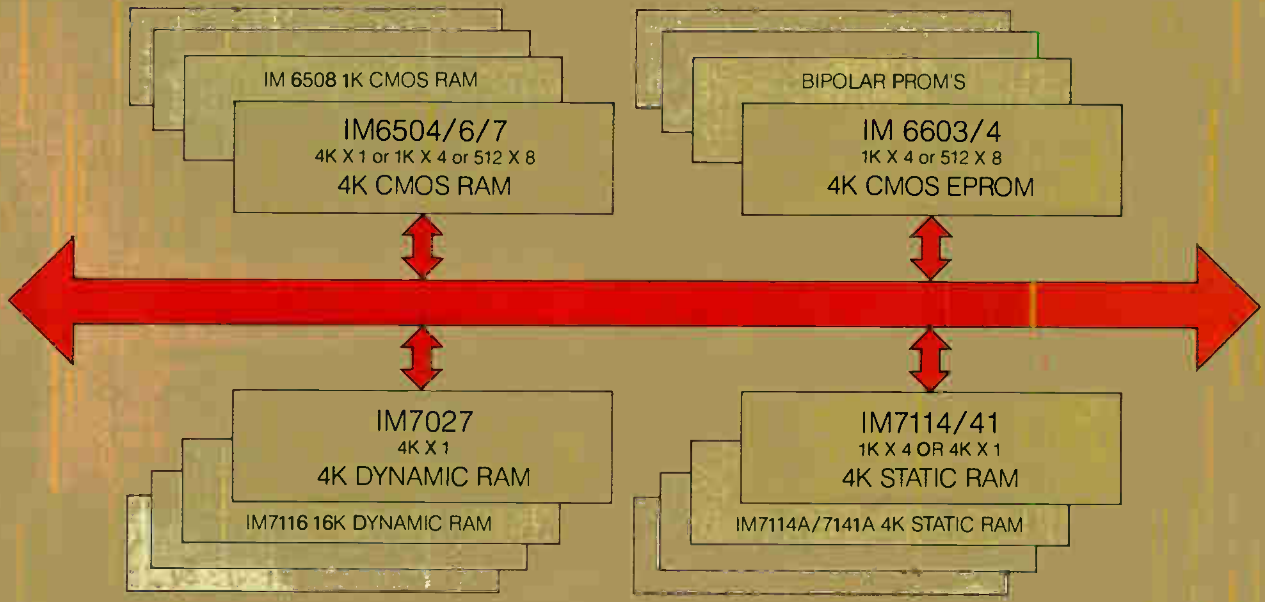
Large potential. Bottoms sees the worldwide market for electron-beam mask makers as somewhere between 40 and 50 machines. But production equipment that directly exposes the wafer, eliminating the mask step, "could make the market a factor of 10 larger than that," he says. He points to three main areas for improvements before that second generation dawns three to five years hence: finer etching, level-to-level pattern registration on the wafer, and the need for faster and less expensive machines than today's $1.5 million systems.

For future etching, he says, "we'll have to be able to define patterns in conductors and insulation materials that are higher than the pattern features are wide," and that is no small task. He thinks there could be two approaches to accurate level-to-level registration, a problem when distortion occurs as the wafer is heated during processing. "One way might be to use the electron beam to define the pattern on one level, then also use it to re-register with the pattern level beneath," adding that the beam itself can measure any distortion and adjust for it.

But he seems more intrigued with the potential for eliminating high-temperature wafer processing. "That means getting rid of thermally grown oxides, so that we heat the wafer only once," he says. "Conceivably, we could eliminate diffusions and substitute ion implantation." Bottoms is also confident that the throughput of Extrion's current EBMG-20 system—70 minutes to produce a mask for a 5-inch-diamenter wafer down to 20 min. for a 2-in. slice—can be boosted by an order of magnitude in a direct-writing system within five years.

in the affairs of men which, flood, lead on to fortune."

William Shakespeare, 1564-1616



4K CMOS STATIC RAM's.

Over the years, Intersil has shipped more CMOS RAM's than any other manufacturer. By mid-year, we'll be adding a new dimension to our line of 1K RAM's with a series of new 4096 bit static RAM's, including the IM6504 (4096 x 1), the IM6506 (1024 x 4), and the IM6507 (512 x 8). Offering power benefits typical of CMOS, plus TTL compatibility, the new IM6504 will be ideally suited to memory systems requiring low power, non-volatility and high performance.

4K DYNAMIC RAM's.

The IM7027/MK4027 dynamic RAM is a second generation dynamic RAM that offers you substantial improvement in page mode, read/write timing and speeds up to 120ns access and 250ns cycle time. It's specifically designed for EDP, computer mainframe memory, microprocessor and microcomputer applications. Speed and power, coupled to a lower power dissipation, mean lower overall costs. Pin compatible with the slower speed, higher power RAM's you've been using.

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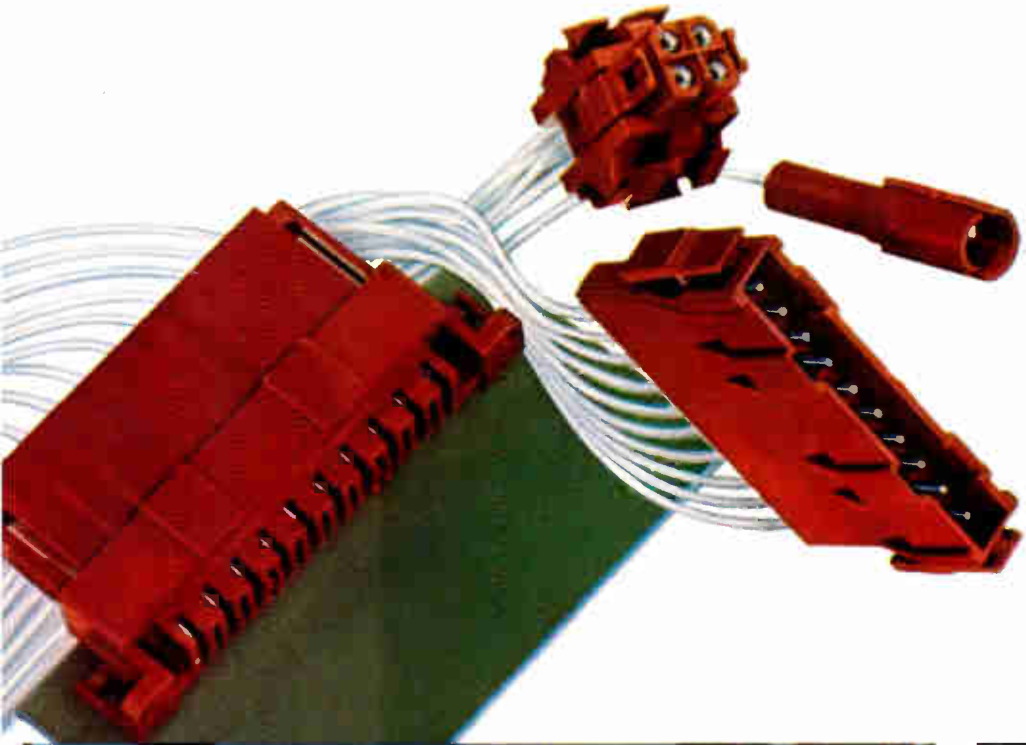

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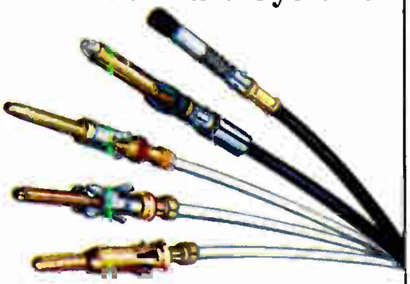

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How the Federal budget skimps on research

The Carter Administration's first attempt to put together an annual Federal budget looks, on the surface at least, like good news for many segments of the electronics industries. For one thing, total spending proposed for fiscal 1979 would rise by a hefty 8% to $500 billion. For another thing, proposed defense spending would jump 9.4% to a peacetime record of $115 billion.

Even more important, though, in terms of long-term effects are the Carter proposals to up Federal research and development expenditures by 8.5% to some $27 billion. Most of the rise is earmarked for particular programs, about half of them military, yet the rise is significant in that it continues an upward trend in research and development, an area that in the Nixon-Ford years was not given the level of support it had enjoyed in previous Administrations. Indeed, some university researchers are now calling the eight years from 1968 to 1976 the Dark Ages for academic research.

Another significant trend is the growth in basic research reflected by the budget figures. Actual outlays in fiscal 1979 are expected to total nearly $3.5 billion, a jump of 10% from 1978's spending projections. And, when compared with 1977's actual expenditures, the growth rate would come to nearly 25% for the two years.

Yet underneath these figures is a picture that is a bit less rosy. For example, while spending on basic research is due to rise 10% in 1979, the rise from 1977 to 1978 was more than 13%. Thus, this year's proposed rise represents a slackening of the pace. Indeed, even the dollar increment is less: a $367 million rise from 1977 to 1978 vs a $319 million rise slated for fiscal 1979.

What's more, the growth in basic research funding for defense will be a solid 14%, compared with a growth of only 2.4% for civilian-related research and development. Space projects, the third major Federal R&D category, will have an 8.8% growth.

It has long been said that basic research is an essential investment in the future. To a nation that has reached the forefront of international power and prestige on the basis of its technological prowess, R&D spending is the key to staying ahead of the competition. It is estimated that some two thirds of all basic research is funded by the Federal government, because private-sector organizations do not have the resources or cannot risk the uncertainty of payoff. While the resumption of an upward trend in Federal research and development support is to be welcomed, the pace is still too leisurely if the United States a decade or two from now is to be as powerful and influential as it could be.

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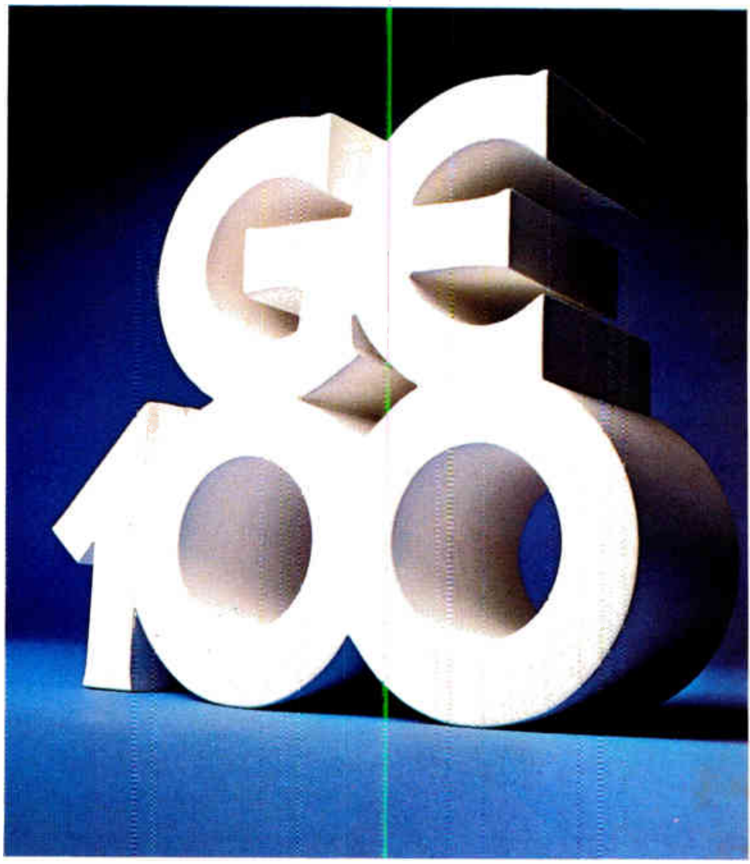

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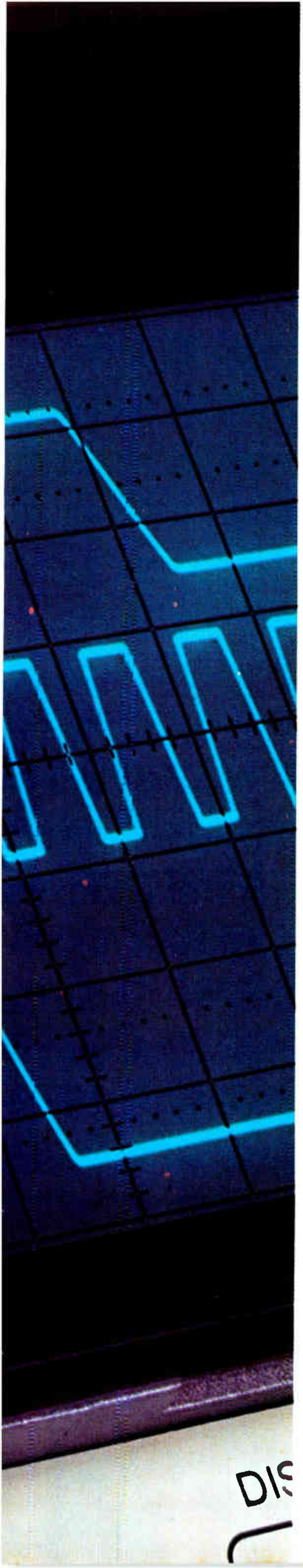

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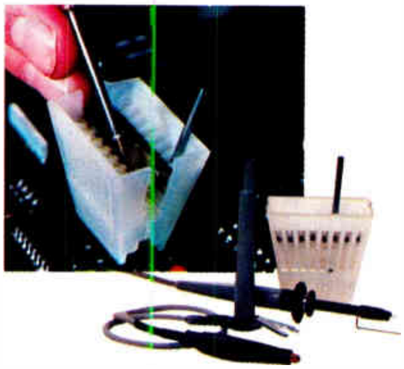

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Mostek does it again! Mostek's 3870 single-chip microcomputer has led the industry in capability and performance for over a year. Now Mostek introduces another industry standard with double the 3870's ROM and RAM. Called the MK 3872, it is second in a growing family of single-chip microcomputer products from Mostek.

*The 3872 features include 4032 x 8 bytes of mask programmable ROM; 64 bytes of scratchpad RAM and an additional 64 bytes of executable RAM. Supporting the executable RAM is a stand-by power mode for easy battery backup.

These characteristics enable the 3872 to control sophisticated mechanical devices and instruments. Or the 3872 may be used to combine several programs into one system, thereby lowering manufacturing costs. In applications that require non-volatile data storage, the stand-by power mode makes expensive CMOS memories unnecessary. No extra components are required to trickle charge standby batteries.

Family design means system compatibility. When designing a microcomputer system, engineering time is one of your largest investments. The 3870 family design concept protects that investment by allowing system expandability while maintaining hardware and software compatibility.

You can start with the 3870's 2K of ROM and upgrade to the 3872's 4K of ROM. Or begin with 4K and then substitute 2K for lower cost applications. This versatility, while retaining a common system base, means new applications with faster development and lower costs.

When Mostek engineers expanded the 3870, they retained all of its important features. Like 32 bits (4 ports) of bi-directional I/O; a programmable binary timer; external interrupt; low power (285 mW typ.); and single +5 volt ± 10% power supply. Pinouts, of course, are unchanged. The best simply got better.

Coming in '78. The Mostek 3870 family will continue to grow, giving you the flexibility and expandability required for new applications. The 3873 Serial I/O version will interface to serial devices such as shift registers and CCD memories, and allow implementation of an asynchronous serial I/O port making low cost multi-processing applications practical. The 3876 version will have the same ROM as the 3870 but with double the 3870's RAM, plus a standby power mode.

Complete Development Support. A full array of development aids is available from Mostek. This includes hardware/software support, complete documentation, field application engineers and 3870 microcomputer workshops.

The Mostek 3870 family. A total system with total support. From the source, Mostek. For more information, contact Mostek; 1215 West Crosby Road; Carrollton, Texas 75006. Telephone: (214) 242-0444. In Europe, contact Mostek GmbH, West Germany. Telephone: (0711) 701096.

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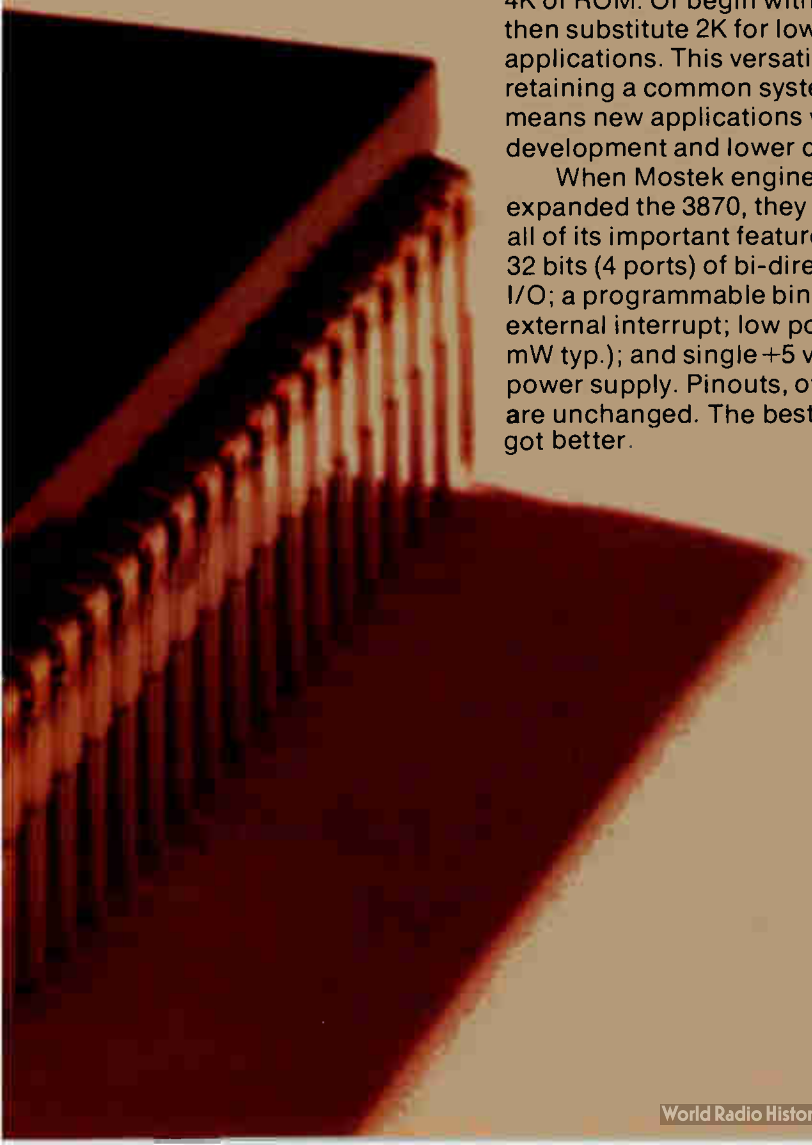

Circle 31 on reader service card

Japanese firms aim for 1979 with 65-k RAM designs . . .

Work on commercially feasible designs for 65,536-bit dynamic random-access-memory chips is well under way in Japan, even though few observers have been impressed by the designs made public so far—notably the 2-μm-geometry, single-level, oversized chip developed under the auspices of Nippon Telegraph and Telephone Public Corp. For example, Nippon Electric Co. **is in the advanced stages of a two-level polysilicon 65-k design that measures about 28 mm^2,** not much more than the 40,000-mil^2 chip size that manufacturers like to work with for high-volume production. (U. S. manufacturers are aiming at a 30,000-mil^2 chip.) The NEC double-polysilicon design, which is tentatively scheduled for introduction in 1979, will come in a 65-k-by-1-bit version in a 16-pin package and a 16,384-by-4-bit model in a 22-pin package.

Other 65-k RAM programs are well along at Hitachi and Fujitsu as well. Like NEC, both of these manufacturers are working with conventional double-polysilicon designs for first cuts, aiming at 16-pin packages on die sizes comparable to present 16-k parts.

. . . as NTT develops 65-ns 16-k RAM

Meanwhile, Nippon Telegraph and Telephone Public Corp. has developed an experimental 16-k dynamic RAM with typical access times of 65 nanoseconds, twice as fast as today's fastest parts. Though not listed in the advance program, the device will be described at the International Solid State Circuits Conference in San Francisco, Feb. 15–17. Its molybdenum-gate structure boosts speed by allowing the fabrication of 2-μm-wide MOS channels having a lower resistance that reduces the memory cell's time constant. NTT **designers see the work as providing experience for building 65-k and larger molybdenum-gate memories** with significantly increased speeds. Such gates also increase the probability of single 5-v power-supply operation, although the device now uses +7 and −2 v.

Optical analyzer on chip built by Rockwell team

A pair of Rockwell International researchers will report later this month that they have fabricated **a single silicon substrate holding all components except the laser light source for a thin-film optical spectrum analyzer.** Dean B. Anderson and Rudy R. August will describe their work Feb. 8 at the biennial Conference on Laser and Electro-Optical Systems in San Diego. "We believe ours to be the first integrated operation of these components, which have been demonstrated for use in a broadband rf spectrum analyzer separately, but not together," they claim. With data garnered from fabricating and operating the components on a 4-inch silicon slice, Rockwell will go after an integrated optic project to be funded by the Air Force [*Electronics*, Dec. 22, 1977, p. 29].

New product line of big LCDs due from Beckman

Now that the boom in liquid-crystal-display watches has settled somewhat, the largest noncaptive producer of the displays in the U. S. is mapping a market assault with a new line of large-area LCDs aimed at other than wristwatch uses. The producer is the Helipot division of Beckman Instruments Inc. **"We're coming out of the starting gate running with half-inch-digit LCDs,"** says Philip R. Strauss, division marketing manager. Prototypes will go to customers this month, and volume production will start in April. The big displays will sell for about $6 in quantity, compared to $2 for Helipot's largest watch display, an 0.18-in. model.

GI to shift to silicon gate for 65-k ROM

In effect conceding that its traditional n-channel metal-gate technology isn't suited for building very dense read-only memories, General Instrument Corp.'s Microelectronics group in Hicksville, N. Y., is shifting to a **new silicon-gate process to fabricate its first 65,536-bit ROM** due out later this year. To be designated the RO-3-9365C, it will use very tight design rules and single-layer processing to hit targets of 350-ns maximum access time and about 40,000 mil^2 in chip area.

Prime fills line of medium machines with model 350

Moving to flesh out its medium-scale minicomputer line, Prime Computer Inc. on Feb. 13 will take the wraps off the Prime 350—a system that will fit in price and performance between the Wellesley, Mass., company's Prime 300 and 400. Prices for the 350 will range from about $100,000 to $150,000. The system's chief innovation **is its ability to run the Primos IV operating system, previously possible only with the 400.** Prime officials expect the 350 to compete with Digital Equipment Corp.'s PDP-11/60 and 11/70, and with Hewlett-Packard Co.'s HP 3000, model 2.

Feerst running for IEEE president, talks of new group

It must be February. Irwin Feerst, perennial candidate for president of the Institute of Electrical and Electronics Engineers, once again has petitions out to get on the ballot for the 1978 presidential election. He's also making plans to organize **a new association of EEs that would take on some of the professional-career tasks** he and his followers believe IEEE is not going to perform. The IEEE board will name its candidates Feb. 19 and 20.

National samples CRT controller for terminal market

Add National Semiconductor Corp. to the list of companies—Fairchild, Intel, Motorola, and Standard Microsystems Corp.—aiming to supply cathode-ray-tube controllers to the growing terminal market. But the Santa Clara, Calif., company says that the DP8350 it's now supplying in sample quantities in the U. S. and Europe is unique among its competitors **in having an internal crystal-controlled dot-rate oscillator and an on-chip dot-logic section for character formatting.** That much internal logic lets a designer of a low-end terminal reduce his part count from 40 or more ICs to only 15 to 20 devices, including the microprocessor, keyboard interface, and memory, National claims.

Addenda

Sanyo Electric Co. and Fairchild Camera and Instrument Corp. have made a cross-licensing deal involving Sanyo's **molybdenum-gate nonvolatile memories and Fairchild's F8 products.** . . . Documation Inc., the fast-growing supplier of computer peripherals including high-speed printers [*Electronics*, Jan. 5, p. 14], has introduced its fastest impact line printer yet. **Called the DOC 3000, it runs at 3,000 lines a minute.** . . . Texas Instruments is rushing to market with a 32,768-bit erasable programable ROM, with samples coming this month and volume production due in April or May. **It will operate from a single 5-V supply**—like Intel's 16-k device—but apparently will not be compatible with the 32-k version that Intel is developing. . . . After using its H-MOS technology to get high-speed performance out of its 2147 family of 4,096-bit static random-access memories, Intel Corp. is turning the technology to low-power static RAMs. It's about to announce a 2141 family that it claims has the best speed-power products of any RAMs to date.

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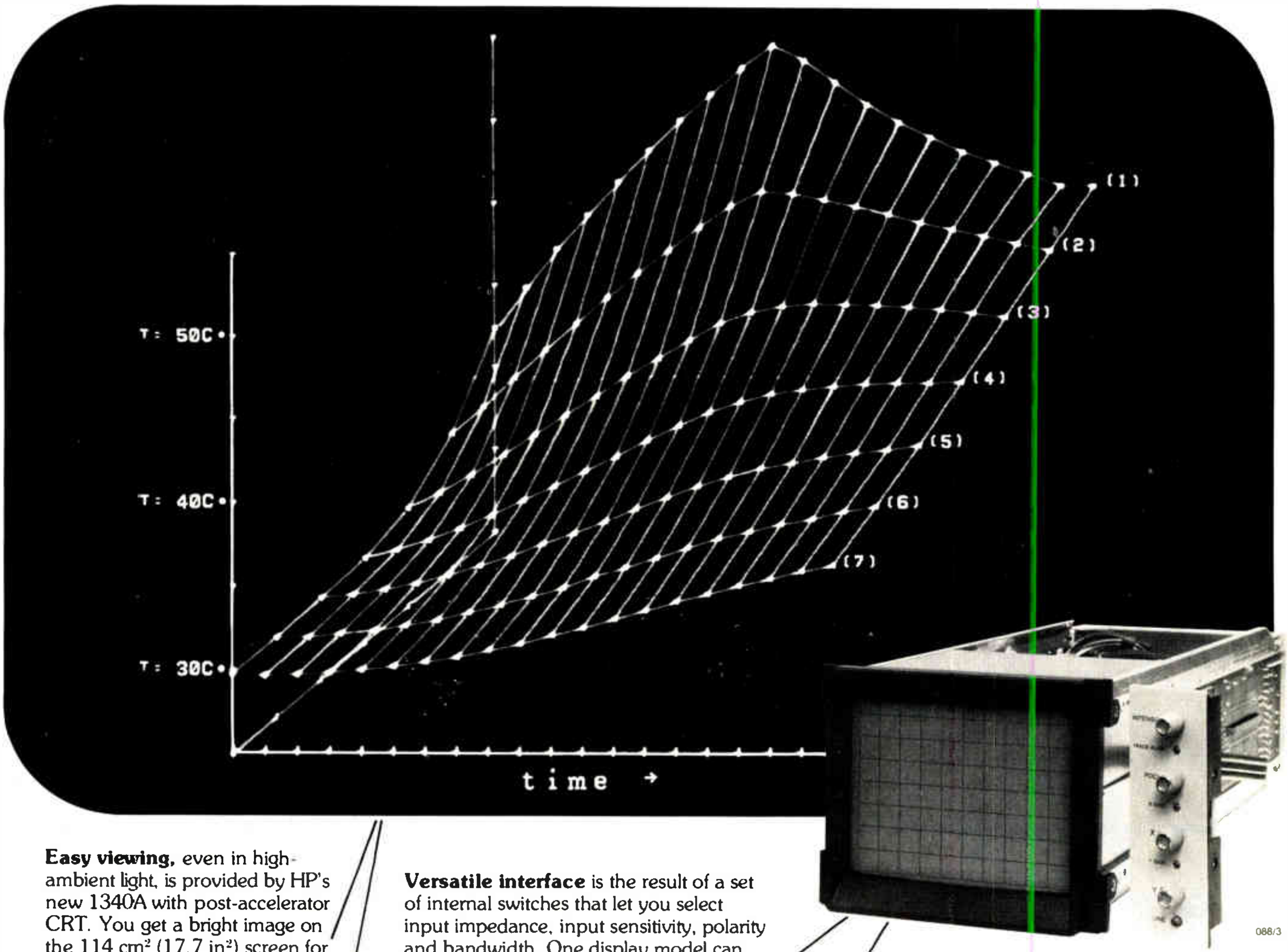
It's easy to design in... it gives you a good system image.



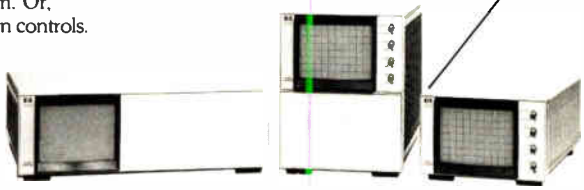
Easy viewing, even in high-ambient light, is provided by HP's new 1340A with post-accelerator CRT. You get a bright image on the 114 cm^2 (17.7 in^2) screen for easy evaluation of intricate presentations.

Versatile interface is the result of a set of internal switches that let you select input impedance, input sensitivity, polarity and bandwidth. One display model can be used with a variety of different instruments and systems.

Crisp displays of complex graphics and alphanumeric data is assured by a 0.46mm (0.18 in.) spot that focuses uniformly over the entire viewing area, regardless of intensity level.

Flexible location of controls is possible with the 1340A's separate control panel. You can locate intensity, focus, gain and trace-alignment controls to suit your particular system. Or, with Option 001 you can use your own controls.

Easy system integration is the result of the 1340A's packaging flexibility. Open frame, desk top, vertical stack and rack mount versions easily adapt to nearly any system configuration.



HP's new 1340A is a true OEM display component. And to accommodate most OEM requirements, options such as different phosphors and TTL blanking as well as a choice of packaging schemes are available. For only $1,000*, you get a cost-effective display that easily adapts to almost any instrumentation system.

So for a better image of your system's performance, look into HP's new OEM display. For further details, ask your local HP field engineer.

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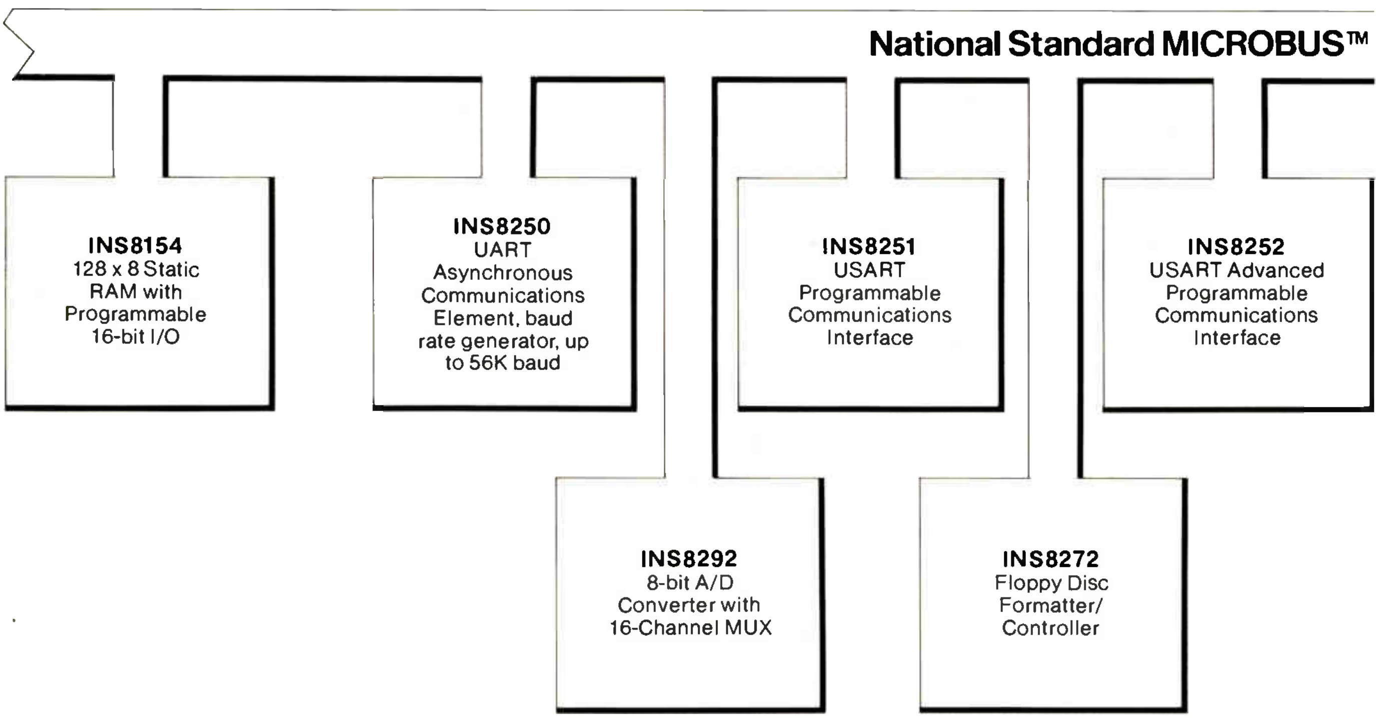

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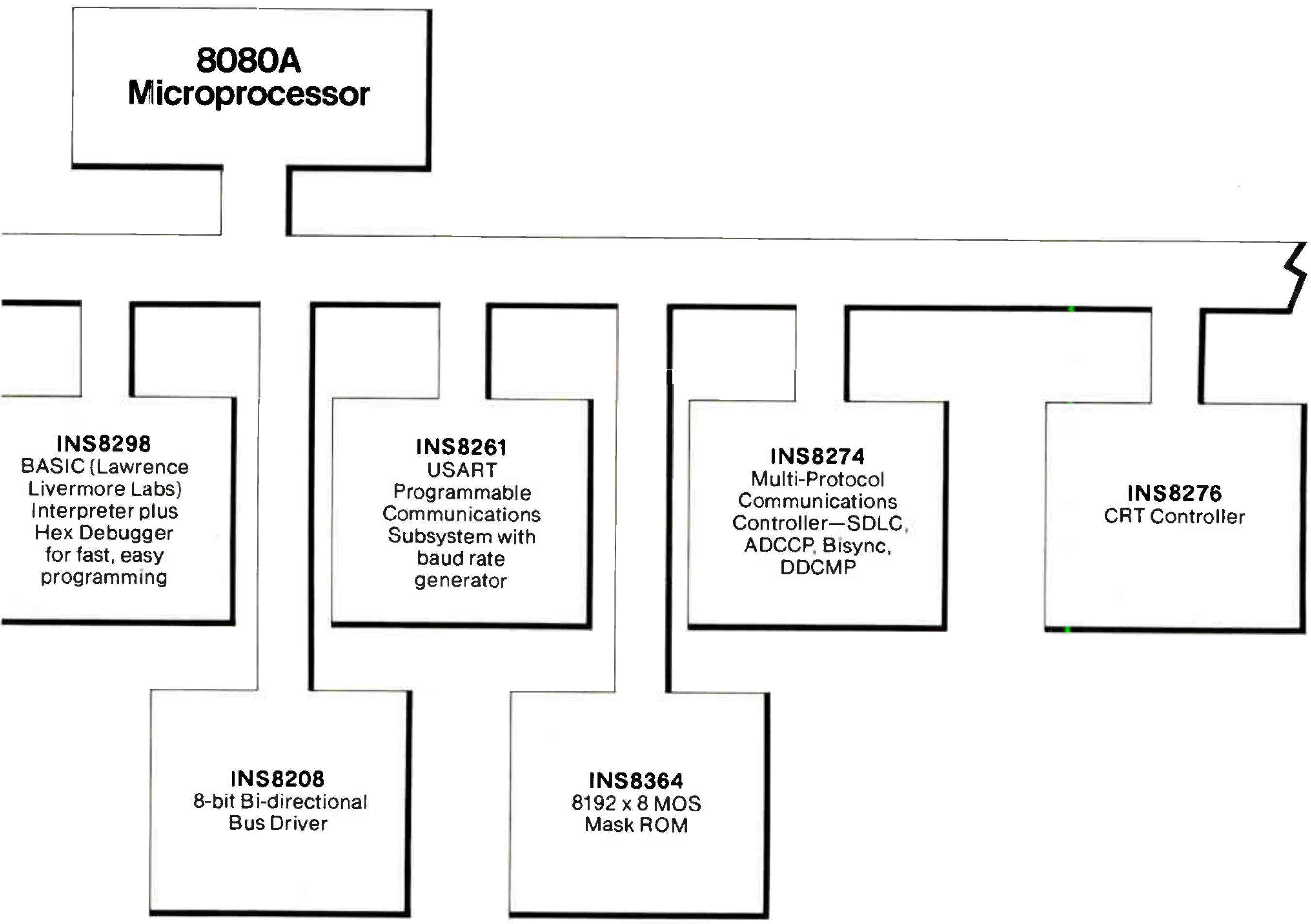


Report blasts lack of standards for Federal computer installations

Conversion costs, now $450 million yearly, tie users to old suppliers and dampen competition for new gear

The nation's largest computer customer is in big trouble that threatens to become worse. Because of its failure to develop hardware and software standards for its own use, the Federal government is wasting a sizable chunk of its $10 billion annual budget for computer equipment and personnel, charges the General Accounting Office in a 94-page draft of a report that has not yet been published.

In the course of an investigation it made for Congress, the GAO discovered that many Federal agencies seeking to replace or upgrade computer systems find themselves locked in with their original suppliers because of the soaring cost of converting programs to a different manufacturer's hardware. Among other agencies, conversion costs are already running to $450 million a year, says the draft report. The Department of Commerce, and more specifically its National Bureau of Standards, are blasted for having failed to develop and enforce Government-wide standards for compatibility between peripherals and mainframes and among software programs, despite a congressional mandate that was first delivered 13 years ago.

Worse still, in the continued absence of standards, competitive procurements "may eventually become impossible to justify," contends the GAO. Headed by Comptroller General Elmer Staats, the General Accounting Office is the investigative arm of Congress. Sources familiar with its draft report say that document is now being "negotiated" with the executive branch and suspect it could be watered down before delivery to Congress in March or April. But the Commerce Department's initial reaction is being read by industry and congressional officials as an attempt to short-circuit the criticism by moving to triple its requested fiscal 1979 expenditures for the NBS standards program (see "Will new funds for standards help?").

To spur the development of standards and ensure they are followed, the GAO urges that "the President, through an executive order, clearly designate the Secretary of Commerce as the central authority for insuring compliance with Government-wide automatic-data-processing standards, including the authority to disapprove requests for

Will new funds for standards help?

When President Carter's fiscal 1979 budget was delivered to Congress near January's end, the 300% increase for a single Commerce Department program went largely unnoticed. Elsa A. Porter, assistant secretary for administration, casually described it as "an increase of $13.4 million, for a total of $17.9 million to develop standards and procedures for Federal automatic data-processing installations." The program, she says, "is needed to fully implement the Brooks Act [of 1965] by improving computer economy and effectiveness."

Is the Commerce Department running scared before the upcoming GAO report to Congress? If not, why did it wait 13 years since the passage of the standards legislation before really getting busy here? One department source familiar with the GAO effort could only answer the question with another: "It [the additional money] does seem a bit coincidental, doesn't it?"

Industry sources call the sudden program increase "overkill" and question whether the National Bureau of Standards will carry out the mandate from the Commerce Department, even with the new money. "That program never should have been in Commerce in the first place," one declares. "It should be in the General Services Administration's Automated Data and Telecommunications Service." The GSA is responsible for procuring all general-purpose computers for the Federal government.

The GAO report tends to support criticism that the standards bureau may not spend its increased funds, if appropriated, on the standards program. The NBS Institute for Computer Science and Technology is responsible for the standards effort. The GAO challenges institute claims that Federal data-processing standards are "its highest-priority work, and over 75% of the institute's $4.1 million appropriation supports standards development." The GAO investigation shows "that only about 38% of the appropriated funds, or 23% of the combined appropriated and reimbursed funds [from other Federal customers], are devoted directly to standards development," despite the Brooks Act's mandate.

is aimed at a data-services market in which a typical system serves the small to medium-sized tasks of 20 to 50 users, it is in I/O that the new machine must shine, he says. Relying on the advanced operating system announced previously by Data General, the M/600 will accommodate up to 64 users.

Not a limit. Scanlon stresses that the M/600's performance "in no way approaches the upper limit of 16-bit architecture." He sees plenty of room for improvement even without going either to logic faster than the low-power Schottky transistor-transistor logic used throughout the M/600 or to bigger random-access memories than the 4-kilobit RAMS employed in the 1-megabyte main memory. If users choose, they can have 512 kilobytes of core main memory instead of semiconductor storage.

The M/600's I/O management system is divided into three parts so that the machine may interface with peripherals of varying speeds and to take as much load as possible off the central processor. Otherwise, users could really bog down a system of this class, says Frank Madren, the firm's manager of product market programs. Accordingly, there is a burst multiplexer channel for handling very-high-speed peripherals, a standard data channel, and an independent I/O processor for low-speed peripherals.

"The BMC [burst multiplexer channel] provides a direct communications pathway between main memory and high-performing peripherals like disks at aggregated rates of up to 10 megabytes per second," Madren points out. This is faster than some mainframes, such as the IBM 370/148, and most 32-bit machines. Thus, the two-circuit-board BMC frees the central processing unit, called the job processor by Data General, to operate on data. The M/600 will accommodate eight disk subsystems in any mix of varieties, resulting in total on-line storage of up to 6 billion bytes.

Other uses. The standard data channel has been used in other Data General machines, providing relatively simple interfaces and controllers for communications between the job processor and medium-speed peripherals, such as magnetic-tape and cartridge-disk drives. It also serves as a high-speed interface, handling up to 2.5 megabytes per second, between the job processor and the I/O processor, for low-speed peripherals.

Host. Eclipse M/600 system could play host in a distributor's inventory management net. Price of $325,000 includes computer, 512 kilobytes of main storage, tape and disk drives, display and printer consoles, and 48 local and remote time-sharing terminals.

That processor is a dedicated front-end unit that is essentially a smaller Eclipse system with 64 kilobytes of memory. In a system of the M/600's class, Madren says, there will be substantial keyboard character input and output from slow terminals like cathode-ray-tube displays and printers and from asynchronous communications devices. The I/O processor will process these a line at a time or more, a full CRT

How the M/600 stacks up

Some of the key indicators of the M/600's performance, in the opinion of Data General's product marketing manager, John Scanlon, include certain typical instruction-execution times. In scientific applications, the system will perform 64-bit double-precision floating-point register arithmetic with times for additions, multiplications, and divisions of 1.0, 2.6, and 6.8 microseconds, respectively. Published numbers for Digital Equipment Corp.'s VAX-11/780 for the same instructions are 1.4, 3.4, and 8.0 μs, respectively. For the Interdata 8/32 the corresponding speeds are 1.04, 2.5, and 6.7 μs. The DEC and Interdata machines are both 32-bit computers.

Frederic "Ted" Withington, senior staff member and computer industry authority at Arthur D. Little Inc., says such performance gives the M/600 "the horsepower to compete for central data-processing applications at prices lower than some mainframes." M/600 prices will range from about $160,000 to $325,000. But Withington wonders how Data General will attract such users away from present suppliers, especially IBM.

screen at a time, or an entire record field at a time, instead of "clogging the CPU with interrupts" to transfer this data in and out a character at a time, which often happens in other systems, he says. □

Instrumentation

New testers measure low-level parameters, calculate process trends in wafer production

The mounting need to increase yields on complex parts by improving wafer fabrication is opening up a promising market for a new kind of wafer tester. This is a microcomputer-based tester that checks the electrical properties of special test devices integrated on the wafer at the same time as the actual circuits.

Such devices, which include resistors, field-effect and bipolar transistors, and diodes, have been incorporated on wafers previously. But they have been probed either manually, with time-consuming measurements of their parameters taken one at a time, or by the same expensive semiconductor testers, such as the Fairchild Sentry, as test the production circuits. Parameters such as gate leakage or the capacitance of a field-effect transistor can give valuable information on how a wafer has been processed. The new testers measure and keep track of these parameters, and they do it automatically—for a price well below the $250,000-and-up cost of the big automatic testers.

Competitors. Two companies have so far brought testers to this area. One is Lomac Corp., Santa Clara, Calif., a company formed five years ago to produce this equipment. The other is Keithley Instruments Inc., Cleveland, Ohio, which is capitalizing on its expertise in making sensitive equipment for measuring low-level voltages and currents. Until recently, not much money was available for such testers. But now, low yields on complex parts are changing company minds.

At the end of January, Lomac introduced its LM-80 wafer tester built around a Zilog Z80 microprocessor. Looking more like a word processor for an office, the LM-80 costs $50,224, versus about $75,000 for the minicomputer-based LM-228A tester that the company introduced last year.

Keithley calls its equipment the System 2/LPT (for linear parametric tester). Built around a Digital Equipment Corp. PDP-11/03, it costs $39,900 and was introduced at the Wescon show last September. So far, sales of both companies have been modest, with only several units sold by each. But, perhaps not surprisingly, both companies believe they are turning the sales corner.

"New, more complex LSI is putting increased demand on precise wafer processing and knowing to the best possible extent what is going on," says John S. Howard, manager of systems marketing for Keithley. It is the ability of the new equipment not only to make picoampere- and millivolt-level current and voltage measurements but to convert them to meaningful process parameters that is so important, explains Lomac president Marshall McComas.

Trends. With the LM-30, for example, a manufacturer can automatically perform 40 to 80 tests that will show trends in threshold and breakdown voltages, plot capacitance versus voltage, and even help determine how many angstroms thick a deposition layer is. "Our machine has the information to tell where fabrication went wrong," McComas declares.

According to Willard L. Kauffman, director of component production in the Components division of Intel Corp., a purchaser of Lomac's earlier model, the 228A, "the automated equipment is more cost-effective when it comes to printing out the distributions of test parameters of various wafers." So much so, that Kauffman is ordering more.

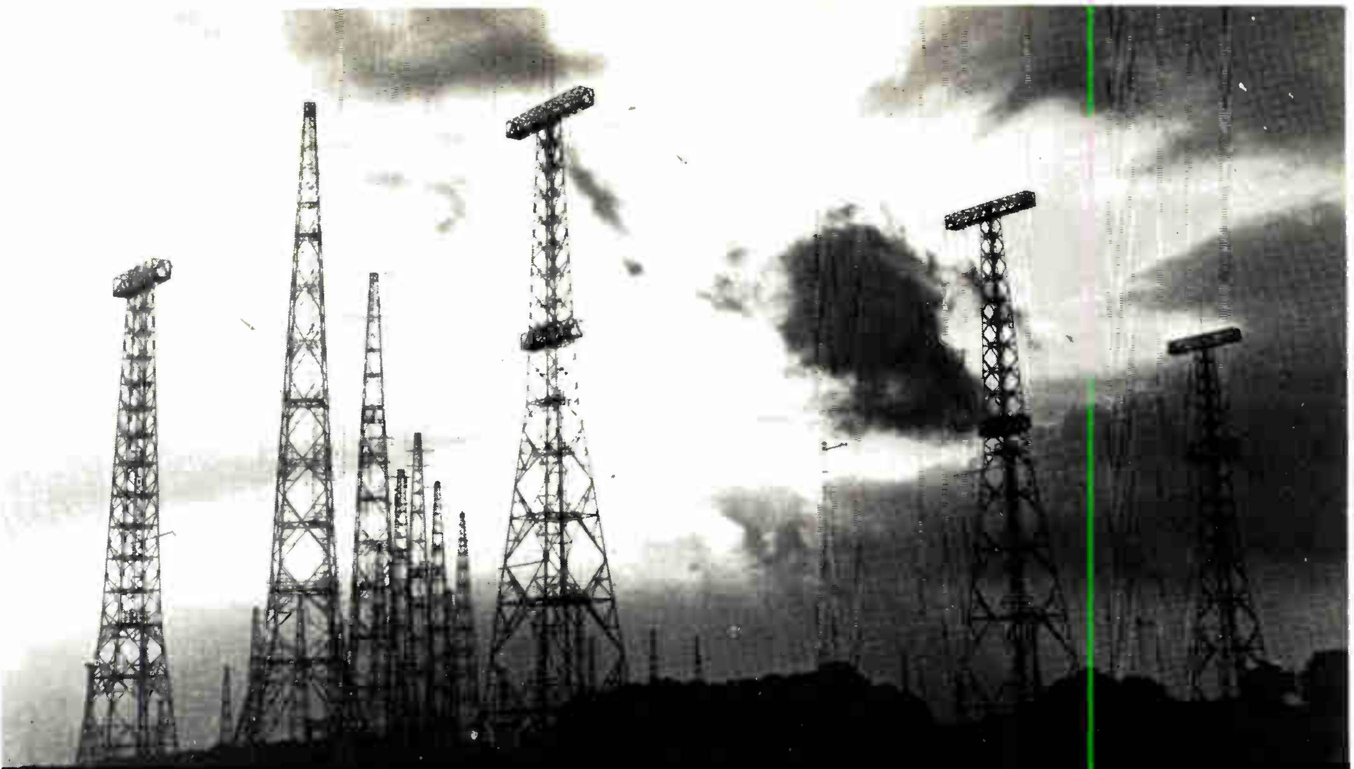
Both the Keithley and Lomac testers include a desk-like control station, video display terminal, dual floppy disks, relay matrix for handling wafer probes, and printer. They also have sensitive current- and voltage measuring units. In Keithley's case, for example, the company's model 445 digital picoammeter and the model 5900/42 5½-digit voltmeter are used, whereas Lomac designs its own measuring circuits. Software packages are available for programming the Keithley tester in Fortran, the Lomac unit in Fortran or Basic. □

Broadcasting

National has designs on a-m stereo chip

National Semiconductor Corp. has become the first semiconductor maker to publicly declare itself in the race to develop an integrated-circuit demodulator for a-m stereo radios, even though the Federal Communications Commission has yet to approve a broadcast system. National's Tim D. Isbell, manager for consumer analog development, told the FCC in a letter that the Santa Clara, Calif., company has "spent considerable engineering effort studying some of the proposed systems so that we can readily supply an a-m stereo IC demodulator at the earliest possible time." Wholesale market potential for a-m stereo equipment has been estimated at $250 million annually—80% of it in auto radios—by broadcast industry sources.

Caution. Isbell cautioned the FCC not to allow the sale of a-m stereo receivers until six months after it makes a system selection. "Without such a time restriction," Isbell wrote, "there is a high probability that poor technical compromises will result from the rush [to bring a chassis to market] and that a-m stereo will get off to a rough start—one that may require much money and a few years to overcome. By waiting six months,



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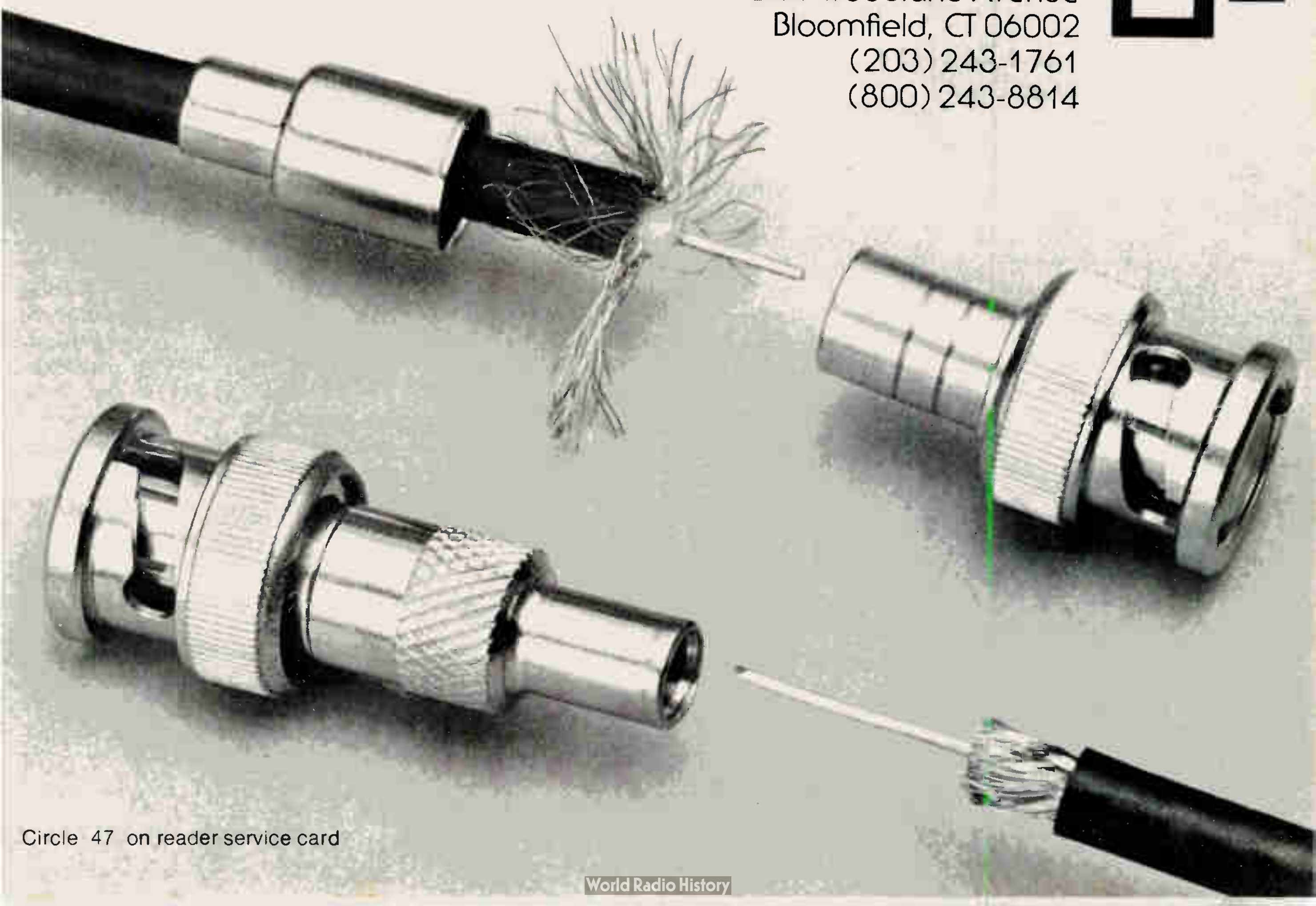

Circle 47 on reader service card

Player. Protective polystyrene permanently covers VideoDisc, shown being inserted in demonstration player. Disk material holds shape to 135°F, RCA says.

20 pounds, operate at 450 revolutions per minute, and sit easily on a table top, as shown above. Signal-to-noise ratio for the playback will be anywhere from 45 to 48 decibels, compared to 41 dB for the tape unit, Sonnenfeldt adds. □

Careers

Salary survey puts average at $27,496

Salaries of the U. S. members of the Institute of Electrical and Electronics Engineers have outpaced the rate of inflation over the last two years, reversing the trend between 1972 and 1975. According to the institute's recently released 1977 survey of members, the mean annual income of the engineers who responded was $27,496 during the 12-month period from July 1, 1976, to June 30, 1977. In 1975 the mean income was $23,544 and in 1972 it was $18,808.

Wide-ranging. However, individual salaries vary widely, ranging from $11,000 at the first percentile to $70,000 at the 99th percentile. There was a consistent increase based on engineering experience (see chart, p. 51). Mean income increased from $15,137 with under two years' experience to $34,949 for 30 years' or more experience—an average annual increase of only about 2.8%. The chart indicates that the steepest salary increases come in the early years of employment and tend to level off after 20 years. The mean salaries found in the latest survey represent a 16.8% increase over the salaries in the 1975 survey. This compares with a 15.6% increase in the Consumer Price Index during that time.

Consisting of 9,227 of the approximately 140,000 IEEE members in the U. S., the survey sample includes management and nonmanagement engineers and electrical (power generation, power production, and utilities employees) as well as electronics engineers. Although management-level engineers pulled up the averages, the salaries of power engineers did not affect them, being right at the average income level. On the other hand, office- and business-machine designers were well ahead of the average with $38,416. Engineers in communications also earned above the mean annual income, while minicomputer designers, surprisingly, earned somewhat less.

Management tops. The highest mean annual incomes went to those in engineering management ($34,628), those working with electron devices ($32,613), and those who reported that their area of primary technical competence was not in the EE field, probably members who have gone into nonengineering management or sales. The lowest mean annual salaries were for those in industrial electronics and control ($23,464), circuits and systems ($24,013), reliability ($24,708), and education ($24,887).

As for fringe benefits, over 10% of the respondents say they are not covered by a company pension plan. Of the remainder, the average

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in large volume but are rather different (see "Game-computer chip lineup"). To gain data storage, input, and communications, both sets could link to peripherals like a tape cassette, keyboard, and telephone coupler.

So far Signetics has concentrated on the market represented by manufacturers of programmable video games, but it plans to introduce chips that will expand its sales to include the makers of home computers. GI has developed a concept called the home information center to demonstrate what the 8900 series can handle besides games.

"We developed the home information center concept because of the blurring of the distinction between programmable games and computer applications of the microprocessor," says Ron Stephens, general manager of microprocessor products. "We predict that game-computer systems will be the largest-selling consumer electronics product, reaching a larger volume than the sum of calculators and digital watches today."

For its part, Signetics is promoting its system's lower pin count—since fewer interconnects mean low total systems cost—in addition to its high resolution and flexibility in generating characters or symbols on the screen. Some game chips generate characters in an internal random-access memory so they produce the same set of characters for any game module they're in, observes Kam Li, the firm's project manager for microprocessor-based video games. "Instead, the Signetics characters are generated externally in a read-only-memory chip put in the program cartridge, so every game can have a different generator."

The system obtains high color resolution partly from its high speed of 3.58 megahertz, about the limit for home TV screens. Because of the way it generates characters, it can shift them fast. Rather than using a RAM that must be addressed and refreshed for each movement at video frame rates to be put on screen, Signetics' circuitry grabs the characters out of the cartridge read-only memory. □

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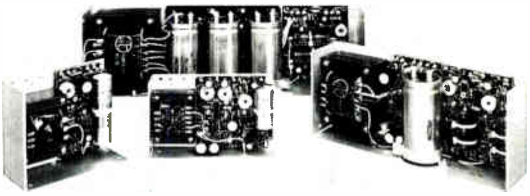

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	6.0	HC5-6/OVP*	49.95
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	5.1	HN12-5.1	64.95
	6.8	HD12-6.8	74.95
	10.2	HE12-10.2	104.95
15	0.5	HA15-0.5	$22.95
	1.5	HB15-1.5	24.95
	3.0	HC15-3	44.95
	4.5	HN15-4.5	64.95
	6.0	HD15-6	74.95
	9.0	HE15-9	104.95

VOLTS	AMPS	MODEL	PRICE 1-9
24	1.2	HB24-1.2	$24.95
	2.4	HC24-2.4	44.95
	3.6	HN24-3.6	64.95
	4.8	HD24-4.8	74.95
	7.2	HE24-7.2	104.95
28	1.0	HB24-1.2	$24.95
	2.0	HC28-2	44.95
	3.0	HN28-3.0	64.95
	4.0	HD28-4	74.95
	6.0	HE28-6	104.95

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	3.0	HD48-3	79.95
	4.0	HE48-4	109.95
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15	15.0	F15-15	$149.00
24	12.0	F24-12	$149.00
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HBB15-1.5	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A or −5V @ 0.7A	49.95
HCC15-3.0	12V @ 3.4A or 15V @ 3.0A	−12V @ 3.4A or −15V @ 3.0A	79.95
±18 to 24V			
HAA24-0.6	18-20V @ 0.4A or 24V @ 0.6A	(−)18-20V @ 0.4A or −24V @ 0.6A	$39.95
±5V			
HBB5-3/OVP	5V @ 3.0A*	−5V @ 3.0A*	$61.95
HCC5-6/OVP	5V @ 6.0A*	−5V @ 6.0A*	92.95
5V and 9-15V (Isolated Outputs)			
HAA512	5V @ 2.0A*	9-15V @ 0.5A	$44.95
HBB512	5V @ 3.0A*	9-15V @ 1.25A	54.95
HCC512	5V @ 6.0A*	9-15V @ 2.5A	86.95

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CBB-75W	5V @ 6.0A	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A	$ 91.95
DBB-105W	5V @ 12.0A	12V @ 1.7A or 15V @ 1.5A	−12V @ 1.7A or −15V @ 1.5A	$126.95

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Washington newsletter

Grumman, Hughes seek to extend life of F-14

Grumman Aerospace Corp. of Bethpage, N. Y., and Hughes Aircraft Co. in Culver City, Calif., are developing alternative system concepts for the F-14 Tomcat that would enable the Navy fighter to meet the threats of the mid-1980s and beyond. **Their idea is to eliminate the need for a new fighter plane.** Under their funded Cilop (conversion-in-lieu-of-procurement) studies, the major airframe and avionics enhancements proposed will be directed first toward the F-14's air-to-air role and then toward air-to-surface and reconnaissance missions.

High on the list of avionics changes are a modified AWG-9 fire-control system for the Phoenix missile built by Hughes. Among the proposed modifications are increased detection range, improved target discrimination and beam and tail look-down detection, reduced electronic-countermeasures susceptibility, and improved tracking for combat maneuvering. Other changes being weighed in the avionics aboard Grumman's Tomcat are the addition of a jam-resistant voice-data link and a MIL-STD-1553A–compatible multiplexed avionics data bus, and new controls and displays, such as an AIDS (aircraft integrated-display system) cockpit with four cathode-ray tubes displaying fuel management and engine and tactical data in both the pilot's and the flight officer's bay.

The final set of alternatives is to be submitted to the Navy in April. Hopes are that money will be released this summer to begin a demonstration and validation phase to run from October 1978 through early 1980, culminating in flight tests of advanced developmental hardware.

White House seen slow to act on CB imports

A 5-to-1 ruling by the International Trade Commission near the end of January that U. S. makers need relief from damage caused by imports of citizens' band radios goes to President Carter this month. But Government and CB industry sources privately agree that the White House will not take immediate action to help the industry, which is depressed by the glut of unsold CBs on the U. S. market. A Carter decision—not expected quickly—may be **to use the ITC ruling as further leverage against Japan on trade issues.**

Yet industry groups like the Committee to Save American CBs, headed by E. F. Johnson Co. president Richard Horner, believe that will be of little help. "Currently, Taiwan, Korea, and Hong Kong manufacture and export to the U. S. as many CB radios as Japan does," the committee says in its call for immediate relief. E. F. Johnson petitioned for an ITC ruling last August and was subsequently joined in the action by Motorola Inc., Hy-Gain Electronics Corp., and the Pace division of Pathcom Inc.

GAO scores NATO's lack of standardization

A General Accounting Office report calls on Congress to restrict funds for U. S. weapons systems that may be used within the North Atlantic Treaty Organization if the weapons are not interoperable with those of U. S. NATO allies. However admirable the GAO goal of urging Congress to use its appropriations power to push for more NATO weapons standardization, **the study—and the timing of its release—has reportedly infuriated the White House and Defense Department leaders,** who have just completed submission of a fiscal 1979 spending program aimed at rebuilding NATO's military capability (see p. 73). The GAO, investigative watchdog for the Congress, says the NATO forces of its 15 member nations now deploy at least 7 basic tank models, 23 combat aircraft types, over 100 different tactical missile systems, multiple guns of different calibers, "and a host of different types of radars—36 in NATO's navies alone," and it states that virtually none of the system types are interoperable.

Army awards two contracts for Divads competitive development

The first two competitive Army development contracts for a new mobile air-defense gun have been awarded to Ford Aerospace & Communications Corp., Newport Beach, Calif., and General Dynamics Corp.'s Pomona, Calif., division. Equal awards totaling $79 million for the system known as Divads—for division air defense gun system—were made by the Armament Research and Development Command, Dover, N. J. Divads, proposed replacement for the 20-millimeter Vulcan gun, will be designed for defense for tanks and mechanized infantry against low-flying, maneuverable aircraft and helicopters. Under the two-year contracts, **each company will develop two prototypes for three months of test and evaluation,** after which both firms will bid for first production. Ford's subcontractors include Westinghouse Electric Co., Baltimore, for the radar in the computer-controlled tracking and firing system; Sweden's AB Bofors for the 40-mm gun and ammunition, and AAI Corp., Baltimore, for the armored turret and its integration with the gun on a Government-furnished, modified M48A5 tank chassis.

I/O-channel-level interface standard is ready, says CCIA

The National Bureau of Standards may get a chance to recognize the adoption of the first input/output-channel-level interface standards following their recent acceptance by the industry-sponsored American National Standards Institute standards committee known as X3. The long-delayed vote by the 51-member ANSI unit on a mail ballot showed 26 in favor, 13 opposed, 2 abstentions, and 10 not voting, says the Computer and Communications Industry Association. "Not voting" is presumed to be a vote in favor of adoption under rules of the International Standards Organization, says CCIA, **making the tally 36 in favor and 13 opposed** and exceeding "the two-thirds-in-favor rule mandating that ANSI report the adoption of the standard as an American national standard to NBS."

Military ATE market will top $1 billion, survey says

Military buys of automatic test equipment should exceed $1 billion in fiscal 1978 and rise by 40% over the following four years to $1.4 billion by fiscal 1982, according to a new market forecast by New York–based market researchers Frost & Sullivan Inc. **Total five-year funding for military ATE should reach about $6 billion,** says the company, acknowledging that its earlier forecasts were too conservative. The related defense market for electronic test equipment reached $615 million in fiscal 1977, has been expanding at an annual rate of 15%, and "should maintain or increase this rate," the company contends.

U. S.-Soviet hotline goes space age

The Washington-to-Moscow hotline, providing secure and reliable communications between U. S. and Soviet officials, **now uses two independent and parallel satellite circuits,** the Intelsat IV and Molniya systems, in conjunction with two earth stations in the U. S. and another pair in Russia. ITT Space Communications Inc. of Ramsey, N. J., a subsidiary of International Telephone and Telegraph Corp., produced high-power amplifiers, low-noise receivers, and associated radio and control units for the Soviet earth stations.

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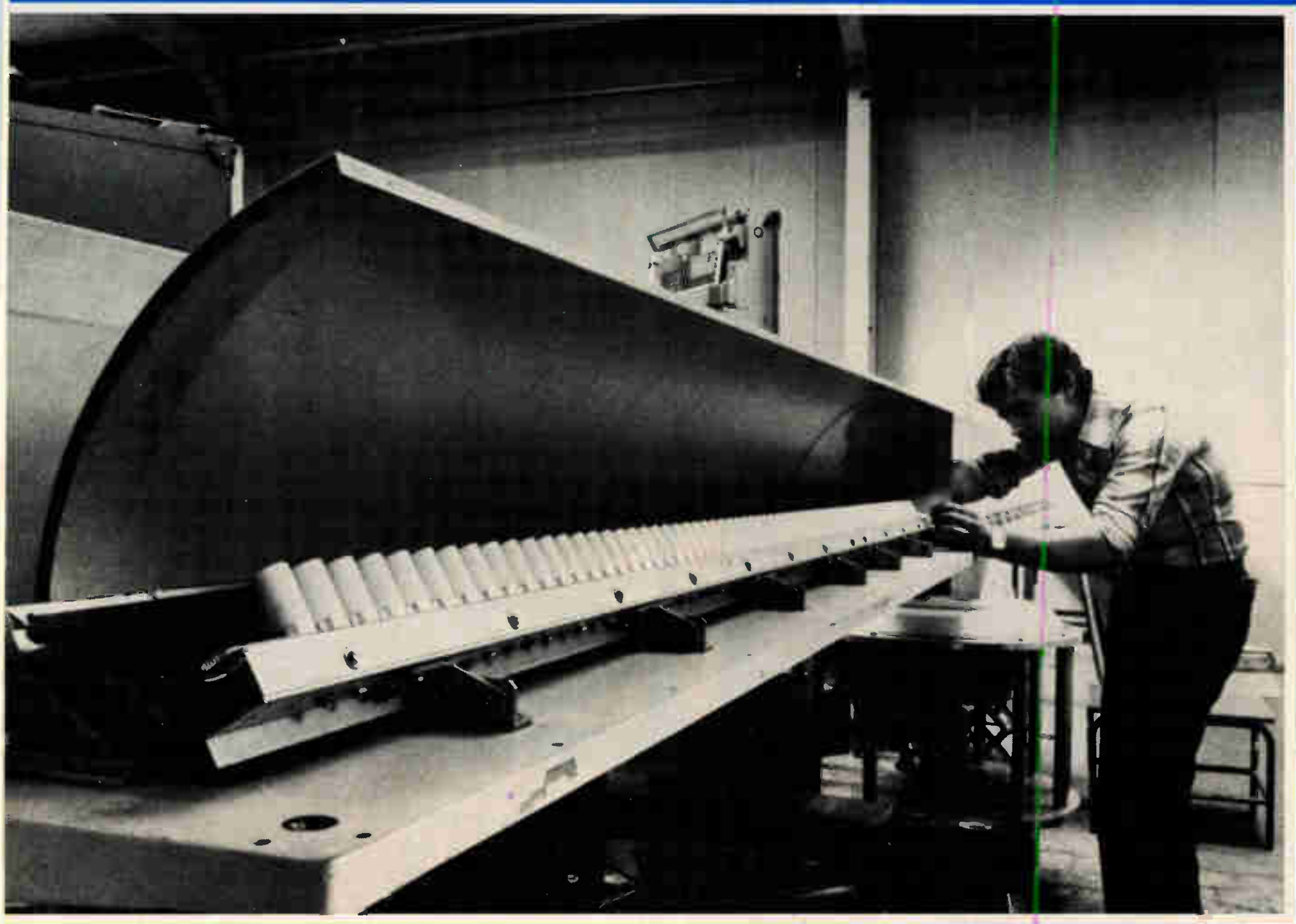
Feb. 2, 1978

Electronics International

Six lasers and waveguides on a chip multiplex optical traffic: page 3E

Cylindrical feeds of radar antenna have radiating heads for polarization- and frequency-diversity operation: page 4E



International newsletter

Quartz-watch IC incorporates a 4-MHz oscillator

Makers of quartz wristwatches can now look at samples of a Eurosil GmbH IC incorporating a 4-MHz oscillator. The Munich-based firm says the high circuit frequency of the device provides cost, space, and accuracy advantages for the watch makers because 4-MHz crystals are smaller, less expensive to make, and mechanically and thermally more stable than the 32-kHz crystals usually used. **Although operating at 4 MHz, the e1154 consumes only about 6 μA at 1.55 V,** the result of using complementary-MOS silicon-gate techniques, the firm says. Price is not set, but volume delivery will get under way within two months.

Fujitsu computer takes over top of the line . . .

Fujitsu Ltd. says it will start deliveries this autumn of its M-200 computer, a new top-of-the-line model in a series it developed with Hitachi Ltd. **The performance of the M-200 is said by the company to be 1.5 to 1.8 times that of its M-190,** the former top model, which itself is roughly equal in performance to the new IBM 3033, says the firm. The new computer features 16-k n-MOS chips in its main memory, which can be expanded to 16 megabytes in 2-megabyte increments. Logic circuits are similar to the 100-gate Amdahl-type ICs used in other large Fujitsu computers. Rent of a minimum-configuration system starts at $145,833 per month.

. . . while Hitachi readies a new top

Meanwhile, Hitachi is racing to complete an even larger computer in the same series, tentatively called the M-210. Industry sources say that **it will feature high-speed logic circuits with 400 gates in the central processor** and 16-k n-MOS chips in the main memory. Fine-pattern technology with reduced capacitance enables Hitachi to decrease the joule input per gate for a given speed. Thus it can put more gates on a single chip without exceeding the power dissipation allowable in practical packages.

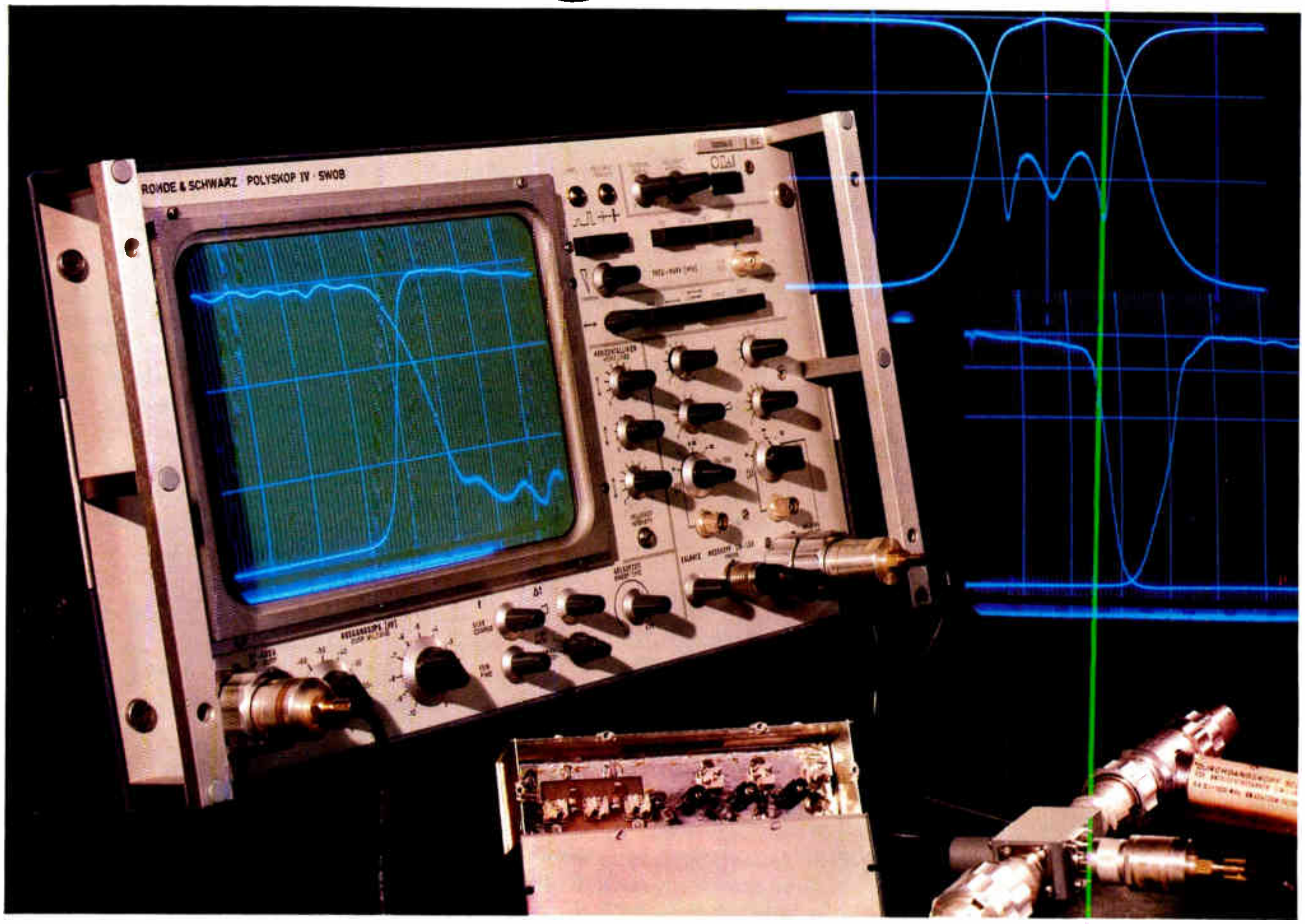
Eurocard holds 8-bit microcomputer that costs $190

Just out from Valvo GmbH is a microcomputer on a Eurocard costing about $190. The 8-bit system on a 10-by-16-cm pc board is built around a 2650 microprocessor from fellow Philips' subsidiary Signetics. The VA200 includes 256 bytes of random-access memory, 4 kilobytes of bipolar programmable read-only memory, a clock generator, and 50 input and output lines. **Company designers say the compactness results from a very tight layout and careful selection of the memory devices for minimum area and pin number.** While Valvo is limiting marketing to West Germany, parent Philips is considering selling it elsewhere in Europe.

GI Microelectronics to build interface unit for BPO Viewdata

The British Post Office will award the contract for development of a Viewdata line-transmission unit to General Instrument Microelectronics Ltd. The unit will permit transmission and reception over the telephone line to and from the BPO's central data bank. **It is likely to comprise a large-scale integrated complementary-MOS chip complete with the tone-generator and tone-decoding circuitry,** a couple of integrated operational amplifiers, and a line-isolated transformer. The company says it also is well advanced with its decoder for Viewdata and the more limited Teletext service.

Polyskop IV – the fourth generation



Polyskop IV SWOB sweeps through 0.1 to 1000 MHz continuously and with one sweep-width setting giving typical harmonics suppression of −40 dB; on the big 21 × 16 cm screen you can work with linear and log scales simultaneously.

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Six lasers on a chip with waveguides give multiplexing

Wavelength-division method of sending optical signals depends on selectivity of distributed-feedback laser

Wavelength-division multiplexing of optical-fiber communications is taking a step closer to reality in Hitachi Ltd.'s central research laboratory. Engineers there are developing a thin-film integrated circuit with six diode lasers operating at different wavelengths, together with branched waveguides that feed all six outputs into a single waveguide.

Interest in wavelength-division multiplexing is high, because it can multiply the information capacity of optical-fiber communications systems the same way that frequency-division multiplexing increases the bandwidth in coaxial-cable and microwave systems. The key to such optical-fiber multiplexing is semiconductor heterojunction diode lasers operating in the distributed-feedback mode, Hitachi says.

"Diode lasers with grating feedback are being looked upon as promising light sources because of their inherent mode and wavelength selectivities," says Michiharu Nakamura of the central lab. Their batch-fabricated configuration, avoiding cleaved mirrors, also makes it possible to integrate them with other optical devices.

Demultiplexing. Work has also started at the lab in Tokyo on a chirped diffraction grating that will demultiplex the signals. The diffraction grating will be integrated with a multiple photodetector that will receive the demultiplexed signals.

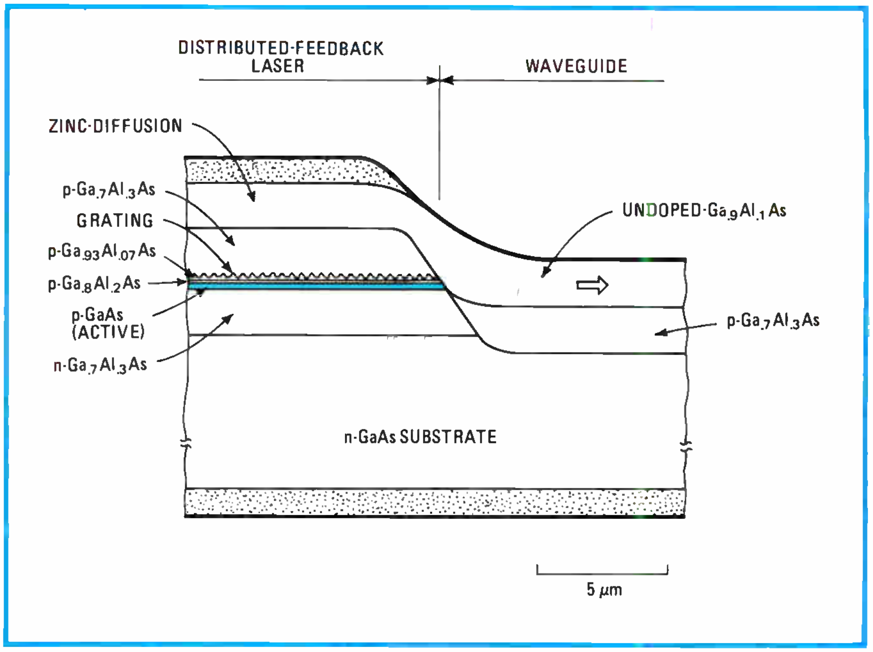
"Optical wavelength-division multiplexing should prove useful in high-speed digital transmission, because of the large transmission capacity achievable without increasing the bit rate," says Nakamura. "It will also be effective in application to video services in subscriber loops."

A distributed-feedback laser [*Electronics*, July 25, 1974, p. 38] operates at a single frequency during both pulse and continuous-wave transmissions. Because the output spectrum is narrow, a single optical fiber can carry many transmissions simultaneously, using little bandwidth.

Separate structure. The diffraction gratings that set the wavelength of the individual lasers on the chip can be fabricated separately. Putting the grating outside the laser's active region is a move that gives a separate confinement structure preventing nonradiative recombination of the injected carriers.

Successive shifts of 9 angstroms in the gratings' wavelengths give 20-angstrom shifts in the lasers' wavelengths. The 20-angstrom shifts compensate for the ±5-angstrom errors caused by the thickness and composition of the epitaxial layer. They also will permit a system of 10 separate wavelengths, since the gain spectrum bandwidth of gallium arsenide typically is 200 angstroms.

Fabrication using mesa etches produces the laser-waveguide combination shown below. The butt joint formed at the intersection of the



More light. Hitachi IC will contain six of these waveguides and associated lasers with grating feedback. It is intended for wavelength-division multiplexing of optical-fiber communications.

tion changes from pulse to pulse and since two different frequencies are used, echo sequences of four different frequency-and-polarization combinations result.

In processing the return signals, the first step is digitization, which uses amplitude-evaluation and video-subtraction methods that suppress return signals from areas of extensive sea clutter. The next step is to correlate echo sequences of different frequency and of identical polarization occurring at the same time.

Then the echoes of differently polarized transmitter signals from successive echo sequences are correlated with respect to time. This step is carried out after each previous echo sequence has been buffered for one radar sweep. In a fourth step, the bandwidth of the video signals is reduced so that they can be transmitted with standard radio-link equipment to a radar control center for automatic signal processing.

More processing. While a contract for the control center has not been awarded, AEG-Telefunken does have plans ready. One plot extractor per radar system would identify targets from the sum of signals offered. The digital plot extractor, modified for sea monitoring from the type used in air-traffic control, would convert the radar signals into target data.

A process computer belonging to the AEG-80 family would be used at the control center for target tracking. Its prime functions would include computing the target position and the velocity vector and, using extrapolation methods, predicting future sea traffic patterns. The computer also would convert the plot data and the traffic-analysis data to a form suitable for screen display.

The information would be shown on indicators for sectional control and on a master display for monitoring a whole sea region. It would be possible to overlay the displays with an electronic map showing the shore lines, the boundaries of navigation channels, the radar center line, and any obstacles such as buoys. Ship targets could be shown in the form of a target trail, a velocity vector or as a lined contour. □

The Netherlands

Flexible voice response unit will have many messages for telephone subscribers

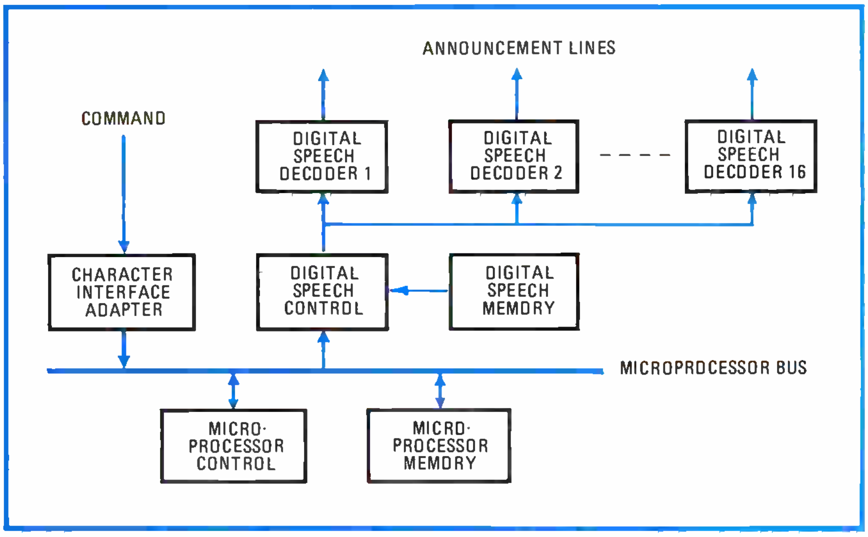
Later this year, some telephone subscribers in two Dutch cities will be able to order wake-up calls and four similar services from a voice response unit tied into the central computer at their telephone exchanges. Under microprocessor control, the unit strings together speech elements to compose messages. The subscribers will use their telephone dials or keypads to program the exchange's computer to deliver each service to them.

To be tried out in Amsterdam and Heerenveen, this cluster of services is a special feature of the PRX205 stored-program-controlled exchange developed at Philips Telecommunicatie Industrie BV and being installed throughout Holland [*Electronics*, Jan. 5, p. 9E]. Besides ordering a wake-up call, the subscriber can ask for the charges on a phone call just made and order the voice response unit to tell callers he is away until a given time or date or does not want to receive calls. Also, the VRU can tell him how to program the central processor for abbreviated dialing services.

While the Philips VRU is not the first voice generator designed for telephone use, "what distinguishes our unit from others is its high degree of flexibility," says Joop Brakel, head of the basic development group for public telephone equipment at the Hilversum laboratories of the firm. With a limited number of speech elements, virtually millions of different messages can be composed and reproduced, he says.

Work elsewhere. In the U. S., American Telephone & Telegraph is trying out a magnetic-bubble memory with eight messages for call-assistance announcement [*Electronics*, Feb. 17, 1977, p. 38]. Moreover, Bell Telephone Laboratories is working on at least two types of "talking" computers, in which digitally encoded information is converted into speech, an AT&T spokesman says.

At the heart of the VRU is a speech memory that can store the digital information for up to 256 speech elements. For the two-year trials, it will contain only about 80 such elements, a number that officials of the Dutch ministry for posts, telegraph, and telephone consider sufficient to compose all announcements



Hello, hello. A Zilog Z80 controls the process of turning commands from a phone exchange's central computer into messages that are part of a cluster of services for subscribers.

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for the five services the unit will initially provide.

In addition to the 80 or so speech elements, the memory contains the information for often-used words like the names of days and months and for the numbers from 1 to 20. Also stored are the syntax rules and the lengths of pauses needed to produce intelligible sentences. Using different combinations of numbers, the subscriber can avail himself of the various services.

The subscriber may receive a series of instructions from the VRU. With the wake-up service, for example, the unit will tell him to key in or dial in the wake-up time and the number of consecutive days for which the service is desired.

Computer commands. Triggering and specifying all VRU operations are 8-bit parallel signals generated in the exchange's central computer (see diagram), in response to the subscriber-initiated pulses or tone-frequency codes. The character-interface adapter enables the 8-bit parallel commands to be fed to the microprocessor bus and to start all VRU actions. An operational program stored in the microprocessor memory constructs the desired announcement, using the speech elements and the appropriate syntax rules from the speech memory. The two memories use metal-oxide-semiconductor 16,384-bit random-access-memory MK4116P3 chips from Mostek Corp., with Intel Corp. as a second source.

Once the message ordered by the central computer has been composed, it goes through the digital speech control, where addressing, parallel/series conversion, and demultiplexing are implemented in low-power Schottky devices, to a Philips large-scale-integrated decoder, which reproduces the signal in analog form and feeds it to an output line called the announcement line. In its trial form, one VRU will be able to handle simultaneously 16 messages to subscribers, through 16 decoders and announcement lines.

The microprocessor memory, controlled by a Zilog Z80 processor, can be extended from its basic 16-kilobyte configuration to 32 kilobytes if a more extensive operational program is needed in future applications. The digital speech memory is also extendable in steps of 128 kilobytes to a maximum capacity of 1,024 kilobytes. This capacity corresponds to 240 seconds worth of speech encoded at a 32,768-bit-per-second rate.

Speech elements. The VRU was conceived at the Hilversum labs, with design carried out at Philips Telecommunicatie's affiliate in Brussels. Engineers from the PTT provided the digital speech elements, produced as words recorded by professionals. A delta-modulation encoding technique then converts the

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Circle 231 on reader service card

words into digital elements.

Brakel explains that this technique, carried out at a 32-kb/s sampling rate gives the same speech quality as a 65,536-bit/s pulse-code-modulation scheme. Since the delta technique requires only half the bandwidth of the PCM method, memory space to store the coded information is half as great. □

France

Magnets to give precision scanning to earth observations by satellite

Magnetism can make for better satellite pictures of the earth, figures the French space agency, Centre National d'Etudes Spatiales. So CNES is designing a scanning system based on magnetic control of a mirror that will pivot on magnetic bearings.

As an earth-observation satellite orbits, building up a picture requires some sort of scanning method to move the image across the detector. One way to do this is with a complex optical system that displaces the image in the focal plane of the telescope, the approach used in the European weather-predicting satellite, Meteosat [*Electronics*, Nov. 10, p. 8E]. The other approach, used in the U. S. Landsat series, is a moving mirror that is placed in front of the telescope.

Precision. Of course, to obtain a reasonable resolution of the image, the movements of the mirror must be extremely precise. For a medium-resolution imaging system, probably to be launched on the French earth-observation satellite SPOT, the space agency settled upon a precision of 5×10^{-6} radian for a 35-centimeter mirror making eight oscillations a second with a crest-to-crest amplitude of 0.2 radian.

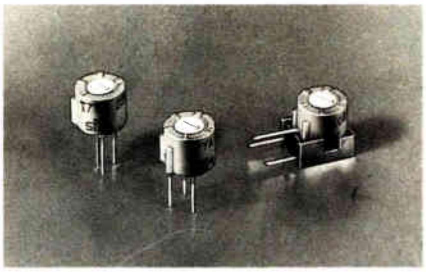
The design team at the CNES space center in Toulouse says that stopping the mirror with contact arms results in unwanted vibration, as well as wear and tear. Moreover, the usual flexible pivots on which the mirror is mounted are not firm enough to provide the degree of precision necessary in moving the mirror.

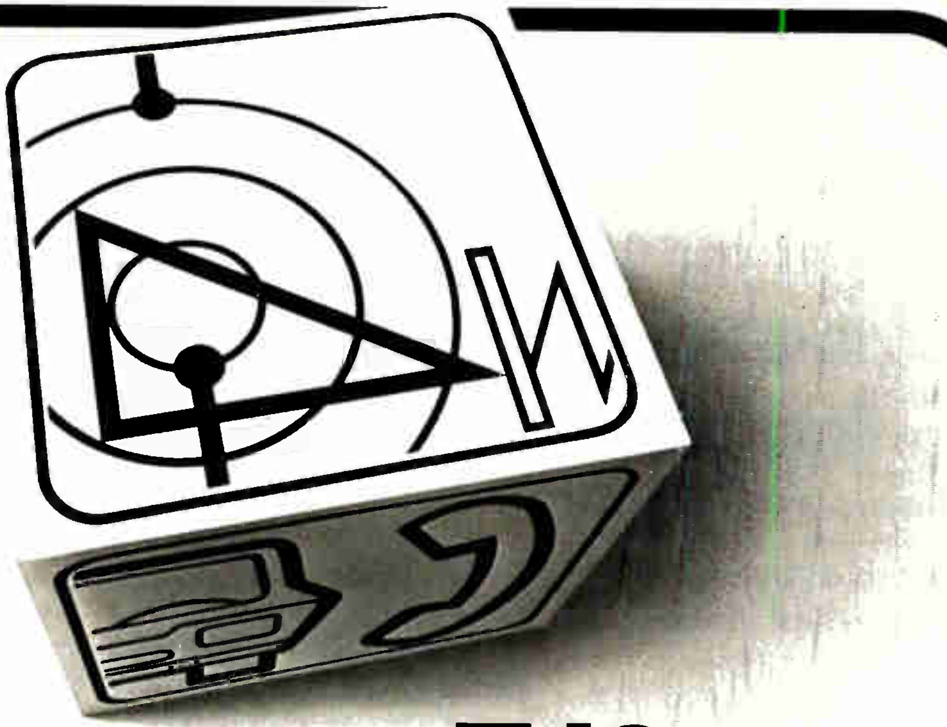
The solution for CNES is to use the principle of passive magnetic rebound, coupled with friction-eliminating magnetic bearings developed by the Société Européenne de Propulsion of Puteaux, a Paris suburb. To make the mirror oscillate, it is first started by a motor. Then magnets on the satellite body or on the mirror assembly create magnetic fields that brake the mirror at the end of each scan, then bounce it back in the opposite direction. Thus the mirror keeps oscillating with only intermittent help from the motor.

While CNES and SEP have not settled upon the exact form of implementation, the space agency has applied for patents covering the magnetic rebound scheme in Europe and the United States.

Expenses. The system will not be cheap, because the magnetic bearings need control electronics to deliver the correct currents to the magnets. The magnet system will probably be 15 to 20 cm larger than the mirror, SEP engineer Claude Fouché estimates. The magnetic bearings will allow the mirror to pivot, but will restrain other kinds of movement. SEP will be constructing a prototype this year.

The combination of passive magnetic rebound and magnetic bearings will give a low energy consumption, says Fouché. The firm cannot say yet just how low, but judging from the specifications for its standard magnetic bearings, a good guess would be a few watts. □





Td2 System

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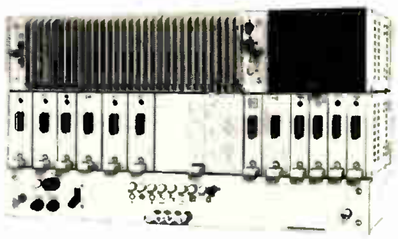

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Circle 233 on reader service card

Huge memory helps logic-state analyzer to find program flaws

by Charles Cohen, Tokyo bureau manager

32-channel instrument built by Japanese firm stores 1,024 bits per channel, helps debug microprocessors

In logic-state analyzers, the larger the memory capacity, the more likely it is that the test operator will be able to catch a flaw that is buried deep in the program. An analyzer developed by Ando Electric Co. of Japan includes a memory of 1,024 bits per channel for 32 channels, compared with the conventional eight channels, for a total capacity of 32,768 bits.

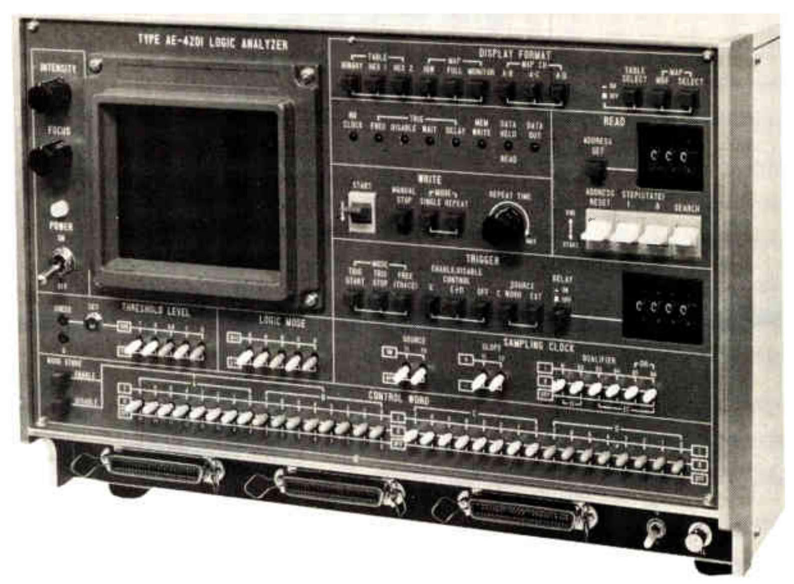
The analyzer, designated the type AE-4201, displays logic states for the 32 channels to aid in system debugging and maintenance of microprocessors. It is ideal for 8-bit microprocessors, the company says, because it provides 16 channels for the address bus, 8 channels for the data bus, and 8 channels for other purposes such as links with peripheral equipment. Besides simplifying analysis of relatively large blocks of program, the large storage capacity of 1 kilobit per channel enhances the probability of capturing the timing of misoperating sequences that occur only infrequently. Maximum clock frequency is 5 MHz, which is more than sufficient for the present generation of microprocessors, the company points out.

Two clock inputs are provided so that data can be recorded for two different varieties of timing states. An example would be at read and write of the system's main memory. Although the minimum repetition period of either clock input is limited to 200 nanoseconds, the minimum period between signals at the two clock input terminals is only 50 ns. For sampling timing, six clock qualifier inputs are available, two for one clock input and four for the other.

On the front panel of the 4201 are 32 control-word switches that can be set at OFF, DON'T CARE, 0 or 1. These controls set the commands TRIGGER WORD, ENABLE WORD, or DISABLE WORD during recording. They are also used to select search words, which are displayed as black on white rather than the standard white on black. These switches are also used for cursor word or select word during mapping display.

Front-panel switches permit setting of the threshold level of each data block, the logic mode of each data block (high equals logic 1 or low equals logic 1), the slope of each timing signal (trigger on positive-going or negative-going signal), and the state (0 or 1) of each qualifier signal. The trigger can be set so that data represents 1,024 events following trigger or the last 1,024 events preceding trigger. Delayed-trigger, sequential-control, and trace-mode operations are also selected by controls built into the front panel.

Three basic modes of state-table display are available, with each showing 16 bits of all 32 channels, 1 bit for every channel on each of 16 successive lines. In the binary mode, data for all four blocks is shown in

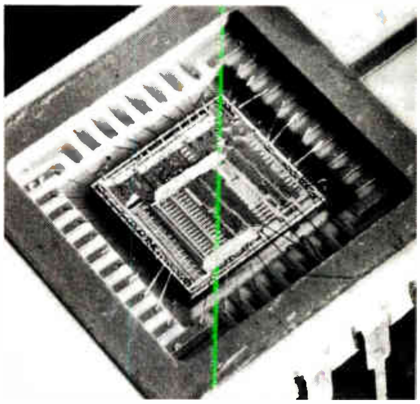


binary format. In Hex 1 mode, data for the first three blocks is shown in hexadecimal format, and data for the fourth block in binary format. In Hex 2 mode, data for all four blocks is shown in hexadecimal format, with data for blocks three and four repeated in binary format. The address of top line can be selected with a three-digit thumbwheel, or line-shaft push buttons can shift the display up or down. Sequential search for lines containing the search word, matching that in control-word panel switches, is also possible. Either way, lines containing the search word are displayed black on white to present an eye-catching contrast to the instrument user.

Map display is also available, with a number of variations. For map display the A_0 through A_7 data block determines the Y position of the spot, while one among the B_0 through B_7, C_0 through C_7, and D_0 through D_7 blocks determines X position.

Price of the logic-state analyzer together with necessary cables is $7,080 in Japan (figured at an exchange rate of 240 yen to $1). Accessories are not needed, and none is available. Deliveries will start in May or June.

Ando Electric Co.,Ltd., 4-19-7 Kamata, Ota-ku, Tokyo 144, Japan [441]

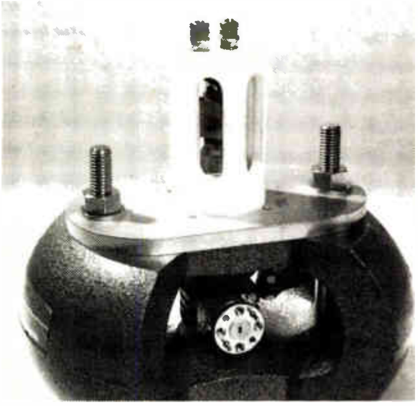


The Ferranti F100-L microprocessor is now available with CORAL 66 compiler facilities. The first release of the software is as a cross compiler to run on ICL 1900 computers. Ferranti Ltd., Microprocessor Marketing Unit, Western Road, Bracknell, Berkshire RG12 1RA, England [447]

The model VP7703A distortion meter is designed to measure total distortion factors as low as 0.01% of full scale. It operates at three spot frequencies: 20 Hz, 1 kHz, and 20 kHz. Matsushita Communication Industrial Co., Tsunashima-higashi, Kohoku, Yokohama 223, Japan [443]

A635 extended-foil polystyrene capacitors are offered with values from 100 pF to 14 nF and have voltage ratings of 63 V dc and 25 V rms. They have a tempco of about 150 ppm/°C. Salford Electrical Instruments Ltd., Peel Works, Barton Lane, Eccles, Manchester M30 0HL, England [445]

The TDE 1607 CM is an analog integrated circuit for the control of lamps, relays, stepping motors, and similar loads up to 750 mA. It is internally protected against shorts and overheating. Sescosem, 50 rue Jean-Pierre Timbaud, B. P. 120, 92403 Courbevoie, France [448]



A high-reliability, fixed-frequency pulsed magnetron, the model M5163, operates in the 94-to-96-GHz band. The 3-kW unit, which is typically operated at a 0.02% duty cycle, has an expected life of 750 hours. EEV, Waterhouse Lane, Chelmsford, Essex CM1 2QU, England [444]

A dc torque motor with a maximum winding temperature of 200°C puts out a peak torque of 40 oz-in. while drawing 114 W of power. Its no-load speed is 380 radians per second. The motor weighs 5.7 oz. Servodata Ltd., Highclere, Newbury, Berkshire RG15 9PU, England [446]

Designed for troposcatter communications, the TH 3588 traveling-wave tube puts out 1.1 kW over the range from 4.4 to 5.0 GHz. The tube, which employs permanent-magnet focusing, has a gain of 36 dB. Thomson-CSF Tubes, 38 rue Vauthier, 92100 Boulogne-Billancourt, France [449]

Opening new frontiers with electro optics

Just what the doctors ordered: RCA-developed PMTs that allow whole-body CT scanning in only 2 seconds.

Computerized tomographic (CT) X-ray scanners are creating a lot of excitement in medical circles. Unlike conventional X-rays, where a dense object can block out something important such as a tumor, a CT scan from hundreds of directions produces a highly revealing, complete cross-sectional view of the patient.

Vital links in this process are the hundreds of photomultiplier tubes which measure light scintillations caused by X-ray beams passing through the body and striking individual crystal detectors. RCA, of course, has a long background in the design and manufacture of PMTs. So we've been able to provide extremely reliable tubes with the performance required for critical measurements at ever-faster scanning speeds—users report as fast as 2 seconds.

These PMTs feature a wide dynamic operating range due to a highly conductive cathode surface and low anode dark current characteristics. Cathode currents of several nanoamperes and anode dark current in the picoampere range are possible when using the PMTs at operating voltages around 600 volts, characteristic of most CT scanning systems.

Two sizes of RCA 10-stage head-on tubes are being used in scanners. The 4886 has a 3/4" diameter and the S83001E a 1/2" diameter bialkali photocathode.

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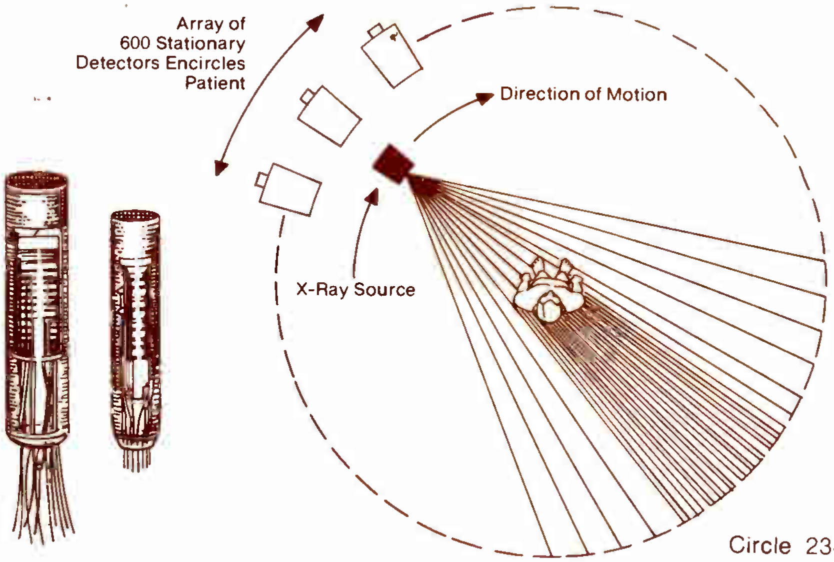

Circle 234

For spectroscopists: PMT with improved responsivity out to 850 nanometers.

The popular RCA 4840 1-1/8" dia., 9-stage PMT has been improved again. Its high responsivity now extends over a broader spectral range—to 850 nm typical. And there are some other benefits from buying this RCA tube. The assurance that comes from domestic manufacture. Prompt delivery. Price—about $55. And in-depth application support from people who really know how to help you get the most from a PMT.

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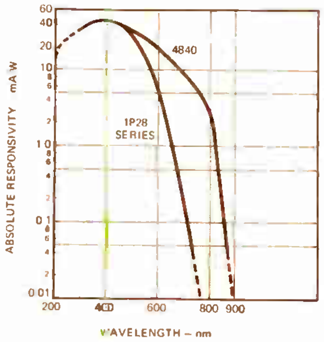
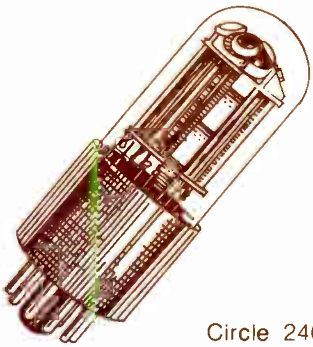


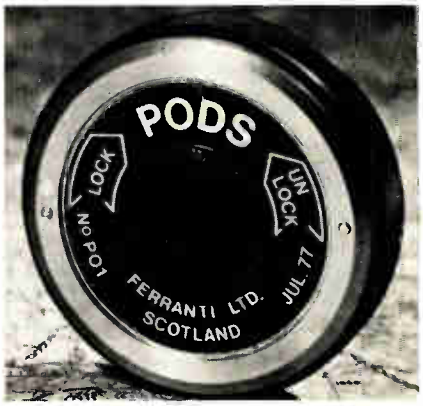


Circle 246

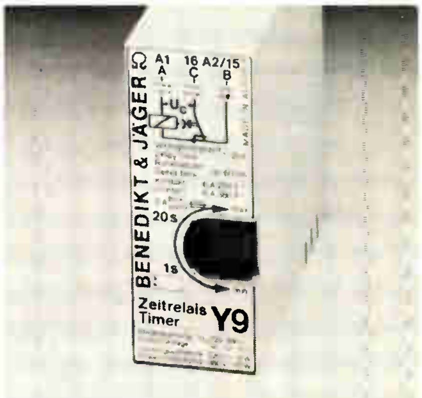
If electro optics can solve your problem, remember: EO and RCA are practically synonymous. No one offers a broader product spectrum. Or more success in meeting special needs. Call us for design help or product information. RCA Electro Optics, Lancaster, PA 17604. Phone 717-397-7661. Sunbury-on-Thames, Middlesex TW16 7HW, England; Ste.-Anne-de-Bellevue, Quebec, Canada; Sao Paulo, Brazil; Hong Kong.

RCA

With the jitter meter PJM-1 it is possible to measure jitter on pulse-code-modulation systems operating at 2,048 and 8,448 kilobits per second. Positive, negative, or peak-to-peak jitter values can be measured. Wandel und Goltermann, 7410 Reutlingen, P. O. Box 259, West Germany [456]



The PODS 2091 portable data store is a robust device designed for airborne applications. Its principal use is in transferring data from ground-based computers to airborne units. Inertial Systems Dept., Ferranti Ltd., Silverknowes, Ferry Road, Edinburgh EH4 4AD, Scotland [457]



An electronic timer, called the Y9, is intended specifically for star-delta starter applications. Dwell time is 75 ms; timing periods range from 0 to 20 seconds. The unit will operate from 220 to 415 V at 40 to 60 Hz. B&R Relays Ltd., Edinburgh Place, Harlow, Essex CM20 2DJ, England [458]

Electronics

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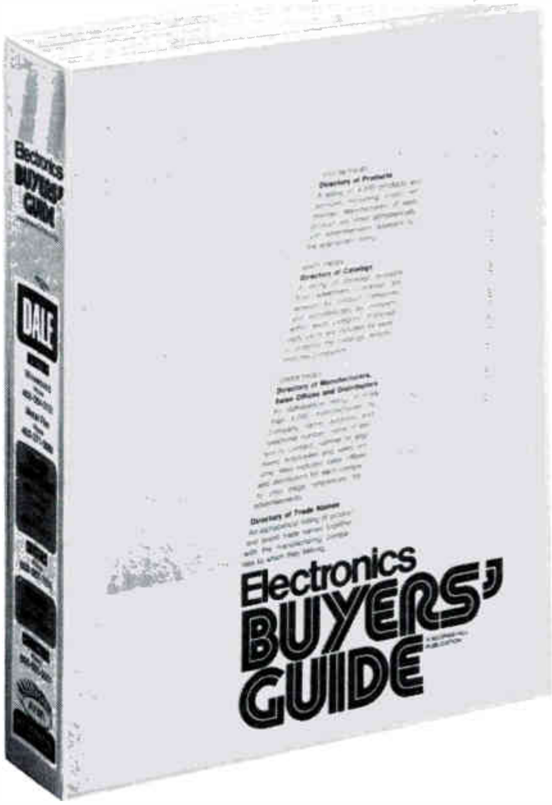

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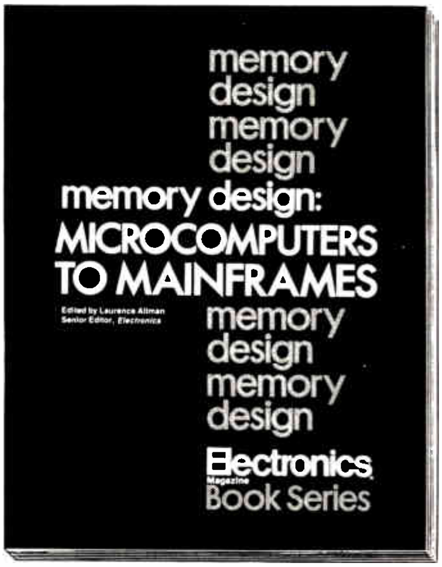

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Carter keeps tight rein on budget

Pentagon spending request is up 9.4% to $115 billion, while significant increase also is ticketed for technology R&D efforts

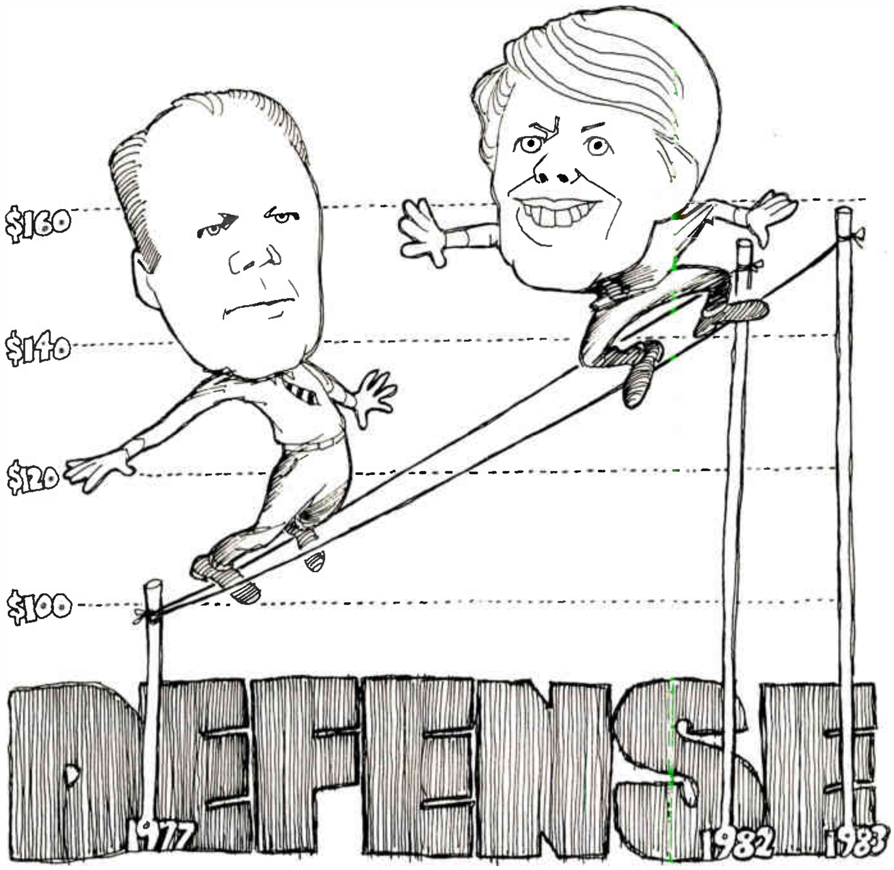
by Ray Connolly, Washington bureau manager

In keeping with the modest image projected in his State of the Union message, President Jimmy Carter delivered his first Federal budget message to Congress at the end of January in a simple brown wrapper, rejecting the costlier, multicolored documents favored by his predecessors. He proposed increasing military outlays by 9.4% to $115 billion and those for overall research and development by 8.5%, both slightly outpacing the total proposed 8% rise in Federal expenditures to $500 billion. Such hikes are a few percentage points above the projected inflation of 5% for the year.

Carter terms the total $126 billion defense package "prudent and tight," although the $115 billion for procurement is a peacetime record. The additional $11 billion is proposed for future commitments. The military budget contains what Secretary of Defense Harold Brown calls "a significant reordering of priorities" to beef up the North Atlantic Treaty Organization with a resultant heavy emphasis on Army procurement of tactical weapons.

Navy shipbuilding will be cut back sharply with a $400 million drop in procurement to $13.9 billion. Heavy stress on tactical aircraft accounts for most of the $700 million boost in Air Force procurement funds to $11.1 billion, as antitank and fighter planes take precedence over such strategic systems as the new M-X mobile intercontinental missile.

The strong NATO orientation of Carter's defense spending plan delights the Army. It emerges as the big percentage winner in the procurement category, after years of



Trends? The Administration has put together a five-year projection of its defense spending that shows significant cuts from the outlays forecast by the Ford Administration.

regularly ranking third in the post-Vietnam annual budget battles with the Air Force and Navy. If Congress concurs with the plan—a questionable prospect—Army buys would rise by 25% to $6.6 billion, exclusive of research, development, testing, and evaluation. Proposed Army procurement increases account for $1.3 billion of the total $1.6 billion boost sought by the Department of Defense to raise fiscal 1979 buys to $32 billion.

A feisty Congress, long suspicious of U. S. NATO outlays that its European partners have failed to match, is already asking hard questions about Carter's military priorities. Those suspicions seem sure to be cultivated by outraged admirals who see their inventory of seagoing combat ships steadily diminishing.

Excluding the Polaris/Poseidon and Trident strategic missile-launching subs that are not designed for sea warfare, the Navy will have no more than 313 warships in the fleet by the end of this fiscal year on Sept. 30;

when the SSN-688 nuclear attack submarines are discounted, that leaves the Navy far short of its long-accepted goal of a fleet of some 600 surface vessels five years hence. Congress seems sure to put back money for new ships in fiscal 1979. Besides the single $1.6 billion Trident sub and $459 million SSN-688 boats already proposed, legislators seem sure to reinstate the second attack submarine the Navy wanted. Moreover, the Navy may also get congressional money for a second DDG-47—a modification of Litton's DD-963 that will carry RCA Corp.'s Aegis surface-to-air missile system using advanced radar to guide the General Dynamics Corp.'s Standard missile.

R&D boosts. Almost submerged by the tactical emphasis is the Carter budget's confirmation that high-technology R&D outlays will rise significantly on both military and civilian fronts [*Electronics*, Nov. 24, 1977, p. 59]. The 8.5% increase that would bring overall Federal R&D expenditures close to $27 billion is keyed largely to specific programs—half of them military. However, the President's policy goal is clearly aimed at keeping U. S. technology at the forefront of an increasingly competitive marketplace that has become global.

Responding to the steady decline in R&D spending by the private sector, Carter says he is convinced that "the Federal government must lead the way in investing in the nation's technological future" (see "Who has what for R&D?").

Initial congressional reaction is to applaud the new Carter R&D initiatives for both industries and universities, but to suspect his motives for taking the axe to Navy shipbuilding and leaving other long-term strategic programs essentially flat. Such high-dollar projects develop a built-in momentum, requiring larger outlays each succeeding year once they are started.

By holding back on initial commitments, Carter could manage to limit outlays in fiscal 1980 and 1981—the years in which he promised to balance the Federal budget.

MAJOR REQUESTS FOR WEAPONS PROCUREMENT
(in millions of dollars; quantities in parentheses)

	FY 1978	FY 1979	Contractor
ARMY AIRCRAFT			
C-12A cargo	$17.2 (20)	0	Beech Aircraft
AH-1S Cobra/Tow	144.5 (83)	$ 151.5 (78)	Bell/Avco/Hughes
NAVY AIRCRAFT			
A-4M Skyhawk, USMC	9.1 (21)	116.9 (18)	McDonnell
A-6E Intruder	184.8 (6)	201.3 (12)	Grumman
EA-6B Prowler	141.4 (6)	172.7 (6)	Grumman
A-7E Corsair II	126.5 (12)	27.2	Vought
F-14A Tomcat	890.8 (44)	674.4 (24)	Grumman
F-18 Hornet	654.4	864.8 (5)	McDonnell/Northrop
CH-53E Sea Stallion (1)	18.5	183.2 (14)	Sikorsky/GE
P-3C Orion	323.6 (14)	347.1 (12)	Lockheed
E-2C Hawkeye	196.2 (6)	208.5 (6)	Grumman
AIR FORCE AIRCRAFT			
A-10 close support	831.9 (144)	924.9 (162)	Fairchild
F-15 Eagle	1,666.7 (96)	1,415.7 (78)	McDonnell
F-16 ACF	1,685.3 (105)	1,594.5 (145)	General Dynamics
*Advanced Tanker Cargo (ATCA)	0	156.8 (2)	McDonnell/Boeing
E-3A AWACS	372.9 (3)	304.1 (3)	Boeing
ARMY MISSILES			
Chaparral, surface-air	34.9 (850)	31.9	Ford Aerospace
Hawk, surface-air (1)	111.2 (559)	75.4 (608)	Raytheon
U.S. Roland, surface-air	131.1	225.4 (314)	Hughes
Stinger, surface-air (1)	50.6 (258)	149.9 (2,678)	General Dynamics
Tow, antitank/assault (2)	80.0 (12,261)	54.1	Hughes/Emerson
Lance, surface-surface	81.7 (360)	70.2	Vought
Pershing, surface-surface	48.3	75.7	Martin Marietta
NAVY MISSILES			
Poseidon, FBM	20.2	24.4	Lockheed
Trident I, FBM	1,504.6 (96)	1,129.7 (86)	Lockheed
Sparrow, air-air (3)	177.8 (1,725)	195.0 (2,010)	Raytheon/GD
Sidewinder IR air-air (3)	150.3 (2,900)	129.9 (3,150)	Raytheon/Ford
Phoenix, air-air	94.2 (210)	114.0 (210)	Hughes
Shrike, air-surface (3)	41.9 (900)	31.4 (605)	Various
Harpoon, ship/air-surface	132.5 (234)	133.4 (240)	McDonnell
Standard MR, surface-air	107.9 (480)	109.2 (480)	General Dynamics
Standard ER, surface-sir	66.1 (40)	102.4 (40)	General Dynamics
AIR FORCE MISSILES			
Minuteman II/III, ICBM	333.4	122.8	Multiple
AGM-86, air-surface cruise	381.5 (24)	416.1 (36)	
AGM-65A/B, E/O Maverick, air-ground	8.3	34.5	Hughes
AGM-65C, Laser Maverick	59.7 (100)	7.9	Hughes
Aerial targets/drones (4)	99.3	130.0	Multiple
NAVY VESSELS			
SSN 688, attack sub	310.6 (1)	474.4 (1)	Newport News/GD
DD963, destroyer	383.5 (1)	57.8	Litton
*CGN-42, cruiser (Aegis)	209.9	19.4	Not selected
DDG-47, destroyer (Aegis)	938.6 (1)	10.2	Not selected
FFG, missile frigate	1,217.6 (8)	1,547.9 (8)	Bath Iron/Todd
OTHER PROCUREMENT			
Navstar GPS, Global Satellites	86.7	129.0	GD/Rockwell
M577 A1, tracked command post	51.2 (565)	0	FMC Corp.
M60 series tank (1)	532.7 (840)	411.7 (508)	Chrysler
MK-48, torpedo	162.8 (300)	113.6 (127)	Gould
MK-60, ASW mine (Captor)	77.6 (390)	17.7	Goodyear
MK-30, mobile ASW target	22.0 (12)	20.7 (10)	Northrop
MK-15 CIWS Phalanx, ship gun	81.8 (21)	113.2 (45)	General Dynamics

*First major procurement (1) Includes Marine Corps procurement (2) Includes Navy/Marine procurement (3) Includes USAF procurement (4) Includes Army/Navy requirements

Source: DOD

The House and Senate Armed Forces Committees are already scrutinizing the heavy NATO emphasis in the Pentagon's programs for the 1979 fiscal year. The traditional resistance to increasing America's funding of the alliance seems certain to stiffen this year in the face of rising political and economic tensions with its European allies.

But both President Carter and Secretary Brown are convinced it is now or never for the treaty organization, if it is to survive. Pentagon procurement requests for fiscal 1979 reflect this view. NATO-oriented buys, for example, would include $200 million for production of 314

Who has what for R&D?

While Federal research and development funds will rise just under 9% in fiscal 1979, that part of the $27 billion total earmarked for basic research will rise 10% to $3.46 billion, says Frank Press, the President's science and technology adviser. With most of that money going to universities and colleges, campus researchers are delighted, as are instrument and computer makers, who see a revitalization of the academic market.

Press's Office of Science and Technology Policy acknowledges a significant share of those new monies will be spent for instrumentation too expensive for what many academicians call the Dark Ages of the Nixon-Ford years. These new funds, a pittance in the context of the overall budget, are not expected to provoke meaningful congressional opposition.

R&D requests are broken out this way by the Office of Management and Budget (in billions):

	FISCAL YEAR	
	1978	**1979**
Military (DOD)	$11.13	$12.31
Energy (DOE)	3.88	4.19
Aerospace (NASA)	3.82	4.09
Health/Education (HEW)	2.89	3.14
Science (NSF)	0.71	0.76
Transportation (DOT)	0.34	0.33
Commerce (DOC)	0.27	0.30
All others	1.81	1.86
TOTAL	**$24.85**	**$26.98**

Roland low-altitude air defense missiles by Hughes Aircraft Corp., using the French-German design for an all-weather system mounted on tracked vehicles. Initial spares and RDT&E for the Hughes version put Roland's fiscal 1979 price tag at $225 million. The Army also proposes to spend $8 million for its first 300 British mortars from the Royal Ordnance Factories and $7.5 million for 1,200 more Belgian armor machine guns from Fabrique Nationale.

Tactical. Proposed Army missile and helicopter buys, as well as Air Force emphasis on production of antitank aircraft like the A-10 and fighters for defensive cover, reflect the heavy emphasis on tactical weapons that could be used in a European ground war. Thus the Army missile budget rises nearly $100 million to $990 million.

In addition to Roland, another big winner would be Raytheon Co.'s Patriot ground-to-air missile, designed to replace both the Hawk and Nike Hercules with a system intended to have a high single-shot kill capability while operating in a strong electronic-countermeasures environment. Patriot's budget request rises more than a third to $296 million, including first procurement money of $67 million.

General Dynamics Corp.'s winner is the shoulder-fired Stinger for Army and Marine Corps air defense. Its budget request triples to $150 million, as procurement goes into high gear with a proposed buy of nearly 2,700 missiles.

While Hughes Helicopters will continue developing the antitank Advanced Attack Helicopter with a modest RDT&E increase to $177 million and hope for a first Army buy in fiscal 1980, Bell Helicopter and Hughes will be funded at a requested $141 million for another 78 Cobra/Tow AH-1S for antitank duty, raising procurement to 243 systems since fiscal 1977. The biggest new Army helicopter buy is in the $377 million request for 129 of Sikorsky Aircraft's UH-60A Black Hawks for transporting infantry squads and for medical evacuation. The procurement would represent the first major order for Sikorsky, up sharply from this year's 56 choppers. Sikorsky may get another $183 million from the Navy for 14 CH-53E Sea Stallion heavy lift helicopters after a year-long gap since six were bought in fiscal 1977.

The Air Force wants fighters and ground-support planes that could be applied to the NATO mission, like Fairchild Industries Inc.'s heavily armed A-10 for close air support. Projected procurement of another 162 planes for $907 million will raise orders over three fiscal years to 406. Similarly, Defense Secretary Brown identifies the General Dynamics F-16 tactical fighter and the Marine Corps' A-4M Skyhawk by McDonnell Douglas as NATO-oriented to rationalize bigger buys next year. McDonnell's F-15 Eagle and the F-16 proved the big-money fighters in the aircraft budget, each with a procurement request near the $1.5 billion level.

Troubled aircraft programs sure to get close congressional review are the Navy's F-14A Tomcat by Grumman, which is being cut back to 24 planes instead of the 36 the service sought. Forty-four were ordered in

WEAPONS R&D FUNDS
(in millions of dollars)

	FY 1978	FY 1979	Contractor
ARMY			
Advanced Attack Helicopter (AAH)	$164.9	$177.4	Bell
Ballistic Missile Defense Technology	106.2	114.0	McDonnell
Hellfire, heliborne missile	50.5	65.1	
Patriot (SAM-D), surface-air	216.4	307.1	Raytheon
SSM, surface-surface missile	46.4	70.8	
Tri-Tac, joint tactical communications	105.7	98.7	GTE-Sylvania
NAVY			
V/STOL aircraft developments	22.5	52.5	Multiple
LAMPS ship helicopter	107.3	124.5	Multiple
AEGIS, surface-air	34.5	14.4	RCA
HARM, air-surface radiation	29.7	43.4	TI
Tomahawk, sub/air-launched missile	210.3	152.1	General Dynamics
Advanced ASW Torpedo	25.0	44.3	
ELF communications	15.0	40.5	
Wide Aperture Array Sonar	17.0	37.4	IBM
AIR FORCE			
E-4 AABNCP, command post	65.8	32.0	Boeing
Precision Location Strike System	31.4	86.8	
M-X, MIRVed ICBM	134.4	158.2	Boeing

Source: DOD

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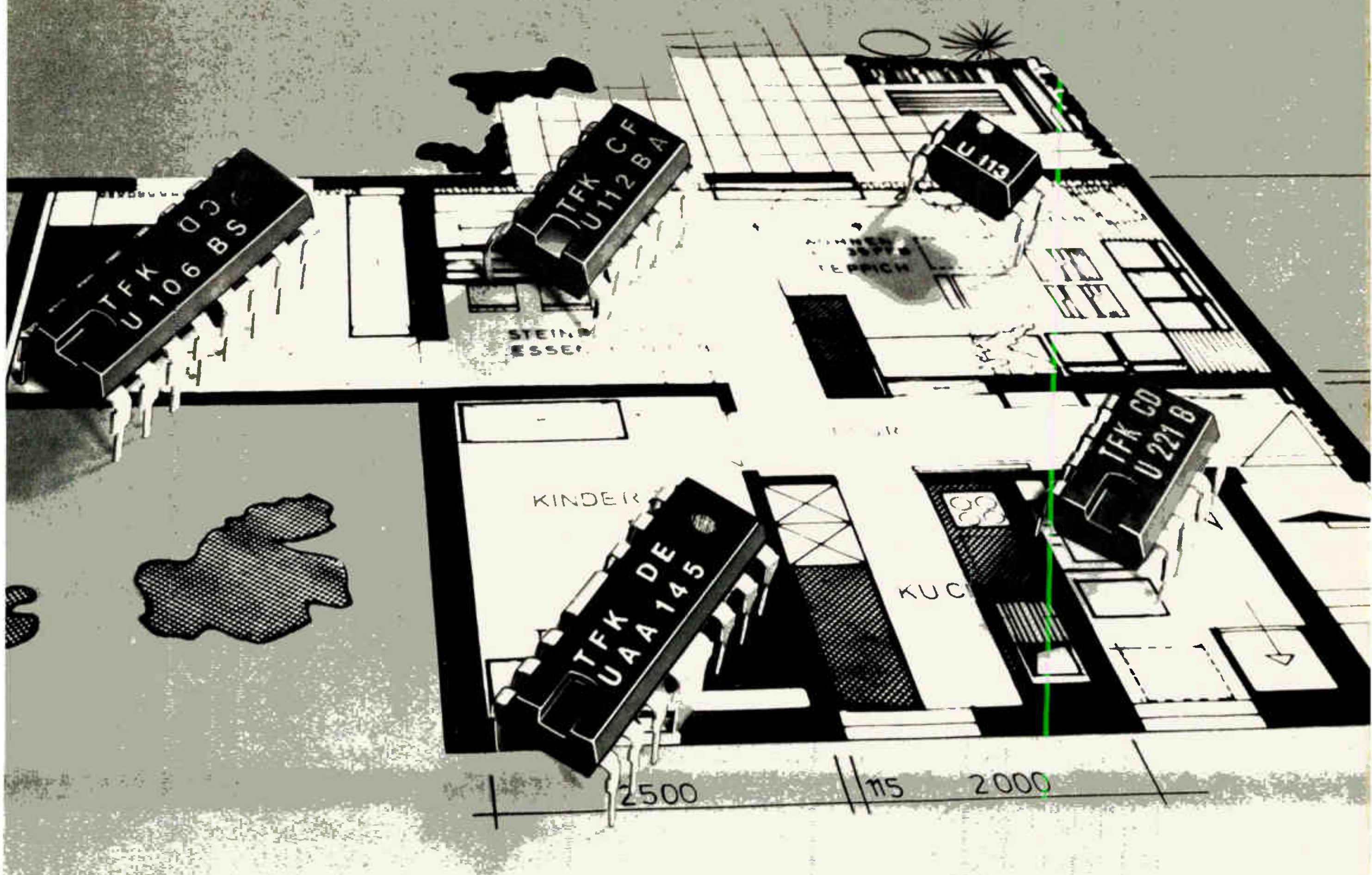

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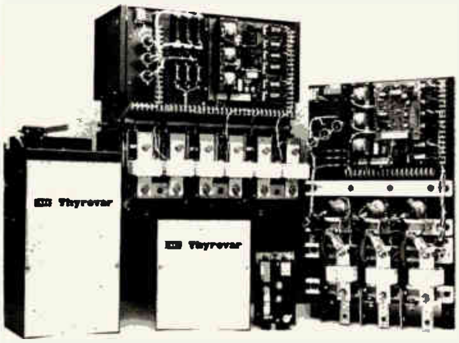

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Integrated electronics

Tests show spotty LSI record

Three-year program at JPL to find devices for use aboard unmanned spacecraft pinpoints chronic faults across spectrum

by Larry Waller, Los Angeles bureau manager

Users of microprocessors and other large-scale integrated circuits often take manufacturers' device specifications as a bedrock for system base design and testing. Then they get in deeper by assuming that parts from second sources are identical to the original.

The shakiness of such assumptions is highlighted by data from probably the most extensive test program on LSI devices ever compiled—a three-year effort at the Jet Propulsion Laboratory. At the facility in Pasadena, Calif., engineering managers are seeking to find and qualify standard LSI devices for unmanned spacecraft that demand far more reliability than earthbound applications. It has been a hard goal to meet.

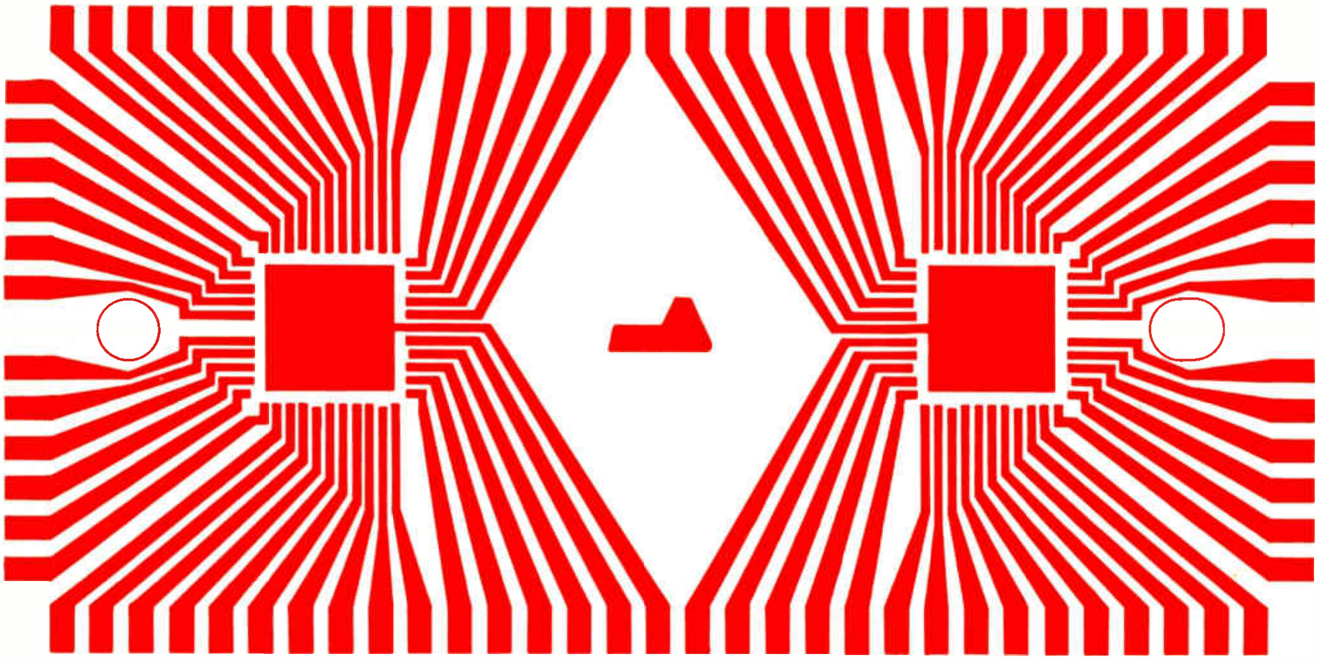
Difficult to test. "The first thing we noticed, "was the lack of testability of LSI," says W. Richard Scott, group supervisor of the electronic parts engineering section. Not only was the manufacturer not forthcoming with sufficient operating data for specifications to be verifiable, he says, but too few test pins were put on the device packages.

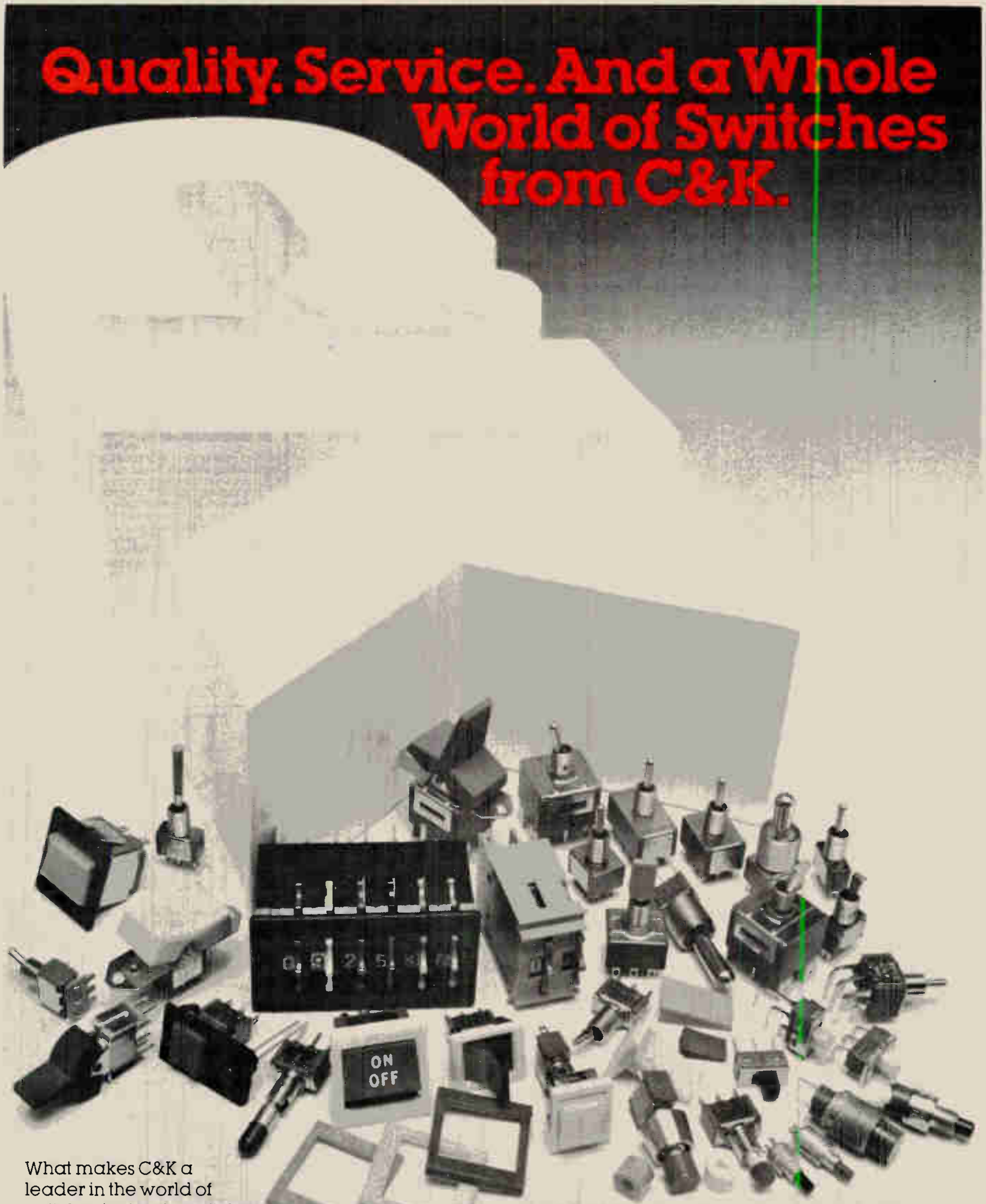
Such problems are the hallmark of "a volatile and immature technology where the manufacturer is more concerned with getting his product out the door than in nailing down all the specifications," Scott says. In the years since JPL started testing, "it's getting worse because they're crunching more and more performance on the chips, especially the peripherals," according to Larry Hess, LSI system task leader for JPL.

So to get a solid hold on which LSI devices come closest to space reliability standards, the laboratory put together what are probably the most exhaustive tests around, subcontracting much of the work out to major testing firms.

The Pasadena lab no longer tries to boil down space component reliability to a failure rate. It has given up on that approach as too simplistic. "Space reliability is definitely a factor of power dissipation and temperature," says Hess, and JPL looks for parts that perform best under broad requirements.

Tests take place at temperature extremes from −55°C to +125°C under virtually all possible power levels. The comprehensive scope of the tests is shown by the number of vectors, exercising all possible functional entities and instructions, for the 1802 and 8080 families: more than 40,000 and 12,000 respectively. Along the way, JPL narrowed its

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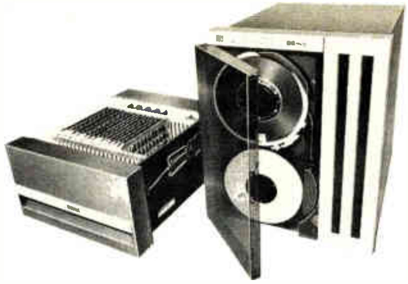

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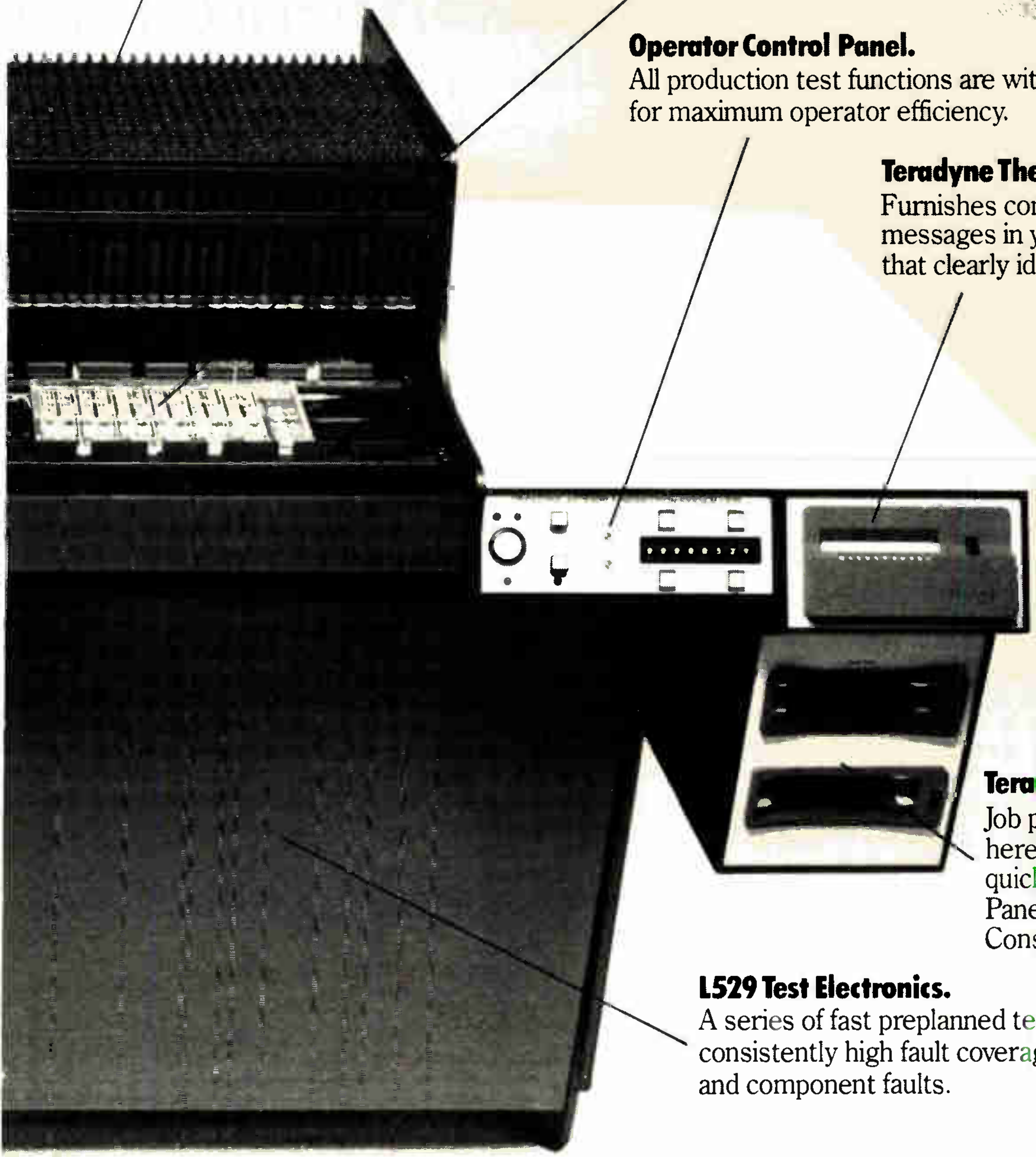

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Electronics abroad

Spain beset by economic woes

Sales of color TV sets to provide a bright spot as nation struggles to cut inflation rate to 15% a year from 30%

by Arthur Erikson, Managing Editor, International

It would not be surprising if Spain's President Alfonso Suárez felt like donning a suit of armor and riding off quixotically to joust with windmills instead of grappling with the country's economic problems. Not with current situation: prices are rising too fast, too many people are out of work, and much more money is being spent abroad for imports than is coming back in from exports. As if they were not enough, these economic troubles have come at a time when the country is feeling its way uncertainly toward democracy after Generalissimo Francisco Franco's long totalitarian reign.

Suárez has managed, nonetheless, to get reasonably wide backing for a broad stabilization plan aimed at first getting inflation under control, next cutting the trade deficit, and then after a couple of years, triggering an economic recovery. A main goal this year is to cut inflation, which was running at a rate of nearly 30% a year in December 1977, down to a 15% annual rate by December 1978.

The fledgling unions have agreed to limit their wage demands accordingly, a big plus. But there are so many uncertainties surronding the stabilization plan—known as the Pacto de la Moncloa—that the economy might very well go nowhere this year. Industrialists particularly are wary about new plant investments. Most have factories working below capacity, and "we still don't know what the rules of the game will be," says Juan Luengo Vallejo. He heads Piher Electronica SA, which makes what in Europe is known as professional electronics equipment—analytic and nuclear instrumentation, for example—and is part of the Piher group, best known as Spain's largest components producer. Although consumer spending except for automobiles should hold up fairly well, the real growth overall for the economy this year does not figure to go much over 1%.

Following the line. Electronics markets will essentially mirror the overall outlook. Mainly because of a solid hike in the consumer market, *Electronics'* survey pegs equipment sales, at factory prices, at $1.325 billion for the year ahead. That is 16% higher than the estimated $1.139 billion for 1977. But actually there is little real gain; the survey is carried out in current pesetas and the increase is thus mainly due to inflationary price rises. (Estimates in dollars are made at a conversion rate of $1 = 84 pesetas.)

Luckily, there is color television to carry the market. The other major equipment sectors—communications gear and computers—will not keep pace with the overall inflation rate. As for components sales, they will be pulled up by color TV, too, since practically all the color sets sold in Spain are made there.

Spain started color broadcasts well after her northern neighbors, and the penetration still is a low 10%. So the market continues to burgeon despite the precarious economic situation. Sets sell for something like $1,400 retail on the average, much higher than in other West European countries. But they have become a status symbol, and working-class people, as well as the well-heeled, are buying them.

Last year, Spanish set makers bounced their color TV output up by

SPANISH ELECTRONICS MARKETS FORECAST
(IN MILLIONS OF DOLLARS)

	1976	1977	1978
Total assembled equipment	892	1,139	1,325
Consumer electronics	366	547	671
Communications equipment	193	215	236
Computers and related hardware	184	209	235
Industrial electronics	58	66	72
Medical electronics	56	60	63
Test and measurement equipment	29	35	40
Power supplies	6	7	8
Total components	179	217	241
Passives	111	126	143
Semiconductors	24	29	31
Tubes	44	62	67

(Exchange rate: $1 = 84 pesetas)

Note: Estimates in this chart are consensus estimates of consumption of electronics equipment obtained from a survey made by *Electronics* magazine in September and October 1977. Domestic hardware is valued at factory sales prices and imports at landed costs.

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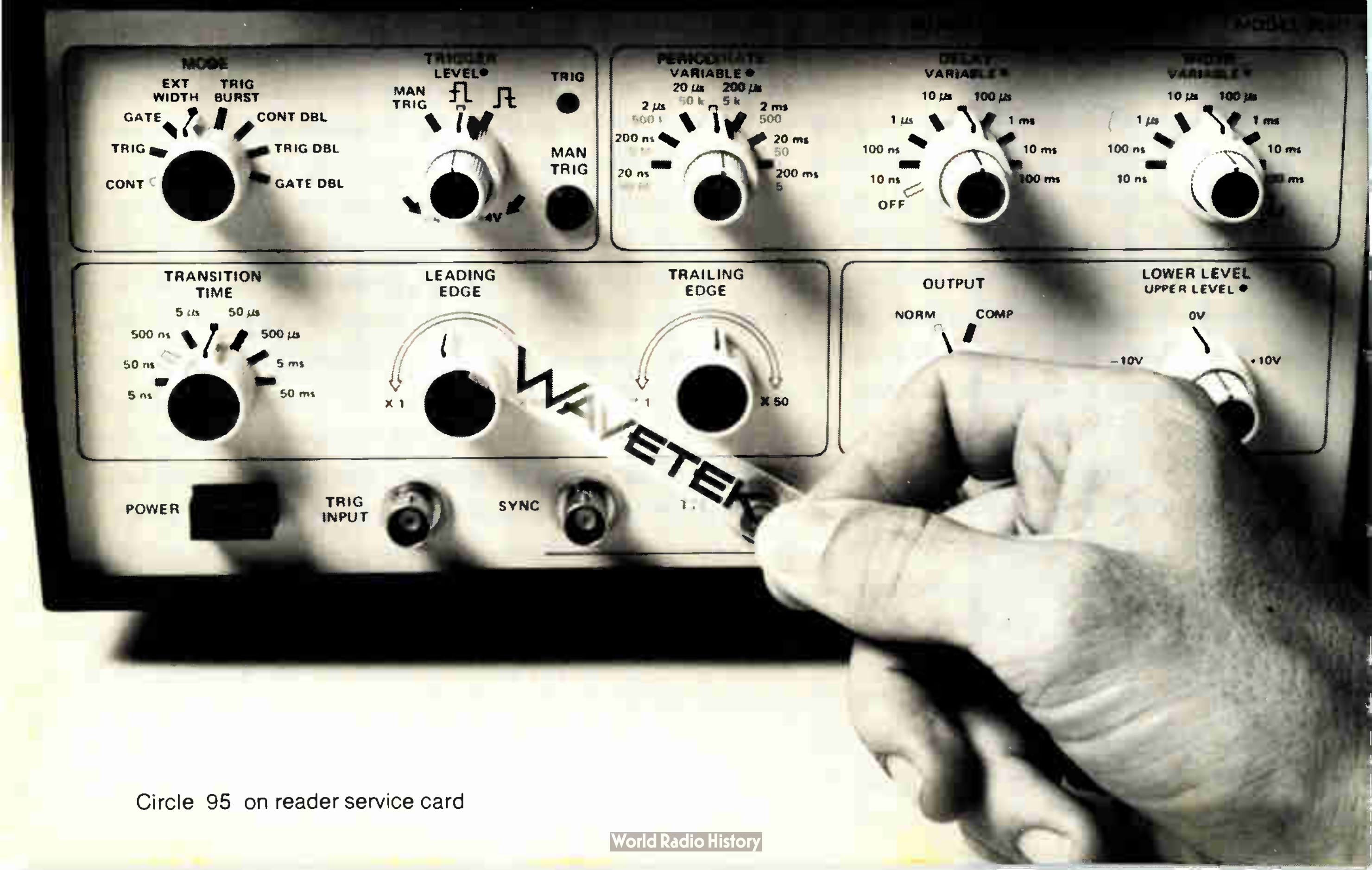


Circle 95 on reader service card

Compatibility cures growing pains of microcomputer family

by Michael Wiles, Fuad Musa, T. Frank Ritter, Joel Boney, and Tom Gunter
Motorola Inc., Semiconductor Products Division, Austin, Texas

☐ For designers of established microcomputer-based systems, this is the year when they can begin benefiting from very-large-scale circuit integration without having to endure revisions in any of the architectural concepts already familiar to them. Thanks to newly developed VLSI techniques, chip manufacturers can now partition their microcomputer designs into fewer, more powerful chips that maintain their kinship with the earlier integrated circuits. This approach lowers system costs and increases system efficiency without forcing engineers into that most dreaded of all computer design dilemmas—weighing the advantages of more advanced hardware against a major reinvestment in software and system design development.

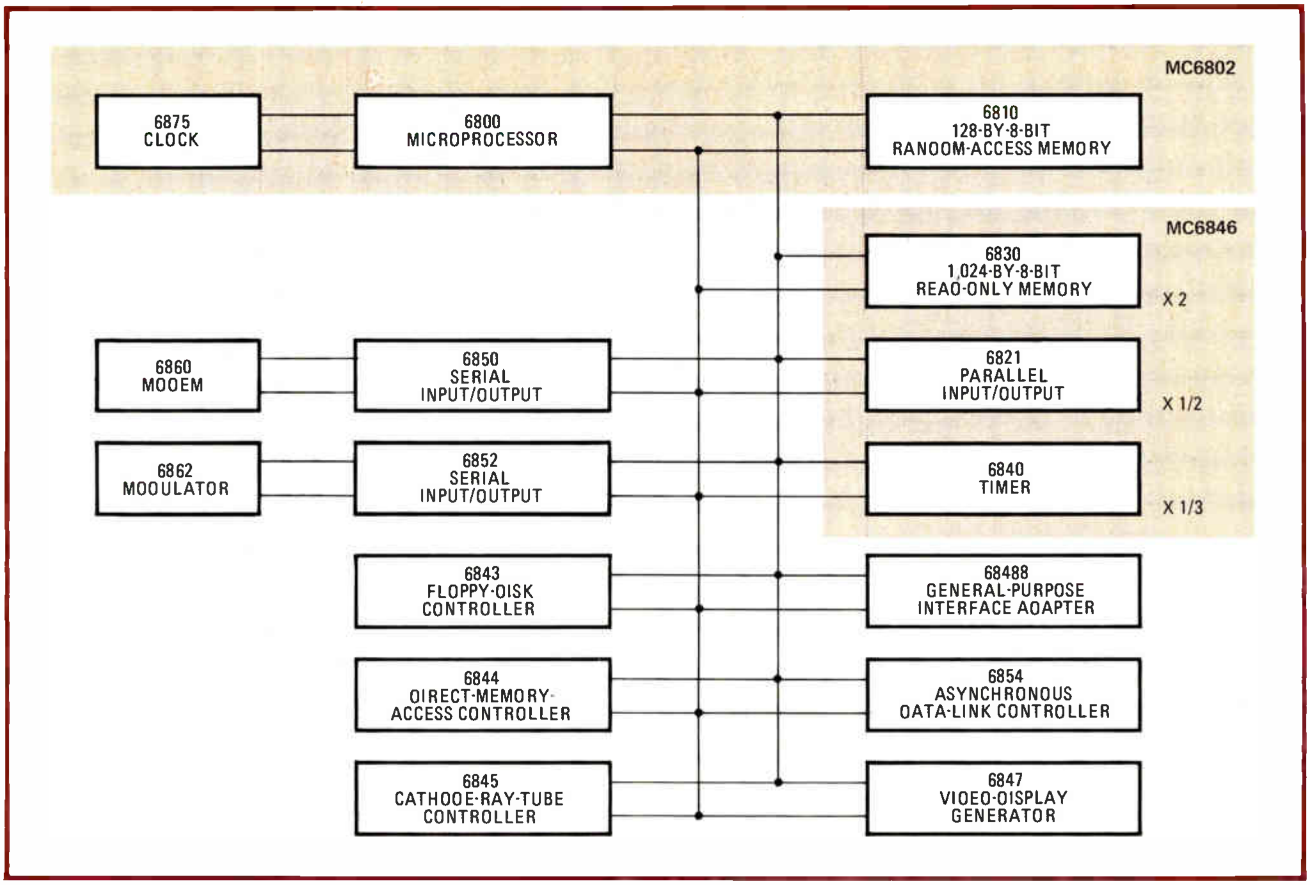
A case in point is a new line of software-compatible single- and minimum-chip 6800 microprocessors. These allow designers to upgrade their existing systems or move upward and downward throughout the applications spectrum with the same software and emulating firmware tools they have used for the basic application.

Already available is a two-chip 6802/6846 microcomputer set that combines the functions of all seven of the original 6800 family members (Fig. 1). As such, it can be used to reduce the cost and package count of any basic 6800 design. Like the original 6800, it is expandable almost without limit in input and output capability and to a maximum of 65 kilobytes of external memory. Moreover, it can address all 6800 peripheral chips directly over the two-chip system bus

A one-chip version

Coming at mid-year is a 6801 single-chip microcomputer that combines practically all the functions of the original seven-chip 6800 (Fig. 2). With central processing unit, random-access memory, read-only memory, timer, and input/output requirements all on one chip, it is intended as a powerful, stand-alone controller or, with one of the specialized 6800 peripherals added, as a powerful, two-chip controller system.

Also in the works is the high-performance 6809 CPU



1. Two equals seven. The two-chip 6802/6846 microcomputer combines the functions of the original 6800 family's seven members, but costs less. Processing power and design flexibility are about the same—external memory, for example, has the same 65-kilobyte maximum.

that extends the 6800 capability into 16-bit applications. The 6809 has more 8-bit (byte) handling efficiency than the 6800 while retaining software compatibility and adding 16-bit operations. By processing data over a 16-bit-wide internal bus and in 16-bit-wide registers and memory stacks, the 6809 increases throughput significantly for memory-intensive, interrupt-driven, minicomputer-like applications.

Indeed, the device will serve as a bridge from 8-bit 6800 system designs into the higher-performance 16-bit applications. Meanwhile, those users of 8-bit systems who require certain 16-bit facilities will not need to move to a completely different product.

A major advance

Finally, there is an advanced computer system called MACS, now at the design stage. A next-generation microcomputer family, it exploits the very-large-scale level of integration now emerging in metal-oxide-semiconductor processes and will be implemented in the high-density short-channel, silicon-gate MOS technology called H-MOS (for high-performance MOS). Throughput will be an order of magnitude greater than in current-generation microprocessors, and the user's software and hardware interfaces will be simplified. The architecture and structure of the MACS microprocessors will make them easy to expand and upgrade as higher-density technologies become available from electron-beam technology in the second generation of VLSI circuits.

The MACS design has a 16-bit data bus architecture and incorporates full 16-bit instruction word capability for still higher throughput. A 24-bit address space provides for memory capacities to 16 megabytes, which allow users to make optimum use of the soon-to-arrive 65,536-bit memory components. Its architecture will also permit MACS to be built into multiple- and distributed-processor systems.

The two-chip machine

To begin at the beginning, the 6802/6846 two-chip system is a low-cost replacement for the 6800 in standard multichip designs. Together, the two chips supply all the power of the 6800 CPU, plus 128 bytes of RAM for real-time scratch-pad operations, 2,048 bytes of ROM for program storage, 10 parallel I/O lines for controlling peripherals and machinery linked to the system, and a 16-bit programmable timer with three control lines for synchronous control of all external circuits. Moreover, since the 6802 has been designed to keep the split address and data bus of the 6800, no external multiplexed interfacing or buffering is needed between it and any peripherals or memories.

The 6802 microprocessor is the heart of the two-chip microcomputer (Fig. 3). It contains the 8-bit 6800 CPU and thus is fully software-compatible with the 6800 microprocessor. Moreover, since the 128 bytes of RAM on the 6802 are at the usual location, hexadecimal address 0000 to 007F, the 6802 can use the same address code as

The 6801: more instructions for less

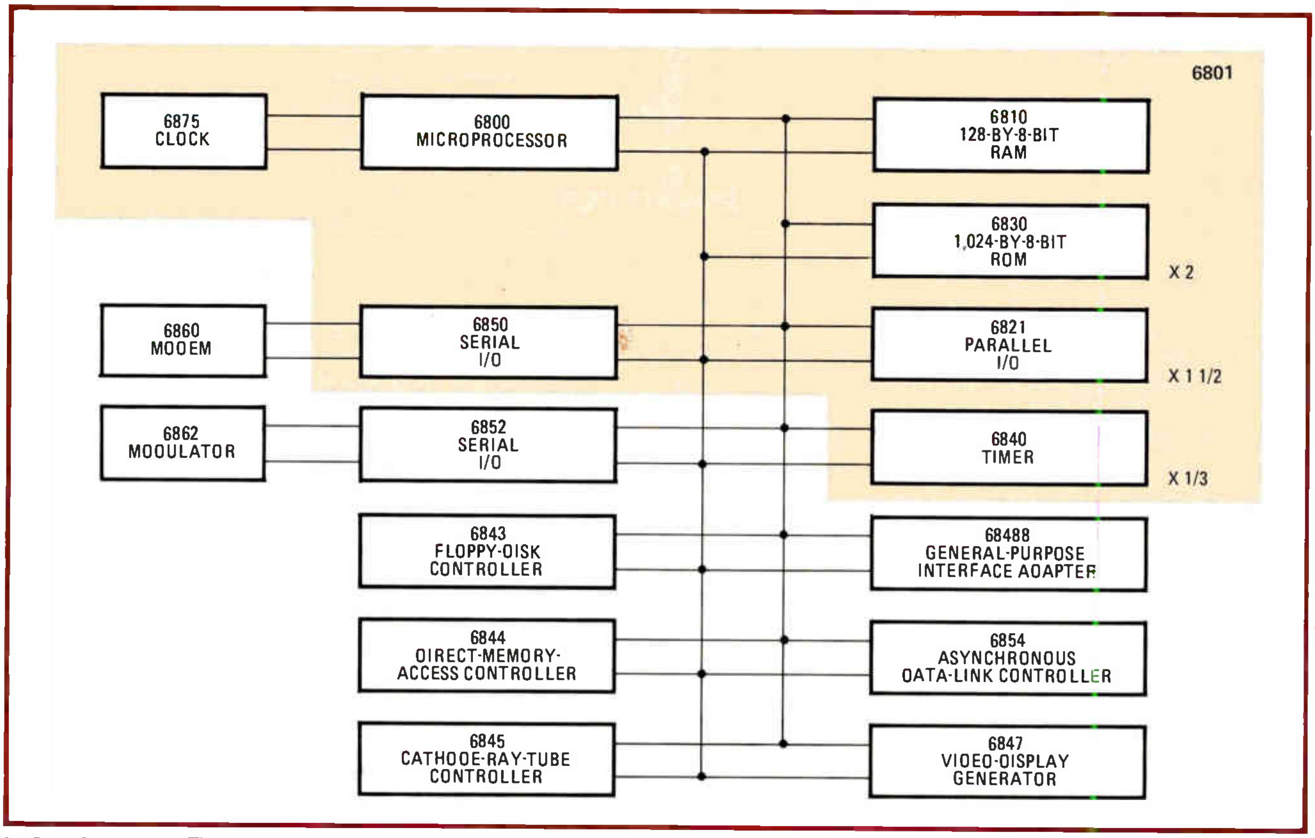
The 6801 is intended to reduce the cost of a 6800 system. The instruction set is both source- and object-compatible with current 6800s. This means current 6800 programs will run on the 6801 without modification. Furthermore, the 6801 has an improved internal architecture that contains 10 new instructions and shortens the execution cycle times of many existing instructions. This was done by basing the core of the 6801's design on that of the advanced 6809 8-bit processor. The instruction set of the 6801 is therefore a superset of the 6800 and a subset of the 6809.

Additions to the 6801 include its six 16-bit operations: load the double accumulator; store the double accumulator; add 16 bits to the double accumulator; subtract 16 bits from the double accumulator; and shift the double accumulator right or left.

Three other new operations manipulate the index (X) register: push X register onto stack; pull X register from stack; and add B accumulator to X register. The push and pull of the index register enhances the 6801's ability to handle position-independent and reentrant code, as well as allowing quick temporary storage of the index register. (The existing instruction to compare index register was also modified to properly set all the condition code bits.) The instruction to add accumulator B to X gives the 6801 the much-needed ability to modify the execution time of addresses in the index register.

The last new instruction on the 6801 is an 8-by-8-bit unsigned multiply that yields a 16-bit result in 10 microseconds. This instruction is 20 times faster than an implementation in software for the basic 6800. The multiply instruction, along with the one for adding accumulator B to the index register, makes real-time table lookup and interpolation go three to four times faster than before.

The programming model for the 6801 is identical to the 6800's, although internally another temporary register and a 16-bit bus were added. These changes not only allow the 10 new instructions to be added but also assure that practically all instructions may be executed in fewer machine cycles on the 6801 than on the 6800.

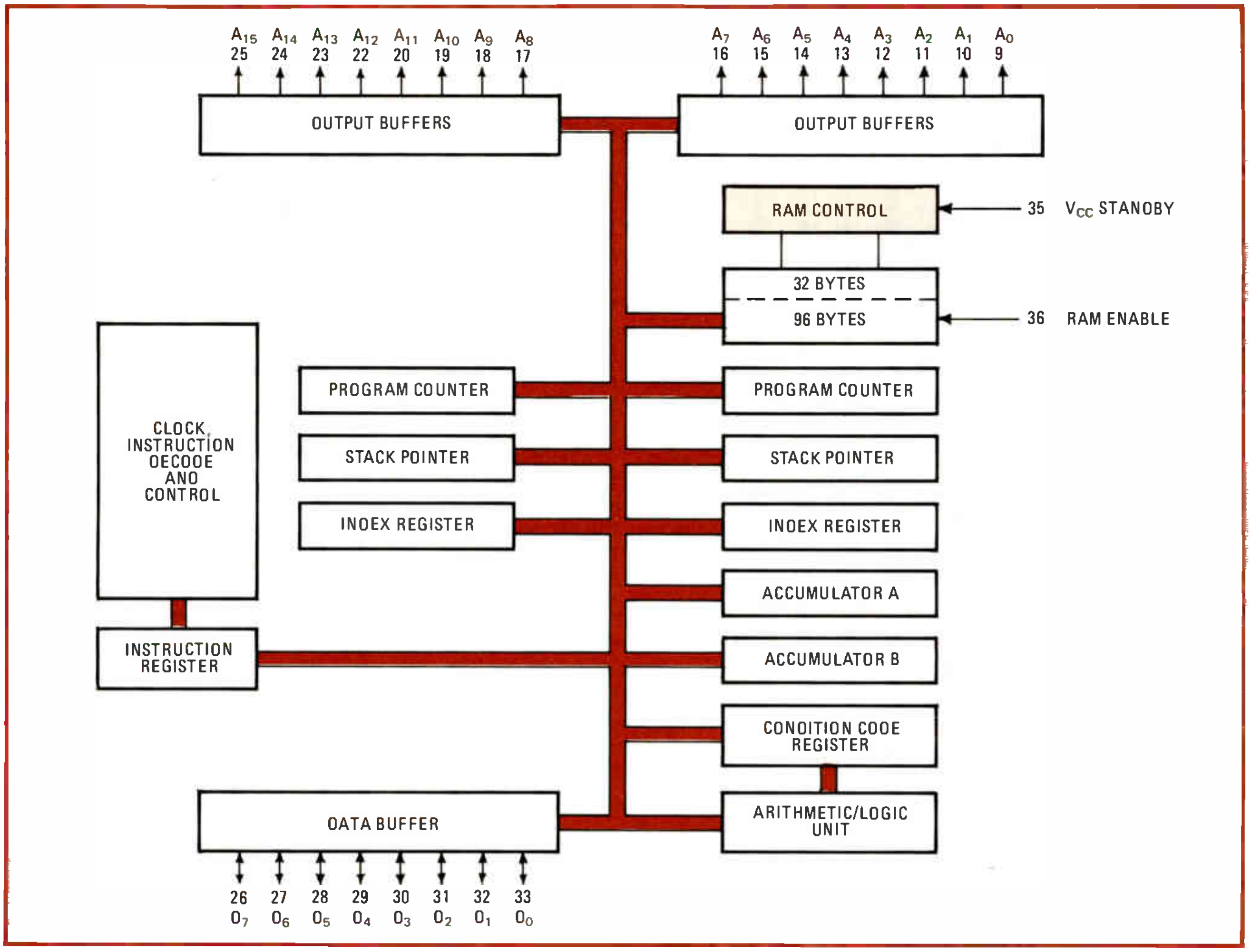


2. One for many. The soon-to-be-available 6801 single-chip microcomputer has all the basic 6800 family functions and even contains instruction enhancements for when it is being used as a stand-alone controller. It can be expanded with standard 6800 peripheral chips.

the 6800—a distinct convenience for designers.

A power-down RAM feature is new. Thirty-two bytes of memory, located at the addresses 0000 to 001F, may be retained in a standby mode if a 5-volt battery is tied to the V_{CC} pin as a standby power supply. Portions of critical data can therefore be retained during power loss, making the 6802 useful in many remote or point-of-sale terminals. In this standby mode, the worst-case current drain on the chip is only 8 milliamperes at 5.25 volts, or less than 50 milliwatts, giving a battery drain life of about 24 hours.

All that is needed to control the RAM is a RAM-enable input signal compatible with transistor-transistor logic. In the high state, this signal enables the on-chip memory to respond to CPU controls. In the low state, it disables the RAM, allowing a designer to select any external RAM



3. The same but better. In the two-chip system, the 6802 processor chip contains the 8-bit 6800 central processing unit plus 128 bytes of random-access memory, 32 bytes of which can be retained in a standby mode. The RAM uses the same address spaces as on the 6800.

at the same memory address. Moreover, this same RAM-enable signal may also be used to disable reading or writing operations of the RAM during a power-up or power-down sequence. Additionally, op code can be executed directly from the RAM.

In expanded systems, a designer uses the memory-ready signal, which stretches the ϕ_2 clock so that the 6802 can interface directly with the low-cost, slow-speed memories contained in most peripheral equipment. When the memory-ready signal is low, the E signal (a system clocking signal equivalent to phase ϕ_2 on the 6800) is stretched to integral multiples of half periods.

The other half

The companion part to the 6802 is the 6846 combination ROM, I/O, and timer. It contains 2 kilobytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable counter-timer. The parallel-I/O port is similar in function and operation to the B port on the 6821 peripheral interface adapter. It includes eight bidirectional data lines and two handshake control signals. The control and operation of these lines are fully software-programmable.

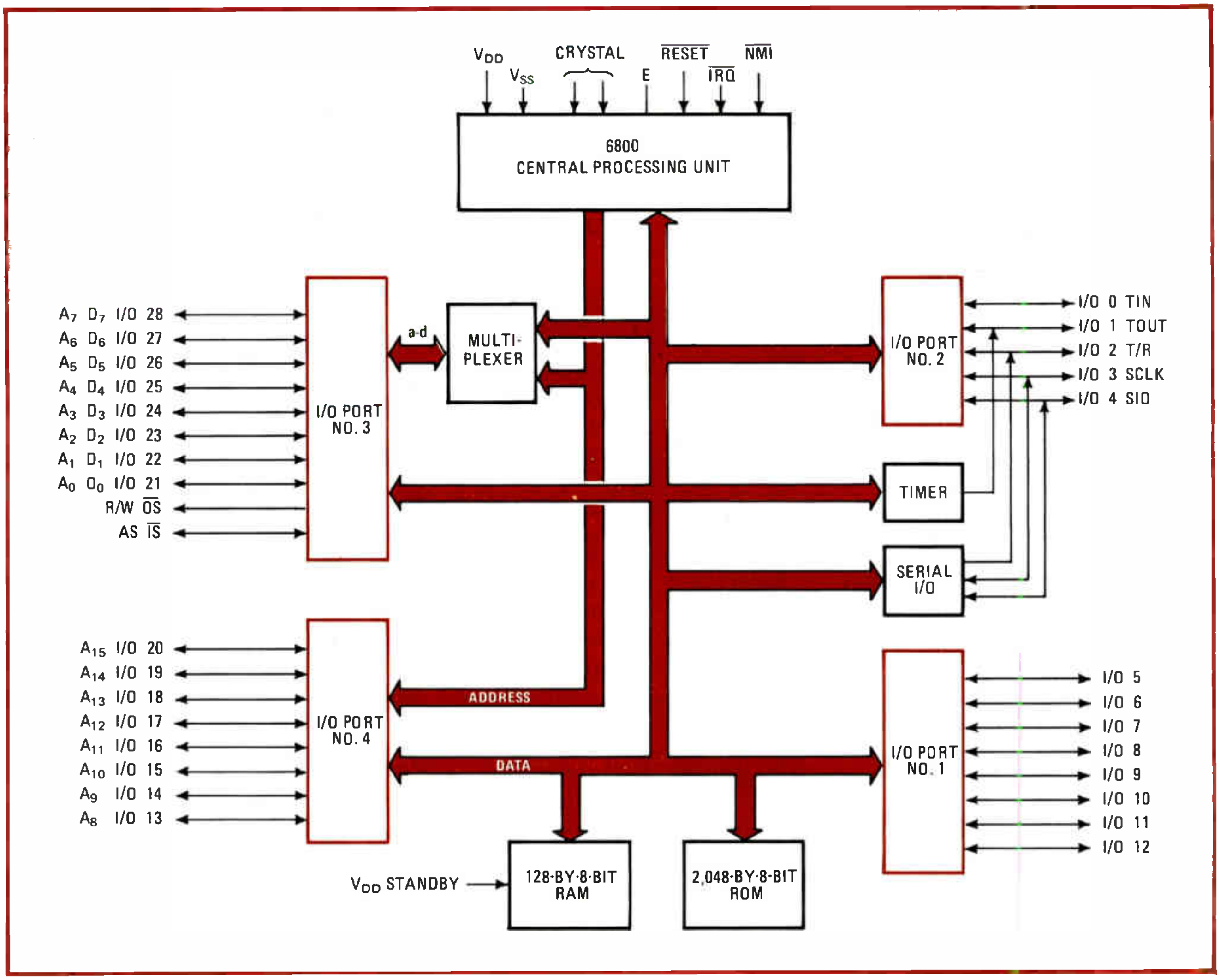
The 6846 counter-timer may be programmed in software to count events and measure frequencies and time intervals. It may also be used to generate square waves, single pulses of a controlled duration, and gated delay signals. Interrupts may be generated from a number of conditions selectable by software means.

The one-chip solution

The 6801 is a third-generation single-chip microcomputer system (Fig. 4). It contains an improved 6800 CPU, 2 kilobytes of ROM, 128 bytes of RAM, three 16-bit timer functions, a serial input/output port for controlling communication interface equipment and multiprocessor applications, and 31 parallel, programmable input/output lines for managing peripherals.

The 6801 retains architectural integrity with the 6800 family, so that it is easily expandable with existing 6800 peripherals. This is evident from the map of its memory (Fig. 5), which contains enough address space (65,536 bytes) to make this single chip compatible with even the most memory-intensive 6800 designs.

In the map, the 2 kilobytes of on-chip ROM are allocated to the top 2 kilobytes of memory from hexadecimal address F800 to FFFF. This space also includes the interrupt and restart vectors from location FFF0 to FFFF. The on-chip 128-byte RAM is located in the direct page at addresses 0080 to 00FF, while the on-chip I/O is



4. It stands alone. The 6801 one-chip microcomputer contains an enhanced 6800 CPU, 2 kilobytes of program memory, 128 bytes of data RAM, and three 16-bit timer functions. It is equipped with one serial input/output port and 31 parallel programmable I/O lines.

allocated to the first 18 locations. The rest of the memory space may be used for memory or expanded I/O.

As in the 6802, the clock for the single-chip unit is supplied by an internal oscillator, which may either be driven by a TTL-compatible clock source external to the 6801 or be controlled by a crystal. A divide-by-four circuit makes it possible to use an inexpensive 4-megahertz crystal.

This oscillator also supplies the clock (the E signal on Fig. 4) for the rest of the system. This clock is used for data synchronization and clocking of devices that may appear on the external bus. In expanded, multiplexed modes of operation, an address strobe samples the address at the proper time, preventing any conflict between address and data on the multiplexed pins.

Simple reset

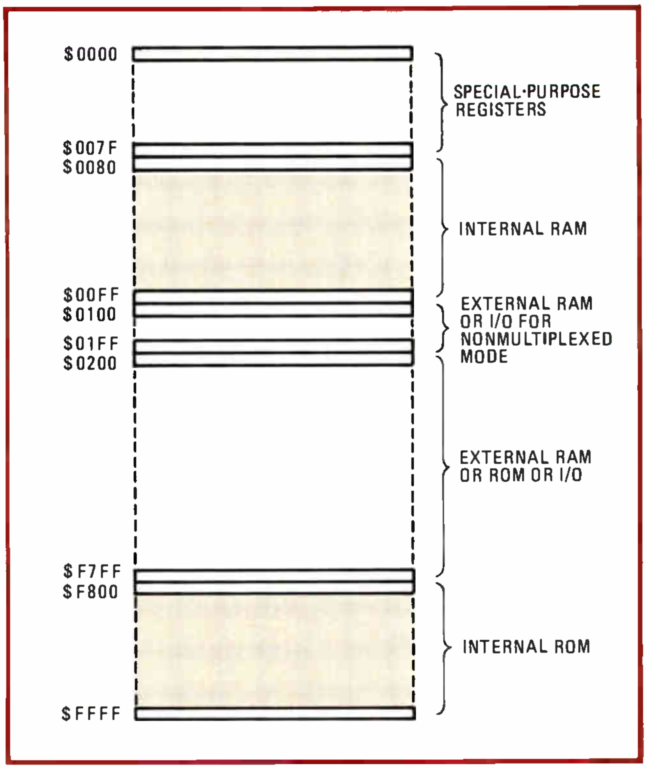
A reset input resets and restarts the 6801 after the kind of power-down condition that results from a power failure. A Schmitt trigger in the reset circuitry guarantees its proper operation even in a high-noise environment or with signals having slow rise and fall times. The designer need use only a simple RC pull-up on the reset pin, which the peripheral devices can also use—no costly external reset logic is necessary.

The 6801 can also cut design costs and boost performance by virtue of its powerful interrupt capability, which eliminates the need for multiprocessors and in some cases high-speed external logic to accommodate real-time interrupts. The chip's eight interrupt levels are serviced through the interrupt-request lines on the CPU.

Interrupt ability

One interrupt level is under software control, being generated by addresses FFFA and FFFB in the ROM memory map. The other seven are hardware interrupts. The nonmaskable interrupt (NMI) has system priority and can be used to initiate critical operations, such as danger signals or must-do operations. Only when its level returns to normal after being in service can other interrupt routines be accommodated.

Another of the 6801's assets is its I/O capability. For stand-alone applications there are 31 parallel I/O lines available. These are arranged in four ports (Fig. 4). The first port consists of five I/O lines that can mix inputs and outputs in any combination under software control. The



5. Big memory. The 6801 retains the basic architecture of the 6800 family. The memory, as the map of it shows, contains enough address space for even the most memory-intensive 6800 designs. A full 65 kilobytes of external memory can be addressed.

serial-I/O and timer-I/O data may also be programmed to be active on this port.

The designer has three 16-bit timer functions available, one to control inputs, one to control outputs, and one to serve as a 16-bit overflow. All functions are performed with the aid of a 16-bit free-running counter that may be read by the 6801 CPU. In the case of inputs, this setup plus a bit-level edge detector allows the designer to measure the input pulse widths used in critical timing operations between processors. Each time the detector detects an edge, the count from the counter is read into an input-capture register on the 6801 for use by the 6801 CPU in computing the pulse width. The input-edge detector may also generate an interrupt that will signal the microprocessor that new data is available.

The serial-I/O port included in the 6801 is intended for I/O expansion and serial communication. As Fig. 6 shows, it can communicate with simple serial-I/O devices, such as shift register latches and other readily available 16-pin I/O devices. In essence, the port is a very low-cost interface for the addition of peripherals not needing high data rates, since in this mode the data is synchronously clocked into peripherals.

The two remaining I/O ports handle eight lines each. Both are general-purpose 8-bit data entries under control of a data direction register in the 6801 CPU. The third port can in addition be used to perform special functions, under the control of an input strobe (IS_3) that strobes data into its latch port. It may also generate an output strobe (OS_3), which can then load data into an external device. This can do the useful job of providing a handshake capability between processors and peripherals.

The 6801 has a wide variety of operating modes. It can stand alone as a one-chip controller, or it can serve as a central processor controlling 6800-type memory and peripheral devices. Or it can communicate with a number of other 6801s under the control of a central 6800 series CPU.

Using the 6801

In the expanded peripheral mode, the 6801's third and fourth I/O ports bring out the chip's data bus and a subset of the address bus. Since the buses are not multiplexed, they are wholly compatible with the nonmultiplexed 6800 bus system and may be directly attached to 6800 family peripheral and memory ports. They are simply inserted into the available address space. For example, Fig. 7 shows a 68488 general-purpose interface adapter and a 6821 peripheral interface adapter being directly interfaced to the 6801 operating in this mode.

When used in the expanded memory and peripheral mode, the 6801 multiplexes its 8-bit bus's address lines A_0–A_7 with data lines D_0–D_7 (see Fig. 4 again). These lines are brought out of the third I/O port, while the fourth I/O port provides address lines A_8–A_{15}. The first and second ports can still be used for I/O functions. Thus, at the expense of some I/O capability, the designer has all 65 kilobytes of address space available to him, except for those sections that are occupied by internal functions. And with the addition of an 8-bit latch, he may address standard family peripherals and memory devices for expanding the system.

For multiprocessor applications, the 6801 architecture allows operation in a number of modes: programmable peripheral control, handshaking, and serial. Each mode lets the processors communicate at a different speed and has different advantages and disadvantages, depending on the hardware configuration.

In a multiprocessor programmable peripheral controller, for example, the 6801 interconnects directly to any 6800 CPU (6800, 6809, or 6802) or to another 6801 bus simply as a peripheral device. Here the 6801 acts as a slave, communicating through the third I/O port on the master processor bus. Through this port, the processors can be made to talk to each other, as well as use the interrupt structure of each processor for handshaking. The other peripheral I/O ports (the first, second, and fourth) are available for peripheral control functions.

Two 6801s handshaking

In the multiprocessor handshaking mode, two independent 6801s may communicate over the 8-bit bus from the third I/O port. The input strobe (IS_3) and output strobe (OS_3) may be used for handshake control. Since this port is the only one used for this mode, the other 21 I/O lines are still available for local control functions, along with the interrupt request and NMI interrupts.

Finally, in the multiprocessor serial mode, a number of 6801s may communicate with each other over a single-wire serial I/O, with one processor being the master and the rest being slaves (Fig. 8). Since the serial I/O is handled with hardware shift registers on the 6801 chip, it is possible to achieve data transfer rates of 125 kilobaud between processors. This is the fastest 6801 multiprocessor mode and makes the most efficient use of the 6801's general-purpose I/O pins in the first, second, and third I/O ports.

When linked in this way, the 6801 locations may be physically remote from each other, and the number of locations is limited only by the minimum data transfer rate required for a particular application.

The 6809 bridge to 16 bits

For byte-oriented systems that need more performance for memory-associated operations than is offered by 6800 or 6802 processors, there is the 6809. It retains source compatibility with all 6800 programs, but it includes a number of 16-bit operations and some powerful new addressing modes for more efficient accessing of memory.

The 6809 design places special emphasis on the software needs of a microcomputer system. Among other modern software methods that it exploits, the trend towards modular programming has been explicitly recognized. A major ingredient in this is the use of subroutines, with their crucial need to be able to pass arguments to and from each other. It is of course essential to make these modules re-entrant—usable by interrupting parts of a real-time system—or recursive—each capable of calling itself, a common technique for evaluating expressions.

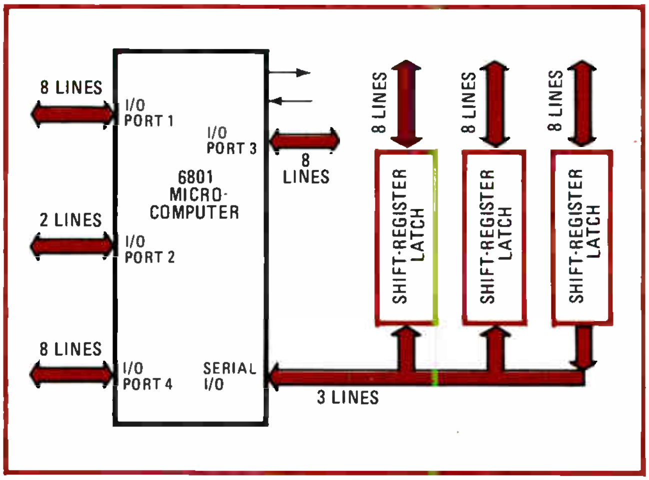
In addition, the 6809 has specific facilities for stack operations of the kind that allow temporary storage and parameters to exist on the stack without the need for absolute memory references. Also facilitated is the use of modern high-level languages, especially those block-structured languages with nested scopes.

The 6809 gives the user the best of the 8- and 16-bit worlds. It performs 8-bit operations more efficiently than 6800 processors, and it also speeds up memory-intensive data processing operations.

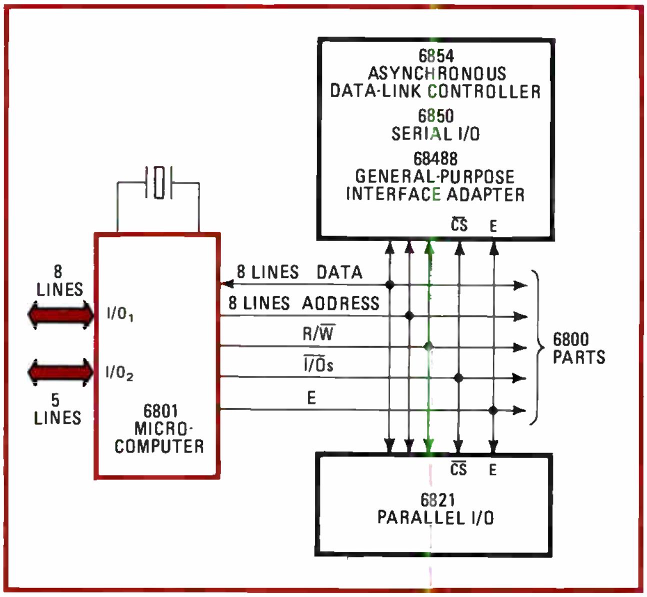
The architecture of the 6809 gives it this dual 8- and 16-bit capability. The chip contains four 8-bit-wide registers and five 16-bit-wide registers (Fig. 9). The 8-bit registers are the A and B accumulators, the condition code register, and the direct page register. The 8-bit accumulators are used for routine computation and byte-oriented data manipulations, such as editing, interpreting, compiling, and so on, and they make the chip better at handling byte-oriented operations than today's 16-bit-only central processing units. The two 8-bit accumulators can also form one 16-bit accumulator for double-byte operations. Meanwhile, registers associated with memory-referenced operations—the X and Y index registers, the user stack pointer, and hardware stack pointer—are all 16 bits wide.

Table 1 lists the greatly expanded indexed addressing modes available in the 6809, which include such sophisticated operations as long relative branches, program-counter relative addressing, and indirection. The auto increment and decrement modes give a programmer easy access to tabular data or to data buffers.

The 6809's instruction set contains about the same number of assembly-language instructions as the 6800 CPU, yet manages to be much more powerful. Combining



6. Serial control. The 6801's serial-I/O port s intended for communicating with simple, 16-pin I/O devices, such as shift registers and latches. It serves as a very-low-cost interface with low-speed peripherals in communications and multiprocessor applications.

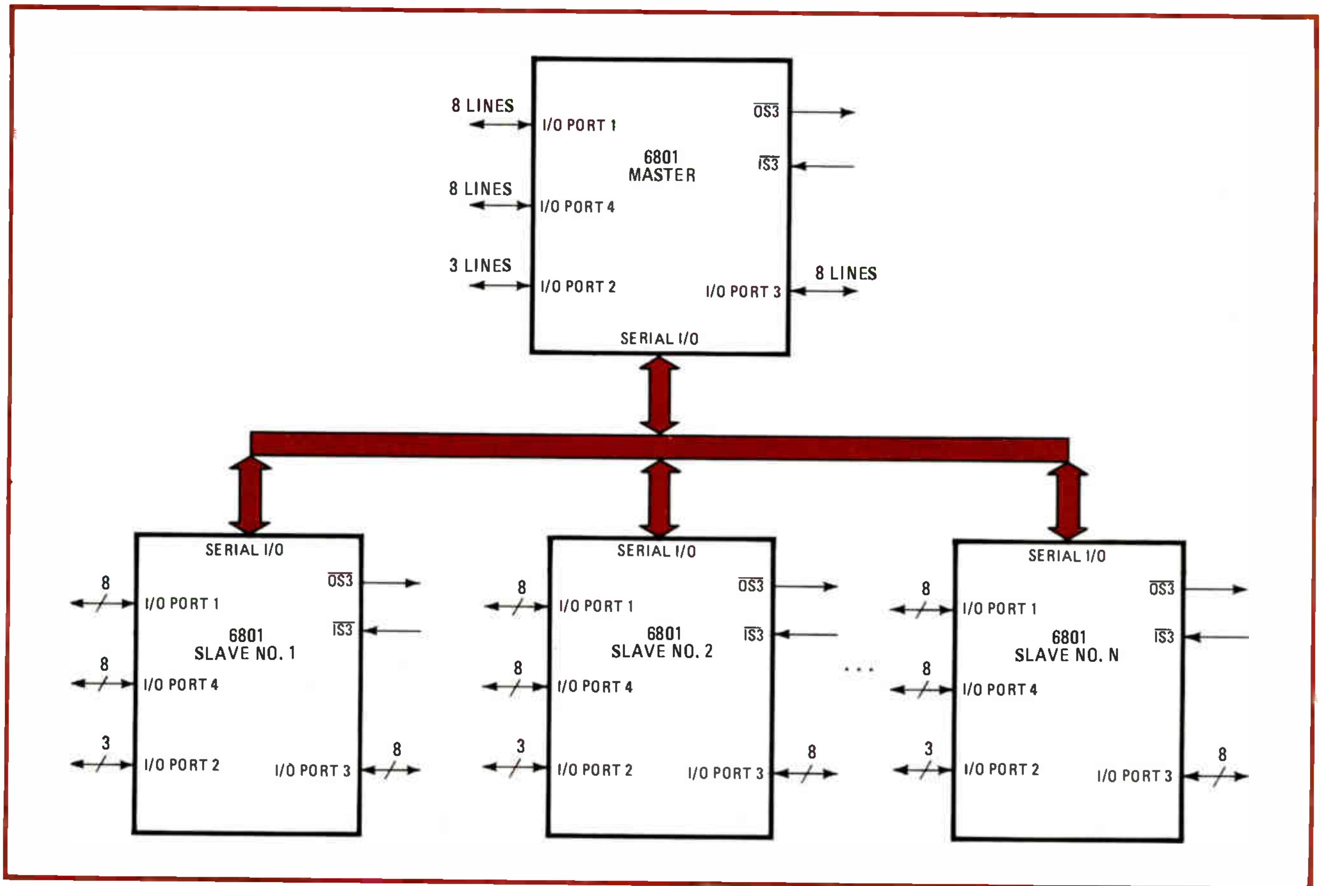


7. Expansion. When the 6801 is operating in the expanded peripheral mode, its third and fourth I/O ports make its data bus and a subset of its address bus available to control 6800 peripheral and memory devices. Here the chip is controlling interface adapters.

existing 6800 instructions into more general and versatile 6809 instructions has made room for many new ones, including many 16-bit instructions (Table 2).

Some of the 16-bit instructions manipulate data in the two accumulators, and others manipulate addresses in the index registers/stack pointers. Of special interest to designers are:

- The load-effective-address instruction, which, for example, allows a programmer to add immediate values or an accumulator to an index register.
- The full set of long branches, capable of reaching any location in memory.
- The presence of high-speed instructions, which push or pull a selectable set of registers. These faciliate argument passage to and from subroutines and allow subroutines to save a set of registers at invocation and restore



8. Multiprocessing setups. The 6801 chips can communicate with each other over single-wire I/O lines, with one chip acting as the master and the others acting as slaves. In this scheme, data can be transferred between the different processors at the rate of 125 kilobauds.

the same set before exit.

- Two new instructions—transfer and exchange—that give the processor greater flexibility and consistency by allowing any register to be transferred or to be exchanged with any like-sized register.
- An unsigned 8-bit-by-8-bit multiply with a 16-bit product. It is unsigned to ease the generation of multi-precision products. In addition to its use for numerical calculations, the multiply helps in calculating array subscripts for programs in a high-level language.
- Sophisticated data movement and block comparisons that can be carried out by using the auto increment and decrement addressing modes in conjunction with memory reference instructions.
- The sync instruction for high-speed synchronization of hardware and software. It stops the processor and lets it start up again only when one of the interrupt lines is pulled low. In this way, the instruction provides a mechanism for synchronizing software with hardware external to the CPU without the delays associated with interrupts or busy-wait loops.

Using the 6809

Operation of the 6809 will be very familiar to users of the 6800 in both hardware and software. Relatively few new hardware signals are needed, and all the old signals (address bus, data bus, R/W$\bar{Q}$, etc.) will be on the same pins as on 6800 or 6802 CPUs. As on the 6802, the 6809 has pins to connect to external crystals and phase output controls for system timing. There is also a ready input signal for slow memory and multiprocessor management.

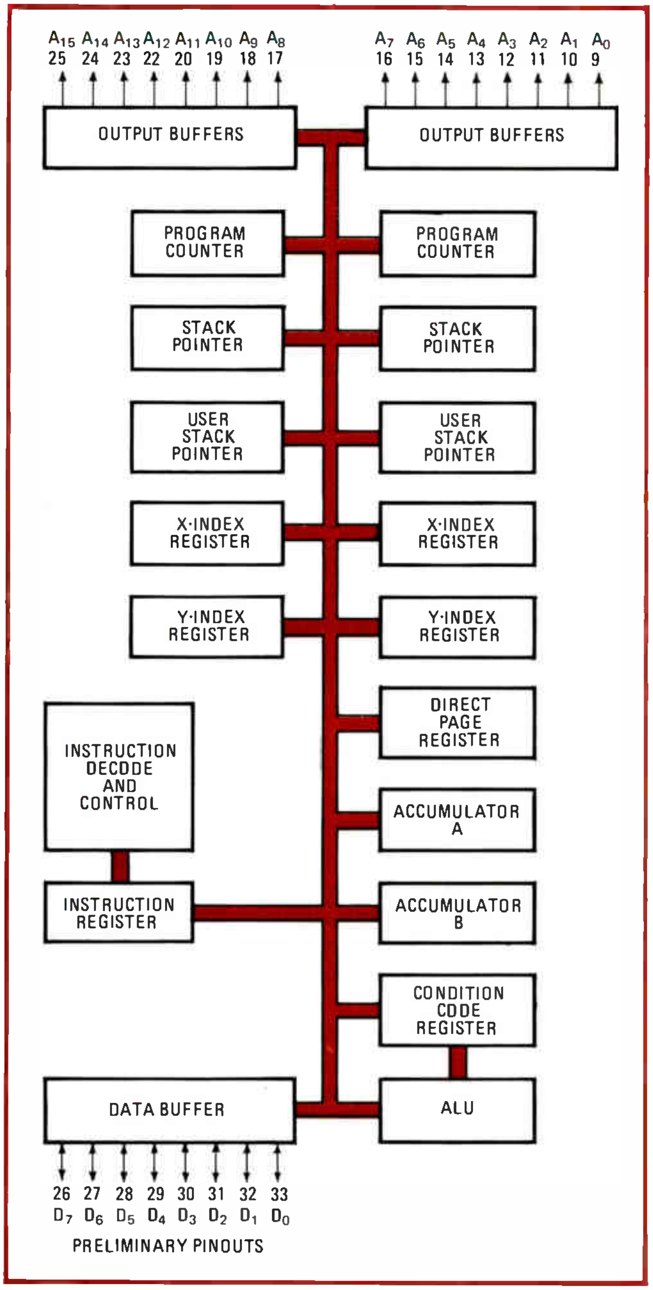
Moreover, a busy signal is made available during read-modify-write operations for disabling other processors in multiprocessor system configurations. This busy signal, which allows system hardware exclusion from the start of the read cycle through the associated write interval, assures that updated data will be processed throughout the system.

The future: systems on silicon

The essence of the microcomputer revolution is that it squeezes ever more complex systems onto silicon. Putting just a simple central processor on a chip is no longer good enough. Today entire microcomputers, like the 6801, are being shoe-horned into just one chip, along with external-world I/O, system protocols, and system software. Tomorrow, very-large-scale integration will make its full impact felt in the next generation of microcomputer products.

The MACS system design takes explicit advantage of VLSI MOS processes to resolve the shortcomings of current microprocessors and microcomputers. Indeed, it is believed that the systems foundation laid down by MACS should endure through the 1980s.

As stated earlier, the MACS system will use a 16-bit data bus architecture and a 16-bit instruction word for higher throughput. The 24-bit address space will provide for memory capacities to 16 megabytes, to take advan-



9. Bridge to 16 bits. The 6809 gives the user 8- and 16-bit word capability, while retaining software compatiblity with the basic 6800 family. Four 8-bit-wide registers and five 16-bit-wide ones process the data, with the 8-bit accumulators supplying routine computation.

TABLE 1: 6809 INDEX ADDRESSING MODES

Mode	Effective address (EA)	Description
,R	EA = R	Indexed with zero offset
[O,R]	EA = [R]	Indexed with zero offset indirect
,R+	EA = R;R+1 → R	Auto increment by 1
,R++	EA = R;R+2 → R	Auto increment by 2
[,R++]	EA = [R];R+2 → R	Auto increment by 2 indirect
,−R	R−1 → R;EA=R	Auto decrement by 1
,−−R	R−2 → R;EA=R	Auto decrement by 2
[,−−R]	R−2 → R;EA=[R]	Auto decrement by 2 indirect
N,R	EA = R+N	Indexed with signed N as offset (N = 5,8, or 16 bits)
[N,R]	EA + [R+N]	Indexed with signed N as offset indirect (N = 5,8, or 16 bits)
A,R	EA = R+A	Indexed with signed accumulator A as offset
[A,R]	EA = [R+A]	Indexed with signed accumulator A as offset indirect
B,R	EA = R+B	Indexed with signed accumulator B as offset
[B,R]	EA = [R+B]	Indexed with signed accumulator B as offset indirect
D,R	EA = R+D	Indexed with accumulator D as offset
[D,R]	EA = [R+D]	Indexed with accumulator D as offset indirect

R = X,Y,U, or S register

TABLE 2: THE 6809's 16-BIT INSTRUCTIONS

Instruction	Description
ADDD	Add memory to D accumulator
SUBD	Subtract memory from D accumulator
LDD	Load D accumulator from memory
STD	Store D accumulator to memory
CMPD	Compare D accumulator with memory
LDX, LDY, LDS, LDU	Load pointer register from memory
STX, STY, STS, STU	Store pointer register to memory
CMPX, CMPY, CMPU, CMPS	Compare pointer register with memory
LEAX, LEAY, LEAU, LEAS	Load effective address into index register
SEX	Sign Extend D accumulator
TFR register, register	Transfer register to register
EXG register, register	Exchange register to register
PSHS (register)?	Push register(s) onto hardware stack
PSHU (register)?	Push register(s) onto user stack
PULS (register)?	Pull register(s) from hardware stack
PULU (register)?	Pull register(s) from user stack

tage of the trend to larger memory components. Moreover, the system bus will be designed to make it easy to interface MACS with a large variety of standard RAMs, electrically alterable ROMs, and ROMs, in addition to existing 6800 peripheral devices. Special features will also ease multiple- and distributed-processor designs.

The MACS microprocessor instruction set will pay special attention to commonly used data types, data structures, and control structures in microprocessor-based applications and to the special features needed to support efficient high-level-language compilers. Using a storage-to-storage architecture, the instruction set will support single-bit, -byte, -word, and multiple-precision data types and will include instructions for multiply and divide and decimal data manipulation.

Meanwhile, flexible addressing modes will allow easy access to all areas of the 16-megabyte address space. Common data structures including stacks, linked lists, and arrays will be simple to address. Other instructions will directly implement subroutine calls, parameter passing, and programmed loops. Code, generated by high-level-language compilers, will make efficient use of the machine organization and be relocated by hardware support included in the processor. It will also be possible to write ROM- and PROM-based firmware to allow physical relocation of the memories in the memory address space. In multiple-processor systems special instructions will permit interprocessor communications. □

eral device is microprocessor-controlled, which makes hookup easy, since the interfacing is programmed.

For I/O architectures involving high-speed data transfers, direct memory access must be used. Consequently it is best in these cases to give the peripheral controller a supervisory function. In DMA data transfer, the device interacts directly with main-memory storage, without intervention by the central processor. The connection is made to the channel controls in the Series/1, so that the channel becomes merely the highway for the data transfer and not a major processing element. The I/O support program resides in the device controller.

In the Series/1, error detection, analysis, and recovery would represent a significant portion of the operating-system program. Therefore, the system architecture provides for the I/O device controllers to perform supervisory functions like chaining together related I/O commands, as well as a limited amount of error recovery and status maintenance. But for each of the attached devices, a cost tradeoff must be made between extensive control and simple data transfer. On the one hand, a microprocessor might handle most of the supervision, while on the other, a hardwired controller may simply perform classical I/O operations. This flexibility is of course desirable, because each device can be given the level of control most cost-effective for it.

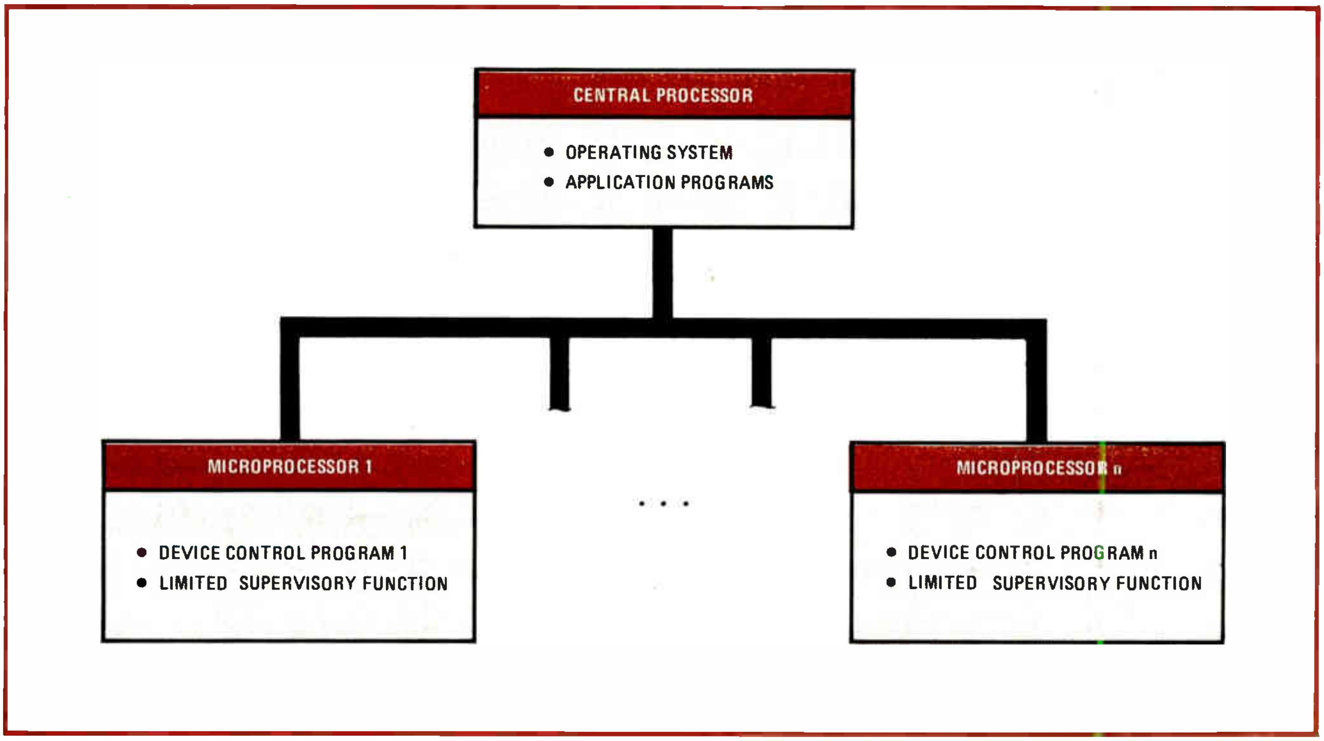
Direct-memory-access I/O operations can be divided into three phases: setup, execution, and completion or recovery. The operation starts with the main processor executing an operate-I/O instruction, which tells a given device to fetch a table of control data from main memory. (It is assumed that the control program in the main processor has created the data table and has established both the necessary linkages for device handling and the other supporting programs. It is also assumed that the I/O device has an interrupt capability.)

The setup phase consists of DMA fetching of the appropriate control data table and checking of its entries for acceptability. Next, in the execution phase, the I/O operation is performed on a high-speed DMA basis. Either execution will proceed to completion or an error condition will cause it to be redirected, in which case data recovery is required. In all cases, information telling what the device will do at each stage of the operation is contained in the control data table.

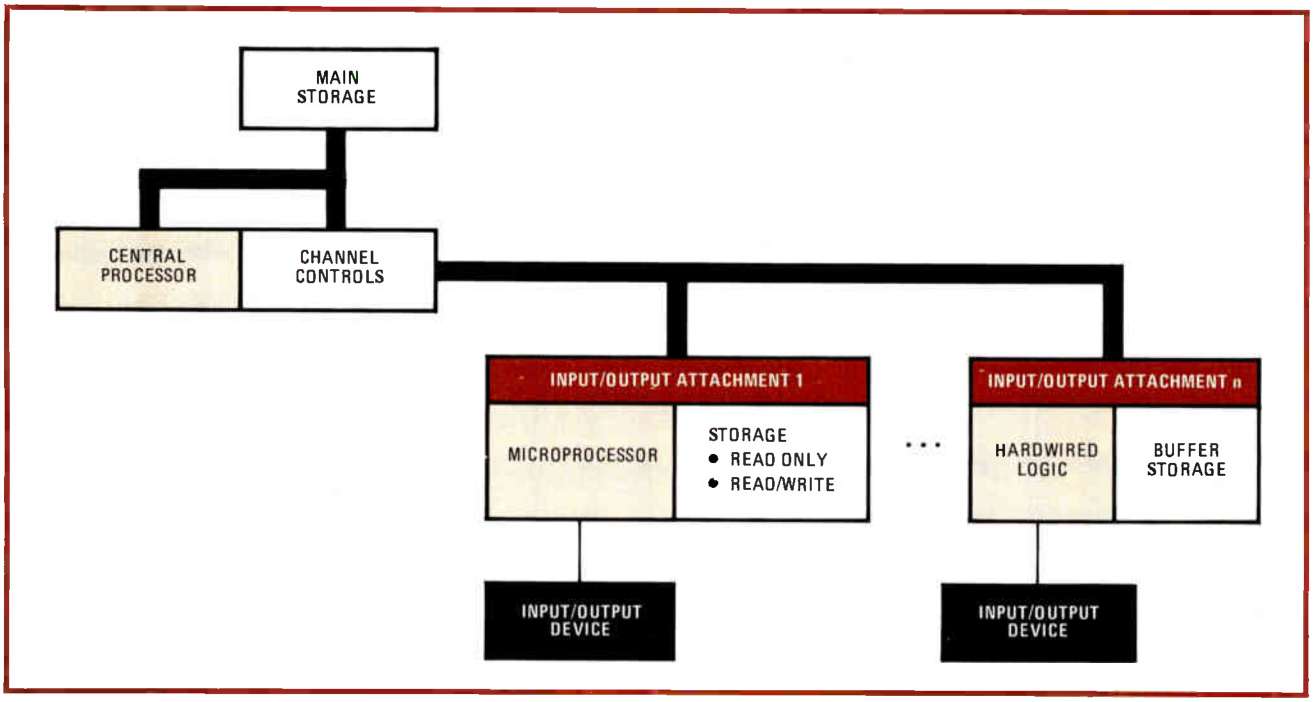
The main system architecture fixes the maximum size of the control data table and the specific location of the entries that support the given functions. All or part of the table is fetched from main memory and stored in the peripheral-device-controlling microprocessor's memory, depending on the extent of the control function. Entries in the table may be encoded as one or more words, as a single bit, or as a multiple-bit field within a word. The choice depends on the architect's tradeoff between compacting the information for storage efficiency and making it comprehensive for easy decoding by the microprocessor. Depending on the performance of the given microprocessor, less highly encoded entries may be desirable, to reduce the length of its decoding program.

One set of entries in the control data table specifies the I/O operation, such as read or write, that is commanded. Another entry specifies the address in main memory to which the I/O data is sent or from which it is to be obtained. Different I/O commands may be chained together so that a sequence of actions—for example, a disk seek followed by a data read—can follow from a single operate-I/O instruction executed in the host.

Usually, the operation for chaining commands



1. Distributed I/O hierarchy. Peripheral-controlling microprocessors can remove many I/O tasks from the main processor. Under command of the host, they may simply control the devices or, through more elaborate programming, they can perform limited supervision.



2. Peripheral hookup. In a distributed I/O processing system built around the IBM Series/1 minicomputer, attachments are made to the 16-bit I/O channel, which is piped directly to memory by the channel controls. High direct-memory-access speeds are thus attainable. Note that the I/O attachment on the right has a hardwired controller—microprocessors are not always necessary for controlling I/O.

together is given its own control data table in main memory. This being the case, each control data table must contain the address of the next control data table to be fetched after the microprocessor has finished the current I/O command. Figure 3 depicts the relation between control table entries and the areas of main memory that they reference.

Crossing the distributed I/O threshold

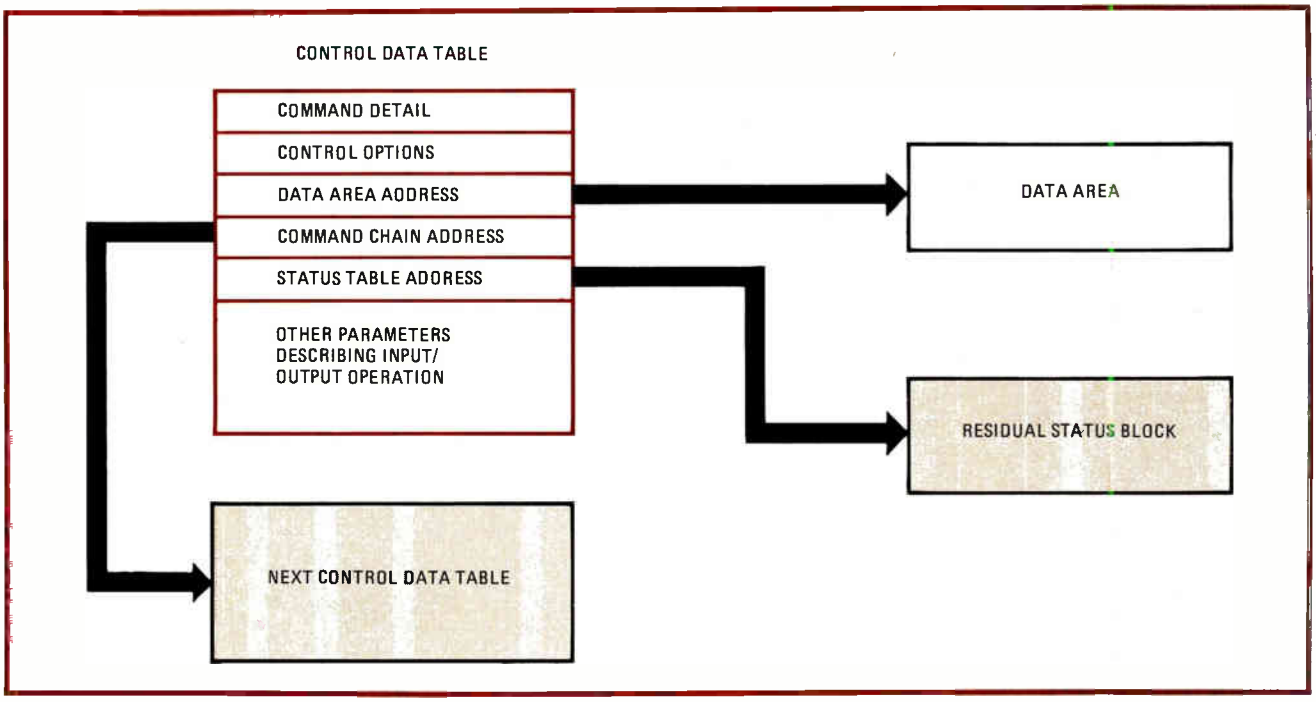
The I/O operations described thus far—DMA and command chaining—can be performed by hardwired-logic controllers, and in some cases such controllers are still the best solution. More often, however, for greater convenience, the operations should be performed by microprocessor-based controllers. In those cases, the microprocessor is firmware-programmed simply to carry out the logical operations of a hardwired controller. But in true distributed I/O processing, the intelligence of the microprocessor is used to its full extent. The distributed I/O threshold is crossed when the controlling microprocessor performs error recovery without intervention by the main processor.

A good example of the distributed I/O processing concept is the synchronous data-link control adapter for the Series/1. This attachment provides the minicomputer with an I/O architecture that divides errors into two categories according to their severity. Serious errors are routed back to the host processor, which decides what action to take. For less serious errors, the SDLC adapter can be directed (according to an entry in the control data table) to perform the data recovery itself and suppress immediate notification of the central processor. In the data-receive mode, the adapter has four such suppressible conditions: overrun, aborted frame, incorrect record length, and block-check error.

If suppression is chosen, the adapter takes the following action. First it marks the occurrence of the error by setting an appropriate status flag. Then it continues in the receive mode until the given transmission or chained operation is completed. Finally, the controller signals the central processor that the I/O operation has been finished, that a suppressed error condition has occurred, and that a table, called a residual status block, is available to describe specifically what has happened. In the case of the SDLC adapter, the residual status block contains two words of information, including the status flags for the suppressed condition. The Series/1 architecture allows a maximum residual status block size of 16 words of 16 bits each.

The idea of distributing supervisory I/O functions can be extended in a variety of ways. One extension is to allow the device controller to retry an I/O operation that failed the first time. Once a given number of attempts is made and the I/O action continues to be unsuccessful, the central processor is notified. However, in assigning this supervisory function, the designer must decide whether the central processor and its operating system can tolerate a slowdown in the I/O operation caused by the multiple attempts.

Another extension worth considering is to have the device controller keep a log of the attempts, for diagnosis and maintenance. If the log is to be maintained at the device, a decision must be made regarding how and when a backup copy is to be sent to the main processor. The object is to keep as much of the log maintenance activity as possible away from the central processor, but bear in mind that a problem can occur when the device fails and the central processor is left with an obsolete log.



3. Control program. A table of control data in main processor storage, fetched by a given device controller upon interrupt, directs the I/O operation. The table, which can be a maximum of sixteen 16-bit words in the Series/1, specifies the operation (read or write), the addresses (including those of data, error-condition status, and another table for chained operations), and other information.

Supporting hardware and software in the central processor govern the speed of the I/O response, determine the ease of the distributed I/O programming, and prevent interference between different I/O tasks. A priority structure helps reduce response times for critical tasks, particularly when many I/O devices are attached. Hardware can be built that facilitates a rapid transfer from the program being executed at the time the I/O interrupt occurs to the program that is to service the interrupt. Further, hardware can be added to make the necessary information concerning the interrupt directly available to the program, without the need for excessive instruction steps to obtain it. Having I/O operations executed only under supervision of the device controller can reduce programmer error, but at the cost of somewhat longer execution times.

Main processor

In the Series/1 processors (the model 4953 of which is shown in Fig. 4), there are four preemptive priority levels of interrupt, each with a complement of program-status and other registers. Instructions need not be executed to save and restore the contents of registers being used by the interrupt program. Instead, the programmer can assign a device any interrupt priority level. This capability makes the I/O device considerably more flexible. Moreover, hardware is available that branches to the individual routine serving the address of the I/O device. In all, 256 devices can be attached.

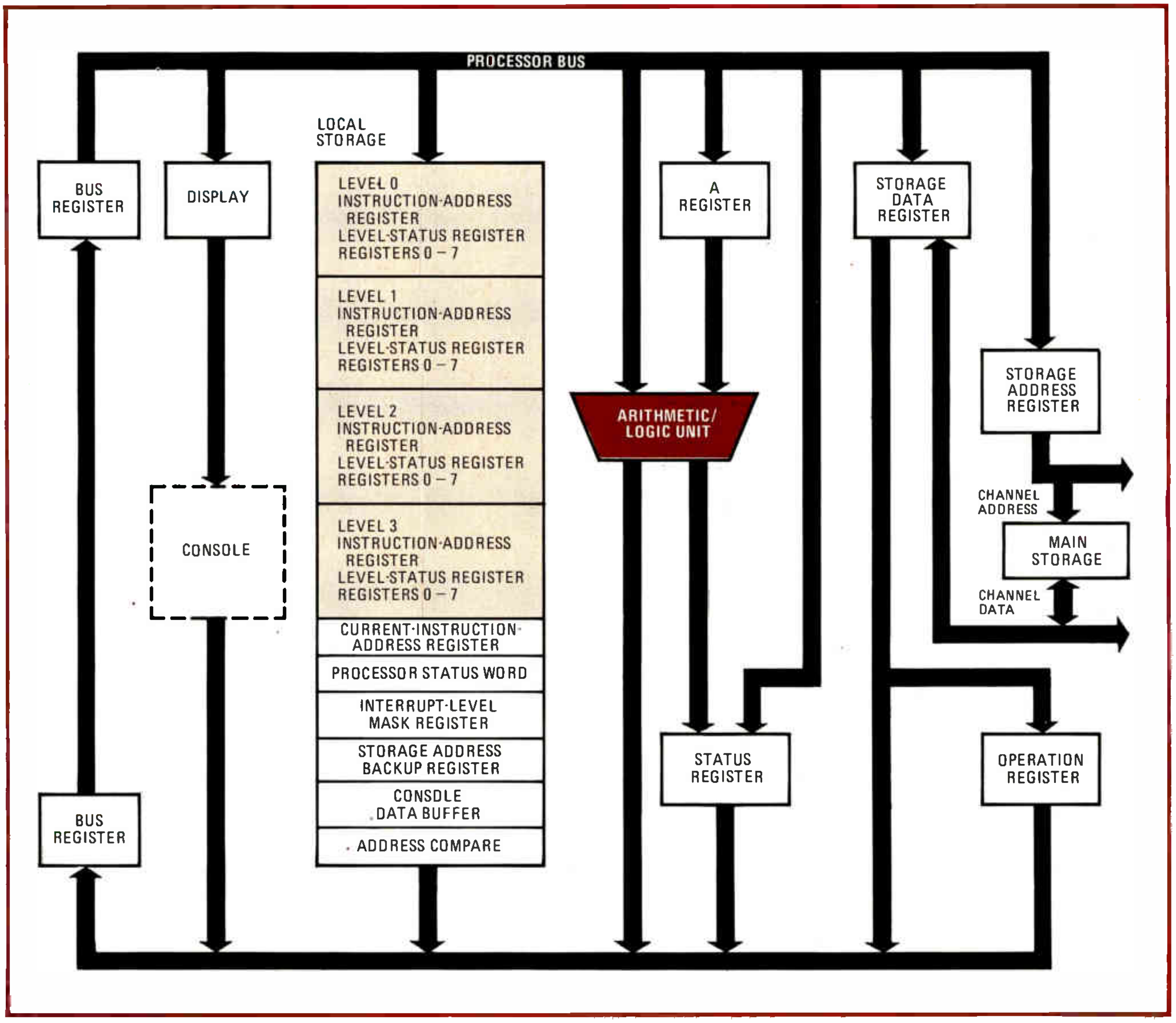
Speed in processing the interrupt is further enhanced by the presentation on the I/O channel of information telling the status of the given device. Nineteen bits suffice to indicate the condition of the interrupt, the address of the I/O device, and additional information.

Three bits give the condition code, one of a possible eight, associated with the interrupt. For example, one condition code would indicate that the interrupt was caused by normal termination of an I/O operation. Another code would signal that an error condition is associated with the interrupt. Still another would declare that the interrupt was caused externally.

The remaining 16 bits contain the 8-bit address of the I/O device and 8 bits of additional information regarding the device and the interrupting condition. Still more information in the form of the previously described residual status block is available, if there is a suppressed exception condition associated with the normal termination of an I/O operation. (Error conditions are just one type of exception condition, which includes, for example, unfilled frames in the blocks of data for the SDLC controller.)

Another noteworthy factor influencing the speed of I/O response is the effectiveness of the central processor's instruction set. On one hand, the instructions may be very fast but have little computational power, so that many instructions are required to do a given job. On the other, the instruction set may be very powerful yet need many storage locations to hold required information. The optimally designed instruction set will quickly execute important tasks, use as little storage as possible, and require as few source-language lines as possible to be coded by the programmer.

The requirements for the microprocessors that control the peripheral devices are quite different from those for the central processor. A very important one is that the hardware occupy a minimum amount of space and be easily packaged with the remaining device hardware. Additionally, the cost and even the speed requirement



4. Series/1 architecture. The 4953 one-board central processing unit in the Series/1 is built around a microprogrammable bipolar microprocessor with an average instruction cycle of 11.8 microseconds. The bus-oriented processor has four priority-level interrupts, each with an instruction-address register, a level-status register, and eight storage registers. The priority structure helps reduce I/O response times.

may be more stringent for microprocessors than for central processors, depending on the system.

For classic device control, microprocessors should have relatively simple instruction sets, with the emphasis placed on bit manipulation and a rapid execution rate. In terms of programming, even basic instruction sets are adequate to support the programs associated with most distributed I/O processing.

The activities of the microprocessor program are either fast or slow. High-speed processing must take place during the execution phase of DMA data transfer. But since the function performed is very simple and repetitive, not much program logic is needed. Data is transferred to and from the data bus, and a storage address, either in the main memory or in the microprocessor memory, is incremented. This portion of the distributed I/O processing dictates the raw speed requirement of the microprocessor. For a very-high-speed device operating on a high-speed channel, a fast bipolar microprocessor or chip set is needed, and in extreme cases, a hardwired controller may be necessary.

In sharp contrast, a much slower processing rate is required for the setup and completion-or-recovery phases of a DMA data transfer, and these phases generally take up the major portion of the microprocessor's program. However, these program steps do not tie up the channel or delay processing in the main processor.

The microprocessor in the Series/1 SDLC adapter has a 16-bit fixed-length instruction format that supports up to 4,096 bytes of instruction addressing. The instruction set is relatively basic and is geared toward device control. Thus the loads, stores, and I/O transfers are 8 bits wide, whereas the internal data flow and the stack of 32 registers are 4 bits wide. All instructions except loads and stores are executed in 750 nanoseconds. This instruction set, basic as it is, can serve most tasks of distributed I/O processing—in device-control applications, a small instruction set goes a long way. □

System design with dynamic memories takes attention to detail

Key principles are adequate margins in power distribution and signal timing

by Stephen Calebotta,
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☐ Memory systems built around dynamic RAMs are multiplying, thanks to the introduction of chips of ever increasing density and the swing to digital design triggered by the microprocessor. However, the first exposure to system design with dynamic random-access memories can be traumatic for the engineer wrestling with the refresh requirement. Fortunately, following a few key design principles will ward off problems that can arise from the dynamic nature of these memories.

Of course, before starting work, the designer must choose between dynamic and static RAMs. The basic difference between the two is the way they store data. The dynamic device uses a capacitor as a storage device, while the static unit uses a flip-flop to store a bit. It is these cell designs (Fig. 1) that give each type its advantages and disadvantages.

In one major respect, the static RAM is easier to use because no refresh cycle is required. Thus its control signals tend to be easier to generate. On the other hand, it draws power continuously to sustain its flip-flops, while the dynamic RAM draws minimal power between cycles. With continuous cycling, dynamic units draw about as much power as the statics, but in a large memory array they save total system power since only one bank of RAMs is ever activated during a memory cycle. All other banks draw minimal current except during refresh cycles. The duty cycle for refresh is approximately 1.5% to 3%.

Die size makes a difference

The vastly simpler cell design means that the die size of the dynamic RAM is often at least 20% smaller than that of a comparable static device from the same manufacturer. Smaller die sizes mean more dice on a wafer, so dynamic RAMs should always remain considerably cheaper than comparable static units.

Also, dynamic memories can save money in larger systems. Their lesser power requirement means smaller and cheaper power supplies, which in turn produce a further saving through reduced cooling requirements. In general, the larger the memory system, the more cost-effective dynamic RAMs become.

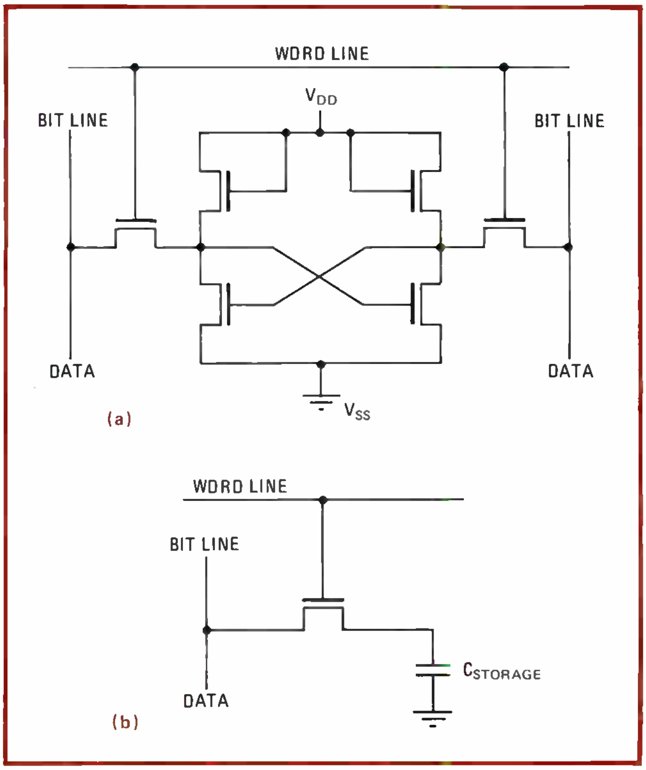
Another important functional difference between static and dynamic devices is the fact that the dynamic units must run through a complete cycle to read or write. Aborting the cycle by removing the chip-enable pulse too early or by trying to start a second cycle too soon after the first will probably cause data loss. Minimum chip-enable on and off times must be observed when designing these memory systems.

Dynamics have a refresh penalty

Since charge leaks off the storage capacitors of a dynamic RAM, it must be replenished periodically to retain its data. The charge in any one cell is refreshed every time that cell is activated for a read or write operation. At the same time, all the cells in the same row are refreshed. Thus, sequencing through all the row addresses can refresh the entire chip over only 64 cycles for a 4,096-bit RAM in 2 milliseconds (128 cycles for a 16,384-bit device). The bit pattern presented to the column addresses does not matter, but the setup and hold times must be maintained to avoid data loss caused by unstable column addresses during refresh.

The hardware required for refresh amounts to a 6- or 7-bit counter for the refresh addresses, some way to multiplex the counter signals onto the RAM row-address lines, a timer to signal when a refresh should be done, and the miscellaneous gating needed to couple into the usual read/write logic.

In some systems, no extra refresh logic is needed. For



1. Static vs dynamic. Storage device for a static RAM (a) is a flip-flop, which imposes greater complexity on a cell but requires no refresh cycle. Dynamic RAMs (b) are much simpler, but the capacitance storage mechanism requires periodic refreshing to retain data.

example, in typical cathode-ray-tube terminals, dynamic RAMs will be refreshed automatically if their row-address inputs are driven from the least significant address bits coming from the screen-refresh logic. In fact, it is good practice in any system to place the most active system-address bits on the RAM row addresses. Then standard system operation will automatically refresh the bulk of the RAM cells.

Designing the RAM board

Assuming that the lower cost and smaller power dissipation of the dynamic RAM outweigh the lesser system complexity of the statics, attention must be paid to the special characteristics of the dynamics to produce a board design with the greatest production yield. The key to success in a dynamic chip system is meticulous concern with power-supply and timing margins. Without this, the system can end up a nightmare from the standpoints of both manufacturing and field service.

The difference between the manufacturing yields of functionally identical boards is usually the amount of margin designed into each system. As the power-supply and timing margins drop, the number of soft errors rises. (A chip is said to have a soft error if a location occasionally cannot be written and read back correctly; if it occurs consistently, it is called a hard error.)

Soft errors usually occur during a memory cycle in which some system parameter has departed from specification. Since the RAM chips themselves have variations in their margins, replacing the offending device with one having a greater margin in the out-of-spec parameter could solve the problem. But doing this results in many rejected units. The real solution lies in careful system design and board layout in the beginning.

Power distribution is the start

By far the single most important aspect of a successful dynamic RAM system is precise power distribution, consisting of carefully designed decoupling and power gridding. All dynamic RAMs have at least two supplies, V_{DD} and V_{BB}; V_{SS} is the RAM internal ground. Most also have a third supply called V_{CC}. Only V_{DD} need be considered here since the others have similar characteristics.

At the beginning and end of a chip-enable pulse, each RAM can draw current spikes of from 50 to 100 milliamperes, with rise times of 20 nanoseconds. In addition, each draws a direct current of 20 to 40 mA for the duration of the chip enable. The power distribution system must supply these currents while the voltages at the RAMs remain constant.

Figure 2a is a schematic of the V_{DD} supply for a row of eight memories. The inductors represent printed-circuit trace inductance, which is typically about 10 nanohenries per inch for a 13-mil trace. If the RAMs are spaced on half-inch centers, a total of 10 nH will appear between each pair of memories.

Assuming only one infinitely large, perfect capacitor per row, the voltage spikes at the first, second and last RAMs would be:

$$V_{1\,spike} = \Delta V_1 = 8 \times 2 \times L/2 \times dI_{dd}/dt$$
$$= 10\text{ nH} \times 8 \times 100\text{ mA}/20\text{ ns} = 400\text{ mv}$$

$$V_{2\,spike} = \Delta V_1 + \Delta V_2 = L \times 15 dI_{dd}/dt = 750\text{ mv}$$
$$V_{8\,spike} = \Delta V_1 + \Delta V_2 \ldots + \Delta V_8$$
$$= 36 \times L \times dI_{dd}/dt = 1{,}800\text{ mv}$$

These spikes are unacceptable. They illustrate that one capacitor, no matter how large, cannot adequately decouple a bank of RAMs. However, if a decoupling capacitor C_{RAM}, having 10 nH of trace inductance in series, is provided for each RAM (Fig. 2b), the voltage spike will be reduced to:

$$V_{spike} = L \times dI_{dd}/dt$$
$$= 10\text{ nH} \times 100\text{ mA}/20\text{ ns} = 50\text{ mv}$$

which is within acceptable limits. Thus, local decoupling should be used to overcome the spiking problem.

The series inductance of the leads (Fig. 2c) also affects the ability of the power distribution system to supply the direct current of 20 to 40 mA drawn per chip during a RAM cycle. If the total power-supply lead inductance is assumed to be 50 nH (ignoring the pc trace inductance within the RAM array itself), then producing 40 × 8 mA within 40 ns requires a voltage step at the RAM inputs of:

$$V = L \times di/dt = 8 \times 50 \times 40/40 = 400\text{ mv}$$

This large step will be avoided with adequately designed decoupling. Thus, the bulk of the direct current for cycling the RAMs must come from the decoupling capacitors themselves, and they should be large enough to supply these currents with little droop. They should also be situated close to the RAMs in order to reduce the effect of spikes.

Using a 0.1-microfarad capacitor, the droop involved a 250-ns cycle would be:

$$V_{droop} = I \times t/C$$
$$= 40\text{ mA} \times 250\text{ ns}/0.1\ \mu\text{F} = 100\text{ mv}$$

which is acceptable for such an array.

To reduce droop further, the board should have 50 to 200 μF of bulk decoupling of the +12-volt power supply. The other supplies can have less. Half of the total should be placed near the point where the power is applied to the board, while the other half should be placed at the far side of the RAMs.

The latter half of the bulk capacitance also may be distributed throughout the array. To decouple V_{DD} and V_{BB}, 5 to 10 μF for each eight RAM chips will suffice. For V_{CC}, 5 to 10 μF for every 32 chips will do.

The choice of capacitor types to accomplish these two types of decoupling is also very important. In the preceding calculations, the influence of effective series resistance was ignored, but it can be at least as great as that of the trace inductance. For minimum series resistance, the use of ceramic capacitors is recommended for local decoupling.

The Memory Systems Group at National Semiconductor Corp. has had good results with ceramic capacitors of Z5U material, which are available from AVX Corp. or Sprague Electric Co. These capacitors are considered so important to good memory board performance that every lot is subjected to an incoming inspection, including a transient-response test.

For bulk decoupling, solid tantalum capacitors are recommended. They have better transient response than most other large-value capacitors, and they pack a lot of capacitance into a small package, which simplifies board layout for the designer.

Another approach to reducing the effects of inductance is through power gridding: running the leads in cross-hatch fashion rather than in a single direction. If there are a number of rows of the memories, all the power-supply traces to the chips should be run vertically and horizontally throughout the array. These multiple paths through the array will reduce the effective inductance of the power distribution system.

Experience has shown that power distribution is the single most important aspect of good RAM board layout. Moreover, it has produced these empirical truths, some of which have been discussed:

■ Plenty of decoupling should be used. The decoupling capacitors not only reduce voltage spikes, but they also provide most of the RAM power during cycling. Lay the board out for one 0.1-μF capacitor per power supply per RAM (up to three per chip). As production history accumulates, it may be possible to omit as many as half the capacitors. Use 50 to 200 μF of bulk decoupling on +12-V supply; on the +5- or −5-V transistor-transistor-logic supplies, use about 25 to 100 μF.

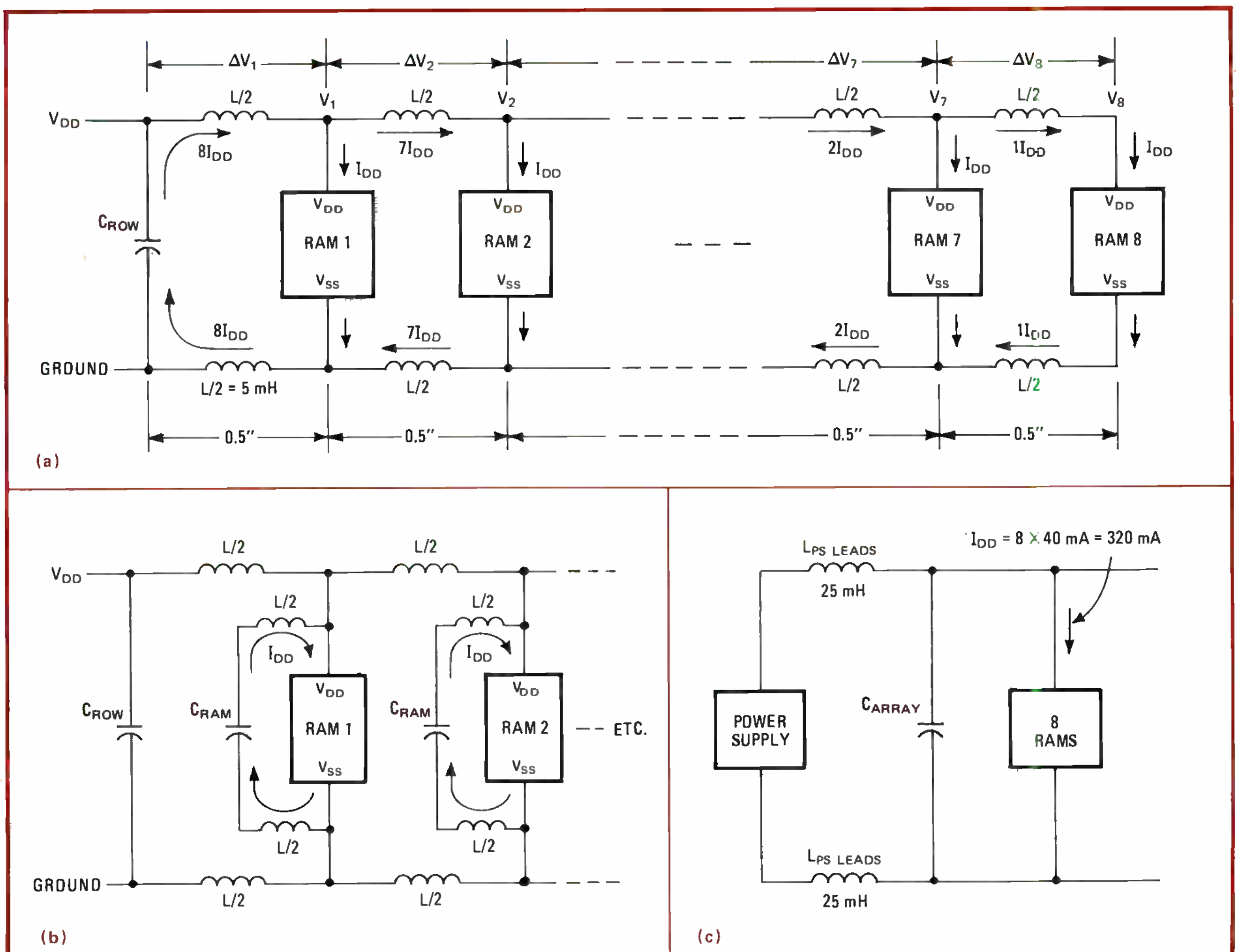
■ Decoupling capacitors should have the shortest possible traces back to their respective RAM power-supply pins. To reduce inductance further, these traces should be as wide as board space will allow.

■ Traces carrying power-supply voltages throughout the array should be as wide as possible, although adequate decoupling allows small trace widths. If some priority of power-supply trace width is feasible, make V_{SS} widest, V_{DD} next, then V_{BB}, and finally V_{CC}.

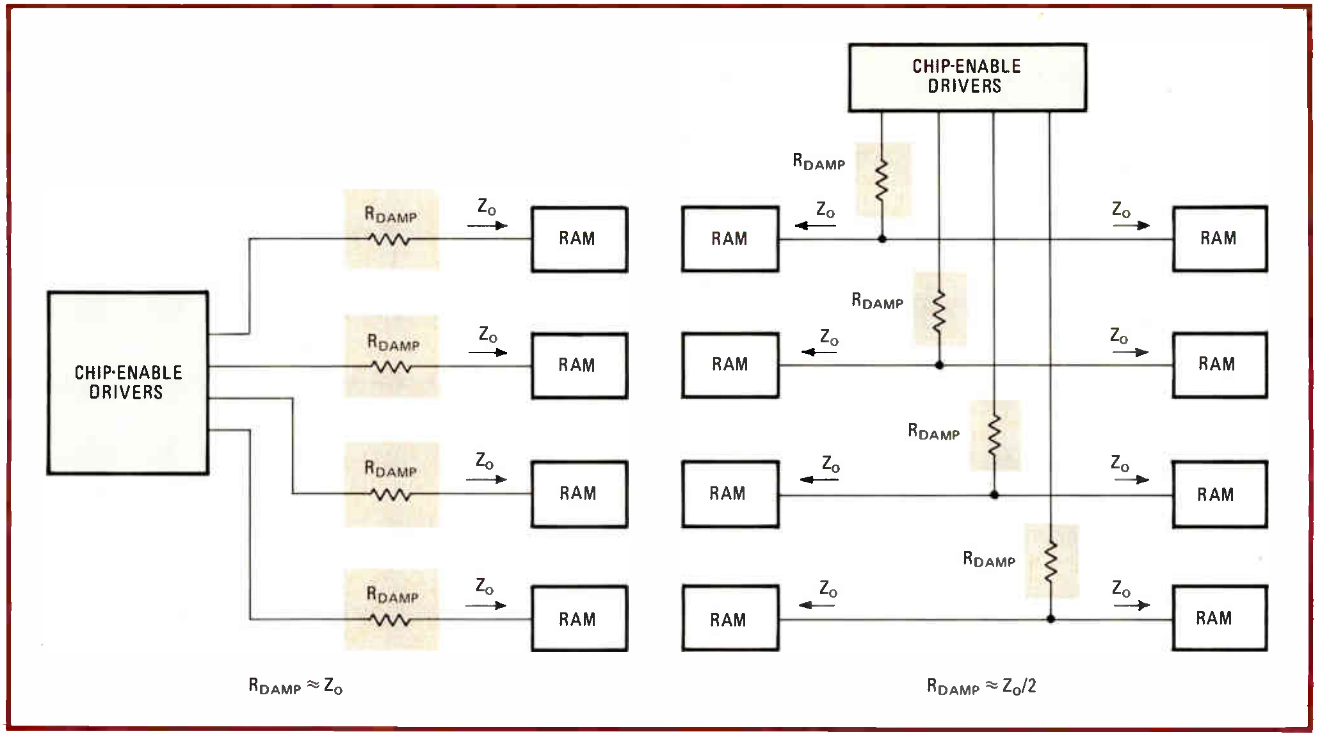
Discussion of multilayer boards has been omitted. Although they tend to simplify power distribution problems, almost everything set down so far is still applicable to multilayer boards.

Timing is next in importance

The second most important aspect of successful RAM system design is the distribution of address, data, and control signals. The most important signal to the RAM is the chip-enable signal, and all timing is referenced to it. There are two types of chip-enable in common use today, the 12-V and TTL-level swings. With both, there are two



2. Decoupling. Schematic of a row of eight RAMs (a) shows distribution of trace inductances and spike-producing currents, assuming one large value of row capacitance for decoupling. A better arrangement is local decoupling capacitors, C_{RAM}, provided for each RAM. Droop in applied voltage caused by power supply lead inductance is overcome by properly distributed bulk decoupling capacitance (c).



3. Damping resistance. A damping resistor with a value between 10 and 51 ohms inserted between drivers and the array of random-access memories helps preserve the clean waveshape of the clock. These are two alternative arrangements the designer may choose.

main considerations for the designer in running chip-enable lines through an array.

The actual driver chip must be situated near the RAM array it is driving in order to keep the chip-enable run short and direct. A damping resistor should be put near the driver. The value of this resistor must give the optimum clock waveform at the RAM chips: it will probably be between 10 and 51 ohms. Figure 3 shows commonly used arrangements.

Driving clock line efficiently

These two considerations stem from the fact that, at the usual clock frequencies encountered, the clock lines behave like transmission lines with a characteristic impedance of $Z_o = (L/C)^{1/2}$. The clock-line impedance within the array of chips is somewhere between 10 and 15 Ω, while the unloaded line between the clock driver and the chip array is in the range of 30 to 50 Ω.

To drive the clock line efficiently, some attempt must be made to match the driver's output impedance to that of the line. The actual output impedance of most monolithic clock drivers varies as much as 3 to 1. So a fast driver with low output impedance should be used, with a damping resistor connected in series to match its effective output impedance to the line with only about 10% variation as a design factor.

Long clock lines or long lengths of unloaded clock lines can cause problems. In the case of the long clock line, an open circuit at the far end of the line can reflect a pulse from the end of the line back to the driver, resulting in ringing. In the case of the long unloaded length, reflection from the junction of the unloaded and loaded sections of the line, due to the mismatch, can cause glitches in clock transitions.

To minimize crosstalk between chip-enable and other signals, it is best to run the chip-enable line at 90° to other lines. This design is usually difficult to accomplish in an actual layout. The alternative is to leave as much room as possible between chip-enable and adjacent signal-carrying traces throughout the array. Signal traces in the array are typically on 50-mil centers, and keeping adjacent traces more than 50 mils from the chip-enable line will help reduce crosstalk.

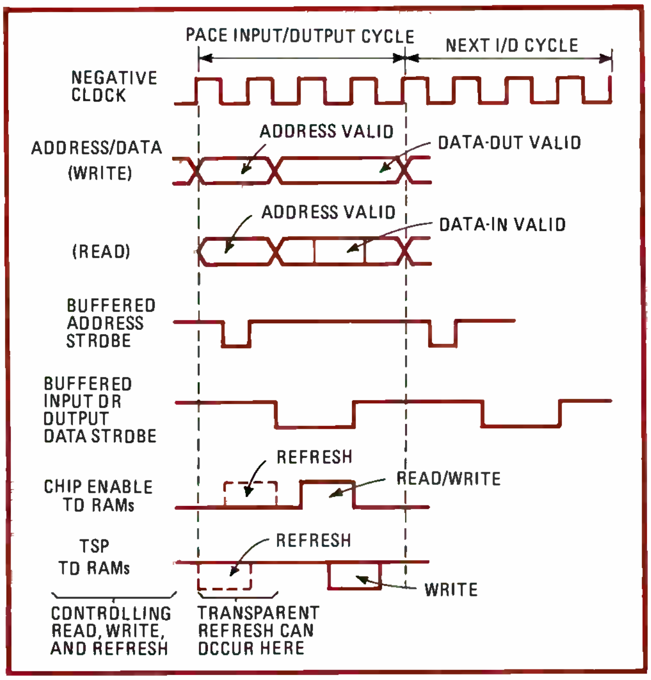
The lines for address, data, and control signals should also be run as directly as possible. Their layouts tend to be noncritical, but timing is critical. The control logic should be designed to maximize setup and hold times with respect to chip-enable.

As an example, consider an actual memory board built for an 8080 system. The chip was a MM5271 4-k RAM, which has a TTL-level clock input where the true state is low. The signal that controls read, write, and refresh is called TSP. The MM5271 data sheet specifies that the setup time for TSP is zero with respect to the leading edge of chip-enable. When refreshing, TSP must be low at the beginning of chip-enable. The original timing for the board brought TSP down at the same time as chip-enable.

Changing the timing

At first, the system seemed to work; however, an error appeared every half hour or so. An oscilloscope failed to disclose anything outside the specifications: when TSP and chip-enable were superimposed on the scope, their leading edges were absolutely coincident in both time and waveshape. So the TSP timing was changed to provide about 50 nanoseconds of setup time, and the problem disappeared from the system.

Obviously the original design was at the limits of the



4. Transparency. In periods when the processor does not require access to the memory, refresh can be accomplished without holding up the CPU, as with this timing diagram for a 16-k-by-8 board used with a PACE microprocessor for byte-mode data storage.

memory specs. Performance under these circumstances depended critically on the shape of the two waveforms to keep the system working. Once adequate margin was designed in, the system operated flawlessly.

In high-speed systems, where such extra-margin design is hard to come by, damping resistors in address, data, and control lines will help control waveshapes. Of course, where signals have time to settle down before they are needed, these damping resistors can be avoided.

On the logic

There are a number of other important aspects in designing dynamic memory boards, among them logic considerations. As already discussed, one of these is that a RAM cycle must never be aborted before its normal completion. So the control logic must be designed never to permit a shortened cycle. Of the several approaches possible, the simplest is to utilize existing system-level control signals. This way is easy to implement in some 8080 and PACE systems.

When the available system control signals are not adequate, another technique that works quite well is to use a high-frequency oscillator and a shift-register connected as a Johnson counter. Any required timing signal can be generated from the counter using a two-input gate.

A minor drawback: if the hf oscillator is asynchronous with respect to the main system timing, the cycle timing of each memory will have a finite uncertainty with respect to the system cycle timing. This uncertainty is equal to the clock period of the oscillator. However, it may be avoided with a gated-delay-line oscillator, which can be started and stopped reliably, instead of using a crystal or RC oscillator.

For refresh timeouts, a count down from a crystal oscillator is best. An astable oscillator is acceptable but must be carefully designed within worst-case limits for minimum frequency with respect to temperature to ensure that the RAM gets refreshed often enough. At the end of the timeout, a flip-flop should be set, and when the refresh cycle is finally completed, it should be reset. It should not matter at what point within the timer period the RAM gets refreshed, as long as it occurs before the period has ended.

Most microprocessors have predictable time periods during which they will not require access to the RAM board. Usually it takes little effort to insert refresh cycles during these periods, thereby making them transparent to the central processing unit. For example, Fig. 4 is a simplified timing diagram for a 16-k-by-8-bit RAM board used by a PACE microprocessor for byte-mode data storage. All timing is generated from existing system signals. Refresh is transparent, done at any time in the absence of any address or data-in or -out strobes, coincident with the rising edge of the clock.

Minimizing delay

When the central processing unit is very fast and is using the bus almost continuously, holding up the processor for refresh cannot be avoided. Even then, some clever design can minimize the delay.

Some systems need the capability of single-stepping through programs. Since dynamic RAMs must be refreshed continuously, the output data must be latched. Then the refresh can proceed behind the latches, never disturbing the data, and the RAM appears static.

Direct memory access requires slightly different considerations from normal cycles—for example, how to handle refresh. One technique is to let the device requiring access permit periodic refresh. Another technique is to limit the DMA time to less than 2 ms and then refresh the entire memory in a burst.

A third technique is to limit the DMA frequency, by making the period between cycles equal to a normal RAM cycle plus a refresh cycle. In this way the refresh will be transparent to the device requiring DMA.

From a system standpoint, the most important aspect of DMA with dynamic RAMs is the polarity of the system-level control signals. With TTL where bus control can change hands, signal logic must be true at low level.

This requirement stems from the fact that, as control moves from the CPU to the DMA device and back again, short periods can occur during which the control lines are floating (since neither device is driving them) and they appear high. If control signals have been defined as high true, then when the lines float even briefly, devices such as the RAM board will think that a command has been issued and will start a cycle.

The problem will be compounded when a real command appears. Either the unintended cycle will be aborted, which can destroy data, or the intended cycle will start too late, causing other problems in the entire system. This problem can occur on the S100 bus, standard in many hobby computers. It mixes the polarities of the control signals and, therefore, makes control logic for dynamic RAMs unnecessarily complex. □

Simplified priority encoder has low parts count

by Tomasz R. Tański
Warsaw, Poland

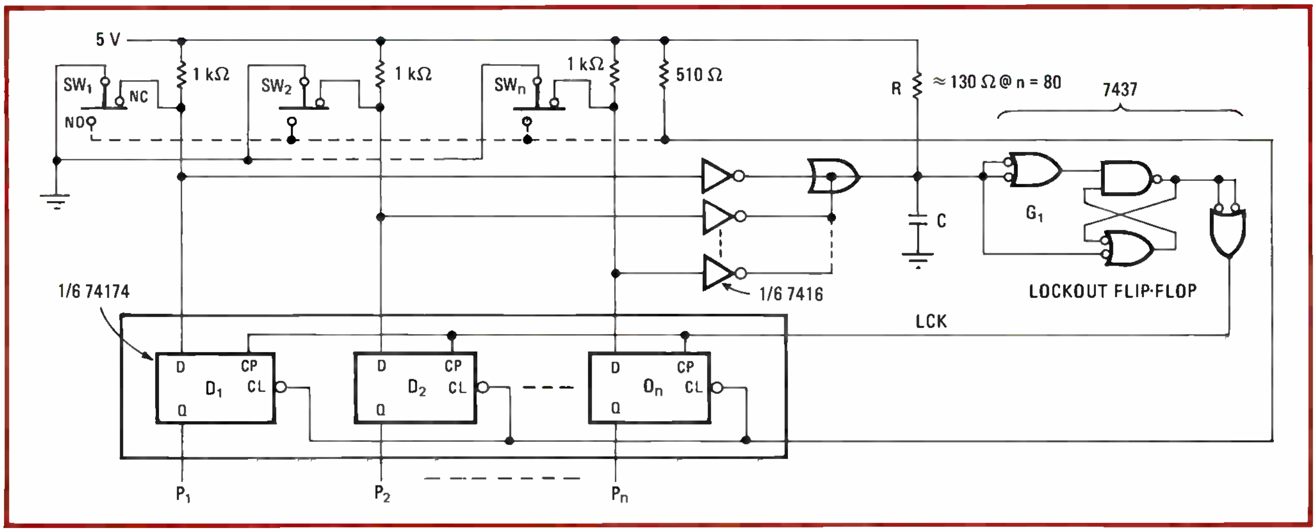
The number of chips in the priority encoder circuit first described by Sterling [*Electronics*, Aug. 18, p. 114] can be drastically reduced by replacing the modularized gate arrays by D flip-flops and a wired-OR gate. As in the original circuit, the output ports of this modified momentary-contact switch array responds to the first command received and locks out all subsequent commands, so as to provide a time-sequence priority scheme that is useful in many industrial systems. But this circuit is simpler to build and test, because the interconnections between elements are minimized.

Depressing any switch, SW_n, shown in the figure sets the corresponding D input of its flip-flop, D_n, high. The switch signal also quickly propagates through the 7416 inverters, which have their open-collector outputs wired together to form an n-input OR gate, and fires the 7437 flip-flop (G). A few microseconds later, the rising edge of the resultant output from G_1 stores the signal generated by SW_n into D_n before the D line, at logic 1 for a time measured in milliseconds, can return to ground.

The strobing signal (LCK) will stay high until all switches return to their normally closed (NC) position. Thus altering the output state of any flip-flop is impossible, because all other switch commands are locked out.

Resistor R serves in a dual capacity. Its primary function is as load resistor for the open-collector inverters forming the wired-OR gate. Its value is selected so that the maximum current drawn is limited to the full-on collector current of one gate, independent of how many gates are activated. Secondly, R, in combination with C, provides effective switch debouncing. For optimum debouncing performance, the value of C should be selected (with the aid of a scope) to provide the trailing-edge delay required for signals from G_1.

Not considering the lock-out flip-flop, only one sixth of a 7416 and 74174 device are needed per switch, compared with the 1½ integrated circuits required in the original circuit. Only one 7437 is required, even for a large number of switches. Each input lead of the 7437 can accommodate an 80-input, wired-OR gate. The LCK signal can drive up to 180 flip-flops. □



Simplification. Momentary-contact priority encoder uses about one fifth the number of chips of previous design. Circuit responds to first command received by switches and locks out all subsequent commands, thus forming a first-come, first-served switch.

Switching multiplier is accurate at low frequencies

by Harold Anderson and Peter Hiscocks
Ryerson Polytechnic Institute, Toronto, Canada

When called upon to multiply low-frequency analog waveforms, switching-type multipliers are at least an order of magnitude more accurate than those that work on the principle of variable transconductance. The typical output error of a transconductance multiplier such as the MC1595 is 1%. But this circuit finds the product of two signals to within 0.05% of the true value and costs only $5.

In the basic switching multiplier (Fig. 1a), an analog signal of constant voltage V_x is applied to the circuit. The voltage at point V_a at any given instant is a function of the switch position, and the switch position in turn depends upon the control signal emanating from the duty-cycle modulator.

The average voltage at point A is:

$$V_a = V_x(t_{on} - t_{off}) \quad (1)$$

as shown in the graph, where t_{on} is the time during which the switch remains in contact with the $+V_x$ position and t_{off} is the time the switch remains in contact with the $-V_x$ position.

If the duty cycle, $t_{on}/(t_{on}+t_{off})$, can be made proportional to a second analog input voltage, V_y, then the following relation holds:

$$V_y = K(t_{on} - t_{off}) \quad (2)$$

where K is a constant. If Eqs. 1 and 2 are combined, the result is:

$$V_a = V_x V_y / K \quad (3)$$

A block diagram of a duty-cycle modulator which satisfies Eq. 2 can be constructed with an integrator network and Schmitt trigger (Fig. 1b).

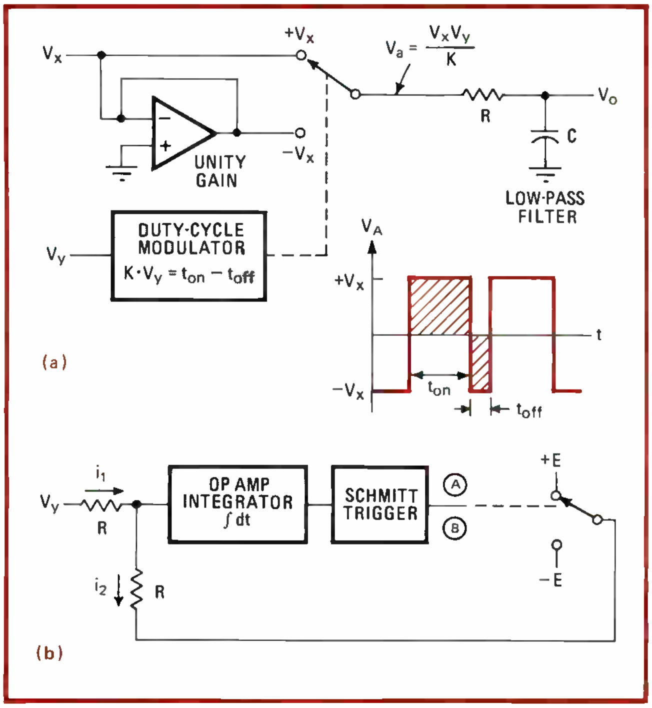
The average current into the input port of the integrator will be zero over a specified time interval, because of the high impedance of the op amp. Thus:

$$\overline{i_1} = V_y/R = \overline{i_2} = (E/R)t_H - (E/R)t_L \quad (4)$$

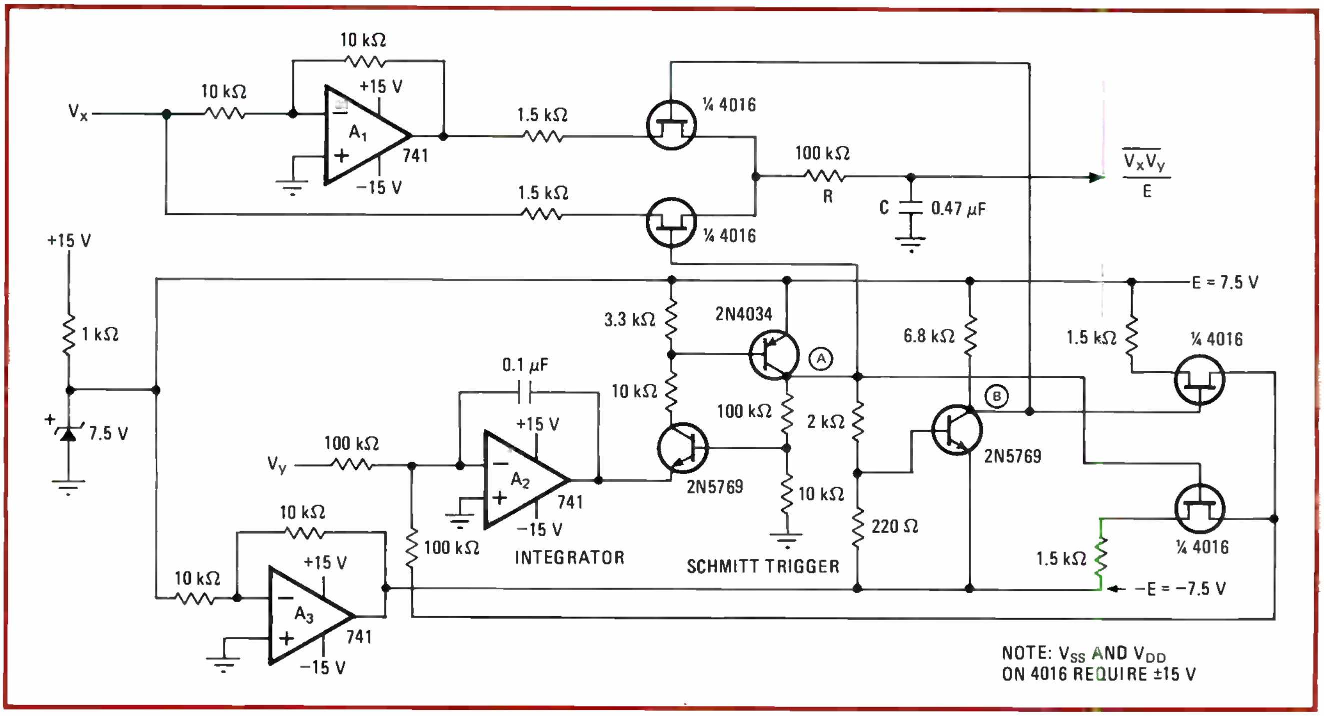
where t_H is the period during which the switch is engaged at $+E$ and t_L is the period the switch dwells at $-E$. It is found from Eq. 4 that:

$$V_y = E(t_H - t_L) \quad (4a)$$

If t_H can be made equal to t_{on} of Fig. 1a and t_L can be made equal to t_{off}, then the preceding equation, when substituted into Eq. 1, yields:



1. Very linear. Switching multiplier (a) is more accurate for finding product of two signals at low frequencies than IC transconductance multipliers. Duty-cycle modulator may be built with op-amp integrator and Schmitt trigger (b). Voltages $\pm E$ and integrator together form oscillator of which the duty cycle is controlled by amplitude of V_y.



2. Multiplier. Building the circuit from the block diagram shown in Fig. 1 is straightforward. A_1 is inverting, unity-gain amplifier. A_2 serves as integrator. Three transistors form standard Schmitt trigger. Four transmission gates provide a practical switching circuit arrangement for $\pm E$, $\pm V_x$. Inverting operational amplifier A_3 ensures that $+E$ is equal in magnitude to $-E$.

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$$V_a = V_x V_y / E \quad (5)$$

This condition is met by wiring the Schmitt trigger to engage not only the $\pm E$ ports but also the $\pm V_x$ ports of the circuit in Fig. 1a as well.

The block diagrams of Fig. 1 are therefore easily transformed into the practical circuit of Fig. 2. Note that voltages $\pm E$ are the feedback voltages to the summing integrator network at the input to A_2 necessary to ensure that $t_{on} - t_{off}$ is proportional to V_y. In essence, this part of the circuit is an oscillator, excited by V_y and driven by $+E$ or $-E$ feedback.

Also, although V_y controls the duty cycle, the basic oscillator frequency is virtually independent of it. (Note than when $V_y = 0$, $t_{on} = t_{off} + 0$).

The Schmitt trigger used is standard. The low-pass filter RC smooths out any transients that are caused by the switching process. Four complementary-metal-oxide-semiconductor transmission gates implement a practical switching circuit.

As suggested by Eq. 4a, this circuit does require that the magnitude of $-E$ tracks that of $+E$. Inverting op amp A_3 generates the mirror voltage required. □

Diode sensor and Norton amp control liquid-nitrogen level

by V. J. H. Chiu
National Research Council, Ottawa, Canada

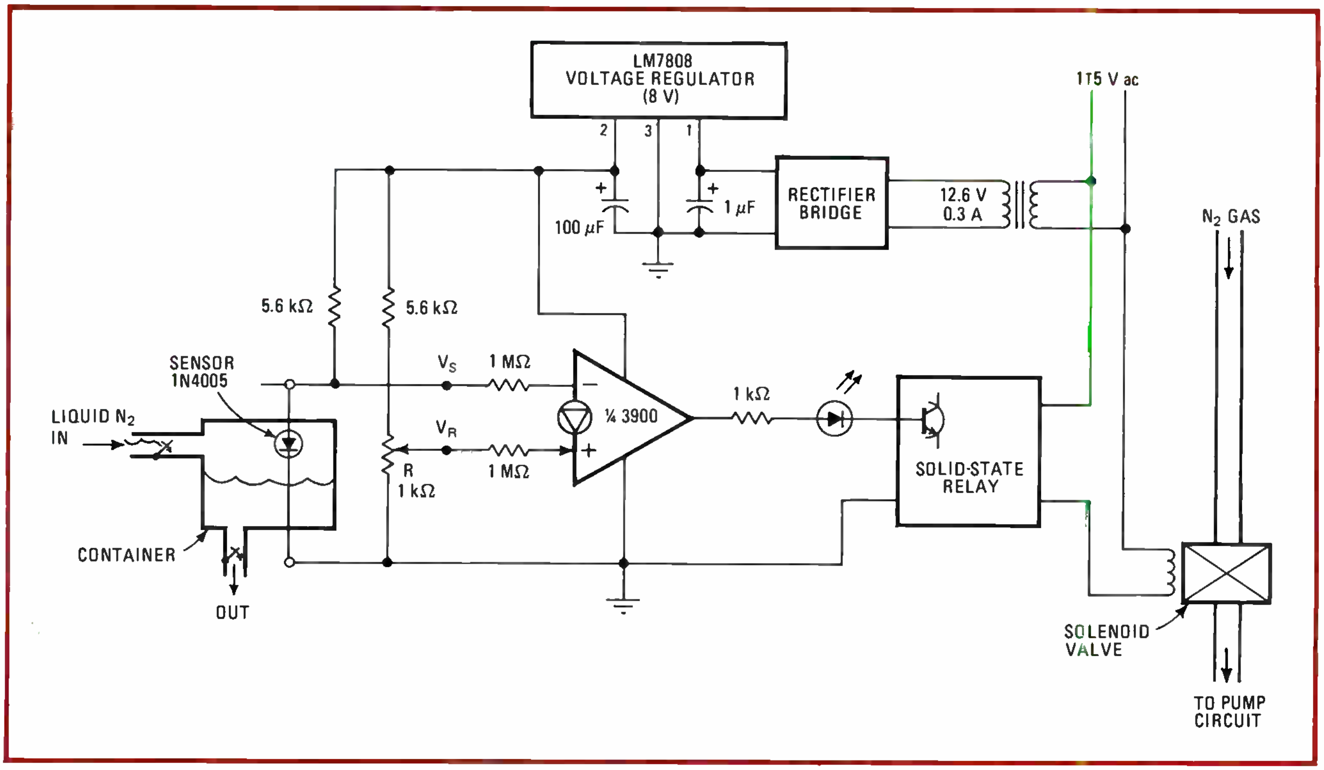
In parametric amplifier and other cryogenic applications, it would be handy to have an inexpensive sensor and controller of the level of liquid nitrogen. One can be built around a standard silicon diode and a Norton (current) amplifier.

The circuit's operation is based on the principle that the diode's junction voltage increases from 0.7 volt at room temperature to 1.05 v in liquid nitrogen (liquefaction temperature: $-196°C$). This voltage change is used to activate the amplifier, which controls a solenoid valve. The valve regulates a nitrogen-gas supply, which pumps liquid nitrogen from a reservoir to the desired container that houses the sensor.

The controller is shown in the figure. The sensor is placed in the container at any desired level. When liquid nitrogen rises to this level, voltage V_S reaches the preset voltage V_R almost instantly, and the output of the 3900 Norton amp becomes zero, closing the valve. When the liquid nitrogen falls below the desired level, V_S drops below V_R, and the valve opens.

Circuit sensitivity is adjusted by R. The diode need not be completely immersed in the liquid nitrogen, for its range is such that liquid as much as 2 inches below it will start the refilling of the container. Frequent cycling is thus avoided. The state of the solenoid valve may be determined by observing the light-emitting diode. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



Fixing the nitrogen level. When liquid-nitrogen level in container is below the diode position, solenoid is turned on and pumps in more N_2. When level reaches that of diode, its junction voltage jumps from 0.7 to 1.05 V, turning off solenoid and stopping N_2 inflow.

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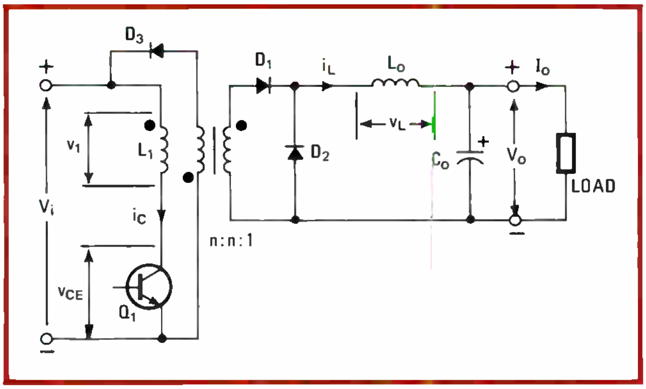
Low-cost forward converters ease switching supply design

Simplified circuitry built around novel transformer converts dc power up to kilowatt range

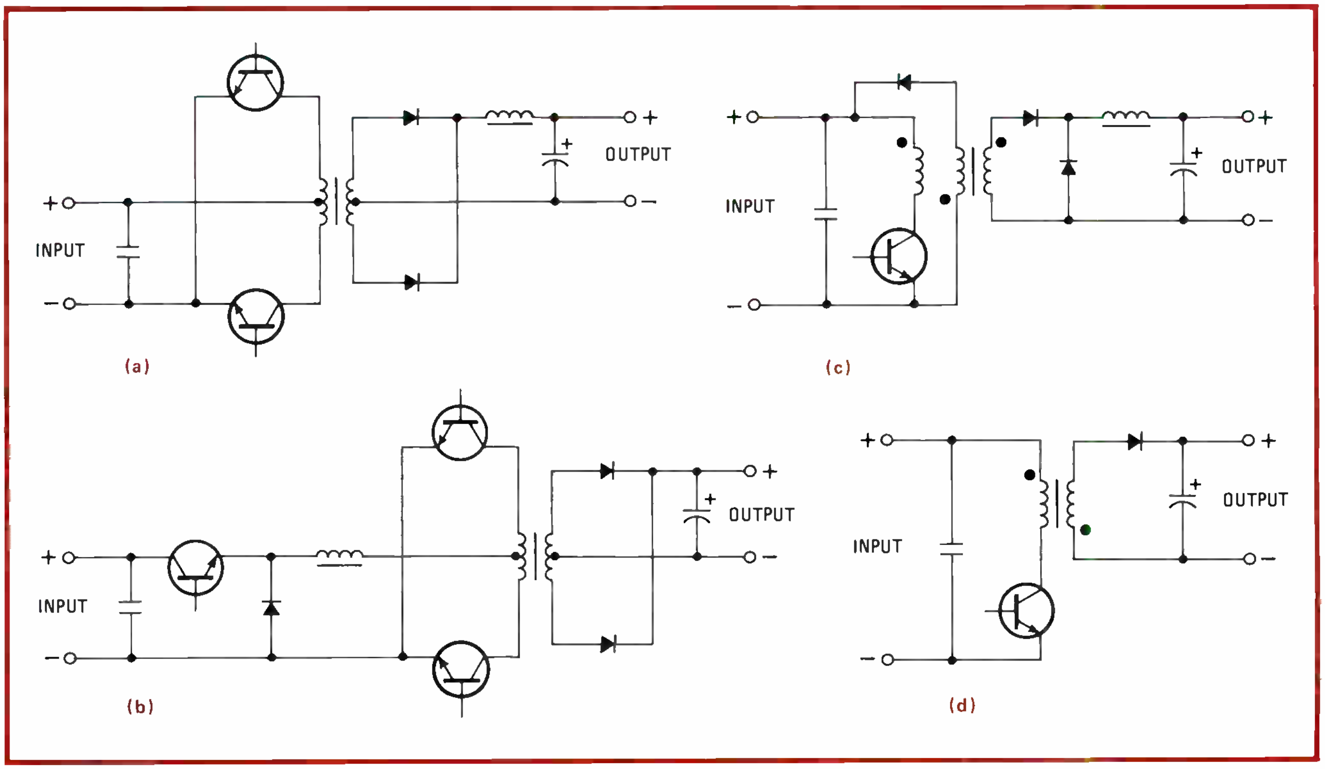
by Kees van Velthooven and Hugo Koppe, *N V Philips Semiconductor Laboratory, Nijmegen, the Netherlands*

☐ Switching power supplies are winning out over linear types because of their higher conversion efficiency, which also makes them smaller and cooler. And as the variable switching element of the supply, transformer-isolated, base-controlled dc-dc converters are winning out over series pass transistors. Transformer isolation of the input and output of course makes for safer operation, while use of a converter allows the output voltage to be greater than the input. In addition, such an approach reduces noise.

Now, the development of the forward and the double forward converter makes this approach even more attractive. These two circuits cost less than other transformer-isolated versions and are inherently easier to design. Furthermore, double forward converters, which have been built with output power in the kilowatt range, have a faster transient response and use smaller compo-



2. Forward converter. A special three-winding transformer is the key to this highly efficient one-transistor converter. A demagnetizing winding tightly coupled to the primary, along with diode D_3, prevents the transformer core from saturating when Q_1 is cut off.



1. Isolated. The push-pull converter (a), switching regulator followed by an unregulated converter (b), forward converter (c), and ringing-choke converter (d) isolate the input dc from the regulated output voltage. A forward converter resembles an isolated switching regulator.

nents than the other types.

Figure 1 shows the various transformer-isolated converter circuits. The push-pull converter (Fig. 1a) is the most widely used, although it suffers from the disadvantage of collector current peaking if its transformer saturates when there is a dc unbalance or a sudden rise in load. This drawback becomes even more serious with lower-loss core materials, which promote saturation-limited rather than loss-limited transformer design.

One approach to preventing collector current peaking employs a switching regulator combined with an unregulated converter (Fig. 1b). The switching regulator effectively limits any voltage surges that could unbalance the switching transformer. However, the circuit is complex and needs separate base drives for the regulating transistor and the unregulated transistor converter.

The forward converter (Fig. 1c), first designed in 1974, is now finding its way into power supplies. It is almost as simple as the low-efficiency, one-transistor ringing-choke supply (Fig. 1d), yet its ripple and its output capability are comparable to those of the push-pull converter. In addition, the forward converter does not have the push-pull converter's problem of dc unbalance in the transformer core, because transistor conduction occurs only once per converter cycle. Moreover, there is less flux peaking in its output transformer during load transients, and there is no interaction between the magnetizing and load currents.

Even more recent is the double forward converter. This type, which will be discussed later, is suitable for high-power applications.

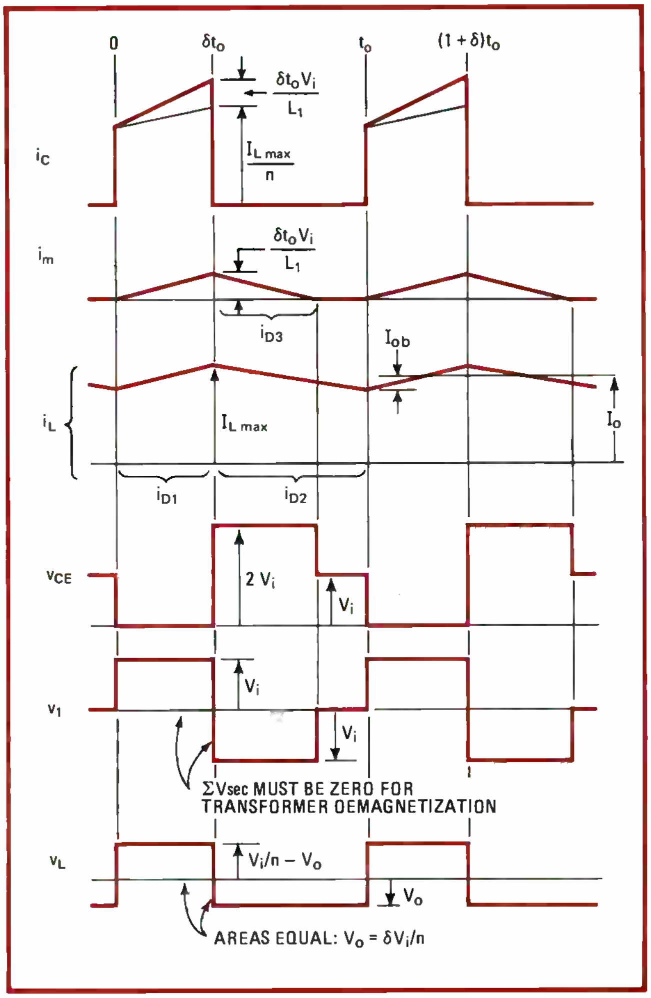
The table gives the behavior of the forward, double forward, and push-pull converters and the size of their components, assuming identical outputs.

The forward converter

The forward converter, whose schematic and waveforms are shown in Figs. 2 and 3 respectively, needs only one transistor for load switching. This is a tremendous advantage in view of the high cost of high-voltage switching transistors.

When Q_1 is switched on by a positive pulse at its base, rectifier D_1 starts to conduct, and energy is passed to output choke L_o and the load. During this stage, choke current i_L is rising. At the same time, magnetizing current begins to build up in the transformer primary. When the pulse at the base of Q_1 goes to zero, Q_1 is switched off, i_L falls, and part of the energy stored in L_o is transferred to the load through flywheel diode D_2. Meanwhile, magnetizing current continues to flow through the demagnetizing winding and D_3, a fast soft-recovery diode that doubles as a collector voltage clamp. Because choke current flows continuously, output ripple is low.

Before Q_1 is switched on again, the magnetizing current must have reached zero, or transformer saturation will occur; that is, with the primary-to-demagnetizing-winding turns ratio assumed to be unity, the transistor duty cycle, δ (the on time of the transistor divided by the cycle time of the converter), must not exceed 0.5. As the V_{CE} waveform shows (Fig. 3), the peak collector voltage is $2V_i$ (ignoring some additional voltage due to



3. Forward-converter waveforms. These waveforms are valid for ideally coupled windings and zero transistor switching times. Magnetizing current is shown cross-hatched. Peak collector voltage is $2V_i$ for primary-to-demagnetizing-winding turns ratio of unity.

ringing). To ensure smooth transfer of the magnetizing current, the primary and demagnetizing windings must be tightly coupled.

In comparison, in push-pull converter transformers the magnetizing current flows alternately in the primary and the secondary. Tight coupling between these windings leads to complex split-winding constructions owing to the necessity for interleaving and isolating windings. Forward-converter transformer design, on the other hand, is relatively simple because tight coupling between the primary and secondary is not necessary.

As seen from the V_L waveform (Fig. 3), the converter's dc output voltage is:

$$V_o = \frac{\delta V_i}{n}$$

where n is the primary-to-secondary turns ratio of the transformer. This relation holds for an uninterrupted choke current. At light load, an interrupted choke current occurs and V_o tends to rise, as is the case with all other converter types.

The boundary value of output current below which the choke current becomes interrupted is:

$$I_{ob} = \frac{V_i t_o \delta}{n L_o 2}(1-\delta)$$

where t_o is the converter cycle time. Below this current level, a large change in δ must occur to maintain regulation. This requires a high open-loop gain from the regulating circuit that controls the base drive of the switching transistor. The value of I_{ob} (which in turn determines the inductance of the output choke) is, therefore, an important design parameter. Normally, I_{ob} is 0.05 to 0.1 times the rated load current.

As with any converter type, the base-drive circuit for the switching transistor must be carefully designed to minimize conduction and switching losses.

To repeat, the merits of the forward converter are:

- Better transistor utilization—because energy still flows into the load while the transistor is off—and lower output ripple than with the ringing-choke converter.
- Simpler circuitry and easier transformer design than with the push-pull converter.

Output ripple

In most switching supplies, high-value output capacitors are used to reduce to acceptable levels output voltage transients caused by abrupt load changes. Therefore the output ripple depends almost entirely on the equivalent capacitor series resistance, ESR, and inductance, ESL, of the filter capacitance, rather than on the value of the filter capacitance itself. Figure 4 shows an equivalent circuit of an output filter for a switching regulator.

For the forward converter, the peak-to-peak output ripple, $V_{r(pp)}$, divided by the output voltage is:

$$\frac{V_{r(pp)}}{V_o} = \frac{ESL}{\delta L_o} + \frac{ESR(1-\delta)t_o}{L_o}$$

In comparison, the ripple equation for the push-pull converter is:

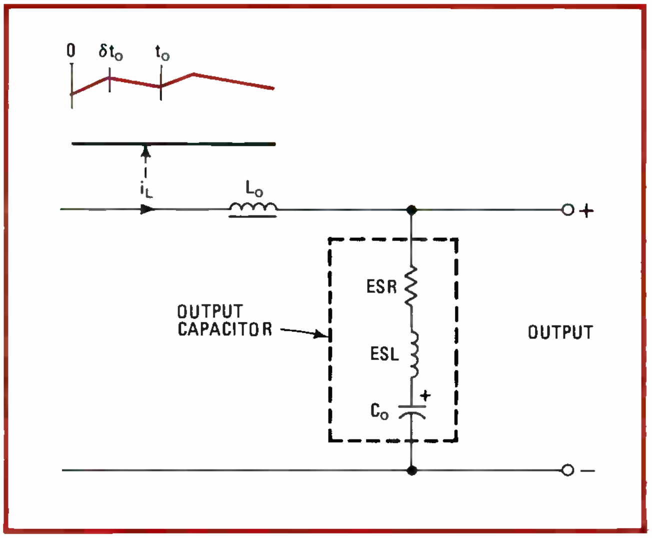
$$\frac{V_{r(pp)}}{V_o} = \frac{ESL}{2\delta L_o} + \frac{ESR(1-2\delta)t_o}{2L_o}$$

If identical output capacitors are taken for both cases, and if the output voltage and power are assumed to be equal, the ripple voltages will not greatly differ. With present-day, low-impedance electrolyte capacitors, a ripple of less than 1% is readily attainable for both converter types.

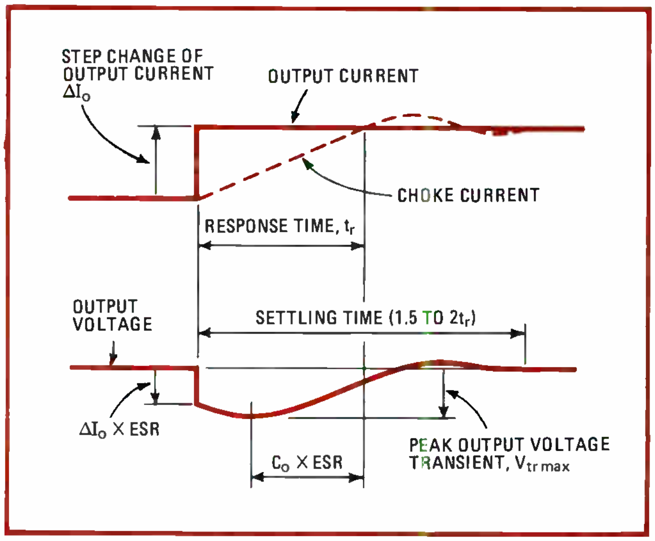
Switching power supplies respond much more slowly to load transients than linear supplies because the current through the choke in series with the output (Fig. 4) cannot change instantaneously. The difference between the choke and load currents must flow through the output capacitor, generating the voltage transient shown in Fig. 5. Output voltage settling time is 1.5 to 2 times the response time, t_r, which is the time required for the choke current to adjust to the new value of the load current. The peak output voltage transient, $V_{tr\,max}$, depends on the values of C_o and ESR, its minimum value being equal to $\Delta I_o \times ESR$. High-value, low-impedance capacitors are therefore essential.

The magnetizing current in the output transformer of the forward converter flows in only one direction (see the i_m waveform in Fig. 3), in contrast to that in the push-pull converter, and thus its core is unilaterally rather than bilaterally magnetized. With the low-loss ferrite cores now available, transformer design is based mostly on the magnetic flux permitted in the core.

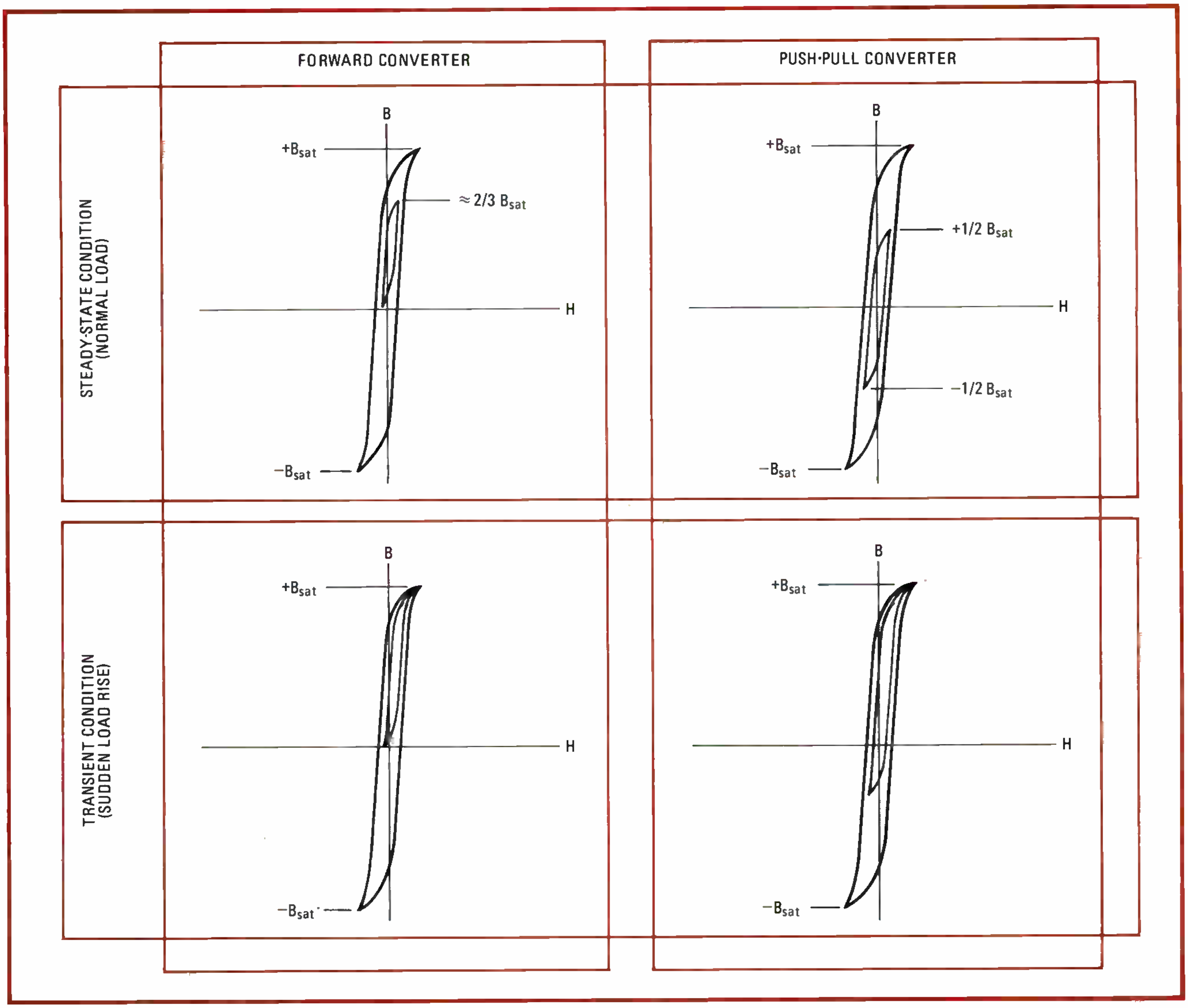
If the push-pull converter's operation could be perfectly balanced, then its core would work close to saturation and its size could be half that of the forward converter. But because of flux peaking during transients (Fig. 6) and the possibility of unbalanced operation, no great reduction in core size is obtained. However, although it can be shown that the peak flux increase due to transients is approximately 100% in the push-pull converter, compared with 50% in the forward converter,



4. Output ripple. Shown is the equivalent ac circuit of the output filter for either a forward or a push-pull converter. Since the output capacitor must be large to meet output voltage transient specifications, output ripple depends almost entirely on the equivalent series resistance and inductance, ESR and ESI, respectively.



5. Transient behavior. In forward and push-pull converters, the current through the filter choke cannot instantly follow a step change in output current. The difference between choke and output currents flows into the output capacitor, causing a slowly decaying transient whose amplitude is $\Delta I_o \times$ ESR or larger.



6. Hysteresis. In a forward converter, flux density, B, of the transformer swings between 0 and 2/3 B_{SAT}, unlike the case of a push-pull converter, where flux density operates between $\pm\frac{1}{2}B_{SAT}$. As a result, the forward converter is less susceptible to load transients than the push-pull converter, which can be driven into core saturation, causing collector current peaking.

COMPARISON OF FORWARD AND PUSH-PULL CONVERTERS (EQUAL OUTPUT VOLTAGE AND POWER)

	Forward converter	Double forward converter	Push-pull converter
Output voltage equation	$\delta V_i/n$	$2\delta V_i/n$	$2\delta V_i/n$
Transformer size	1	2 × 0.5	1
Choke size (equal boundary output currents)	1	0.3	0.6
Output capacitor size (equal output voltage transients)	1	0.3	0.6
Number of switching transistors	1	2*	2*
Number of output diodes	2	3†	2
Response time	1	0.3	0.6

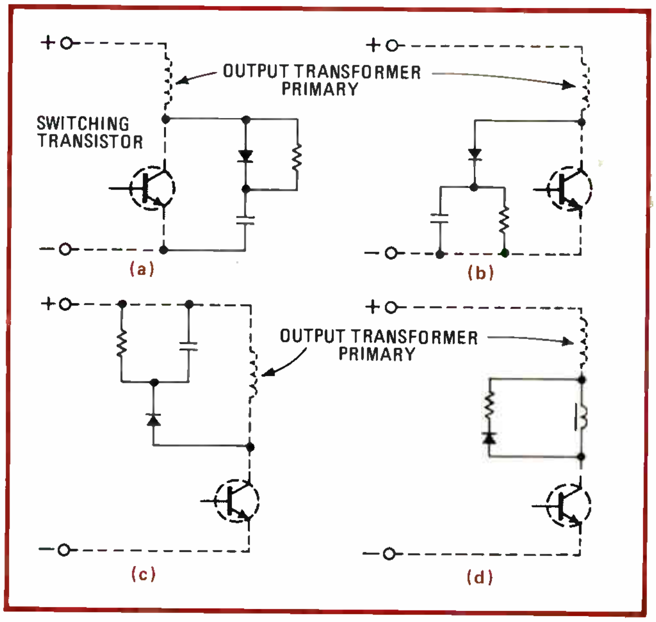
*Required collector current rating is half that for forward converter.
†Required flywheel diode reverse voltage rating is half that for forward converter.

transformer size is about the same for both types.

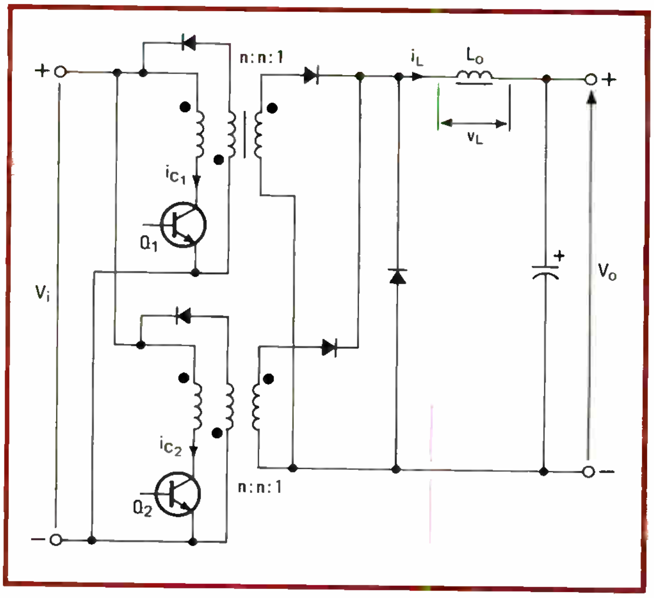
Since switching supplies run at high frequencies, fast output diodes are necessary to avoid large diode reverse-recovery currents, which could cause high diode turn-off power losses and high turn-on peak collector currents. Diode reverse-recovery times should be at most approximately 100 nanoseconds, and preferably less. Soft-recovery properties are necessary to minimize electromagnetic interference and diode turn-off voltage surges, both of which can jeopardize the diodes themselves.

Epitaxial diodes or, for low output voltages, Schottky barrier diodes should be used for switching supplies. The reverse-voltage rating required varies between $4V_o$ and $5V_o$, depending on output voltage, diode voltage drop, and ringing suppression.

Protection networks are indispensable for keeping a supply's switching transistor within its safe operating area. In push-pull converters, RC networks across the switching transistors or the transformer primary provide protection. A low-value resistor (to keep the network



7. Protection. Four protective networks used with forward converters to keep the power transistor within its safe operating area are dV_{CE}/dt limiting (a), peak-rectified clamping (b), clamping with reduced losses (c), and turn-on di_C/dt limiting (d).



8. Doubling up. The double forward converter consists of two forward converters switched alternately. The waveforms produced are similar to those of the single forward converter. However, output power and ripple frequency are doubled and transient response is improved over the one-transistor version.

time constant low) will limit the turn-on peak collector current to some extent, but high power losses will result because of the large capacitor charge and discharge currents. Forward converters, on the other hand, offer much greater freedom in network design, and the protection networks possible ensure safe turn-on and turn-off collector current with acceptable loss.

One of the most successful types, the dv_{CE}/dt limiter (Fig. 7a), ensures that collector current has dropped to the cut-off level before collector voltage exceeds the rated V_{CEO}. It does so by decreasing the collector voltage rise rate to between 400 and 800 volts per microsecond. For effective action, the capacitor should discharge almost fully during transistor conduction.

The peak-rectifier clamper (Fig. 7b, 7c) limits the peak collector voltage to about twice the converter dc input voltage by suppressing voltage surges due to inductive switching. A third kind, the di_C/dt limiting network (Fig. 7d), prevents turn-on dissipation. It is used where the transformer has low leakage inductance, which together with the collector current would otherwise rise abruptly because of the winding capacitance charge current and the output-diode reverse recovery.

The diodes in these protective networks are high-speed, soft-recovery types. They cause negligible surge voltage and electromagnetic interference.

Switching transistor choice is governed by the dc input voltage and the transformer throughput power. With any of the recommended networks, the required V_{CE} rating is twice the converter dc input voltage plus some additional overvoltage (approximately 50 v) for ringing. The peak collector current is the sum of the reflected peak choke current, which equals $(I_o+I_{ob})/n$, and the peak magnetizing current; depending on transformer size, the peak magnetizing current is 0.01 to 0.1 times the reflected peak choke current.

With present-day state-of-the-art components, forward converters can be built to handle up to 500-watt outputs. Higher power can be obtained by paralleling transistors or transistor-transformer pairs. Where the power requirement exceeds 1,000 w, the double forward converter (Fig. 8) becomes attractive. This circuit consists of two forward converters with a common choke, the converters being switched alternately by base drives to Q_1 and Q_2 that are 180° out of phase.

Doubling output power

Total output power of the double forward converter is twice that delivered by the individual converters. Because ripple frequency is doubled, lower values of filter capacitance and inductance are needed. Also, load transient response is much faster than that of the forward converter. These improvements, however, are bought at the cost of somewhat greater circuit complexity and a more intricate base drive. The latter remains simpler than that of push-pull circuits, since no measures are needed to counter unbalance.

Performance is similar to that of the push-pull converter, but with two advantages: there is no interaction between magnetizing current and output current at low output power, and the circuit is hardly sensitive to dc unbalance. As in the case of the push-pull converter, the output voltage is:

$$V_o = \frac{2\delta V_i}{n}$$

As in the case of the forward converter, a boundary value of load current exists:

$$I_{ob} = \frac{V_i t_o \delta}{n L_o 2}(1-2\delta)$$

below which output regulation will worsen. □

Determining the dynamic range of logarithmic amplifiers

by Brent Bardsley
Department of Bioengineering, University of Utah, Salt Lake City

The dynamic range of a logarithmic amplifier can be easily determined by observing its response to an exponentially decaying input voltage. The test procedure is based upon the principle that when an exponential waveform, e^x, is operated upon by its inverse function, log(x), the product that appears at the amplifier's output is a linear function of x. Thus the dynamic range, not surprisingly, will be directly proportional to the time during which the amplifier generates a linear response.

The graph in Fig. 1 plots the input/output characteristic of a typical log amp. Its dynamic range is easily found by plotting its input-voltage values on a logarithmic scale, as shown. The response is linear over an input-signal range of 60 decibels for this amplifier. The output dynamic range is 12 dB.

Although the methods for testing linear amplifiers are not valid for logarithmic amps, the dynamic range may be found just as easily for these nonlinear devices. A response similar to the one in Fig. 1 can be simply constructed, and without the need for point-by-point plotting of the input-to-output relation, by using an oscilloscope and a periodic exponential waveform.

Figure 2 shows how it is done. Simply differentiate the output of a square-wave generator to generate Ae^{-x} and then introduce this signal to the input of the log amp. Trigger the scope on the rising edge of the square wave, and observe the output of the log amp. The dynamic range is defined by the equation:

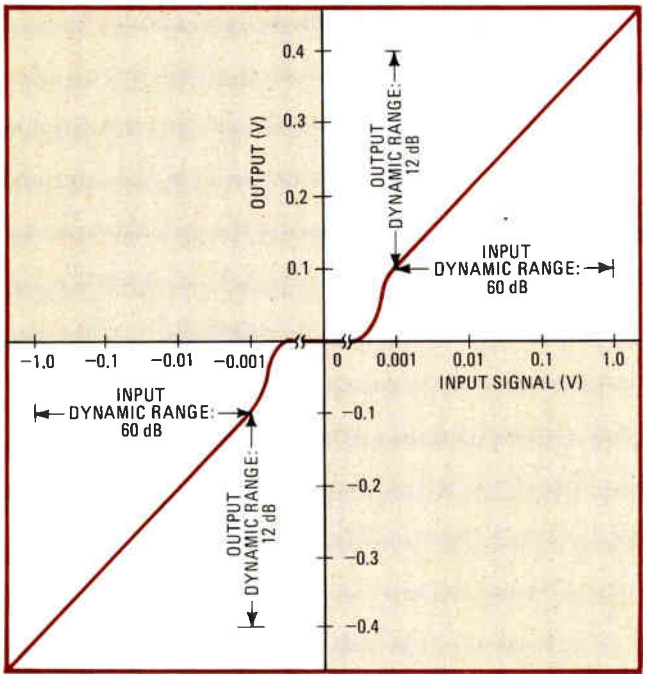
$$D\,(\text{dB}) = 8.69\ t/RC$$

where RC is the time constant of the differentiator and t is the time, measured with the aid of the scope, during which the response is linear.

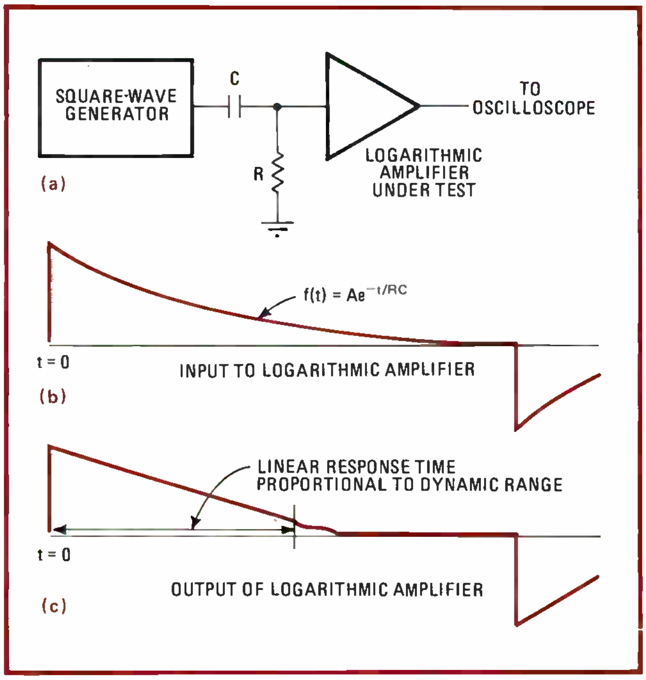
To serve as an effective differentiator, the actual time constant should be at most one tenth the value of the time, corresponding to the dynamic range measured over one period of the input square wave. For example, if the dynamic range is expected to lie in the region of 60 dB, and a square wave input frequency of 100 kilohertz is to be used (t = 10 microseconds), then:

$$RC_{max} = \frac{8.69}{60}\ \frac{(10)(10^{-6})}{10} = 0.145\ \mu s$$

In addition, the time constant should be selected so that the output impedance of RC is not so large that it will be loaded down by the log amp. Otherwise, a buffer amplifier may have to be inserted between the two. □



1. Characteristic. Input dynamic range of typical logarithmic amplifier is 60 decibels; the output range is 12 dB. Both of these ranges are easily measured if input-signal values are plotted on a logarithmic scale. Dynamic-range measurement circuit discussed in text can generate a response similar to the one shown here.



2. Measurement. Exponential waveform Ae^{-x} is processed by logarithmic amplifier (a), and the resulting output waveform proves to be linearly proportional to x. Dynamic range will vary directly with the time the amplifier's output is in the linear region, as described in the text. Typical input and output waveforms (b,c) are shown.

Calculator program analyzes transmission-line problems

by Jesse L. Peters
Eddyville, Kentucky

This SR-56 program aids in the lossless-case analysis of many transmission-line problems by determining the value of the voltage and current transfer functions at any point along the line, and it therefore detects impedance changes caused by varying any system parameter.

The program generates results that are far more accurate than those produced by a Smith Chart. It is especially useful in high-frequency applications (100 megahertz or more), where the calculator will produce results that complement those generated using the chart and a slotted line. Although the program space of the calculator is limited to 100 steps, it is sufficient for storing the more complex equations. The relatively simple ones, if required, can be solved manually.

The program is based on the classical voltage and current equations derived for a lossless transmission line:

$$V(x,j\omega)=\frac{V_o}{1+[(Z-Z_o)/(Z+Z_o)]e^{-2\theta}}\left[e^{-\gamma x}+\left(\frac{Z-Z_o}{Z+Z_o}\right)e^{-2\theta}e^{\gamma x}\right] \quad (1)$$

$$I(x,j\omega)=\frac{V_o/Z_o}{1+[(Z-Z_o)/(Z+Z_o)]e^{-2\theta}}\left[e^{-\gamma x}-\left(\frac{Z-Z_o}{Z+Z_o}\right)e^{-2\theta}e^{\gamma x}\right] \quad (2)$$

where:

- x = the distance along a line of impedance Z_o as measured from the voltage generator, V_o
- $\theta = \gamma D$
- $\gamma = j\omega(LC)^{1/2} = j\omega/v$
- D = line length
- ω = radian frequency
- L = distributed inductance of the line
- C = distributed capacitance of the line
- $v = 1/(LC)^{1/2}$ = the line's velocity factor.

Substitution of the reflection-coefficient equation:

$$\Gamma = (Z-Z_o)/(Z+Z_o) \quad (3)$$

into Eqs. 1 and 2 yields:

$$K_v(x,j\omega) = \frac{e^{-\gamma x} + \Gamma e^{-2\theta}e^{\gamma x}}{1 + \Gamma e^{-2\theta}} \quad (4)$$

$$K_I(x,j\omega) = \frac{e^{-\gamma x} - \Gamma e^{-2\theta}e^{\gamma x}}{1 + \Gamma e^{-2\theta}} \quad (5)$$

These are the equations evaluated by the program.

Either x, ω, v, D, or Γ may be designated the independent variable. When each is placed into Eqs. 4 and 5, the voltage and current at any point on the line is found, assuming the generator is a unity-value source.

Normally, K_v is determined first. K_I may then be found by modifying one instruction step in the program.

The program yields results in rectangular coordinates, with the real part of the function contained in register 7, and the imaginary part in register 6, but these can be easily converted to polar form if the impedance at any point on the line is desired.

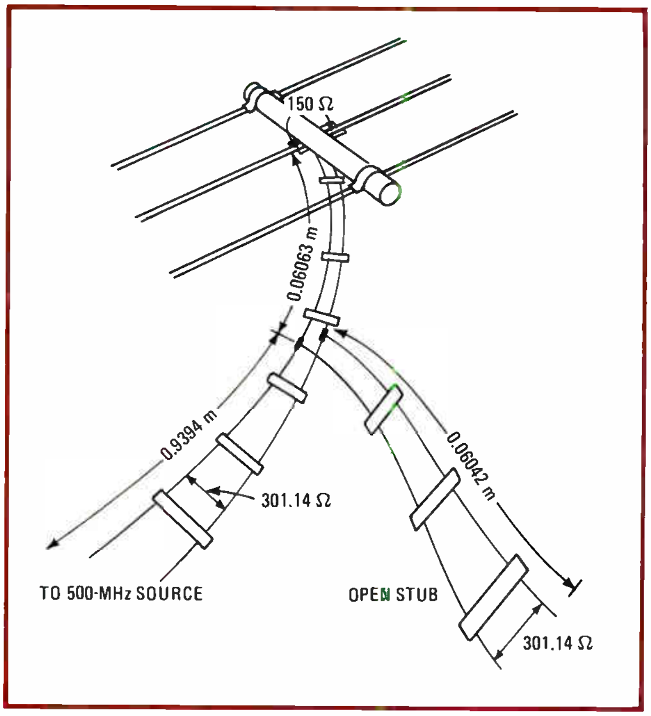
The following stub-matching example will illustrate the usefulness of the program. A two-conductor transmission line, 1 meter long, with an impedance of 301.14 ohms (determined from the line's L and C constants and the line geometry) and a velocity factor of 1.9924×10^8 m/second must be matched to a load impedance (Z_L) of 150 Ω when driven by a 500-MHz source. The program will aid in finding the length of the stub required and its position along the line. The validity of the program will be checked in this example by assuming that the exact stub-to-load distance required for a perfect match is known beforehand.

From Eq. 3, Γ is found to be -0.335017954. The values for ω, v, D, and Γ are then entered into registers 1 through 4, respectively. The stub-to-load distance, x', is found from the equation:

$$\tan^2[(w/v)x'] = (Z_xZ_o^2 - Z_o^2Z_L)/(Z_LZ_o^2 - Z_xZ_L^2) \quad (6)$$

where Z_x is the desired impedance of the line at this point, 301.14 Ω. The value of x' is found to be 0.06063 meter from the load or 0.9394 m from the source. Thus $x = 0.9394$ m, and this value is entered into register 0.

Pressing R/S initiates the calculation for K_v at $x = 0.9394$ m. After a few seconds the real part of the voltage transfer function (Re K_v) is displayed; the imaginary part (Im K_v) is stored in register 6. To display K_v in



Optimum coupling. SR-56 transmission-line program confirms that, given a stub-to-source distance (x') of 0.06063 m, stub length must be 0.06042 m in order to match a 301.14-Ω transmission line to a 150-Ω load. In a practical example, the stub-to-load distance would be the independent variable, and program would find impedance changes at any point on line due to changes in x'.

the standard polar form, $re^{j\theta}$, the following should be entered immediately after Re K_v is displayed: x⪰t, RCL 6, *f(n), R→P. Theta (θ) will be displayed, and r will be stored in the t register. The value of r may be displayed by pressing x⪰t, ÷, (Z_o), =. K_I may be found in similar fashion by changing instruction step 30 from the NOP to the +/− operator, repeating the procedure, and dividing the answer by Z_o. Thus the program will generate:

$$V_x = -0.7649 - j1.5503 = 1.7287e^{j4.2540}\ \text{V}$$

$$I_x = 0.004682e^{j3.6356}\ \text{A}$$

from which:

$$Z_x = 369.22e^{j0.6184} = 300.84 + j214.05\ \Omega$$

This result confirms that the resistive component of the line impedance at $x' = 0.06063$ is 301.14 Ω, to within 1%, and that to match the line to the load a stub having a reactance of −214.05 Ω is required. The impedance at $x' = 0.06063$ is repeated every half wavelength in a direction toward the generator, so the line can be matched with the same stub at any of these points.

The reactance is negative and thus requires an open stub. Its length is found from:

$$Z_x' = -jZ_o \cot(\omega x''/v) \tag{7}$$

where Z_x' is the stub impedance, 214.05 Ω. The stub length, x'', is found to be 0.06042 m. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.

SR-56 TRANSMISSION-LINE PROGRAM

Locations	Codes	Keys	Comments
00 – 01	33 00	STO 0	
02 – 04	34 04 32	RCL 4 x⪰t	can be STO 0 through STO 4, depending upon line parameter varied.
05 – 08	57 07 08 93	*subr 78 +/–	
09 – 11	26 02 32	*f(n) P→R x⪰t	
12 – 15	84 01 94 32	+ 1 = x⪰t	compute $1 + \Gamma e^{-i2\omega D/v}$ store in R_6 and in R_7 as R_7 (e^{iR_6})
16 – 17	34 08	RCL 8	
18 – 19	26 03	*f(n) R→P	
20 – 22	33 06 32	STO 6 x⪰t	
23 – 26	33 07 20 64	STO 7 *1/x X	
27 – 29	34 04 94	RCL 4 =	
30	46	*NOP	to find K_V, use NOP here; to find K_I, use +/– here
31	32	x⪰t	
32 – 35	57 09 00 74	*subr 90 –	compute $(1/R_7)e^{i(\widetilde{90}-R_6-\widetilde{78})}$
36 – 38	34 06 74	RCL 6 –	
39 – 41	57 07 08	*subr 78	$\widetilde{78}$, $\widetilde{90}$: result of subroutines 78 and 90, respectively
42 – 43	26 02	*f(n) P→R	
44 – 47	34 07 20 32	RCL 7 *1/x x⪰t	
48 – 50	34 06 84	RCL 6 +	
51 – 54	57 09 00 93	*subr 90 +/–	
55 – 58	33 05 34 08	STO 5 RCL 8	compute $(1/R_7)\,e^{-i(R_6+\widetilde{90})}$
59 – 62	33 06 34 09	STO 6 RCL 9	
63 – 66	33 07 34 05	STO 7 RCL 5	
67 – 68	26 02	*f(n) P→R	
69 – 71	35 06 32	SUM 6 x⪰t	
72 – 75	35 07 34 07	SUM 7 RCL 7	
76 – 79	41 42 02 64	R/S RST 2 X	
80 – 82	34 01 64	RCL 1 X	
83 – 85	34 03 54	RCL 3 ÷	subroutine 78: $2\omega D/v$
86 – 89	34 02 53 58	RCL 2) *rtn	
90 – 92	34 01 64	RCL 1 X	
93 – 95	34 00 54	RCL 0 ÷	subroutine 90: $\omega x/v$
96 – 99	34 02 53 58	RCL 2) *rtn	

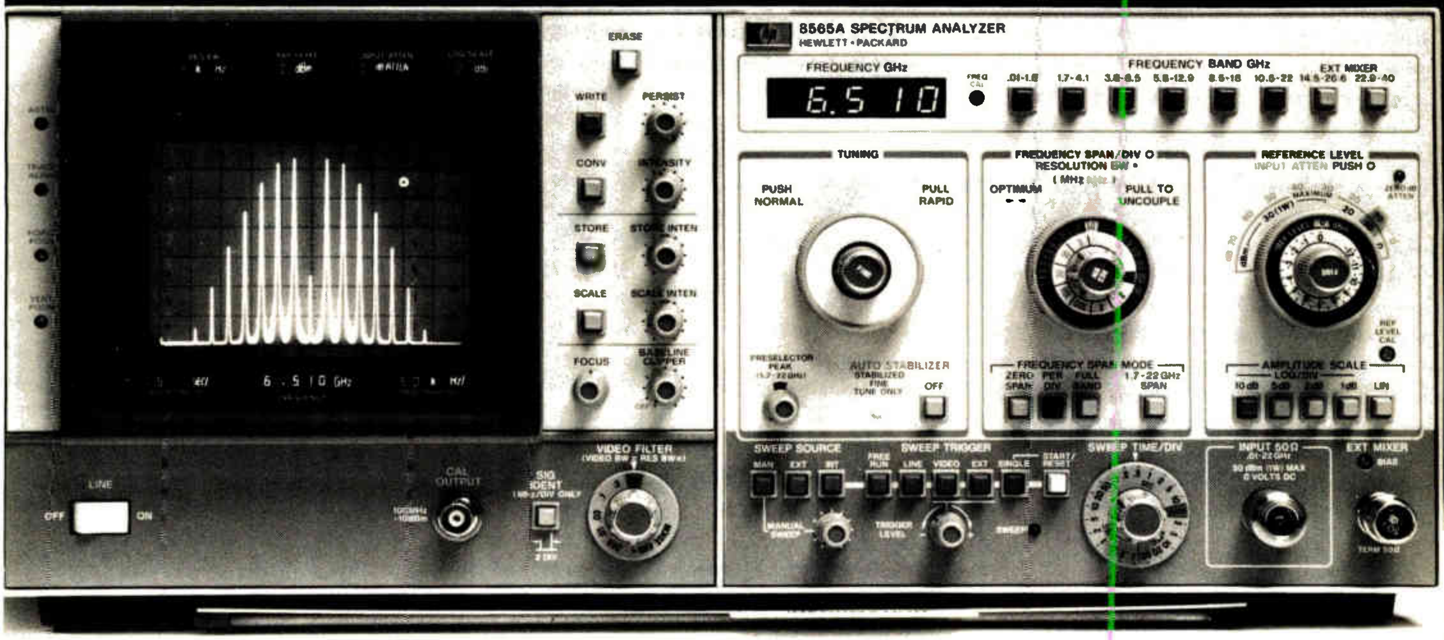
Instructions

- Key in program
- Initialize:
  RST, *RAD
- Enter radian frequency, velocity factor of line, the total line length, and the reflection coefficient:
  (ω), STO 1, (v), STO 2, (D), STO 3, (Γ), STO 4
- Enter the distance from source where voltage-transfer function will be calculated:
  (x), R/S → Re K_V will be displayed and stored in R_7
- Press RCL 6 to find Im K_V

Registers

R_1	ω
R_2	v
R_3	D
R_4	Γ
R_5	used
R_6	Im K
R_7	Re K
R_8	used
R_9	used
R_0	x

The performance you need. | The convenience you want.



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Frequency response is within ±1.2 dB to 1.8 GHz, and from ±1.7 dB at 4 GHz to ±4.5 dB at 22 GHz. These figures include all input circuitry effects as well as frequency band gain variations. Internal distortion products are 70 dB down from 10 MHz to 18 GHz; 60 dB, 18 to 22 GHz.

Resolution bandwidths from 1 kHz to 3 MHz are provided, with 100Hz optionally available. The resolution filters are all synchronously tuned to prevent ringing. For frequencies from 1.7 to 22 GHz, an internal preselector provides more than 60 dB rejection, permitting measurements of distortion products as small as 100 dB down.

As for convenience, the 8565A makes most measurements using just three controls: tuning frequency, frequency span and amplitude reference level.

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Circle 127 on reader service card

Engineer's newsletter

Bumps on chips prove a blessing in disguise

All IC chips used in the highly automatic tape-automated bonding method must have their input/output pads built up with special metallic layers or bumps. Such bumping has been tolerated up to now as a necessary evil. But now **several volume users are reporting 3% to 5% higher probe yields on bumped chips** as opposed to unbumped ones, says Tom Angelucci of International Micro Industries. This Cherry Hill, N. J., firm supplies both bonders and tape to users of the bonding process.

According to Angelucci, there are three variables that degrade probe yields on unbumped chips—the probe's contact resistance, the damage done to the pads by the probe, and residual oxides on the pads. Bumped wafers are protected against these accidents by their special metalization. What's more, the better passivation of the bumped chips is enabling a number of tape-automated-bonding users to go to lower-cost plastic packages. The improved chip hermeticity also gives added protection through subsequent assembly stages.

How to plot other neat frequency response curves

Remember the method for obtaining evenly spaced frequency plots on semi-log paper that Glenn Darilek advocated on this page late last year [*Electronics*, Nov. 10, p. 120]?

Well, an extension of it has now been proposed by Don Davis, who's president of Synergetic Audio Concepts in Tustin, Calif. Davis notes that by using the base 10, Darilek restricts his calculation to working in even decades, and **a more general relationship for evenly spaced intervals that's easily solved on any calculator with a y^x key** is:

$$\text{LFL}(\text{UFL}/\text{LFL})^{1/\text{N-1}}(\text{UFL}/\text{LFL})^{1/\text{N-1}} \text{ etc.}$$

where LFL is the lower frequency limit, UFL is the upper frequency limit, and N is the total number of plots desired, including the starting and finishing frequency.

For example, if 10 plots are desired between 50 and 10,000 Hz, the basic constant multiplier is $(10{,}000/50)^{1/9}$, or 1.8016. Use of this figure produces a plot with the following spacing: 50.00 Hz, 90.08 Hz, 162.30 Hz, 292.40 Hz, 526.81 Hz, 949.12 Hz, 1,709.98 Hz, 3,080.78 Hz, 5,550.47 Hz, and 10,000 Hz.

Samarium-cobalt magnets make powerful motors

Rare-earth permanent magnets of samarium cobalt have about 10 times the usable magnetic strength of conventional alnico magnets—an asset that's exploited in a research model of an aircraft actuator now in development at the Air Force Dynamics Laboratory, Wright Patterson Air Force Base, Ohio. **The actuator is driven by two small but powerful motors generating 4 hp each** and competitive in size and weight with less reliable hydraulic actuators ordinarily used in aircraft.

The high-strength magnets in these motors were developed for the laboratory by Karl Strnat of the University of Dayton's Research Institute. Samarium-cobalt magnets are still fairly expensive, says Daniel Bird of AFDL's flight control division, but he expects their price will drop because they are being used in more and more industrial machinery.

Jerry Lyman

Expect a great future from these stars of the screen.

Until the advent of fibre optics, photographic recording of information was performed by oscilloscopes plus external camera.

M-OV cathode ray tubes with fibre optic face plates have replaced both in one fell swoop. And, in so doing, they have improved recording quality enormously and even extended recording techniques into previously unheard of areas.

Fibre optic screens are made of bundles of small diameter glass fibres which carry light from the CRT interior to the external face plate without distortion. So, the image on the face plate is exactly as generated at the phosphor surface. No more, no less.

Parallax errors, common with conventional glass face plates, are a thing of the past.

This advantage is only the start.

Fibre optic light gathering ability is much greater, the risk of scattered light is reduced, and fibre optics perform much better in bright illumination conditions, like sunlight.

If you have no camera, you have no camera work. The recording paper is placed directly on to the cathode-ray tube and the recorded image is developed and fixed by ultra-violet exposure.

New applications for fibre optics are being discovered continuously, but they have already had a big impact on communications, computing, medicine, power, printing, transport and ultrasonic imaging. If you are in one of these industries you should know about fibre optic cathode-ray tubes.

If not, could this technical protégé be of use to you?

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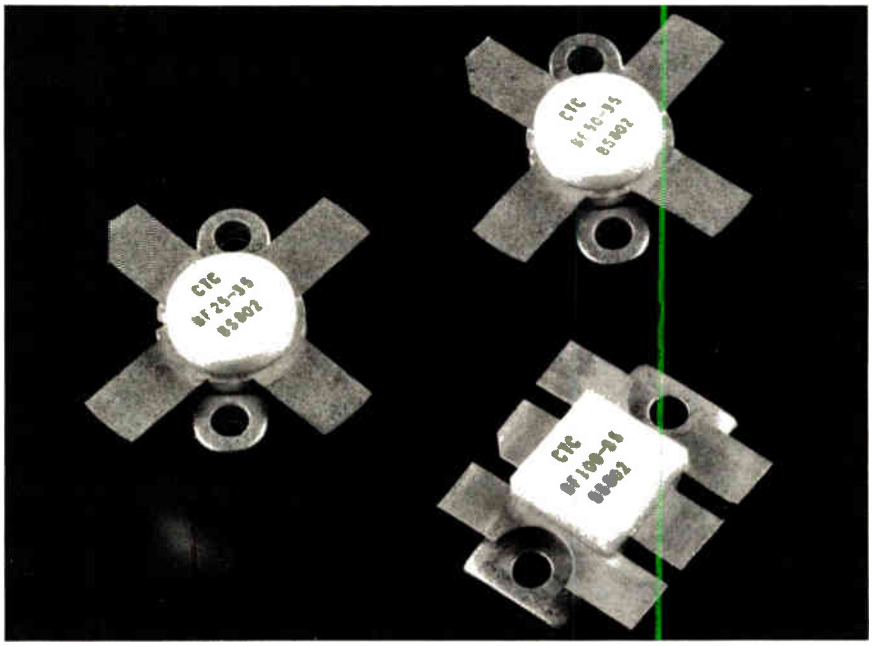
FETs move up in power and frequency

V-channel devices rated for up to 100 W cw at 175 MHz are easy to bias, hard to destroy

by William F. Arnold, San Francisco bureau manager



Having initially challenged the dominance of bipolar transistors at low powers and low frequencies, power field-effect transistors are now moving up to radio frequencies and 100-watt ratings. Employing vertical V-channel geometries for what it calls V-FET technology, Communications Transistor Corp. is making a trio of metal-oxide-semiconductor FETS suitable for rf amplifier applications. Designated the BF25-35, the BF50-35, and the BF100-35, the units can handle 25, 50, and 100 W of continuous-wave power, respectively. They are characterized for operation at either 80 or 175 MHz.

"The devices we're introducing represent the first generation of power FETs designed for rf circuit applications," declares Steven Ludvik, senior product engineer. Adds Danny Wong, military marketing manager: "They won't obsolete bipolar at all. Rather they give the circuit designer a new tool to use."

But what a tool they are. For one thing, a V-FET device gives the circuit designer "simplicity of biasing," Ludvik says. "It draws negligible dc input current, so biasing it and modulating it are much simpler than with bipolar devices."

The new V-FETS are rugged, too, compared with bipolar devices. Thermal runaway or breakdown is a problem with bipolar transistors, but FETs do not experience this condition, Wong says. Consequently, they are more tolerant of load mismatch than bipolar devices. And, on the linearity scale, where bipolars might be expected to have an edge, the new FETs feature a third-order distortion product similar to that of the same-sized bipolar device. However, the FET technology because of its "square-law-type" characteristics gives 5 to 10 dB less higher-order (fifth, seventh, and the like) distortion than bipolar units.

Noise performance is also good. Unlike bipolar transistors, where noise increases indefinitely with increasing bias current, a "FET is fairly flat when you bias it up because it is a majority-carrier device," Ludvik points out.

Key to the new V-FET's frequency and power performance is its vertical V-channel structure, Ludvik explains. "One-micron-and-less diffusion is easy to do" with a V-FET but difficult with planar devices, he says. These narrow diffusions yield the good frequency response, he explains. And being able to interconnect a large vertical area of tightly defined gates also produces the power levels, which, again, is hard to do with any planar process, whether in bipolar transistors or gallium-arsenide FETs, he points out.

The present 25-, 50-, and 100-W devices provide a maximum gain of 10 dB at 175 MHz. Breakdown voltage from source to drain is more than 65 V, and the source-to-gate breakdown voltage is more than 25 V. Typical on-resistance is less than 1 Ω measured at a 10-A drain current for the 100-W transistor.

Preliminary prices for 1-to-24 and 25-to-100 quantities are $37.50 and $33.75 for the 25-W unit, $48.50 and $43.65 for the 50-W FET, and $85 and $76.50 for 100-W device. Delivery time is four weeks. Large-volume prices will be announced later.

Communications Transistor Corp., 301 Industrial Way, San Carlos, Calif. 94070 [338]

a measurement range of −40°C to +300°C (−40°F to +600°F) and is available with more than 30 interchangeable probes for determining the temperature of surfaces, liquids, powders, air, and gases. Among its applications is electronic-design evaluation, in which the thermometer can check the temperature rise of components in an operating circuit.

The converter contains a cold-junction reference and automatic zeroing circuitry, which together limit total system error to 3°F (1.5°C). It will stand off voltages to 350 V dc on components under test.

DVM Division, William Wahl Corp., 12908 Panama St., Los Angeles, Calif. 90066 [353]

In-line rf wattmeter has dual displays

A pair of side-by-side analog meters allow the WV-552A in-line wattmeter to read forward and reflected power simultaneously. The meter, which covers the range from 20 to 230 MHz in three bands, has two ranges on each of its meters: 20 W and 100 W full scale for forward power, and 5 W and 20 W full scale for reflected power. Measurements on both meters are accurate within 5% of full scale. The WV-522A has an impedance of 50 Ω ±2% and a VSWR of no more than 1.15 over the entire frequency range. Supplied with M-type connectors, the instrument sells for $150.

For users who need only a dummy-load wattmeter, the WV-551A covers the frequency range from 1.9 to 512 MHz in one band and sells for $60. It has a single full-scale range of 15 W and a measurement uncertainty of 5% of full scale. The unit has a maximum VSWR of 1.15 at 500 MHz. Like the WV-552A, the WV-551A is supplied with an M-type connector. M-to-N and M-to-BNC adapters are available.

VIZ Test Instruments Group, VIZ Manufacturing Co., 335 E. Price St., Philadelphia, Pa. 19144. Phone Bob Liska at (215) 844-2626 [355]

TOPICS

Instruments

Hewlett-Packard Co., Palo Alto, Calif., has combined its model HP 8410 microwave network analyzer system with a desktop computer and programmable signal sources to form a system that can make error-corrected network measurements under program control. The system, designated the HP 8409A, covers from 110 MHz to 18 GHz and sells for $78,225. Current delivery estimate is 16 weeks. . . . **Ailtech, Farmingdale, N. Y.,** is offering its 7370 system noise monitor with an optional interface for the IEEE-488 instrumentation bus. The interface adds $875 to the price of the monitor. . . . **Philips Test & Measuring Instruments Inc., Mahwah, N. J.,** has reduced the prices on four of its pulse generators. The reductions, which the company says have been made to compensate for changes in currency-exchange rates, range from 2% to 11%. The 50-MHz PM 5712 has been dropped from $895 to $850; the PM 5715, a 50-MHz unit with variable rise and fall times, has been reduced from $1,115 to $1,050; the complementary-MOS-oriented PM 5716 has been slashed from $2,245 to $1,995; and the 100-MHz PM 5771 has been cut from $2,245 to $2,195. . . . **B & K Precision, Dynascan Corp., Chicago, Ill.,** has introduced a function generator, the model 3010, that sells for only $175. The unit covers the frequency range from 0.1 Hz to 1 MHz in six ranges. Its sine-wave distortion is less than 1% from 0.1 Hz to 100 kHz. Harmonics are more than 30 dB down at maximum output amplitude.

Semiconductors

Multiplexers get 20 dB better

8- and 16-channel bi-FET units combine 80 dB of isolation with low prices

When electronic data-acquisition systems meet the tough world of industrial control, the brunt of the burden is borne by the front end of the systems—usually their analog multiplexers. The challenge of surviving in the electrically hostile industrial environment while delivering precision analog levels on command has been the prime motivating force behind the development of a succession of multiplexer technologies: complementary metal-oxide-semiconductor, protected C-MOS, and a combination of junction field-effect transistors with bipolar circuitry (bi-FET).

Now Precision Monolithics Inc. has taken the evolution one step further with a family of four protected bi-FET multiplexers that combine small size and low cost with typical input-to-output and channel-to-channel isolation ratings of 80 dB—some 15 to 20 dB better than anything else currently available commercially.

The four multiplexers come in two sizes: 8 and 16 channels. The MUX-08 is a standard 8-input, 1-output device. The MUX-24 is really a pair of 4-channel multiplexers ganged together and controlled by the same channel-selecting input code. Since the two outputs of the MUX-24 are mutually isolated, the unit can be used in a 4-channel differential system to acquire small signals in the presence of large common-mode voltages. The remaining two devices are the 16-channel MUX-16 and the 2-by-8-channel MUX-28.

For 100 or more, the 8-channel multiplexers sell for $6.50 each, while the 16-channel devices are priced at $12.50. Those prices are about half of what competing protected C-MOS products go for, declares Donn Soderquist, PMI marketing manager. Their size is also about half of that of C-MOS units—82 by 59 mils for the 8-channel units and 75 by 109 mils for the others.

Another important area in which the new device outperforms its competition is speed, although as senior marketing applications engineer Will Ritmanich points out, you have to be careful how you define that term. C-MOS circuits, he explains, have faster access times—that is, they reach, say, 50% of final value more quickly than do the bi-FET units. But the C-MOS multiplexers ring a lot, so their overall settling time to within, say, 0.01% is longer. The new PMI units will typically settle to within 0.025% of final value within 2.9 μs for a 10-V step input, compared with about 3.5 to 4.0 μs for C-MOS devices. Thus the bi-FET switches are faster when used in 12-bit data-acquisition systems, the industrial norm. For 10-bit applications, Ritmanich concedes, C-MOS probably has the speed edge.

Despite all these advantages, bi-FET multiplexers do not have C-MOS completely beaten. High-quality C-MOS devices that include current-limiting resistors are protected against input overvoltages up to ±20 V beyond the supply voltage. PMI's bi-FET products are protected, by a diode, only up to +11/−20 V. Actually, Ritmanich points out, if the input goes more than 11 V more positive than the positive supply voltage, the device will not be destroyed, but it will start drawing current and will not work properly. Latching, however, is not a problem, he emphasizes: when the voltage drops back into the normal operating range, the multiplexer will again function normally.

One final advantage of C-MOS devices is their lower power consumption. For battery-powered applications, they are undeniably attractive, the PMI engineer concedes.

The 8-channel PMI multiplexers are housed in standard 16-pin, dual in-line packages, while the 16-channel units come in 28-pin DIPS.

is packaged in three full-ATR (air-transport-rack) chassis, containing the central processor unit, memory and input/output modules, and power supplies. As with all previous Norden PDP-11M computers, the militarized version has software identical to the commercial version. Although the hardware is, of course, not identical, it is compatible with the commercial machine.

The PDP-11/70M will be ready for delivery in October. Prices are dependent upon the configuration desired.

Norden Division of United Technologies Corp., Norwalk, Conn. 06856. Phone (203) 838-4471 Ext. 214 [363]

Printers use microprocessors for easy interfacing

Three nonimpact alphanumeric printers—the 6310, 6320, and 6330—use internal microprocessors to simplify systems interfacing and to reduce component counts by factors as high as 10 for enhanced reliability. All three printers use electrosensitive paper, and all three offer double-font printing and variable data formatting.

The 6310, which operates at data rates from 110 to 600 bauds, is

designed for either RS-232-C or 20-mA current-loop inputs. It sells for $595.

The 6320 handles both RS-232-C and 20-mA inputs at rates up to 1,200 bauds. In addition, it has a built-in 24-hour clock and day-month calendar. The 6320 is priced at $795.

Priced at $695, the 6330 has an

New products

8-bit parallel bus input and a maximum data rate of 1,000 characters per second. Like the 6320, it has a clock and calendar that operate even when the printer is turned off.

All three printers are offered in board-only versions (minus the power supply and case) at substantial savings to original-equipment manufacturers. Present delivery time is 11 weeks.

United Systems Corp., 918 Woodley Rd., Dayton, Ohio 45403. Phone (513) 254-6259 [366]

Stand-alone computer system with disks sells for $4,595

The RD-11C computer is a complete stand-alone system, which includes an LSI-11 central processor and 205 kilobytes of mass storage in a dual microfloppy-disk subsystem. The entire system, with up to 65 kilobytes of random-access memory, four serial interfaces, the two microfloppies, two quad expansion slots, and a power supply, is housed in a bench-

top enclosure with a volume of only 1.03 cubic feet.

The unit is compatible with DEC's RT-11 operating system and supports a macro-instruction assembler, Fortran IV, Multi-User Basic, APL, Focal, Forth, Pascal, SAL 11, and MINBOL programming languages. A minimum configuration, with 8 kilobytes of RAM and a serial console interface, sells for $4,595. A more useful system, with 40 kilobytes of

Circle 146 on reader service card

Circle 223 on reader service card

RAM, two serial interfaces, and RT-11 with an ASR communications emulator is priced at $7,975. Both units include the dual microfloppies, and both have the same delivery time of 30 days.

RDA Inc., 5012 Herzel Pl., Beltsville, Md. 20705. Phone (301) 937-2215 [365]

Instrument interfacing added to HP-97

Based on the popular HP-97 programmable printing calculator, the HP-97S is a computing data-acquisition device that uses binary-coded-decimal interfacing to gather and process data from a wide range of instruments. The unit has 10 BCD input lines for connection to the outputs of a variety of instruments. In addition, four output lines aid in instrument control. These output lines, which can be set and cleared under software control, can open and close relays, provide pulses for a stepper motor, or perhaps change ranges on a measuring instrument. The HP-97S input/output calculator sells for $1,375 and has a delivery time of 12 weeks.

Inquiries Manager, Hewlett-Packard Co., 1507 Page Mill Rd., Palo Alto, Calif. 94304 [364]

Tabletop computer has graphics capability

The 8510/a graphics computer system comprises a Digital Equipment Corp. LSI-11 microcomputer, a floppy-disk drive, a controller capable of handling four drives, 56 kilobytes of read-write random-access memory, an asychronous serial interface, video electronics, a 12-inch cathode-ray-tube display, and a keyboard. The raster-scan display shows text as 24 lines of 80 characters and graphics in bit-map fashion using a 320-by-240-dot matrix. The hardware system sells for $7,850; software is extra.

Terak Corp., 14425 North Scottsdale Rd., Suite 100, Scottsdale, Ariz. 85260 [367]

Packaging & production

Plastic barrier protects wires

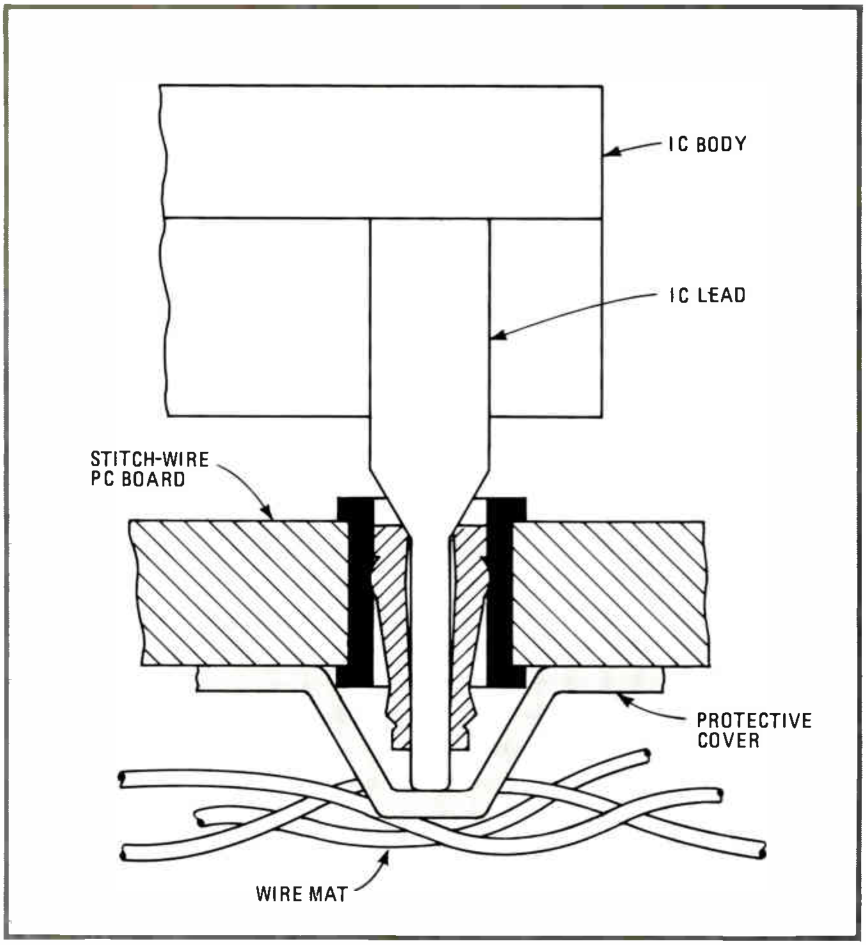
Thermoplastic cover prevents IC leads from puncturing stitch-wire insulation

Many space and military electronics packages are being built with a highly reliable, semi-automatic, point-to-point wiring system called stitch wiring. In this method Teflon-insulated nickel wire is cold-welded to either a matrix of steel pins or stainless-steel plated copper lands on one side of an epoxy-glass circuit board. Components are normally wave-soldered to the other side of the board—and must be desoldered if replacement is necessary.

The parts involved are generally integrated circuits in dual in-line packages. So engineers at the Multi Link division of Odetics Inc. observed that low-profile solderless socket pins were available from Augat Inc. and got the bright idea of applying them in DIP-socket patterns to planar stitch-wire boards—those constructed with stainless-steel lands.

Theoretically, the approach allows 14- and 16-pin DIPS to be easily removed from the board without being desoldered. But in practice, the Holtite contacts and the IC leads inserted through them protrude beyond the board into the matrix of Teflon-coated wire, threatening to displace its insulation and to cause shorts between themselves and the wire.

So Multi-Link came up with a solution for that, too—a patented device that acts as a physical barrier between the exposed IC lead/contact



New products

and the wire mat. It resembles the bottom half of an egg carton and is made from the thermoplastic material of nylon for commercial and industrial applications or from thermosetting diallyl phthalate for the higher-temperature requirements of the aerospace and military area.

The drawing shows one such device. It is available as a universal strip of modules on 0.100-inch centers, which can be used on stitch-wire boards employing DIPs arranged in virtually any pattern, or as individual IC patterns for DIPs on 0.100-, 0.300-, 0.400- and 0.600-inch lead centers. The device comes with the end of each protection module open, for optimum (low) wire build-up, or with a solid end cap, to allow the wiring to be conformally coated without risk of contaminating the Holtite contact.

The protective devices have double-backed adhesive tape permanently attached to them. To apply one to a board, an acetate film or plastic-coated paper is peeled off the adhesive layer and the device is pressed down over the Holtite ends. Clearance holes beneath the devices prevent the adhesive from contaminating the Holtite contacts.

An alternative method of attachment is to mold a fastener right into the protective device. This split prong is pressed through an arrangement of mounting holes in the stitch-wire board.

Besides protecting the insulation of the stitch wire, the protective device also forms channels or conduits in which the stitch wire can be routed. This could be a necessary step in the use of fully automatic stitch-wire machinery, which has not yet been developed.

Multi Link Division of Odetics Inc., 2121 South Manchester Ave., Anaheim, Calif. 92802. Phone (714) 634-2227 [391]

Digital system performs 200,000 tests per second

The ATS-961 automated test system provides digital testing complete with guided-probe fault isolation to

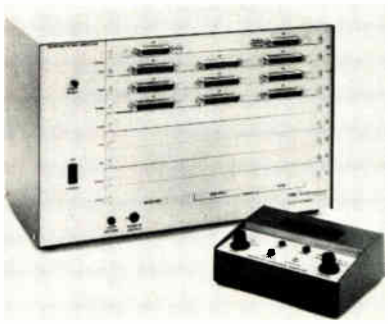
the failed device. As an option, it can also supply digital logic simulation. The system, which can operate at a rate of 200,000 tests per second, has a capacity for 256 stimulus-response leads. Other features include external synchronization of an applied digital test pattern, array software for data analysis, and programming in the Atlas test language.

The system can accommodate two test stations, permitting the simultaneous testing of different board types. In addition, programs can be prepared off line by using magnetic-tape cassettes. The price of the ATS-961 test system is less than $50,000; deliveries are scheduled for the second quarter of this year.

Texas Instruments Inc., P. O. Box 1444, Houston, Texas 77001. Phone (713) 494-5115 [393]

System speeds wire-harness assembly and testing

Designed to provide in-process test and assembly instruction for wire-harness makers, the RWD-1000 random work director system consists of a remote control display, a mainframe enclosure for circuit interfacing, and 50-wire plug-in modules. The three-part system identifies each conductor numerically, defines ter-



The new CS-1352 oscilloscope is a portable 75 mm dual-trace model boasting outstanding features usually found only in large size models:

Formost is ability to observe even small signals thanks to wide DC to 15 MHz bandwidth and exceptionally high sensitivity up to 2mV/div.

Other quality features include auto-free-run, highly sensitive X-Y system, triggered sweep, etc., with reliability and stability increased through incorporation of dual FET's, integrated circuitry, Logic Control system and other sophisticated arrangements.

But the most practical feature of the new CS-1352 model is its facilitated ease of measurement in a variety of applications. Three-way power source includes built-in rechargeable lead-acid battery (optional) which makes this a truly portable and versatile instrument.

As an indispensable test instrument for production-line checks and post-sales servicing of color TV sets, stereo receivers, and maintenance of computer systems, the oscilloscope is daily widening its scope of application. A new "must" for inclusion in a serviceman's kit.

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NEW CS-1352

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mination points with indicator lamps, and performs continuity testing after final assembly. It is designed to increase productivity by reducing the need for rework.

The RWD-1000 is interfaced to the assembly to be built through a programmed back-wired harness board. When interfacing is complete, the unit is activated for instructing, verifying, and testing. The base price of the system is $1,850.

T&B/Cablescan Inc., 145 E. Emerson Ave., Orange, Calif. 92665. Phone (714) 998-1961 [394]

Forced-air heat sinks range up to 30 in. long

The model 2450 forced-air, finned heat sink is actually a family of customized heat sinks in which fins are staked to a base plate that can range in size up to about 30 inches long by 11 in. wide. Fin height and density can be varied to meet specific application needs, and the base plate, as well as the fins, can be notched, drilled, milled, or profiled to fit various packages. The unit is available in both aluminum and copper in a variety of finishes.

Astrodyne Inc., 353 Middlesex Ave., Wilmington, Mass. 01887. Phone Zane B. Laycock at (617) 272-3850 [395]

Meter measures minority-carrier diffusion length

An instrument for the measurement of minority-carrier diffusion lengths (or, equivalently, minority-carrier lifetimes) in silicon solar cells and other shallow-junction devices has a range of 5 to 400 μm (equivalent to carrier lifetimes of 10 ns to 100 μs). The unit, which uses the surface photovoltage method, is capable of accommodating specimens up to 10 cm in diameter. It also allows the specimen to be moved to obtain diffusion-length profiles.

Solar Semiconductor Instruments, 13500 Midway Rd. at Alpha, Suite 230, Dallas, Texas 75240 [396]

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New products

modules and zeners into dc units. Further, quick-disconnect tabs are provided as options to screws, "in response to large users who complained about mounting-time requirements," he adds.

The new size is important, says Bishop, particularly for designers who want to get more than one row of modules in a standard 19-inch rack. Width of the new 673 series package is 1.75 in. (down from 2.50 in.), and the height has been cut from 2.06 to 1.50 in.

In thermal characteristics, the temperature rating of the 3-A output operating level has been extended to 55°C for ac units and 40°C for dc units from the previous 25°C. This improvement largely results from shifting the indicator light-emitting diode from the power to the logic side of the modules. (The LED indicates status for monitoring and troubleshooting.) Potting also improves thermal characteristics.

In operation, output modules are functionally equivalent to conventional four-terminal solid-state relays, with ac and dc load current ratings of 3 A maximum—sufficient for most standard solenoids, motor starters, and other components. Input modules provide the reverse switching function of output modules, converting high-voltage ac and dc control signals from sensing switches or devices to clean logic signals for computer input.

In all, the 673 series consists of 11 modules. Two ac-input units offer a choice of input ranges—either 95 to 132 V ac or 187 to 250 V ac—and deliver an output of 12 V dc. Inputs may range from 4 to 10 V dc or 10 to 32 V dc for the four ac-output units, which switch an output of 132 or 250 V ac. All three dc-input modules develop a 12-V dc output, while inputs may be 0 to 55, 95 to 132, or 187 to 250 V dc. Finally, there are two dc-input units, each of which has a 55-V dc output. Inputs for the latter may range from 4 to 10 V dc or from 10 to 32 V dc.

Besides solid-state optical isolation, the new modules offer a number of other features, including: ac outputs with synchronous zero-

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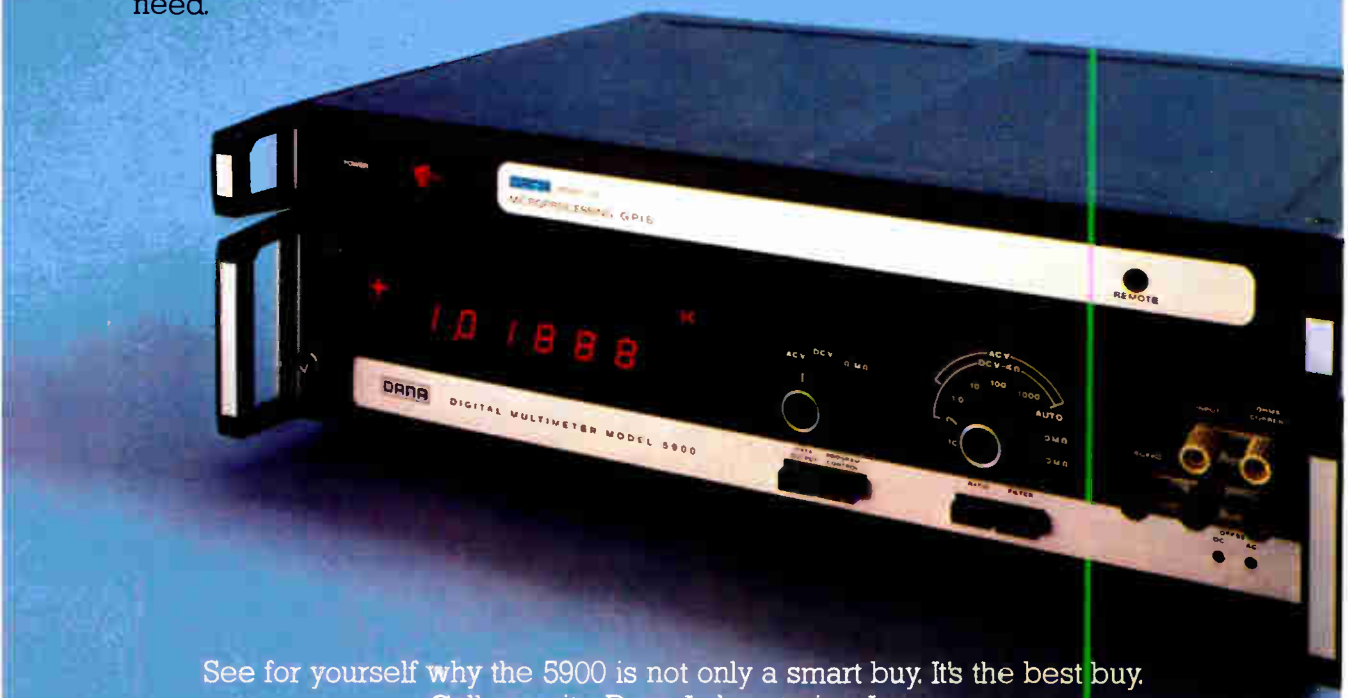

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Others measure by us.

Circle 216 for Product Demonstration   Circle 159 for Literature Only voltage switching and built-in snubber network, logic terminals isolated from ac line terminals, and high noise immunity for withstanding severe industrial environments without misfiring. Also, barriered power terminals for wiring hookups eliminate the need for external power-line terminal strips. When panel-mounted in rows, the terminals become in effect an integral terminal strip for wiring, providing maximum physical isolation of power lines from logic circuits, according to Bishop. Custom 19-in. mounting panels designed for both the 673 and earlier series modules, with prewired logic interconnections, are available; they accept up to 16 modules. Both series are designed to be electrically interchangeable.

A representative price for ac-input versions, covering about 50% of the new modules, is $7.90 each in quantities of 5,000 or more, compared with $9.45 for the previous line. Ac-output units drop to $11.25 each from $12.40 and dc-output modules to $9.85 apiece from $12.66. Dc-input units are also $7.90, down from $9.15. Delivery is from stock.

Teledyne Relays, 3155 West El Segundo Blvd., Hawthorne, Calif. 90250. Phone (213) 973-4545 [381]

Digital combiner simulates two-speed s-d converter

The performance of a two-speed synchro-to-digital converter can be simulated by a pair of single-speed s-d converters and the model TSL1036 digital combiner. The module takes the outputs of a 7-bit coarse converter and a 14-bit fine converter and combines them.

The TSL1036 accepts signals from any binary-output converter, including tracking and sampling types as well as multiplexed systems. It accommodates speed ratios of 36:1, 36:2, 18:1, or 9:1. In small quantities, the combiner sells for $249. Delivery is from stock.

Natel Engineering Co., 8954 Mason Ave., Canoga Park, Calif. 91306. Phone (213) 882-9620 [384]

Microwaves

Transmitter has little jitter

Modulator-magnetron assembly for MTI radars weighs only 37.5 pounds

Most existing radar systems use hydrogen thyratrons to modulate pulsed magnetrons. Now, however, a solid-state microwave transmitter in a package designed for use aboard aircraft is available for new designs and retrofitting. Smaller, lighter, and longer-lived than its gas-tube predecessors, the new unit's main claim to fame is its ability to maintain nearly constant pulse-to-pulse amplitude and very little frequency jitter—essential in ground and airborne moving-target-indicator (MTI) radar systems.

The V/RO 200651 microwave transmitter, which includes a modulator unit and an SFD-349 pulsed coaxial magnetron, measures 6 by 9.5 by 11 inches and weighs approximately 37.5 pounds. A highly reliable silicon-controlled-rectifier-driven magnetic modulator containing a dequeuing-type energy regulator assures that the energy contained in each pulse is the same as the energy contained in every other pulse. This is extremely important in MTI radars, where any change in the current drive to the magnetron is translated into a frequency shift in the rf output.

In addition, the modulator is protected against open and short circuits and has available a coincident trigger should the system require one. The transmitter also provides a 1-μs pretrigger.

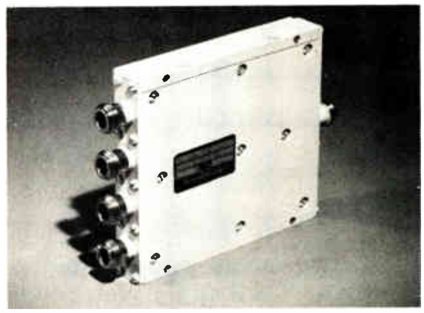
When operated with the Varian SFD-349 coaxial magnetron, the transmitter produces a minimum pulsed output power of 200 kW over the tube's tunable range of 8.5 to 9.6 GHz. The unit, however, can also be fitted with various C- and X-band Varian magnetrons.

With the SFD-349, the transmitter is priced in the range of $13,000 to $15,000. It has a delivery time of 120 days.

Varian, Beverly Division, Ritter Operation, Salem Road, Beverly, Mass. 01915. Phone (617) 922-6000 [401]

Resistor-isolated divider handles 100 W cw

A four-way power divider, the model D363AS, can handle a continuous-wave input power of 100 W while maintaining an insertion loss of only



0.3 dB. The unit operates from 400 to 500 MHz, has a maximum VSWR of 1.15, is amplitude-balanced to within 0.2 dB, and has a minimum isolation of 25 dB. Phase balance is within 1.5°. Other, similar, high-power resistor-isolated dividers are available in two- and eight-way configurations, with the same basic specifications. The D363AS sells for $275, and it has a delivery time of 30 days.

Engelmann Microwave Co., Skyline Drive, Montville, N. J. 07045. Phone Carl Schraufnagl at (201) 334-5700 [403]

Tubular low- and band-pass filters handle up to 100 W

Multisection filters in the FS-21 series of tubular low-pass and band-pass devices are low-ripple Chebyshev units with available power ratings of 2, 20, and 100 W. The low-pass models have cut-off frequencies from 200 MHz to 12.4 GHz and are offered with from 5 to 13 sections. The bandpass filters have from three

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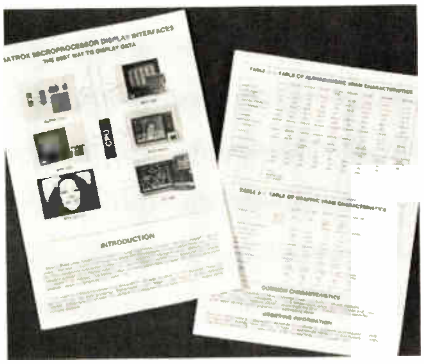
Circle 169 on reader service card

Microprocessor-display interfaces. A five-page brochure provides information on microprocessor-display interfaces that are basically random-access memories with alphanumeric or graphic outputs to television or cathode-ray tubes or light-emitting-diode displays. Graphic CRT controllers have resolutions from 256 by 256 to 512 by 512, while the other devices control 16 or 32 alphanumeric 5-by-7-dot-matrix LED displays. Data tables summarize the physical and electrical characteristics of each member of each family. Matrox Electronic Systems, P. O. Box 56, Ahuntsic Station, Montreal, Quebec, Canada. Circle reader service number 426.



Silicone products. A 40-page catalog, "A Guide to Dow Corning Products," covers over 100 silicone, organosilicon, and silicon products and their uses in over 25 industry classifications. Included are products for appliance fabrication, chemical specialty applications, chemical and petroleum processing, construction, food and drug processing, medical and surgical use, electrical design and utility maintenance, electronic equipment, metal fabrication, moldmaking, mining, paints, paper production and conversion, plastics and rubber, general production and maintenance, science and engineering, textiles and leather, aerospace, and automotive, marine, and railroad applications. A selection guide summarizes the technical properties, benefits, and features of these products. Dow Corning Corp., Box 1767, Midland, Mich. 48640 [435]

Remote data acquisition. A nine-page brochure describes a wide range of capabilities of the Recon 3200 series remote data-acquisition and -control system, including standalone control of simple light displays and peripheral functions in computer-based systems. The system is designed for the mining and communications industries but can be used for water filtration, waste-water treatment, and security monitoring. Sangamo Weston Inc., P. O. Box 3041, Sarasota, Fla. 33578 [427]

Modification and repair. "Modification and Repair for Printed Circuit Boards and Assemblies," IPC-R-700B, reports on commonly used modification and repair techniques

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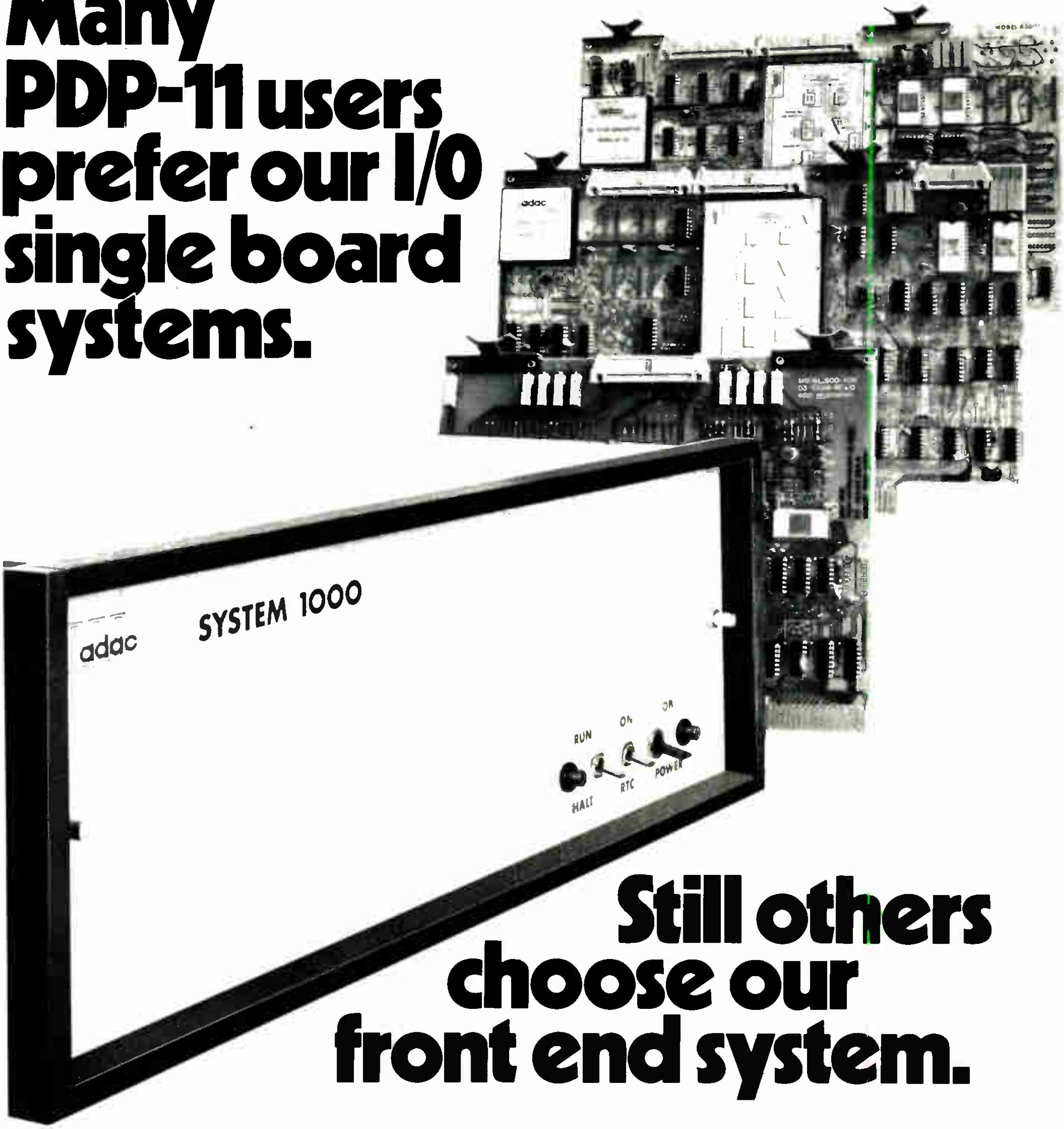

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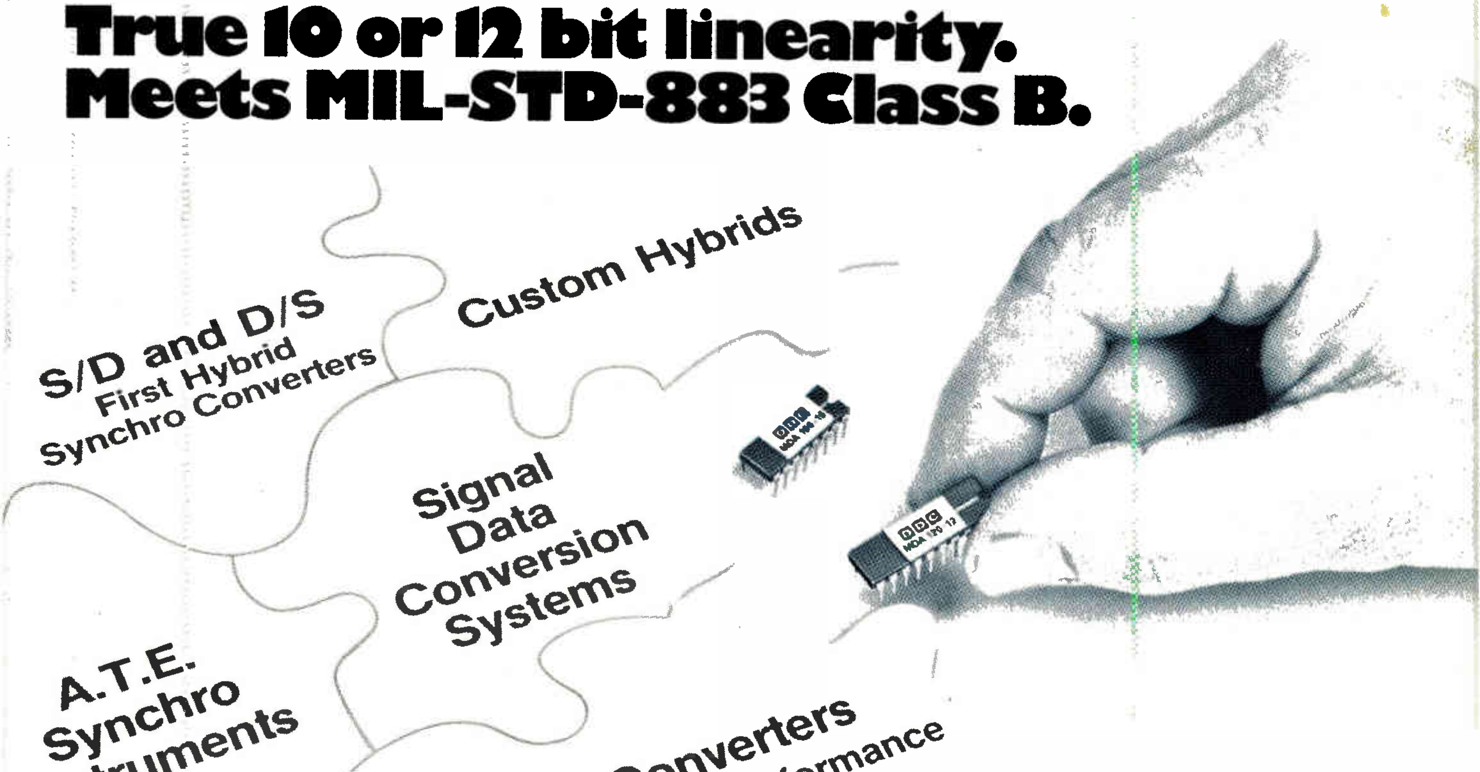

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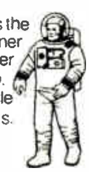

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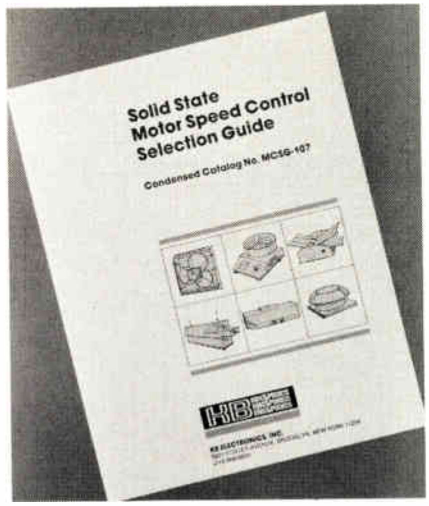

consumer appliances to business equipment. The motor control series includes ac, ac-dc, and dc types. The guide details each model in each series, giving a full description, dimensions, ratings, type of mounting, standard and optional features, and typical applications. KB Electronics Inc., 5803 Foster Ave., Brooklyn, N. Y. 11234 [433]

Display screens. A two-page brochure describes low-reflectance display screens and filters for use with light-emitting diodes in digital panel meters, planar displays, liquid-crystal displays, and gas-discharge and cathode-ray tubes. The brochure explains how to improve display readability as well as resolution in order to reduce gross distortion and edge and surface defocusing. CRT filter and LED/gas-discharge charts are included along with a selection guide. SGL Homalite, a Division of SGL Industries Inc., 11 Brookside Dr., Wilmington, Del. 19804 [436]

Tubing. Beading, tubing, and wire insulation made from a variety of fluoroplastic resins are described in a 24-page catalog. These products can be used in the aerospace, electronics, medical, automotive, nuclear, chemical, industrial, and electrical fields. They feature good heat resistance and chemical stability. A table of properties of fluoroplastic resins is provided. Zeus Industrial Products Inc., Foot of Thompson Street, Raritan, N. J. 08869 [437]

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