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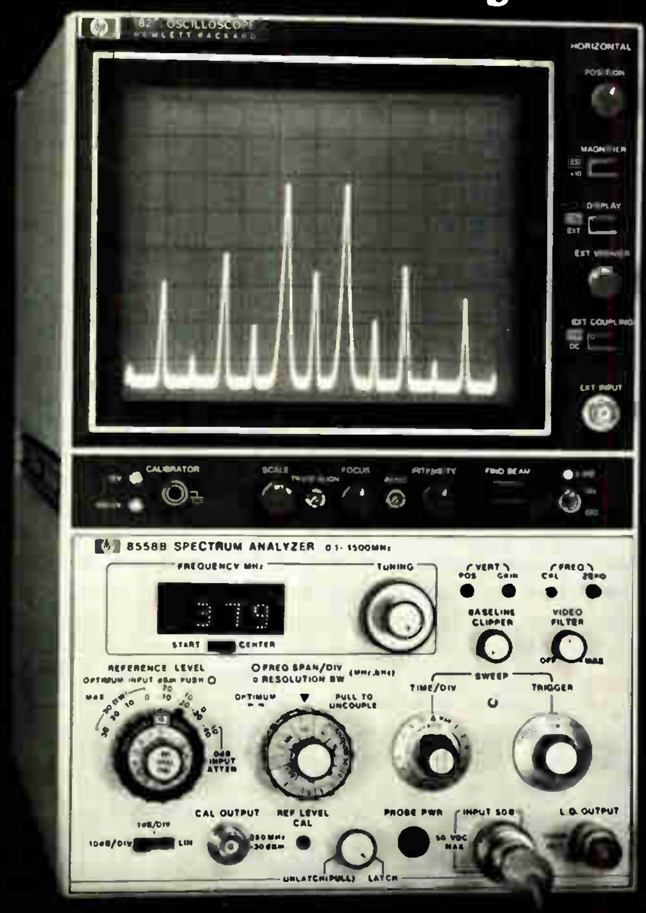

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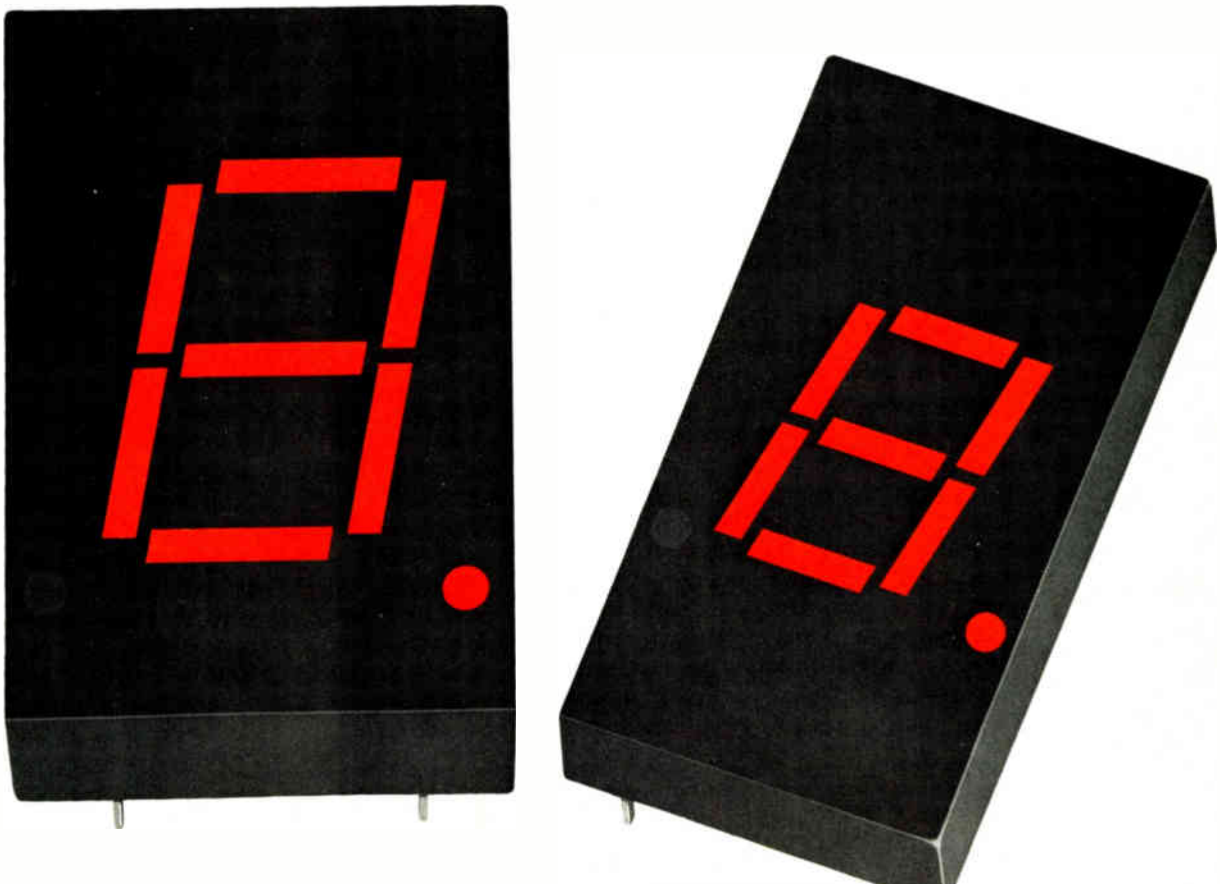

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Electronics
The International Magazine of Electronics Technology
Vol. 47, No. 9 • May 2, 1974

Highlights

Cover: Microprogramable mini exploits 4k RAM, 87
A family of general-purpose minicomputers is the first production series to profit from the low power and high density of the new 4,096-bit random-access-memory chips. Greater microprogramability gives the user more freedom to adapt his machine to changing applications.

Success of 6th satellite in ATS series likely, 69
Due for launch on May 30, the sixth and last of the applied technology satellites promises to advance long-distance communications techniques and could help improve usage of the communications spectrum.

Computer networks give users more scope, 98
By pooling such data-processing resources as data bases and sophisticated programs, computer networks handle large and complex tasks very fast. But research into their potential continues even as commercial nets grow in number and popularity.

NCC aims at computer builders and users, 126
A recordbreaking 119 technical sessions at the National Computer Conference cover every aspect of data processing, from technological advances to its rapidly diversifying applications.

And in the next issue . . .
The film-carrier approach to high-volume IC assembly . . . measurement and control using programable calculators . . . how readers evaluate EE evaluation.

Electronics

Publisher's letter

You'll find a preview of the National Computer Conference starting on page 126. Our two-part coverage of the conference opens with a report on the record number of 119 technical sessions, which cover a broad range of technology and applications. Then, on page 129, we take a look at some of the significant products that are being introduced at the show.

Al Rosenblatt, our New York bureau manager, who prepared the technical-session preview, says that the technical program "reflects the move of information processing into a host of newer businesses, such as data communications, point-of-sale systems, and computer networks."

Indeed, the shift in emphasis toward attracting the non-computer professional, which was first made by NCC management a year ago, illustrates, once again, how pervasive electronics technology has become. More and more, the computer user is someone who did not start out as an expert in computer usage. Instead, his data requirements are pushing him into harnessing the power of electronic technology.

Also illustrating that trend are six special sessions. They will cover such broad social topics as computers and personal privacy and energy in an evolving society.

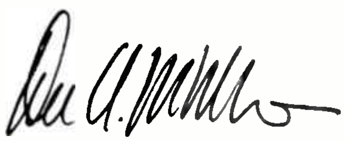
Risk is certainly one of the most challenging elements of the electronics business. And our cover story this issue is, partly, the story about a risk successfully taken. To ready their new minicomputers for market, designers at Hewlett-Packard had to take the risk that 4,096-bit random-access memories would be ready, too.

As the article that starts on page 87 points out, the first breadboards were based on core, even though the design was committed to semiconductor memory long before the costs came down to ferrite-core levels. Then came the jump to 1,024-bit devices—and the decision that 4k RAMs of high reliability would reach competitive cost levels in time.

The story of how the design progressed—even to the point of adding the ability to accept 4k RAMs of a variety of characteristics from several sources—is fascinating. What's more, it shows that the calculated risk—which pushes technology forward in the process—is one of the elemental forces that keeps electronics so strong.

Resource sharing is just about the most significant trend in computer technology today. Tie together a number of computers into a network, and you have a system that has a computational power far greater than the mere summing of the parts might indicate.

As Wally Riley, our Computers Editor, brings out in his special report (see p. 98), networks not only offer shared computuational resources—including data bases, special equipment, and sophisticated programs—they offer advantages peculiarly their own. "They show the way to low-cost, high-performance computing systems," he says, "since for some jobs a network of smaller systems can duplicate the capability of one large expensive system at lower total cost."



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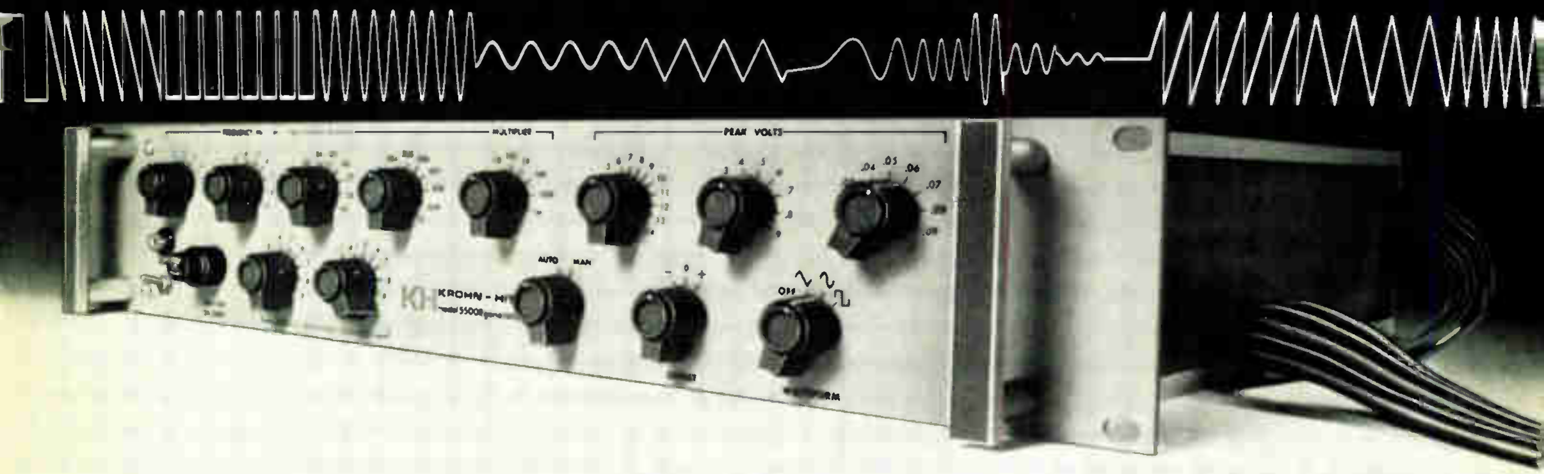

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Circle 5 on reader service card

Readers comment

Crediting IBM 1k RAM roles

To the Editor: My article, "Pinch-load resistors shrink bipolar memory cells," [*Electronics*, March 7, p.130] has resulted in some confusion on the relative role of the Boeblingen, Germany, and Burlington, Vt., IBM locations in developing the 1,024-bit random-access memory used in the 370 models 135 and 145.

My work consisted of the invention and early experimental investigations of cells employing pinch-load resistors [U. S. Patent No. 3,693,057]. The application of these and other inventions in the development of the 1,024-bit chip and its subsequent reduction to practice was accomplished in the Burlington facility, where that 1,024-bit chip is currently in production. The product is also being produced in Corbeilles-Essonnes, France.

S. K. Wiedmann
IBM Deutschland GmbH
Boeblingen, Germany

■ *The article appearing on p. 110 of this issue describes the design of the memory module, as worked out in Burlington.*

Tone encoder won't interface

To the Editor: The [Frequency Devices Inc.] tone encoder described in the New products section [*Electronics,* March 21, p. 167] won't interface with the Bell System tone receivers using the upper oscillator set of frequencies listed.

The frequencies should be *1,209,* 1,336, *1,477,* and 1,633 hertz to be compatible with Bell System frequencies. The error in the first frequency looks like a transposition by your typesetters. The 1,477 Hz has a longer error background.

It appears that a typesetting error in Table 14 on page 30–22 of the fifth edition of the [ITT] "Reference Data for Radio Engineers" caused the 1,447 Hz to get propagated in various subsequent articles. Table 6 on page 2-14 of "Reference Data" has the correct frequency set. I hope this letter will alert the engineering-design community that 1,477 Hz is the correct upper frequency for push buttons 3, 6, 9, and #.

E. G. Baldwin
Winston-Salem, N. C.

40 years ago

From the pages of Electronics, May 1934

Microphones in the cemetery

Many persons are pursued by an unreasoning fear that they may some time undergo a temporary coma simulating death, and be actually buried alive, only to "wake up" and find themselves interred in a coffin five feet underground.

One victim of this fear of being buried alive, has made advance arrangements with his undertaker and cemetery, by means of which a sensitive microphone will be installed inside the coffin and connected with loudspeakers in the cemetery caretaker's dwelling nearby. This microphone circuit is to be kept continuously energized for at least a year after interment, during which year it is to be regularly tested by sounding a small gong in the coffin.

Guarding a $1 million painting

When the famous painting, Whistler's "Mother," was on view at Dayton, Ohio, the million-dollar canvas was guarded by a series of electronic protection devices, installed under the direction of Gisbert D. Bossard, president of the General Kontrolar Company, of Dayton.

A system of infrared "black light" beams, with all generating and light-sensitive equipment installed in the walls, made it impossible for anyone to approach or disturb the canvas without sounding several alarms, including a police siren that could be heard for several blocks.

Sam Browne belt radio

A miniature radio receiving set has been invented by Ralph O. Gordon of Los Angeles, to be worn by patrolmen. The set is worn on a Sam Browne belt with an earphone attached to the cap, the whole weighing less than three pounds.

Associate Press facsimile

Newspapers of the Associated Press have approved the plan to transmit pictures by wire facsimile, using the A.T.&T. process. Pictures up to 11 by 17, half a newspaper page, will be sent at average rates of 11 square inches per minute.

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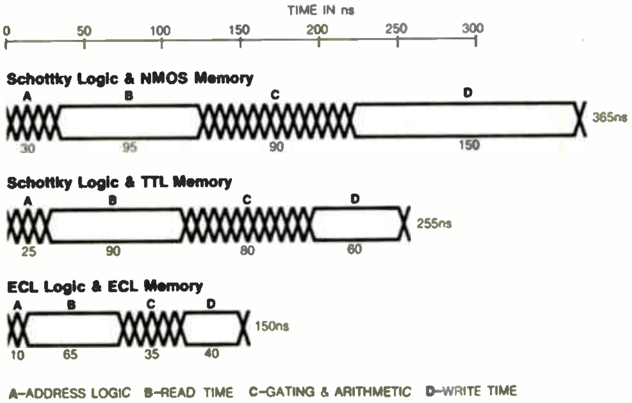

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For new ECL designs, some new competitive advantages.

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10010	Decade Counter	12.10
10016	Binary Counter	12.10
10101	Quad OR/NOR	1.67
10102	Quad NOR	1.67
10103	Quad OR	1.67
10105	Triple OR/NOR	1.67
10106	Triple NOR	1.67
10107	Triple Exc. OR/NOR	2.09
10109	Dual OR/NOR	1.67
10110	Dual 3/3 OR	2.09
10111	Dual 3/3 NOR	2.09
10114	Triple Line Receiver	2.09
10115	Quad Line Receiver	1.67
10116	Triple Line Receiver	1.67
10117	Dual 2 W AOI	2.09
10118	Dual 2 W OA	2.09
10119	4 W OR/AND	2.09
10121	4 W AOI	2.09
10124	TTL To ECL	4.50
10125	ECL To TTL	4.50
10130	Dual D Latch	4.46
10131	Dual D Flip-Flop	5.65
10132	Dual MUX-Latch	5.02
10133	Quad Latch	6.19
10134	Dual MUX-Latch	5.02
10160	12-Bit Parity	6.84
10161	1-8 Demux/Decode (L)	5.42
10162	1-8 Demux/Decode (H)	5.42
10164	8-1 MUX	5.42
10170	9 + 2 Bit Parity	6.84
10171	Dual 1-4 Demux (L)	5.42
10173	Quad MUX-Latch	6.19
10174	Dual 4-1 MUX	5.42
10175	Quint Latch	7.33
10179	Look Ahead	6.84
10180	Adder/Subtractor	18.00

F10K ECL Logic Available Soon

Device	Description
2nd Quarter 1974	
10014	Active Terminator
10104	Quad AND Gate
10141	4-Bit Shift Register
10153	Neg Clock 10133
10172	Dual 1-4 Demux/Decode (H)
3rd Quarter 1974	
10135	Dual JK Flip-Flop
10136	Binary Counter
10137	Decade Counter
10176	Hex D Flip-Flop
10210	High-Speed 10110
4th Quarter 1974	
10145	16 x 4-Bit RAM
10165	Priority Encoder
10166	5-Bit Comparator
10181	4-Bit ALU
10186	Hex D Flip-Flop/Reset

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Device	Description	Price 100-999
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Our F10K is virtually immune to voltage variation, ripple and gradients. And holds noise immunity constant.

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Circle 13 on reader service card

People

NDC's Thorpe spreads his wings

When does a former Air Force colonel volunteer to give up some of his command? In the case of National Data Corp.'s president George W. Thorpe, the time was this year when the company reached a value of $30 million and set out to double its size.

The Atlanta-based computer/communications systems house, which specializes in electron-funds-transfer programs (see p. 72), has been under Thorpe's command ever since he organized it in 1967, three years after he retired from the Air Force. He had the idea that a lot of what he learned while heading the Strategic Air Command's intelligence-data-processing centers could be applied to credit-card authorization and other money-managing services.

The concept worked. By now, company growth has prompted Thorpe to reorganize, to take some of the day-to-day management load off his shoulders, and to rev up the corporate engines for another growth spurt.

Thorpe's Air Force experience is reflected at NDC in other ways. For example, he picked up an aversion to paperwork while in the military and still does much of his executive memo-writing on the back of envelopes.

Another aversion that survives from his military days is overstaffing. "Having too many people on top is bad—in fact, it's worse than not having enough personnel," he observes. "That's why we have limited the recent changes to four functional responsibilities and just two staff positions."

Between his Air Force retirement and the formation of NDC, Thorpe spent three years with the Southern Railway System where he set up the railroad's data-processing and communication operations.

Thorpe, who has a BS degree in engineering from the U.S. Air Force Institute of Technology, believes that NDC can influence point-of-sale system technology not by building its own hardware but by culling the best from present manufacturers. With a new management organization in place, NDC will be set to prove this contention during 1974 as the company begins to install the first of specially designed authorization terminals recently ordered from Addressograph-Multigraph and National Cash Register Co.

SAC style. George W. Thorpe has applied his Strategic Air Command training to National Data Corp.'s operations.

One thing that won't change is Thorpe's penchant for working himself and his executives on weekends. After all, credit authorization—just like SAC—is a seven-day-a-week operation.

Lucus heads Xynetics after it acquires his firm

The president of a small company acquired by a larger one is not always happy about the arrangement, but Gerald E. Lucus probably won't complain. A year ago, he was president of Electroglas Inc., a maker of production equipment for integrated circuits, when it was acquired from Electronic Memories & Magnetics by Xynetics Inc. But now, because the Electroglas subsidiary performed better than the parent Xynetics, Lucus has been promoted to the presidency of Xynetics itself.

Xynetics, which is moving to Santa Clara, Calif., from Canoga Park, Calif., sells a high-speed, high-accuracy X-Y positioner that uses linear motors.

Electroglas, which has been in Santa Clara, Calif., makes wafer probers and scribers. "Electroglas

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—Dr. Steven R. Hofstein, President,
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No other technology approaches Lithocon II systems in performance, or in answering so wide a range of application requirements. For example, in medical, diagnostic and clinical environments, the doctor can count on consistent, reproduceable X-ray, ultrasonic or nuclear camera images, reproduced by the Lithocon II's wide dynamic range (64 gray levels) and high resolution. These same features make practicable X-ray baggage inspection at airports.

With Lithocon II's unique features, you no longer have to make a trade-off between editing speed, retention time and erase speed. Our new Lithocon II system lets you have over two hours storage time with the ability to store TV images, and still get single-frame erase—full screen in 33 milliseconds. These are the features you need for such applications as remote industrial process monitoring, computer-aided design, medical electronics and cable and closed-circuit television systems.

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People

Lead acquisition. Within a year Gerald E. Lucus moved into the presidency of the firm that had acquired his own company.

and Xynetics made an excellent fit says Lucus. "Electroglas gave Xynetics an outlet in the fast-growing and important semiconductor industry, and the Xynetics positioner gave Electroglas' products a leg up on competition using other types of positioning." Among other features, the positioner can move in two axes at once— an impossibility with other positioners that do comparable tasks.

Xynetics, which has been in business about five years, has doubled its sales every year since shipping started. Recently, however, Xynetics has been overshadowed by Electroglas, whose sales last year were $17 million.

Lucus thinks that much growth can still come in the semiconductor industry, but he expects to penetrate at least two additional market areas per year. "We've just signed an agreement with Boeing for government applications, for example, and there are probably 20 different industries other than semiconductors in which the positioning stage can be applied." He's also looking at a number of acquisitions, but notes "the end-user business is much more difficult over the long term than OEM marketing." To OEMs, multiple orders can be sold with little more effort then it takes to sell one user, so he's looking hardest in this direction.

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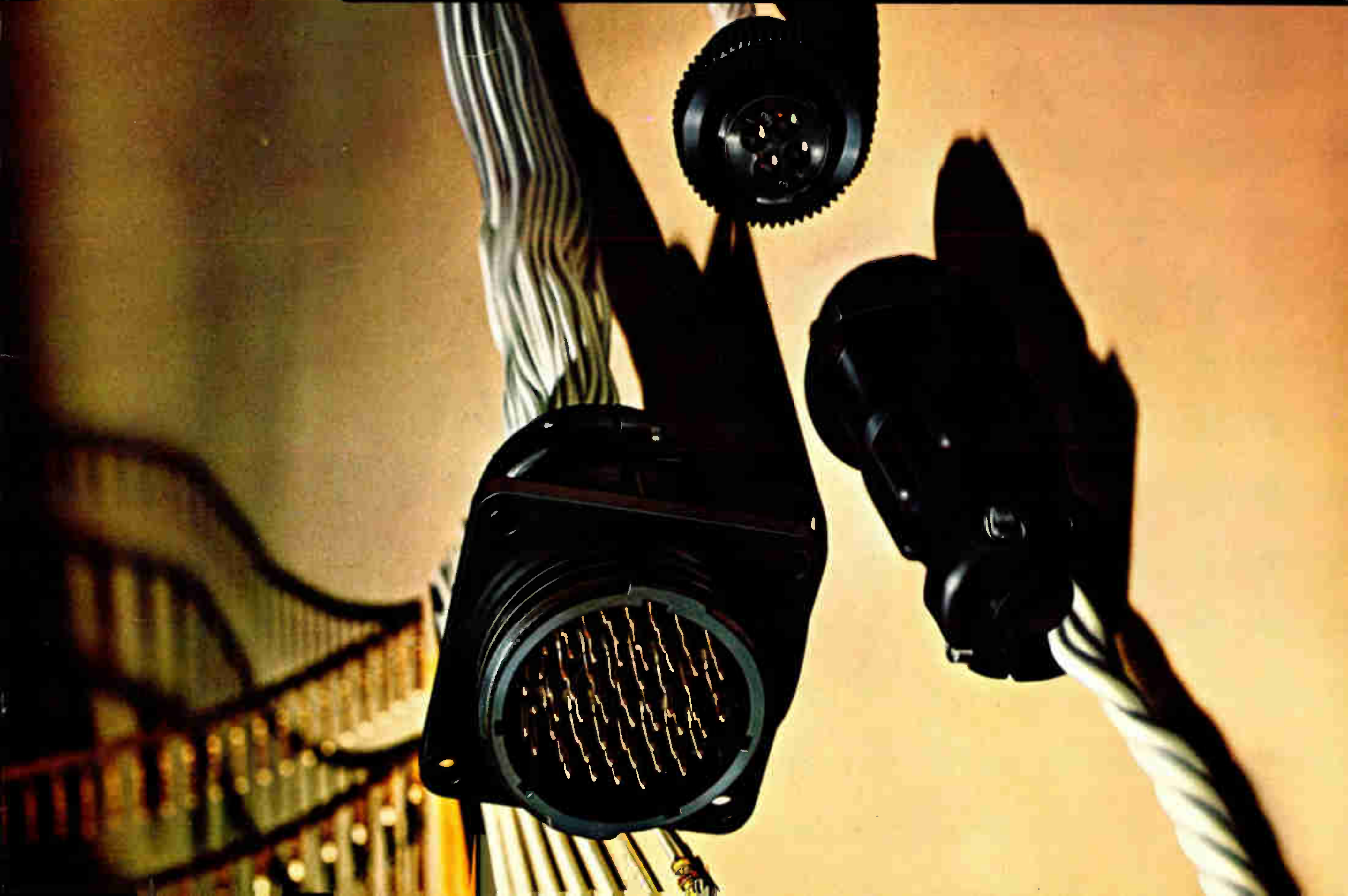


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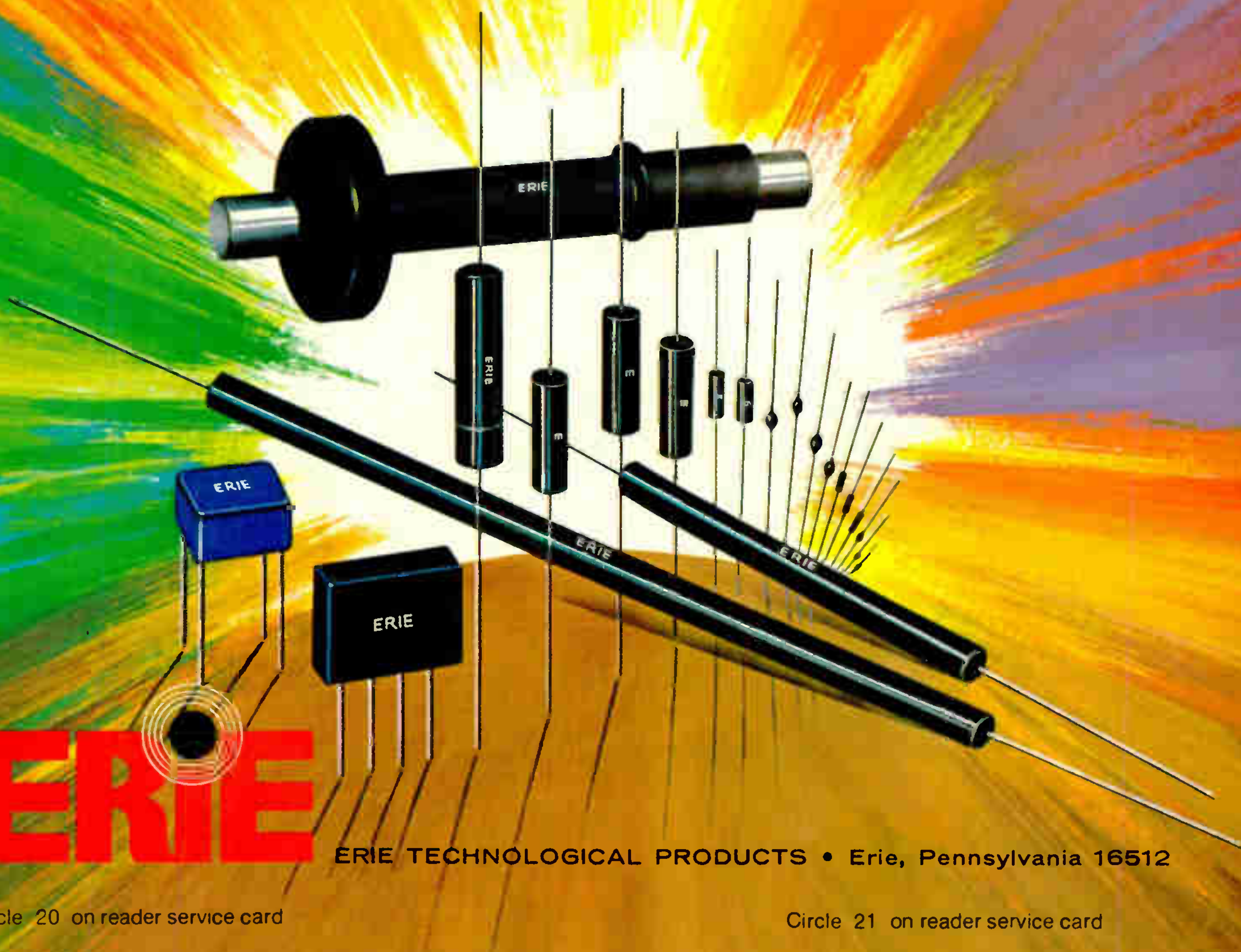

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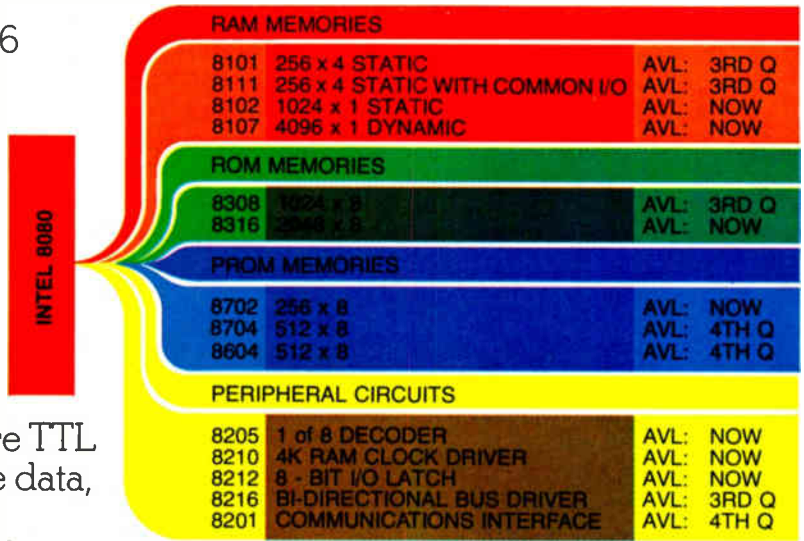

INTEL 8080 PRODUCT FAMILY

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The 8080 microcomputer has 78 basic instructions, including the 8008 set plus new ones that make possible such features as vectored multi-level interrupt, unlimited subroutine nesting and very fast decimal and binary arithmetic.

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International Instruments, Electronics, and Automation Exhibition, Olympia, London, England, May 13–17.

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Society for Information Display International Symposium, Town and Country Hotel, San Diego, Calif., May 21–23.

International Instrumentation Symposium, Instrument Society of America, Hilton Inn, Albuquerque, N. M., May 21–23.

Semicon/West '74, SEMI, San Mateo Fairgrounds, San Mateo, Calif., May 21–23.

International Symposium and Technical Exhibition on Electromagnetic Compatibility, Swiss Federal Telecommunications Authority, Montreux, Switzerland, May 23–29.

Microwave Power Symposium, International Microwave Power Institute, Marquette University, Milwaukee, Wis., May 28–31.

Consumer Electronics Show, EIA, McCormick Place, Chicago, Ill., June 9–12.

Power Electronics Specialists Conference, IEEE, Bell Laboratories, Murray Hill, N. J., June 10–12.

Quantum Electronics International Conference, IEEE, Hyatt Regency, San Francisco, June 10–13.

Utilities Telecommunications Council Annual Meeting, UTC, Chalfonte-Haddon Hall Hotel, Atlantic City, N. J., June 16–20.

International Microwave Symposium, IEEE, Atlanta, Ga., June 12–14.

1974 Government Microcircuit Applications Conference, Dept. of Defense, NASA, AEC, University of Colorado, Boulder, Colo., (confidential clearance required), June 25-27.

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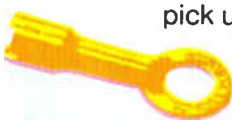

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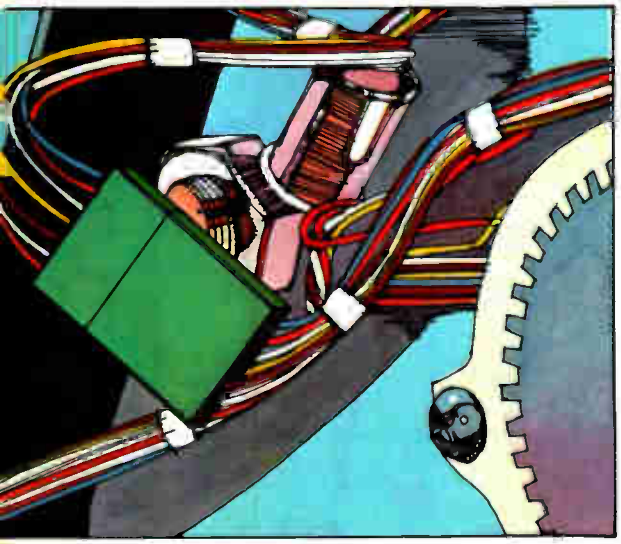
Circle 25 on reader service card

Growing with the

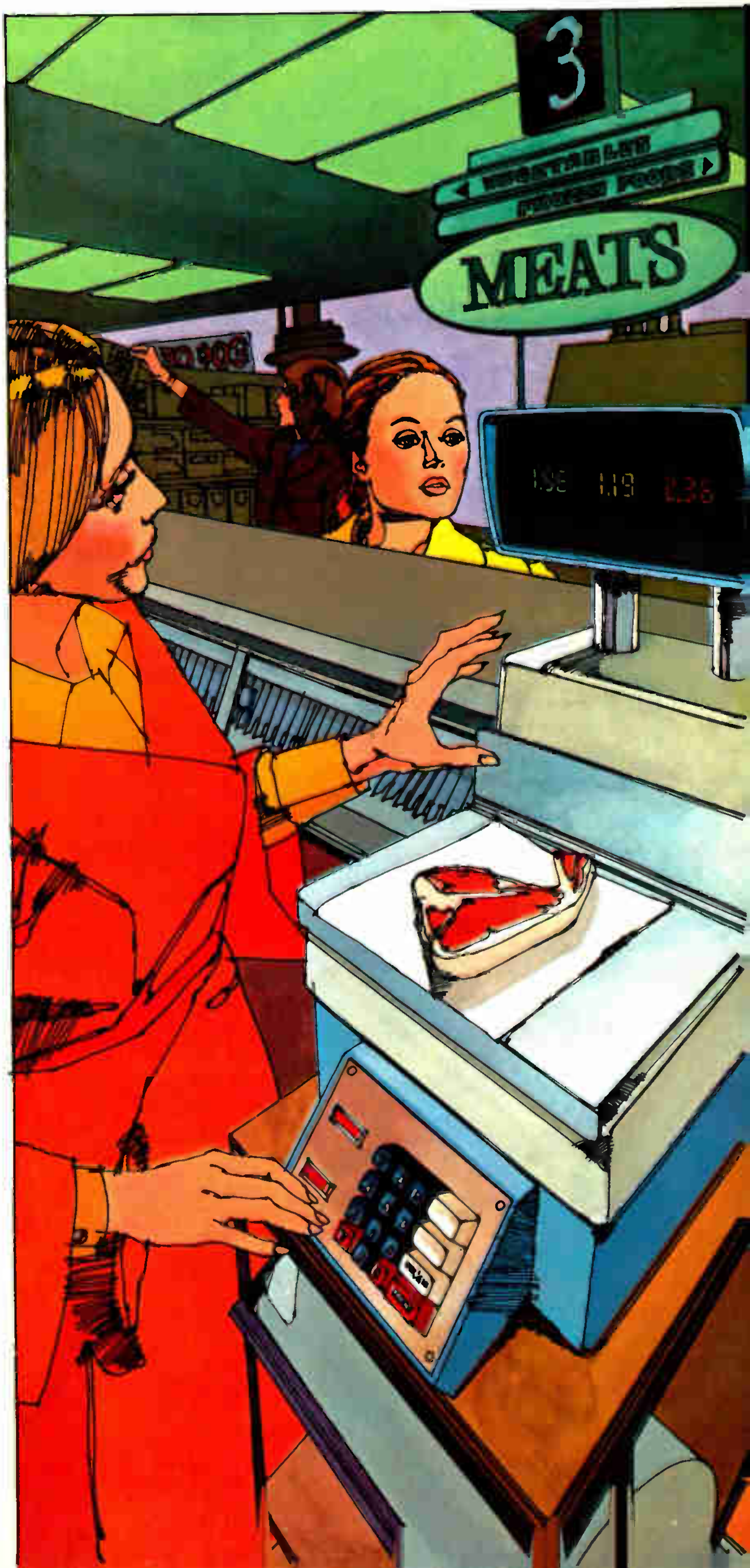
Amphenol connectors help assure correct weight in new automatic weighing system.



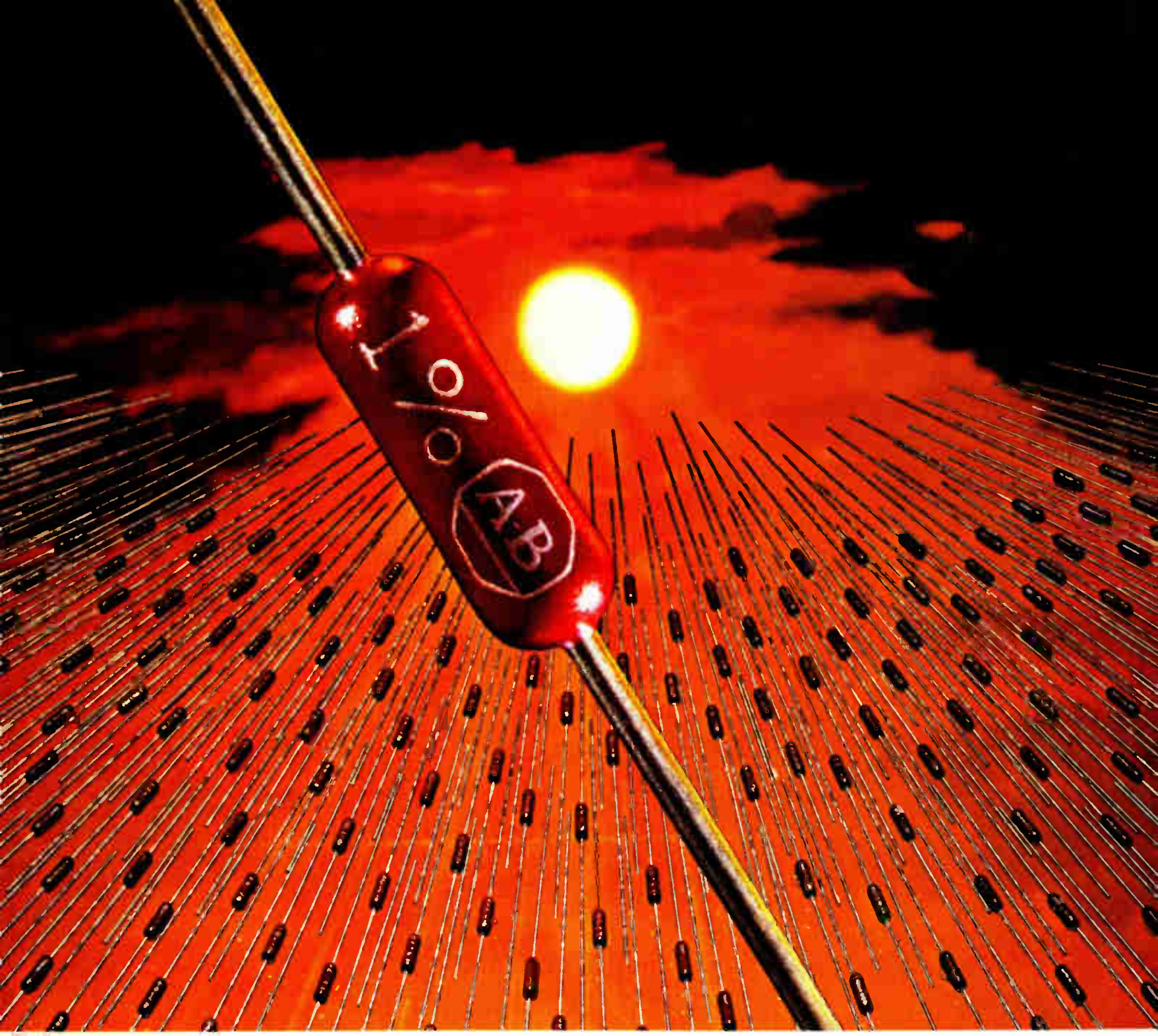
Meat merchandising has taken a big step forward with advanced solid state circuitry. The system includes a scale, mini-computer, and a printer in an integrated modular package that can weigh and price meat in seconds.

Amphenol 221 Series micro-miniature connectors share the responsibility for transmitting weight and price data to the mini-computer. Their low cost, sturdy design, and high-reliability contact configuration make them ideal for this application.

The 221 Series does the same kind of reliable work in a variety of equipment in the electronic data processing, telecommunications and home entertainment industries.



Introducing the new standard of quality in cermet film fixed resistors.



Now Allen-Bradley quality is available in cermet film fixed resistors. We coupled 40 years of know-how in reliable fixed resistor mass production with 15 years of experience in metal film resistive elements.

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For complete technical information on the Type CC cermet film fixed resistor, write Allen-Bradley Electronics Division, 1201 South Second St., Milwaukee, Wisconsin 53204.

There's more to resistors than resistance.

Circle 28 on reader service card

Actual Size

EC68

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Milwaukee, Wisconsin 53204

TI is to ship minis that use its own 4,096-bit RAM . . .

One customer apparently unworried by Texas Instruments' difficulties in making 4,096-bit MOS random-access memories [*Electronics,* March 21, p. 70] is TI's own Digital Systems division. Not only did the division begin last December to ship systems using the part to Ramada Inns, **but it will introduce a commercial version plus a new minicomputer—** both using the RAM—at the National Computer Conference, May 6 to 10. The 960B computer, a second-generation model in TI's 960 series, contains new error-detection and correction circuitry. The minicomputer is priced at $3,915 in quantity.

As for the 4k production problems, TI appears to be getting a handle on the process. **The company will begin discussing delivery schedules with customers** "in the near future," a spokesman says, "and we expect that significant shipments will be made in the second half."

. . .and another maker considers supply adequate

Although some potential customers for 4,096-bit MOS RAMs have been hesitant to commit to them, Prime Computer Inc., a three-year-old minicomputer manufacturer in Natick, Mass., **feels it can get enough parts.** So Prime has introduced a memory board built around 4k RAMs, to be offered with its models 100, 200, and 300 computers (see p. 129). The new memory system has 32,000 words, with 16 bits and 2 parity bits per word, on a 16-by-18-inch pc board.

The company is using chips from TI and Intel, but Joseph Cashen, director of engineering, says, **"We are not limited by pinout."** Accommodating chips with different pinouts would mean different board configurations. But, says Cashen, "We don't have a hangup about having more than one board." Prime says that because its logic is micro-programed, the cost of designing a second board is minimized.

TTL crunch easing, say distributors

Distributor supplies of transistor-transistor logic are catching up with demand. But for factory orders, don't look for lead times to drop below 18 weeks. Peary A. Nelson, marketing vice president at Semiconductor Specialists Inc. in Elmhurst, Ill., says, "As for production coming in from suppliers, some areas have opened up. **We even have on the shelf again 7400-series devices** that were hard to get a couple of months ago."

Nelson says his company can ship almost any TTL device out of stock on orders up to 5,000 or 10,000 pieces, and inventory on some parts is in six figures. But on large quantities of hard-to-get parts, the distributor must place a new order with semiconductor manufacturers, and the makers are still quoting 18- to 40-week lead times.

Simple gates have been hardest to get, Nelson points out, "but now that supply is catching up with demand, manufacturers are producing gates in large quantities. A major Eastern distributor agrees. Seymour Schweber, president of Schweber Electronics, Westbury, N. Y., says TTL simple functions, in short supply for months, are coming in stronger now. Deliveries are better than they were three months ago, he says.

At least one major TTL supplier challenges the distributor claims. **National Semiconductor's Gene Carter says gates and flip-flops are not in large supply.** In fact, some vendors have tried to overstock distributors with higher-price MSI, he maintains. Carter is director of marketing for the Microcircuits division.

Electronics newsletter

IC-fault tester makes use of microprocessor

Microprocessors are finding their way into instruments for testing integrated circuits via a small Titusville, Fla., company called Testline Instruments. What the firm has done in its AFIT (automatic fault-isolation tester) is to use **a brute-force in-circuit test, controlled by a microprocessor, to pinpoint both IC and board failures.** This is a departure from the usual technique of resorting to ever more powerful computerized diagnostic schemes in which elaborate procedures are applied to a board's input/output connector.

The simplicity of Testline's system saves time and money, claims president Roger Boatman. Use of a microprocessor instead of a minicomputer means that Testline **can sell its AFIT for $8,800, compared with around $25,000** for computer-controlled machines, he says. And even though a clip must be moved from IC to IC, says Boatman, the Testline method is faster because each test is performed so quickly, and faults are isolated down to specific ICs.

Two U.S. firms vie for Swedish police contract

The interest of police departments in digital communications [*Electronics,* April 18, p. 68], has spread to Europe, and now two American companies are bidding to provide equipment for tests to be run by the Swedish national police. **Competing with European terminal makers are Kustom Electronics Inc. of Chanute, Kan., and E-Systems Inc. of Dallas.**

In what is believed to be the first such tests to be conducted outside the U.S., the Swedes plan to install a display and keyboard in an unspecified number of patrol cars. The screen would be capable of handling eight 40-character lines. However, a police official says that any mass purchases of digital communications equipment would have to wait until prices are lower.

General Radio, in first public report, tells of comeback

General Radio Corp., the old-line Massachusetts instrument firm, has made a financial comeback. It had been beset in 1972 by difficulties resulting from unprofitable acquisitions and heavy expansion commitments undertaken just when the 1970-71 recession hit. **In its first publicly released annual report,** the firm, which is almost wholly owned by its employees, shows a turnaround from a net loss of more than $2 million in 1972 to a net income in 1973 of $1,157,000 on sales of $45 million. In making public its annual report, the company is paving the way to go public "in a few years."

Addenda

Hard on the heels of its new Series 60 computer systems (page 81) and its high-speed electrostatic printer (page 35), **Honeywell Information Systems plans to expand its Series 16 line of minicomputers,** probably in June. It'll be a new version of the two-year-old H-716, at lower price and with better peripheral equipment. . . . Watch for core memory maker Fabri-Tek Inc. to **enter the computer market with a 12-bit microprocessor** at the National Computer Conference. The $990 unit has a TTL processor, nonvolatile core memory of 4,096 words by 12-bits, and requires a single 5-volt power supply.

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1N5802	50						
1N5803	75						
1N5804	100	2.5	35	0.875 @ 1	1	25	Axial leaded
1N5805	125						
1N5806	150						
1N5807	50						
1N5808	75						
1N5809	100	6	125	0.875 @ 4	5	30	Axial leaded
1N5810	125						
1N5811	150						
1N5812	50						
1N5813	75						
1N5814	100	20	250	0.900 @ 10	10	35	Stud-mount D04
1N5815	125						
1N5816	150						

See Electronic Buyers' Guide Semiconductors Section for more complete product listing.

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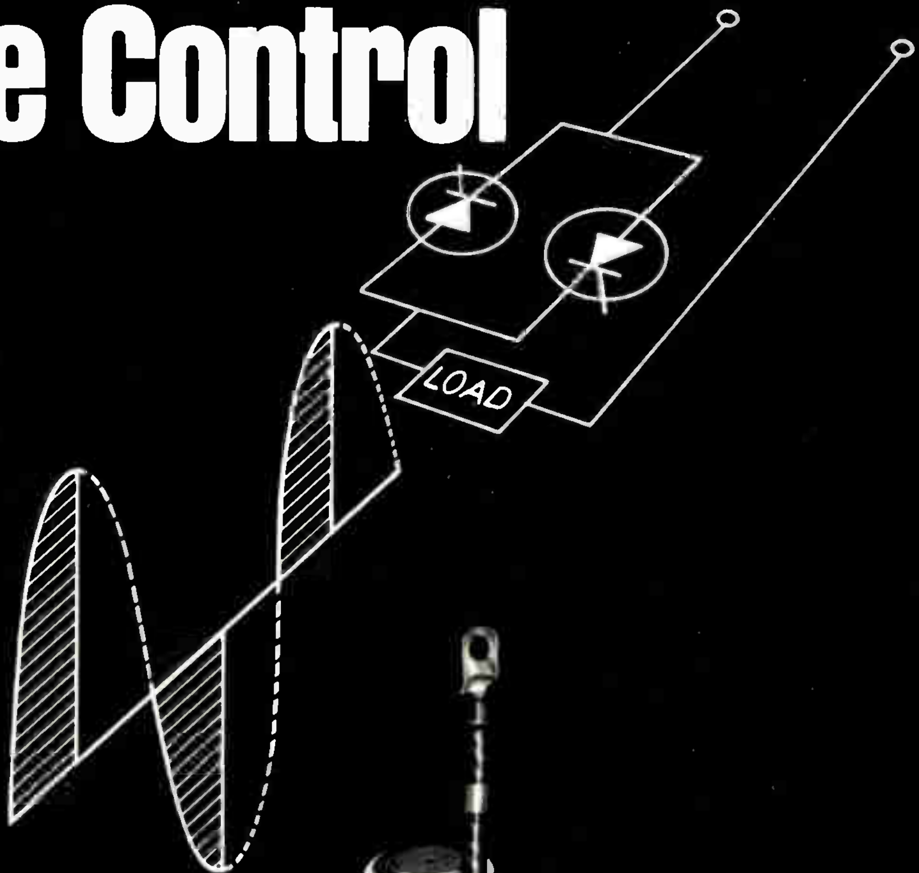

New C701 from General Electric incorporates 53 mm pellet...offers 1950A RMS, up to 1800V, 18,000A surge rating, 800A/μsec di/dt. Amplifying gate and 12% lower $\Theta_{J\text{-}C}$ with new Press Pak.

C280, C380 series offers choice of flat mount or Press Pak, 400A RMS, up to 1800V and years of field proven operation.

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New C147 operates 15% cooler than competitive types, 63A RMS, up to 1200V, 1000A pk one cycle rating, 200V/μsec dv/dt.

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GENERAL ELECTRIC

MOS computer vies for spot on new Minuteman

Rockwell p-MOS version is demonstration model designed to attract funds for one that uses SOS

The Air Force is studying follow-ons to its Minuteman III intercontinental ballistic missile, and the Autonetics division of Rockwell International Corp. hopes to prod the service into funding a radiation-resistant solid-state replacement for the Minuteman III guidance computer.

Autonetics has built a demonstration computer that uses 32-bit p-channel MOS and a nonvolatile metal-nitride-semiconductor (MNOS) memory. This machine, the advanced ballistic computer (ABC) is an order of magnitude faster than Autonetics' high-performance bipolar D37D, first designed in 1967, which has a disk memory and is used in the Minuteman III.

However, the ABC is only a demonstration unit that Rockwell hopes will persuade the Air Force to fund a computer that makes use of the company's silicon-on-sapphire technology to guide the forthcoming Minuteman-X. The C-MOS-on-sapphire technology will provide an even higher level of speed and require less power than the p-MOS model, plus better resistance to radiation.

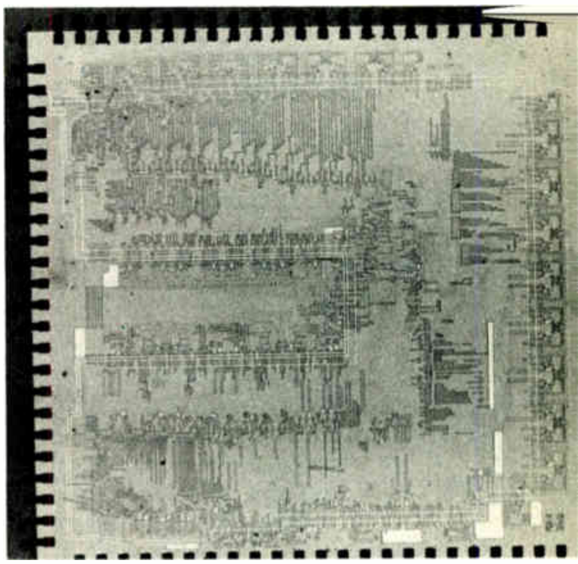
Although Rockwell isn't predicting publicly how much better performance its dream computer will deliver, the company implies some expected advantages through a comparison of its ABC with the D37D. The ABC is much smaller and lighter than the older machine, requires less power, and appears to be even more reliable. Apparently the ABC also would be much less expensive.

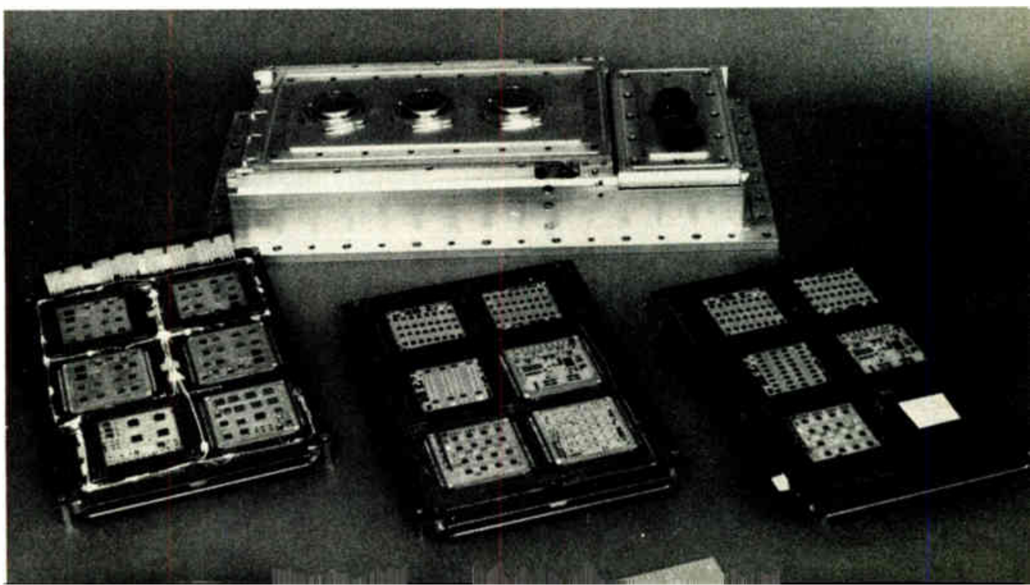
Comparison. The D37D is a 24-bit-per-word bipolar computer with 13,568 words of disk memory. The ABC has 16,000 words of memory, mostly nonvolatile MNOS. Add speed is 2 microseconds vs 78 μs for the D37D; it occupies 0.13 cubic foot, compared with 0.6 ft^3, and it weighs 16 pounds, vs 42 lb. In addition, the ABC requires less than half the power of the older machine—160 watts vs 380.

That's only the start, however. The new computer also has such functional features as hardware floating-point arithmetic, including multiplication and division, and microprogramed organization. Speed is 22 μs for 32-bit floating-point multiplication.

Reliability is also an important factor. The dramatic reduction in the number of semiconductor devices and the elimination of the rotating electromechanical disk memory has increased calculated failure rates from 0.06% per 1,000 hours to 0.01%. Component cost should also be reduced dramatically, with $20 MOS devices replacing some $1,400 worth of bipolars.

The four-phase central-processing unit of the advanced computer is





Test model. Three modules—power supply, central processor, and input/output—make up advanced ballistic missile computer designed with Minuteman-X in mind. One chip has a whopping 92 beam-type leads.

made up of p-MOS LSI. Most of it is fabricated by the Rockwell Microelectronic Device division, Anaheim, Calif., but it was designed by the Autonetics Components and Microelectronics Laboratory under Thomas Gunckel. The CPU contains 57 chips of 10 types, plus six microprogramable read-only-memory chips.

The input/output section contains 14 MOS chips of three types (one common to the CPU), and the memory contains three types of MOS chips: 2,048 bits of MOS random-access scratchpad memory, 2,048 bits of MNOS electrically alterable read-only memory (Earom), and 12,288 bits of MNOS RAM. The Earom is made by National Cash Register Co., but was designed by Rockwell. The other MNOS is from the Rockwell Microelectronics group. Bipolar devices are used in the clocks, memory timing, control, and power supply, as well as for drivers and receivers.

All semiconductor devices are in chip form and mounted by beam leads on multilayer thick films deposited on 2-by-2-inch ceramic substrates. The devices, which have up to 92 pins, typically measure 250 mils on a side. The hybrid substrates themselves have 348 leads and can be plugged into connectors for testing or in lead frames for flight use.

Most of the beam leads are actually gold ribbons that Rockwell has added to finished, nitride-passivated MOS and bipolar devices. A full complement of beam-lead parts is not available, points out Gunckel, but "the parts look and act like true beam leads after the ribbons are attached." He also says they can meet military standards. The parts are wobble-bonded to the substrate. □

Displays

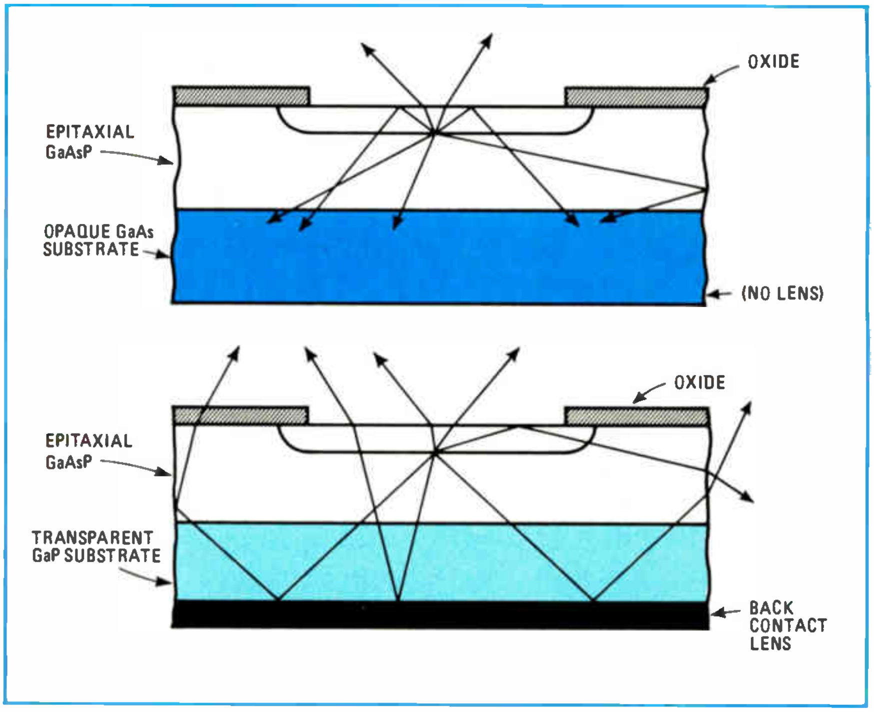
GaP under GaAsP brightens LED colors

Gallium-phosphide diodes that emit green or yellow light cost more and are usually dimmer than red LEDs made of gallium-arsenide-phosphide because it's difficult to manufacture high-bandgap, short-wavelength GaP material with good enough yields and output efficiencies. But workers at the HPA division of Hewlett-Packard Co. now appear to have the problem licked.

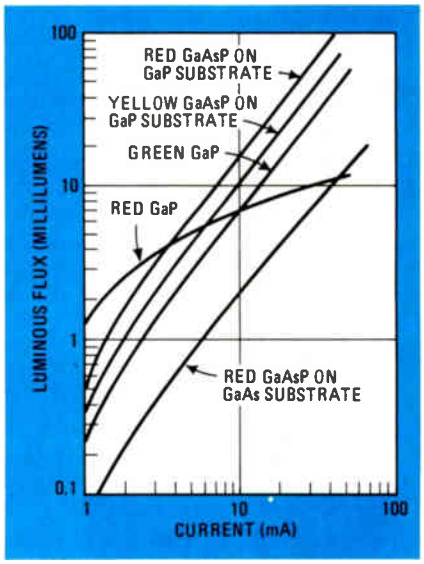
HPA obtains efficient high-bandgap emission by combining the easier-to-manufacture GaAsP pn junction with a GaP substrate. Using this system, the division plans to introduce discrete LED lamps in yellow, green, and high-efficiency red by the end of the month and to follow them with 0.6-inch-high digits in the same colors.

The success of the new structure derives from GaP's transparancy to light emitted by a GaAsP junction—as opposed to its opaqueness to the shorter wavelengths emitted by GaP junctions. When the GaAsP-on-GaP combination is backed by a reflecting lens, a much greater fraction of light can be collected at the output cavity, and the resulting colors appear brighter and clearer than is the case with GaP-only systems.

Rick Kniss, product marketing manager at HPA, claims that because of the transparent substrate and lens system, the lamps have an 180° viewing angle of near-constant intensity, in contrast to many other yellows and greens that have narrow viewing angles. Equally important, Kniss points out that "although GaP junctions emitting at yellow and green wavelengths may be more efficient at low currents, it saturates at about 20 milliamperes, while GaAsP remains linear." This



Bright idea. New LED has a GaAsP pn junction on a transparent GaP substrate that transmits a maximum amount of light. Old GaAsP on GaAs substrate is less efficient because the substrate is opaque. Output of the new structure is higher than is straight GaP.



is important in high-current strobe systems, where a high drive current, say 50 mA, is needed to power the lamps in parallel. GaP lamps will saturate, but GaAsP-on-GaP lamps won't. □

Instrumentation

Laser triggers 8-MV test jolt

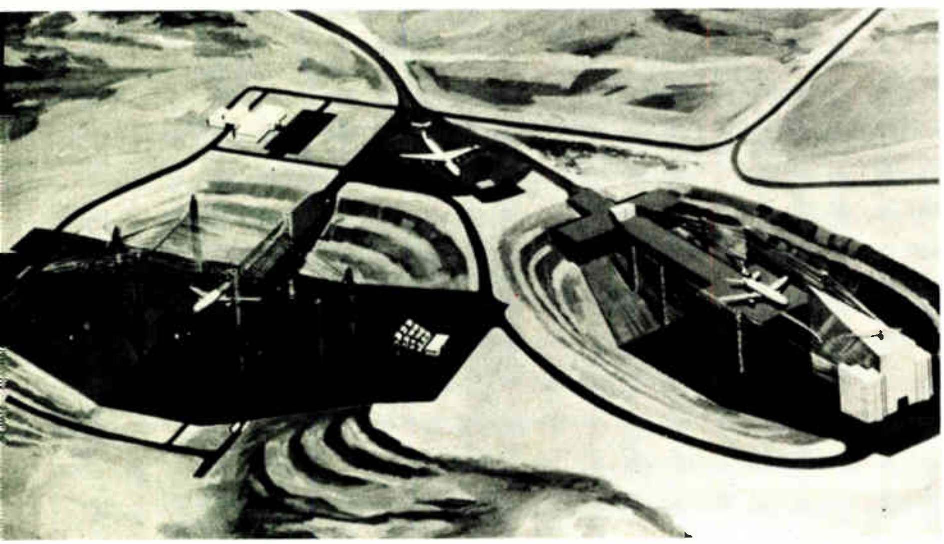
An 8-megavolt discharge that simulates the electromagnetic pulse (EMP) of a nuclear blast is being triggered by a laser signal carried by fiber-optic cables. These blasts are designed to test the effects of EMP on electronic systems in aircraft at the Air Force Weapons Laboratory, Kirtland AFB, Albuquerque, N.M. The fiber-optic transmission system, which is 100 feet long, is needed to isolate the sensitive triggering and monitoring equipment from the 8-MV bang. Fiber-optic pipes are used to transmit the test measurements, and to detect the time of firing.

McDonnell Douglas Astrionics Co. is prime contractor for the $19.5 million Trestle, so-called because the nonmetallic trestle-like structures that hold the aircraft are built entirely of wood, held together with nonconducting nylon screws and epoxy so that the aircraft appears to be in flight when undergoing tests.

This facility, scheduled for completion early in 1976, is as long as three football fields. One trestle is for testing horizontal components of the EMP wave, and the other tests the vertical ones. Each trestle is large enough to handle aircraft the size of a Boeing 747.

The pulse that simulates the nuclear blast is generated by triggering an 8-MV pulse in 10 nanoseconds through an antenna near the aircraft. Maxwell Laboratories, San Diego, has a $4.2 million subcontract to supply the high-voltage pulse generator. American Laser Systems, a small Santa Barbara, Calif., firm is supplying three subsystems: a dielectric trigger link with 350-picosecond rise time, usable with a maximum of 200 feet of fiber-optic cable, an optical transmission set that uses an LED transmitter and avalanche photodetector coupled by fiber optics, and a monitor for the output switch that handles the high voltage.

Test site. Fiber-optic light pipe triggers 8-megavolt blast at Air Force test facility.



Optical coupling. To prevent dangerous feedback, optical coupling is used to trigger the 8-MV pulse. The trigger, which consists of a gallium-arsenide laser actuated by a 5-V input pulse, has been operating since last November at a Maxwell Laboratories test site in San Diego.

Using low-loss fiber-optic cables [*Electronics*, March 21, p.89], the light is carried from the laser via four separate light pipes to avalanche-diode photodetectors 100 feet away. These fast-acting detectors—the delay in the trigger must be less than 1 ns—then trigger four Marx generators. These generators employ a well-known technique for generating high voltage by charging capacitors in parallel and discharging them in series.

On the receiving end, the photodetector is followed by a wide-band preamplifier and threshold detector that can drive a 50-ohm load to more than 100 V with a rise time of 2 ns. Extremely low jitter is vital, since the four units must drive the separate Marx pulse modules, points out American Laser's president, Duncan Campbell. The jitter is held to less than 250 picoseconds.

The 8-MV pulse travels down antenna wires placed on either side of the aircraft. The two sides form a transmission line so that the plane is, in effect, inside a parallel-plate line that has an impedance of about 108 ohms. To prevent ringing, the plates are terminated in sea-water with a resistance of that value.

The American Laser system also includes two other fiber-optic links. One link transmits data that's been monitored to show the performance of the electronic equipment involved in the test. It consists of a LED transmitter, another 100-foot fiber-optic link, and an avalanche photodetector. The second link is placed next to one of the firing switches that helps to discharge the Marx generators. A fiber-optic cable carries the switch signal to a detector as a zero-time base for the monitored data. □

Computers

Speedy printer is electrostatic

In introducing its new series of computers, Honeywell Inc. (see p. 81) has also brought to market what is likely to be the world's fastest commercially available computer-output printer. It is an off-line electrostatic machine that can print as many as 210 pages per minute, equivalent to 18,000 lines per minute with up to 132 characters. This is three or four times as fast as the fastest output printers—also electrostatic units—available until now.

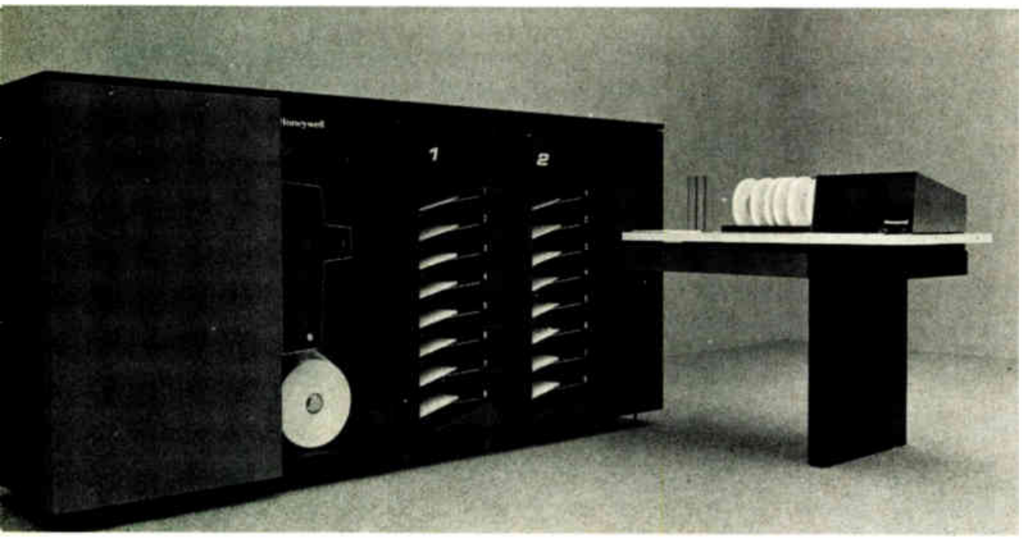
The first two printers have been shipped to Lawrence Livermore Laboratory in Livermore, Calif. The laboratory is replacing its 10-year-old Radiation Inc. electric-arc printer, a one-of-a-kind machine that produces 30,000 lines per minute. [*Electronics,* July 19, 1971, p. 32; Nov. 6, 1972, p. 44]. The printers will be programed for graphics and run with Livermore's vast Octopus computer network. The machine can print a fixed form along with variable data, and can collate up to 32 copies printed in succession.

Costs of the systems are high—the 210 page per minute machine is priced at $193,620, while a slower model that handles 140 pages per minute is priced at $162,120. However, Honeywell believes the machines will find their niches in other large-scale data-processing centers.

Electrode design. The design of the electrodes is a key point in the over-all design of the printer. These electrodes deposit the static charges for fixing the toner, or "ink," on the paper in an electrostatic machine. Most other electrostatic printers use a single row of either round or square electrodes connected to drive circuits through closely spaced etched wiring or through tightly packed cables—all of which present relatively high-capacitance loads to the drive circuits. At conventional speeds, this capacitance is only a minor problem, but in the Honeywell printer, the high printing speed requires narrow pulses with fast rise times, for which a capacitive load is formidable.

So, to reduce the capacitance, the electrodes were put in two well-spaced rows; they were made rectangular, with the closest spacing between the shorter sides of the rectangles; and the etched connections to the drive circuits fan out widely to well-separated connectors that plug directly into the boards carrying the drive circuits.

The electrodes consist of 2,112 etched-copper rectangles in two rows on a flexible substrate. Each rectangle measures 1 by 5 mils, with the long dimension in the direction perpendicular to the paper motion. The rectangles in each row are 5 mils apart. The second row of electrodes is staggered so that its electrodes lie exactly opposite the gaps in the first row.



Speed champ. Electrostatic printer from Honeywell spews out 18,000 lines of up to 132 characters each per minute on 8½- or 11-inch-wide paper.

Raster. A raster-scan technique places a voltage of about 500 V on selected electrodes in the array; as long as this voltage remains, the surface of the paper passing nearby is charged, resulting in a solid vertical line 5 mils wide, such as the left side of the letter E.

For a single 5-mil-square dot, which would be nearly invisible, the 1-mil-wide electrode would be left on long enough for 5 mils of paper to go by—approximately 160 microseconds at 30 inches per second. For a solid horizontal line, several adjacent electrodes in one row would be turned on long enough to produce a series of dashes of the desired width; then, when the paper is under the second row, electrodes would be turned on to fill in the gaps between dashes.

The system is controlled by a Honeywell 716 minicomputer, which also translates data, if necessary, from the magnetic-tape input code to Ascii for the printer's character generator. Tape drives are available for either 7- or 9-track tapes or both. Honeywell has also designed a drive to handle both formats. This dual-drive system has two heads, of which only one operates at a time.

The system uses coated electrographic paper in roll form, either 8½ or 11 inches wide, on which it prints characters spaced 12.56 to the inch horizontally and 10 to the inch vertically, compared to 10 and 6 per inch in conventional printers.

The printer's standard character generator accepts the 96 printable characters in Ascii; the set can be expanded to as many as 512 by substituting the proper character generator. Unlike most conventional printers, expanding the character set in this way doesn't slow down the printer. □

Communications

Optical, mm-waves offer promise

The wideband systems that will be transmitting large volumes of data at high speeds in the 1980s will combine optical and millimeter-wave links. That's the prediction of a study recently completed for the Air

Force's Rome Air Development Center by Martin Marietta Aerospace, Orlando, Fla.

The Air Force commissioned the study as an aid to planning future intrabase communications between rapidly deployed command posts and a central headquarters unit. But the authors say much of the report applies equally well to commercial intracity links.

The major conclusion is that optical links are superior to mm-wave links only for distances of 1 kilometer or less, according to Terry Duffield, Martin Marietta staff engineer. In a paper being presented this week at IEEE Southeastcon in Orlando, Duffield says that the cost and performance studies performed by RADC show that the two types of systems are about equal between 1 and 3 km, but that millimeter waves take over at longer distances. In a related paper, Martin Marietta's H.B. Muench adds that today's optical systems are ready for serious consideration as short links.

Duffield's study, which projected cost and performance figures through the late 1970s and into the 1980s, centered on systems with information bandwidths greater than 500 megahertz and all-weather reliability of 99.9%. The millimeter wave systems were solid-state systems using bulk-effect devices for sources. The optical systems used light-emitting diodes for the short links, gallium-arsenide lasers for links in the 2- to 3-km range, and carbon-dioxide and neodymium-doped yttrium-aluminum-garnet lasers for the longer links.

The recent price reductions for gallium-arsenide lasers is the basis for Muench's conclusion that they could be used in communications today. Lasers that were selling for more than $100 six months ago, he says, now are available for less than $20. In his paper, he quotes a recent Army (Fort Monmouth, N.J.) estimate of a $1,000 cost per terminal for a gallium-arsenide system operating at 10 megabits per second. Muench says that this cost may be achieved by early next year.

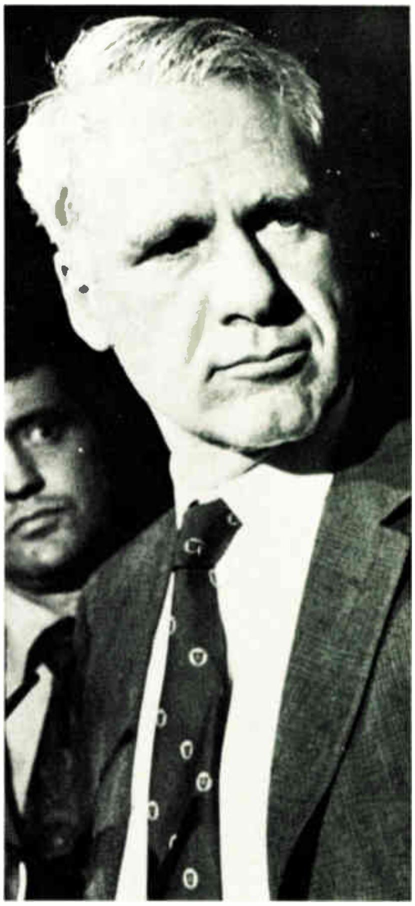
With such a system operating at 1.5 megabits per second, Muench points out that it could be useful for setting up short links in a telephone system to avoid the need to lay cables for a T1-type link, the Bell System designation for equipment that multiplexes 24 voice conversations on one wire pair. Muench says that such a system could be useful in, say, new housing developments to bring voice signals to a central switching office, or for setting up emergency communications. □

Military electronics

Schlesinger wants to save Sanguine, despite Navy's decision to suspend it

Secretary of Defense James R. Schlesinger reportedly wants to save the controversial Project Sanguine. He is convinced that the secure, extremely-low-frequency transmission system for the Navy's fleet ballistic missile force is indispensable. Schlesinger's views—linking Sanguine to his doctrine of precise targeting and limited use of submarine-based ICBMs—were being circulated by Pentagon officials following the Navy's April disclosure that it was suspending work on the project for the remaining two months of the fiscal year. The reason: a 42% overrun on Sanguine's $8.3 million budget for fiscal 1974.

Sanguine's public problems and its priority among Pentagon programs have resembled a wildly bouncing ball in the five years since the Naval Electronic Systems Command began serious work on it. The transmission system, which is to be based in the continental United States, is designed to provide a secure means of ordering submarine missile launches. Last December, the decision to appropriate 50% of



Adamant. DOD's Schlesinger considers Sanguine vital for sub-launched missiles.

the Navy request for fiscal 1974 proved a last-minute compromise by a House-Senate conference committee, after the House had eliminated the $16.7 million sought and had ordered the program terminated [*Electronics*, Dec. 6, 1973, p. 59]. This year, Navelex is asking $13.2 million in the fiscal 1975 budget now before Congress.

DOD officials say the Navy again is unlikely to get the full fiscal 1975 request, but they note that Schlesinger is prepared to fight for the program, even at a lower funding level.

The Defense Secretary is described as convinced that Sanguine is essential to give the U.S. the capability to launch selected missiles at enemy military targets in the event of "a limited nuclear exchange" with the Soviet Union. By giving Sanguine the capability of transmitting weather and other data affecting missile trajectories, along

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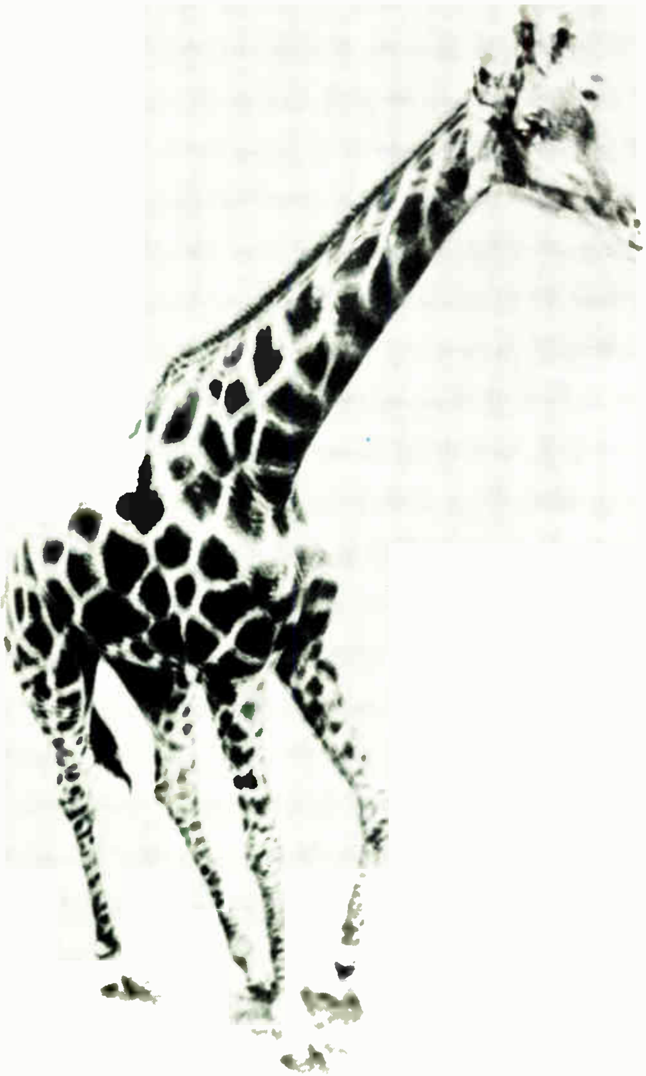

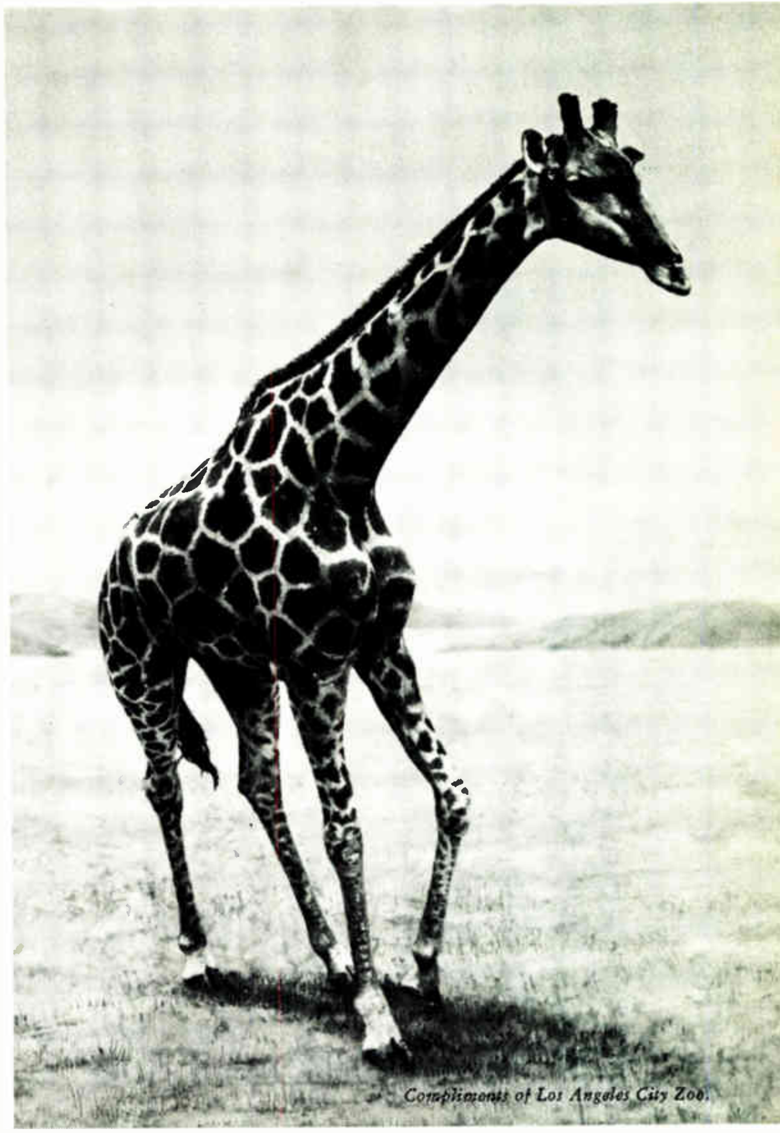

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with an attack order, U.S. submarines could then adjust missile guidance systems to compensate for such factors and could aim their weapons with greater precision at smaller military targets, instead of being limited to targeting large industrial urban areas.

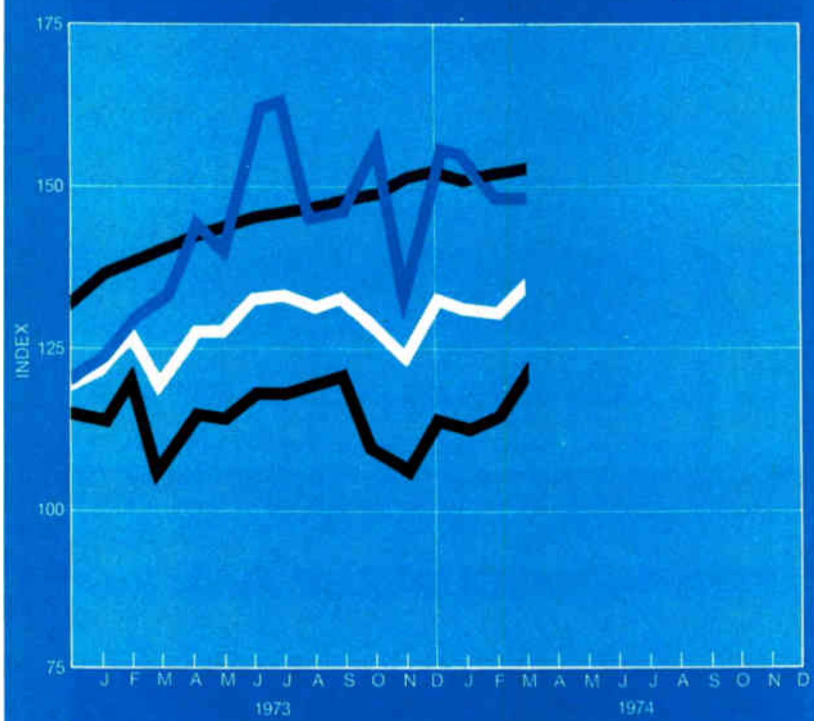
The Navy has spent $73 million overall on Sanguine so far. Estimates of what it would cost to complete the program initially ran between $800 million and $1.2 billion, but the Navy said it determined last year that it could halve the radiated power from 300 to 150 amperes at a likely carrier frequency of 45 or 75 hertz and still have a satisfactory system costing $100 to $400 million, exclusive of R&D.

Dispute. Sanguine site locations, in which a checkerboard-like grid of cables ranging from 40 to 80 miles square, must be built into massive nonconductive rock strata, have been a matter of controversy almost from the beginning [*Electronics*, Nov. 24, 1969, p. 48]. Opposition to the first site proposed, at Chequamegon National Forest in Wisconsin, came largely from environmentalists and local residents. Similar groups objected to alternative sites in northern Texas and the upper Michigan peninsula.

The site issue, compounded by Sanguine's need for a large nonconductive rock formation to contain its buried cable grid, is expected to be as much a problem for Secretary Schlesinger as the project's costs. Nevertheless, DOD is expected to push hard for continuing the project. One approach to the Congress being considered is to hold the program in low-profile studies "for another year," according to military sources, and to use that time to persuade opponents to the program of its importance in strategic policy, as well as its environmental safety when operated at the reduced powers now being contemplated.

Suspension of the Sanguine effort came before the award of two parallel development awards later this year but after completion of design validation proposals by three contractors. They were GTE Sylvania Electric Products Inc., Waltham, Mass., RCA Communications Systems, Camden, N.J., and TRW Systems Group, Redondo Beach, Calif. Other studies had been performed by MIT's Lincoln Laboratory and the Naval Underwater Systems Center, Newport, R.I. □

Electronics Index of Activity



Segment of Industry	Mar. '74	Feb. '74*	Mar. '73
Industrial-commercial electronics	148.6	148.6	141.5
Consumer electronics	122.4	114.4	117.9
Defense electronics	153.0	152.7	140.4
Total industry	136.1	131.7	128.8

The index registered its fourth straight monthly increase, rising 3.3% in March and bucking a declining national trend. The largest gainer was the defense component, which climbed 7.0% from February's level. The industrial-commercial sector inched up 0.2%, but was 9.0% higher than a year ago. Consumer electronics was unchanged.

Indexes chart pace of production volume for total industry and each segment. The base period, equal to 100, is the average of 1965 monthly output for each of the three parts of the industry. Index numbers are expressed as a percentage of the base period. Data is seasonally adjusted.
*Revised.

Government

Contractors seek more IR&D freedom

Full reimbursement of independent research and development costs and bid and proposal costs, the elimination of cost ceilings, and elimination of the requirement for "potential military relationships" for IR&D is being urged on the Congress by a three-association committee of Government electronics and aerospace contractors. The recommendations, developed jointly by the Electronic Industries Association, the National Security Industrial Association, and the Aerospace Industries Associ-

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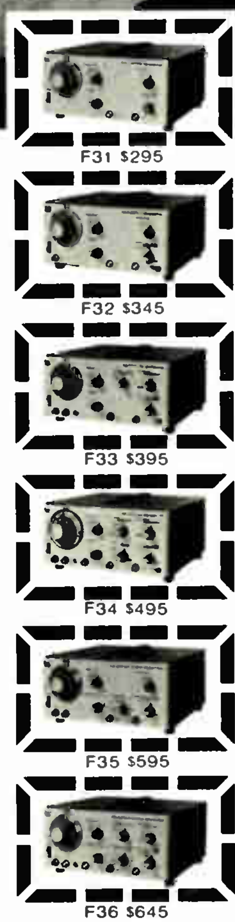

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ation, were disclosed near the end of April in response to renewed congressional interest in the reimbursement of IR&D and bid and proposal costs by Defense Department, NASA, and the Atomic Energy Commission.

In disclosing the recommendations of their *ad hoc* committee, the three trade groups said they had developed their position in response to 22 questions on IR&D posed to the General Accounting Office last October by Sen. William Proxmire (D., Wis.), chairman of the Senate subcommittee on priorities and economy in Government, and Sen. Thomas J. McIntyre, (D., N.H.), chairman of the research and development subcommittee of the Armed Services Committee. The senators' joint queries to the GAO have produced a full-scale investigation of the IR&D and bid and proposal issue by the congressional watchdog agency.

GAO officials say the study is expected to be complete near the end of the year, although an interim report may be available to the two senators in May.

Funds. At stake is an annual Federal fund of approximately $400 million for IR&D reimbursement and an estimated $300 million more in bid and proposal costs, according to the industry associations. Citing one DOD study last year summarizing statistics from 77 major contractors, the group notes that "in 1972, DOD obtained access to $776 million of IR&D work, while accepting only $400 million as its share of the costs" to the contractors.

In a 34-page summary position paper, the three associations contend that "IR&D and B&P expense allocated to defense contracts has modestly increased in recent years. While absolute dollars increased from $685 million in 1968 to $704 million in 1972 because of inflation and the new Government requirement to burden the direct man-hour base, man-hours of effort have actually declined by approximately 28%."

Challenging the view that these costs are insufficiently controlled, the contractors contend that

News briefs

Motorola asked to find new buyer

Motorola Inc.'s sale of its TV receiver business to Matsushita Electric Industrial Co. [Electronics, April 18, p. 40] raises "antitrust questions," according to the U.S. Dept. of Justice. The proposed sale has therefore been ordered postponed until May 28. In that period, Motorola has agreed to make "a good faith effort" to find another buyer. The Department said it would not block the sale if Matsushita's purchase were "the only means of retaining Motorola's TV business as a viable competitor," but called on Motorola to entertain any offer from other companies regardless of how the offer compares to Matsushita's. Motorola says it has retained the brokerage firm of Goldman Sachs & Co. to try and find an alternate buyer.

AT&T and GTE join forces . . .

AT&T and GTE Satellite have announced that they will join their proposed domestic satellites into a $90 million system using three GTE and four AT&T earth stations and the three satellites that AT&T will lease from Comsat. Pending FCC approval, AT&T has agreed to suspend a lawsuit filed last fall aimed to overturn an FCC decision that provided that both communications companies could provide the same service in the same areas.

. . . while AT&T suffers a setback

The FCC has ordered AT&T and its Bell System affiliates to cease and desist the removal of interconnection services to MCI Communications Corp. customers. Prior to this order, Bell companies had disconnected nine MCI customers. MCI had filed a suit against AT&T. The FCC order came on the heels of a Federal Appeals Court ruling that turned jurisdiction back to the FCC and overturned a lower court ruling that ordered AT&T to service specialized carriers [Electronics, Jan. 10, p. 30]. AT&T has gone to court to have the FCC decision reviewed.

Comsat, Solarex dispute

Communications Satellite Corp. has sued Solarex Corp., Rockville, Md., [*Electronics*, Oct. 11, 1973, p. 14] claiming that Solarex partners Joseph Lindmayer and Peter Varadi are using "violet" solar-cell techniques [*Electronics*, May 22, 1972, p. 30] developed while they were with Comsat. Comsat is asking injunctive relief and about $1 million in damages. Solarex has countersued for $35 million stating that Comsat's suit, based on false charges maliciously interferes with Solarex's business and acquisition of solar cell producer Centralab [Electronics, March 7, p. 40]. Solarex also says its charter is violated by Comsat's interest in terrestrial solar cells.

Philco-Ford wins ground-station contract . . .

A $96.3 million contract has been awarded to Philco-Ford Corp. to build a worldwide network of 21 AN/MSC-60 ground terminals for the U.S. Defense Department's second generation Defense Satellite Communications System. The company's Western Development Laboratories, which won an $8 million development contract in June 1970, will build the terminals.

. . . and Westar is tested

Western Union's Westar, the first U.S. domestic communications satellite, launched April 13, is in stationary orbit over the equator, almost due south of Dallas, Texas. Western Union is now testing Westar's 12 transponders and will continue to do so until the satellite is put into operation in June, at the launching of Westar II for backup.

Allen promoted to defense research deputy

John L. Allen, former associate director of research for electronics at the Naval Research Laboratory, has been appointed Deputy Director of Defense Research and Engineering for research and advanced technology. Allen is a specialist in antennas and radar-systems research.

"present regulations tend toward over-control and inhibition of IR&D and B&P." In addition to calling for full reimbursement of Government contractors and the elimination of both cost ceilings and the required military relationship for IR&D, the associations also:

- Oppose establishment of line items in agency budgets for IR&D and bid and proposal costs "as though these efforts were commodities to be priced. These are indirect costs, part of industry overhead, and as such, are appropriately included in product or contract estimates."
- Oppose creation of a new Federal agency responsible for operational aspects of IR&D and bid and proposal costs, but favor establishment of a common Federal policy and practice for all agencies.
- Want Congress to "specifically express positive support for IR&D and B&P and correct the current motivation to continually reduce this effort." □

Memories

'Bulk' hologram uses organics

By using organic materials in an optical memory, researchers at Battelle Memorial Institute, Columbus, Ohio, expect to achieve a bit density 10 times greater than has been yielded in holograms made of such single-crystal inorganics as lithium niobate. Chemically classed as stilbenes, colored powders used in the manufacture of textile dyes, the material can store 100 million bits per square centimeter by stacking as many as 100 holograms per millimeter of material depth.

Although organic materials have been tried for surface holograms, this is the first reported use in a volume hologram, meaning that storage is in the bulk of the material, claims Battelle chemist Richard A. Nathan. Prototype material to demonstrate the storage ability will be delivered to NASA's Langley Research Center this month, and "we estimate that we could have an optimized, fully complete memory within two years," says Nathan. Moreover, based on the laboratory experiments conducted so far, he continues, the concept shows promise for meeting most of the requirements set by NASA for optical-memory systems.

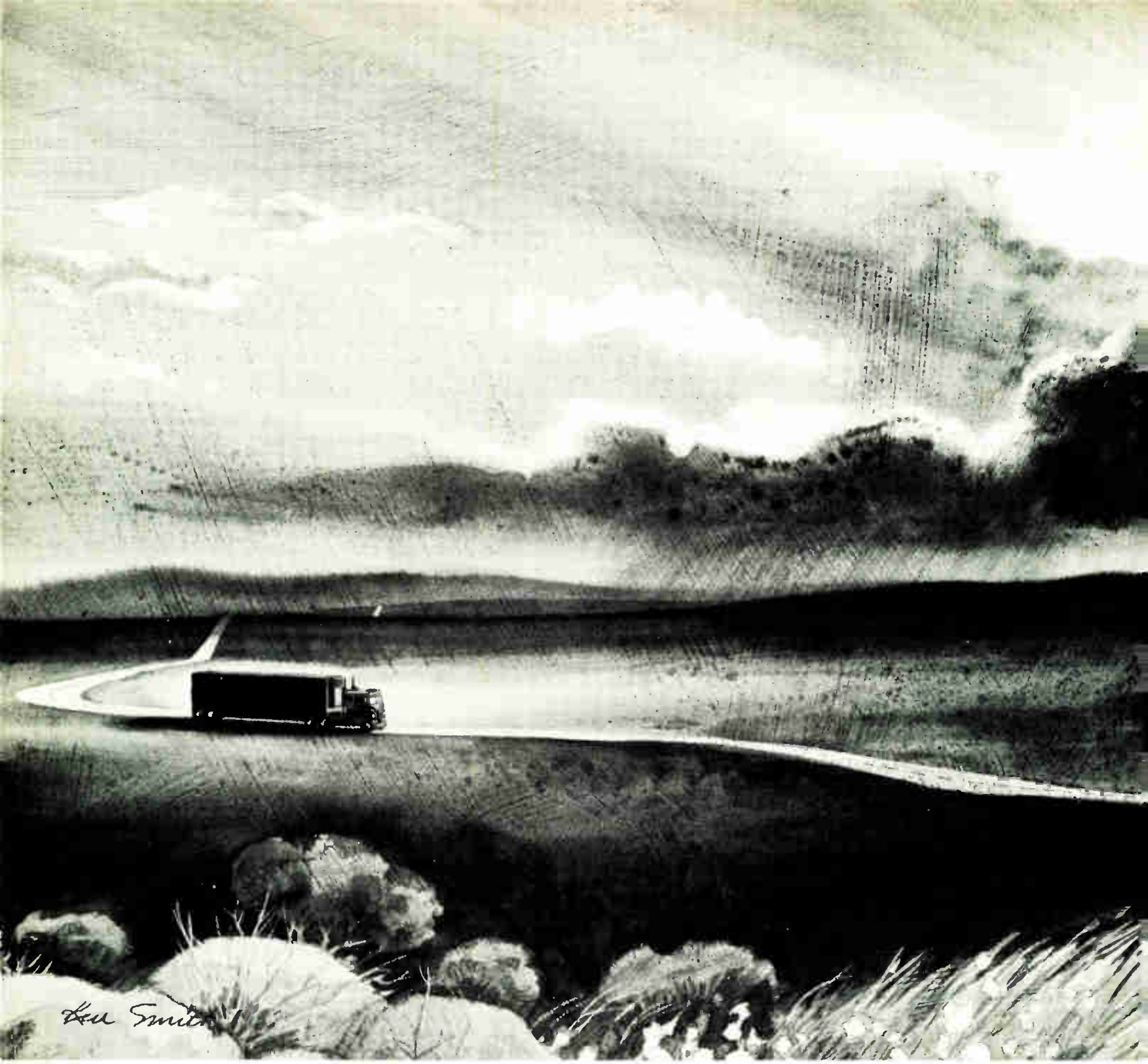
Storage relies on differences in the index of refraction of two stable isomers—materials with the same molecular formula but different geometric structures—of selected stilbenes; the change from one isomer to another is triggered by a laser.

"We've found that we can store a lot more information per unit volume than we can with single-crystal inorganics," Nathan continues. These inorganics also rely for information storage on differences in indexes of refraction. However, with the stilbenes, "the difference in the change in the index is two or three times greater. This permits us to superimpose up to 100 holograms, instead of the five or 10 possible with inorganic materials.

Stacking. Different holograms are stacked by changing either the angle or the wavelength of the incident light.Holograms are sorted out by reading data out at the same angle at which it was recorded.

At a particular incident angle, writing requires one wavelength, and erasing, another. Reading is done with a third wavelength that does not cause the material to be converted from one isomer to another. "In this class of materials, we can find materials that isomerize with high efficiency from one form to another at wavelengths produced by small economic lasers," Nathan explains. "We'd like to have the three wavelengths sufficiently close together so that we could use a single, tunable laser."

While all materials have limiting properties, he points out, the ability to tailor the organic compounds far exceeds that of single-crystal inorganics, and organic materials are generally more economical. Also, isomerization of organics requires less energy, permitting the lasers to be compact and inexpensive. □



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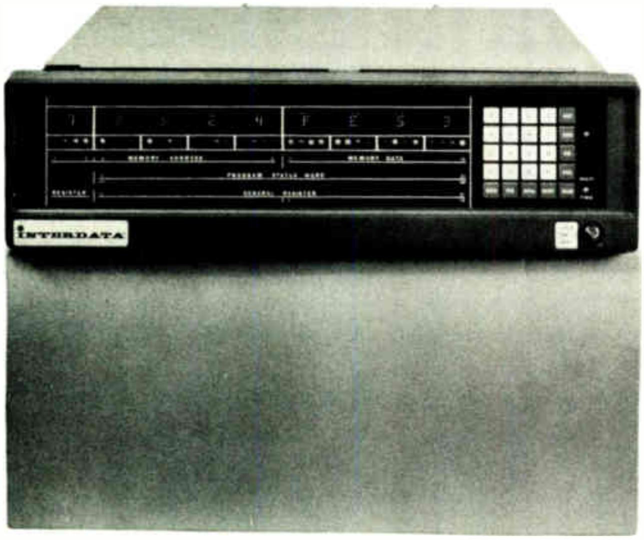

Performance	7/32	Nova 840	PDP-11/40
Word length	32	16	16
Memory speed (nanoseconds)	750	800	900
Maximum memory capacity (bytes)	1,048,576	262,144	262,144
Addressing range (bytes)			
Direct	1,048,576	512	65,536
Relative	±16,384	±256	±32,768
Indexed	1,048,576	65,536	65,536
Double indexed	1,048,576	No	No
General-purpose registers	32 32-bit	4 16-bit	8 16-bit
Index registers	30 32-bit	2 16-bit	8 16-bit
Vectored interrupt levels	Yes	No	Yes
Minimum interrupt overhead time (usec)	6.5	47.5	46.5

Price	7/32	Nova 840	PDP-11/40
32 KB processor	$ 9,950	$12,930	$15,345
64 KB processor	14,450	19,330	26,925
128 KB processor	23,450	35,630	44,725
256 KB processor	41,450	61,230	80,825
1 Megabyte processor	171,650	Not available	Not available

Source: Data General Price List, 5/15/73. DEC PDP-11/40 Price List, 6/73. DEC OEM & Product Services Catalog, 1972. Auerbach Minicomputer Characteristic Digest, June, 1973. "How to use Nova Computers", 1973.

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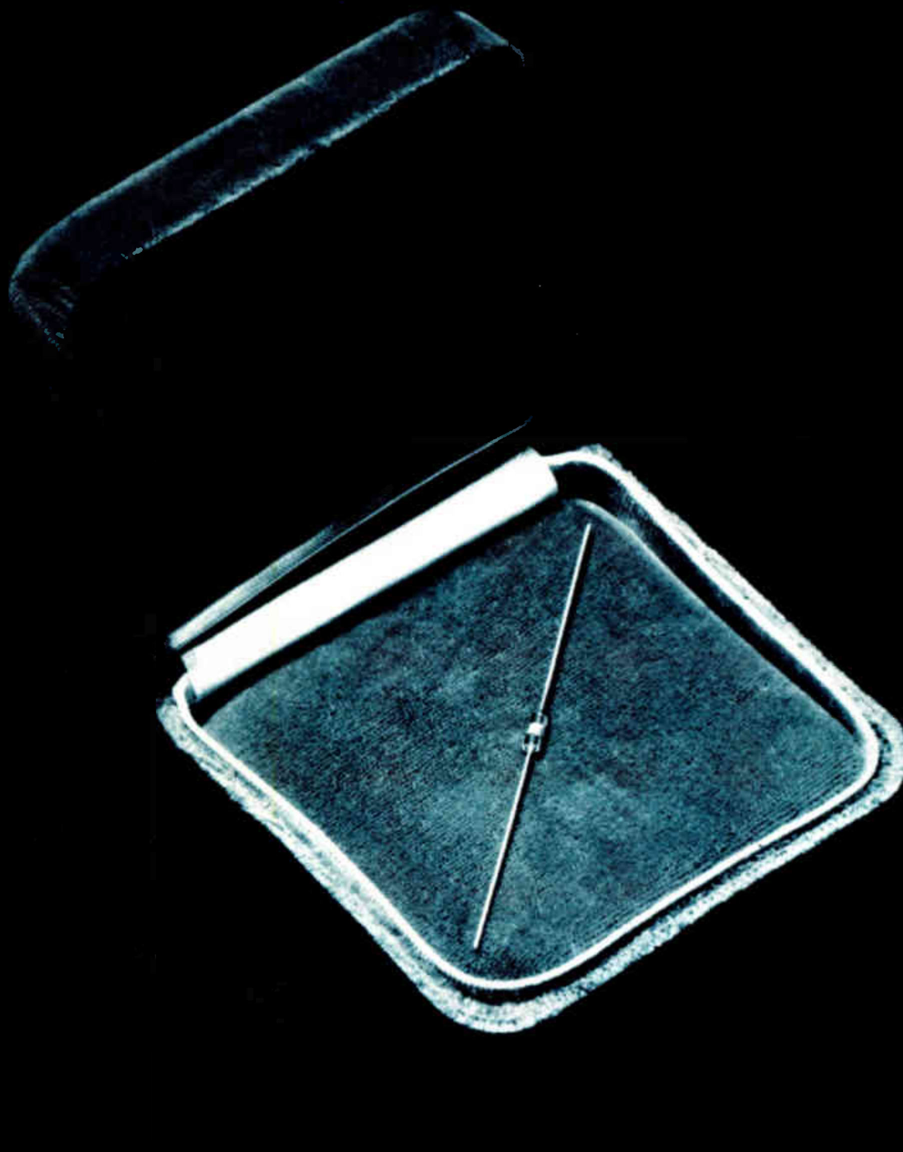
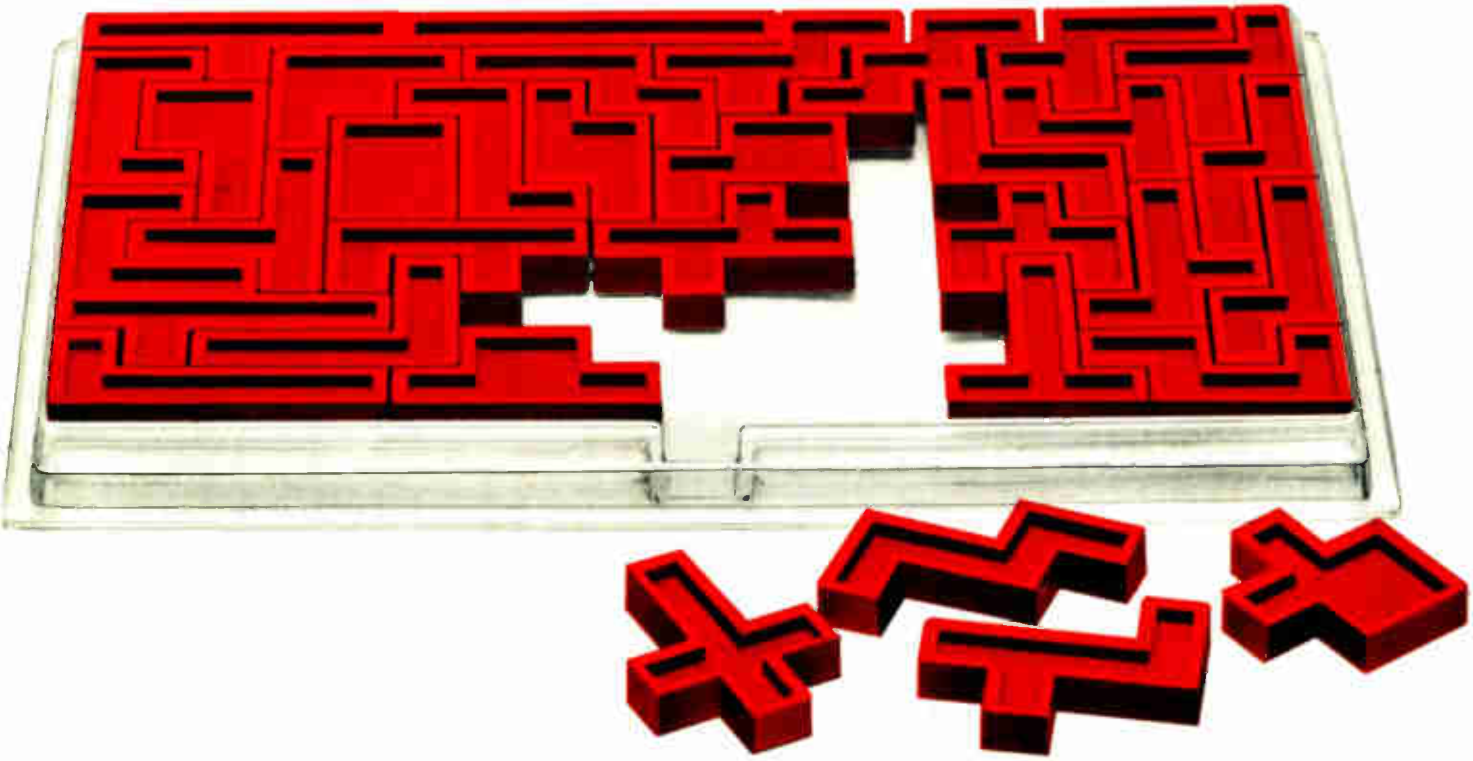


The world of temperature and resistance... Applications open up endless possibilities



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Circle 52 on reader service card

PTC THERMISTOR

Washington newsletter

FCC reorganizes Common Carrier Bureau . . .

Watch for a summer upswing in Federal Communications Commission telecommunications activity now that a number of key housekeeping chores have been completed. Most important among them are **the restructuring of the Common Carrier Bureau under its new chief, Walter R. Hinchman,** and the permanent assignment of Kelley E. Griffith to the position of bureau deputy chief. Griffith replaced Asher Ende, who resigned earlier this year when not promoted to chief.

Under the reorganization, the bureau will have five, instead of seven, divisions, plus two staff units reporting directly to Hinchman. The divisions include: Economics, to handle accounting, depreciation, economic analysis, and rate issues; Facilities, responsible for technical issues and international matters; **Tariffs, including a new interconnection branch;** Mobile Radio, to be spun off from the old Domestic Radio Facilities division, plus an unchanged Hearing and Legal unit. The two new staff groups include a special unit for coordinating division work and another to research and evaluate new projects and programs.

. . . as four commissioners act on 900-MHz docket

Despite three vacancies on its seven-man panel, **the Federal Communications Commission has quietly decided Docket 18262, and so opened up 115 megahertz of space** in the 900-MHz region for expansion of land-mobile communications [*Electronics,* May 10, 1973, p. 29]. The mid-April vote **made good on chairman Richard E. Wiley's promise to push for early action** on the docket [*Electronics,* March 21, p. 49]. FCC sources point out that it would not have helped to wait for the seating of commissioner James H. Quello, the retired Detroit broadcaster approved by the Senate without dissent on April 22, because "he is not familiar with the issues" in the complex docket.

In its allocation **the FCC set aside an initial 12.5 MHz for wireline carriers' development of high-capacity land-mobile telephone service using "cellular" techniques,** and it left another 27.5 MHz in reserve for later allocation as common carrier demand requires. There will be a general reserve of 12 MHz, and the rest goes to multi-user systems, industrial-scientific-medical systems, and private radio systems.

Speed up approval of export licenses, WEMA tells Senate

More money, more export specialists, more precise legislative language, and a computer data bank are needed by the Department of Commerce if the U.S. is to compete successfully in exporting electronics to eastern Europe and mainland China, the U.S. Senate has been told by WEMA. The trade association, representing western U.S. electronics and information technology companies, urged the Senate subcommittee on international finance to incorporate these and similar amendments in S. 3282, the bill to extend 1969's Export Administration Act till 1977.

Speaking for WEMA, Ampex president Arthur Hausman recommended seven changes in the extension, including **more department money, to speed export licensing** by adding "an adequate number of well qualified licensing officers," and a computerized data bank, to replace the present manual system. He also called for: **more precise definition of exports with "military potential," in order to facilitate export control decisions;** representation of six specific Government agencies on the technical advisory committees; wider dissemination of the reports of these committees, and greater staff support for them.

AT&T's march on Congress

Competition that its chairman decries as "selective" and "contrived" is abhorrent to the telephone company. Yet it is an issue on which American Telephone & Telegraph Co. has lost battle after battle with Federal regulators who administer the laws. So now AT&T and its affiliates are taking their case against competition to those who write the laws. "Unfortunately, the Congress is the one place where they might win," says one industry communications specialist in the capital. "They have lost before the Federal Communications Commission, and they are losing in the courts. Where else can they turn?"

Lobbying the Congress has never been a Bell System specialty, but there is increasing evidence that AT&T chairman John D. deButts means to remedy that inadequacy quickly. As he wrote the company's shareholders earlier this year: "Eventually it may fall to the Congress of the United States to decide where the public interest lies and to determine once and for all whether the goals of the Communications Act of 1934—'to make available . . . to all the people of the United States a rapid, efficient, Nationwide . . . communications service at reasonable charges'—would be better served by modes of competition or, as we believe it would, by a reaffirmation of the common carrier principle that has governed the development of telecommunications in this country thus far."

In that message last year, deButts devoted half of his text to the issue of competition. AT&T, he said, will "oppose it with all the energies we can command."

Management's priorities

Any question about deButts' determination to place the Bell System's case before the Congress was dispelled near the end of April when a Washington daily newspaper published the text of some of the chairman's remarks to a private meeting of the presidents of AT&T's operating affiliates last summer. There deButts declared "how important I believe it is that every man in this room take upon himself personally the responsibility for assuring that our case is understood by the people who may come to decide it eventually. I mean your senators and congressmen."

The chairman then went on to make clear his belief that not only had the chiefs of the Bell System companies flunked this requirement in the past but that he expected that situation to change. "I must tell you, however, that again and again I have been disappointed to discover—usually too late—that we have no more than a superficial acquaintance, if any, with legislators whose understanding turned out to be critical to us," he said. And he called it "a basic responsibility of a chief executive officer to represent his business to the people whose views have a significant bearing on its future. I consider this to be a top priority. . . ."

In its new drive to find friends in the Congress, AT&T is, of course, doing nothing more than many industries have developed into a fine art through years of practice. There is not a hint of anything illegal in lobbying when it is done correctly. And deButts made clear to his managers that he was "not talking about ITT-type influence-peddling or arm-twisting." What does concern communications-equipment manufacturers, however, is the size of the resources at AT&T's disposal. Says one equipment maker's Washington lobbyist, "I am frankly afraid. With the size of their staff—all those economists, engineers, and lawyers—they can kill us. It will be like racing a kiddy car against a Rolls."

Should Bell lobby?

Only time can tell how successful deButts' turn to lobbying the Congress will be. But some of his competitors believe the AT&T chairman's concern about competition is overdrawn. As MCI Communications Corp. chairman William McGowan sees it, "Competition from MCI and other specialized carriers impacts only one small area of AT&T's total service offerings—a market served by AT&T Long Lines, and one that currently comprises only $1 billion of the Bell System's total annual revenue of over $25 billion. As a consequence, the effect on the local telephone companies and their exchanges' customers should be negligible. Competition may, in fact, even have a beneficial effect on the local companies' revenues, since MCI pays for all interconnection facilities leased from them."

However correct the MCI argument may ultimately prove to be, it is unlikely to produce any split in the ranks of the Bell System management. Today, Ma Bell is going forward in a determined drive to get the Congress to take another look at—and perhaps rewrite—the Communications Act of 1934. Nevertheless, that action raises a related issue that the Congress may want to address first: is congressional lobbying a legitimate endeavor for a company that claims the title of "a natural monopoly," one that is subject to Government regulation?

—Ray Connolly

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There's no compromise in the Centralab line of standard monolithic ceramic capacitors. It now includes chip, axial and radial lead types. They are available in 288 standard values — that's twice the number previously offered. And 244 values are directly cross referenced to major competitive units, making them not only an excellent first choice but an ideal second source.

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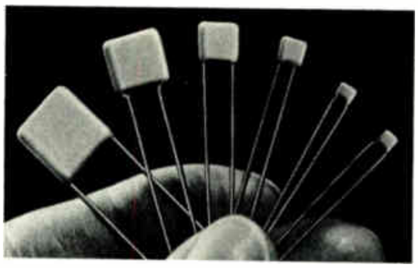
Tubular axial lead types are available in 84 values for 100 VDCW, rated 1 pf to .1 mf with COG (NPO) and X7R temperature characteristics and tolerances of ±0.5 pf or ±10%.



The radial lead, epoxy coated Mono-Kap™ is offered in general purpose, temperature stable and ultra stable types. You can select from 50 or 100 VDCW with COG (NPO), X7R, and Y5V characteristics. Tolerances include ±0.5 pf, ±10%, ±20% or +100 −0% (GMV).

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In addition to stocks of monolithic ceramic capacitors at Centralab Distributors, this 20,000 square foot warehousing facility in Milwaukee maintains an extensive back-up inventory exclusively for distributor orders.

Circle 55 on reader service card

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Piezoelectric polymers aimed at audio transducer jobs

Quality audio speakers that are as thin as picture frames are among the goals of researchers at Japan's Pioneer Electronic Corp., which this year will introduce transducers utilizing piezoelectric high-molecular materials. Pioneer plans to introduce headphones, a tweeter, a phonograph cartridge, and a microphone containing the polymer transducers, while research continues on adapting the piezoelectric material to low-frequency speakers.

Takeo Yamamoto, managing director and general manager of Pioneer's Acoustical Engineering Research Laboratory, says the piezoelectric devices that will be introduced over the next year will include the first ever used as an output transducer in commercial audio equipment. He adds that, once engineers are able to reduce voltage requirements for the polymer in low-frequency equipment, they can make speakers that take up little more room than a wall painting.

Film. The polymer developed by Pioneer is made of polyvinylidene fluoride in film form that ranges from 8 micrometers thick for headphones to 30 μ thick for use in tweeters. Aluminum electrodes are attached to each side of the film, producing a poling effect that causes the film to behave like an ideal pulsating-sphere radiator. Polyurethane backing serves as a damper.

Yamamoto says that, in addition to the structural simplicity of transducers constructed with the new piezoelectric material, the polymer does not react to humidity conditions as do condenser and electret-type transducers. Moreover, the total actuation offered by the film gives better directional qualities. Distortion of the tweeter that will be built with the new material is rated at 0.3%. Overall, Yamamoto says, smooth, flat frequency responses up to 25,000 hertz have been recorded in tests on the piezoelectric transducers now being developed.

A 1-to-10 step-up transformer is used with the tweeter, and 4 volts is applied at the primary source. With low-frequency speakers, the necessarily large stroke requires transformers too large to be commercially feasible in audio equipment. Researchers are attempting to lower the low-frequency voltage requirements for the polymer.

Pioneer developed the polymer in cooperation with Japan's Kureha Chemical Industry Co., and Yamamoto says that because the polymer is being produced in small quantities at present, its cost is higher than that of the equipment it replaces in conventional transducers. However, Pioneer plans to use piezoelectric tweeters in both medium and high-priced speaker sets in the hope that, by using the film in such quantities, material price will drop. Piezo electric headphones will be introduced this month, the tweeters and microphones toward year-end, and the cartridge next spring. □

Around the world

Cassette recorder aimed for military

Backed by some $600,000 in development money from the French army, Schlumberger Instruments and Systems (SIS) has readied a ruggedized digital-tape cassette recorder that meets French and international military standards. The first units will go to the French army for a battlefield artillery computer system. The French navy has also ordered these recorders for the data-processing systems for a new class of ships. All told, there's an immediate 1974 market of several hundred recorders, estimates Alain Piro, who heads the company's equipment department. But, since SIS so far is the only European company to offer a ruggedized tape-cassette recorder, Piro estimates that unit sales could add up to several tens of thousands over the next decade.

Right now, the ruggedized recorder carries a price tag of $5,000 or more. However, Piro predicts that the price will edge down to about $2,000 within five years if the company lands enough orders to warrant reasonable production runs. SIS, which calls the cassette recorder the PS 6020, guarantees an accuracy within one bit per million under military operating conditions. Capacity of the cassette is 600 feet of half-inch, eight-track tape, enough to handle 30 million bits of data without gaps. The top data rate that keep accuracy within 10^{-6} bits is 20,000 bits per second, but 60,000 b/s are possible when an error rate of 10^{-4} is acceptable.

Remote video terminals control mail-sorter

Faced with the task of handling some 30 million letters every day, West Germany's Post Office is increasingly turning to electronically controlled equipment for its letter-sorting operations. The latest addition to its arsenal is its highest-capacity automatic sorting system, a computer-controlled installation that will have a throughput of 72,000 letters an hour. Built by AEG-Telefunken, it features remote video coding stations.

In the sorter, video pick-up devices scan the letters' addresses. The various gray shades are then converted into digital data, which is stored in a special memory. At the remote video coding stations, the complete address of the next letter to be routed is automatically retrieved from the memory and displayed in its original, but enlarged, form on a television screen. On a keyboard, the operator punches in the four-digit postal-area code. The main advantage of video coding stations is that such equipment can be installed at a distance from the noisy printing and letter-sorting machinery. Also, these stations make for better use of the mechanical equipment and do away with the need for intermediate letter-stacking gear. Letter-stacking is, in effect, replaced by storing addresses in the memory.

Overseas investments pushed by Japan's electronics giants

Japan's major electronics producers will invest an estimated $33 million in overseas ventures this year to help offset rising production costs at home. Nearly all the investments will be for production of consumer electronics ware, and will include establishment of sales subsidiaries. **Sony Corp. will spend approximately $20 million** to expand its color-TV manufacturing plant in San Diego, while **Matsushita has earmarked an estimated $60 million for overseas investments,** including its purchase of Motorola's Consumer Products division.

TV data service comes closer with British agreement

British television-set makers and the two broadcasting authorities—British Broadcasting Corp. and Independent Broadcasting Authority—have agreed to a technical format for alphanumeric data service. Both broadcasting authorities have been working independently on such a viewer service for some time. **Four lines per frame will be used for carrying the data in digital form—lines 17, 18, 330, and 331, all off the screen and at present unused.** The data will be coded in non-return-to-zero binary form and transmitted at a bit rate fractionally under 7 megabits a second. That rate is a lot faster than the experimental systems, but it means that one TV line can carry all the data needed for housekeeping and a complete row of 40 Ascii-coded alphanumeric characters. Using a maximum of 24 rows of characters per page of data on the screen, 99 pages can be cycled through in about 25 seconds. Therefore, if a viewer selects for freezing a page that has just gone, he doesn't have to wait too long for it to come around again. **For the IBA—a commercial organization—it also means more space for advertising.**

Though BBC and IBA still have to decide that an operational service is worthwhile, and the government has to authorize it, it's more likely than not that a service will start—because it can be done inexpensively. Ultimately, reception equipment in TV sets is likely to be a half-dozen LSI circuits costing no more than $100 or so. The most expensive equipment item at the transmission end is the small computer that digitizes the data and inserts it in the video signal. **So far, BBC has started experimental transmissions on the new format, and IBA hopes to start in the fall.** TV-set component makers Texas Instruments Ltd. and Mullard Ltd., as well as major set-maker Rank Radio International Ltd., are building test demodulators, which are part linear, part digital.

Color TV still paces Germany's consumer-gear sales

By all appearances, 1974 is shaping up like another banner year for West Germany's entertainment-electronics industry. After a successful first quarter for color-TV sets, the industry **expects above-average sales to keep up, with the prime stimulant coming from the world soccer championship games in Germany this summer.** Following that event, demand will slacken somewhat but should still rise at a 15% nominal growth rate until the end of this year. That rate should put the country's total market for entertainment-electronic products—including radio receivers, tape recorders, disk players, and stereo equipment—well above the $2.8 billion level. Sales in 1973 were $2.4 billion.

Japan's computer sales led by minicomputers

Japanese computer sales climbed a healthy 18% in fiscal 1973, thanks mainly to a boom in minicomputers, sales of which skyrocketed 50% to 60%, to total 60% of the 10,531 computers now in use. Growing capacity and refinements in ICs that permit manufacture of easy-to-handle computers at small costs are cited as major reasons for growing popularity of minicomputers. The sales boom is typified by Nippon Electric Co.'s NEAC System 100. Sales of the system have passed the 500-units mark, even though it was only put on the market in the middle of the year. Other big minicomputer sales gains were reported by Takachiho Burroughs Co., a 50-50 joint venture, and by Mitsubishi Electric Corp. **Takachiho Burroughs sales of small computers have topped 8,000 units since their introduction six years ago.**

AEG-Telefunken goes East to up output

To avoid production bottlenecks at home, West Germany's AEG-Telefunken is quietly expanding its semiconductor operations in the Far East. The firm's latest move in that area is the foundation of a Philippine semiconductor company in which Manila-based Stanford Micro-Systems Inc. is an equal partner. **The new company, Telefunken Semiconductors Philippinas Inc., will begin device assembly around the middle of this year, with machinery and know-how to be supplied from West Germany.** Using parts from AEG-Telefunken's Heilbronn facilities, TSP will put together low- and high-frequency silicon transistors, as well as bipolar and MOS integrated circuits for reexport to West Germany or for shipment to other markets. One of the prime reasons for the move, AEG-Telefunken officials say, is **to take some of the load off their domestic facilities, where production capacity is severely strained by high market demand.** The company's semiconductor sales increased by more than 50% annually during the last two years.

Ericsson chalks up more orders for computer-run exchanges

L M Ericsson has strengthened its position as supplier of computer-controlled telephone exchanges by **racking up $20 million worth of contracts recently.** The orders include new exchanges for Rotterdam, Aarhus in Denmark, and Guadalajara, Mexico, as well as extensions of earlier contracted exchanges in Aabo, Finland and Monterrey, Mexico. The new orders **bring to 29 the number of computer-controlled trunk exchanges that Ericsson has in use or on order in nine countries.** The exchanges, designed for national, international, and intercontinental traffic, use multiprocessors. The total capacity of Ericsson exchanges in use and on order is 220,000 trunk lines, which is equal to 1.3 million subscriber lines.

Addenda

The pocket TV set with 2-inch-diagonal screen that Sinclair Radionics Ltd. has said it will announce this summer won't appear before next year at the earliest. Managing director Clive Sinclair says that he can't find a tube maker prepared to make the tube in quantity. The set is intended to have the vast majority of the circuitry integrated onto four chips. . . . **Norwegian shipboard-computer maker Noratom-Norcontrol A/S has landed one of its biggest single orders:** 10 DataBridge navigation systems for Mobil oil tankers. Most of the 21 orders received so far this year have come from Amoco, Exxon, and Mobil. The systems use computers made by A/S Norsk Data-Elektronik. . . . **In a $25 million deal, Iran** will get an electronics and optical production facility designed and equipped by Hughes Aircraft Co. The installation will be called the Electro-Optical division of Iran Electronics Industries.

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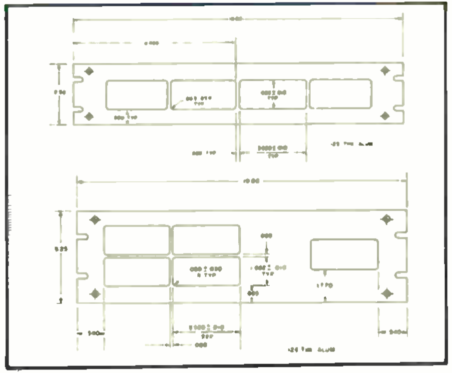

The 1230 can be mounted horizontally or in vertical "stacks." It takes up only 7 square inches of panel space, and can be mounted entirely from the front of the panel.

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The Weston 1230 DPM offers full 3½-digit, plug-in, 7-segment Sperry display; all solid-state design with reliable TTL packages and advanced CMOS circuits; automatic zeroing; maximum bias current of only 2 nA; and 80 dB Common Mode noise rejection.

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*U.S. Pat. #3,051,939

Model 1230 circuit board.

The complete circuitry is on a single sturdy PC board, and the readout board is soldered to the main board, eliminating contact problems which could arise from connectors.

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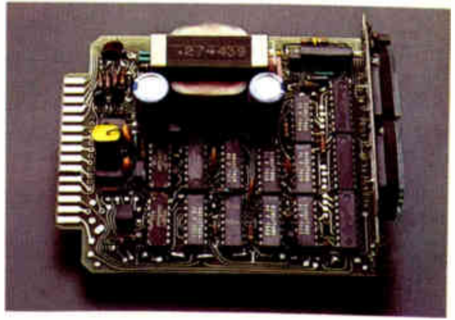

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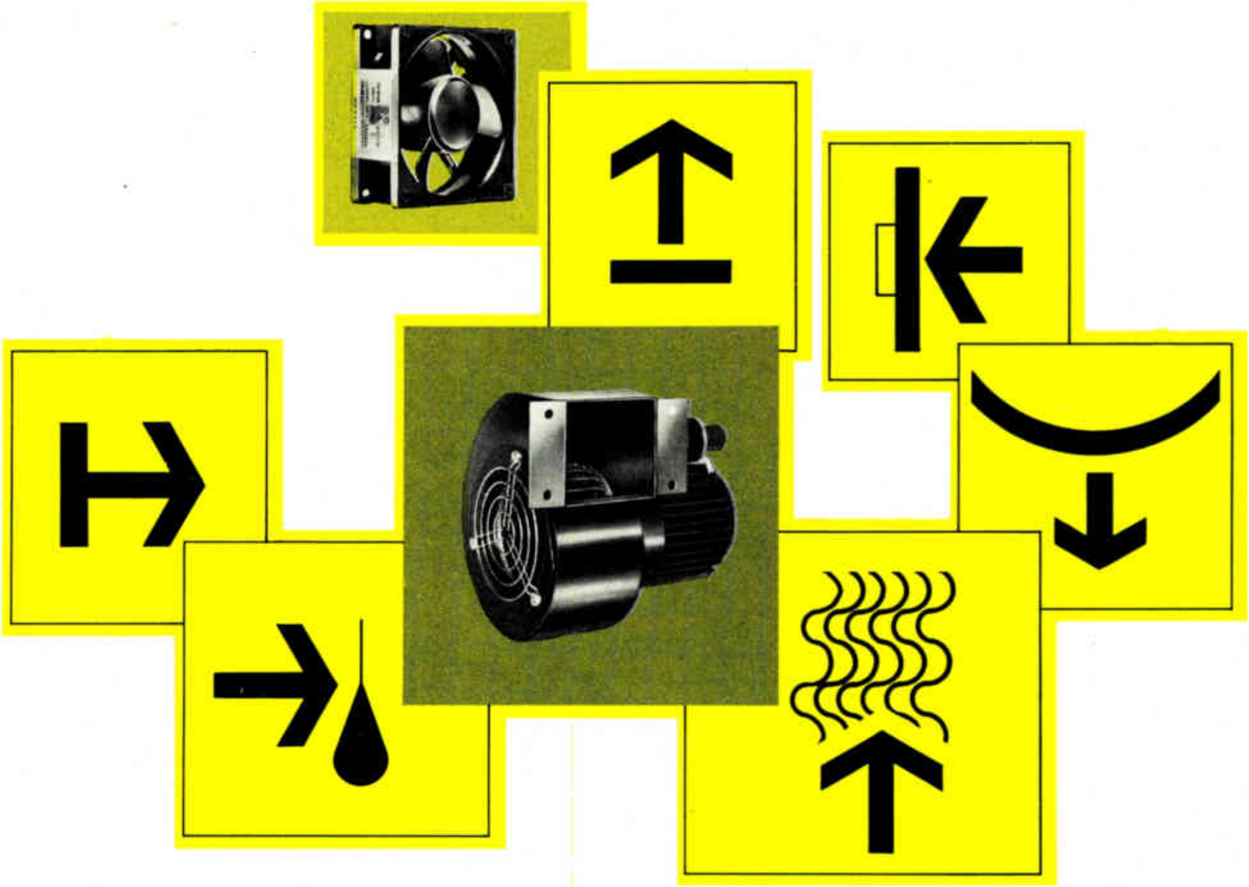

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DIVA'S COMPUTROLLER BEGAT AND...

An Episode in the True Chronicle of the DIVAS, Proudest Peripheral Family in the Computerworld.

Forever stored in the computerworld memory is that incredible marriage four years ago, immortalized by this painting, of mini processor technology to DIVA controller — a marriage that united distinguished minicomputer families with great storage capacity disc drives of the IBM 2311 and 2314 types.

Once again, the elite of the computerworld find themselves at what appears to be a joyful celebration. They had been summoned here by a mysterious masked messenger who said only that they must come to witness an astonishing event. Marvel at the great throng! DEC, Data General, TI, Interdata — all of those with whom DIVA controller has interfaced in the past are here. A driving murmur fills the hall as all speculate upon the possible reason for this grand assemblage. Bits of conversation issue from the minis.

"They say mini processor and DIVA controller are now proud parents. They say we are here to see the spin off."

"No, no," unwinds another mini. "Another marriage is my input. DIVA plans a bold coupling that will further maximize us minis. That's the way I read it."

"Saving money. A million dollars saved on the purchase of a DIVA system, as compared with a comparable IBM system. *That's* news. *That's* why we're here."

On and on minis calculate. Discs and tapes drive and search. Output increases rapidly. Information is being transferred at fantastic rates — up to 624K bytes/sec by a DIVA Disc Drive 30 system alone. The combined interchange of data reaches din-like proportions.

BUT WHAT HAS HAPPENED?

Two awful, blinding electronic flashes coupled with ear-piercing, supersonic cracks of sound reveal a shrouded figure holding up the DIVA medallion. Instantaneously all eyes focus upon this commanding sight. A shuddering gasp sweeps the hall, followed by electric silence. The newcomer steps forward and a sonorous pronouncement issues from deep behind royal purple robes.

"I am DIVA COMPUTROLLER here to tell you of my mighty workings."

COMPUTROLLER? COMPUTROLLER? All units go into search mode.

"Nor will you find me in your memories. I was not.

I am *NOW*. Born full-blown of mini processor and DIVA controller. Brought to maturity by expanded research facilities and a rapid growth curve. I was begat to interface all minis with IBM compatible 3330 type drives."

A tumultuous spontaneous exclamation of surprise and joy thunders from the throng. Mesmerized by this magnetic figure, they see he is a DIVA in every way: powerfully-built, solid-state throughout, capable of simultaneous control of up to eight disc drives in either mini or IBM formatting.

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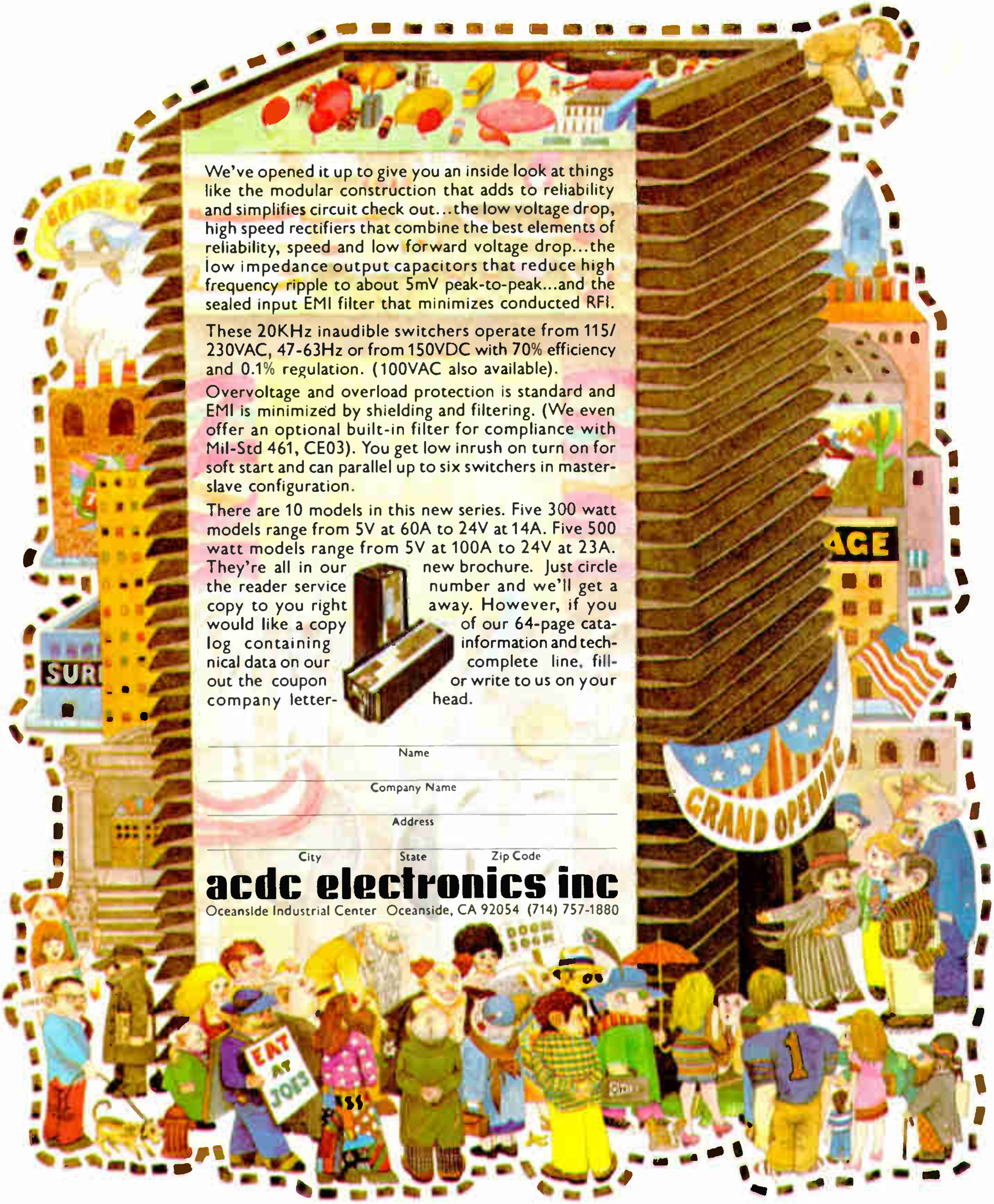


ATS-F poised to chalk up firsts

$200 million package, designed to advance satellite communications, will experiment with tracking, data relay, enlarged spectrum

by William F. Arnold, Aerospace Editor

The sixth, and last, applied technology satellite may be the most exciting one in the series. ATS-F promises to open a new dimension in satellite-communications technology when it is launched the morning of May 30.

The experimental spacecraft will carry a host of sophisticated electronic gear designed to test and extend long-distance communications techniques on an international basis for education, plane and ship tracking, and data relay between earth and other spacecraft. But it also will conduct experiments on high-frequency propagation and interference that may enlarge the communications spectrum.

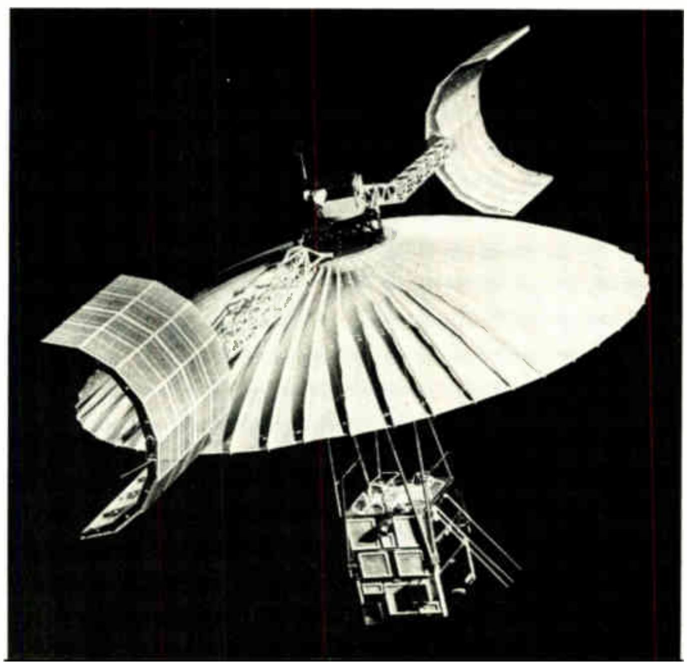
If successful, ATS-F will provide more communications uses to serve mankind and foster production of new equipment to service additional markets. The $200 million program should bear rich fruit. For example, the spacecraft may, through its high-resolution radiometer to detect cloud fronts, help increase the yield of rice for the hungry millions in India. Since rice must be planted within a precise time before the onset of the monsoon season, the radiometer will spot the buildup of monsoons in time for successful planting.

Key ATS experiments are:

- **Educational and health TV experiments.** Sponsored by the Department of Health, Education and Welfare, these tests will seek to deliver health and educational services to millions of Americans in remote regions of the Rocky Mountain states, Alaska, and Appalachia. Voice, color-video, and data signals will be used. Each of ATS's two high-powered transmitters operating in the 2,500-megahertz range will bounce a beam off the parabolic reflector to produce a pair of almost tangentical beams covering 1,000 by 300 miles. The TV programs can be simultaneously broadcast in four languages, tied in with local microwave or cable systems, and be sent to individual receiving stations. A 10-foot fiberglass receiver antenna will operate from -50°C to +70°C and cost about $5,000 each, says Albert A. Whalen, the health education telecommunications coordinator at NASA, Goddard.
- **Position-location and aircraft-communications experiment.** Involving both the Federal Aviation and the Maritime Administrations, this C-band test will seek ways of more economic and efficient routing by providing continuous communications and navigation information between ships, planes, and ground stations.
- **Tracking and data-relay experiment.** To prove the capability of transferring data from an out-of-sight satellite through another one to the ground, this experiment will use ATS to relay weather data from NASA's Nimbus F to ground receivers when the weather bird is out of sight of earth stations.
- **Radio-frequency-interference experiments.** These experiments will enable experts to measure the mutual interference between satellite and earth communications systems, the results of which should affect the design of future systems.
- **Millimeter-wave-propagation and radio-beacon experiments.** Also important for future communications design, these tests will be used to define the way millimeter waves are propagated from space to earth, help determine how radio waves in specific bandwidths are affected by rain and other climatic conditions, and investigate the effect of ionospheric particles on radio propagation and the affects of atmosphere layers on radio-wave reflection.

After the experiments on the far side of the world, the spacecraft will be brought back so that it can transmit across the U.S. However, since the specified performance life is two years, but the design goal is at least

Teahouse. That's what the fully deployed ATS-F suggests, with its 48 radial ribs and antenna. The satellite will weigh 3,080 lbs.



five years, ATS isn't booked up for the rest of its time. The remaining five to six years are as yet unplanned.

Teahouse transmitter. Weighing 3,080 pounds at launch, ATS, about the size of an Intelsat-4 satellite, will be launched into a synchronous orbit to conduct experiments over the U.S. From its geostationary perch 22,300 miles high, the spacecraft will resemble a teahouse delicately supported by a giant parasol suspended from two booms. The teahouse, called the earth-viewing module, contains the "antenna-feed farm" on top, the communications module, the service module for altitude, command and telemetry control, and the experiment module housing earth-viewing experiments within a package that's 4.5 by 4.5 by 5 feet.

The parasol is a huge 30-foot parabolic reflecting antenna made of 48 flexible radial ribs covered by a dacron mesh. The large antenna is primary to the spacecraft's tremendous potential because it provides a vast area to reflect beams. But, unfurling the antenna from its doughnut-shaped ring hours after launch will be a tricky and key part of the complicated process to get the bird on station and in operation. At the end of the booms are curved paddles containing 21,600 solar cells that will provide 470 W of power at the end of their life. The booms and paddles are 54.8 feet across.

As prime contractor, Fairchild used several electronic subcontractors. Philco-Ford Corp.'s Western Development Laboratories built the communications subsystem which will operate over a range of 17 uhf, vhf, L-band, S-band, and C-band frequencies ranging from 136 MHz to 6 gigahertz. Lockheed Missiles and Space Co. fabricated the 180-pound reflector, which has a contour precise enough to handle a top frequency of 10 GHz. IBM's Federal Systems division built the orbital-attitude and receive- and decode-command equipment. Honeywell's Aerospace division made the attitude-control system, the first all-digital spacecraft-control system.

Firsts. Fairchild and NASA officials boast of many unique features aboard the craft. William A. Johnston Jr., Fairchild program manager, claims that, for the first time, ATS will use a graphite composite structure for the support cage, deploy its 30-foot reflecting antenna, use a completely digital computer in the altitude-control system, use a new system of heat pipes to lower and dissipate the heat profile, use solid-state transmitters to achieve the highest power yet in space—more than 100 watts of rf power in some experiments. And the effective radiated power, the intensity of the beam received on earth, will be 200,000 W. □

ATS-F sails along

From a turbulent history, the ATS-F has sailed into a clear course lately. In fact, it is passing all its preflight tests with such high grades that the sophisticated spacecraft should have a very successful career in orbit, surmises Richard B. Marsten, communications program director in NASA's office of applications. "I've never seen a spacecraft program go so well," he says, adding that he had been involved with about 70 satellites when he was with RCA.

It wasn't always so. ATS was born in controversy when NASA first awarded the contract for the program to the General Electric Co. in April 1970. Fairchild protested and was upheld by the General Accounting Office and two NASA committees. The agency then reversed itself and gave the spacecraft job to Fairchild in September 1970.

Delays in getting the mission defined and lagging subsystem contractors threw the program into funding and timetable problems [*Electronics*, Feb. 14, 1972, p. 49]. Consequently, the follow-on ATS-G was scratched, and F's 1973 launch was postponed a year. Fairchild bore down and encountered only a six-week delay in launch because NASA wanted to check out some "suspect" transistors in the power supply.

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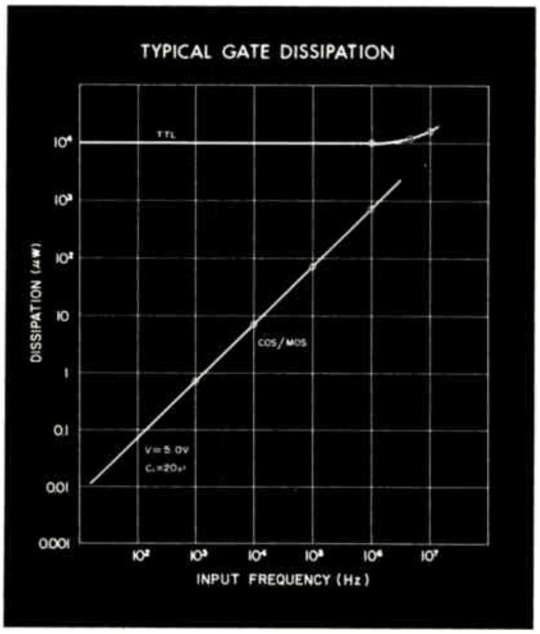

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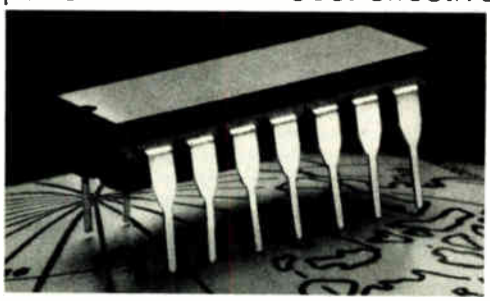

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Pacing the paperless parade

National Data Corp. is developing computer/communications systems that have led the march toward the all-electronic transfer of funds

by Gerald M. Walker, Consumer Editor

Electronic funds-transfer systems—the basis of a "cashless society"—are gaining momentum in retailing, banking, and other consumer transactions. Riding the crest of the wave is seven-year-old National Data Corp., which is in a position to be a data middleman for a widening range of users in need of nationwide authorization and billing networks.

But back in 1967, this concept didn't seem too promising, particularly since National Data had nothing tangible to offer—no hardware manufacturing of its own, no experience in credit authorization, and no proof that a real-time net was necessary.

Founded by eight retired Air Force officers and a couple of civilians under the leadership of a former Strategic Air Command intelligence deputy, what National Data did offer was computer/communications know-how. Most of it was gained in the Air Force well in advance of developments for commercial firms.

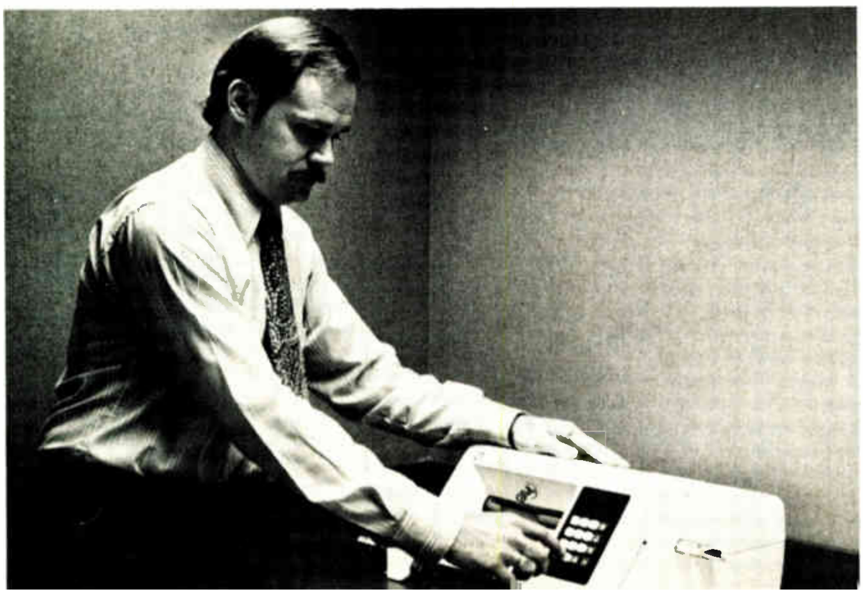
The man in command, George W. Thorpe, the retired colonel from SAC, got the company off the ground by using the now-familiar strategy of applying defense-industry techniques to civilian endeavors. National Data's first two targets were the credit-card system of the petroleum industry, which is the granddaddy of card issuers, and the trucking industry's freight records. The petroleum venture flew, but the trucking program didn't.

Today, National Data has several systems up and running; all are clustered around some form of electronic funds-transfer. For one, it announced early this year that it would begin installing 25,000 point-of-sale terminals in a nationwide credit authorization system over the next three years. Its hardware arsenal consists of a large-scale Burroughs B6700 computer, Univac 494 equipment plus backup, RCA communications gear, and numerous Digital Equipment Corp. minicomputers, as well as modems and cathode-ray-tube terminals numbering in the hundreds.

Credit-card authorization, which now serves 28 petroleum companies in the U. S. and Canada, last year accounted for more than 29 million transactions. Banks offering both big credit-card plans, Interbank/Master Charge and National BankAmericard, have hooked into the system. So have airline credit-card issuers and one of the travel and entertainment-card plans. In all, approximately $80 million in credit purchases may be in process at any given time inside National Data's Atlanta headquarters.

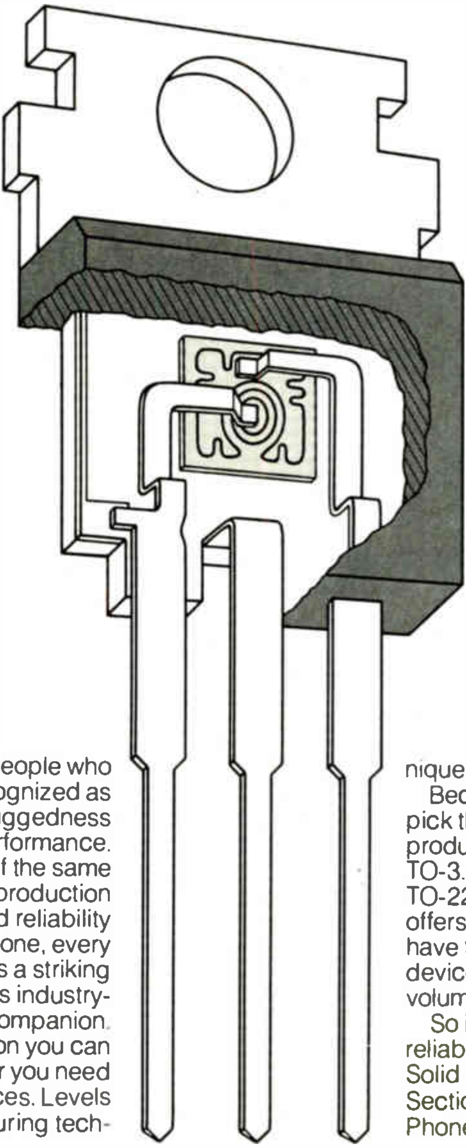
Another fast-growing portion of National Data's business is a bank-deposit-reporting system that was started in 1970 and now numbers some 350 subscribers linked to about 75 banks. This service involves the concentration of funds collected by users into banks via a deposit-transmission-information link from National Data's central computer. The company does not actually handle any of the $1 billion to $1.5 billion a day transferred by the users; it concentrates these funds so that companies have virtually on-line use of their cash, rather than having to wait for incoming payments to be sifted through the paper-clogged banking apparatus. Receipts at all user locations are reported to the National Data EDP center, then retransmitted to the banks.

Influence. Although National Data has not built its own hardware, the company has developed enough clout to influence the design of the terminals now on order. Addressograph-Multigraph Corp. has included alterations that were suggested by National Data equipment to its AmCat-I terminals, and Na-



Credit influence. Senior vice president Joseph A. Mattes demonstrates one of the Addressograph-Multigraph credit-authorization terminals ordered by National Data and altered to NDC's own specifications.

Seven ways to tell a Darlington that's great from a Darlington that's merely good.



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Circle 73 on reader service card

tional Cash Register Co. has built a credit-authorization terminal to National Data specifications.

The reason for this cooperation is that National Data considers itself a marketing company for other people's hardware. And, of course, credit-authorization terminals at the point of sale now represent a big market. Thorpe estimates that there's a potential need for 700,000 terminals in the continental U.S. and Canada, but only 700 are actually in place.

In addition, the company is a big user of the mails (the Atlanta office has its own zip-code number) and more importantly, the telephone. The possibility of more than 750,000 of its own terminals hanging out at the ends of Bell's telephone lines has caused National Data considerable concern. So, along with the design work the firm has done on the authorization terminal, it has been forced to concentrate on remote test and maintenance of the terminals around the country.

National Data recently built its own computer-based terminal-diagnosis system. The program, run off a minicomputer, not only checks out point-of-sale terminals in the field, but in effect, it peers over Bell's shoulder to ensure proper data transmission. •

Finding the trouble. The first stage of the plan monitors the frequency portion of transmission from the terminals. It analyzes distortion and indicates the source—the terminal or the transmission system. The reason for this approach, says Joseph A. Mattes, senior vice president for planning and development, is to anticipate a communications failure before the user detects it and to know immediately if any repairs are necessary.

"We want to be able to have our maintenance man arrive at the user's place of business and tell him there's something wrong with the terminal, rather than have him crying for help after a breakdown," Mattes explains. As the number of terminals on line grows, it will be necessary to sweep the entire network, then troubleshoot on an exception basis, he adds. □

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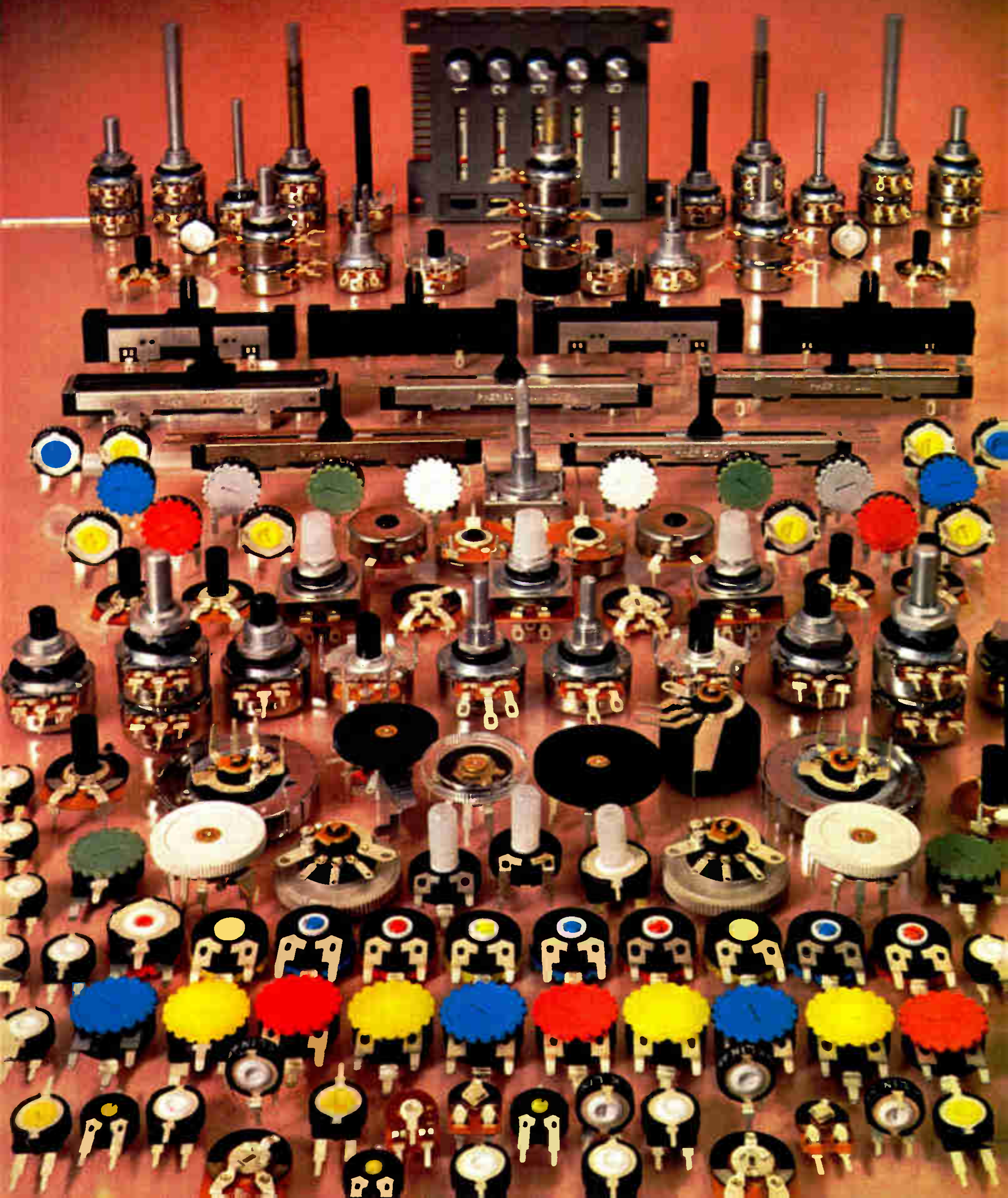


Packaging & Production

Printed-circuit makers take additive route

Plating copper on, rather than etching it away, cuts costs in latest breed of double-sided plated-through boards

by Stephen E. Grossman, Packaging & Production Editor

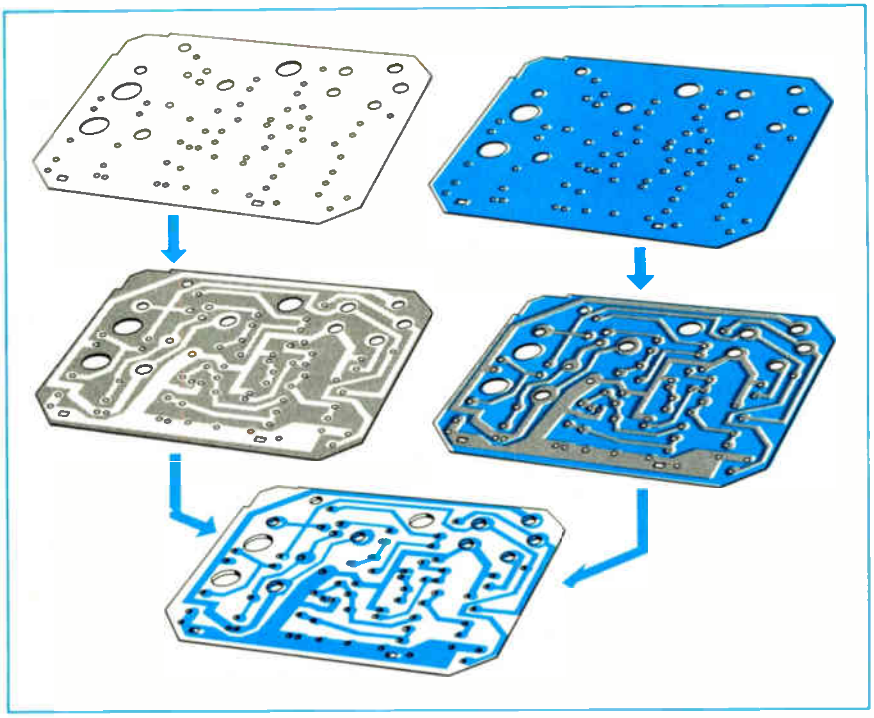
The additive approach to making printed-circuit boards is gaining a firm foothold, thanks to mounting automotive and consumer market demands for high-volume, low-cost boards—and heightened competition between the process's promotors. Already boards made by the additive process account for about 8% of worldwide pc-board production, and that share may climb to 25% by 1975.

Making boards the additive way means building up copper where it's required, instead of taking it away where it's not wanted—as in traditional, selective-etch processing. In the highly cost-conscious pc-board field, the innovation represented by the additive approach holds out the promise of shaving precious pennies from manufacturing costs.

Indeed, in double-sided, plated-through boards, the additive approach can save pc-board makers anywhere from 15% to 25%. What's more, additive boards can deliver copper-to-laminate peel strengths as good as, and solderability probably better than, subtractive boards.

Start up. In the early 1950s, printed-circuit pioneers had no

Two routes. Additive-pc-board making (left) starts with uncoated board. Masking protects areas where copper is not wanted, instead of where it is wanted, as in the traditional subtractive approach (right). Both ways give same finished board.



choice between additive and subtractive processing because no one had mastered the technique of plating thick, ductile copper onto an insulated board. What they could do was to attach a sheet of copper to an insulated board with an adhesive. After masking to protect the regions where copper was wanted, the board was bathed in an etchant to remove the unneeded copper.

Ten years. A decade ago, the Photocircuits division of Kollmorgen Corp., Glen Cove, N.Y., began additive production by figuring out how to plate on an intermediate adhesive. Then, in 1971, MacDermid Inc., Waterbury, Conn., a leader in the plating of plastics, introduced its version, which differs from the Photocircuits approach by plating directly onto the board.

Today, Photocircuits and MacDermid are battling it out in the marketplace. Says A.J. Siegmund, product-marketing manager at MacDermid: "It used to be that everyone tried additive, but nobody bought it. But now the printed-circuit industry is more cost-consicous than ever, and the evidence is building that additive can save money."

Convinced of its advantages, some large companies with captive shops switched to additive in the past few years—RCA in 1971 and IBM in 1968. Now the contract shops, which produce about 30% of the industry's boards, are also turning to the additive method.

For example, Circuit-Wise Inc., North Haven, Conn., went to additive processing in 1972 for electronic-ignition boards, which now account for 100,000 of the 400,000 boards the company turns out a month. Says Jack Mettler, Circuit-Wise vice president: "Making boards by the additive method promised labor costs one-fifth that of the subtractive boards."

What's more, he says, in the past two years the company has brought the copper price down to 85 cents per mil-foot^2 from $1.35. And he expects the cost to fall to 50 cents per mil-ft^2, or about 5 cents below the present cost of copper for subtractive boards. Now that the Government has taken the price lid off copper, prices for copper-clad laminate and copper anodes—the basic ingredients of a subtractive board—are expected to jump 25%. On the other hand, electroless copper, the heart of the additive process, is a high-profit item for its suppliers, and they are expected to soak up most of any price rise.

Concludes Mettler: "I recommend that manufacturers handling 10,000 pieces or more per month try additive on 500 to 1,000 pieces. Then they can decide if they want to commit themselves to the additive process."

Competition. Photocircuits has licensed its CC-4 process to 31 companies—including Western Electric, Hitachi, IBM, and Motorola—to make additive boards. The license route with companies having large captive operations is particularly attractive to Photocircuits because there is little likelihood that they will compete with Photocircuits' own pc-production capability.

However, it has also licensed a competitor. Methode Electronics Inc., Chicago, signed up with Photocircuits in 1973 and is going on stream with a 22,500-square-foot additive plant. William J. McGinley, president of Methode, says that additive is about 30% less expensive than subtractive for two-sided plated-through circuitry. "Since yields are better with the additive process, there is a price advantage for very dense boards," he adds.

"Finer spacings of lines is possible because there's no undercutting, as there is in subtractive etching." For the pc board in its simplest form—the single-sided board—subtractive remains less costly than additive, he points out.

MacDermid introduced the Plaid II version of its additive printed-circuit technology in May 1972 and has attracted Circuit-Wise and Litton Advanced Circuitry division in Springfield, Mo., among others. "While there's always going to be more room for subtractive two-sided plated boards," says Neal Hales, marketing vice president at Litton, "we look for additive to be big in automotive and consumer-electronic applications." Hales estimates that additive-board volume will reach $6 or $8 million in 1975. □

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Computers

HIS completes its consolidation

New Series 60 fully integrates at last the former Honeywell and GE machines into a single multilevel line with semiconductor memories

by Wallace B. Riley, Computers Editor

Three and a half years after buying out General Electric's computer-manufacturing business, Honeywell Information Systems Inc. has introduced a new line. Called the Series 60, it ranges all the way from minicomputers to supercomputers and represents the final step in consolidating the GE and Honeywell product lines.

Technologically, the Series 60 has some innovations that are new to Honeywell, but not to the industry:

- All levels of the series use semiconductor memory. Honeywell has used semiconductor memory before, but never to the extent that it has in the Series 60.
- A few of the largest models use high-speed buffer (cache) memories in front of the relatively slow main memories. IBM introduced the cache concept in its big machines five or six years ago and has used it repeatedly since then, but, until now, no other computer manufacturer has followed suit.
- A high-speed non-impact printer that can produce 18,000 lines per minute of hard copy was announced at the same time as the Series 60. The printer can be used as a Series 60 peripheral, but because it is an off-line device it is essentially a separate development.

Series 60 will appear on five levels, called the 61, 62, 64, 66, and 68, in order of increasing size. Each model is optimized for a particular class of user, but offers a modular growth path so that users can graduate easily to larger systems as their needs increase. In general, several models are available at each level. The basic models are compatible with each other, but the successive levels are not cross-compatible, although all can be upgraded to higher levels.

Semiconductor main memory in the new machines is built with 1,024- and 2,048-bit MOS packages in all models at every level. Capacities range from 64,000 to 8 million bytes in various models. Before the Series 60, Honeywell had used MOS only in its top models of the 6000 series.

Cache memory. The MOS main memory has an access time of 750 nanoseconds, while the much smaller cache, made of bipolar circuits, can produce data in less than 200 ns. Whenever the processor calls for a word from the main memory, the system transfers a much larger block of data into the cache, including the requested word. This ensures that data needed by the processor is nearly always in the cache, and thereby makes the machine run as if its entire memory were producing data at the rate only the cache can achieve.

Virtual memory is available in the larger models. The smaller versions have something Honeywell calls integrated data store, which is a method of data-base management—

A new standard for the data quantum?

Despite the industry standard of 8-bit bytes plus parity, the largest models in the Honeywell Series 60 are built with 9-bit bytes plus parity. This choice is based on the computer's 36-bit word, a legacy of the 6000 and GE 600 series, dating back to the early 1960s. Honeywell's large computers have always kept this word length because it permits superior single-precision floating-point arithmetic. Too much accuracy is lost with a 32-bit word, the IBM standard, and when accuracy is restored with double-precision computation, the speed decreases sharply. For data communications and character-oriented processing, the 36-bit word can be easily divided into 9-bit segments, but not into 8-bit segments.

The extra bit also allows instant conversion between today's two "standard" data codes, ANSI'S ASCII and IBM'S EBCDIC. Needless to say, the two codes are incompatible. A ninth bit in a byte could be useful as a flag to indicate which code is represented by the other 8 bits, thus permitting the two codes to be mixed in a single system.

Unstated—officially, at any rate—is the rumor circulating through the computer industry that the 9-bit byte may be adopted by IBM in its next major computer announcement, expected in 1975. This change would enable IBM computers to use ASCII when communicating with outside networks, while retaining EBCDIC internally. It would improve the accuracy of single-precision floating-point arithmetic. And it would upstage those competitors who try to be IBM-compatible but aren't geared up to switch quickly to a 9-bit byte.

Thus, by going to 9 bits in its new large computers, Honeywell seems to have jumped well ahead of the rest of the industry.

sort of a poor man's virtual memory.

All the logic in the new machines is TTL, most of it off-the-shelf standard products in medium-scale integrated circuits. A few custom parts, including some using Schottky TTL, are used, especially in the larger models. "We found TTL available in larger volume and therefore more cost-effective than ECL," says Ugo O. Gagliardi, director of the HIS technical office.

Firmware control is used at all levels, both in mainframes and in peripheral controllers. Honeywell has used firmware (microprograms) in a few of its older machines, but never across the board. Basic firmware is in fast read-only memories in all models and in the input/output controls; in the smaller machines, other microroutines that are not time-dependent or critical in over-all performance are in a read/write control memory made with the same technology as the main memory.

A new line of peripheral equipment is also being produced for use with the Series 60. This includes three new disk-storage units, two families of magnetic-tape drives and controllers, and two new belt printers that run at 1,200 and 1,600 lines per minute, as well as the high-speed page printer. Many of the peripheral controllers, especially in the smaller models, are integrated with the mainframe, eliminating the need for a raised floor in the room where the computer is installed.

James A. Synk, director of advanced-marketing planning, says, "Our data on user trends shows that most new applications for computers of all sizes are being programed in high-level languages. Therefore, in the Series 60, we are emphasizing high-level language capability at all levels"—including a new version of Cobol recently issued formally as a standard by the American National Standards Institute, a new ANSI Fortran, now being developed but not yet formalized, and a report-program generator (RPG) derived from the version supported by IBM for its small System/3 computer. Because ANSI has not begun to consider a formal standard for RPG, the IBM version offers the most convenient *de facto* standard. All software for the Series 60 will be separately priced.

Levels listed. Level 61, which includes the models 61/58 and 61/60, is being sold only in Europe. It represents an evolution of the Honeywell 58, a product of Honeywell Bull, in France.

Level 62 consists of only the 62/60 in the United States and of two models, 62/40 and 62/60, in Europe. They are intended for customers starting to use computers for the first time and for users of the smaller models of Honeywell's older 200 and 2000 series in the U.S. or of the G-10, a product of Honeywell Italia, in Europe, who want to switch over to the new series. Compatibility with these two different lines is through simulation. The new

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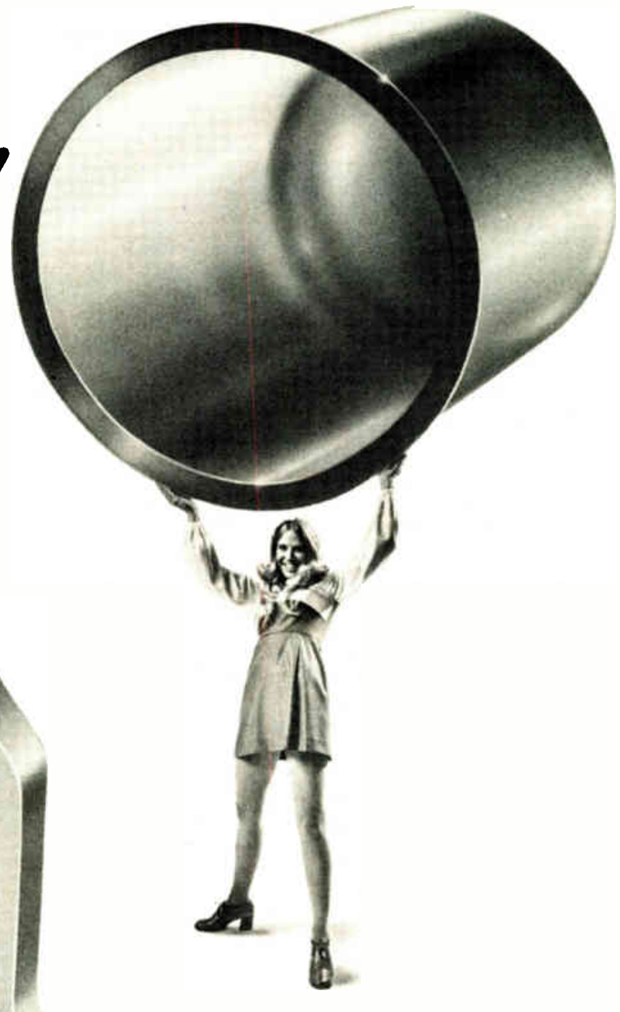

Under the dome of every Red-Lit series LED lamp is a bipolar IC current regulator that holds the LED's brightness constant through a supply voltage range as wide as 4.5 to 16 volts.

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Circle 83 on reader service card

level 64 consists entirely of one model at present, the 64/20, but compatibility is optional with the larger 2000s in the U.S. and with G-100 in Europe.

Four models constitute the level 66. They are the 66/20, 66/40, 66/60, and 66/80—all compatible with various versions of Honeywell's current 6000 series, and compatibility with the 2000 series is optional.

At the top of the new line is the level 68, which again consists of only one model, the 68/80. It is a replacement for the present Honeywell 6180, built specifically for the Multics time-sharing system. Multics was developed jointly by GE and Massachussetts Institute of Technology around a souped-up General Electric 635 computer that became known as the GE 645; the Honeywell 6180 is an improved version of the 645.

None of the older machines is being discontinued. "We find that 80% of our business comes from former customers," says Synk. "We don't want to force them to convert to the new series, so we're continuing to support the older ones to permit the user to move up in either the old line or the new."

GE plants. Although the distinction between the Honeywell and GE computer lines is now disappearing, most of the new line will be made in former GE plants. Levels 61 and 64 will be made by Honeywell-Bull in France, formerly known as GE-Bull; levels 66 and 68 will be built in Phoenix, and peripheral equipment in Oklahoma City—both former GE facilities. Level 62 will be made primarily by Honeywell Italia, which was at one time part of the Olivetti organization. Most other Honeywell plants will continue with the same equipment as before—for example, the series 16 minicomputers in Framingham, Mass., 200/2000 in Brighton, Mass., which also will build levels 62 and 64, 6000 in San Diego, Calif., and both new and old peripheral equipment in Lawrence, Mass. Framingham's 716 minicomputers are used in the non-impact printer and in the Datanet front-ends that go with the level 66 in a data-communications net. □

Microprogramability lets user tailor new minicomputer to his requirements

A new family of general-purpose minicomputers that meet custom needs is also one of the first production series to exploit the high density and low power dissipation of 4,096-bit semiconductor chips

by John Stedman, Hewlett-Packard Co., Cupertino, Calif.

□ Today's minicomputer must be flexible enough to fit readily into individual applications without bringing with it the performance tradeoffs that "general purpose" often implies. Yet, a mainframe tailored to solve a specific problem should have the ability to expand its capabilities as requirements increase.

The first two members of a family of user-microprogramable minicomputers, the Hewlett-Packard 2105A and 2108A, have been developed with these goals in mind. With user-microprogramability, the minicomputer maintains its versatility and yet adapts readily to users' custom requirements. The new machines are also among the first in full production to use 4,096-bit semiconductor memory chips in their main memories. Furthermore, many new instructions are available in the new machines, which nevertheless remain compatible with previous models.

Semiconductor memories give the new machines a number of advantages—such as high density, low power dissipation, and potential improvements in speed and reliability. Furthermore, with 4,096 bits per chip, they seem to have reached the stage of costing less than ferrite-core memories.

Nevertheless, the design was committed to semiconductor memory long before the cost decreased below the level of ferrite-core memory. The new units were breadboarded with core, but the change to semiconductor random-access memories—1,024-bit devices first—was made soon thereafter. During this period, the designers' contact with semiconductor suppliers made them confident that 4,096-bit RAMs of high reliability would become available in adequate quantity for 1974 equipment production. The design centered around these devices very early, and the risk had to be taken that costs would come into line.

Volatility is no problem

The advantages of semiconductor memory, of course, are accompanied by disadvantages. An important one is volatility, or loss of stored data in the event of a power failure. But accepting this disadvantage wasn't difficult. Power failure has always been an important hazard to computers, even those with core memories. Some core-based computers commonly go into power-fail routines upon the absence of as little as a single cycle of main line power.

Because of the semiconductor memory's special characteristics, the design of the power module of the new minis received special consideration. The design study included ways to build in immunity to low or high power-line voltage and line-frequency variations, as

Small. First of new user-microprogramable minicomputers from Hewlett-Packard, the 2105A comes with 16,384 or 32,768 16-bit words in its memory and has four input/output channels. Memory is assembled from 4,096-bit MOS chips and is among the first to use these components extensively.

Architecture for microprogramability

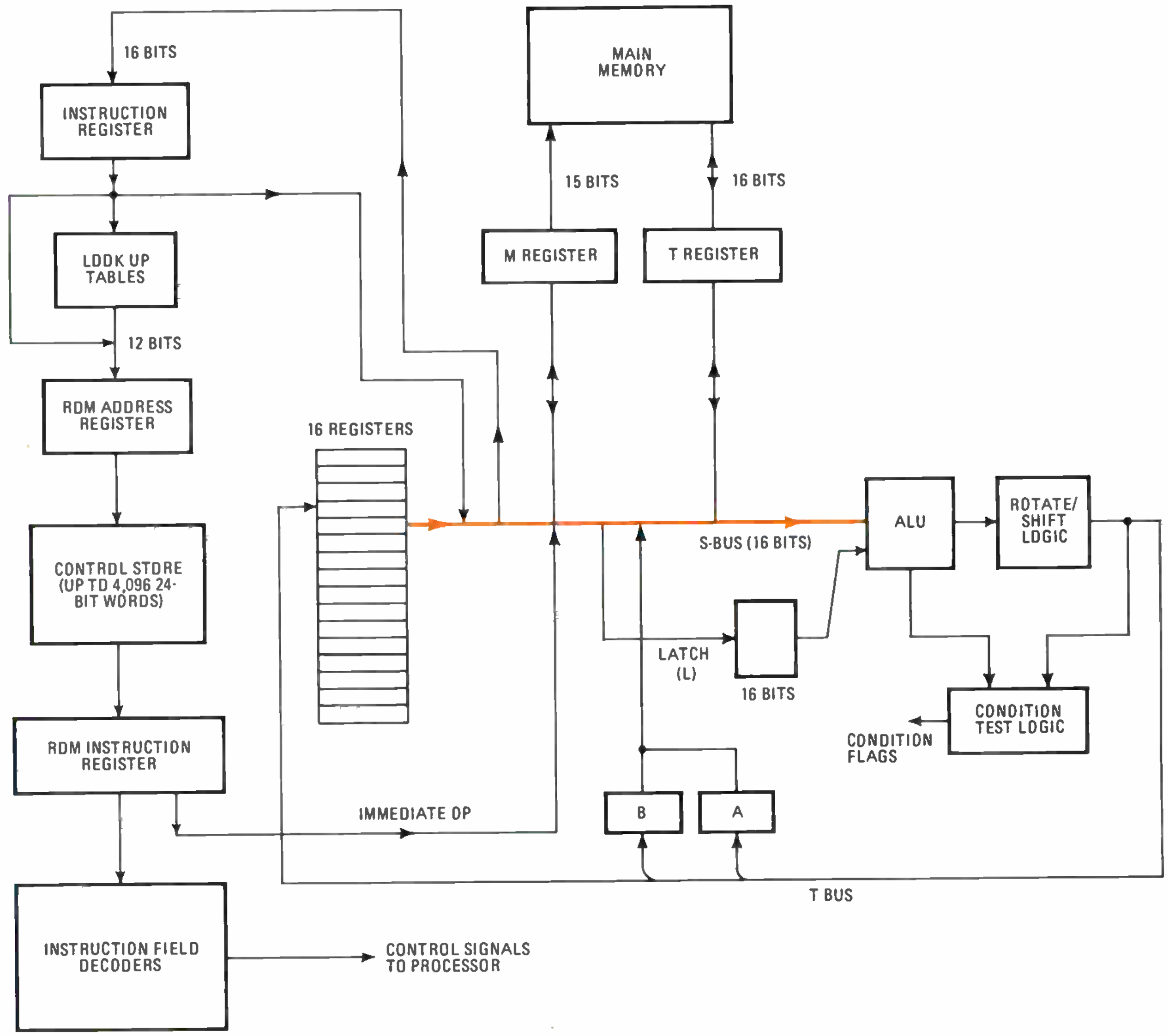
The control logic of the computer, through microprograms stored in the control memory, executes all machine-code instructions. Because of its use of microprograms, the control logic is sometimes called a microprocessor. (But note that this term is also used to refer to one-chip large-scale integrated-circuit processors, which are not used in H-P computers). Because much of the hardware of the control logic is used commonly by many instructions and is available for future instruction-set enhancements, much less hardware is required than where some is dedicated to each individual instruction.

In the H-P 2105A and 2108A, the primary bus is the S-bus, a three-state transistor-transistor logic bus that interconnects most of the machine's registers and the arithmetic-logic unit (ALU). The ALU implements functions such as ADD, SUBTRACT, COMPLEMENT, AND, inclusive-OR, exclusive-OR, INCREMENT, and DECREMENT. It is made from commercially available medium-scale-integration products. Its input comes from the latch register, a 16-bit register loaded from the S-bus. The latch register holds one operand for the ALU, while the other operand is supplied directly via the S-bus.

The 16-word register stack is put together from fast 64-bit read-write memory ICs. This "memory" contains twelve 16-bit scratch registers, two index registers, the program counter, and the switch register.

When an instruction is read from the main memory under control of the microprogram, it is passed into the transfer register, onto the S-bus, and then into the instruction register. Instruction-register outputs consult several look-up tables to generate a control-memory address. This goes to the read-only-memory address register to locate the particular microcoded execution routine for that instruction.

The routine is found among 4,096 24-bit microinstructions in the control memory. Outputs of the control memory are loaded, one word at a time, into the ROM instruction register, a 24-bit register that is divided into five fields: op-code, ALU, S-bus, store, and special. A separate decoder serves each of these fields. The signals they generate, and the operations performed by the processor, depend on the coding of each field in the micro-instruction.



well as from outright power loss. Such precautions were necessary because the family was intended for use even in environments traditionally hostile to computers. The machines had to tolerate brownout conditions and unstable sources of power, such as auxiliary generators, without sacrificing performance. Providing battery standby protection for the volatile semiconductor memory was only one of many design decisions related to these special characteristics.

Perhaps the most appealing advantage of semiconductor memory is reliability. A large part of the project effort was devoted to testing memories from all suppliers, and results indicate that mean time between failures will be at least twice that of core memories. An improvement of 15 times may well be established. This improved reliability is particularly important in the larger memory capacities.

The cost of semiconductor memory already has fallen to about 10% below that of equivalent core memory. As more vendors of semiconductor memory enter the field, and as they gain more experience with the manufacturing processes involved, the price of 4,096-bit RAMs is certain to drop even further. Meanwhile, core-memory making is a well-established art, so that further large reductions in core cost seem unlikely.

Semiconductor-memory technology is not the exclusive province of any single manufacturer, and none could be ignored. From the beginning of the project, therefore, relationships were established with all U.S. manufacturers who were willing to be considered potential suppliers. Their cooperation has been most gratifying. Designs differ, of course, but the project included accommodation to all those differences at the printed-circuit-board level, and every plan included the ability to make these differences invisible to the processor. Thus, as the new minis go into production, memories from any of the suppliers can be used. Texas Instruments, Motorola, and Mostek have delivered the memories in quantity, and all will be represented in the new machines. Several others have supplied promising samples, which are now being tested.

The design of other parts of the minicomputers were also affected by the decision to use solid-state memory. For example, the interface between the memory and the processor was designed to be as flexible as possible to allow for memories from various sources. The design also allows for various memory cycle times, various refresh intervals in dynamic MOS memories, and even the absence of refresh cycles in static memories.

Microprogram is key

Microprogramed control is a basic element in the design. The control-memory capacity now is 4,096 words, of 24 bits each; approximately 250 of these words emulate the entire instruction set of earlier HP-2100 minicomputers. The remainder is available for new instructions introduced with these machines, for options, and for user-defined microprograms. The 2100 control memory had a capacity of 1,024 words, of which 256 words implemented only part of the basic instruction set, leaving the remainder to be hard-wired. The earlier unit is thus emulated by the new one, executing 2100 programs with comparable performance.

In any microprogramed processor, source-code instructions are interpreted in the instruction register as pointers to microprocessor programs that emulate the particular instruction set being executed. In the conventional approach, on the other hand, each instruction is decoded and executed with specific control logic wired into the machine. The conventional method sometimes has an advantage in speed over microprogramed control, but it requires that the hardware and the instruction set be fixed at an early stage in the design of the system. Thus it is inflexible, and adding new capabilities is often difficult and expensive.

The total user-microprogram approach used by H-P differs from other levels of microprograming that are not quite as basic as hard-wired control logic. In the first microprogramed computers, microprograms were stored in read-only memories. The whole memory or a large part of it, however, had to be replaced when a change or an improvement was to be installed. Many microprograms are still implemented this way—including the basic portions of H-P microprograms—but semiconductor read-only memories are much smaller and more amenable to change than the older arrays of capacitors or transformers.

More recently, some microprograms have been realized in memories in which changes can be written without physically replacing anything. However, these microprograms are carefully protected from access by the user through the use of a reloading mechanism that permits only the computer manufacturer to specify the control information to be loaded. On the other hand, as in the H-P machines, when the user can specify what he wants loaded into his control memory, he can completely specify what he wants his machine to do and how it does it, and thus tailor it more closely to the application than is possible with wired logic, read-only programs, or any other means of control.

No hybrid design

In the microprogramed processor, as used in the 2105A and 2108A, every source code instruction is executed via a microprogram, allowing great commonality in processor hardware. For example, most processor operations utilize the central arithmetic and logic unit. In the conventional hard-wired approach, some instructions require unique hardware. This commonality, together with the recent availability of many new types of medium-scale integrated circuits—64-bit fast read-write memories for registers and fast arithmetic-and-logic-unit packages, as examples—significantly reduce the number of components in the processor, compared with previous machines.

The basic portion of the microprogram is stored in fast read-only memories, with 60-nanosecond access time. Read-write and programable read-only memories store the custom portions of the microprogram. Microcode words are 24 bits long, permitting a microinstruction to specify more parallel machine operations than is possible with a single 16-bit word in the source program. These relatively long microinstructions can be executed in less time than source-code instructions, which also adds to to the machine's performance.

The processors in the 2105A and 2108A include a set of sixteen 16-bit registers, two of which are reserved for use as a switch register and a program counter. Two others are used as index registers, leaving 12 available to the source programer. But all 14 are available to the microprogramer, for storing temporary or intermediate results during arithmetic operations. With fewer memory references, correspondingly faster program execution is obtained, and less main memory is required to solve the problem.

Microcode packages

A user-microprogramable computer has other advantages besides instruction-set enhancements. For example, single-precision floating-point arithmetic, optional on some minicomputers and not available at all on others, is standard on both the 2105A and the 2108A, and is implemented in firmware. Other options are continually being developed, such as the Scientific Instruction Set, which executes many common subroutines in microcode instead of assembly language, taking advantage of improved cycle time and flexibility of the microprogram control logic. Speed increases of more than 28:1 are sometimes achieved in executing these routines.

This microprograming technique is accessible by the user to increase the performance of the 2105A and 2108A processors for a specific application. The basic instruction set, as in many other microprogramed machines, is stored in a standard read-only memory that comes as part of the machine. Some optional instructions are also coded in special read-only memories that are installed at the customer's request when the machine is purchased.

But the user may also put the most commonly used subroutines in his particular application programs into microcode. In microcode, these subroutines speed up the machine because the microinstructions are executed more quickly and the program spends a lot of time in these subroutines. Several options support this practice. One option, a writeable control store (WCS) plus a micro-assembler and editor/debug package, enables the user to write, edit, and test his microcode routines easily in his system at full system speed. Once the routines are tested, the user's system software can load the microcode routines into the WCS through the input/output channel at the beginning of the run. To obviate reloading the micro-routine for every run, the user can store his microcode in firmware, but he needs an optional writer for the programable read-only memory and an associated software package.

All in the family

The new design, for cost-effectiveness, is for a family of minicomputers, rather than a single "all-purpose" design. All users need some capabilities, but they differ in their need for main-memory capacity and input/output channels. The smaller of the initial machines is the 2105A. Only 5¼-inches high, it can contain within its mainframe as many as 32,768 16-bit words of main memory and four powered input/output channels. The larger 2108A, 8¾-in. high, has nine powered I/O channels and 32,768 words of memory, extendable further without loss in speed. The memory cycle times of some minicomputers lengthen by as much as 150 nanoseconds when the memory is expanded beyond the restrictions imposed by the mainframe. The extra time is imposed either by extra cycles or by hardware that, in effect, maps the extended portion of the memory onto the basic portion. The hardware includes a register that is loaded in advance with a "pointer" that shows where the mapping process is to begin. The H-P scheme uses mapping, too, but it is implemented with fast circuits that impose little or no extra delay on the system.

With a family of mainframes, the memory capacity,

Packing 300 W on two pc boards

The power supply for the new H-P minicomputers includes several features made possible by recent technological advances such as inexpensive transistors that can switch 600 volts at 8 amperes in 500 nanoseconds, 25-ampere Schottky-barrier rectifiers, photo-isolators, and various new types of ferrite cores, capacitors, and printed-circuit boards.

Electrically the power supply consists of a high-voltage, high-frequency switching preregulator, two dc-to-dc converters, and several series-pass final regulators. It has over-voltage and over-current protection for all output voltages, as well as a battery-powered standby system to protect the contents of the semiconductor memory if line power fails. The total available output power is 300 watts at eight different voltages.

Physically, this power supply assembly consists of two main eight-layer printed-circuit boards, plus three smaller boards that provide the battery standby system. This method of assembly reduces the cost of initial assembly and testing and makes field service easier than many older designs of computer power supplies.

The preregulator and the dc-to-dc converters operate at 20 kilohertz, an unusually high frequency. Because of this, all power transformers and other magnetic components are small and light enough to be mounted directly on the pc board. Likewise, all power-handling stages are highly efficient, so that heat sinks have minimal volume and all power semiconductor devices are mounted on the board, instead of on a metal chassis.

Placing the power supply's main energy-storage capacitors ahead of the preregulator and rating them at twice the rectified line voltage (for 115-volt operation) results in both smaller size for the capacitors and increased energy storage. Since the volume occupied by an aluminum electrolytic capacitor is proportional to the voltage while the energy stored is proportional to the square of the voltage, the advantages of using a relatively high voltage for energy storage are obvious. As a result, this power supply maintains its regulated output power at full load even though line power is interrupted for 2½ cycles at 60 hertz. Stored data is kept for up to 10 cycles.

The preregulator stage, controlled by feedback from the +5-volt output, maintains a nearly constant input voltage for the converter, even with ±20% variation in power line voltage. Other memory and input-output voltages are regulated by small series-pass regulators.

number of I/O channels, and selection of options can be closely matched to individual user requirements. To keep down the cost of giving the user so much flexibility, special efforts were made to modularize the design, and to use as many common assemblies as possible. All members of the family are program- and I/O-compatible, too, and although they include many new features, they are upward-compatible with all previous H-P minicomputers, thus protecting the investment users have made in more than 8,000 minicomputers belonging to the series.

The entire processor is on a single printed-circuit board, which is common to all members of the minicomputer family. The single board requires fewer connectors and between-board cables and thus accounts for part of the cost savings. This p-c board has multiple layers, which improves reliability because the internal interconnections are less subject to noise.

Many new instructions have been added as standard features to all members of the family. For example, several bit and byte manipulation instructions have been added, for use in data-communications and data-acquisition applications. These include instructions to set, test, and clear single bits in a given data word, instructions that load or store individual bytes of data, and instructions that compare two strings of bytes and determine whether a less-than, equal, or greater-than condition exists.

Two hardware index registers and 28 instructions that use them help relocate blocks of data brought in from mass storage—an increasingly useful function in disk-based systems. For more efficiency, several new data-movement instructions are included to move bytes, words, or blocks of data with a single instruction. These are helpful in manipulating data in information-management applications.

Large. Beefed-up cousin, the H-P 2108A, appears here at the top of the rack in a typical disk-based system. It has a 32k-word memory and nine I/O channels. Both machines are among the first large-scale applications of 4,096-bit MOS memories.

Protection from accidents

The family is designed for use with operating-system software, and incorporates several features to protect the integrity of the operating system from accidental modifications—as can sometimes happen when the system is time-shared. Memory protect, one of these options, has a "fence" register that effectively divides the memory space into a system area and a user area. The operating system, which must maintain control of the computer even though several users may be executing programs at different times, loads this fence register with an address corresponding to the upper bound of the control program—the part of the operating system that is always in the memory. Users' programs are kept above the fence. If one of the user's programs inadvertently tries to obtain access to any address below the fence, the operating system interrupts the attempt, taking back control from the user's program.

A similar interrupt also occurs if one of the users' programs attempts to execute an I/O instruction, since all input/output is under the operating system's control. In addition, the memory-protect option safeguards the system from some common programing errors. For example, "infinite indirects" are permitted to repeat themselves only three times before the operating system takes over control to correct the situation.

An infinite indirect is the improper use of an indirect address, by which an instruction tells the processor to perform an operation on data found, not in a location whose address is specified in the instruction, but in a location whose address is specified in another location specified in the instruction. In some computers, several levels of this indirect addressing are possible. If the instruction specified a location that contains its own address, or two locations each of which contains the other's address, the computer can oscillate indefinitely, always looking for useful data but finding only more addresses, unless external means are provided to stop it. In the 2105A and 2108A, the operating system can continue with as many levels of indirect addressing as it wants to, unhindered by the hardware, but the user is limited to three levels.

Memory protect also interrupts any operation in which a parity error is detected, and stores the memory address in a violation register, which can be read later by a diagnostic program. Without the memory-protect option, a parity error stops the computer.

Parity detection is standard on all family members, as it was on the earlier 2100 minicomputer, with a 17th bit in every word in main memory. Parity is automatically checked on every word read from memory, including data transferred via the dual-channel port controller. This feature is considered essential for reliable operation of any complete system, no matter what size, to assure program or data integrity.

Although memory protect is a standard feature on the 2100, it is not required for many applications. Therefore, it was made an option for the new minicomputers, allowing an additional cost saving to those who do not need this capability.

Several branch-on-test microprogram instructions are also available, allowing more efficient programing than if only skip-on-test instructions were available. Normally, of course, in any computer program, instructions and microinstructions are executed in sequence. Skip-on-test instructions look for a specified condition. If that condition exists, the program skips the next instruction, and goes to the third instruction in sequence, which initiates a routine that reacts to the condition.

Obviously the skipped instruction must be an unconditional branch, so that if the tested condition does not exist, the program can bypass the conditional routine. But branch-on-test instructions cause the program to go to a specified location for its next instruction if the condition exists, so that in its absence—which may be most of the time—the program can continue in its normal sequence without any unnecessary unconditional branches. In the new minicomputers, the conditions include the presence of a carry, a zero result, a particular bit, or one of several front-panel settings.

Access by the user

To take advantage of these powerful microprocessor features, a programer must have access to them from his assembly language program. This access is built into the basic instruction set—one of the key differences between these user programable minicomputers and other microprogramed computers. In addition to the 80 instructions in the basic set, 512 instructions, called "macros," are available for microprogram routines.

The use of macros is an old trick to programers in assembly or higher-level languages. In writing a long program relatively free of conditional or unconditional branches, the programer may find himself writing the same small sequence of instructions many times with only minor variations. When that happens, he can define a macro—short for macroinstruction—which gives an arbitrary name to that small sequence and specifies any variables it may include. Then, while writing his program, when he encounters a need for that sequence, he simply specifies the name of the macro. The assembly program, when it translates his program listing into machine language, replaces the name with the actual sequence of instructions.

Likewise, in the new H-P machines, a user can take advantage of macros to define new microprogram routines tailored to his own custom requirements. When he assembles his program with the standard assembler, the writable control store or the PROM writer can produce a minicomputer to match his particular needs.

Overlapped processing and I/O

Another useful feature is the dual-channel port controller, an option both on this new family of minicomputers, and on the 2100. This option, which offers direct memory access (DMA) also includes all control logic, memory address registers, and word count registers for two channels, which the program can assign to any I/O devices. When it is installed, data can be transferred directly between an I/O device and the memory, without passing through the processor, and thus without interrupting what the processor may be doing, permitting processing and I/O operations to overlap. Other machines with DMA capability require this hardware or its equivalent to be duplicated in each controller that must have direct memory access.

An important performance specification of a machine's direct-memory-access capability is the DMA latency time, defined as the maximum time from the device request to the initiation of the DMA transfer to or from the device, in the absence of any higher priority

Safety in numbers—of sources

From very early in the project to develop the new family of minicomputers, Hewlett-Packard has worked closely with all the potential producers of 4,096-bit MOS memories, including Texas Instruments, Motorola, and Mostek. It now appears that Mostek will be the first to deliver, but Hewlett-Packard can take chips from any supplier who can deliver them.

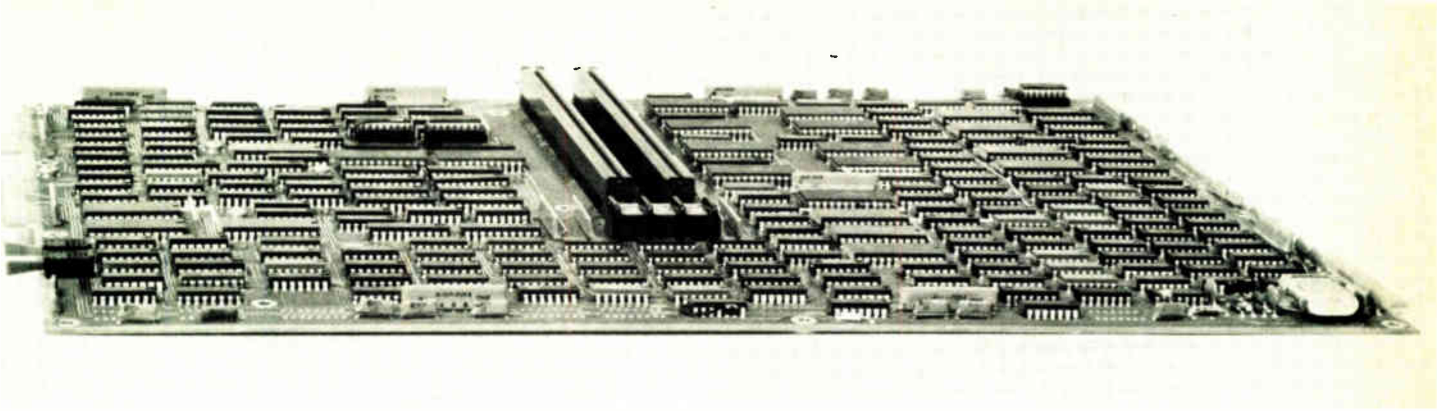
Mostek and TI use a 16-pin package for their memory chips, while American Microsystems Inc. and Motorola use 22 pins; thus the two circuits are not compatible. Anticipating these differences, H-P designed modules for each configuration, so that any of them can be used in any machine. However, they won't all look alike to the customer: more 16-pin than 22-pin packages will fit into a given space, and the computer that uses the 16-pinners will cost a little more than one with the larger packages.

Dick Conrad, standard product marketing manager for AMI, says that his company is shipping the 4,096-bit memories to H-P in sample lots only, but nobody seems to be delivering in any quantity. "Nobody's got anything wrapped up yet," says Conrad. "We have 12 major customers who want to buy our entire 1974 production—the same customers everyone else is talking to"—which means Univac, Burroughs, and Control Data, to name just a few.

Right now, Conrad says, the semiconductor people are all running pilot lines and telling each other how good things will be in the fourth quarter—but nobody has any substantial number of circuits in stock. That could cast a shadow on Hewlett-Packard's plans to begin delivering the new machines on schedule next month, but H-P spokesmen insist that the company has what it needs initially, although it can use more.

So, with plenty of customers signed up, the question now is one of delivery. Probably, no matter who delivers in bulk first, the rest will be able to pick up some business, perhaps with the same customer list.

—Walter Barney



Processor. Both new minicomputers, and all future models in the family, use identical processors on one board. Plug-in connections in the center ease assembly and trouble-shooting. Multilayer board enhances noise immunity of on-board interconnections.

operation in progress or pending. The maximum DMA latency for the new family is 1.625 microseconds, compared with 2-5 μs maximum latency time on some other minicomputers. This is another important characteristic in data-acquisition or sensor-based applications where quick response to a device's request to transfer a word of data is essential. All I/O channels have this minimum DMA latency time.

Included in the standard instruction set are other capabilities not offered in many other minicomputers. One of these is the ability to perform logical or arithmetic operations on data in memory locations. For instance, to add the number in a memory location Y to a register A, one executes the single 16-bit instruction, ADA Y. The step requires only two memory cycles—one to fetch the instruction and one to execute it—and one word of memory. Other machines without this capability might require the following:

LOAD REGISTER B with Y
ADD REGISTER A to REGISTER B

each of which requires three memory cycles and two words in memory. This feature is invaluable because less memory is used to solve the problem, specifically in applications where many logical or arithmetic operations are to be performed on large amounts of data.

"Cold loading" of programs or data—as, for example, when the memory is completely empty—is easy with the front panel arrangement and "bootstrap" feature. Up to four different 64-word loader programs can be stored in read-only-memory chips included as part of the processor. A user can very easily select, load and execute any of these programs from the front panel of the machine.

The selected program is transferred to the upper 64 words of main memory from the ROM and configured for the address of the peripheral unit containing the rest of the program. The main program is then read from that peripheral unit and may begin to be executed as soon as it is fully loaded. All of these tasks, and most other front panel operations, are controlled by special routines in the microprograms. This allows a very simple and very reliable front panel.

All the front panel switches and light-emitting-diode indicators and a small amount of logic are mounted on a single printed-circuit board. The switches are an adaption of a novel design developed for the HP-35 pocket calculator. These are strips of beryllium-copper with a dimple at each switch location. Pushing the switch causes the dimple to touch a circuit-trace beneath it. The "oil can" or "cricket" principle gives a snap action to the switch and provide definite feedback to the user that contact has been made.

Wide applicability

The last few years have seen a large increase in the use of minicomputers. With continual improvement they are now able to perform routinely tasks that only a few years ago would require large, expensive computer systems. Moreover, their rising computational power and falling price are continually opening new applications that cannot be met by microcomputers or programable calculators.

The specific uses to which predecessors of the new machines have been put may point to their first applications. The HP 2100 has been widely employed in time-shared systems for computer-aided instruction and design. In disk operating systems, it is used for batch-oriented problem-solving in scientific and other situations. More recently, with new software, many were used for dedicated, on-line terminal systems for database management and business transaction processing. The 2100 is a part of many data-acquisition, or sensor-based systems, for monitoring large amounts of measurement information in a real-time environment. Other 2100-based systems are used in Fourier analyzers, gas chromatography, electron spectroscopy, microwave spectrum analyzers, network analyzers, cardiac medicine, and nuclear medicine. The goals of the new family are to provide a more cost-effective processor for all of these uses, and to introduce new features with which designers of these systems can enhance performance.

With improvements in environmental immunity, ability to function on unstable power sources, and established long mean time between failure, applications should open in previously unserved functions. Computer control of operations on an oil-prospecting ship in rough North Sea waters is under serious consideration, for example. Small size can be important, as in a satellite navigation system now under construction. Such minicomputers are beginning to be used for control purposes on large supertankers, where resistance to the effects of vibration is an important consideration. □

Schottky diode pair makes an rf detector stable

by Roland J. Turner
AEL Communications Corp., Lansdale, Pa.

If broadband rf detection is to be efficient at low signal levels, detection thresholds must be stable—a design goal achievable with a pair of matched Schottky diodes. The diode-stabilized circuit shown here, for instance, maintains a detection stability of ±0.06 decibel over a temperature range of -20°C to +90°C for an rf drive level that is a 10th of that of a conventional detector.

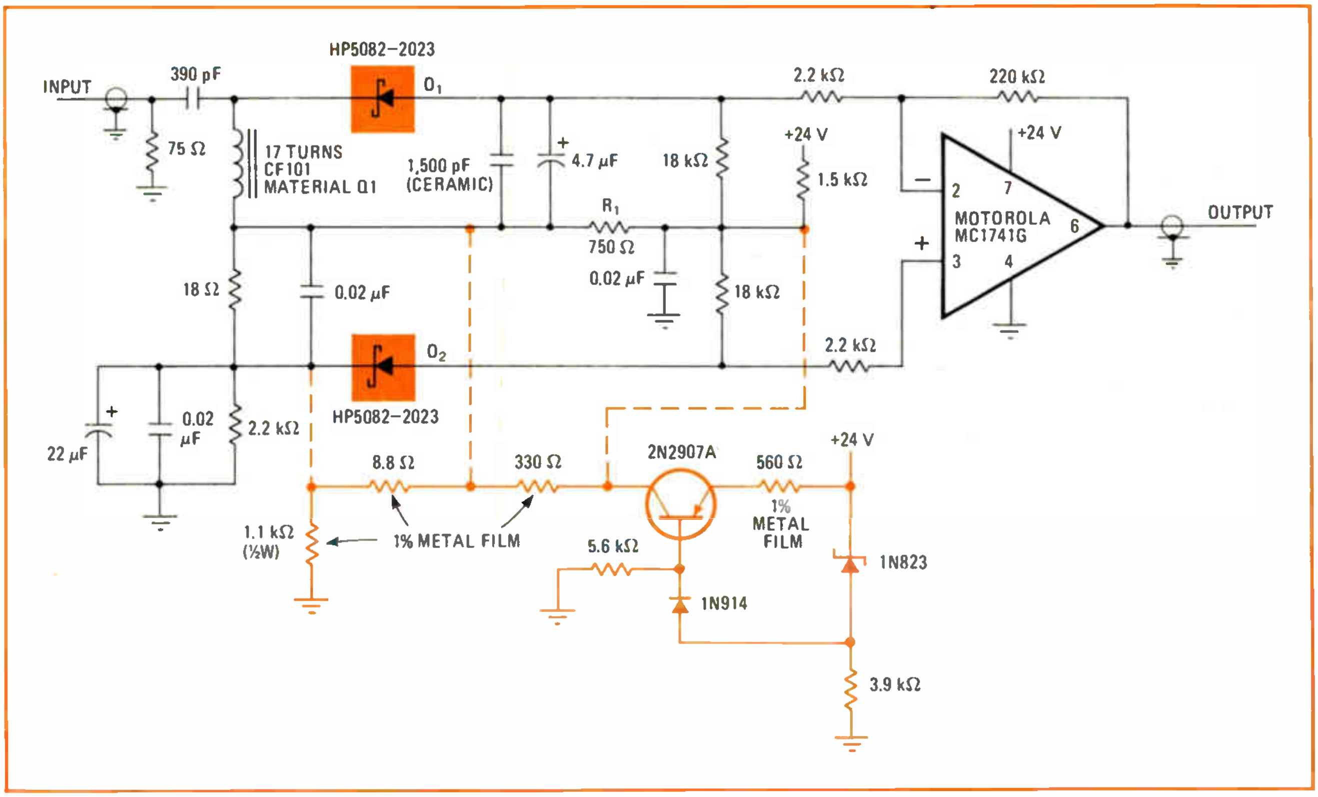
With such a circuit, the amount of rf circuitry required can be much reduced because accurate stabilized detection thresholds can be set for low rf drive levels. Also, the circuit's temperature stability and detection efficiency permit the realization of a sensitive receiver—one that can have a high video gain as well as a low rf gain.

Normally, it is hard to achieve high detection efficiency at a low rf drive level while keeping detection efficiency constant over a wide temperature range. This is because of the nature of the forward blocking voltage of a diode. For example, at room temperature, a silicon diode has a forward voltage of about 500 millivolts and a temperature coefficient of 2 mv/°C, so that the forward voltage will vary considerably—from 370 mv at 90°C to 590 mv at -20°C.

The rf drive level needed to start the detection action must exceed the diode's forward blocking voltage so that load current may flow. However, since the forward voltage changes by 220 mv from -20°C to +90°C, the rf drive level required must vary accordingly to maintain detection action. The inherent detection efficiency, therefore, is low and strongly dependent on temperature, limiting the maximum video gain that may follow the detector.

The rf detector depicted here, though, solves these problems. The two Schottky diodes, D_1 and D_2, are matched to within 5 mv from 0.1 to 0.5 milliampere and are connected in a half-wave rf detector configuration. The dc bias developed across diode D_2 and resistor R_1 serves as an arming bias for the detector diode, D_1, establishing temperature tracking between the two diodes.

The voltage drop across resistor R_1 establishes a reverse offset bias on diode D_1, in this way setting a known rf threshold that the rf drive level must exceed before detection action takes place. And the voltage drop across diode D_2 acts as a temperature-dependent forward arming bias on diode D_1. The level of this arm-



Temperature stabilized. High-efficiency rf detector operates at low input drive levels over a wide temperature range. Matched Schottky diodes (D_1 and D_2) and a fixed rf threshold bias (via resistor R_1) permit the circuit to hold voltage detection stability to ±0.06 dB from −20°C to +90°C for a 55-mV input. Sensitivity to supply-voltage changes can be minimized by adding colored network (and omitting R_1).

ing bias tracks the forward blocking voltage of diode D_1 as the temperature changes.

Because of this temperature-compensating arming bias, it is possible to realize constant detection efficiency over a wide temperature range, in addition to a constant rf threshold detection level. For a constant rf input of 55 mV, the detection voltage developed by the circuit varies only 1.8 mV between -20°C and +90°C. Rf peak voltages as large as 80 mV can be detected quite efficiently.

The operational amplifier at the output of the circuit senses the detection voltage and translates it to a 12-volt level. This output voltage varies only 2.1% from -20°C to +90°C for a constant rf input drive. Here, the op amp's gain is 40 dB, a figure that can be safely increased to 50 dB without adversely affecting the output stability of the circuit.

The circuit's performance will be further enhanced if the detector is made insensitive to variations in supply voltage. This can be done by adding a current source (shown in color in the diagram). The current source keeps the rf threshold voltage constant, despite supply variations of ±0.5 V. In connecting this source, resistor R_1 must be omitted. □

Crowbar protection circuit senses load voltage directly

by Thomas E. Skopal
Acopian Corp., Easton, Pa.

The triggering point of the overvoltage-protection crowbar circuit for a power supply can be decreased without increasing the circuit's sensitivity to transients. The trick is to have the crowbar circuit sense the voltage across the load, rather than the output voltage of the power supply, as is usually done.

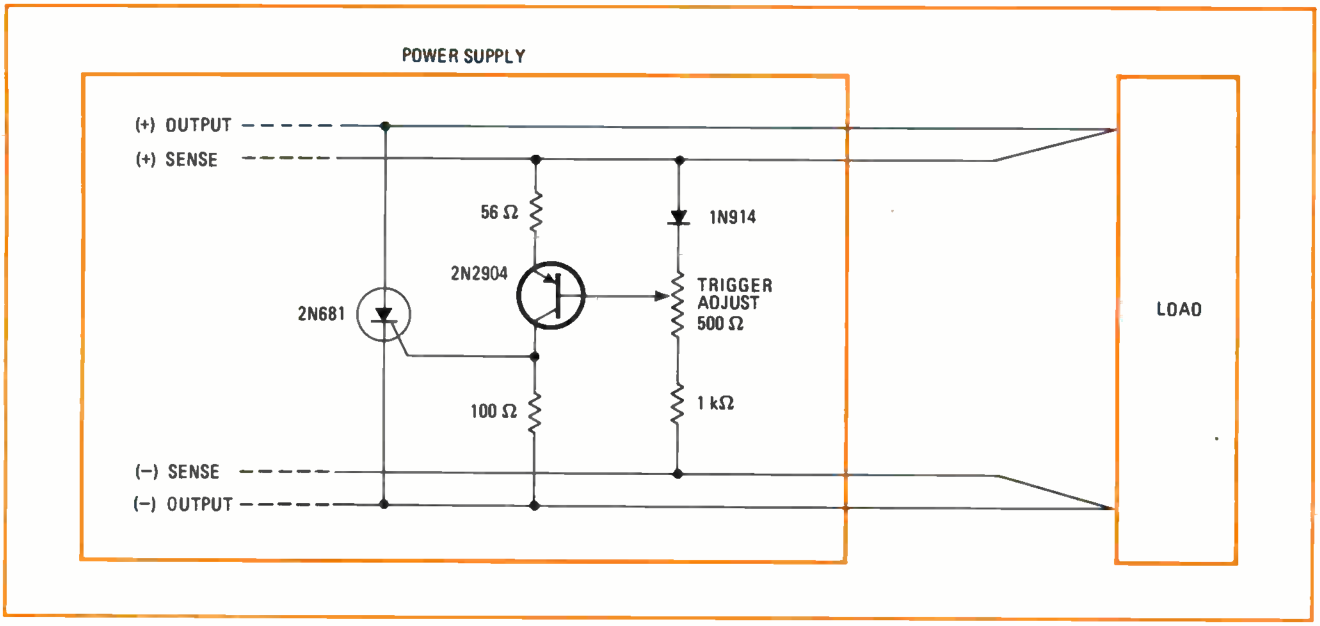
To provide maximum protection, a crowbar circuit is generally set reasonably close to the operating voltage required by the load. Typically, a compromise setting of about 15% above the load's operating voltage is chosen, because commonly encountered transients may cause spurious crowbar triggering and interfere with normal system operation if a tighter differential is used.

However, when voltage drops in the supply's output wiring exceed 2% or 3% of the output voltage—a common occurrence with low-voltage, high-current logic supplies—the system designer is faced with a dilemma. If he compensates for these drops with an increase in power-supply output voltage, the differential will be reduced and the crowbar's sensitivity to transients increased. And if crowbar setting is increased to maintain the same differential, load protection is degraded.

This conflict can be resolved by using the four-terminal crowbar circuit shown in the figure. It senses the voltage across the load, much as a supply's remote-sensing connections may be used to automatically compensate for voltage drops caused by long wires.

The crowbar's triggering point is a function of the voltage seen by the load, as opposed to the output voltage of the supply, and it is unaffected by the amplitude of the wiring voltage drops. Since the sensing connections of the crowbar share the sense lines of the supply's regulator, no additional system wiring is required.

The diode in the circuit provides temperature compensation for the transistor. The component values given are appropriate for power supplies having outputs of 4 to 10 volts and of up to 20 amperes. □



Better protection. Crowbar circuit protects a power supply from overvoltages by sensing the voltage across the load, instead of the supply's output voltage, which is the usual approach. This means that overvoltage sensing will not be affected by wiring voltage drops, nor will there be an increased sensitivity to voltage transients. The components shown here are for a power supply of 4 to 10 volts at up to 20 amperes.

Simple gating circuit marks both pulse edges

by Ralph Tenny
Texas Instruments, Central Research Laboratories, Dallas, Texas

A bidirectional edge detector can be built from only two integrated-circuit packages—or with only one package if exclusive-OR gates are used. Applications for the circuit include triggering for event counters and frequency doubling for digital data communications.

The configuration for the standard edge detector is drawn in black in (a). If NAND gates are used, as indicated here, the circuit responds to positive-going edges. If NOR gates are used, it detects negative-going edges.

When the input signal is low, the output of gate G_4 will be high. And when the input becomes high, G_4's output goes low one gate propagation delay later. Meanwhile, the input signal ripples through gates G_1, G_2, and G_3, causing G_3's output to go low after three gate delays. The output of G_4 then become high again one gate delay later. This means that G_4's output is a negative pulse that is three gate delays wide. The four gates, therefore, mark the positive-going edges of the input.

Adding three NOR gates to this standard circuit, as shown in color in (a), enables the circuit to mark both positive and negative edges. Gate G_5, together with gates G_1, G_2, and G_3, form a negative-edge detector. Gate G_6 simply inverts the output from gate G_4, while gate G_7 simply sums and inverts the detected edges.

The same dual edge detection can be obtained from a single quad exclusive-OR gate package when the gates are connected as indicated in (b). Or, an equivalent circuit can be constructed by hooking up three inverters and four NAND gates, as in (c).

The timing diagram shows the key waveforms for all the circuits. □

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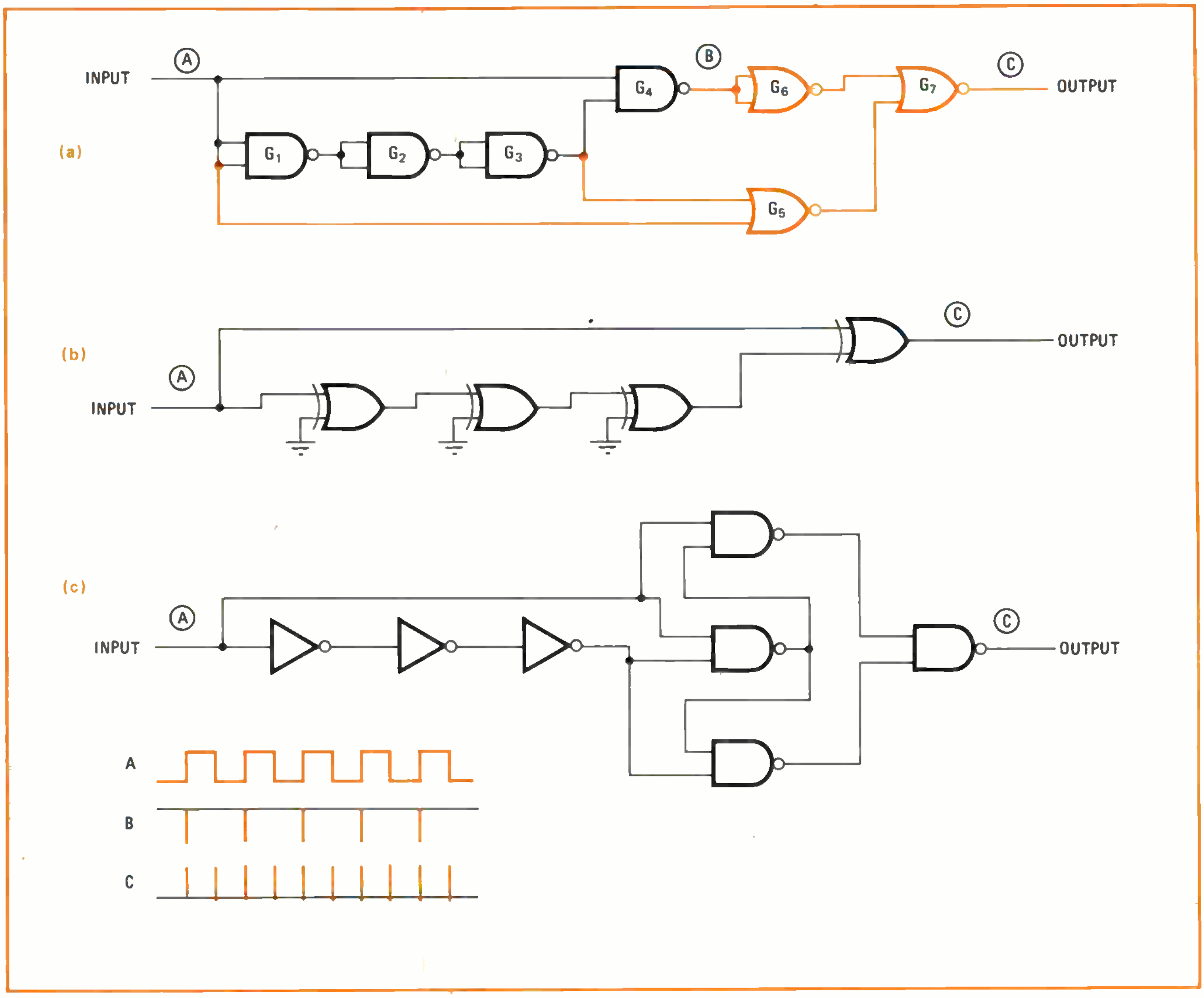

Noting each pulse-edge direction. Both positive and negative pulse edges can be detected with the same circuit by adding the three gates drawn in color in (a) to a standard unidirectional edge detector (drawn in black). If exclusive-OR gates are used, as in (b), the bidirectional edge detector requires only one IC package. Inverters and NAND gates, as in (c), can also provide the same circuit function.

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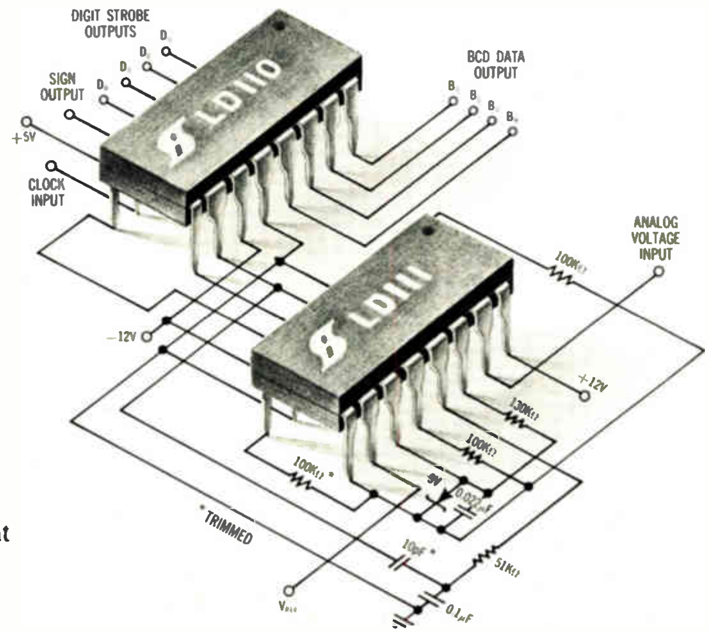

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Computer networks are taking on the heavyweight computations

The most significant trend in computer technology today is the growth of resource sharing—the linking of big and little computers by leased and dial-up communication lines into centralized or distributed networks

by Wallace B. Riley, *Computers Editor*

☐ Computer networks today are the wave of the future, just as time-sharing was, a few years ago. In a sense, networks are an extension of the time-sharing concept. A time-shared computer is merely accessible from a distance, offering multiple users more or less simultaneous access and producing its output faster than a batch-processing computer. Networks, however, offer shared computational resources, including data bases, special equipment, and sophisticated programs.

But networks and network technology also offer advantages peculiarly their own. They show the way to low-cost high-performance computing systems, since for some jobs a network of smaller systems can duplicate the capability of one large expensive system at lower total cost. And beyond this is the possibility of interconnecting networks of the new microprocessors [*Electronics*, April 18, p. 81] into networks of powerful computational systems at what would seem by today's standards to be microscopic cost.

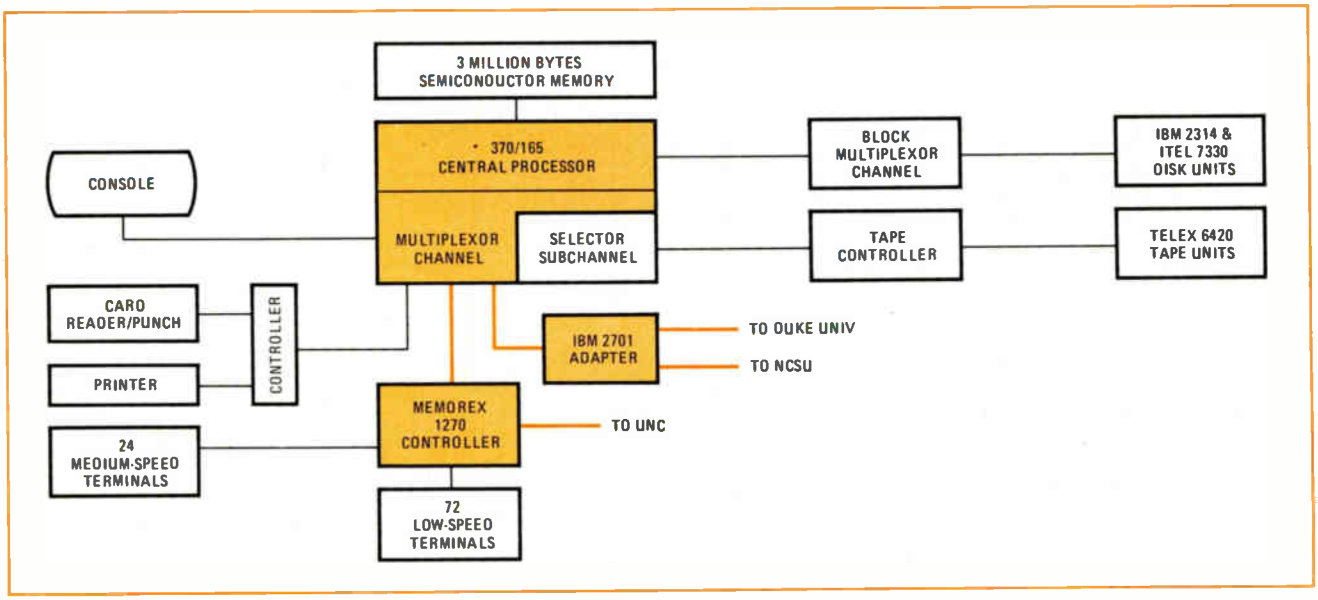
Some commercial networks are already off and running—notably General Electric's Mark III system and the Tymnet operated by Tymshare Inc. Both of these are direct outgrowths of commercial computation services that were based on time-sharing.

Other networks, still in development, will go into commercial operation within the next few months or in 1975, the fruition of recent research projects. Examples are the networks of Telenet Communications Corp. and of Packet Communications Inc., both of which are based on technology developed in the Defense Department's Advanced Research Projects Agency.

Still others are services operated primarily by and for the research community without the intent of turning a profit on an investment—such as the network of the Triangle Universities Computation Center, one of the earliest to become operational; the Octopus network at Lawrence Livermore Laboratory in California; the Merit network, serving three universities in Michigan; and the network at Carnegie-Mellon University in Pittsburgh, Pa.

Finally some networks are the basis for research into how they can extend computer capability. Examples are Prime and DCS (for distributed computer system) at two campuses of the University of California, and ongoing research in Arpanet, which was set up for this purpose but today operates largely as a research service.

While the technology of computer-to-computer communication, on which computer networks are based,



1. TUCC. One of the earliest networks to begin operation was TUCC at Triangle Universities Computation Center in North Carolina. Today it has been expanded with modern equipment to serve, not only the original three universities, but other sites statewide.

dates back in its most embryonic forms into the early 1960s, only after some time had elapsed did the concept gain a foothold in practice. One of the earliest networks to begin actual operation, for example, was started in 1966, with the establishment of the Triangle Universities Computation Center. TUCC (pronounced tuck) was set up to provide computational capability for the University of North Carolina, Duke University, and North Carolina State University, located respectively in Chapel Hill, Durham, and Raleigh.

More needed

All three institutions needed extra computing capability in the mid-1960s. They saw this extra capability available in the IBM System 360, which was just then appearing on the market. They also saw that larger models of the 360 had extensive communication capability plus attractive price/performance ratios. But because these models were beyond the needs and means of the individual universities at the time, there arose the idea of utilizing the communication capability to connect all three campuses to a single computation center.

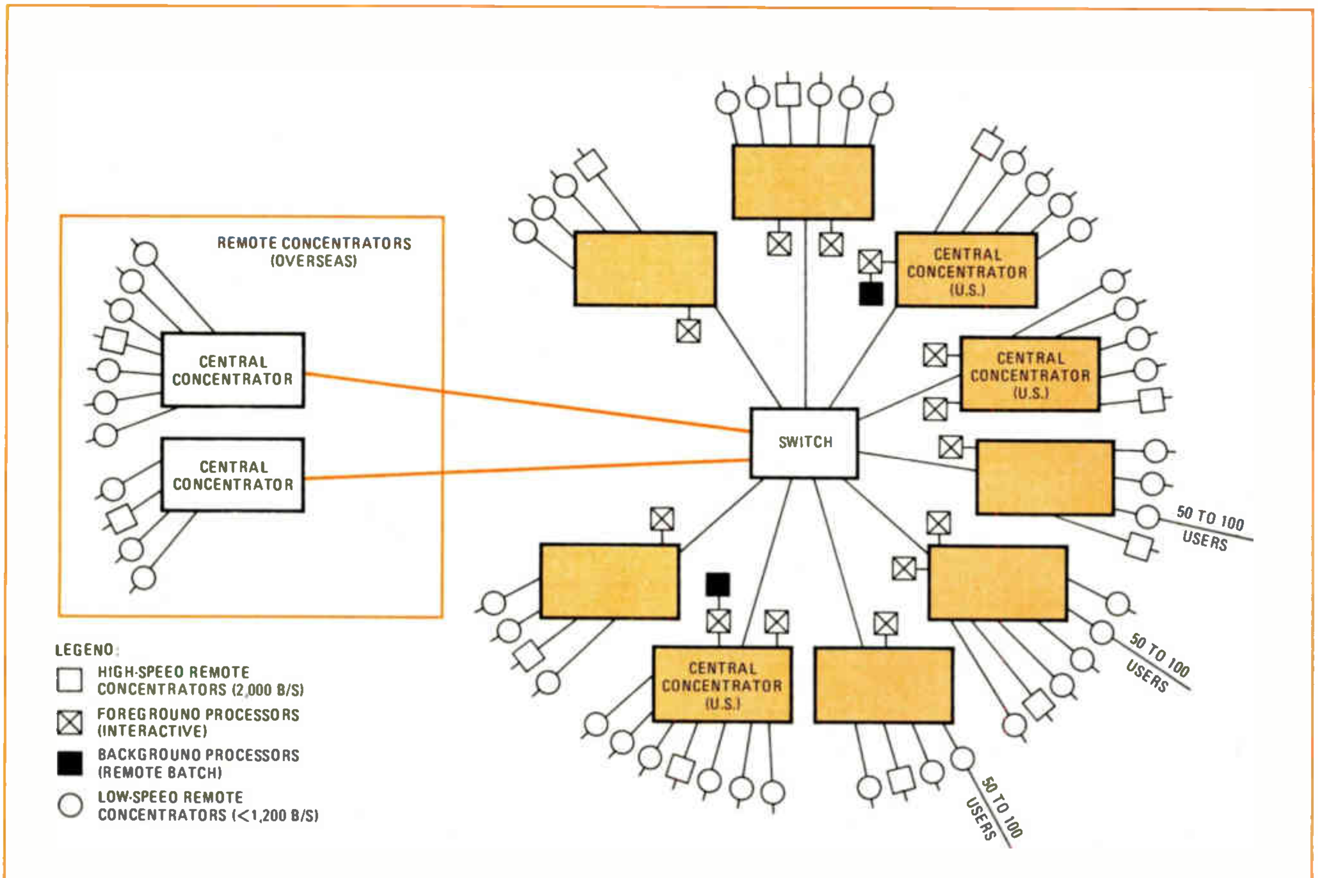
"We were guinea pigs," says Leland H. Williams, director of TUCC. "But we had to make the idea work because it was the only way all the schools could get the computation they needed, and because the remote location depended heavily on data communication."

Both the center and the three individual campuses have continued to grow in their computational needs and in the kind of equipment they use. Today, an IBM 370/165 is the network's single source node. All terminals communicate with it more or less directly, but not with each other. The network topology is therefore the "star" type (as opposed to the "ring" type, which is discussed later). But the network contains no unusual hardware—with one possible exception (see page 149).

Connected to the TUCC 370/165, as shown in Fig. 1, are a 370/135 at Duke, a 360/75 at UNC, and a 360/40 at NCSU, as well as 72 low-speed terminals operating at 110 to 1,200 bits per second and 24 medium-speed terminals operating at 2,000 to 9,600 b/s. These terminals permit TUCC to communicate directly with the three main campuses and also with the campuses of small colleges around the state. These obtain from TUCC, through the North Carolina Educational Computing Service, computational power on a scale they could not otherwise afford.

At present the TUCC network contains no minicomputers. But that situation may change shortly. Since the capacity of the controller for low-speed terminals is fully utilized, plans are being made to attach a minicomputer to the controller and to add 32 more low-speed lines to the system through the minicomputer. Conceivably, at some later time, another minicomputer may be added in one of the North Carolina cities containing multiple nodes in the TUCC network. A likely choice would be Charlotte, where two colleges and 10 high schools are already using the system.

Contrasting with university-oriented networks like TUCC are commercial networks, of which an example is



2. Mark III. General Electric's commercial network is probably the largest in operation today and reaches more than halfway around the world. Everything in the network is doubled, providing 100% redundancy and therefore an extremely reliable operation.

General Electric Co.'s Mark III system (Fig. 2), probably the largest network in operation today. Through its Information Services division, GE offers computational services to a wide variety of users. The network is basically the "star" type, like TUCC's, and the equipment is conventional, for the most part. The system covers more than half the globe, and two of everything provide 100% redundancy for reliability.

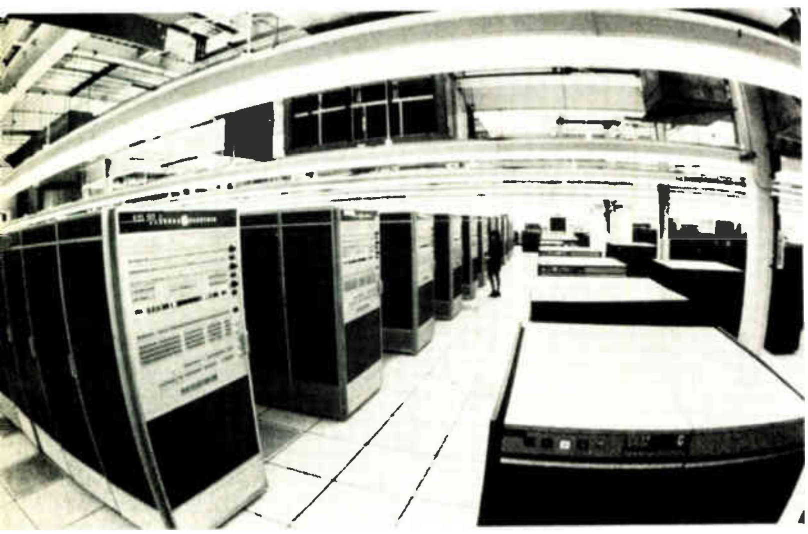
Terminal access only

The GE network, which began operation in 1969, comprises over 100 computers of various sizes, including some very large models. But these are accessible to the user only through a terminal on the network—whether interactively or for a remote batch job. In interactive use, the customer "converses" with the network asynchronously at 110 to 1,200 b/s. In remote batch, transmission is synchronous at 2,000 to 4,800 b/s.

The customer normally makes his connection by dialing a local telephone number in his own city. This connects him to what GE calls a remote concentrator in that city, or occasionally, over a foreign-exchange or leased multiplex line, to a remote concentrator in a nearby city. Each remote concentrator can handle 50 to 100 customers interactively or five to 10 for high-speed remote job entry.

Up to eight remote concentrators are connected, over leased telephone lines, to a central concentrator. Sixteen central concentrators—14 in Cleveland, Ohio, and two in Europe—form the heart of the network. Each Cleveland concentrator is connected, on its "inboard" side, to one or two large host computers, which are the "foreground" systems for interactive processing. All the central concentrators are also connected to a large central switch, so that an interactive job coming in from any user can be directed to any foreground processor. Of all incoming jobs, only 5% to 10% reach a processor by passing through only one central concentrator—the majority involve two concentrators and the switch.

Finally, for remote batch jobs, two background processors are connected to two of the central concentrators. These are very large computers that chew away at big jobs and are not required to produce immediate outputs. They may finish a job in a few minutes, or they may work overnight, either directly on a problem or on a queue of big problems, before producing outputs.



3. Network center. Large-scale Honeywell computers in Cleveland, Ohio, constitute the 15 foreground and two background computers to which the world-wide GE network is connected.

Double without trouble

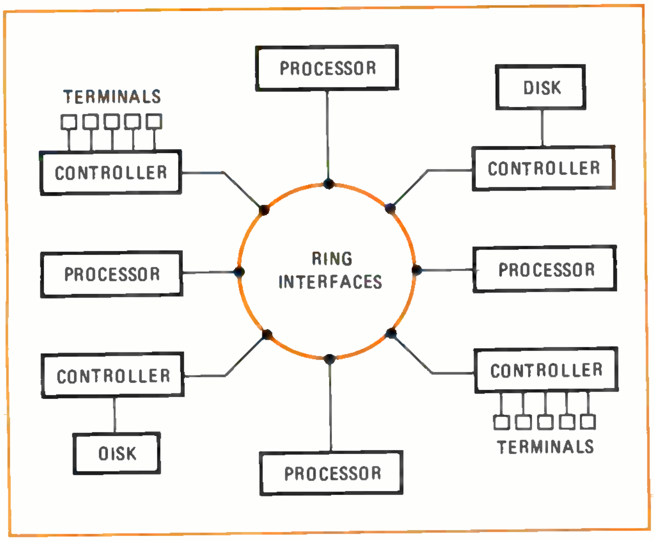
For reliability, everything in the system is duplicated, and all the interconnections are made by dual lines through different exchanges. Both lines are in use all the time, at half capacity, but if one line goes down, the other can immediately assume the full load. Even the second line can go down for as long as 10 seconds without imposing any burden on the user. If a remote concentrator goes down, users have access to a second one, usually in the same city. The 14 central concentrators in Cleveland offer a similar backup. The two European concentrators are connected to the Cleveland center by two links—undersea cable and satellite. With this degree of redundancy, obviously, failure of the whole network is highly unlikely, although individual parts give trouble from time to time.

All the machines—remote concentrators, central concentrators, switchers, and foreground and background processors—are themselves computers of various sizes. The 15 foreground units (Fig. 3) are large-scale Honeywell systems running on GE's own special operating-system software, designed for the particular requirements of the interactive network operation. Likewise, the two backgrounders are large Honeywell systems, but they run on the manufacturer's own standard software, suitable for batch operation. (Coincidentally, Honeywell's "own standard" software is really GE's, for the designs for these large machines were included in the transfer of the General Electric computer manufacturing business to Honeywell in 1970. Although the computers are part of the Honeywell 6000 series and were not announced until well after the transfer, the hardware and software were far along in development at GE at the time.)

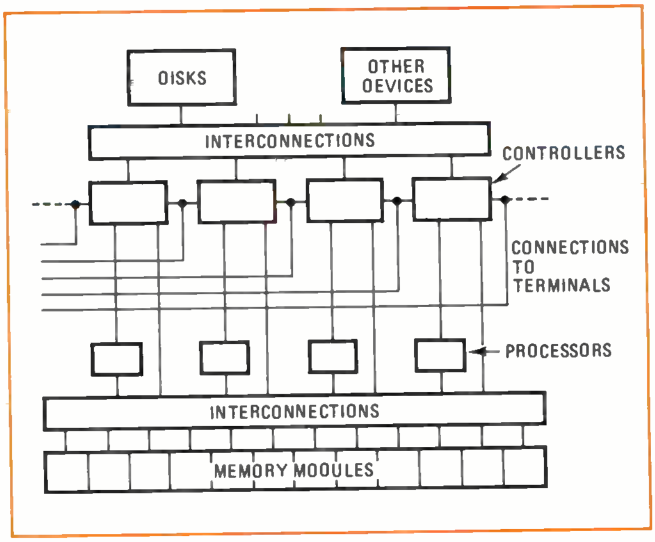
The network continues to evolve technically. For example, GE has recently found a way to improve its mass storage facilities, which serve the foreground and background computers at the center of the network. At present, each computer has its own complement of external storage plus other input/output equipment, but this soon will be replaced by four file systems serving six computers, with access by any computer to any file system. Conceptually, the interference is horrendous when two users, neither of which knows or cares that the other exists, simultaneously try to obtain access to the same file through two computers that do not interact with each other directly. GE claims to have licked the problem without lowering its level of reliability.

Another advance that will shortly appear in the GE network will be the installation of more background computers. The technical challenge is that the computers will be from different manufacturers—the first to go in will probably be from IBM, but any others may be added later without undue complications.

The GE network evolved largely to provide computer service at a reasonable price to the user and at a reasonable profit to GE. That the service is provided by a network is incidental.



4. California's DCS. Collection of processors and input/output devices bid on jobs submitted by the user. Selected unit can subcontract its job to other processors if work load demands it.



5. Prime. Designed specifically for users, not computer experts, this network consists of a pool of resources from which a supervisory processor puts together what's needed to do a user's job. High bandwidth in the path between primary and secondary memories, a characteristic of this network, is important for high performance.

Nevertheless, the network concept raises a number of questions that are best answered in a research environment, where customer service and income production are not the primary considerations. For example, how can a system adapt itself most readily to a variety of tasks? How can it reconfigure itself into a working system, at a lower level of performance, if some of its components fail? Can this reconfiguration occur without affecting availability too much? How can privacy and security for multiple users best be achieved? Are networks the best means to these ends?

Network research

Questions like these are being studied at the University of California at Irvine, for example, where David J. Farber is developing a distributed computer system, or DCS. His interest is in adaptability and reconfiguration. He regards his system as functioning at different times as a very large and complex machine, or as a network of smaller machines, or as something in between.

Such a system, Farber argues, should not have any supervisory element, because the failure of the supervisor would cause the entire system to go down, canceling the requirement for soft failure. As a result, the system is based on a ring configuration—as distinguished from TUCC's and GE's star configuration (Fig. 4). In a pure ring, the various nodes are arranged around the rim of a circle, with each computer connected only to those on either side of it. All data transmitted from any computer to any other except its immediate neighbors has to pass through all the intervening nodes en route. (Practical implementations of ring networks are usually not this simple, and will be described later.)

The configuration is more reliable than the basic star configuration in this respect: if one link in a star network fails, the nodes outboard of that link are isolated from the center (unless GE's dual-channel approach is used), but if one link in a ring network fails, nodes that normally communicate through that link can still communicate around the ring in the opposite direction.

In the absence of a supervisor, particular tasks are assigned to particular elements of the system through a process of bidding. A user describes the job he wants done through a terminal connected to some element of the system. His request goes around the ring picking up bids from any elements that can do the job and, on completing the circuit, displays the list of bids to the user. The user picks one, and the system goes to work. However, unbeknownst to the user, the system configuration may change while his job is in progress, so that it is not necessarily completed by the same machine that started it.

At the moment, four minicomputers are connected into the DCS at the University of California. Three of them are Lockheed's SUE computers, and the other is a Varian 620i. Interfaces between these computers, each of which has its own complement of peripherals, have been built from standard TTL integrated circuits at a component cost of about $1,000 each. Farber estimates, however, that the design could be implmented with two LSI packages for perhaps $40, plus design cost.

Eventually many other machines at Irvine and other southern California campuses may be connected to the network. But by that time Farber feels that DCS will no longer be a research activity, and he will turn it over to an operating authority.

Another research project, called Prime, is also at the University of California but on the Berkeley campus, some 400 miles north. It is under the direction of Herbert Baskin. Although Baskin is a computer expert working among other computer experts, he is putting together a continuously available, high-performance system designed for computer users as distinct from computer experts. "Experts are unusual," says Baskin. "They write their own programs, and if the programs don't work or if the hardware fails, they fix it. But the great bulk of computer users are like the bulk of motorists—when something goes wrong with the vehicle, they yell for help."

Baskin sees the ordinary computer user taking quarter to half a minute for input and output at his terminal, with no more than a few 10ths of a second of processing time between them. Furthermore, taking into account time to study the output, sip coffee, chat with passersby, and so on, his interaction rate will be at most two requests per minute.

Thus the computer can be expected to get a new job from one user every 30 seconds or so and to process this job in half a second, giving it a duty cycle for that user of approximately 2%. At this rate, the computer should be able to service 50 users at once, on the average.

Baskin uses this kind of analysis as the basis for the architecture of the Prime system. The system consists of a pool of processors, memory, and input/output equipment. One of the processors supervises the rest of the pool, but this supervisory function can be automatically transferred to another processor at any time. As requests come in from users, the supervisor puts together a small computer from elements of the pool. The computer thus assembled processes the request until it is finished, generally in a fraction of a second, and will not be disturbed during this time unless the system receives a request when its pool is exhausted of one or more kinds of elements. Even so, the job will only terminate if the computer has had it for some time.

Wide-band link

The Prime network aims for high performance by establishing interconnections of exceptionally high bandwidth between the primary and secondary memories. This is the path taken by data during "swapping" operations, when the currently active portion of one program or block of data is replaced by another. Since most requests from the ordinary user cause file manipulation or computation related to file manipulation, swapping is a large part of the work done during the half-second that the processor is serving a particular users. A high bandwidth in the swapping path keeps the job from getting bogged down in swapping, and also can permit several different users' programs to swap all at once. This, together with the fact that secondary memory (a magnetic drum or disk) is likely to have an access time of tens or hundreds of milliseconds, implies that many, parallel, wideband paths between secondary and primary memories are necessary. A single path is quickly bogged down and remains a bottleneck even if the capacity of secondary storage is enormous.

Baskin's group is currently putting together a network (Fig. 5) containing five processors, 26 memory modules, and 15 high-speed disk drives in the pool. The processors are Meta 4 computers from Digital Scientific Corp. and include general-purpose emulators—Digital Scientific's stock-in-trade—that run programs written for the Xerox 940. Later, other emulators for the DEC PDP-10 and other computers will be added.

Four-center network

Ring networks are not limited to university research projects, for Tymshare Inc. operates a distributed network of computers commercially. Called Tymnet, it is a practical version of the basic ring shape, which usually has to become a distributed network to cope with specific applications. For example, traffic conditions may require more interconnections than the pure ring makes available, or reliability may call for more than two paths between nodes.

Much like the GE network, Tymshare began by supplying service on a time-shared basis and grew into a network to satisfy its customers' requirements for capacity and reliability. Tymshare's emphasis is on low-speed interactive service, going from widely scattered terminals to nodes in over 70 cities, to a dozen or so switching centers, and finally to 33 large host computers in four centers—Cupertino, Calif., Englewood Cliffs, N.J., Houston, Texas, and Paris, France.

Most of these 33 large computers are aging Xerox 940s, which remain in use because of their superlative time-sharing software. Six DEC PDP-10s and one IBM 370/158 are also installed in the Cupertino facility. The nodes and switching centers scattered about the U.S. and Europe are all Varian 620 minicomputers, as are the small front-end computers that interface the network and the large central computers (Fig. 6).

Both GE and Tymshare networks can incorporate a customer's own computer, affording it access to remote facilities for special purposes and giving access to it to other network users. Tymshare, in particular, has 19 such connections with nine different customers. One is the National Library of Medicine, whose Medline data base is accessible from the Tymnet. Subscribers to the library can, for example, look up unusual combinations of symptoms, as an aid to diagnosis, or the specifications of rare drugs and medicines and their sources. One of Medline's outstanding files is on toxicology, which provides information on the symptoms and antidotes for a wide variety of poisons.

Other networks

In Michigan, three universities are interconnected over a network called Merit. Although the University of Michigan, Michigan State University, and Wayne State University have different computing requirements, the network lets their students and faculty share resources, augmenting one another's capabilities and avoiding duplication of effort.

Wayne State in Detroit and the University of Michigan in Ann Arbor, 35 miles west, each have an IBM 360/67. Michigan State, in East Lansing, 60 miles northwest of Ann Arbor, has a Control Data 6500. The interface between each computer and the leased 4,800-b/s line that interconnects the network is a DEC PDP-11 computer. Eventually the network may be extended to other institutions in Michigan, in much the same way that TUCC serves the state of North Carolina.

In Pennsylvania, a rather diversified network has grown up at Carnegie-Mellon University in Pittsburgh. It began several years ago with the installation of a relatively simple link between the university's IBM 360/67 and its Univac 1108, both large-scale computers. A more flexible yet less expensive connection was later made through a DEC PDP-11/45, which also allows ports to be added to the connection at low cost, and by now a second 11/45 has been tied to the first. The two 11/45s share a common memory and serve 90 teletypewriter and similar terminals scattered around the campus, plus two minicomputers in the departments of psychology and biotechnology, plus four other time-shared machines at various research centers in the U.S. and Canada. All of these have access, through an 11/45, to both the 1108 and the 360/67. Besides, in the department of physics, a PDP-8 is used as a remote job entry terminal to the 1108 alone, over a private connection.

This network is operated by the university's computation center. In addition, the department of computer science maintains a connection to the Arpanet, described later. The computation center network is not connected to the Arpanet node at present, although it may be in the future.

In California, a network called Octopus provides an impressive level of computing capability to the personnel of the Lawrence Livermore Laboratory, which has an exceptionally large and highly concentrated computer center to simulate nuclear reaction experiments that cannot actually be performed. The network's name comes from its original configuration—a single large switching unit connected to an array of worker computers on one side and to a collection of mass storage units on the other. But by now it's a cross between an octopus and a hydra, since to improve reliability, the single switch was replaced by five concentrators, with more to be added in the near future. (Another network, at Los Alamos Scientific Center, is called Hydra.)

All the worker computers—presently four Control Data 7600s and one CDC 6600, and shortly to include CDC's giant Star-100 (Fig. 7)—are connected in general to all the concentrators, each of which is itself a computer of substantial capability. For example, the one that controls the data files for the system is a large Digital Equipment Corp. PDP-10. Originally the "head" of the octopus, it now also maintains a time-sharing system of its own and controls raster-scan terminals that display graphic data in conjunction with Teletypes. Other concentrators handle interactive terminals, remote job entry terminals, and a subnetwork of data-collection devices. New concentrators are planned for additional peripheral equipment—notably the new Honeywell high-speed printers [*Electronics,* Nov. 6, 1972 p. 44, and in Electronics Review, this issue].

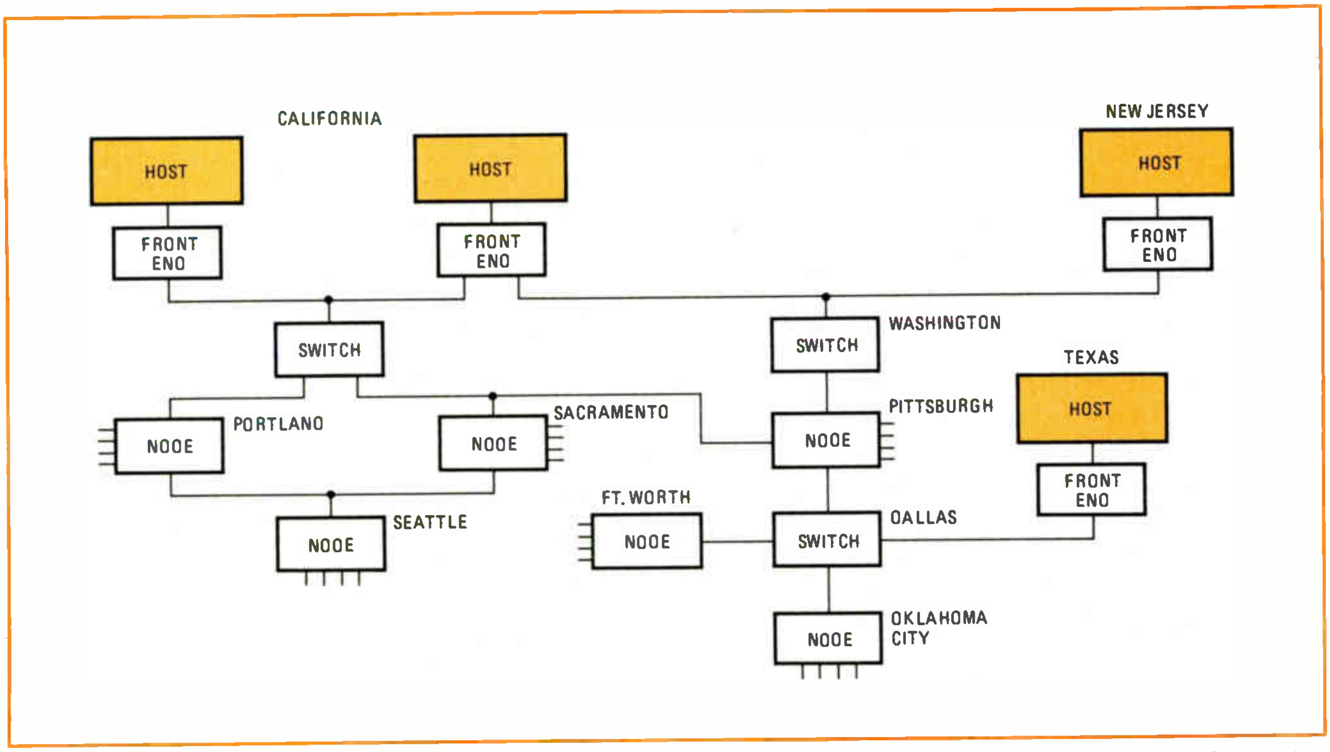
A borderline case

Both research and commercial networks are obviously going propositions. Moreover, one very impressive network, the Arpanet, built as a basic research project in its own right, seems to be turning into a commercial operation or at least a research service. It even seems to be spawning several purely commercial enterprises patterned after it (see "Commercial Arpanets," p. 105).

The Arpanet is a project of the office of information processing techniques in the Defense Advanced Research Projects Agency of the U.S. Department of Defense. Over the years, Darpa has also provided much of the funds for MIT's Project MAC, for Illiac 4, and for work on many other computer-related research projects—as well as advanced projects in space, seismology, and other fields.

The Arpanet interconnects about 30 or so research organizations, working under contract to Darpa. It permits people at any one of these laboratories to obtain access to a computer at any other. Its overwhelming advantage is that every node has access to all the computing resources of all the nodes, including special data bases, special programs, and unusual equipment.

At each host computer is an interface message processor (IMP), which translates the hardware and software idiosyncrasies of the particular computer at that node—



6. Distributed commercial network. Tymnet offers service from four centers (three shown here) through switching centers and concentrators in various locations such as those named, interconnected to provide alternative paths in the event of localized failures.

such as interface requirements, cycle time, word length, and operating system—into the requirements for data transmission over the network. The IMP also performs the reverse translation for incoming data. All data is transmitted over the network in the form of "packets" of a maximum of 1,000 bits, with an address on each packet that indicates its destination and its position in a larger block, if any.

Packet switching permits a message to be sent over the network without having a path established for it in advance. This is unlike telephone switching, where a customer has the exclusive use of a circuit during his call. Voice communication is essentially continuous, whereas computers tend to talk in bursts and use as little as 1% to 10% of a continuous channel capacity. But routing can change from moment to moment, depending on traffic, equipment failures, and so on, so that the packets may arrive at the destination in a different order from the one in which they were sent—this is why the address includes packet-ordering information.

Not all nodes in the Arpanet have host computers. Some rely on terminal IMPs, or TIPs, which give them access to the network but provide no service to other users of the network.

Packets by radio

Another packet-switching project is the Aloha system centered at the University of Hawaii and linking computer centers and terminals in the islands that constitute the state of Hawaii. Aloha was initiated as a separate project but, under the direction of Norman Abramson, has become part of the Arpanet, through a satellite link to the mainland via Intelsat.

Although Aloha's packet-switching approach is much like the Arpanet's, it does differ from the Arpanet in two major respects. First, it has only one central computer and therefore is a star-type network, not a distributed network, as is the Arpanet. Second, its remote terminals communicate with the central computer over a two-channel radio broadcast link rather than by wire (Fig. 8). One channel is for incoming data and the other for outgoing.

Since many remote users may be communicating with the central computer at once, a multiplexer is required as a front end to that computer. This multiplexer operationally resembles the Arpanet's IMPs, so, rather puckishly, Aloha's designers called the multiplexer a Menehune. (In Hawaiian folklore, a menehune, rhyming with penny loony, is an elf, or imp.)

At Darpa, the network is in care of J.C.R. Licklider, director of the office of information processing techniques. Now that the network is in many respects past the R&D stage, one of Licklider's tasks is to help develop a means of operating the network outside his office, which is concerned only with basic research and exploratory development. In all probability such a means will be another Government agency or a commercial organization designated to run the network, followed by a transfer of technology over a year or so. Meanwhile, Licklider cautions that, although the network is in many ways a service now, much developmental work remains that can be suitably done within his office.

For example, the network isn't as reliable as some users would like it to be. One critic, whose organization has a host computer at one node, says that he uses it only a couple of times a month, generally just to send messages to colleagues at other nodes—"and even then it's often shut down when I want to use it," he says.

Certainly a weak spot in the network is that IMPs in general are on the same site as their hosts. As a result, when host personnel shut down their computer for the weekend or for any other reason, they sometimes shut down the IMP, too, so that it can't handle packets passing through to another destination.

Licklider points out another weakness—the nonredundancy of the IMPs at source and destination, and of the connections from the IMPs to their respective hosts. As originally envisioned, the IMPs were to be linked to the host by no more than 200 feet of straight wire. But experience has shown that sometimes cables as long as 2,000 feet are needed between an IMP and its host, calling for the installation of line drivers and receivers. In a few cases, the hosts have been so far away that the only feasible connection between the IMP and its host was to add another modem and a common-carrier line. The alternative in these cases was relocating the wideband line of the network itself.

Licklider also cites work going on toward increasing the throughput of the network itself. For example, present 50,000-b/s lines could be replaced by lines with a capacity of a megabit or more. Alternatively, satellite connections could be used between nodes.

Abramson's experience with the Aloha network is germane to this issue. He chose the radio links for the network, partly as a research exercise, and partly to overcome technical problems that occur with telephone-line links (telephone cables *do* exist between the islands of Hawaii). But instead of merely substituting the radio for the telephone, Abramson's system architecture matches the unique characteristics of the radio link, as distinguished from those of the telephone. These characteristics include low duty cycle per user and nearly noise-free uhf transmission along a line-of-sight path.

Like the Arpanet, Aloha uses packets of data that are standardized at a maximum of 80 characters, plus control and parity bits, for a total of 704 bits (compared to Arpanet's 1,000 bits). The Aloha terminal transmits such a packet in about 30 milliseconds, though the average user is unlikely to send more than about one such packet per minute, for a duty cycle much below 1%.

One frequency for all

All users share a single radio frequency. But because of the low duty cycle, there is only a slight probability that two users will send a packet at the same time and interfere with one another. Of course, the probability is not zero. But if two independent packets do overlap, or if any packet is received in the presence of obscuring noise (unlikely with the uhf channels used), an error-checking code included in each packet signals an error, and the originating terminals retransmit their packets. Only when a packet is received without error does the receiver send back an acknowledgement (Fig. 9).

With uhf broadcasting, transmission is essentially only along the line of sight. Consequently, all the terminals of the Aloha network installed so far are on the is-

Commercial Arpanets

The technical success of the Arpanet has led to the formation of two commercial enterprises, Telenet Communications Corp. and Packet Communications Inc., which each have close links to the parent project. Both have been boosted by the reluctance of the Defense Department to operate the Arpanet as a service and by certain deficiencies in the network that have become apparent from experience with it. Both are value-added networks (VANs), which means that both will lease wide-band communication lines from a common carrier (AT&T), add terminal, computer, and interface facilities, and resell the package. Both are expecting patronage from banks, credit bureaus, and other large organizations of all kinds that need data communications in bulk, and that now must build their own networks to get the service they need.

Lawrence G. Roberts, who was director of the Defense Advanced Research Projects Agency's information processing technology office from 1969 to 1973 and a special assistant to the director from 1967 to 1969, is now the president of Telenet Communications Corp. He made the move from Darpa to Telenet because, he says, the technology had gone about as far as it could within the Government agency. "It had to become a commercial service to demonstrate its real value and to continue its development. It's also attractive, both in a business sense and because it provides a needed service."

Roberts plans to have a seven-city network in operation by next January and to expand the network to 18 cities during 1975. Each city will have an interface message processor (IMP)—something like Arpanet's—in a Telenet-owned facility, reachable by local subscribers over 4,800-b/s dial-up lines, and connected between cities by 50,000-b/s leased lines, or by 1½-million-b/s satellite channels. The land lines will be better for short messages, because they are not subject to the quarter-second delay imposed in satellite transmission by the satellite's high altitude. But large blocks of data can go by satellite because the bandwidth of the channel is larger and hence the cost is less.

"The satellite links will also be very effective in a broadcast mode," says Roberts, "when you have a block of data that must go to many nodes at once. To do that with land lines would require moving it step by step across the country, with larger capacity on each of the segments en route."

Telenet's IMPs will be duplexed at each node and concerned only with forwarding messages that pass through; local connections will be handled by duplexed terminal interface processors (TIPs). The duplexing will provide a degree of reliability not enjoyed by Arpanet users. Telenet's IMPs and TIPs ("I invented the words, so I'm going to use them," says Roberts) will be dual-source machines from Honeywell and from Prime Computer Corp.; the two are compatible. Arpanet's IMPs are Honeywell 516s and 316s.

The other Arpanet spinoff, Packet Communications Inc., has Lee R. Talbert for its president. Talbert was formerly an employee of Bolt, Beranek & Newman Inc., the prime contractor for the IMPs and other Arpanet hardware. His task was to study the commercial opportunities offered by the company's work with the Arpanet. He found BB&N unwilling at the time to make the investment he thought would be necessary, so he decided to make the attempt independently, starting PCI in July, 1972. (Paradoxically, just a few months later, BB&N backed the establishment of Telenet, of which Larry Roberts eventually became president. Today BB&N owns 54% of Telenet's stock.)

The level of investment Talbert is talking about is shown by the size of network he says is necessary for economical operation. To transmit 1,500 packets per second, none of which is delayed by more than 0.2 second in reaching its destination, would require about 13,000 terminals connected to 50 to 100 large computers. However, to ease the financial problems of getting started, Talbert and his associates have decided to back off from immediate implementation of these specifications—most notably in the delay from source to destination of 0.2 second. If a full second is allowed, PCI would have five times as long to get a packet onto a line, and the network can break even with fewer terminals and computers.

"Therefore, our initial offering will be on lines running at 9,600 bits per second and costing that much less than the faster lines," says Talbert. "We'll grow into the faster lines with correspondingly better service as our business increases." PCI will begin selling its service this month, and hopes to begin operation in 18 cities during the summer of 1975.

PCI's network will resemble those of Darpa and Telenet in many ways, but will have some important characteristics of its own to escape some of the problems of the Arpanet. "Darpa's experience with the IMPs gives about 200 to 400 hours mean time between failures," says Talbert. "We want something like 10,000 hours. And we don't like the idea of adding redundancy, because it creates new problems with interfacing." When interviewed, Talbert hadn't made any commitment to a particular vendor, but felt that General Automation was out in front as a likely source for the computers, which will be called packet switching processors and terminal access processors—PSPs and TAPs—corresponding to Darpa's IMPs and TIPs.

One problem that both Telenet and PCI face is the unwillingness of commercial network customers to adapt the software in their computers to work with the network. The Arpanet's users are research laboratories whose people are able to tackle the software modifications—"but in the commercial world they're not about to do that at all," says Roberts. Talbert emphasizes that his network processors provide the host—any kind of host—with an interface exactly like the one the host works with in its own data communications. This standardized (to the host, anyhow) interface removes the need for a network control program, which the Arpanet requires, but still lets the design of the network processor evolve.

Roberts

Talbert

land of Oahu, where the university's main campus is, and on Maui, 100 miles southeast. Conventional repeaters are used in the link between the two islands, which passes over the island of Molokai.

These repeaters, however, are quite unsuitable for a packet-switching system. Designed for use with voice-transmission and similar analog channels, they receive a signal on one carrier frequency, remodulate it onto a different frequency, and retransmit it. The frequency shift is necessary to prevent the repeater from picking up its own continuously transmitted signal. When many different repeaters are being used in a single system, careful choice of frequencies is necessary, together with filtering, to avoid interference.

Abramson's group is developing a new kind of repeater, one that can store an incoming packet and retransmit it at the same frequency—separating the incoming and outgoing messages in the time domain. A single frequency could then be used for the entire system. The storage presents no problem, Abramson points out, since a 1,000-bit storage module can be hand-held.

The radio link is also encouraging the group to develop a portable terminal—a much simpler task with radio transmission than with telephone lines. Abramson expects a prototype requiring plug-in power to be ready this month. Later, an even smaller battery-operated unit will be developed, he thinks.

European networks

Networks, of course, are not the monopoly of the United States. Arpanet, General Electric, and Tymshare have links to Europe and Japan, and Europe has some impressive networks of its own.

In West Germany, some networks link banks with one another, and others store and exchange data on wanted persons between computers at state and federal police centers. One network, undergoing continual expansion, links the stock exchanges in Düsseldorf and Munich, is now adding the Berlin exchange, and will link up with the Stuttgart bourse shortly.

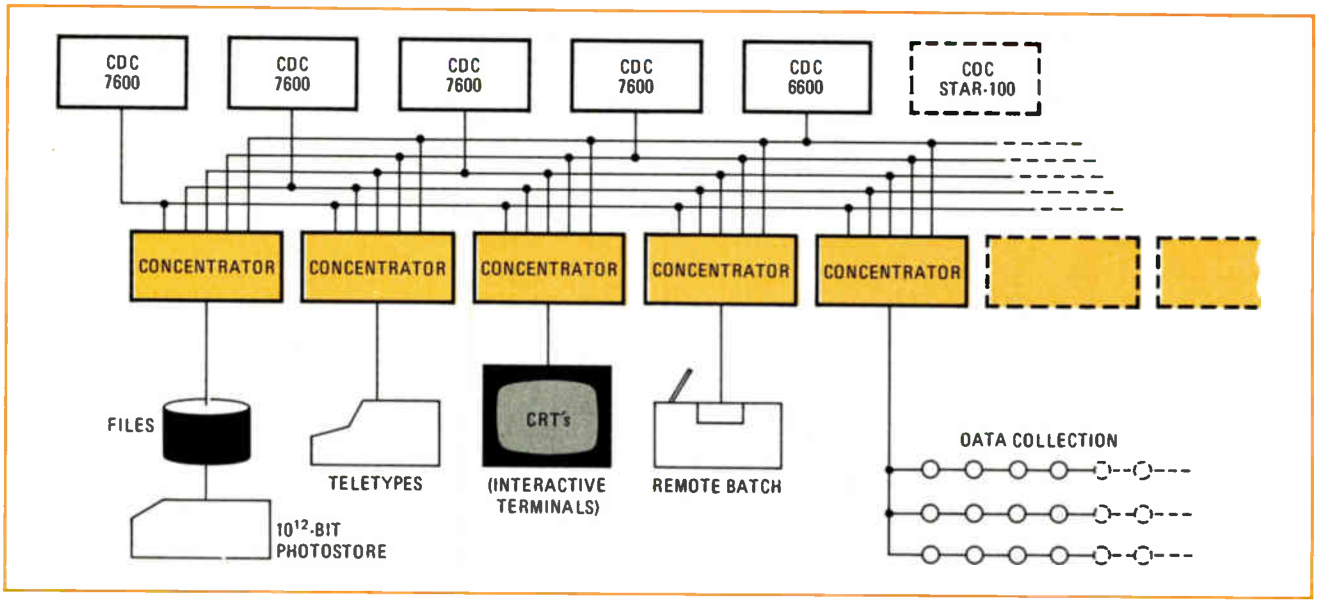
In Scandinavia, 1,600 savings banks with 5,200 offices in four countries are to be interconnected through a network now being installed by Saab-Scania AB of Sweden. It consists of teller terminals at individual bank windows, local minicomputers in each bank branch, larger computers coordinating all the banks in a given district, and finally large central computers. Machines from several different manufacturers are included in the network. Saab has also sold a similar system to the Central Savings Bank in New York.

Sweden's two largest commercial banks, Svenska Handelsbanken and Skandinaviska Enskilda Banken, have also installed their own networks linking about 500 branches apiece throughout the country. The Handelsbanken system is being installed by Svenska Philips AB, a subsidiary of Philips Gloeilampenfabrieken of Holland, which is also putting in a network to link 750 of Sweden's largest post offices. The system will handle a variety of postal operations, from registering letters and handling payments, to printing receipts. It includes 570 minicomputers (some shared by nearby offices) and large central computers in Stockholm.

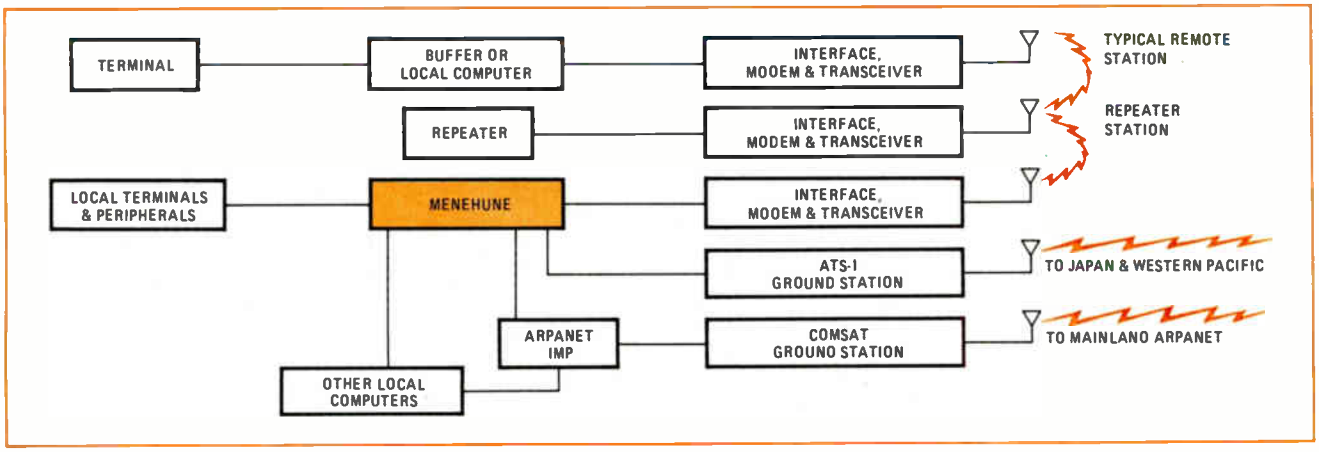
French ambitions

Right now France is lagging behind its European neighbors in installed computer networks, but by next year at least two government-backed packet-switching networks will be operating on a more than experimental scale. The government's plans are very ambitious. To meet its target of 110,000 terminals installed by the end of 1977, the growth rate will have to exceed 100% a year, since only about 8,250 are installed now.

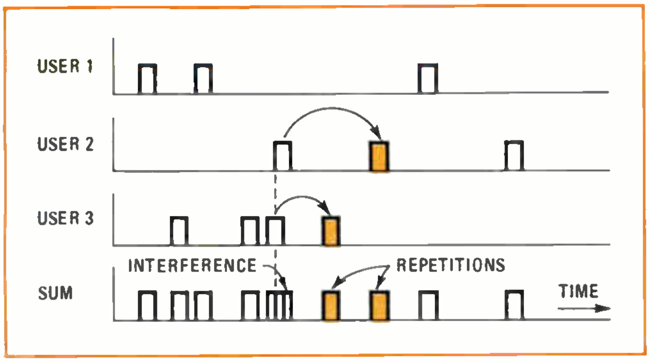
One of the planned networks, called Cyclades, will interconnect the country's main government research bases and will permit a dialog between scientists or between data banks in different computers. Various sizes and types of computers will be included, ranging from the IBM 360/67 and Control Data 6600 down to the Hewlett-Packard 2100 and the Philips 1100. The network will resemble the Arpanet in the U.S. in many



7. Octopus. At Lawrence Livermore Laboratory a variety of high-powered computers is interconnected with bulk storage units, data collection devices, and remote terminals. The network can simulate complex nuclear experiments that cannot be carried out in the real world.



8. Through the air. In Hawaii, several remote stations are connected to a central host computer with radio links instead of the usual telephone line. Similar links are maintained between this Aloha network and the Arpanet, in mainland U.S., and western Pacific computers.



9. Low interference. Because each user occupies an Aloha data channel much less than 1% of the time, two users are unlikely to transmit simultaneously. But if neither message will be acknowledged by the receiver, and both will therefore be repeated.

ways: the function of Arpanet's IMPs will be carried out by small Mitra 15 computers built by Compagnie Internationale pour l'Informatique (CII).

Another network, for commercial applications, will be the RCP, for Réseau de Commutation par Paquets, being developed by the French Post and Telecommunications Ministry Research Laboratories [*Electronics*, March 7, p. 52]. At one time RCP was to be combined with the general telephone network, but the authorities now have lowered their sights to achieve an extensive packet-switching network on its own set of leased telephone lines.

The Russians are planning computer networks as well. The OGAS program, which stands for All-Union Automated System for Planning and Management when translated, will link a system of regional computer centers to Moscow and to local computer rings in each region, all as part of a long-range effort to bring management of the economy up to date. The Soviet Union has signed an agreement with Control Data Corp. under which CDC will provide technical assistance and perhaps two large CDC computers for use as part of the network, which would be patterned after CDC's Cybernet system in the U.S. The network would also include IBM-360-like Russian Ryad computers.

However, the agreement is not final, pending clearance by the U.S. Government under existing regulations that restrict the export of militarily significant computers and computer technology to the Soviet Union. Such clearance is not expected for some time. Even if it is granted, the Soviet network is not slated to begin operation before 1990.

Nontechnical problems

Many university research networks are or have been supported in part by the National Science Foundation, whose principal interest has been in the sharing of resources, computer-based or otherwise. According to Donald D. Aufenkamp, head of computer applications in research, in the division of computer research at NSF, one of the foundation's major recent projects was to fund several star networks that would let a major university share its computational facilities with a dozen or so other colleges in the area.

The biggest problem turned out to be the missionary work that was necessary to make that kind of resource-sharing useful. "It's not enough just to hook up all the computers and buy terminals for people," says Aufenkamp. "You need a mechanism to facilitate the use of the resources. In some cases you need instructional material. You have to make it easy for people to use the system, and that depends on the level of sophistication they have to begin with."

Other problems arise over the transferring of funds between institutions. Sometimes a small college with its own computer center may suffer some dislocation because an on-campus terminal also offers access to a major center on another campus, a bright light some miles away. That may generate a lot of resentment. Or if the local campus has access to the Arpanet, it may save money on hardware and communication costs, but it may lack the expertise needed to productively use the network's broader expanse of machines and services. Indeed, the local college may have to increase its own staff, offsetting some of the hardware savings.

"Many subtle issues and considerations are involved in determining what savings and over-all costs may accrue to an institution when it is tempted to join a network," Aufenkamp concludes. "Furthermore, determining the total cost alone doesn't consider the effect on the individual groups that contribute to that cost. Even if the dollar cost is reduced, what do you do if the results are unsatisfactory in some way?" □

Data General introduces the first stereo computer system.

Current steering simplifies and shrinks 1k bipolar RAM

Steering a current through the decoder matrixes simplifies circuitry and eliminates the many resistors needed by voltage-mode TTL devices; moreover, a single circuit can perform an entire logic function

by John E. Gersbach, *IBM Corp., Essex Junction, Vt.*

☐ To pack 1,024 bits of random-access memory on a single bipolar chip requires a combination of processing advances and innovations in circuit design. IBM's 1,024-bit RAM, introduced in 1973 into the System /370 and System /7 computers, is no exception.

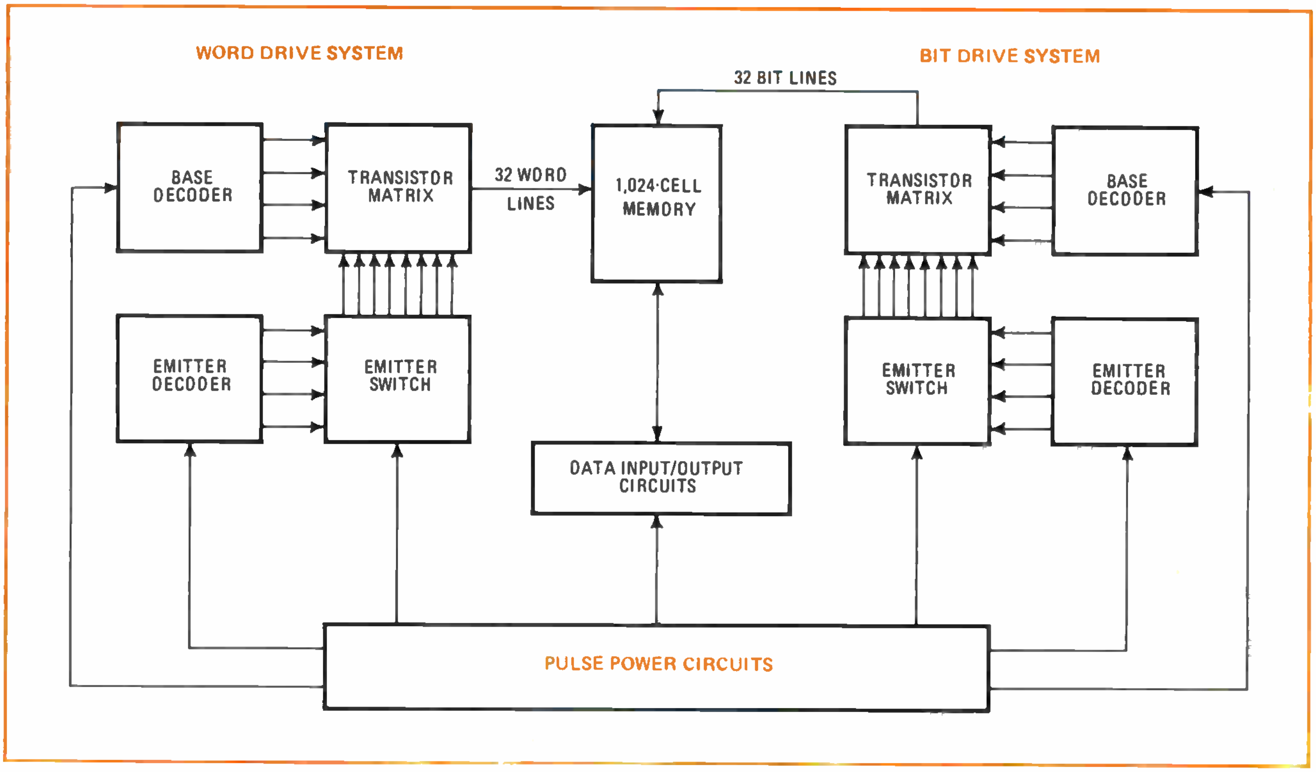
The processing advances used to obtain smaller chip size and better performance included self-aligning emitter contacts and thin (3.5-micrometer) epitaxial layers, while double-layer metalization eliminated the need for conductive underpasses in silicon that would have added to parasitic capacitance. The use of emitter-over-base pinch resistors also reduced both the size and the power dissipation of the individual memory cells [*Electronics*, March 7, p. 130]. The new circuit approach was to access each cell, not with the voltage-mode circuits of TTL, but with current-steering circuits, which afford space and power savings.

The current-steering approach also made it possible to perform entire logic functions in single circuits, rather than in an assembly of such separate circuits as AND gates and inverters. Essentially, the logic design was worked directly into the circuit design.

The 1k RAM is organized in a 32-by-32 array. To access individual cells, five bits of the 10-bit address code steer an 8-milliampere current through decoders to one of the 32 lines in the X direction (called word lines), while the other five address bits steer another 8-mA current to one of the 32 Y lines (or bit lines).

The use of current-steering circuits has many advantages over the use of TTL voltage-mode circuits:

- Small size—for the same power and performance, total resistance is two to three orders of magnitude lower than in TTL circuits, increasing packing density.
- Low power—only small voltage swings (±400 milli-



1. Complete memory. Currents are steered by address bits through decoders (emitter switches, base decoders, emitter decoders, and transistor matrixes) to word and bit lines to gain access to one of 1,024 cells. Output from the cell appears on data bus and is switched to data out line. Pulse-power circuits generate currents used throughout the memory.

volts) are required to steer just one current, performing many functions, through many circuits.

- Light loading of driver circuits—only base currents are required to drive inputs.
- Wide design margins—performance depends not on the absolute but the relative tolerances of resistors and diodes. Since these are inherently good in integrated circuits, yields rise and costs drop.
- Simplicity—powering the circuits with pulsed power is easily accomplished, and it takes relatively few transistors to steer a current. Packing density is thus increased. In addition, the power-performance product can be dramatically improved by such circuit simplification as "collector-AND" functions (connecting collectors together to perform AND operations) and cascoding (so that the drive current is used only for on-devices, and none is used to keep off-devices off).

Performance and power

The memory basically consists of address decoders and drivers for the word and bit lines, the memory cells, the data input/output circuits, and the pulse-power circuits (Fig. 1). In the IBM applications, the chips are packaged four to the module. Only one of the four is powered at any one time, during which period chip-select pulses gate the decoder circuits.

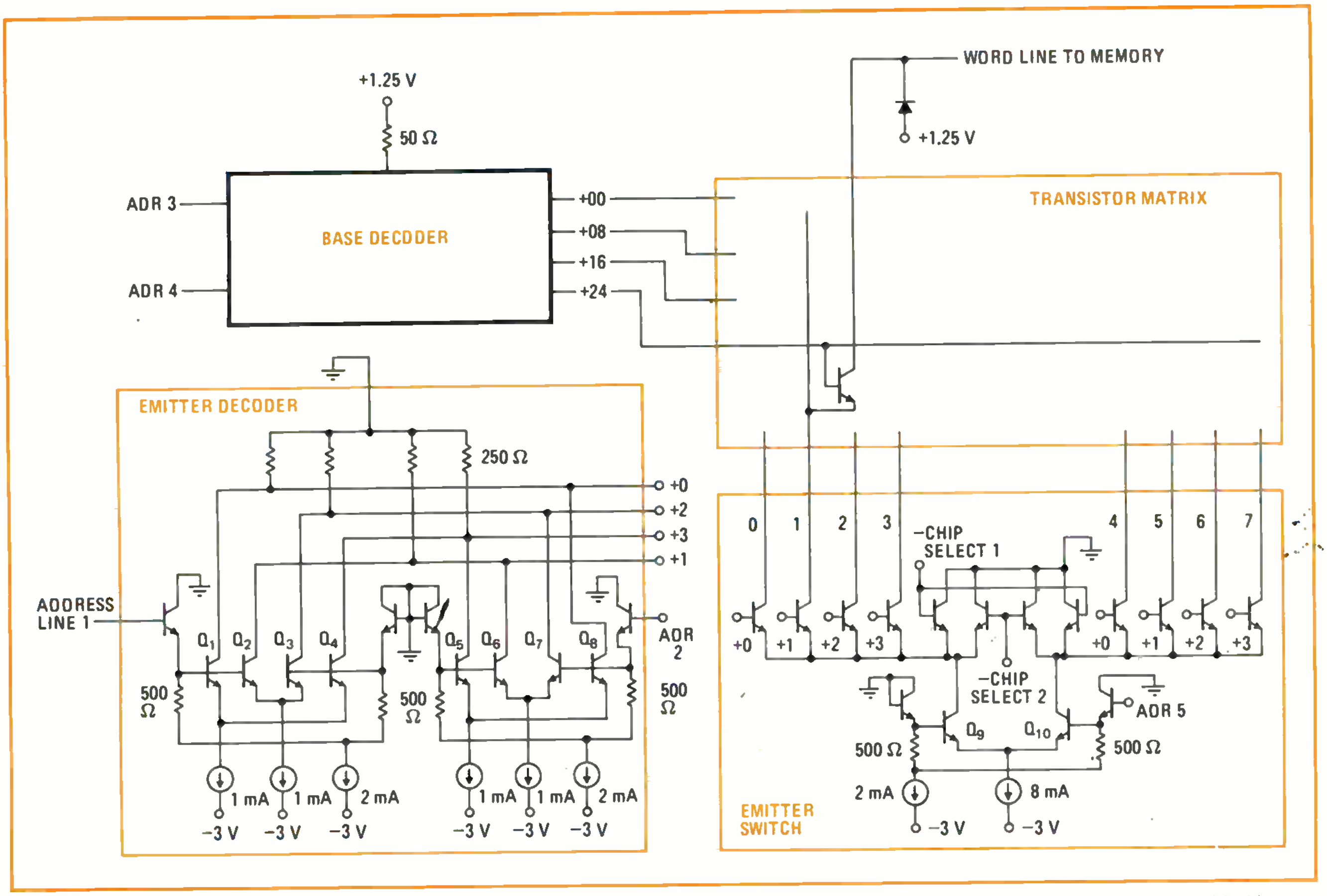
The access time over the path that goes from the chip-select inputs through the power gate and decoder matrices to the data I/O circuit is typically 20 nanoseconds, and cycle time is 50 ns. These two figures could be reduced to 12 ns and 40 ns, respectively, if the power gate circuits remained on continuously. (This would be done by disconnecting the –3(P)V terminal in the power gate circuit, shown later in Fig. 5.)

Chip standby power is 58 milliwatts, and, while the chip is selected, power is 425 mW. This power, however, is reduced because of the duty cycle and is distributed among the chips of a large matrix, so that the average chip power is close to the standby value.

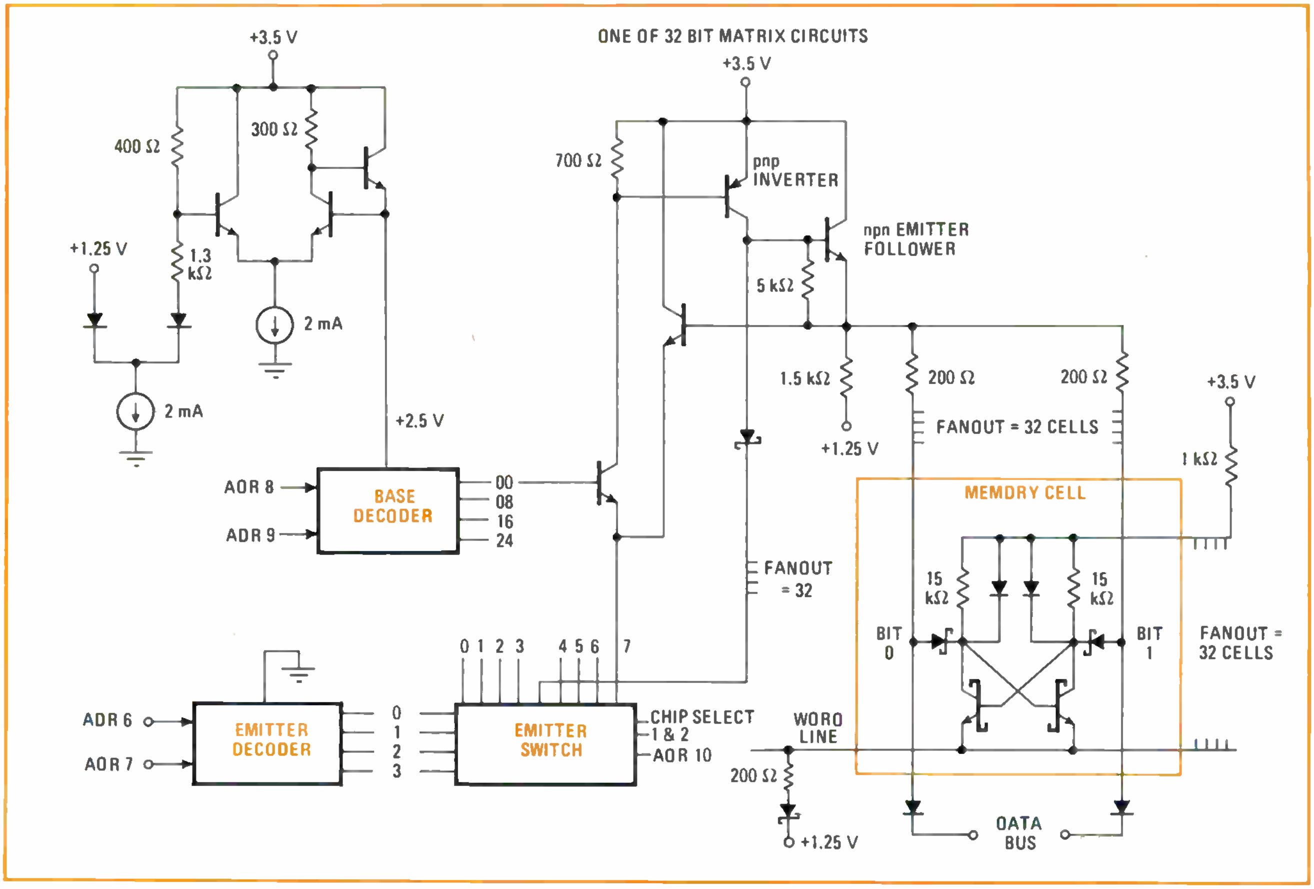
To understand how the circuit operates, take the example of an address input of all logic 0s. Logic 0s are negative voltages of about 400 mV (logic 1 is +400 mV).

First, consider the word-drive system (Fig. 2). This system comprises an emitter switch that decodes the fifth bit of the address code (ADR 5), an emitter decoder, which decodes ADR 1 and ADR 2, a base decoder similar to the emitter decoder, but which decodes ADR 3 and ADR 4, and a transistor matrix, which finally steers the current to the proper word line.

In the emitter decoder, a negative input at ADR 1 causes the input transistor to turn off and thus turns off transistors Q_1 and Q_2, too. Transistors Q_3 and Q_4, however, turn on since their corresponding input transistor has its input grounded. The two transistors thus draw 1 mA each through their respective 250-ohm load resistors, which are connected to output lines +2 and +3. Likewise, ADR 2 causes Q_5 and Q_6 to conduct, drawing 1 mA through the resistors for lines +1 and +3. Thus,



2. Word drive system. Negative and positive inputs on the address lines (ADR) switch transistors on or off, steering current provided by current reference circuits through the emitter switch (as determined by the emitter decoder output) and through the transistor matrix (as determined by the base decoder output) to one of 32 word lines. Nonselected matrix transistors need no power.

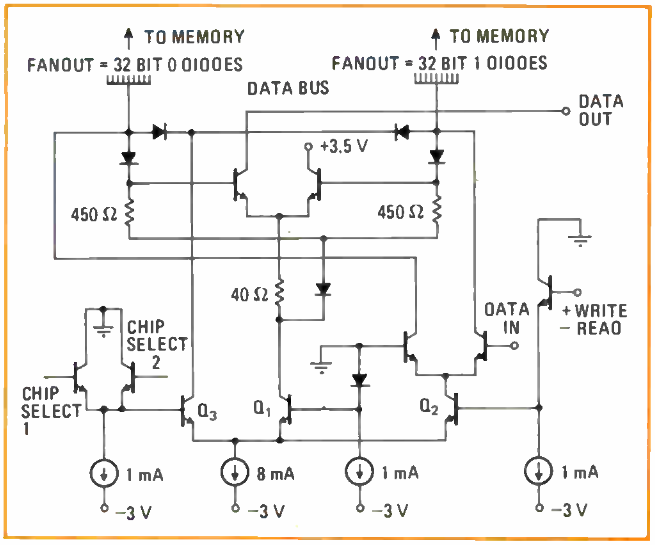


3. Bit drive and memory cell. The word and bit drive systems are similar, except the latter requires an inverter to provide a positive output, plus an emitter-follower to shorten the delay thus introduced. In the memory cell, Schottky diodes (not shown) clamp the collector junctions of the flip-flop cells to improve writing speed.

the selected output, line +0, has no current and is at ground voltage, lines +1 and +2 have 1 mA and are at -250 mv, and line +3 has 2 mA and is at -500 mv.

In the same way, ADR 3 and ADR 4 cause the base decoder output line +00 to be at ground voltage.

In the emitter switch, with ADR 5 negative, the 8-mA current is steered through Q_9 to the left-hand side of the



4. Data input and output. Negative voltage applied to +write/-read terminal governs read operation, steering current to the data out line. Positive voltage at terminal governs write operation.

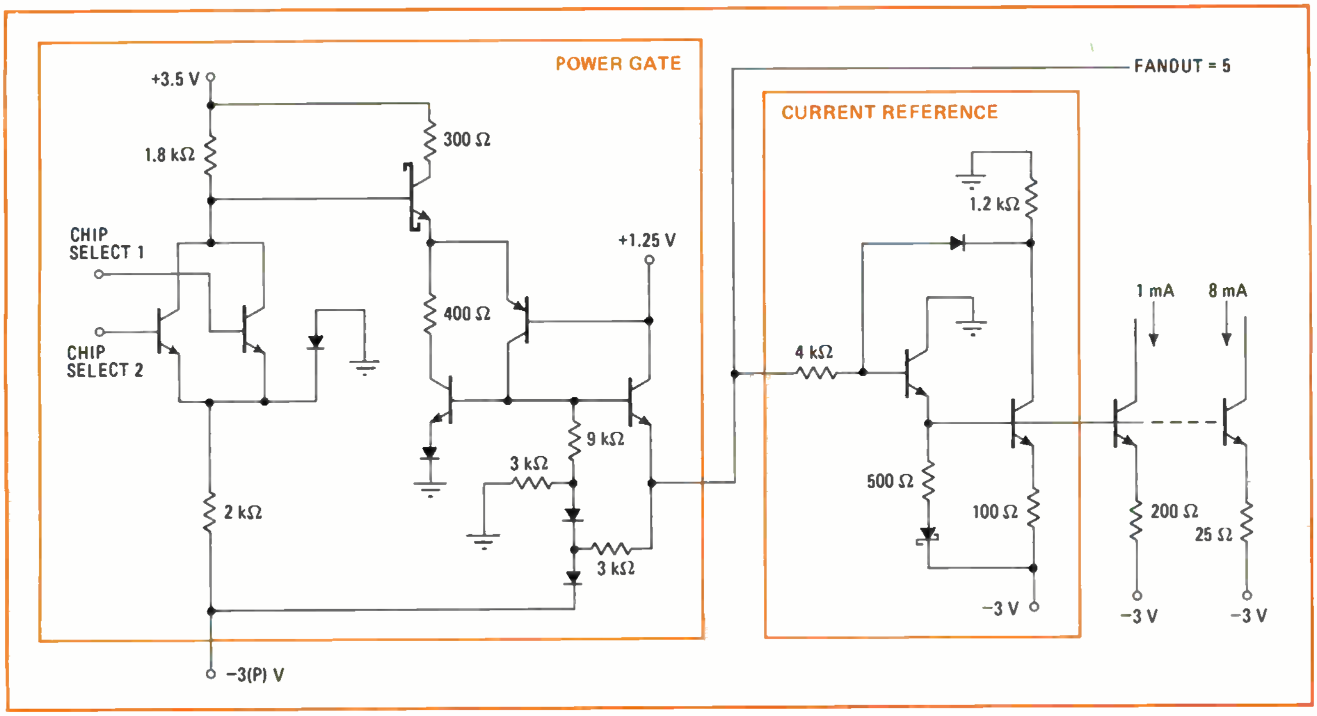
switch. Because emitter decoder line +0 is at ground, the current is next steered through the line's corresponding transistor and up into the transistor matrix, where it is connected to the bases of four transistors. Base decoder output +00 then lets it turn on only one of the four transistors, which steers the current to the selected word line. (Note that in the transistor matrix, all drive power is concentrated in the selected word, while unselected words require no off-bias.)

The bit drive system, similar to the word drive system, decodes address bits 6 through 10 (Fig. 3). However, before the decoded negative output pulse is applied to the bit line, it must be inverted by a lateral pnp transistor, since a positive output is necessary.

A slightly different bit drive

This extra stage is also needed to provide a delay between the word and bit line pulse to ensure stability of the storage latch—if the bit line became positive simultaneously with the word line, the cell could be induced to switch prematurely. However, the pnp transistor, a low-current device, is overdriven and made to drive the bit lines through an npn emitter follower, so that the turn-on delay provided is actually extremely short.

One additional transistor provides feedback to remove the current from the bit decoder's matrix transistor when the bit drive output voltage reaches its desired value. This reduces the pnp collector current at the trailing edge of the chip selection pulse. In order to provide



5. Pulse-power circuits. Power gate circuit, turned on by simultaneous occurrence of two logic level selection pulses, drives current reference circuits for rest of memory. If the −3(P)V terminal is left unconnected, access and cycle times are reduced.

further drive to the off state at the end of the chip selection pulse, the current in the bit emitter switch is diode "OR-ed" to all pnp collectors. The point at which the feedback transistor turns on is set by the bit base decoder's reference voltage of +2.5 V.

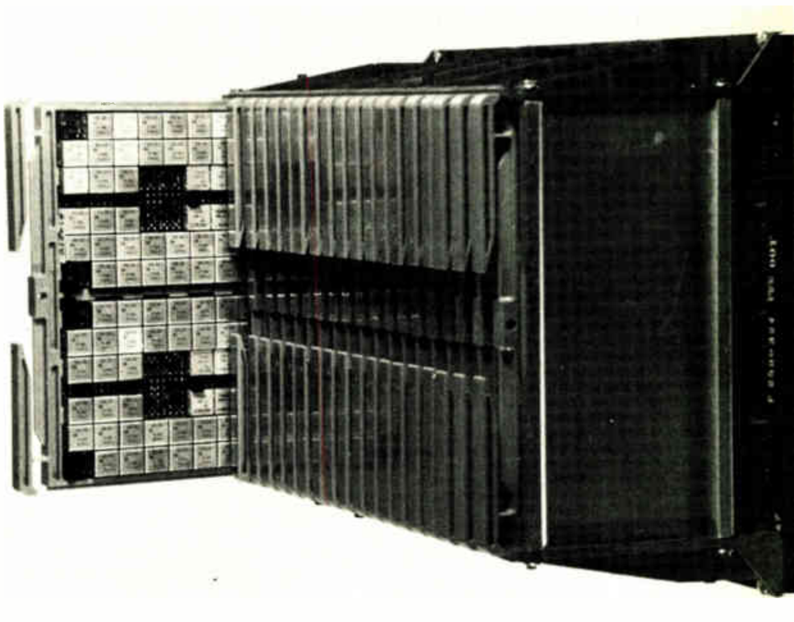
The memory cell (Fig. 3) is a diode-gated flip-flop with 15-kilohm load resistors (the pinch resistors described in the March 7 article). In the standby condition, each cell draws about 20 microamperes from the 3.5-V supply through the conducting half of the flip-flop and then through the 200-ohm resistor connected from the word line through a diode to the +1.25-V supply. The offset voltage between the conducting and nonconducting halves thus is about 300 mV, and standby power is about 45 microwatts.

The flip-flop transistors are shown as "Schottky" transistors since they have Schottky diodes (not shown) clamping the collector-base junctions out of saturation. Once a cell is selected by the negative 8-mA pulse on the word line and the positive pulse on the bit line, the information appears as a differential voltage across the bit output lines and, through the two diodes, on the data bus.

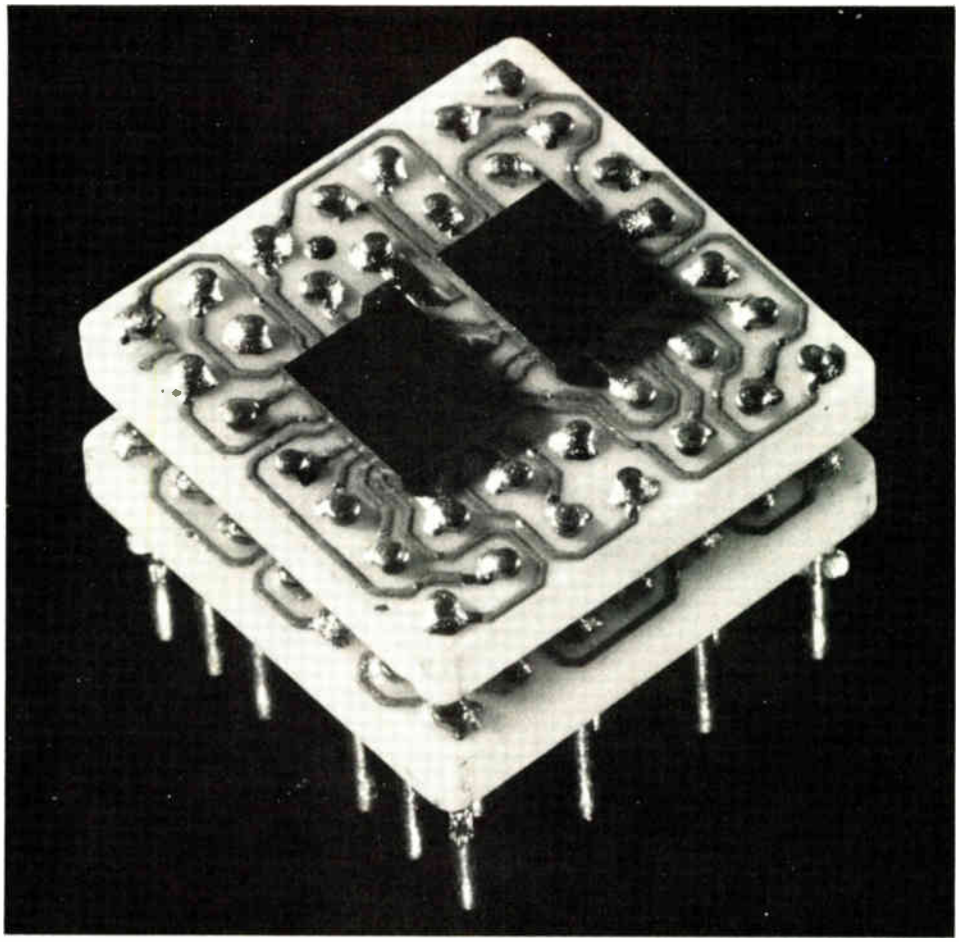
When the bit lines go positive, both Schottky coupling diodes turn on. If, for example, the right-hand transistor is conducting, its collector would be about 400 mV lower than the other collector, making the bit 0 line more positive than the bit 1 line. Since the Schottky diodes are conducting at about the same currents, they have about the same voltage drops, so that the differential voltage is also about the same as the voltage difference across the internal cell collector nodes.

In the data I/O circuit (Fig. 4), during a read operation, a negative voltage is applied at the +write/−read terminal. With the chip-select inputs negative, the 8-mA current source flows through transistor Q_1 and divides between the 40-ohm resistor and the diode—6 mA through the resistor and 2 mA through the diode. The OR diodes that connect to the bit lines and the translation diodes are biased on by the 2-mA current. The 6-mA current flows to the "data out" pad or to the 3-V supply, depending on the stored data.

For a write operation, the +write line is positive, causing the 8-mA current to flow through Q_2. If the "data in" line is negative (to write in a logic 0), the 8-mA current is further steered through the left-hand ("data-in") current switch transistor to hold the bit 0



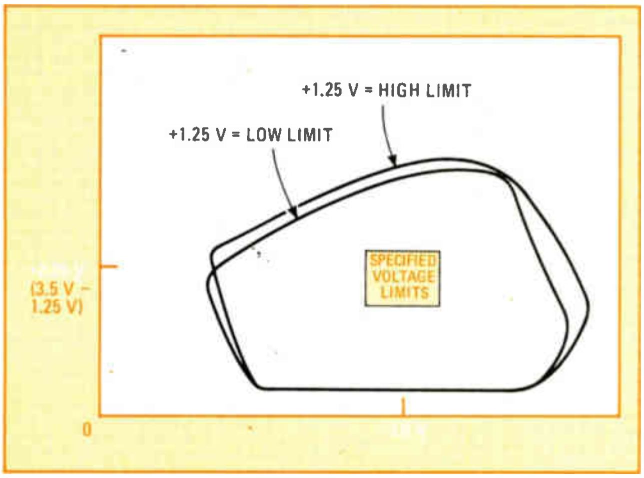
6. Rack-up. Memory modules mount cards which plug into a board 13 inches wide (holding 36 cards). Each card contains 128-k bits; total capacity is about 0.5 megabyte (a byte is nine bits).



7. Double-decker. Two ½-inch-square ceramic substrates each hold two 1-k RAM chips, to make the four-chip module used in IBM's System/370 and System/7 computers.

line negative before the cell is selected. When the bit line goes positive, only the memory cell's right-hand Schottky diode will conduct, pulling up the collector of the left-hand transistor, turning the right-hand transistor off and turning on the left-hand transistor. Bit line recovery is provided through Q_3 when the chip-select line goes positive at the end of the chip-selection pulse.

All the current reference circuits, which provide the many current sources used on the chip, are driven by the power-gate circuit (Fig. 5). This circuit turns on with the coincidence of two logic level selection pulses. For voltage translation, the power gate also uses a lateral pnp transistor that here, too, is driven on hard and has its turn off hastened by feedback.



8. Wide margins. The "Shmoo" plot for a 128-kilobit memory card shows significant range between the specified limits on the three power-supply voltages (−3 V, +2.25 V, and +1.25 V) and the edge of the plot, which represents the limit of proper memory operation.

The big picture

Large memories are built using a 3.25-by-4.5-inch card (Fig. 6) that contains 128 kilobits of storage as a basic building block. Every card is populated with 32 four-chip modules (Fig. 7), plus 10 single-layer modules for buffering, decoding, and sensing. A board containing 36 such cards can package up to 0.5 megabytes of storage (a byte is nine bits). The boards, which are 13 inches wide, 8 in. high, and 6 in. deep for a density of 7,562 bits per cubic inch, can be stacked vertically and cooled by forced convection.

The memory will operate over a wide range of variations in the three power supplies, as shown in the "Shmoo" plot for a 128-kilobit card (Fig. 8). There are wide margins between the specified tolerances on the power-supply voltages and the edges of the plot. This means that chips with defects, which fail near the voltage specification limits and are likely to fail in the field, can be screened out without any testing loss of chips that are defect-free. □

ACKNOWLEDGMENT

The author is indebted to IBM's Adolf Zehle and Joseph Maslack for the chip layout; Roy Flaker for the cell analysis; Robert McMahan and Paul Zerr for the peripheral circuit analysis; Paul Steiner for management of the design into manufacturing; and Siegfried Wiedmann for early work on the pinch resistor.

Measuring the access time of bipolar read-only memories

by Joseph J. McDowell
Monolithic Memories Inc., Sunnyvale, Calif.

The access time of a semiconductor memory, particularly that of a bipolar read-only memory, can be difficult and time-consuming to measure. But here's a tester that makes this measurement quickly and does not require the data pattern stored in the ROM to be known. There is one condition, however. The ROM must be tested first for its dc parameters.

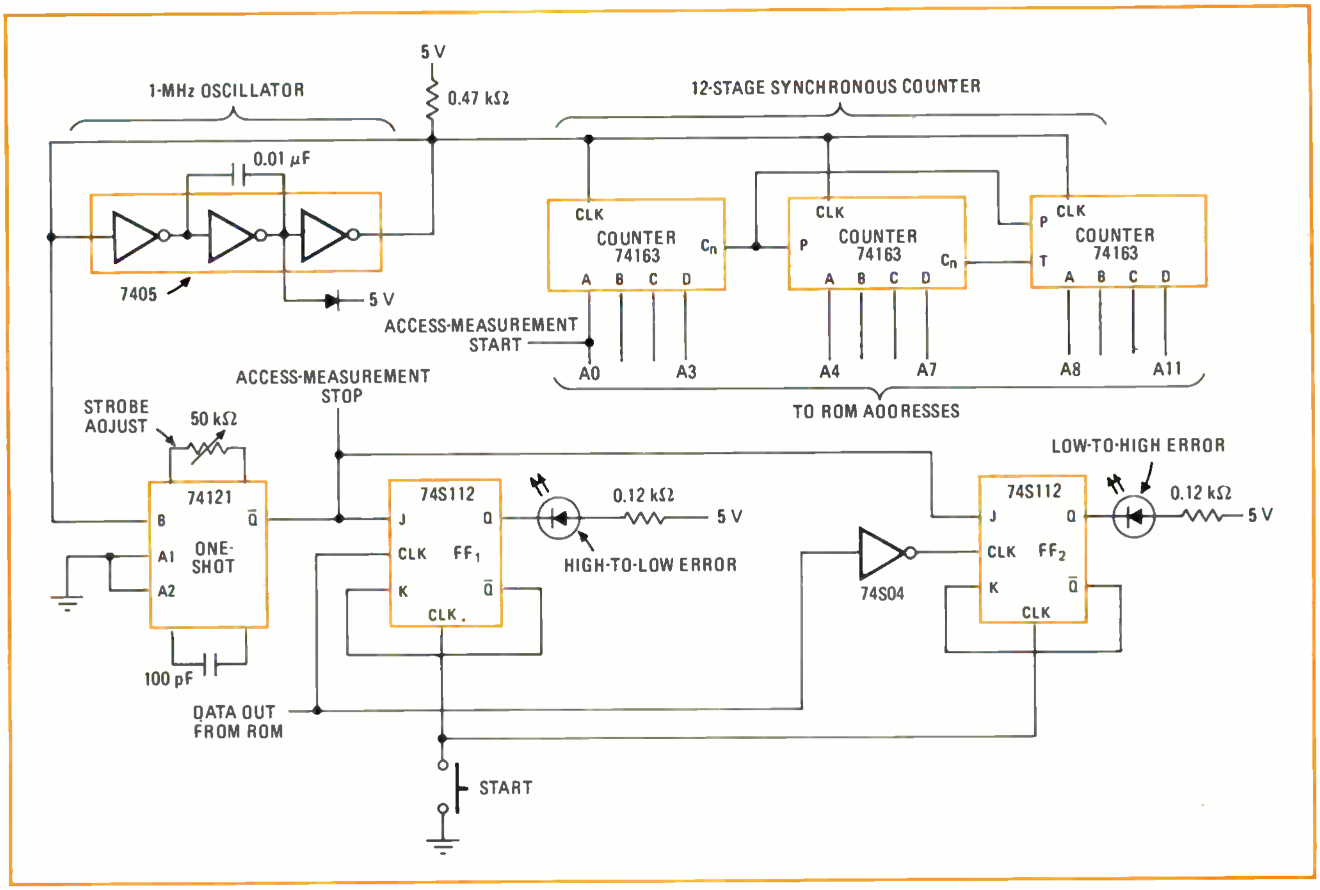
Memory access time is considered to be the maximum address-to-output delay from any address to any output. For bipolar ROMs, access time typically ranges from 30 to 150 nanoseconds, and storage capacities can be as large as 8,192 bits. Conventional testing techniques require a single-shot time-interval measurement for each bit, since each address and output of the ROM generally has a different delay time. The maximum delay measured in this way is recorded as the access time.

Single-shot time-interval measurements, however, have two major drawbacks. Each reading requires about a millisecond, which can add up if the memory is a large one. And the Schmitt-trigger discriminators, which are used to establish the start and stop times, rely on a specific transition direction (either high to low or low to high) through a voltage threshold to implement the start or stop.

This last condition is a problem because the transition direction cannot be predicted for a ROM, unless the data pattern in the ROM is stored in a random-access memory. The problem then becomes one of finding a RAM that is as large and as fast as the ROM being tested to tell the measurement system what to expect. Even if such a RAM can be found, spikes can appear prior to the access time and can trigger the discriminators.

Another measurement technique is to compare the ROM with a RAM that is loaded with ROM data. But again, there is the problem of finding a RAM as fast as the ROM to be tested.

The tester in the figure uses a totally different ap-



Time-saving tester. This circuit checks out the access time of a bipolar read-only memory by regarding any transition occurring at the memory output after the allowable access time as an error. The counter string changes all of the ROM's addresses at the same time. The one-shot acts as a strobe whose timing cycle is set to the allowable access time. A pair of Schottky-TTL flip-flops monitors each ROM output line. If a high-to-low transition error occurs, FF_1 lights its LED; if a low-to-high transition error occurs, FF_2 lights its LED.

proach. It looks for transitions after the expected access time, and defines any transition from this access time until the next address change as an error. This method takes advantage of the fact that the memory reaches a steady-state value before the access time, and the data outputs should not change again until the address is changed. Although the data pattern stored in the ROM does not have to be known, the unit must first be checked for dc parameters, since a package without a chip inside will pass the test.

In the test circuit, 4-bit totally synchronous counters are used to count through all the addresses of the ROM, guaranteeing that all the addresses change at the same time. These address transitions define the start of the access measurement. The counters are driven by a 1-megahertz oscillator, which is constructed with logic inverters. Two Schottky-TTL J-K flip-flops are employed to look for transitions after the access time—FF_1 looks for high-to-low transitions, while FF_2 looks for low-to-high transitions.

The one-shot stops the flip-flops from watching for transitions prior to the access time by holding each one's J input low until the access time is reached. This prevents the flip-flops from changing state. They remain in their initially cleared condition, with their Q outputs low and their $\bar{Q}$ outputs high.

After the one-shot completes it timing cycle, the J input of each flip-flop goes high. If a high-to-low transition now occurs on the memory output line, flip-flop FF_1 changes state—its $\bar{Q}$ output goes low, and its Q output goes high, turning on the error-indicating light-emitting diode. The flip-flop, and therefore the error, remain latched because the unit's $\bar{Q}$ output is tied to its K input. (Depressing the START button will clear the error.)

Flip-flop FF^2 operates identically, but turns on its error-indicating LED for a high-to-low transition on the memory output line. This scheme can be expanded to monitor n memory outputs by adding 2n flip-flops to the test circuit. (A pair of flip-flops is required for each memory output.)

The tester can be calibrated by attaching a pulse generator or delay line of known duration between the access-measurement start and stop inputs to the circuit. This simulates the memory access time, so that the one-shot strobe can be adjusted until a failure just occurs for a set GO/NO-GO limit. The tester can accurately measure an access time to within an accuracy of ±4 ns. □

Eliminating stray signals in remotely gain-switched op amps

by Ernest J. Kacher & Forrest Fox
The Methodist Hospital, Texas Medical Center, Houston, Texas

When the gain switch for a variable-gain amplifier is physically distant from the amplifier itself, stray signal pickup and/or capacitance loading can affect circuit performance. A special switching arrangement, however, can eliminate both of these problems.

The circuits drawn in (a) show how cable capacitance can be introduced at the amplifier's input. While the circuits of (b) show where noise generators appear when the amplifier input leads remain open. (In all these circuits, the amplifier is connected in its non-inverting mode.)

In contrast, the switching arrangement illustrated in (c) has no current paths through unused resistors, and it eliminates switching at the amplifier input. All of the resistors are used with each gain configuration, and all of the lines to the switch are always connected either directly to signal ground or to the low-impedance output of the amplifier.

The maximum allowable cable capacitance, therefore, is now determined by the capacitance load that the amplifier can tolerate, rather than the signal phase shift. Another advantage of this switching arrangement is that the circuit's bias-current compensation remains optimum for each gain, as long as the correct value is selected for resistor R_0.

To make use of this type of switching, the resistors required, as well as the right switching arrangement, must be determined for the specific set of desired gains: G_0, $G_1, \ldots, G_n$. First, arrange the gains in ascending order according to magnitude (so that G_i is less than G_{i+1}), but let $G_0 = 1$ and $G_{n+1} = \infty$. Since there will be n + 1 resistors required, they should be designated as R_1, $R_2, \ldots, R_{n+1}$. Compute the values of resistors R_2 through R_{n+1} sequentially, in terms of resistor R_1:

$$R_{i+1} = \frac{G_{i+1}(G_i - G_{i-1})R_i}{G_{i-1}(G_{i+1} - G_i)}$$

where i varies between 1 and n.

Next, arrange the switch so that, starting with the minimum gain of G_0, all the resistors connect from the amplifier's inverting input to the output. To obtain gain G_1, switch the end of R_1 from the output to ground, leaving everything else unchanged. To obtain gain G_2, switch the end of R_2 from the output to ground, leaving everything else unchanged. In general, then, to obtain gain G_i, resistors R_1 through R_i are connected to ground, and resistors R_{i+1} through R_{n+1} are connected to the output.

This same switching technique can be used for an inverting amplifier configuration. However, gain G_0 must be set equal to zero, and the values for resistors R_2 through R_{n+1} are found sequentially in terms of resistor R_1 from:

$$R_{i+1} = \frac{(G_{i+1} + 1)(G_i - G_{i-1})R_i}{(G_{i-1} + 1)(G_{i+1} - G_i)}$$

where i again varies between 1 and n.

Resistor R_0 can be computed as the parallel combination of all the gain resistors, R_1 through R_{n+1}. Or, for the non-inverting amplifier, it can be determined by:

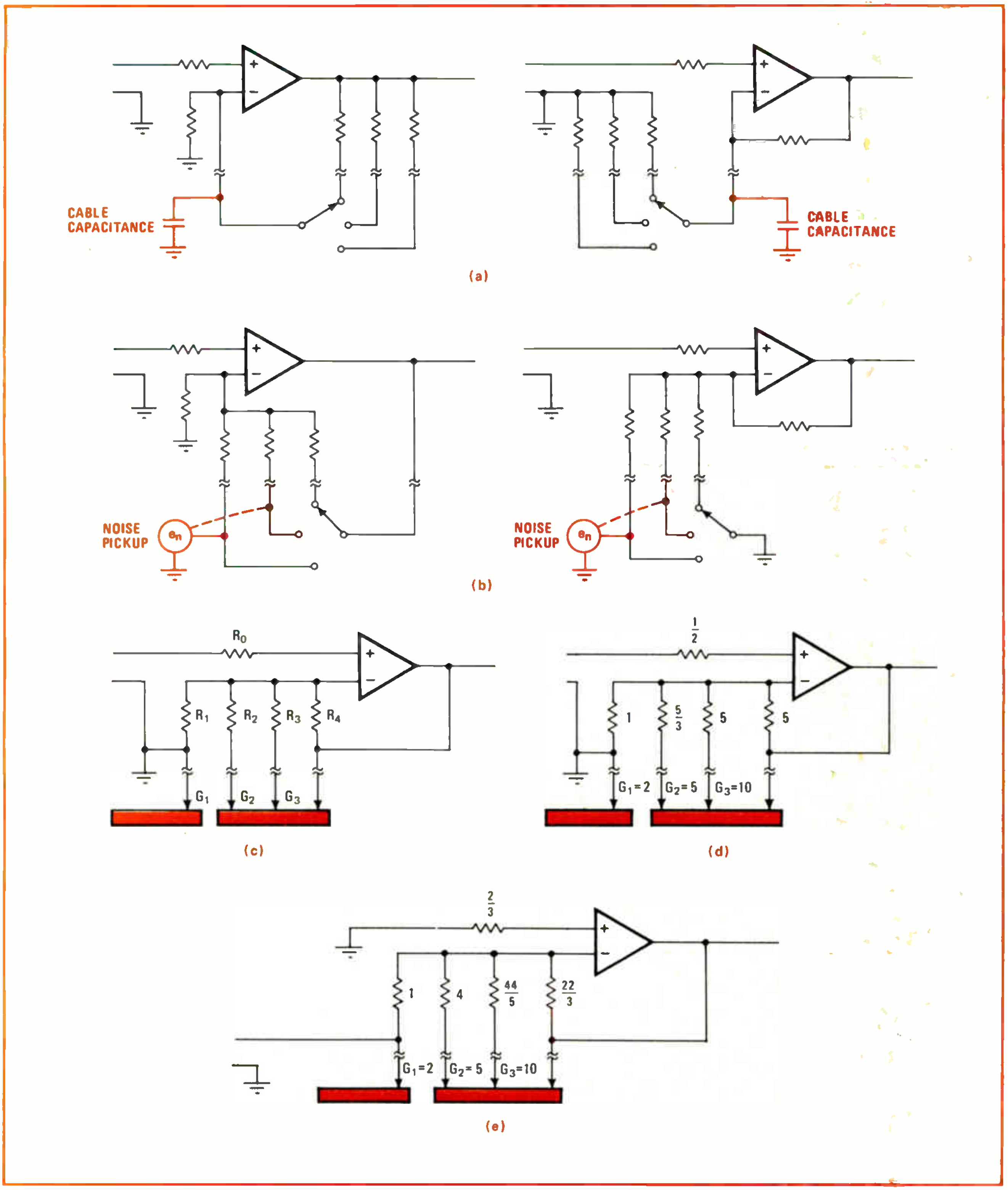
$$R_0 = [(G_1 - 1)/G_1]R_1$$

And for the inverting amplifier, the value of R_0 is:

$$R_0 = [G_1/(G_1 + 1)]R_1$$

Circuits (d) and (e) give the resistor values for producing gains of 2, 5, and 10 when $R_1 = 1$. Amplifier (d) is noninverting, while amplifier (e) is inverting. □

Engineer's notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.



Switched-gain amplifiers. Remotely switched variable-gain amplifiers can suffer from the capacitance loading (a) of long wires or can pick up noise (b) through unused resistor paths. The switching arrangement of (c) doesn't have these problems because all of the switched points have low-impedance paths to ground. The noninverting (d) and inverting (e) amplifiers given here provide gains of 2, 5, and 10.

Engineer's newsletter

Save power by using switching regulators . . .

Here's a great but simple power-saving idea: **switch to switching regulators.** Robert J. McCue, marketing manager for Sorensen Power Supplies, Manchester, N.H., points out that switching regulators are about three times more efficient than their series-pass counterparts. **A 5-volt, 50-ampere ac-to-dc power supply that uses series-pass regulation will dissipate over 500 watts, while the equivalent switching regulator will dissipate about 135 W.**

McCue estimates that the about 40,000 series-pass modular power supplies sold in the U.S. annually dissipate 250 W on average or about 10 million watts altogether. Assuming a seven-year life, and allowing for demand growth, approximately 200,000 series-pass devices must be dissipating 50 million watts. Assuming again an on-time average of 10 hours a day in a 240-day year, the total **wasted on useless heat in a year is 120,000 kilowatt-hours. Conversion to switching regulators would save two thirds of this energy.**

. . . and checking out square-wave generators

Users of dc-to-ac inverters who pay for good, low-distortion sine waves when they don't really need them waste power as well as dollars. According to J. L. Harris of Wilmore Electronics, Durham, N. C., who should know because his company makes both sine- and square-wave generators, a cheaper and more efficient square-wave generator is often enough. **Typical sine-wave inverters in the power range of a few hundred watts are 60% to 70% efficient at best. Comparable square-wave inverters have efficiencies in the range of 85% to 90%.** Price differences are even more dramatic—a typical 500-watt sine-wave inverter costs about $900, but an equivalent square-wave is about $200.

Zener diodes can give you fast protection

Zener diodes, the widely used protection devices, are **just no good for applications involving fast pulses because of their high junction capacitances,** which can easily get into the thousands of picofarads. But you can reduce a zener's capacitance, improve its response, and retain its limiting function, if you **put an ordinary signal diode in series with it.** The signal diode should have its junction oriented in the opposite direction to that of the zener, as if you were using it to thermally compensate the zener. **The very small capacitance of the signal diode in series with the zener will reduce the total capacitance by about two orders of magnitude,** down to around 10 pF.

Get with those microprocessors

Feeling lost trying to apply the new microprocessors to your system design specs? Another series of **seminars on microprocessors is to be held this spring in Atlanta, Boston, New York, Philadelphia, and Washington.** These last from one to three days and cover introductory material on both hardware and software, programing, and system design and applications, specifically with reference to Intel's MCS-4, MCS-8, and 8080, and National Semiconductor's IMP-8, IMP-16, and GPC/P. **Fees are $125 to $350,** depending on the material covered and the length of the seminar. Contact Microcomputer Technique Inc., 11227 Handlebar Road, Reston, Va. 22091, or call (703) 620-9676.

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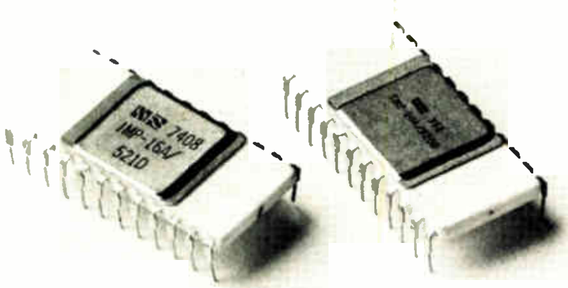
National's building blocks are the Register and Arithmetic Logic Unit (RALU) and Control and Read-Only Memory (CROM). Together they contain all the gates and flops you used to have to wire together to build your own processor.

The thing that does the work.

RALU.

A 4-bit slice of the Register and Arithmetic portion of a general purpose computer.

In one 24-pin package using standard +5V and −12V supplies



we've crammed all of the following: seven general-purpose registers, a status flag register, an arithmetic logic unit, an I/O multiplexer, and a 16-word LIFO stack that improves speed and performance while conserving main memory. The RALU number is IMP-00H/520D.

The thing that tells the other things what work to do.

The only trouble with RALUs is that they don't understand English. Or even the zeros and ones that you feed into the microprocessor.

CROMs do understand zeros and ones.

They're souped-up ROMs that translate your binary instructions into operational commands. A single instruction to the CROM triggers a series of commands to the RALUs.

CROMs are currently available in three varieties:

A standard-instruction 16-bit CROM, IMP-16A/521D, with 43 instructions.

An extended-instruction 16-bit CROM, IMP-16A/522D, that speeds up processing with 17 additional powerful instructions including divide, multiply, double precision add/subtract, etc.

And an 8-bit CROM, IMP-8A/520D with 38 instructions.

You can buy the RALUs and CROMs in these set numbers: IMP-16A/500D: 16-bit standard set; IMP-16A/502D: 16-bit extended set; IMP-8A/500D: 8-bit standard set.

THE CARDS

For people who want to save time, National offers its "ready-mades."

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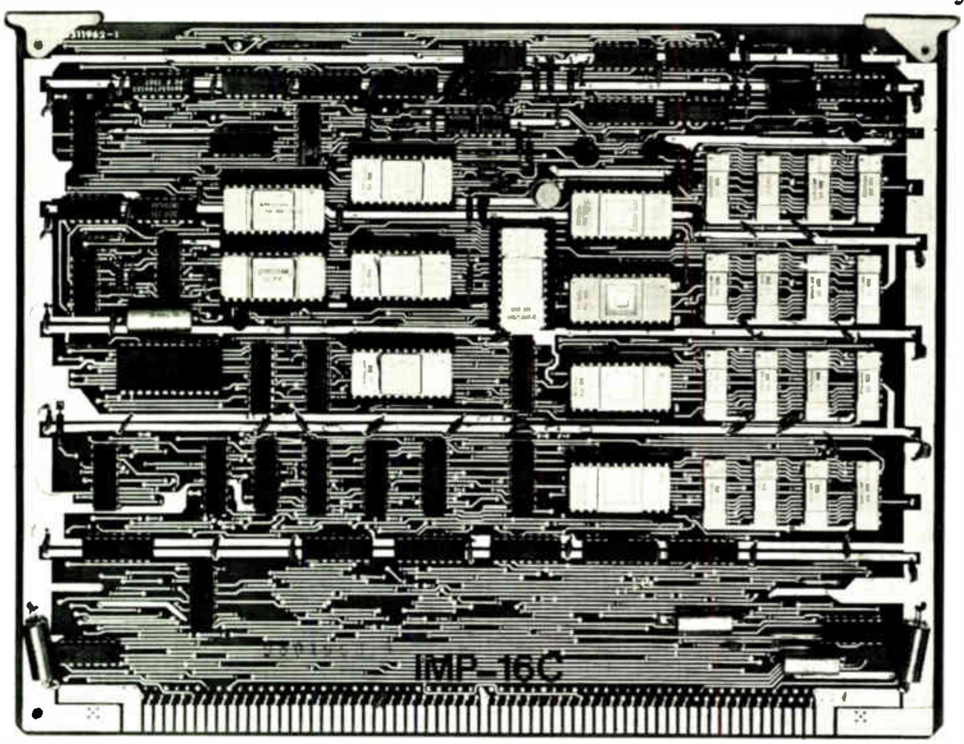
Our big ones.

The IMP-16C is a 16-bit microprocessor built around four RALUs and one or two CROMs.

The one-CROM version has a standard-instruction-set CROM and an empty socket for another (IMP-16C/200). Add the extended instruction-set CROM and you've got the IMP-16C/300.



The IMP-16L/300 card is similar to the 16C/300, but we optimized it for high performance applications with a Direct Memory Access bus controller and multi-level interrupts.

Our little one.

IMP-8C, 8-bit microprocessor.

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If 8-bits is your thing, you'll find some things here to turn you on: 8 addressable control flags—control jump multiplexer provides 16 programmable branch conditions. Eight-bit buffered-data-out bus. Memory addresses 16 bits wide to provide a memory address range of 65,536 bytes. On-card memory expandable to 2304 bytes, consisting of 256 bytes of read/write memory and up to 2048 bytes of read-only memory (ROM/pROM).

But whether you go for 8-bit or 16-bit, cards or chips, the question is, what are you going to do with them once you've got 'em?

Please turn the page.

THE BOXES

The advantages of the whole microprocessor thing lies in the fact that it is standard hardware designed and built for you to *program* to your specific application.

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They're program debugging and prototyping systems, providing everything you need to develop and test both the interfaces and application programs.

Each box includes a microprocessor card, programmers control panel, peripheral interfaces, memory, power supply and chassis.

Box #1

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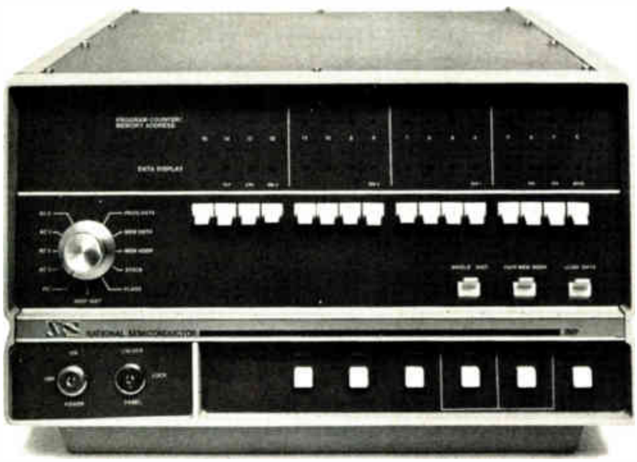
A microcomputer for use with the IMP-16C microprocessor cards. With a Teletype®, the IMP-16P provides all equipment necessary for the immediate evaluation and use of the IMP-16C (both 200 and 300) cards and chips.



Box #2

The IMP-16L.

A prototyping system for the IMP-16L/300 card. (And if you're starting to get confused by all the different numbers, the chart on this page should help unconfuse you.)

The basic IMP-16L and options provide an unusually versatile tool for developing a variety of OEM equipment, software, and full-scale processing systems.

Box #3

The IMP-8P.

For 8-bit fans this is the prototyping tool for the IMP-8C card. Like the others, IMP-8P puts all you need for hardware and software development all in one box.

What goes with what.

	CROM Types:	# of RALUs	Cards:	Boxes:
standard 16-bit	IMP-16A/521D	4	IMP-16C/200	IMP-16P/204
extended 16-bit	IMP-16A/521D IMP-16A/522D	4	IMP-16C/300	IMP-16P/304
extended 16-bit with DMA	IMP-16A/521D IMP-16A/522D	4	IMP-16L/300	IMP-16L/304
8-bit	IMP-8A/520D	2	IMP-8C/200	IMP-8P/208

So that's our basic hardware. Our boxes, our cards, and our chips. But we're not quite through yet...

THE WORKS

National wouldn't leave you out on a limb. We support our hardware with software, firmware, and accessories that help make the whole thing easier to apply.

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Expanding marketplace augurs well for 1974 National Computer Conference

Technical sessions to cover a broad range of technology and applications for users, as well as the EDP industry

by Alfred I. Rosenblatt, *New York bureau manager*

☐ With both computer technology and applications sharing the spotlight, the technical program at next week's National Computer Conference in Chicago offers a record number of 119 sessions. That figure reflects the move of information processing into a host of newer businesses, such as data communications, point-of-sale systems, and computer networks.

As it did last year in New York, the NCC management is trying, especially through its technical program, to attract the "so-called non-computer professional who, because of his data requirements, actually winds up as the eventual computer user," explains Thomas C. White, director of communications for the sponsor, the American Federation of Information Processing Societies. "Appealing to the data-processing manager alone, as the Afips conferences did in the past, is just tunnel vision," he adds.

Accordingly, the program is divided into 10 major industry and business categories and five areas of computer science and technology. These represent, says general chairman, Stephen S. Yau, chairman of the Computer Sciences department at Northwestern University, "the most comprehensive analysis ever undertaken of the U.S. data-processing field."

The industry categories include communications and data-network systems, health care and biotechnology, education, manufacturing, retailing and distribution, government, finance, industrial-process control, and transportation. The science and technology areas deal with architecture and hardware, software systems, computer networking, and information-management systems.

And, finally, six special sessions will cover topics of general interest to computer professionals. Included is a review of computers and personal privacy, a three-part session marking the 10th anniversary of the inauguration of the computer time-sharing system at Dartmouth College, an overview of energy in an "evolving society," plus discussion of computer communications in a regulatory environment, computer development and applications outside of the United States, and computing and mathematics in society.

As in past years at Afips conferences, computer design and technology will receive major attention. Eleven sessions from next Monday through Thursday will deal with various aspects of computer hardware and architecture. All are aimed at either updating some of the most recent work or looking into what the future may bring.

In recognition of the number of large-scale data-processing installations and mass-memory systems increasing throughout the country, two sessions are devoted to discussing how the systems are designed and have been operating. The session on "Mass Memories" reviews the technologies, architecture, and software used in several representative systems. Speakers include spokesmen from such manufacturers of mass memories as IBM Corp., Control Data Corp., and Ampex Corp. An overview of the field will be presented by a speaker from an important user of the systems, the Department of Defense.

Large-scale systems to be discussed

The experience gained in operating several new jumbo computers delivered within the past year will be detailed in "Operating Status of Large-Scale Data Processors." Included will be discussions of the Control Data Star systems and the Advanced Scientific Computer from Texas Instruments Inc.

Trying to stimulate wider thinking about the possibilities of its application, "Associative Processing" examines the basic aspects of parallel processing, which, although it has been available for years and promised great increases in processing speed, has had but limited applications. Included are papers describing software, rather than hardware, methods for improving the speed of Goodyear Aerospace Corp.'s Staran processor, plus the possibilities of applying associative processing to the problems of air-traffic control, information retrieval, and ballistic-missile defense.

A number of papers will describe progress in both new magnetic and semiconductor memory designs in "Advances in Memory Technology." The status of magnetic bubbles, domain-tip propagation, charge-coupled devices, and metal-nitride-oxide semiconductors will be described by speakers for some of their principal developers, including IBM, Cambridge Memories Inc., RCA Corp., and Westinghouse Electric Corp. In particular, the speakers will tackle the question of how these new technological alternatives can be matched to the requirements of current and evolving systems.

Communications and computers

Using speech to communicate with computers could eventually be the ultimate form of programing; it would certainly be the easiest. A couple of papers, as well as a panel discussion, will look at some recent progress during the session, "Computers in Communications and Voice Recognition." Leon D. Wald, of Honeywell Information Systems, will describe how he's applied associative-processing techniques for recognizing words in real time, and Rein Turn of the Rand Corp. will deal with several experiments he's made in voice recognition.

As computer-based processing and communications systems proliferate, how to design the input/output terminals becomes a key issue. A panel discussion "Intelligent Terminals—Rationale and Implications" examines the bases for deciding how much intelligence should be designed into terminals, including such information as which processing and computation functions should be performed in the terminal and which in the central processor, the system software required to allocate tasks between terminal and processor, and kinds of peripheral equipment that should be used with the terminal.

Advancing technology in the form of a proliferation of compact, low-cost microprocessors and memories is also having an effect on interactive graphics systems, which will be discussed in "The Effect of Changing Technology on Computer Graphic Systems," while "Display Processing and Technology" examines, not only text and graphic display, but also the entry of such material into time-sharing systems.

As computer usage expands, one of the fastest technologies combines data communications with computer networking, to which two separate groups of sessions are devoted. Communications is the subject of six sessions, and one, "Mini- and Micro-computers in Data Communications Systems," also highlights the impact of the new developments in semiconductor technology applied to such chores as store-and-for-

Showtime. Exhibitors will be allowed to post prices discreetly at next week's 1974 National Computer Conference, which promises to be the nation's biggest-drawing electronics show this year.

Showman. As the range of people using computer systems broadens, Afips' Thomas C. White tries to attract likely users to NCC, besides the usual computer designers and technologists.

ward buffering, job scheduling, and the handling of input/output devices.

"Planning and Design of Data Communications Networks" presents in five separate papers by Wushow Chou and his colleagues at Network Analysis Corp. an overview of some of the latest techniques. Chou also is the organizer of the communications sessions. And, as a number of different companies are getting set to launch commercial domestic satellites, a panel on "Domestic Satellite Services and Their Impact on Information Processing Networks" will touch on the tradeoffs between terrestrial and satellite options for data-communications users. Another panel will look at the future of the "wired city" during a discussion of "Digital Communications in Cable Systems." Such services as electronic mail, banking, retail marketing, working and earning at home, and surveillance will be included.

With the proliferation of communications systems will also come the burgeoning of both private and public computer networks. "We've only seen the beginning of networking," says the organizer of seven networking sessions, Thomas N. Pyke Jr., of the National Bureau of Standards. "There will be both more and different kinds of networks for computational and information purposes, and more attention will be paid to the user's needs."

One key issue might come in allowing the user to gain access to multiple networks through but a single set of terminal facilities, Pyke points out. And the session, "Standards for Computer Networks," examines the issues involved in establishing standards that would allow this to be done.

Network standards to be considered

Some of the first attempts at evaluating the performance of networks will be discussed in "Network Performance Measurements," including the first public presentation of measurement results on the trend-setting Department of Defense Arpanet, which has more than 40 computers with upwards of 1,000 terminals connected. Pyke points out that the entire networking industry lacks adequate techniques for gauging performance—factors that would allow networks to be compared with each other with respect to internal efficiency and external effectiveness.

Moving from computer science and technology into industrial and business-information processing, the NCC technical program has sessions organized around some of the fastest-growing applications. The largest group of sessions is devoted to point-of-sale (POS) systems.

George E. Buchik of Gimbels Inc. department stores, hopes his session, "Impact of POS on Data Communications," will educate both a user and manufacturer on the possibilities of POS that may often be ignored. "A lot of manufacturers really don't know what the retailer wants and what he can use his terminal for," Buchik asserts. "And a lot of users think all you have to do is hook a POS terminal into the wall and that's it."

Turning to a field that's just beginning to make waves, "Point-of-sale Systems for Supermarkets" also has a session of its own. The financial community has been allocated five sessions, including the fast-moving "Electronic Funds Transfer and Check Collection Developments." During this session, George C. Mitchell, vice chairman of the board of governors of the Federal Reserve System, will discuss possible future development of a check-processing system.

System requirements for government information-processing at federal, state, and local levels will be delineated. Glen E. Pommerening of the U.S. Department of Justice will lead a panel discussion on the effectiveness of police-oriented systems in "Law Enforcement—do the systems really provide the information and safeguards promised?" And major issues in data security and privacy, topics of increasing nationwide controversy, will be handled at two panels, "Computers and Personal Privacy—a Major Societal Issue," and at "Security, Privacy and the Information Processing System." □

A forecast of 40,000

NCC conference manager Gerard Van Dijk is predicting attendance of 40,000 at next week's National Computer Conference—7,000 more than last year in New York. The 815 booth spaces will cover 81,500 square feet—one entire level of the three-floor McCormick Place in Chicago—and will encompass the computer, peripheral, and systems hardware of 250 companies.

By comparison, the IEEE's Intercon 74 in the New York Coliseum in late March drew fewer than 25,000 and had approximately the same number of exhibitors, but it occupied only 39,000 square feet. However, the booths for the computer shows necessarily require more space to accommodate larger products than the components and instruments that typify Intercon.

The technical program and exhibition take place throughout the five days of the conference, May 6 to 10. Registrations are available either for the total conference plus exhibits or for a day's tour of the exhibits only. Fees range from a high of $60 all the way down to $5. For any last-minute questions, there's a toll-free telephone number, (800) 631-7070. In New Jersey, it's (201) 391-9810.

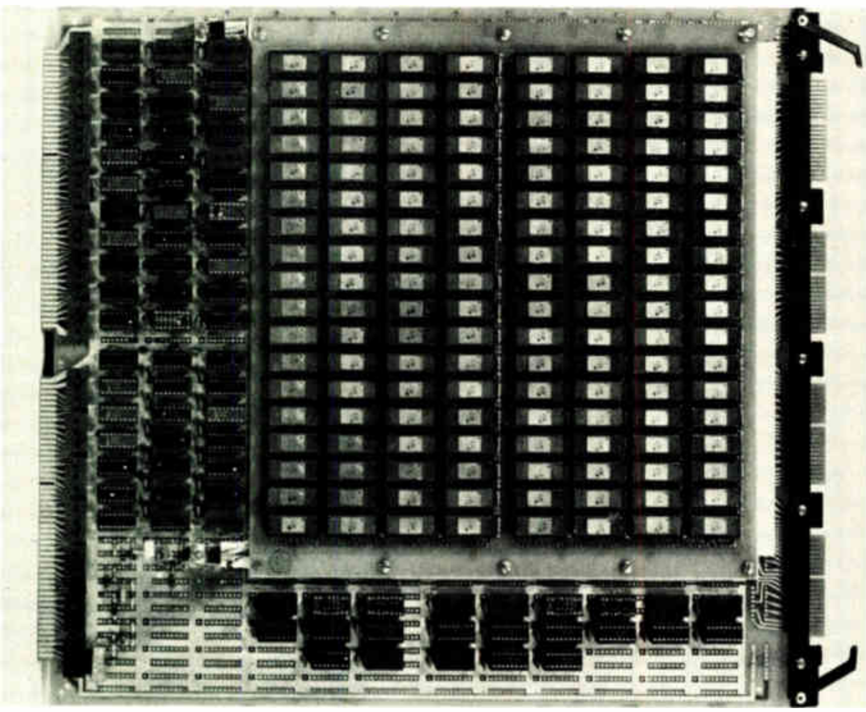
PRODUCT PREVIEW

Using 4,096-bit MOS RAMs, single memory board for computer mainframes packs in 32,768 words

Though interest in 4,096-bit MOS random-access memories is running high, start-up problems with yield and performance have kept them from being used in many systems. But Prime Computer Inc., which has committed itself to semiconductor memories since its founding in 1971, feels it can get a good enough supply of 4k MOS with good enough performance to let it introduce a new memory board built around 4k MOS RAMS.

The new board, which will be offered with Prime 100, 200, and 300 computers, has 32k words, with 16 bits and two parity bits per word—the most MOS memory ever packed onto a 16-by-18-inch printed-circuit board, the company says. This density will allow users to build systems with up to 256k of main memory in a single 21-inch chassis.

Prime is now using 22-pin Intel and Texas Instruments chips, but director of engineering Joseph F. Cashen says, "We are not limited by pinout." Accommodating chips with different pinout would require a differently etched board but "we don't have a hangup on having more than one etch board," he says. Prime says that because its logic is microprogramed, the cost of designing a second etch board is minimized, and even that cost is offset by the advantage of being able to use more parts.



Cashen feels that, so far, the 4k chips that Prime has worked with are better than 1k chips were at a similar stage in their product life. He notes that problems are often found in new products, but so far Prime has found none in its 4k chips.

The principal benefit that 4k MOS contributes is lower price; a Prime 300 with 32k of 1k MOS memory costs $26,000; with 32k of 4k memory, it costs $19,000. While 4k chips are more expensive than 1k chips, they enable the component count to be substantially decreased, reduce supporting circuitry, and allow the unit to fit into a smaller chassis—with 1k MOS, Prime fits 8k words on one pc board. And since 4k MOS is still relatively new, Prime projects cost reductions as the price of the chips drops.

However, use of 4k MOS results in a tradeoff in speed: Prime's fastest 300 has a cycle time of 600 nanoseconds, while cycle time with 4k MOS is 750 ns. Prime expects that speed will increase in the future, and notes that since basic control for the memory is on the central-processor board, the microcode can be adjusted to different memory times as new products become available.

Use of 4k MOS makes a large amount of main memory available to the small-computer user, says Cashen, allowing him to be less dependent on slower mass storage and to save software costs of trying to squeeze his programs into smaller memories. In the Prime 300 virtual-memory system, availability of more real memory improves response time.

Price for a 32k system with a single memory board using 4k MOS will be $13,000 with a Prime 100 CPU, $15,000 with a Prime 200, and $19,000 with a Prime 300. Purchased separately to upgrade systems in the field, the 32k board will sell for $11,000. Evaluation quantities are available now and quantity shipments will begin in late 1974.
Prime Computer Inc., 23 Strathmore Rd., Natick, Mass. 91760 [371]

Low-cost modem built for high-speed local links

Codex Corp. is going to this year's NCC with a low-cost modem for local high-speed data transmission. The model 8200, priced at about $1,000, includes many control and indicator features as standard equipment. But, says John Pugh, director of marketing, the 8200 has only 10% of the complexity of a functionally similar unit intended to operate on a limited-bandwidth voice-grade line.

The 8200 provides the capability for an error rate of 10^{-8} over unloaded, unconditioned local telephone loops or on private cable systems. It operates at rates of 2,400, 4,800, 7,200, 9,600 and 19,000 bits per second.

This synchronous data modem or "line driver" will accommodate four-wire half/full duplex and two-wire half-duplex/simplex configurations. The basic operating range can be doubled in four-wire applications by utilizing additional units as repeaters approximately midway in the link.

Immunity from background noises, line distortion, and parameter variation is provided via differential diphase modulation. The company says this method of taking the differential of two sampling points has an inherent capability for noise rejection. Diphase modulation is more ideally suited to channels of wider bandwidth, says Pugh.

Transmit level is strap-selectable in seven steps from −16 to +3 dBm to provide compatibility with Bell System power-versus-frequency restrictions for private-line metallic circuits. Equalization is accomplished through a compromise equalizer. The Codex 8200 has a wide-range automatic gain control of 50 dB to maintain constant output signals.

Transmit timing is provided internally or is externally derived from the data terminal. The data-derived receive-timing utilizes a decision-directed feedback-recovery technique to eliminate any potential data-pattern sensitivities. In this technique, complementary-MOS circuitry recognizes data content and compensates for shifts in sampling time that might occur. C-MOS, which uses 10% of the power supply and has a higher noise immunity than TTL, provides more stable timing recovery, which ultimately produces superior operating performance, the company says.

A series of modem controls on the 8200 include a local loopback, a data clamp to secure the transmit data to a known pattern and check against receive data, and a direct-current busback to connect the received data and clock back to the transmit data and clock.

The system-monitoring and fault-isolation features include a signal-detect light and a remote loopback, which provides dc busback at a remote site by transmitting a 343-hertz signaling tone. If the data-clamp switch is also activated, a known data pattern will be transmitted, and the signal-detect indicator will extinguish for 200 milliseconds if an error is detected in the receive data pattern.

The Codex 8200 uses a power supply of ac inputs of either 115 or 230 volts, ±10%, 47 to 63 Hz, at 6 watts. The modem measures 4 by 11 by 11 inches and weighs 10 pounds. Temperature range is 0 to 50°C.

Delivery time is 60 to 90 days, starting in June.

Codex Corp., 15 Riverdale Ave., Newton, Mass. 02195 [372]

Controller handles cluster of eight video displays

Carefully avoiding any identification with "smart" terminals that have come to the market in the past several years, Texas Instruments' Digital Systems division is introducing at NCC a powerful, clustered-processing terminal. The system, which will also give users their first look at a TI-built video display terminal, is a spin-off of the company's recent 1,000-terminal contract with Ramada Inns.

The system features one to eight TI model 913 video displays clustered about a processing-terminal controller, and each terminal's 960-character memory is connected via a high-speed link to the controller. Each terminal has a 12-in.-diagonal non-glare screen to present up to 960 characters at once, and it includes programable cursors, a selection of keyboards, and a private refresh memory.

Dial-up, private-line point-to-point, and private-line polled multi-drop circuits are supported through either synchronous or asynchronous modems, or a combination.

"The programable cluster-terminal processor typically assumes control of operator/terminal dialogue and provides operator-prompting and dialogue techniques that are impractical with conventional terminals," says Richard Jennings, computer marketing manager. Each terminal has its own memory on an input/output board in the processor chassis so that the processor computer can go in parallel with display and refresh activity to change any character, he says.

"Keyboards and CRTs are independent input devices to the processor," Jennings adds. Ascii-coded characters from the keyboard are fed to the processor, but the user can program the processor to use that character any way he wants—for data-formatting or editing, for example.

The system will also accommodate high-speed hard-copy printers or low-speed impact printers with bulk-data storage. Jennings indicates that processors will sell for about $1,000, and terminals will be less than $2,000.

Texas Instruments, Digital Systems Division, P.O. Box 2909, Austin, Texas 78767 [373]

Memory unit, graphic tablets work with any terminals

A floppy-disk memory system built by Tektronix Inc. contains a first-in, first-out (FIFO) integrated-circuit buffer that checks input and output accuracy. The FIFO buffer holds data after it has been written on one sector of the disk, and, on the next revolution, it checks what has been written against what was entered. A second buffer accepts input data while the first is checking.

Textronix offers the system in both single- and dual-drive units, the 4921 and 4922. The systems are designed to plug in directly to the Tektronix 4010 and 4023 family of terminals, but either will work with any terminal or directly with a time-shared computer.

The disks will store data in either binary or Ascii form. Ascii data will be displayed on a cathode-ray-tube terminal; binary data is suppressed. Disk capacity is 262,144 8-bit bytes. Read/write data rate is 250,000 bits per second. Approximate prices are $2,495 for the single-disk unit and $4,995 for the dual version. Both are to be available July 1.

In March Tektronix began shipping a display terminal, the 4014/15, with the largest direct-view storage screen on the market, 15 by 11 inches. At NCC, the company will show a new 40-by-30-inch graphics tablet, the 4954, designed for use with the 4014. A smaller version of the tablet, the 11-by-11-in. 4953 for use with the Tektronix 4010, 4012, and 4013 terminals, will also be introduced.

The tablets will interface with any manufacturer's terminal, and the company is willing to tailor a tablet of any size desired by a customer.

The small tablet, with a 10-bit format, works with a grid of 1,924 points, each 0.01 inch apart. The larger tablet maintains 0.01-in. resolution with a 12-bit format and a grid of 4,096 by 3,072 points.

The tablets can transmit to both a display terminal and a computer simultaneously so that the terminal display can be suppressed if the operator wishes. Tektronix says that eliminating the display while tracing an outline with the input stylus reduces tracing error.

Because the size of the input buffer (1,000 bits) can limit data-entry rate and even cause data to be lost, the tablets may be operated in a single-point data-entry mode, in which the computer logs each bit entered before letting more data in. In the multiple-point mode, also used by both tablets, the operator can enter coordinates, and the computer will fill in the lines.

Approximate prices are $2,795 for the small tablet and $5,995 for the large one. They will be available Aug. 1.

Tektronix Inc., P.O. Box 500, Beaverton, Ore. 97005 [374]

Digi-Log Systems builds acoustic coupler into CRT

Building an acoustic coupler into a CRT terminal—particularly one with batch capability—is unusual. But Digi-Log Systems Inc., Horsham, Pa., has done just that. In addition, the terminal has an MOS memory and microprocessor-controlled circuitry.

Called the model 3302, the interactive terminal is designed to replace Teletype models 33 and 35. The model 3302 has a buffer memory that gives it editing capability, so that with a push of the character insert/delete or multiple clear buttons, the text can be altered before it is transmitted.

The built-in coupler, together with the unit's integral modem, allows communication over any telephone at speeds of 110 and 300 bits per second. A standard RS-232-compatible interface connector

is provided for direct connection to a central processor for remote or local operations or to a serial printer. Switch-selectable rates of 110, 150, 300, 600, 1,200, 2,400, 4,800, and 9,600 bits per second are provided.

Data is displayed on the 12-inch-diagonal screen, formatted into 16 lines by 80 characters which each use a 5-by-7 dot matrix. Other features offered in the 3302 include a silent electronic keyboard for fast data entry and a keyboard- and program-addressable cursor. Character or block entry is selectable, and screen-erase may be controlled remotely.

Price of the 3302 ranges from $2,250 for one to nine units to $1,800 for 100 to 250 units. Delivery time is 45 days.

Digi-Log Systems Inc., Babylon Rd., Horsham, Pa. 19044 [375]

Versatec printer/plotter quadruples resolution

By staggering the nibs in the writing head, Versatec Inc. of Cupertino, Calif., has achieved a density of 40,000 points per square inch in its new family of electrostatic printer/plotters.

The writing head common to all three members of the family has 2,112 points in a 10.56-inch line, or 200 per inch. These points are scanned electronically, in a raster pattern, so that inertia and friction are eliminated as sources of error. A stepper motor moves paper past the head at 0.75 inch per second; the machines print in an area 10.56 in. wide by any length up to 500 feet.

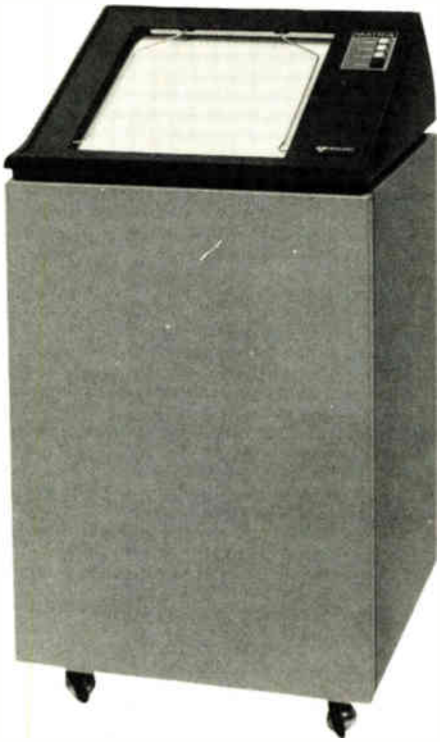
Dividing the nibs between two combs was necessary to accommodate so large a number of them and their attendant lead wires and insulation. The dots printed by the nibs overlap on the paper.

The Matrix LP-1250 printer uses a read-only memory to decode Ascii input and generate characters in a 16-by-16 matrix. Best previous resolution was obtained with a 7-by-9 matrix, so Versatec has in effect quadrupled resolution in the new series.

In addition to the standard Ascii set of 96 characters, the company offers the user an optional 128-character set with whole numbers and fractions.

The Matrix 1200 plotter controls the raster scan with software but otherwise functions like the LP-1250. The 1200A plotter/printer will print 132 characters per line from Ascii input data, at 400 lines per minute, or it will function as an X-Y plotter. With optional extra equipment, it will print and plot simultaneously.

Price of the LP-1250 printer is $7,400. The 1200 plotter costs $8,600 and the price of the 1200A printer/plotter is $9,700. Discounts are available on quantity and OEM orders.



Versatec Inc., 10100 Bubb Rd., Cupertino, Calif. 95014 [376]

Recorder using 3M cartridge has the ANSI format

Apparently the first cartridge recorder to meet the American National Standards Institute (ANSI) format, the series 4000 recorder from Kennedy Corp. uses the increasingly popular 3M ¼-inch cartridge. It accepts byte-oriented data, which it phase-encodes at 1,600 bits per inch, complete with preamble, postamble, and cyclic redundancy check. Easily interfaced, the system also provides timing and control for up to four ¼-in.-tape drives.

Designed for minicomputer and other data-processing applications using 8-bit bytes, the series 4000 organizes the data to bit serial on the tape, without needing an additional parallel-to-serial converter. The bytes are not separated by start/stop bits, so that all available space is used for data. Preceding the data for read synchronization is a 16-character preamble, and immediately following it is a 16-character cyclic redundancy check (CRC) and a 16-character postamble. Record gaps are 1.2 in. All timing is provided by a crystal-controlled oscillator in the format unit.

The 16-bit CRC checks errors so precisely that there's no need for redundancy in the data portion of the record. Using a circuit that implements a polynomial defining the most common errors, the CRC operates on the entire data-bit stream in the block. For speed, the configuration makes the check word available immediately after the last data bit has been shifted in. The check is made in both forward and reverse.

The formatter is organized to al-

low independent read and write sections and can initiate the read process in either the forward or reverse direction. Since preamble, CRC, and postamble contain no useful information, they are stripped off by the formatter before they reach the computer interface.

The recorders employ a unique isoelastic drive system, which monitors tape tension and tape motion with a single servo-drive motor. Fully bidirectional, the recorders operate at a data rate of 5 kilobytes per second at 1,600 bits per inch. Forward-search, reverse-search and rewind modes are accomplished at 90 in./s. Use of phase-encoding improves reliability, error detection, and packing density.

The four-track drive is equipped with a dual-gap, read-after-write head for optimum performance. Each track is treated independently, allowing cartridge interchange between transports of different track configurations. Total storage is 2.875 megabytes per cartridge. With four recorders the series 4000 has a maximum storage capacity of 11.5 megabytes of information.

The low-profile system mounts in standard 19-inch racks. The one-recorder model, 4000-1, is 5.25 in. high; the two-recorder model, 4000-2, is 8.75 in. high; the three-recorder model, 4000-3, requires 10.5 in.; and the four-recorder model, 4000-4, is 14 in. high.

Single-unit prices, including power supply, cables, and connectors, are: model 4000-1, $2,495; model 4000-2, $3,600; model 4000-3, $4,950; and model 4000-4, $6,050. Delivery is 45 days.

Kennedy Co., 540 West Woodbury Rd., Altadena, Calif, [377]

Computer Devices' portable terminal prints 132 columns

Portable teleprinter terminals need to keep their weight down and have therefore usually been limited to a width of 80 columns. Now Computer Devices Inc. has built the CDI 1132 Teleterm, which weighs only 25 pounds yet can handle paper up to 15 inches wide and print 132 columns. Speeds of 10, 15 and 30 characters per second are selectable from the operator's keyboard. An integral acoustic coupler allows communications over ordinary telephone lines to any time-sharing system.

CDI says it took "careful and conservative engineering" to make a wide-carriage, portable teleprinter and a special printer mechanism. The 1132 is also available in a model that is compatible with the IBM 2741 terminal—an advantage for portable teleprinter users, since the 2741 requires reprograming if it is to be used with printers with narrower carriages.

At $1,000, the 1132 costs about as much as nonportable units, but, unlike such units, which use IBM Selectric printing mechanisms and produce multiple copies, the 1132 is a single-copy thermal printer with dot-matrix characters.

Quantity discounts are available.

Computer Devices Inc., 9 Ray Ave., Burlington, Mass. 01803 [378]

Fluke adds to low-cost multimeter line

4½- and 5½-digit instruments for bench use and field service employ a custom IC for economical dual-slope a-d conversion

by Michael J. Riezenman, Instrumentation Editor

Building on the success of its 3½-digit model 8000A multimeter [*Electronics,* Aug. 28, 1972, p. 100], the John Fluke Manufacturing Co. has decided to complete its coverage of the low-cost multimeter market by bringing out two new instruments—the 4½-digit (20,000-count) model 8600A, and the 5½-digit (200,000-count) model 8800A. But there's a difference: though the approach taken in the new units and the 8000A is the same—high reliability and no gimmickry—the means have changed.

Dual slope. Instead of the 8000A's voltage-to-frequency converter, which is incapable of the accuracy needed by higher-precision units [*Electronics,* Sept. 11, 1972, p. 102], the new models use dual-slope conversion—the process owned by Schlumberger, which recently licensed Fluke to use it. And to keep the costs of the dual-slope converter down, most of its circuitry has been implemented in a custom-designed IC.

Like their predecessor, the new meters feature LED displays, automatic zeroing, automatic polarity detection, and rugged cases molded of high-impact plastic. Unlike it, the new instruments have autoranging in addition to manual range selection. Prices of the new meters are $595 for the 4½-digit unit and $995 for the 5½-digit machine.

Though meant for bench and field use, they can be given a systems orientation by an optional, isolated printer output for data-logging applications. Prices of this option are $100 for the 8600A and $150 for the 8800A. An option available for the model 8600A only is a rechargeable battery pack, priced at $95.

Protection. A basic design consideration was adequate overload protection. The 8600A can withstand overloads of up to 1,200 volts dc or 1,700 v peak ac on all its voltage ranges. Its ohms ranges are protected up to 250 v rms or dc, and its current ranges are all protected by a 2-ampere fuse which is accessible from the front panel.

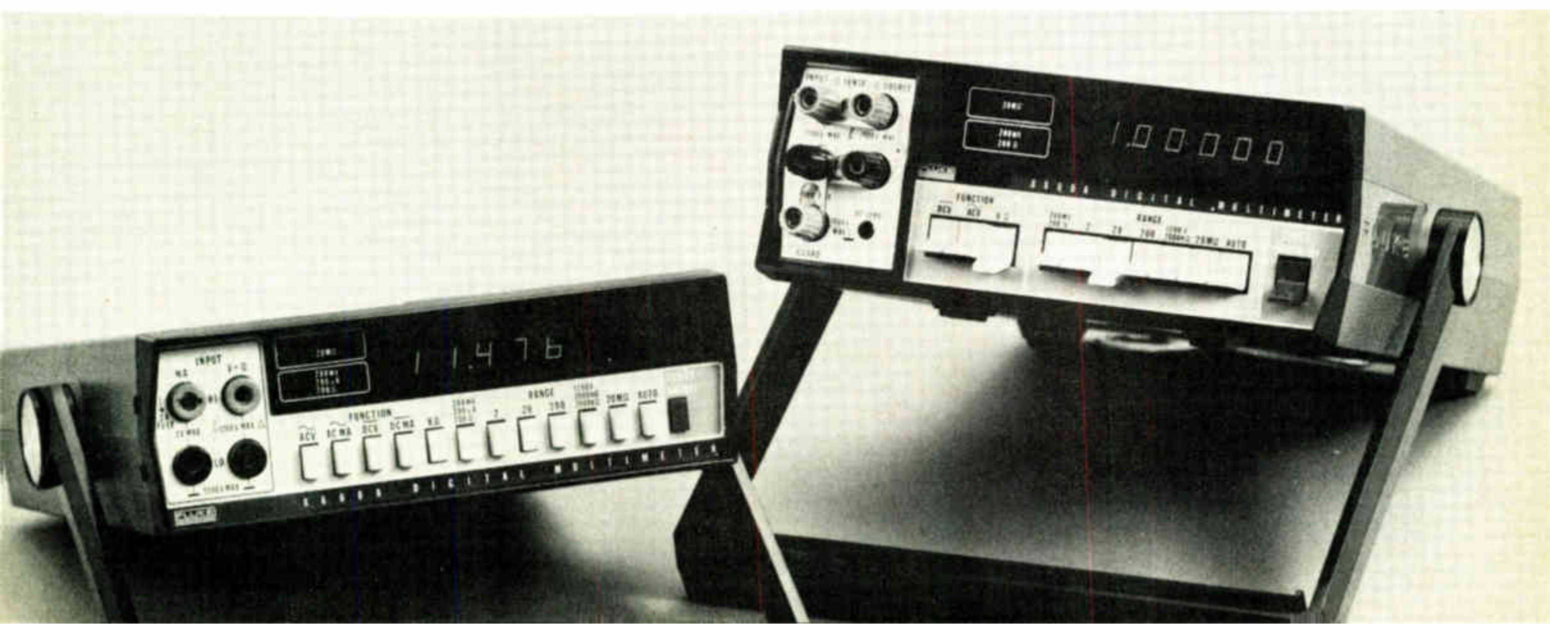
The 8800A is protected up to 1,000 V dc or 1,700 v peak ac on its dc voltage ranges, and up to 1,200 V rms on its ac ranges. Ohms protection is the same as on the 8600A; the 8800A has no current ranges.

The 4½-digit 8600A has five ac and dc voltage ranges, five ac and dc current ranges, and six ranges of ohms. The voltage scales range from 200 millivolts full scale to 1,200 v, while the current scales run from 200 microamperes full scale to 2 A. The resistance ranges run from 200 ohms full scale to 20 megohoms. Maximum error on the 2-, 20-, and 200-v dc ranges is ±(0.02% of input + 0.005% of range). Input resistance is greater than 1,000 megohms on the 200-mv and 2-v ranges, and 10 megohms on the others.

The 5½-digit 8800A has essentially the same ranges, except it has no 100-mv ac voltage range.

Under the best of conditions, over a 24-hour period, at a stable temperature of 23°C ±1°C, the worst error in measuring dc voltage is only ±(0.005% of input + 0.002% of range). More realistically, over a 90-day period, in the temperature range from 18 to 28°C, the maximum error is ±(0.01% of input + 0.003% of range).

The John Fluke Manufacturing Co., P. O. Box 7428, Seattle, Wash. 98133 [338]



Some of the best things about our new Digivac® 1000 are what you can't see.

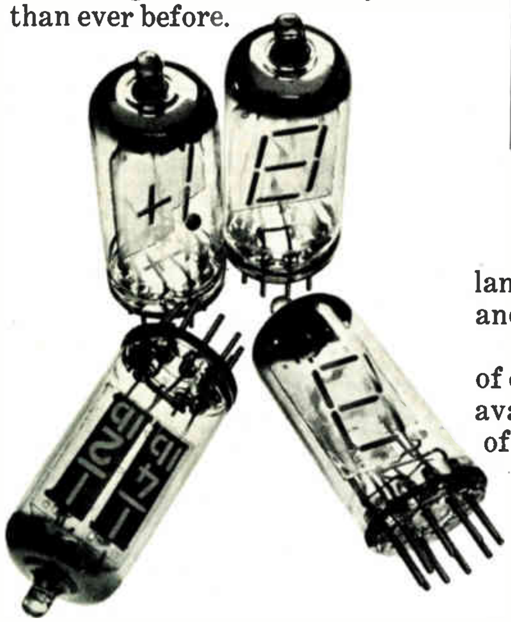
When you look at our vacuum fluorescent readout, you won't see the low voltage requirements making it directly compatible with available MOS IC logic packages.

You won't see the exclusive mica substrate which supplies mechanical strength and helps emphasize lighted segments through a desirable halo effect.

You won't see the low cost, lower than competing readouts with fewer customer advantages.

Of course, there are things about our Tung-Sol® Digivac 1000 you can see.

Like the Digivac 1000's brightness. 50% more brightness and greater uniformity than ever before.



You can see the flexible language with alpha, numerical and symbolic figures.

You can see the wide range of colors, including white, available with common types of filters.

And because of the unique construction, you can see the accurate viewing assured from virtually any angle.

With the Digivac 1000 readout, whether you see it or you don't . . . it's still nice to know it's all there.

For additional information on the Digivac 1000, write to: Tung-Sol Division, Wagner Electric Corporation, 630 W. Mt. Pleasant Avenue, Livingston, New Jersey 07039.

Wagner makes other quality products in volume for the electronics industry, including bridges, power supplies and subsystems, silicon rectifiers, resistors, miniature lamps and status indicators. And Wagner offers contract manufacturing.

WAGNER®

We've got a lot more riding for you.

Components

Detector uses heterojunction

Technique in photovoltaic unit is said to increase current output, sensitivity

A new heterojunction photovoltaic detector supplies 30% to 50% more output current than can be obtained from conventional light-sensitive silicon devices, its manufacturer claims. The detector, fabricated by the Innoductor division, Innotech Corp., Norwalk, Conn., uses a pn heterojunction consisting of semiconducting glass and silicon. This is formed when a thin layer of a specially developed n-type glass is deposited on a layer of p-type single-crystal silicon.

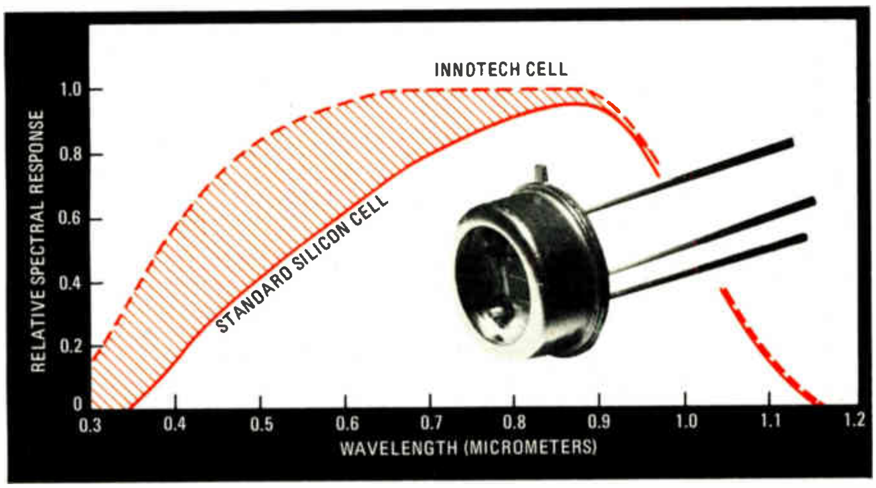
Moreover, because the glass is basically transparent to visible light, the detector is sensitive to the blue-violet portion of the light spectrum. Ray Pennoyer, Innoductor general manager, points out that this sensitivity opens up the possibility of designing the new detectors into color-sensitive applications. In conventional photodetectors, these frequencies are absorbed before they can reach the electron-emitting pn junction formed between p- and n-type layers of silicon, Pennoyer says.

Intended applications include use in light detectors, card readers, optical character-recognition equipment, industrial counting and measuring devices, level sensors, and punched-tape readers. The company also wants to use the device in solar cells for converting light to electricity on a commercial scale. Because of their greater output current, the new devices offer a greater signal-to-noise ratio than conventional parts, and, in a complete system, they can be followed by less critical circuitry.

The first detector in the family of devices, the model PVDO90F, has a typical short-circuit current of 165 microamperes when using a 500-foot-candle standard incandescent tungsten light source. The light-sensitive area measures .090 by .090 inch. Open-circuit voltage is a minimum of 200 millivolts.

Sensitivity of the devices is 13 microamperes per milliwatt per square centimeter at 7,500 angstroms, which is the red wavelength emitted by a gallium-phosphide light-emitting diode, for example. This is 70% higher than the output obtained from standard silicon units, says Pennoyer. At 5,000 Å in the green, the device's sensitivity level is 8μÅ/mw/cm^2—three to four times the sensitivity of a purely silicon photodetector, Pennoyer claims.

The PVD090F is packaged in a TO-5 low-profile flat-glass windowed case. Sample quantities are available from stock at $20 each, and the price tails off to $5 each in quantities approaching 500. Custom-chip sizes are also being offered, and other packages, as well as mul-



tiple units on 100-mil centers, will be offered in about a month.

Innotech Corp., 181 Main St., Norwalk, Conn. 06851 [341]

LC filters offer 51.2-MHz center frequency

A line of crystal filters includes an LC filter designated the model 6918LA. Specifications include a center frequency rated at 51.2 megahertz, a 3-decibel bandwidth (28.4 MHz minimum), an operating temperature range of −10°C to +65°C, and a price of under $50 in quantities of 100. The LC filters are also available in low-pass, high-pass, bandpass, band-reject, and combination configurations.

Electronics Division, Damon Corp., 80 Wilson Way, Westwood, Mass. 02090 [339]

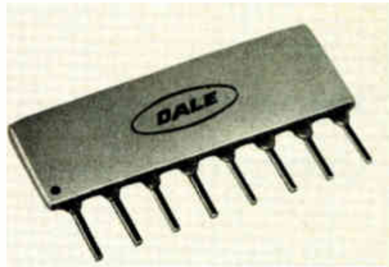
Microwave capacitors range from 5 to 125 picofarads

Small capacitors for use in microwave integrated circuits are designed for volume production in such specific applications as by-pass capacitors, bias current capacitors, and blocking capacitors. The line offers a wide range of capacitances, starting at 5 picofarads and extending to 125 picofarads. Blocking voltages offered are dc, 70 or 50 volts. Five models are available in the VCC series.

Varian, Solid State East Division, Salem Rd., Beverly, Mass. 01915 [345]

Thick-film networks offer from three to nine resistors

A series of single in-line thick-film networks designated series CSP provides from three to nine resistors in a flame-retardant package. Models are available with four, six, eight, and 10 terminals with a choice of 0.100- and 0.125-inch spacing. Lead-frame construction provides built-in standoffs to facilitate board washing and wave soldering. The



networks are designed to operate in the temperature range of −55 to +150°C, and they have a resistance range of from 10 ohms to 1 megohm with a temperature coefficient of ±200 ppm.

Dale Electronics Inc., Box 609, Columbus, Neb. 68601 [343]

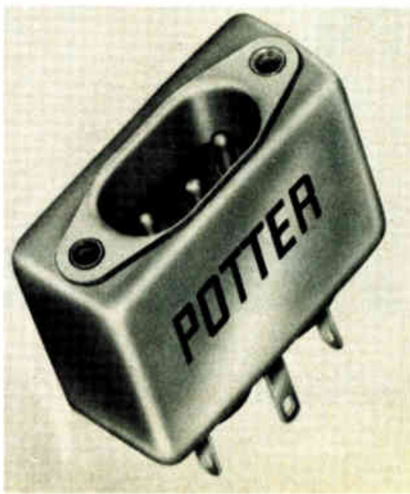
Linear filters range from 400 Hz to 50 MHz

Linear phase lowpass resistance-capacitance filters are offered in Bessel, Gaussian, equal-phase, and transitional types. Frequency range extends from 400 hertz to 50 megahertz with impedances from 50 ohms to 20 kilohms. The filters offer low phase and delay distortion in passband and very low pulse distortion. At 50 MHz, attenuation is typically 70 decibels, and delay is 100 nanoseconds. The units are encapsulated in epoxy or sealed in metal cans.

Allen Avionics Inc., 224 E. 2nd St., Mineola, N.Y. 11501 [346]

Emi filters have low leakage current

A line of filters for electromagnetic interference is designed for use in test instrumentation and computer

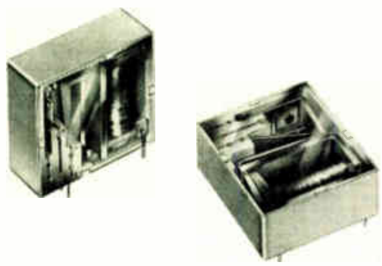


peripherals. They meet UL specifications for equipment requiring a detachable power line, and to minimize shock hazards, they offer a low leakage current. Frequency range is from 150 kilohertz to 100 megahertz. The filters accommodate a three-conductor line cord and withstand a variety of environmental hazards.

The Potter Co., Box 337, N. Highway 51, Wesson, Miss. 39191 [344]

Power relay offers 3 contact materials

A miniature printed-circuit-board power relay, called the model V23027, is offered with three different contact materials, silver-gold flashed, silver-nickel, and silver-cad-



mium-oxide. The unit provides resistive, lamp, and inductive loads up to 8 amperes continuous or 15 A switching. The relay is designed for mounting on a 0.1-inch grid, and typical applications include automotive, consumer electronics, process control, and data processing. Price is about $1.92 in 500-lots.

Siemens Corp., Special Components Dept., 186 Wood Ave. South, Iselin, N.J. 08830 [348]

Voltage protector lasts beyond 900 operations

The model CG-350 transient voltage protector, when subjected to a current pulse of 500 amperes, exhibits a typical life beyond 900 shots, or 250 operations at 1,000 A. When the half-width duration of a transient surge exceeds 500 to 750 microseconds, however, appropriate life tests must be performed by the user. Applications are in telecommunications, instruments, control systems, intrusion detection, and traffic control.

Signalite, 1933 Heck Ave., Neptune, N.J. 07753 [347]

Plastic pots range from 100 ohms to 4 megohms

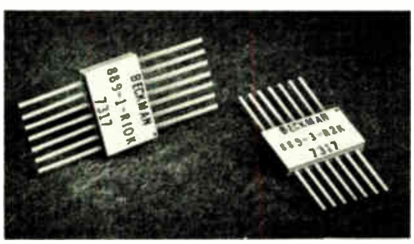
The series 7PT precision conductive plastic potentiometers are intended for commercial and industrial applications. These include medical instrumentation and sound systems for radio and TV. Life expectancy is a minimum of 3 million revolutions. The pots are available in ranges from 100 ohms to 4 megohms.

Sigma-Netics Inc., 1 Washington Ave., Fairfield, N.J. 07006 [350]

Resistor flatpacks offer varied ratings

The series 889-1 and 889-3 resistor networks are designed for applications requiring low package profile and ribbon lead terminations to the circuit board. The flatpacked networks are particularly suited for high-density applications. The 889-1 is a 13-resistor unit rated at 0.15 watt for each resistor, and the 889-3 is a seven-resistor unit with each device rated at 0.25 watt. Power rating at 25°C for the package is 0.6 watt. Maximum resistance tolerance is ±2%, and maximum resistance shift is 0.25% over the operating temperature range of from −55 to +125°C. Price in 1 to 9 quantities is $7.50 for both series.

Beckman Instruments Inc., 2500 Harbor Blvd., Fullerton, Calif. 92636 [349]



 Circle 139 on reader service card

Instruments

Ac standards reach 1 GHz

Thermal voltage converters compare ac voltages with precision dc levels

It being difficult, at best, to build an ac equivalent of a standard cell, precision ac measurements are necessarily derived from ac-dc transfer standards. These standards are devices for calibrating ac meters and

work by comparing ac voltages with dc voltages whose accuracies are traceable to the National Bureau of Standards.

Until now, the highest frequency that could conveniently be covered with NBS certification was 100 megahertz. Now Ballantine Laboratories is producing a thermal converter, based on an NBS design, that covers the frequency range from 100 MHz to 1 gigahertz. The new converter comes in three different models, each of which spans a different voltage range, and all three of which cover the full frequency range. The model 1386A-1 spans the voltage range from 0.25 volt to 1.0 V; the 1396A-2.4 goes from 1.0 to 2.4 V; and the 1396A-7 covers 2.4 V to 7.0 V. Price of the two lower-voltage models is $475; the 7-V unit costs $530.

The heart of the thermal converters is a small vacuum element containing a fine heater wire to which a tiny thermocouple is attached. In operation, an unknown ac voltage, after passing through a frequency-compensated attenuator, is applied to the heater wire while a Lindech potentiometer is used to null out the dc voltage generated by the thermocouple. Then, leaving the potentiometer alone, the ac signal is removed and replaced with an adjustable dc supply. The dc voltage is adjusted until the potentiometer is again balanced, at which point the dc voltage is equal to the rms value of the ac voltage. The dc level, of course, can be read on a high-accuracy dc voltmeter.

The thermal converters are supplied with calibration charts giving the measured differences between the dc and rf voltages at different frequencies. The maximum error in the rf-dc differences is 1%, and the Ballantine standards against which the measurements are made can contribute as much as another 1% error, so that total worst-case error is 2%. This uncertainty can be reduced to 1% by having the units calibrated by NBS, but at about $80 per frequency point, NBS certification can easily cost more than the converters themselves.

Ballantine Laboratories Inc., P.O. Box 97, Boonton, N. J. 07005 [351]

Wave analyzer offers built-in counter

Single-frequency measurements can be made quickly with the model 3581A wave analyzer. A built-in counter displays the tuned frequency with 1-Hz resolution on an LED readout. Signal amplitude is read on a four-scale analog meter. Two scales are for log displays of 90 dB and 10 dB (expanded), and the other two are linear with 1 or 3 full scale. Amplitude can be read to better than 0.1 dB on the meter's expanded 6-inch 10-dB scale. Automatic frequency control is used for locking onto drifting signals, and afc pull-in is rated at 800 Hz.

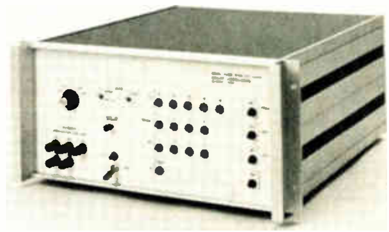
A communications version, model 3581C, is designed for analysis of telephone voice channels, both single and up to 12 channels multiplexed. The unit can also be used to pinpoint interference on data channels, detect spurious tones, and analyze levels of transmitted tones. Specifications of both the 3581A and 3581C are identical, except the latter has some modifications to make it compatible with telephone systems.

Sensitivity of both units is 100 nanovolts full scale. This low-level measurement capability is especially valuable in sonar. Maximum input to the models 3581A/C is 30 volts. Dynamic range is 85 dB, and minimum bandwidth is 3 Hz. Price starts from $2,600.

Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, Calif. 94304 [353]

Triac-SCR tester operates in less than 30 milliseconds

A tester that automatically checks and categorizes Triacs and SCRs in less than 30 milliseconds measures: repetitive peak off-state voltage, peak off-state voltage, maximum

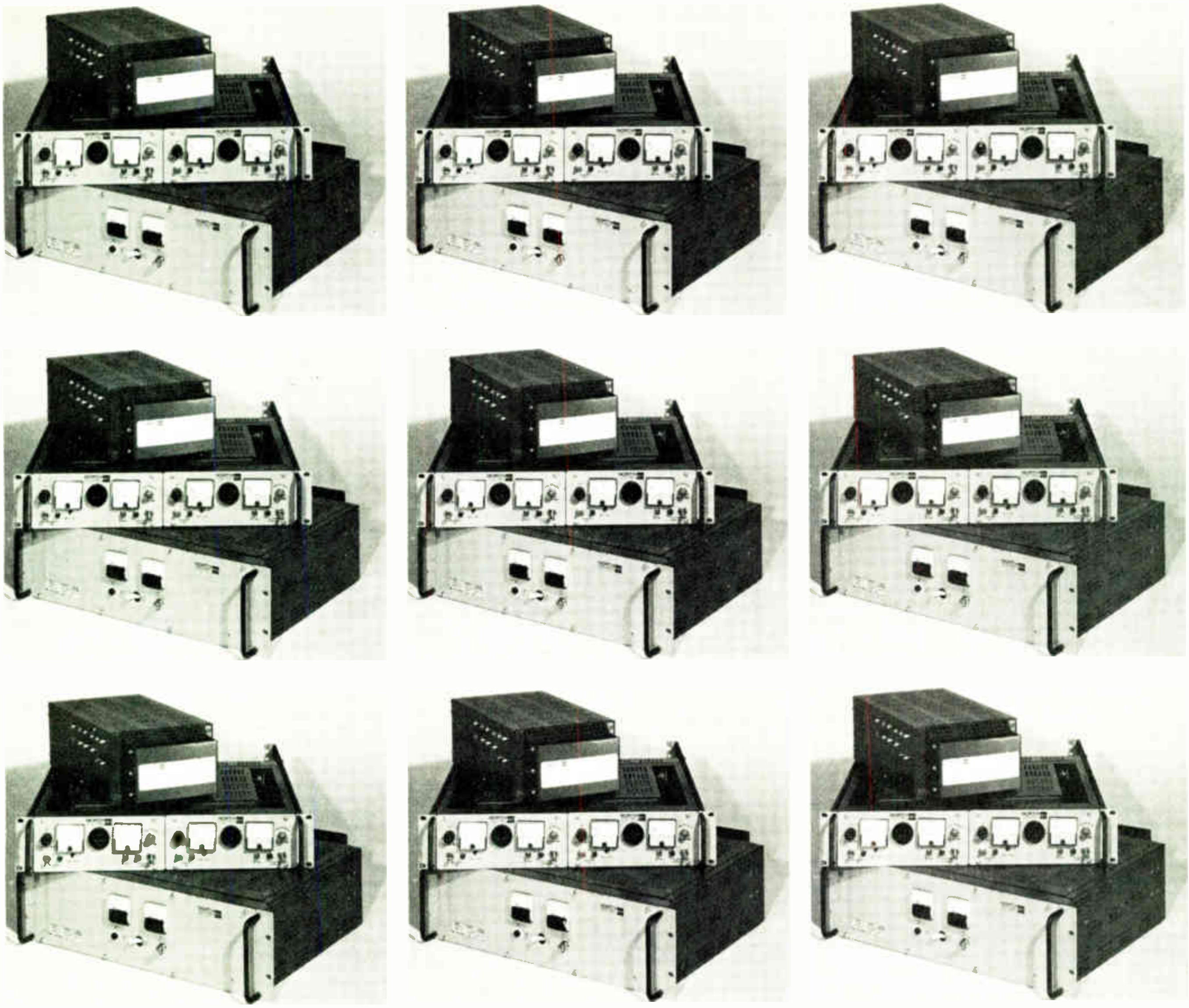


on-state voltage, rms on-state current, gate trigger current, gate trigger voltage, and dc holding current. Devices are tested to determine the on-state current rating and then are tested at gate current levels programed for the on-state current rating. Price is $3,350.

Bailey Engineering Co., 2206 Michael, Box 621, Garland, Texas 75040 [355]

Modular instrument line is for control applications

The 520 series of modular instruments has been expanded to include units that accept the output of standard thermocouples, resistance bulbs, radiation pyrometers, and



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MODEL	10000
VDC	AMPS
0 7 5	2 10
0 16	1 25
0 25	0 85
0 33	0 68

OUAL OUTPUT SUPPLIES	
MODEL	N03052
VOC	AMPS
±15-12	400MA
MODEL	N60052
VOC	AMPS
±15-12	1.0A

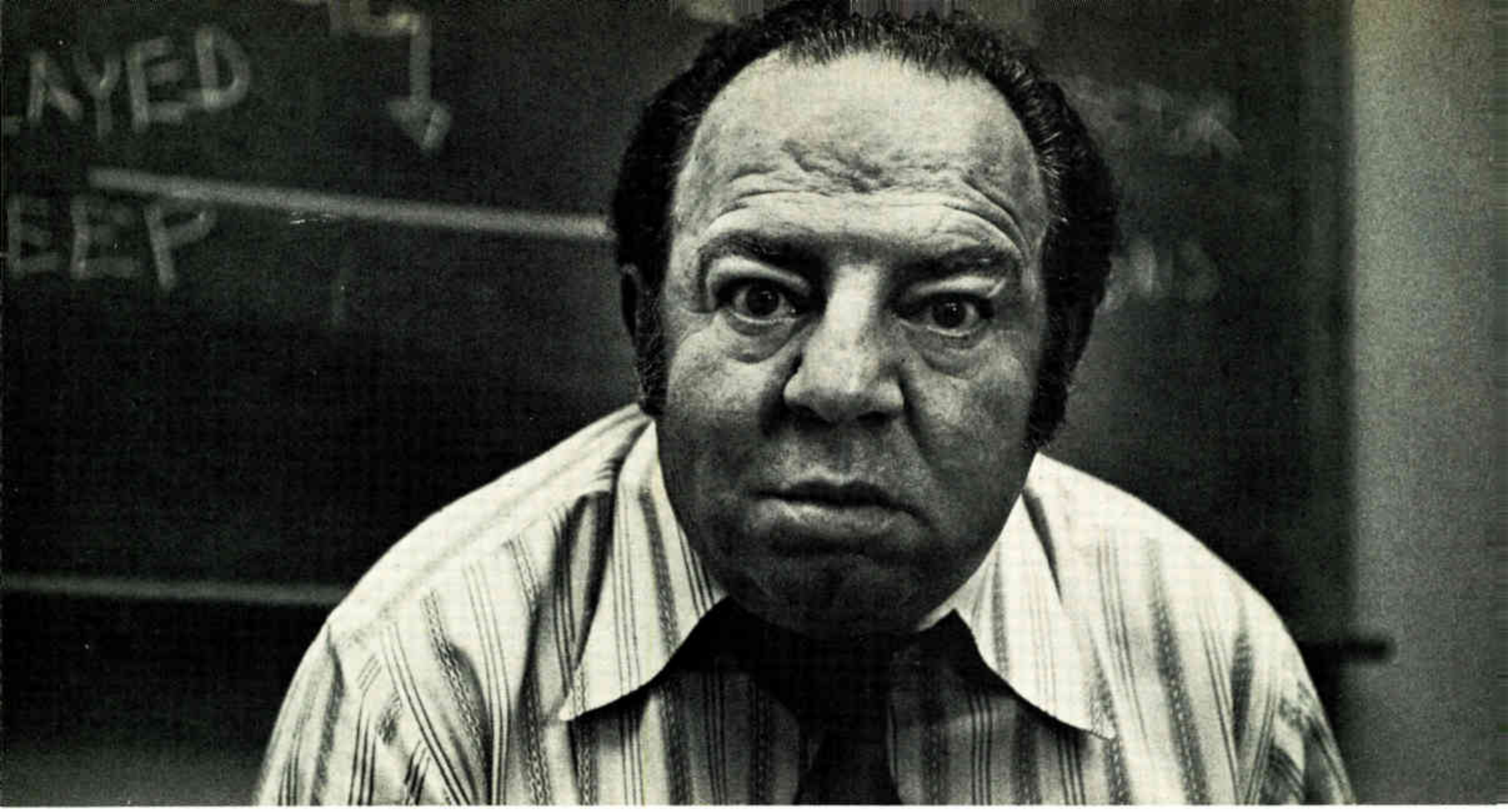
Listed here are the more popular models—many other voltages are available.

MODEL	11000	12000	13000	14000	15000	16000	17000	18000
VDC	AMPERES							
5 0	3 9	5 3	11 3	13 0	20 0	32 5	49 0	82 0
12 0	2 8	4 2	8 0	10.5	15 0	23 0	36 0	58 0
15 0	2 4	3 7	7 5	9 5	14 0	20 5	27 0	47 0
18 0	2 1	3 3	6 0	8 0	13 0	18 0	26 0	40 0
24 0	1 5	2 8	4 2	7 0	11 0	15 0	21 0	33 0
28 0	1 4	2 4	4 0	6 3	9 0	14 0	20 0	29 0
36 0	1 2	2 2	3 1	5 6	8 0	11 0	14 0	23 0
48 0	95	1 8	2 6	4 2	6 0	8 0	10 0	18 0

NORTH ELECTRIC COMPANY

North Electric Company / Galion, Ohio 44833 / A United Telecom Co.

Circle 141 on reader service card



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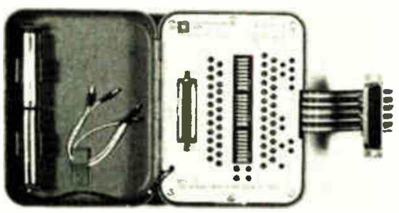
other millivolt sources. Process variables such as temperature or pressure can be monitored by a deviation meter, or an analog process meter, or a digital process meter. For control as well as measuring applications, four control modes are available: on-off, proportional, proportional plus integral, and proportional plus integral plus derivative. The on-off mode is available only on the single output on-off models.

Barber-Colman Co., Industrial Instruments division, Rockford, Ill. 61101 [354]

Monitor-breakout panel is for data communications use

The model 60 interface monitor and breakout panel is a pocket-sized test set providing access to all 25 conductors of the EIA RS232 interface for data communications applications. Twelve LEDs are used to monitor the status of the source of 12 primary signals, and two additional digits are provided for display of plus or minus voltage levels greater than ±3 V. The conductors can be interrupted, allowing isolated testing and observation of terminal



modem signals. Price is $135.
International Data Sciences Inc., 100 Nashua St., Providence, R.I. 02904 [356]

Noise meter measures to 115 decibels

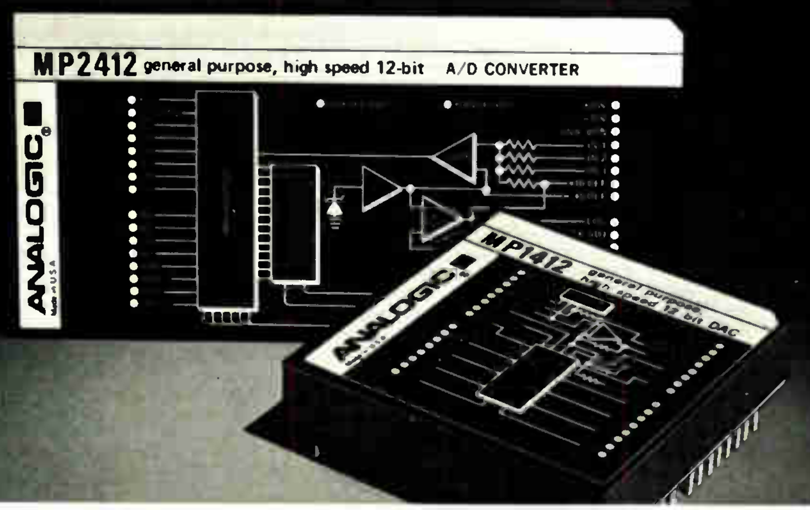
A noise meter for personal use is designed to measure brief doses of noise, mainly in factories. Engineered to meet OSHA requirements,

the meter offers a dynamic range of 90 to 115 decibels. An alert light for readings over 115 dB is provided, as well as a built-in condenser microphone and a remote microphone with optional preamplifier. Called the model 4425, the unit cuts off below threshold.
B & K Instruments Inc., 5111 W. 164th St., Cleveland, Ohio 44142 [358]

Probe station handles to 900 circuits/hour

A manually operated probe station, called the model MP-0200-PCH, offers a fixed-point probe-card holder for use with the company's fixed-point probe cards. The unit checks resistors and other devices used for thick- and thin-film hybrid circuit applications. An automatic

ENDING THE CONVERTER PARADOX



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South, 713-785-0581, 214-620-1551, 305-894-4401, 919-227-3639, 205-534-9771, 305-773-3411, 813-867-7820
West, 303-744-3301, 505-523-0601, 602-946-4215, 505-292-1212, 714-540-7160, 415-398-2211, 206-762-7664, 503-643-5754,
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SPECIFICATIONS

MP1412 12-BIT DAC	MP2412 A/D CONVERTER
$39 in 100 quantities	**$75** in 100 quantities
Settling time 4 μsec	**Throughput** to 50 kHz
Linearity 0.012%	**Linearity** 0.012%
Reliability 200,000 hours MTBF	**Reliability** 100,000 hours MTBF
Stability 15 PPM/°C.	**Stability** 20/PPM/°C.

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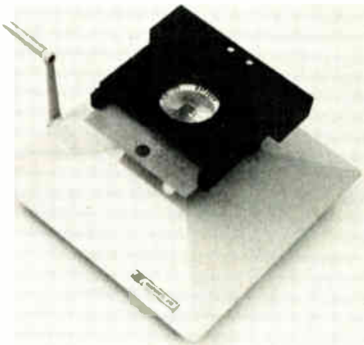
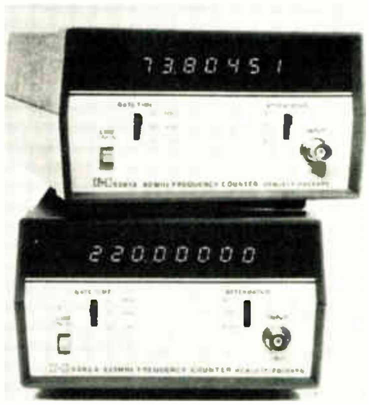
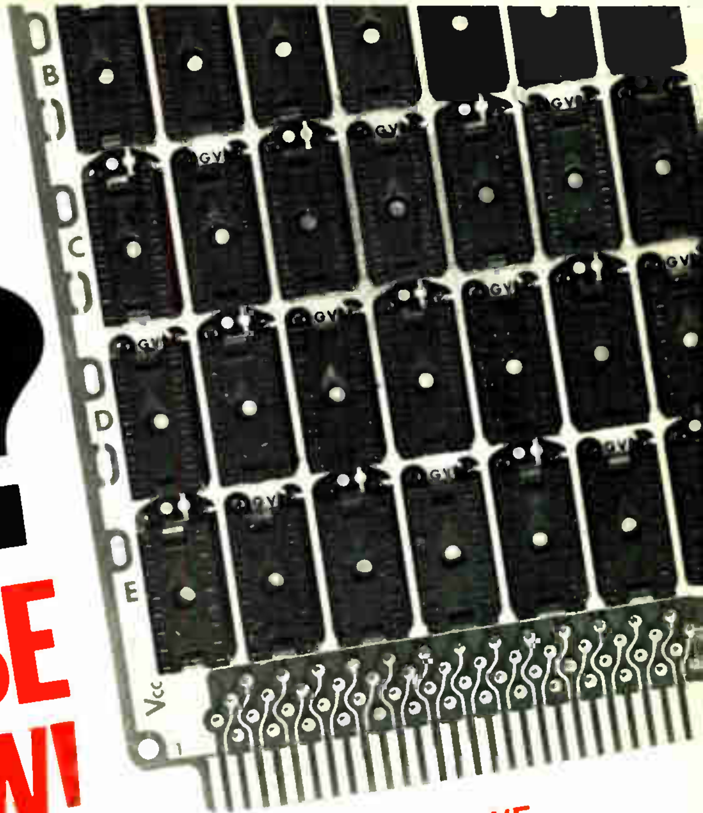


vacuum system holds substrates in place and comes with an interchangeable chuck, which can be tooled for any substrate measuring up to 2¼ inches square. Production rate is from 700 to 900 circuits per hour, depending upon test time.
Wentworth Laboratories Inc., Rte. 7, Brookfield, Conn. 06804 [357]

High-performance counters are low in price

Two counters using high-stability crystal time bases and offering a sensitivity of 25 mV make ratio as well as frequency measurements. Model 5381A is priced at $249, model 538A at $450. The former is an 80-MHz, seven-digit counter, the latter a 225-MHz, eight-digit machine. Resolution for both instruments is 10 hertz at 0.1-second gate time, 1 Hz at 1 second, and 0.1 Hz in 10 seconds. The units are also available with a high-stability temperature-compensated oscillator, which adds $100 to the price.
Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, Calif. 94304 [359]





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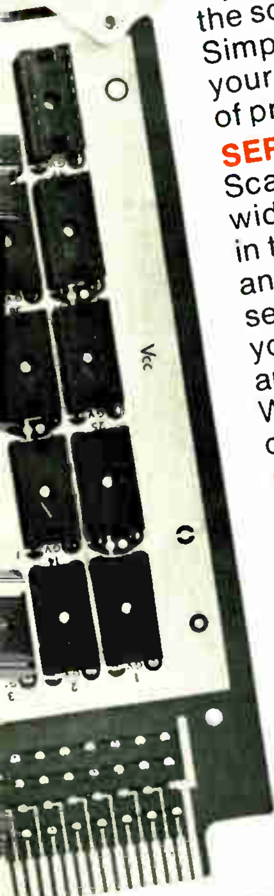

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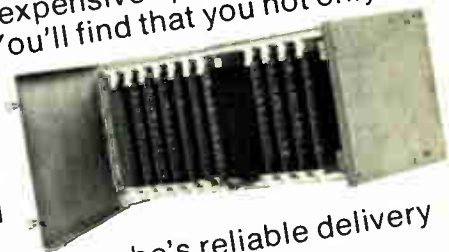

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Data handling

Simplicity built into card reader

Optical data units handle up to 800 punched or marked cards per minute

Card readers aren't the most exciting of computer peripherals, but a line of inexpensive card readers developed by True Data could be called elegant in their simplicity. Each reader has a single 4-inch capstan that picks up the cards, transports them past a fiber-optic read head, and then stacks them. The readers have only half the number of parts of most competitors, and only three bearings are used, instead of the 40 of older designs, thus improving reliability and lowering the price.

The True Data readers are modular in design. The basic deck is upgradable in the field or factory from 200 to 800 cards per minute, and it can be adapted to punched or optical-mark cards. For OEM buyers, this means that a single basic line of readers can be stocked, and simple changes can meet differing customer requirements. Modularity also simplifies stocking of spare parts, documentation, and service. The readers weigh 55 pounds and are 17 inches high, 14 in. wide, and 21 in. deep.

James McKee, president of True Data and developer of the mechanism, says that the transport permits the reader to handle damaged, misregistered, oily, and colored cards as easily as clean cards. It can select a single card at a time and separate interlaced webs, as well as handle cards with damaged leading edges, he says. Card flutter and skewing are avoided because the transport mechanism eliminates the track commonly used for the passage of cards.

The readers have built-in self-diagnostic capability, and checks are provided for such errors as loss of synchronization, extinguished light, and feeding jams. Data output is 12-bit parallel in serial columns. Switch-selectable input/output polarities and standard TTL outputs are provided. The model 400 has a 1,000-card hopper and 500-card stacker, and the 800 has a capacity of 1,000 in each. Cards can be added or removed during operation.

For servicing, hinged panels can be opened to expose the electronic and mechanical subassemblies. Little maintenance is required; the read head is automatically brushed each time a card passes.

In OEM quantities of more than 5,000 units, the basic decks, providing speeds of 200 to 1,200 per minute, sell for as little as $500 each. Complete with all electronics and packaging, the decks are priced at $2,095 each in single quantities for the model 400 ODR, which operates at 200 or 400 cards per minute, and $2,395 for the 800 ODR, which processes 300 to 800 cards per minute. OEM discounts are available. Delivery time is 30 days.

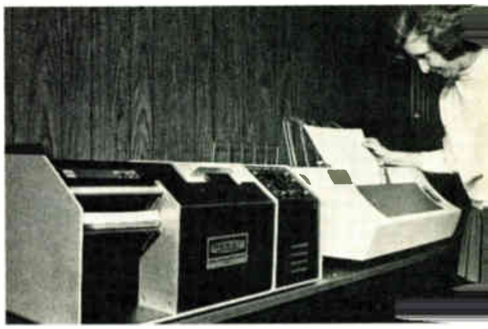
True Data Corp., 2701 Halladay St., Santa Ana, Calif. 92705 [361]

Remote-batch terminal plugs gap in market

As Triangle Universities Computation Center in North Carolina expanded its services beyond its three constituent institutions to small colleges throughout the state (see page 98), it encountered a problem in specifying the terminals to be installed on the distant campuses.

TUCC found that applying such terminals as the IBM 1050 in a remote-job-entry mode was possible at a very low price—in the neighborhood of $100 a month—but that the data transmission rate of a few hundred baud, at most, was too slow. Terminals with faster rates generally cost too much—in the neighborhood of $800 a month.

A TUCC manager mentioned the existence of this gap in the market structure to Joel V. Perry, president of Perry Electronics Inc., a small company in Raleigh concentrating on the production of printed-circuit boards. As a result, Perry and his associates produced a terminal that met the requirements of TUCC by



working at 1,200 baud yet could be leased for $370 a month or sold for $10,750.

The unit has an OEM-supplied printer and card reader and a Perry-built controller. It works at any rate over the range of 110 to 1,200 baud, converting the Hollerith card code to parallel Ascii, and then to serial form for transmission, and converting the incoming serial data to parallel form for the printer. On unconditioned lines, it runs at 1,200 baud asynchronously but it can do 1,800 baud, also asynchronously, if the lines are conditioned—that is, carry loading coils to compensate for phase delay.

Perry Electronics installed its first terminal at TUCC in September 1972. Since then, it has been busy perfecting the design and installing units elsewhere in the TUCC network, while maintaining its principal pc card business. It hopes to expand into educational installations

in neighboring states soon, as well as into other applications.

Perry Electronics Inc., 2323 Campbell Street, Raleigh, N.C. 27605 [362]

Core-memory modules have 16,384 or 32,768 words

A family of 20-bit memory modules, designated the 1600 series, offers capacities of either 16,384 or 32,768 words. Designed for OEM users, the core memories are priced at 0.5 cent per bit. Each module is comprised of a single double-sided printed-circuit board and a plug-in stack. Access times range from 300 to 650 nanoseconds, and cycle times from 650 to 1,500 nanoseconds. Further, word lengths of 20, 18, 16, and 10 bits are available. Up to eight series 1600 modules can be combined to provide either 128,000 words using 16,000-word modules or 256,000 words using 32,000-word modules. Temperature-independent cores are used to provide stable operation over the range from 0 to 55°C.

Ampex Corp., 401 Broadway, Redwood City, Calif. 94063 [363]

Printer operates at 600 lines per minute

Designated the model 2260, a printer can operate at 600 lines per minute using a 64-character set or at

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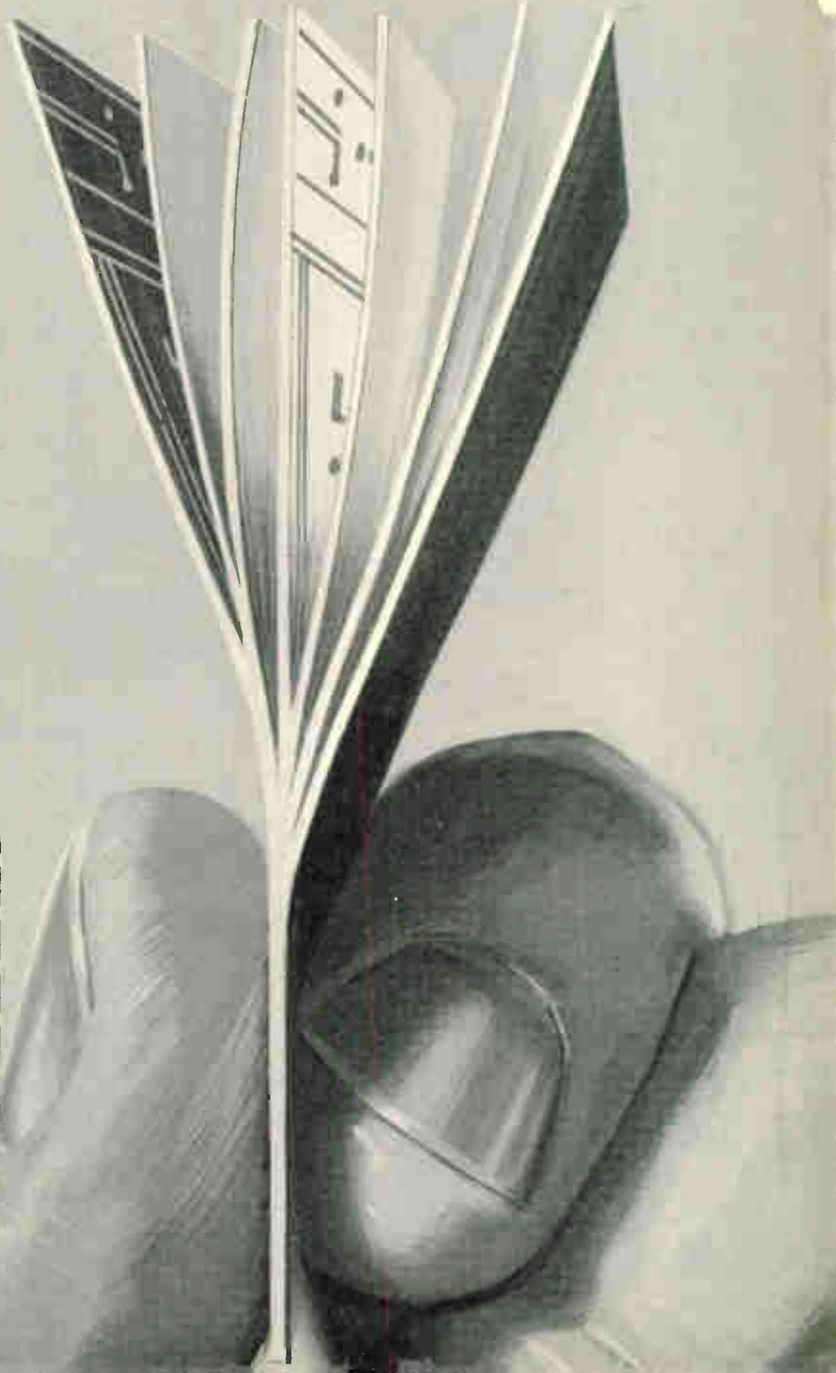

Circle 153 on reader service card

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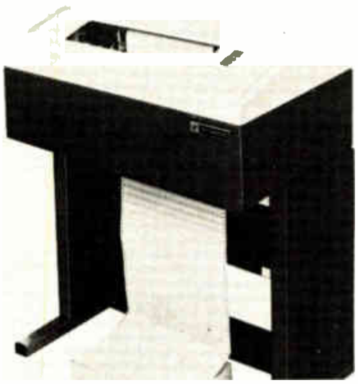

480 lines per minute using a 96-character set. Format is 136 characters per line, 10 characters per line horizontal, and 6/8 line per inch vertical. When used at a speed of 600 lines per minute, the printer accommodates a 9,600-bit-per-second communications rate. Single-line advances and slew rates are in excess of 20 inches per second. Price is under $8,700, with quantity discounts available.

Dataproducts Corp., 6219 De Soto Ave., Woodland Hills, Calif. 91364 [364]

Punched-tape reader transmits to 3,000 b/s

Designed for transferring data from remote to central locations, the Teleterminal is a punched-tape reader that operates on a desktop, table, or bench with any standard telephone-line modem. Teleterminal transmits data from punched tape at up to 3,000 serial bits per second. Rate may be specified as 110, 300, 600, 1,200, 2,400, or 3,000. The reader has an integral power supply and is TTL-, DTL-, and RTL-compatible. It operates with strip or loop and, by use of an adapter, with fanfold applications. Teleterminal uses matched LED/phototransistor sets that read all 5-, 6-, 7-, and 8-level tapes. Price is

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It has been generally assumed that MOS IC memory systems are less expensive and more suitable to use than a ferrite core memories to employ in a field of small-capacity random access memories whose capacities are smaller than 8K bytes.

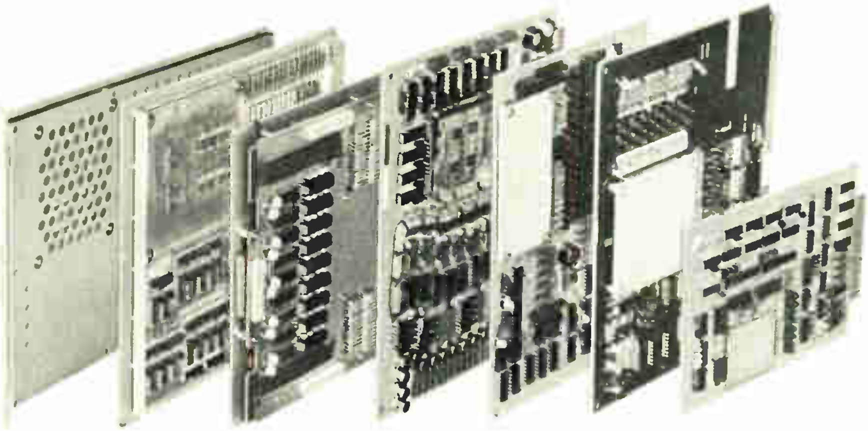
However, today this assumption shall be contradicted. FUJI's new series of memories, Small-capacity Ferrite Core Memory Modules, incorporated with Hybrid integrated circuit as its peripheral circuits, offering a more economical price and better reliabilities rather than MOS IC memories.

Everyone knows that volatility and reliability of stored information is the most important factor in handling of cash transactions at banking system as well as operating cash registers, POS terminal mechines, and on-line devices. Consequently, at least the last digits of calculation must be nonvolatile.

Which do you think is more rational...a system designed by a MOS IC memory with the last calculated digits to be stored by a nonvolatile core memory or a whole entire system simply designed with a nonvolatile core memory? Answer is clear, that is FUJI Core Memory!

STANDARD MODELS

A wide variety of standard models are available over a wide range of memory capacities from 128 words-4 bits to 8K words-9 bits. Furthermore, we are ready to design and manufacture special systems with quick delivery service, according to your requirements.



MODEL	CAPACITY	CYCLE TIME	POWER	DIMENSIONS (size in inch)
CMS2101A	128W-4B	3 μs	±5V	5.8×8.7×0.5
CMS2101B	256W-4B	3 μs	±5V	5.8×8.7×0.5
CMS2112	512W-4B	3 μs	+5V	6.0×8.0×0.5
CMS2113	1024W-4B	3 μs	+5V	6.0×8.0×0.5
CMS2114	2048W-4B	3 μs	+5V	8.0×10.0×0.5
CMS2115	4096W-4B	3 μs	+5V	8.0×10.0×0.5
CMS2116	1024W-9B or 512W-18B	1.5 μs	±5V, +24V	9.8×11.8×0.6
CMS2201A	1024W-10B	1 μs	±5V	9.5×10.5×0.5
CMS2201B	2048W-10B	1 μs	±5V	9.5×10.5×0.5
CMS2107	1024W-18B	1.5 μs	±5V, +24V	7.4×8.3×1.4
CMS2401	4096W-18B or 8192W-9B	1 μs	±5V, +15V	10.0×15.0×0.5
CMS2403	4096W-18B or 8192W-9B	1.5 μs	+5V	10.0×15.0×0.6

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New products

$945. Delivery time is 8 weeks.
Electronic Engineering Co. of California, 1441 E. Chestnut Ave., Santa Ana, Calif. 92701 [366]

Push-button switches are rated at 2 A or 100 mA

The S190 series of lighted push-button switches for terminals and keyboards, offer DPDT operation in momentary action, priced at $1.62 each, and in alternate action at $1.92 each in quantities of 1,000 pieces. Employing dual wiping contacts, switch capability is 100,000 cycles at 2 amperes resistive, and

250,000 cycles at 100 mA resistive. Widely spaced silver-inlaid terminals accept either two #22 AWG soldered wires or 0.110-inch quick-connect receptacles. Neck bushings are provided for subpanel installations, and front-panel mounting is accomplished with any of five adapters.
Clare-Pendar Co., Box 785, Post Falls, Idaho 83854 [367]

Serial printer handles 30 characters per second

An asynchronous serial printer, called the Mark II, includes a split platen, which independently drives two forms. Other features include tabulation to any one of 64 positions. Printing speed is 30 characters per second, with 192 characters in one line. The printer can produce up to five copies, and offers red and black printing. Its adjustable pin-fed tractors provide flexibility in the use of forms.
Litton ABS, OEM products division, 34 Maple Ave., Pine Brook, N.J. 07058 [365]

16K x 18 = more core in Fabri-Tek's reliable 600 Series

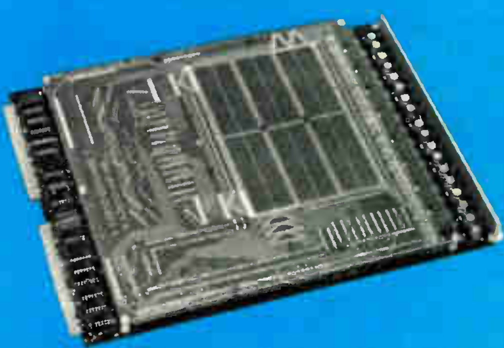
We have an addition to our 600 Series! It's the Model 686 Core Memory System with a basic module capacity of 16K x 18. Like all 600 Series models, the 686 combines off-the-shelf availability with reliable performance and minimum cost.

Modular constructed, ferrite core memories permit operation of up to eight modules in a single enclosure. Developed for a wide variety of data storage applications, the entire 600 Series is completely compatible with TTL logic. So, check the specifications, then specify the 600 Model that best fits your application.

The 620 Core Memory System

Capacity of 1,024 words by 10 bits on a single card. Planar 3-D, 4-wire configuration measures 6.0 x 6.4 inches. Expandable. Access time: 350 nanoseconds. Full cycle time: 1.0 usec.

The 684 Core Memory System



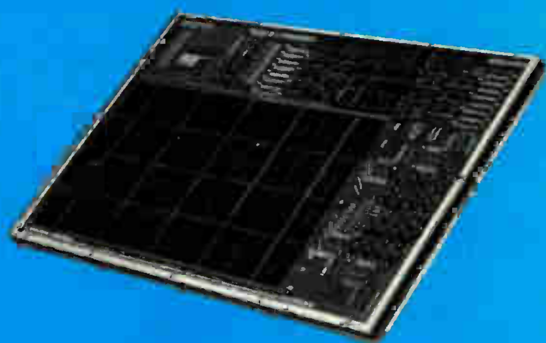
Basic module capacity of 8,192 words by 18 bits on a single card. Expandable to 32K x 36, 64K x 18 or 128K x 9 bits. Planar 3-D, 3-wire configuration measures 11.0 x 14.75 inches. Access time: 300 nanoseconds. Full cycle time: 650 nanoseconds. System options include: enclosures with printed circuit back panels, power supplies and test exerciser, and 250 nanosecond access time option.

The 686 Core Memory System

NEW

Basic module capacity of 16,384 words by 18 bits on a single card. Expandable to 64K x 36, 128K x 18 or 256K x 9 bits. Planar 3-D, 3-wire configuration measures 11.625 x 20.0 inches. Access time: 350 nanoseconds. Full cycle time: 750 nanoseconds. System options include: enclosures with printed circuit back panels, power supplies and test exerciser.

The 688 Core Memory System



Basic module capacity of 32,768 words by 20 bits on a single card. Expandable to 128K x 40, 256K x 20, or 512K x 10 bits. Planar 3-D, 3-wire configuration measures 15 x 21.5 inches. Access time: 500 nanoseconds. Full cycle time: 1.2 microseconds. System options include: enclosures with printed circuit back panels, power supplies and test exerciser.

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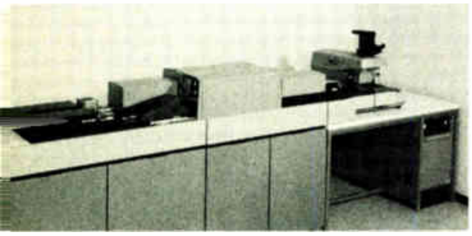
Packaging & production

Wafer processes are automated

Photoresist, other modules complete automatic front-end fabrication systems

A continuing goal of semiconductor manufacturers is to increase production and yield while decreasing time and costs in the wafer-fabrication process. The key, of course, is automation. And now the Cobilt division of Computervision Corp. has developed three additional processing modules that make possible a series of in-line front-end fabrication systems, designated Autofab, for about $100,000.



Designed modularly to allow semiconductor makers to phase gradually into fully automated fabrication, the major individual components of Autofab include:

- The model 1501 single-track coat/bake or develop/bake processor, a stand-alone unit that automates the processes of wafer coating (or developing) and either soft or hard baking.
- The model AF 1101 single-track coater/developer, containing a proprietary new spinner for coating wafers with photoresist or dispensing developers.
- The model AF-1201 single-track baking oven, a compact oven with 50-wafer capacity in an over-all length of only two feet.

Multiple-track units of each model contain up to four independent processing tracks mounted side by side in the same cabinet. Combining these components with two other Cobilt products on the market—the Autolign automatic mask-alignment/exposure system and the AF-520 Autoload load/unload system—make possible a fully automatic in-line fabrication system.

Cobilt offers this system in two configurations: the model AF-2100, a straight-through system combining a load station, spin-coater, soft-bake oven, Autolign mask aligner, spin developer, hard-bake oven, and unload station, in addition to the model AF-2200, a "U-track" system that performs the same functions as the AF-2100, but which has the develop/bake track in the same cabinet as the coat/bake track. This forms the "U" configuration: wafers travel from left to right as they approach the Autolign and return to the unload station from right to left.

In initial tests of the system, Cobilt engineers report substantially higher throughput than present techniques provide. Typical rates are 100 to 150 an hour and as many as 180 wafers an hour occasionally. The system is designed to process wafers up to 4 inches in diameter.

Cobilt offers substantial yield improvement, depending on the stability and refinement of the rest of the wafer-fabrication process. While good yield averages are hard to pin down, Cobilt officials say that a company with an already dependable production capability can expect improvements of 8% to 20% by using the Autofab process.

The new four-foot long oven in the Autofab offers consistent baking uniformity because of a special rotary transport design, plus high density—as many as 50 wafers in process at any given time. Power demand is 300 to 600 watts.

The coater/developer, equipped with its own solid-state controller, is designed for fully automatic operation while applying various solutions to the wafer surface. It provides complete flexibility of process control—variable acceleration spin speeds as high as 10,000 revolutions per minute and the ability to program up to three solvent sprays and two applications of photoresist. Total length is four feet.

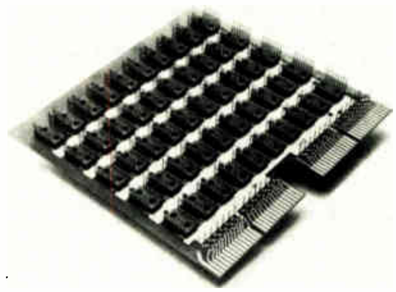
The coat/bake or develop/bake processor consists of seven major assemblies: a solid-state control module; load and unload stations for standard 23-wafer carriers; a new spinner for dispensing solvents, photoresists or developers; a bake oven with a capacity of 50 wafers, and a storage buffer for emptying the oven during downstream slowdowns. It is seven feet long.

Cobilt officials expect the Autofab line to be in full production during the first quarter of 1975 and say that, when in production, the entire system could be sold for about $100,000. Stand-alone subsystem prices are expected to range from $20,000 to $45,000.

Cobilt division of Computervision Corp., 1135 E. Arques Ave., Sunnyvale, Calif. 94086 [391]

Socket panel permits close board-to-board spacing

A single-sided wire-wrap socket panel is available on a custom design basis so that any size and configuration is possible. Board-to-board center spacing is as small as 12.7 mm or 0.500 inch. The unit is

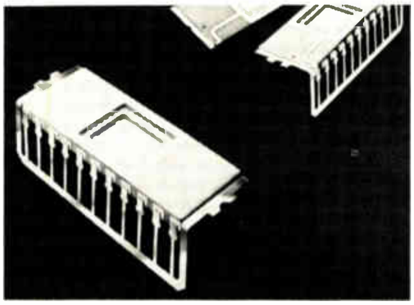


compatible with two-sided printed-circuit-board centers, permitting direct interface with existing back panels.

Augat Inc., 33 Perry Ave., Attleboro, Mass. 02703 [394]

Side-brazed DIP designed to house 2k and 4k RAMs

A 22-lead side-brazed DIP with an extra large rectangular cavity of 0.220 by 0.285 inch is designed for housing 2,048-bit and 4,096-bit MOS RAMs. The package is formed from layers of 94% alumina tape, metalized in the green state, then laminated and high-temperature-fired to produce a rugged, monolithic, ceramic body. Hermeticity of 1×10^{-8} cubic centimeters per second of helium is achieved because all metalized feedthroughs from internal cav-



ity to external braze pads are buried within the body walls. Kovar or alloy-42 leads are supplied as standard. The package is available spot-plated, with gold applied only to such critical areas as dice-attach pad, wire-bonding fingers, and cover-seal ring. This is accomplished by recently developed selective gold-plating equipment.

Metalized Ceramics Corp., Huntington Industrial Park, Providence, R.I. [393]

Laser trims resistors at low operating cost

A laser that trims resistors to desired tolerances uses air-cooled tungsten-halogen pump lamps, which cost about 10 cents per hour to operate. (Most laser resistor-trimmers are said to require $1-per-hour Krypton lamps.) Designated the model 607, the unit produces 1¼ watts of out-

put power, single traverse mode, at a 5-kilohertz repetition rate when Q-switched. Continuous-wave output is 1½ W, transverse electromagnetic mode, and 10 W multimode. Price is less than $5,500 for the cw version and under $10,000 with Q-switching.

GTE Sylvania, Laser Products Department, Box 188, Mountain View, Calif. 94042 [398]

Wafer developer can also be used as an etcher

The model K-1124X is designed especially for developing silicon wafers at high production rates. One feature of the system is a balanced fan-spray aspirator, which provides a uniform pattern over all the wafers. Other features include explosion-proof components, Teflon

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	Price	
Rating	EM	SCR
6V-600A	$1,900	$2,200
7.5V-300A	1,200	1,400
10V-250A	1,200	1,400
10V-500A	1,900	2,200
20V-125A	1,100	1,300
20V-250A	1,500	1,800
20V-500A	2,300	2,700
30V-100A	1,100	1,300
30V-200A	1,500	1,800
40V-60A	1,100	1,300

	Price	
Rating	EM	SCR
40V-125A	$1,400	$1,700
40V-250A	2,100	2,500
50V-200A	2,300	2,700
80V-30A	1,100	1,300
80V-60A	1,400	1,700
100-100A	2,300	2,700
120V-20A	1,100	1,300
120V-40A	1,400	1,700

	Price	
Rating	EM	SCR
160V-15A	$1,100	$1,300
160V-30A	1,400	1,700
160V-60A	2,100	2,500
250V-10A	1,100	1,300
250V-20A	1,500	1,800
250V-40A	2,300	2,700
500V-5A	1,400	1,600
500V-10A	1,900	2,200

19" Rack, 20" depth. Voltage and current adjustable over wide range.

See EEM Vol. 1, Pages 673, 674, 675 for additional product information.

E/M

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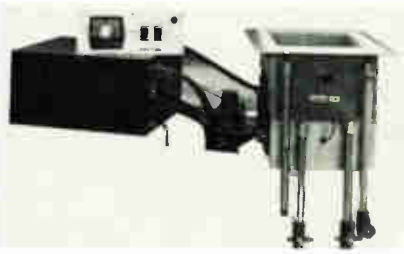
valves, solution delay, cycle overlap, and a choice of turntables. A 10-cycle programable controller is standard, with a four-cycle controller available as an option. With modifications, the K-1124X can also be used as an etcher.

Fluoroware Systems Corp., 335 Lake Hazeltine Dr., Chaska, Minn. 55318 [397]

Ultrasonic etch system uses very hot bath

Designed for semiconductor process applications, the model 24 ultrasonic etch system uses a hot bath for hydrofluoric etching of wafers. In other systems, where acid reaches the silicon, the hydrogen outgassing that occurs could affect the uniformity of the etch process, but model 24 drives out hydrogen bubbles and provides full control over etching uniformity. The use of ultrasonics also permits the slope of the etch to be controlled.

Collins Machinery Corp., 2565 Cloverdale Ave., Concord, Calif. 94520 [399]



Subassemblies

Lead-acid cell finds its niche

Charging, supply circuitry make battery suitable for portable instruments

Despite long shelf-life, low cost, and high ampere-hour capacity, modern sealed and gelled lead-acid batteries have not caught on with makers of portable instruments and communications equipment. Yet they appear to fit well in the applications niche between nickel-cadmium cells, which are appropriate for relatively short discharge intervals, and disposable carbon-zinc cells, best suited for low-drain or intermittent usage.

Engineers at Seven Sciences Inc. think they know why lead-acid batteries have not caught on: there are problems in properly interfacing the batteries with both charging and power-supply circuitry. And they think they have a solution—the CellMate 1000 cyclic battery power supply. Manufactured by the company's new CellMate division, the CellMate 1000 includes both charging circuitry and power-supply circuitry.

The charging circuitry accepts ac voltages from 105 to 125 V and 210 to 250 V at any frequency from 48 to 440 hertz, as well as dc voltages from 18 to 36 V To minimize recharging time without damaging the battery, the charging proceeds in three stages: constant-current charging at a current of about three times the 20-hour discharge current; constant-voltage charging during which 14 V is placed across a 12-V battery to rapidly finish the charging while cleansing the cells of impurities that might damage the plates if not removed; and a float stage, during which a voltage of 13.2 V keeps the battery fully charged without damaging it.

The power-supply circuitry, which regulates the output of the battery, includes a dc-to-dc converter for generating either ±12 or ±15 V dc. In addition to the ±12- or ±15-V supplies, the CellMate can provide a supply of +5 V and an auxiliary +9-V supply, or +6 V with an auxiliary +11-V supply. The CellMate comes in four different total-power ratings—1.5, 4.5, 9, and 20 watts.

Various features of the CellMate can be eliminated to minimize size, weight, and cost. The dc-to-dc converter can be eliminated, as can the auxiliary output. This would leave the basic +5- or +6-V regulated supply. Overload protection to prevent damage to all outputs, even under continuous short-circuit conditions, is standard on all models, the company points out.

Special overvoltage protection, to prevent damage to load circuitry, is optional. Finally, the capability of running off ac can be eliminated, when it is known that dc recharging power will always be available to the user.

Because of the large number of options, pricing can vary widely. The cheapest system can cost as little as $59 in single units, and the most expensive one as much as $207. Discounts as high as 55% are available for quantities of 1,000 and up, and smaller discounts are available for smaller quantities of the battery power supply.

Delivery time is 30 days for most models.

CellMate Division, Seven Sciences Inc., 933 Kifer Rd., Sunnyvale, Calif. 94086 [381]

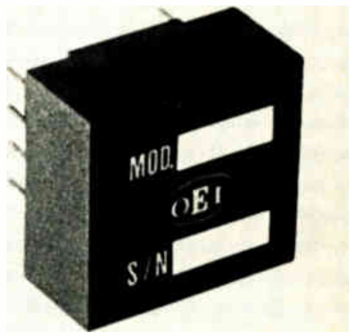
Voltage sources are digitally programed

Two modular, digitally programed voltage sources are designed to be used in automatic computer-controlled test equipment and process control systems, as well as in laboratory applications. Designated the models 4800 and 4801, the units are compatible with most minicomputers. They combine a d-a converter with a high-power output stage, digitally programable current limit and output ranges, storage resistors, current sense output, and digital output flags to indicate current limiting and voltage setting. Small-quantity price is $650. Delivery is from stock to four weeks.

Burr-Brown Research Corp., International Airport Industrial Park, Tucson, Ariz. 85706 [386]

Op amp provides 200-MHz gain-bandwidth product

The model 9829 operational amplifier provides a 200-megahertz gain-bandwidth product and unity gain frequency at a power-supply current level of less than 7 milliamperes on ±15-volt supplies. The device is designed for use in portable, battery-operated equipment, where differential input, wide bandwidth, and a

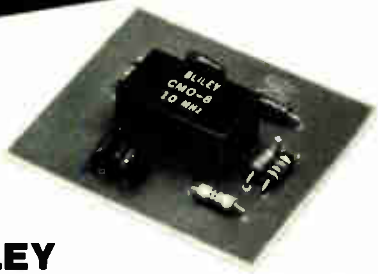


moderately fast slewing rate are required. Other specifications include a 110-dB minimum common-mode rejection, an 80-dB minimum open-loop gain, and a temperature range from -55 to +100°C. Price ranges from $46.50 to $57.50, depending on quantity.

Optical Electronics Inc., Box 11140, Tucson, Ariz. 85734 [384]

Power supply is designed for self-scan displays

Meant for use with the Burroughs Corp. self-scan displays, the model 9760-PS power supply operates a 16- or 32-character array, with or without memory, and also powers



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Write Gould Inc., Instrument Systems Division, 3631 Perkins Avenue, Cleveland, Ohio 44114. Or Kouterveldstraat Z/N, B 1920 Diegem, Belgium.

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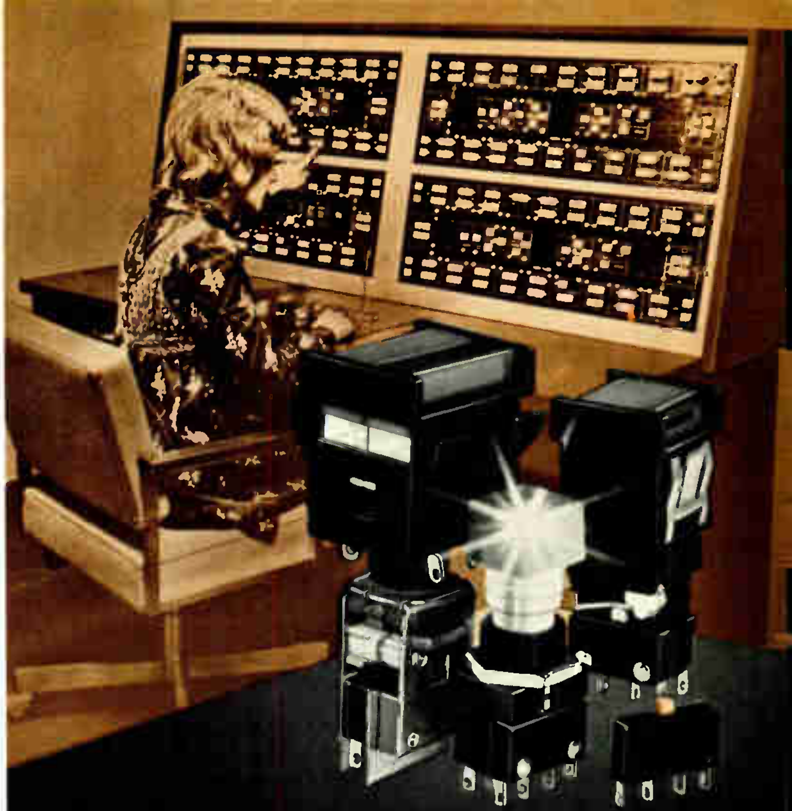

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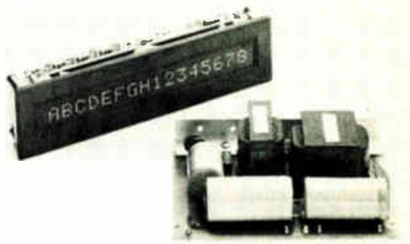
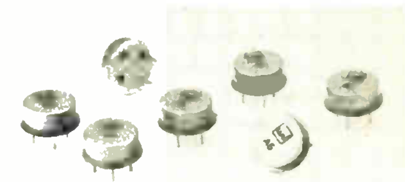


additional TTL or MOS circuitry. Output voltages are 250 V dc at 30 mA, −12 V dc at 200 mA and 5 V dc at 1 A. An optional −5 V dc output is also available. All output voltages are regulated within 5% for an input of 105 to 125 V ac. Price is $96.

Texas Digital Systems Inc., Box 3701, Bryan, Texas 77801 [385]

Cascadable amplifiers are rated from 5 to 500 MHz

The models A5 and A7 cascadable amplifiers, rated at from 5 to 500 megahertz, are stable for any source and load condition. The integrated devices cascade up to four stages to



achieve a typical gain of 58 decibels and a typical flatness of ±0.5 dB. The application of either 15 V dc to the A5 or 24 V dc to the A7 produces a gain of 14.5 dB and a gain flatness of less than ±0.3 dB, in addition to a VSWR of less than 1.2 (input) and less than 1.5 (output). Price of the A5 is $99; and of the A7, $109.

Watkins-Johnson Co., 3333 Hillview Ave., Palo Alto, Calif. 94304 [387]

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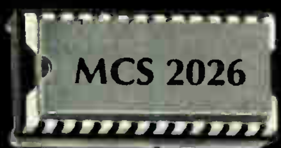

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7 x 10 x 32	MCS 2020	$11.00

HEADQUARTERS — Applications Mgr.: Mr. Julius Hertsch; MOS Technology, Inc., Norristown, Pa. 19401

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EASTERN REGION — Mr. William Whitehead, Suite 307 — 88 Sunnyside Blvd., Plainview, N.Y. 11803 • (516) 822-4240

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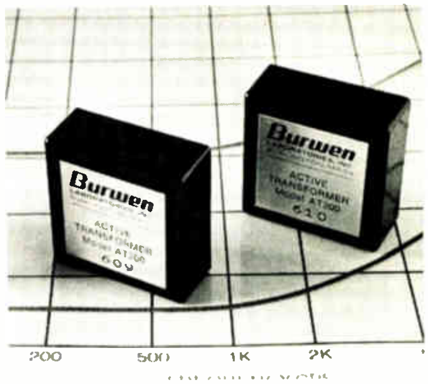
performance, the model AT200 solid-state transformer links electrically isolated circuits, solves both gain and impedance problems, and passes 360-kilohertz signals. Moreover, the unit performs these functions with a low harmonic intermodulation distortion, immunity to

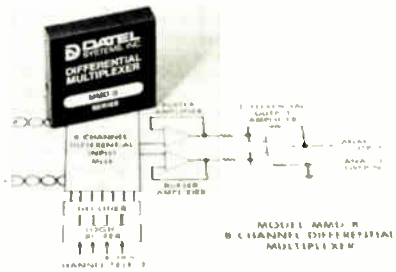


interference, high input impedance, and differential or single-ended operation. The transformer handles signals down to dc levels and is priced at $200 each.

Burwen Laboratories Inc., 209 Middlesex Turnpike, Burlington, Mass. 01803 [389]

Differential multiplier uses eight pairs of analog switches

The model MMD-8 differential multiplexer consists of eight pairs of analog switches. Each pair is switched simultaneously through two buffer amplifiers into a true differential-input, singled-ended output amplifier. The output pair from the analog switches, the inputs and outputs of the two buffer amplifiers, and the differential amplifier are all brought out to the pins. The analog switches and amplifiers can be used separately if desired. In addition,



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Senior Development Engineer
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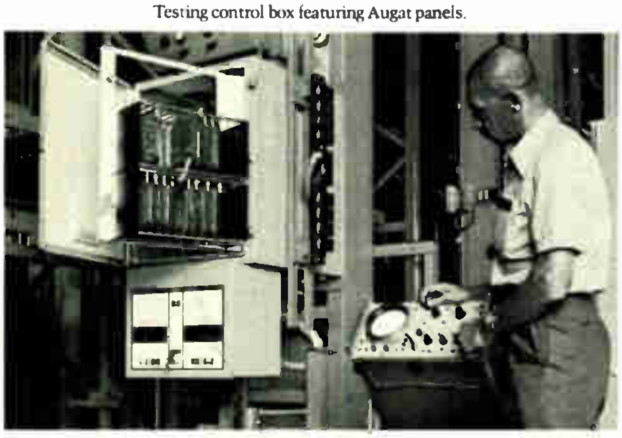

Chuck Bates

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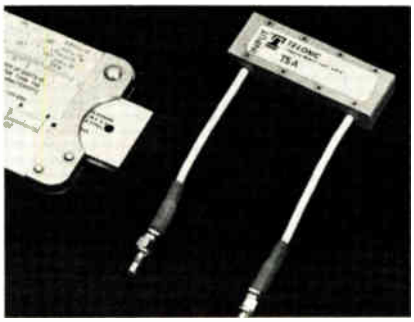
Europe—Augat International, Inc., Boulevard A. Reyers, 103, 1040 Brussels, Belgium, Tel. (02) 36-93-99.
Japan—Kyokuto Boeki Kaisha Ltd., New Otemachi Bldg., 2-1, 2-Chome Otemachi, Chiyoda-Ku, Tokyo 100-91, Japan, Tel. (03) 244-3788.

the MMD-8 offers good transfer characteristics with high-speed break-before-make switching. A channel select inhibit (all channels off) is provided so that two MMD-8s can be stacked to provide 16 channels of differential analog multiplexing. Differential input signals up to ±10 volts can be accepted by the MMD-8. Without the amplifiers, switching time is typically 500 nanoseconds, while the output settling time of the amplifier is 4 microseconds. Price is $169.

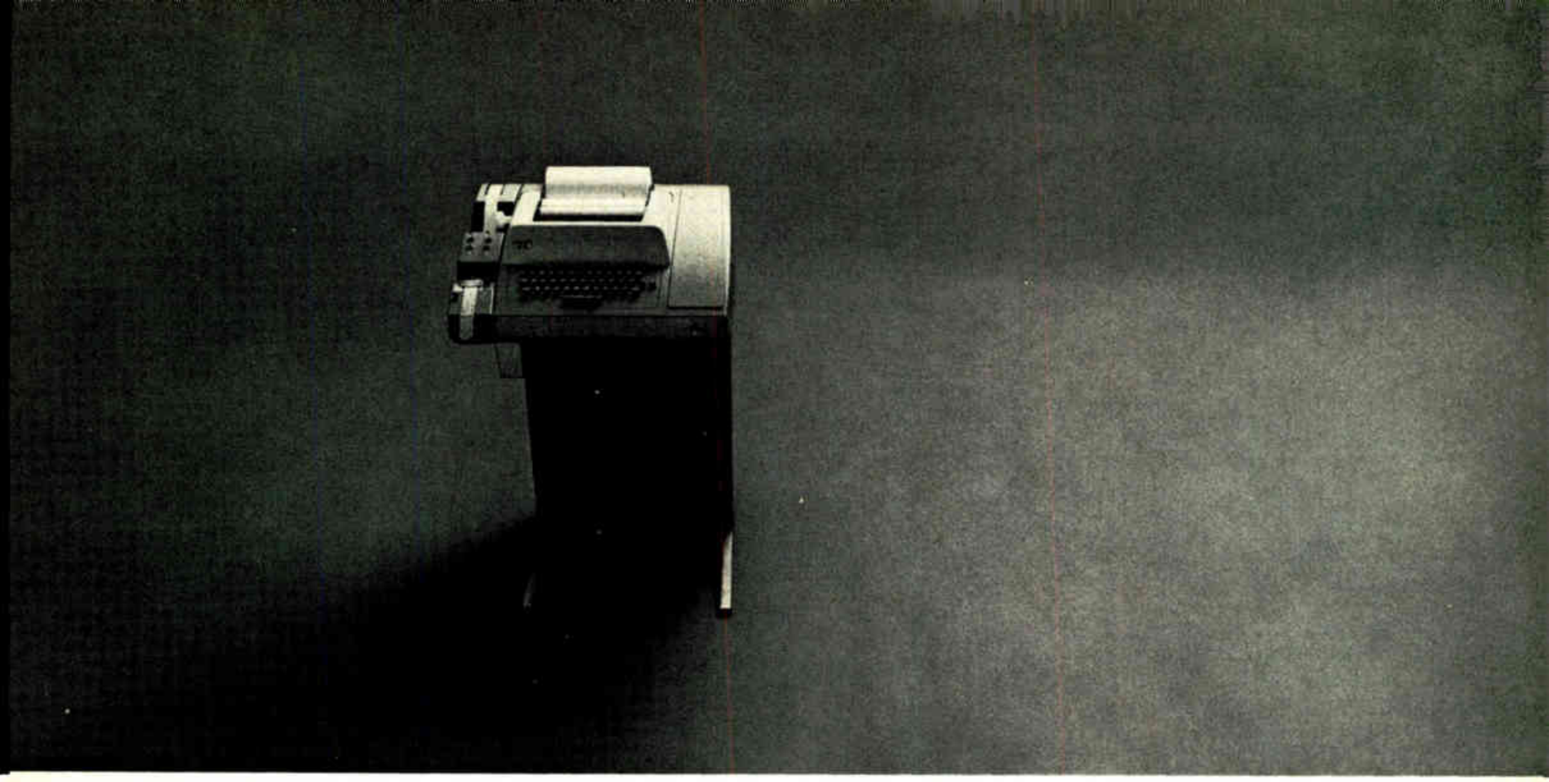
Datel Systems Inc., 1020 Turnpike St., Canton, Mass. 02021 [388]

Subminiature filter handles peak power up to 30 watts

A series of subminiature filters of .01-dB Chebyshev design offers center frequencies from 200 to 600 MHz and handles peak powers of 1 to 30 watts. Designated model TSA, the new filter is constructed with a magnetically coupled resonator design and may be specified with two to eight sections, depending on bandwidth and other characteristics desired. In cross-section, the filter measures ⅓ in. by 11/16 in. and is 2 to 3-½ in. long, length being a function of the number of sections and pass bandwidth. Input and output connectors may be specified as Sealectro, or OSM, or any combination, and may be located at ends or sides. Minimum 3-dB bandwidths range from 1.0 to 15%, also depending on the number of sections. Price ranges from $150 to $300.



Telonic Industries Inc., Box 277, 21282 Laguna Canyon Rd., Laguna Beach, Calif. 92652 [390]



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Circle 171 on reader service card

New literature

SCR gate drives. Vectrol Inc., 1010 Westmore Ave., Rockville, Md. 20850, has issued a four-page catalog covering the Phasetrol series of SCR gate drives and regulator control modules. The line includes feedback amplifiers, current limiters, lockout circuits, and current-voltage regulators, all offered in either plug-in or panel-mounted versions. Circle 421 on reader service card.

Test equipment. A 64-page catalog describing electronic test equipment, including oscilloscopes, pulse generators, and voltmeters, has been published by Baynton Electronics Corp., 2709 N. Broad St., Philadelphia, Pa. 19132. Specifications, prices and general information are given. [422]

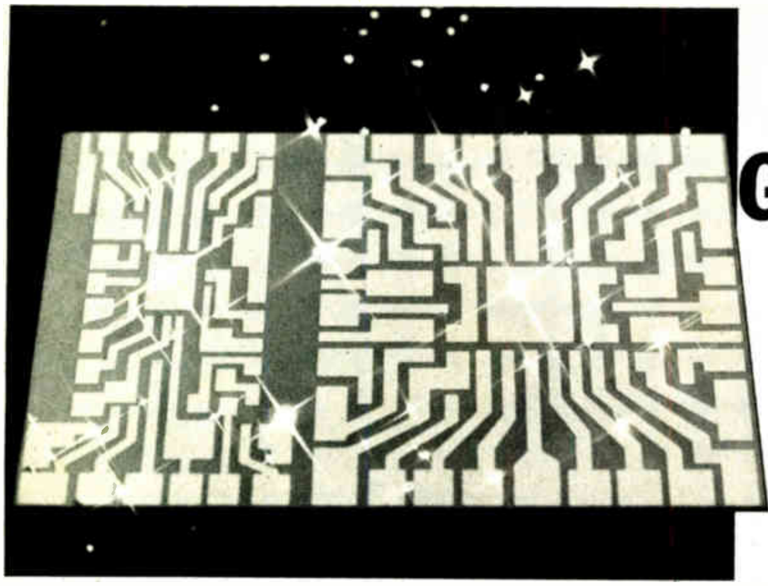
Laminates. Dynthane-Taylor, Valley Forge, Pa. 19482. A 12-page brochure gives details of a line of glass-base laminates that can be used with any method of circuit manufacture. [423]

Power supplies. A technical bulletin from Induction Process Equipment Corp., 32251 N. Avis Dr., Madison Heights, Mich. 48071, describes the Statiron line of heating inverter power supplies that convert low-frequency ac line current to rf ac current. [424]

Breadboarding equipment. A 20-page catalog of circuit design and breadboarding equipment from E&L Instruments Inc., Derby, Conn., features the ADAM modular breadboarding system, two op-amp designers, socket boards, and other equipment. [425]

Microwave products. Texas Instruments Incorporated, Box 5012, MS-84, Dallas, Texas 75222. Bulletin CB-161 describes a line of beam-lead microwave semiconductors, which include p-i-n switching diodes, Schottky barrier mixer diodes, and capacitors with Jedec values. [426]

Silicon rectifiers. International Rectifier Corp., Semiconductor division, 233 Kansas St., El Segundo, Calif.



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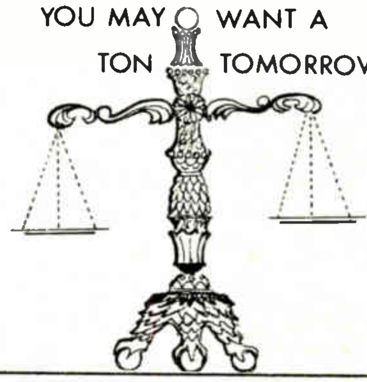

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New literature

90245, has issued a data sheet describing three versions of a 6-ampere medium-power silicon rectifier. [427]

Transducers. Technical bulletin 1001A from Schaevitz Engineering, Box 505, Camden, N.J. 08101, provides information and a selection guide for ac- and dc-operated linear variable differential transformers. [428]

Film deposition. Scientific Gas Products Inc., 513 Raritan Center, N.J. 08817. Information is provided in a technical bulletin on the deposition of silicon-nitride and silicon-dioxide films on prepared gallium-phosphide substrates. The bulletin also describes how to achieve fast growth rates at low temperatures. [429]

Ceramic capacitors. Republic Electronics Corp., 176 E. 7th St., Paterson, N.J. 07524, has made available catalog K-1, which describes the line of Mucon subminiature ceramic capacitors. [430]

Digital panel meters. A package of updated data sheets describing the 11 series of digital panel meters is obtainable from Electronic Research Co., Box 913, Shawnee Mission, Kan. 66201. [432]

Oscilloscopes. Nicolet Instrument Corp., 5225 Verona Blvd., Madison, Wis. 53711. "The General Purpose, High Precision, Digital Oscilloscope" is the title of a 12-page technical brochure that discusses design, operation, midsignal trigger, display capabilities, accuracy, resolution, and interfacing techniques when digital electronic components are used in oscilloscopes. [433]

Microwave diodes. Unitrode Corp., 580 Pleasant St., Watertown, Mass. 02172, lists the specifications of a line of microwave diodes in a six-page catalog. [434]

Converter modules. A two-page data sheet describing digital-to-synchro converter modules is available from Astrosystems Inc., 6 Nevada Dr., Lake Success, N.Y. 11040. [435]

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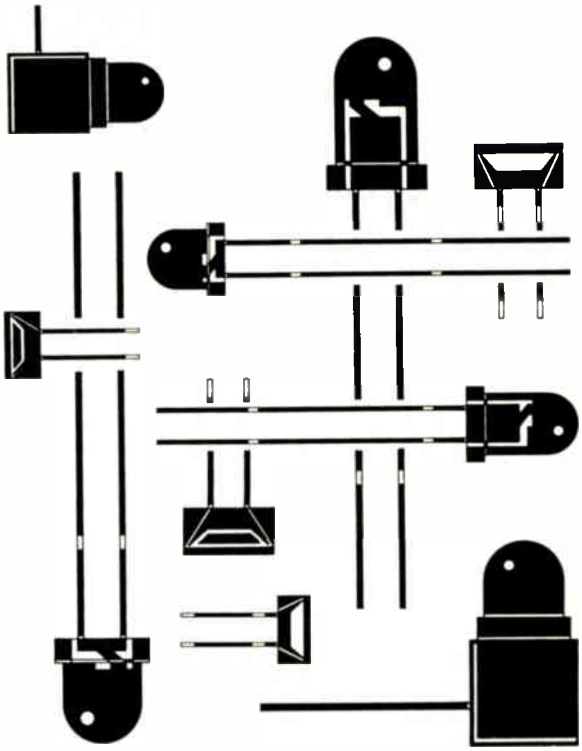

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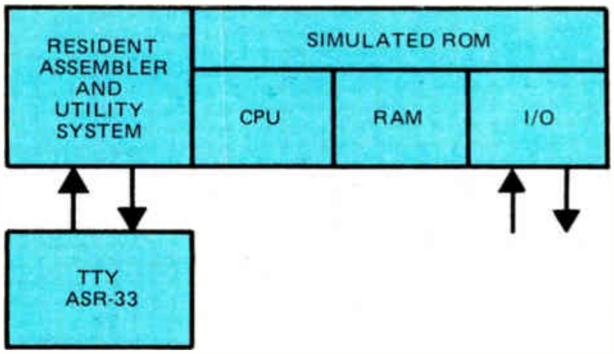

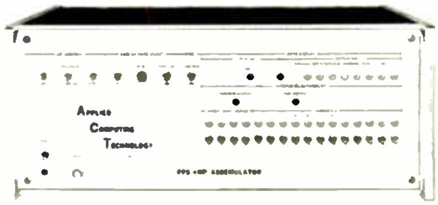

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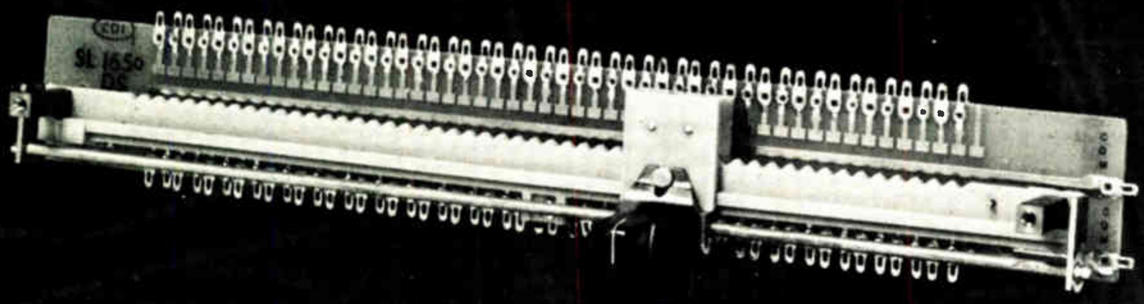

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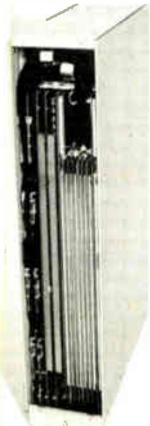
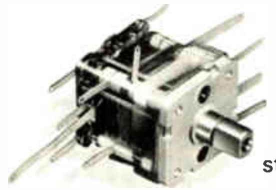


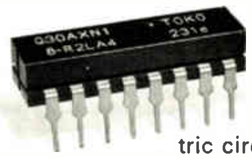
A high-speed, large-capacity, low-cost memory bank designed for use as the main memory in medium-to-large computers and various data processing systems. Access time operating speed, 200ns; cycle speed, 350ns. Memory capacity, 65k bytes Memory capacity readily increased by combining as many HS-200S II units as desired.

Polyethylene Capacitor



The CY2 Series polyethylene variable capacitor is highly stable and only 20mm square. It was developed by challenging the limits of parts precision and by making radical improvements over all existing products.

Pulse Transformer Dual In-Line



IC circuits are currently replacing all other electric circuits. There is also an increasing demand to combine active as well as activated elements into identical IC packages. In particular, the Dual In-Line Package (DIP) is gradually becoming the standard for IC packages. Used in electronic computers and other electronic machinery.

EXCELLENT SET WITH TOKO PARTS

TOKO, INC.

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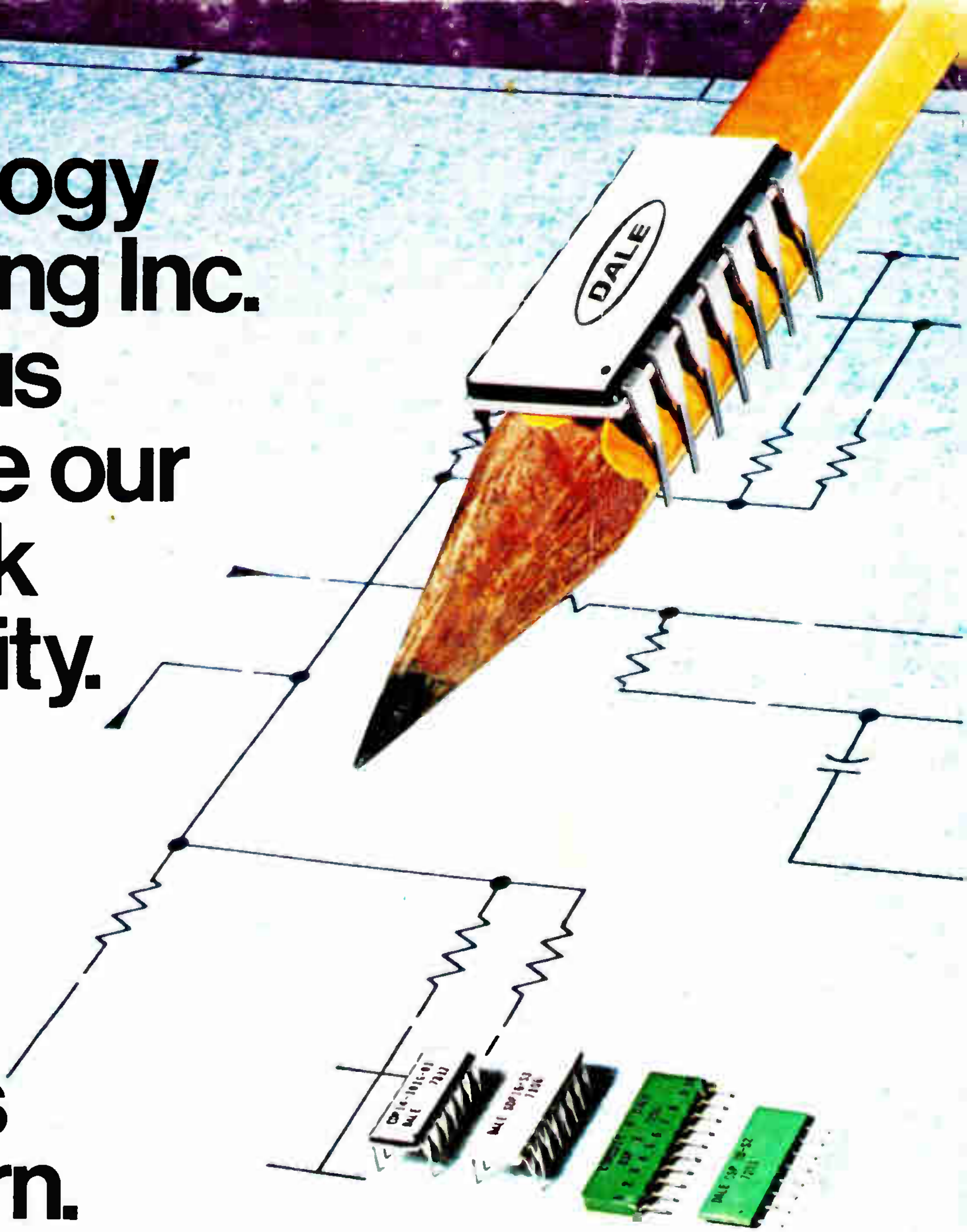
Technology Marketing Inc. asked us to prove our network capability.



Now it's your turn.

Respected computer systems developers like Technology Marketing Incorporated are making good use of Dale's thick film network capabilities. The network above is used to set threshold voltage and provide termination for two sense windings in a P.C. layout compatible with 7500 Series memory sense amplifiers. It has been used effectively in high volume production memory and computer systems developed by Technology Marketing Inc.

Standard or Special, Dale can provide the resistance function you need...in the quantities and at the price you require. Make us prove it.

Models immediately available for these and many other standard functions:

- MOS/ROM pull-up/pull-down
- Open collector pull-up
- "Wired OR" pull-up
- Power driver pull-up
- High speed parallel pull-up
- TTL unused gate pull-up
- TTL input pull-down
- Digital pulse squaring
- Line termination
- Long line impedance balancing
- LED current limiting
- ECL output pull-down resistors
- TTL input

Power Rating: 1/8 watt max./resistor; 2 watts/package (single in-line); 1-1/2 watts/package (DIP).

Resistance Range: 10 ohms to 1 Meg., depending on tolerance.

Tolerance: 1%, 2%, 5%, 10%, 20%.

T.C.: ±200 ppm/° C.

Packaging: Flame retardant epoxy coating or sandwich-type ceramic construction.

Double width and discrete networks also available in standard or special designs.

For complete information, call your Dale representative or phone 402-371-0080.

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