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volume three

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185

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Editor: Jan Vernon
Editor-in-chief: Roger Harrison
Layout: Bill Crump

Managing editor: Collyn Rivers

CONTENTS

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Voltage and window comparators

Comparators are circuits in which the output changes state when the input varies above or below a set limit, or within two limits. Applications abound.

Ray Marston

THERE ARE MANY occasions in electronics when it is necessary to have a circuit that abruptly changes its output stage when an input voltage, or a quantity that can be represented by a voltage (such as a current, resistance, temperature or light level, etc), goes above or below a preset reference value. Circuits that perform this basic function are known as voltage comparators.

Voltage comparators have plenty of practical applications apart from the obvious ones of over and under-voltage switches. They can readily be made to activate relays, alarms and other mechanisms when load currents or temperatures or light levels exceed, or fall within, preset limits, and have a stack of domestic and industrial uses. We'll look at some practical circuits in the next few pages.

Basic voltage comparator circuits

The easiest way to make a voltage comparator is to use a CA3140 op-amp in one or other of the basic configurations shown in Figures 1 and 2. The 3140 op-amp has a typical basic

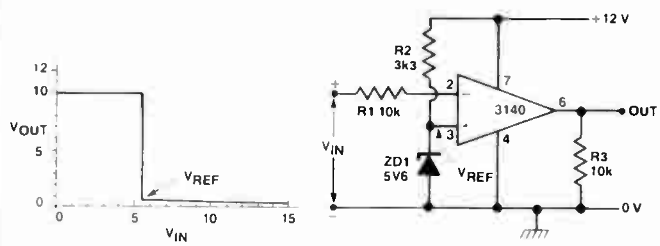


Figure 1. **Basic op-amp comparator that functions as an under-voltage switch: the output is high when Vin is below Vref.**

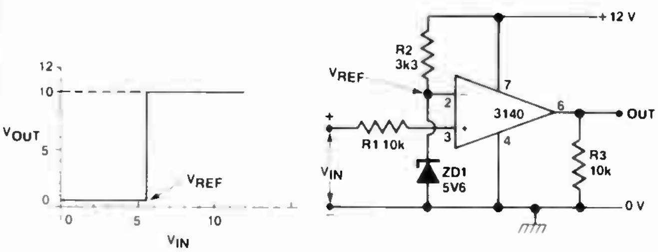


Figure 2. **Alternative op-amp voltage comparator that functions as an over-voltage switch: the output is high when Vin is above Vref.**

(open-loop) low frequency voltage gain of about 100 dB, so its output can be shifted from the high to the low state (or vice versa) by shifting the input voltage a mere 100 uV or so above or below the reference voltage value. This particular op-amp can be powered from either single-ended or split supply rails and provides an output that typically swings to within a couple of volts of its positive rail value or to within a few millivolts of its negative (or zero) supply rail value: Unlike many other op-amps, the 3140 can accept input voltages all the way down to the negative rail value.

The operation of the Figure 1 circuit is very simple. A fixed reference voltage (Vref) is generated via R2-ZD1 and is applied directly to the non-inverting input terminal (pin 3) of the op-amp, and the test or input voltage is applied to the inverting input terminal (pin 2) via current-limiting resistor R1. When Vin is below Vref the op-amp output is driven high (to positive saturation), but when Vin is above Vref the output is driven low (to negative saturation) as shown in the diagram. The action of the circuit can be reversed, so that the op-amp output is normally low but goes high when Vin exceeds Vref, by simply transposing the pin 2 and pin 3 connections of the op-amp, as shown in Figure 2.

There are a few points worth noting about the basic single-supply Figure 1 and Figure 2 3140 voltage comparator circuits. The first point is that the 'reference' voltage can be given any value from zero up to within two volts of the positive supply rail value, so either circuit can be made to trigger at any desired value between these limits by simply interposing a preset pot between a fixed voltage-reference source and the 'Vref' pin of the op-amp.

The second point to note is that the 'input' pin of the op-amp must be constrained to the range from zero volts up to within two volts below the positive supply rail value. Thus, if you want the circuit to trigger at some high value of input voltage, this action can be obtained by feeding the input voltage to a simple potential divider before it reaches the actual input of the op-amp.

The final point to note about the basic voltage comparator circuits is that they give a non-regenerative switching action, so that the op-amp is driven into the linear (non-saturated) mode when the 'input' voltage is within a few tens of microvolts of Vref, and under this circumstance the op-amp output generates lots of spurious noise. In some applications this type of action may be unacceptable, in which case the problem can be overcome by feeding a small part of the op-amp output voltage back to the non-inverting input terminal, so that a regenerative switching action is obtained. The feedback signal introduces a degree of hysteresis in the voltage switching levels, the degree of hysteresis being directly proportional to the amount of feedback.

Special voltage comparators

Figures 3 to 7 show how the three points mentioned above can be put to practical use to make various types of 'special' voltage comparator circuits; plenty of other variations are possible.

Figures 3 and 4 show how the basic comparator circuits can be modified to give variable-voltage switching by using a pre-set pot (PR1) to set the desired 'reference' or trigger voltage at any value in the range 0 — 5V6, and to give regenerative ('noiseless') switching by feeding part of the op-amp output back to the non-inverting terminal via R3; note in the Figure 4 circuit that the input terminal is terminated via R5, to ensure controlled hysteresis.

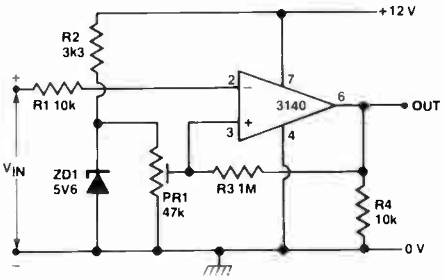


Figure 3. **Variable under-voltage switch with degenerative feedback overcomes intermediate-voltage problems with Figure 1 and 2 circuits.**

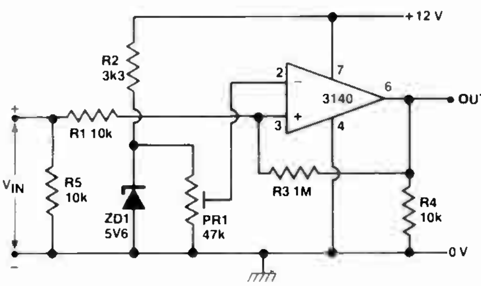


Figure 4. **Variable over-voltage switch with regenerative feedback.**

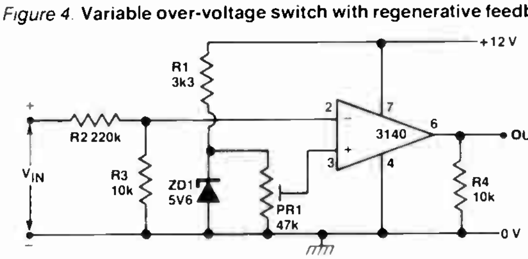


Figure 5. **High value (0 — 130 V) under-voltage switch.**

Figures 5 and 6 show examples of how the circuits can be modified to give high-value variable-voltage (0 — 130 V) triggering by interposing a simple potential divider (R2-R3) between the input signal and the input of the op-amp: The Figure 5 circuit gives non-regenerative switching, while the Figure 6 circuit gives regenerative switching.

Finally, Figure 7 shows how the comparator can be used as a sensitive audio sine-square converter that can operate from input signal amplitudes as low as 10 mV peak-to-peak at 1 kHz and which produces decent squarewave outputs from sinewave inputs with frequencies up to about 15 kHz. Input impedance is 100k.

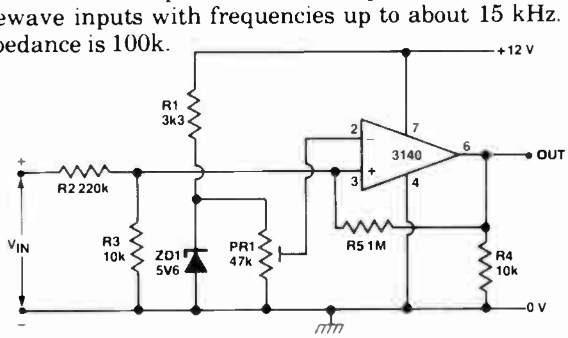


Figure 6. **High value (0 — 130 V) regenerative over-voltage switch.**

The operation of the Figure 7 circuit is simple. Voltage divider R1-R2 and capacitor C2 apply a decoupled reference voltage to pin 2 of the op-amp and an almost identical voltage is applied to signal-input pin 3 via isolating resistor R3. When a sinewave is fed to pin 3 via C1 it swings pin 3 about the pin 2 reference level, causing the op-amp output to change state at

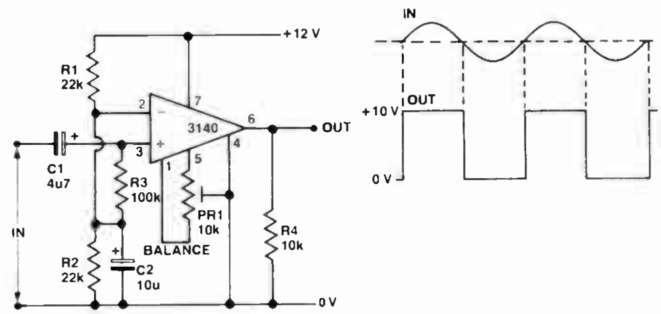


Figure 7. **This sensitive sine-square converter needs only a few tens of millivolts of input signal to produce a decent squarewave output up to about 15 kHz.**

the 'zero voltage difference' crossover points of the input waveform and produce a squarewave output. Preset pot PR1 is used to bias the op-amp so that its output is just pulled low with zero input signal applied, so that the circuit operates with maximum sensitivity and stability. Note that, because of the gain-bandwidth product characteristics of the op-amp, the circuit sensitivity decreases as the input frequency is increased.

Window comparators

The voltage comparator circuits that we've looked at so far give an output transition when the inputs go above or below a single reference voltage value. It's a fairly simple matter to interconnect a pair of voltage comparators so that an output transition is obtained when the inputs fall between, or outside of, a *pair* of reference voltage levels. Figure 8 shows the basic circuit configuration, which is generally known as a *window comparator* or *discriminator*.

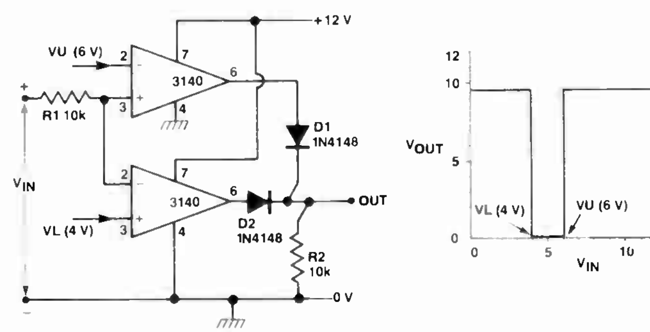


Figure 8. **A voltage window comparator or discriminator. The output goes high when Vin goes outside of the V_L or V_U limits.**

The action of the Figure 8 circuit is such that the output of the upper op-amp goes high when Vin exceeds the six volt V_U 'upper limit' reference value, and the output of the lower op-amp goes high when Vin falls below the four volt V_L 'lower limit' reference value. By feeding the outputs of the two op-amps to R4 via the D1-D2 diode OR gate we get the situation where the final output is low when Vin is within the limits set by V_U and V_L, but goes high whenever the input goes beyond these limits.

The action of the Figure 8 circuit can be reversed, so that its output goes high only when the input voltage is within the 'window' limits, by taking the output signal via a simple inverter stage. Alternatively, the required action can be obtained by transposing the two reference voltages and taking the output via a diode AND gate, as shown in Figure 9.

Window discriminators can readily be made to activate from any parameter that can be turned into an analogue voltage, in the same way as a 'normal' voltage comparator can. They can thus be used to activate relays or alarms whenever temper-

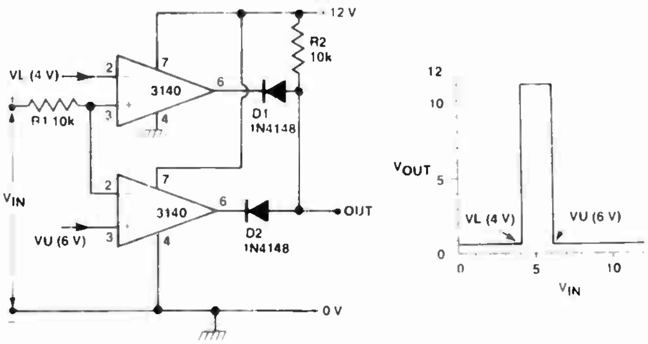


Figure 9 An alternative window discriminator in which the output goes high when Vin falls between the two limits.

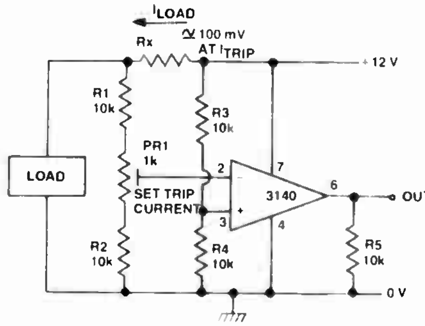


Figure 10 An over-current switch: the output goes high when the load current exceeds a preset value. The action can be reversed by transposing pins 2 and 3 of the op-amp.

atures, voltages, currents or light levels etc. go outside of preset limits. Let's look now at some examples of 'analogue-activated' comparator circuits.

Analogue-activated comparators

Figure 10 shows how a comparator circuit can be made to function as an over-current switch that gives a high output when the load current exceeds a value preset via PR1; the value of Rx is chosen so that it develops roughly 100 mV at the required trip current level. A fixed half-supply 'reference' voltage is fed to pin 3 of the op-amp via R3-R4 and a similar but current-dependent voltage is fed to pin 2 via Rx-R1-PR1-R2; in effect, these two sets of components are configured as a Wheatstone bridge, with one side feeding pin 3 and the other side feeding pin 2, and the op-amp is used as a bridge-balance detector; consequently, the trip points of the circuit are not significantly influenced by supply voltage variations but are highly sensitive to load current variations.

Note that the action of the Figure 10 circuit can be reversed, so that it functions as an undercurrent switch, by simply transposing the connections to pins 2 and 3 of the op-amp. The circuit can then be used as a lamp or load-failure indicator in cars or in test gear, etc.

Figure 11 shows the circuit of a sensitive ac over-voltage switch, which gives a high output when the input signal exceeds a peak value (6 mV to 111 mV) preset via PR1. The ac input signal is applied to the input of non-inverting variable gain amplifier IC1, which has its gain variable from x45 to x850 via PR1. Note that the input of IC1 is dc-grounded via R1-R2, so the op-amp responds only to the positive half-cycles of the input signal. Consequently, the output of IC1 is an amplified but positively half-wave rectified version of the input signal; this signal is peak-detected via R5-D1-C2-R6-R7 and fed to the input of non-inverting voltage comparator IC2, which thus gives a positive output when the C2 voltage exceeds the value on the junction of R8-R9.

Figures 12 to 15 show a variety of ways of using comparator circuits as light or temperature-activated switches. All of these circuits use a light or temperature-sensitive transducer (and LDR or cadmium sulphide photocell for light, or a negative-temperature-coefficent thermistor for temperature) as the sensing element and use the element as one arm of a Wheatstone bridge and the op-amp as a simple bridge-balance detector so that the 'trip' point of each circuit is independent of supply line variations. In all cases, the sensing element must have a resistance in the range 5k to 100k at the required 'trip' point and PR1 is chosen to have the same resistance value as

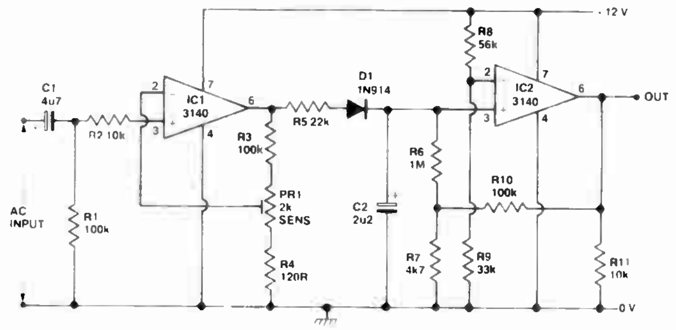


Figure 11 This ac over-voltage switch can be triggered by input signals in the range 6 mV to 111 mV peak.

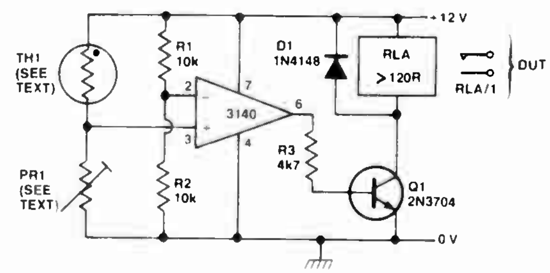


Figure 12 Precision over-temperature switch with transistor/relay output.

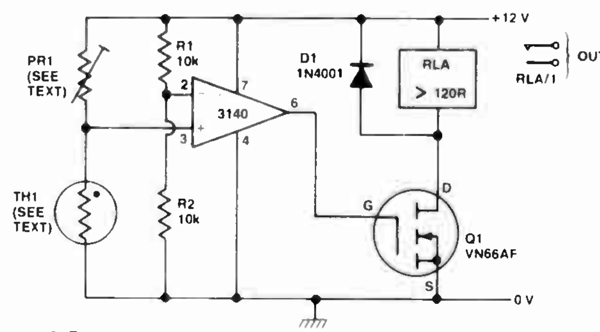


Figure 13 Precision under-temperature switch with VFET/relay output.

the sensing element at the required trip level.

The Figure 12 to 15 circuits also show a variety of ways of using the output of the op-amp to activate a relay or to generate an acoustic alarm signal. Thus, the Figure 12 over-temperature switch has a transistor-driven relay output, while the Figure 13 under-temperature switch has a VFET-driven relay output. Similarly, the light-operated switch circuit of Figure 14 generates a monotone alarm output signal in a small speaker, while the dark-operated switch of Figure 15 generates a low-power pulsed-tone signal in a small piezo-electric transducer.

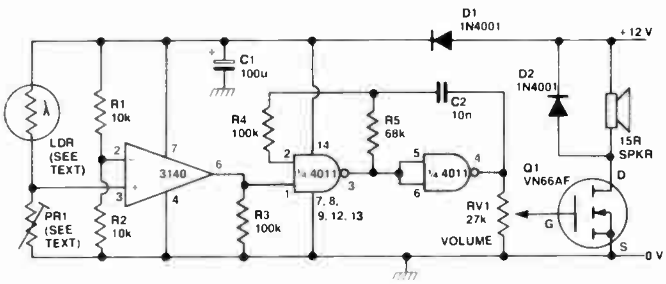


Figure 14. **Light-operated switch with monotone alarm output.**

Micro-power operation

All of the 3140-based comparator circuits that we have looked at so far are continuously powered; they draw continuous currents of about 4 mA per op-amp and will thus flatten a small 9 V battery in less than two days of continuous operation. These circuits are thus not well suited to battery operation in 'portable' applications. In practice, however, all of these circuits can easily be modified for long-life battery operation by using a micro-power 'sampling' technique: the principle can be explained with a simple example, as follows.

The Figure 13 under-temperature switch circuit monitors temperature continuously and draws about 5 mA of quiescent current (with the relay off). In reality, however, temperature is a slowly-varying parameter and thus does not need to be monitored continuously; instead, it can be efficiently monitored by briefly 'inspecting' or 'sampling' it (by connecting the supply power and inspecting the op-amp output) only once every second or so; if the sample periods are very brief (say 300 uS) relative to the sampling interval (one second), the *mean* current consumption of the monitor can be reduced by a factor equal to the interval/period ratio (e.g: by a factor of 3300) by using the sampling technique, so that, for example, the 5 mA consumption of the Figure 13 circuit can be reduced to a *mean* value of a mere 1.6 uA, thus giving years of continuous operation from a 9 V battery. The 'sampling' technique thus enables true micro-power monitor or comparator designs to be implemented.

Figure 16 shows the basic circuit of a 'micro-power' or sampling version of the Figure 13 under-temperature switch, which operates the relay when the TH1 temperature falls below a preset value but which draws a mean quiescent current of only a few uA. The TH1-PR1-R1-R2-IC1 monitor network is almost identical to that of Figure 13, but instead of being continuously powered it is powered via a 300 uS pulse just once every second via a sample-pulse generator and Q1.

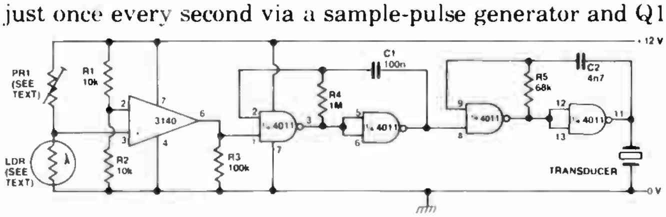


Figure 15. **Dark-operated switch with low-power pulsed-tone output.**

Note that the output of IC1 is fed to temporary 'memory' store R4-C1 via D1, and that the memory store operates the relay via VFET Q2.

Thus, if the TH1 temperature is outside of the trip level when the sample pulse arrives, IC1 output will remain low and no charge will be fed to C1, so Q2 and the relay will be off, but if the TH1 temperature is within the trip level when the sample pulse arrives the IC1 output will switch high for the duration of the pulse and thus rapidly charge C1 up via D1 and thence drive the relay on via Q2; the C1 charge will then easily hold the relay on until the arrival of the next sample pulse.

The Figure 16 circuit, then, illustrates the basic principles of the micro-power sampling technique. In reality the sampling interval and pulse-width used (and thus the reduction in mean power consumption) will depend on the specific application. If, for example, you wish to monitor transient changes in light or sound levels and know that these transients have minimum durations of 100 mS, you may have to use a 50 mS sampling interval and (say) a 500 uS sample pulse, in which case the mean consumption of your circuit will be reduced by a factor of 100.

In some cases you may have to slightly modify the operating principle of the sampling circuitry to obtain the desired micro-power operation. Figure 17, for example, shows how the

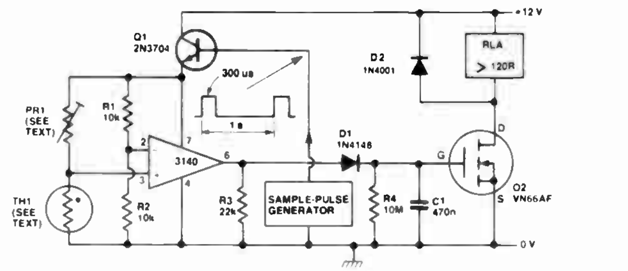


Figure 16. **This micropower or 'sampling' version of the Figure 13 under-temperature switch draws a mean quiescent current of only a few microamps.**

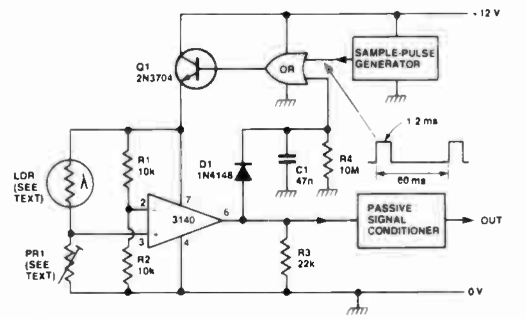


Figure 17. **This coded light beam detector circuit uses a modified version of the micropower 'sampling' technique.**

principle may be adapted to make a coded lightbeam detector, in which the 'code' light signal is modulated at 1 kHz for a minimum duration of 100 mS. Thus, the sample-pulse generator is designed to produce a minimum pulse width of 1.2 mS so that it can 'capture' at least one full 1 kHz code cycle, and the sampling interval is set at 60 mS so that part of a tone burst will always be captured. The sampling circuitry thus gives a 50:1 reduction in monitor current consumption.

Thus, in the Figure 17 circuit, the sample generator repeatedly feeds 1.2 mS 'inspection' pulses to the 3140 detector circuitry via one input of the OR gate and via Q1 to see if any trace of a coded signal exists. If no trace of a code signal is detected the output of the op-amp remains low and another sample pulse is applied 60 mS later, but if a trace of a code signal *is* detected the output of the op-amp immediately switches high and the resulting pulse is 'captured' by C1 via D1 and applied to the remaining input of the OR gate, thereby temporarily applying *full* power to the 3140 circuitry so that the code signal can be properly inspected via the passive signal conditioning circuitry to see if it conforms to the specified 'code' characteristics.

Note that, for a sampling system to be truly efficient, the actual sample-pulse generator must itself consume negligible current and may thus have to be a non-standard design. We'll show some possible suitable circuits in the next edition of 'Circuit File'. ●

Using the 4007UB 'FETset' IC

The 4007UB comprises two pairs of complementary MOSFETs and a simple MOSFET inverter stage, all independently accessible, which makes this simple IC a very versatile chip indeed.

Ray Marston

THE 4007UB is the simplest chip in the entire CMOS range. It contains little more than two pairs of complementary MOSFETs, plus a simple CMOS inverter stage. All of these elements are, however, independently accessible, enabling them to be configured in a wide variety of ways, thereby making the IC the most versatile in the entire CMOS range.

The 4007UB is an ideal device for demonstrating CMOS principles to students, technicians and engineers. It is sometimes known as the 'design-it-yourself' CMOS chip, and can readily be configured to act as a multiple digital inverter, NAND or NOR gate, transmission gate, or as a uniquely versatile 'micropower' linear amplifier, oscillator or multivibrator. We'll look at some practical examples of these applications later. In the meantime, let's look at 4007UB basics.

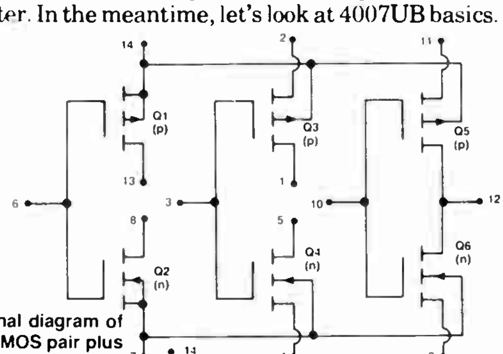


Figure 1a. **Functional diagram of the 4007UB dual CMOS pair plus inverter.**

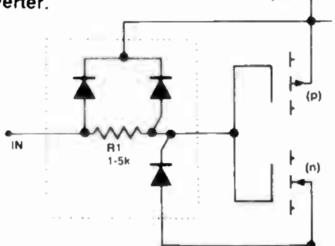


Figure 1b. **Internal input protection network (within dotted lines) on each input of the 4007UB.**

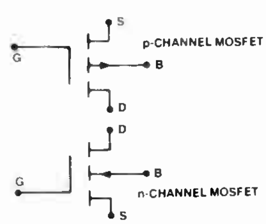


Figure 1c. **MOSFET terminal notations. G = Gate. D = Drain. S = Source. B = Bulk substrate.**

Basics: digital operation

Figure 1a shows the functional diagram and pin numbering of the 4007UB. Each of the three independent input terminals of the IC is internally connected to the standard CMOS protection network shown in Figure 1b. All MOSFETs in the 4007UB are enhancement-mode devices; Q1, Q3 and Q5 are p-channel MOSFETs, and Q2, Q4 and Q6 are n-channel MOSFETs. Figure 1c shows the terminal notations of the two MOSFET types; note that the B terminal represents the bulk substrate.

The term 'CMOS' actually stands for 'Complementary Metal Oxide Silicon field-effect transistors' and it is fair to say that all CMOS ICs are designed around the basic elements shown in Figure 1. It is thus worth getting a good basic understanding of these elements. Let's look first at the digital characteristics of the basic MOSFETs.

The input (gate) terminal of a MOSFET presents a near-infinite impedance, and the magnitude of an external voltage applied to the gate controls the magnitude of source-to-drain current flow. Basic characteristics of the enhancement-mode n-channel MOSFET are that the source-to-drain path is open circuit when the gate is at the same potential as the source, but becomes a near short-circuit (a low resistance) when the gate is heavily biased positive with respect to the source. Thus the

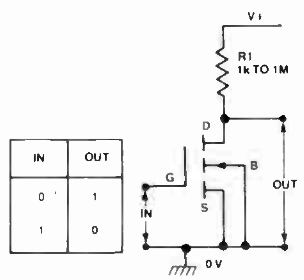


Figure 2. **Digital inverter made from n-channel MOSFET.**

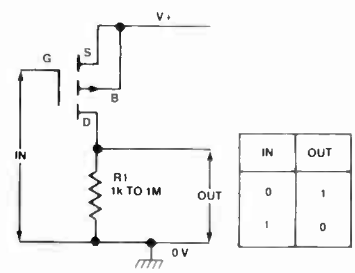


Figure 3. **Digital inverter made from p-channel MOSFET.**

n-channel MOSFET can be used as a digital inverter by wiring it as shown in Figure 2. With a logic 0 (zero volts) input the MOSFET is cut off and the output is at logic 1 (positive rail voltage), but with a logic 1 input the output is at logic 0.

Basic characteristics of the p-channel enhancement-mode MOSFET are that the source-to-drain path is open when the gate is at the same potential as the source, but becomes a near-short when the gate is heavily biased *negative* to the source. The p-channel MOSFET can thus be used as a digital inverter by wiring it as shown in Figure 3.

Note in the Figures 2 and 3 inverter circuits that the *on* currents of the MOSFETs are determined by the value of R1 and that these circuits draw a finite quiescent current when they are in one of their logic states. This snag can be overcome by connecting a complementary pair of MOSFETs in the standard CMOS inverter configuration shown in Figure 4a.

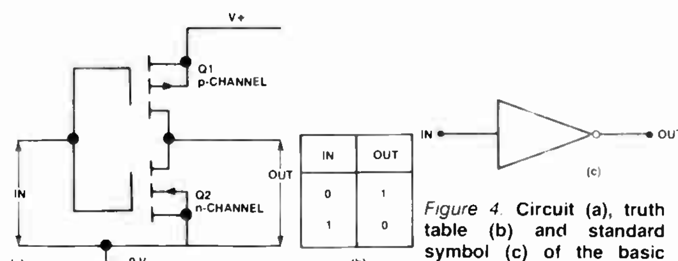
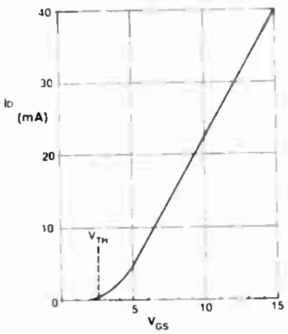


Figure 4. **Circuit (a), truth table (b) and standard symbol (c) of the basic CMOS digital inverter.**

Here, with a logic 0 input applied, Q1 is shorted, so the output is firmly tied to the logic 1 (positive rail) state, but Q2 is open and the inverter thus passes zero quiescent current via this transistor. With a logic 1 input applied, Q2 is shorted and the output is firmly tied to the logic 0 (zero volt) state, but Q1 is open and the circuit again passes zero quiescent current. This 'zero quiescent current' characteristic of the complementary MOSFET inverter is one of the most important features of the CMOS range of digital ICs, and the Figure 4a circuit forms the basis of almost the entire CMOS family. Figure 4c shows the standard symbol used to represent a CMOS inverter stage. Q5 and Q6 of the 4007UB are fixed-wired in this inverter configuration.



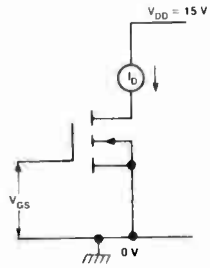


Figure 5. **Typical gate-voltage to drain-current characteristics of an n-channel MOSFET.**

Basics: linear operation

To truly understand the operation and vaguaries of CMOS circuitry, it is essential to understand the linear characteristics of basic MOSFETs. Figure 5 shows the typical gate-voltage to drain-current graph of an n-channel enhancement mode MOSFET. Note that negligible drain current flows until the gate voltage rises to a 'threshold' value of about 1.5 to 2.5 volts, but that the drain current then increases almost linearly with further increases in the gate voltage.

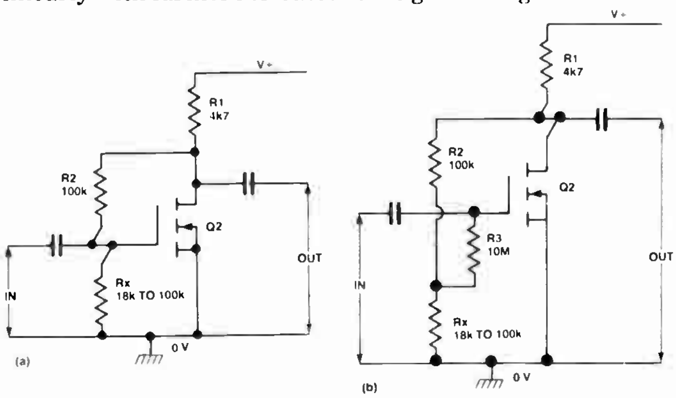


Figure 6. **Methods of biasing an n-channel 4007UB MOSFET for use as a linear inverting amplifier.**

Figure 6 shows how to connect an n-channel 4007UB MOSFET as a linear inverting amplifier. R1 serves as the drain load of Q2 and R2-Rx bias the gate so that the device operates in the linear mode. The Rx value must be selected to give the desired quiescent drain voltage; the Rx value is normally in the range 18k to 100k. If you want the amplifier to give a very high input impedance, wire a 10M isolating resistor between the R2-Rx junction and the gate of Q2, as shown in Figure 6b.

Figure 7 shows the typical I_D to V_{DS} characteristics of an n-channel MOSFET at various fixed values of gate-to-source voltage. Imagine here that, for each set of curves, V_{GS} is fixed at the V_{DD} voltage, but that the V_{DS} output voltage can be varied by altering the value of drain load R_L. The graph can be divided into two characteristic regions, as indicated by the dotted line, these being the triode region and the saturated region.

When the MOSFET is in the saturated region (with V_{DS} at some value in the nominal range 50% to 100% of V_{GS}) the drain acts like a constant current source, with it's current value controlled by V_{GS}. A low V_{GS} value gives a low constant-current value, and a high V_{GS} value gives a high constant-current value. These saturated 'constant-current' characteristics provide CMOS with its short-circuit proof feature and also determine it's operating speed limits at different supply voltage values.

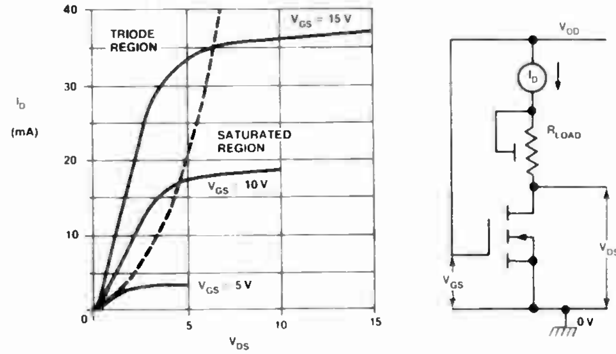


Figure 7. **Typical I_D to V_{DS} characteristics of the n-channel MOSFET at various fixed values of V_{GS}.**

When the MOSFET is in the triode region (with V_{DS} at some value in the nominal range 1% to 50% of V_{GS}) the drain acts like a voltage-controlled resistance, with the resistance value increasing approximately as the square of the V_{GS} value.

The p-channel MOSFET has an I_D to V_{DS} characteristics graph that is complementary to that of Figure 7. Consequently, the action of the standard CMOS inverter of Figure 4 (which uses a complementary pair of MOSFETs) is such that it's current-drive capability into an external load, and also it's operating speed limits, increases in proportion to the supply rail voltage.

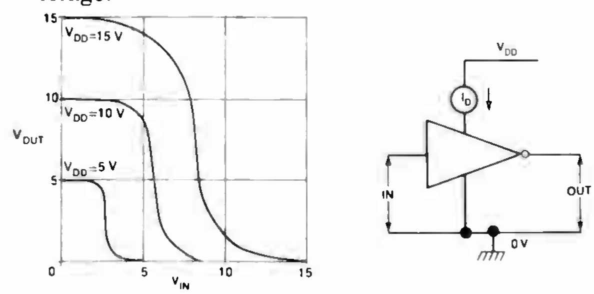


Figure 8. **Typical voltage transfer characteristics of the 4007UB simple CMOS inverter.**

Figure 8 shows the typical voltage-transfer characteristics of the standard CMOS inverter at different supply voltage values. Note (on the 15 V V_{DD} line, for example) that the output voltage changes by only a small amount when the input voltage is shifted around the V_{DD} and 0 V levels, but that when V_{in} is biased at roughly half-supply volts a small change of input voltage causes a large change of output voltage.

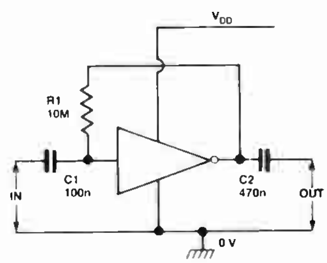
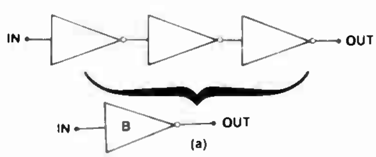


Figure 9 **Method of biasing the simple CMOS inverter for linear operation. Typical gain and bandwidth performance figures are 30 dB and 2.5 MHz at 15 V supply, 40 dB and 710 kHz at 5 V.**

Typically, the inverter gives a voltage gain of about 30 dB when used with a 15 V supply, or 40 dB at 5 V. Figure 9 shows how to connect the CMOS inverter for use as a linear amplifier; the circuit has a typical bandwidth of 700 kHz at 5 V supply, or 2.5 MHz at 15 V. ▶



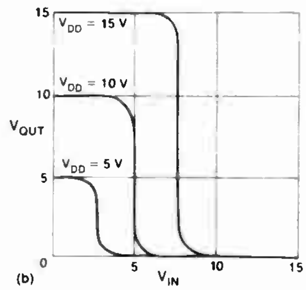
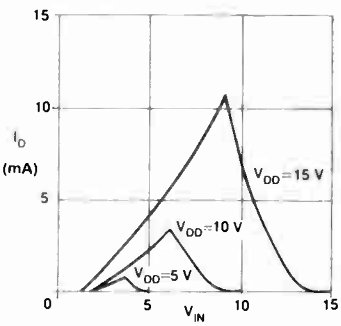


Figure 10. **Wiring three simple CMOS inverters in series (a) gives the equivalent of a B-series 'buffered' CMOS inverter, which has the transfer characteristics shown in (b).**

Wiring three simple CMOS inverter stages in series (Figure 10a) gives the direct equivalent of a modern B-series 'buffered' inverter stage, which has the overall voltage transfer graph shown in Figure 10b. The B-series inverter, typically gives about 70 dB of linear voltage gain, but tends to be grossly unstable when used in the linear mode.



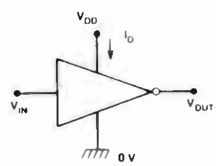


Figure 11. **Drain-current transfer characteristics of the simple CMOS inverter.**

Finally, Figure 11 shows the drain-current transfer characteristics of the simple CMOS inverter. Note that the drain current is zero when the input is at zero or full supply volts, but rises to a maximum value (typically 0.5 mA at 5 V supply, or 10.5 mA at 15 V supply) when the input is at approximately half-supply volts, under which condition both MOSFETs of the inverter are biased on. In the 4007UB, these *on* currents can be reduced by wiring extra resistance in series with the source of each MOSFET of the CMOS inverter; we use this technique in the 'micropower' circuits shown later in this article.

Using the 4007UB

The usage rules of the 4007UB are quite simple. In any specific application, all unused elements of the device must be disabled. Complementary pairs of MOSFETs can be disabled by connecting them as standard CMOS inverters and tying their inputs to ground, as shown in Figure 12. Individual MOSFETs can be disabled by tying their source to their substrate (B) and leaving the drain open circuit.

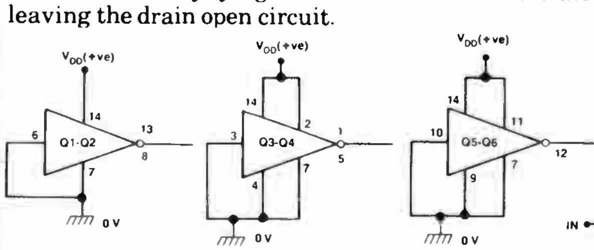


Figure 12. **Individual 4007UB complementary MOSFET pairs can be disabled by connecting them as CMOS inverters and grounding their inputs.**

In use, the input terminals must not be allowed to rise above V_{DD} (the supply voltage) or below V_{SS} (zero volts). To use an n-channel MOSFET, the source must be tied to V_{SS}, either directly or via a current-limiting resistor. To use a p-channel MOSFET, the source must be tied to V_{DD}, either directly or via a current-limiting resistor.

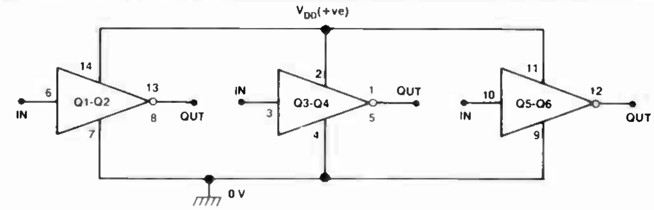


Figure 13. **4007UB triple inverter.**

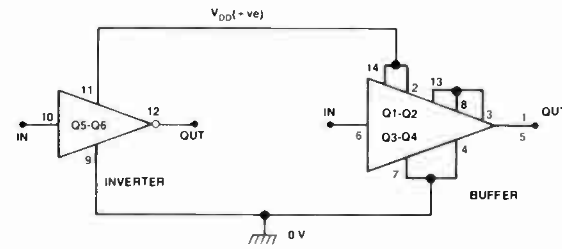


Figure 14. **4007UB inverter plus non-inverting buffer.**

Practical 4007UB circuits: digital

The 4007UB elements can be configured to act as any of a variety of standard digital circuits. Figure 13 shows how to wire it as a triple inverter, using all three sets of complementary MOSFET pairs. Figure 14 shows the connections for making an inverter plus non-inverting buffer; here, the Q1-Q2 and Q3-Q4 inverter stages are simply wired directly in series, to give an overall non-inverting action.

The maximum source (load-driving) and sink (load-absorbing) output currents of a simple CMOS inverter stage self-limit at 10-20 mA as one or other of the output MOSFETs turns fully on. Higher sink currents can be obtained by simply wiring n-channel MOSFETs in parallel in the output stage.

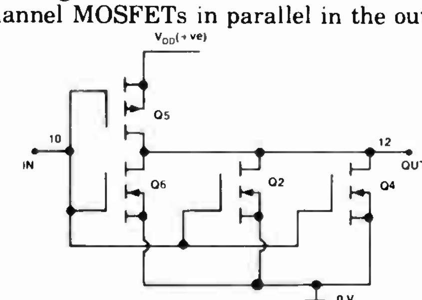


Figure 15. **4007UB high sink-current inverter.**

Figure 15 shows how to wire the 4007UB so that it acts as a high sink-current inverter that will absorb triple the current of a normal inverter. Similarly, Figure 16 shows how to wire the IC to act as a high source-current inverter, and Figure 17 shows the connections for making a single inverter that will sink or source three times more current than a standard inverter stage.

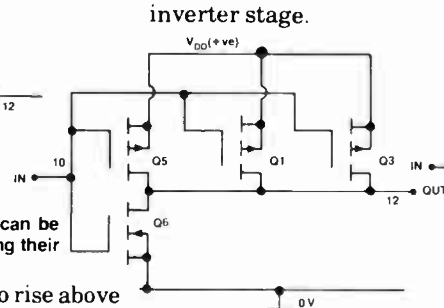


Figure 16. **4007UB high source-current inverter.**

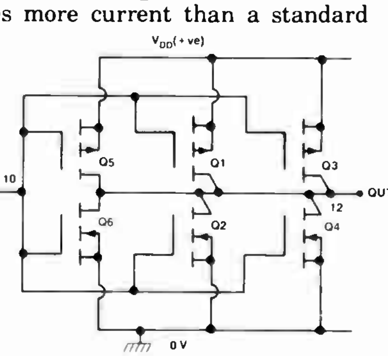
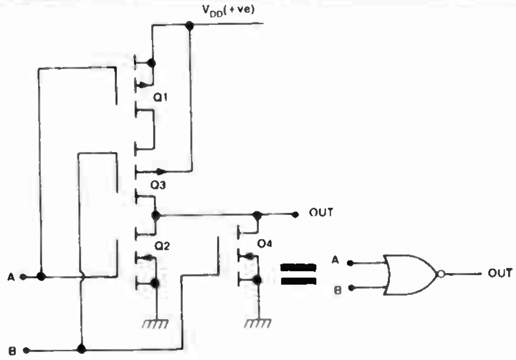


Figure 17. **4007UB high-power inverter, with triple the sink- and source-current capability of a standard inverter.**



A	B	OUT
0	0	1
0	1	0
1	0	0
1	1	0

Figure 18. **4007UB two-input NOR gate.**

The 4007UB is a perfect device for demonstrating the basic principles of CMOS logic gates. Figure 18 shows the basic connections for making a two-input NOR gate. Note that the two n-channel MOSFETs are wired in parallel so that either can pull the output to ground from a logic 1 input, and the two p-channel MOSFETs are wired in series so that both must turn on to pull the output high from a logic 0 input. The truth table shows the logic of the circuit. A three-input NOR gate can be made by simply wiring three p-channel MOSFETs in series and three n-channel MOSFETs in parallel, as shown in Figure 19.

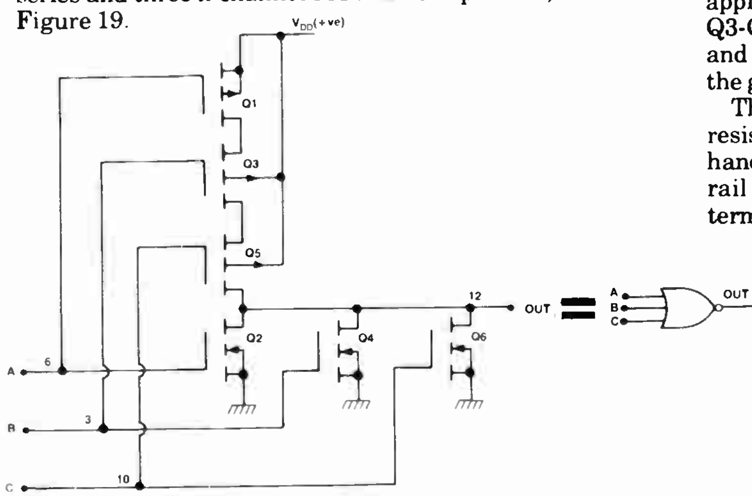
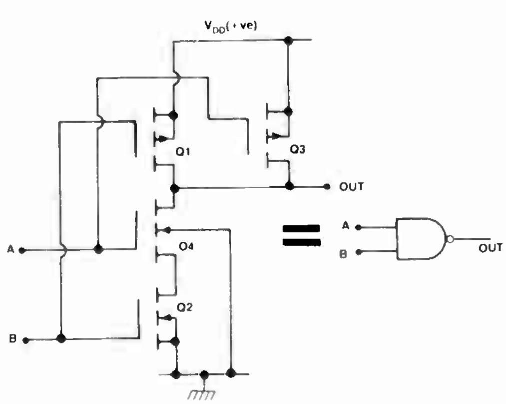


Figure 19. **4007UB three-input NOR gate.**



A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure 20. **4007UB two-input NAND gate.**

Figure 20 shows how to wire the 4007UB as a two-input NAND gate. In this case the two p-channel MOSFETs are wired in parallel and the two n-channel MOSFETs are wired in series. A three-input NAND gate can be made by similarly wiring three p-channel MOSFETs in parallel and three n-channel MOSFETs in series.

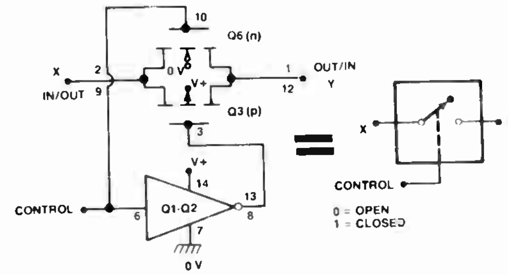


Figure 21. **4007UB transmission gate or bilateral switch.**

Figure 21 shows the basic circuit for using the 4007UB to make another important CMOS element, the so-called transmission gate or bilateral switch. This device acts like a near-perfect switch that can conduct signals in either direction and can be turned on (closed) by applying a logic 1 to the control terminal or turned off (open) via a logic 0 control signal. Here, an n-channel and a p-channel MOSFET are wired in parallel (source-to-source, drain-to-drain), but their gate signals are applied in anti-phase via the Q1-Q2 inverter. To turn the Q3-Q6 transmission gate on (closed), Q6 gate is taken to logic 1 and Q3 gate to logic 0 via the inverter. To turn the switch off, the gate polarities are simply reversed.

The 4007UB transmission gate has a near-infinite OFF resistance and an ON resistance of about 600 ohms. It can handle all signals between zero volts and the positive supply rail value. Note that, since the gate is bilateral, either of its terminals can function as input or output.

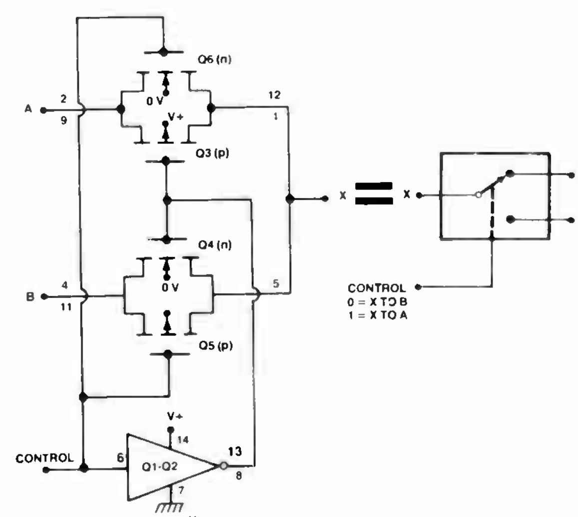


Figure 22. **4007UB two-way transmission gate.**

Finally, Figure 22 shows how the 4007UB can be wired as a dual transmission gate that functions like a single-pole double-throw (SPDT) switch. In this case the circuit uses two transmission elements, but their control voltages are applied in antiphase, so that one switch opens when the other closes, and vice versa; the 'X' sides of the two gates are shorted together, to give the desired SPDT action. ▶

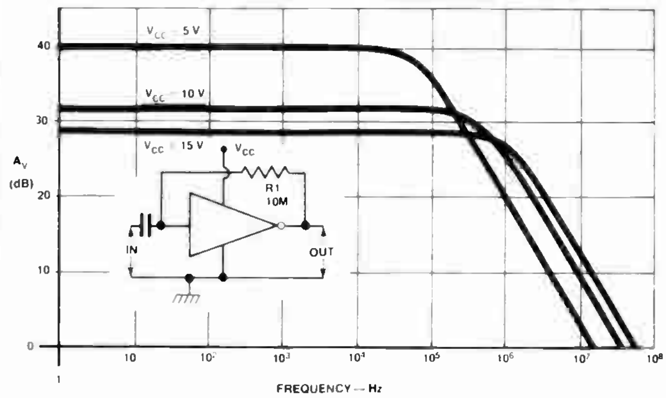
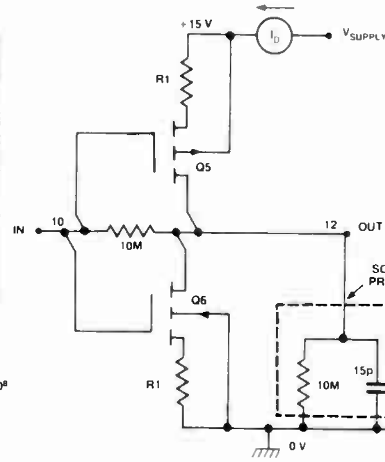


Figure 23. **Typical A_V and frequency characteristics of the linear-mode basic CMOS amplifier.**



R1	I_D	A_V (V_{OUT}/V_{IN})	UPPER 3dB BANDWIDTH
0	12.5 mA	20	2.7 MHz
100R	8.2 mA	20	1.5 MHz
560R	3.9 mA	25	300 kHz
1k0	2.5 mA	30	150 kHz
5k6	600 uA	40	25 kHz
10k	370 uA	40	15 kHz
100k	40 uA	30	2 kHz
1M0	4 uA	10	1 kHz

Figure 25. **'Micropower' 4007UB CMOS linear amplifier, showing method of reducing I_D, with measured performance details.**

Practical 4007UB circuits: linear

We've already seen in Figures 6 and 9 that the basic 4007UB MOSFETs and the CMOS inverter can be used as linear amplifiers. Figure 23 shows the typical voltage gain and frequency characteristics of the linear CMOS inverter when operated from three alternative supply rail values. This graph assumes that the amplifier output is feeding into the high impedance of a 10M/15 pF 'scope probe. The output impedance of the open-loop amplifier typically varies from 3k at 15 V, to 5k at 10 V, to 22k at 5 V, and it is the product of the output impedance and output load capacitance that determines the bandwidth of the circuit, increasing the load capacitance or output impedance reduces the bandwidth.

As you would expect from the voltage transfer graph of Figure 8, the distortion characteristics of the CMOS linear amplifier are not particularly wonderful. Linearity is quite good for small-amplitude signals (output amplitudes up to 3 V peak-to-peak with a 15 V supply), but the distortion then increases progressively as the output approaches the upper and lower supply limits. Unlike a bipolar transistor circuit, the CMOS amplifier does not 'clip' excessive sine wave signals, but progressively rounds off their peaks.

Figure 24 shows the typical drain-current versus supply-voltage characteristics of the basic CMOS linear amplifier. Note that the supply current typically varies from 0.5 mA at 5 V to 12.5 mA at 15 V.

In many applications, the quiescent supply current of the 4007UB CMOS amplifier can usefully be reduced, at the expense of reduced amplifier bandwidth, by wiring external resistors in series with the source terminals of the two MOSFETs of the CMOS stage, as shown in the 'micropower' circuit of Figure 25. This diagram also shows the effect that different resistor values have on drain current, voltage gain and bandwidth of the amplifier when it is operated from a 15 V supply and has it's output feeding to a 10M/15 pF CRO probe.

It is very important to appreciate in the Figure 25 circuit that these additional resistors add to the output impedance of the amplifier (the output impedance is roughly equal to the R1-Av product) and this impedance and the external load resistance/capacitance has a great effect on the overall gain and bandwidth of the circuit. When using 10k values for R1, for example, if the load capacitance is increased to 50 pF the bandwidth falls to about 4 kHz, but if the capacitance is reduced to 5 pF the bandwidth increases to 45 kHz. Similarly, if the resistive load is reduced from 10M to 10k, the voltage gain falls to unity; for significant gain, the load resistance must be large relative to the output impedance of the amplifier.

The basic (unbiased) CMOS inverter stage has an input capacitance of about 5 pF and an input resistance of near-infinity. Thus, if the output of the Figure 25 circuit is fed directly to such a load, it will show a voltage gain of about 30 and a bandwidth of 3 kHz when R1 has a value of 1M; it will even give useful gain and bandwidth when R1 has a value of 10M and will consume a quiescent current of only 0.4 uA!

The CMOS linear amplifier can be used, in either its standard or micropower forms, to make a variety of fixed-gain amplifiers, mixers, integrators, active filters and oscillators, etc. Three typical basic applications are shown in Figure 26.

A particularly attractive linear application is as a crystal oscillator, as shown in Figure 27a. Here, the CMOS amplifier is linearly biased via R1 and provides 180° phase shift, and the Rx-C1-XTAL-C2 pi-type crystal network provides an additional 180° of phase shift at the crystal resonant frequency, thereby causing the circuit to oscillate. If you simply want the crystal to provide a frequency accuracy within 0.1% or so, Rx can be replaced by a short and C1-C2 can be omitted. For ultra-high accuracy, the correct values of Rx-C1-C2 must be individually determined (Figure 27 shows the typical range of values). In micropower applications, Rx can be incorporated in the CMOS amplifier, as shown in Figure 27b. If desired, the output of the crystal oscillator can be fed directly to the input of an additional CMOS inverter stage, for improved waveform shape/amplitude.

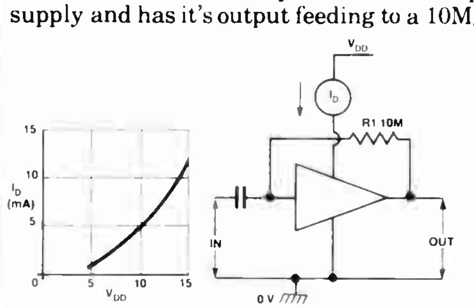


Figure 24. **Typical I_D/V_{DD} characteristics of the linear-mode CMOS amplifier.**

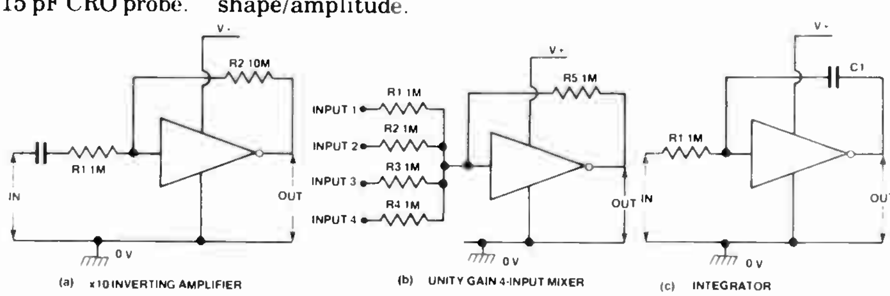


Figure 26. **The CMOS amplifier can be used in a variety of linear inverting amplifier applications. Three typical examples are shown here.**

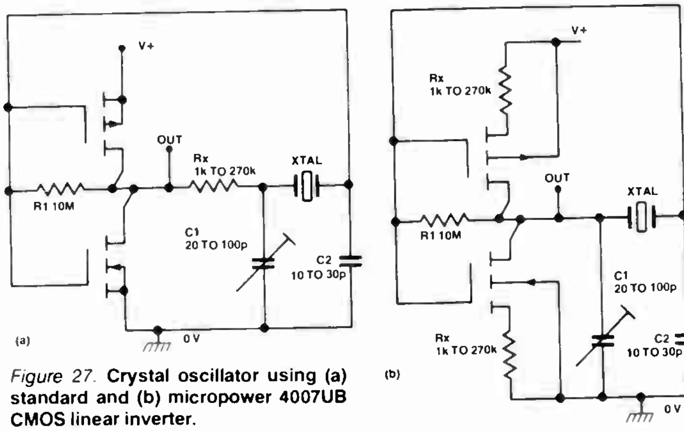


Figure 27. **Crystal oscillator using (a) standard and (b) micropower 4007UB CMOS linear inverter.**

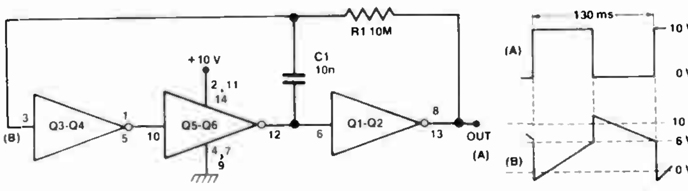


Figure 28. **This 4007UB ring-of-three astable consumes 280 uA at 6 V, 1.6 mA at 10 V.**

Practical 4007UB circuits: astables

One of the most useful applications of the 4007UB is as a ring-of-three astable multivibrator. Figure 28 shows the basic configuration of the circuit. Waveform timing is controlled by the values of R1 and C1, and the output waveform (A) is approximately symmetrical. Note that for most of the waveform period the front-end (waveform B) part of the circuit operates in the linear mode, so the circuit consumes a significant running current.

In practice, the running current of the Figure 28 astable circuit is far higher than that of an identically configured B-series 'buffered' CMOS chip such as the 4001B, the comparative figures being 280 uA at 6 V and 1.6 mA at 10 V for the 4007UB against 12 uA at 6 V and 75 uA at 10 V for the 4001B. The 4007UB circuit, however, has far lower propagation delays than the 4001B and typically has a maximum astable operating speed that is three times higher than that of the 4001B.

The running current of the 4007UB astable can be greatly reduced by operating it's first two stages in the 'micropower' mode, as shown in Figure 29. This technique is of particular value in low frequency operation, and the Figure 29 circuit in fact consumes a mere 1.5 uA at 6 V or 8 uA at 10 V, these figures being far lower than those obtainable from any other IC in the CMOS range. The frequency stability of the Figure 29 circuit is not, however, very good, the period varying from 200 ms at 6 V to 80 ms at 10 V.

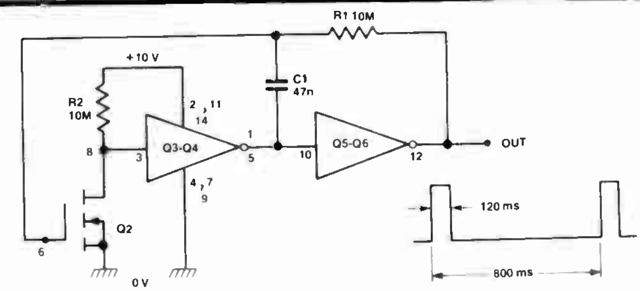


Figure 30. **This 4007UB asymmetrical ring-of-three astable consumes 2 uA at 6 V, 5 uA at 10 V.**

Figure 30 shows how the 4007UB can be configured as an asymmetrical ring-of-three astable. In this case the 'input' of the circuit is applied to n-channel MOSFET, Q2. The circuit consumes 2 uA at 6 V or 5 uA at 10 V.

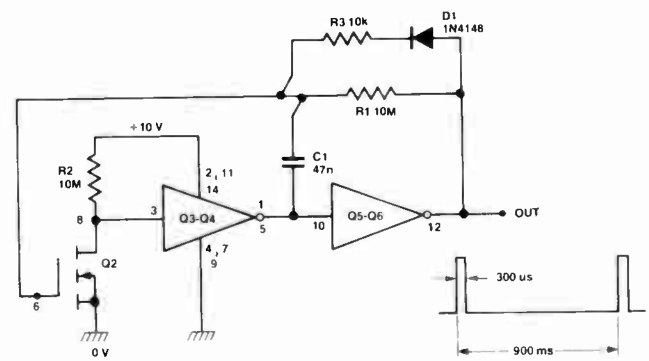


Figure 31. **This dual time constant version of the 4007UB astable generates a very narrow output pulse.**

Figure 31 shows how the symmetry of the above circuit can be varied by shunting R1 with the D1-R3 network, so that the charge and discharge times of C1 are independently controlled. With the component values shown, the circuit produces a 300 us pulse once every 900 ms and consumes a mere 2 uA at 6 V or 4.5 uA at 10 V. Note that these characteristics are similar to those of the ideal 'sample-pulse generator' circuit that was mentioned at the end of the last Circuit File, on Voltage and Window Comparators (ETI, November '82, pp 48-51).

Finally, to round off this edition of Circuit File, Figure 32 shows how the current consumption of the above circuit can be even further reduced, by operating the Q3-Q4 CMOS inverter in the micropower mode. The table gives details of circuit performance with alternative C1 and R3 values. This circuit will give years of continuous operation from a single battery supply. ●

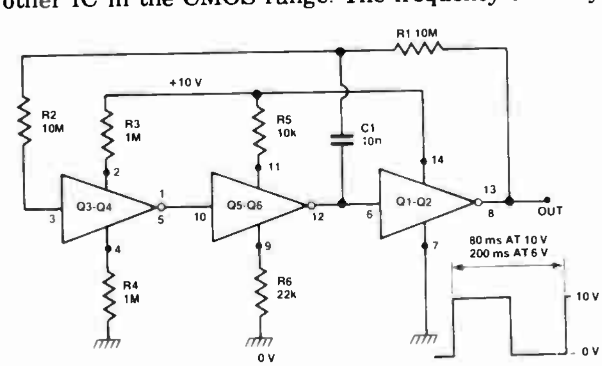


Figure 29. **This micropower ring-of-three symmetrical 4007UB astable consumes 1.5 uA at 6 V, or 8 uA at 10 V.**

C1/R3 VALUE	I_{MEAN} AT 9 V	W	P
47n/10k	1.5 uA	300 us	900 ms
10n/33k	3.5 uA	160 us	180 ms

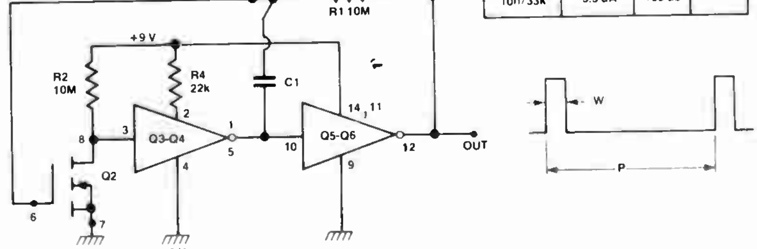


Figure 32. **This micropower version of the 4007UB dual time constant astable consumes absolutely minimal currents.**

Light and power from dc supplies

Generating mains-independent light and power from batteries is fraught with many unrealised difficulties. Whether you want dc back-up to operate equipment when the mains goes 'off the air' or a wholly independent 240 Vac supply, you should know the problems up front.

Roger Harrison

THAT'S THE TROUBLE with Electricity Commissions — they've insidiously crept into our lives and made us quite dependent on them. For those occasions when we cannot avail ourselves of their 'services', we have to rely on other sources to provide light and power. The old kerosene pressure lamp has its advantages — and disadvantages — but how on earth do you keep a disk drive running when the ac mains 'browns out'? As storage batteries are ubiquitous, the 12 V car battery in particular, it's natural that we turn to them to provide back-up and mains-independent supplies.

Back-up supplies

For equipment designed to be powered directly from a nominal 12 Vdc source or from either 12 Vdc or 240 Vac, back-up supplies are employed to maintain continuity of supply, the battery being kept charged from the mains, but the battery acts to maintain power supply to the equipment in the event of mains failure. This sort of system is commonly installed with burglar alarms, amateur radio repeaters and geophysical monitoring equipment, for example.

The 'power budget' of such systems is carefully considered to provide maximum service period from the battery supply when mains is unavailable. Hence a single 12 V storage battery — generally a low maintenance type — is employed. Let's learn a bit about lead-acid batteries first.

The fully-charged, no-load terminal voltage of a lead-acid cell is between 2.3-2.4 volts. This drops under load to about 2.0-2.2 volts. When discharged, the cell voltage is typically 1.85 volts. The amp-hour capacity is determined from a 10-hour discharge rate. The current required to discharge the battery to its end-point voltage of 1.85 V/cell is multiplied by this time; e.g: a 40 Ah battery will provide four amps for 10 hours before requiring recharge. Note however that the amp-hour capacity varies with the discharge current. The same battery discharged at a rate of 10 amps will not last four hours; on the other hand if it is discharged at 1 amp it will last somewhat longer than 40 hours. The typical discharge characteristics of a (nominal) 12 V battery are shown in Figure 1.

The ideal initial charging current for the fully discharged battery (cell voltage under 2.0 V) should be about 20 amps per 100 amp-hours of capacity (i.e: 8 amps for a 40 Ah battery). Once the electrolyte begins to gas rapidly, the terminal voltage will be around 13.8 volts and rising rapidly. At this point, the charging current should be reduced to somewhere between 4-8 amps per 100 Ah until charging is complete.

At the end of charging, terminal voltage may rise to about 15.6 volts or more, but this decreases slowly after the charger is removed, the terminal voltage then usually reading around 14.0 to 14.4 volts (see Figure 2).

Back-up supplies are generally of the 'trickle-charge' type or the 'battery condition' sensing type. Two good examples are ETI projects 597 — Emergency Lighting Unit (December 1980) — and 1503 — Intelligent Battery Charger (August 1981). The ETI-597 trickle charges a 12 V battery when the mains is on and provides automatic switchover when the power drops out. It's cheap and simple, but needs to be *used* for the batteries to stay in condition so that they deliver their rated capacity when

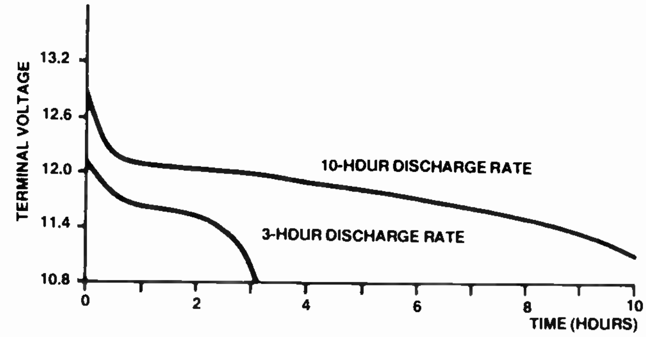


Figure 1. **Typical discharge characteristics of a 12 V (nominal) lead-acid battery.**

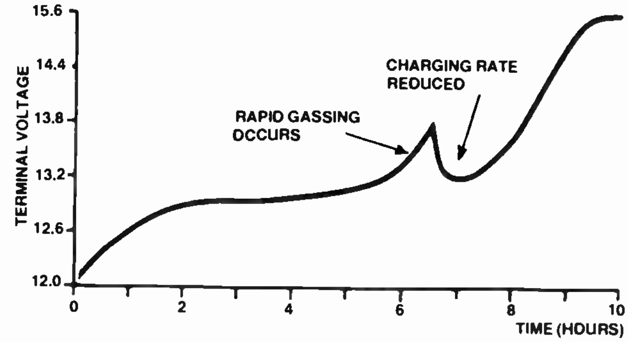


Figure 2. **Charging characteristics of a 12 V (nominal) lead-acid battery. The 'kink' in the curve near six hours is explained in the text.**

needed. Back-up supplies of this sort are only practical where the load on the supply is not too heavy — generally 20 W or so.

To drive a heavier load, upwards of 50 W for example, it's best to power the equipment from the battery *all the time* and have a charger which senses the battery terminal voltage, charging the battery when the terminal voltage falls to a preset level and turning off when the terminal voltage rises to the desired operating level again. This is what the ETI-1503 does. There is a slight element of luck involved as to how charged the battery will be at any one time, but the lower limit is usually set so that the equipment will operate for a specified period. The ETI-1503 can be used with batteries with a capacity up to 100 Ah. Such a battery can drive a 10 A load at the 10-hour discharge rate — which effectively means it's a good back-up supply for equipment with a power budget of up to 120 W mean consumption. This means that actual consumption can be greater than that from time to time provided that consumption falls below the mean level for an equivalent period. An amateur VHF or UHF repeater is a good example. Whilst 'listening' only — no stations active on the input channel — consumption is quite low. When 'activated' by a station or stations, the repeater spends most of its time transmitting, and consumption can be four to ten times that during inactive periods, depending on the power output of the transmitter employed in the repeater.

As stated earlier, the major consideration with back-up supplies is the power budget of the equipment being supplied. If you anticipate the necessity of operating the equipment for periods exceeding, say, eight hours, then a battery of adequate ampere-hour capacity needs to be used. It is always prudent to choose a battery with 20-50% more capacity than strictly necessary.

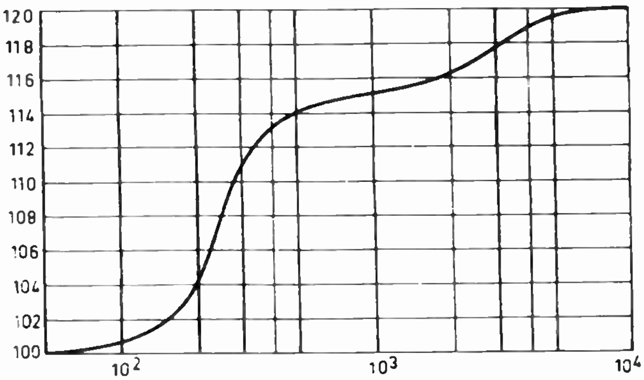
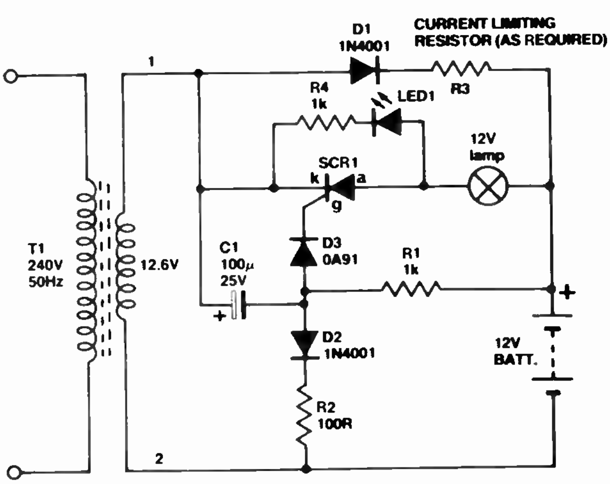


Figure 3. **The light output of a fluorescent tube increases with increasing supply frequency in the manner shown in this graph. The property is exploited in dc-ac square wave inverters for lighting.**

dc-ac inverters

Like storage batteries, 240 Vac mains-operated equipment is ubiquitous! The huge variety of products have been designed to be *convenient,* thus making themselves *necessary.* Or so it seems. Why on earth anyone would want to take an electric razor on a camping expedition and expect to power it from an ersatz 240 Vac supply is beyond this writer — but then I haven't had a shave in more than 15 years except when my appendix was removed and then they didn't shave my face!

There are two common approaches to providing 50 Hz ac power for mains operated appliances: provide square wave drive of the appropriate amplitude, or derive a sinewave (or pseudo sinewave) supply of appropriate amplitude. Both are fraught with hidden difficulties. If you want any substantial amount of power output — like 200 W — you're in hot water — and probably unable to boil a billy, to boot!



Circuit of the ETI-597 'Emergency Lighting Unit', a simple back-up supply that can be used for other than lighting applications.

A square wave dc-ac inverter has the advantage of simplicity and efficiency — depending somewhat on the design. Inverters generally take two forms: *self-excited,* usually employing a feedback winding on the transformer, and *driven,* where an oscillator drives a switching circuit, generally with transformer output. Where the precise frequency of the ac output is unimportant, self-excited inverters are employed. Where a stable 50 Hz output is required, a driven inverter is necessary.

Lighting is one area where self-excited dc-ac inverters find application. The common tungsten filament incandescent light globe is a poor choice for lighting where a dc supply is employed. They have an efficiency of less than a fifth of that of a fluorescent light of the same power rating — viz: around 12 lumens/watt for the tungsten filament lamp versus better than 60 lumens/watt for a fluorescent tube. A 20 W fluorescent tube would provide as much light output as a 100 W incandescent globe! Those figures are based on 50 Hz ac supply. Fluorescent tubes *actually improve in efficiency* when driven from a higher frequency supply. Figure 3 shows how the light output of a fluorescent tube increases with increasing supply frequency. Driving the tube from a supply frequency of 10 kHz or more will result in a 20% increase in light output.

The circuit of a self-excited inverter driving a fluorescent tube is shown in Figure 4. This is taken from Project ETI-516 of November 1972. It ran at around 2 kHz and employed a ferrite-cored transformer. Consumption was 2.5 amps. An incandescent globe to pro- ▶

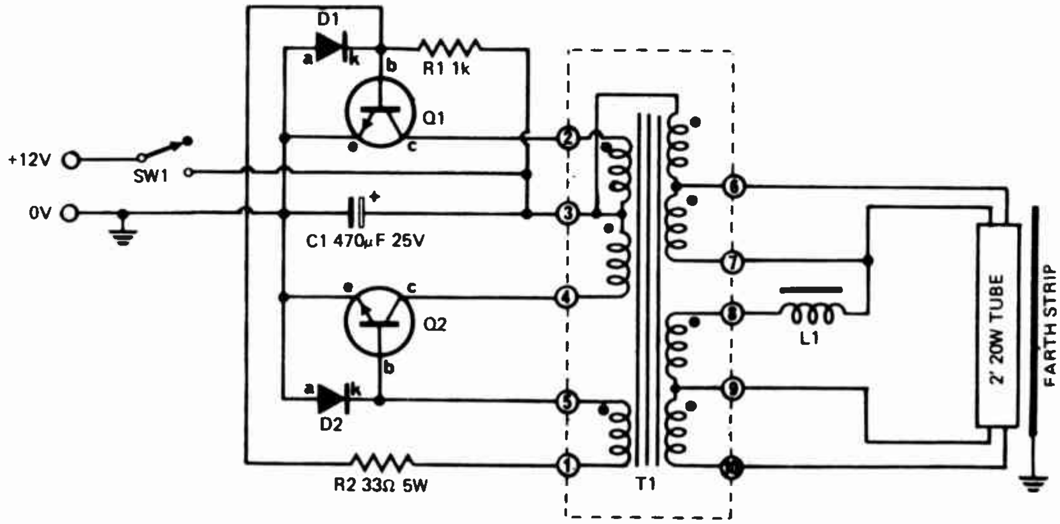


Figure 4. **ETI project 516 (Nov. '72!) employed a self-excited dc-ac square wave inverter operating at 2 kHz to drive a 20 W fluorescent tube — an efficient solution to providing light from a dc supply.**

vide a similar light output would draw around 10 amps! Such inverters have one drawback — the transformer core 'sings' owing to the magnetostrictive forces on the core pieces (which generally come in two pieces). That can be solved in two ways — put the inverter in a 'soundproof' box or operate the inverter at a frequency above audibility. The first solution was employed with the ETI-516 inverter, but is inevitably only partially successful (though often acceptable). The second solution will be described next month in Project ETI-1505.

When it comes to powering 240 Vac-operated equipment or appliances a number of considerations have to be looked at. First, will the equipment operate from a square wave supply? Many appliances employing an ac or ac/dc motor will operate quite happily from a square wave supply. One of ETI's correspondents employed battery back-up for his computer's disk drives, supplying these with 240 V, 50 Hz square wave ac from a driven inverter. The general arrangement is shown in Figure 5. A 100 Hz oscillator drives a flip-flop, which drives a pair of HEXFETs connected in push-pull across the secondary of a toroidal transformer. Battery supply was 24 V. The transformer is operated 'back-to-front' here, where input is applied to the secondary and the load connected across the primary. Toroidal transformers perform much better in this application than conventional types as core losses are lower and primary-to-secondary coupling is generally better. Some losses are involved, the saturation voltage of the HEXFETs generally being the greatest source. Hence the use of a 20-0-20 V winding and not a 24-0-24 V winding.

The saturation voltage loss in switching devices driving a transformer is an important consideration. One or two volts lost from a 24 V supply represents only about 4% to 8% loss, but at 12 V it's twice that! Any further losses only magnify the problem.

A square wave ac supply is inherently rich in harmonics. These can play havoc with audio and digital equipment and it's often difficult to suppress interference generated by the supply. Then again, some equipment — particularly anything containing a transformer and rectifier, will produce entirely different performance from when it's operated from a sine wave supply. The problem arises because the peak and RMS values of a square wave are the same, whereas the peak/RMS ratio for a sinewave is 1.414. To deliver the same *work value* as a sine wave supply, the peak output voltage of a square wave dc-ac inverter is generally set at 240 V. When driving a motor or resistive load, the square wave supply will deliver the same amount of power as a sine wave supply; i.e: the same amount of *work* will be done (all else being equal). But, where the load or equipment expects a peak voltage of 340 V (as we have with the ordinary mains), then a square wave supply of a nominal 240 V output will not 'deliver the goods' as its peak voltage is only 240 V.

So much for that; let's look at sine-wave dc-ac inverters. At this stage, I recommend you read the letter from reader Barry Brown in the accompanying panel.

Requests of a similar nature arrive quite commonly, though Mr Brown's is a little unusual compared to many we receive. Where Mr Brown suggests a dc-ac inverter to operate from a 24 V or 32 V supply, many readers ask for a

Dear Sir,

Despite the financial burden of component costs for an ever-expanding range of new projects, please find enclosed my cheque for subscription renewal. Would you consider a three-to-six-month moratorium on new projects to enable those of us who are more enthusiastic about starting the new than finishing the old to clear some of the backlog?

No?

Well, to an area with possibly more appeal — that of small domestic power supplies. With most homesteads using 32 Vdc power for lighting and almost all travellers using 24 or 12 Vdc power, a stable inverter producing 240 Vac at 50 Hz in the 500 W-1 kW range could be of enormous benefit to many people. With an increasing range of domestic electronic equipment becoming available, the only way for many people to enjoy these products is to crank over the, if available, 240 V diesel generator. This is great stuff during the day, especially with auto-start, but can be a bit distressing when you discover that your evening music selection is really a duo for harpsichord and Lister Diesel.

More ambitious, and probably a lot heavier: a larger inverter capable of starting a fridge/freezer would win many friends. Although these devices may have considerable losses in conversion, there are advantages in using converters for many applications. Not the least of these would be the lifetime supply of European carp likely to be donated by the Darling River United Naturalists Kangaroo Appreciation, Research and Development Society (DRUNKARDS). Such a society, although unformed, could be initiated at the drop of a cold tinny after publication of a suitable circuit.

Barry Brown,
Young NSW.

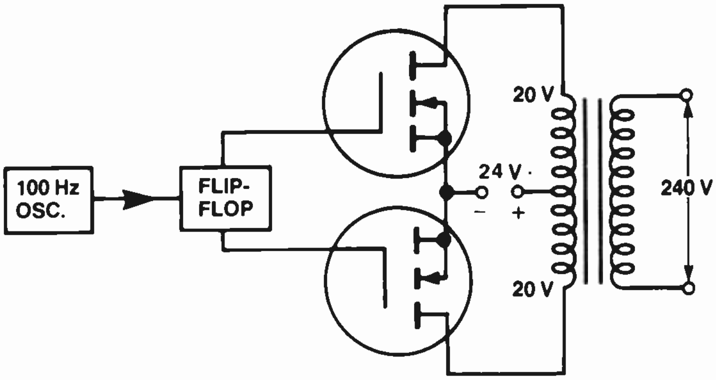


Figure 5. **Example of a 'driven' dc-ac square wave inverter with nominal 240 Vac output. This technique has been employed by one of our correspondents as a computer back-up supply.**

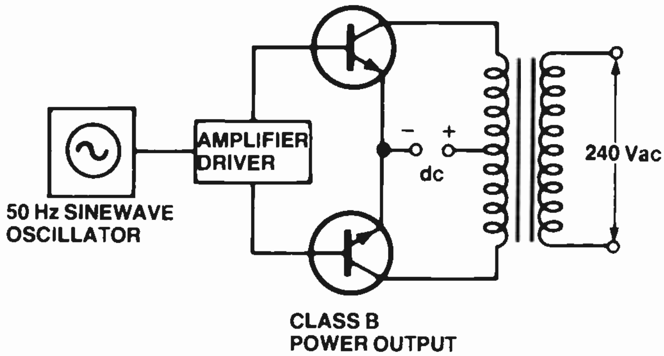


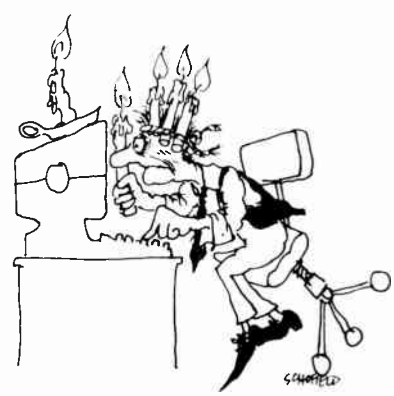
Figure 6. **Class B driven sinewave inverter technique for providing 240 Vac from a dc supply.**

1 kW or similarly rated inverter to run from a 12 V battery. The latter is impractical, for the following reasons.

Consider this: a sinewave dc-ac inverter needs to be of the driven type. Hence it generally consists of an oscillator driving a class B power amplifier — usually a push-pull type. The theoretical maximum efficiency obtainable with a class B power amplifier is 78%. With losses and power consumption of drive circuitry taken into account the dc power input to ac power output efficiency of an inverter of this type is generally around 65-70%. Thus a 1 kW dc-ac inverter to run from a 12 V battery *would draw in excess of 120 amps* at full load! Few batteries available would supply that sort of current for long. With currents of that magnitude, special arrangements have to be made for primary circuit conductors. A resistance of 5 milliohms (0.005 ohms) will result in a power loss of more than 70 watts. Then again, special consideration has to be given to heat dissipation in the power output stage. The devices used would dissipate something over 400 W at peak load. No load dissipation would probably be in the vicinity of 40-50 W, which is no mean amount to get rid of.

Apart from the weight of a heatsink, consider the weight of a 1 kVA (or 1000 W) transformer (assuming a single transformer is used). We'll leave the expense to your imagination.

The problems are reduced somewhat when a much higher dc supply voltage is available. However, in the latter case other techniques of dc to ac conversion present themselves — but that should be the subject of another article as it's a whole new ballgame.



Where a 12 V battery supply only is available, there is a practical limit to the maximum power of a dc-ac inverter, and that's probably around 300 W output. At typical efficiencies, the dc input power is around 450 W, or close to 35-40 amps current from the battery.

As you would already appreciate, this brings its own special problems. A battery to supply that sort of power for any appreciable or worthwhile period would need to have a considerable ampere-hour capacity. Your typical 40-60 Ah car battery would barely deliver an hour's worth of power. If the inverter is installed within the vehicle, or close by, and you are willing to keep the engine running during operation, then the battery will deliver the goods for quite a period, provided you can 'set' the throttle to suit so that battery charge is maintained. At this stage, I might point out that an alternator coupled to the motor would provide a more efficient energy conversion.

To gain, say, four to six hours of operation for a 300 W inverter, you would need a battery system of more than 200 Ah capacity.

A more practicable power level for a sinewave dc-ac inverter would be around 120 W. Such an inverter would pull 12 to 15 amps from the battery, a much more manageable figure.

Having seen the primary side of the problem, let's consider the secondary side — the load. How many appliances do you have rated at less than 300 watts? Very few. The humble electric kettle is rated from 1 kW to 2.4 kW. Monochrome TV sets, particularly portables, may only consume 100 W, but a colour TV may draw three times that or more. A 'low power' (say, 30 W/ch.) domestic hi-fi will draw around 100 W, depending on how much equipment is in use and how loud you like it. Anything more ambitious has a proportionately larger consumption. A 300 W dc-ac inverter is best considered where the full output is only required intermittently.

Conclusion

As can be seen, many factors have to be taken into account when considering obtaining light and power from a battery supply — whether it be in a back-up application, for lighting or 240 Vac substitution. The ubiquitous 12 V battery is not up to the job in some instances — in which case higher voltage dc systems are better considered.●

Lab Notes

Using BiFET and BiMOS op-amps

The availability of BiFET and BiMOS op-amps has revolutionised circuit design since they appeared on the scene five or so years ago. While we've used devices like the CA3140 op-amp in projects we've not got around to describing practical applications circuitry. This 'Lab Notes' fills that gap.

Brian Dance

THE AVAILABILITY of BiFET and BiMOS devices in various packages with one to four operational amplifiers per package has revolutionised the operational amplifier market. Apart from the relatively expensive hybrid FET input devices, other FET input operational amplifiers had been available for some considerable time, so why should BiFET and BiMOS devices be so important?

The first point to note is that amplifiers with FET input stages can offer far higher input impedances than devices with ordinary bipolar transistors in their input stages. For example, the well-known 741 has an input impedance of the order of 1M and a maximum input bias current of 500 nA. The use of bipolar transistors to obtain a high input impedance has been pushed to the limit in devices such as the LM108, using supergain input devices to provide a typical input impedance of 70M and an input bias current of just under 1 nA. These values may be compared with those of some of the economical BiFET and BiMOS devices, where typical input impedances are of the order of 1 Terra-ohm (one million Megohms!) and input currents are some tens of picoamps (pA) at room temperature.

Thus if one connects the input of one of these BiFET or BiMOS amplifiers to almost any circuit, it will impose a very small load on that circuit. This can be a vital consideration when one is designing such high-impedance circuits as those used in pH meters or in ionisation chamber smoke detector circuits, whose output current is inadequate to drive devices such as the 741.

If one considers the very early types of monolithic FET input operational amplifiers (such as the Fairchild μA740), they do have the desired high input impedance, but their disadvantage is that their input offset voltage and its temperature coefficient are so high that they do not approach the high standard of performance required by the modern

INTRODUCTION TO THE BIMOS AND BIFET OP-AMP

The first BiFET products were announced by National Semiconductor in 1975 (the LF155, LF156 and LF157 series, where LF signifies Linear FET device). The main advantages of these products is that the junction FET devices used in their input stages are fabricated on the same silicon chip as the remainder of the operational amplifier. Although hybrid operational amplifiers with FET input stages had been available for some considerable time previously, all of these hybrid devices contained the junction FET devices fabricated on a separate silicon chip from the remainder of the operational amplifier. Such hybrid devices can be made to have a very good performance if adequate trouble is taken in their design, but the extra labour costs involved in the testing of the separate chips for appropriate matching characteristics and in connecting the two chips in a single hybrid package inevitably resulted in a price tag far above that of modern BiFET devices. The general type of construction of a BiFET device is shown in Figure 1, the channel between the source and the drain electrodes of the FET input devices being fabricated by ion implantation.

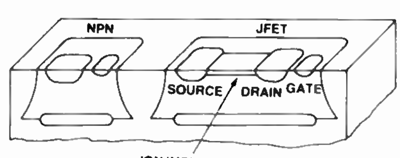


Figure 1. **Construction of a BiFET device.**

Although National Semiconductor produced the first BiFET products, it was not long before other manufacturers entered the BiFET market, and such products are now available from Advanced Micro Devices, Analog Devices, Fairchild, Harris Semiconductor, Motorola, Intersil, Precision Monolithics, Raytheon and Texas Instruments, although National Semiconductor still offer the widest range of BiFET products, details of which can be found in their Linear Databook.

Very soon after National Semiconductor had announced the first BiFET products, RCA introduced their first BiMOS product, the economical CA3130 operational amplifier. This has some similarities to the BiFET amplifiers, but employs MOSFET transistors in the input stage rather than junction FET devices. RCA soon introduced further BiMOS devices, one of the best known type being the CA3140, which can be used as a pin-for-pin replacement for the 741 when a higher performance is required. More recently the CA080 series has been introduced as pin-for-pin replacements for the Texas Instruments series of TLO80 BiFET types.

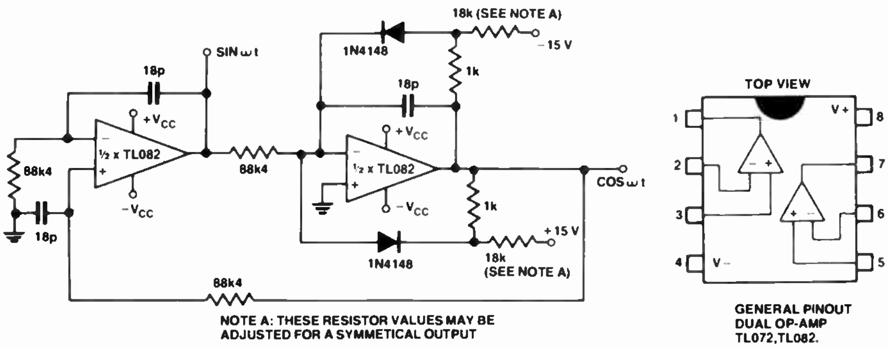


Figure 3. **Quadrature oscillator producing two outputs 90° out of phase, using a TL082 dual op-amp — pinout at right.**

professional engineer. Modern BiFET and BiMOS devices provide a very high input impedance with relatively good stability and temperature performance — although the input impedance of any of these devices at 25°C is much greater than over the full temperature range.

In general BiFET and BiMOS economical devices offer a comparable performance. If anything, BiMOS devices tend to offer the lower input bias currents and BiFET products the lower noise levels. However, premium devices of both types are available with performances far above the average for the type of device concerned.

Half-Hertz oscillator

Figure 2 shows the use of the economical TL081 device in a simple 0.5 Hz square wave oscillator. The TL081 is a

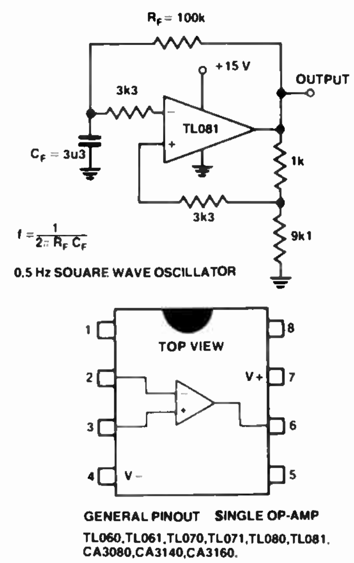
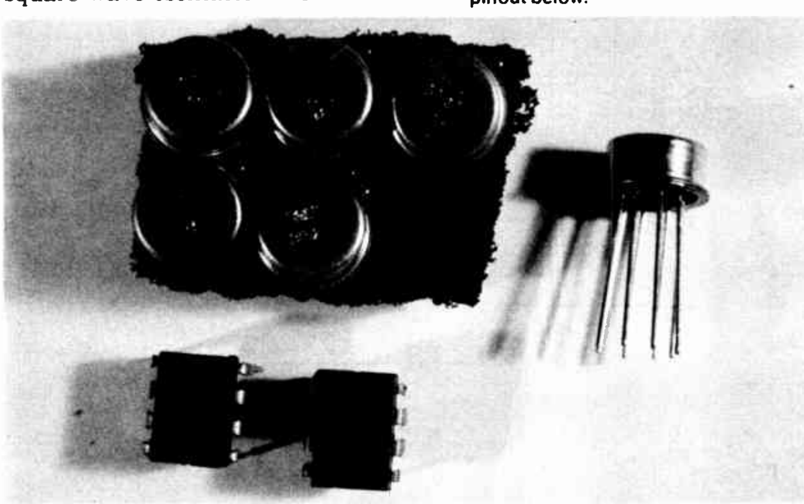


Figure 2. **Half-Hertz oscillator using a TL081 — pinout below.**



Modern BiMOS and BiFET op-amps come in both can and DIL packages.

single operational amplifier in a dual-in-line package with the connections shown in Figure 2; the pin connections are the same as those of the well-known 741 devices, internal frequency compensation being employed so that no external compensating capacitor is required. External offset adjustment can be made when required by means of an external variable resistor. The TL071 is a similar low-noise device with the same connections, and is quite suitable for use in this circuit, but its low-noise characteristics are not needed. The TL061 is a low-power device with the same connections.

The frequency of oscillation of the Figure 2 circuit is given by $f = 1/(2\pi R_F C_F)$, or about 0.5 Hz with the values shown. The high input impedance of the circuit enables a relatively high value of feedback resistor, R_F, to be employed, so the value of C_F can be reasonably small for a given frequency of operation. About nine-tenths of the output voltage is fed back to the non-inverting input to provide positive feedback to maintain oscillation. The capacitor C_F charges and discharges through R_F according to whether the state of the output voltage is 'high' or 'low' at the time concerned.

The circuit of Figure 2 generates square waves which are approximately symmetrical. However, if a circuit which generates waves with an unequal mark-to-space ratio is required, it is only necessary to connect a resistor of perhaps 10k to 50k in series with a diode across R_F. The direction in which the diode is connected determines whether the output spends the greater part of its time in the 'high' or in the 'low' state.

100 kHz oscillator

Figure 3 shows the circuit of a 100 kHz oscillator providing two outputs which are 90° out of phase with each other. Although the TL081 is perfectly satisfactory for use in this circuit, it is more convenient to use the dual TL082 device so that this one device is all that is needed. The connections of the 8-pin dual-in-line TL082 device are shown in Figure 3; it employs internal frequency compensation, but has no external offset adjustment facilities. ▶

Lab Notes

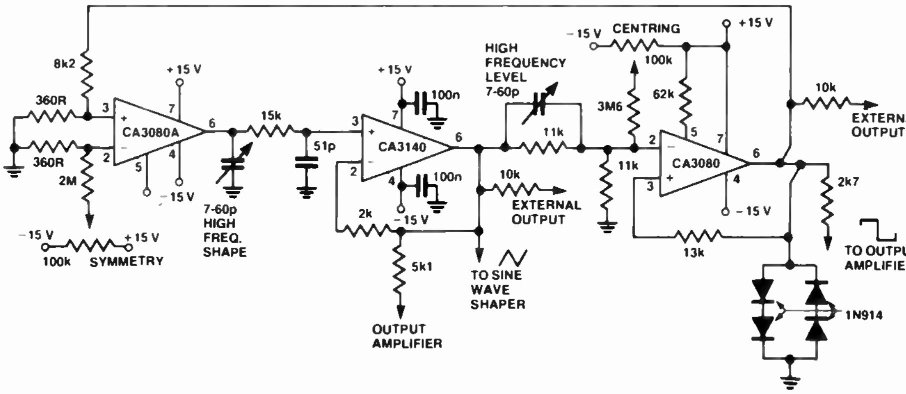


Figure 4. **Function generator circuit. Sourcing or sinking current from pin 5 of the left hand CA3080 will vary the frequency.**

BiMOS generator

A function generator which produces square and triangular waveforms is shown in Figure 4. It employs a CA3140 BiMOS device together with a CA3080A and CA3080. A particular feature of this circuit is that a frequency range of one million to one can be obtained by the use of a single variable resistor, or alternatively by the use of an auxiliary sweeping signal.

A CA3130 device may be employed instead of the CA3140 shown, but in this case a frequency compensating capacitor (about 56p) must be connected between pins 1 and 8, since the CA3130 is not internally compensated. The CA3160, which does not require any external frequency compensation, is also suitable for use in this circuit.

The high frequency linearity of the ramp is adjusted by the 7-60p variable capacitor connected between the output of the CA3140 and the output CA3080 device. The triangular wave output level is determined by the four 1N914 level-limiting diodes in the output circuit and the network connected to pin 2 of the CA3080.

It is important to minimise lead length and parasitic coupling capacitance in this circuit by careful layout.

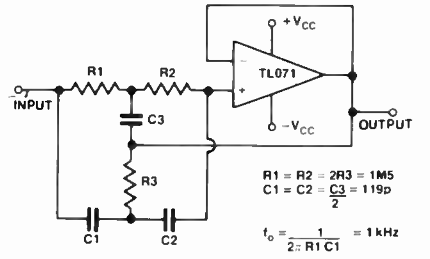


Figure 5. **Notch filter using a 'Twin-T' filter section on the input of a TL071 op-amp.**

Notch filter

The circuit of Figure 5 shows the use of a TL071 low-noise amplifier in a notch filter circuit. This is the normal 'twin-T' filter in the input circuit, in which one of the 'T' sections consists of R1, R2 and C3 and the other part of C1, C2 and R3. It is designed to reject signals of one particular frequency (the notch frequency), whilst passing signals of any other frequency virtually unattenuated.

For optimum performance, when a sharp notch in the frequency response is required, the components should have matched values (to within 1% or 2%). When the values shown are employed, the notch frequency occurs at approximately 1 kHz. An advantage of using a high input impedance device such as the TL071 is that relatively large values may be employed for R1, R2 and R3 and,

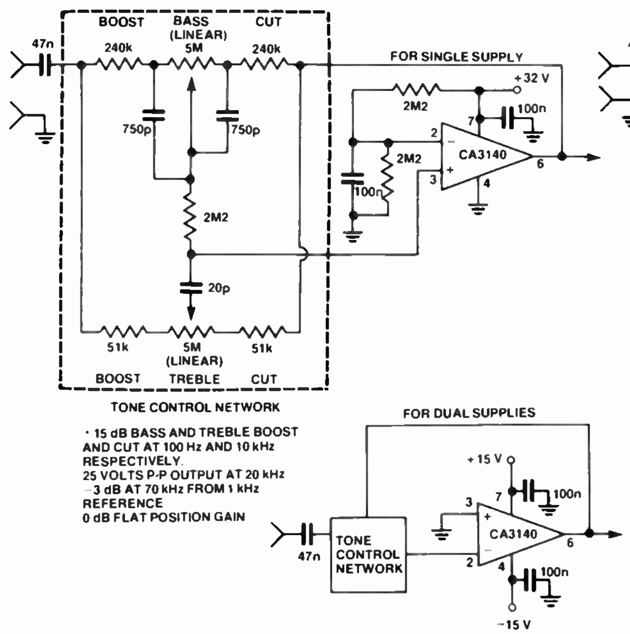


Figure 6. **Baxandall type tone control circuitry, with unity gain (flat position).**

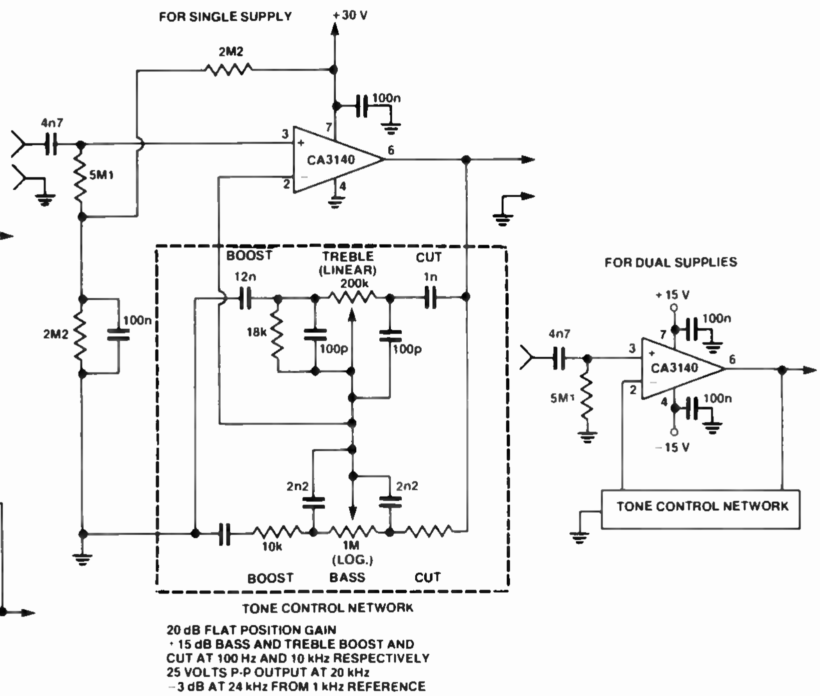


Figure 7. **Tone control circuit with 20 dB of gain, flat position.**

therefore, for any given frequency, C1, C2 and C3 can have a relatively low value. Large value, close tolerance capacitors are expensive, so the ability to employ devices of low value is important.

Tone controls

Two tone control circuits using the CA3140 are shown in Figures 6 and 7. Figure 6 is of the Baxandall type, which provides a gain of unity at the mid-frequencies and uses standard linear potentiometers. The high input impedance of the CA3140 enables low-value (and therefore cheap) capacitors to be employed in a circuit which has an impedance great enough to avoid excessive loading of the stage feeding this circuit.

Bass/treble boost or cut are about ±15 dB at 100 Hz and 10 kHz respectively. Full peak-to-peak audio output is available up to at least 20 kHz, since the CA3140 has a relatively high slew rate (about 7 V/us). The gain falls by about 3 dB at a frequency of around 70 kHz.

The circuit of Figure 7 provides similar boost and cut facilities, but the gain of this circuit is about eleven. The input impedance is basically equal to the resistor from pin 3 to ground.

off between bandwidth and power consumption which is required). Figure 9 shows the response of the Figure 8 circuit.

Mic preamp

A moving-coil microphone preamplifier with tone control is shown in Figure 10. A TL061 low-power device which is internally compensated is employed in this circuit.

Distribution amp

The Texas Instruments series of BiFET devices is also available with four separate amplifiers in a single 14-pin dual-in-line package. Figure 11 shows the connections of the TL064 low-power BiFET quad amplifier, together with a circuit for an audio distribution amplifier using one of these quad devices. The input stage acts as an input buffer and the other three stages act as output buffers, so that no signal from output A finds its way into any of the other outputs.

The TL084 and the low-noise TL074 have the same pin connections (which are the same as those of the LM324 type of device), whereas the TL085 and the low-noise TL075 devices are quad types with connections similar to the RC4136. There is no TL065 at present. ▶

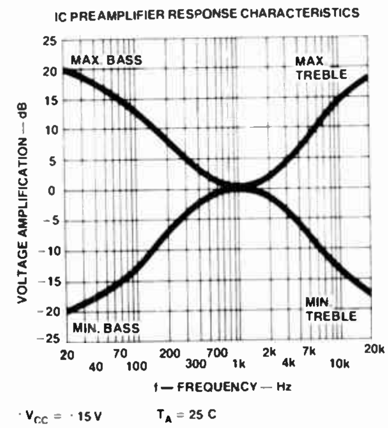


Figure 9. **Response characteristics of the Figure 8 circuit.**

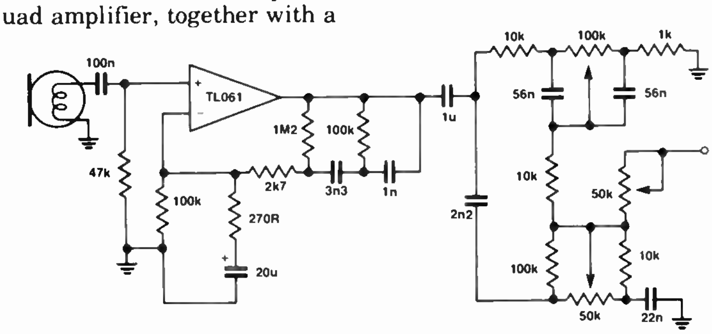


Figure 10. **Moving-coil mic preamp with tone controls, using an internally compensated TL061 device (same pinout as TL071).**

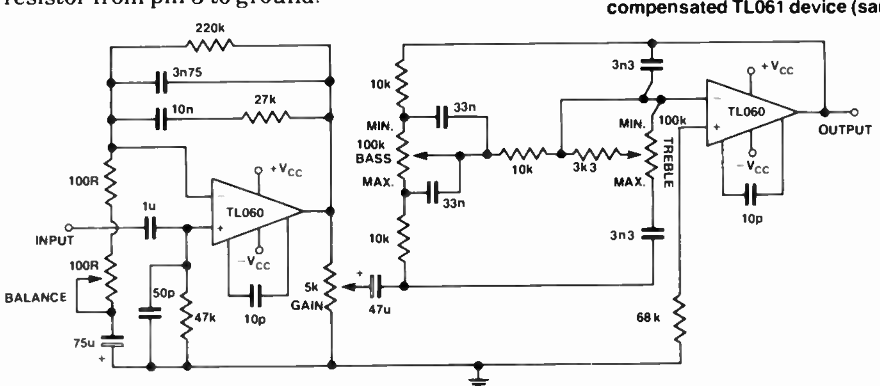


Figure 8. **A two-stage tone control circuit using TL060 devices. (Same pinout as TL070).**

A tone control circuit using the TL060 low-noise BiFET devices is shown in Figure 8. The TL060 is not internally compensated and therefore requires the 10p external frequency compensation capacitor shown connected in the circuit of each device. Similar circuits can, of course, be made using the TL080 devices at the expense of a higher power level. A further alternative is the use of TL066 programmable BiFET device without any compensating capacitors, but with a suitable value of the programming resistor between pin 8 and the negative line (about 1k, depending on the trade-

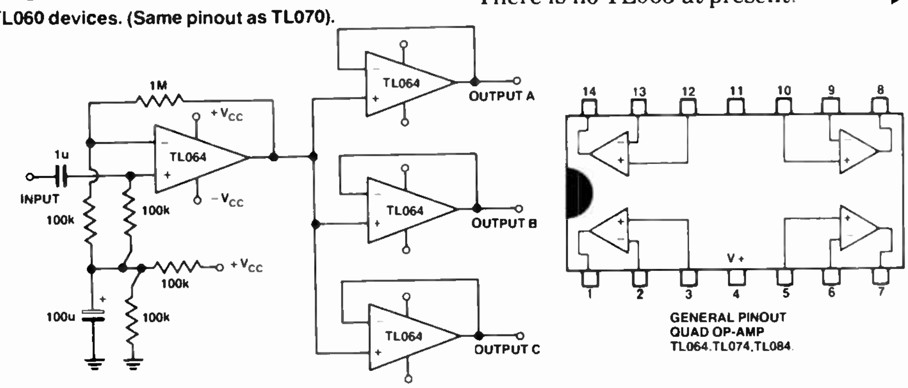


Figure 11. **An audio 'distribution' amplifier for 'slaving' several pieces of equipment from a single source. Pinout for the quad op-amp is shown at right.**

Lab Notes

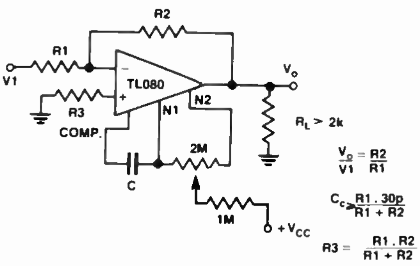


Figure 12. **Simple voltage-variable gain amp using the TL080.**

Variable gain

The simple circuit of Figure 12 is an amplifier which provides a variable gain set by the potentiometer. A TL080 device is employed, so the compensating capacitor C_c is required, since this device is not internally compensated.

Ice warning

The circuit of Figure 13 employs three of the four amplifiers of the TL084 device in an ice warning detector. It is especially suitable for use in vehicles to warn the driver when the temperature of the thermistor (placed outside the vehicle) falls below 0°C.

When the temperature of the thermistor falls, its resistance rises and the current flowing through the thermistor decreases. Thus the inverting input of the TL084 connected to this thermistor receives less current from the positive supply line and its output voltage tends to rise. This output voltage is fed to the TL084 output amplifier and produces a voltage across the LED, which lights, providing the required warning.

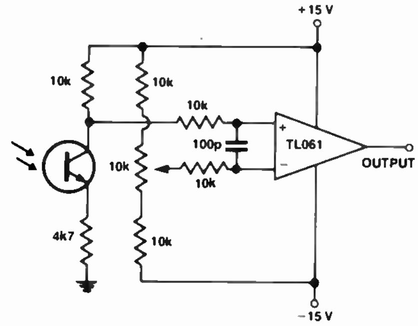


Figure 14. **Low-level light detector using FPT100 or similar phototransistor.**

Light detector

The circuit of Figure 14 is a low-level light detector preamplifier using the low-power TL061 device with a TIL601 or similar phototransistor. The variable resistor can be used to balance the output at any particular value of light level.

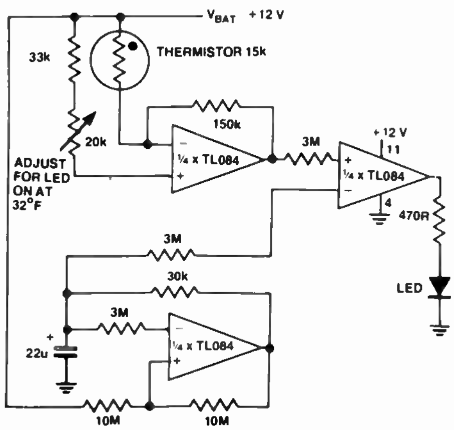


Figure 13. **An ice warning indicator.**

Sine shaper

The circuit shown in Figure 15 uses a CA3140 as a voltage follower device in combination with diodes from the CA3019 array to convert the triangular signal from a function generator into a sinewave output, which has typically less than 2% harmonic distortion.

The circuit is best adjusted using a distortion analyser, but a fairly good adjustment can be made by comparing its output signal on an oscilloscope with that from a good sinewave signal generator. The initial slope is adjustd by R1, followed by an adjustment of R2. The final slope is established by adjusting R3, thereby adding additional segments that are contributed by these diodes. Repetition of the adjustments may be necessary, since there is some interaction between the adjusting potentiometers.

Wien bridge

A CA3140 BiMOS amplifier is used in the circuit of Figure 16, together with a CA3019 diode array, to form a Wien bridge oscillator. The zener diode shunts the 75k feedback resistor and, as the output signal amplitude increases, the zener diode impedance rapidly decreases so as to produce more feedback, with a consequent reduction in gain. This action stabilises the output signal amplitude. This combination of a monolithic zener diode and the bridge rectifier tends to provide a zero temperature coefficient for this regulating system.

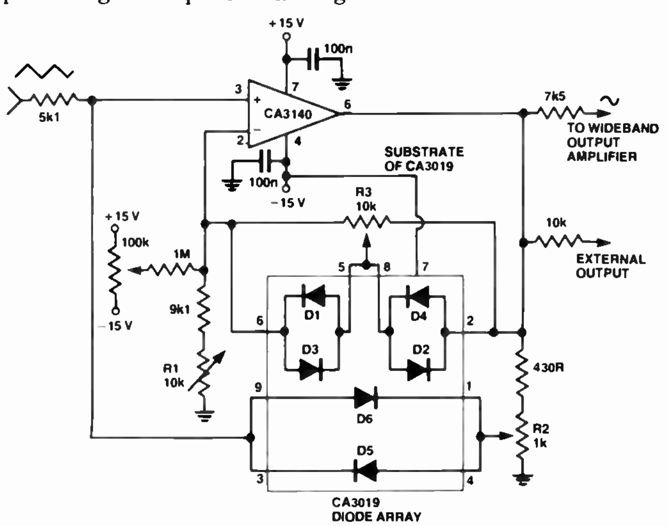


Figure 15. **A triangle-to-sine waveshaping circuit employing a CA3140 op-amp and a CA3019 diode array.**

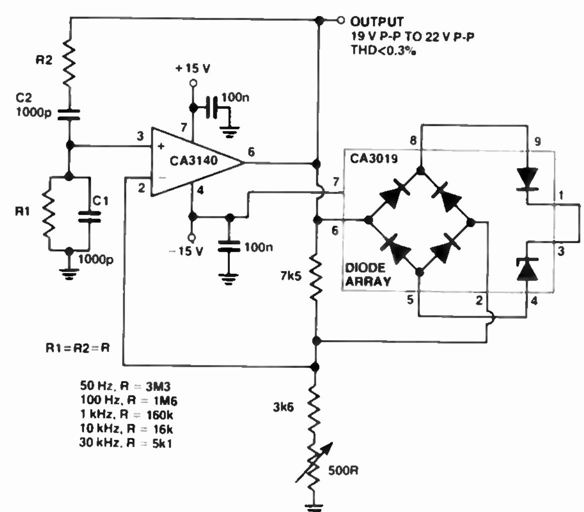


Figure 16. **A Wien bridge oscillator featuring amplitude stabilisation via the zener action from the CA3019 diode array.**

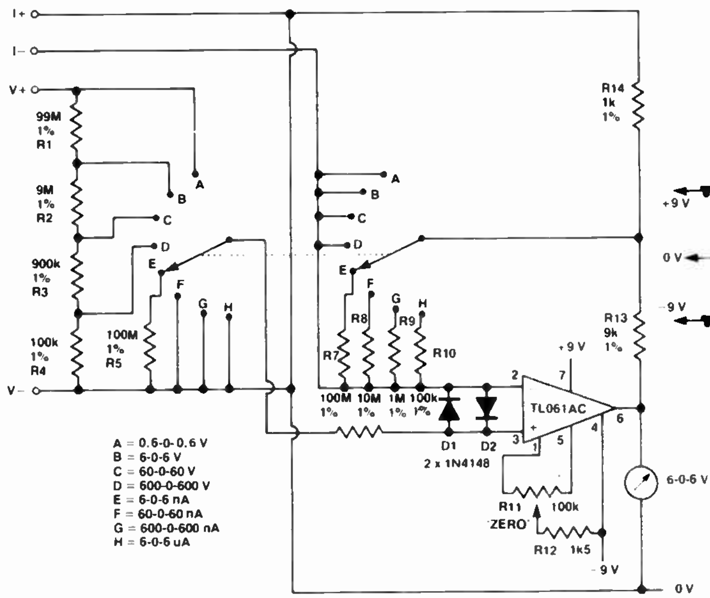


Figure 17 **A multi-range voltmeter with high impedance input plus multi-range low-current meter.**

As the output circuit contains no RC time constant, there is no lower frequency limit for operation. If C1 = C2 = 1u (polycarbonate) and R1 = R2 = 22M, the operating frequency can be about 0.007 Hz. At high frequencies, as the frequency is increased the amplitude of the signal must be reduced to prevent slew rate limiting from taking place. An output frequency of about 180 kHz will reach a slew rate of about 9 V/us when the output voltage amplitude is about 16 V peak-to-peak.

Meter

The high input impedance of BiFET and BiMOS devices has led to their use in many voltmeters of high input resistance and also in meters to measure very small currents.

The circuit of Figure 17 was designed by Texas Instruments for the measurement of voltages in the range ±0.6 V to ±600 V, where the source resistance may be quite high, and to measure currents from 6 nA to 6 uA. The instrument was required to accept inputs of either polarity and be inexpensive, robust and reliable. It also had to have a long battery life, so a TL061 low-power operational amplifier device was selected. An inexpensive centre zero meter is considerably cheaper than a liquid crystal display and would provide adequate accuracy for the purpose.

When the switch is in one of the positions A to D inclusive, the instrument is set for the measurement of voltages. The amplifier has a non-inverting gain of 10 and range selection is achieved by a simple potential divider network with a fixed input impedance of 1000 megohm. A panel-mounted 'centre zero' control is included in the circuit to facilitate corrections for the mechanical movement of the meter zero and for the change in the operational amplifier input voltage offset (for example, with temperature).

In the current measuring mode of switch positions E to H inclusive, the amplifier operates as a current-to-voltage converter. For the most sensitive range of 6 nA, a transimpedance of 1 Gigaohm is required to produce a full-scale deflection of the meter. Rather than use a resistor of such a high value, a resistance multiplier arrangement was devised with a 100M feedback resistor for the most sensitive range.

The two diodes across the input of the operational amplifier in conjunction with R6 provide protection against any gross overloading of the instrument. A suitable arrangement incorporating a fullwave rectifier into this circuit would allow alternating input signals to be measured, but arrangements would have to be made to allow for frequency roll-off of the response at high frequencies.

3 pA meter

A CA3160 and a CA3140 are used in the circuit of Figure 18 to construct a picoammeter with ±3 pA full scale deflection (one picoamp = 10^{-12} amps). Pins 2 and 4 of the CA3160 are connected to ground, so the input pin 3 between them is effectively 'guarded'. If slight leakage resistance is present between terminals 3 and 2 or 3 and 4, there would be zero voltage across this leakage resistance and this would reduce the leakage current by a large factor.

It is preferable to operate the CA3160 with its output pin 6 near the ground potential, so as to reduce the dissipation by reducing the device supply current. The CA3140 serves as a x100 gain stage to provide the required plus and minus output voltage swing for the meter and feedback network. A 100:1 voltage divider network consisting of a 9k9 resistor in series with a 100 ohm resistor sets the voltage at the 10 kMohm resistor to ±30 mV full-scale deflection. This 30 mV signal results from ±3 V appearing at the top of the voltage divider network, which also drives the meter circuitry.

It is possible to switch the 9k9 and 100 ohm network in the output circuit so that current ranges from 3 pA to 1 nA can be handled using the single 10kM resistor.

The writer has seen circuits using BiMOS devices published for use in measuring currents down to 100 femtoamps (0.1 pA), but obviously extreme care is required to ensure the insulation is adequate when such small currents are being measured. ▶

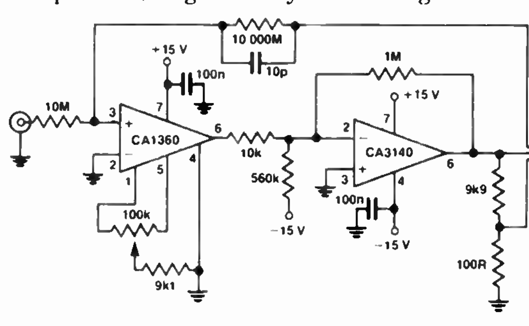
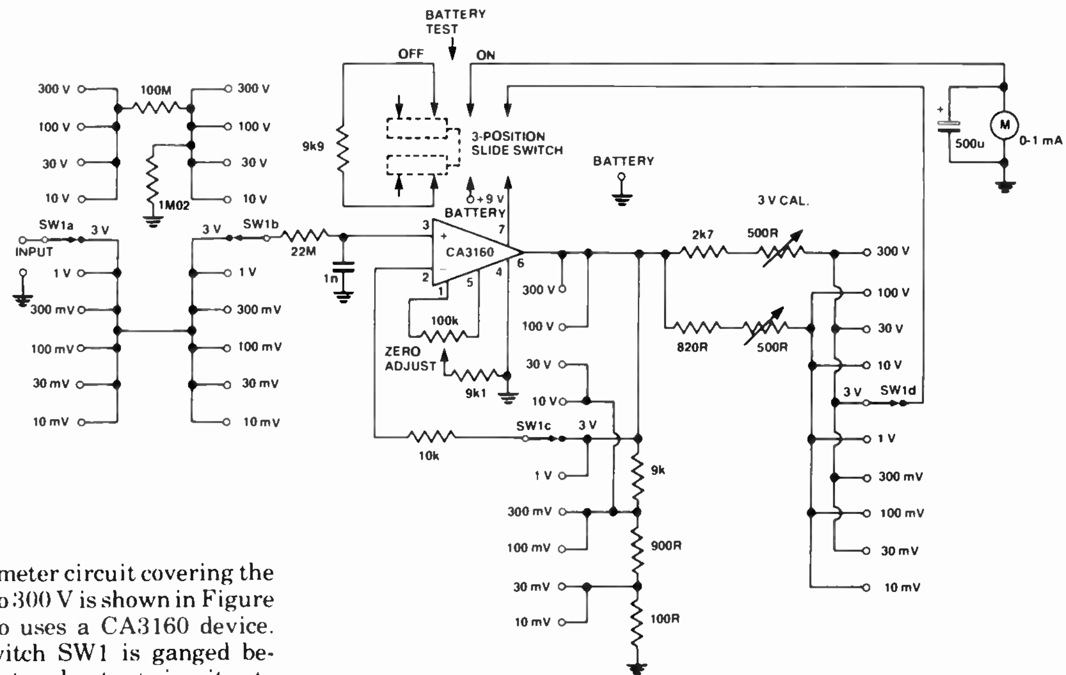


Figure 18. **This circuit will measure *very* low currents — full-scale deflection is ± three picoamps!**



Voltmeter

A further voltmeter circuit covering the range 10 mV to 300 V is shown in Figure 19, which also uses a CA3160 device. The range switch SW1 is ganged between the input and output circuitry to enable the proper output voltage for feedback to terminal 2 through the 10k resistor to be selected.

Figure 19. **Example of a multi-range voltmeter measuring from 10 mV to 300 V.**

This circuit is powered by a single 8.4 V mercury battery, the power supply current being somewhat less than 500 uA plus the meter current required to indicate a given voltage. Thus the supply current rises to about 1.5 mA at full-scale deflection.

Any readers who experience problems in obtaining a CA3160 may use a CA3130 with a frequency compensation capacitor of about 56p between pins 1 and 8.

The aim of this article has not been to introduce readers to all the latest BiFET and BiMOS devices (of which there are large numbers), but rather to give an indication of the wide selection of circuits that can be made with just a few of the standard types of device which are readily available. ●

Digital car alarm

Ian Robertson

The aim in developing this alarm unit was to provide the most comprehensive system yet developed for home construction. To this end, the circuit includes most of the features found in better known commercial alarms, with the added bonus of converting into a wiper delay system when the alarm is not in use.

A MAJOR DIFFERENCE between this and other alarm circuits is the use of digital rather than analogue methods. The circuit uses a master oscillator feeding a divider chain to obtain the many time delays needed. Indeed the arrangement is in many ways similar to an electronic organ circuit.

An advantage of the digital technique is that all the delays maintain a fixed ratio to one another. They do not vary, as an analogue circuit will, due to component tolerance, leakage, temperature, etc and, by adjusting a single potentiometer in the master oscillator, all timing functions can be varied simultaneously. This means it is sufficient to check the accuracy of a single delay period to have, in effect, checked the accuracy of all delay periods. Further, by running the oscillator at, say, ten times normal frequency, a complete test that would normally take two minutes, will take under fifteen seconds.

With any alarm of this complexity the time and skill needed to carry out the installation within the car should not be underestimated. Fortunately there are a number of optional features in the system, and even if these are not used, the alarm will still be very effective. This gives each constructor the means whereby he can make the initial installation as simple or as complex as he wishes, while retaining the option of fitting the missing items at a later date.

Features

The following is a list of the main features in the system. Each item gives only a brief description. Greater detail will be found elsewhere in the text.

Flashing indicator

In operation whenever the alarm is set. Intended to deter a potential burglar, the indicator also reminds the owner to disable the system upon entering the car.

Battery detector

Sensitive to the drop in voltage occurring whenever the load on the electrical system changes. Normally opening a door, operating the brake, switching the headlights on, or a number of similar actions, will trip the detector.

Two delayed trigger inputs

Used in addition to (or in place of) the battery detector. These inputs are particularly useful in cars equipped with electric clocks, where the battery detector cannot always be successfully used. Suitable trigger inputs are the roof light, boot, bonnet and glove box lights. However, these must be powered from a circuit that remains energised at all times, even when the ignition is switched off.

Four instantaneous trigger inputs

These are suitable for the protection of driving lights, cassette player, radio, etc. In use a wire is clamped under one of the mounting bolts of the item to be protected. Should this wire become detached from the chassis, as it will if the protected item is removed, the horn will sound immediately.

Hidden switch option

Normally the alarm is cancelled by operating the ignition switch, however with this extra switch in circuit, a thief must locate both switches before he can cancel the alarm. The hidden switch will also prevent children, or curious adults, setting the alarm while the car is parked.

Alarm relay

The alarm section is fitted with a two pole relay. One contact set is used to operate the horn while the other contacts may be used to flash the headlights or disable the ignition circuit or perhaps operate a second horn installed in the boot. It helps to have a second line of defence should the horn be faulty or disconnected.

Alarm timing

- Time to exit vehicle: 15 seconds
- Time to enter vehicle: 15 seconds
- Duration of horn: 96 seconds
- Horn pulse rate: one second on, one second off
- Indicator pulse rate: half second on, half second off.

Wiper option

Whenever the alarm is not in use, the circuit converts into a wiper control unit. The output from this section is once again via a relay, it has a single changeover contact and will suit most wiper systems.

Wiper timing

The wiper control switch settings are:

- Continuous wipe (CW), normal slow speed wiper operation
- Single wipe (SW), single operation every 2, 4, 8, 16, 32 or 64 seconds.
- Multiple wipe (MW), dual operation every 8, 16, 32 or 64 seconds.

Operation

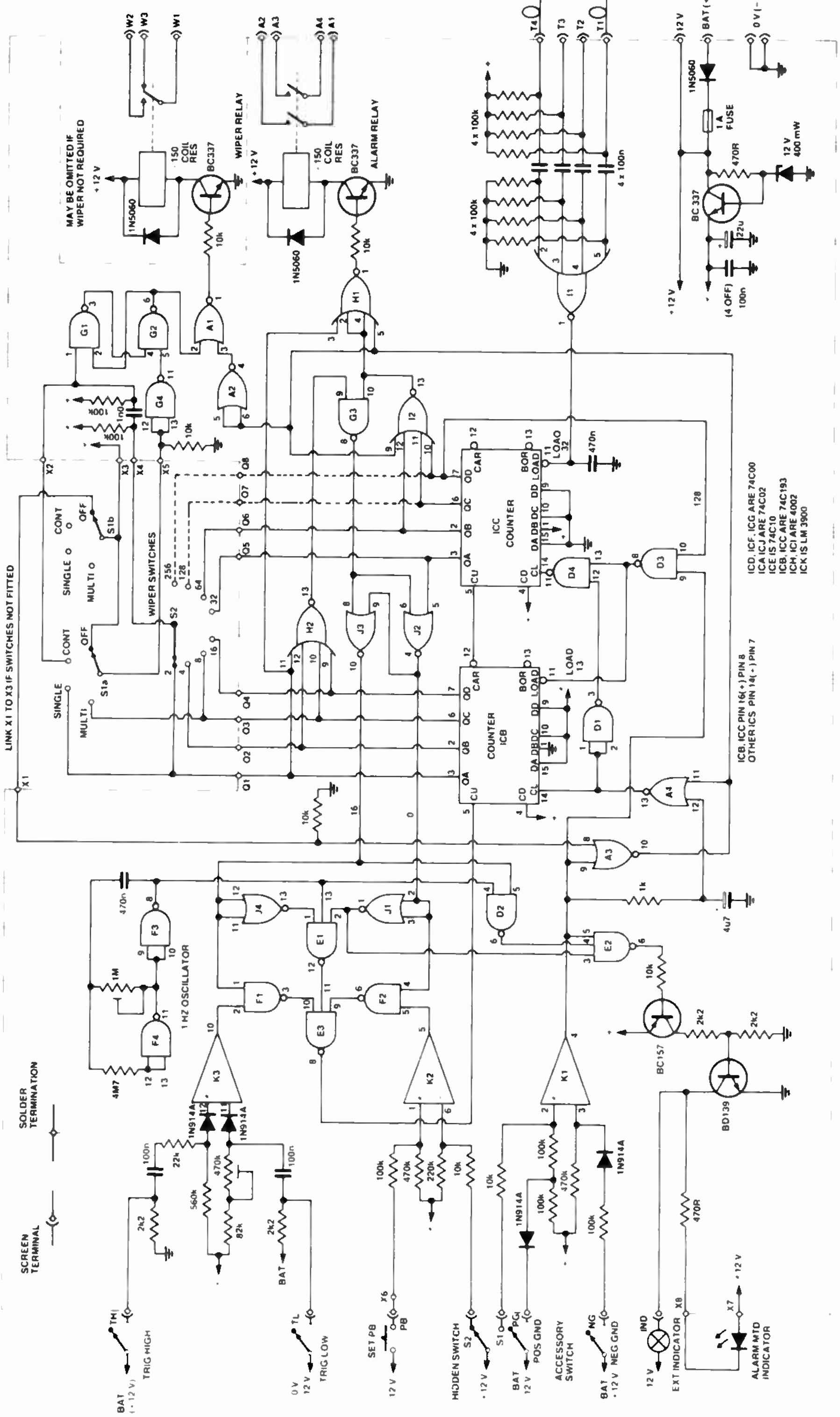
The heart of the alarm is an eight stage binary counter (ICs B & C) clocked by a 1 Hz master oscillator. By this means a delay of 256 seconds will occur whenever the counter is taken from zero count to maximum count. Shorter delays are available by using the various outputs, Q1 through Q8. In fact, any delay between one second and 256 seconds can be obtained by suitably decoding the 'Q' outputs.

Below is a list of the outputs that have been decoded and also their main functions:

- **Zero** — Interrupts the clock pulses, freezes the counter, holds the indicator off. Pressing the set pushbutton advances the counter. ▶

- **1 to 15** Time allowed to leave the car without triggering the alarm. During this period the indicator remains on.
- **16** Interrupts the clock pulses, freezes the counter, flashes the indicator. Counter restarted by a signal from the battery detector or the delayed trigger inputs.
- **17 to 31** Time allowed to enter the car without the horn sounding. The alarm may be reset to zero by operating the ignition switch (also the hidden switch should this be fitted).
  The indicator will remain on for any count greater than 16.
- **32 to 127** Alarm relay operates, pulsing the horn at one second intervals.
- **128** Returns the count to 16 where it may be retriggered should further interference to the car be detected.

Circuit of the car alarm system. The dashed line indicates the electronics located in the diecast box I used to house the unit.



In addition to the above, if at any time one of the instantaneous trigger inputs becomes detached from the chassis, the counter will set to 32 and the sequence will begin with the horn sounding immediately.

Similarly, any interruption to the power supply will set the counter to 32. This item is included to prevent cancelling of the alarm by simply removing the battery lead for a few seconds.

The conversion of the circuit from an alarm to a wiper system is under the control of the car ignition circuit:

- With the ignition and hidden switches OFF the alarm is activated, the wiper disabled
- With the ignition and hidden switches ON the wiper is activated, the alarm disabled. Or more simply, the alarm is enabled when the car is not in use, the wiper when the car is in use.

The basic requirement of any wiper control system is to pulse the wiper motor for approximately one second, then follow with a delay (variable) before the next one-second pulse. The length of the pulse is not critical, once the wiper has started to move the normal parking contacts will take over and complete the wipe cycle. Should the pulse be longer than required for a single wipe of the screen then more than one wipe will occur, and this is the method used to obtain dual wipes in the multi-wipe switch setting.

This circuit operates by allowing the counter to free run, while feeding the signal from a Q output (selected for the delay required) via a one-second pulsing network to the wiper relay. This gives a chain of one-second pulses separated by a switched delay interval. The pulse is extended to four seconds in the multi-wipe setting.

Circuit description

Readers should refer to the various logic and circuit diagrams to clarify points raised in the following description.

All system timing is developed around the eight stage binary counter (ICs B & C). Two 74C193 up/down counters are used. However, in this circuit the down-count facility is not used. This proved to be the simplest way to obtain asynchronous load and clear inputs. Other counters I considered either lacked these inputs or they were of the synchronous type.

The counters are clocked by the 1 Hz master oscillator (ICs F3 & F4). This is a standard CMOS two-gate squarewave oscillator where the frequency can be adjusted over a wide range by the 500k preset.

Selective decoding of the counter outputs is carried out by the gates shown above the counter (main circuit); decoded are 0, 16, › 32 and 128.

Normally the counter will free run unless the clock pulses are interrupted by gates E1 & E3, and this will occur at counts 0 and 16. If the count is stopped at zero it may be restarted by a pulse from the set push button, if stopped at 16 may be restarted by a pulse from the battery detector, trigger high or trigger low inputs.

Any counter greater than 32 will operate the horn via the horn relay and gate H1. Note also that gate H1, and therefore the horn, is pulsed on and off by output Q1 on counter B.

Various gates below ICs C and B are used to clear and load the counters. These inputs, as mentioned earlier, are synchronous and may be operated at any time, even during periods when the clock is halted. The way these inputs have been used needs explanation.

Turning the ignition on resets both counters, and this in turn interrupts the clock and holds the alarm in the standby position.

A signal from one of the four instantaneous trigger inputs will set the counter. In this instance a count of ⩾ 32 will be loaded, causing the horn to sound, and continue to sound, while the counter steps through to 128. In a similar manner, the capacitor on the load terminal of C will force the output to ⩾ 32 for each power up of the circuit.

Reaching a count of 128 resets the counters to 13 which involves clearing counter C while loading 13 into counter B. Loading 13 will silence the horn while giving three counts for the electrical system to settle before the battery detector is rearmed at a count of 16.

Most input signals are buffered by the LM3900 quad op-amp. Keep in mind that this device compares input currents whereas the conventional op-amp compares input voltages. Using resistors to convert voltages to currents, standard operational amplifier circuitry can be realised, but note when testing that both inputs are clamped to within 0.5 V of negative by the base-emitter junction of the input transistors.

Nonetheless, the circuit operation is straightforward with K1 handling the accessory switch inputs (positive or negative ground systems), K2 buffers the set push button, while the hidden switch feeds both K1 and K2. The low value (10k) resistors used in the switch circuit can override any other input signal and will prevent the alarm being set in position S2 or cancelled in position S1.

A short RC delay network is fitted in one line from the output of K1, which resets the counters each time the accessory switch is turned off, thereby ensuring the alarm sequence will start from zero and overcome a problem that occurs if the ignition is switched off with the wiper running.

Section K3 functions as the battery drop detector while also functioning as the trigger high/low input buffer. Figure 10 shows the battery detector in a simpler form. Both inputs are fed from a common voltage, but the lower value resistor feeding the inverter input drives the output low.

If a negative pulse occurs on the battery line it will be coupled into the inverting input by the 100n capacitor. This will reverse-bias the inverting input resulting in the op-amp output going high and developing a pulse to advance the counter one count. In the final circuit a diode is included in series with the op-amp input, this means the diode and not the inverting input is driven negative, and prevents possible damage to the IC.

Delayed trigger inputs TL and TH operate in a similar fashion. Note that in this instance the TL input feeds a negative pulse into the inverting input while the TH input is somewhat different as it feeds a positive pulse into the non-inverting input. The result however, is the same — a positive pulse at the output of K3.

The instantaneous trigger inputs (T1 and T4) are quite different. Normally, the four inputs are held at earth potential so that, should any input be detached, a pulse will enter the NOR gate via the appropriate RC network. A negative-going pulse occures at the output of the gate, loading 32 into the counter, thereby enabling the horn sequence. Unused inputs can in practice be left floating, as they respond to the change in voltage not the voltage level.

An important feature is the indicating light. This may be a LED or lamp and is operated by a two transistor driver stage, under the control of gate E2. The indicator may be off, illuminated or flashing and the sequence is as follows:

- Off when wiper operation selected
- Off for standby mode, counter zero
- Flashing when armed, count of 16
- Illuminated for all other counts.

The ICs are supplied via a series pass transistor and the function on this stage is not primarily as a regulator. The intention is to limit the voltage fed to the ICs to below the rated maximum of 15 V. In order to limit dissipation in the series transistor a 12 V zener is used. This means that the transistor is hard on with a nominal 12 V rail and will not start to regulate until the input voltage is some volts above this value.

Conversion into a wiper control unit requires that the counters free run, and to obtain this the load and clear inputs must be overridden and the gates decoding 0 and 16 must be blocked. This is under the control of the ignition switch. A logic '0' on the output of K1 sets the circuit as a wiper control and a logic '1' at this point sets the alarm function.

The free-running counter will give a squarewave signal from the various 'Q' outputs. The period in seconds given at each stage is two at Q1, four at Q2, eight at Q3, extending through to 256 at Q8. By means of an RS flip-flop (cross-coupled gates, G1 and G2) the squarewaves are converted into an asymmetrical wave having one second ON periods and switch-selectable OFF periods.

Diagram 12 shows Q3 with a period of eight seconds setting the RS flip-flop, while the inversion of Q1 resets the same flip-flop every two seconds. The resulting output, one second on seven seconds off, is clearly shown.

On the multiple wipe setting the flip-flop is reset by the inversion of Q3, not Q1, and this will give a pulse four seconds long in lieu of the previous one-second pulse. Depending on the speed of individual wiper motors two or three wipes will occur during this period.

Construction

Construction is fairly straightforward, however there are two forms this may take. The first is to build only the alarm, the second is to built the alarm/wiper combination. There are points for and against either approach and these are covered in the installation notes. In the construction there is little difference between systems, although in units without the wiper option, one relay, two switches and a couple of minor components can be omitted.

(Note that this article is not intended as an ETI constructional project and thus no pc board details are given.)

Testing

A completed unit should operate with a minimum of adjustment, however I recommend setting up the test circuit (Figure 9) to check out the alarm before fitting it into the car.

Simple faults may be located with a multimeter, but for more elusive faults an oscilloscope will be required.

The 12 V for testing may be obtained from the car's own battery, in situ, or more conveniently from a battery on the work bench. Alternatively a bench power supply may be used with the restriction that it may not test the battery detector circuit in all respects.

Steps for testing using Figure 9 are:

- Set preset potentiometers to approximately mid-way ▶

- With the power and accessory switches on, all other switches off, check that the indicator light, alarm relay and wiper relay are all off
- Move the wiper switch to continuous wipe (CW) and the wiper relay will pick up and remain up
- Move to the single wipe position (SW) and the relay will pulse at an interval determined by the second wiper switch. By adjustment of the 1M oscillator preset, the interval can be matched to the times marked on the switch. Reducing the resistance of the preset too far (frequency increasing) will stop the oscillator
- The multiple wipe setting (MW) is similar to the single wipe setting, however the relay pulse will be longer (four seconds) and switch settings 2 and 4 will give the same timing as position 8
- Turn the wiper and accessory switches off and the indicator, alarm relay and wiper relay should be off
- Momentarily operate the push button. This will set the alarm, and light the indicator for a period of 15 s (exit time)
- After the exit time the indicator will flash at one second intervals showing the alarm is set
- The alarm may now be triggered by means of the battery detector, opening a car door if the car battery is being used, or with a bench supply momentarily reducing the voltage by about three volts. If a bench battery is being used, connect a load, say a 15 W lamp, across the battery terminals. For correct operation the 470k sensitivity preset may need adjustment as maximum sensitivity is obtained with maximum resistance in circuit. Slowly rotate the preset until the indicator latches on, back off 1 mm, reset circuit (using accessory switch and the push button) and then try again
- The 15 s entry delay will occur, followed by the horn relay pulsing at one second intervals for a period of just over one and a half minutes. The circuit will reset with the indicator flashing
- The alarm may also be triggered by either the TH or TL switch and these operate in the same manner as the battery detector
- At any point during the above sequence, closing the accessory switch should cancel the alarm, forcing the relay and indicator off
- Close the instantaneous trigger switch (T1). Reset the alarm using the accessory switch and push button. Opening switch T1 will cause the horn relay to operate, pulsing for the normal 1½ minute horn period
- Momentarily opening the power switch will also cause the horn relay to operate
- Other switches can be added for a more detailed test. Add the hidden switch, PG, T2, T3, T4 switches and with either an ohmmeter or lamp, check the alarm relay contacts, wiper relay contacts and also the indicator output.

Installation

The alarm may be installed with or without the wiper components. The combined alarm/wiper system must be mounted within reach of the driver, and this can mean the unit is more accessible if the car is broken into. By foregoing the wiper control the electronics may be hidden, and by using extended leads, the push button and indicator may still be fitted in the dash. I, however, advise against mounting the wiper switches outside the alarm as the circuit could be effected by noise pulses introduced by the connecting cables.

Keep the wattage of the indicator down and use a high output LED or a low power lamp. Each time the indicator turns on it attempts to trip the battery detector. This in turn is set less sensitive, and if taken too far the system may not respond in an emergency. The roof light must be not less than four times the wattage of the indicator.

In mounting the alarm, each constructor must determine the most suitable position in his car.

Wiring should be carried out in stages, starting with the basic circuit (Figure 1 or Figure 2) followed by the optional items (Figure 3 to Figure 8). As each stage is fitted, the circuitry may be tested and the faults found. Testing stage by stage is possible with this alarm circuit because careful design has eliminated the need to bridge unused terminals to override the redundant function.

Care is required to select the correct horn circuit as this should match the existing wiring whilst also taking into account the current demand of the horn(s) to be driven. The wiring must suit the currents involved. As a guide the cables used for the relay contacts (also the 0 V and BAT circuits) should have approximately the same area as the horn wiring already fitted in your car. The remaining runs can be any standard hook-up wire and the size can be chosen for mechanical rather than electrical reasons.

During the alarm installation it is easy to overlook the part played by the wiring, for it is often the wiring and not the alarm that is most vulnerable. Take particular care to conceal the cable runs and to ensure all connections are sound and will not cause intermittent operation at a later date.

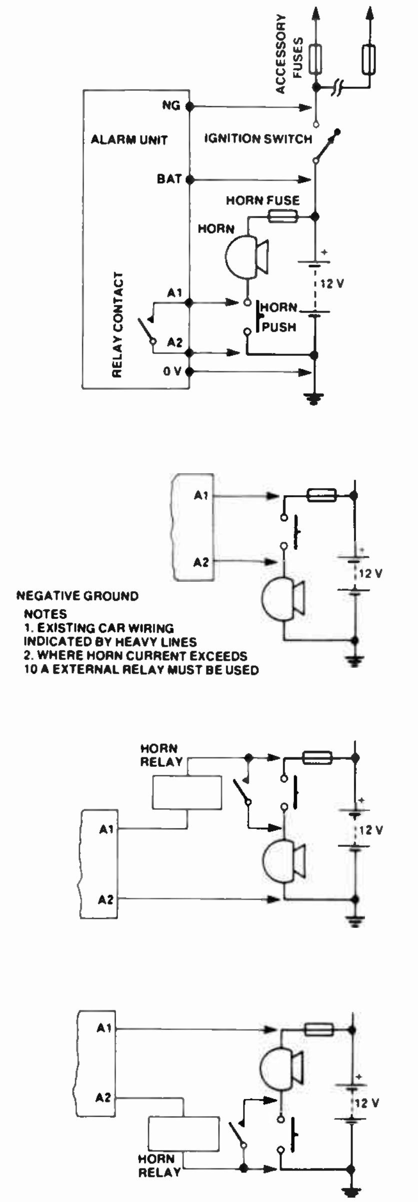


Figure 1. **Basic alarm system, negative ground, with variations to the horn circuit.**

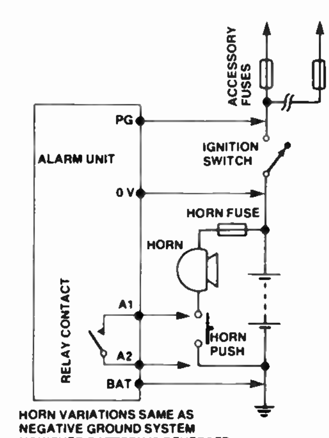


Figure 2. **Basic alarm system, positive ground.**

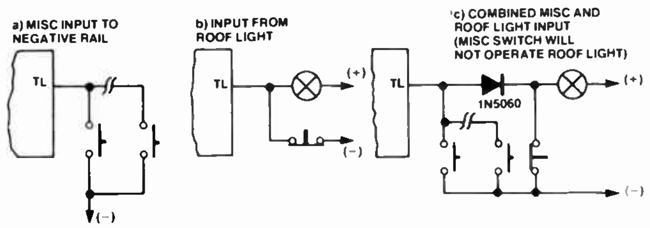


Figure 3. **TL input: using added switches or roof light.**

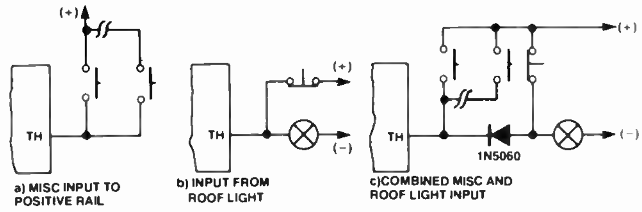


Figure 4. **TH input: using added switches or existing roof light.**

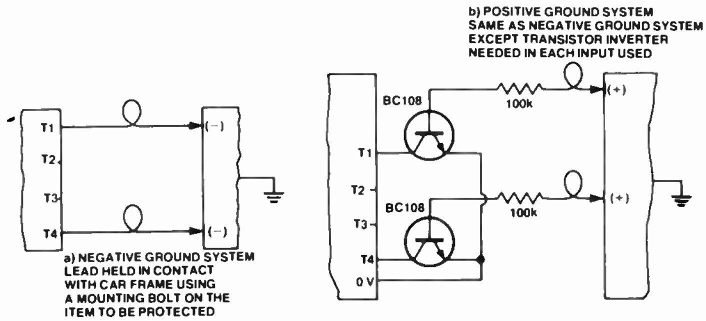


Figure 5. **T1 to T4 inputs: for driving light and radio protector.**

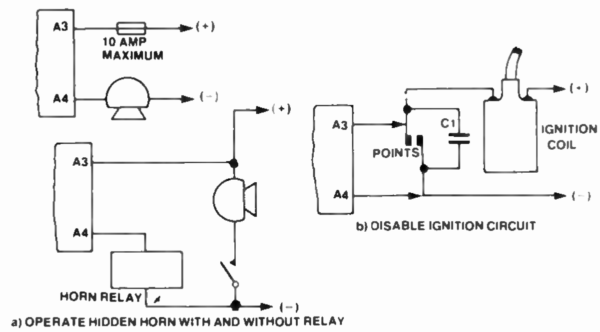


Figure 6. **A3 and A4 alarm relay contact; giving extra protection.**

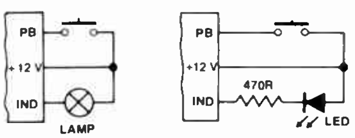


Figure 7. **PB and IND terminals: external pushbutton and indicator.**

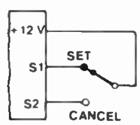


Figure 8. **Wiring a hidden switch.**

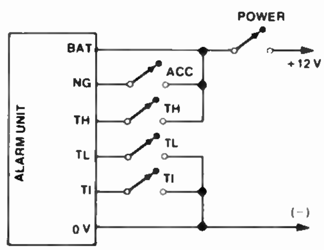


Figure 9. **Basic test circuit.**

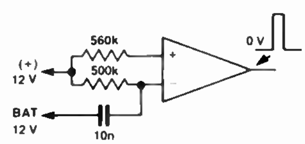


Figure 10. **Simplified battery-drop detector.**

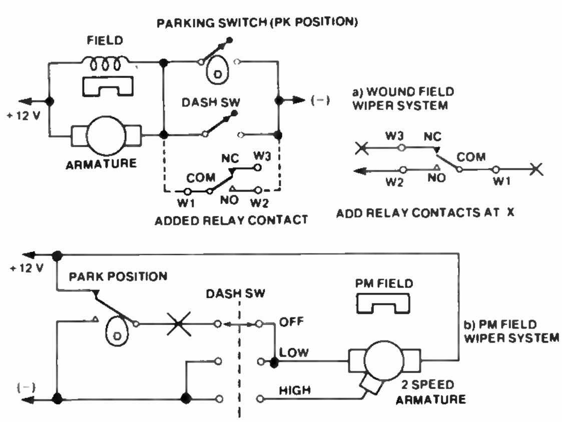


Figure 11. **Wiper operation.**

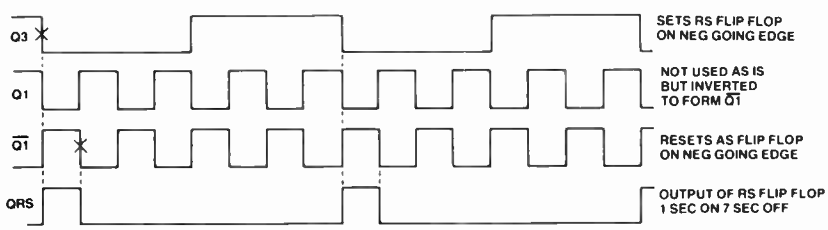
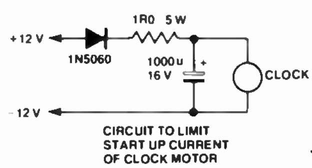


Figure 12. **Wiper circuit timing diagram.**



◁ *Figure 13.* **Clock circuit modification to prevent tripping of alarm.**

Included are a number of diagrams and these show how to wire the optional features.

- **TH & TL** Delayed inputs for connection to the roof light circuit may also be fed from any number of additional points. Possible switch positions are rear doors, tail-gate or glovebox (Figure 3 & 4).
- **T1 to T4** Instantaneous inputs are clamped under driving lights, cassette, radio, etc and will sound the horn as soon as the connection is broken. A transistor inverter stage will be necessary in vehicles with a positive ground system, however this stage should only be fitted to inputs that are actually used (Figure 5).
- **A3 & A4** Spare contacts on alarm relay may be used for a number of auxiliary functions. The contacts have a current limit of 10 A and larger currents require a horn or lamp relay to be fitted (Figure 6).

(continued on page 50)

Lab Notes

Integrated switching regulator

As we are already aware, switching power supplies are replacing linear supplies in many applications because of their higher efficiency, reduced size and generally lower cost. National Semiconductor has introduced a switching regulator building block, the LH1605.

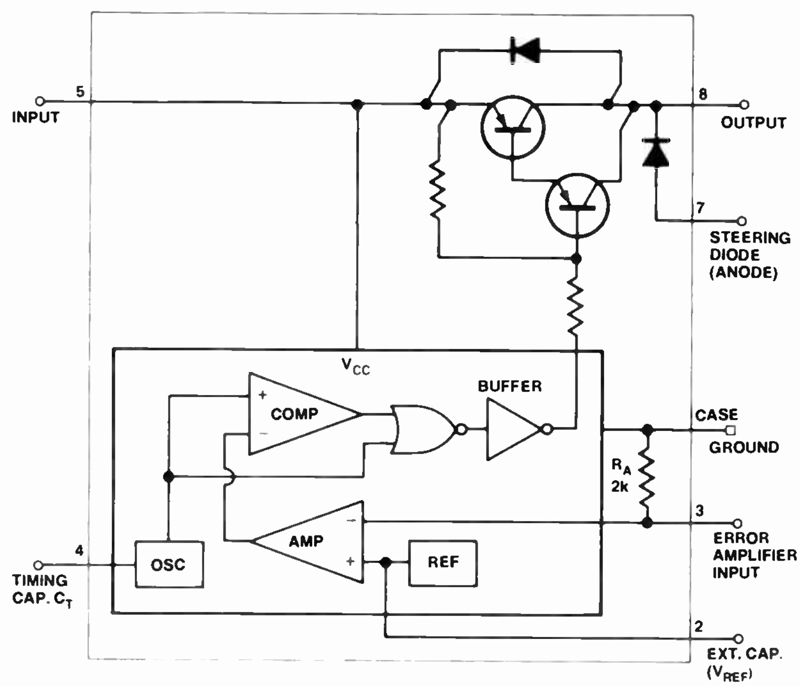
Barry Davis

THIS NEW regulator contains the power switching transistor, catch diode, and control circuitry to enable you to build an efficient switched mode power supply (SMPS). It has an adjustable output from 3 to 30 volts, a current capability of 5 amperes and is available in an 8-pin TO-3 package.

The features of the regulator are:

1. Output adjustable from 3 to 30 V.
2. 5 A output current
3. Step-down operation
4. High efficiency
5. Frequency of operation adjustable to 100 kHz
6. Maximum input voltage 35 V
7. Minimum input-output voltage differential = 5 V
8. TO-3 package.

The internal construction and the base connections of the integrated circuit are shown in Figure 1.



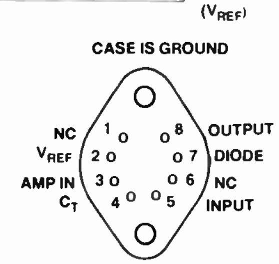


Figure 1. **Block diagram and base connections of the LH1605.**

Application details

The LH1605 is a step-down positive dc to dc switching converter with built-in control circuits, power transistor and catch diode. Few additional external components are required to provide an SMPS of 5 A capability. In the simplest design form, a timing capacitor (C_T) determines the operating frequency, an LC filter provides a low ripple dc output voltage and a single resistor sets the level of the output voltage. (R_s).

The value of R_s may be calculated from the formula:

$$R_s = 2\,k\Omega\,\frac{V_{out} - 2.5\,V}{2.5\,V}$$

A typical circuit is shown in Figure 2. R_s is made adjustable to allow the output voltage to be varied. Capacitor C1 is included to improve noise rejection by bypassing the reference (pin 2).

Operation

A basic step-down switching regulator circuit is shown in Figure 3.

Transistor Q is the switching element which has the 'on' and 'off' times controlled by a pulse width modulator (PWM). When Q *is on* power is drawn from the input and supplied to the load. The capacitor (C) charges and a voltage is developed across the inductor L. The diode (D) has a positive potential at its cathode, because Q is saturated, and is therefore held in reverse bias (off).

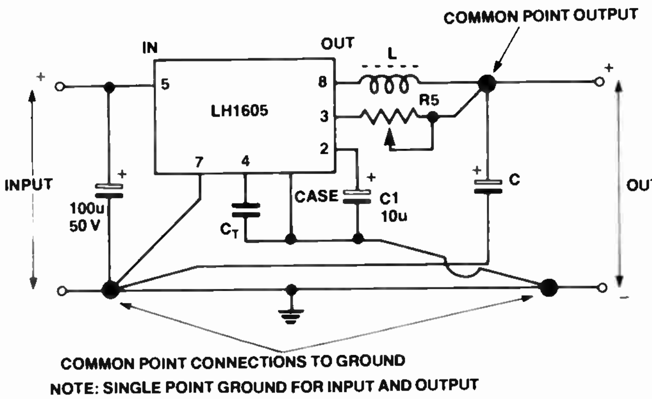


Figure 2. **Typical circuit applications.**

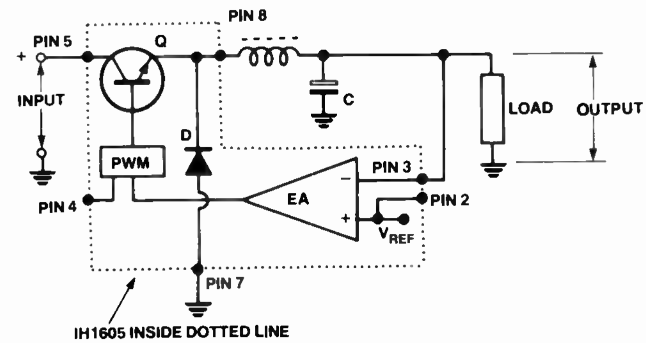


Figure 3. **Basic switched-mode power supply.**

When *Q is off,* the magnetic field stored in the inductor collapses. The polarity of the voltage across L reverses, forcing the diode into forward bias (on).

The energy stored in the inductor is released and the inductor current passes through the loop formed by the diode, inductor, and capacitor/load, thereby maintaining an output current.

The control circuit error amplifier (EA), samples the output voltage and automatically increases the 'on' time of Q if the output voltage decreases. Likewise it increases the 'off' time of Q if the output voltage increases.

This automatic action constantly compares the output voltage with a reference voltage and provides the necessary correction by varying the conduction time of Q.

With this type of circuit, the output can be calculated from the formula:

$$V_{out} = V_{in} \times \frac{t_{on}}{T}$$

where t_{on} = Q conduction time in seconds and T = period of one cycle of PWM (i.e. $t_{on} + t_{off}$).

Design procedure

The design of a complete voltage regulator with the LH1605 is relatively straightforward. However, prior to designing an operational circuit we must be aware of five circuit parameters. These are:

1. Maximum and minimum input voltage.
2. Required output voltage.
3. Maximum and minimum load current.
4. Maximum allowable ripple voltage.
5. Desired switching frequency.

Using the following parameters a design example can be given.

V_{in} (max) = 15 V
V_{in} = 10 V
V_{out} = 5 V
I_o (max) = 3 A
I_o (min) = 1 A
Output ripple Ωv_o = 20 mV
Operating frequency = 25 kHz

The values of the output L and C can be calculated, but firstly the 'off' time is required.

$$t_{off} = \frac{1 - \frac{V_{out}}{V_{in\,(max)}}}{f} = \frac{1 - \frac{5}{15}}{25\text{ kHz}} = 26.7\text{ usecs}$$

The minimum equivalent frequency of the switching transistor at minimum input voltage is:

$$f(min) = \frac{1 - \frac{V_{out}}{V_{in\,(min)}}}{t_{off}} = \frac{1 - \frac{5}{10}}{26.7\text{ us}} = 18.7\text{ kHz}$$

The allowable peak to peak ripple current through L is:

$$\Delta i = 2 \times I_{o\,min} = 2 \times 1A = 2A$$

The inductance L can now be calculated.

$$L = \frac{V_{out} \times t_{off}}{\Delta i} = \frac{5 \times 26.7\text{ us}}{2A} = 67\text{ uH}$$

The value of minimum output capacitance is given by:

$$C = \frac{\Delta i}{8 \times f_{(min)} \times \Delta v_o} = \frac{2A}{8 \times 18.7\text{ kHz} \times 20\text{ mV}} = 688\text{ uF (minimum)}$$

Because of the high value of ripple current, the capacitor must have a low equivalent series resistance (ESR):

$$ESR_{max} = \frac{\Delta v_o}{\Delta i} = \frac{20 \times 10^{-3}}{2} = 0.01\text{ ohms}$$

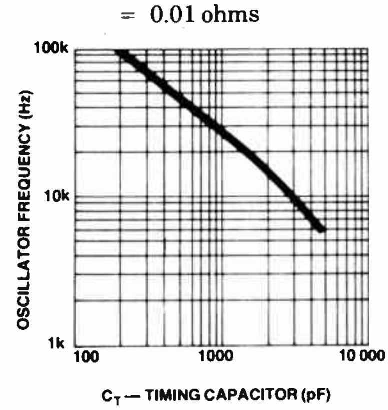


Figure 4. **Frequency vs. timing graph.**

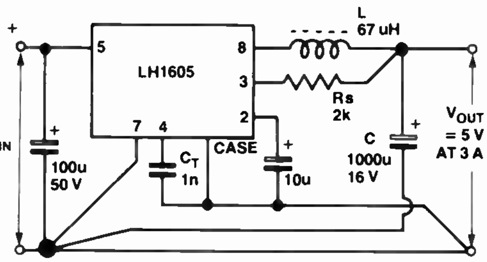
Using the frequency/timing capacitor graph in Figure 4, a 0.001 uF (1 nF) capacitor used as the timing component will provide an operating frequency of 25 kHz. ▶

Lab Notes

The output voltage of 5 V can now be programmed by calculating the value of Rs.

$$Rs = 2\,k\Omega\ \frac{V_{out} - 2.5}{2.5}$$
$$= 2\,k\Omega\ \frac{5 - 2.5}{2.5}$$
$$= 2\,k\Omega$$

The completed circuit is shown in Figure 5.



NOTE: $V_{IN} - V_{OUT}$ DIFFERENTIAL MUST BE 5 V MINMUM

Figure 5. **Example circuit values.**

Choice of inductor core

The power handling capability of the inductor is reflected in the type of core material chosen. LI^2 must be calculated to determine the minimum useable inductor core *without* core saturation. L is the inductance previously calculated and I is the dc output current. It equals $Io_{(max)} + \Delta i$.

There are two popular core materials available —

1. molypermalloy
2. ferrite.

Ferrite potcores have the advantage of ease of winding and self-shielding against inherent magnetic fields. Molypermalloy cores are capable of higher flux density for a given core size.

Once the core is selected from the manufacturer's catalogue, the number of turns for the winding (N) can be calculated:

$$N = 1000\sqrt{\frac{L}{L_{1000}}}$$

N = number of turns, L = inductance required. L_{1000} = inductance (mH/1000 turns) for the core, given by the manufacturer.

For example, in the design exercise, the desired value of L was 67 uH:

$$\text{Peak } I^2 = (3\text{ A} + 2\text{ A})^2$$
$$= 25\text{ A}$$

Therefore:

$$LI^2 = 67\text{ uH} \times 25\text{ A}$$
$$= 1.68\text{ millijoules}$$

The permalloy core chosen has a nominal inductance of 120 mH per 1000 turns. Therefore:

$$N = 1000\sqrt{\frac{67\text{ uH}}{120\text{ mH}}}$$
$$= 24\text{ turns}$$

Heatsinking

There will be significant self-heating due to internal power dissipation, even at moderate output power. The junction temperature must be kept as low as possible under operating conditions (maximum temperature 150°C). Good heatsinking is essential and a mica washer complete with 'thermal' paste is recommended, along with a TO-3 styled heatsink.

Short circuit protection

The LH1605 will be *permanently damaged* if under a short circuit condition for longer than 10 milliseconds, and it is therefore desirable to add current limit protection to the circuit. A current limit circuit is shown in Figure 6.

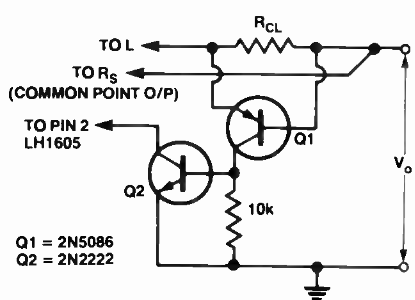


Figure 6. **Short circuit protection.**

The value of R_{CL} is determined by the current limit you decide to set. It can be calculated from the formula:

$$R_{CL} = \frac{660\text{ mV}}{I_{sc}}$$

where I_{sc} = short circuit current.

The voltage developed across R_{CL} by the short circuit current (600 mV) will turn transistor Q1 on. The increase in I_c of Q1 will develop a voltage across the 10k resistor, making the base of Q2 more positive with respect to the emitter. Q2 will turn on, pulling the reference of the control circuit (pin 2) down towards ground. The error amplifier suddenly sees too high an output voltage. This shuts the series pass transistor off in the LH1605 by reducing the switching time, thereby reducing the output voltage to the level of the reference.

A complete power supply with current limiting at 3.25 A is shown in Figure 7.

Evaluation kit

A *complete* evaluation kit including the printed circuit board, inductor, and specification sheet is available from:

National Semiconductor
Cnr. Stud Road & Mountain Highway
Bayswater
Vic. 3153.

The evaluation kit, SR1605, is fully assembled and ready for immediate use. It is designed to accept any unregulated input voltage from 10 to 25 V and provide a 5 V 3A output.

Acknowledgement

This article was made possible by the courtesy of National Semiconductor. Data was taken from their publication: LH1605 5 Amp High Efficiency Switching Regulator.

Further information on the operation of switched mode power supply circuits can be obtained from the book 'Understanding dc Power Supplies', by Barry Davis; publisher: Prentice Hall. ●

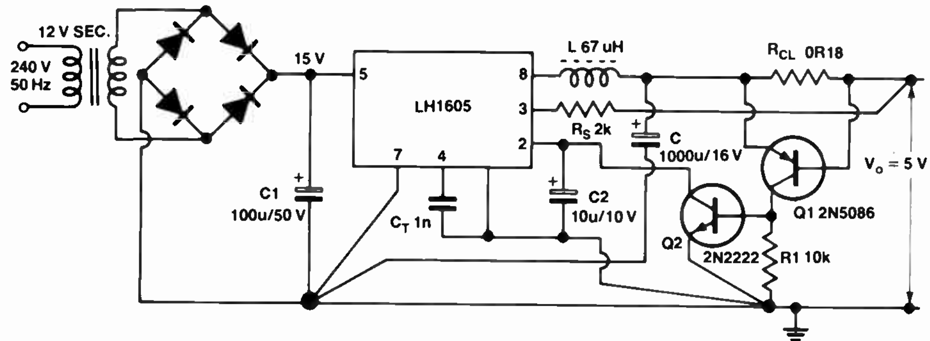


Figure 7. **5 V SMPS with short circuit protection.**

Instrumentation techniques

Tim Orr

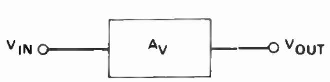
The following sections describe several electronic measurement techniques, and by adopting a modular approach it will be possible to construct a wide range of electronic measurement systems. First of all, though, we'll look at some of the units involved and try to clear up some of the confusion about them.

The Decibel

The decibel (dB) is a convenient way of expressing signal gain or loss in a system. When a signal passes through several amplifiers or filters the signal level may alter; the overall system gain is the product of all the individual gains. However, it is easier to add a series of numbers than to multiply them and so it is easier to convert the signal gains into a logarithmic equivalent which can then just be added or subtracted. This is equivalent to multiplying and dividing in the linear world. The calculation of gain in dBs is shown Table 1. The chart shows a range of dB values and their equivalent multiplier. These multipliers are often abbreviated by engineers (see rule of thumb), just to make life easy.

TABLE 1

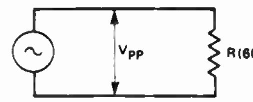
dB	MULTIPLIER	RULE OF THUMB MULTIPLIER
+80	×10,000	10,000
+70	×3162	3,000
+60	×1000	1,000
+50	×316.2	300
+40	×100	100
+30	×31.6	30
+20	×10	10
+18	×7.94	8
+12	×3.98	4
+10	×3.16	3
+6	×1.99	2
+3	×1.41	1.4
0	×1.00	1.0
−3	×0.708	0.7
−6	×0.501	0.5
−10	×0.316	0.3
−12	×0.251	0.25
−18	×0.126	0.125
−20	×0.100	0.10
−30	×0.032	0.03
−40	×0.010	0.01
−50	×0.0032	0.003
−60	×0.001	0.001
−70	×0.00032	0.0003
−80	×0.0001	0.0001



$A_V = \frac{V_{OUT}}{V_{IN}}$, OR IN dBs $= 20LOG\left(\frac{V_{OUT}}{V_{IN}}\right)$

0dBm IS USED AS A VOLTAGE MEASUREMENT.

0dBm IS A SINEWAVE LEVEL THAT DISSIPATES 1 MILLIWATT OF POWER INTO A 600R LOAD



THE POWER DISSIPATED $= \frac{V_{PP}^2}{8 \times R}$

∴ FOR 1mW, $V_{PP}^2 = 8 \times R \times 10^{-3}$

$V_{PP} = \sqrt{8 \times 600 \times 10^{-3}} = \sqrt{4.8}$

$V_{PP} = 2.1909V$

∴ 0dB IS EQUIVALENT TO 2.1909 V_{PP} or 0.7746 V_{RMS}

THIS IS USUALLY ROUNDED OFF TO 2.2 V_{PP} or 0.775 V_{RMS}

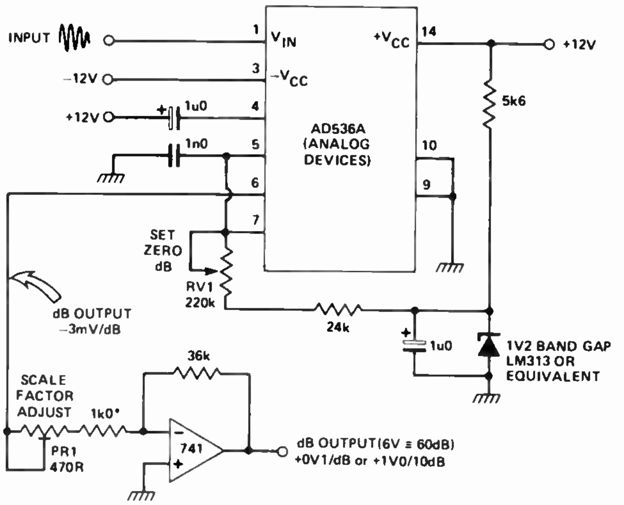
Fig. 1 Everything you ever wanted to know about the dBm!

The dBm

The dBm is used to describe a signal level and not signal gain and loss as for the dB (Fig. 1); it is widely used in audio and telecommunication engineering. For example, microphone amplifiers often have their equivalent input noise voltage expressed in dBm. If, say, this noise is −124 dBm and a microphone is being used that delivers a signal level of −40 dBm, then the signal-to-noise ratio at the output of the amplifier is 124 − 40 = 84 dB. Not exactly a difficult calculation! Table 2 shows a chart of dBm signal levels. The dBm is meant to be used for 600 ohm impedances; however the same signal level across any load is referred to as the dBU. ▶

TABLE 2

dBm	V RMS	$V_{p\text{-}p}$
+20	7V75	22V
+18	6V16	17V47
+12	3V08	8V76
+10	2V45	6V95
+6	1V55	4V39
+3	1V094	3V11
0	775 mV	2V2
−3	549 mV	1V56
−6	388 mV	1V1
−10	245 mV	695 mV
−12	197 mV	553 mV
−18	97.6 mV	277 mV
−20	77.5 mV	220 mV
−30	24.5 mV	69.5 mV
−40	7.75 mV	22 mV
−50	2.45 mV	6.95 mV
−60	775 uV	2.2 mV
−70	245 uV	695 uV
−80	77.5 uV	220 uV
−90	24.5 uV	69.5 uV
−100	7.75 uV	22 uV
−110	2.45 uV	6.95 uV
−120	775 nV	2.2 uV
−130	245 nV	695 nV



*USE A TEL LABS Q81 IF POSSIBLE. THIS HAS A T_C OF +3500PPM/°C. IT COMPENSATES FOR DRIFT IN THE AD536A

Fig. 2 Circuit for a dB meter using an Analog Devices IC.

Measuring Decibels

The AD536A is an RMS-to-DC converter chip, which is made by Analog Devices. It contains an absolute value circuit, a squarer/divider and a current mirror. With these elements it can compute a true RMS value or a log (dB) equivalent of the input signal. The circuit in Fig. 2 has a useful operating range of 60 dB. PR1 sets the scale factor of the meter. Insert a 1 V peak-to-peak sine wave and then change it to 100 mV peak-to-peak; this is to a change of 20 dB and so the preset PR1 should be adjusted for a 2 V change in the output voltage. RV1 sets 0 dB by inserting a current that cancels the log output current from the squarer/divider. This can be used to measure absolute voltage in dBm by setting zero at an input voltage of 775 mV RMS. Alternatively it can be used to compute a dB ratio. Insert a signal, set zero and then change the input signal level — the resulting output change will represent the dB change in input level. Note that the input of the AD536A can accept DC signals, but a small DC offset on the input signal will add a large error to low level readings. For the computation of dBs for AC signals it is best to AC-couple the input with a 4u7 capacitor.

RMS To DC Conversion

The AD536A calculates the true RMS value of the input signal by converting it to an absolute value. It is then squared, averaged and then square rooted. The result is a DC voltage that is equal to the RMS value of the input signal (Fig. 3). Most moving coil AC voltmeters are

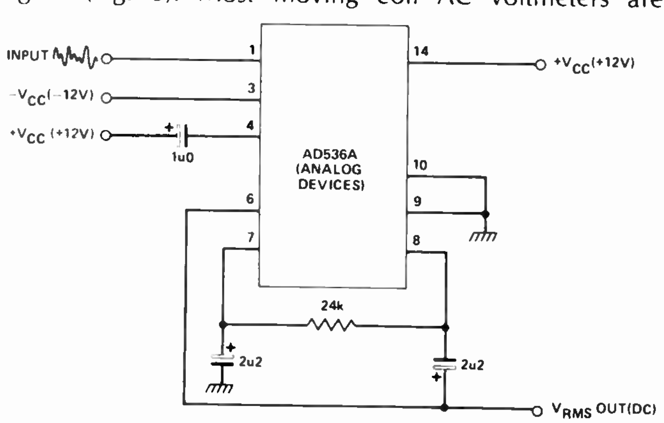
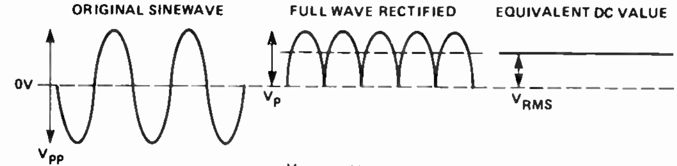


Fig. 3 The same chip can be used for an RMS to DC converter.



$$V_{RMS} = \frac{V_P}{\sqrt{2}} = \frac{V_{PP}}{2 \times \sqrt{2}}$$

$$V_{RMS} = 0.707\ V_P = 0.353\ V_{PP}$$

Fig. 4 Sine wave level measurement.

calibrated for sine wave operation only; the peak voltage of the sine wave is multiplied by 0.707 to produce the RMS value (Fig. 4). This type of meter will give wrong readings if noise, square waves, triangle waves or any non-sinusoidal signals are measured, as in Fig. 5. To measure any non-sinusoidal waveform a true RMS converter is needed, otherwise the reading could be wrong by a factor of 5!

WAVEFORM	RMS	CREST FACTOR*
SINEWAVE (V_P)	0.707 V_P	$\sqrt{2} = 1.414$
SYMMETRICAL SQUAREWAVE (V_P)	1.0 V_P	1.0
TRIANGLE WAVE (V_P)	$\frac{V_P}{\sqrt{3}} = 0.577\ V_P$	$\sqrt{3} = 1.732$
NOISE (2 V_P)	TRUE RMS	3.0 TO 4.0 DEPENDS ON THE SPECTRUM
SPIKE (V_P)	TRUE RMS	10.0 DEPENDS ON SHAPE!

$$\text{*THE CREST FACTOR} = \frac{V_P}{V_{RMS}}$$

Fig. 5 Measuring different waveforms.

Noise Annoys

All electronic components generate noise, and the combined effect of all the noise components in a system gives rise to the phenomena of a noise floor. This is a background noise signal that is forever present. The measurement that is often used to describe the noise performance of a system is called the signal-to-noise ratio which is expressed in dB. This is the ratio between the normal operating signal level and the residual noise level with the signal removed. Measurement of the signal is relatively straightforward; a sine wave signal can easily be measured with an AC voltmeter, to give the RMS value. The noise measurement is more difficult. First, the noise level will probably be very low and so it will need amplification. Second, we will only be interested in noise within a certain bandwidth. Noise outside our selected bandwidth will make the noise reading seem larger than it really is. Therefore we will need to band-limit our amplifier. For audio applications a bandwidth from 20 Hz to 20 kHz is often used.

Finally, noise is a random process and it has a constantly varying ratio between its peak and RMS voltage. A simple rectifying and smoothing process will give an erroneous reading and a *true* RMS-to-DC converter is need-

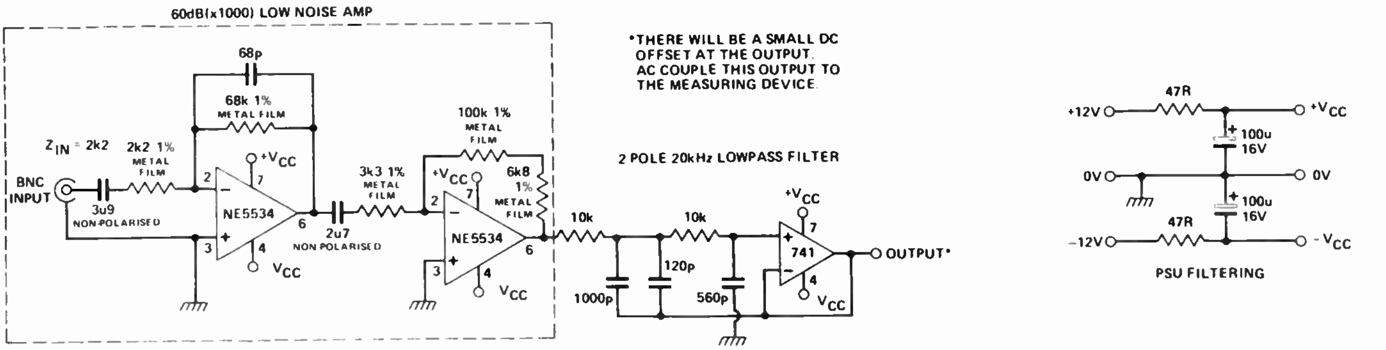
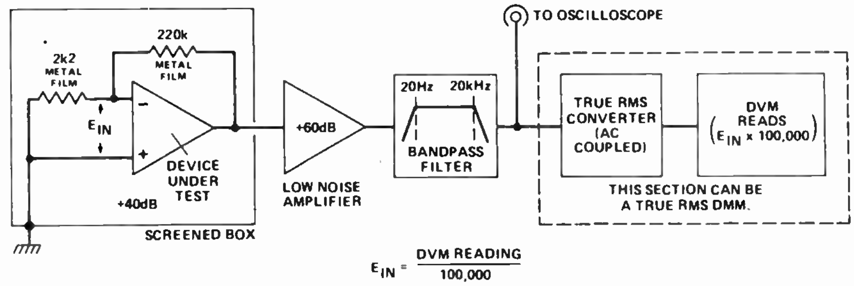


Fig. 6 (Above) A low noise 60 dB amplifier and 20 Hz to 20 kHz filter.

Fig. 7 (Right) Measuring noise in op-amps.



ed for correct readings. Thus by using a band-limited amplifier with a true RMS converter it is possible to accurately measure the residual noise level. A suitable amplifier and filter for audio work is shown in Fig. 6. The NE5534 op-amps are low noise devices, so they will contribute very little noise to the output signal. The amplifier has a voltage gain of 60 dB and so the output reading must be attenuated by the same amount; Table 1 shows the equivalent is ×1000, so millivolts turn into microvolts. This calculation assumes a flat noise spectrum.

Figure 7 is a circuit that measures the equivalent input noise of op-amps. The circuit has an overall gain of 100 dB (× 100,000) and so the DVM reading must be attenuated by this factor; additional filtering may be included to remove hum or to produce an A-weighting.

The noise often has an A-weighting frequency response applied to it before measurement (Fig. 8). This curve is similar to the frequency sensitivity of the human ear and so by A-weighting the noise measurement it becomes a subjective quantity. It also improves the apparent noise performance figure. Usually when you make a noise reading there is a mains hum component that is actually bigger than the noise. This can be removed with a 400 Hz high pass filter as in Fig. 10. This filter also removes some of the energy of the noise below 400 Hz, but even so the noise reading is still useful. Sophisticated digital multimeters often give you the choice of 400 Hz high-pass, 30 kHz and 80 kHz low-pass and A-weighting filters; sometimes they also have the facility for true RMS, dBm and dB ratio measurements.

Noise in op-amps is specified in nV/√Hz. The equivalent input noise voltage is:

$$E_{IN} = E_n \times \sqrt{\text{BANDWIDTH}}$$
$$= (E_n \times 141) \text{ nV for a 20 kHz bandwidth}$$

where E_{IN} is the equivalent input noise voltage in V RMS

E_n is the input noise in nV/√Hz.

The calculation assumes a flat noise spectrum.

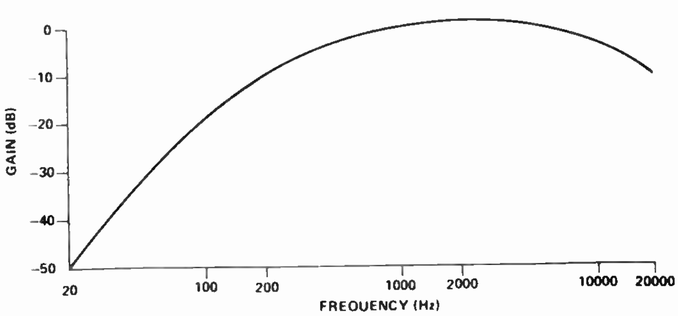


Fig. 8 The IEC 'A' weighted curve.

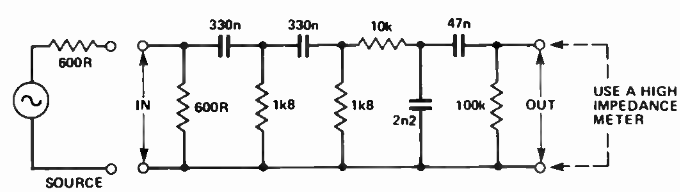


Fig. 9 An IEC 'A' weighting circuit.

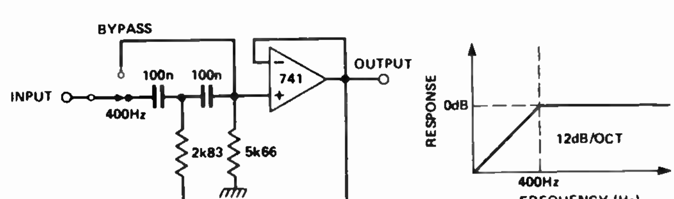


Fig. 10 A 400 Hz two pole high pass filter.

Clock or square wave generators

How to use transistors, op-amps and 555 timers to make a variety of square wave or 'clock' generator circuits.

Ray Marston

THE 'SQUARE WAVE' generator is one of the most basic circuit blocks used in modern electronics. It can be used for 'flashing' LED indicators, for generating audio tones, or for 'clocking' logic or counter/divider circuitry, etc. The generators themselves may produce either symmetrical or non-symmetrical waveforms, and may be of either the free-running or the 'gated' type.

Square wave generator circuits are quite easy to design, and may be based on a wide range of semiconductor technologies, including the humble bipolar transistor, the op-amp, the 555 timer chip or on CMOS logic elements, etc. In this month's edition we'll confine our discussion to designs based on the transistor, the op-amp and the 555; next edition we'll continue the subject by showing 22 different CMOS-based square wave generator circuits!

Transistor astables

One of the easiest and cheapest ways of generating repetitive square and rectangular waveforms is to use the basic, two-transistor astable multivibrator circuit shown in Figure 1. A major advantage of this rather old-fashioned transistor circuit is that it can quite happily operate from supply voltages as low as 1.5 volts or, with a slight modification, from supply voltages up to several tens of volts.

The Figure 1 circuit acts essentially as a self-oscillating regenerative switch, in which the on and off periods of the circuit are controlled by the C1-R1 and C2-R2 time constants. If these time constants are equal (C1 = C2 and R1 = R2), the circuit acts as a square wave generator and operates at a frequency of approximately

1/(1.4 C1 R1)

Thus the frequency can be decreased by raising the values of C1-C2 or R1-R2, or vice versa. The frequency can be made variable by using twin-gang variable resistors (in series with 10k limiting resistors) in place of R1 and R2.

Outputs can be taken from either collector of the Figure 1 circuit, and the two outputs are in antiphase. The operating frequency of the circuit is substantially independent of supply rail values in the range 1.5 to 9 volts. The upper supply voltage limit is set by the fact that, as the transistors switch regeneratively at the end of each half-cycle, the base-emitter junction of the transistor is reverse-biased by an amount roughly equal to the supply voltage. Consequently, if the supply voltage exceeds the reverse base-emitter breakdown voltage of the transistor (typically about 9 volts), the timing operation of the circuit will be upset. This snag can be overcome by using the circuit modification shown in Figure 2.

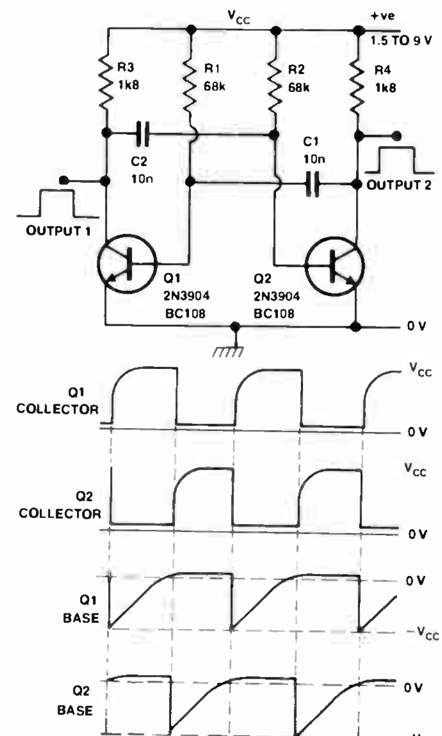


Figure 1. **Circuit and relevant waveforms of basic 1 kHz transistor astable multivibrator.**

Here, a 1N4148 diode is wired in series with the base input terminal of each transistor and effectively raises the reverse base-emitter breakdown voltage of each transistor to about 80 volts. The maximum supply voltage of the circuit is then limited only by the collector-emitter breakdown characteristics of the transistors, and may be several tens of volts. In practice, the 'protected' circuit of Figure 2 gives a frequency variation of only 2% when the supply voltage is varied from 6 V to 18 V.

The leading edges of the output waveforms of the Figure 1 and Figure 2 circuits are slightly rounded. The lower the values of R1 and R2 become relative to collector resistors R3 and R4, the worse this rounding becomes. Conversely, the larger the values of R1 and R2 relative to R3 and R4, the better the wave shape will be. The maximum permissible values of R1 and R2 are equal to the products of transistor current gain (say 90) and the R3 (or R4) values (1k8 in this case), so the maximum possible values of R1 and R2 are 162k in the Figure 1 and Figure 2 circuits.

The rounding of the leading edges of the basic astable circuit occurs because the collector voltage of each transistor is prevented from rising immediately to the positive rail voltage as the transistor turns off, because of loading by its cross-coupled timing capacitor. This deficiency can be overcome, and excellent square waves obtained, by effectively disconnecting the capacitor from the collector of its transistor as it turns off, as in the 1 kHz generator of Figure 3. Here, D1 and D2 are used to disconnect the timing capacitors at the moment of regenerative switching. The main time constants of the circuit are

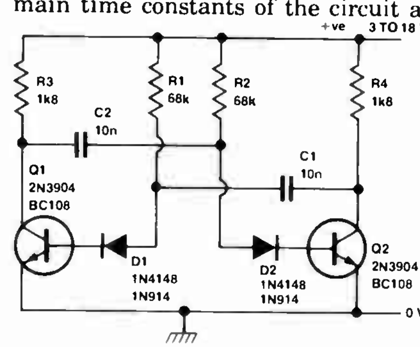


Figure 2. **This version of the 1 kHz astable has frequency correction applied via D1 and D2**

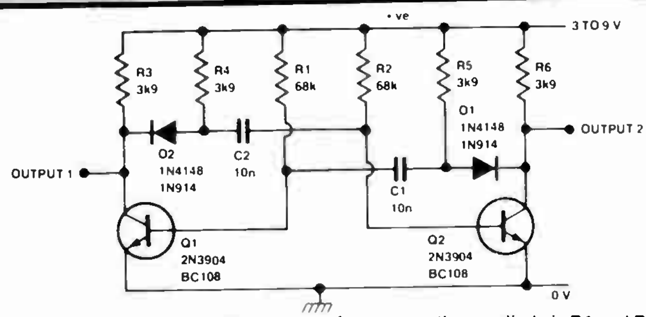


Figure 3. **This version of the 1 kHz astable has waveform correction applied via D1 and D2 and produces excellent square waves.**

again determined by C1-R1 and C2-R2. The effective collector loads of Q1 and Q2 are equal to the parallel resistances of R3-R4 and R5-R6 respectively.

Operation of the basic astable multivibrator relies on slight imbalances of the transistor characteristics, so that one transistor turns on slightly faster than the other when power is first applied. If the voltage to the circuit is applied by slowly increasing it from zero volts, both transistors may turn on simultaneously, in which case oscillation will not occur. This snag can be overcome by using the sure-start circuit of Figure 4, in which the timing resistors are connected to the transistor collectors in such a way that only one transistor can ever be turned on at a given moment.

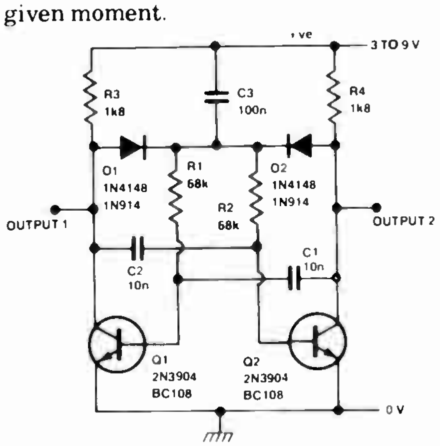


Figure 4. **The 1 kHz astable with 'sure-start' facility.**

The transistor astable circuits we have looked at so far are designed to give a symmetrical output waveform, with a 1:1 mark-to-space ratio. A non-symmetrical waveform can be obtained by simply making one set of astable time-constant components larger than the other. Figure 5a shows the connections for making a fixed-frequency (about 1100 Hz) variable mark-to-space ratio waveform generator, in which the ratio can be fully varied over the range 1:10 to 10:1.

The leading edges of the output waveforms of the above circuit may be objectionably rounded for some applications when the mark-to-space control is set to its extreme positions. Also, the circuit may be difficult to start if the supply voltage is applied to the circuit slowly. Both of these snags can be overcome by using the connections of Figure 5b, in which the circuit is fitted with sure-start and waveform-correction diodes.

Op-amp generators

Good square waves can be generated by using a fast op-amp, such as the LF351, in the basic relaxation oscillator configuration shown in Figure 6. This circuit requires the use of dual power supplies and, because of the slew-rate limitations of op-amps, its output waveform rise and fall times are not as good as those obtained from transistor, 555, or CMOS astables. The op-amp circuit has, however, some distinct advantages over these alternative types of square wave generator; specifically, it has excellent frequency stability and the waveform can be varied over a wide range by altering any *one* of its four passive component values.

The basic operation of the Figure 6 cirucit is fairly easy to follow. The output of the op-amp alternatively switches between the positive and negative supply rail values and thus applies a positive or negative 'reference' voltage to the non-inverting terminal of the op-amp, this reference voltage being a fixed fraction or ratio (determined by the R2-R3 ratios) of the supply voltage.

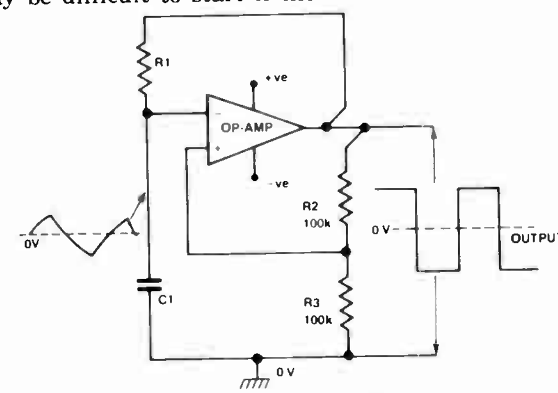


Figure 6. **Basic op-amp relaxation oscillator.**

Suppose initially that C1 is discharged and the op-amp output has just switched positive. In this case C1 will charge positively via R1 until its voltage reaches the positive reference value on the non-inverting terminal of the op- ▶

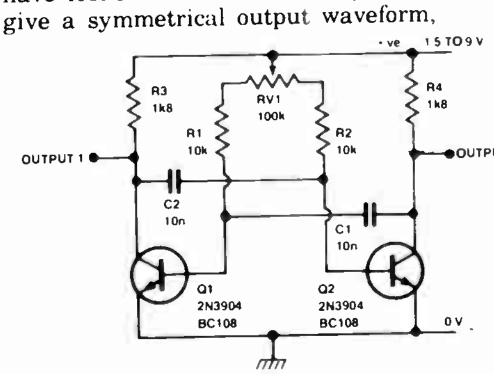


Figure 5a. **Basic variable M/S ratio astable operating at about 1100 Hz.**

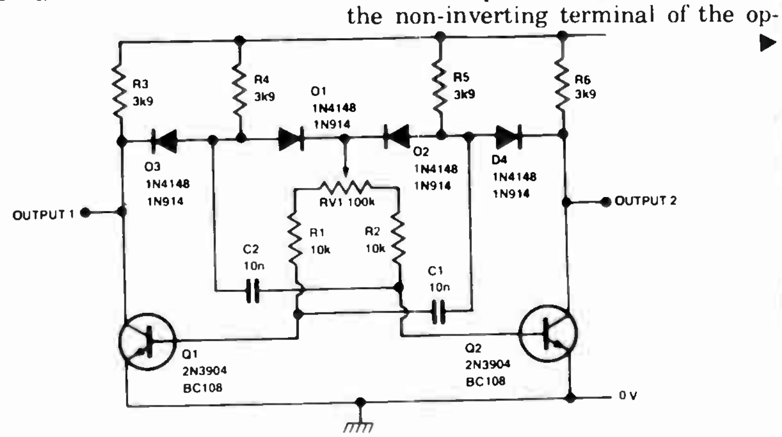


Figure 5b. **Improved version of variable M/S ratio astable with waveform correction and sure-start facility.**

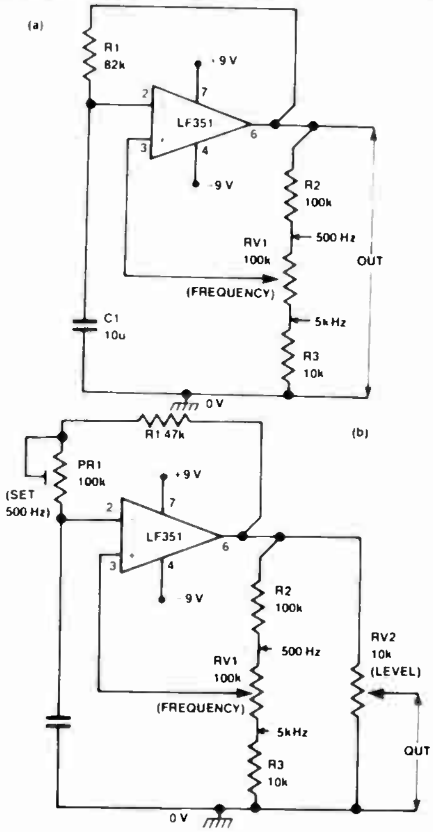


Figure 7. **(a) Simple 500 Hz to 5 kHz squarewave generator and (b) an improved version.**

amp, at which point the op-amp voltage (and thus the reference voltage) will start to fall and thus initiate a regenerative switching action in which the output switches abruptly to the negative rail voltage. C1 will then start to charge in a negative direction via R1 until its voltage reaches the new (negative) reference value on the non-inverting terminal, at which point the op-amp output will again switch regeneratively high and initiate a new action in which the whole sequence repeats itself.

The action of the op-amp circuit is such that a symmetrical square wave is developed at the output of the op-amp, and a non-linear triangle waveform is developed across C1; each waveform swings symmetrically about the zero volts line. Note that the operating frequency is virtually independent of the supply rail voltages, but can be varied by altering the R1 and C1 values, or by altering the R2-R3 ratios.

Figure 7a shows the practical circuit of a simple 500 Hz to 5 kHz op-amp square wave generator in which the frequency variation is obtained by altering the attenuation ratio of the R2-RV1-R3 potential divider, and Figure 7b shows how the circuit can be improved by using PR1 to preset the frequency range of the RV1 frequency control to a precise minimum value, and by using RV2 as an output amplitude control.

Figure 8 shows how the above circuit can be modified to make a general-purpose square wave generator that covers the range 2 Hz to 20 kHz in four switched decade ranges. Note that preset controls PR1 to PR4 are used to precisely set the minimum frequencies of the 2 Hz — 20 Hz, 20 Hz — 200 Hz, 200 Hz — 2 kHz, and 2 kHz — 20 kHz ranges respectively, without calling for the use of precision components.

Finally, Figure 9 shows how the basic relaxation oscillator circuit can be modified so that it provides both a variable frequency and a variable mark-to-space ratio output. The mark-to-space ratio is variable via RV1, and the circuit action is such that C1 alternately charges positively via R1-D1 and the left-hand side of RV1 and charges negatively via R1-D2 and the right-hand side of RV1. The mark-to-space ratio is variable over the range 11:1 to 1:11, and the frequency is variable over the approximate range 650 Hz to 6.5 kHz via RV2; varying the mark-to-space ratio setting causes only slight interaction with the frequency control.

Note that the Figure 6 to Figure 9 circuits can be used with virtually any types of op-amp, but that the maximum usable frequency and the quality of the output rise and fall times depend on the slew rate of the op-amp that is used; the LF351, for example, gives a performance about ten times better than the 741 in these respects. Also note that although we've shown the circuits as

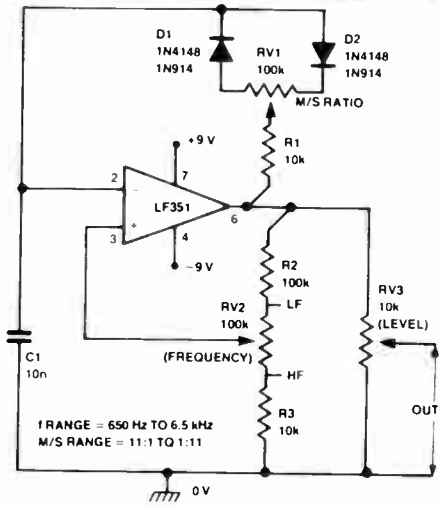


Figure 9. **Variable frequency, variable M/S ratio generator.**

being powered from 9 volt split supplies, they can in fact be powered from any split supplies in the range 5 to 18 V.

555 astables

The IC known as the '555 timer' makes an excellent square wave generator when used in the astable mode. The device is readily available, inexpensive, and is housed in an 8-pin dual-in-line (DIL) plastic package. It can be powered by any supply in the range 4.5 to 15 volts, has a low-impedance output that can source (supply) or sink (absorb) load currents up to 200 mA and, when used in the astable mode, generates output square waves with typical rise and fall times of about 100 ns. The 555 astable has excellent frequency stability, can span the frequency range from near zero

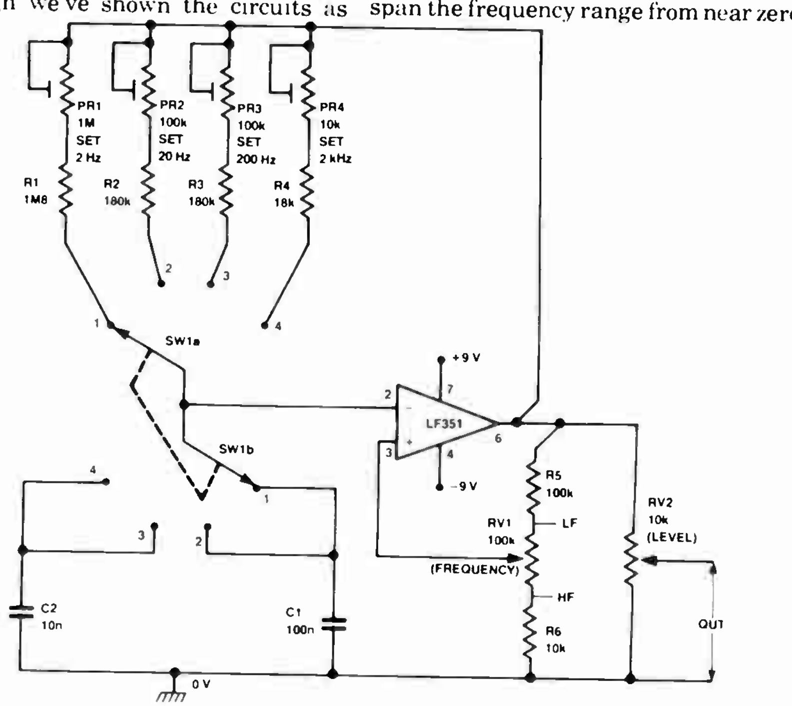
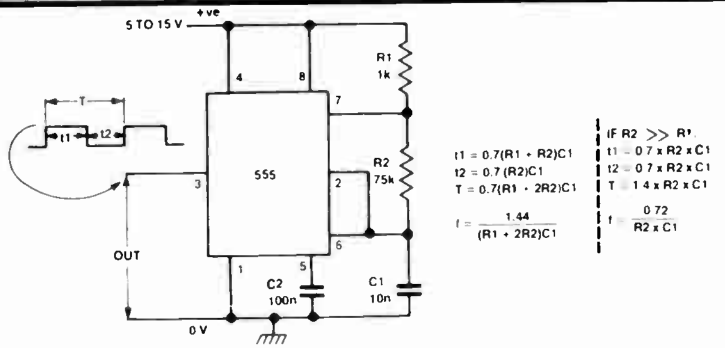


Figure 8. **Four-decade (2 Hz to 20 kHz) square wave generator. The presets enable the circuit to use a single calibrated frequency scale.**



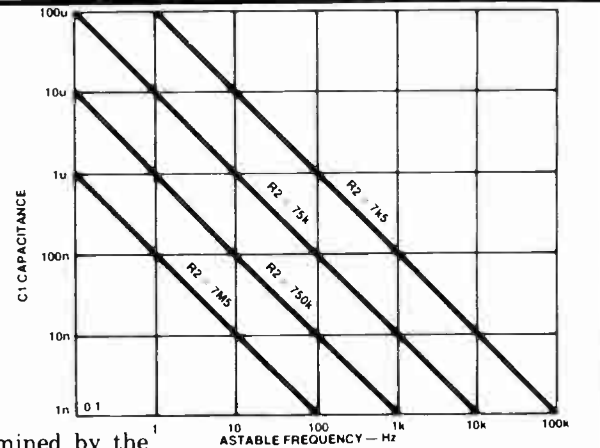


Figure 10. **(a) Basic circuit of a 1 kHz 555 astable with design formulae. (b) Approximate relationship between C1, R2 and f for the 555 astable when R2 is large relative to R1.**

to about 100 kHz, and its frequency and mark-to-space ratio can be accurately controlled with two external resistors and one capacitor.

Figure 10a shows the practical circuit of a basic 1 kHz 555 astable, together with the formulae that define the timing of the circuit. The circuit operation is such that C1 first charges exponentially via the series R1-R2 combination until eventually its voltage rises to two-thirds of the supply voltage, at which point a regenerative switching action takes place and C1 starts to discharge exponentially via R2 until eventually its voltage falls to one-third of the supply voltage. At this point a second regenerative switching action takes place and C1 starts to re-charge towards two-thirds of the supply voltage via R1-R2, and the whole sequence repeats. C2 is used in this circuit (and those that follow) to decouple the internal circuitry of the 555 chip from the effects of supply line transients.

Note that the operating frequency of the above circuit is virtually independent of the supply voltage value, and that both the mark-to-space ratio and the frequency are determined by the R1-R2-C1 values. Also note that if R2 is large relative to R1, the operating frequency is determined mainly by the R2 and C1 values and that an almost symmetrical output waveform is generated. The graph of Figure 10b shows the approximate relationship between frequency and the C1-R2 values under the above condition. In practice, the R1 and R2 values can be varied from about 1k to 10M.

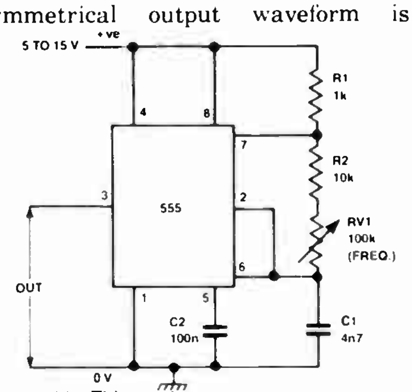


Figure 11. **This variable frequency generator covers 1.4 kHz to 15 kHz.**

The basic Figure 10a circuit can be modified in a number of ways. Figure 11, for example, shows how it can be made into a variable frequency square wave generator by replacing R2 with a fixed and a variable resistor in series. With the component values shown, the frequency can be varied over the approximate range 1.4 kHz to 15 kHz via RV1.

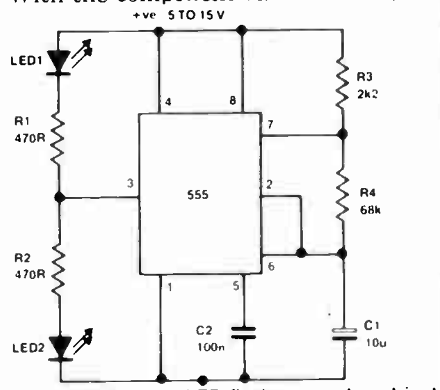
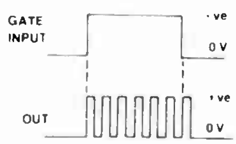


Figure 12. **This two-LED flasher operates at just under 1 Hz. The LEDs flash alternately.**

Figure 12 shows how the circuit can be used as a two-LED 'flasher' unit, in which one LED turns off as the other turns on, and vice versa. The circuit▶

circuit file



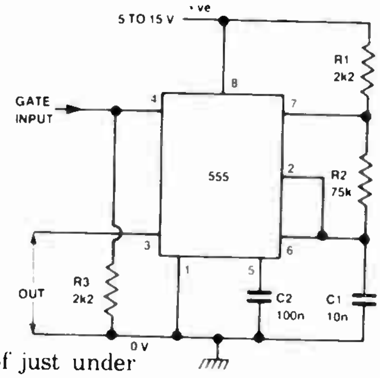


Figure 15. **Gated astable with gate signal applied to the pin 4 RESET terminal of the IC.**

operates at a frequency of just under 1 Hz.

Figure 13 shows how the circuit can be modified so that its mark and space periods are independently variable over the approximate range 15 us to 1.5 ms.

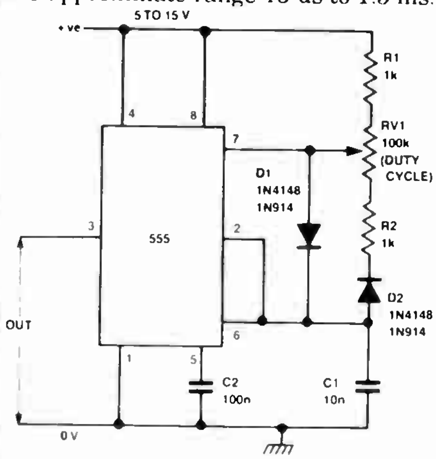


Figure 13. **Astable with mark and space periods independently variable over about 15 us to 1.5 ms.**

Here, timing capacitor C1 alternately charges via R1-RV1-D1 and discharges via RV2-R2-D2.

Figure 14 shows how the circuit can be modified so that it acts as a fixed-frequency square-wave generator with a mark-to-space ratio or duty cycle that is fully variable from 1% to 99% via

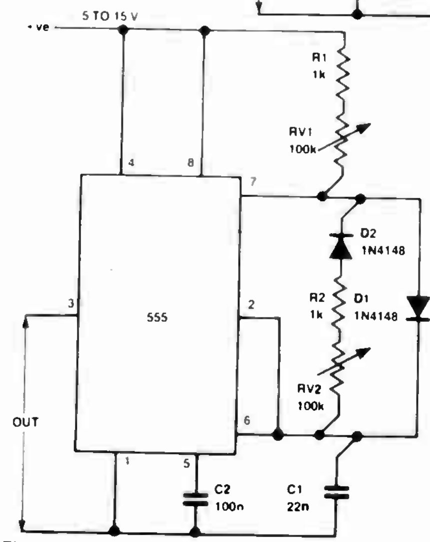


Figure 14. **555 astable with duty cycle variable from 1% to 99%. Frequency is almost constant at about 1 kHz.**

RV1. Here, C1 alternately charges via R1 and the top half of RV1 and D1, and discharges via D2-R2 and the lower half of RV1. Note that the sum of these two timing periods is virtually constant, so the operating frequency is almost independent of the setting of RV1.

The 555 astable circuit can be gated on and off (enabled or disabled) either

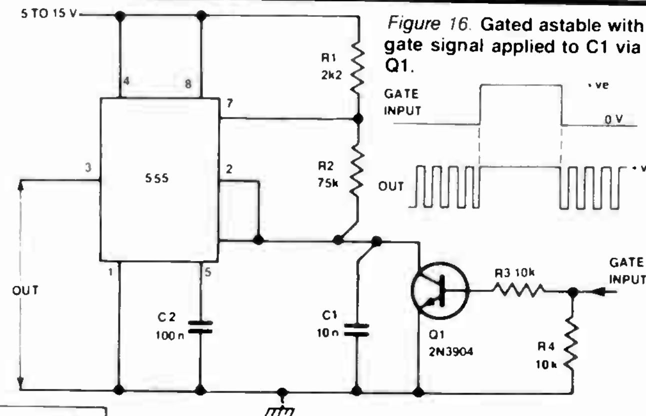


Figure 16. **Gated astable with gate signal applied to C1 via Q1.**

by applying a gate signal to pin 4 or by disabling or enabling the main timing capacitor via a transistor switch.

Figure 15 shows how the circuit can be gated via the pin 4 (reset) terminal. The characteristic of this terminal is such that if the terminal is biased above a nominal 0.7 volts, the astable is enabled, but if it is biased below 0.7 volts by a current greater than 100 uA (by taking pin 4 to ground via a resistance less than 7k, for example) the astable is disabled and its output is grounded. Thus in the Figure 15 circuit the astable can be turned on by applying a high or logic 1 signal to pin 4, or off by applying a zero or logic 0 signal to pin 4.

Finally, to complete this month's look at square wave generator circuits, Figure 16 shows how the 555 astable can be gated on and off via a transistor wired across the main timing capacitor, C1. Here, with zero gate drive applied, Q1 is cut off and the astable is free to operate in the normal way, but when a high gate signal is applied, Q1 is driven on and discharges C1, thus disabling the astable. Note that the output of this circuit is driven high when the astable is disabled in this way. ●

More clock generators

In the last article, Ray covered clock or square wave generators using transistors, op-amps and 555s. This time he covers the use of CMOS gates and the 4046B VCO chip.

Ray Marston

INEXPENSIVE CMOS logic ICs such as the 4001B and the 4011B can easily be used to make very inexpensive but highly versatile square-wave or 'clock' generator circuits. They can be designed to give symmetical or non-symmetrical outputs, and can be of the free-running or the gated types; in the latter case, they can be designed to turn on with either logic 0 or logic 1 gate signals, and to give either a logic 0 or a logic 1 output when in the 'off' mode. You can even use these 'cheapo' circuits as simple voltage-controlled oscillators (VCOs) or as frequency-modulated oscillators.

If you want really good VCO operation from a square-wave generator, with excellent linearity and versatility, you can turn to the slightly more expensive 4046B CMOS IC. We'll look at some applications of this chip later, but let's start by looking at some basic two-gate CMOS square-wave generator or astable circuits.

Basic two-gate astable circuits

The simplest way to make a CMOS astable circuit is to wire two CMOS inverter stages in series and use the C-R feedback network shown in Figure 1a. This circuit generates a decent square wave output and operates at about 1 kHz with the component values shown. The frequency is inversely proportional to the C-R time constant, so can be raised by lowering the values of either C1 or R1. C1 must be a non-polarised capacitor and can have any value from a few tens of pF to several uF, and R1 can have any value from about 4k7 to 22M; the operating frequency can vary from a frequency of 1 Hz to about 1 Mhz. For variable frequency operation, wire a fixed and a variable resistor in series in the R1 position.

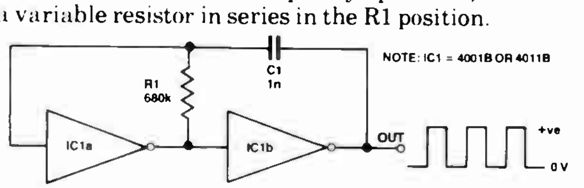


Figure 1(a). **Circuit of the basic two-gate CMOS astable. This operates at 1 kHz with the component values shown.**

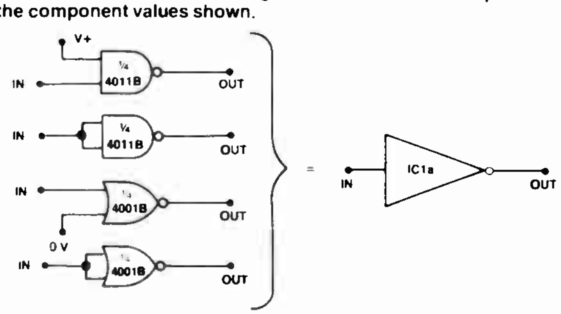


Figure 1(b). **Ways of connecting a two-input NAND (4011B) or NOR (4001B) gate for use as an inverter.**

Note at this point that each of the 'inverter' stages of the Figure 1a circuit can be made from a single gate of a 4001B quad two-input NOR gate or a 4011B quad two-input NAND gate by using the connections shown in Figure 1b. Thus each of these ICs can provide two astable circuits. Also note that the inputs to all unused gates in these ICs must be tied to one or other of the supply-line terminals; the Figure 1a astable (and all other astables shown in this feature) can be used with any supplies in the range 3 to 18 V; the 'zero volts' terminal goes to pin 7 of the 4001B or 4011B, and the '+ve' terminal goes to pin 14.

The output of the Figure 1b astable circuit switches (when lightly loaded) almost fully between the zero and positive supply rail values, but the C1-R1 junction is prevented from swinging below zero or above the positive rail levels by built-in clamping diodes at the input of IC1a. This characteristic causes the operating frequency of the circuit to be somewhat dependent on supply rail voltage. Typically, the frequency falls by about 0.8% for a 10% rise in supply voltage; if the frequency is normalised with a 10 volt supply, the frequency falls by 4% at 15 V or rises by 8% at 5 V.

Also, the operating frequency of the Figure 1a circuit is influenced by the 'transfer voltage' value of the individual IC1a gate that is used in the astable, and can be expected to vary by as much as 10% between individual ICs. The output symmetry of the waveform also depends on the 'transfer voltage' value of the IC and, in most cases, the circuit will give a non-symmetrical output. In most 'hobby' or other non-precision applications, these defects of the basic astable circuit are of little practical importance.

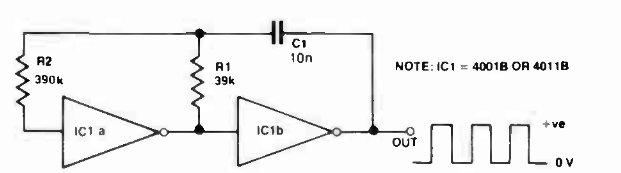


Figure 2. **This 'compensated' version of the 1 kHz astable has excellent frequency stability with variations in supply voltage.**

Some of the defects of the Figure 1a circuit can be minimised by using the 'compensated' astable of Figure 2, in which R2 is wired in series with the input of IC1a. This resistor must have a value that is large relative to R1, and its main purpose is to allow the C1-R1 junction to swing freely below the zero and above the positive supply rail voltages during circuit operation and thus improve the frequency stability of the circuit. Typically, when R2 is ten times the value of R1, the frequency varies by only 0.5% when the supply voltage is varied between 5 and 15 volts. An incidental benefit of R2 is that it gives a slight improvement in the symmetry of the output of the astable.

The basic and compensated astable circuits of Figures 1 and 2 can be built with a good number of detail variations, as shown in Figures 3 to 6. In the basic astable circuit, for example, C1 alternately charges and discharges via R1 and thus has a fixed symmetry. Figures 3 to 5 show how the basic circuit can be modified to give alternate C1 charge and discharge paths to thus allow the symmetry to be varied at will.

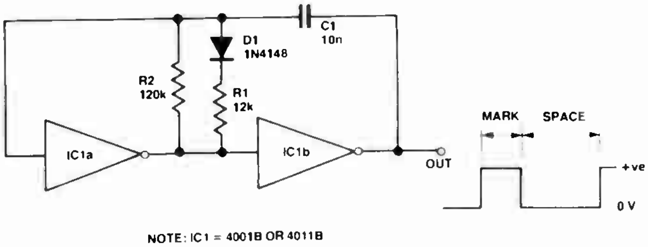


Figure 3. **Modifying the astable to give a non-symmetrical output: MARK is controlled by the parallel values of R1 and R2; SPACE is controlled by R2 only.**

The Figure 3 circuit is useful if you need a highly non-symmetrical waveform, equivalent to a fixed pluse delivered at a fixed 'timebase' rate. Here, C1 charges in one direction via R2 in parallel with the D1-R1 combination, to generate the mark or pulse part of the waveform, but discharges in the reverse direction via R2 only, to give the space between the pulses.

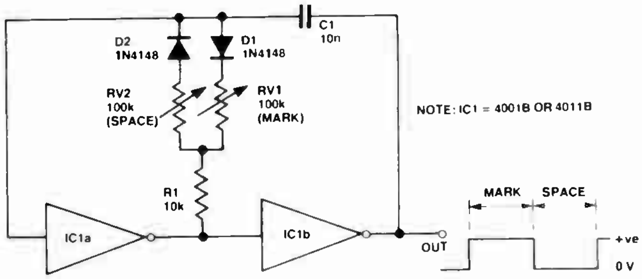


Figure 4. **This astable has independently variable MARK and SPACE times.**

Figure 4 shows the modifications for generating a waveform with independently variable mark and space times; the mark time is controlled by R1-RV1-D1, and the space time is controlled by R1-RV2-D2.

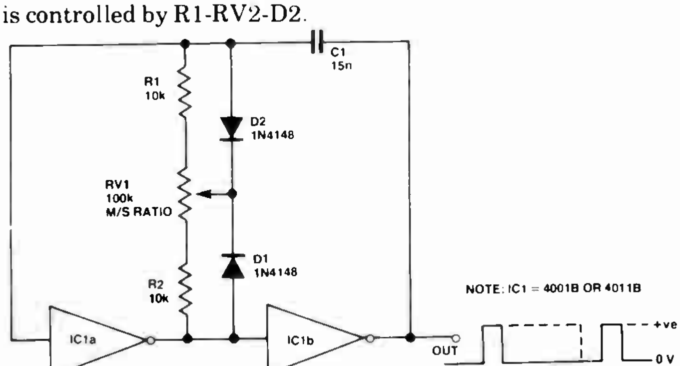


Figure 5. **The mark/space ratio of this astable is fully variable from 1:11 to 11:1 via RV1; frequency is almost constant at about 1 kHz.**

Figure 5 shows the modifications to give a variable symmetry or mark/space ratio output while maintaining a near-constant frequency. Here, C1 charges in one direction via D2 and the lower half of RV1 and R2, and in the other direction via D1 and the upper half of RV1 and R1. The M/S ratio can be varied over the range 1:11 to 11:1 via RV1.

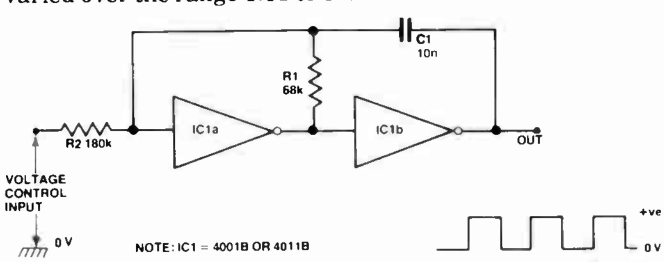


Figure 6. **Simple voltage-controlled oscillator (VCO) circuit.**

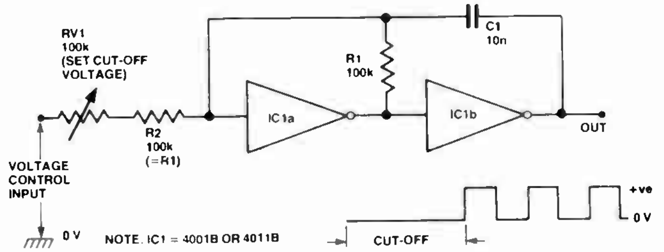


Figure 7. **Special effects VCO which cuts off when V_{in} falls below a preset value.**

Finally, Figures 6 and 7 show a couple of ways of using the basic astable circuit as a very simple VCO. The Figure 6 circuit can be used to vary the operating frequency over a limited range via an external voltage. R2 must be at least twice as large as R1 for satisfactory operation, the actual value depending on the required frequency shift range; a 'low' R2 value gives a large frequency shift range, and a 'large' R2 value gives a small frequency shift range. The Figure 7 circuit acts as a special-effects VCO in which the oscillator frequency rises with input voltage, but switches off completely when the input voltage falls below a value preset by RV1.

Gated astable circuits

All of the astable circuits of Figures 1 to 5 can be modified for gated operation, so that they can be turned on and off via an external signal, by simply using a two-input NAND (4011B) or NOR (4001B) gate in place of the inverter in the IC1a position, and by applying the input gate control signal to one of the gate input terminals. Note, however, that the 4001B and the 4011B give quite different types of gate control and output operation in these applications, as shown by the two basic versions of the gated astable in Figures 8 and 9.

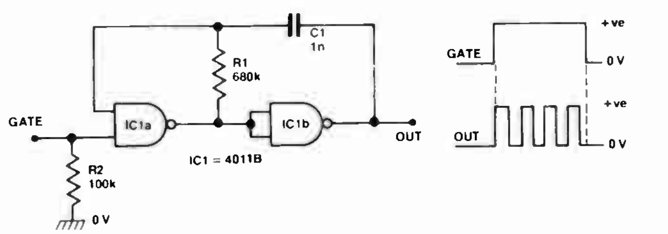


Figure 8. **This gated astable has a normally low output and is gated on by a high (logic 1) at the input.**

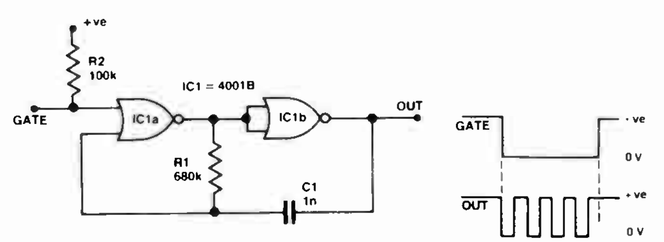


Figure 9. **This version of the gated astable has a normally high output and is gated on by a low (logic 0) at the input.**

Note specifically from these two circuits that the NAND version is gated on by a logic 1 input and has a normally low output, while the NOR version is gated on by a logic 0 input and has a normally high ouput. R2 can be eliminated from these circuits if the gate drive is direct-coupled from the ouput of a preceding CMOS logic stage, etc.

Note in the basic gated astable circuits of Figures 8 and 9 that the output signal terminates as soon as the gate drive signal is removed; consequently, any noise present at the gate terminal also appears at the outputs of these circuits. Fig- ▶

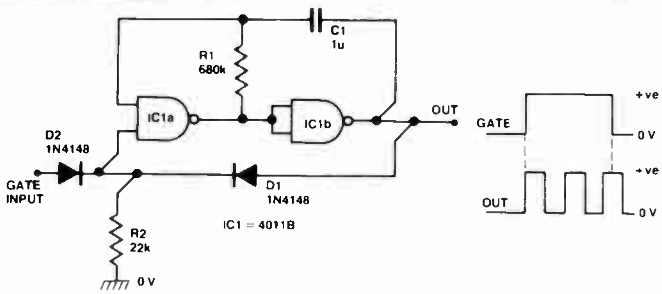


Figure 10. Semi-latching or 'noiseless' gated astable circuit, with logic 1 gate input and normally zero output.

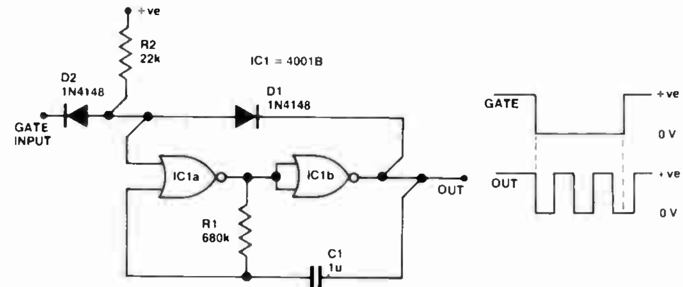


Figure 11. Alternative semi-latching gated astable, with logic 0 gate and normally high output.

ures 10 and 11 show how to modify the circuits to overcome this defect. Here, the gate signal of IC1a is derived from both the outside world and from the output of IC1b via diode OR gate D1-D2-R2. As soon as the circuit is gated from the outside world via D2 the output of IC1b reinforces or self-latches the gating via D1 for the duration of one half astable cycle, thus eliminating any effects of a noisy outside world gate signal. The outputs of the 'semi-latching' gated astable circuits are thus always complete numbers of half cycles.

'Ring of three' clock-generator circuits

The two-gate astable circuit is not generally suitable for direct use as a 'clock' generator with fast-acting counting and dividing circuits, since it tends to pick up and amplify any supply line noise during the 'transitioning' parts of its operating cycle and thus to produce square waves with 'glitchy' leading and trailing edges. A far better type of clock generator circuit is the 'ring of three' astable shown in Figure 12.

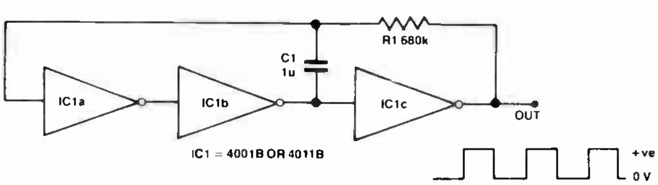


Figure 12. This 'ring-of-three' astable makes an excellent clock generator.

The Figure 12 'ring of three' circuit is similar to the basic two-gate astable, except that its 'input' stage (IC1a-IC1b) acts as an ultra-high gain non-inverting amplifier and its main timing components (C1-R1) are transposed (relative to the two-gate astable). Because of the very high overall gain of the circuit, it produces an excellent and glitch-free square wave output, ideal for clock-generator use.

The basic ring-of-three astable can be subjected to all the design modifications we've already looked at for the basic two-gate astable; e.g: it can be used in either basic or compensated form and can give either a symmetrical or non-symmetrical output, etc. The most interesting variations of the circuit occur, however, when it is used in the 'gated' mode, since it can be gated via either the IC1b or IC1c stages. Figures 13 to 16 show four variations on this 'gating' theme.

Thus the Figures 13 and 14 circuits are both gated on by a logic 1 input signal, but the Figure 13 circuit has a normally low output, while that of Figure 14 is normally high. Similarly, the Figures 15 and 16 circuits are both gated on by a logic 0 signal, but the output of the Figure 15 circuit is normally low, while that of Figure 16 is normally high.

4046B VCO circuits

To close this look at CMOS square wave generator circuits, let's look at some practical VCO applications of the 4046B phase-locked loop (PLL) IC. Figure 17 shows the internal block diagram and pinouts of this chip, which contains a couple of phase comparators, a VCO, a zener diode and a few other bits and pieces.

For our present purpose, the most important part of the chip is the VCO section. This VCO is a highly versatile device; it produces a well-shaped symmetrical square wave output, has a top-end frequency limit in excess of 1 MHz, has a voltage-to-frequency linearity of about 1% and can easily be 'scanned' through a 1 000 000:1 range by an external voltage applied to the VCO input terminal. The frequency of the oscillator is governed by the value of a capacitor (minimum value 50p) connected between pins 6 and 7, by the value of a resistor (minimum value 10k) wired between pin 11 and ground, and by the voltage (any value from zero to the supply voltage in use) applied to VCO-input pin 9.

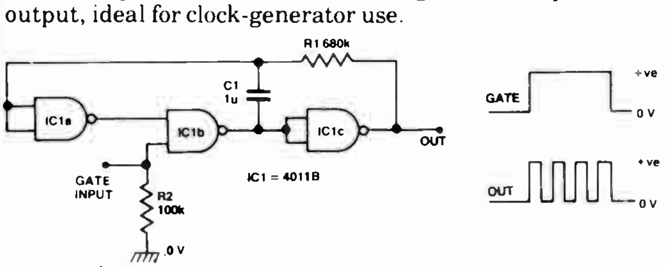


Figure 13. This 'ring-of-three' astable is gated by a logic 1 input and has a normally low output.

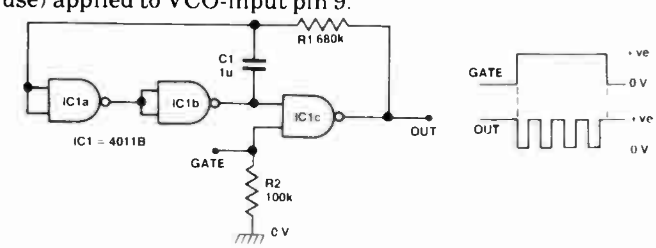


Figure 14. This gated 'ring-of-three' astable is gated by a logic 1 input and has a normally high output.

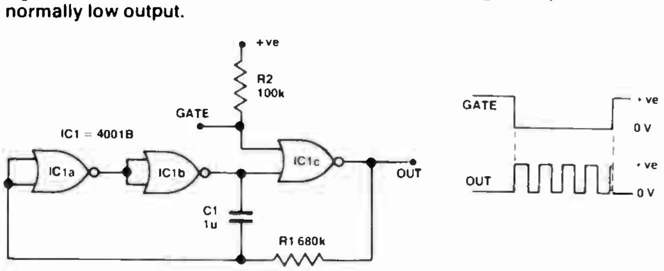


Figure 15. Ring-of-three gated by a logic 0 input and having a normally low output.

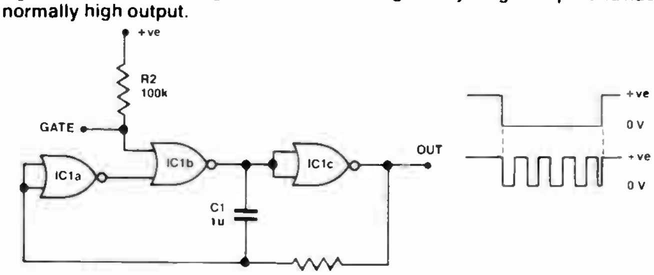


Figure 16. Ring-of-three with normally high output and logic 0 gating.

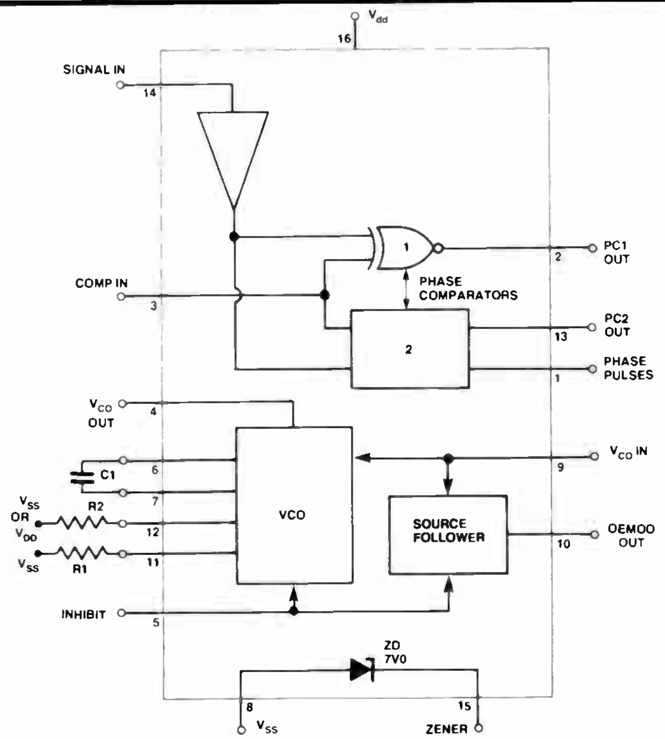


Figure 17. **Internal block diagram and pinouts of the 4046B.**

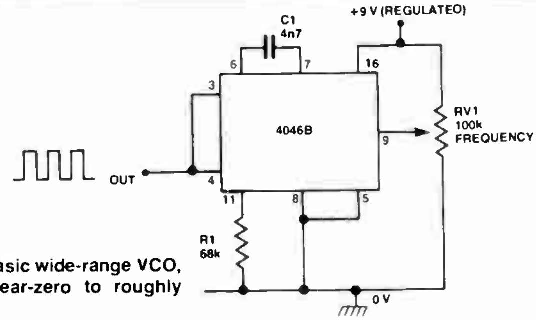


Figure 18. **Basic wide-range VCO, spanning near-zero to roughly 5 kHz.**

Figure 18 shows the simplest possible way of using the 4046B VCO as a voltage-controlled square wave generator. Here, C1-R1 determine the maximum frequency that can be obtained (with the pin 9 voltage at maximum) and RV1 controls the actual frequency by applying a control voltage to pin 9. The frequency falls to a very low value (a fraction of a Hz) with pin 9 at zero volts. The effective voltage-control range of pin 9 varies from roughly 1 V below the supply value to about 1 V above zero, and gives a frequency span of about 1 000 000:1. Ideally, the supply voltage to the circuit should be regulated.

We've said above that the frequency of the Figure 18 circuit falls to near-zero when the input voltage is reduced to zero. Figure 19 shows how the circuit can be modified so that the frequency falls all the way to zero with zero input, by wiring a high-value resistor (R2) between pins 12 and 16. Note here that when the frequency is reduced to zero, the VCO output randomly settles in either a logic 0 or a logic 1 state.

Figure 20 shows how the pin 12 resistor can alternatively be used to determine the minimum operating frequency of a restricted-range VCO. Here, f_{min} is determined by C1-R2 and f_{max} is determined by C1 and the parallel resistance of R1 and R2.

Figure 21 shows an alternative version of the restricted-range VCO, in which f_{max} is controlled by C1-R1 and f_{min} is determined by C1 and the series combination of R1 and R2. Note that by suitable choice of the R1 and R2 values, the circuit can be made to 'span' any desired frequency range from 1:1 to near-infinity.

Finally, it should be noted that the VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic 1 level) or enabled by taking pin 5 low. This feature makes it possible to gate the VCO on and off by external signals. Thus Figure 22 shows how the basic VCO circuit can be gated via a signal applied to an external inverter stage. Alternatively, Figure 23 shows how one of the internal phase comparators of the 4046B can be used to provide gate inversion, so that the VCO can be gated via an external voltage applied to pin 3. ●

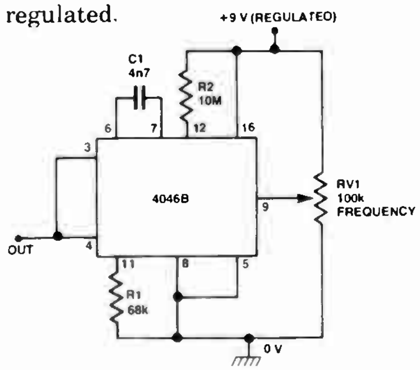


Figure 19. **Modification of the Figure 18 circuit takes it all the way down to zero.**

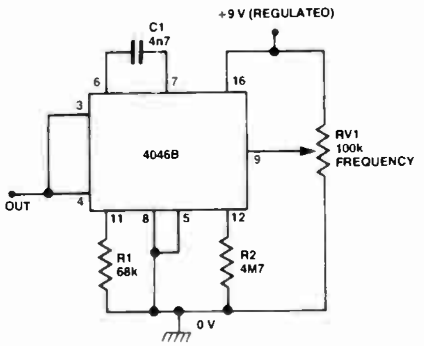


Figure 20. **Restricted-range VCO, with frequency variable from roughly 72 Hz to 5 kHz via RV1.**

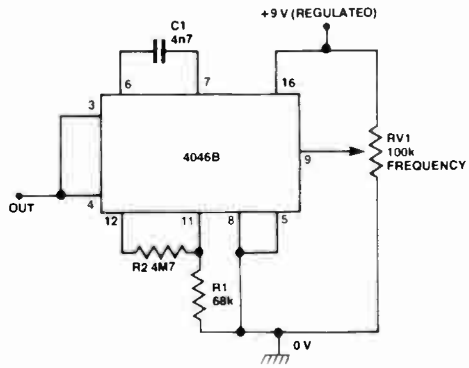


Figure 21. **Alternative version of the restricted-range VCO. Maximum frequency is controlled by C1-R1, minimum by C1-(R1+R2).**

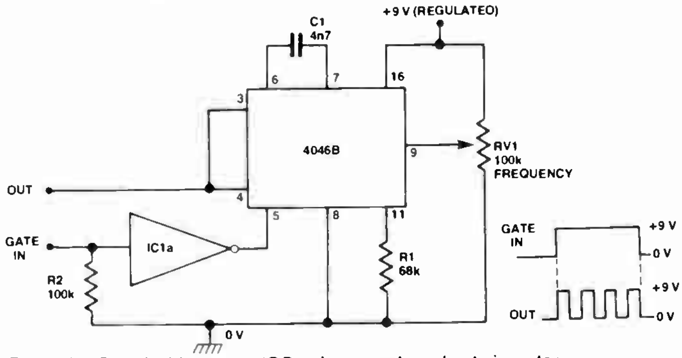


Figure 22. **Gated wide-range VCO using an external gate inverter.**

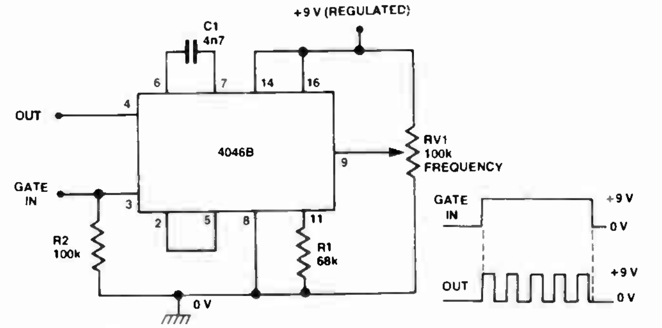


Figure 23. **Gated wide-range VCO using one of the internal phase comparators as a gate inverter.**

Beating the RS232 blues

A serial interface should be the simplest way to connect two pieces of computer gear together. Unfortunately, RS232 complicates matters.

Graham Wideman

ONLY TWO pieces of wire are needed to allow one computer device to talk to another, and three if you want a two-way conversation. So you would think that hooking together computer equipment with serial interfaces would be easy — provided, of course, that the various equipment manufacturers had adopted a standard for their interfaces. And herein lies a problem.

The 'standard' which was adopted for serial interface was one known as 'RS232'. RS232 is a standard of the American Electronics Industries Association, and was originally intended for the interface between 'Data Terminal Equipment' (DTE — in other words a computer 'dumb' terminal) and 'Data Communications Equipment' (DCE — equipment which facilitates communication to a remote computer, like a modem).

The standard specifies the electrical characteristics of the interface signals, along with the shape and pin assignments of the connectors to be used. In addition there are certain other conventions which go along with this standard, like the commonly used data rates and formats.

Now, although it's possible to borrow the electrical and timing conventions from this standard, many aspects are ambiguous. As mentioned above, RS232 specifies two different 'sexes' of equipment, terminal equipment and communications equipment, each with their own sex of connector, and their own connector pin assignments. But the standard is now being applied also to computers, printers, plotters, digitising tablets, speech synthesisers and so on, which don't fall conveniently into the category of either sex. Consequently any particular piece of equipment has a more or less arbitrary sex assignment.

Furthermore, RS232 contains specifications for using its connectors and signals for a large number of different applications. Since today's equipment needs only the simplest of such arrangements, most of RS232's features are not used, and in fact merely add to the confusion as manufacturers arbitrarily select the few features they need for their interface.

OK, the fact that the interface is somewhat arbitrary on any particular piece of equipment would be compensated if the equipment manual told you how it worked. Not the case. In fact the description of how the RS232 interface works is *almost universally the worst described part of the manual*, ranging from extremely ambiguous to downright wrong.

This month I am going to describe the theory of how RS232 is supposed to work. In a following issue I will describe a test unit which will patch any two devices together, and monitor what they are saying. You may wish to build one, or borrow the principles to understand how to test an interface by some alternative method.

The basics of a serial interface

There are many possible ways to make a serial communications 'channel'; RS232 is just one method. Let us examine serial interfaces in general, and see how RS232 implements the various features involved.

I should point out here that many of these features are not strictly a part of RS232, but are conventions which are used with it. The best way to declare something as a 'convention' is by referring to data on the ICs used to implement RS232 serial interfaces, namely the 'UART' which formats the data (such as the National 5303 and similar), and the 'line driver' and 'receiver' which actually send and receive the electrical signals on the serial cable (National LM1488 and 1489 respectively).

Suppose we are dealing with the simplest type of interface, one in which there is a 'sender' and a 'receiver', such as may be the case where a computer sends data to a line printer. Two wires connect the two devices, one wire being 'Ground' or zero volts, the other wire carrying the data.

Ones and zeros

The first task is to decide how to represent the binary 'one' and 'zero' as voltages. A TTL logic IC regards a voltage less than 0.4 V as a logic zero, and a voltage greater than 2.8 V as a logic one. A TTL output is not, for various reasons, suited to sending data down a long wire, so RS232 does things differently. A 'zero' is represented by a 'high' voltage between +3 V and +12 V (for some reason also called 'space'), while a 'one' is represented by a 'low' voltage between −3 V and −12 V (also called 'mark'). The range between −3 V and +3 V is undefined.

Next we must decide in what order and with what timing the bits are to be sent down the wire. RS232 calls the unit of data transmission a 'character', even though the data sent may not actually represent a character. A particular device may be set to transmit or receive 5, 6, 7 or 8-bit characters, with seven being the most common (because seven bits will represent the entire ASCII set of 128 characters), and eight the next most popular. These characters are sent *least significant bit first.* Using the scheme as I have so far described it, the letter 'B', which is ASCII 42 hexadecimal, or 66 decimal, would appear on the line as (see also Figure 1):

High low high high high high low
(7-bit code)

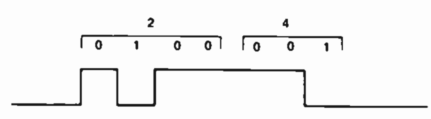


Figure 1. **The letter 'B' (hex 42) represented as a sequence of voltage levels, as used by RS232 devices.**

How does the receiver know when a particular character starts? We could use a third wire to signal that a character is starting on the second wire. This is a form of 'synchronous' communication, and is not used with any personal computer equipment. Instead RS232 has a way of telling the receiver that a character is starting. It works as follows.

Start bit

Suppose the receiver receives the above letter 'B'. Normally the communications line sits at 'mark' or low. Along comes bit one, which is a high, and immediately the receiver knows a character is coming in. Now, assuming that the receiver and sender are set so that they agree as to how long each bit is, the receiver will be able to recognise a high, then a low, then another low and so on, until the whole 'B' has been received.

However, suppose that instead the letter 'A' was sent, which is 41 hex, and therefore is represented (also see Figure 2) as:

Low high high high high high low

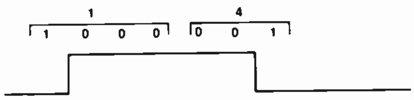


Figure 2. **The letter 'A' (hex 41) represented in RS232 voltage levels.**

This time, by the time the receiver finds out something is happening, it's already on the second bit! And what if you had a character composed entirely of lows?

The way around this problem is to prefix every character with a 'start' bit, which is invariably high.

Stop bit

This still leaves one problem. Suppose we send several hundred characters in a row. It would be unreasonable to expect that the sender and receiver agree as to the time-per-bit to such great accuracy that they would still be in step after so many bits. To overcome this each character is suffixed with one or two (according to how the devices are set) 'stop' bits, which are always low. After each character we always have a low-to-high transition which can be relied upon to keep the two devices in step.

Notice that there is nothing particularly special about the start and stop bits. They look like any other bits, except that there is always a low-to-high transition at least once per character, and it's between these two bits. I point this out because it means, for example, that if you are sending serial data to a printer, if the signal is momentarily disconnected (transmission continuing but reception interrupted) then upon reconnection the printer will probably not be able to interpret the incoming stream of highs and lows. The printer will be confused until the next pause in transmission, unless the combination of received characters enables the printer to determine where the stop-start location is.

Transmission speed: 'Baud Rate'

Naturally, both sender and receiver must be set to the same nominal communications speed. This speed is measured in bits-per-second, a unit also known as the baud. (One bit per second is one baud.) Commonly used rates are: 110 and 133 (for Selectric terminals, for example), 300 baud (modems communicating via telephone), 600, 1200, 2400, 4800 and 9600 baud. Some devices also communicate at 19 200, 38 400 and even 76 800 baud, but such are rare.

Parity

An embellishment which is occasionally seen is the use of 'parity' as an error checking method. In a seven-bit code, for example, an extra bit may be added after the last bit (but before the stop bit). The sender counts the number of 'one' bits in the character, and if the answer is even it sets the parity bit to 'one', if not it is made 'zero'. (This is the even parity convention. There's an equally little-used odd parity convention which makes the parity bit 'one' for an odd total.)

When the receiver gets the character it does the same arithmetic and compares its answers to the parity bit received with the character. If it has the same answer it knows all is well; if the answer is wrong an error has occurred somewhere. For example, suppose an 'A' is transmitted (seven-bit, even parity). This would be represented as in Figure 3.

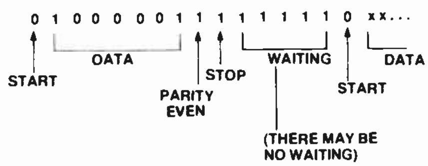


Figure 3. **Representation of the letter 'A' in seven-bit even parity code. Note that a '1' is a low voltage and a '0' is a high. The line normally sits at low or '1'.**

Now if one of those bits were accidentally changed somewhere along the way, there would be either one or three '1's, which is an odd number and does not agree with the parity bit. (And of course if the parity bit was accidentally changed, it wouldn't agree properly either.) You can probably see that this scheme cannot show where the error occurred or how to fix it, nor does it signal double errors. It is basically a low-overhead warning device.

In fact parity is generally ignored, since most personal computer equipment is not operated in electrically noisy environments where such errors are likely to occur, and in any case such equipment has no convention for requesting that the sender resend the faultily received data. (Often the receiving device may be set to expect the parity bit but not use it.) However, I have included this description so that you know what parity is when the equipment has a switch to select or deselect its use.

Lots of options!

As you can see, even thus far there are plenty of options to choose from. In a typical device many of these options may be switch selectable, usually miniature DIP switches inside the box, or perhaps soldered jumpers. In some cases, such as terminals and computers, some of these features may be programmed from the keyboard or from software.

So there are plenty of ways in which your two little darlings won't be able to talk to each other! But wait, there's much more!

How many duplexes?

Although not strictly of direct concern in the RS232 interface, some equipment, particularly terminals and modems, provide a 'Full/Half Duplex' switch.

'Full Duplex' means that when the terminal transmits a character to the remote computer the computer immediately echoes the character back to the terminal, whereupon it appears on the terminal's screen (or paper, if a teletype). If there is no echo then the character you typed will not appear on the terminal's screen. This is a kind of insurance method to let you know that the computer is listening.

In 'Half Duplex' set-ups it is assumed that the computer will not echo the characters from the terminal, and thus the terminal puts the typed characters on the screen whether or not the computer is awake.

The surprise comes if you have your terminal (or modem) set to Half Duplex, *and* the computer you are talking to echoes the characters. Then if you type 'FRED' you'll see 'FFRREEDD'.

Not so fast!

A commonly needed feature is the ability to tell the sending device to slow down. I don't mean to send at a lower baud rate, but rather to pause for a moment. A typical situation where this occurs is in slow printers. When the carriage reaches the end of the line the printer must tell the sender to wait until the carriage returns before sending more characters.

Such a signalling system is known as 'handshaking'. Typically this is implemented by adding an extra wire to the interface cable. The receiver maintains this wire at a 'high' signal level while it's OK for the sender to send, pulling it 'low' to tell the sender to halt the flow of data. Sometimes an interface will have handshaking lines both ways, so that either device can halt the other.

A complete two-way interface would consist of two data wires, two handshaking wires and ground — a total of five ▶

wires. Most RS232 hook-up problems occur because one piece of equipment needs some of these signals which the other does not provide, or because the wires in each piece of equipment are not connected to the corresponding pins in the interfacing connectors.

Not so fast type two

A quick note here that on some intelligent printers handshaking is carried out using a method called 'X-on, X-off'. Instead of a separate handshaking wire, the printer has a data output wire (normally printers only receive data). If the printer wishes to halt the sender the printer sends a control character to the sender (usually control-S, hex 13, which is also known as 'Direct Control 3'). Subsequently sending the same character will restart the data. Note that this is the same character which you use in CP/M (and Apple) to stop and start a continuous display to the screen from the keyboard.

Handshaking and buffers, etc

How necessary is handshaking in practice? A major sore point in the small computer industry has been the need for handshaking in printers. The Epson MX-80, for example, was available at one time with a serial interface known as 8141. This interface could only remember a maximum of two characters as they arrived from the computer. Since the 'line-feed' time exceeds the time of two characters, even at the slowest baud rates it was necessary for the interface to signal a halt after each line. The Exidy Sorcerer and the standard Apple printer interface board do not have any handshaking inputs, and consequently it would be impossible to make this combination of equipment work serially. (This particular problem rarely comes up since the MX-80 has a parallel input which is usually used. The Sorcerer has a parallel output, and the Apple has available for it a parallel printer board. I am simply showing how close to the surface such problems are swimming.)

A solution to this dilemma which is finding widespread adoption is to incorporate a 'buffer' into the serial interface. Such is the Epson 8145 interface, which has a 2000-character (approx.) buffer. Since the MX-80 chugs along at 80 characters-per-second (cps), if the computer transmits at 300 baud (30 cps) the buffer is normally virtually empty. At line-feed time the buffer fills up a little as the computer continues to transmit. But the MX-80 catches up on the next line. There is thus no need for handshaking. You can, however, get into trouble if the computer sends a large number of form-feeds, which take a long time

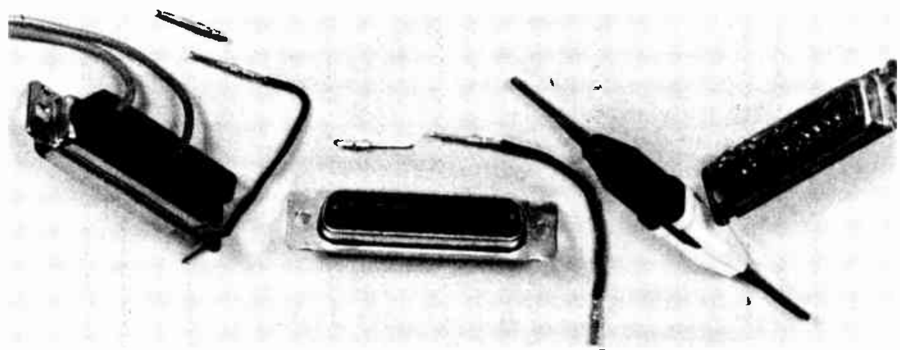


Figure 4. **Photo showing two different styles of RS232 connectors. In each case the individual wires are soldered to the connector pins or receptacles.**

To the left is a connector which comes with all the pins or receptacles permanently fixed in place; wires are soldered into 'cups' on the rear, which is the side in view here.

In the centre and to the right are shells which come 'empty', into which may be inserted male pins (into centre shell) or female receptacles (right). These can be more convenient, as the pins (shown separately and attached to wires) are easier to wire to before being placed in the shell, and in fact when installed are well separated by the shell (as can be seen in the rear view of the female connector on the right). The tool on the left is for the installation or removal of the male and female contacts.

In each case the connector may be bolted to a chassis, or put in a plastic cover for use as on the end of a cable.

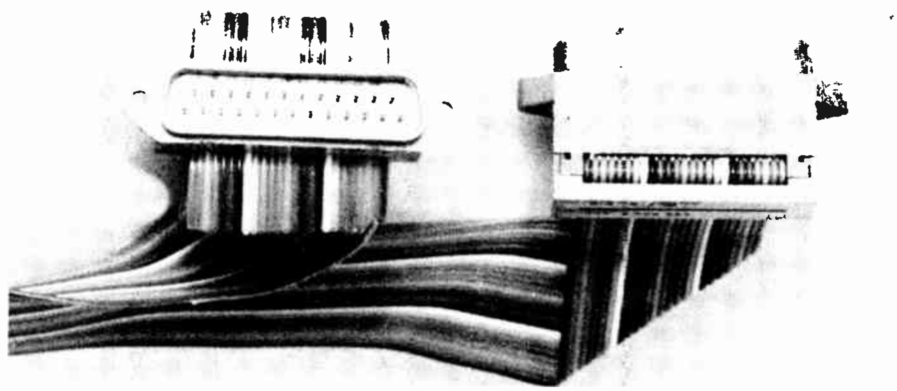


Figure 5. **These are called 'Insulation Displacement Connectors' (IDC) and of course must be used with ribbon cable. They can only be used if it is desired to connect all 25 pins at one end to all 25 at the other. However, they are very easy to install; all that is needed is a small vice to squash the connector onto the ribbon.**

Wires and connectors and stuff

The connector used with RS232 is known as a 'DB25', which has 25 pins in the male, and 25 receptacles in the female. Various styles are shown in Figures 4 and 5, with pin numbering shown in Figure 6. But why 25 pins?

RS232 was endowed with a pile of features not now used, and these were implemented using most of the 25 pins. Now very few of the pins are used. The extra pins provide two opportunities for confusion and problems, however. One problem is that with such a profusion of pins it can be difficult to figure out which ones you are supposed to use for your application.

'Business end' of male, or solder side of female.

1 2 3 4 5 6 7 8 9 10 11 12 13
14 15 16 17 18 19 20 21 22 23 24 25

'Business end' of female, solder side of male.

13 12 11 10 9 8 7 6 5 4 3 2 1
25 24 23 22 21 20 19 18 17 16 15 14

IMPORTANT NOTE: This numbering scheme means that with the IDC connectors the pin numbers do *not* correspond to the ribbon conductor numbers; 1 will be 1, but pin 14 will be ribbon conductor 2, etc.

Figure 6. **DB25 contact numbering.**

The second problem area is that with all those extra tantalising pins available and otherwise doing nothing, many manufacturers use the 'spare' pins for other purposes. Exidy uses them for the cassette interface. IDS, in their Paper Tiger printers, use the same DB25 for both serial and parallel interfaces.

'Official' Signal Name	Abbrev[(1)]	Pin No.	DTE 'Terminal'	DCE 'Modem'	Comments
Protective ground	PG	1	—	—	Optional
Signal ground	SG	7	—	—	Necessary
Data:					
Transmitted data	TxD	2	Out	In	
Received data	RxD	3	In	Out	
Handshaking:					
Request to send	RTS	4	Out	In)	Basically
Data terminal ready	DTR	20	Out	In)	same use
Clear to send	CTS	5	In	Out)	Basically
Data set ready	DSR	6	In	Out)	same use
Connector Sex:			Male[(2)]	Female	

(1) Note that the handshaking lines are sometimes indicated as inverted signals (e.g: $\overline{\text{DTR}}$). The idea is that if for the data a low is a '1', then if the data terminal is ready it should send out a '1'. In fact it sends out a high, which corresponds to a zero, hence the desire to use inverted signal notation. This refers, however, to the identical signal. In contrast there is the rare occasion when the equipment actually does put out an inverted signal, i.e: low means ready, high means not ready. Yeah, I know, but don't complain to me!

(2) In fact almost all terminals use female chassis-mount connectors. (A notable exception is the Heathkit H19.) It seems that it is almost standard practice to use females on equipment chassis, and male on cables (except for much DEC equipment, which uses male chassis mounts on equipment, and female connectors on cables). Note that this means you can't tell the DTE/DCE gender from the sex of the connectors.

Figure 7. **Table of signals, what they do, and connector pin assignments.**

That's fine except that if between such units you use a cable with too *many* wires implemented (and this can easily be the case if you use a standard RS232 cable in a set-up which does not use handshaking) then you are likely to blow something at one or both ends!

The pins which *are* commonly used are shown in Figure 7. Note that the naming convention can result in a variety of confusions. If the equipment is masquerading as a DCE the manual may tell you that, for example, pin 2 is 'Transmitted Data', which strictly speaking is an *input*. However, the manual writer may not know this and instead call it 'Received Data', intending 'Received' in a looser sense.

Fighting back

The first thing to do before connecting *anything* is to make yourself a chart like the one in Figure 8 for each piece of equipment you may have to connect together. This is *especially* important if you are involved with many different units. I have a whole binder full of such charts on the equipment I work with. Using this binder I can almost instantly connect any two units with few problems.

The point to this chart is that for each of your pieces of equipment (and I assume you're working with at least two!) it serves to collect the titbits of information you will glean from the manuals, the schematic and so on. You end up with the info in the same format for each unit, where it can be simply compared to give you the best idea of how to wire things up *before* you blow anything, and before you have the frustrating experience of having the system not work.

If handshaking lines are provided, try to find out if they actually do anything, or if they are dummies. For example, one printer may have an output which signals the sending computer to halt. Another printer may claim to have the same handshaking output, but it is actually internally wired permanently high, and is provided merely for supposed compatibility to a computer which may need such an input so as not to halt. Got that?!

Wiring up the cable

You will notice that if one of your units is a true DTE and the other a true DCE then a standard cable (pin 1 goes to pin 1, 2 to 2 and so forth, which is called a 'straight-through') will work. You are unlikely to see this situation very often, which is something you should know before you buy such a cable made up (they're likely to be expensive ready-made), or before you get convinced by the salesman that the printer hook-up is trivial.

So you decide to wire your own cable. First, of course, you must obtain the appropriate sexes of connectors to mate with what you have on the equipment, and a cable with a sufficient number of conductors. If it's over 20 feet you may wish to use shielded cable, but I've used unshielded up to several hundred feet. ▶

PIN NO.	SIGNAL ABBREV.	SIGNAL NAME	IN/ OUT	OPEN OK?	COMMENTS
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

EQUIPMENT TYPE: **CONNECTOR SEX ON EQUIPMENT:** **DATE:**

Figure 8. **Interface chart to save you headaches.**

(continued from page 29)

- **S1 & S2** Hidden switch, normally concealed under the dash or front seat, must be in the set position to activate the alarm or the cancel position to deactivate the alarm (Figure 8).
- **W1 to W3** Wiper control relay contact with W1, W2, W3 corresponding to the common, normally open and normally closed relay contacts. This relay is suitable for the majority of wiper motors, the exception being a continuously variable system.

A number of wiper arrangements have been used over the years but these can be loosely divided into two categories, motors with wound fields or motors with permanent magnet fields.

The earliest type of motor employed a wound field, and these were characterised by a good self-braking action. All that is required for control is a simple on-off switch. Self parking is achieved by a mechanically linked parking switch which keeps power applied in all but the parking position (Figure 11a).

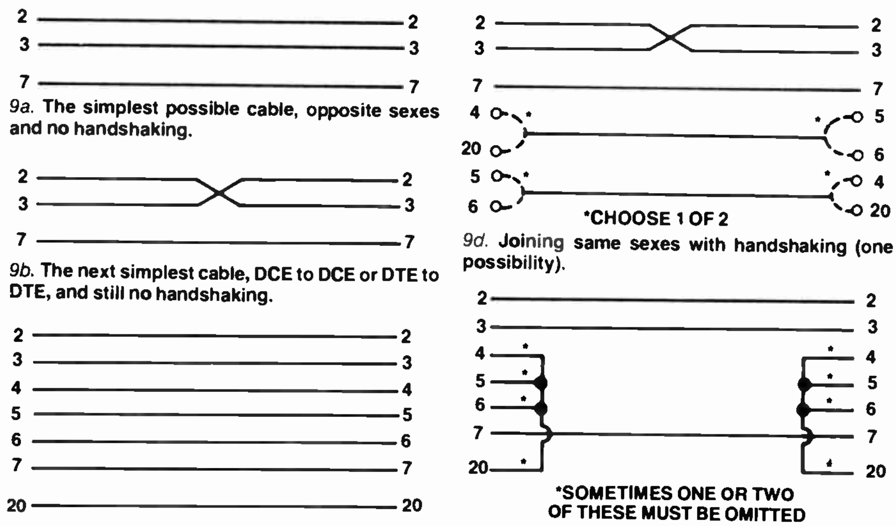
The more recent type of permanent magnet motor does not have the same braking characteristics, and it is necessary to apply dynamic braking by placing a short across the armature. Here a changeover self-parking contact is used which either applies power to the armature or places a short across it (Figure 11b). The added relay contact opens the brake circuit and then applies power to the armature low speed brush. (Dashboard switch is off.) Once the wipers are in motion the cam-operated contacts parallel the relay contacts, allowing the relay to be released and the wiper action to continue until one complete sweep has been made. Thus the wiper will give a single low speed stroke for each relay operation.

In vehicles fitted with an electrically driven clock there is a possibility of false alarms. This applies particularly to clocks that are rewound at intervals by a small motor.

Two general approaches may overcome this problem. Reduce the sensitivity of the battery detector or limit the starting current of the clock motor.

The sensitivity of the battery detector is adjusted by the 470k preset, while the start-up current can be reduced by the network shown in Figure 13. The component values are a guide only and in certain instances a series resistor may be found to be all that is required.

If all else fails the alarm may be triggered by the TH or TL inputs via the roof light circuit. Hopefully the battery detector can still be set to operate with the brake light or similar high current circuit. ●



9a. **The simplest possible cable, opposite sexes and no handshaking.**

9b. **The next simplest cable, DCE to DCE or DTE to DTE, and still no handshaking.**

9c. **Cable to join opposite sexes with handshaking. ('Standard' straight-through cable.)**

9d. **Joining same sexes with handshaking (one possibility).**

9e. **Joining opposite sexes, with defeated handshaking at both ends.**

Figure 9. **Some typical cable hookups.**

Next, no matter what the equipment involved, wire pin 7 to pin 7. If it's a straight-through you are making, then go right ahead, 2 to 2, 3 to 3, etc.

The next-most-delightful situation is where the two units are of the same sex and need no handshaking lines. For the data lines simply wire 2 to 3 and 3 to 2.

If handshaking lines *are* needed then determine which handshaking outputs actually mean something (as opposed to the dummies). Then connect these to the handshaking inputs of the opposite units.

You may have a sender which is sending to a receiver which does not need to halt the sender. If this is the case you need to decide what to do with the sender's handshaking input. In some units it can merely be left open (unconnected), and this is seen as the same as 'high'. On other units open is taken as a 'low' and halts transmission. The handshaking input may be wired permanently high by jumpering it to a handshaking *output* on the *same device*. This is normally done inside the plug on that unit's end of the cable. Figure 9 shows some typical cable configurations.

The initial hook-up

Armed with the appropriate (we hope) cable, plug in and see if it works! It probably won't, so refer to Figure 10, which is a summary of all the things to check to make the two pieces of equipment compatible communicators.

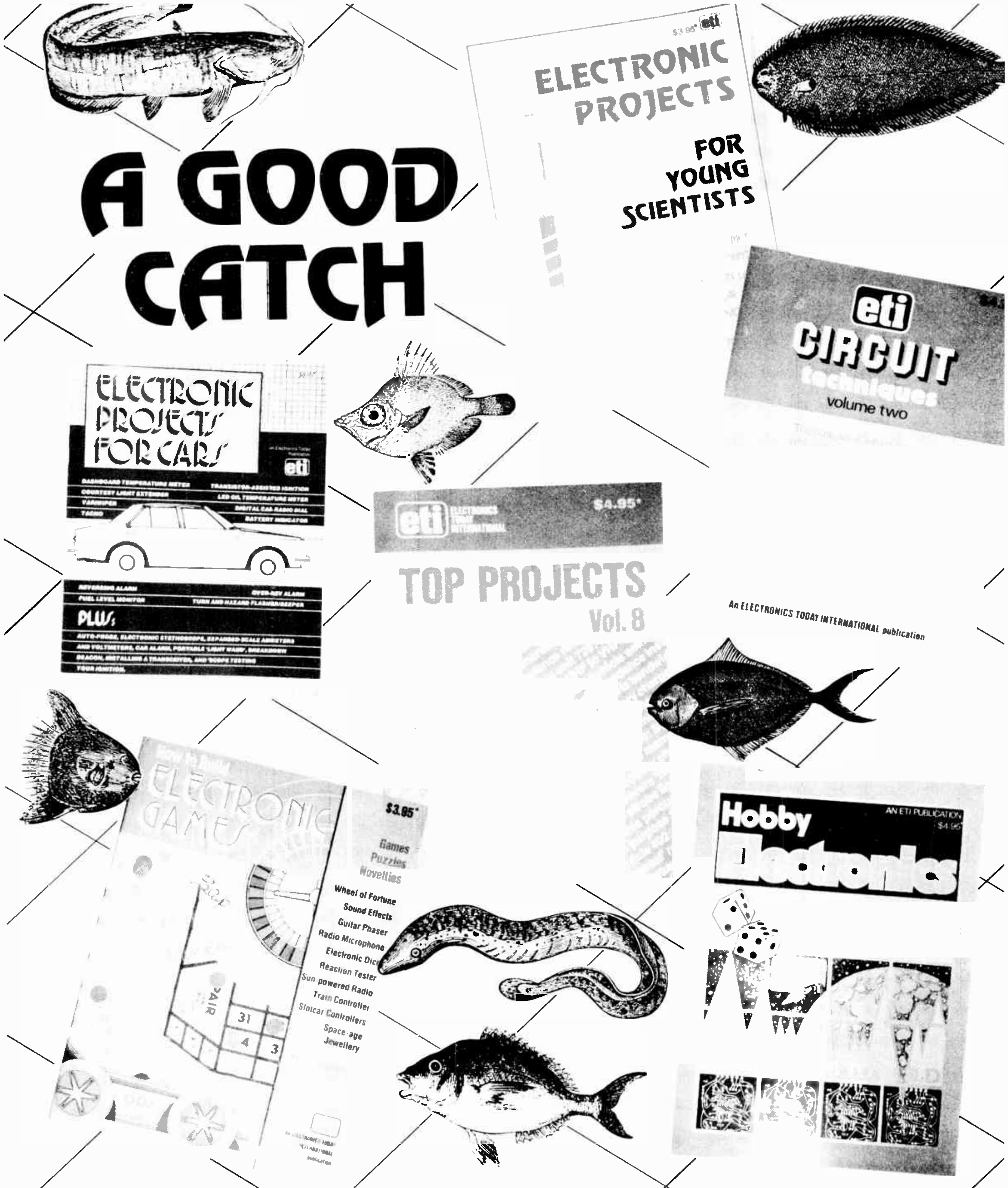
A test box to defeat all problems

So perplexing are some RS232 problems which I have encountered that I highly recommend obtaining a test unit of some kind if you are going to be involved with many such situations. In the next part of this article we intend to present details of a device which is designed to handle these problems, and which also permits quickly patching together any trial interface configuration. Unlike commercial units, it will even enable you to determine the inputs and outputs of a completely unknown interface with no documentation. ●

1. Number of **bits per character:** 5, 6, 7, or 8.
2. Number of **Stop bits:** 1 or 2.
3. **Baud Rate:** 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600 or other.
4. What to do with **Parity:**

   On transmission: No Parity, Even Parity, Odd Parity, Parity bit set to 0, or Parity bit set to 1.
   On reception: No Parity expected, Ignore Parity, Expect Odd, or Expect Even.
5. **Full** or **Half Duplex.**
6. Make sure machines are **On Line** if they have the ability to be off line.
7. A rather rare final item which can cause problems is an option on a few machines which allows for the inversion of the polarity of the data signals and/or handshaking signals. You should set these to: Negative Mark for the data lines, and handshaking lines should indicate OK to proceed with a high level, STOP with a low level.
8. What to do with a system which can't be made to work after all this is the subject of next month's article.

Figure 10. **List of quick checks to make when hooking up two pieces of gear for the first time.**



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RS232 serial interface troubleshooter

Making a 'standard' RS232 interface work can be a nightmare. 'Standards' not withstanding, you can regain lost sleep with this troubleshooting unit.

Graham Wideman

THE PREVIOUS feature explained how computer serial interfaces of the RS232 type are supposed to work, and why they frequently won't. Here we present the design and construction details of a test unit which solves most of these problems. You may wish to build it as described here, or simply borrow the principles to troubleshoot interfaces using other instruments.

The troubleshooter provides the capability to patch together any wiring arrangement, and to monitor what is happening on each wire. In this much it parallels the better commercially-available RS232 'problem solvers'.

However, it also includes an apparatus for determining exactly which interface wires are outputs, inputs, not connected, or shorted, thereby making possible a complete picture of a totally unknown interface. This is extremely useful if the equipment in question has no manual, or as is more likely, has a manual which leaves the subject of the RS232 interface completely ambiguous.

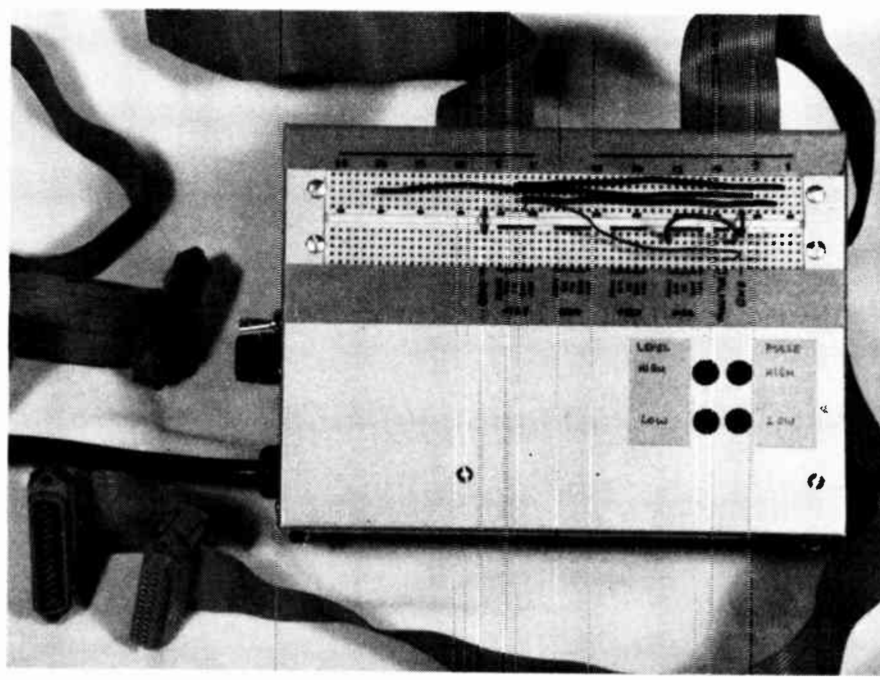


Figure 1. **The RS232 troubleshooter.**

Patching board

The heart of the troubleshooter is a breadboard patching block which is wired permanently to a pair of ribbon cables, each cable having attached to it both male and female DB25 connectors of the 'insulation displacement' squash-on variety. After peeling the adhesive plastic backing off the breadboard block (and cleaning it up a bit), the individual conductors of the ribbon cable are soldered to the *underside* of the rows of contacts in the breadboard, as shown in the photo of Figure 2, and detailed in the diagram of Figure 3.

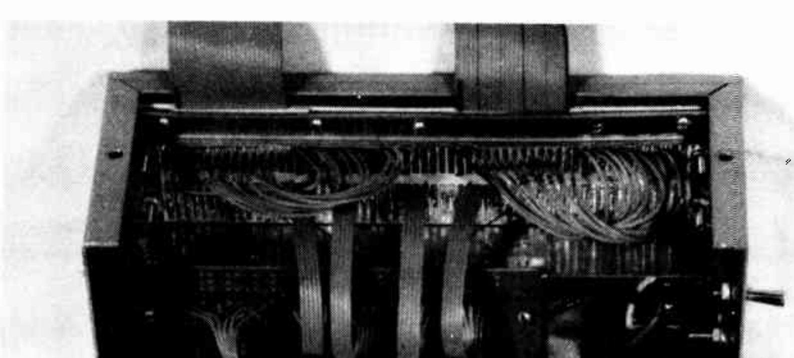


Figure 2. **Closer view of breadboard area used for patching the troubleshooter's two DB25-equipped ribbon cables, and for connection to the unit's signal monitor and test signals.**

This simple device already gives two capabilities, as shown in Figure 4. First, both cables can be attached, one to each of the pieces of equipment which are to be interfaced together. Having both a male and female connector on each cable ensures that plugging in will be no problem. Then the particular pin-to-pin wiring can quickly be tried out using jumper wires on the tester's breadboard patching area, before a permanent cable is made up.

The second way to use the device as so far described, is for 'tapping into' an existing interface arrangement which is now perhaps malfunctioning. Suppose

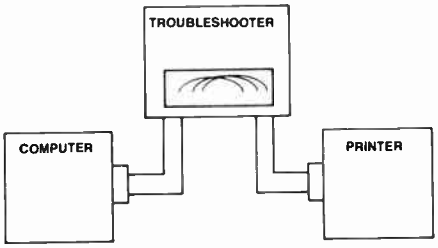


Figure 4a. **Using the troubleshooter's patching area to rig new trial cable before making permanent version.**

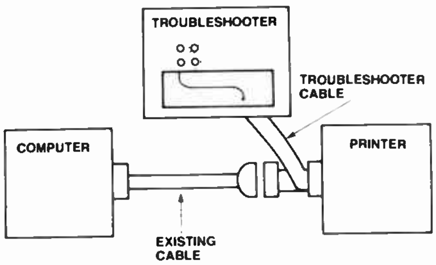


Figure 4b. **Using just one ribbon cable, the troubleshooter provides a convenient way to tap into and monitor the signals on a 'supposed to be working' RS232 hookup.**

the 'existing system' is a computer talking to a printer. Simply unplug one end of the computer-to-printer cable (let's say the printer end), and plug it into one of the two connectors (male or female as appropriate) on one of the troubleshooter's ribbons. Plug the remaining connector on the *same* ribbon into the receptacle on the printer. Now the short length of ribbon between male and female DB25s carries the connection from computer to printer, and in addition this ribbon brings out all 25 lines to the breadboard where they may be conveniently monitored.

Signal monitor

In order to monitor the signals on an RS232 line it is possible to get away with simply a LED with a resistor in series. However this loads the line, possibly changing the conditions you were trying to monitor. Additionally, you would not see any quick pulses of activity which may be important.

Consequently the monitor incorporated in this tester has been designed to address these two problems. Four LEDs are used, two to indicate a steady high or low level, while the other two flash on for about a half second in response to a positive or negative pulse. The level LEDs respond only to valid high or low signals; a voltage in the middle (around zero), or an open line will cause neither LED to illuminate. The LEDs are powered from a built-in mains power supply, and the RS232 line is monitored via high impedance buffers, so as not to disturb it.

(It should be remembered here that the RS232 line levels are −3 V to −12 V for a 'low' representing a data '1', and +3 V to +12 V for a 'high' representing a 'zero'. With no data the line sits at low.)

The monitor input is soldered to the underside of a contact strip on the breadboard (actually two strips, in case of wear), and thus may be patched to any other contact as desired for observation of the signals there. ▶

```
Test Signals                                                 From DB25s
                                               Ribbon
                          ooooo   ooooo               DB25
                          ooooo   ooooo        24     25     DB25 Cable A
                          ooooo   ooooo        22     24          |
                          ooooo   ooooo        20     23          |
                          ooooo   ooooo        18     22          |
                          ooooo   ooooo        16     21          |
                          ooooo   ooooo        14     20          |
                          ooooo   ooooo        12     19          |
                          ooooo   ooooo        10     18          |
                          ooooo   ooooo         8     17          |
                          ooooo   ooooo         6     16          |
                          ooooo   ooooo         4     15          |
                          ooooo   ooooo         2     14          |
                          ooooo   ooooo        25     13          |
                          ooooo   ooooo        23     12          |
                          ooooo   ooooo        21     11          |
                          ooooo   ooooo        19     10          |
                          ooooo   ooooo        17      9          |
                          ooooo   ooooo        15      8          |
             Ground       ooooo--ooooo         13      7          |
                          ooooo   ooooo        11      6          |
 -12V     100k            ooooo   ooooo         9      5          |
  "         4k            ooooo   ooooo         7      4          |
  "         1k            ooooo   ooooo         5      3          |
  "       300             ooooo   ooooo         3      2          |
  "       100             ooooo   ooooo         1      1     DB25 Cable A
                          ooooo   ooooo
                          ooooo   ooooo
Ground    100k            ooooo   ooooo
  "         4k            ooooo   ooooo
  "         1k            ooooo   ooooo
  "       300             ooooo   ooooo
  "       100             ooooo   ooooo
                          ooooo   ooooo        24     25     DB25 Cable B
                          ooooo   ooooo        22     24          |
 +12V     100k            ooooo   ooooo        20     23          |
  "         4k            ooooo   ooooo        18     22          |
  "         1k            ooooo   ooooo        16     21          |
  "       300             ooooo   ooooo        14     20          |
  "       100             ooooo   ooooo        12     19          |
                          ooooo   ooooo        10     18          |
                          ooooo   ooooo         8     17          |
Osc.      100k            ooooo   ooooo         6     16          |
  "         4k            ooooo   ooooo         4     15          |
  "         1k            ooooo   ooooo         2     14          |
  "       300             ooooo   ooooo        25     13          |
  "       100             ooooo   ooooo        23     12          |
                          ooooo   ooooo        21     11          |
Monitor                   ooooo   ooooo        19     10          |
  "                       ooooo   ooooo        17      9          |
                          ooooo   ooooo        15      8          |
             Ground       ooooo--ooooo         13      7          |
                          ooooo   ooooo        11      6          |
                          ooooo   ooooo         9      5          |
                          ooooo   ooooo         7      4          |
                          ooooo   ooooo         5      3          |
                          ooooo   ooooo         3      2          |
                          ooooo   ooooo         1      1     DB25 Cable B
                          ooooo   ooooo
```

Figure 3. **Diagram showing one possible arrangement for the breadboard connection area. Note that the DB25 ribbon cables occupy one 'side' of the board, and the test monitor and signals occupy the other. Opposite each ribbon's pin number 7 is a ground connection, across which would normally be installed a small jumper.**

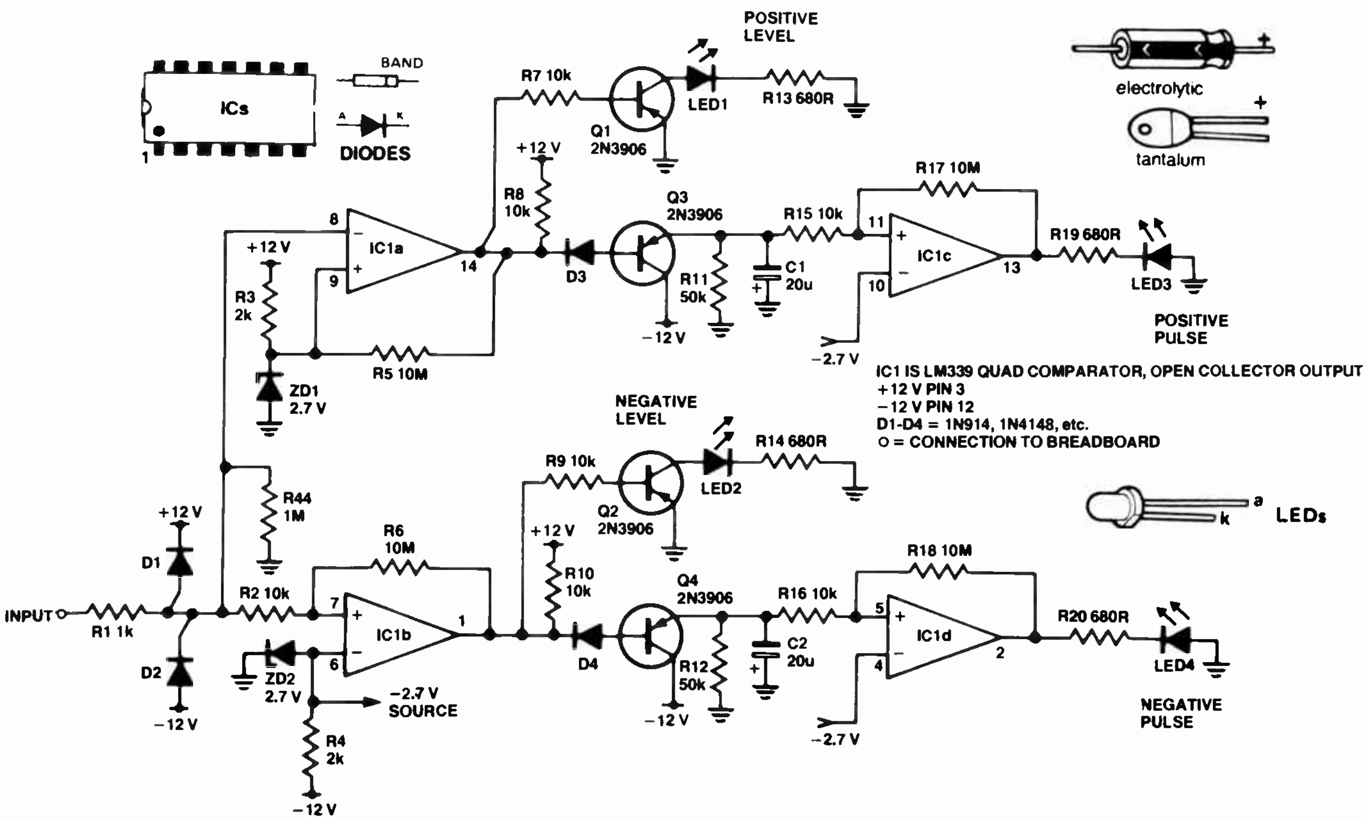


Figure 5. **Circuit diagram of monitor section.**

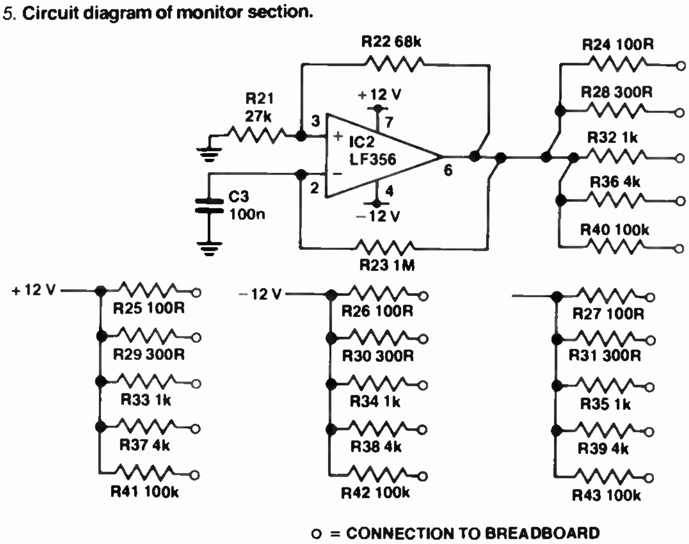
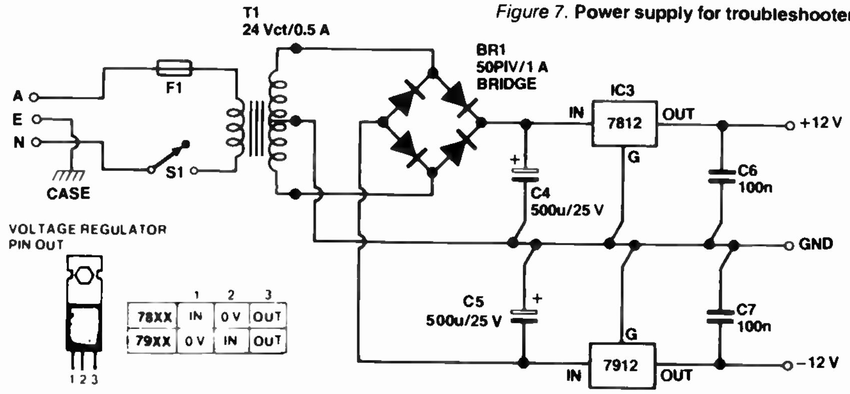


Figure 6. **Circuit of test oscillator, and other test levels.**

Figure 7. **Power supply for troubleshooter.**

T1
24 Vct/0.5 A



The circuit diagram and description for the monitor, the test oscillator to be described, along with the power supply, are to be found in Figures 5 to 7.

Generated signals

Of immediately obvious use are the 'high' and 'low' signals provided. These may be used to apply 'halt' or 'go' signals to handshaking lines. Additionally there is built-in a square-wave generator which continuously oscillates between high and low conditions at a rate of approximately five times per second.

Each of these signals, along with ground, is supplied to contacts on the breadboard via a selection of resistors, from 100 ohms to 100k ohms. The usefulness of this arrangement may not be immediately apparent, and for explanation I must describe the electronic circuits which transmit or receive on an RS232 line.

How it works

The monitor

The schematics for the troubleshooter's main monitor, test oscillator and power supply are to be seen in Figures 5 to 7.

Components R1-D1-D2 prevent the input signal from causing damage should it happen to exceed the troubleshooter's power rail limits. From there the input signal is routed to two very similar 'channels', one concerned with 'high' levels and pulses, the other with 'low' levels and pulses.

Looking then at the positive channel, the input signal arrives at the negative input of comparator IC1a, where it is compared to a reference of about 2V7 (which is set by ZD1 at the positive input of IC1a). Supposing that the input signal exceeds 2V7, then IC1a's output is low, turning on Q1 via R7, and illuminating LED1 to indicate a 'high level'.

At the same time, the low level (about −10 V) at the output of IC1a turns on Q3, quickly charging C1 'down' to about −9 V. IC1c sees this voltage and compares it to −2V7, sees that it is lower and lowers its own output illuminating LED3 to indicate a 'high pulse'.

If the monitor input now drops below 2V7, IC1a's output will go high, turning off Q1 and the 'high-level' LED1, and also Q3. However the 'high pulse' LED3 will remain on for a short while (about a half second) as C1 is charged up past the 2V7 point by R11. Notice that this delayed LED3 action would have occured even if LED1 had been on for only an invisibly short length of time. Hence LED3 makes visible short pulses which cannot be seen by simply watching the level, whether on the troubleshooter's level LEDs, or even with an oscilloscope.

The negative channel works similarly, the only change being to swap the positive and negative inputs of the input comparator.

Test oscillator

As we shall see, IC2's output must sit in either high (about +10 V) or low (about −10 V) states. Let us assume that it is initially low, and that C3 starts out uncharged, so that there is 0 V at the op-amp's negative input.

Since the op-amp output is at say −10 V, the positive input will be at approximately −3 V, established by the R21-R22 voltage divider. Remembering that we assumed the negative input to be at 0 V, the 'low' output will remain temporarily unchanged.

However, the low output will charge C3 via R23 downwards. After a while the op-amp negative input will be less than its positive input (at −3 V), and thus the output will change states to +10 V. When this happens the voltage at the positive input changes, of course, to +3 V, maintaining this state of affairs.

Again we must wait for C3 to be charged via R23, this time up to +3 V. You should be able to see that this oscillating action will continue, and that the period is the time taken for C3 to charge from −3 V to +3 V, then back down to −3 V, when R23 is pulled up to +10 V and then down to −10 V respectively.

The values given provide a frequency of about 5 Hz, quite suitable for this testing purpose.

The oscillator output is delivered to the breadboard area via various values of resistor, as described in the text.

Of drivers and receivers

For various reasons, special purpose buffers are used to send signals and receive signals on an RS232 line. These are called 'drivers' and 'receivers', and are exemplified by the National LM1488 and 1489 respectively. Figures 8 and 9 show a simplified view of how the driver output and receiver input look electrically.

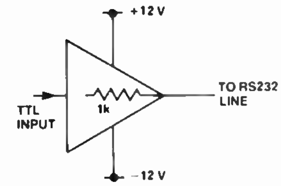


Figure 8. **Simplified view of an RS232 'driver' output.**

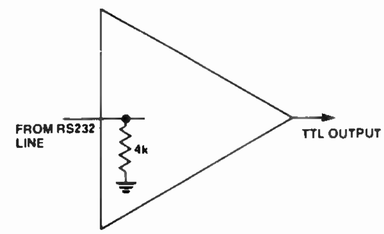


Figure 9. **An RS232 'receiver' looks like this electrically.**

The points to notice are that a receiver input looks like a (approximately) 4k resistor to ground. An operating driver output looks like a (approximately) 500 ohm resistor pulling up to 12 V (nominally), or pulling down to −12 V, according to its state.

Knowing these facts it is apparent that if a high or low signal is applied through a resistor to a receiver input or driver output, the resulting signal on the line (which can be monitored) will be high, low or in-between depending upon the value of resistor used.

Therefore, when looking at an unknown line, by applying the test oscillator's output via each resistor in turn, it is quickly possible to tell what that line does. The chart in Figure 10 details this. ▶

Parts List

Resistors .... ¼ W unless specified
- R1 .... 1k
- R2 .... 10k
- R3, 4 .... 2k
- R5, 6, 17, 18 ...... 10M
- R7, 8, 9, 10, 15, 16 . 10k
- R11, 12 .... 50k
- R13, 14, 19, 20 680
- R21 .... 27k
- R22 .... 68k
- R23 .... 1M
- R24, 25, 26, 27 100
- R28, 29, 30, 31 300
- R32, 33, 34, 35 .... 1k
- R36, 37, 38, 39 .... 4k
- R40, 41, 42, 43 .... 100k
- R44 .... 1M

Capacitors
- C1, 2 .... 20u/20 V electrolytic
- C3, 6, 7 .... 0u1 tantalums
- C4, 5 .... 500u/25 V electrolytic

Diodes
- D1, 2, 3, 4 .... 1N914 or 1N4148 etc
- ZD1, 2 .... 2V7 small zener diode
- BR1 .... Bridge rectifier, 50 PIV/1 A
- LED1, 2, 3, 4 ...... LEDs of your choice of colour

Transistors
- Q1, 2, 3, 4 .... 2N3906

Integrated circuits
- IC1 .... LM339
- IC2 .... LF356A
- IC3 7812
- IC4 7912

Transformer
- T1 .... 240 V primary, 12-0-12/500 mA secondary

Miscellaneous
Breadboard, case, fuse and holder, switch for power, power lead and plug etc.

Line Condition	Oscillator Signal via Resistor (ohms) 100k	4k	1k	300	100
Open	HL	HL	HL	HL	HL
Receiver Input	None	HL	HL	HL	HL
Driver Out-Low	L	L	L	FL/HL	HL
Driver Out-High	H	H	H	FH/HL	HL
Short to Ground	None	None	None	None	None
Short to +12 V	H	H	H	H	H
Short to −12 V	L	L	L	L	L

Charts shows the Level LEDs (not 'pulse' LEDs) activated in various cases.

H = High; L = Low; None = neither LED on; HL = alternating H and L; FL = Flashing Low; FH = Flashing High

Figure 10. **Chart showing how to test an unknown RS232 line, and the monitor's indications under various conditions.**

A word of warning is in order here however. Proper use of the monitor assumes that you at least know which pin on the connector is ground. This is almost always pin 7, so consistently in fact that we located the monitor's ground points on the breadboard opposite to the pins 7 of each of the two ribbon cables, and permanently left a small jumper installed at these two locations (see Figure 3). However, there are lurking about some units which don't abide by this standard. The only thing you can do about this (if you are documentationless and suspect this problem) is to open the case and actually trace the unit's circuit-board ground and see what DB25 pin it goes to.

Construction notes

The construction is not too critical. As can be seen the prototype version was built using Veroboard. One plan which is extremely useful to follow is to make a simple frame assembly like the one shown in Figure 11, which serves two purposes.

First it includes a flat clamp to grip the two ribbon cables (liberal use of double-sided wall-tile sponge adhesive tape also helps). Secondly, it keeps together the circuit board and the breadboard. In both these respects it makes wiring to the breadboard easier, and virtually eliminates any problems of wire breakage when the various parts are moved about during construction or testing of the project. As the photos show, the entire guts of the prototype can be removed in one piece, connected to the case only by the leads to the PSU.

Another hint: DON'T FORGET when soldering the ribbons to the breadboard that the numbering of the DB25 pins is *not* the same sequence as the ribbon cable conductors. This is shown in Figure 3.

Improvements

Although our troubleshooter has proved tremendously useful, I cannot claim that our prototype is the last word. In fact, I feel that if done again we would add several extra LEDs as simple on-off high-low indicators along with the existing level plus pulse monitor, so as to keep an eye on several lines at once. You may wish to adopt this idea in your unit. ●

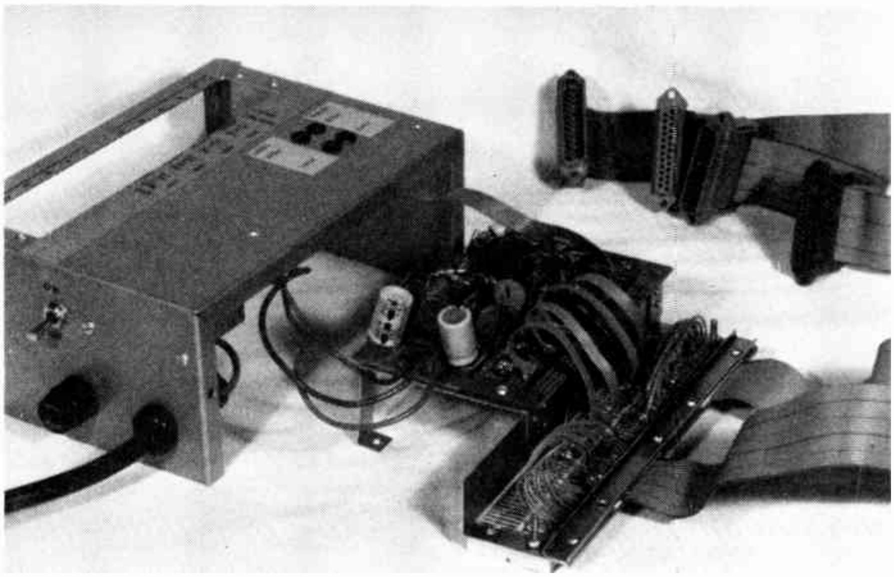


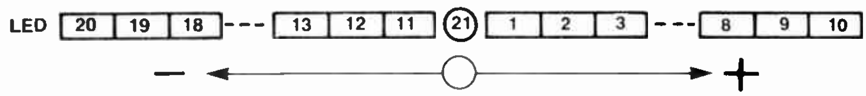
Figure 11. **When constructing a unit such as this, where there are a lot of wires hanging around, it's helpful to use brackets and cable clamps like the ones in this photo. They prevent undue strain on soldered connections, improving reliability, and enable the circuitry to come out of the box in one piece, more or less, for testing purposes during construction, or later if the unit needs repair.**

Centre zero LED bar/dot meter

D.H. Dawes
Granville NSW

THIS CIRCUIT drives twenty LEDs with a single bar/dot driver. Ten LEDs (green) are for a positive input signal and ten LEDs (red) for a negative input signal. A yellow LED, which is lit permanently, gives the centre zero indication. The LEDs would, for best effect, be mounted on a panel as shown below:

CENTRE ZERO BAR/DOT METER



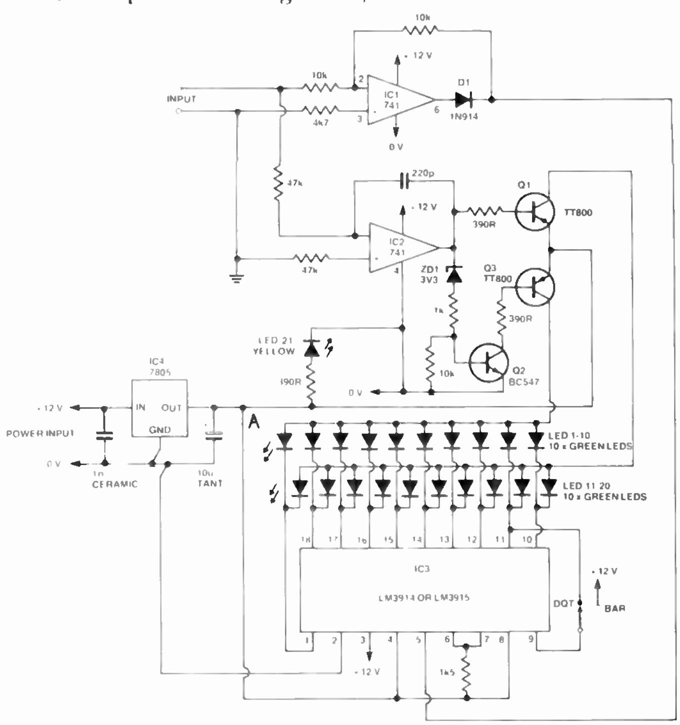
When used in the bar mode, the bar of light elongates to the left for an increasing negative signal and to the right for an increasing positive signal.

The circuit runs from a single 12 Vdc supply. A 5 V regulator is included, which serves both to power the LEDs and to provide a reference line for the positive and negative input signals.

IC1 is connected as a simple (but effective) 'absolute value' amplifier. This drives the LM3914, which will only accept positive input signals. IC2 is connected as a comparator, and serves as a polarity indicator. When the input is positive the output of the comparator is high, which drives Q3 via ZD1 and Q2, enabling LEDs 1-10.

When the input is negative, the output of the comparator swings low, switching off Q3 and switching on Q1, which enables LEDs 11-20. As there is no gain in the absolute value amplifier, the full-scale reading is equal to that set by the internal reference of IC3. This means that the full-scale value of this circuit is about ±1.2 V. This value can be altered by conditioning the required input signal. The LM3915 may be substituted for the LM3914 if a logarithmic, rather than a linear, scale is desired.

This circuit can, apart from its obvious applications as a general centre zero meter, be used to display the difference between two voltage levels, e.g: a reference level and an unknown level. In this application the position on the circuit marked 'A' would be separated from the +5 V line and would be connected to the reference voltage. The unknown voltage to be compared would be connected to the input terminal. Both the reference and the unknown would be referred to 0 V. The only limitation is that the reference voltage should be between 4 and 8 volts above 0 V when using a 12 V supply. ●



Dual wiper unit

Ian Robertson

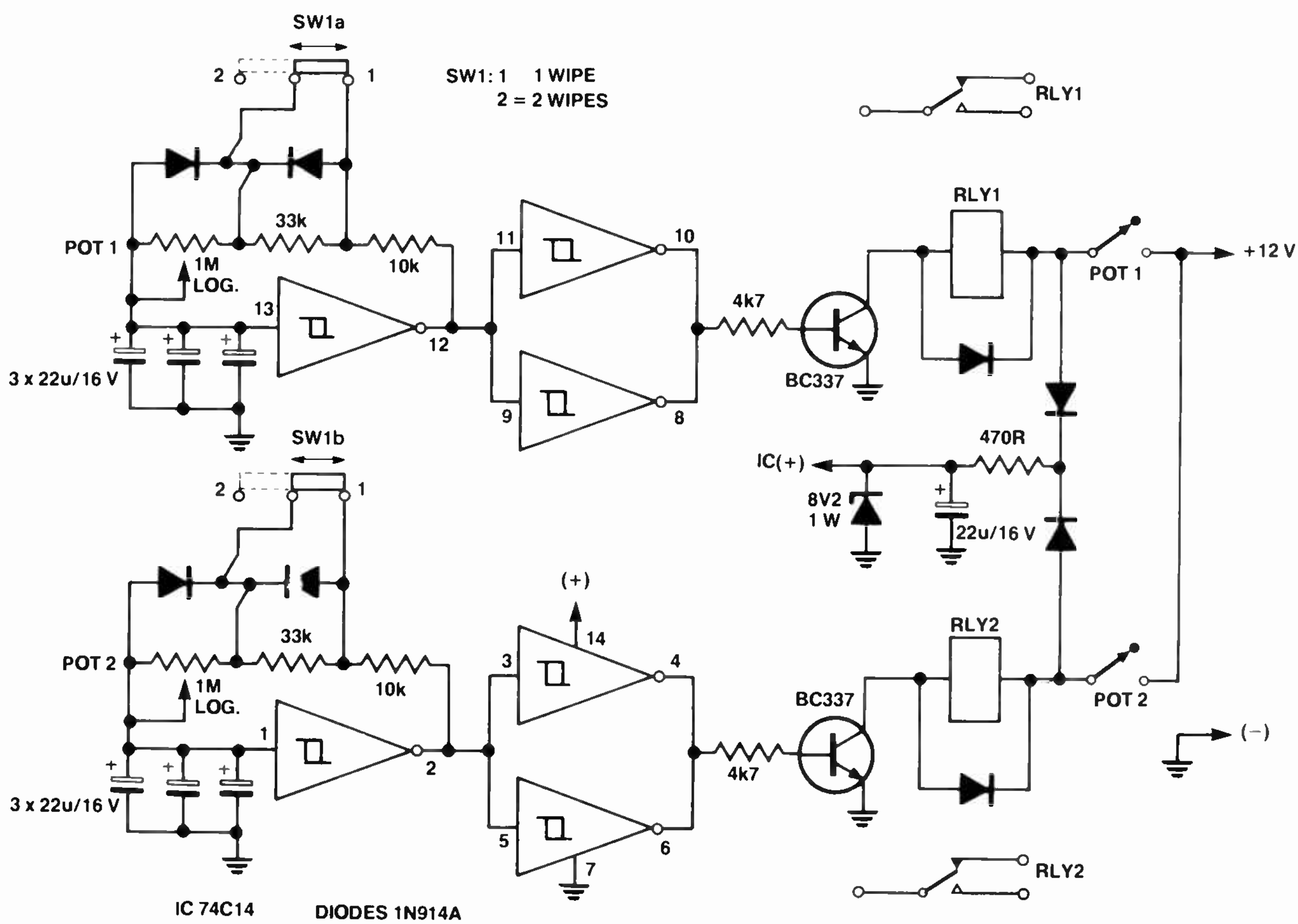
Helensburgh NSW

The recent spell of unsettled weather quickly demonstrated how useful the intermittent wiper control that had been fitted to my previous car was. In common with a number of contemporary hatchbacks, my new Mazda 323 is fitted with front and rear wipers, but this feature actually serves to lengthen the time spent fiddling with the wiper controls.

I soon found the fixed delay provided by Mazda a poor substitute for a fully variable system for the front windscreen; any fixed delay seems to be right only about 5% of the time! A fixed delay may be OK for the rear window, however, since even in heavy rain the glass needs only an occasional wipe.

I therefore developed this dual wiper unit, which is given here as fitted to the Mazda 323 hatchback, but which should also fit the Ford Laser without modification. For other cars only the external wiring should require change. The circuit can be used on cars with only one set of wipers by simply not using, or more likely not building, the rear part of the circuit.

This design has two identical delay sections, each feeding a miniature relay — one relay for the front wiper and one for the rear. Each section has a potentiometer to adjust the cycle rate, varying from continuous operation to a wipe every 60 seconds. An additional switch is provided to enable single or double wipes to be selected, two wipes being better on the longer delay settings. Each potentiometer incorporates a switch to turn the relevant section off; this arrangement guarantees that the screen is wiped immediately the wiper is

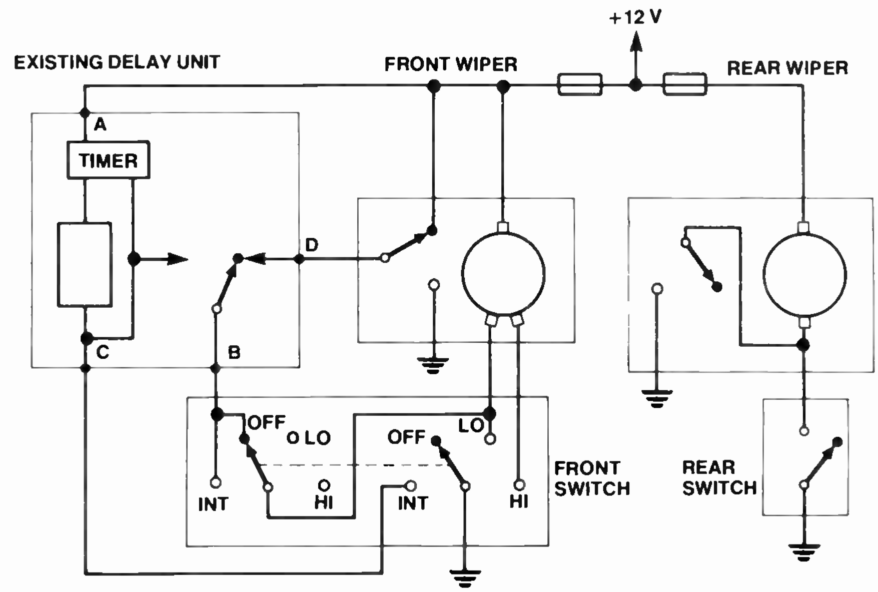


turned on, rather than after whatever delay is set on the pot.

The circuit operates by pulsing the wiper motor for approximately half a second and then following with a variable delay before the next pulse. The length of the pulse is not critical; once the wiper has started to move the inbuilt 'parking' contacts will complete the cycle. If the pulse is made longer than the time taken by a single wipe, two or more wipes will occur, the exact number depending on how long the pulse is made.

Wiper motors may use either permanent magnets or electromagnet field assemblies, the latter being easier to control with a simple on/off switch; the permanent magnet type will tend to run on unless brought to a stop by a short in the armature. The Mazda is fitted with a permanent magnet wiper in the front and a wound field wiper in the rear. Refer to the circuits to see how each type is driven by the wiper relays.

The circuit has two identical timer sections: one for the front and one for the rear. A single IC is used, the 74C14 Schmitt trigger hex inverter, using three inverters in each wiper section. Each section consists of an oscillator, followed by a buffer stage; this in turn feeds the output transistor and relay. The oscillator gives both the fixed half-second pulse and the variable delay between pulses. Normally an oscillator of this type has equal 'on' and 'off' times; however, diodes may be used to separate the timing capacitor charge and discharge paths and obtain any ratio of 'on' to 'off' times.



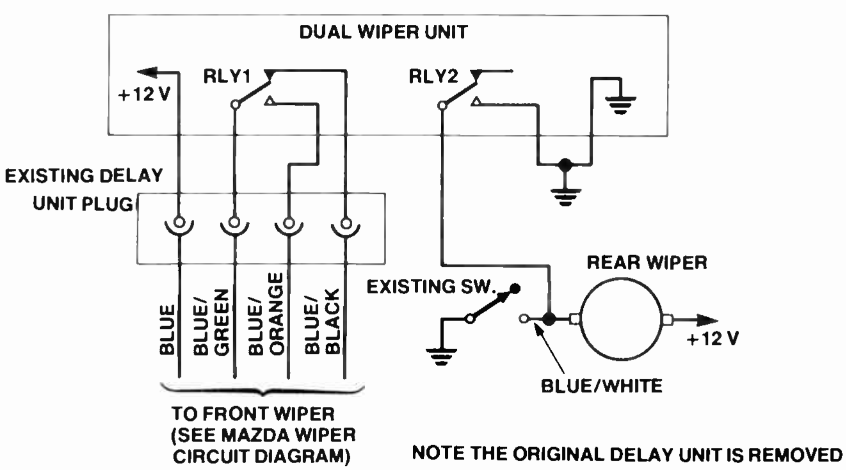
ORIGINAL WIPER CIRCUIT FOR MAZDA 323

In this circuit the charge path is via the 1 MHz potentiometer, which may delay the charge for up to 60 seconds, while the discharge path bypasses the pot and is determined by either the 10k or 33k fixed resistors, giving the desired half-second delay, single wipe setting, or half-second, dual wipe setting. In practice the actual times are component-related, and can be adjusted by varying the timing capacitor. The circuit shows three 22u tantalum capacitors in parallel; other values can be used, the aim being to reliably obtain a single and dual wipe on the respective switch settings.

Construction and fitting vary from car to car, so details will have to be left to individual constructors. Whatever form the unit takes, do not separate the potentiometer from the electronics board; if you want to reduce the size of the dash unit, mount the relays separately. Long leads on the potentiometer would be open to noise pick-up, leading to erratic wiper operation. Use pots with a logarithmic or 'C' curve; this will spread the short times, making the controls easier to use. Some constructors may prefer to use a 500K/C potentiometer, which is fine, the only effect being to reduce the maximum delay to 30 seconds.

A zener-regulated supply is used for the IC, which is powered whenever the front or rear wiper section is turned on and fed by the diodes immediately after the switches. Observe the usual precautions with the CMOS IC; it may be best to use an IC socket and fit the 74C14 after everything else is finished. If the rear wiper section is left out, tie the unused IC inputs to earth or to positive.

I have included diagrams of the original Mazda circuit, and how the unit fits into it. Using your car's circuit diagram it shouldn't be too difficult to work out the external wiring for other makes of car. ●



INSTALLATION DETAILS FOR MAZDA 323

Lab Notes

Improved text display for video monitors

Modify your video monitor to uncramp the lines of text. Here are the principles and practical circuitry.

Graham Wideman

REMEMBERING WHAT we were all playing with ten years ago, there is no denying that today's personal computers are marvellous pieces of equipment, and whatever your brand preference, tremendous value for money. And that sentiment is doubled for those of us who use a computer for 'serious' purposes — in our work. However, the serious user will notice that most personal computers sacrifice some degree of convenience of use for particular specialised applications. This is not surprising, as the manufacturers have tried to make their products as generally appealing as possible without unnecessarily increasing their prices with luxury features.

One such area is that of text display, where many personal computers 'trade in' some text readability in order to accommodate graphics capabilities. For many users this is of little consequence, but it becomes a major headache when using the computer for word processing, or even for long hours of programming. This article describes a method whereby a video monitor can be modified to counteract one of these shortcomings, and provide a display which will save your eyes and your temper.

Cramped lines

The problem which this article solves is that of 'cramped lines', where the lines of text are too close together to allow ease of reading or scanning. As an example, the author's computer, an Exidy Sorcerer, is of all the popular computers one of the most suited to text processing because it displays 30 lines of 64 characters, lower case letters, underlined characters using the programmable character set, has an extra keypad for word processor function keys, and has built-in parallel and serial ports for a printer. When teamed with an Exidy or Vista disk drive (which require no expansion interface) the result is a system which performs admirably . . . except for the display.

Each character in the display occupies an 8-by-8 dot matrix. The matrix squares butt up against each other both horizontally and vertically, so that pictures made using graphics characters appear to have continuous lines with no gaps where the characters touch each other. Normal capital letters use 5-by-7 dots, which leaves three dots' worth of space between adjacent characters on the same line, but only one dots' worth between characters on adjacent lines. This is not very nice, but excusable. The big problem arises when using both upper and lower case letters, such as normal text. Then characters such as 'y' and 'p', which have 'tails' (descenders) hanging below the line, use the bottom row of dots in the matrix for these tails. Now there is no space between lines, and for example a 'g'

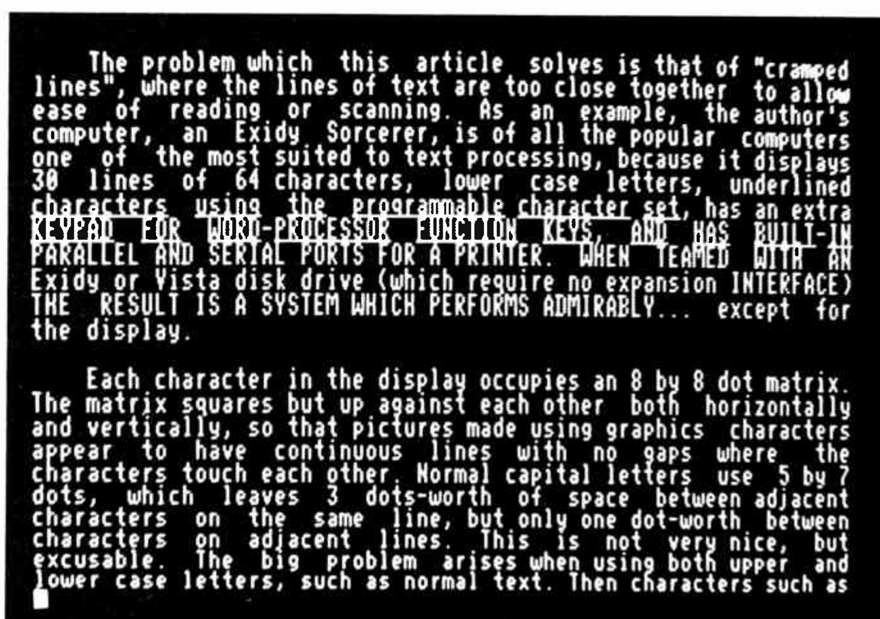
NOTES AND KEY FOR DIAGRAMS

POSITIVE POWER SUPPLY

CONNECTION TO GROUND

SCHMITT TRIGGER SYMBOL

~ APPROXIMATELY



You can turn this screen display into . . .

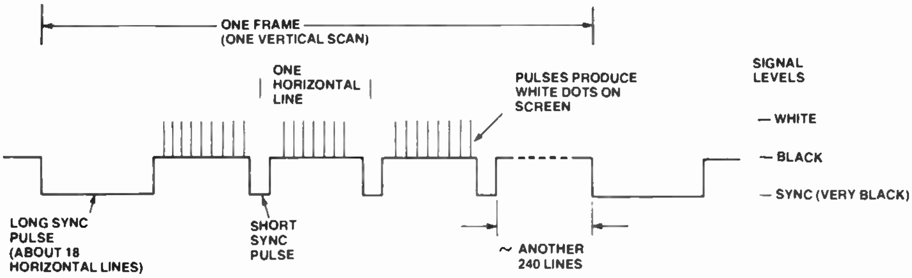


Figure 1: **Simplified diagram of the composite video signal.**

appearing above a 'T' will touch. In addition, underlined characters are most unreadable, since they too use this bottom row of dots in the matrix. It is thus desirable to be able to introduce some more space between each row of characters.

More space

There are several methods which are potentially useful in obtaining the desired spacing. One possibility is to modify the computer so that it allows a picture scan-line (or two) in between each row of characters. This proves to be unfeasible in the case of the Sorcerer because its 30 lines of characters already occupy 240 of the approximately 256 scan lines that you might be able to squeeze onto your monitor, which doesn't provide even one spare line per row of characters. In any case, such a modification to the computer could be rather messy.

Consequently, it is logical next to look at the video monitor itself to see if it could be modified to provide space between rows of characters. The answer is *yes*. The following description of how this is done is *not* a complete design for any particular monitor, but is instead intended to be adapted to whatever monitor you have. The simple circuitry shown was incorporated into a 'monitorised' TV set, and demonstrates the techniques involved.

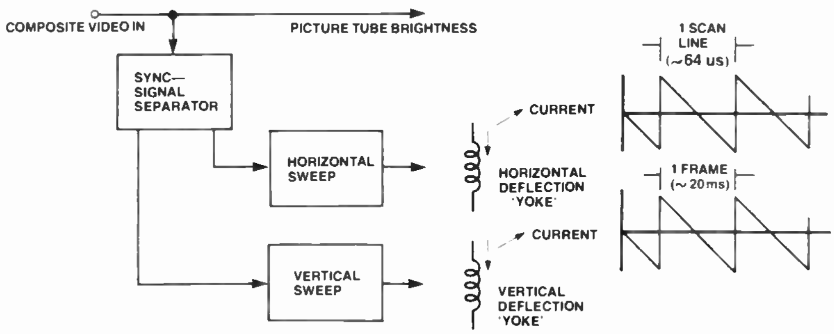
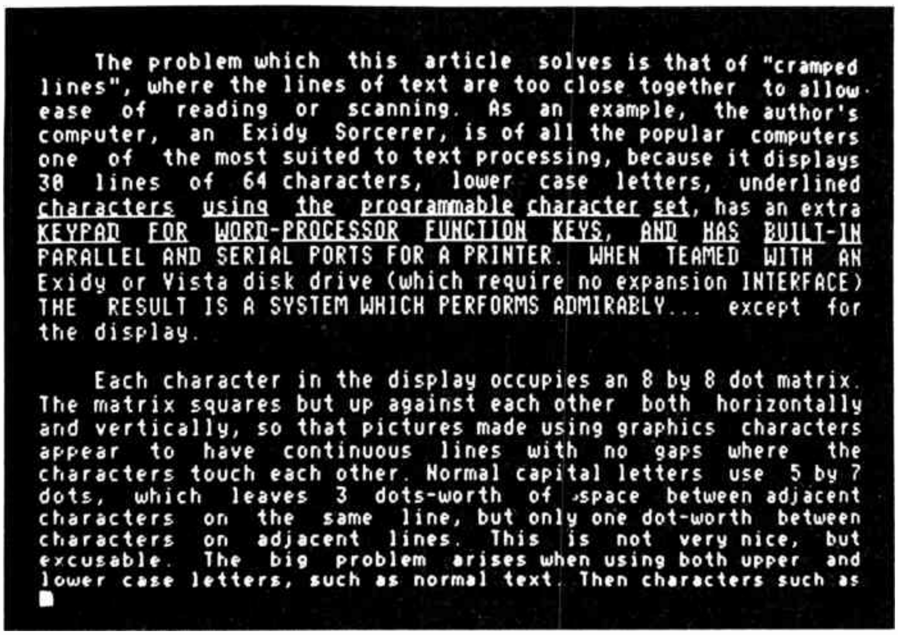


Figure 2: **Conceptual picture of TV or monitor sweep sections.**

Vertical sweep operation

Before proceeding to the design of the 'line uncramper' itself, it is necessary to describe the salient features of the vertical and horizontal scanning systems in a typical monitor. The signal which is passed by your computer to the monitor is called 'composite video' and looks something like Figure 1 when displayed on an oscilloscope. The signal is 'composed' of three separate sets of information added together. They are: the actual picture information which tells where white dots are to appear on a line; the horizontal synchronising pulses which identify the beginning of a line and tell the monitor to start a new line at the left side of the screen; and the vertical synchronising pulses which tell the monitor to start a new frame at the top of the screen. What happens to these signals is shown in Figure 2.

The electron beam inside the picture tube is scanned from side to side and from top to bottom by two sets of electromagnets, called the horizontal and vertical 'yokes' respectively. An electromagnet deflects the electron beam away from the centre of the screen by a distance which is more or less proportional to the amount of current flowing through the magnet coil. Thus it is not surprising that in order to provide a smooth sweep rate over the screen followed by a rapid retrace to the starting position, the current through the coils in both horizontal and vertical cases is a sawtooth wave shape, as Figure 2 shows. ▶



... this screen display. Letters on adjacent rows no longer touch, and a screenful of text (only a small area is shown here) becomes far more easily readable.

Lab Notes

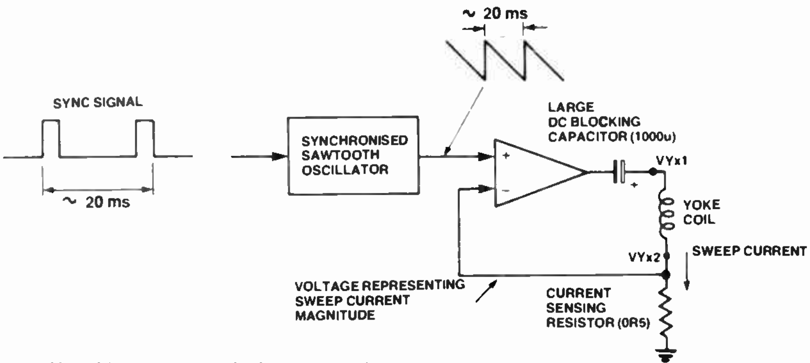


Figure 3: **Simplified look at vertical sweep section.**

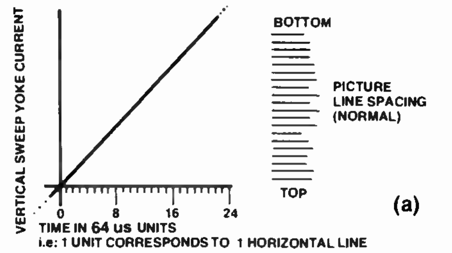


Figure 4a: **Graph showing the vertical yoke current during a portion of the sweep. Beside the graph is a representation of the spacing of the scan lines with this normal (unmodified) sweep current.**

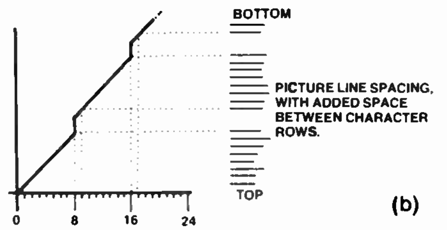


Figure 4b: **Graph shows the effect of adding a step of current after each character row. Note the spaces in the scan lines.**

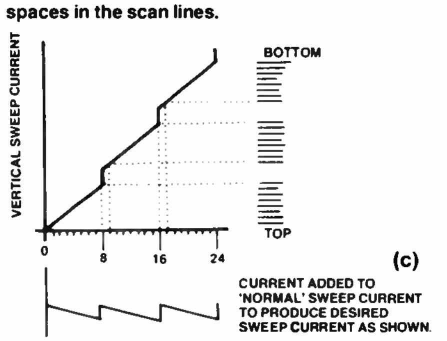


Figure 4c: **In this graph the scan lines for each character row are vertically squeezed together to obtain a space between rows. The current to be added to the normal yoke current is shown beneath.**

A more detailed look at the vertical sweep section is provided by Figure 3. The synchronising signal controls the frequency of the sawtooth oscillator. The sawtooth voltage is amplified, then applied across the vertical yoke coil. The output from the amplifier is a sawtooth-like waveform which varies between, say, 1 V and 7 V. However, the yoke must conduct both positive and negative currents in order to deflect the electron beam up and down to cover top and bottom of the screen. The vertical amplifier cannot generate a waveform with both positive and negative voltages, since it is supplied with only a 'single-sided' positive power supply. Hence a large dc blocking capacitor is inserted so that the voltage applied to the yoke averages out to zero and thus must have both positive and negative parts, say −3 V to +3 V.

A small-value resistor (typically half an ohm) does little to reduce the sweep current through the yoke to ground. Instead, the small voltage generated across it is used as a measure of the yoke current, and is fed back to the negative input of the sweep amplifier. Here it is compared to the intended sawtooth, and any correction is made. The result is that a sawtooth *current* is supplied through the yoke, and a sawtooth *voltage* may be observed at the 'top' of the current-sensing resistor. However, the voltage waveform observed at the top of the yoke (output from the capacitor) is a somewhat distorted sawtooth because the yoke coil has inductance.

This is a simplified description of how the vertical sweep section works, but it points out the three components (yoke, dc blocking capacitor and current-sensing resistor) which are important to the line uncramper. If you are contemplating modifying your monitor then you must be able to locate these three components both inside the monitor and on the monitor circuit diagram.

Sweep modifying

Having recognised that the deflection of the electron beam (and hence the spacing of the scan lines on the screen) is controlled by the current flowing through the yoke, it is straightforward to conclude that we could add a little bit of extra space between the bottom of one row of characters and the top of the next row by somehow altering the yoke current at the appropriate instant.

Figure 4a shows a graph of normal vertical sweep current during a portion of a frame (about 20 lines' worth), and the relative spacing of the picture lines. It would be possible to add current in steps after each character row, as shown in Figure 4b (one character row here is shown as consisting of eight lines, as would be the case for the Sorcerer). This would provide the desired space between character rows; however, all the additional spaces would add to the total picture height, possibly making the picture too high for the screen even with the monitor's picture height adjustment set to minimum. In any case this arrangement would require readjustment of picture height when switching between graphics and text modes.

The basic solution lies in Figure 4c. Here, each set of eight lines belonging to one row of characters is vertically squeezed together. This makes the characters less tall, the skrinkage leaving the desired space between character rows. Figure 4c also shows the waveform of the basic current to be added to the normal yoke current to achieve this result.

The circuitry

Now the actual line uncramper circuitry can be discussed. The circuitry has been broken into sections so that the function of each can be clearly understood, and so that, where necessary, modifications can be made simply. Figures 5 to 11 show these circuit modules.

The line uncramper needs to be supplied with power. This can most readily be obtained from the monitor itself, as shown by Figure 5. Needless to say, it is assumed that the monitor or TV set in question is a transistor or IC type and has such voltages available. (Modification of valve type monitors is not recommended, both from safety and practicality viewpoints.) The 'power supply' circuitry filters the supplied voltage so that any noise on the monitor's supply line will not interfere with the line uncramper, and perhaps more importantly, vice-versa. The voltage supplied to the line uncramper can be anywhere between 9 V and 15 V; the components are not very fussy.

Horizontal and vertical signals

The line uncramper needs to be informed of the start of each horizontal line (so it can count them) and the start

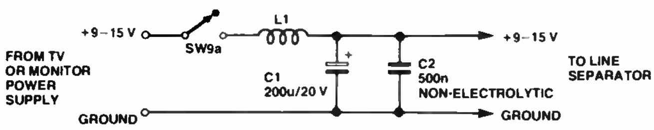


Figure 5: **Schematic of 'power supply' for Line Uncramper.**

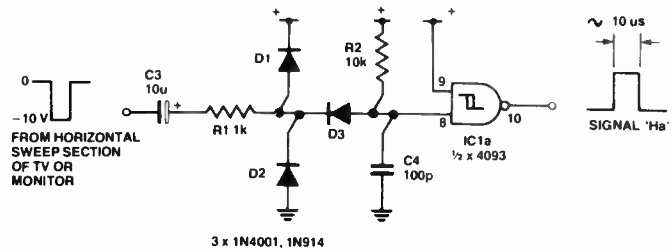


Figure 6: **This circuit is the horizontal pulse conditioner, taking a signal from the monitor and producing a well-defined pulse at the beginning of a scan line for the subsequent circuitry to use.**

of each picture frame (so it can properly register the spaces between character rows). To facilitate this, signals are taken from the horizontal and vertical sections and conditioned into nice pulses for use by the rest of the circuitry. This job is done by the circuits shown in Figures 6 and 7. In the TV set which the author modified, a 0 V to −10 V pulse was found in the horizontal sweep section. The horizontal pulse conditioner converts this first to a +10 V-to-0 V pulse (components C3, R1, D1, D2) then generates a 10 us pulse on the falling edge of the input pulse (D3, R2, C4) which is inverted and squared up by IC1a. (Note the use of Schmitt trigger-type gates. These give more 'positive' switching action, which is important when attempting to change relatively slowly varying signals into digital pulses. Although the 4093 is shown, any CMOS Schmitt inverters will do).

The vertical signal used was taken from the yoke (point VYx1 on Figure 3). This signal is less 'nice' than the horizontal signal used, and its pulse conditioner consequently is fancier. The waveform is a sort of sawtooth with a pulse on top of each peak, and it measures 1 V to 7 V. This is 'floated' by C5, and the average voltage adjusted by RV1 and R3 (i.e: the signal is moved up or down) so that the signal which feeds into IC1b produces a stable and reliable pulse at IC1b's output, as shown. This pulse triggers a pulse generater (C6, D6, R6, RV2 and IC1c) whose output pulse width is 60 us ±30 us approximately. (Pulse width adjusted by RV2.)

This gives us two nice pulses indicating the start of the horizontal and vertical sweeps. It is quite likely that the signals available in your monitor or TV will differ from the ones shown here; you will have to try to find signals that you can use either by studying the monitor circuit or prodding around with an oscilloscope. The techniques shown in Figures 6 and 7 are quite generally applicable and should be useful in most cases. In any event, your input signal conditioners should provide the same kind of pulses for the subsequent circuitry to work with. ▶

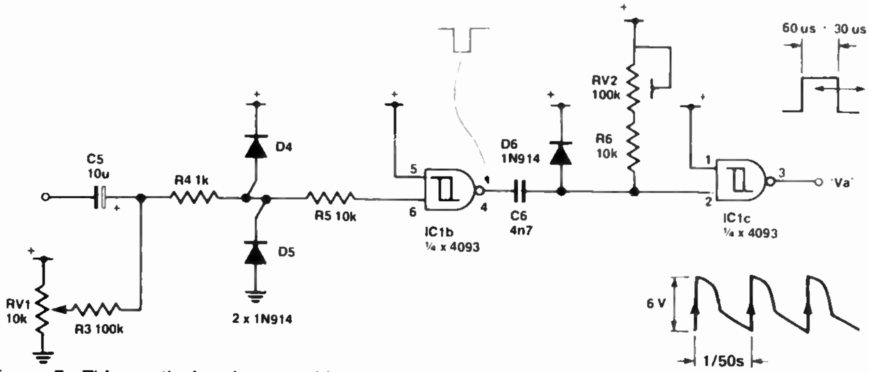
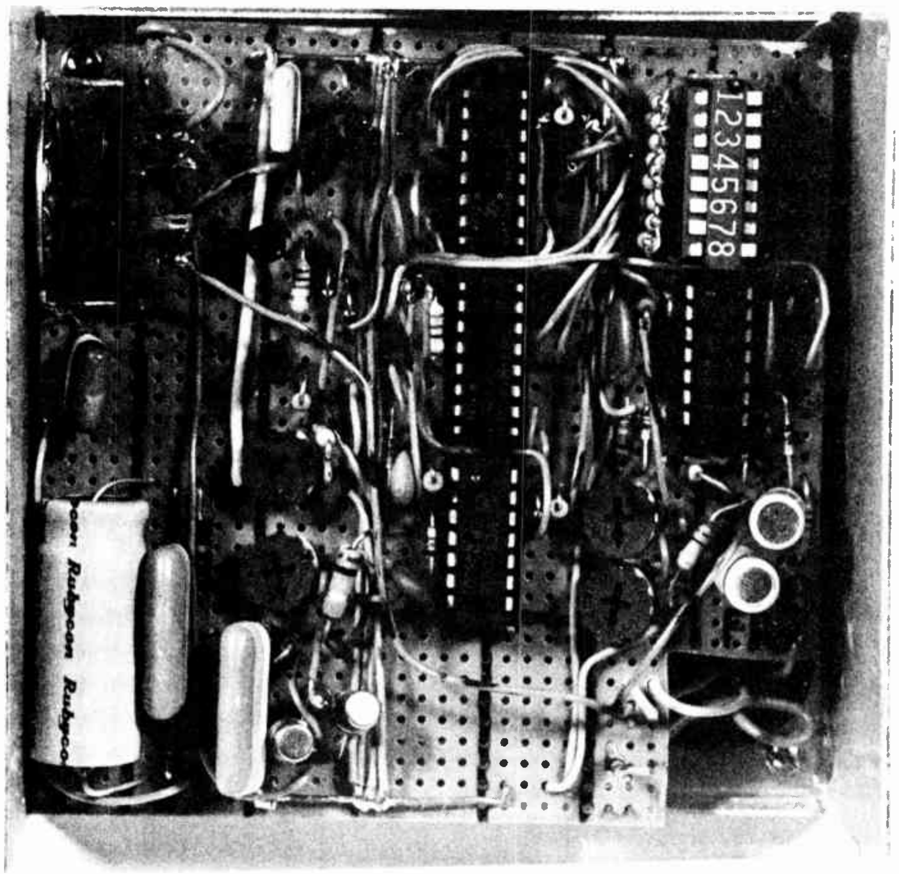


Figure 7: **This vertical pulse conditioner performs an analogous function on the vertical signal to the circuitry in Figure 6.**



The Line Uncramper fits neatly into a small metal box attached to the side of the TV set/monitor. The circuit board is supported by the rotary switch only. Connections to the TV set pass through a hole behind the board through the box and TV set cabinet walls.

This short pulse, 'T', serves both as the signal to put a space in the display scan, and also presets IC4 again ready to count the lines in the next character row.

The remaining circuitry is triggered by pulse 'T' to provide the required current to the yoke. First, some words about current sources and sinks, and about how to supply current to the yoke.

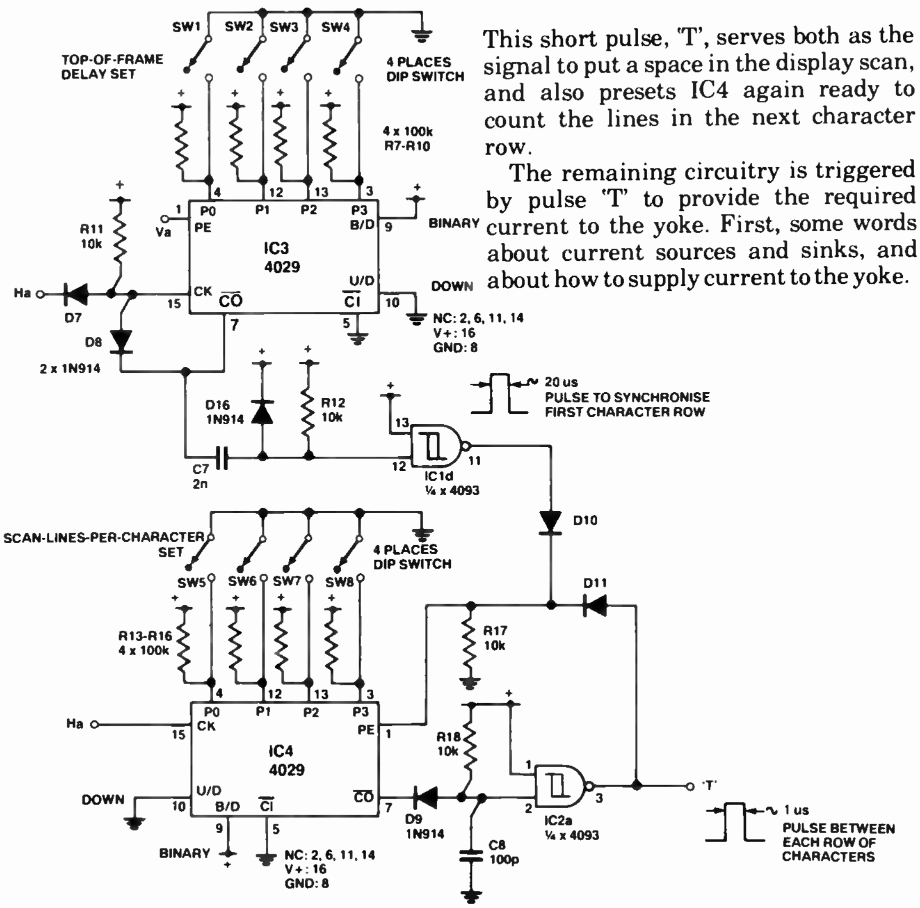


Figure 8: **The timing circuitry is the real heart of the Line Uncramper. It determines where the first space will appear on the screen, and the number of scan lines between subsequent spaces.**

Timing

The purpose of the section shown in Figure 8 is to generate a pulse which indicates that a space is to be made in the screen scanning. It therefore must determine where the first space must occur, and then must repeatedly signal a space after the bottom of each character row. Counter IC3 handles the first part of this task. The pulse from the vertical signal conditioner, 'Va', loads this counter with the number set on DIP switches SW1 to 4. The counter is set up to count in binary, and to count downwards, and it counts the horizontal pulses 'Ha'. When it counts down to zero its 'carry' output synchronises the second counter IC4 by presetting it (via pulse generator C7-D16-R12-IC1d, and then D10) with the value on DIP switches SW5 to 8. This value is the number of lines in a character, which for the Sorcerer is eight or 1000 binary (SW8 open, SW7 to 5 all closed). IC4 also counts downward, and each time it reaches zero its 'carry' output triggers a pulse generator (D9, R18, C8, IC2a).

Current sinks

Some current sources and sinks are shown in Figure 11. In each case the collector lead (marked 'c'), if connected to some other circuit, is able to supply (source) or draw away (sink) a predetermined amount of current, *without* affecting the voltage present on that other circuit (within limits). In Figure 11a, for example, the current drawn away is labelled Ic (collector current). For our approximate purposes, Ic is the same as Ie. Ie in turn is determined by Ohm's Law to be the voltage across resistor R, divided by R. The voltage across R is Vb, less the fixed base-emitter voltage of 0.6 V. Consequently, by setting Vb we can determine Ic. As a formula:

$$Ic = (Vb - 0.6)/R$$

The formula for Figure 11b is the same, while those for Figures 11c and d are similar except that there are two base-emitter voltages, and hence the formula is:

$$Ic = (Vb - 1.2)/R$$

(These circuits, of course, only work for positive values of Ic.

The advantage of the two-transistor design is simply that about 50 to 100 times less base current (Ib) is required to operate it. The limit within which these circuits must operate is that the voltage on the circuit to which the current sink or source is connected must allow at least a certain minimum voltage from collector to ground (11a and 11c) or from collector to the positive supply V+ (11b and 11d). This minimum is Vb−0.4 V approximately.

Uncramper outputs

Now, looking back to Figure 3, what we are attempting to do is to add to, or subtract from, the current flowing in the yoke. Increasing the current through the yoke can be done by feeding more current into point VYx1, or drawing more current away from VYx2. In the first case a current source would be attached to VYx1, while in the second a current sink would be attached to VYx2. The second of these two is not feasible since the small voltage across the current-sensing resistor is insufficient for a current sink to operate.

To reduce the current through the yoke, a current sink may be attached to VYx1, or a current source attached to VYx2. (It may be thought that where the current added or subtracted affects the voltage across the current-sensing resistor, the negative feedback would cause the vertical amplifier to 'correct' for the difference and cancel the desired addition or subtraction. This does not happen because in fact the amount added or subtracted is relatively small, and the indicated feedback loop is not the only feedback path.)

The basic sawtooth current to be added to the yoke is generated by the circuit of Figure 9. Here, the pulse 'T' turns on Q1 and Q2 for a short time. Q2 forces the voltage across C9 to about 2 V. When Q2 turns off, C9 slowly charges via R21 and RV3. The repetition of these events results in a sawtooth waveform at the base of Q3, the height of which is adjusted by RV3. This sawtooth voltage controls a current source (Q3, Q4, R22) which supplies a sawtooth current to the yoke.

That *should* finish the job. Unfortunately, the sawtooth current source is not able to force the drop in current at the end of each tooth to occur fast enough, due to the slowing effect of the yoke's inductance. The result is that the space which should occur *between* scan

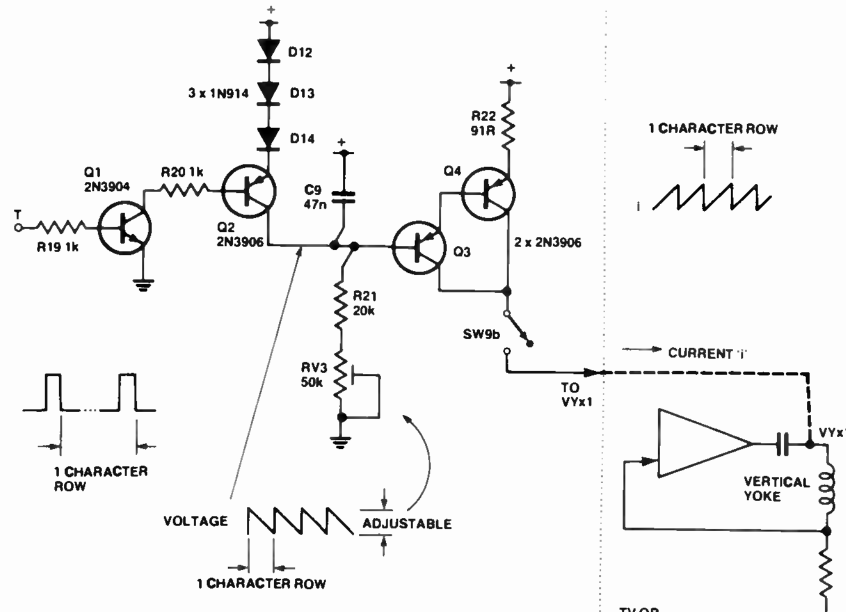
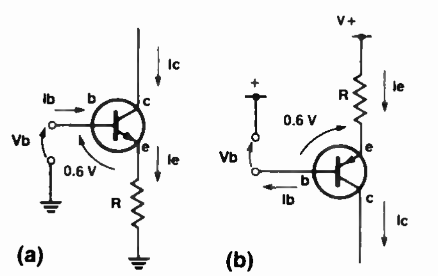
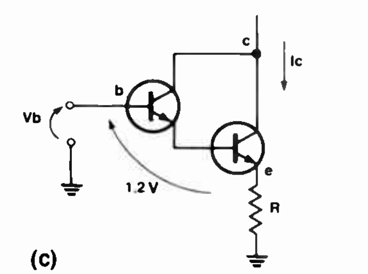


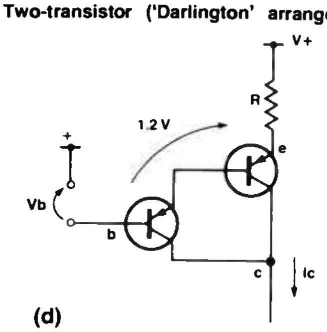
Figure 9: **A sawtooth current is generated by this circuit, which feeds the vertical yoke and causes the vertical squeezing of the scan lines belonging to one character row.**



11a: **NPN current sink.** *11b:* **PNP current source.**



11c: **Two-transistor ('Darlington' arrangement)**



11d: **Darlington current source.**

Figure 11: **Circuitry for current sources and sinks.**

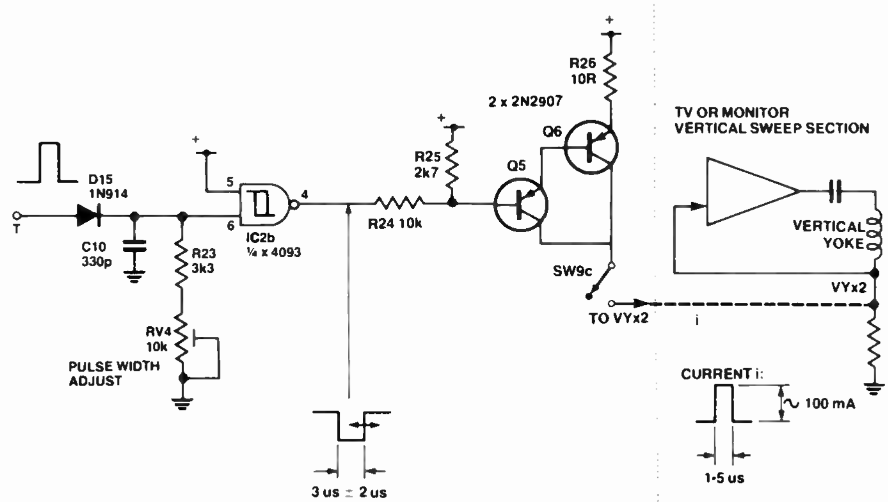


Figure 10: **This circuit sends a pulse to the yoke to make the between-row step in the scan occur sharply.**

lines (in about 5 us or less) actually takes so long (about 50 us) that the top scan line of each character row is on an angle, the left end joined to the upper row of characters, and the right end finally dropped down to join with the lower row of characters. What is needed is to give the yoke a swift kick to cause the step in the vertical sweep to occur smartly. This function is performed by the circuitry of Figure 10.

Pulse 'T' is 'stretched' by D15-C10-R23-RV4 and produces a pulse at the output of IC2b which is 3 us ±2 us long. This pulse is applied to a current source (R24, R25, Q5, Q6), which supplies a pulse of current to VYx2, sharply reducing the voltage across the yoke for a few microseconds.

Switch SW9a-b-c turns on the power to the uncramper, and connects the two current sources to the monitor.

Construction

Any construction method which you have found satisfactory for digital circuitry should be appropriate for the line uncramper. The author's prototype was constructed on Veroboard and mounted in a small metal box attached to the side of the TV set/monitor. Rotary switch SW9 is mounted on the front of the box, and supports the circuit board. Wires into the TV pass through a hole drilled through the box and TV walls.

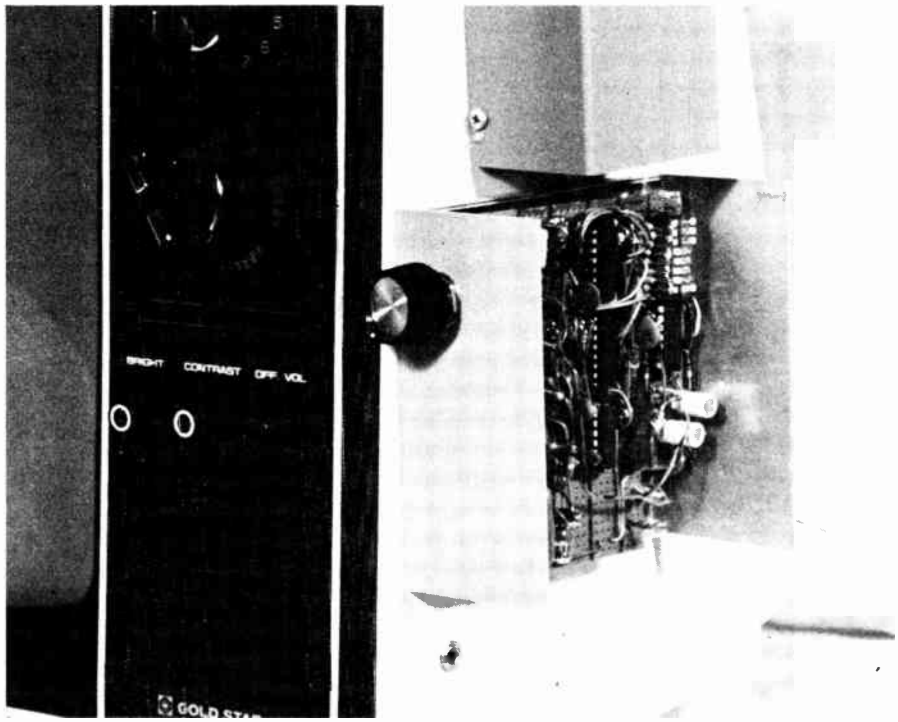
Adjustment

An oscilloscope will probably already have been needed to find the necessary horizontal and vertical signals in the monitor, and will be required now for setting up the uncramper. First set all trimmer potentiometers for the middle of their ranges. Then power up the modified monitor and quickly ensure that the supply voltages on the uncramper are as supposed to be, and that nothing is getting extremely hot, etc. With your computer connected to the monitor, the horizontal and vertical pulse conditioners should be adjusted and verified for proper operation. (It is probably a good idea not to connect the two current sources to the monitor until this stage is reached and the generally satisfactory operation of the uncramper has been checked with the 'scope.)

Next, DIP switches SW5 to 8 can be set for the appropriate number of scan lines per character row. The display ▶

PARTS LIST

Resistors	**all 5%, 1/8 W or greater unless noted**
R1, R4, R19, R20	1k
R2, R5, R6, R11, R12, R17, R18, R24	10k
R3, R7-10, R13-16	100k
R21	20k
R22	91R
R23	3k3
R25	2k7
R26	10R 1/4 W
Trimpots	**all linear, miniature, multiturn units are desirable but not necessary.**
RV1, RV4	10k
RV2	100k
RV3	50k
Capacitors	
C1	200u or greater/20V electrolytic
C2	500n non-electrolytic
C3, C5	10u/25 V electrolytic
C4, C8	100p
C6	4n7
C7	2n2
C9	47n
C10	330p
Inductor	
L1	1 mH or greater RF choke
Semiconductors	
D1-D16	1N914 or similar silicon signal diode
Q1	2N3904, BC107, BC547
Q2, Q3, Q4	2N3906, 2N5139, 2N3250
Q5, Q6	2N2907, 2N3645, 2N4143
IC1, IC2	4093
IC3, IC4	4029
Switches	
SW1-8	8-section DIP switch
SW9	3-pole 2-position



The Uncramper switch is positioned in a convenient location for operation alongside the TV set's controls. The upper box attached to the set is the monitor input circuit, allowing the TV set to use the computer video signal directly.

should be looking somewhat reasonable, with horizontal black spaces appearing in the picture. (Increase the brightness so that you can see what the scan lines are doing.) Now switches SW1 to 4 can be changed until the black lines are between rows of characters. Finally, RV3 and RV4 must be alternately adjusted to provide the desired amount of space and proper vertical stepping respectively.

The line uncramper should provide you with a video monitor which is easier to read, and a computer system which is more enjoyable to use. It is a device which may not be necessary with future generations of computers, but in the meantime you can save your eyes . . . and perhaps some enterprising company would like to pick up the idea and provide uncramper kits for the more popular monitors? ●

Lab Notes

Super timer — from μs to days

Timing long periods has always been a problem because of the high leakage characteristics of the timing capacitor. This is no longer true! The XR-2240 IC is a programmable timer capable of producing ultra-long time delays without sacrificing accuracy.

Barry Davis

THIS IC can generate time delays from microseconds up to five days, and with a little ingenuity can generate a delay of a couple of years! A functional block diagram of the IC is shown in Figure 1.

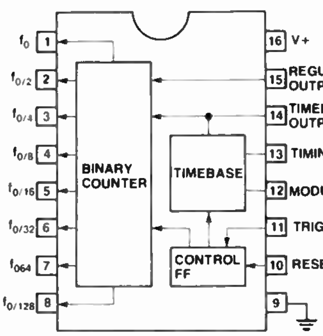


Figure 1. **Functional block diagram of the XR-2240.**

The circuit consists of an internal timebase generator, a programmable 8-bit counter and a control flip-flop. The time delay at the output is set by an external CR network and can be any period from 1.CR to 255.CR. Herein lies the secret. The CR timebase generator can be set to give a very accurate short period, and binary multiples of this short period are then programmed and taken from the output. Each output is capable of sinking approximately 5 mA of load current.

The features of the IC are:

1. Timing from microseconds to days.
2. Programmable delays: 1.CR to 255.CR
3. Wide supply voltage range: 4 V to 15 V
4. TTL compatible inputs and outputs
5. High accuracy: 0.5%
6. Excellent temperature stability
7. Period T = C x R

Circuit operation

The timing cycle is initiated by a positive-going pulse on pin 11. This trigger pulse performs three functions:

1. Activates the timebase generator
2. Enables the counter
3. Sets all counter outputs to the *low* state

The timebase generator produces timing pulses with a period, T, equal to 1.CR. These clock pulses are counted by the binary counter inside the IC and the timing period is complete when a positive-going pulse is applied to pin 10 (i.e: the circuit is reset). In most applications one or more of the output terminals are connected back to the reset input. The circuit will commence timing when the trigger pulse is applied, and automatically reset on the completion of the timing period.

Remember, the outputs are normally high and are set to low when timing is initiated, returning again to the high level on completion of the timing period.

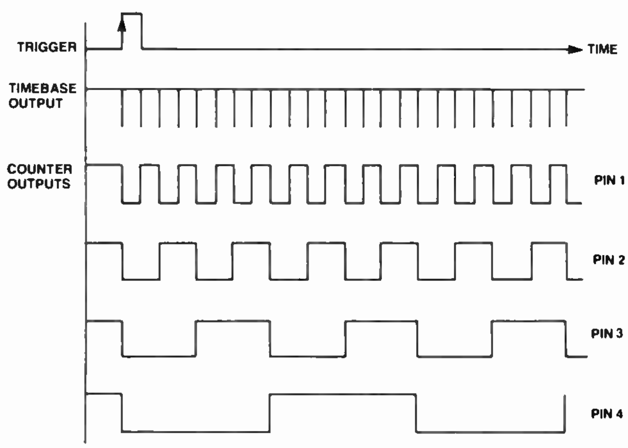


Figure 2. **Output waveforms and timing diagram.**

Lab Notes

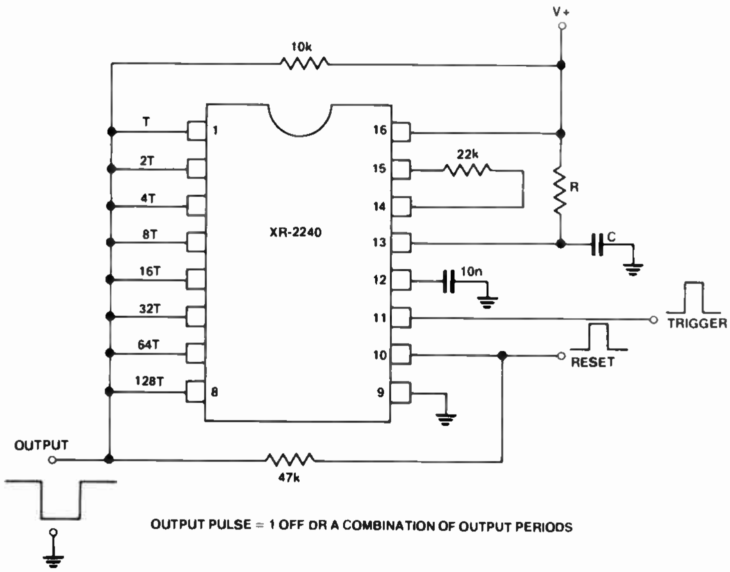


Figure 3. **Connections for a practical circuit.**

Circuit construction

The binary outputs, pins 1 to 8, are open collector and can be connected together to a common pull-up resistor. The output of the timer will be low as long as any one output is low. In this manner the time delays associated with each output can be added by simply connecting them together to a common bus. The outputs can be used individually or wired together.

For example, the output at pin 4 is 8 x CR = 8T. If pins 4 and 3 are connected together the output will become 12 x CR = 12T.

Figure 3 shows the actual connections for a practical circuit. When the power is applied, with no trigger or reset inputs, the circuit sets up to the initial state of all outputs high. Once triggered, the circuit is totally immune to any additional trigger inputs until the timing period is completed, or a reset pulse is applied.

Choice of timing components

Once a signal timing period, T, is established, the output can be determined by 'wiring-in' periods of T following a binary progression. However, the procedure may have to be reversed when a certain accurate output period is required.

For example, if a timing period of 6 hours 30 seconds is required, firstly convert the time to seconds:

$$= 6 \times 60 \times 60 + 30$$
$$= 21630 \text{ seconds.}$$

The maximum number of timing periods available with one IC is $(1+2+4+8+16+32+64+128)T = 255\,T$. Therefore the period of T can be calculated:

$$T = \frac{21630}{255}$$
$$= 84.82 \text{ seconds}$$

With a low-loss capacitor (such as tantalum) as one timing component, R can be calculated. If C = 100 uF:

$$T = CR$$

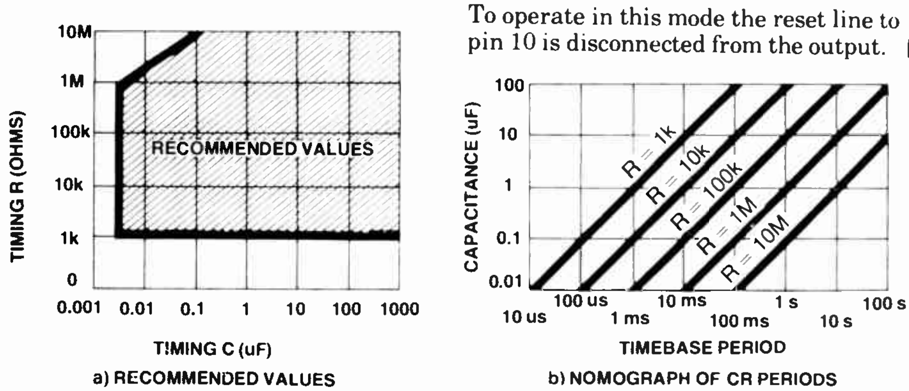


Figure 4. **Graphs to assist in the choice of values of C and R.**

Therefore:

$$R = \frac{T}{C}$$
$$= \frac{84.82}{100 \times 10^{-6}}$$
$$= 848.24\,k\Omega$$

This can be tailored precisely for very accurate timing with a resistive network or potentiometer, or simply rounded off to 850k.

Figure 4 shows two graphs which will assist you in choosing:

1. The recommended range of timing component values.
2. The time period, (T) up to 100 seconds, to be expected from combinations of C and R values.

An example of output periods to be expected using a 100 uF capacitor (tantalum) and 1M resistor as the timing components is shown in Table 1.

T = CR = 100 μF x 1 M = 100 seconds	Period of Output
T	100 secs = 1.7 min
2T	200 secs = 3.3 min
4T	400 secs = 6.7 min
8T	800 secs = 13.3 min
16T	1600 secs = 26.7 min
32T	3200 secs = 53.3 min
64T	6400 secs = 1.8 hours
128T	12800 secs = 3.6 hours
255T	25500 secs = 7.1 hours

Table 1. Example of accurate time available using the XR-2240.

The type of circuit operation discussed to this point has been monostable i.e: the output goes low on triggering, stays low for the timing period and returns to a high level. It will not time again until it is retriggered. An XR-2240 can also be used in a free-running or astable mode.

Astable operation

To operate in this mode the reset line to pin 10 is disconnected from the output. ▶

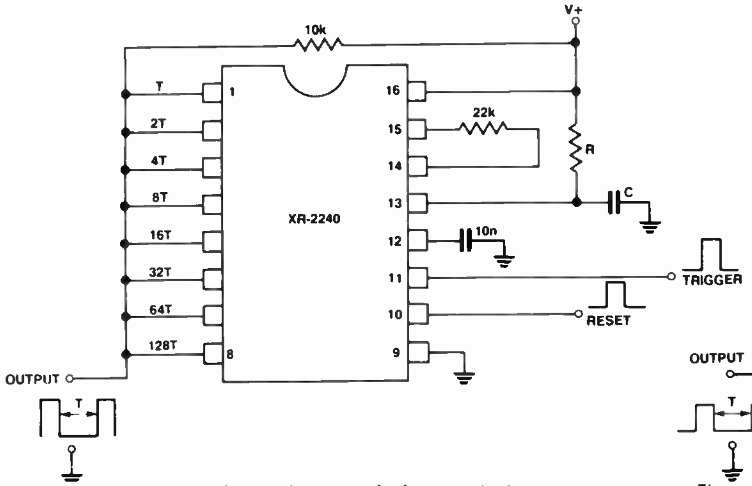


Figure 5. **Astable operation under control of external trigger and reset controls.**

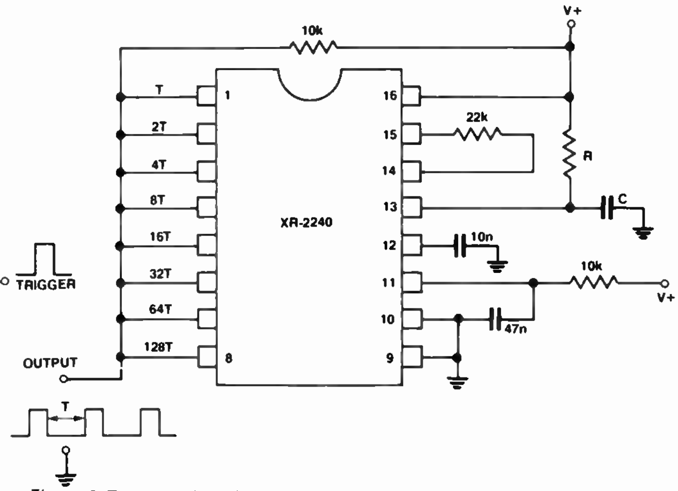


Figure 6. **Free-running circuit.**

Figure 5 shows an astable circuit under the control of the external trigger and reset signals. It will start timing when an external trigger pulse is applied, and will not stop until a reset pulse is applied.

Alternatively, the circuit can be made truly free running. The circuit in Figure 6 self-triggers automatically when the power is switched on, and continues to operate in its free running mode indefinitely.

When the timer is used in this mode, each counter output can be used individually as synchronised oscillators, or they can be connected together to provide complex pulse patterns.

Ultra-long delays

In some applications delays of four days may be required. This is particularly useful in electronic farming for controlling the rate of supplementary feeding. The timing components required can be calculated thus:

4 days = 96 hours
= 5760 minutes
= 345 600 secs.

Maximum number of T combinations = 255

Therefore

$$T = \frac{345600}{255}$$

= 1355.3 secs

= 22.6 minutes

Incidentally, 20 minutes is about the longest time recommended for 1.CR as anything beyond this suffers from leakage problems.

$$T = CR$$

if $C = 500$ uF (low leakage)

$$R = \frac{T}{C}$$

$$= \frac{1355.3}{500 \times 10^{-6}}$$

= 2M7

Two XR-2240 ICs can be cascaded to generate extremely long time delays. When used in this format the reset and trigger terminals of the ICs are tied together and the timebase of unit 2 disabled as shown in Figure 7.

The output is normally high. When a positive-going trigger pulse is applied the output goes low and stays in the low state for $(256)^2 = 65\,536$ periods of the timebase oscillator. Therefore the total timing period of two cascaded units can be from 256.CR to 65 536.CR. The output is available in 256 discrete steps by selectively connecting one or a combination of the outputs from unit 2 to the output bus.

With T = 20 minutes an example of an ultra-long delay can be given.

CR = T = 20 mins.

65 536T = 1 310 720 min
= 21 845 hours
= 910 days
= 2.5 years!

This article highlights the use of an XR-2240 as a precision timer. Other application suggestions are:

1. Sequential timing
2. Binary pattern generation
3. Frequency synthesis
4. Pulse counting or summing
5. A/D conversion
6. Digital sample and hold

Further information on the IC can be obtained from Exar Integrated Systems or their agents (Total Electronics).

This article was made possible by the courtesy of Exar Integrated Systems. Data was taken from their publication 'XR-2240/2340 Programmable Timer Counter'. ●

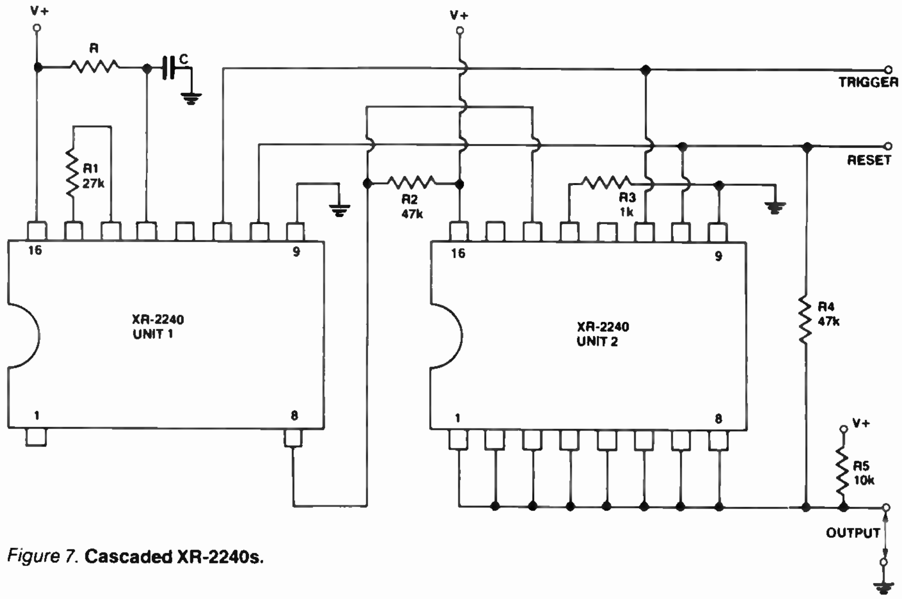


Figure 7. **Cascaded XR-2240s.**

Audio amplifiers using nested differentiating feedback loops

Part 1 — The present state of the art

The use of nested differentiating feedback loops (NDFLs) is a new technique for reducing audible-frequency distortion in an amplifier to a vanishingly low level. As the name implies, NDFLs rely on negative feedback, but they use it in a new way.

Edward M. Cherry
Associate Professor
Department of Electrical Engineering
Monash University

IN ORDER TO UNDERSTAND just how far the new NDFL technique can improve an amplifier, we first need to know the fundamental limits to the reduction of distortion that can be achieved with conventional techniques. In this first of three articles we survey familiar negative-feedback theory.

Figure 1 is a block diagram of an amplifier with negative feedback. In this diagram, the forward path corresponds to the amplifier before feedback is applied, and its gain is traditionally designated by the Greek letter μ. The feedback network returns a fraction β of the output to the input circuit, where it is in some way subtracted from the true input to provide the actual input to the forward path.

In many practical amplifiers, the subtraction is accomplished by applying the input and feedback signals to the two inputs of a balanced differential first stage of the forward path. Figure 2 is an outline practical circuit. In this circuit the feedback factor β is the attenuation of the network comprising R_{F1} and R_{F2}

$$\beta = \frac{R_{F1}}{R_{F1} + R_{F2}} . \qquad (1)$$

A typical value for an audio power amplifier might be 1/20. The forward-path gain μ in Figure 2 corresponds to gain from input to output when the feedback network is removed. A typical value for a simple audio power amplifier might be 1000.

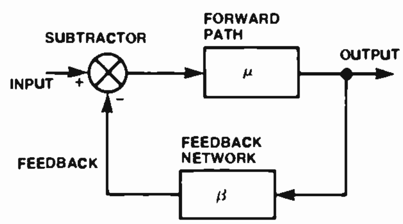


Figure 1. **Block diagram of a feedback amplifier.**

For Figure 1, the overall closed-loop gain A is given precisely by

$$A = \frac{\text{Output}}{\text{Input}} = \frac{\mu}{1 + \mu\beta} . \qquad (2)$$

The quantity $\mu\beta$ is called the loop gain. Physically, loop gain is the gain that would be observed if the feedback 'loop' in Figure 1 was cut at some point, a signal was injected into one side of the cut, and the resulting signal at the other side of the cut was measured.

If the values of μ and β are such that loop gain is small compared with unity, the closed-loop gain is very nearly equal to the forward-path gain (that is, the gain without feedback)

$$A \underset{\mu\beta \ll 1}{\longrightarrow} \mu . \qquad (3)$$

However, if loop gain is large compared with unity, the closed-loop gain approaches the reciprocal of the feedback factor and becomes almost independent of the forward-path gain

$$A \underset{\mu\beta \gg 1}{\longrightarrow} 1/\beta . \qquad (4)$$

The quantity $1/\beta$ is often called the demanded gain, as it is the value the overall closed-loop gain would take in ideal circumstances.

As a numerical example, if we substitute the above values $\mu = 1000$ and $\beta = 1/20$ into Equation 2, the gain of our 'typical' audio power amplifier works out as $A = 19.6$. The approximate Equation 4 predicts $A \rightarrow 20$, within 2% of the correct answer.

The quantity $1 + \mu\beta$ occurs often in feedback theory. It is called the return difference F

$$F = 1 + \mu\beta . \qquad (5)$$

Physically, return difference has the significance

$$F = \frac{\text{forward-path gain}}{\text{closed-loop gain}} \qquad (6)$$

For values of loop gain greater than about 10, loop gain and return difference are almost equal — in our 'typical' example the values are 50 and 51 respectively.

Simplified treatments of feedback theory show that, if the distortion generated in the forward path (that is, the amplifier without feedback) at a particular output signal amplitude is D_μ, then the resulting closed-loop distortion D_A at the same output signal amplitude is

$$D_A = D_\mu / F . \qquad (7)$$

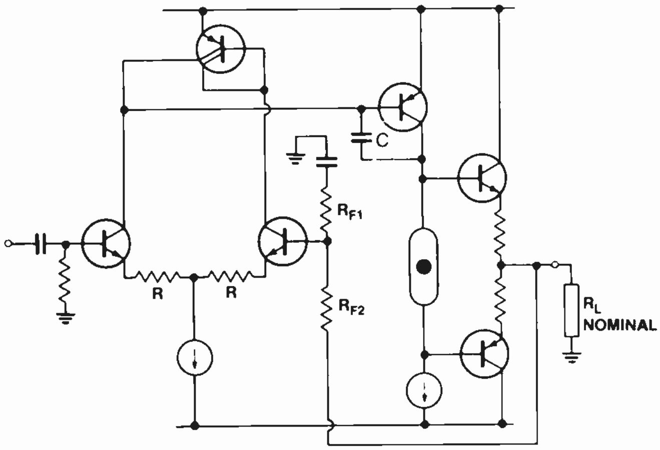


Figure 2. **Outline circuit of an audio power amplifier.**

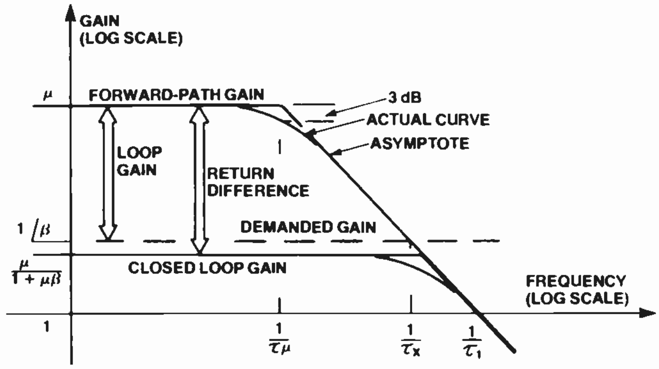


Figure 3. **Logarithmic plots of gain versus frequency for Figure 1.**

Distortion is improved when feedback is applied to an amplifier by a factor equal to the return difference. In our 'typical' amplifier, $F = 51$; if the distortion without feedback happened to be 10%, then feedback should reduce the distortion to 0.196%.

More rigorous treatments of feedback theory show that Equation 7 is no more than a poor approximation to the truth. In the first place, real amplifiers are far more complicated than Figure 1 suggests, because several different feedback paths (not all intentional!) can be identified. For example, the collector-base capacitances of transistors inevitably provide some unintended feedback at high frequencies. There is a very real problem in interpreting just what loop gain and return difference mean when there is more than one feedback loop. Once the correct interpretation is established, return difference invariably turns out to be a function of frequency, and the reduction of distortion corresponding to Equation 7 depends on the value of return difference at the frequency of the distortion, not the frequency of the input. Feedback therefore, does not reduce all distortion components equally.

Finally, it is found that the closed-loop distortion of an amplifier can contain new components that were not present in the distortion that existed in the forward path before feedback was applied. These new distortion components initially increase as loop gain is increased, but they fall away again towards zero as loop gain is made large.

Despite all these complications, the fact remains that adequate negative feedback, properly applied, does reduce distortion. Why, then, do amplifier designers not simply apply some arbitrarily large amount of feedback and reduce amplifier distortion to the vanishing point?

TIM, IIM, PIM, ...

In the last 10 years or so, readers of audio magazines have been made aware of a conjecture that goes something like this:

"Harmonic distortion and the usual intermodulation distortion decrease with increasing feedback. Transient intermodulation distortion (TIM) increases with increasing feedback, and is approximately directly proportional to the feedback. Therefore, there is an optimum value for the feedback at which the subjective distortion sensation is least. This optimum feedback is unlikely to exceed about 20 dB."

More recently, there has been conjecture that heavy overall feedback should be applied with caution if interface intermodulation distortion (IIM) is to be avoided. An amplifier should provide a low open-loop output impedance so that the need for feedback-generated loudspeaker damping is minimised.

There has also been conjecture that negative feedback, which reduces the usual intermodulation distortion, may increase phase intermodulation distortion (PIM) by converting amplitude nonlinearities into phase nonlinearities.

Unequivocally, none of these conjectures has any basis in the new NDFL amplifiers. As an aside, there is a substantial body of opinion that none of these conjectures has any basis, full stop; interested readers should refer to References 1 — 12.

Instability and oscillation

A fundamental limit to the amount of feedback that can be applied to an amplifier is set by the onset of instability and oscillation.

If the magnitudes of the forward-path gain and demanded gain of the idealised Figure 1 are plotted versus angular frequency ω (in radian/second) on logarithmic scales, the resulting graph looks something like Figure 3. The 3 dB bandwidth of the amplifier without feedback is $1/\tau_\mu$, and the gain-bandwidth product (at which gain drops to unity) is $1/\tau_1$.

Because the graph is on logarithmic scales, the separation between the curves of forward-path gain and demanded gain is the loop gain (remember that, to divide two numbers, you subtract their logarithms; if you divide μ by $1/\beta$, you get $\mu\beta$). The magnitude of loop gain falls to unity at the frequency $1/\tau_X$ where the curves intersect and their separation is zero (remember that the logarithm of unity is zero).

By a similar argument, return difference is the separation between the curves of forward-path gain and closed-loop gain, as indicated in Figure 3.

We could make a similar graph to Figure 3, showing the phases of μ and $1/\beta$. Again, the phase of loop gain would turn out to be the separation between the two curves. However, there is a remarkable piece of mathematics due to Bode, who used a transformation evolved by Hilbert (1862-1943), which shows that there is a relation between the magnitude and phase of the response of any linear system. Subject to some qualifications, our proposed graph of the phases is completely predictable from Figure 3 and contains no new information. Interested readers may refer to Chapter 14 of Bode's book (Reference 13), but are warned that it is anything but easy going!

As an example, many readers will know that, if the forward-path in Figures 1 and 3 has a high-frequency cut-off rate variously described as single pole, 20 dB/decade, or 6 dB/octave, then ▶

its phase shift is 45° at the 3 dB cut-off frequency $1/\tau_\mu$, and is asymptotic to 90° at very high frequencies.

In 1932, Nyquist applied a theorem which dates back to Cauchy (1789-1857) to derive the condition for a feedback amplifier to be stable and free from oscillation. If a polar plot is made of the magnitude and phase of return difference as frequency is varied, a vaguely 'snail-shaped' curve results. Such a polar plot is called a Nyquist diagram. Subject again to some qualifications, the stability criterion for a feedback amplifier is that its polar plot of return difference should not enclose the origin. Figure 4 shows one example each of a stable situation and an unstable situation.

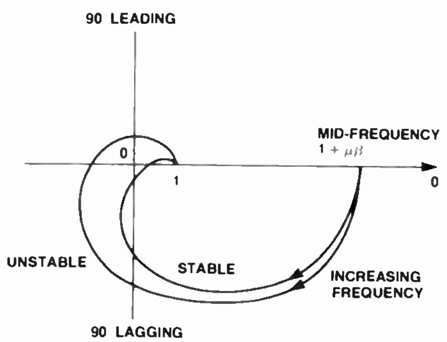


Figure 4 Nyquist's stability criterion. The curves are polar plots of return difference for changing frequency.

Because the phase of return difference can be predicted from Figure 3 via Bode's result a Nyquist diagram can also be constructed from Figure 3 and the onset of instability can be predicted. In 1945 Bode showed that Nyquist's criterion could in fact be expressed in terms of the gradients of the curves in Figure 3, thereby eliminating the work of finding the phase explicity and plotting the Nyquist diagram. Bode's exact rule is complicated, but a useful paraphrase is

> "If in graphs such as Figure 3 the separation between the forward-path gain and demanded gain decreases toward zero at a rate not exceeding 30 dB/decade, the amplifier is unlikely to oscillate."

This paraphrase makes no allowance for the tolerances on components. It assumes, in effect, that everything about the forward path is well known and constant. In the audio context, the paraphrase takes no cognizance of the fact that the capacitance of the leads that connect an amplifier and loudspeaker is anything but well known. A more conservative rule, applicable to the audio context, is therefore

> "In graphs such as Figure 3, the separation between the forward-path gain and demanded gain should not decrease towards zero at a rate exceeding 20 dB/decade."

The practical consequence is that the forward path of an audio amplifier with conventional resistive feedback should have a single dominant pole which sets the fall-off of gain at frequencies above $1/\tau_\mu$. The second and subsequent poles should all lie at frequencies substantially above $1/\tau_X$ (the frequency where the separation reaches zero), because each pole contributes a 20 db/decade downwards slope to the graph of forward-path gain.

Maximum available feedback

In Figure 2, the first stage is a long-tailed pair with a current mirror at its output; the input and feedback signals are applied to the two bases to perform the subtraction process of Figure 1. The second stage provides a large voltage gain, and the lag compensating capacitor C provides the dominant pole of the forward path corresponding to $1/\tau_\mu$ in Figure 3. The third stage is a complementary class-B emitter follower whose function is to transfer the output voltage from the second stage to the loudspeaker load. In practice, the transistors in the second and third stages are often Darlingtons, and the input transistors are often replaced by FETs.

In any amplifier, there is at least one pole associated with the finite transit time of electrons through each transistor. The transit time for typical small-signal transistors is a fraction of a nanosecond, but for power transistors of the ubiquitous 2N3055 class the transit time may be as long as a few tenths of a microsecond. Thus, the output stage of Figure 2 may have a pole in the vicinity of 1 MHz.

As we saw in the previous section, the unity-loop-gain frequency $1/\tau_X$ in Figure 3 must be substantially less than the frequency of all poles except the dominant pole $1/\tau_\mu$ if an amplifier is to be stable. If the power transistors are of the 3055 class then, no matter how fast the other transistors may be, there is going to be one pole at about 1 MHz. Therefore, $1/\tau_X$ must be chosen to correspond to something like 200 kHz. Even with more modern power transistors, $1/\tau_X$ is restricted to about 1 MHz. The art of designing a stable power amplifier involves choosing the lag compensating capacitor C such that $1/\tau_X$ is appropriate to the transistors actually used.

The geometry of Figure 3 is such that, no matter how μ, β and τ_μ are separately chosen, the return difference $F(\omega)$ at any angular frequency ω cannot exceed

$$F(\omega) \leq 1/\omega\tau_X \,. \qquad (8)$$

Thus, if $1/\tau_X$ is designed to correspond to 200 kHz, return difference at 20 kHz cannot exceed 10 (= 20 dB), and cannot exceed 200 (= 46 dB) at 1 kHz. An amplifier that boasts 80 dB of feedback (F = 10 000 at low frequencies) must have $1/\tau_\mu$ corresponding to about 20 Hz; return difference must begin falling above 20 Hz, and the former values at 1 kHz and 20 kHz (46 dB and 20 dB) still apply.

Returning now to Equation 7, the effectiveness of feedback in reducing distortion is set by the frequency of the distortion, not the frequency of the input. The audible frequency range is generally reckoned to extend to about 20 kHz and, with the foregoing constraints, return difference at this frequency cannot exceed 10. Remembering that 20 kHz is the third harmonic of 6.667 kHz, we see that feedback cannot reduce offensive odd-harmonic distortion of mid-treble input signals by more than a factor of 10. Remembering too that 20 kHz is the seventh harmonic of 2.857 kHz, we see that feedback cannot reduce crossover distortion of mid-range input signals by more than a factor of 10.

Until recently there has been no way around this problem except to increase the unity-loop-gain frequency $1/\tau_X$, and this demands that the frequencies of the transistor poles must be increased if stability is to be preserved. Fragile, expensive power transistors, with narrow bases to achieve short transit times, become mandatory. ●

(continued on page 74)

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Audio amplifiers using nested differentiating feedback loops

Part 2 — The basic idea

Edward M. Cherry
Associate Professor
Department of Electrical Engineering
Monash University

Here we get to see how this technique is applied to an amplifier and the effect it has on performance under differing conditions.

PREVIOUSLY we saw that, for a feedback amplifier to be stable, the separation between the forward-path gain and the demanded gain in graphs such as Figure 3 should not decrease towards zero at a rate exceeding 20 dB/decade. If an amplifier uses conventional resistive feedback, this stability criterion requires that the forward path must have just one dominant pole $1/\tau_\mu$, usually achieved in practice by suitable lag compensation. All the poles associated with transit time effects in transistors must be at substantially higher frequencies than $1/\tau_X$, the frequency of intersection of the curves of forward-path gain and demanded gain. Thus, available transistor types ultimately force the choice of $1/\tau_X$, and hence set a limit to the reduction of distortion that can be achieved by feedback because the return difference $F(\omega)$ at angular frequency ω in Equation 7 cannot exceed

$$F(\omega) \leq 1/\omega\tau_X . \qquad (8)$$

There is, however, another solution to the stability problem. If the forward-path gain has two dominant poles, so that its gain falls at 40 dB/decade, the rate of closure between the graphs of forward-path gain and demanded gain would still be 20 dB/decade provided the demanded gain itself were to fall at 20 dB/decade. In essentials, this requires that the usual frequency-independent resistive feedback factor β should be replaced by something having a frequency dependence of the form $\omega\tau_F$ (remember that the demanded gain is the reciprocal of the feedback factor). Mathematicians tell us that a linearly rising frequency response corresponds to differentiation with respect to time and, in hardware terms, a capacitive feedback network will perform just this action.

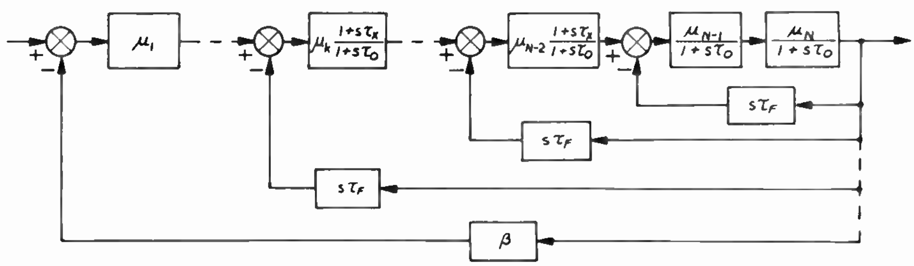

Figure 5. **Block diagram of an NDFL amplifier.**

Figure 5 shows the outline of an amplifier incorporating nested differentiating feedback loops.

Notice first that the forward path has been separated into a number of stages, whose mid-frequency gains are μ_1 to μ_N respectively. The variable s is what mathematicians call complex frequency; for sinusoidal signals its magnitude is equal to the angular frequency ω of the sinusoid. Factors of the form $(1 + s\tau_X)$ represent a frequency response that rises proportional to frequency above the frequency $1/\tau_X$ — that is, they represent a zero. Similarly, factors of the form $1/(1 + s\tau_0)$ represent a frequency response that falls inversely proportional to frequency above the frequency $1/\tau_0$ — that is, they represent a pole. Thus, the stages in Figure 5 have special frequency responses: all stages except the first have a pole at $1/\tau_0$, and all except the first and last two have a zero at $1/\tau_X$.

Notice also that there are differentiating feedback networks, each denoted by $s\tau_F$, linking the output back to various points in the forward path. The resulting feedback loops are arranged one inside another, like a nest of Chinese boxes — hence the name nested differentiating feedback loops.

The amplifier is completed by an overall resistive feedback network β.

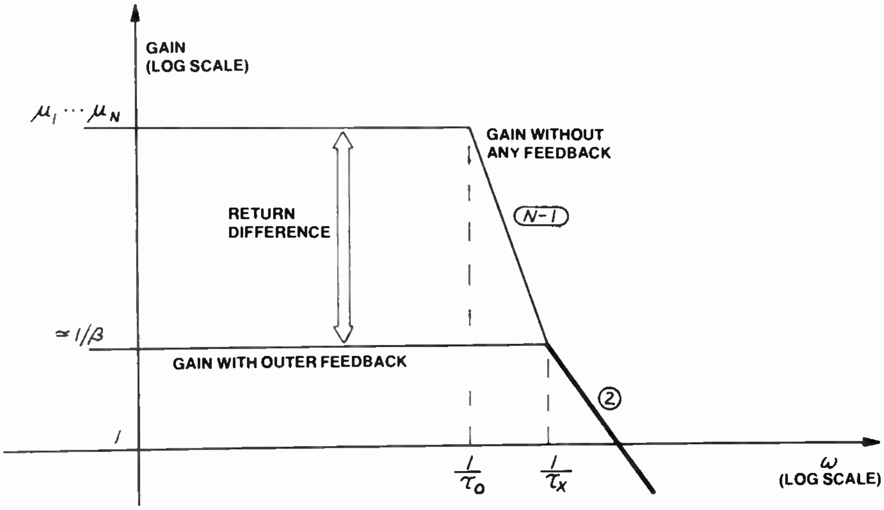

Figure 6. **Logarithmic plots of gain versus frequency for Figure 5.**

If we removed all the feedback from Figure 5, the forward-path gain would be shown in Figure 6: constant up to the frequency $1/\tau_0$, then falling at an (N-1)-pole rate (20(N-1) dB/decade) up to $1/\tau_X$, and finally levelling off somewhat to a two-pole rate (40 dB/decade).

If we now applied just the overall resistive feedback β, the return difference would be as shown in Figure 6. Distortion would be reduced by a constant large amount, approximately $\mu_1 \mu_2 \ldots \mu_N \beta$, at all frequencies up to $1/\tau_0$. Choosing $1/\tau_0$ to correspond to 20 kHz would virtually eliminate audible-frequency distortion. *But the amplifier would be unusable because of oscillation.*

The rate of closure of the forward-path gain and demanded gain curves breaks the rule of 20 dB/decade. Let us see how inclusion of the nested differentiating feedback loops solves the problem.

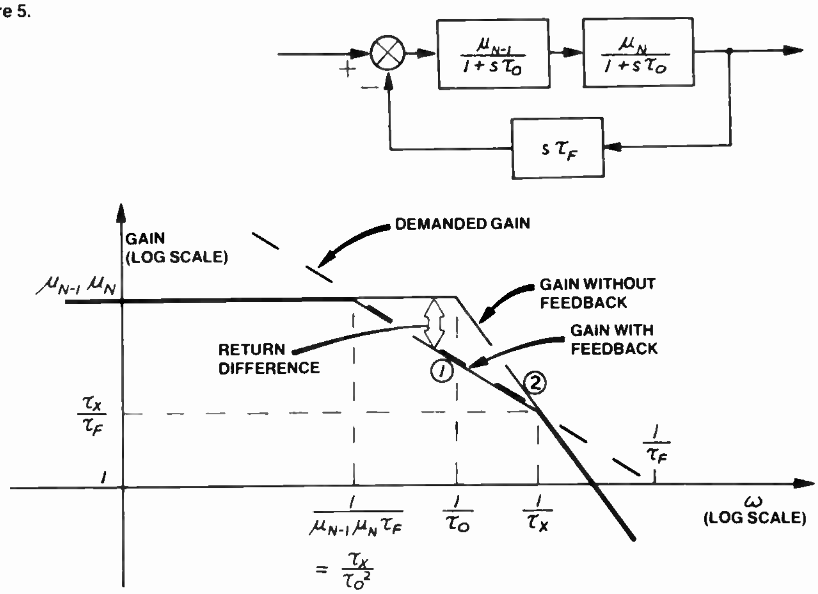

Figure 7. **The inner loop of Figure 5.**

Figure 7 shows just the last two stages and the inner differentiating feedback factor. This 'clump' is a feedback amplifier in its own right, and Figure 7 shows its forward-path gain (that is, the gain of the last two stages without any feedback), the demanded gain, and the resulting closed-loop gain. Although the forward-path gain falls at a two-pole rate (40 dB/decade), the demanded gain falls at a one-pole rate (20 dB/decade), and their rate of closure is 20 dB/decade. By itself, this 'clump' is stable.

Figure 8 shows what happens when we add the antepenultimate stage and another differentiating feedback factor.

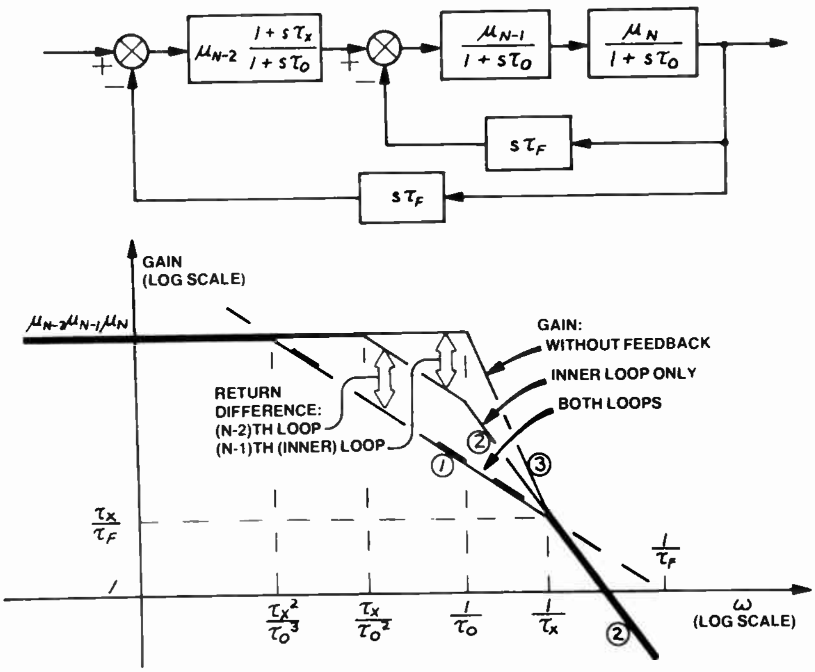

Figure 8. **The (N-2)th loop of Figure 5.**

Again this 'clump' can be considered as a feedback amplifier in its own right. Provided we choose

$$\mu_{N-2} = \tau_0/\tau_X$$

the various gains line up as shown. The forward-path gain is the combined gain of stage (N-2) and stages (N-1) and N with their local feedback, and this is the middle solid curve in Figure 8. The demanded gain is the dashed curve passing through $1/\tau_F$. Once again the forward-path gain and demanded gain close at 20 dB/decade, so the stability criterion is satisfied for this larger 'clump'.

And so it goes on. We can add more stages and differentiating feedback factors, and each time the curves line up as required for stability provided we choose

$$\mu_1 \mu_{N-1} \mu_N \beta = (\tau_0/\tau_X)^2, \qquad (9)$$

$$\tau_F = \mu_1 \beta \tau_X, \qquad (10)$$

$$\mu_k = \tau_0/\tau_X \text{ for } 2 \leq k \leq N-2 . \qquad (11)$$ ▶

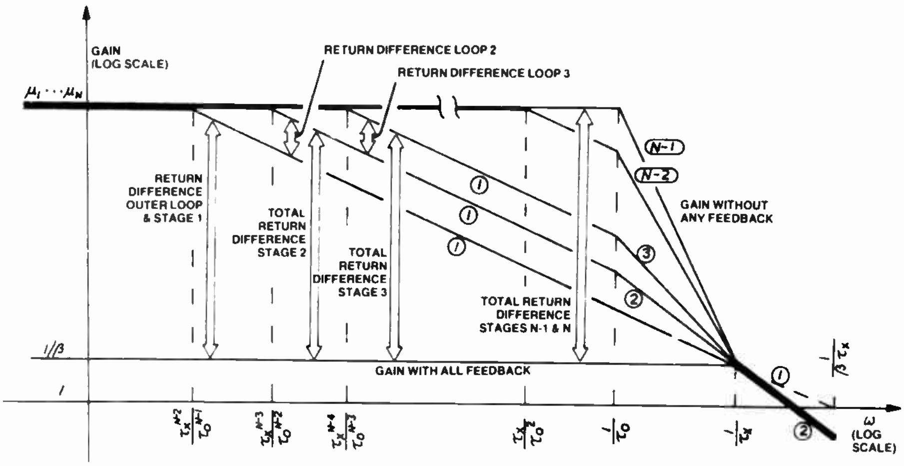

Figure 9 **Complete plots of gain versus frequency for Figure 5.**

Figure 9 shows the gain curves for the complete amplifier.

In designing an NDFL amplifier, the starting point is to choose the frequency $1/\tau_X$ so that the various transistor poles are sure to lie at substantially higher frequencies. Next choose the frequency $1/\tau_0$ up to which the return difference should remain constant; 20 kHz is a suitable value for audio amplifiers. After this, the circuit more or less designs itself via Equations 9 — 11 above.

Outline practical circuit

Figure 10 shows how an amplifier of the basic topology of Figure 2 can be modified to include two NDFLs. Interested readers should refer to references 14 — 16 for more details.

Notice first that the lag compensating capacitor, C, in the penultimate stage of Figure 2 has been removed in Figure 10. In its place are two capacitors (C) linking the output back to various points in the forward path. These capacitors are the feedback networks of the nested differentiating feedback loops.

The output stage has been changed to include a modified form of Thiele's load-stabilising network. Some form of LRC filter is required to locate one of the poles correctly, and with the circuit shown we get double value from the components (see references 17, 18).

The input stage itself is unchanged, but an inexpensive small capacitor in the overall feedback network β can be used to correct the group delay and improve the reproduction of transient waveforms.

Another essential addition is an amplifying stage between the two nested differentiating feedback factors. This rather peculiar circuit (which dates back to Rush in 1964) seems largely to have been forgotten. It uses one n-p-n transistor and one p-n-p to provide a well-defined gain (19).

As already suggested, once the demanded gain $1/\beta$ and the critical frequency $1/\tau_X$ are chosen, the circuit almost designs itself. The equations are:

$$\frac{R_{F1}}{R_{F1}+R_{F2}} = \beta, \qquad (12)$$

$$RC = \beta\tau_X, \qquad (13)$$

$$R_Y C_Y = \tau_X, \qquad (14)$$

$$\tau_L = (\sqrt{3}-1)\tau_X. \qquad (15)$$

All stage gains and poles and zeros automatically look after themselves.

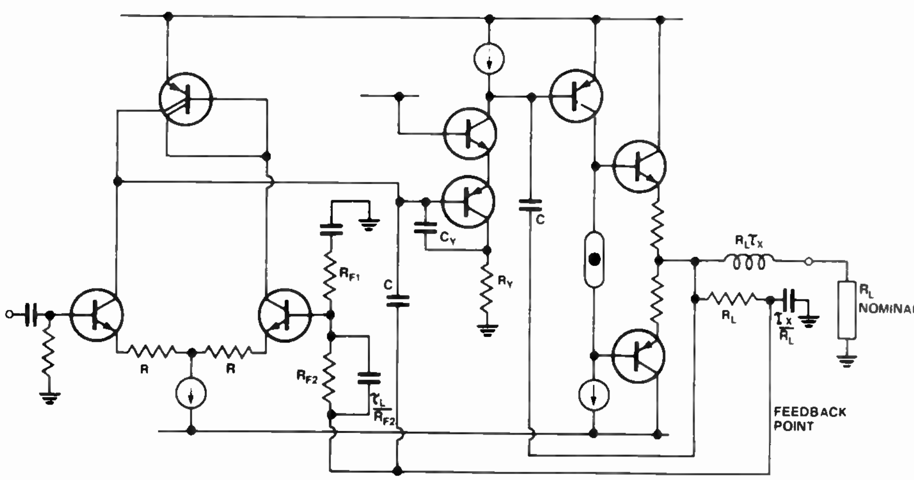

Figure 10. **Outline circuit for an NDFL amplifier.**

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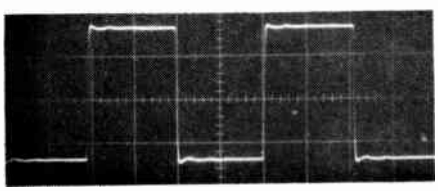
...nested differentiating feedback loops

Figure 11(a) shows the 5 kHz square-wave response of Figure 10 as built from:

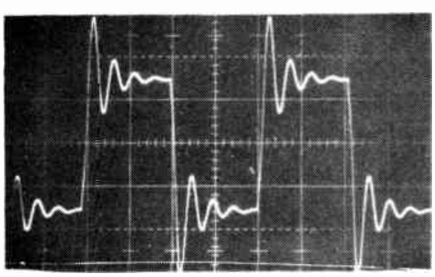
5%-tolerance resistors,
20%-tolerance capacitors,
unselected production transistors.

Evidently the circuit is 'designable': Equations 12 — 15 really do predict component values for good transient response.

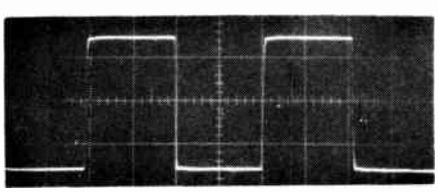
A nice feature of the modified Thiele circuit in Figure 10 is that, when the load is made capacitive (a well-known source of high-frequency oscillation in amplifiers), the voltage waveform at the FEEDBACK POINT is the waveform the amplifier would have delivered into its nominal resistance load. Figures 11(b) and (c) illustrate this: the violent ringing in Figure 11(b) is simply an LC resonance between the filter inductor and the load capacitance, and is in no way indicative of approaching instability.



(a) 8 ohm resistance load.



(b) 8 ohm and 2 uF parallel load



(c) waveform at feedback point for (b)

Figure 11 5 kHz square-wave response of Figure 10.

Figure 12 shows details of the 1 kHz sinusoidal response under overdrive conditions. Note the quick, clean recovery.

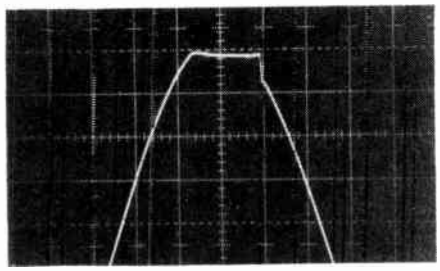


Figure 12 Detail of output waveform from Figure 10 under overdrive.

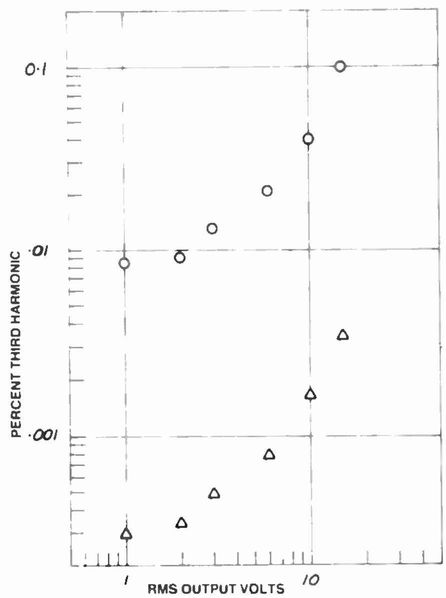
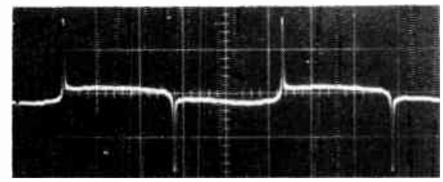


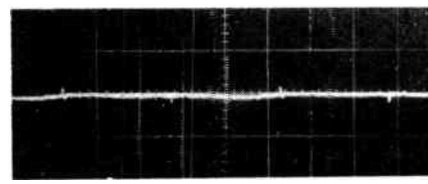
Figure 13 1 kHz third harmonic distortion
o — Figure 2 (conventional amplifier);
— Figure 10 (NDFL amplifier)

An amplifier has been built in which the circuit can be switched from Figure 2 to Figure 10, to illustrate the improvement in performance of adding two NDFLs. Figure 13 compares the measured third-harmonic distortions of 1 kHz. Notice how the distortion of Figure 10 drops away to below three parts per million at small signal amplitudes. Such behaviour is more typical of class-A amplifiers than class-B amplifiers, and may account for the clean sound of NDFL amplifiers.

Crossover distortion associated with incorrect bias of the output stage is one of the most audibly annoying forms of distortion. Audio amplifiers based on Figure 2 sometimes have a type of crossover distortion that does not show up in normal measurements. Correct biasing of the output stage relies on close tracking of the thermally-compensated biasing device and the power transistors. At best the biasing device can be thermally bonded to the power transistor cases. More usually it is bonded to the heatsink, but there is no way it can simultaneously sense the actual junction temperatures of all the power transistors. Under rapidly-fluctuating dynamic signal conditions, the junction temperatures may be wildly different from each other and from the case or heatsink temperatures, and therefore the biasing may be wrong.



(a) Figure 2 (conventional amplifier)



(b) Figure 10 (NDFL amplifier)

Figure 14 2 kHz crossover distortion when bias is set wrongly

Figure 14 compares the static crossover distortion of Figures 2 and 10 when the bias is deliberately set 0.5 V too low. Dynamic mistracking of the biasing circuit should not introduce audible crossover distortion in an NDFL amplifier.

One final point. The NDFL technique maximises the return difference (and hence minimises distortion components) at frequencies up to $1/\tau_0$. Above this frequency the return difference falls away rapidly, and distortion rises. Choosing $1/\tau_0$ to correspond to 20 kHz minimises audible-frequency distortion, but does not minimise ultrasonic distortion.

For example, a common specification for audio power amplifiers is their THD at 20 kHz. The harmonics of 20 kHz lie at 40 kHz, 60 kHz, 80 kHz, and so on. All are ultrasonic (and hence inaudible) and the NDFL technique does not minimise them. A measurement of THD at 20 kHz may therefore give a quite misleading indication of an NDFL amplifier's audible performance. Valid objective tests include the SMPTE and CCIF tests for two-tone intermodulation distortion, the proposed IEC test for TIM (20), Cordell's proposed three-tone test for TIM (21) and the proposed test for input-output intermodulation distortion IOD (9). The distinguishing feature of all these tests is that they measure the distortion at audible frequencies. ●

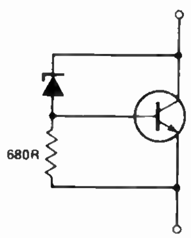
Designer's notebook

Phil Walker

EVER NEEDED a two-bit digital to analogue converter, an awkward low current supply rail, logic level shifting? These are just three of the nine design ideas presented here.

Uprated Zener Diode

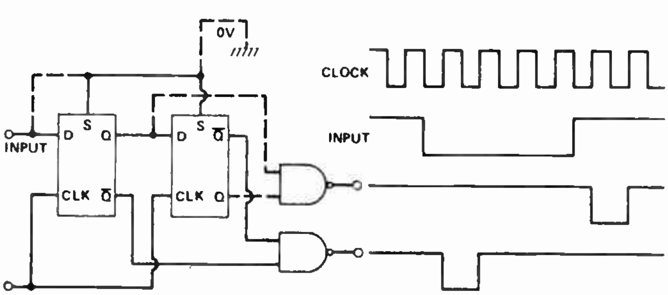
This circuit can be used to simulate a high power zener diode where the correct component is not available or is too expensive. The configuration increases the allowable dissipation in the circuit up to the limit of the transistor, or the diode rating times the transistor current gain. The stabilised voltage is about 0.6 V to 1 V greater than the nominal zener voltage. The variation of output voltage with load current may not be quite as good as a normal diode but this may well be offset by convenience or cost considerations.



Single Output Pulse From An Input Change

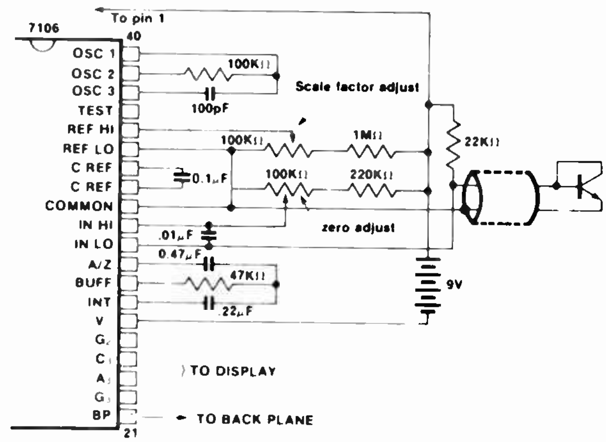
When dealing with asynchronous inputs to a digital system it is often necessary to signal that a change of input has occurred. This circuit is mainly concerned with producing a single pulse synchronous with the system clock when the input changes state. The output is a pulse, one clock period wide, after the input goes from high to low or vice-versa (depending upon which output is used).

If only the falling edge of the input is of interest, then the input signal may be taken to the set inputs of the latches. This will enable the circuit to respond more quickly and reliably to successive pulses. In general the clock frequency should be at least four times the input frequency.



LCD Thermometer

The ICL 7106 used as a digital centigrade thermometer. A silicon diode-transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

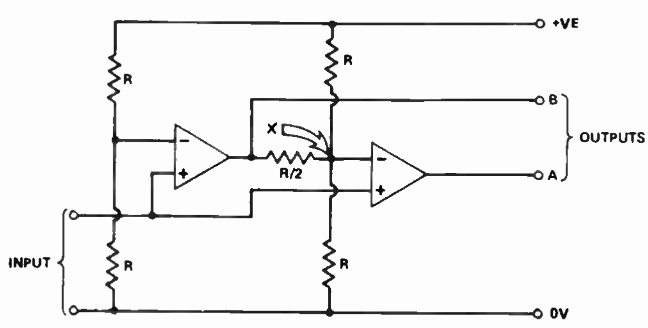


Two Bit A/D Converter

This is a very simple circuit which gives an approximate conversion of an input voltage level to a two bit binary code. Its accuracy is limited by the output circuitry of the op-amps and for best results CMOS types could be used.

As the input voltage rises from 0 V, at first both the A and B outputs are low. This makes the voltage at point X about one-quarter the supply voltage. As the input voltage reaches this level, output A will go high. Later, when the input voltage reaches half the supply voltage, output B will go high. This then makes the voltage at point X go to three-quarters of the supply, forcing output A to go low. Still later, as the input voltage continues to rise it will reach this last value and output A will again go high.

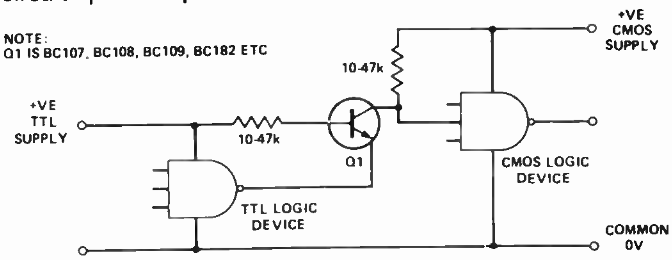
The reference for this circuit is the supply rail. If the op-amps or comparators used cannot drive to very near the supply rails then adjustments may be made to the resistor values to compensate.



TTL to CMOS Logic Interface

When using mixed logic families it is necessary to transfer the signal from one set of logic levels to another. If all the devices are operated from the same supply rails this is easy, but if the rails are different then some form of interface circuit is needed.

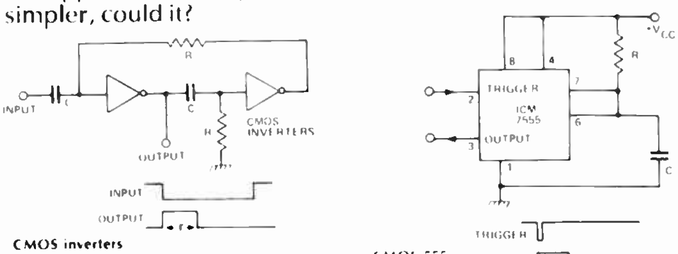
For a TTL to CMOS interface this can be most simply a TTL gate with an open collector output and pull-up resistor, but if this is not available then the following circuit may be used. The circuit operates quite well for low to medium frequencies.



Monostables

A commonly-used circuit block is the monostable. There are several convenient ways to realise one and these two general circuits show how. Suitable CMOS inverters for the upper circuit would be 74C04, 4009, 4049 and 4069. Inverters can be made by tying the inputs of NAND gates together, don't forget. 'Rule of thumb' timing equations are given.

The ICM7555 is a CMOS version of the ever-popular 555. In this application the input is pin 2, output is pin 3. It couldn't be simpler, could it?



CMOS inverters
T = 1.38RC
Keep R greater than 47k

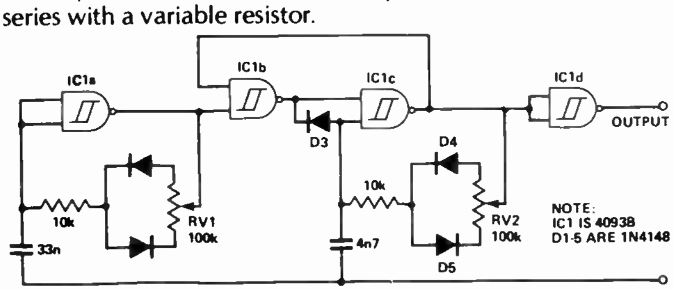
CMOS 555
T = 1.1RC

Simple Pulse Burst Generator

Using a 4093 CMOS quad NAND gate package it is very easy to make a circuit which produces bursts of pulses. These bursts have the property that they are composed of complete pulses, all of which have the same duration. The circuit shown here is configured to produce a variable number of pulses in each burst while the repetition rate of the bursts remains roughly constant.

The first IC section produces the variable mark/space ratio burst control signal, the next two sections are the gated oscillator while the last section acts as a buffer and gives the output as positive-going pulses.

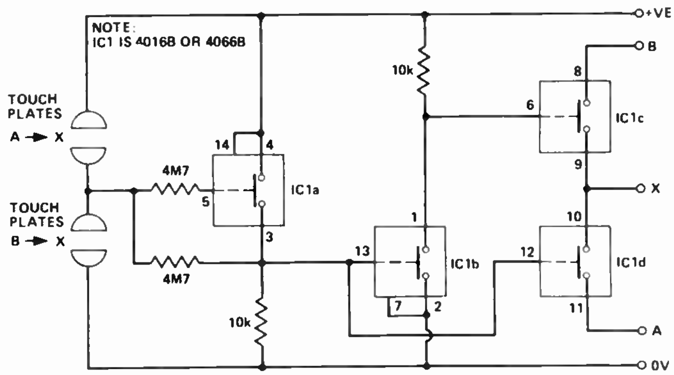
The frequency of operation for both sections is determined by the product of the capacitance and the fixed plus variable resistance. If a 50% fixed duty cycle is desired then the resistor/diode combination can be replaced by a fixed resistor in series with a variable resistor.

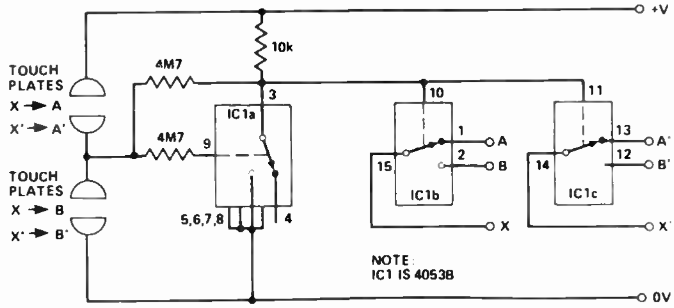


Bistable Touch Switch For Analogue Signals

This uses two sections of a 4016 or 4066 CMOS switch IC. One section of the device is used as a latch, while the others can be used as a changeover switch or as three make or break switches.

A similar switch can also be made using a 4053 triple 1 of 2 selector. In this case we get two analogue change-over switches with a bistable action. Either of these circuits could be used where audio control or signal selection is required but the hi-est of fi is not essential.



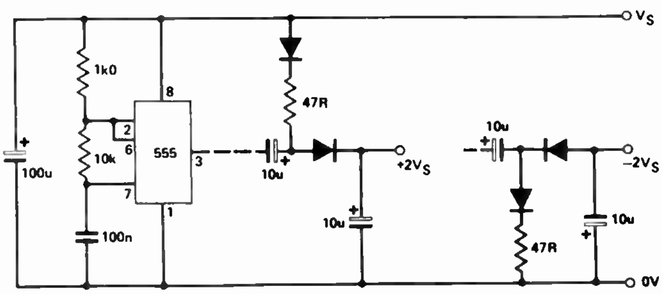


Extra Supply Rails

A 555-type timer IC can be used to provide that awkward low current supply rail when an extra battery would be inconvenient. The device is connected as a free-running astable oscillator and drives a simple charge pump. The polarity of the diodes and capacitors in the output circuit determines whether the output is positive or negative. Output impedence of this circuit is usually quite high, being determined by the capacitor values. The capacitor values should not be too high as this will overload the output circuit of the IC.

If the standard type of 555 IC is used the main supply rail should be decoupled at the IC pins with an electrolytic capacitor to prevent the well-known switching spike of the device affecting the rest of the circuitry.

The output voltage from this arrangement will range up to about equal to the input voltage, superimposed on to the relevant supply rail. ●



Use your Motorola 6800 D2 kit to progam 2716 EPROMs

If you have been waiting for cheap, easy to program and easy to use EPROMs before incorporating non-volatile memory into your microcomputer system or building dedicated microprocessor projects, then you need wait no longer. With the 2716-type EPROMs now available and this very simple interface you can program EPROMs very quickly and cheaply using a Motorola 6800 D2 kit.

David L. Craig.

OVER THE PAST couple of years there has been a remarkable development in the EPROMs available for use in microprocessor systems. After the difficult-to-program 1702 EPROMs with 512 x 8 storage, we saw the 2708 EPROM arrive with twice the storage capacity (1024 x 8 bits) and considerably simpler programming requirements. The 2708 has become relatively cheap, but many hobbyists have probably been put off using this device because it requires three power supply voltages (+12 V, +5 V, −5 V) when the rest of the microprocessor system probably only uses one (+5 V); it also requires a programmer capable of switching a +26 V programming supply, and it requires each location to be programmed about 100 times in a loop, making programming of individual locations difficult.

Now we have the 2716, which makes EPROMs much more attractive to hobbyists. It contains 2K x 8 bits of storage, uses only a single +5 V power supply, requires a static +25 V programming supply, with each location being programmed with a single 50 ms TTL-level pulse, and allows programming of any number from 1 to 2048 locations at a time. And best of all is the price — around $5 each in one-off quantities from some sources. This represents far better value than the 2708 ever did.

2716 EPROMs can be programmed using a Motorola 6800 D2 kit and the very simple and low-cost interface circuit shown in Figure 1. The programmer interface connects to the user PIA (Peripheral Interface Adaptor) of the D2 kit. A programming power supply of

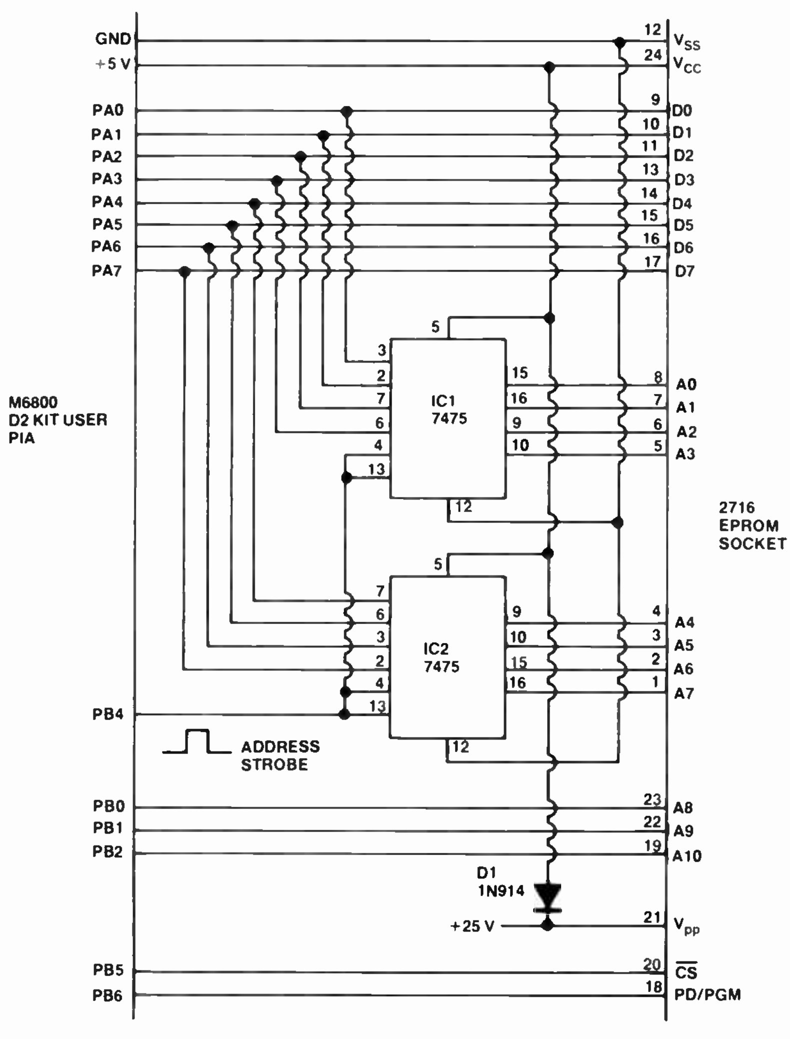


Figure 1. **2716 EPROM programmer interface circuit.**

+24 V to +26 V is also required. The interface circuit simply uses two 7475 quad latch ICs to latch the address information from the PIA, and one diode to feed +5 V to the Vpp pin of the 2716 with the +25 V programming supply turned off. No pc board layout is given since the circuit is so simple and the method of construction will depend on the system with which the interface is to be used.

All the signal generation and timing required are handled by a software routine called 'PG2716', for which a full listing is given. The routine latches the address of the location to be programmed into the 7475s, then reads the contents of that location, checking that it is erased (i.e: $FF), programs the location and then again reads the contents to verify the programmed data. Each address of the EPROM is programmed in turn in this way. The waveforms required by the 2716 for this sequence are shown in Figure 2. Using these waveforms and the comments in the listing the operation of the routine should be fairly easily followed. The routine occupies only 170 bytes of memory, and while the listing shows it assembled beginning at location $1E00, it is relocatable without changes. The only fixed locations used are $A002-A005 and $A042-A043, which are in the D2 kit stack RAM.

The principle of operation of the programmer is that the data to be stored in the EPROM is first loaded into RAM and then copied as a block into the EPROM. The only restriction on loading the data into RAM is that the eleven low-order address bits (A0-A10) of the data in RAM must correspond to the address in the EPROM at which that data byte is to be stored; i.e: a 2K x 8 block of data in the D2 kit RAM maps directly to the 2716 EPROM.

The sequence of steps to be followed in using the programmer is:

a. connect the interface circuit to the D2 kit
b. insert the EPROM into the interface socket
c. power up the D2 kit
d. load the programmer program and the data to be programmed into the D2 kit memory
e. power up the +25 V programming supply
f. enter the beginning address of the data in the D2 kit memory into $A002-3, and the end address into $A004-5 via the D2 kit keyboard (note that any number of data bytes from 1 to 2048 can be specified.)
g. start the programmer by entering $1E00 G via the D2 kit keyboard
h. if the EPROM is programmed successfully, the JBUG prompt '-' will appear on the D2 kit display after approximately 100 seconds
i. power down +25 V programming supply
j. power down D2 kit

The EPROM is then programmed ready for use.

In the event of an error, a software interrupt of the programming routine will occur.

a. if the SWI occurs at $1E33, the EPROM was not correctly erased
b. if the SWI occurs at $1E34, programming did not occur correctly

In either case, after the SWI, X = location at which failure occurred, A = data expected at failed location, B = data in EPROM at failed location.

2758 (1K x 8 bit) EPROMs can also be programmed with this programmer. 2758 EPROMs are 2716 EPROMs with only the lower or upper half working. To program a 2758, load the data to be programmed into the appropriate half of a 2K x 8 block in the D2 kit RAM so that the 1K x 8 data maps directly into the working half of the 2K x 8 locations in the 2758.

One note of warning should be given for purchasers of 2716-type EPROMs. Some manufacturers, e.g: Texas Instruments, have designated a three power supply 2K x 8 EPROM with the 2716 code (e.g: TMS 2716). Be careful to purchase the single power supply version — from Texas this is the TMS 2516.

A place suitable for using 2716 EPROMs, though it is not mentioned in the manual, is in the two sockets on the main D2 kit board provided for optional PROMs. The straps on the board necessary for 2716 use are E0-E4, E1-E2, E3-E7 and E5-E9. All other connections on the pc board are correct. Wherever it is that you use 2716 EPROMs, one thing is certain — you will never go back to 2708s.

The principle of using a programmable input-output port with a single interface to program 2716 EPROMs could easily be applied to microprocessor systems using other processors, e.g: Z80, 8080, etc. It can also be applied to programming other EPROM types, and the author has built such an interface for Intersil IM6654 512 x 8 bit CMOS EPROMs.

(Ref. 'An Ultra-Low-Cost Programmer for CMOS EPROMs', Electronic Engineering (UK), Jan. 1981, pp 23-25.) ▶

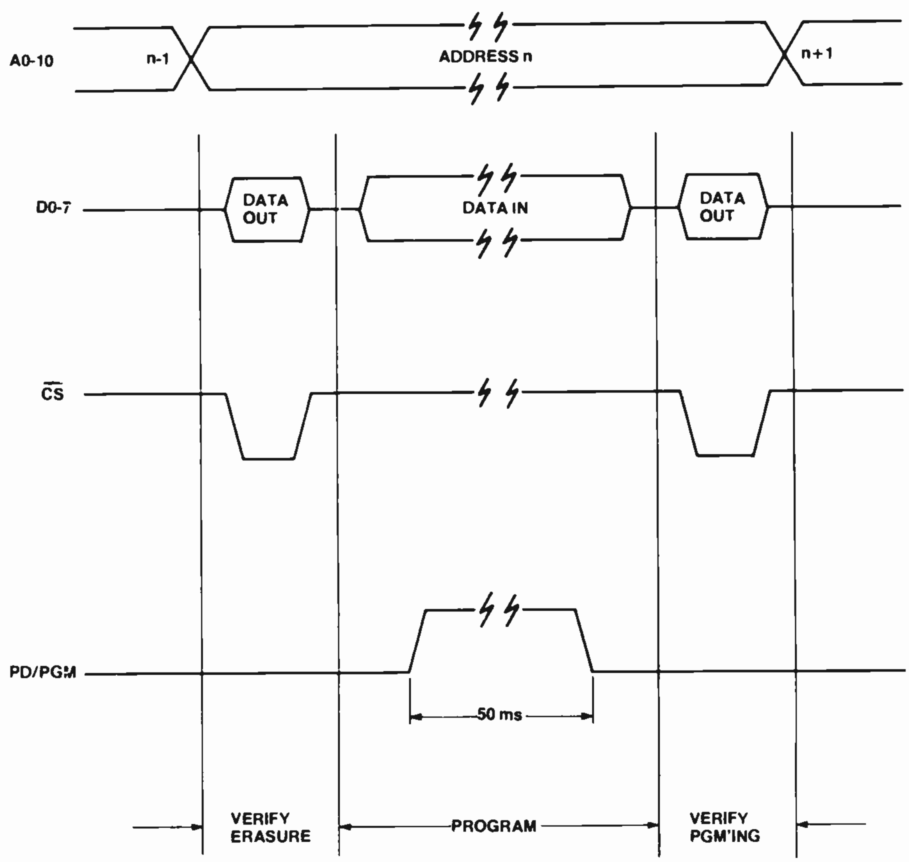


Figure 2. **2716 EPROM programmer waveforms.**

Program Listing

```
            **  2716 EPROM PROGRAMMER PROGRAM  **

        8004    PIAA     EQU $8004      User PIA
        8005    PIACRA   EQU $8005
        8006    PIAB     EQU $8006
        8007    PIACRB   EQU $8007

A002            BEGADD   RMB2           From begin address
A004            ENDADD   RMB2           From end address

A042            ADDPNT   RMB2           Pointer at address to be
                                        read or programmed

1E00  C6 FF     PG2716   LDAB #$FF      Set PIAB as outputs
1E02  CE 8006            LDX  #PIAB
1E05  8D 31              BSR PIASET
1E07  C6 20              LDAB  #$20     Initialize PIAB
1E09  E7 00              STAB 0,X

1E0B  FE A002            LDX BEGADD     Initialize ADDPNT
1E0E  09                 DEX
1E0F  08        LOOP     INX
1E10  FF A042            STX ADDPNT     Update pointer

1E13  8D 33              BSR OUTADD     Output address

1E15  8D 53              BSR DATARD     Read data and
1E17  86 FF              LDAA  #$FF
1E19  11                 CBA            verify EPROM
1E1A  26 14              BNE ERROR1     location erasure

1E1C  8D 66              BSR DATAWR     Program EPROM location

1E1E  8D 4A              BSR DATARD     Read location to verify
1E20  FE A042            LDX ADDPNT     programming
1E23  A6 00              LDAA 0,X
1E25  11                 CBA
1E26  26 0C              BNE ERROR2

1E28  BC A004            CPX ENDADD     Test if all locations
1E2B  26 E2              BNE LOOP       programmed
1E2D  7E E08D            JMP RESTAR     Return to JBUG

1E30  FE A042   ERROR1   LDX ADDPNT     Not properly erased
1E33  3F                 SWI

1E34  3F        ERROR2   SWI            Not properly programmed

   ** SUBROUTINE TO SET PIA LINES AS INPUTS OR OUTPUTS **

Entry - X = PIA peripheral register address
        B = required data direction pattern  (0 = in, 1 = out)

1E38  6F 01     PIASET   CLR 1,X        Access DDR
1E3A  E7 00              STAB 0,X       Set lines as I/O
1E3C  86 04              LDAA #$04
1E3E  A7 01              STAA 1,X       Access PR
1E40  39                 RTS

       ** SUBROUTINE TO OUTPUT ADDRESS TO EPROM **

Entry - ADDPNT  =  address to be output

1E48  C6 FF     OUTADD   LDAB #$FF      Set PIAA as outputs
1E4A  CE 8004            LDX #PIAA
1E4D  8D E9              BSR PIASET

1E4F  B6 A043            LDAA ADDPNT+1  Output low byte
1E52  A7 00              STAA 0,X       to PIAA
1E54  B6 A042            LDAA ADDPNT
1E57  84 07              ANDA #$07      Mask off high 5 bits
                                        of high byte
1E59  8A 10              ORAA #$10
1E5B  E6 02              LDAB 2,X       Output high 3 bits
1E5D  C4 E0              ANDB #$E0      of address to PIAB
1E5F  1B                 ABA            and output low
1E60  A7 02              STAA 2,X       byte into latches by
                                        setting address strobe
                                        high
1E62  86 EF              LDAA #$EF      Set address strobe low
1E64  A4 02              ANDA 2,X       to latch address
1E66  A7 02              STAA 2,X
1E68  39                 RTS

          ** SUBROUTINE TO READ DATA FROM EPROM **

Entry - address latched
Exit  - data in B

1E6A  5F        DATARD   CLRB           Set PIAA as inputs
1E6B  CE 8004            LDX #PIAA
1E6E  8D C8              BSR PIASET

1E70  86 DF              LDAA #$DF      Set PB5 low to read
1E72  A4 02              ANDA 2,X       data
1E74  A7 02              STAA 2,X

1E76  E6 00              LDAB 0,X       Read data

1E78  86 20              LDAA #$20      Set PB5 high to end
1E7A  AA 02              ORAA 2,X       data read
1E7C  A7 02              STAA 2,X

1E7E  39                 RTS

          ** SUBROUTINE TO WRITE DATA TO EPROM **

Entry - address latched
      - ADDPNT points to data

1E84  C6 FF     DATAWR   LDAB #$FF      Set PIAA as outputs
1E86  CE 8004            LDX #PIAA
1E89  8D AD              BSR PIASET

1E8B  FE A042            LDX ADDPNT     Point to data
1E8E  E6 00              LDAB 0,X       Fetch data

1E90  CE 8004            LDX #PIAA
1E93  E7 00              STAB  0,X      Output data

1E95  86 40              LDAA #$40      Set PB6 high for

1E97  AA 02              ORAA 2,X       50ms to program
1E99  A7 02              STAA 2,X       EPROM location

1E9B  CE 0F00            LDX #$0F00     50ms delay
1E9E  09        DLY50    DEX
1E9F  26 FD              BNE DLY50

1EA1  CE 8004            LDX #PIAA      Set PB6 low to end
1EA4  86 BF              LDAA #$BF      programming pulse
1EA6  A4 02              ANDA 2,X
1EA8  A7 02              STAA 2,X

1EAA  39                 RTS
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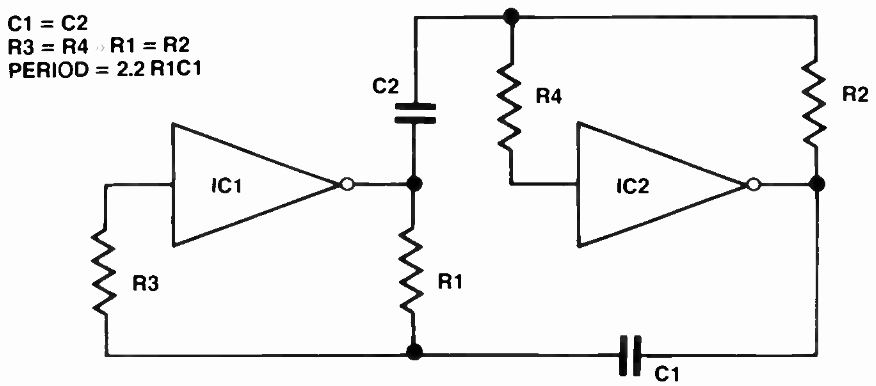
Symmetric multivibrator using two inverting gates

Dr. Ton Trancong



THIS CIRCUIT provides a frequency fairly independent of supply voltage, the output having a near-perfect 1:1 duty cycle. It is based on the improved astable multivibrator circuit described in *ETI Circuit Techniques Volume 1*, p.68, and is useful when low power consumption and simplicity are the main considerations.

The circuit uses the dual RC relaxation circuits formed by R1C1 and R2C2, and is self-starting as it has no stable steady-state. While astable multivibrators using a single RC relaxation circuit suffer non-unity space-to-mark ratio due to the transfer voltage not being exactly halfway between the supply voltages, this circuit avoids the problem by using a dual relaxation circuit based on *two inverter sections on the same IC chip.*

The voltages applied to the gates of both inverters relax exponentially until one of them reaches its gate's transfer voltage. Hence the states of the inverters change instantaneously and the cycle repeats with the two inverters swapping their roles.

Resistors R3 and R4 should have a value of more than three times that of R1 and R2 for the RC relaxation circuits to behave as if R3 and R4 were infinite. However, too high values of R3 and R4 may affect the operation of the circuit as the voltages at the inputs of the inverters may then fail to follow the relaxation voltages. The only requirements for proper operation are that IC1 and IC2 must be sections of the same physical integrated circuit chip, and that corresponding components of the dual circuits must have the same nominal values.

In my particular application, I used a 4009 CMOS hex-inverter chip with R1 = R2 = 300k (20% tolerance), R3 = R4 = 1M (20% tolerance), C1 = C2 = 680p (10% tolerance) of the same production batches. The frequency obtained is fairly stable (with only 33% variation when the supply voltage varies between 3.3 V and 15 V) and its duty cycle is almost a perfect 1:1 over the whole permissible range of supply voltage. When the ratio R3/R1 = R4/R2 is high, the period of the circuit should have the value of 2.2R1C1; in my application it is about 400 ns.

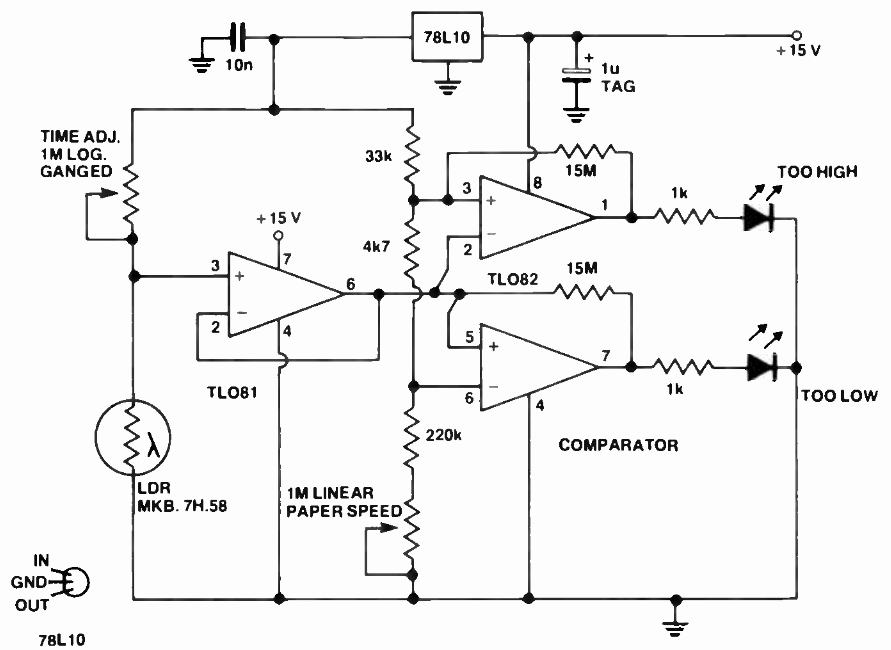
Exposure analyser for black and white prints

This exposure analyser, coupled to a timer, simplifies making black and white prints. A light intensity reading is taken from the image, the 'time' control is adjusted to the balance point and lights two LEDs, the timer is started — and your enlarger is turned on for the correct time.

Peter Cox

THE REASON for building an exposure analyser such as this was to avoid making test strips for different negatives or for different degrees of enlargement. Commercially available analysers are often either fiddly to use or comparatively expensive. Some operate by adjusting the aperture of the enlarger and keeping a constant exposure time, which is less satisfactory than varying the exposure time as most enlarger lenses give better performance when stopped down from maximum aperture.

There have also been several analyser circuits in electronics magazines, but I found these to be either too full of drafting errors to be practicable or, in one case, going into technical overkill — using 23 ICs, digital exposure readout to tenths of a second, and requiring an IC (CA3140) to perform better than its published specifications. So I decided to design and build my own exposure analyser.



NOTES:
1. TLO81, TLO82 ARE BIFET OP-AMPS, VERY HIGH INPUT IMPEDANCE: 10^{12} OHMS TYPICAL.

2. BYPASS 78L10 REGULATOR WITH CAPACITORS SHOWN MAKE SURE THEY'RE CLOSE TO THE IC.

3. SET 1M LOG. (GANGED) POT TO 50% ROTATION: RESISTANCE SHOULD BE CLOSE TO 100k. WITH 2k 'CALIBRATE' POT NEAR MIDDLE, PICK CAPACITOR TO GIVE PULSE DURATION OF 10 SECONDS. TRIMPOT HAS ADJUSTMENT RANGE OF +40%, −20%.

USE:
1. SET TIME ADJUST POT TO 10 SECONDS. MAKE A PRINT THAT REQUIRES 10 SECONDS EXPOSURE: WITH LDR MEASURE MID-GREY OR HIGHLIGHTS (NOT BOTH) AND ADJUST PAPER SPEED POT FOR BRIDGE BALANCE: BOTH LEDS LIGHT.

2. PUSH START BUTTON TO BEGIN TIMING CYCLE.

Circuit operation

The circuit is in two parts, excluding the power supply: the light-measuring comparator has an LDR in one leg of a resistive bridge.

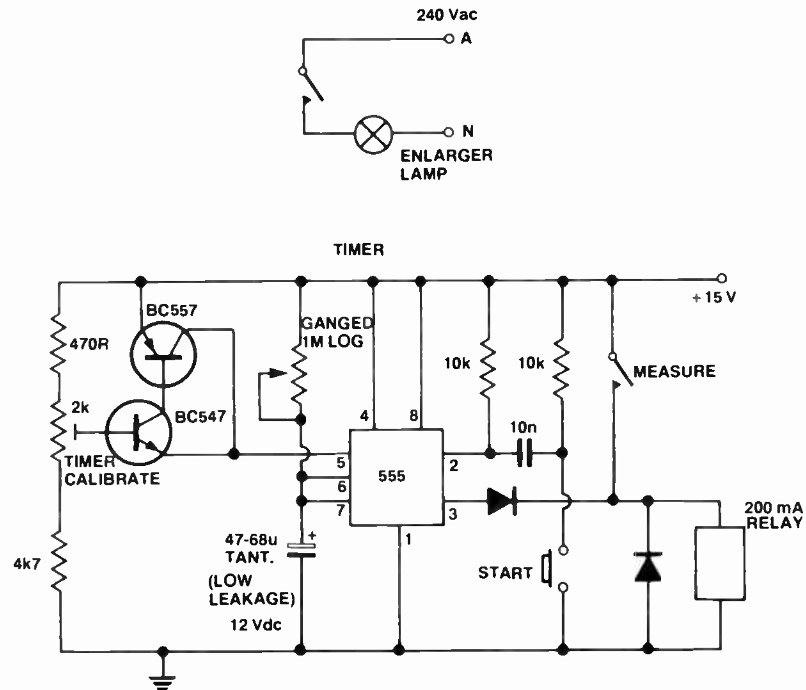
As the LDR resistance can be up to 20-30M, the voltage is buffered by a TLO81 BiFET op-amp. Voltages from the bridge are applied to a window voltage comparator made from a dual BiFET IC. A small amount of hysteresis is provided by the 15M resistors. I didn't worry about using buffering on the other side of the bridge because of lower resistances.

The bridge is fed from a 10 V voltage regulator, as otherwise the IC output voltages may be restricted, the inputs working within 0.75 V or so of the positive rail. The time adjust pot, a 1M log unit, is ganged, and the other section determines the output duration of a 555 monostable. A timer calibrate pot is included to simplify setting up the timer.

The capacitor used in the 555 RC network should be very low-leakage, but ordinary tag tantalums seem to give consistent timings despite leakage currents of 50 nA/uFV (maximum quoted on ITT tag data sheet).

Parts

BiFET op-amps are freely available — singles, duals or quads; the TL084 quad costs $3 or less. The LDR is made in Japan by Moririca, and is sold by Plessey Professional Components of Villawood NSW, costing $1 each in small quantities (when I bought some a while ago). There are many Moririca types available, so others may be more suitable than the ones I used; I bought the LDRs originally for use in an AGC amplifier, as an LDR-LED gain reduction element. ●



Design your own digital test equipment

An extensive range of test equipment may be designed and constructed using the information given here.

Tim Orr

The following sections should give you enough information to go ahead and design your own digital multimeter, customised to give exactly the ranges and features you find most useful. We also look at techniques for measuring temperature and dealing with very small signals.

Dedicated DVMs

Intersil make a pair of DVM chips (Fig. 1, Fig. 2) that make life very easy if you want to measure and display a voltage. These chips are the ICL7106 and the 7107 and they seem to have become an industry standard. The first device is an LCD version and the whole lot consumes a mere 1 mA when running; it can run from a single 9 V 216 battery. The second device uses an LED display. The display may consume up to 100 mA, making battery operation a problem. Several companies make modules that contain both the DVM chip and a display. All you need to do is power it up and send it a voltage. It is, in fact, an 'instant' DVM module — no talent required.

The Intersil chips have a differential input with an input current of only 10 pA maximum, 1 pA typical. The devices have an auto zero facility so that they automatically cancel out any offset voltages at the input. The input sensitivity is 200 mV, but by connecting various amplifers, attenuators, RMS and dB converters and filters to the DVM chip a wide range of signal measurements can be performed.

Measuring Voltage . . .

Figure 2 shows the standard 1 megohm input impedance decade attenuator that is used in most digital multimeters. The very high input impedance of the 7106/7 produces negligble loading of the attenuator network. Figure 4 shows a standard four decade DC voltmeter circuit. If voltages below 200 mV are to be investigated then a preamplifier with low offset and drift characteristics is needed. The resistors used in the attentuator are standard E96 values and can be obtained with a 0.5% tolerance.

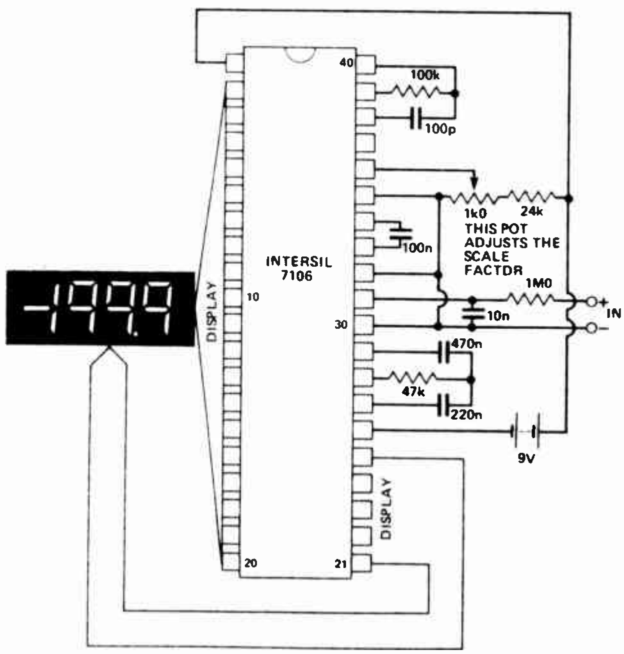


Fig. 1 The Intersil ICL7106 with liquid crystal display.

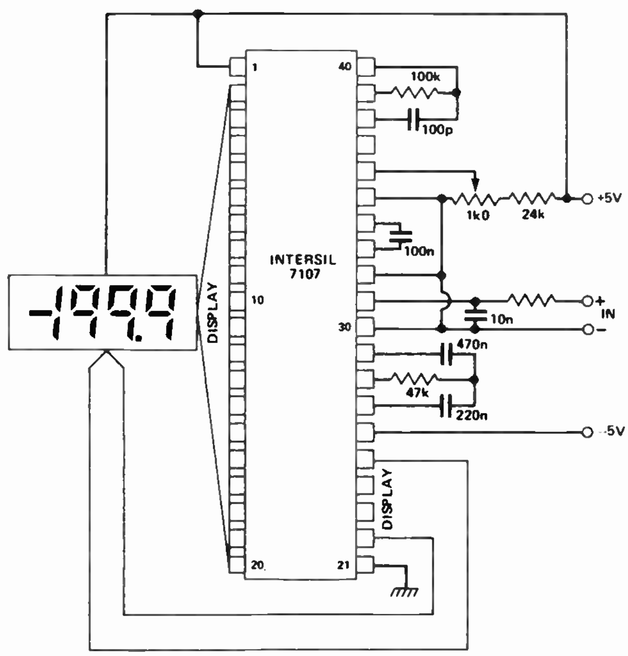


Fig. 2 The Intersil ICL7107 with LED display.

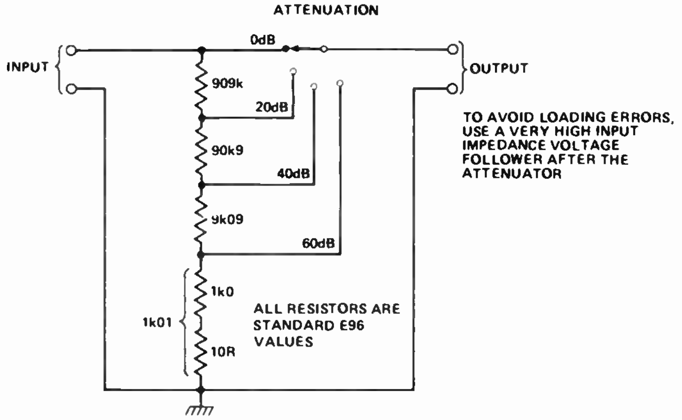


Fig. 3 A 20 dB step attenuator.

. . . Current . . .

Figure 5 is a current meter circuit; the current is made to pass through shunt resistors. This sets up a DC voltage (no more than 200 mV) which is measured by the

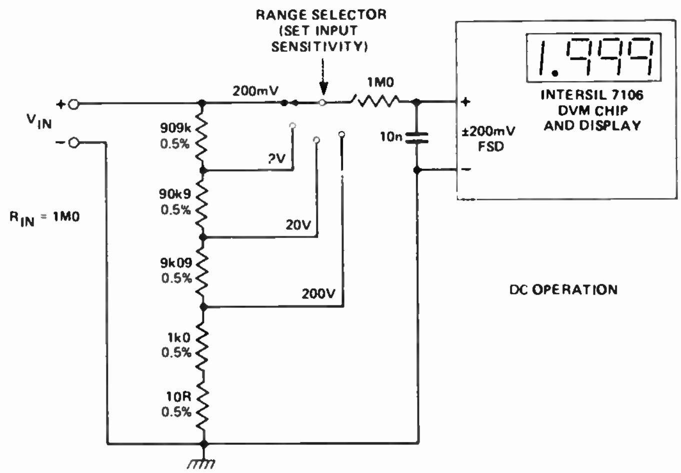


Fig. 4 A decade 3½ digit digital voltmeter.

DVM chip. The input is protected by a diode bridge that pops the fuse when the input voltage exceeds 1V8 (three diode voltages) and the current exceeds 3 A. If you could pass unlimited current through the resistor network then you would probably end up with a fire!

. . . And Ohms

Figure 6 is an ohmmeter circuit. The 741 op-amp generates a precision and stable −1V2 DC reference voltage which causes a fixed current to flow into the virtual earth input of the LF355; the current will be 10 mA using the 120 ohm resistor, 1 mA using the 1k2 resistor and so on. This fixed current also flows through the test resistor which is the feedback route for the LF355 and in doing so sets up a voltage that in linearly proportional to the value of the test resistor. At 'full-scale-deflection' the output of

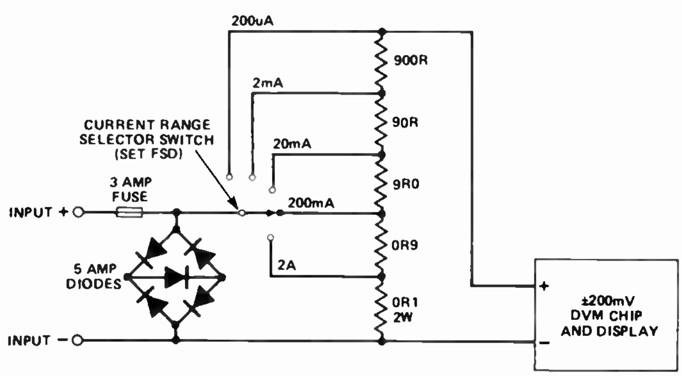


Fig. 5 A five decade DC current meter.

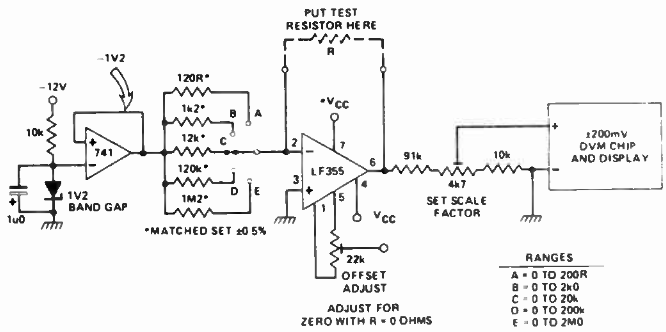


Fig. 6 A five decade ohmmeter.

the LF355 is 2 V which is attenuated to 200 mV; this voltage is then fed to the DVM chip. The LF355 is a JFET op-amp which has a small input current and offset voltage and low temperature drift characteristics. Even so it is bet-

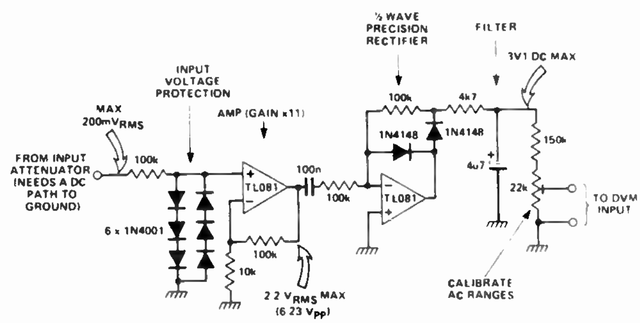


Fig. 7 An AC voltage and current converter. This is only accurate for sine waves.

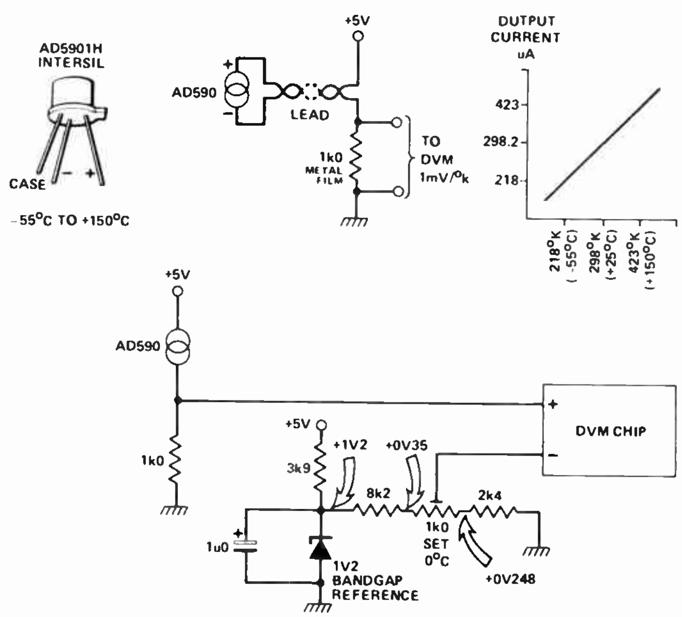


Fig. 8 Reading degrees Kelvin (top) and Centrigrade (bottom). ▶

ter to run the output at 2 V and then attenuate it to 200 V, because this also attenuates any residual offsets and other errors.

Figure 7 shows a simple AC converter circuit that is a cheaper alternative to the RMS to DC converter published last month. It can be used to measure V RMS and I RMS for a sine wave input. The circuit is a high impedance buffer/amplifier with a half-wave precision rectifier and smoothing circuit.

Measuring Temperature

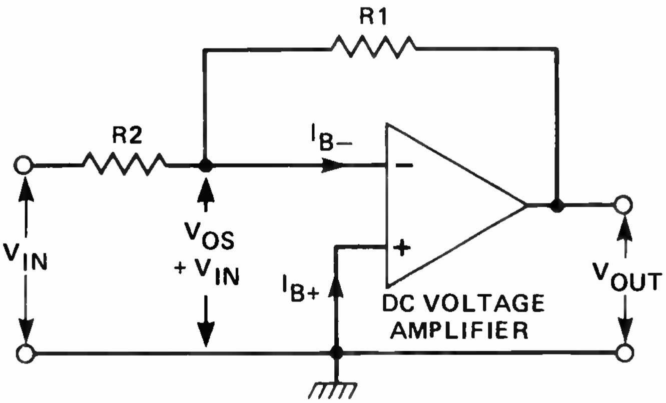
Intersil makes a device called the AD5901H which converts temperature into current; the device generates an output current of 1uA per degree Kelvin. Absolute zero in degrees Kelvin is −273.2°C and so 0°C = 273.2°K. If this temperature-dependent current is dumped into a 1k0 resistor then the voltage across the resistor will increase by 1 mV per degree K (or C) — see Fig. 8. The operating range of the device is −55°C to +150°C which will generate a voltage change of 205 mV across the 1k0 resistor. This can easily be displayed on the ±200 mV range of the DVM chip. The sensor plus the DVM and display make a very simple and compact battery operated digital thermometer.

Amplifying Small Signals

Often you need to amplify very small DC voltages. The output from strain gauges or thermocouples is very small, often below 1 mV. This would hardly cause any movement in a 200 mV DVM chip. However, an amplifier that will operate in the sub-millivolt area is quite difficult to make with any accuracy. For example, a 741 op-amp might have an input offset of 2mV (Table 2). this error is actually bigger than the voltage we are measuring!

There are four main sources of error. I_B, the input bias current, has to flow through R1 and R2 and in doing so upsets the gain equation. Note that I_{B-} is not exactly the same value as I_{B+}! V_{OS} is the input offset voltage which represents a DC input imbalance. This also upsets the gain equation. Furthermore, V_{OS} has a temperature coefficient V_{OSTC} which is the maximum change in V_{OS} per degree C. So the amplifier will drift with temperature. V_n is the input noise voltage, which is multiplied by the fixed gain on the amplifier. If the noise is similar in amplitude to the input voltage then you are going to get noisy readings. Finally, the input offset voltage drifts with time — it ages! Very few manufacturers provide information regarding this parameter.

The selection chart (Table 2) shows a range of instrumentation and ordinary op-amp error parameters. The way to overcome these errors is to use a suitable op-amp rather than to use a low performance part and to try and cancel out all the drifts and offsets. The details given in the chart only show some of the many parameters that manufacturers specify. Devices are often graded into several performance categories, so if you want to design high quality amplifiers then refer to the manufacturers' detailed data. ●



$$V_{OUT} = \left(V_{IN} \times \frac{R1}{R2} \right) + \text{ERRORS}$$

Fig. 9 Choosing a precision op-amp. Table 1 (left) gives some typical noise results, Table 2 (below) shows typical values for the errors shown in the above diagram.

TABLE 1

DEVICE	E IN uV RMS (AVERAGE OF SEVERAL SAMPLES)	NOISE LEVEL RELATIVE TO NE5534 IN dBs
NE5534 (SIGNETICS)	0.59	0
RC4136 (RAYTHEON)	0.87	+3.4
RC4739 (RAYTHEON)	1.00	+4.6
RC4558 (RAYTHEON)	1.05	+5.0
TL081 (TEXAS)	1.61	+8.7
741 (VARIOUS MANUFACTURERS)	1.72	+9.3

TABLE 2

DEVICE MANUFACTURER	LM363 NAT. SEMI	ICL7650 INTERSIL	LF355 NAT. SEMI	TL081 TEXAS	741 —	725 —	OP-27A/E PMI
I_B	2 nA	10 pA	30 pA	5 pA	80 nA	42 nA	10 nA
V_{OS}(uV)	30	1	2000	5000	2000	500	10
V_{OSTC} (uV/°C)	2	0.05	5	20	2	0.6	0.2
NOISE (V_n) (nV/√Hz)	12	2 uV_{pp}	20	20	14	9	3
LONG TERM DRIFT	—	100 nV/month	—	—	—	—	200 nV/month
COMMENTS	Av = 100	Chopper stabilised op-amp	JFET op-amp	JFET op-amp	Bipolar op-amp	Instrumentation op-amp	Ultra-low noise precision op-amp

240 V To 120 V Converter For Resistive Loads

M. Greenfield

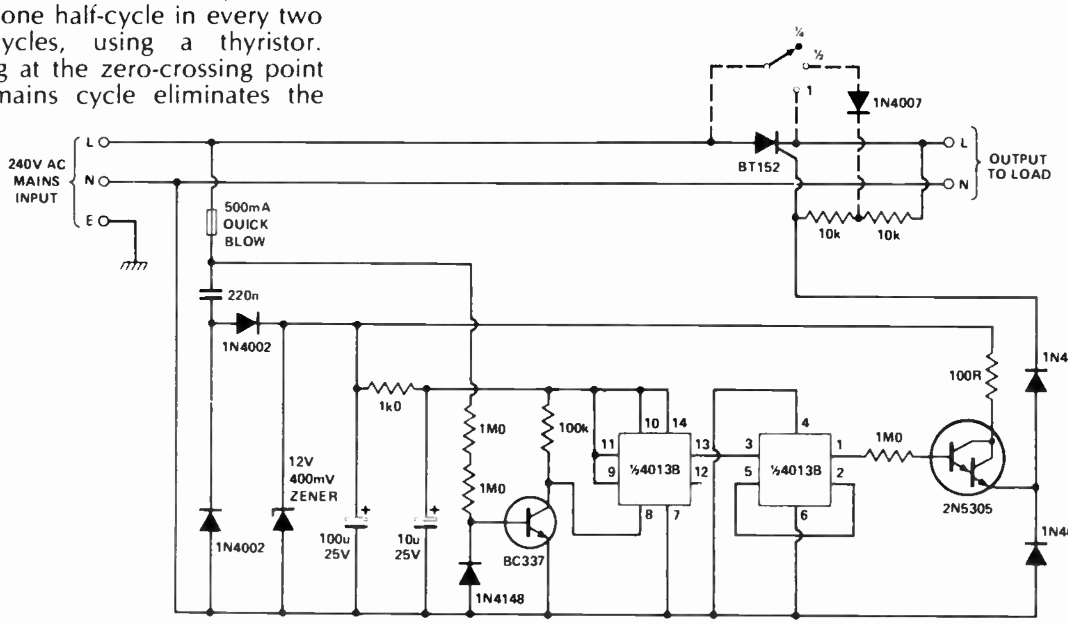
A friend visiting the USA has brought back with him a percolator and an electric stewing pan, both for 110 V operation, rated at 600 W and 1.2 kW respectively. He was under the impression that a small transformer would do but this, of course, was not practical and the solution had to be electronic.

Since the power in the load is V^2/R it will have quadrupled with respect to the American wattage. Thus the control circuit is required to produce one half-cycle in every two mains cycles, using a thyristor. Switching at the zero-crossing point of the mains cycle eliminates the need for RFI suppression.

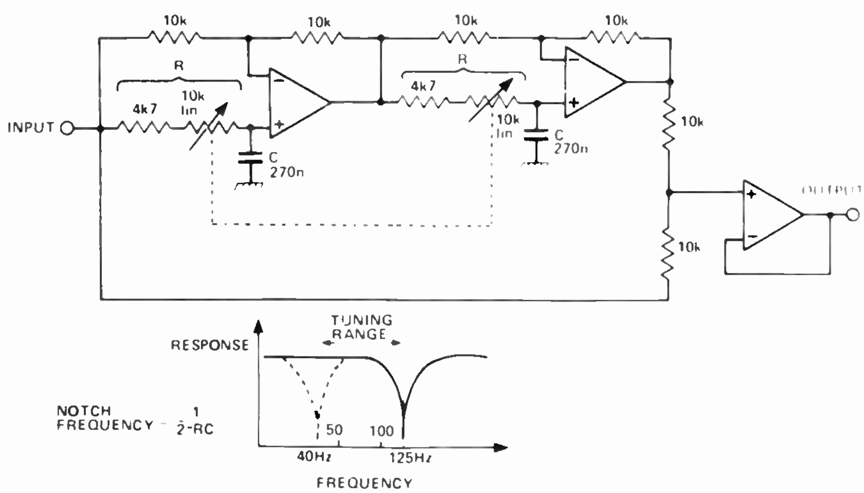
The circuit consists of a 12 V 50 Hz square wave shaper, this being a BC337 transistor followed by one flip-flop within a 4013 CMOS IC. The signal is then divided by two, using the other flip-flop of the IC, producing a 25 Hz square wave which is further buffered by a 2N5305 Darlington transistor. The latter drives the thyristor, a BT152. Note the two 1M0 and two 10k resistors in series; this combination overcomes the resistor voltage rating limitation.

Power to the logic circuit is provided by means of a diode pump. The 220n pump series capacitor is effectively connected across the mains and it should have a corresponding voltage rating (250 V AC suppression capacitor).

The circuit was tried with resistive loads of up to 1.5 kW. A further application would be to control resistive loads rated for 240 V AC operation (eg a 1 kW bar heater) to full, half or quarter power. This can be done using the additions shown in dotted lines.



Notch filter



An audio notch filter has many and varied applications. This circuit will provide a very 'deep' (high attenuation) notch in the input-to-output response at a frequency set by the value of the ganged-pot sections. With the circuit values shown, it is tuneable over a range from about 40 Hz to 125 Hz. Varying the value of C will shift the range up or down the audio spectrum. If you use internally compensated op-amps then no extra frequency compensation will be required. Types such as the NE5534 (N or AN) or TL071 are suitable, or multi-op-amp packs such as the LM324 or TL074 may be employed. Note that C should be a good-quality film or polycarbonate capacitor.

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This book discusses IC op-amps and their application in audio systems, and describes the numerous advantages of using op-amps, including small spatial needs, low power consumption, reliable performance and low cost. Assumes a basic understanding of op-amp theory.

UNDERSTANDING CMOS INTEGRATED CIRCUITS
21598P $9.95
This book tells you what CMOS ICs are, how they work, and how they can be used in electronic circuit designs. Many practical circuits, complete with parts values, are included.

DESIGN OF TRANSISTOR CIRCUITS WITH EXPERIMENTS
21626P $20.75
A self-teaching course to provide the background and explanations necessary to teach the reader the art of designing transistor circuits.

GUIDE TO CMOS BASICS, CIRCUITS, AND EXPERIMENTS
21654P $14.95
If you are already familiar with TTL devices and are ready to examine the benefits of CMOS, this book is your complete source. It tells you what CMOS devices are, their characteristics and design rules. 22 experiments demonstrate the concepts discussed.

PRACTICAL TRANSFORMER DESIGN HANDBOOK
21657P $35.50
An easy to understand, illustration-filled guide to designing and constructing transformers. Reviews the fundamentals of electricity, magnetism and algebra needed to understand transformer theory, and covers general design considerations, transformer types, power losses and transformer use in converters and inverters

Z80 MICROCOMPUTER DESIGN PROJECTS
21682P $20.75
This book provides a complete look at the internal architecture of the Z80, the heart of many microcomputers, and even shows how to build a microcomputer, the EX80, using this powerful chip.

DESIGN OF VMOS CIRCUITS, WITH EXPERIMENTS
21686P $17.50
The authors look at the technology which makes dramatic advancements possible with VMOS, and show how these components can easily and effectively be integrated into common circuit designs to enhance their responses.

IC OP-AMP COOKBOOK
21695P $23.75
Basic op-amp theory in detail, with 200 practical, illustrated circuit applications. JFET and MOSFET units are featured, plus manufacturers' data sheets and company addresses

EXPERIMENTS IN ARTIFICIAL INTELLIGENCE FOR SMALL COMPUTERS
21785P $13.25
Artificial intelligence is the capability of a device to perform functions normally associated with human intelligence. With this book, a small computer with extended BASIC and some knowledge of BASIC language, you can conduct interesting and exciting experiments in artificial intelligence.

PRACTICAL SOLID-STATE CIRCUIT DESIGN
21787P $14.95
An introductory course in practical solid-state circuit design for the experimenter, designer or technician who is interested in constructing tailor-made circuits

SCRS AND RELATED THYRISTOR DEVICES
21806P $19.25
Written for experimenters, technicians and engineers, this book is a practical and comprehensive guide to theory, operation, specifications and applications of silicon-controlled rectifiers (SCRs) and related thyristor devices

REGULATED POWER SUPPLIES
21808P $29.75
Comprehensive discussion of the internal architecture and operation of the latest solid-state regulators. Explains when regulated supplies are needed and how to incorporate them in your projects, and discusses modern circuitry including linear and switching circuits and late ICs

ANALOG INSTRUMENTATION FUNDAMENTALS
21835P $29.75
Numerous practical, hands-on lab experiments and solved problems are included, plus discussions of movements, dc ammeters, voltmeters, ohmmeters, bridges, filters and attenuators. No calculus is required.

RF CIRCUIT DESIGN
21868P $33.95
A practical approach to the design of RF amplifiers, impedance-matching networks and filters. Uses a minimum of complex maths.

SOLAR CELLS
22270P $37.95
In-depth description of the basic operating principles and design of solar cells. It also covers the techniques currently used to produce solar cells and reviews system applications.

ELECTRONIC DESIGN WITH OFF-THE-SHELF ICS
50274P $14.70
It contains virtually all the information you need to design and build electronic circuits, systems and subsystems with readily available ICs. Shows how to interface them into highly complex systems

MODERN FILTER DESIGN
94663P $49.95
This book details the advances in active RC filters, both from a practical standpoint and from a state-of-the-art point of view. It is the first book that gives detailed analysis and design procedures for switched capacitor filters.

COIL DESIGN AND CONSTRUCTION MANUAL
160B $6.56
How to make RF, IF, audio and power coils, chokes and transformers. Maths is simplified

50 PROJECTS USING CA3130 ICS
223B $4.32
The CA3130 is an advanced operational amplifier capable of higher performance than many others: circuits often need fewer ancillary components. Audio projects. RF projects. Test equipment. Household projects. Misc projects.

PRACTICAL INTRO TO DIGITAL ICS
225B $4.32
Introduction to digital ICs (mainly TTL 7400). Besides simple projects, includes logic test set to identify and test digital ICs. Also includes digital counter-timer

50 CIRCUITS USING GERMANIUM, SILICON AND ZENER DIODES
BP36 $3.36
50 interesting and useful circuits and applications using the germanium and silicon signal diodes, silicon rectifier diodes and zener diodes etc.

50 PROJECTS USING RELAYS, SCRS AND TRIACS
BP37 **$5.92**
Practical working circuits using silicon controlled rectifiers, relays and bi-directional triodes. With a minimum of difficulty you can use them in motor control, dimming and heating control, timing and light sensitive circuits, warning devices and many others.

50 FET PROJECTS
BP39 **$5.92**
Projects include amplifiers and converters, test equipment, tuners, receivers and receiver aids, mixers and tone controls etc etc. The FET used is not critical. This book is of interest and value to SW listeners, radio amateurs, hi-fi enthusiasts and general experimenters.

50 SIMPLE LED CIRCUITS
BP42 **$3.36**
50 interesting and useful circuits and applications using the LED. Also includes circuits for the 707 Common Anode Display for the beginner and advanced enthusiast.

IC555 PROJECTS
BP44 **$6.56**
One wonders how life went on before the 555! Included are basic and general circuits, motor car and model railway circuits, alarms and noise makers plus section on subsequent 556, 558 and 559s

PROJECTS IN OPTO-ELECTRONICS
BP45 **$5.92**
Included are simple circuits using ordinary LEDs as well as more sophisticated designs such as infra-red transmitters and detectors, modulated light transmission and also photographic projects etc.

RADIO CIRCUITS USING ICS
BP46 **$4.64**
This book describes ICs and how they can be employed in receivers for the reception of either amplitude or frequency modulated signals. Also discussed are stereo decoder circuits, quadrophonic circuits and voltage regulator devices.

LM 3900 IC PROJECTS
BP50 **$4.64**
Unlike conventional op-amps, the LM 3900 can be used for all the usual applications as well as many new ones. It's one of the most versatile, freely obtainable and inexpensive devices around. This book provides the groundwork for simple and advanced uses — it's much more than a collection of projects. Very thoroughly recommended.

50 CIRCUITS USING 7400 SERIES ICS
BP58 **$5.12**
50 interesting and useful circuits and applications using these inexpensive and versatile devices.

50 CMOS IC PROJECTS
224B **$4.64**
Projects include multivibrators, amplifiers and oscillators, trigger devices and other special devices.

SECOND BOOK OF CMOS IC PROJECTS
BP59 **$5.12**
Leading on from book number 224 '50 CMOS IC PROJECTS', this second book provides a further selection of useful circuits mainly of a fairly simple nature. Contents have been selected to ensure minimum overlap between the two books.

COUNTER DRIVER AND NUMERAL DISPLAY PROJECTS
BP67 **$5.92**
Well-known author F.G. Rayer features applications and projects using various types of numerical displays, popular counter and driver ICs, etc.

VMOS PROJECTS
BP83 **$6.56**
Though primarily concerned with VMOS power FETs and their applications, power MOSFETs are dealt with too, in a chapter on audio circuits. Projects include audio circuits, sound generator circuits, dc control circuits and signal circuits.

DIGITAL IC PROJECTS
BP84 **$6.56**
Helps the reader to develop a knowledge of the workings of digital circuits. Board layouts and wiring diagrams are included.

HOW TO USE OP-AMPS
BP88 **$7.52**
Design notes and applications on many topics including basic theory, amplifiers, power supplies, audio circuits, oscillators, filters, computers and control engineering. It's written around the 741 IC but includes design notes for most of the common op-amps.

ELECTRONIC TIMER PROJECTS
BP93 **$6.56**
These may have a high degree of accuracy with quartz control or they may be quite simple designs, using only a few components. A number of specialist timer projects are car windscreen wiper delay unit, darkroom timer, metronome etc.

ETI CIRCUITS BOOKS 1/2/3 **$2.95 ea**
Many of these circuits have been published in the 'Ideas for Experimenters' section in ETI

ETI CIRCUIT TECHNIQUES VOLS 1/2 **$4.75 ea**
The how, what, which, where, why and how much anthology of electronic components, circuits and techniques

test equipment and fault finding

AUTOMOTIVE TUNE-UP AND EMISSION CONTROL SERVICE
21712P **$20.75**
Car owners who wish to save money and maintain their cars at peak performance will learn from this book how to adjust, repair and maintain the systems that ensure best operation.

TROUBLESHOOTING WITH THE OSCILLOSCOPE
21738P **$15.95**
Excellent for the professional service technician or the serious hobbyist, as it combines step-by-step procedures for using the scope with the specific nuts and bolts of TV receiver troubleshooting.

EFFECTIVELY USING THE OSCILLOSCOPE
21794P **$14.95**
Excellent for the professional service technician or the serious do-it-yourself, as it combines the correct step-by-step procedures for using a scope with the specific nuts and bolts of TV receiver troubleshooting.

MICROCOMPUTER DESIGN AND TROUBLESHOOTING
21819P **$26.75**
Tells you how to design microcomputer systems and make them work without an expensive commercial development system or the need for costly test instrumentation. The author also provides a complete description of two popular microprocessors — the 8085 and the 6502

USE OF THE DUAL-TRACE OSCILLOSCOPE
40023P **$23.75**
This programmed text breaks down the process of operating a scope into a series of logical steps starting with the deflection of the electron beam and continuing through proper use of the triggering controls to measure the phase difference between two waveforms.

ELECTRONIC TROUBLESHOOTING HANDBOOK
52585P **$10.50**
This workbench guide shows you how to pinpoint transistor troubles in minutes, how to test almost everything electronic and how to get the most out of low cost test equipment.

PRACTICAL REPAIR AND RENOVATION OF COLOUR TVS
BP34 **$4.32**
This book shows how to obtain a working colour TV for very little outlay by repairing and renovating a set that has been 'written off' by a dealer. Includes practical details of how to construct your own CRT tester/rejuvenator and cross hatch generator.

HOW TO BUILD YOUR OWN SOLID STATE OSCILLOSCOPE
BP57 **$5.12**
The oscilloscope is divided into various sections which can be individually constructed and tested and then assembled together to complete the whole instrument. Also tells you how to use the instrument.

TRANSISTOR RADIO FAULT-FINDING CHART
BP70 **$1.92**
Used properly, this chart should enable the reader to trace most common faults quickly. Across the top of the chart are four rectangles containing brief descriptions of the faults. Selecting the appropriate fault, the reader simply follows the arrows and carries out the suggested checks in sequence until the fault is cleared.

ELECTRONIC TEST EQUIPMENT CONSTRUCTION
BP75 **$5.92**
Describes construction of wide range of test gear including FET amplified voltmeter, resistance bridge, field strength indicator, heterodyne frequency meter etc

POWER SUPPLY PROJECTS
BP76 **$5.92**
Includes simple unstabilised types, fixed voltage regulator types and variable voltage stabilised designs. The designs are all low voltage types for semiconductor circuits.

HOW TO GET YOUR ELECTRONIC PROJECTS WORKING
BP110 **$6.56**
Helps you to overcome the problems of a circuit that doesn't work by indicating how and where to start looking for many of the common faults that can occur when building up a project.

TEST GEAR — METERING AND POWER SUPPLY PROJECTS **$3.00**
Includes many types of meters, audio noise and signal generators, simple CMOS tester, oscilloscope calibrator etc.

TEST GEAR — VOL. 2 **$3.95**
Projects include audio oscillator, transistor tester, true RMS voltmeter, RF signal generator, versatile logic test probe, microwave oven leak detector etc.

ELECTRONIC PROJECTS FOR YOUNG SCIENTISTS **$3.95**
PH meter, geiger counter, helium-neon laser, sound level meter, solar cells, negative ion generator and much more.

electronic music/audio/video

AUDIO CYCLOPEDIA
20675P **$66.00**
A complete in-depth look at the art of audio — from the basic principles of sound to solid-state and integrated circuits. Over 3000 entries and hundreds of illustrations and circuit diagrams cover acoustics, amplifiers, recording, reproduction, test equipment, audio measurements, and much more.

ELECTRONIC MUSIC CIRCUITS
21833P **$24.95**
How to build a custom electronic music synthesiser, outlines numerous other circuit designs and then shows you how to modify them to achieve particular responses. Many of the circuits can be used as special-effects boxes for guitars and other musical instruments.

INTRODUCTION TO ELECTRO-ACOUSTIC MUSIC
81515P **$15.95**
This book assumes no previous technical knowledge. It discusses the relationship between the technology and the composition of electro-acoustic music.

MODERN RECORDING TECHNIQUES
21037P **$19.25**
Explains the equipment controls and techniques found in a modern recording studio and how to use them creatively and correctly to produce a desired result. Numerous photographs, diagrams and charts.

SOUND SYSTEM ENGINEERING
21156P **$32.50**
Dealing with audio systems as a whole, it includes installing and equalising the sound system and interfacing the electrical and acoustic systems. Instrumentation, the acoustic environment and designing for acoustic gain are covered.

TUBE SUBSTITUTION HANDBOOK
21746P **$8.75**
Complete, accurate, up-to-date guide to direct substitutes for receiving and picture tubes. Contains over 6000 receiving tube substitutes, over 4000 monochrome and colour picture tube substitutes, and 600 communications substitutes. Also includes pinouts for quick operational checks.

HOW TO BUILD SPEAKER ENCLOSURES
20520P **$8.75**
A practical guide to the 'whys' and 'hows' of constructing high-quality top-performance loudspeaker enclosures.

ACTIVE-FILTER COOKBOOK
21168P **$21.95**
Learn how to construct filters of all kinds — highpass, lowpass, bandpass. The book is easy to understand — no advanced maths or obscure theory is used.

DESIGN OF ACTIVE FILTERS WITH EXPERIMENTS
21539P **$15.95**
Introduction to the theory, implementation and design of active filters using the 741 op-amp.

AUDIO IC OP-AMP APPLICATIONS
21558P **$13.25**
This book discusses IC op-amps and their application in audio systems, and describes the numerous advantages of using op-amps, including small spatial needs, low power consumption, reliable performance and low cost. Assumes a basic understanding of op-amp theory.

VIDEO TAPE RECORDERS
21521P **$17.50**
In this completely revised second edition, the author tells in simple language how helical VTRs work and how to operate and service them. Includes numerous examples of circuits and mechanical systems.

OOPS! More books!

CHEAP VIDEO COOKBOOK
21524P $11.75
Complete discussion of a new, low-cost way to get words, pictures and opcode out of your computer and onto any ordinary TV screen, using a seven-IC easy-to-build circuit which you can build for less than $20.

AN INTRODUCTION TO VIDEO
BP100 $6.56
This book is written in layman's language and is for anyone who is thinking about buying or renting or who has just bought or rented a video recorder and wants to get the best out of the machine.

MOBILE DISCO HANDBOOK
BP47 $4.64
Most people who start mobile discos know little about equipment or what to buy. This book assumes no preliminary knowledge and gives enough info to enable you to have a reasonable understanding of disco gear.

ELECTRONIC MUSIC AND CREATIVE TAPE RECORDING
BP51 $5.92
Shows how electronic music can be made at home with the simplest and most inexpensive of equipment. Describes how the sounds are generated and how these may be recorded to build up the final composition.

PRACTICAL CONSTRUCTION OR PREAMPS, TONE CONTROLS, FILTERS, ATTENUATORS
BP60 $4.96
This book shows the enthusiast how to construct a variety of magnetic tape recording, microphone and disc preamplifiers, and also a number of tone control circuits, rumble and scratch filters, attenuators and pads.

ELECTRONIC SYNTHESISER PROJECTS
BP81 $5.92
For the electronic music enthusiast, an invaluable reference. This book is full of circuits and information on how to build analogue delay lines, sequencers, VCOs, envelope shapers, etc etc. The author takes a clear and logical approach to the subject that should enable the average enthusiast to understand and build up what appears to be a quite complex instrument.

AUDIO PROJECTS
BP90 $6.56
Covers a wide range of audio projects including preamplifiers and mixers, power amplifiers, tone controls and matching etc. A number of board layouts and wiring diagrams are included.

ELECTRONIC MUSIC PROJECTS
BP74 $5.92
Provides constructors with practical circuits for the less complex music equipment including fuzz box, waa-waa pedal, sustain unit, reverb and phaser, tremolo generator etc. Text covers guitar effects, general effects, sound generators, accessories.

SONICS 1982 YEARBOOK $5.35
An interview with Kraftwerk, how to cope with recording, lighting, rock acoustics, guitars, equipment reviews and more.

SONICS MAGAZINE $2.35 ea
The Australian music magazine dedicated to the art and craft of sound. Published April, July, October. Yearbook in December. $15 for one year subscription. Please indicate starting issue.

computers for beginners

COBOL FOR BEGINNERS
39378P $21.95
It is a solid text for introductory programming courses in Cobol, using a format that is easy to understand, yet comprehensive enough to make supplementary readings unnecessary.

THE PET PERSONAL COMPUTER FOR BEGINNERS
61827P $20.95
This handy guide is written for use with all varieties of PET computer, from the original 2001 to the new 8032 Super PET. It is suited to novices with no practical experience and provides advice and practical examples.

BIG THINGS FROM LITTLE COMPUTERS
77859P $19.25
A layperson's guide to personal computing with all the basic information and lots of examples of how personal computers can be used.

BEGINNER'S GUIDE TO DIGITAL ELECTRONICS
BP61 $3.36
Covers all essential areas including number systems, codes, constructional and sequential logic, analogue/digital/analogue conversion.

BEGINNER'S GUIDE TO MICROPROCESSORS & COMPUTING
BP66 $5.92
Introduction to basic theory and concepts of binary arithmetic, microprocessor operation and machine language programming. Only prior knowledege assumed is very basic arithmetic and an understanding of indices.

A MICROPROCESSOR PRIMER
BP72 $5.92
Learning about microprocessors is easy with this book, written in a style that is easy to follow. The shortcomings of this basic machine are discussed and the reader is shown how these are overcome by changes to the instruction set. Relative addressing, index registers follow as logical progressions.

AN INTRO TO BASIC PROGRAMMING TECHNIQUES
BP86 $6.56
Ideal for beginners seeking to understand and program in BASIC. Book includes program library for biorhythms, graphing Y against X, standard deviations, regressions, generating musical note sequences, and a card game.

BEGINNING BASIC
39806A $19.95
Intended for beginners with no computing experience one should be able to intelligently program in BASIC in a short time.

BEGINNING FORTRAN
46011A $19.95
Starts with simple elementary examples and proceeds to intermediate level programs. Also includes references, tutorials, flow charts, deck set-ups and matrix algebra.

UNDERSTANDING COMPUTERS
39815A $17.95
This book describes how computers work. For people who use small computers, it starts with the most elementary gates and works up to the complete computer. Gives an understanding of languages and how they operate in the computer.

NAILING JELLY TO A TREE
39842A $24.95
This guide to software teaches you about machine language, assembly language programming and BASIC. The emphasis is not on learning to write programs but on learning to use the thousands of available programs that have already been written.

PEANUT BUTTER AND JELLY GUIDE TO COMPUTERS
39813A $14.95
A simple, easy-to-digest source of information on personal computing for the potential buyer who is less than an expert in the field.

INTRODUCTION TO WORD PROCESSING
88076A $17.95
Written for the non-technical reader, this book tells about the concepts common to all word processing systems, then analyses all features in detail.

YOUR FIRST COMPUTER
88045A $12.50
An easy-to-understand beginner's book to small computers. Understanding them, buying them and using them for personal and business applications.

FROM CHIPS TO SYSTEMS: AN INTRODUCTION TO MICROPROCESSORS
88063A $19.95
Explains exactly what a microcomputer system is and how it works. Introduces fundamental concepts and covers all aspects of microprocessors and related components, internal operation, memories, interfacing and system development etc.

COMPUTERS FOR EVERYBODY
39849A $8.95
In this easy-to-understand book it is explained how a computer can be used at home, in the office or at school. Includes a consumer's guide to computer equipment that will help the reader decide what to buy and who to buy it from.

computers hardware & techniques

USING THE 6800 MICROPROCESSOR
21512P $13.25
This will guide the reader through the conception, configuration, writing and running of a variety of programs that demonstrate practical use of a 6800 system.

Z80 MICROCOMPUTER DESIGN PROJECTS
21682P $20.75
This book provides a complete look at the internal architecture of the Z80, the heart of many microcomputers, and even shows how to build a microcomputer, the EX80, using this powerful chip.

MICROPROCESSOR CIRCUITS VOL. 1
21877P $14.75
Presents basic microprocessor concepts in simple language for beginners and teaches you to construct a useful microcontroller system. Offers 30 demo circuits which take you through assembly, operation and programming of a microcontroller.

INTERFACE PROJECTS FOR THE APPLE II
69387P $15.95
A series of interface projects that are easily built and enable the user to realise the computer's potential through project construction. Projects are primarily hardware-orientated, with some software supporting the hardware.

PET INTERFACING
21795P $25.25
Demonstrates how to build numerous interfacing devices for PET hardware. BASIC language programs are used throughout, and the book includes a discussion of the microprocessor's internal architecture and general hardware/software interfacing.

6809 MICROCOMPUTER PROGRAMMING AND INTERFACING, WITH EXPERIMENTS
21798P $21.95
Gives a solid understanding of how to program and interface the high-performance 6809 microprocessor. The author completely explores internal structure, addressing modes, data movement instructions, registers, arithmetic logic and test instructions for the 6809.

Z80 MICROCOMPUTER HANOBOOK
21500P $17.50
This thorough handbook covers hardware, software and microcomputers built around the Z80.

THE S100 ANO OTHER MICRO BUSES
21810P $13.25
The key to successful computer expansion is a complete understanding of the bus system, through which the computer communicates with peripherals. This book will give you that understanding.

MICROCOMPUTER DESIGN ANO TROUBLESHOOTING
21819P $26.75
Tells you how to design microcomputer systems and make them work without an expensive commercial development system or the need for costly test instrumentation. The author also provides a complete description of two popular microprocessors — the 8085 and the 6502.

DON LANCASTER'S MICRO COOKBOOK, VOLUME 1
21828P $20.75
This 'cookbook' starts with the very fundamentals of microprocessors and microcomputers and takes you through number systems, codes, memory, etc. until you can work intelligently with micros.

DON LANCASTER'S MICRO COOKBOOK, VOLUME 2
21829P $20.75
Carries on where Volume 1 left off.

APPLE INTERFACING
21862P $15.95
Using this book, you will be able to perform useful experiments which will provide a much clearer understanding of the fundamentals of computer interfacing and computer electronics. A better understanding of interactions between hardware and software will enable you to communicate more effectively with your Apple.

MICROPROCESSOR CIRCUITS VOL. 1
21877P $14.75
Presents basic microprocessor concepts in straightforward language for beginners. Teaches you to construct a useful microcontroller system through progressive demonstration circuits.

8080 MICROCOMPUTER EXPERIMENTS
39808A $29.50
This hands on book includes 105 experiments presenting programs and diagrams as required for clarification.

A STEP-BY-STEP INTRODUCTION TO 8080 MICROPROCESSOR SYSTEMS
39804A $16.95
Doesn't require any electronics or computer background. This book describes the 8080 architecture and instruction set through simple examples. Some basic software is introduced.

DIGITAL CIRCUITS WITH MICROPROCESSOR APPLICATIONS
46032A **$39.50**
An introductory text, this book provides readers with the basic ideas and tools needed to analyse and design digital circuits and computer systems. Discusses microprocessor computer organisation, machine language number systems and gate circuits

MICROPROCESSOR INTERFACING TECHNIQUES
88029A **$24.95**
Teaches you how to interconnect a complete microprocessor system and interface it to the usual peripherals. The hardware and software skills needed to effectively interface peripheral devices are covered along with various buss standards and A/D conversion.

PRACTICAL INTRO TO DIGITAL ICS
225B **$4.32**
Introduction to digital ICs (mainly TTL 7400). Besides simple projects, includes logic test set to identify and test digital ICs. Also includes digital counter-timer

BEGINNER'S GUIDE TO MICROPROCESSORS & COMPUTING
BP66 **$5.92**
Introduction to basic theory and concepts of binary arithmetic, microprocessor operation and machine language programming. Only prior knowledge assumed is very basic arithmetic and an understanding of indices

A MICROPROCESSOR PRIMER
BP72 **$5.92**
Learning about microprocessors is easy with this book, written in a style that is easy to follow. The shortcomings of this basic machine are discussed and the reader is shown how these are overcome by changes to the instruction set. Relative addressing, index registers follow as logical progressions.

PRACTICAL COMPUTER EXPERIMENTS
BP78 **$5.92**
How to build typical computer circuits using discrete logic. This book is a useful intro to devices such as adders and storers as well as a general source book of logic circuits.

THE 6809 COMPANION
BP102 **$6.56**
It is not a beginners introduction to microprocessors in general but a discussion of the features of the 6809 and a reference work for the 6809 programmer in particular

COMPUTERS & COMPUTING YEARBOOK 1980
$4.95
Includes beginners buying guide, the Apple, Tandy's TRS-80, the Vector MZ, introducing BASIC, S100 VDU, EPROM programmer, microcomputer power supply and lots more

COMPUTERS & COMPUTING YEARBOOK 1982
$4.95
Includes disks, CP/M and your computer, learners microcomputer, programming in CHIP-8, alphasort, fast plotter, PET talk, the System 80 etc

computing software

CP/M PRIMER
21791P **$21.95**
A complete one-stop course on CP/M, the very popular operating system for 8080, 8085 and Z80-based microcomputers. Complete terminology, hardware and software concepts, startup of a CP/M system, and a complete list of CP/M-compatible software.

THE CP/M HANDBOOK (WITH MP/M)
88048A **$19.95**
Contains a step-by-step description of all the CP/M command features. Designed for the beginner, the book progresses to detailed explanations of the file transfer program, the debugging program and CP/M's text editing program.

HOW TO GET STARTED WITH C''/M
39832A **$19.95**
This practical book eases the r ader into the essentials of the system, giving an overvie of the operating system, an idea of what it will be like to se and what it can do for the reader.

AUSTRALIAN MICROCOMPUTER HANDBOOK
72505 **NOW $15.00**
Normally $25.00. A detailed buyer's guide to microcomputer systems and application packages in commercial industrial, scientific, educational and home/hobby areas

THE C PROGRAMMING LANGUAGE
10163P **$21.95**
C is a general purpose 'low-level' programming language. It is not specialised to any particular area of application, but its absence of restrictions make it convenient and effective for many tasks.

THE 68000: PRINCIPLES AND PROGRAMMING
21853P **$19.95**
An easy-to-read, systematic approach to the 68000 advanced 16-bit microprocessor. The book guides you through the complex architecture, instruction set, pinouts and interfacing techniques. Written for design engineers, programmers and students

PROGRAMMING IN BASIC FOR PERSONAL COMPUTERS
30739P **$14.75**
Simple instructions show how to give BASIC commands and statements a wide range of applications, from programming video games to developing business or scientific programs

PROGRAMMABLE CALCULATORS
46008A **$24.95**
This book suggests which calculators to buy, their possibilities and limitations, and the how-tos of programming them

TAKE A CHANCE WITH YOUR CALCULATOR
39807A **$14.95**
An introduction to modern mathematics, this book deals with programming of programmable calculators and includes probability problems

AN INTRO TO BASIC PROGRAMMING TECHNIQUES
BP86 **$6.56**
Ideal for beginners seeking to understand and program in BASIC. Book includes program library for biorhythms, graphing Y against X, standard deviations, regressions, generating musical note sequences, and a card game

BASIC FOR EVERYONE
61481P **$19.75**
349 pages of BASIC information for all purposes

BEGINNING BASIC
39806A **$19.95**
Intended for beginners, this book discusses how a programmer and a basic computer interact with the computer, problems likely to be met by the beginner, the need for and uses of documentation etc

FIFTY BASIC EXERCISES
88056A **$17.95**
Designed to teach BASIC through actual practice, this book contains graduated exercises in math, business, operations research games and statistics. The programs were designed to run directly on a TRS-80 and will run with minor or no changes on any system with Microsoft BASIC.

INSIDE BASIC GAMES
88055A **$19.95**
The medium of games teaches readers how to design error-free, interactive BASIC programs. Rules, algorithms and coding differences for the PET, APPLE II and TRS-80 are also included

MICROSOFT BASIC
39823A **$19.95**
Includes branching and loops arithmetic in BASIC, strings, editing, arrays and files, the disk and a description of the Radio Shack Level II BASIC.

INTRODUCTION TO FORTH
21842P **$14.95**
The most complete book available on the MMS FORTH version of FORTH, but also a fundamental approach to programming in all versions of FORTH. Many programming examples are provided, with direct comparisons to the Microsoft Level II BASIC version of these programs.

STARTING FORTH
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