# Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

VOL. 25 NO. 2

JAN. 18, 1977


**The growing choice of software** development aids for µPs can confuse even the experienced programmer. Moreover, the range of features differs widely even for similarly named aids. Cost, time and available memory size are yardsticks that simplify your selection decision. For a look at what's available turn to p. 20.

Here are three electromagnetic X-Y display scopes that have a lot in common: each has a big 12-inch diagonal CRT, is economically priced, and is ideal for applications requiring continuous monitoring of response signals with bandwidths up to 15 kHz.

The one in front is specifically for use in OEM systems. With the Model 1951, you can have controls mounted on the rear panel, or they can be pre-set on an easily accessible PC board. And the unit's power supply can be removed and installed elsewhere in your system. The 1951 is particularly well suited to medical electronic systems.

The scope on the left is our Model 1901C which can be used with our (or anybody's) RF or microwave sweepers. The unit has a sensitivity of 1 mV per division which is ideal for low-level detection requirements. Features such as Z axis intensity modulation, Y marker adders and a blanking protection circuit contribute to the unit's versatility.

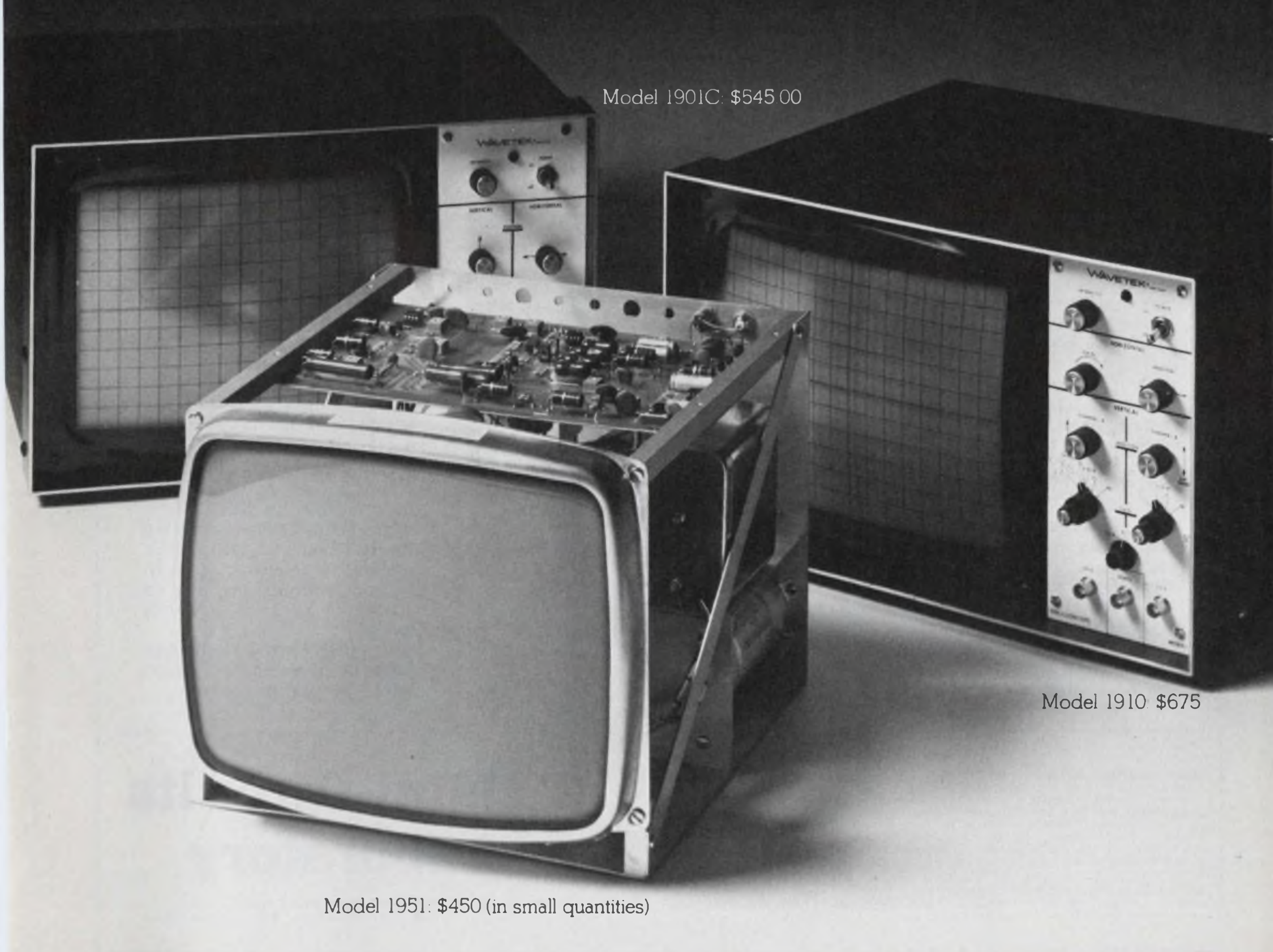
Finally, the scope at right is our Model 1910. It's basically the same as the 1901C except that it provides dual trace capability.

So just decide which of these low-priced scopes has the most in common with your operation. We'll be happy to ship as many as you want. WAVETEK INDIANA, P.O. Box 190, Beech Grove, Indiana 46107, Telephone (317) 783-3221, TWX 810-341-3226.

WAVETEK®

**CIRCLE NUMBER 2**

# Scope City!



Model 1901C: $545.00

Model 1910: $675

Model 1951: $450 (in small quantities)

# Tough... Tougher!

# DOUBLE BALANCED MIXERS



**Model SBL-1**

**$2.95** 500 pieces

$3.95 (10-49)

For demanding industrial and commercial applications, where low-cost and high-performance are critical, model SBL-1 will fill your need.

Don't let the low price mislead you. Only well-matched, hot-carrier diodes and ruggedly constructed transmission-line transformers are used. Every SBL-1 is RF tested four times, and every solder connection is 100 percent inspected under a high-power microscope. Internally, every component is bonded to the header and metal case for excellent protection against shock.

Of course, our one-year guarantee applies to these ruggedly constructed units.

| Model SBL-1 | | Model SRA-1 |
|---|---|---|
| LO 1-500<br>RF 1-500<br>IF DC-500 | **Frequency Range, MHz** | LO 0.5-500<br>RF 0.5-500<br>IF DC-500 |
| Typ. Max. | **Conversion Loss, dB** | Typ. Max. |
| 5.5 7.5 | One Octave from Band Edge | 5.5 7 |
| 6.5 8.5 | Total Range | 6.5 8.5 |
| +1dBm | **Signal, 1dB Compression Level** | +1dBm |
| Typ. Min. | **Isolation, dB** | Typ. Min. |
| 50 35 LO-RF<br>45 30 LO-IF | Lower Band Edge to One Decade Higher | LO-RF 50 45<br>LO-IF 45 35 |
| 45 30 LO-RF<br>40 25 LO-IF | Mid Range | LO-RF 45 30<br>LO-IF 40 25 |
| 35 25 LO-RF<br>30 20 LO-IF | Upper Band Edge to One Octave Lower | LO-RF 35 25<br>LO-IF 30 20 |
| 50 ohms | **Impedance, All Ports** | 50 ohms |
| | **Phase Detection** | |
| 1mV typical<br>Negative | DC Offset<br>DC Polarity | 1mV typical<br>Negative |
| | **Electronic Attenuation** | |
| 3dB | Minimum Attenuation (20mA | 3dB |

**Model SRA-1**

**$7.95** 500 pieces

$9.95 (1-49)

For stringent military, space or commercial applications, model SRA-1 has become the industry standard. Packaged within an RFI shielded metal enclosure and hermetically-sealed header, these high-performance units are specified by branches of the Dept. of Defense, NASA, FAA and major communications firms. Each Schottky diode is preconditioned by the *HTRB technique, (with the diode operated for 168 hours at 150°C with one-volt reverse bias applied), to accelerate aging and to screen out potentially unreliable units.

Our SRA-1 is the only double-balanced mixer in the industry with a two-year guarantee.

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**CIRCLE NUMBER 3**

VOL. 25 NO. 2
JAN. 18, 1977

# Electronic Design®

FOR ENGINEERS AND ENGINEERING MANAGERS

## NEWS



## TECHNOLOGY



## PRODUCTS



## DEPARTMENTS



**Cover:** Photo by Lennie Zbiegien, courtesy of Motorola, Phoenix, AZ.

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| Device | Size | Supply Voltages | Worst Case Access Time (nanoseconds) | Comments |
|---|---|---|---|---|
| Am9214 | 512 x 8 | +5 | 500 | Plug in replacement for 3514 |
| Am8308 | 1024 x 8 | ±5, +12 | 450 | |
| Am9208 | 1024 x 8 | +5, +12 | 250 | Plug in replacement for 8308 |
| Am8316A | 2048 x 8 | +5 | 850 | |
| Am9217 | 2048 x 8 | +5 | 450 | Plug in replacement for 8316A |
| Am8316E | 2048 x 8 | +5 | 450 | |
| Am9218 | 2048 x 8 | +5 | 350 | Plug in replacement for 8316E. |
| Am9216 | 2048 x 8 | +5, +12 | 300 | |

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CIRCLE NUMBER 4

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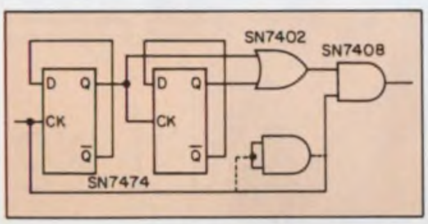
# Across the Desk

## Murphy vs Wolfe

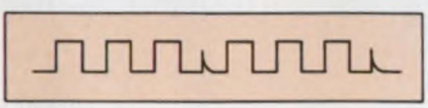
On page 7 of the November 22 issue of Electronic Design, we compared Murphy's Law with Wolfe's Law. Murphy won. We identified Jim Wolfe as general manager of Centralab Electronics, which is correct, and as vice president of Gould Inc., which is wrong. Mr. Wolfe is vice president of Globe-Union.

## Watch for the glitch

The frequency-division techniques presented by Cornelis van Holten and Jan Obdralék (ED No. 18, Sept. 1, 1976, p. 104) are most useful. When they are implemented, however, the problem of "glitches" immediately arises. The authors' Fig. 1 shows a × 3/4 multiplier that can be implemented as follows:

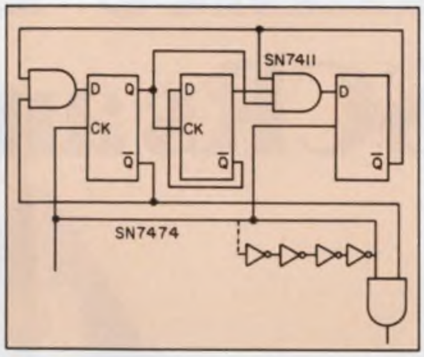



The propagation delays introduced by the second flip-flop produce the waveform shown:



The glitch is marginally recognized as an additional pulse that stops frequency division under some conditions. Inserting another AND gate as shown delays the clock pulse until the output of the OR gate reaches its true value, thereby producing a "glitch-free" output.

The × 3/5 multiplier shown in the authors' Fig. 2 is perhaps not so obvious in its implementation. A satisfactory way to do it is shown below:




In this case the output contains a severe glitch that can be removed by inserting four inverters, as shown. Internal to the multiplier is a glitch at the D input to the third stage divider. Since it occurs after the clock pulse on that divider stage, it is ignored.

*Stanley Wood*

Star Route
Box 176
Inyokern, CA 93527

## Misplaced Caption Dept.

I knew we should have checked out that radar set before we left.

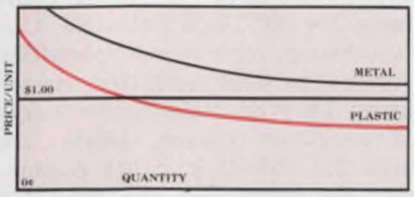
Sorry. That's Theodore Gericault's "The Raft of the Medusa," which hangs in The Louvre in Paris.

*(continued on page 10)*

**Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Managing Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld on request.**

# Can Metal Can!

**Motorola TO-220**
## First to Save 30%




Save ⅓ out of your next thyristor buck by specifying Motorola TO-220 SCRs and Triacs.

And get better performance!

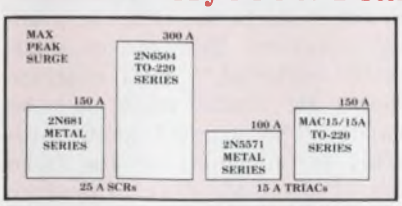
These 25 A SCRs and 15 A Triacs actually cost ⅓ less than comparable RCA and GE metal studs in almost any quantity.

The 2N6504–09 SCR is a natural-born replacement for those goodie-but-oldie 2N681-series sockets where you're operating to max limits set by data sheet ratings . . . motor and heating controls, power supplies, battery chargers, crowbars, ad infinitum.

It's got super low, 1.8 V max $V_F$ at 50 A peak or just 26 W $P_D$ at full rated current. You can heat sink to 85°C case with lower thermal excursions and potentially longer life.

Use MAC15/15A Triacs for full-wave designs and realize the same ⅓ saving! Like the SCR, it blocks to 800 V and operates from −40°C to 125°C.

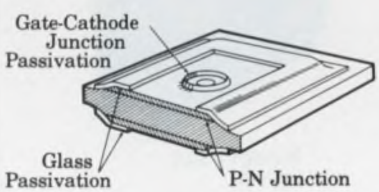
**Motorola TO-220**
## First to Defy 300 A Peaks




Whoever heard of a TO-220 SCR with 300 A peak surge ratings? You did — exclusively from Motorola.

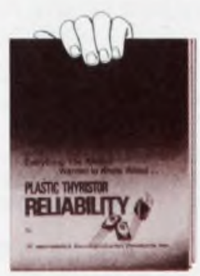

That's *twice* the performance available from 2N681 metal studs in less than half the space.

We've maximized the technology in TO-220 to state-of-the-art levels by enlarging the active die area approximately 15% in each package — SCR and Triac — so much more capability is available than from any other comparable plastic OR metal package.




And who else but the industry's technology leader would offer the only truly upgraded thyristor process technology to come down the road since glassivation began — Photo-Glass.

Result? Total assurance that voids, moisture and impurity penetration don't exist — but excellent reliability does.




**Motorola TO-220**
## First to Raise Reliability

Our TO-220s can take almost anything you can throw at them.

Like worst-case, full-on, full-off power cycling with package temps reaching 'way beyond your design limits . . . 95°C excursions.

Our plastic packages survived 43 MILLION of these power cycles with just 15 failures. An MTTF of 3 MILLION cycles!

Or blocking life tests at rated ambients. Our TO-220s survived 279,000 hours with zero failures.

Or 100 days at MIL-S-750 conditions — 92% to 98% relative humidity with units alternately drenched, then dried, during 24-hour cycles. Just one failure.

Motorola TO-220s can take it. Our brochure proves it.

**Motorola Thyristors**
## First in Price, Quality, Availability

There is nobody else with more to offer in SCRs and Triacs to 40 Amps than Motorola. Check it out.


And the best costs even less now through Motorola's unmatched volume production capability.

We won't be undersold. By anyone.

Try us. Contact an authorized distributor, sales rep or Box 20912, Phoenix, AZ 85036 for Guide to Thyristors and Everything You Always Wanted To Know About Reliability.

See the Plastic SCR and Triac world for what it really is. Motorola's.

**MOTOROLA Semiconductors**

CIRCLE NUMBER 8

## ACROSS THE DESK

*(continued from page 7)*

### The response was great, but they don't sell it

In the list of suppliers that followed your article on conductive elastomers (ED No. 23, Nov. 8, 1976, p. 60), you included our client, Instrument Specialties Company, Inc., of Little Falls, NJ. Unfortunately, Instrument Specialties does *not* produce conductive elastomers. They do make finger strips of beryllium copper, which are used for shielding. Since conductive elastomers are also used for this purpose, perhaps the confusion occurred in this connection.

You should know that Instrument Specialties and its reps have received many phone calls and letters from prospective customers for conductive elastomers. When the reps tell the callers that Instrument Specialties does not make this product, the callers frequently become irate, and accuse the rep of being stupid and not knowing what his company manufactures—since, after all, "Electronic Design says you do make it."

*David Levy*
*President*
Levy Advertising Associates, Inc.
1 Rockefeller Plaza
New York, NY 10020

### What was the point?

I read with interest Editor-in-Chief George Rostky's editorial on planning ahead (ED No. 15, July 19, 1976, p. 61). As an admirer of the various management techniques, I have also at times wondered if all the "paper work" they call for is worth the effort in practical situations. However, on reading the editorial, I can't conclude whether Mr. Rostky wants us to be Charlie (who worried about producing instruments) or Joe (who worried about planning to produce instruments).

*R. Venkatraman*
*Deputy Manager*
Bharat Electronics Ltd.
Jalahali, Bangalore -560013
India

*Ed. note: It depends on whether you want to produce instruments or paper.*

# "As the first interactive small plotter, it was the only intelligent choice."

**Problem: Until now, no small plotter could carry on an intelligent conversation.**

Because most B-sized plotters have been pretty much the same: slow, unreliable, and dumb. Even with large off-line plotters you can wait hours, even days, for results ... and if there's a mistake—start over.

**Solution: Tektronix' new microprocessor-based 4662. For interactive plotting, page scaling, digitizing, and camera-ready output. Just $3995.†**

The 4662 is the first smart buy among 11"x17" flatbed plotters. Its digital design and vector generation offer exceptional accuracy and repeatability without drift or slidewire dirt build-up. Its 1600-byte buffer lets the host work while the 4662 plots ... at speeds up to 22 ips.

**It's the first B-sized plotter with graphic input.** Digitizing capability and built-in joystick mean you can input corrections in seconds, experiment with designs, and run off camera-ready copies practically as fast as you load paper.

**It's plug-to-plug compatible with virtually any RS-232 system ... from minis to mainframes.** You can plot circles around any other B-sized plotter, for about the same price as the competition. For a demonstration, call your local Tektronix Sales Engineer, or write:

The 4662 contains its own character generator, alpha rotation, and page scaling, thus minimizing support software. Proven graphic and plotter software is provided by Tektronix.

**Tektronix, Inc.**
Information Display Group
P.O. Box 500
Beaverton, Oregon 97077
**Tektronix Datatek NV**
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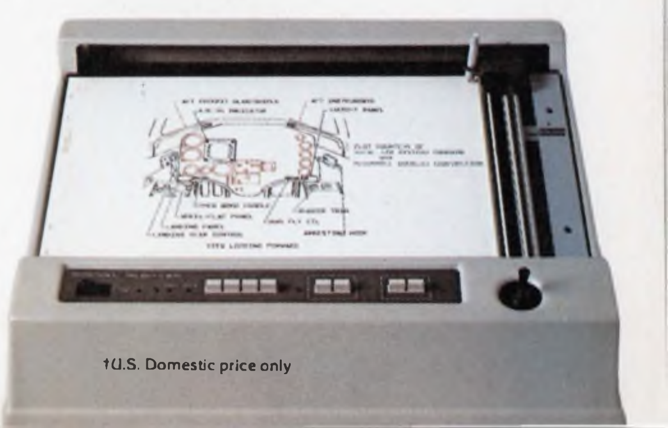
Badhoevedorp, The Netherlands

## The 4662. Plug it in. It speaks for itself.

TEKTRONIX®



†U.S. Domestic price only

# At long last! A that doesn't do

# Touch & Trigger

## Automatic displays to 25 MHz at 2 mV

As illustrated, the PM 3212 has an impressive combination of features that add up to unbeatable all-round performance.

Bandwidth, sensitivity, triggering facilities, weight and dimensions are all what you expect for $ 1155.00*

* US domestic price only

*"Auto" triggering on the PM 3212 is more than a trace finder – much more. In this mode not only is a zero line displayed when there is no input signal, but in the presence of a signal the trigger level is derived from the peak-to-peak amplitude of the signal. This gives instant and unambiguous triggering for a wide variety of measurement conditions.*

But we give you more. A brighter trace, a sharper display, a double insulated supply, battery operation and versatile X-Y facilities. And the usual Philips plus: the unbeatable front panel layout.

**For further information contact, Philips Test & Measuring Instruments, Inc.**

*Continuously variable timebase for easier measurements of phase, for timing comparisons and to avoid "double writing" problems in digital applications.*

*Automatic TV triggering at the touch of a button. Frame triggering occurs in the lower sweep speeds, changing over automatically to line from 200 µs/div upwards.*

*High light output displays through 10 kV tube. Small spot size. Continuously variable illumination of fine-line internal graticule.*

*Composite triggering when both buttons are depressed. When used in the alternate mode this gives a stable display of two unrelated signals.*

*DC coupled triggering without which variable duty cycle waveforms cannot be handled. This is a vital feature for digital measurements.*

*Level control can be used instead of "Auto" when the instrument needs to be triggered at an exact point in the input signal.*

*PM 3212 has compact dimensions of 445 x 300 x 145 mm (l x w x h). Weight approx. 7.9 kg (17.4 lb)*

*Double-insulated power supply eliminates need for earth connection (i.e. 2-wire line cord).*

*Any of the selected trigger sources can be switched to the horizontal channel.*

*Separate source triggering for unambiguous, stable displays without the inconvenience of changing probes.*

*Carrying handle automatically protects crt and controls.*

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**PHILIPS**

**FOR INFORMATION CIRCLE #260**

**FOR DEMONSTRATION CIRCLE #261**

# News Scope

JANUARY 18, 1977

## Put your product in space and see what happens

Ever wonder what would happen to your firm's product if it were sent into space? How it would react to intense solar radiation, bombardment with micrometeorites and charged particles, or exposure to high vacuum and low gravity. The National Aeronautics and Space Administration is providing the first opportunity to find out—for free.

The opportunity is a project called the University Space Experiments (USE), which is open to the electronics industry for comparative studies of shieldings, coatings and circuitry implemented in various technologies, such as TTL, MOS and SOS.

Beginning in 1979, NASA will put into orbit its long-duration exposure facility (LDEF) satellite for six months at a time. An open aluminum frame cylinder 30 ft long and 14 ft in diameter, the satellite can expose more than 70 different experimental packages directly to the solar winds.

Colonization of the moon and other planets will require commercial equipment that stands up to the rigors of outer space," says Dr. M. H. Davis, program director of LDEF/USE. "We are particularly interested in encouraging potential experimenters who haven't had previous experience in space research."

The experiments can either utilize the orbital environment or study it. Housed in NASA-supplied trays, 50 in. long, 38 in. wide and up to 12 in. deep, the experiments will be mounted around the periphery of the satellite, facing outward. The cylinder will maintain a constant attitude toward earth. An experimenter can request a particular location on the satellite for his experiment.

Simple experiments are particularly well-suited to the LDEF mission because no essential power source or telemetry can be provided. Consequently, each experiment must be self-sufficient—that is, it must be electromagnetically passive and draw power either from solar cells or a battery pack. The satellite's payload is limited to 175 lb of equipment in each tray. However, a large experiment can be mounted inside the structure. And power facilities may become available on subsequent flights.

The LDEF satellite will be borne aloft by a space shuttle and left in near-circular orbit whose period will last 90 min. and whose altitude will be 300 nautical miles (556 km). After the six-month period, the shuttle will retrieve it.

The LDEF program is being coordinated by the Universities Space Research Association (USRA), which is a consortium of some 50 universities and a branch of NASA. "Our program has no deadlines and is noncompetitive, but industry applicants should be able to relate their experiments to an academic institution in order to qualify for the 'no cost' status. USRA will assist them in doing this."

Firms interested in participating in the LDEF/USE program should write to USRA, P.O. Box 3006, Boulder, CO 80307, or telephone (303) 449-3414.

## Elephant with μP brain skates in Rose Parade

One of the more unusual sights during the 1977 Tournament of Roses Parade was a panic-stricken mother elephant with a mouse on her trunk, pulling a baby elephant in his red wagon. The "mother" had roller skates on its feet and a microprocessor for a brain.

Designed and built by engineering students at California State Polytechnic University, the 16-ft tall model pachyderm's animation is built around a Rockwell PPS-4 microprocessor and 4 kbits of PROM, 4 kbits of RAM and 40 channels of I/O.

The I/O channels monitor and control the position of the big elephant's legs, trunk, head and eyes. Potentiometers inputted to a/d converters detect the positions of the float's animated parts instantaneously. The progress of all the motions is monitored by a PROM-resident supervisor program in the μP-based control system.

A control panel enables the float's crew of four to modify and enhance the sequence of actions to obtain the most dramatic effect. And since the float's actual animation sequence is stored on cassette tape and loaded into RAM, the μP system is flexible enough to be used in other floats and displays.

"This is the first Rose Parade float to use a microprocessor," says Doug Dubrall, Electronics chairman of Cal Poly's Rose Bowl Committee.

The animation includes side-to-side roller skating by the mother elephant, up and down swaying of her trunk, rolling head, blinking eyes and bending knees. The baby elephant in the wagon holds a pinwheel that spins. For safety, limit switches are located at the extreme ends of motion.


**Artists sketch** of μP-controlled elephant float in Rose Bowl parade.

## New standard to improve computer security

A new federal data encryption standard to be released by the Commerce Dept. is aimed at improving the security of computer data.

Registered as FIPS PUB 46, the standard will be "the first publicly available standard that can be used to provide a high level of protection for computer data," says Ruth M. Davis, director of the Institute for Computer Sciences and Technology at the National Bureau of Standards.

Hardware is used to encrypt (reduce to cipher) and decrypt (decipher) digital information. Encryption is accomplished by electronic devices that implement the mathematical algorithm specified in the standard.

In addition to government agencies, the standard will be available to private organizations and individuals. It will be unveiled at a conference to be held Feb. 15 at the Gaithersburg, MD, headquarters of NBS.

The hardware devices have been patented by IBM, which has agreed to grant nonexclusive, royalty-free licenses to users.

## Ultrasonic system turns the lights on and off

A guest leaves his hotel room, and a minute and a half later all the lights he's left on, including the television set, switch off. When he returns and enters the room, all the appliances turn on.

This discrete economy move is accomplished by an ultrasonic transmitter-receiver system that is set to sense the entrance or exit of any bulk the size of a human being moving at from 1 to 2 ft/s. Small animals don't trigger the system because they're the wrong size and usually don't move at the right speed.

Called EASE, for Energy Activation Systems Equipment, the system contains an oscillator that consists of transmitters and receivers recessed in the ceiling. Each device commands a radius of approximately 10 feet. The transmitter consists of an oscillator that generates ultrasonic emissions at 42 kHz.

The sensor contains a microphone transducer, an AGC circuit, and a circuit that makes comparative analysis between a reference signal and the ultrasonic sound in the space being monitored. If, for example, a frequency above or below 42 kHz is received, it means a doppler shift has been created by movement in the room.

The circuit is similar in design to that of an ultrasonic burglar alarm. A switching module causes the relay to open or close, thus turning the appliances on or off.

EASE is being manufactured by Elcobar, a joint venture formed by Barnum Enterprises, Leonia, NJ, and Elco, Ltd. of Israel. The system is marketed by MRCA, Inc., Leonia, NJ.

## ITT head gets patent on wrist pulse monitor

Besides serving as chairman and chief executive of the International Telephone and Telegraph Corp., Harold S. Geneen has been granted a patent on a "wristwatch" pulse-rate indicator that warns a jogger when to slow down.

Besides its usefulness for joggers who would like to know if they're exceeding their own safe limits of cardiovascular activity without having to stop and take their pulse, the indicator could also prove helpful during sedentary situations for people whose emotions tend to boost their heart rates.

The device displays the wearer's heart rate in three forms: digital, color (green for rest, amber for safe exercise level, and red for danger), and by an audible beep in conjunction with the red light.

The device consists of a contact-type pulse-detector worn over the radial artery in the vicinity of the user's wrist or as a headband. The detector may comprise a thin silicon-metal piezoelectric transducer or a piezoelectric strain guage.

The sensor produces an electric output signal which is played to a programmable IC within the unit's housing. The signal is amplified and peak detected in the shaper circuit. The shaper circuit is made variable to conform to the individual's physiological characteristics.

The shaped output pulse is applied to a counter. At the end of a predetermined period, which may consist of 15 seconds or one minute, the count is transferred through transfer gates to storage circuits.

At the end of a predetermined number of counts, an averaging circuit determines the average rest pulse rate over a predetermined period. This average is applied to a comparator circuit and displayed.

The averaging circuit also includes a set element to fix or set the average of the pulse rate so that this figure remains constant during jogging. If, however, an individual knows his rest pulse rate, he can set it into the averaging circuit by hand.

How soon, and even whether, ITT will produce the pulse rate indicator is still under consideration.

## News Briefs

**Detection and identification of single atoms** of various elements are now possible with a laser technique developed at Oak Ridge National Laboratory. Among potential applications, the technique promises to provide a more sensitive method for identifying and measuring chemical pollutants in the environment.

**Prototypes of a nickel-zinc battery,** which will have three times the energy output of a lead acid battery, are now under development at Gould Inc. William Ylvisaker, chairman, believes that by the late 1970s and early 1980s commercial versions of the battery will enable electric cars to attain speeds of 60 mph and a range of 125 miles.

**The first commercial bubble memory chips** will be introduced by Plessey Microsystems, Irvine, CA, during the second quarter of 1977. The 64-kbit chip, which will have a price tag in the $20-to-$30 range, will be used in serial memory devices.

**Production of capacitors containing PCB** materials (polychlorinated biphenyl) will be discontinued by Sprague Electric by July 1—10 months sooner than originally planned. Sprague's Clorinol family of oil-paper capacitors will be replaced by a new series of Eccol capacitors which use a biodegradable synthetic-oil impregnant.

# Now from Amperex– a group of high-performance, 4- and 5-GHz PNP's

## at prices between $2.40 and $3.15.

The ever-growing Amperex line of high-performance, economical, small-signal GHz transistors now opens up still more design possibilities in the GHz region. These six new low-noise PNP's offer the key to both new and retrofit/upgraded circuits for portable pagers and transceivers...for high bit rate communications gear...for high frequency spectrum analyzers and oscilloscopes...for counters...and for CATV/MATV amplifiers.

Like their NPN complements, the six new PNP's have $f_T$ of 4-or 5-GHz at $I_C$'s from 14 to 30 mA and offer high linearity and low noise; they provide maximum available gain as high as 19 dB. Two of them, the BFR92 and the BRF93 are in the new SOT-23 microminiature plastic package for high frequency hybrid circuit applications.

There's simply nothing else like them available at anything like our prices anywhere else today. For further information on the Amperex line of high-technology GHz transistors...and for applications data on PNP's in high frequency circuits...write Amperex Electronic Corporation, Slatersville Division, Slatersville, Rhode Island 02876, or telephone 401-762-9000.

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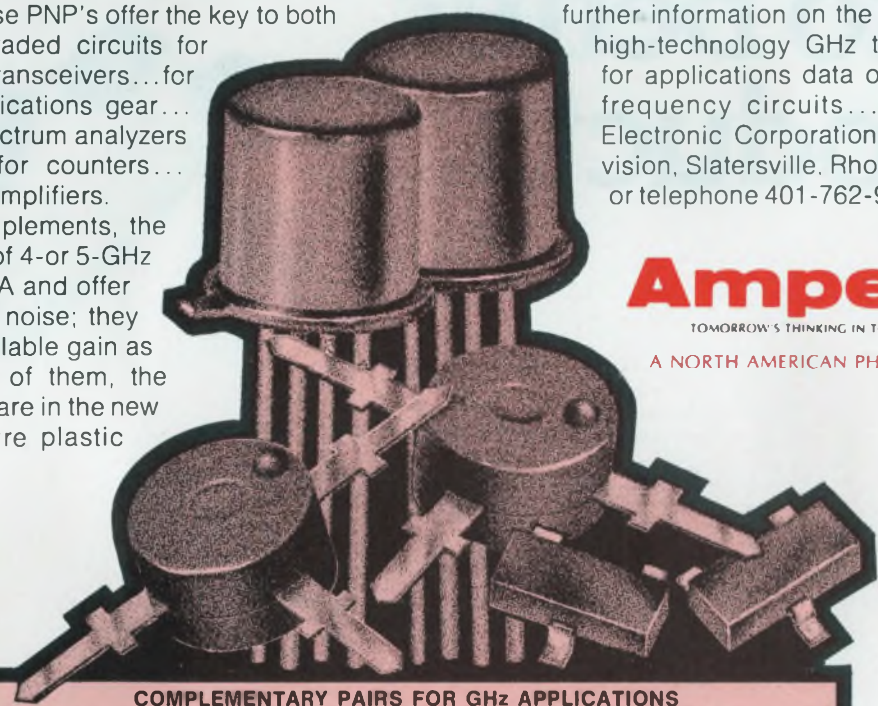
TOMORROW'S THINKING IN TODAY'S PRODUCTS

A NORTH AMERICAN PHILIPS COMPANY



**COMPLEMENTARY PAIRS FOR GHz APPLICATIONS**

| New PNP Types | | | Complementary NPN Types | |
|---|---|---|---|---|
| TYPE | FEATURES | PRICE* | TYPE | PRICE* |
| **A440** (TO-72) | $f_T$ ....5 GHz @ 14 mA<br>NF ...2.3 dB @ 200 MHz<br>$G_{max}$ ..18 dB @ 500 MHz | $2.40 | **A400** (TO-72) | $1.65 |
| **A441** (TO-72) | $f_T$ ....5 GHz @ 30 mA<br>NF ...2.4 dB @ 200 MHz<br>$G_{max}$ ..14 dB @ 500 MHz | $2.65 | **A401** (TO-72) | $1.75 |
| **ON586** (SOT-37) | $f_T$ ....5 GHz @ 14 mA<br>NF ...2.5 dB @ 500 MHz<br>$G_{max}$ ..19 dB @ 500 MHz | $2.85 | **BFR90** (SOT-37) | $2.25 |
| **BFQ23** (SOT-37) | $f_T$ ....5 GHz @ 30 mA<br>NF ...2.4 dB @ 500 MHz<br>$G_{max}$ ..15 dB @ 500 MHz | $3.15 | **BFR91** (SOT-37) | $2.45 |
| **BFT92** (SOT-23) | $f_T$ ....4 GHz @ 14 mA<br>NF ...2.7 dB @ 500 MHz<br>$G_{max}$ ..17.5 dB @ 500 MHz | $2.53 | **BFR92** (SOT-23) | $2.30 |
| **BFT 93** (SOT-23) | $f_T$ ....4 GHz @ 30 mA<br>NF ...2.4 dB @ 500 MHz<br>$G_{max}$ ..15.5 dB @ 500 MHz | $2.70 | **BFR93** (SOT-23) | $2.45 |

*In 1000 piece quantities

CIRCLE NUMBER 10

# Why Rockwell microcomputers turn your good ideas into better products.

Rockwell's broad line of microprocessor systems are making all kinds of new products possible as well as practical because they fit the application so precisely. You get the right functional capability at the right price—and the Rockwell in-house capability to make sure your product idea becomes a reality.

### The Rockwell advantage—a 5-family approach.

Rockwell offers five compatible microcomputer families, from low-cost one chippers through multi-chip 8-bit systems. You select the most cost-effective microprocessor system for your immediate design requirements, then expand models up or down with our compatible systems. You don't need to redo your total program.

**5 families of Rockwell microcomputers.**

- PPS-4/1
- PPS-4/2
- PPS-4
- PPS-8/2
- PPS-8

Our one-chip PPS-4/1 family with CPU, ROM, RAM, and 31 or more I/O ports cover a wide range of applications at lowest possible cost.

The two-chip PPS-4/2 and the multi-chip PPS-4 systems offer more power at low cost. Both have fast execution speeds, high throughput, and are expandable with dozens of LSI I/O peripheral controllers and memory options.

Rockwell's 8-bit systems include the PPS-8/2 (two chip microcomputer with I/O) and the fully compatible multi-chip PPS-8 system. Both use the same multi-function 109 instruction set and accept the same broad range of provided LSI memory and I/O controller options.

And Rockwell backs its microcomputers with all needed design aids and a worldwide network of applications centers, representatives and distributors.

### Better products like these are made possible with Rockwell cost-effective systems.

**Cash registers and P-O-S terminals**—Inside some of the most popular machines on the market today are Rockwell microcomputers. At the low end, PPS-4/1 one-chippers. In P-O-S terminals, two-chip microcomputers combine with any of dozens of available LSI I/O and memory options.

**Home and commercial products**—Weighing scales, security systems, copiers, scanning radios, hi-fi record changers and appliances are now being controlled or automated with Rockwell microcomputers.

**High-speed printer**—The functional ability and low cost of a six-chip PPS-8 Rockwell microcomputer is why it was selected to control a matrix printer which zip-prints at 200 characters/second and tabs at 550.

**Hand held computer terminals**—Two and a half hours of paperwork for meter readers and sales clerks are reduced to 30 seconds. The reason—a Rockwell PPS-4/2 microcomputer in a hand-held terminal that records transactions and interfaces directly with central computers.

**Electronic games and pinball machines**—Rockwell's compatible microcomputers are reducing manufacturing costs and shortening design time in all kinds of exciting new games. We have supplied custom design services for makers of these games.

**Heart-monitoring bicycle exerciser**—This unique but functionally complex idea was made economically possible with a Rockwell PPS-4/2 microcomputer. Rockwell is producing the microcomputer as a cost-saving subassembly.

**Automobile computers**—A 1977 production car has the first digital computer to control spark firing—based on a custom Rockwell two-chip system.

**Stationary and mobile telephones**—Our versatile one, two and multi-chip systems have expanded telephone usage with features like credit verification and automated mobile service. Other types of communications equipment, like auto-dialers and facsimile machines, now also use Rockwell microcomputers.

Get the full story. Write on your company letterhead to: Marketing Services, D/727-B Microelectronic Device Division, Rockwell International, P.O. Box 3669, Anaheim, CA 92803, U.S.A. or phone (714) 632-3729.

**Rockwell International**

# It's getting easier to program μPs with the new software design aids

**Low-cost cassette tapes and CRT monitors** can be used by such development systems as this one from Microkit, Santa Monica, CA. Important to any software-development system, however, is the support literature for the programs.

While grateful for the circuit simplification microprocessors permit, the designer is not so pleased with the difficulty and high cost of programming them. Designers have almost learned to live with the programmer's rule of thumb: Three to five lines of valid code represent a good day's work.

The meager output is understandable, however: With over 40 available μP types—and each with a different instruction set—the designer/programmer can't be an expert in them all. Changing from one to another requires preparation and time.

To remedy the costly bottleneck many companies that make or use μPs offer myriad forms of programming aids—from simple programs that help you develop your own to full libraries of working programs for use on your system.

Software support is available in four basic levels and in almost as many forms:

- If you're familiar with machine language, you can work directly with the microprocessor in hexadecimal notation. For large programs, however, working in hex can be extremely cumbersome.
- If numbers bother you, go one step away from machine language and do the programs in assembly language—mnemonic equivalents of the hex codes. Once the program is written, however, you'll have to convert it back to hex.
- If you don't like mnemonics, go down one more level to a more English-like language (such as Basic) with special operators or even a more simplified form called Tiny Basic. However, complex languages like Basic require more memory support and are not often as efficient (with more lines of machine code to do a specific task) in the long run.
- If you're most familiar with programming large computers in such languages as Fortran, PL/1, or Cobol, you can also use these languages as the fastest route to a program. However, these languages are the most inefficient.

## Software in many forms

You can purchase the software, for use on in-house computer systems, in the form of firmware ROMs, paper-tapes, mag-tapes, floppy discs, card decks or source listings. And, if no in-house computer is available, a terminal and any one of the many time-sharing services offer viable alternatives with high-level languages, simulators and emulators.

For short microprocessor programs, say 200 lines or less, you can readily put the program together by hand. A pencil and paper are the only tools absolutely necessary to hand-assemble and compile a program. Almost every μP vendor offers pads of specially lined

**The 6100-based dual-floppy disc system** from Intersil offers a file system, monitor, text editor, assembler, binary loader, octal debugger, high-level interpreter and utilities.

**Dave Bursky**
Associate Editor

paper to permit you to keep track of all points by setting up columns for instructions, address data and comments. Even non-$\mu$P vendors have picked up on this method, and some companies, like Walton Electronics in Bethany, OK, offer pads of coding forms.

But aside from some demonstration routines, few programs are less than 200 lines long. Typical lengths range from 200 to 4000 lines (often equatable with 500 to 8 kbytes of memory). For programs longer than 200 lines you'll end up whittling a lot of pencils unless you're sharp in hex notation. Vendors who have foreseen this problem offer a wide variety of assemblers, debuggers, compilers and disassemblers to help you.

Software for microprocessor-program development can be split into two major groups—resident and nonresident. Resident software consists of programs written in the instructions of a specific microprocessor and designed to run on a system that uses that microprocessor. Nonresident software consists of programs that run on one processor (typically, a minicomputer or larger) for the benefit of developing the software of another processor (typically, a $\mu$P).

Most of the microprocessor-development systems, from the $100 kit to the $10,000 work station, come with some form of resident software. (For more about development hardware see ED No. 25, December 6, 1976, p. 30). In the lower-cost systems, the software, usually minimal, appears in the form of ROMs—often referred to as firmware. The more expensive development systems usually contain either mag-tape or floppy-disc drives, which permit large support programs.

Three basic programs permit software development: resident assemblers, editors and debuggers. Another program usually included in most utility packages is some form of communications routine that permits the microcomputer to communicate with a teletypewriter or other I/O device.

Each of the various $\mu$P manufacturers offers his own version of an assembler, editor, debugger or other program—and the available features and capabilities vary widely. For example, the Kitbug ROM included in the SC/MP kit from National Semiconductor, Santa Clara, CA, requires 512 bytes of memory and enables you to:

- Initiate execution of your program at any point desired.
- Establish breakpoints within your program to allow execution of selected program segments.
- Examine memory contents and SC/MP registers to determine if your program is producing the desired results.
- Change the contents of any memory location.
- Alter the contents of SC/MP registers to set up conditions.
- Communicate with the SC/MP via a teletypewriter control routine.

Motorola, Phoenix, AZ; Fairchild, Mountain View, CA; RCA, Somerville, NJ; Intel, Santa Clara, CA; Signetics, Sunnyvale, CA; and MOS Technology, Norristown, PA, all offer similar ROMs in their evaluation boards. But in most cases, you can't buy just the ROM —it comes with the entire package.

The ROMs from Motorola appear to offer the widest range of capabilities. Seven ROM-based programs are available. The smallest is the monitor included with the Educator 2. It has six commands that are intended to handle binary-entered instructions and data. Jbug, which comes with the two-board Evaluation Kit 2, offers eight commands and is designed to handle data from a hex keyboard. Available with the Micromodule $\mu$P board is Microbug, a monitor and assembler with 13 commands and an RS-232 interface routine.

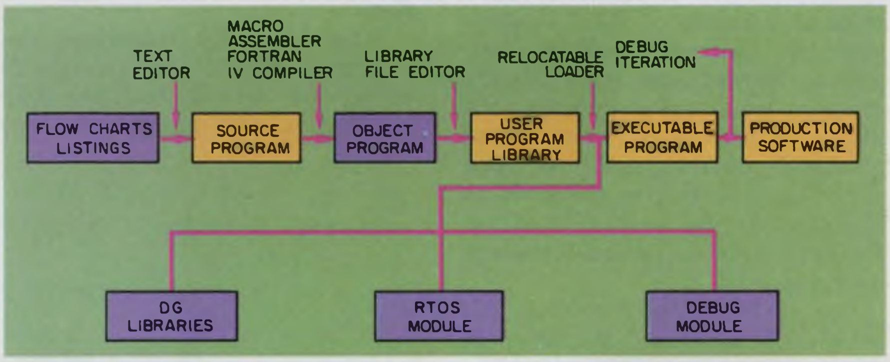
Two versions of Minibug, one that uses the peripheral interface adapter as an RS-232 port and one that uses the asynchronous interface adapter to do the RS-232 interface, are available with the Evaluation Module 1 and the Evaluation Kit 1, respectively. A five-command program known as Mikbug comes with the Evaluation Module 1.

The most complex program is EXbug, which provides 34 commands and requires 3 kbytes of ROM. Of the 34 commands, 26 are used for interactive debugging.

Only the EXbug and Mikbug ROMs are available by themselves, for $200 and $18.15 respectively.

Included on the MOS Technology Kim microcomputer board is the Kim monitor, which resides in two 6530 ROM/RAM and I/O circuits. The monitor program, called TIM (terminal interface monitor), communicates with you over a full-duplex port and adjusts the data speed to that of your terminal. I/O routines similar to SC/MP also come with TIM. Coming soon are ROM-based line editors, assemblers and even a mathematics package.

Even nonmicroprocessor manufacturers are developing firmware that helps you cut $\mu$P-program development time. Wintek, Lafayette, IN, for instance, has ROM programs called Fantom I and Fantom II designed to support the 6800 $\mu$P. Fantom I is similar to Motorola's Mikbug, and has five basic commands that let you load, examine, print and display data and instructions as well as initiate programs. Fantom II is a 1-kbyte loader and diagnostic program that, in addition to the commands used in Fantom I, permits you to operate the $\mu$P in the single-instruction step mode, examine instructions in




**A general program-development cycle,** as suggested by Data General, can be a long and tedious process. However, for microNova users, real-time operating systems, large software libraries and debug aids can speed programming.

memory, dump memory to console, and examine/modify the A, B, condition-code and, index registers and program counter.

### ROMs limit programming ease

Most of the ROMs in the small systems permit you to work only in hexadecimal—a severe limitation when you have to develop a lengthy program. The next step up is to get a system that offers a program that can assemble and then compile assembly language listings.

The program necessary to do the assembly usually requires several kbytes of memory. Resident programs in Motorola's EXORciser, Intel's Intellec-MDS, Zilog's development system, Fairchild's Formulator and RCA's development system are often sold with a minimum of 4 kbytes of RAM in addition to the resident ROM programs. Resident-assembler/editor/compiler programs require up to 4 kbytes of ROM and up to 1 kbyte of RAM working space to store variables. The rest of the RAM is allocated by the monitor program for your own workspace (program development).

One of the largest program development systems available is Intel's 8080-based MDS-800. The minimum system consists of 16 kbytes of RAM, 2 k of ROM, an 8080-based microcomputer, hardware interfaces and software drivers for TTY, CRT, floppy discs, line printer, high-speed paper-tape reader/punch, and PROM programmer. A system monitor is included in the resident ROM for program loading, debugging and execution.

A resident assembler, written in Intel's PL/M, a high-level system programming language, occupies 12 kbytes of RAM and translates symbolic 8080 assembly-language instructions into machine-operation codes. Also available is a text editor that permits manipulation of entire lines of text or individual characters within a line. The text editor requires 8 kbytes of RAM and is also written in PL/M.

A resident PL/M compiler program that is designed to operate on the dual floppy disc-based MDS system has been introduced recently by Intel. However, a full 65-kbyte memory is necessary to support the $10,000 system. Specially developed routines in the disc control system permit up to 200 files to be packed onto the disc. To provide maximum code storage, the disc-monitor program keeps track of the empty space and the location of files.

Zilog's recently introduced development system uses a single Z-80 $\mu$P for driving both the user hardware and the resident monitor. The system monitor permits programs to be entered into memory, then edited, assembled and loaded for execution.

A debug ROM module allows user-designated operations to be stored in an independent memory and the user to specify an operation that can stop processing and cause the system to go into the monitor mode. In addition, all oper-


**Development programs for M6800 microprocessors** are available in just about every format from Motorola.

```
PL/M-80 COMPILER    FACTORIAL GENERATOR - PROCEDURE


              SOBJECT(:F1:FACT.OB2)
              SDEBUG
              SXREF
              STITLE('FACTORIAL GENERATOR - PROCEDURE')
              SPAGEWIDTH(80)


  1           FACT:
              DO;

  2    1      DECLARE NUMCH BYTE PUBLIC;

  3    1      FACTORIAL: PROCEDURE (NUM,PTR) PUBLIC;
  4    2         DECLARE NUM BYTE, PTR ADDRESS;
  5    2         DECLARE DIGITS BASED PTR (161) BYTE;
  6    2         DECLARE (I,C,M) BYTE;

  7    2         NUMCH=1; DIGITS(1)=1;
  9    2         DO M = 1 TO NUM;
 10    3            C=0;
 11    3            DO I = 1 TO NUMCH;
 12    4               DIGITS(I) = DIGITS(I) * M + C;
 13    4               C = DIGITS(I)/10;
 14    4               DIGITS(I) = DIGITS(I) - 10 * C;
 15    4            END;

 16    3            IF C <> 0 THEN
 17    3            DO;
 18    4               NUMCH = NUMCH+1;  DIGITS(NUMCH) = C;
 20    4               C = DIGITS(NUMCH)/10;
 21    4               DIGITS(NUMCH) = DIGITS(NUMCH) - 10 * C;
 22    4            END;
 23    3         END;

 24    2      END FACTORIAL;

 25    1      END;
```

**Programming in PL/M,** Intel's high-level language, can slash the time needed to develop 8080 software. English-like commands replace many lines of hard-to-write assembly-language statements. A PL/M compiler in the Intellec development system can cut the cost of time-shared program development costs.

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CIRCLE NUMBER 45

ations preceding the suspension are stored in an independent memory and can be examined to find errors.

With two 2650 $\mu$Ps to speed program development, the Twin system from Signetics can offer many advantages. Software includes an operating system, a file-management system, debugging software, a text editor and a resident macroassembler.

The dual-$\mu$P structure provides a common (user) memory space and a master processor/operator system that is independent of the user system.

### Mini-like micros have software

For the $\mu$Ps that approximate full minicomputers, such as the 6100 from Intersil, Cupertino, CA, the LSI-11 from Digital Equipment Corp., Maynard, MA, the TMS-9900 from Texas Instruments, Dallas, TX, and the microNova from Data General, Southboro, MA, a wealth of available software and programming aids already exists.

**A resident Fortran compiler** for 8080 software development is available on a floppy-disc system offered by Realistic Controls.

## Software Definitions

*Machine code:* commands for the $\mu$P system, often written in binary or hexadecimal format. Machine code is often referred to as machine language or object code.

*Assembly language:* commands for the $\mu$P system written in mnemonic form. Typically, three letter abbreviations, called mnemonics, are used to represent each instruction, and each mnemonic can usually be equated to one machine-code instruction.

*High-level:* commands for computer systems where each instruction is actually equated to many machine-code instructions strung together.

*Monitors:* programs that control the operation of the entire computer system. They often contain routines that tell the computer how to communicate with the outside world and how to allocate resources.

*Editors:* programs that permit data or instructions to be manipulated and displayed. Their most common use is in the preparation of new programs.

*Assemblers:* programs that permit you to represent instructions, addresses and data in symbolic form (character strings that represent machine instructions, addresses, data, among others). An assembler automatically translates symbols into their corresponding numerical values. It permits symbolic addressing by assigning values to labels used to indicate program-jump locations.

*Compilers:* programs that usually translate an assembled program into a complete machine-code listing. No matter how many times a section of code is used in the assembled program, it will be translated only once and put in its proper place.

*Interpreters:* programs that, much like the compiler, translate an assembled program into a complete machine-code listing on a line-by-line basis. If a statement is used in a program 10 times, it will be translated 10 times.

*Disassemblers:* programs that do the opposite of compiler programs. Given a machine-code program listing, the disassembler turns it back into an assembly listing, with mnemonic representations, for troubleshooting purposes.

*Debuggers:* programs that help track down and eliminate errors that occur in the normal course of program development.

*Cross-assemblers and cross-compilers:* programs that are usually designed to run on a large computer for the purpose of translating instructions for use on another processor, usually a $\mu$P.

*Simulators:* programs that help to evaluate a $\mu$P by duplicating all logic operations within the software of a large computer.

Data General, for example, has a diskette-based disc-operating system for the microNova with such utilities as an editor, assembler, relocatable loader and symbolic debugger. A real-time Fortran IC program also can run on the microNova.

Digital Equipment Corp.'s user library, DECUS, provides many programs that can be used on the 6100 since the 6100 emulates, to a great extent, the PDP-8 minicomputer originally developed by DEC. And for LSI-11 program development, DEC offers a wide range of compatible PDP-16 software.

A new language, developed by RCA and Forth, Manhattan Beach, CA, is designed to run on the Cosmac development system. Dubbed microForth, this language is an interactive program that can compile assembly-language statements directly into RAM. An 8 kbyte system is recommended to hold microForth. About 2 k of RAM workspace is available.

Other new languages are being developed by outside (non-IC manufacturers) companies and individuals to make programming easier. One such program is a string-oriented language called SLP that permits large arrays of instructions to be assembled with fast and compact listing.

Scelbal, developed by Scelbi Computer Consulting, Milford, CT, and originally intended to run on the older 8008 $\mu$P, is similar to Basic in capabilities. The language operates in an interpretive mode—both the user and the resident programs must be held in RAM. When a run command is given, the resident program converts each line of high-level language program into executable code.

Slam, a symbolic language adapter for microcomputers, works on 8080-based equipment. Developed by Penn Micro, Lancaster, PA,

# HYBRID

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| μA78H15KC | 15 | $7.00 ea. |
| μA78HGKC | 5-20 | $7.50 ea. |

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CIRCLE NUMBER 14

Slam is an interpreter-type language with editing capability and English-like instructions.

## Pull apart programs to debug

Not only is there a wide variety of languages that assemble assembly-language listings, but there is also a specialized group of programs called disassemblers that rip apart an assembled listing to help in the debugging. MOS Technology's MDT development system has such a program. Tranti Systems, North Billerica, MA, has a similar program in its Model 8000 universal programming system.

The MDT system's assembler assembles from a source tape or RAM, has six character labels and symbols, permits free-form entry of the source statement, delivers a symbol table, puts error flags on listings and delivers an assembled program in executable code. Once the assembler has done an assembly, the disassembler can pull the listing apart and give back the mnemonics from the hex code. Of course, the disassembler does even more, such as setting program traps, goes forward or backward one instruction, shows next or last cycle of operation and more.

A text-editor program comes with the MDT. Available text-manipulating routines include load text buffer, insert or delete a line or character, step forward or backward one character or one blank, go to top or bottom of text index up or down one line, find a specified string of characters and provide output to printer/punch.

## Time-sharing cuts capital costs

Because of the accessibility of large computers or time-sharing services, many of the $\mu$P vendors have developed programs written in PL/1, Fortran, Cobol and other languages that will deliver microprocessor-compatible machine code. National CSS, Norwalk, CT; General Electric Information Services, Bethesda, MD; First Data, Waltham, MA; United Computer Systems, Kansas City, MO; and Tymeshare, Cupertino, CA, are just some of the firms that offer a wide variety of $\mu$P-development software.

All the programs offered on time-sharing systems are designed to run on large computers—the IBM 360/370, the GE Mark 111a, and even the DECsystem 10s. Cross-assemblers, cross-compilers, debuggers, simulators and other programs are available for $\mu$Ps and bit-slice processors. Each company's programs offer slightly different features, so make sure you know the capability of the various time-sharing programs before you hook up.

The familiarity of engineers with Fortran and PL/1 makes these two languages the most popular choices, although Cobol is favored by most programmers. Cross software typically operates faster than resident software and often has more commands or a library of available routines to select from.

A high-level system often permits you to develop the program for a $\mu$P before the actual hardware can be prototyped—sometimes even before a dollar is spent for hardware, since complete simulators are available for some $\mu$Ps. Cross-assemblers are commonly available in Fortran, versions of PL/1, and assembly language. Some assemblers can even produce more than one machine-code format to allow for absolute and relocatable code listings.

Compilers and integrator programs in PL/M, PL/W, PL/Z, MPL, Forth, Cobol and Fortran are available, and there are probably others still to be found. Programs in PL/M, PL/W, PL/Z and MPL are all optimized by the IC vendors to work only for their $\mu$Ps.

The last type of program just starting to appear is a resident form of Fortran. Motorola has available a condensed form of Fortran that runs on the EXORciser system and is available on floppy disc. However, it will burn up quite a bit of RAM—about 16 k is needed to hold the program. ■■

```
                          LEVEL I ASSEMBLY LANGUAGE
                          _________________________

FL LOC  COSMAC CODE       LNNO SOURCE LINE
    0000                     1 .. THIS SAMPLE CALCULATES THE ARITHMETIC
    0000                     2 .. AVERAGE OF TWO NUMBERS.  THE NUMBERS ARE
    0000                     3 .. STORED IN TWO ADJACENT LOCATIONS
    0000                     4 .. POINTED TO BY REGISTER R2.  THE
    0000                     5 .. RESULT IS STORED IN THE HIGH ORDER BYTE
    0000                     6 .. OF REGISTER 3.
    0000                     7 .. ----------------------------------------
    0000 42                  8 LDA R2
    0001 E2                  9 SEX R2
    0002 F4                 10 ADD
    0003 F6                 11 SHR
    0004 B3                 12 PHI R3
    0005                    13 .. ----------------------------------------


                          LEVEL II ASSEMBLY LANGUAGE
                          __________________________

FL LOC  COSMAC CODE       LNNO SOURCE LINE
    0000                     1 .. THIS SAMPLE CALCULATES THE ARITHMETIC
    0000                     2 .. AVERAGE OF TWO NUMBERS.  THE NUMBERS ARE
    0000                     3 .. STORED IN TWO ADJACENT LOCATIONS
    0000                     4 .. POINTED TO BY REGISTER R2.  THE
    0000                     5 .. RESULT IS STORED IN THE HIGH ORDER BYTE
    0000                     6 .. OF REGISTER 3.
    0000                     7 .. ----------------------------------------
    0000 42E2F4F6B3          8 @R2!+@'R2/2->R3.1
    0005                     9 .. ----------------------------------------


                              FORTH LANGUAGE
                              ______________

          THE EXAMPLE BELOW CALCULATES THE AVERAGE OF ANY TWO NUMBERS.
          THE NUMBERS ARE ENTERED FROM THE TERMINAL AT EXECUTION TIME.
          THE FIRST LINE STATES THE FORTH DEFINITION.
          THE SECOND LINE IS AN EXAMPLE OF ITS EXECUTION AND PRINT OUT.
          .. ---------------------------------------------------------

          : AVR + 2 /
          12 46 AVR . 29
```

**Programming the Cosmac $\mu$P** from RCA can require knowledge of assembly language, a higher symbolic assembly language, or an interactive language called microForth—depending on the money spent for software development.


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CIRCLE NUMBER 15

# Intel 8080 peripherals

Now you can get microcomputer based products out of the lab and into production faster than ever before. Intel® 8080 programmable LSI peripherals give you the competitive advantage by helping you reduce design time, component count and manufacturing and inventory costs. Most of all they'll help you get to market first.

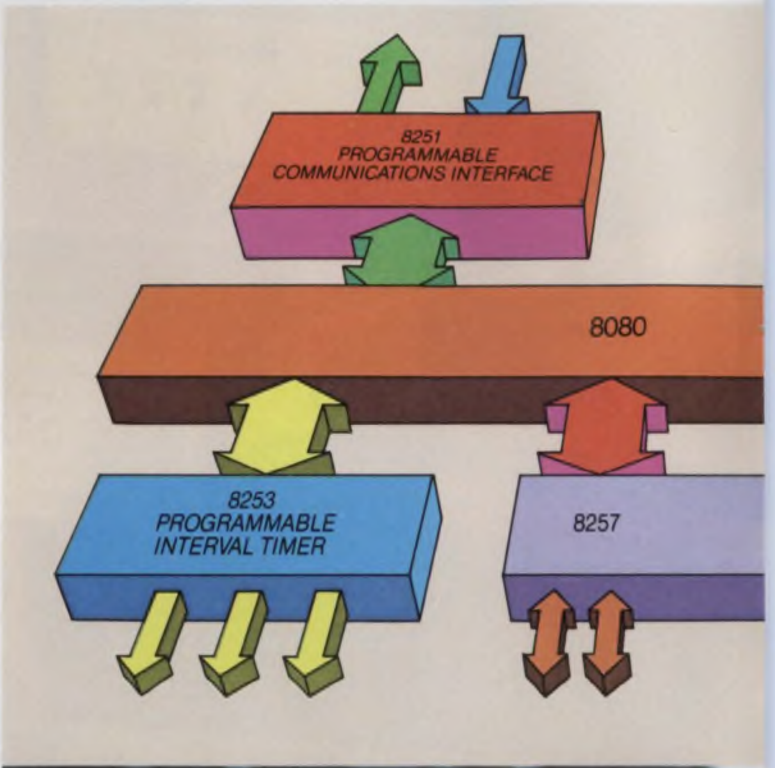
Intel 8080 programmable peripherals are software controlled LSI replacements for hardwired SSI/MSI logic assemblies. You simply attach the appropriate peripherals to the system bus and the +5V supply. Then, with system software, you personalize device operating configurations to suit your applications. Reconfiguration and design changes are made with software. No expensive and time consuming hardware redesigns are necessary.

One peripheral, the 8253 Programmable Interval Timer, is the first LSI solution to system timing problems. It counts out I/O servicing delays, eliminating software timing loops and increasing CPU throughput. It also saves hardware when you need event counters, rate generators or real-time clocks. Each 8253 contains three 16-bit timer/counters.

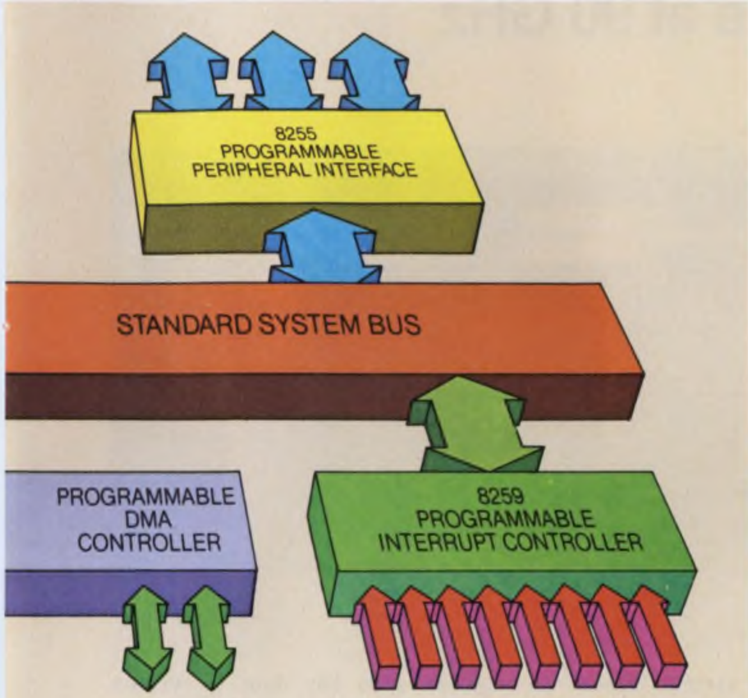
Our 8257 Programmable DMA Controller is the lowest cost way to handle applications that require high speed data transfer such as disks, magnetic tape, analog interfaces and high speed communication controllers. The four channel 8257 contains all the logic necessary for bus acquisition, cycle counting and priority resolving of the channel requests.

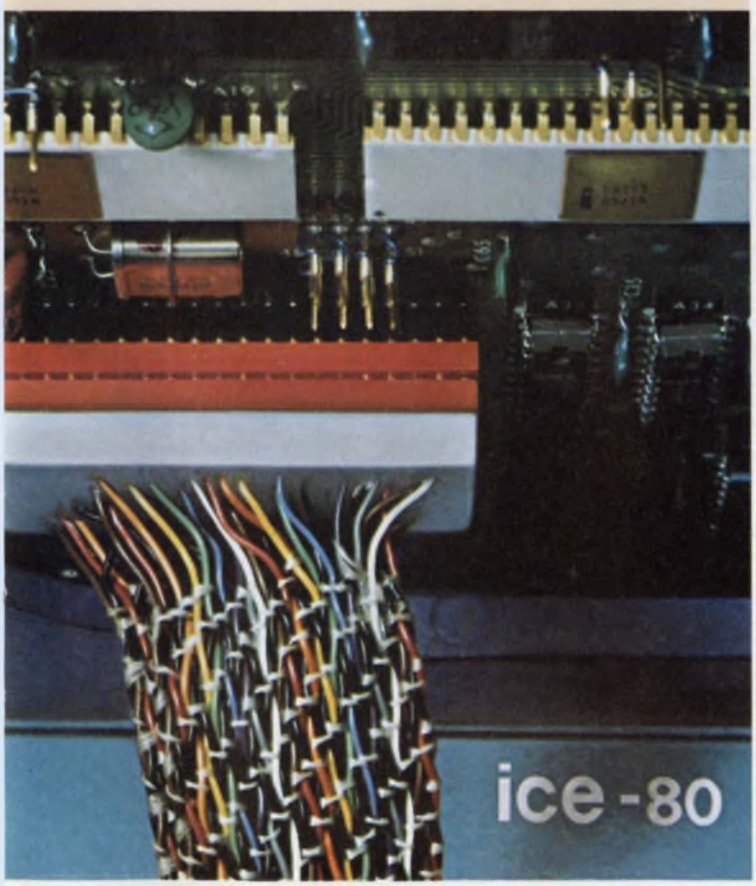
The 8259 Priority Interrupt Controller replaces complex TTL arrays and minimizes component costs. The CPU can change interrupt structure "on the fly" to suit changes in the operating environment, such as time of day or process control parameters. The 8259 handles up to eight vectored priority interrupts. Multiple 8259's can control up to 64 interrupt levels.

Use the 8251 Programmable Communication Controller for "serial I/O." The first true USART in a single chip, the 8251 implements all popular com-




# get you to market first.




munication protocols, including IBM Bi-Sync. For "parallel I/O," each 8255 Programmable Peripheral Interface gives you 24 versatile I/O lines to interface relays, motor drives, printers, keyboard/display and other parallel equipment.

Once you've selected the peripherals to fit your application, use the Intellec® Microcomputer Development System for both software and hardware development. Using the Intellec CRT terminal, call up the resident text editor. Write the source program to initialize the peripheral and the subroutines for peripheral/system operation. Then you assemble or compile the source programs into an object file using resident macroassembler or resident PL/M compiler— and store the object file on the Intellec diskette. With the relocation and linkage capability of the Intellec ISIS II diskette operating system, these routines can be added to a system library and called from user programs as needed. Once the main system program is written, the new peripheral device routines are easily linked in. The entire program is now ready to be run on your prototype via the Intellec ICE-80™ in-circuit emulation module. ICE-80 lets you debug your software and hardware in your actual prototype environment. Move from system integration and debugging to production in a fraction of the time previously required.

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CIRCLE NUMBER 16

# Schottky diode mixer enables imaging system to operate at 90 GHz

A GaAs Schottky diode-mixer with a conversion loss of less than 8 dB sharpens the resolution of radiometric imaging systems by a factor greater than 2. Developed by Aerospace Corp., El Segundo, CA, the diode mixer's low conversion loss permits an operating frequency of 90 GHz—the maximum operating frequency of previous imaging systems had been 35 GHz.

The 8-dB conversion loss overcomes the main impediment to increasing the frequency—hence, the resolution—of radiometric imaging systems, an inefficient mixer stage.

The advantage to 90-GHz operation is twofold. For a given-sized antenna, the system's resolution increases directly with frequency to permit the use of smaller antennas. And terrain signatures peculiar to 90 GHz can be observed.

Variations in ground temperature cause corresponding variations in the amplitude of a wide spectrum of emitted radiation. This electromagnetic radiation is detected and used to construct an image of the terrain below: Each detected frequency provides a different signature.

Developed in a cooperative effort with NASA and Naval Research Labs the diode mixer was built into a radiometer and then tested in an aircraft flown over Virginia's Chesapeake Bay area.

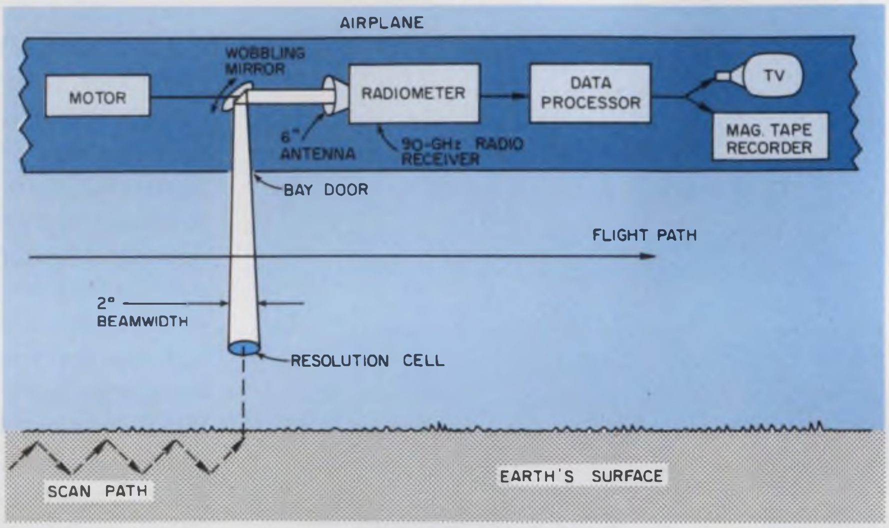
The radiometer's output was fed into an on-board data processor, which provided both a real-time TV image and a tape recording.

"The real-time monitor gave us a dramatic view of the terrain below, even though it was obscured by 2000 feet of opaque cloud cover," notes Howard King, head of the Antenna and Propagation Department at Aerospace.

The 90-GHz imaging system can replicate ground features matching geological survey maps of the ground below. Flights were conducted at various altitudes during the field test, and the imaging system was able to identify natural terrain features and man-made objects smaller than 30 feet across, as well as bridges, rivers, islands, marshes, aircraft at rest and ships at sea and their wakes.

A wobbling mirror is used to focus the radiometer's 6-in. antenna toward the ground and scan 32 degrees to each side of the flight path. At a forward speed of 173 mph and a scan rate of 0.1 s per

**Dick Hackmeister**
Western Editor




**Radiometric imaging system "looks" through an open bay door** to receive electromagnetic radiation from Earth's terrain. A wobbling mirror causes receiving antenna to scan both sides of flight path. The radiometer selects frequency of interest and provides input raster to data processor. The system is entirely passive; no radio transmission takes place.

**This high-resolution radiometer needs** only the small, cylindrical antenna at left to "see" Earth terrain signatures at 90 GHz. A new GaAs Schottky diode-mixer stage permits an 88-GHz local oscillator to be mixed with the 90-GHz reflections from the ground.

# If the 2900 isn't already the industry standard TTL processor family, this'll do it.

# Motorola introduces

# m2900

**M2900** is Motorola's second source for the popular Am2900 low power Schottky TTL four-bit processor family. It's a contractual, mask-exchange second source, and the key family devices are available now.

## *Key M2900 devices available now*

**MC2901** is the expandable four-bit microprocessor slice with a high-speed eight-function ALU, a 16-word by four-bit two-port RAM, and shifting, decoding and multiplexing circuitry.

**MC2909** is the expandable four-bit wide microprogram sequencer, an address controller for sequencing through a series of microprograms stored in ROM or PROM. It includes a register to hold a reference address, a microprogram counter and a four-word deep push-pop stack for subroutine linkage. It can jump to any address.

**MC2902**, the look-ahead carry generator, generates carries for three MC2901s from the Generate and Propagate outputs, producing them in 8 ns from the G and P inputs.

## *M2900 prices are right on the money*

All three introduced M2900 Family devices are available now from authorized Motorola distributors and Motorola sales offices, at prices you'll find right on the money. In 100-up quantities, the MC2901LC is $21.00, the MC2909LC is just $12.98, and the MC2902LC is $3.78.

## *Eight more in the M2900 Family from now to May*

| Device | Function | Available |
|---|---|---|
| MC2905 | Quad Bus Transceiver | May '77 |
| MC2906 | Quad Bus Transceiver | May '77 |
| MC2907 | Quad Bus Transceiver | May '77 |
| MC2911 | Microprogram Sequencer | Feb. '77 |
| MC2915 | Quad Bus Transceiver | May '77 |
| MC2916 | Quad Bus Transceiver | May '77 |
| MC2917 | Quad Bus Transceiver | May '77 |
| MC2918 | 4-Bit Register | Feb. '77 |

For data, circle the reader service number, or write to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

**MOTOROLA Semiconductors**

*—and you thought we were just a production house*

CIRCLE NUMBER 17

excursion, the differential temperature resolution of the system is 2.8 K, which can be enhanced with longer dwell times.

For example, the Navy is planning to put a similar radiometric imaging system aboard an Earth satellite to monitor America's proposed 200-mile fishing limit. The Navy is using the new imaging system onboard aircraft to provide electromagnetic maps of the globe. Correlated radiometric images at different frequencies (including 90 GHz) are revealing such natural and man-made surface features as land masses, icebergs, fault lines, cities and underwater vessels. These are now being catalogued for a wide variety of purposes. ■■

# Temperature, not current switches p-n-p-n element

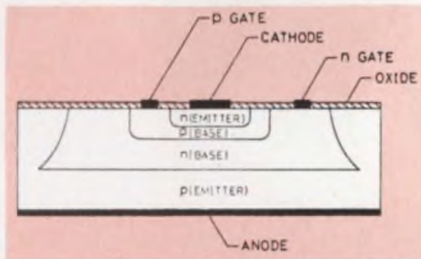
A simple temperature-sensitive switching device is similar in design to a thyristor but can be triggered by temperature instead of gate current.

Called Thermosenstor and developed by the Mitsubishi Electric Corp., Itami, Japan, the three-terminal device is said to have the following advantages over conventional solid-state temperature-sensitive devices:

- It combines temperature-sensitive and switching functions, so its circuitry is less complicated than a thermistor-based switching circuit. For example, it does not require a differential amplifier and a Schmitt circuit.
- The turn-on temperature can be remote-controlled through the gate terminal.
- Once the Thermosenstor is turned on, conduction is maintained until on-state current is reduced to almost zero—even though the temperature falls below the switching temperature.
- Below the turn-on temperature, the Thermosenstor can be switched by gate current as in a thyristor.

The Japanese device is constructed with a silicon p-n-p-n structure (see Fig.). The chip is 0.5 mm square and 0.2 mm thick.

The minimum rated off-state voltage is 50 V; the rated average on-state current is 100 mA, at an ambient of 87 C.




**Thermosenstor** is a new temperature switch from Mitsubishi Electric.

### High gain at low temperatures

To obtain low turn-on temperature without increasing the applied voltage requires high current gains at low temperature. This reduced temperature is accomplished in the device by reducing the width of the base layers and increasing the leakage current of the collector junction.

The turn-on temperature is regulated by connecting a shunt resistance from one of the gates to either the cathode-emitter junction or the anode-emitter junction. This gate-shunt resistance shifts the turn-on temperature upward under an applied forward voltage. The temperature can be shifted from 50 to 150 C.

Like conventional thyristors, once the Thermosenstor is turned on in a dc circuit, its conduction is maintained until the on-state current is reduced to almost zero—even though temperature decreases below the turn-on temperature.

When operating in an ac circuit, the device will, of course, turn off at the zero value after each positive half cycle if the junction temperature falls below the turn-off temperature, But this turn-off temperature is not always identical to the turn-on temperature. The difference between temperatures is caused by the effects of the dv/dt of the reapplied off-state voltage following the termination of conduction. ■■

# By sealing out liquids, this Amphenol® connector keeps you out of hot water.

## While it saves you some cold cash.

**It's the Amphenol 44 Series connector.** It lets you save money and still get a connection that's waterproof. And resistant to lubricants, fuel, abrasion, ozone. It even withstands salt spray, vibration, and shock.

**You can use it almost anywhere.** Anywhere you want a connector that's both easy to service and trouble-free. That's because 44 Series connectors are self-sealing. They're molded of a resilient material that stays tough. They're simple to mate and unmate. And you can't mis-mate them, either. Rating for 44 Series connectors is 250 VDC, 200 VAC, 8 amps continuous.

**There's an insert arrangement right for you.** Five different ones—with 2, 3, 4, 5, or 6 easy-to-use crimp Poke-Home® contacts. A complete line of tools for crimping and contact insertion by machine or hand minimizes installation costs.

**Available in quantity. Available now.** Just call your Amphenol Industrial Distributor to find out that low price and to get fast delivery. For further information, see *EEM Catalog* 76-77 Catalog Volume, pp. 588-589. Or write or call: Ray Hayer, Amphenol Connector Systems, Bunker Ramo Corporation, 900 Commerce Drive, Oak Brook, Illinois 60521. (312) 986-3749.

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**CIRCLE NUMBER 19**

# AMP component sockets are sealed with silicone rubber. And can be inserted at up to 7,000 an hour.

# You can't beat that.

AMP component sockets. They're the ones that come in strip form. You can insert them at high speed and cut your costs. Use a bench press or, for really fast loading, a N/C machine. AMP can furnish the applicator and interface module for compatibility with most N/C machines.

And AMP keeps your product out of trouble by sealing its component sockets with silicone rubber. Which ends solder flux contamination and solder flooding.

Of course, they provide easy pluggability with either rectangular integrated circuit leads or .016 inch-.019 inch diameter leads. Their small head diameters permit .100 inch center-to-center mounting. Our sockets help you save on board costs too, as they seat securely in wide tolerance holes.

For more data on AMP component sockets, ask your AMP Sales Engineer. He's ready to help you in any way possible.
Or write or call AMP Incorporated,
Harrisburg, PA 17105.
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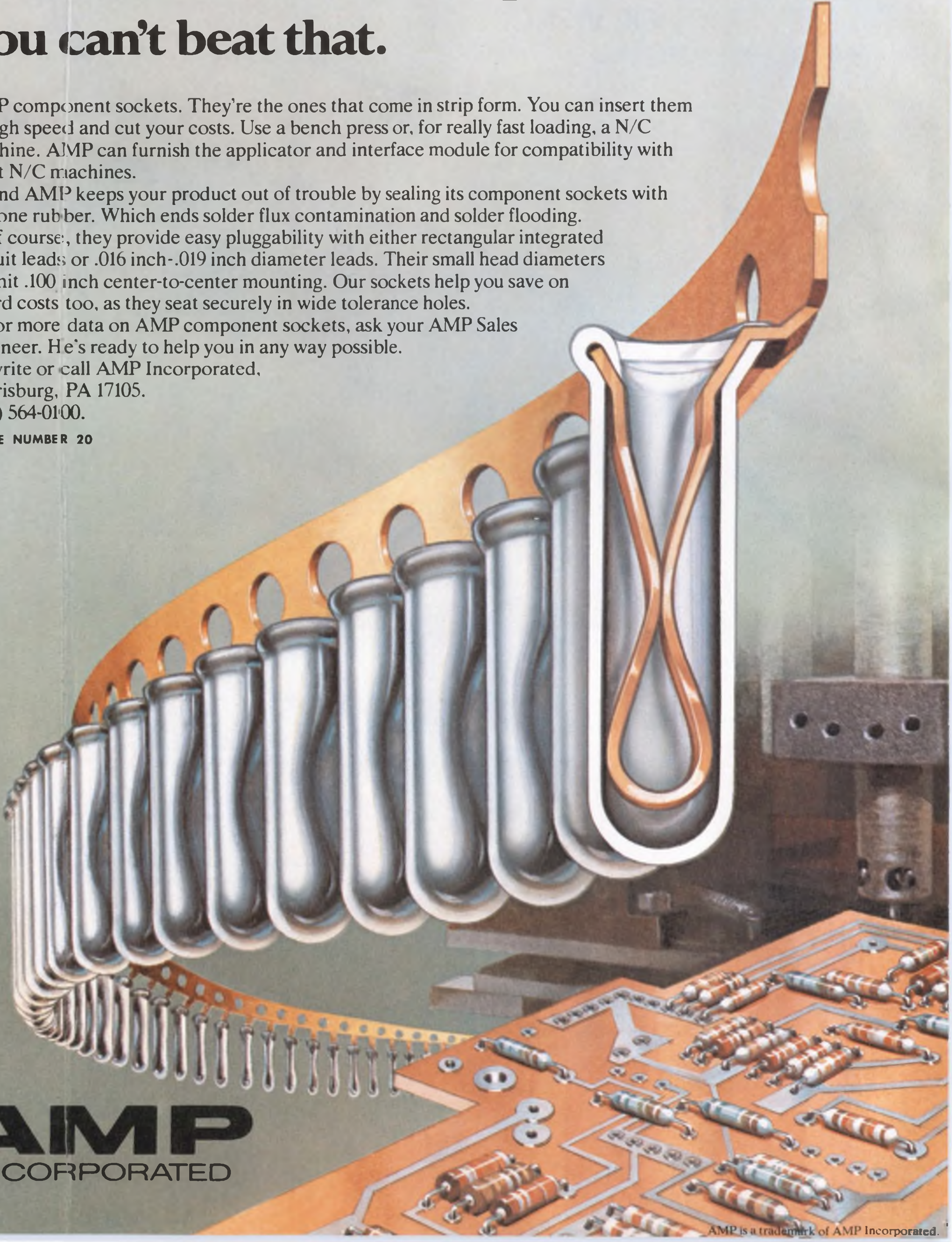
CIRCLE NUMBER 20



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# Washington Report

## FAA adds altitude warning feature to ground radars

A safety feature known as Minimum Safe Altitude Warning (MSAW) has been added by the Federal Aviation Administration to Dulles International Airport, Washington, DC, and Los Angeles International Airport. Four more airports will get the feature in February.

Produced by Sperry Univac, St. Paul, MN, MSAW works in conjunction with the automated radar terminal systems (ARTS III) to monitor aircraft altitudes automatically and compare them to an altitude table programmed into the ARTS III computer. Monitoring begins as soon as the aircraft approaches the terminal area and is picked up by the ARTS III radar. The aircraft must be equipped with a 4096-code transponder and altitude encoder. When the computer detects a potentially unsafe altitude condition, an alarm sounds and the words "LOW ALT" appear above the aircraft's symbol on the air-traffic controller's radar scope.

## Defense contractor shifts keyed to foreign sales

Major shifts among the top defense contractors are reflected in the Pentagon's latest list of its 100 major suppliers. The reason—expanded foreign military sales.

McDonnell Douglas vaulted into first place for the fiscal year ended last June 30, as its sales rose from $1.4 billion the previous year to $2.5 billion in fiscal 1976. McDonnell Douglas, which was in fourth place in fiscal 1975, is supplying 25 F-15 fighters to Israel, which wants to buy 25 more.

The biggest gainer was Northrop, which rose from 12th place the year before with $620 million in DOD contracts to third place with $1.4 billion. The firm recently completed its 3000th F-5 fighter—most of them sold abroad.

The Pentagon awarded $42 billion in prime contracts last year, and the top 100 received $29.9 billion, or 69% of the total.

## Army to fund helicopter avionics system

The Army expects to select two parallel development contractors about the first week of March for a new day-and-night target-designation system to be used in its future helicopters.

Known as the Target Acquisition and Designation System/Pilot Night Vision System (TADS/PNVS), it will contain internal forward looking infrared (FLIR) sensors, television units and laser subsystems that can lock onto a target about 2 meters square from as far away as 5 to 6 km.

The TADS/PNVS will be installed initially in the Army's new Advanced

Attack Helicopter (AAH), which is being developed by the Hughes Helicopters Division of Summa Corp., to direct the laser-guided Hellfire missile to ranges that will be twice that of the present TOW missile fired from Cobra helicopter gunships.

The target tracking system is also being considered for the Army's proposed Advanced Scout Helicopter (ASH). (Congress disallowed a program to develop a similar system for the ASH last year, but did provide sufficient funds for a TADS/PNVS to be used by both helicopters.)

Seven firms have submitted proposals on the new system to the Army Aviation Systems Command in St. Louis: Ford Aerospace & Communications, General Electric, General Motors' Delco Division, Hughes Aircraft Corp., Martin Marietta's Orlando Division, Northrop and Texas Instruments. While the Army hopes to fund two of the companies for at least a year of engineering development, it may be able to fund only one because of a rumored shortage of money.

The winning contractor will outfit the 536 projected AAH helicopters, plus an undetermined number of ASH helicopters if Congress approves that program this year.

## TWTA problems afflict NASA Mariner spacecraft

A variety of minor problems have cropped up during tests with the Watkins-Johnson traveling-wave-tube (TWTA) amplifiers for NASA's two Mariner Jupiter/Saturn spacecraft to be launched in August and September. The problems are serious enough for NASA to consider backup units from Ford Aerospace & Communications and Hughes.

Both the X-band and S-band units have been afflicted, according to Mariner program manager Rodney A. Mills. As a result, costs have been driven up and deliveries delayed about nine months. The life testing still has to be done.

NASA will have to decide by April if a substitution is necessary. The first flight spacecraft is already in assembly at Jet Propulsion Laboratory (JPL). The second will begin in January.

The possible X-band replacement is a Hughes unit used in the NATO communications satellites. It has the same output as the Watkins-Johnson TWTA, 20 W, but is less efficient. The Hughes substitute requires 100-W input, the TWTA 70 watts. For an S-band replacement, NASA will consider a device by Ford Aerospace that is comparable in efficiency, but lower in power—about 20 W vs the TWTA's 29 W.

Under subcontract to JPL, Motorola will integrate the TWTAs into the spacecraft's radio subsystem.

**Capital Capsules:** The Army plans to build a **5000-m test range at Fort A. P. Hill, VA, to accommodate high-energy research** being relocated from Fort Monmouth, NJ. . . . The Army's Patriot anti-aircraft missile (formerly SAM-D) has **successfully knocked down a drone target while being jammed by airborne electronic countermeasures** during tests at White Sands Missle Range, NM. . . . **The Navy's controversial Seafarer extremely-low frequency (ELF) system** for communicating with submerged submarines has received a qualified blessing from the National Research Council. NRC's preliminary report said the 0.07 volt per meter radiated by the communications grid would cause no biological damage but did raise questions about the 15 V/m around the terminal points. The system of underground antennas is being considered for Michigan's Upper Peninsula, where local residents have opposed it. A final report from NRC, an affiliate of the National Academy of Sciences, is due this spring.

## Save Space. Save Weight. Increase Reliability.

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For information, application assistance, and free design guide call Sales Engineering. PowerTech, Inc., 0-02 Fair Lawn Avenue, Fair Lawn, New Jersey 07410; Tel. (201) 791-5050.

| Type # | (pk.) $I_c$ | $V_{ceo}$ | ($h_{fe} = 10$) $V_{ce}$ (sat) @ $I_c$ |
|---|---|---|---|
| JAN-TX 2N5926 | 90A | 120V | 0.6V @ 50A |
| PT-7511 | 90A | 200V | 0.6V @ 50A |
| JAN-TX 2N5927 | 120A | 120V | 0.6V @ 70A |
| PT-6502 | 200A | 80V | 0.7V @ 100A |
| PT-9502* | 500A | 80V | 0.5V @ 300A |

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*625 Watt Power Rating
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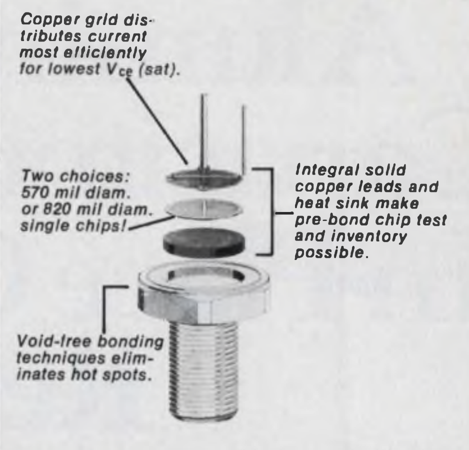
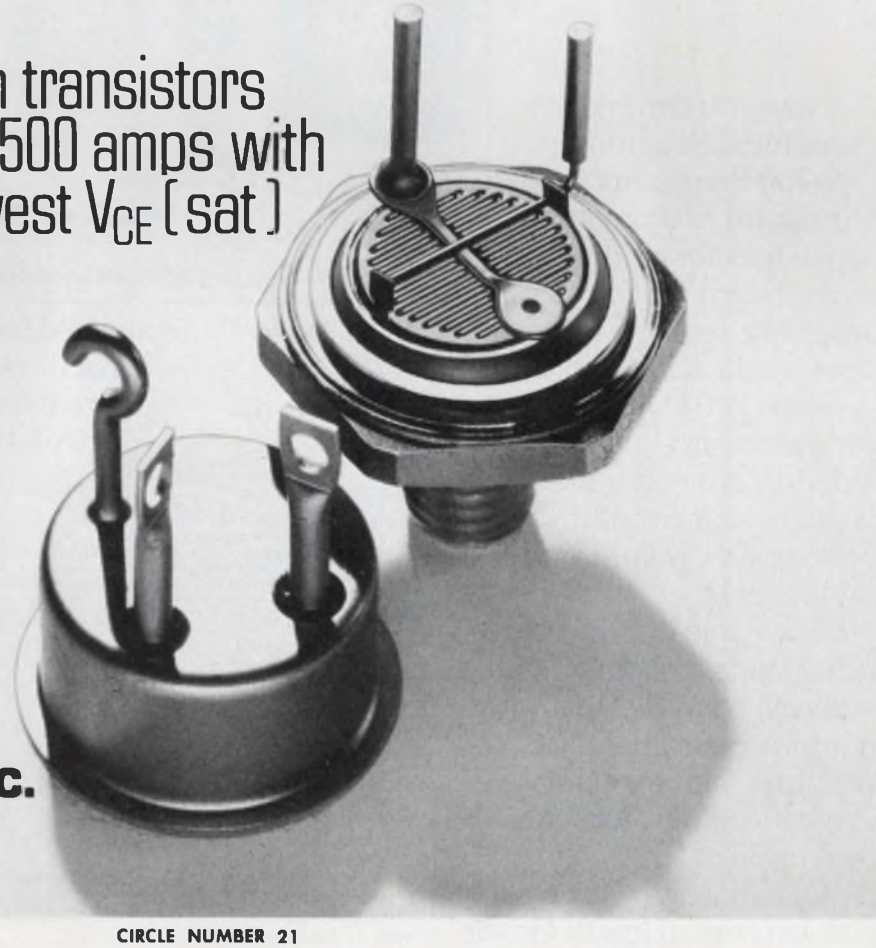



# TO *UN*PARALLEL IS TO SAVE:

Silicon transistors to 500 amps with lowest $V_{CE}$ (sat)



**PowerTech, Inc.**
**"BIG IDEAS IN BIG POWER"**

CIRCLE NUMBER 21

# New Sangamo Type 300 Aluminum Electrolytic Capacitors Slash Space and In-Place Cost in Switching Regulator PC Boards.

Sangamo Type 300 Capacitors (actual size)

Now you can specify economical Sangamo Type 300 Premium-Grade Aluminum Electrolytic Capacitors for printed circuit board mounting in switching regulator power supplies and other applications from 10 to 100 kHz.

Type 300 Capacitors give you low ESR, low inductance, high capacitance and long life—in a unique package that dramatically reduces size, weight and in-place cost.

The basic unit has three radial leads arranged in an isosceles triangle. Just plug in and wave-solder. No fumbling. No reversing. No screw terminals. You can even parallel them.

Or choose the Type 301 with two radial leads. Or the horizontal Type 301A with the dummy lead on the bottom for rigid mounting without using a strap.

If you're now using stacked foil, four-terminal or wet tantalum capacitors, look into the new, economical alternatives—Sangamo Type 300 Aluminum Electrolytic Capacitors.

**Type 300 Capacitors**
**Electrical/Mechanical Specifications**

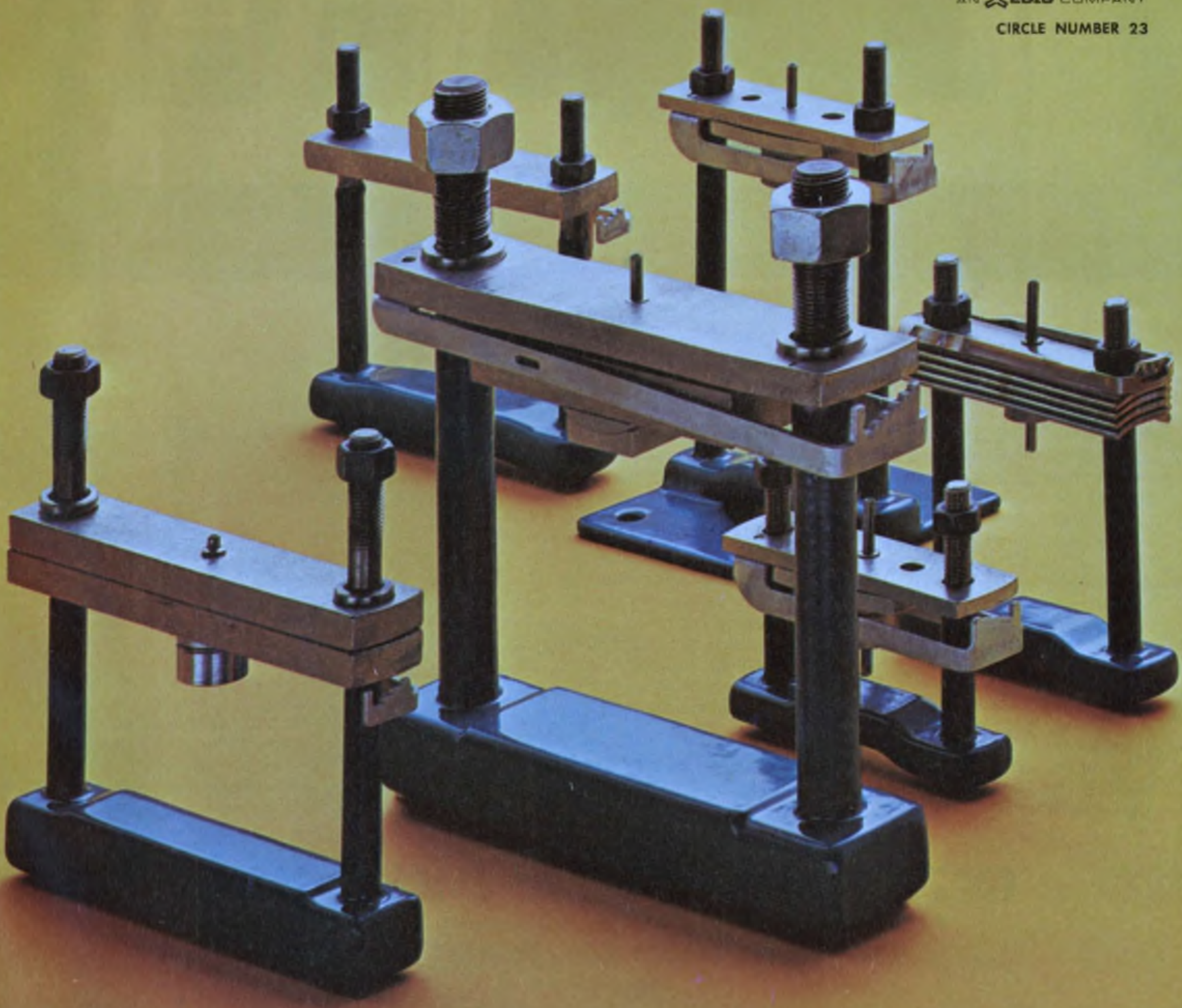
| | |
|---|---|
| Capacitance Range | 130 uF to 16,500 uF |
| ESR Values at 10 kHz | From .012 ohms |
| Impedance Value at 100 kHz | From .015 ohms |
| Typical Inductance | 12 to 15 nanohenries |
| Max. Ripple Current Capability at 10 kHz* | 15.9 amps at 65°C; 11.6 amps at 85°C |
| Operating Temperature Range | −55°C to +105°C |
| Voltages Available | 6.3 to 100 VDC |
| Nominal Case Sizes | .750" x 1.625" (19.05 mm x 41.27 mm) to 1.000" x 3.625" (25.40 mm x 92.08 mm) |

**For high ripple current applications, units may be installed in parallel.*

Write for specs and engineering samples. Sangamo Capacitor Division, Box 128, Pickens, SC 29671; phone: (803) 878-6311; TWX: 810-397-2496; Telex: 57-0441.

SANGAMO WESTON
Schlumberger

CIRCLE NUMBER 22



# The 8080As are not all alike; you should know the differences

While the various 8080A chips are pin-compatible and essentially alike, there are several logic differences in the flag flip-flops that are set and reset by arithmetic and logic instructions—as well as differences in speed, power and noise immunity.

The 8080A, which has rendered the 8080 obsolete, is now available from Intel, Advanced Micro Devices (AMD), National Semiconductor, Nippon Electric Corp. (NEC), and Texas Instruments.

"Many companies use the different vendors' 8080As interchangeably, once they understand about the auxiliary carry flag," says one industry engineer. "But there are usually some problems in incoming inspection because of the flag differences. The tester shows up the fact that the chips from different manufacturers treat these flags differently."

Furthermore, he believes, the 8080A, for all its popularity, doesn't quite have the status of a production device. "When you go to multiple-sourcing, you can't just turn the problem over to purchasing. You have to involve engineering and the incoming-inspection people, too."

Andrew Allison, AMD's MOS $\mu$P marketing manager, agrees. "The Intel 8080A and the National device, which appears to be an exact copy of it, have what we think is an internal design error. Intel's design allows logic operations to disturb the contents of the auxiliary carry-flag register. We developed our chip design

*(continued on page 42)*

## Eliminate microprocessor bugs with system analyzer

Designed to develop and debug microcomputer systems built around 6800 $\mu$P, the AQ6800 system analyzer from AQ Systems connects to the microprocessor via a buffered, 40-pin clip-on probe. It also displays all address and status data.

The system analyzer is interactive, and can transmit or receive data from all 6800 internal registers; modify the contents of any RAM location; examine any memory location; and send and receive data from selected I/O ports.

Front-panel controls permit getting to the memory and internal registers, controlling the microprocessor, setting the breakpoints and monitoring specific memory locations. An optional sequence recorder can record up to 128 instruction addresses to help simplify program tracing and debugging.

All circuitry is mounted on one motherboard. The entire system measures 19 × 10.5 × 1.875 in. and requires 5 V at 3 A.

Base price of the analyzer is $875 and delivery takes as long as six weeks. Although the analyzer is made by AQ Systems of Yorktown Heights, NY, it can be ordered from E & L Instruments.

*E & L Instruments, 61 First St., Derby, CT 06418. (203) 735 8774.*

CIRCLE NO. 508

*(continued from page 41)*
independently, as did NEC, and neither of us made that error.

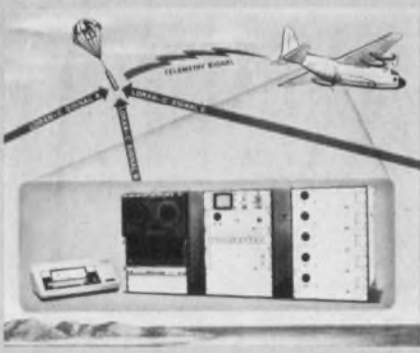
"To sidestep this problem, you save the carry bit *before* a logic operation and reload it into the carry-flag register afterwards. Any program that does this will work the same with all 8080As. The logic differences among the versions become insignificant."

Dave Millet, a $\mu$P product manager at NEC, adds: "We included a decimal subtract flag in the NEC 8080A that allows people to do decimal subtraction more efficiently. This saves program steps by storing the fact that the last operation was a subtraction."

Other differences in the available 8080As may make a particular version the best for a particular application. The AMD 9080A dissipates only two-thirds as much power as the Intel chip, and handles 3.2 mA on all outputs —Intel handles 1.9 mA. So the 9080A can drive two TTL loads instead of one. This capability can save two or three buffer ICs and reduce circuit delays. AMD's minimum voltage for a logic ONE is 3.0 V, Intel's 3.3 V. This means better noise immunity.

The NEC 8080A also specifies an input voltage of 3 V for a logic ONE, uses fewer clock cycles for some operations, and eliminates one 80-ns data-setup time requirement. To simplify interfacing to CMOS, the NEC 8080A has no internal pull-up resistors on the chip inputs. Moreover, this unit operates over a temperature range of $-10$ to 70 C, compared to Intel's 0-to-70-C range.

## Atmospheric-measurement system uses $\mu$Ps to preprocess data



Providing detailed atmospheric profile measurements, the WL-3DS Environmental System developed by Beukers Laboratories, Bohemia, NY, uses five 6800 microprocessors. The $\mu$Ps are used to preprocess meteorological parameters sent in by five dropsondes—free falling sensors—before the data are logged on tape and processed by a Nova minicomputer.

The system continuously samples wind speed, direction, temperature, humidity and pressure via the dropsondes. Dropsondes can provide readings starting at altitudes as high as 30,000 ft and dropping down to sea level.

Usually the dropsondes are released at five-minute intervals from an aircraft over the measurement area. Using the retransmission of Loran-C long-range, navigational-aid signals, the Beukers system determines dropsonde position, speed and direction. The Loran-C signals are processed by an on-board minicomputer and then logged with the data.

## Bipolar microprocessor kit permits system evaluation

Dubbed the 8X300KT100SK, this evaluation kit allows designers to assess the 8X300 bipolar $\mu$P developed by Signetics. The single-board kit includes all components necessary to get a minimal system up and running: one 250-ns, instruction-cycle-time CPU, four I/O ports, 256 bytes of RAM and a preprogrammed monitor system in ROM.

Controls in the evaluation kit for diagnostic and instructional purposes include a wait mode for single stepping, the ability to change program flow and to change or examine internal registers, and one-shot or repeated-instruction jamming. The board layout permits simple system modification and expansion.

*(continued on page 44)*

# DUAL COIL CIRCUIT BREAKER

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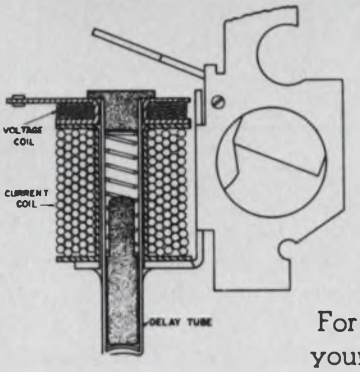


**Current Coil Ratings.** The current coil ratings are from 0.050 to 30 amperes at 65V dc or 250V ac maximum, 60 or 400 Hz. (Other models to 100 amperes.)

For more detailed information, call your local Airpax representative or contact Airpax Electronics, Cambridge Division, Cambridge, Md. 21613. Phone (301) 228-4600. Telex: 8-7715. TWX: 865-9655. Other factories in Europe and Japan. European Sales Headquarters: Airpax S.A.R.L., 3 Rue de la Haise, 78370 Plaisir, France.

AIRPAX™

THE PRO IN PROTECTION

CIRCLE NUMBER 25

*(continued from page 42)*
All signals from the $\mu$P can be brought off the board. A bare section permits custom interfaces to be built.

One of the few fixed-instruction bipolar microprocessors, the 8X300 has a 13-bit address bus and a separate 16-bit instruction bus. An 8-bit interface vector bus, which is supported by four additional control lines, and a clock perform data handling and I/O-device addressing.

The evaluation kit costs $299 and is available from stock.

*Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Robert Lanford (408) 739-7700.*

**CIRCLE NO. 509**

## Compact software development system emulates the EA9002

Designed to speed up software development for the EA9002 microprocessor, the EASE 2000 emulator includes an Editor program and 2 kbytes of workspace. The self-contained development/debug system from Electronic Arrays also has its own hexadecimal keyboard, 14 special-function keys and an 8-digit hexadecimal LED display.

There are two basic operating modes, Execute and Edit, and a resident assembler is optionally available. In the Execute mode, the program can run at normal clock speeds, or it may be stepped one instruction at a time. In the Edit mode, both internal and external memory can be examined or modified.

Specialized function keys include reset, jump, read, write, step, edit, continue, memory-select, register-select, scratchpad select, TTY-select and breakpoint-select. Programs can be loaded via the hex keyboard or with paper tape through a TTY port.

The entire EASE 2000 system is housed in a case almost as big as a large printing calculator. All power supplies are built in, and all I/O lines fully buffered. Base price is $995, and the optional resident assembler package costs an additional $250. Delivery takes 30 days.

*Electronic Arrays, 50 E. Middlefield Rd., Mountain View, CA 94043. Richard Eiler, (415) 964-4321.*

**CIRCLE NO. 510**

## Micro Capsules

**A simplified version of Basic,** developed for industrial users, is being readied by National Semiconductor, Santa Clara, CA. Called NIBL (National Industrial Basic Language), the program will fit in less than 4-k words of ROM and require 2-k words of RAM workspace. . . . **The Intelligent Breadboard,** soon to be released by IMSAI, San Leandro, CA, connects directly to the bus on the company's 8080-based microcomputer. Two forms of the breadboard will be available—a kit for $435 and a completely assembled unit for $625. . . . **A low-cost intelligent terminal,** being developed by Southwest Technical Products, San Antonio, TX, promises to be a boon to companies that need intelligence but can't justify paying several thousand dollars for a terminal. The terminal will be available in kit form for under $300, less monitor. . . . **The First West Coast Computer Fair,** reportedly the first west coast convention exclusively devoted to personal, home and hobby computing, is scheduled for April 15 to 17, 1977 at San Francisco's Civic Auditorium. Additional details can be obtained by contacting Jim Warren at (415) 851-7075 or writing to him at Star Route Box 111, Woodside, CA 94062.

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CIRCLE NUMBER 26

# CB servicing is PROFITABLE with the B&K-PRECISION 40-channel CB Test Bench

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- **Measure adjacent channel rejection on any channel**
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- **Measure SSB power output with TRUE peak-reading RF Wattmeter**
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- **Check SSB modulation with a two-tone test—the only accurate way!**
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**· Audio wattmeter · Audio generator · Distortion meter · RF wattmeter/dummy load · DB meter · SWR bridge**

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**MODEL 1403A—3", 5 MHz Recurrent Sweep Oscilloscope**

Checks CB modulation and provides viewing of 27MHz CB envelope when used with the Model 1040. Small, compact and inexpensive, it frees other scopes for more effective use. **$209**

**MODEL 1640—Regulated Power Supply**

Designed especially for CB and other mobile equipment, the 1640 eliminates changes in supply voltage due to load variations. A stable power supply is essential to precise testing of the transceivers. Less than 0.8% variation from zero to full load, 3 amps continuous, 5 amps surge. Adjustable to any output from 11 to 15 VDC. Suppressed zero scale for greater accuracy. Overload protected. **$100**

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**CIRCLE NUMBER 27**


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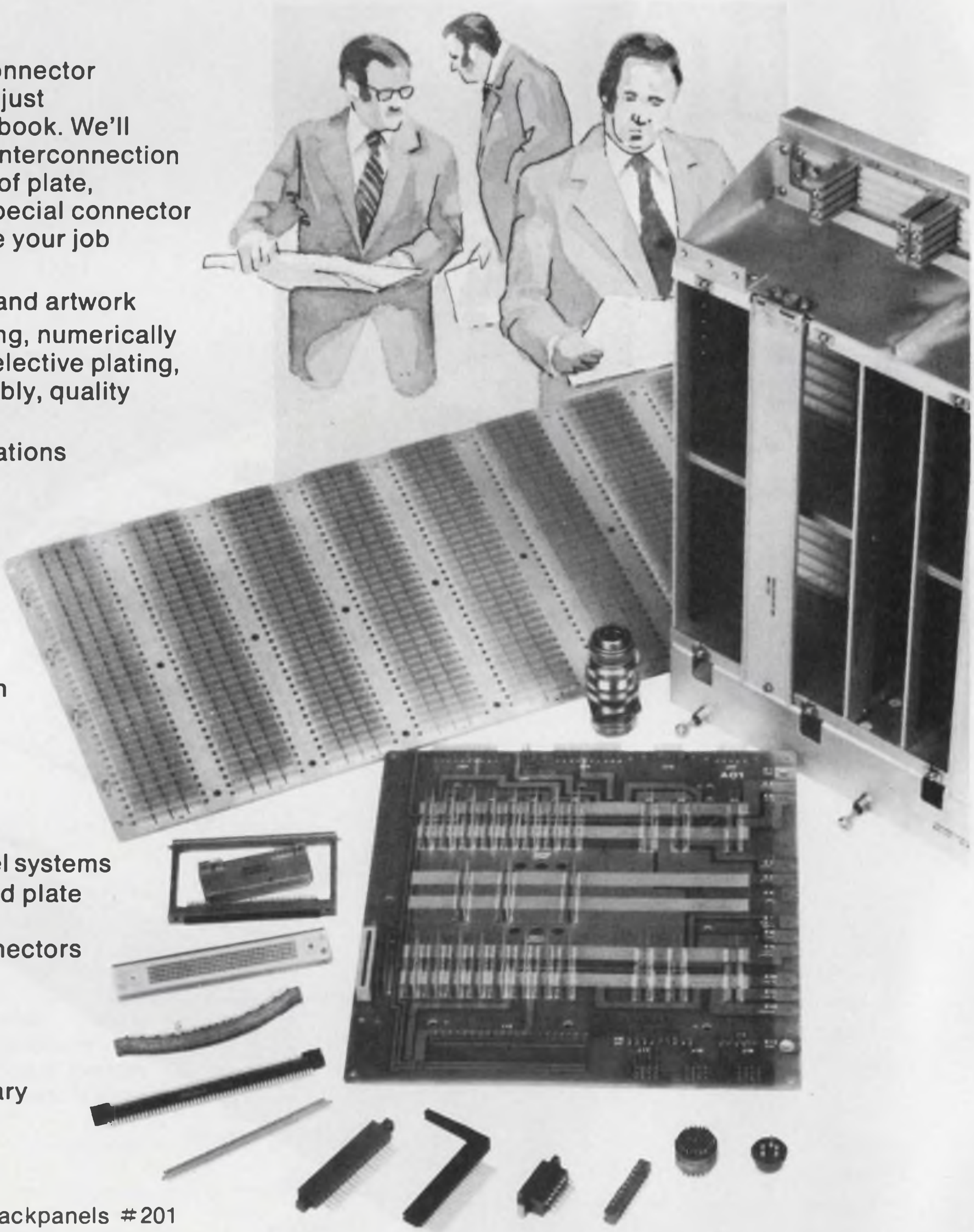

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Editorial

# Are all men brothers?

I've always been deeply moved by the line, "All men are brothers," in the "Ode to Joy" at the conclusion of Beethoven's magnificent Ninth Symphony. In this choral setting of Johann Schiller's poem, Beethoven emphasized the brotherhood of man in receiving the blessings of joy.

But I've always felt that in almost all other ways as well, men are much the same all over the world. The men I know in Europe and Asia share with men in the States the same interests —mainly women. After that, all people seem to prefer good food, good wine, good entertainment, good books, good everything.

I thought of this some weeks ago at a Motorola bowling party during the Electronica Show in Munich. After an hour of beering and bowling, I noticed that my buddies included a chap from England, one from France, one from Finland, one from Sweden and three from Germany. What distinguished us were the facts that I, alone, could speak only English; my bowling skill was worse than anyone else's; and our Englishman could hoist and put to proper use an enormous mug of beer. Beyond that, we were indistinguishable.

A few nights later, I was dining with Dr. Friedrich Baur, a delightful gentleman who runs the Components Div. of Siemens. And he shook me up. "Why," he challenged, "do people in different parts of the world buy so differently?" Taking time out to appreciate some delicate smoked trout and some hearty venison, we talked of national differences that affect all engineers designing for world markets.

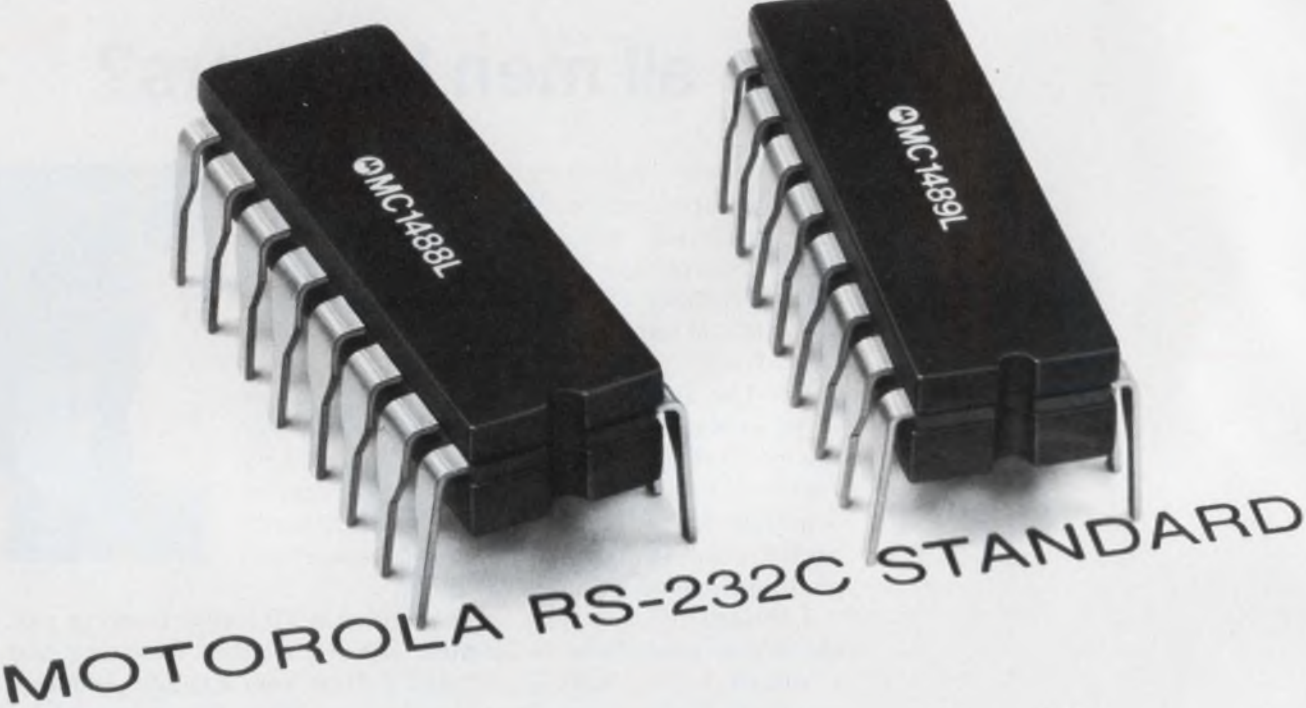
In the States, most people buy cars with automatic transmission; in Europe, relatively few do. In the States, "instant-picture" cameras are enormously popular; in Europe, they're not. In Europe, most full-size television receivers are sold with remote control. In the States, almost nobody buys remote control. Why?

Well, we kicked around some possible answers. It's because the European demands quality, one of us suggested, and he's willing to pay for it. But that's really no answer; it's the doorstep to another question.

There's no clear answer, we agreed. But is there, at least, a plausible theory? I wonder if readers of ELECTRONIC DESIGN can offer one. Ideas anyone?

George Rostky

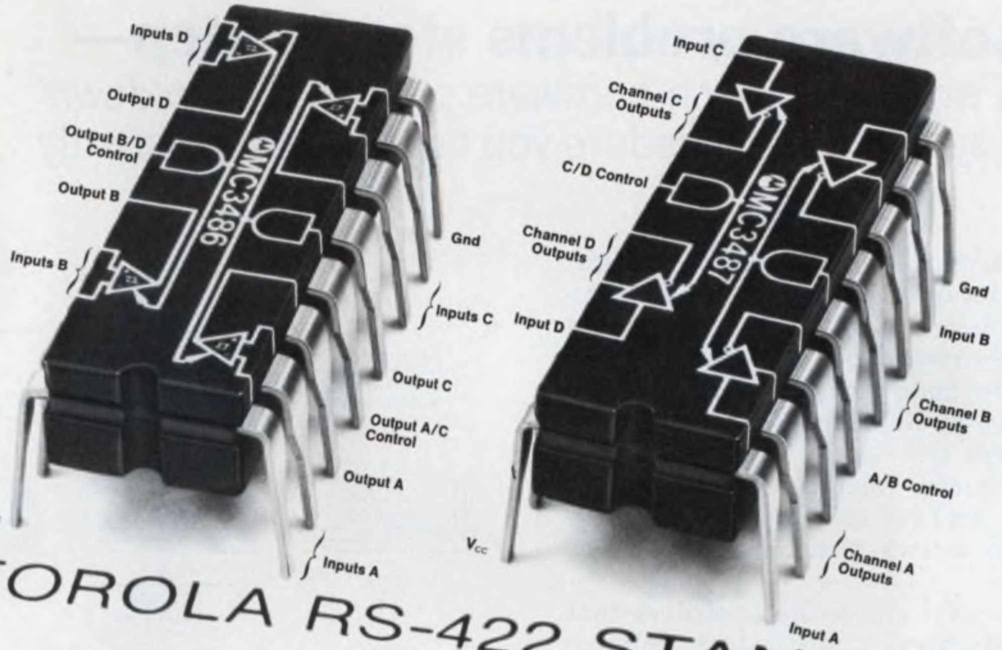
GEORGE ROSTKY
Editor-in-Chief




# Once A Linear Winner,

The quads everybody copied. Motorola-originated MC1488/1489 Line Drivers/Receivers set the RS-232 data comm standard since their introduction in 1969.

MOTOROLA


Inputs D
Output D
Output B/D Control
Output B
Inputs B
MC3486
Gnd
Inputs C
Output C
Output A/C Control
Output A
$V_{cc}$
Inputs A
Input C
Channel C Outputs
C/D Control
Channel D Outputs
Input D
MC3487
Gnd
Input B
Channel B Outputs
A/B Control
$V_{cc}$
Channel A Outputs
Input A

# Solve software problems step by step—

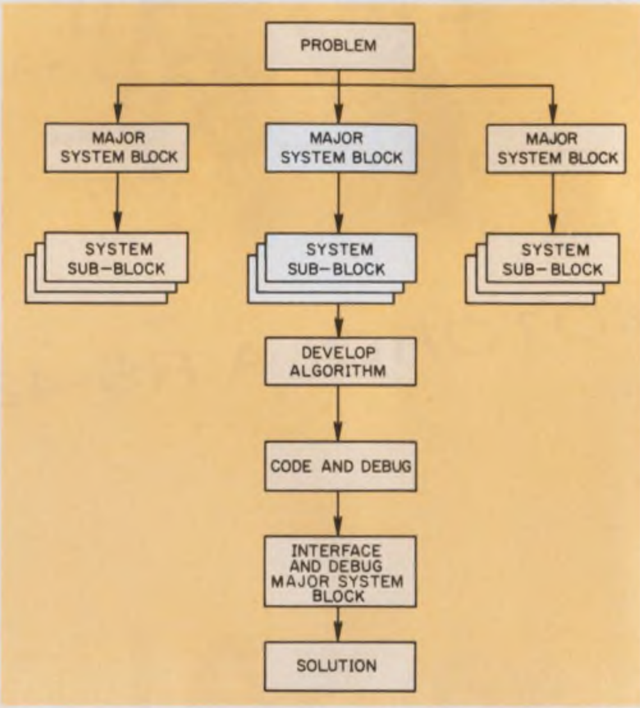
## just as you would approach hardware problems. 'Top-down' design is a systematic procedure you can follow consistently.

Is there a secret to good software design? Judging by the incantations that used to accompany software design in the past, you might think so. But the secret simply is to be systematic and consistent in your design. Once you have established a step-by-step procedure that works, stick with it, even for "trivial" tasks. You will find your programming faster, more efficient and less error prone. And you can pay more attention to the economic factors that separate success from failure.

To establish a software design procedure that works, you must learn to distinguish between strategy and tactics. The strategy part of software design is independent of the language and the computer to be used. To develop the strategy you look at the big picture, objectively state the problem, and break it down into manageable functional blocks that can be analyzed individually.

Systematic software design strategy is often called top-down design, because it follows the procedure outlined in Fig. 1.

Once your strategy is established, you can tackle the tactics—namely, the ways to implement the solution on a specific machine with a specific language. Consistent tactics for good program design require the discipline of structured programming, which will be discussed later.




1. **Solving problems systematically** is the secret to good software design. This flow chart illustrates the sequence of events for the "top-down" design approach.

### Step 1: Define the problem

Before you can solve any software problems, you have to decide exactly what the finished software system must do. Defining the system's operational characteristics is called the "functional specification." Writing a functional specification can be easy for small problems that require specific solutions. But a large and complex problem may require judgment, conceptual design decisions, and hardware/software tradeoffs. Simple systems can be specified in a few pages, while complex systems can require hundreds. So, the following information should always be present in any functional specification:

- Problem statement—one short paragraph that concisely describes the problem the system must solve.
- Hardware—a list of all hardware required, including the characteristics of each input and output signal or device.
- Software interfaces—when new programs co-exist with other programs, the details of the interfaces must be included in the specifications. They may have a significant effect on the new design.
- User's description—the largest section of the functional spec. It includes a complete description of the system from the outside world's point of view. It should also describe user interaction, data required, output produced, special features,

**Robert W. Ulrickson,** President, Logical Services Inc., 711 Stierlin Rd., Mountain View, CA 94043.

error-condition handling, and so forth.

A thorough specification is the key to a successful project. It is well worth spending the time to specify the problem carefully and completely at the beginning. Otherwise you will interrupt yourself constantly, fill in the blanks of the problem definition.

Once you have a completely functional specification, stick with it. If you don't, you are likely to run into that dreaded software disease known as "creeping features." This infection occurs when an inadequate problem specification permits organisms known as "neat features" to creep in, after you've started to work on the solution.

As a result, changes that are easily accommodated in the planning stage may require massive redesign efforts during the implementation stage. The farther the work progresses, the worse the problem becomes. The disease is often well advanced before detected, and has proven fatal to many software projects. Marketing people who are frequently the carriers have been known to infect entire engineering departments. While you certainly should incorporate advanced product features, they must be designed in from the top, not added from the side. If you do fall prey to creeping features, then you probably should have spent more time brainstorming during the specification stage.

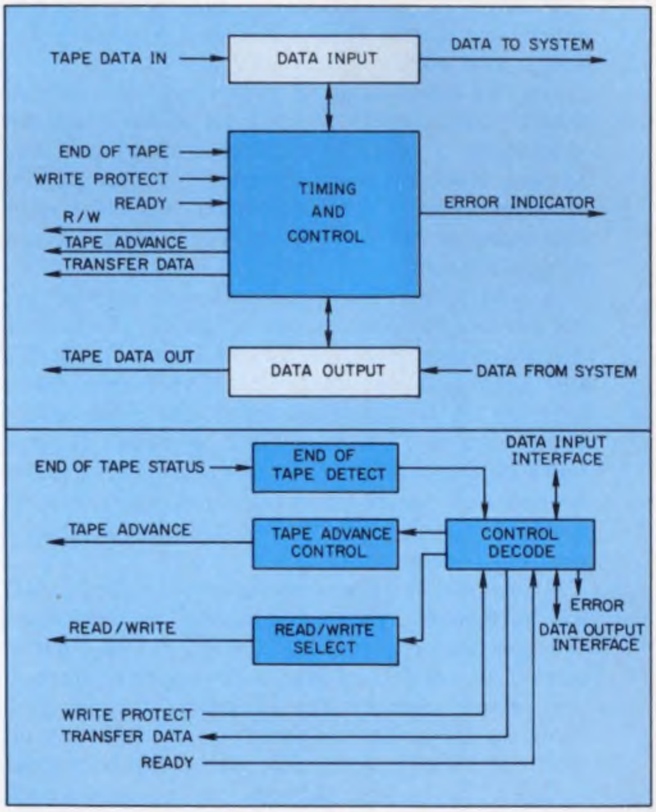
### Step 2: Partition the problem

Once the functional specification is complete, divide the whole problem into smaller functional blocks that can be analyzed and implemented individually. These blocks can be as complex as a complete floating-point arithmetic package or as simple as a few data-conversion instructions.

During program execution, control passes from one functional block to another, so that the functional block diagram can be considered the highest level of system flow chart. You continue partitioning the problem to as many levels of blocks and sub-blocks until algorithm development for each block becomes straightforward. If you are new to the game, do not hesitate to partition down to blocks that are almost trivial. You will often find that the algorithm for each detailed block becomes very simple. The partitioning process is quite flexible and allows you to adjust the level of block detail to the complexity of each part of the problem.

The initial system blocks can usually be determined from the functional specification. You only have to identify major system structures without being concerned how they operate. Some common initial blocks are: input operations; output operations; program functions (such as data transfers, memory searches, arithmetic operations); system timing and control; and major data structures such as tables and lists.

Once the initial blocks are defined, they are




2. **The block diagram for a tape I/O system** contains the major functional blocks (top). A major block, i.e., "timing and control" can usually be broken down into subblocks (bottom).

# The economics of software vs hardware

Microprocessor-based systems tend to be either hardware or software intensive because few engineers are equally familiar with hardware and software design. Almost any computer function can be performed in either hardware or software, but the choice should be based on economics, not personal preference. The most valuable tradeoffs between hardware and software can be made at the block diagram stage of the "top-down" design procedure.

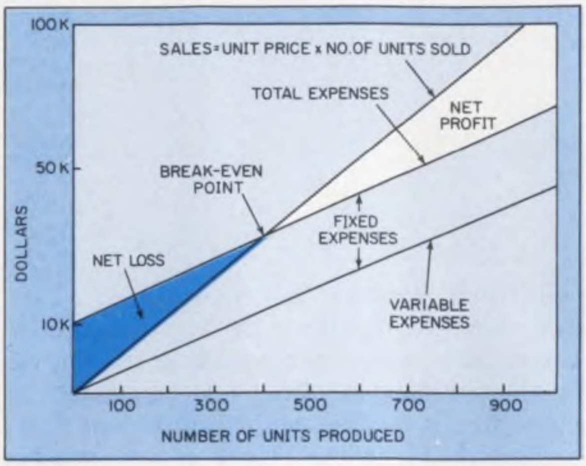
The total cost of a new product is the sum of fixed costs and variable costs. Fixed costs include all expenses independent of the number of units manufactured—hardware design, tooling, software design, system debug, documentation, and most overhead costs. Variable costs are directly proportional to the number of units manufactured and include the cost of components, materials, direct labor, the remaining overhead, and (usually inexpensive) copies of the software.

Evaluate the effect of fixed and variable costs on profits, with a break-even chart. By plotting costs vs the number of units sold, you can determine how many units you have to sell before loss turns into profit. Clearly, if you intend to sell 100,000 systems, you must minimize the variable cost of each system. You can spend $100,000 on development for every dollar per system saved in production. So, fancier software is much less costly than additional hardware for every unit sold.

On the other hand, if your production run is small, you shouldn't spend a lot on software development. Using the breakeven chart and the system block diagram together, you can decide whether to implement each functional block with hardware or software at an early stage of the design process.

A well known hardware/software tradeoff involves the decision to use a UART (Universal Asynchronous Receiver Transmitter) for serial interface to a terminal. The UART chip takes care of all the protocol for serial communications with a TTY or a CRT terminal. It provides all the timing, control logic, and data paths needed for parallel-to-serial conversion, start-and-stop-bit formatting for transmitting, and receiving serial data.

All of the functions performed by the UART in hardware can be replaced by software routines that require only a single bit of a hardware I/O port. Increased software development cost, more memory for program storage, and tying up the processor during serial I/O may or may not be less costly than using the hardware UART. The answer depends on the number of units produced and whether the processor can




be used to perform other tasks during serial I/O.

One of the thorniest tradeoffs involves system speed, memory size, and software. High-speed operations are usually equivalent to high-cost operations in the microprocessor world. Most Most single-chip microprocessors have clock rates in the 2-MHz range, and it takes a bunch of clock cycles to execute a string of instructions. Any operation you want the computer to perform that takes less than 100 microseconds, or must be repeated more often than every 100 microseconds, may tax the microprocessor's ability to respond. You can often overcome speed problems by using a TTL microprocessor, adding buffer memories, adding special-purpose hardware I/O devices and optimizing critical paths.

To develop your microcomputer system, you need a software development system. You can either use a time-share service, or buy your own. Time-sharing offers faster software development because a large, high-speed computer and powerful editing programs are available. On the other hand, you can connect your own hardware-development system to your I/O devices and terminals, and use it for real-time interfacing and debugging during prototype design. It can be a tough choice.

To better understand this tradeoff, assume that time-sharing costs about $15 per hour for connect time, plus about $200 per minute for CPU time, plus about $25 per month per 100 k-bytes of storage. With these rates, you can calculate the approximate cost of time-sharing for your projected usage. Don't be surprised if it comes out in the range of $2000 to $10,000 per month. Buying your own development system can cost you between $4000 and $15,000 up front for reasonable systems. If you plan to do a lot of program development over many months, plan to have your own system.

interconnected to form the system's block diagram. You must make sure that this block diagram is complete. It should contain blocks to implement all the features of the functional specification. The blocks must also be detailed enough for you to develop algorithms for them. If some blocks seem vague or ill-defined, add sub-blocks until they clearly and completely represent the functional specifications.

For example, examine the block diagram for a magnetic tape I/O driver program shown in Fig. 2. The major system blocks are at the top. The bottom section shows the second level of blocking for the most complex major block.

So far, you have not decided whether to implement a block with hardware, software or any combination of the two. Economic considerations should determine the optimum combination. The economics of hardware/software tradeoffs is a complex subject, which is discussed in the box.

### Step 3: Develop the algorithms

Having defined the problem, you can begin to seek solutions in the form of algorithms for each functional block. Each algorithm contains the fundamental logic required for each block, but remains independent of any specific computer or language.

When you develop the detailed logic of an algorithm, your most useful tool is the flow chart. It provides a convenient notation that is easy to document and check for logic errors. Flow charts may be used at any level of detail, but are especially valuable at a level that is more detailed than the block diagram but not so detailed that every line of code has its own block. To keep the design procedure consistent, and help others understand your work, you should adhere to the standard set of flow chart symbols shown in Fig. 3.

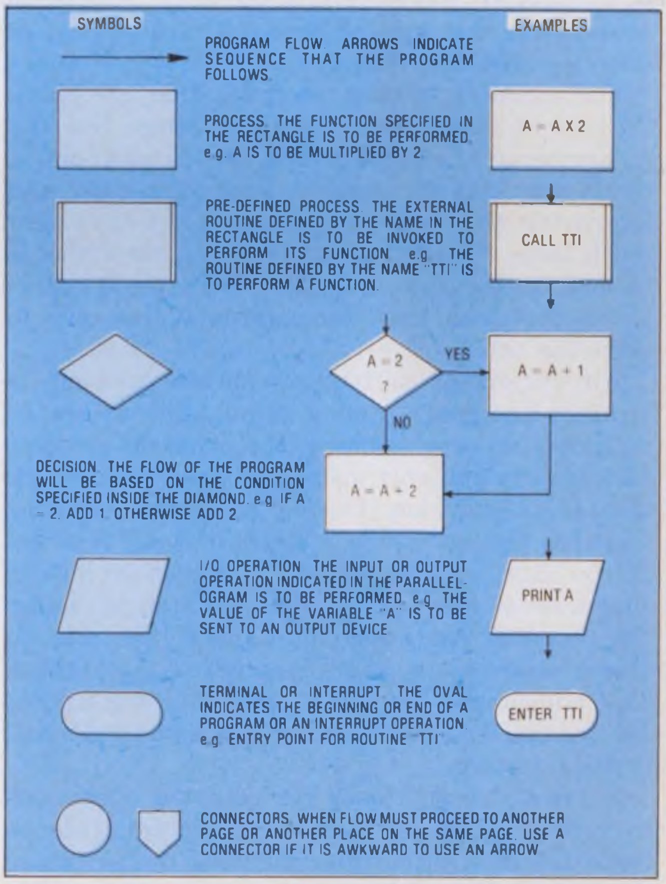
Algorithm development is the most creative part of software design, and experience plays a big part in your ability to develop creative algorithms. But some general procedures can help you to translate a logical system block into an algorithm:

- Decide what the block should do. You have done this to specify the problem, but now you are dealing with a particular program segment instead of the whole system.
- Determine how to obtain the raw data. Are they read into the system? Passed from another block? Looked up in a table? You need operational blocks in your flow chart to input the required data.
- Determine if the data require any pre-processing before they can be used. Do they have to be complemented? Rotated? Masked? Scaled? If so, insert the proper data-transformation blocks in the flow chart.
- Decide how to transform the raw data into the required outputs. This step requires process blocks, data, and decision blocks.
- Decide what to do with the processed data. Should they be re-formatted? Saved? Passed back to the calling routine? Add the blocks that prepare the data for output.
- Examine your flow chart. Make it your goal to keep it simple, straightforward, logical and clear. Be particularly careful about entering and exiting routines.

### If at first you don't succeed . . .

Algorithm development accounts for the largest portion of your work. It is an iterative process and may require several tries before it is complete and correct. Start by writing down the sequence of operations in the order they will be performed. For example, "read data in, test for control characters, then test for lower case characters," and so on. After you determine the general steps to be performed, add the process and decision blocks that actually perform these operations to your flow chart.

Test your preliminary algorithm on paper with actual data to make sure that it works. Consider the extreme cases and try to imagine every




3. **Standard flow-chart symbols** help clarify the sequence of events in a program or algorithm, not only for the designer but also for other engineers.

possible data condition. Does the algorithm still work? Be patient and thorough, or your algorithm will cost you extra debug time later.

When your algorithm is complete you should have a logic flow chart that looks something like the example in Fig. 4. This chart solves the problem of reading a tape without reference to any specific hardware. Each block of the flow chart may require several instructions when translated into a specific language.

When you have developed algorithms for each program block, the complete strategy for solving the problem is established. What's left is tactics. You now need to know what machine will be used to solve the problem and what language will be used to implement the solution.

### Dig for gold—in your software

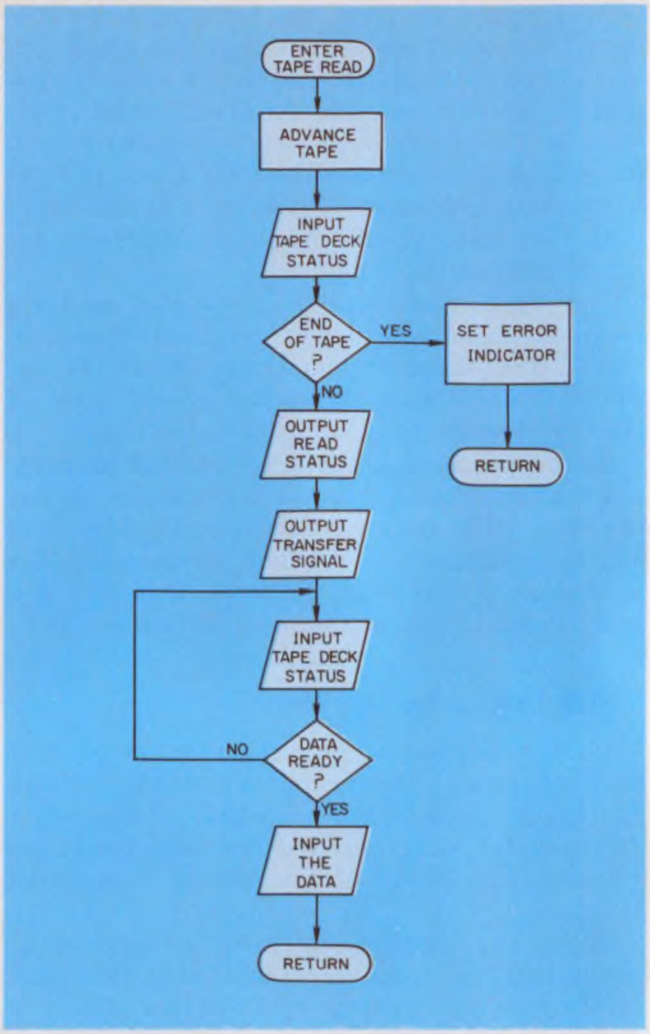
Not only hardware/software tradeoffs (see box) but also software/software tradeoffs may reduce your costs. One important consideration is the speed of execution.

Within the constraints of your microprocessor's clock rate, there are many ways to trade speed for memory size without impacting the other hardware. The best way to speed up a "slow" program is to find a more efficient algorithm. Selecting or designing a better algorithm is invariably more rewarding than efforts to squeeze the last byte of code out of a sloppy, or ill-considered, algorithm.

For example, take a program that calculates the sine of an angle to a given accuracy. Normally, an iterative algorithm evaluates a polynomial, but it may take an excessive time to execute. And improving the code will probably not save very much time. An alternate, and faster, algorithm is to look up the sine in a table. Now the question is whether you have the additional memory to store the table.

An important software/software tradeoff is straight-line programming versus subroutines. In straight-line programming, the program executes each instruction only once as it proceeds through the entire program. During execution you may find that the same code is repeated several times. If you sacrifice a little speed, you may be able to save a lot of memory by writing a subroutine for the repeated operation and calling that subroutine from the main program each time it is needed. The additional "overhead" housekeeping chores for the call and return process is usually a small penalty to pay.

Subroutines and loops for repeated operations may hide more pay dirt. When subroutines or loops are used often in a program, the processor may spend 80% of its time to execute 20% of the code. So, if you have a speed problem, you should first try to optimize the code that is repeated most often. If you can save one byte in a loop or subroutine that is executed 100 times, you will save 100 times more than if you save a byte in the main program.



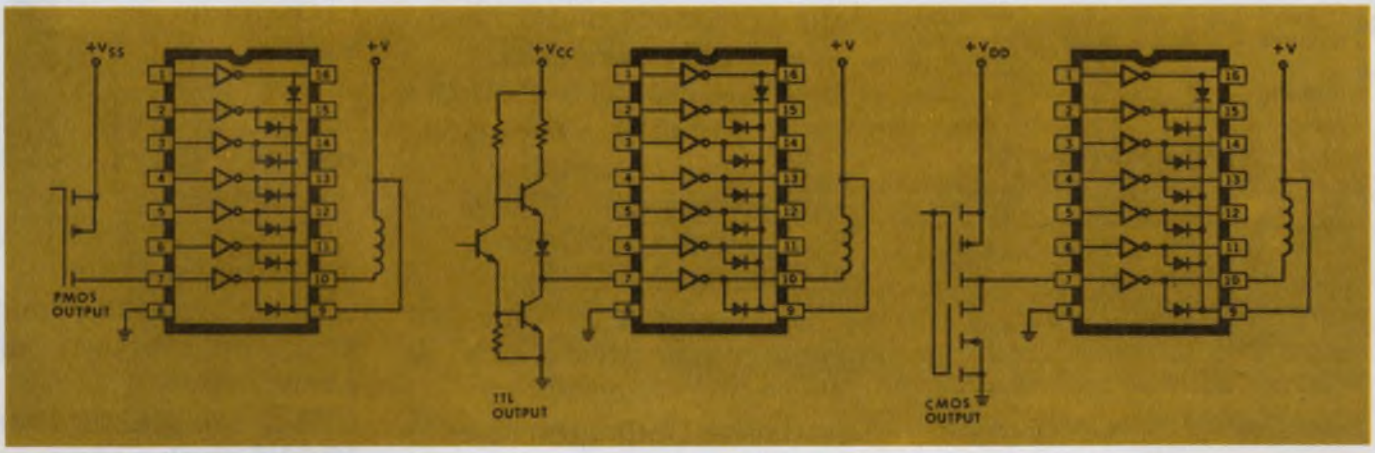

**4. This flow chart for reading a tape deck** is derived from the block diagram shown in Fig. 2. Each flow chart symbol may correspond to several computer instructions.

Your choice of language to develop your programs can also affect system cost greatly. Most higher level language processors produce at least 1.5 to 2 times as much machine code as programs written directly in assembly language, which means that 1.5 to 2 times as much memory is required to store the program. Also the program will take longer to execute. On the other hand, development time will be less because you can write and debug your programs much faster in a higher level language. And studies show that assembly language is usually more cost-effective for high-volume products, where minimum memory space and fast execution are most important.

Hardware/software tradeoffs and your programming strategy are vital steps in the over-all design process. But the tactics you employ to implement your strategy can be equally important, and will be discussed in the next part of this series. ■■

# INTERFACE ACE


## For High-Voltage, High-Current Interface with PMOS, CMOS, TTL, DTL . . . Sprague Darlington Transistor Arrays Have No Equal




A new exclusive Sprague development, Series 2000 Transistor Arrays are high-voltage, high-current integrated circuits comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. They feature open collector outputs and integral suppression diodes for inductive loads.

Supplied in 16-pin dual in-line plastic, these devices greatly reduce the number of discrete components used to interface between digital logic and high-voltage and/or high-current loads. In some applications, all discrete components can be replaced by a single DIP, resulting in substantial space and cost reduction.

With broad commercial/industrial application, these unique arrays are an excellent choice for interfacing to LEDs, solenoids, relays, lamps, and small stepping motors in printing calculators, cash registers, and control equipment.

Type ULN-2001A is a general-purpose array, pinned with inputs opposite outputs to facilitate circuit board layout. Type ULN-2002A is designed for use with 14 to 25 V PMOS inputs. Type ULN-2003A and ULN-2005A interface with TTL, low-power Schottky TTL, DTL, or CMOS operating at a 5V supply voltage. ULN-2004A has series input resistor to allow operation directly from CMOS and PMOS outputs utilizing 6V to 15V supplies.

***For more information, write or call George Tully, Semiconductor Division, Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606. Tel. 617/853-5000.***

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CIRCLE NUMBER 33

# DELCO'S NEW 25-AMPERE HIGH VOLTAGE DARLINGTONS WITH THE SPEED AND ENERGY CAPABILITY YOU ASKED FOR.

Good news for motor speed control designers who have expressed a need to upgrade horsepower ratings. The 25-ampere gain of these new Darlingtons permits increased horsepower ratings of existing AC motor speed control systems and a reduction in paralleling in new designs. However, grouping of $t_{off}$ is available for current sharing in designs with parallel Darlingtons. A speed-up diode is built into the DTS-4074 and DTS- 4075 permitting data sheet $t_f$ typicals of 1.0 $\mu$s. Drive circuit techniques involving $I_{B2} \geqq 2$ A and a Baker clamp produce $t_f$ typicals in the 0.4-0.6 $\mu$s range for the DTS-4066, DTS-4067, DTS-4074, and DTS-4075.

Our experience with tolerances, faults, transients, and start-stall conditions in most systems convinces us that these Darlingtons have the right trade-off between speed and peak power handling capability. Note the greater than 10 kVA region of the reverse bias safe operating graph. All this, and you still get Delco's traditional solid copper TO-3 hermetic package that has a conservative 0.75°C/W thermal resistance.

These Darlingtons are already in high volume production and are available on distributor shelves. Prices, applications literature, and data sheets from your nearest Delco sales office or Delco distributor can complete the story on these new Darlingtons.

### MAJOR PARAMETER LIMITS

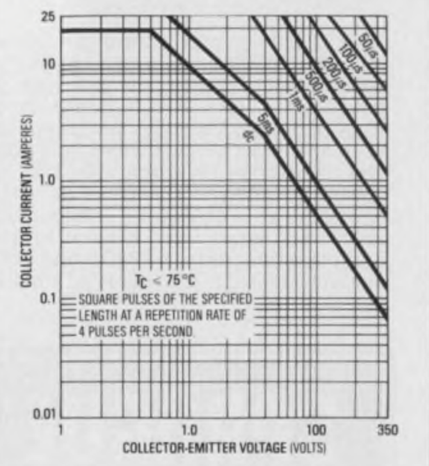
| Type | $h_{FE}$ @25A | $h_{FE}$ @10A | $V_{CEO}$ (sus) | $V_{CE}$ (sat) @20A | $I_{CEO}$ @600V |
|---|---|---|---|---|---|
| DTS-4066 | 5 | 75 | 350V | 3.5V | 0.25mA |
| DTS-4067 | 10 | 150 | 350V | 2.0V | 0.25mA |
| DTS-4074 | 5 | 75 | 350V | 3.5V | 0.25mA |
| DTS-4075 | 10 | 150 | 350V | 2.0V | 0.25mA |

### TYPICAL SWITCHING

| | DTS-4066 DTS-4067 | DTS-4074 DTS-4075 |
|---|---|---|
| $t_r$ | 0.5$\mu$s | 0.5$\mu$s |
| $t_s$ | 5.0$\mu$s | 3.2$\mu$s |
| $t_f$ | 4.5$\mu$s | 1.0$\mu$s |

NPN triple diffused silicon Darlingtons are packaged in solid copper cases conforming to JEDEC TO-3 outline dimensions.

### SAFE OPERATING CURVES




**Features of Delco's new DTS-4066, 4067, 4074, 4075 Darlingtons.**

- ☐ **Upgrade existing motor speed control horsepower ratings.**
- ☐ **Reduce need for paralleling in new systems.**
- ☐ **Offer switching speed improvements over our earlier types.**
- ☐ **Achieve greater than 10 kVA peak power dissipation.**
- ☐ **Available with $t_{off}$ grouping**
- ☐ **Delco hermetic copper package with 0.75°C/W.**
- ☐ **Currently in high volume production.**

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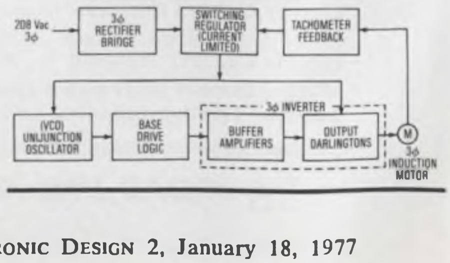

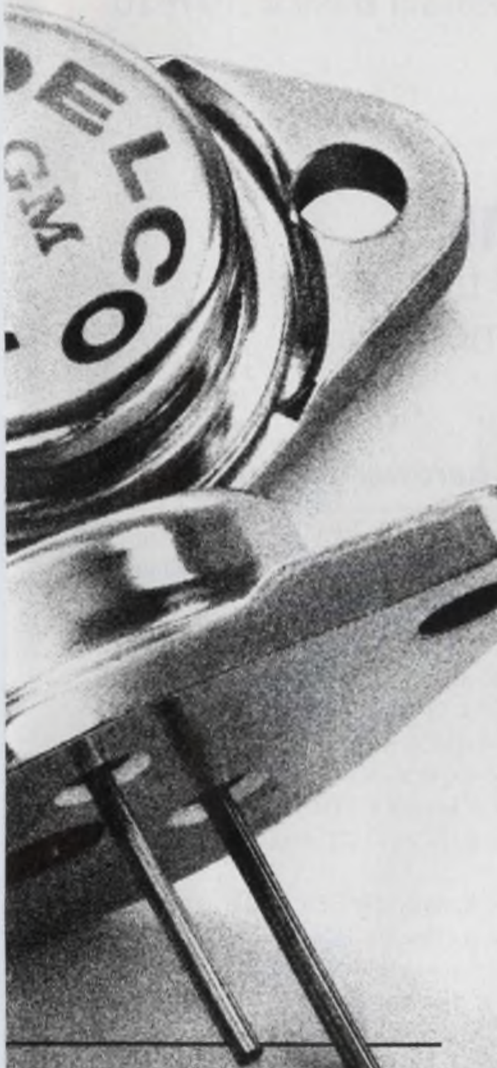


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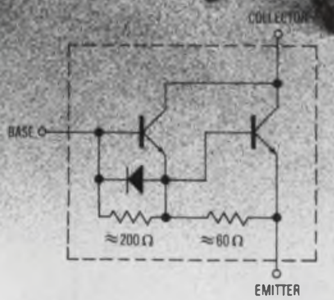


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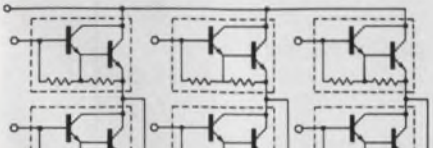


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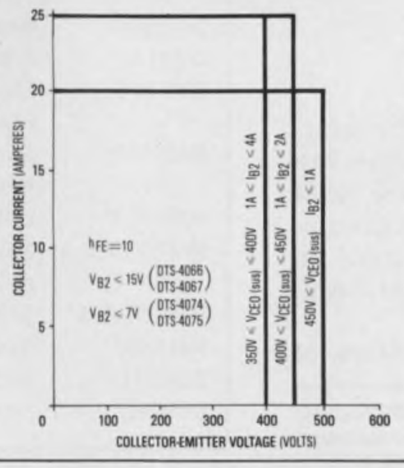



**Delco Electronics**
Division of General Motors
Kokomo, Indiana

CIRCLE NUMBER 34

# Develop systems around the SC/MP.

Two versions permit performance selection, and the versatile instructions allow simple addressing of the 65-k memory.

Available in either PMOS or NMOS, the SC/MP (simple, cost-effective microprocessor) enables you to choose an 8-bit $\mu$P by performance. And the multiprocessing capability of the $\mu$P, combined with its low cost, lets you put computing power where it's needed.

The SC/MP comes in a 40-pin dual in-line package with a set of 46 instructions. Both the p and n-channel parts are pin-compatible (except for three minor signal reversals), so system upgrades are simple—just pull out the p-channel unit, plug in the n-channel version and modify the ground and power lines. The NMOS $\mu$P can operate at clock rates of up to 4 MHz while the PMOS version is limited to 1 MHz rates.

Both the SC/MP and its development tools are easy to use. All necessary timing and clock signals are generated by SC/MP's built-in clock that can be either crystal-controlled or capacitively tuned. Like the 6100 $\mu$P, the SC/MP uses a 12-bit address bus. But it also uses four bits siphoned from the data bus to make a 16-bit address and thus address 65-k words of memory.

Of the 40 pins on the SC/MP, 20 are needed for data and address, two for power, two for clock generation, two for a serial I/O, three for flag lines and the remaining 11 for system control (Fig. 1a). All data transfers between memory and the $\mu$P are controlled by just two timing signals—negative address strobe and negative write or read data strobe (Fig. 1b).

### Systems assemble easily

Input/output procedures and memory interfacing are straightforward. A minimal system can be built from the SC/MP, along with some ROM and RAM (Fig. 2). For applications that require just a few words of RAM, pointer registers inside the $\mu$P can be used instead of external RAM. Then a two-chip system is possible.

Systems that require more than 4-k words of

**Dan Moss,** Design Engineer, and **Hash Patel,** Microprocessor Product Marketing Manager, National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051.

### Table 1. SC/MP hardware support

| Product | Description | Price (100-up) |
|---|---|---|
| SC/MP | 8 bit CPU chip | $ 9.00 |
| MM2102-1 | 1024 × 1 500-ns static RAM | 2.45 |
| MM2101-1 | 256 × 4 500-ns static RAM | 3.20 |
| MM2111-1 | 256 × 4 500-ns static RAM | 3.20 |
| MM74C89 | 16 × 4 CMOS static RAM | 4.50 |
| MM74C920 | 256 × 4 CMOS static RAM | 12.15 |
| MM1702A | 256 × 8 erasable ROM | 25.25 |
| MM5203 | 256 × 8 (512 × 4) erasable ROM | 25.25 |
| MM5213 | 256 × 8 maskable 5203 ROM | 12.50 |
| MM5204 | 512 × 8 erasable ROM | 29.50 |
| MM5214 | 512 × 8 maskable 5214 ROM | 17.50 |
| MM2708 | 1024 × 8 erasable ROM | * |
| MM5242 | 1024 × 8 MOS ROM | 12.50 |
| MM5246 | 2048 × 8 MOS ROM | 21.25 |
| DM8597 | 256 × 8 bipolar ROM | 15.85 |
| DM8596 | 512 × 8 bipolar ROM | 27.00 |
| DM85S28 | 1024 × 8 bipolar ROM | 27.00 |
| DM74S287 | 256 × 4 bipolar PROM | 3.22 |
| DM74S471 | 256 × 8 bipolar PROM | 8.25 |
| DM74S570 | 512 × 4 bipolar PROM | 6.98 |
| DM81LS95-98 | Three-state octal buffers | 1.35 |
| DM8542 | Quad I/O register | 4.50 |
| DM74LS374 | Three-state octal register | 1.75 |
| DS8833 | Three-state quad bus transceiver | 1.90 |
| DM8334 | 8-bit bit-addressable latch | 3.20 |
| DM8131 | 6-bit unified bus comparator | 2.56 |
| DM8546 | Three-state 8-bit I/O shift register | 3.84 |
| MM5307 | Baud rate gen./prog. real time clock | 12.00 |
| MM5303 | UART | 6.00 |
| MM74C922,3 | 16 & 20-key keyboard encoders | 3.80 |
| DS8692,3,4 | Seiko printer interface set | * |
| MM5357 | 8-bit a/d converter | 7.95 |
| CD4051 | 8-channel analog mux/demux | 1.17 |
| DP8212 | 8-bit I/O port | * |

* To be announced

RAM must use an external quad latch connected to the data bus (the four lower-order bits) to hold the block number of the 16, 4-k memory blocks.

No nonstandard peripheral circuits are required to support the SC/MP, so common latch circuits and RAMs and ROMs work with no interfacing problems (Table 1). All lines of the SC/MP are TTL compatible and can each handle one TTL load. When larger loads must be serviced, standard unidirectional and bidirectional buffers can be used to drive the bus. Both the address and data-bus outputs from the SC/MP use three-state logic to present minimal loading on the buses.

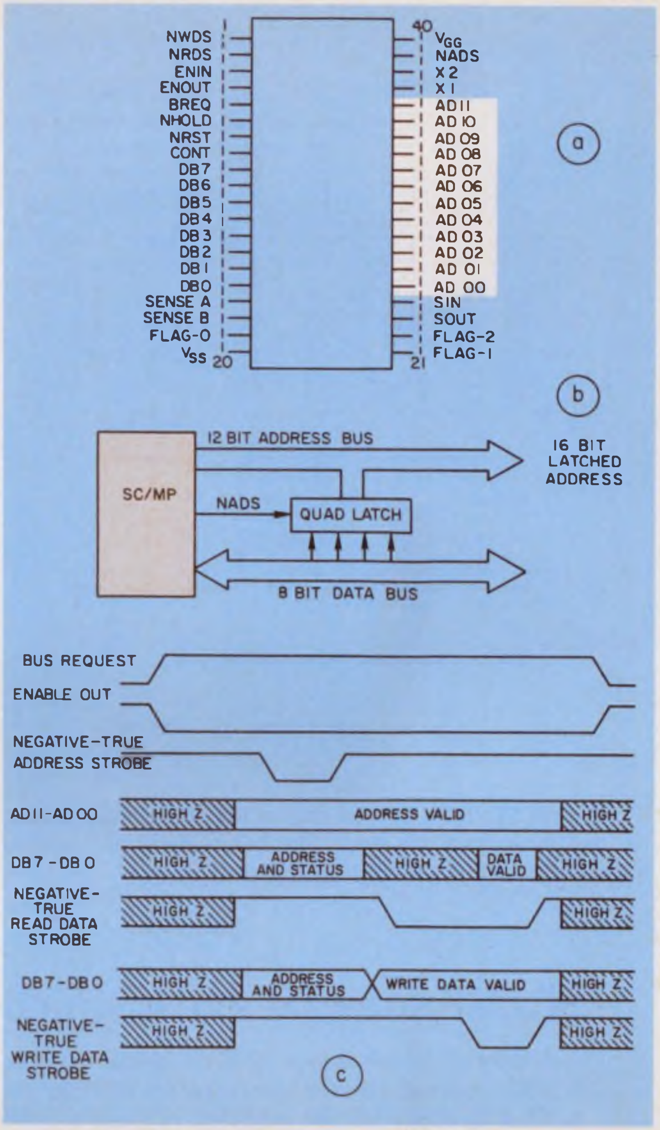
Several lines on the $\mu$P permit a few SC/MPs to be cascaded—all with direct interface to the address and data buses (Fig. 3). If the SC/MP is the only bus controller, the bus access control line can be hard-wired in the active state. All that's needed for using the SC/MPs in a multiprocessing mode are three control lines—enable in, enable out and bus request.

To power up the SC/MP, you can choose from several options. The PMOS units operate from +5 and −7 V supplies (Fig. 4a and b). The NMOS version of the SC/MP requires just a 5-V supply and can interface directly to most 5-V logic families (Fig. 4c).

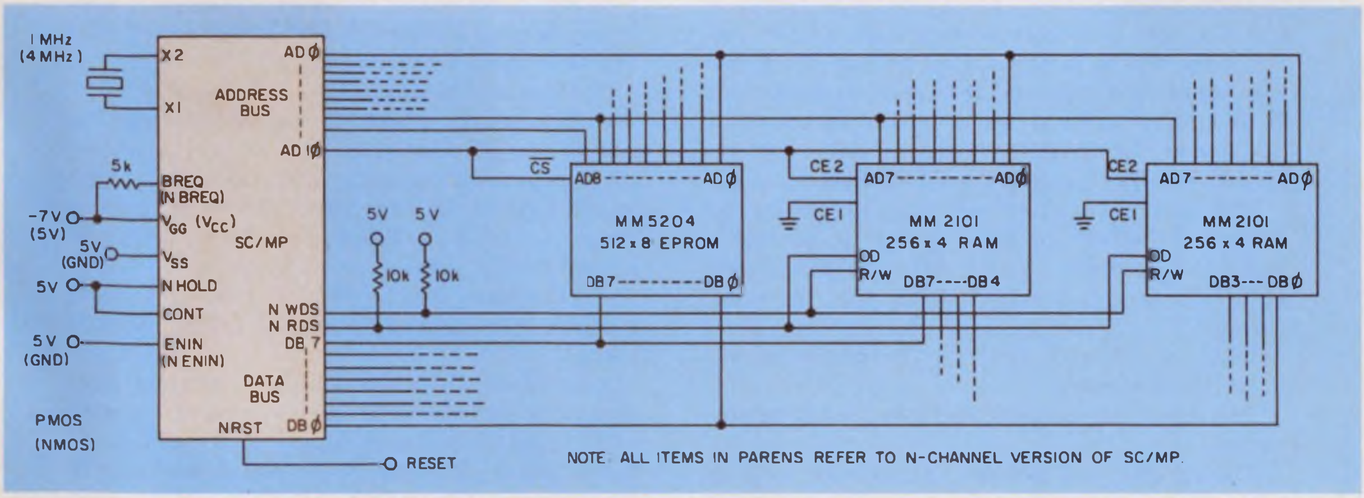
### Three signals control data flow

Before the $\mu$P can transfer data to or receive data from memories or peripherals, it must have access to the system-address and control bus. Bus access is controlled by three signals—the bus-request (BREQ), the enable-input (ENIN), and the enable-output (ENOUT). For simple systems with a single $\mu$P, the BREQ and ENOUT lines need not be used and the ENIN line can be permanently enabled.

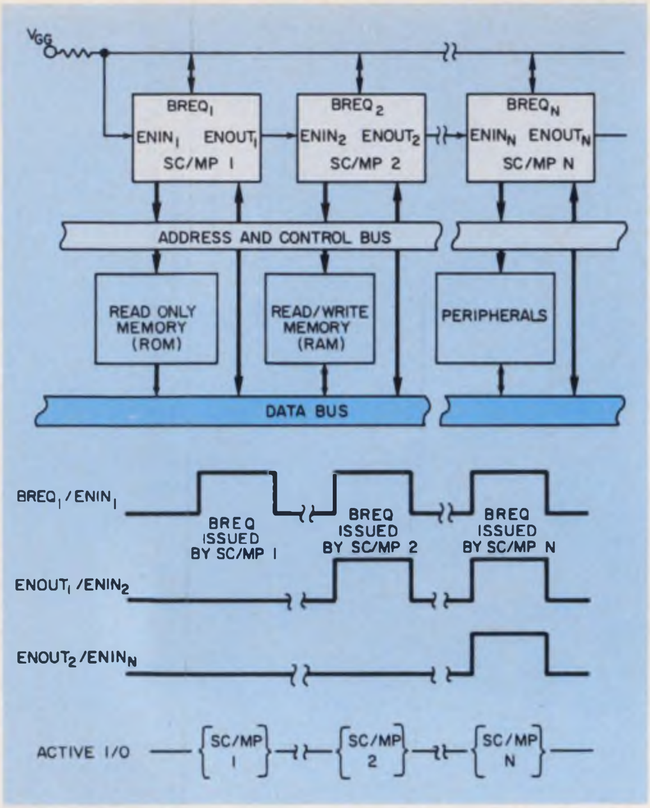
*(continued on page 64)*




1. **Because the SC/MP is crowded into a 40-pin package** (a), only a 12-bit address bus is used. To get full 65-k addressing capability, four bits of the data bus are used in addition to the 12 address lines (b). Only two lines, at the most, are necessary to control all the I/O timing (c): negative-true address strobe and negative-true read (or write) data strobe.




2. **Building a minimal operating system** with the SC/MP requires few external circuits. If little RAM is needed, the on-chip oscillator and pointer registers permit even smaller systems than the one shown.




**3. Several SC/MPs can be connected to common buses** for multiprocessor systems. The bus-request and enable lines permit simple control of the various $\mu$Ps.

In large systems, especially those with peripherals that transfer data at high speed, direct-memory access (DMA) can be implemented without involving the SC/MP. When a DMA is externally requested, the SC/MP requests bus access by bringing the BREQ line high. This signal alerts the DMA controller, and if the bus is idle (no peripheral is currently transmitting or receiving data) the ENIN line goes high and grants the bus access.

When the DMA transfer is completed, the BREQ line goes low and bus access is terminated. Peripherals can also request a DMA operation by using the peripheral-request and peripheral-enable lines on the user-designed DMA controller circuit.

The SC/MP can use readily available memories. For slow memory systems the SC/MP has several features that can circumvent the long access times. For example, its NHOLD (negative-true hold) input line lengthens the input/output cycle. When low, it holds the I/O cycle by delaying the rising edge of the NRDS or NWDS (negative-true read or write data strobe) pulses.

The NHOLD signal can also be used to add a simple debugging circuit to a SC/MP system. All the bus signals remain valid while NHOLD is low, so if LEDs are connected to each buffered

## SC/MP software and instruction set

Although it only has a 12-bit address bus, the SC/MP microprocessor can directly address up to 65-k words with the addition of just a quad latch. The $\mu$P handles both serial and parallel data transfers, has DMA capability, five flexible addressing modes, and can operate in multiprocessor systems. The software set has 46 commands, including some special instructions.

Three instructions, increment and load (ILD), decrement and load (DLD) and delay (DLY) provide some unusual capability. For instance, the ILD and DLD commands are useful for loop counters. These two instructions can fetch the loop count from memory, increment or decrement it and store the new value in the accumulator (AC) and the RAM. A "jump if AC = 0" instruction (JZ) completes the loop-count test.

The DLY instruction can delay processing by a variable length of time, which is computed from the contents of the AC, and the second style of the instruction with the following formula:

$$\text{DLY} = 12 + 2\,(\text{AC}) + 2\,(\text{displacement}) + 2^9\,(\text{displacement}).$$

The delay can range from 13 to 131,593 microcycles.

The SC/MP can address any byte in memory with only a two-word instruction: It uses one of the pointer registers and an offset value specified in the second byte of the instruction.

The SC/MP instruction set contains single and double-byte instructions. A single-byte instruction consists of an 8-bit operation code that defines an operation the SC/MP will execute. The double-byte instruction consists of an 8-bit op code and an 8-bit data or displacement field. When the second byte represents a data field, the data are processed by the $\mu$P during execution of the instruction. If the second byte represents a displacement value, the byte is used to calculate a memory address that will be accessed during execution of the instruction.

The five addressing modes include:

- PC-relative, which forms an address by adding the current contents of the program counter to a displacement value specified in the second byte of the instruction. The displacement range is from $-128_{10}$ to $+127_{10}$ locations around the PC value.
- Immediate, during which the second byte of a double-byte instruction is used as the operand (data).
- Indexed, which permits any memory location to be addressed. It uses a pointer register (PTR) and a displacement value, but otherwise works like the PC-relative method. A double-byte instruction specifies both the PTR and an 8-bit displacement to that pointer.

address and data line, they will show step-by-step program execution.

Serial-data transfers under program control are also possible with the $\mu$P. The serial-input and output pins (SIN and SOUT, respectively) work in conjunction with the extension register built into the SC/MP. A serial input/output (SIO) instruction shifts the contents of the extension register one bit position. The contents of bit position Ø are shifted into a built-in output flip-flop that holds the bit for the SOUT line. At the same time, data present at the SIN line are shifted into bit position 7 of the extension register.

Transfers on the data bus don't have to be synchronized to any particular timing sequence; devices with widely different data rates can all connect to the common bus.

### System timing starts with the clock

The SC/MP's built-in clock can operate at frequencies of up to 1 MHz for the PMOS version and 4 MHz for the NMOS model. For both models, either an external crystal with an equivalent series resistance of 600 $\Omega$ can be used for precision timing, or a capacitor can be connected across the clock terminals.

All necessary timing signals are generated by the on-chip clock and timing generator. If desired, the on-chip oscillator can be disabled and the $\mu$P's timing generator driven by an externally generated clock.

Inside the $\mu$P, instructions are executed in multiples of microcycles. In the PMOS unit, 1 microcycle is twice the period of the oscillator; in the NMOS unit, the microcycle equals four times the clock period.

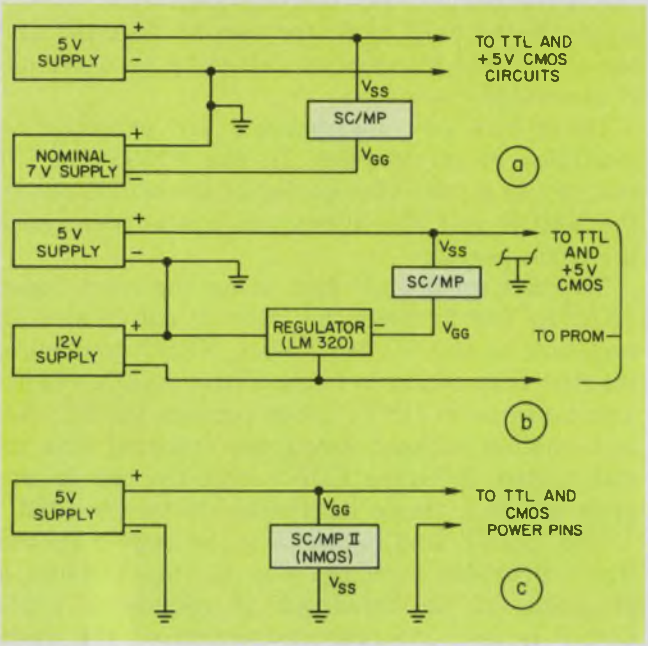
To start up the $\mu$P first bring the reset input (NRST) low to clear the internal status and all registers on the SC/MP. When NRST goes high, the first instruction is fetched from location ØØØ1. The continue (CONT) input permits the SC/MP to be halted without losing any internal data on status info. Bringing CONT high for one microcycle allows a single instruction to be executed.

The CONT line, since it is an asynchronous input, provides a simple way to step through a program. If an interrupt is requested while CONT is low, the first instruction of the user-

- Auto-indexed, which provides the same capabilities as the indexed mode, along with the ability to increment or decrement the designated PTR by the value of the displacement. In the indexed mode, the value of the PTR remains unchanged. However, in the auto-indexed mode the PTR value changes. If the displacement is less than zero, the PTR is decremented by that value before the contents of the effective address are fetched or stored. When the displacement is equal to or greater than zero, the PTR is incremented by that value after the contents or the specified location are fetched.
- Implied, which specifies only internal registers. For example, the copy status register-to-accumulator (CSA) command defines the status register as the originating operand and the accumulator as the destination operand.

The SC/MP can handle interrupts. When one occurs, the contents of PTR 3 are automatically exchanged with the PC to do a subroutine jump to the interrupt service routine. A jump-to-subroutine command also follows the same exchange procedure, except that any PTR can be used. For subroutine jumps, however, the PTR should be set to a value one less than the subroutine-starting address: The PC is incremented prior to the instruction fetch cycle.

| Double-byte instructions | | |
|---|---|---|
| Mnemonic | Description | Format |
| Memory reference instructions | | 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 |
| LD | Load | 1 1 0 0 0 m ptr disp |
| ST | Store | 1 1 0 0 1 |
| AND | AND | 1 1 0 1 0 |
| OR | OR | 1 1 0 1 1 |
| XOR | Exclusive-OR | 1 1 1 0 0 |
| DAD | Decimal add | 1 1 1 0 1 |
| ADD | Add | 1 1 1 1 0 |
| CAD | Complement and add | 1 1 1 1 1 |
| Memory increment/decrement instructions | | 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 |
| ILD | Increment and load | 1 0 1 0 1 0 ptr disp |
| DLD | Decrement and load | 1 0 1 1 1 0 |
| Immediate instructions | | 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 |
| LDI | Load immediate | 1 1 0 0 0 1 0 0 data |
| ANI | AND immediate | 1 1 0 1 0 1 0 0 |
| ORI | OR immediate | 1 1 0 1 1 1 0 0 |
| XRI | Exclusive-OR immediate | 1 1 1 0 0 1 0 0 |
| DAI | Decimal add immediate | 1 1 1 0 1 1 0 0 |
| ADI | Add immediate | 1 1 1 1 0 1 0 0 |
| CAI | Complement and add immediate | 1 1 1 1 1 1 0 0 |
| Transfer instructions | | 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 |
| JMP | Jump | 1 0 0 1 0 0 ptr disp |
| JP | Jump if positive | 1 0 0 1 0 1 |
| JZ | Jump if zero | 1 0 0 1 1 0 |
| JNZ | Jump if not zero | 1 0 0 1 1 1 |
| Miscellaneous instructions | | 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 |
| DLY | Delay | 1 0 0 0 1 1 1 1 disp |
| Single-byte instructions | | |
| Extension register instructions | | 7 6 5 4 3 2 1 0 |
| LDE | Load AC from extension | 0 1 0 0 0 0 0 0 |
| XAE | Exchange AC and extension | 0 0 0 0 0 0 0 1 |
| ANE | AND extension | 0 1 0 1 0 0 0 0 |
| ORE | OR extension | 0 1 0 1 1 0 0 0 |
| XRE | Exclusive-OR extension | 0 1 1 0 0 0 0 0 |
| DAE | Decimal add extension | 0 1 1 0 1 0 0 0 |
| ADE | Add extension | 0 1 1 1 0 0 0 0 |
| CAE | Complement and add extension | 0 1 1 1 1 0 0 0 |
| Pointer register move instructions | | 7 6 5 4 3 2 1 0 |
| XPAL | Exchange pointer low | 0 0 1 1 0 0 ptr |
| XPAH | Exchange pointer high | 0 0 1 1 0 1 |
| XPPC | Exchange pointer with PC | 0 0 1 1 1 1 |
| Shift, rotate, serial I/O instructions | | 7 6 5 4 3 2 1 0 |
| SIO | Serial input/output | 0 0 0 1 1 0 0 1 |
| SR | Shift right | 0 0 0 1 1 1 0 0 |
| SRL | Shift right with link | 0 0 0 1 1 1 0 1 |
| RR | Rotate right | 0 0 0 1 1 1 1 0 |
| RRL | Rotate right with link | 0 0 0 1 1 1 1 1 |
| Single-byte miscellaneous instructions | | 7 6 5 4 3 2 1 0 |
| HALT | Halt | 0 0 0 0 0 0 0 0 |
| CCL | Clear carry/link | 0 0 0 0 0 0 1 0 |
| SCL | Set carry/link | 0 0 0 0 0 0 1 1 |
| DINT | Disable interrupt | 0 0 0 0 0 1 0 0 |
| IEN | Enable interrupt | 0 0 0 0 0 1 0 1 |
| CSA | Copy status to AC | 0 0 0 0 0 1 1 0 |
| CAS | Copy AC to status | 0 0 0 0 0 1 1 1 |
| NOP | No operation | 0 0 0 0 1 0 0 0 |




4. **No ground pin is available** on the PMOS SC/MP (a and b), but operation is possible with a +5 and −7 V supply. On the NMOS version the $V_{ss}$ pin is used as the ground and the $V_{cc}$ line to +5 V (c).

generated-interrupt service routine is automatically executed.

The first operation performed by the μP for each I/O cycle loads the 12 least significant address bits onto the address bus and the four most significant address bits, along with four special status-flag bits onto the data bus. While all the bits are loaded, the NADS (negative-true address strobe) output is brought low to indicate that address and status information are valid.

The four status bits, R, I, D and H-flag, indicate the following: RFLG—when high, the current I/O cycle is a read cycle; when low, a write cycle. IFLG—when high, the instruction op code (single-byte instruction or first byte of double byte instruction) will be output from memory after a NADS signal. DFLG—when high, a delay instruction is being executed. HFLG—when high, the processor is held in the halt mode.

Systems based on the SC/MP can handle externally generated or program-initiated interrupts. When set, the internal-interrupt enable (IE) flag lets the sense-A line serve as an interrupt-request input (Fig. 5). When reset, the IE flag stops the SC/MP from detecting any interrupts.

While the IE flag is set, the sense-A input gets tested prior to the fetch phase of each instruction. Upon detection of an interrupt request, the IE flag gets reset, the contents of the program counter are exchanged with the contents of pointer register 3, and the contents of the program counter are incremented by 1 to address the first instruction of the user-generated service routine, thus handling the interrupt.

The various addressing modes of the SC/MP (see software box, p. 64) allow the μP to rapidly access any location in memory. The pointer registers are considered very powerful because all memory-reference instructions specify either a pointer-register or the program counter. An example might help illustrate the μP's versatility.

### An example illustrates the pointer

The example lets the SC/MP load a number from a RAM location into the accumulator (AC), add it to the value in the extension register (E), push the result onto a software stack and, finally, call a subroutine.

To set up the program, first make some pointer-register assignments:

P1 = RAM address pointer.
P2 = Stack pointer.
P3 = Subroutine pointer.

Next, write the program (the indexed addressing mode should be used):

```
LD 5(P1)      ; Load data stored at (pointer
                register 1) +5 into AC
ADE           ; Add value previously stored
                in E to AC
ST @-1(P2)    ; Push onto stack with auto-
                increment (@) addressing
XPPC P3       ; Jump to subroutine
```

To pull the value dumped onto the stack, use

LD @ 1(P2).

However, since P2 always points to the top of the stack, make sure that no other operations take place to change P2 before you access the stack.

If possible, the three pointer registers should be assigned so that each points to an important block of RAM or ROM, such as a subroutine, RAM variable list, a table, stack or I/O device.

For example, if all I/O devices are within a 255-word block of memory, one pointer can access all devices by using indexed addressing. A pointer must be loaded in two parts. The following list shows P2 being loaded from "lower" and "upper" RAM locations, which use P1 as their base pointer:

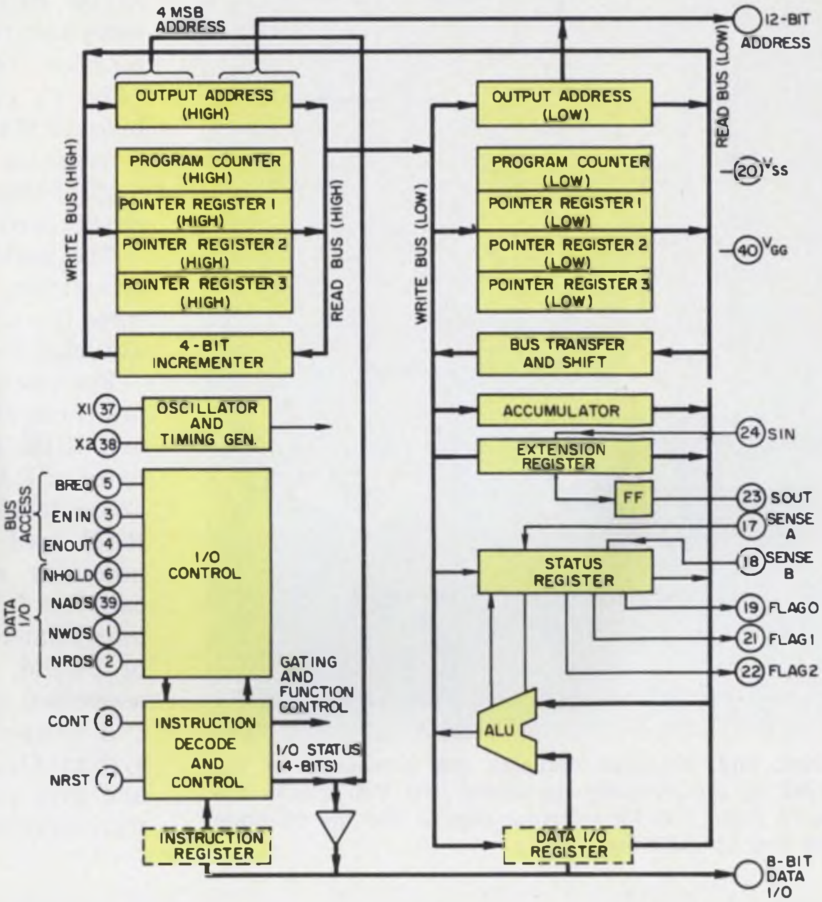
```
LD lower (P1)  ; Load lower 8 bits into AC
XPAL P2        ; Exchange AC with lower
                 half of P2
LD upper (P1)  ; Load upper 8 bits into AC
XPAH P2        ; Exchange AC with upper
                 half of P2
```

Load immediate (LDI) instructions can be used if data are in the program, not in RAM.

### System support comes in all forms

Since the SC/MP is designed with low system cost in mind, a variety of low-cost development aids are available to you (Table 2). The cheapest

# What goes on inside the SC/MP microprocessor?




The SC/MP microprocessor, in either its p or n-channel versions, forms an almost complete minimal microcomputer system. The chip has all the registers, the arithmetic and logic unit (ALU), an oscillator and enough buffers to drive one TTL load on every pin.

There are seven major registers in the SC/MP $\mu$P: a 16-bit program counter (PC), an 8-bit accumulator (AC), three 16-bit pointer registers (PTR), an 8-bit extension register (E) and an 8-bit status register (SR). Like other microprocessors, the PC holds the address of the instruction being executed. However, the PC's output is divided into a 4-bit, high-order address and a 12-bit, low-order address. When incremented, only the 12 low-order bits act as a counter; no carry is generated to the four high-order bits.

For systems that require more memory than the 12 low-order bits can address (4 kwords), the four high-order memory-address bits can be loaded into a 4-bit latch fed by the data bus when the address strobe line is low. They can also select any one of 16, 4-k blocks.

The AC is the main working register of the $\mu$P and is used for storing the results of ALU operations, as well as for data transfers, shifts and rotates.

Three pointer registers can be used as temporary memory storage, memory address-base pointers and subroutine address pointers but their primary use is in memory references. Either the upper or lower eight bits of a PTR can be exchanged with the contents of the AC, which permits the PTRs to be used as either address-storage or data-storage registers.

The E register, similar to the accumulator in function, can be used three ways:

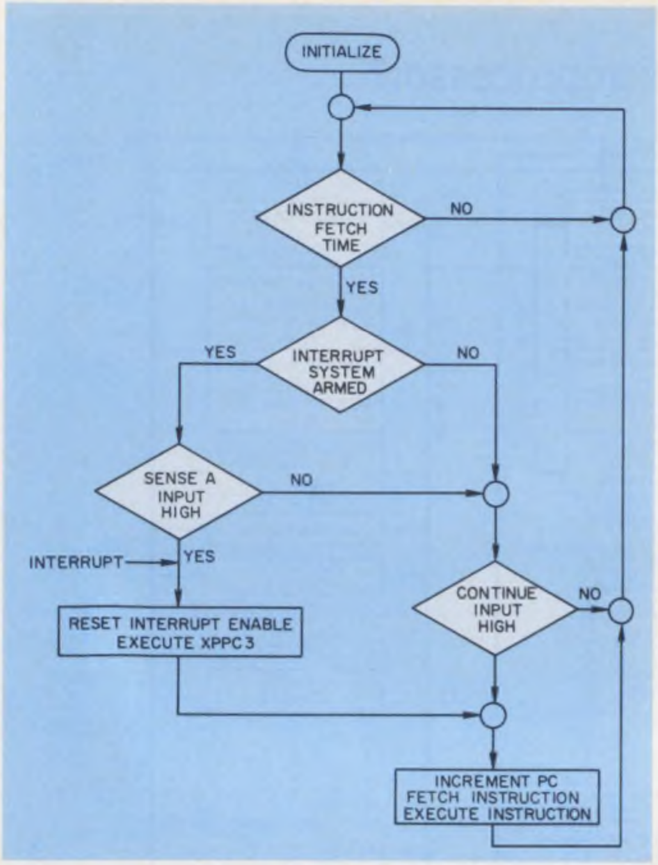
1. As an 8-bit extension of the accumulator and to store a computation's partial result.
2. To hold an address displacement value if the second byte of a memory-reference instruction is equal to $-128_{10}$. (This feature applies to PC-relative, indexed and auto-indexed addressing modes described in the box discussion on software, p. 64.)
3. As a serial input/output port under software control.

The last major register is the SR, whose eight bits are used for various indicator and sensing functions. Bits 0, 1 and 2 are software controllable flag bits (F0, F1 and F2). The next bit, bit 3 (interrupt enable), can also be set or reset under software control. When set, the $\mu$P will recognize an interrupt request on the sense-A input line (interrupt input).

Both the sense-A and sense-B bits (bits 4 and 5) are inputs and can be tested by copying the SR into the AC. When the interrupt-enable bit is set and sense A goes high, an interrupt occurs. The sense-B input doesn't have the interrupt capability, but otherwise performs like the sense-A input. The sense-A and sense-B bits in the SR are read-only indicators and are not affected if the AC is copied into the SR.

Bit 6 represents an overflow and is set if an arithmetic overflow occurs during an add—ADD, ADI or ADE—or complement-and-add—CAD, CAI or CAE—instruction. It is not affected by decimal-add instructions—DAD, DAI or DAE. (For mnemonic explanations see software discussion, p. 64.)

The last bit of the SR is a carry/link bit, which gets set if a carry from the most significant bit occurs during an add, complement-and-add or decimal-add instruction. It is used in the link form with such AC shift instructions as shift right with link (SRL) and rotate right with link (RRL).




5. **Halt and interrupt requests** are processed in the SC/MP by a continually monitored loop that checks the sense-A input line for interrupt signals and the continue input line for halt signals.

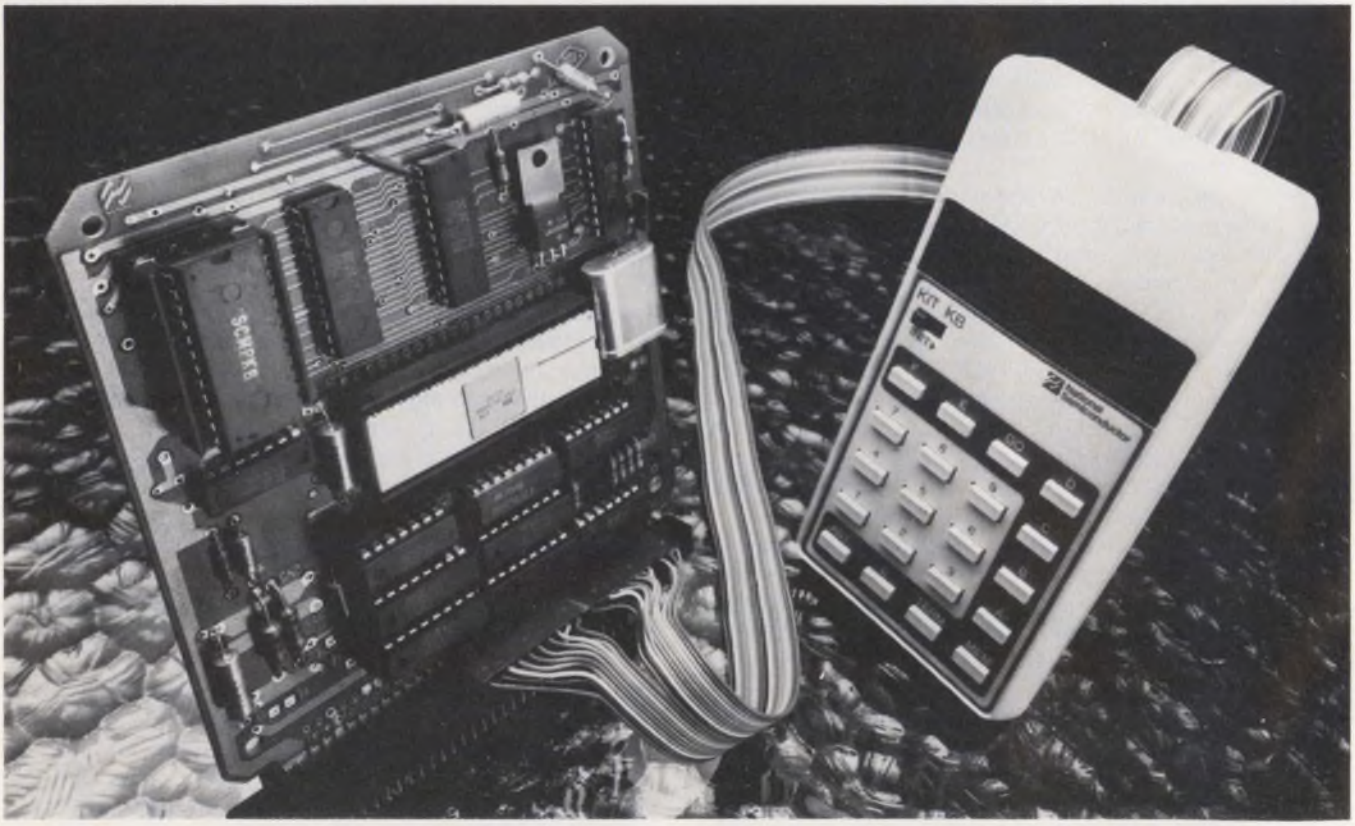
is the SC/MP kit, which is a minimal system with a teletypewriter interface.

A recently introduced portable terminal, known as the SC/MP keyboard kit, permits program entry and register and address display. The combination of the SC/MP and keyboard kits (Fig. 6) provides you with a SC/MP μP, 256 bytes of RAM, 512 bytes of preprogrammed ROM (containing Kitbug—a debug and I/O program), a teletypewriter interface, a voltage regulator, a circuit card and all required discrete components.

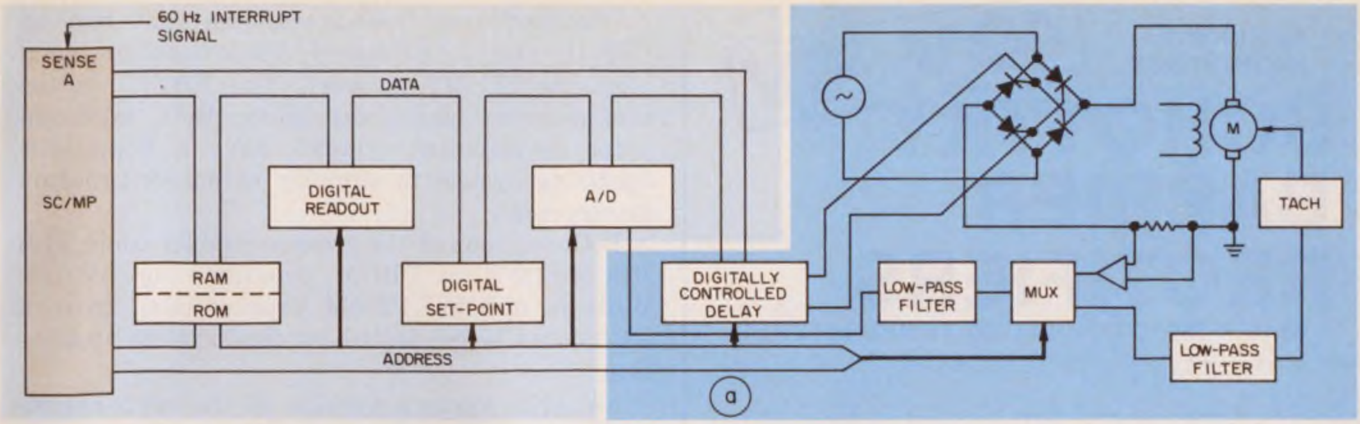
The keyboard kit, which can replace the teletypewriter, links with the SC/MP via a cable and some interface circuitry. The SC/MP kit is also available completely assembled and tested.

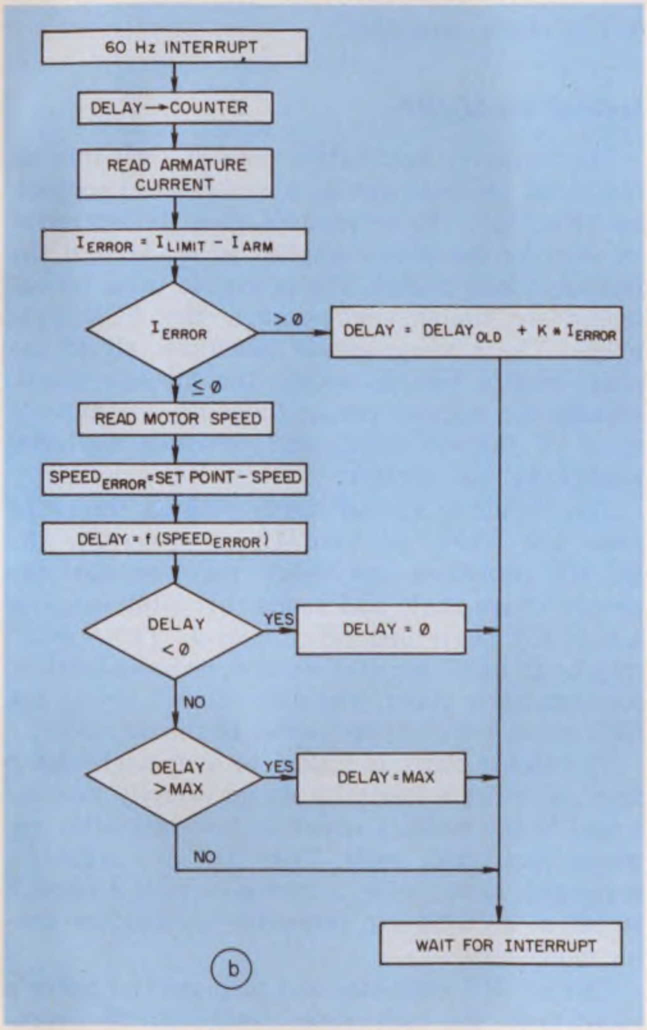
For more extensive system development there are three SC/MP application cards—CPU, RAM and ROM/PROM. The CPU card contains 256 bytes of RAM and space for 512 bytes of PROM, and can address the full 64-k of memory. The RAM card contains 2-k bytes of RAM and all necessary address decoding. The ROM/PROM card has full address decoding built in and comes unpopulated, but has space for 4-k bytes of ROM or PROM. All application cards come factory-assembled and tested.

A complete, stand-alone, low-cost development system (LCDS) can hold the application cards and give you detailed system control and software-debugging capabilities. With a 6-digit hexa-




6. **The SC/MP kit and keyboard kit combine** to make a low-cost minimal operating system. All that's needed for operation is a power supply. The keyboard's built-in display shows addresses and data.




7. **A typical industrial application** may use the SC/MP to control the speed of a dc motor (a). The controller senses the motor speed via a tachometer and feeds it to the SC/MP through an a/d converter. The SC/MP in turn sends back a digital control to the SCR bridge. The entire process, outlined in flow-chart form, shows one possible approach to the control (b).

## Table 2. SC/MP system support

| Product | Description | Price (1-24) |
|---|---|---|
| SC/MP kits and development systems | | |
| ISP-8K/200 | SC/MP kit | $ 99 |
| ISP-8K/220 | SC/MP kit assembled | 125 |
| ISP-8P/301 | SC/MP low cost development system (LCDS) | 499 |
| ISP-8K/400 | SC/MP kit keyboard | 95 |
| SC/MP application cards | | |
| ISP-8C/002 | SC/MP RAM card (2-k × 8) | 160 |
| ISP-8C/004 | SC/MP ROM/PROM card (4-k × 8), with sockets for eight MM5204/MM5214 | 125 |
| ISP-8C/100 | SC/MP CPU card (includes 256 × 8 RAM and sockets for 512 × 8 of ROM/PROM) | 250 |
| SC/MP cross assembler software packages | | |
| ISP-8S/100C,Q | SC/MP (IMP-16 based) 4-k cross assembler (object paper tapes/punched cards, and listing) | 150 |
| ISP-8S/101C,Q | SC/MP (IMP-16 based) 8-k cross assembler (object paper tapes/punched cards, and listing) | 150 |
| ISP-8S/103C | SC/MP (Pace based) cross assembler | 150 |
| ISP-8S/102P | SC/MP (ANS Fortran) cross assembler | 495 |
| NIBL | National Industrial Basic | 25 |

decimal display and a control keyboard, you can display and alter the contents of the SC/MP's program counter, register and accumulator, as well as any memory location. You can also initiate program execution at any memory address, set software breakpoints, load IMP-16 or Fortran cross-assembler-generated paper tapes, and dump programs onto the paper tapes.

LCDS I/O is switch-selectable between the front-panel keyboard and a user-supplied teletypewriter. Although all features on the LCDS are available through the TTY, the TTY's paper-tape reader and punch are needed to do cross-assembler memory loads and dumps.

Software available for the SC/MP includes a high-level interpretive language written especially for the industrial user, National Industrial Basic Language (NIBL), which requires no intermediate files or paper tapes. NIBL fits into 4-k of ROM and uses 2-k of RAM for program and variable storage.

Conversational cross-assemblers that run on IMP-16 and PACE-based minicomputers complete the SC/MP support. The PACE version also provides macro capability. Both minicomputer development systems have a floppy-disc operating system to simplify extensive program development.

Both versions of the cross-assembler come with PROM-SOFT, a PROM programming routine. With an optional PROM programming card, a PROM can be generated for final system application.

An ANS Fortran version of the cross-assembler, on GE Timeshare and National CSS networks, is also available.

### Applying the SC/MP

The following application puts SC/MP into an industrial environment as a motor-speed controller (Fig. 7a). The dc motor's speed is controlled by varying the power applied to it through the full-wave SCR bridge. The power, in turn, is controlled by timing, or phasing, the SCR gate pulses. The microprocessor generates all of the phase-control timing, senses the motor's speed, adjusts the applied power to bring the motor's speed to the set point, and provides a digital readout to the operator.

The circuit operation starts with an interrupt from the 60-Hz ac line. Upon interrupt, the SC/MP computes the delay required for the proper phase angle and sends this 8-bit value to a digitally controlled delay circuit. This circuit may be an oscillator and counter, or some form of programmable timer. The delay circuit drives the SCR gates, which apply power to the dc motor.

The motor shaft is linked to a dc tachometer that generates a feedback signal directly proportional to the motor's speed. A low-pass filter removes any brush noise. This feedback signal is presented, along with a motor-current feedback signal, to an 8-bit a/d converter through an analog multiplexer.

The SC/MP computes and displays the motor's speed from the tachometer feedback, then compares the motor speed with the digital set point and corrects the phase angle accordingly. The loop starts over again. (The flow chart for the actual program is shown in Fig. 7b.)

A SC/MP subroutine can give the desired motor start-up, including corrections for back EMF. The SC/MP can drive the digital readout with a minimum of external hardware and receive digital set-point information from a keyboard or computer. Computations or conversions on the incoming data can also be done. For example, if the motor is driving a conveyor belt, the SC/MP can compute and display the speed of the belt in ft/min. ■■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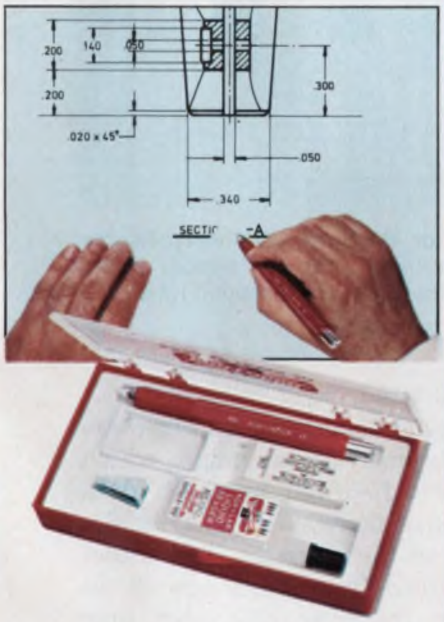


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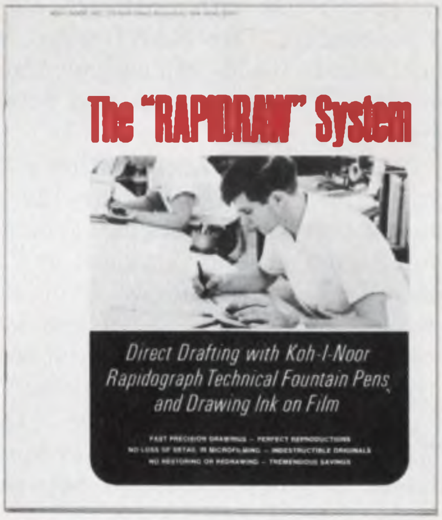


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CIRCLE NUMBER 150

# **Control an intelligent teletypewriter** with a simple $\mu$P system. Pack all control and communication functions into the system's software instead of the hardware.

Low-cost, intelligent teletypewriters that require text storage and the printing of a few hundred characters can benefit from a $\mu$P-based controller. Not only can this type of controller satisfy the requirements with minimal hardware, but it also can supervise the storage with software-based commands that are easily changed or added as required.

Just five ICs complement the controller's microprocessor. And since the $\mu$P's power isn't exhausted, it can do things that might otherwise have to be done by extra single-function chips:

- Handle serial-input and output data communication.
- Recognize and execute typed commands.
- Control text storage in the controller's RAMs.

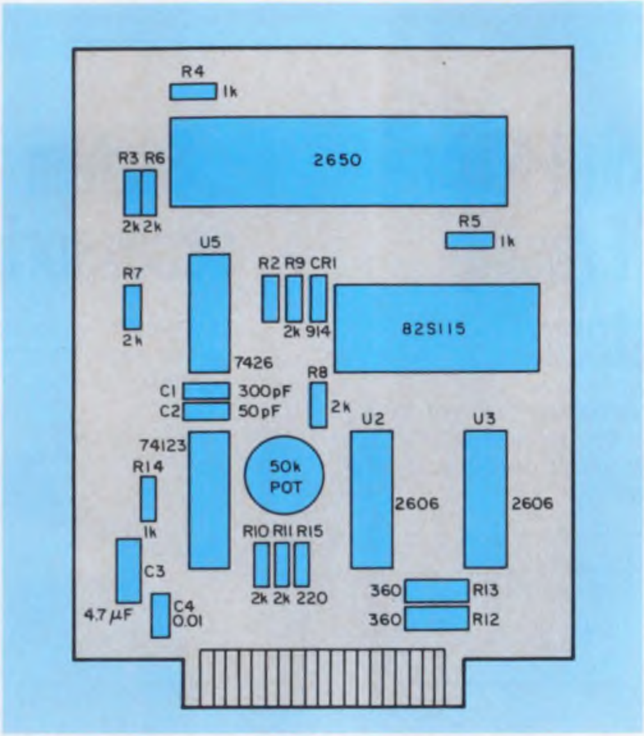
### The system uses only six chips

The intelligent-teletypewriter controller (ITC) uses the Signetics 2650 $\mu$P (Figs. 1 and 2). Two static RAMs can hold up to 250 typed characters, and one PROM with a 512-byte capacity holds the $\mu$P's program. Two NAND gates, in a package of four, decode RAM-chip selects; the other two buffer the $\mu$P's serial input and output lines to the terminal.

The ITC connects with either a 20-mA current-loop or lines capable of swinging ±7.5 V around the teletypewriter's signal ground ($V_s$ Out−). That signal ground is biased at 7.5 V above the controller's power-supply ground so that the driver's high state (15 V) and low state (0 V) look like ±7.5 V to the external receiver.

Since the current-loop is usually noisy because of mechanical-relay switching in the terminal, the TTY-In line is pulled below ground by a voltage-divider network connected between −15 V and +5 V.

A dual one-shot chip generates the system clock. The 1-MHz clock signal drives the $\mu$P and controls the serial baud rate. Changing a one-shot timing resistor varies the character-transmission rates from 110 to 300 baud.

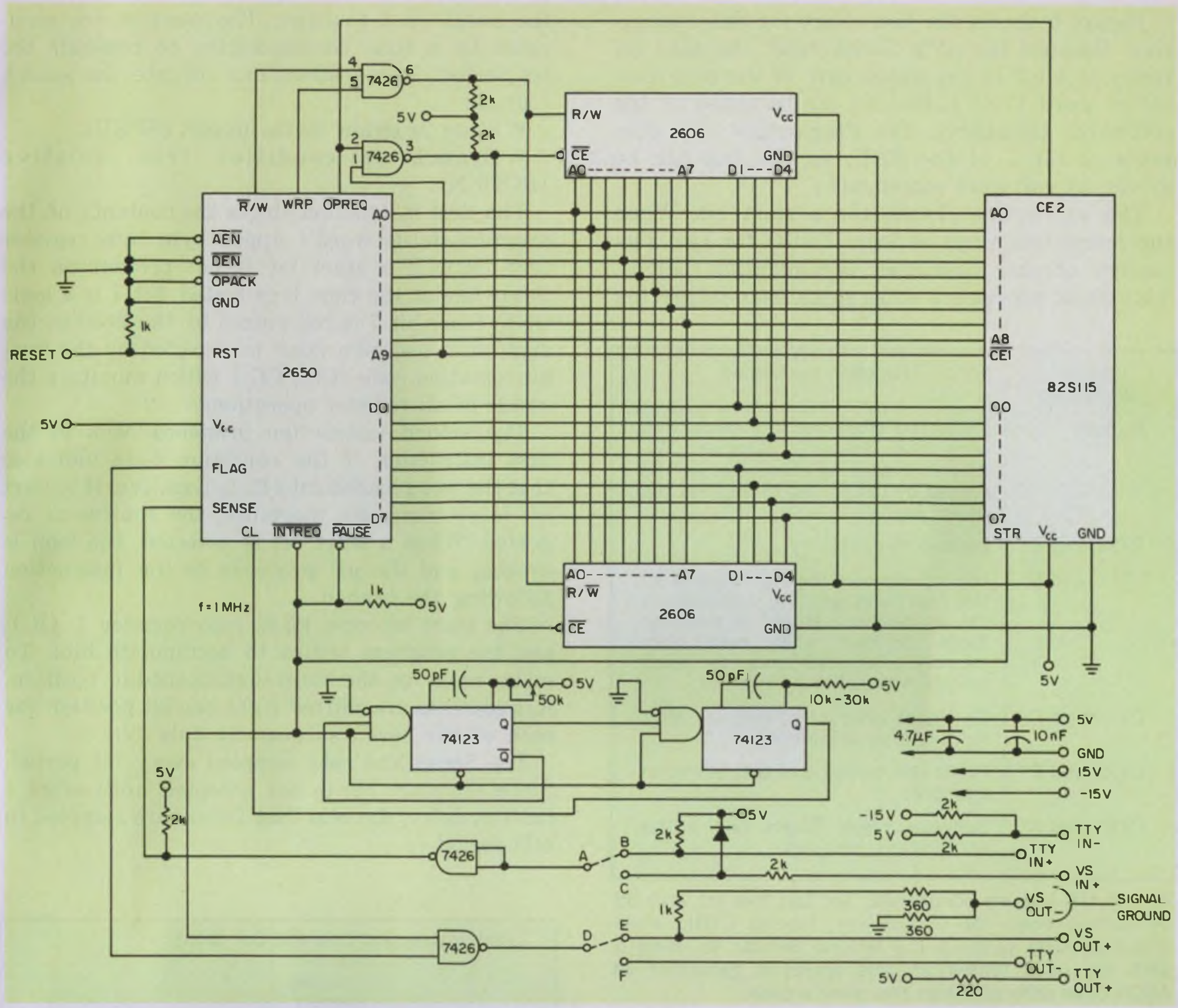



**1. The PC-board layout of the intelligent-teletypewriter controller** includes a pot that varies the system clock, which indirectly changes the serial transmission rate.

Input and output serial-asynchronous lines carry the standard teletypewriter language, which begins with a start bit followed by seven data bits, and ends with one or more stop bits (Fig. 3). The $\mu$P synchronizes on the start bit. The subsequent bits are assembled into characters in an internal register. An incoming character may command the ITC to perform an operation, or it may be a data character that must be stored in memory. The six commands that control ITC responses are listed in Fig. 4.

The ITC program (Fig. 5) is designed with structured programming techniques that require self-contained subroutine modules to be written for each function. The Out subroutine, for example, formats the bits that go to the terminal. Each subroutine is called by the main program, which functions as a central switching center.

**Roy Blacksher,** Applications Manager, Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086.



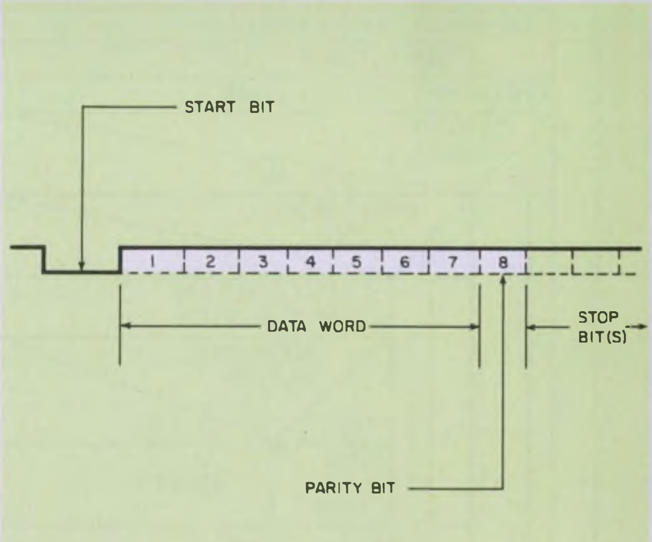

2. **The controller schematic** shows the $\mu$P, with PROM, RAM and support circuits. Standard 74-series TTL gates drive and receive the serial lines.

Adding or changing modules requires very little modification of the main program. If more teletypewriter commands are needed they can be programmed into additional PROMs. For example, a command may be added to delete a line and push the remaining lines together.

At power up, the main program branches to an initialization routine that performs necessary housekeeping tasks. Then control returns to the main program, and the ITC enters a "do forever" loop that includes several subroutines.

### The In subroutine takes the serial data

The subroutine, called In, loads a character into one of the $\mu$P's registers. When the character is accepted, the program executes the appropriate operation, then returns to the start-bit search routine.




3. **The serial-data format** between controller and teletypewriter is standard. Communication starts when the start bit, always a logic ZERO, is received.

Figure 6 shows the flow chart for this subroutine. Because the $\mu$P's Sense-input line goes directly to bit 7 in the upper byte of the program-status word (PSU), this bit can be tested by the software. (Similarly, the Flag-output line connects to bit 6 of the PSU, so the flag can be driven by software commands.)

The subroutine checks for a start bit. When the Sense line stays at logic ZERO for two successive checks, character accumulation begins. This check prevents a noise spike from triggering the serial-input routines. The samples are separated by a time corresponding to one-half the bit period. Two instructions initiate the search routine:

- Store program status upper (SPSU).
- Branch on condition true, relative (BCTR,N).

The first instruction stores the contents of the program-status word's upper byte into register zero ($R_0$). If a start bit is not present on the Sense line at the time it is tested, bit 7 is a logic ONE. Since bit 7 is recognized by the 2650 as the sign bit, a negative value is reflected by the two-bit condition code ($CC_0$, $CC_1$) which monitors the status of all register operations.

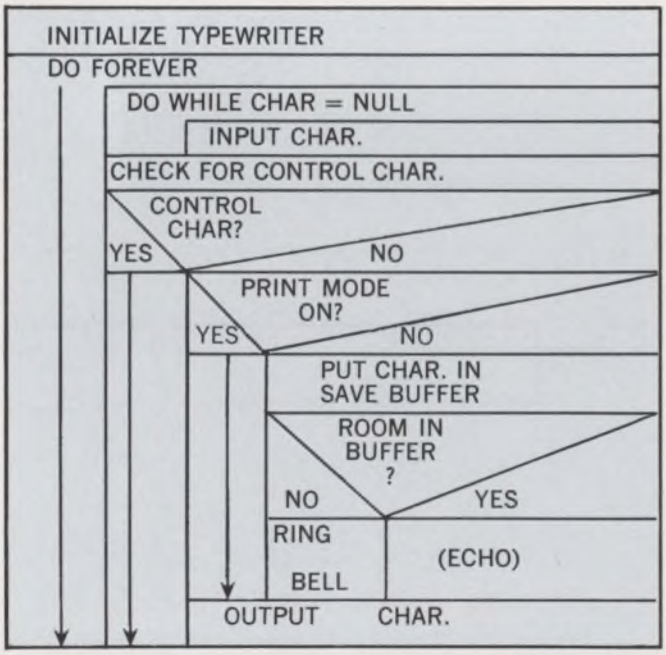
The second instruction branches back to the first instruction if the condition code indicates that the word loaded into $R_0$ is negative. If a start bit is not detected, therefore, the routine is repeated. When a start bit *is* detected, the loop is broken, and the $\mu$P proceeds to the instruction following the branch.

The start bit now loads into register 1 ($R_1$), and the program begins to accumulate bits. To make room in the most-significant-bit position, $R_1$'s contents are shifted right one bit position for each of the seven subsequent data bits.

The Sense line gets sampled every bit period. Since the start bit is not accepted until after a half-bit delay, the bits that follow are sampled in mid-period.

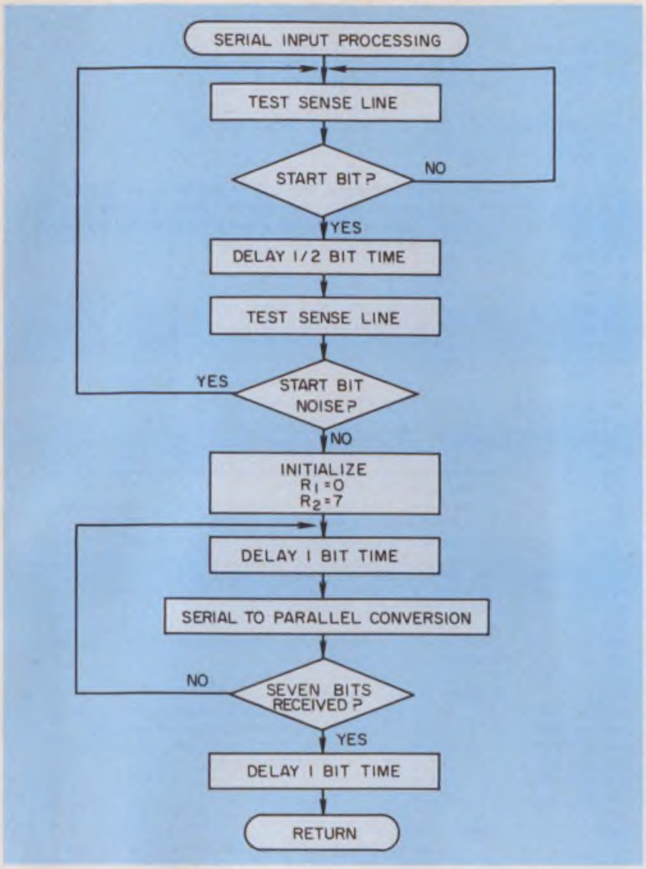
| Keys depressed | Function performed |
|---|---|
| Rubout | Erase last character in memory and echo the erased character. Additional preceding characters can be erased by continuing to depress the delete key. |
| CTRL and E | Erase entire memory. |
| CTRL and B | Used to indicate the beginning of an inserted message. The command is not printed, but stored in memory. Stops printout when read from memory. Required once for each unique information entry point. |
| CTRL and C | Continues printout of memory after entry of unique information. |
| CTRL and P | Prints out contents of text stored in memory. |
| CTRL and R | Software reset. Clears text buffer and restarts program. |

4. **The ITC has six commands.** The last five are entered by holding down the control key, labeled CTRL, while simultaneously pushing the letters. Similar to using a shift key on a typewriter, this operation generates an ASCII code different from the letter's code.




| Label | Instruction | Operand (subroutine name) | Comments |
|---|---|---|---|
| MAIN | BSTA, UN | INIT | Unconditional branch to initialize subroutine. |
| LOOP | BSTA, UN | IN | Unconditional branch to input char: subroutine (put char in $R_1$). |
| | COMI, $R_1$ | NULL | Compare $R_1$ with ASCII for null (00). |
| | BCTR, EQ | LOOP | If a null. Go back and look again. |
| | BSTA, UN | CNTL | If not a null check for control char. |
| | BCTR, Z | LOOP | If a control char. go back and get next char. |
| | LODA, RO | PMOD | If not a control char check to see if print mode. |
| | BCTR, N | LOP1 | If print mode set don't save char, just echo. |
| | BSTA, UN | SAVE | If not set, save in buffer. |
| | BCFR, Z | LOOP | If no room in buffer go back to find next char. |
| LOP1 | BSTA, UN | OUT | Print out char either saved or printed. |
| | BCTR, UN | LOOP | Go back and find next char. |

5. **The structured flow chart of the main program** (left) and instructions (right) shows the order in which the subroutines are called.




6. **The flow chart for the subroutine In** shows how serial data are entered into $R_1$. Register 2 serves as a seven-bit counter, allowing only the seven data bits to fill up $R_1$.

Register 2 ($R_2$) is initially loaded with a binary 7. For each bit transferred, $R_2$ counts down. When all seven bits are accumulated ($R_2 = 0$), control returns to the main program.

Now the main program must decide what to do with the character. So the program branches to subroutines that compare the contents of $R_1$ against a list of possible character types. Subroutine Null determines if the character has the ASCII code, 00 (hex). If it does, the program ignores the character and looks again.

Other subroutines match $R_1$'s contents against a known list of control characters. An identified control function is serviced by its subroutine.

If the character isn't a control or null, then it must be a data character. The program then proceeds to store it in RAM. The main program gets a pointer that indicates the first RAM location available for storing the data. That pointer is first compared with a RAM location containing the number of available buffer locations. If that number isn't 0—the buffer isn't full—the character is stored in RAM. The pointer is incremented, and the buffer-number indicating buffer size is decremented. A final instruction sets a condition code that indicates if the memory has room for more characters.

If the buffer is already full, the program branches to a subroutine that directs a bell on the terminal to ring. The bell also rings if the operator requests printing when there are no stored characters, or if he wants to delete more characters than are stored.

When a print command from the teletypewriter sets a print-mode flag, all characters in the ITC's memory are printed until a stop command is received. The print flag is reset at the end of the routine that transfers characters from the save buffer to an output-holding register.

The character-output subroutine called (Out) is similar to the In subroutine, except that it is reverse order. The eight bits of data in the output register go through the $\mu$P's Flag line to the serial-output line.

Before starting an output routine, the program first ensures that two stop bits have been sent after the last output subroutine. This delay gives the terminal time to complete such mechanical functions as moving a hammer to the print head.

A start bit is first sent out by clearing the flag bit in the PSU. The flag output now stays low for one bit period. The first bit of the ASCII character is then shifted to the MSB of $R_1$. If it is a logic ZERO, the flag line stays low. If it is a logic ONE, the flag is set high, and a one-bit delay is performed before transferring the next bit. When all seven bits are output, the main program again takes control. ■■

## Table 1. Program listing for the intelligent teletypewriter controller

```
TWIN ASSEMBLER VER 2.0      ITS06 - 2650 INTELLIGENT TYPEWRIT PAGE 0001

LINE ADDR  OBJECT  E SOURCE

0002                 ****************************************************************
0003                 * INTELLIGENT TYPEWRITER SYSTEM - MODEL C - VERSION 6
0004                 ****************************************************************
0005                 * PROCESSOR SYMBOLS
0006 0000            R0     EQU     0        PROCESSOR REGISTERS
0007 0001            R1     EQU     1
0008 0002            R2     EQU     2
0009 0003            R3     EQU     3
0010 0080            SENS   EQU     H'80'    PSU - SENSE
0011 0040            FLAG   EQU     H'40'    PSU -  FLAG
0012 0020            II     EQU     H'20'    PSU - INTERRUPT INHIBIT
0013 0007            SP     EQU     H'07'    PSU - STACK POINTER
0014 00C0            CC     EQU     H'C0'    PSL - CONDITION CODE
0015 0020            IDC    EQU     H'20'    PSL - INTERDIGIT CARRY
0016 0010            RS     EQU     H'10'    PSL - REGISTER BANK SELECT
0017 0008            WC     EQU     H'08'    PSL - 1=WITH CARRY, 0=WITHOUT
0018 0004            OVF    EQU     H'04'    PSL - OVERFLOW
0019 0002            COM    EQU     H'02'    PSL - 1=LOGICAL COMPARE, 0=ARITHMETIC COMP
0020 0001            C      EQU     H'01'    PSL - CARRY/BORROW
0021 0000            Z      EQU     0        BRANCH CONDITIONS - ZERO
0022 0001            P      EQU     1                            POSITIVE
0023 0002            N      EQU     2                            NEGATIVE
0024 0000            EQ     EQU     0                            EQUAL
0025 0001            GT     EQU     1                            GREATER THAN
0026 0002            LT     EQU     2                            LESS THAN
0027 0003            UN     EQU     3                            UNCONDITIONAL
0028                 *
0029                 * I/O SYMBOLS
0030 0000            NULL   EQU     H'00'
0031 000D            CR     EQU     H'0D'    CARRIAGE RETURN
0032 000A            LF     EQU     H'0A'    LINE FEED
0033 0020            SPAC   EQU     H'20'    SPACE KEY
0034 007F            DELE   EQU     H'7F'     DELETE KEY
```

(continued on page 78)

```
0035 0003           CTLC   EQU      H'03'       CONTROL+C KEYS
0036 0005           CTLE   EQU      H'05'       CONTROL+E KEYS
0037 0010           CTLP   EQU      H'10'       CONTROL+P KEYS
0038 0012           CTLR   EQU      H'12'       CONTROL+R KEYS
0039 0013           CTLS   EQU      H'13'       CONTROL+S KEYS
0040 0007           BELL   EQU      H'07'       OUTPUT CHAR TO RING BELL
0041 0008           CRLN   EQU      8           KBD/PTR  CHARACTER LENGTH INCL PARITY BI  T
0042                *
0043                *
0044                ***********************************************************************
0045 0000                  ORG      H'700'      RAM PORTION OF PROGRAM
0046                *                           VARIABLE STORAGE IS DEFINED AT LOC H'700'
0047                *                           FOR PROTOTYPING SYSTEM CHECKOUT ONLY  ITS
0048                *                           PERMANENT ADDRESS WILL BE H'200'
0049                * VARIABLE STORAGE
0050 0700           VSTR   EQU      $           START OF VARIABLE STORAGE
0051                * GLOBAL VARIABLE
0052 0700           PMOD   RES      1           PRINT MODE SWITCH=0 IF OFF, =H'FF' IF ON
0053                * SAVE BUFFER MODULE VARIABLES
0054 0701           SOPT   RES      1           POINTER FOR FILLING SAVE BUFFER
0055 0702           SIPT   RES      1           POINTER FOR PRINTING SAVE BUFFER
0056 0703           SBUF   RES      250         SAVE BUFFER FOR LATER PRINTING

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0002

LINE ADDR  OBJECT  E SOURCE

0057 07FD           SEND   EQU      $           END OF SAVE BUFFER
0058 07FD           VEND   EQU      $           END OF VARIABLE STORAGE AREA

TWIN ASSEMBLER VER 2.0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0003

LINE ADDR  OBJECT  E SOURCE

0060 07FD                  ORG      0           PROM/ROM PORTION OF PROGRAM
0061                *
0062 0000 1F0003    RSET   BCTA,UN  MAIN        RESET ENTRANCE - MAIN PROGRAM
0063                *
0064                ***********************************************************************
0065                * MAIN PROGRAM - INTELLIGENT TYPEWRITER SYSTEM
0066                *
0067 0003 3F0021    MAIN   BSTA,UN  INIT        INITIALIZE TYPEWRITER
0068 0006 3F0039    LOOP   BSTA,UN  IN          GET INPUT CHAR INTO R1
0069 0009 E500             COMI,R1  NULL        IF ITS A NULL
0070 000B 1879             BCTR,EQ  LOOP        THEN GET NEXT CHARACTER
0071 000D 3F0097           BSTA,UN  CNTL        IF CONTROL FUNCTION - EXECUTE  FCN
0072 0010 1874             BCTR,Z   LOOP             AND GET NEXT CHARACTER
0073 0012 0C0700           LODA,R0  PMOD        IF PRINT MODE ON
0074 0015 1A05             BCTR,N   LOP1        THEN DONT SAVE CHAR - ECHO CHAR ONLY
0075 0017 3F00C9           BSTA,UN  SAVE        ELSE PLACE CHAR IN SAVE BUF IF ROOM
0076 001A 986A             BCFR,Z   LOOP        IF NO ROOM, DONT ECHO CHAR
0077 001C 3F0069    LOP1   BSTA,UN  OUT         ELSE ECHO LITERAL CHARACTER
0078 001F 1B65             BCTR,UN  LOOP             AND GET NEXT CHARACTER
0079                *
0080                ***********************************************************************
0081                * INITIALIZE SYSTEM
0082 0021 7620      INIT   PPSU     II          INHIBIT INTERRUPTS
0083 0023 7518             CPSL     WC+RS       SELECT BNK0 REGS + ARITH/ROTATE W/O CARRY
0084 0025 7702             PPSL     COM         SELECT LOGICAL COMPARE
0085 0027 07FD             LODI,R3  VEND-VSTR   R3=LENGTH OF VARIABLE STORAGE
0086 0029 20               EORZ     R0
0087 002A CF4700    INI1   STRA,R0  VSTR,R3,-   ZERO VARIABLE STORAGE AREA
0088 002D 5B7B             BRNR,R3  INI1
0089 002F 3F0036           BSTA,UN  ITIN        INITIALIZE INPUT DEVICES
0090 0032 3F0066           BSTA,UN  ITOT        INITIALIZE OUTPUT DEVICES
0091 0035 17               RETC,UN              EXIT
0092                * END OF INITIALIZATION MODULE

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0004

LINE ADDR  OBJECT  E SOURCE

0094                ***********************************************************************
0095                * INPUT CONTROL MODULE
0096                *     THE FOLLOWING SUBROUTINES WOULD NORMALLY SWITCH INPUT CONTROL
0097                *     BETWEEN THE VARIOUS INPUT DEVICES  SINCE THERE IS ONLY ONE INPUT
0098                *     DEVICE THESE ROUTINES ARE EQUATED DIRECTLY TO THE KEYBOARD ROUTINE
0099                *
0100 0036 1F003C    ITIN   BCTA,UN  ITKY        ROUTINE TO INITIALIZE THE INPUT DEVICE
0101 0039 1F003D    IN     BCTA,UN  KYIN        ROUTINE TO GET AN INPUT CHARACTER
0102                * END OF INPUT CONTROL MODULE
0103                *
0104                ***********************************************************************
0105                * KEYBOARD PROCESSING MODULE
0106                *
0107                * NO KEYBOARD INITIALIZATION NECESSARY
0108 003C 17        ITKY   RETC,UN
0109                *
0110                * GET A KEYBOARD CHARACTER
0111                *
0112                *     THIS ROUTINE SERIALLY INPUTS A CHARACTER FROM THE KBD THRU THE
0113                *     SENSE BIT  THE ROUTINE DOES NOT INPUT THE PARITY BIT
0114 003D 0500      KYIN   LODI,R1  0           R1 WILL HOLD CHAR ON EXIT
0115 003F 0607             LODI,R2  CRLN-1      R2=CHARACTER LENGTH-PARITY BIT
0116 0041 12        KYI1   SPSU                 GET SENSE BIT (BIT 7)
0117 0042 1A7D             BCTR,N   KYI1        IF NOT A START BIT-LOOP UNTIL IT COMES
0118 0044 20               EORZ     R0          DELAY 1/2 BIT TIME TO MIDDLE OF START BIT
0119 0045 3F005F           BSTA,UN  DHAF
0120 0048 12               SPSU                 IF NOT STILL A START BIT
0121 0049 1A76             BCTR,N   KYI1        THEN IT WAS NOISE SO KEEP LOOKING
0122 004B 3F005A    KYI2   BSTA,UN  DLAY        DELAY 1 BIT TIME TO MIDDLE OF NEXT BIT
0123 004E 12               SPSU                 GET SENSE BIT
0124 004F 4480             ANDI,R0  SENS
0125 0051 61               IORZ     R1               AND SHIFT IT INTO R1
0126 0052 C1               STRZ     R1
0127 0053 51               RRR,R1
0128 0054 FA75             BDRR,R2  KYI2        IF ALL BITS ARENT IN-CONTINUE AT KYI2
0129 0056 3F005A           BSTA,UN  DLAY        DELAY 1+1/2 BIT TIMES TO END OF PARITY BIT
0130 0059 17               RETC,UN
0131                * END OF KEYBOARD PROCESSING MODULE

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0005

LINE ADDR  OBJECT  E SOURCE

0133                * DELAY ROUTINE - TO PROVIDE TIMING FOR 110 BAUD SERIAL INPUT/OUTPUT
0134                *     BASED ON A 1MHZ INPUT CLOCK.  ENTRY AT DLAY PROVIDES A ONE BIT
0135                *     DELAY:  ENTRY AT DHAF PROVIDES A HALF BIT DELAY AND REQUIRES THAT
0136                *     R0 BE PREVIOUSLY SET TO 0
0137 005A 20        DLAY   EORZ     R0
0138 005B F87E             BDRR,R0  $
0139 005D F87E             BDRR,R0  $
0140 005F F87E      DHAF   BDRR,R0  $
0141 0061 04E5             LODI,R0  H'E5'
0142 0063 F87E             BDRR,R0  $
0143 0065 17               RETC,UN

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0006

LINE ADDR  OBJECT  E SOURCE

0145                ***********************************************************************
0146                * OUTPUT CONTROL MODULE
0147                * THESE ROUTINES WOULD NORMALLY SWITCH OUTPUT CONTROL BETWEEN THE VARIOU
0148                *     OUTPUT DEVICES  SINCE THERE IS ONLY ONE OUTPUT DEVICE THESE
0149                *     ROUTINES ARE EQUATED DIRECTLY TO THE PRINTER ROUTINES
0150                *
0151 0066 1F006C    ITOT   BCTA,UN  ITPR        INITIALIZE OUTPUT DEVICE
0152 0069 1F0079    OUT    BCTA,UN  POUT        WRITE A CHARACTER TO OUTPUT DEVICE
0153                * END OF OUTPUT CONTROL MODULE
0154                *
0155                ***********************************************************************
0156                * PRINTER PROCESSING MODULE
0157                *
0158                * PRINTER INITIALIZATION ROUTINE
0159 006C 7640      ITPR   PPSU     FLAG         ASSURE STOP BITS ARE BEING SENT TO PRINTR
0160 006E 050D             LODI,R1  CR          OUTPUT CARRIAGE RETURN AND LINE FEED
0161 0070 3F0079           BSTA,UN  POUT        CALL POUT DIRECTLY SINCE THIS IS PRINTER
0162 0073 050A             LODI,R1  LF             PECULIAR INITIALIZATION
0163 0075 3F0079           BSTA,UN  POUT
0164 0078 17               RETC,UN              EXIT
0165                *
0166                * PRINTER OUTPUT ROUTINE
0167                *     THIS ROUTINE SERIALLY OUTPUTS THE CHARACTER IN R1 THRU THE FLAG
0168                *     BIT TO THE PRINTER
0169 0079 0608      POUT   LODI,R2  CRLN        CHARACTER LENGTH TO R2 FOR COUNTER
0170 007B 3F005A           BSTA,UN  DLAY        ASSURE 2 STOP BITS ARE OUTPUT
0171 007E 3F005A           BSTA,UN  DLAY
0172 0081 7440             CPSU     FLAG        SEND START BIT
0173 0083 3F005A    POU1   BSTA,UN  DLAY        DELAY 1 BIT TIME
0174 0086 51               RRR,R1               SHIFT NEXT BIT OUT TO MSD POSITION TO TEST
0175 0087 1A04             BCTR,N   POU2        IF ITS A 1 THEN BRANCH
0176 0089 7440             CPSU     FLAG        OUTPUT A ZERO BIT
0177 008B 1B02             BCTR,UN  POU3
0178 008D 7640      POU2   PPSU     FLAG        OUTPUT A 1 BIT
0179 008F FA72      POU3   BDRR,R2  POU1        IF ALL BITS OF R1 NOT SENT CONTINUE AT POU1
0180 0091 3F005A           BSTA,UN  DLAY        DELAY 1 BIT TIME
0181 0094 7640             PPSU     FLAG        OUTPUT STOP BIT
0182 0096 17               RETC,UN
0183                * END OF PRINTER PROCESSING MODULE
0184                *

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0007

LINE ADDR  OBJECT  E SOURCE

0186                ***********************************************************************
0187                * INPUT CHARACTER DECODE MODULE
0188                *
0189                * CONTROL FUNCTION ROUTINE - CHARACTER IS IN R1 UPON ENTRY
0190                *     IF CHARACTER NOT A CONTROL CHARACTER, RETURN CC NOT=0 ELSE CC=0
0191 0097 E57F      CNTL   COMI,R1  DELE        IF DELETE CHARACTER
0192 0099 9808             BCFR,EQ  CNT1
0193 009B 3F00F3           BSTA,UN  DCHR        THEN DELETE LAST CHAR FROM SAVE BUFFER
0194 009E 3F0069           BSTA,UN  OUT         ECHO DELETED CHAR (OR BELL IF BUF FULL)
0195 00A1 1B21             BCTR,UN  CEXI
0196 00A3 E505      CNT1   COMI,R1  CTLE        IF ERASE FUNCTION
0197 00A5 9805             BCFR,EQ  CNT2
0198 00A7 3F00E1           BSTA,UN  ERAS        THEN ERASE ENTIRE SAVE BUFFER AND RESET PTR
0199 00AA 1B18             BCTR,UN  CEXI
0200 00AC E510      CNT2   COMI,R1  CTLP        IF PRINT FUNCTION
0201 00AE 9805             BCFR,EQ  CNT3
0202 00B0 3F010A           BSTA,UN  PRNT        THEN PRINT SAVE BUFFER FROM THE TOP
0203 00B3 1B0F             BCTR,UN  CEXI
0204 00B5 E503      CNT3   COMI,R1  CTLC        IF    CONTINUE FUNCTION
0205 00B7 9805             BCFR,EQ  CNT6
0206 00B9 3F0125           BSTA,UN  CONT        THEN PRINT SAVE BUFFER FROM LAST STOP
0207 00BC 1B06             BCTR,UN  CEXI
0208 00BE E512      CNT6   COMI,R1  CTLR        IF RESET FUNCTION
0209 00C0 9804             BCFR,EQ  CNT7
0210 00C2 9B00             ZBRR     RSET        EXECUTE SOFTWARE RESET
0211 00C4 20        CEXI   EORZ     R0          SET CC=0 TO INDICATE CHAR WAS A CNTL FCN
0212 00C5 17               RETC,UN
0213 00C6 04FF      CNT7   LODI,R0  H'FF'       SET CC NOT= 0 TO INDICATE NOT A CNTL CHAR
0214 00C8 17               RETC,UN
0215                * END OF INPUT CHARACTER DECODE MODULE
0216                ***********************************************************************

TWIN ASSEMBLER VER 2 0      ITSC6 - 2650 INTELLIGENT TYPEWRIT PAGE 0008

LINE ADDR  OBJECT  E SOURCE

0218                ***********************************************************************
```

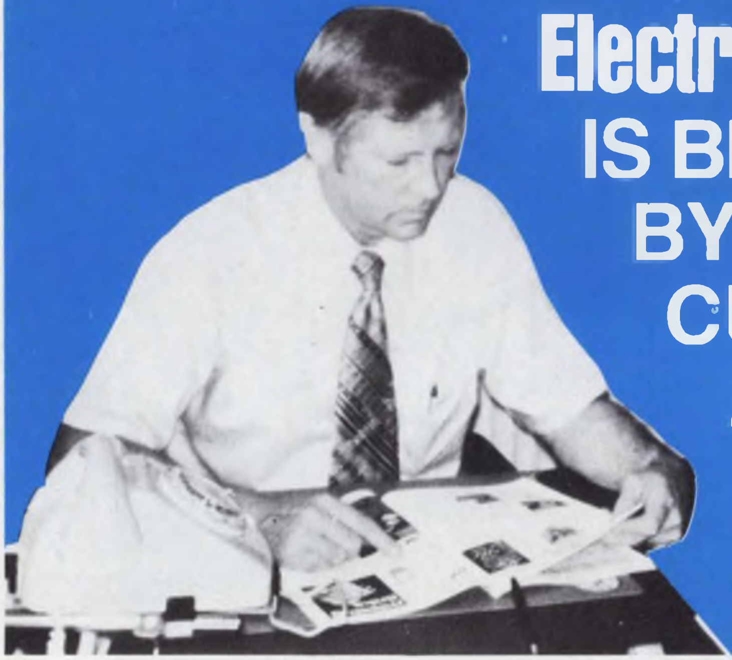
```
                   * SAVE BUFFER MODULE
                   *
                   * SAVE BUFFER ROUTINE
                   *     THIS ROUTINE SAVES LITERAL CHARACTERS AND OUTPUT CONTROL
                   *     FUNCTIONS FOR LATER PRINTING WHEN THE PRINT COMMAND IS INPUT
                   *     ON EXIT CC=0 IF ROOM FOR CHAR IN BUFFER. CC NOT=0 IF BUFF FULL
00C9 0F0701        SAVE  LODA,R3  SOPT        GET SAVE BUFFER POINTER
00CC E7FA                COMI,R3  SEND-SBUF   IF BUFFER FULL
00CE 1809                BCTR,EQ  SFUL        THEN BRANCH
00D0 01                  LODZ     R1          PLACE CHAR FROM R1 INTO SAVE BUFFER
00D1 CF2702              STRA,R0  SBUF-1,R3,+
00D4 CF0701              STRA,R3  SOPT        SAVE NEW BUFFER POINTER
00D7 20                  EORZ     R0          CC=0
00D8 17                  RETC,UN
00D9 0507          SFUL  LODI,R1  BELL        RING BELL - BUFFER IS FULL
00DB 3F0069              BSTA,UN  OUT
00DE 04FF                LODI,R0  H'FF'       CC NOT= 0 TO SHOW BUFFER FULL
00E0 17                  RETC,UN              EXIT
                   *
                   * ERASE ROUTINE
                   *     THIS ROUTINE ERASES THE ENTIRE SAVE BUFFER AND RESETS BOTH POINTER
00E1 07FA          ERAS  LODI,R3  SEND-SBUF   ZERO SAVE BUFFER
00E3 20                  EORZ     R0
00E4 CF4703        ERA1  STRA,R0  SBUF,R3,-
00E7 5B7B                BRNR,R3  ERA1
00E9 CF0702              STRA,R3  SIPT        ZERO SAVE BUFFER PRINT POINTER
00EC CF0701              STRA,R3  SOPT        ZERO SAVE BUFFER LOAD POINTER
00EF CC0700              STRA,R0  PMOD        DESELECT PRINT MODE
00F2 17                  RETC,UN
                   *
                   *DELETE CHARACTER ROUTINE
                   *     THIS ROUTINE DELETES THE LAST CHARACTER IN THE SAVE BUFFER
                   *     AND RETURNS THE CHARACTER IN R1    IF THE BUFFER IS EMPTY.
                   *     IT RETURNS WITH THE BELL CODE IN R1
00F3 0F0701        DCHR  LODA,R3  SOPT        GET BUFFER POINTER
00F6 E700                COMI,R3  0           IF BUFFER EMPTY
00F8 180D                BCTR,EQ  DCH1        THEN BRANCH
00FA 0F4703              LODA,R0  SBUF,R3,-   ELSE GET LAST CHAR AND DECREMENT POINTER
00FD C1                  STRZ     R1          CHAR TO R1
00FE 0400                LODI,R0  NULL        AND REPLACE IT WITH A NULL
0100 CF6703              STRA,R0  SBUF,R3
0103 CF0701              STRA,R3  SOPT        SAVE NEW POINTER
0106 17                  RETC,UN
0107 0507          DCH1  LODI,R1  BELL        OUTPUT BELL FOR IMPROPER REQUEST
0109 17                  RETC,UN
                   *
                   * PRINT SAVE BUFFER ROUTINE
                   *     THIS ROUTINE PRINTS THE SAVE BUFFER STARTING AT THE BEGINNING
                   *     UNTIL THE END OF DATA OR A STOP CODE IS REACHED
010A 0700          PRNT  LODI,R3  0           SET POINTER TO START OF BUFFER
010C 0F6703              LODA,R0  SBUF,R3     GET NEXT PRINT CHAR BUT DONT INCR INDEX
010F E400                COMI,R0  NULL        IF BUFFER EMPTY
0111 180C                BCTR,EQ  PEEL        THEN BRANCH
0113 04FF                LODI,R0  H'FF'       TURN ON PRINT MODE SWITCH

TWIN ASSEMBLER VER 2.0     [illegible] 2650 INTELLIGENT TYPEWRIT PAGE [illegible]

LINE ADDR  OBJECT  E SOURCE

0115 CC0700              STRA,R0  PMOD
0119 3F0142              BSTA,UN  MOVP        MOVE CHARACTERS TO OUTPUT BUFFER
011B CF0702              STRA,R3  SIPT        SAVE NEW PRINT POINTER
011E 17                  RETC,UN
011F 0507          PEEL  LODI,R1  BELL        OUTPUT BELL FOR IMPROPER REQUEST
0121 3F0069              BSTA,UN  OUT
0124 17                  RETC,UN
                   *
                   * CONTINUE PRINTING ROUTINE
                   *     THIS ROUTINE CONTINUES PRINTING THE SAVE BUFFER FROM WHERE THE
                   *     THE LAST PRINT OR CONTINUE REQUEST LEFT OFF, UNTIL THE END OF
                   *     DATA OR A STOP CODE IS REACHED
0125 0F0702        CONT  LODA,R3  SIPT        GET PRINT POINTER
0128 E700                COMI,R3  0           IF SAVE BUFFER EMPTY
012A 1810                BCTR,EQ  CREL        THEN BRANCH
012C E7FA                COMI,R3  SEND-SBUF   IF POINTER AT END OF BUFFER
012E 180C                BCTR,EQ  CBEL        THEN BRANCH
0130 0F6703              LODA,R0  SBUF,R3     GET NEXT PRINT CHAR BUT DONT INCR INDEX
0133 1807                BCTR,EQ  CBEL        IF ITS A NULL (END OF DATA) BRANCH
0135 3F0142              BSTA,UN  MOVP        MOVE CHARACTERS TO OUTPUT BUFFER
0138 CF0702              STRA,R3  SIPT        SAVE NEW PRINT POINTER
013B 17                  RETC,UN
013C 0507          CBEL  LODI,R1  BELL        OUTPUT BELL FOR IMPROPER REQUEST
013E 3F0069              BSTA,UN  OUT
0141 17                  RETC,UN
                   *
                   * MOVER ROUTINE
                   *     THIS ROUTINE TRANSFERS CHARACTERS FROM THE SAVE BUFFER TO THE
                   *     OUTPUT BUFFER   IT EXPECTS R3 TO BE SET UP AS THE STARTING INDEX
                   *     TO THE SAVE BUFFER  TRANSFERS WILL STOP WHEN A STOP CODE OR THE
                   *     END OF DATA IS REACHED
0142 E7FA          MOVP  COMI,R3  SEND-SBUF   IF END OF BUFFER REACHED
0144 1812                BCTR,EQ  MOV2        THEN EXIT
0146 0F2702              LODA,R0  SBUF-1,R3,+ GET NEXT CHAR FROM SAVE BUFFER
0149 E400                COMI,R0  NULL        IF END OF DATA REACHED
014B 1809                BCTR,EQ  MOV1        THEN EXIT
014D E413                COMI,R0  CTLS        IF STOP CODE IN BUFFER
014F 14                  RETC,EQ              THEN EXIT
0150 C1                  STRZ     R1          CHAR TO R1
0151 3F0069              BSTA,UN  OUT         AND OUTPUT IT
0154 1B6C                BCTR,UN  MOVP        CONTINUE MOVES
0156 A701          MOV1  SUBI,R3  1           MOVE INDEX BACK TO NULL CHARACTER
0158 20            MOV2  EORZ     R0          TURN OFF PRINT MODE
0159 CC0700              STRA,R0  PMOD
015C 17                  RETC,UN
                   *
                   * END SAVE BUFFER MODULE
                   ********************************************************************
0003                     END      MAIN
                   TOTAL ASSEMBLY ERRORS = 0000
```

# ITT CANNON FOUND OUT...



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# Marry your $\mu$P to monolithic a/ds.

## Size, price and power compatibility team up with simple interfaces to give you an efficient on-line system.

Interfacing microprocessors to the world of analog data requires a new approach. The hundreds of data-acquisition systems and modules that have served minicomputers well are inappropriate for micros. They're too expensive, too power-consuming or too large.

The new monolithic a/d converters stand apart with their combination of cost, efficiency and size (under $10, in hundreds, for an 8-bit, 20-mW DIP). With monolithic converters in your micro-based system, you get the size and cost that have prompted you to go to the $\mu$P in the first place.

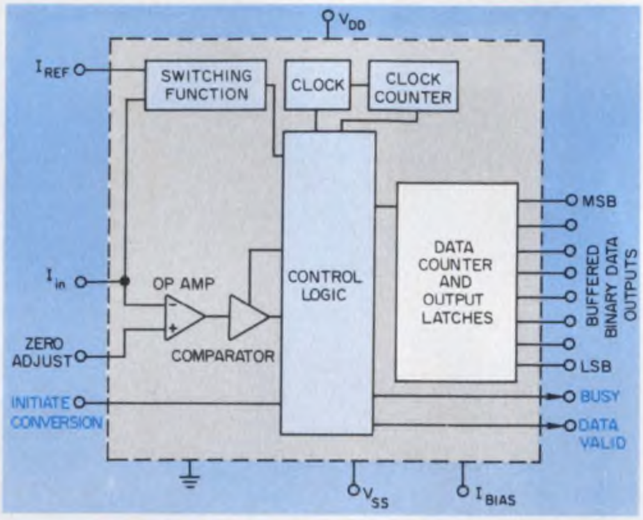
But the monolithics are slow—1.8 ms is a typical conversion speed for an 8-bit unit. So, instead of treating the a/d as a memory location as you would for $\mu$s-conversion devices,[1] interface your micro to a monolithic a/d as you would to a slow peripheral. Assign the converter an input/output (I/O) address, decode the address in the interface, and let the $\mu$P go about its other business while a conversion takes place. After the conversion, when the resulting data are in the converter's output latches, request an interrupt. When the processor is ready to service the interrupt, have it address the converter's I/O port to read the data.

For multiple-input channels, don't tolerate the errors and complexity of multiplexing into a single faster converter. Assign each one a dedicated monolithic a/d. If priorities are necessary, implement them in the software. Eliminate reading stale data with simple storage and comparison circuitry in the interface.

### The converter/$\mu$P system

Obviously, you need both circuitry and service routines to integrate monolithic converters into your $\mu$P-based system. Fortunately, the hardware is not complex, and the software is equally simple. Consider, for example, Teledyne Semiconductor's 8-bit 8700 a/d in an 8080A-based system.

**Dave Guzman,** President, lasis, 815 W. Maude Ave., Sunnyvale, CA 94086.



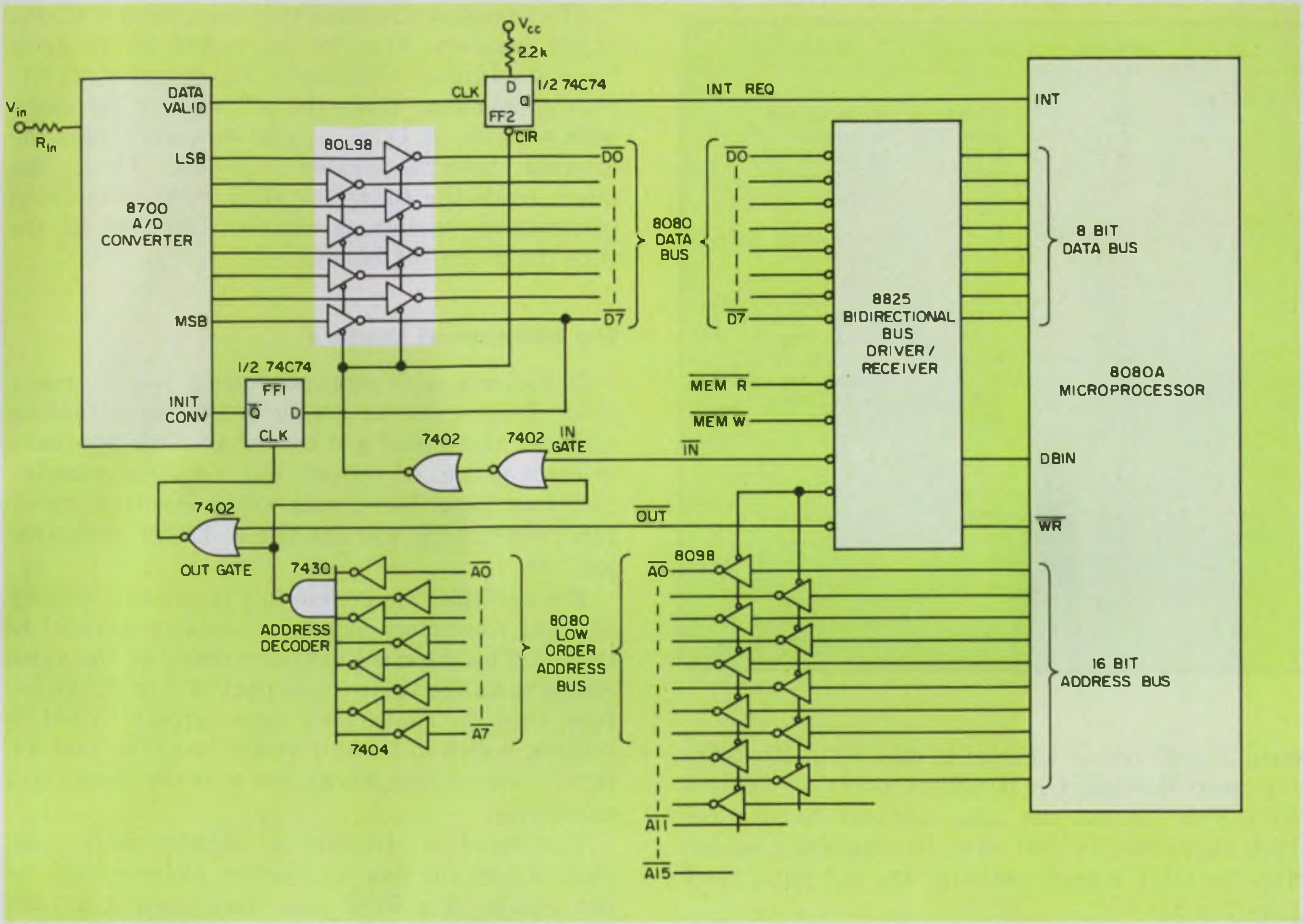

1. **Busy, Data Valid and Initiate Conversion** control signals link the 8700 a/d converter to a microprocessor. The a/d stores its binary outputs in latches.

The 8700 a/d converter is an 8-bit monolithic CMOS device. An integrating converter (Fig. 1), it accepts an unlimited voltage input, which is changed to a current input by a scaling resistor, and produces latched parallel-binary output.

In addition to the buffered data output lines, three handshaking (control) signals pass between the converter and the host $\mu$P:

- Initiate Conversion, an input to the converter that starts the conversion cycle. A positive-going pulse of at least 500-ns duration causes the conversion to begin. With this input tied high, conversions occur in a free-running mode at approximately 50 per second.
- Busy, an output that, when high, informs the $\mu$P that a conversion is in progress.
- Data Valid, an output that, when high, informs the $\mu$P that the converter's output latches contain valid data. Normally, Data Valid is high for the entire cycle except for about 5 $\mu$s before the end of the conversion, when data in the latches are updated.

Control of the a/d is simple. Pulsing Initiate Conversion starts the cycle. Data Valid and Busy give the processor the converter's status.




2. **The basic interface for a monolithic converter/$\mu$P system decodes the micro's address bus to access the a/d.** Data pass from the converter port to the processor on the data bus, which the $\mu$P services with interrupts.

The 8080A is an 8-bit $\mu$P with two internal buses.[2] One carries 16-bit memory addresses, and the other 8-bit data. During each machine cycle, the address bus transports the number in the program counter to the memory, which receives the address and returns the contents of the selected memory location via the data bus. During an instruction-fetch cycle, the returning data are interpreted as an instruction.

The $\mu$P system plugs into the outside world by means of I/O ports that are addressed on the address bus. The I/O instructions use 8-bit addresses, which are duplicated on both the low and high-order address lines of the 16-bit address bus.

With a set of control signals, the $\mu$P also communicates with its memory and I/O ports. Two control lines, $\overline{\text{DBIN}}$ and $\overline{\text{WR}}$, enable the I/O ports. A ZERO on $\overline{\text{DBIN}}$ enables the addressed port to input to the $\mu$P. $\overline{\text{WR}}$ functions similarly for outputs from the microprocessor.

### The basic interface

Conversion starts on command from the $\mu$P to the Initiate Conversion input of the converter. The interface logic for a single-channel data-acquisition system is shown in Fig. 2.

When the conversion is complete, the converter requests an interrupt via its Data Valid output. In the $\mu$P, an interrupt service routine transfers the current data from the working registers to the stack memory, and the a/d input port is read. A control signal is then sent to the Initiate Conversion input to restart the conversion, and the main-program activity is resumed.

If the data bus is shared by many devices, include inverting drivers/receivers (such as the 8228) in the 8080A system to service this bus. Use 80L98 buffers at the a/d to drive an inverted input over the data bus, and provide the three-state function. Where inverted signals are not needed, use the version of the 8700 that has three-state outputs.

For selection, assign each port an address and decode the address bus accordingly. For the input port (Fig. 2) to the $\mu$P, the 80L98s are enabled by the low output of the address decoder. This output is low only when all the decoder's inputs are high, as a result of address $FF_H$.

To initiate a conversion in the a/d, employ the

## Table 1. Interrupt service routine

| Label | Mnemonic | Operand | Explanation |
|---|---|---|---|
| Initiation | | | |
| | MVI | A, 80H | The conversion |
| | OUT | 0FFH | is initiated |
| | MVI | A, 0 | by sending a |
| | OUT | 0FFH | brief pulse |
| | | | to port FF |
| Interrupt | | | |
| | PUSH | B | The processor |
| | PUSH | D | registers and |
| | PUSH | H | status are saved |
| | PUSH | PSW | in the stack, and the |
| | IN | 0FFH | data are read and |
| | MOV | B, A | stored in reg. B. |
| | MVI | A, 80H | The conversion is |
| | OUT | 0FFH | initiated and |
| | MVI | A, 0 | the data are |
| | OUT | 0FFH | processed. |
| | • | | |
| | • | | |
| | • | | |
| | • | | |
| | POP | PSW | When complete, |
| | POP | H | the registers |
| | POP | D | are restored, the |
| | POP | B | interrupts enabled |
| | RET | | and program |
| | | | control returned |
| | | | to the main program. |

output port whose address is also $FF_H$. By defining both the input and output ports as address $FF_H$, you can use the same address decoder for both functions. In this case, the decoder's output and the OUT signal, gated by the out gate, clock flip-flop 1.

The D input of the flip-flop is tied to the $D_7$ line of the data bus, so in effect, the flip-flop is a one-bit output port. Sending the data word, $80_H$, to port $FF_H$ with an output (OUT) instruction sets flip-flop 1, and thereby supplies an Initiate Conversion signal to the a/d. Send $00_H$ to the same port with a second output instruction. This process resets flip-flop 1 and removes the Initiate Conversion signal. After beginning the conversion, the μP is free to perform other operations.

After completing its conversion cycle, the a/d latches the results onto its internal output latches. Its Data Valid output goes high. This output triggers flip-flop 2 and clocks a ONE from the D input (tied high) onto the μP's Interrupt Request line.

Consequently, the microprocessor is interrupted when the conversion is complete. The interrupt service routine shown in Table 1 saves the CPU's working-register contents by pushing them onto the stack, and then reads the output of the a/d.

To read the converter port, simultaneously put $FF_H$ on the address bus and send out a ZERO on the $\overline{DBIN}$ control line. Use the combination of the address decoder and in gate to supply a ZERO to the enabling input of the three-state input-port buffers on the outputs of the converter. Send the same ZERO to the Clear input of flip-flop 2 on the Interrupt line. In this way, you put counter data on the data bus and remove the interrupt request, after it is serviced.

After reading the converter data, save it in one of the registers. Then let the system again pulse the a/d's Initiate Conversion input and start the next conversion. Have the μP restore its stack with a series of POP instructions, and reset the internal interrupt-enable flip-flop. Thus, the micro reads the converter after newly converted information becomes available. The rest of the time the processor is free.

### The multichannel interface

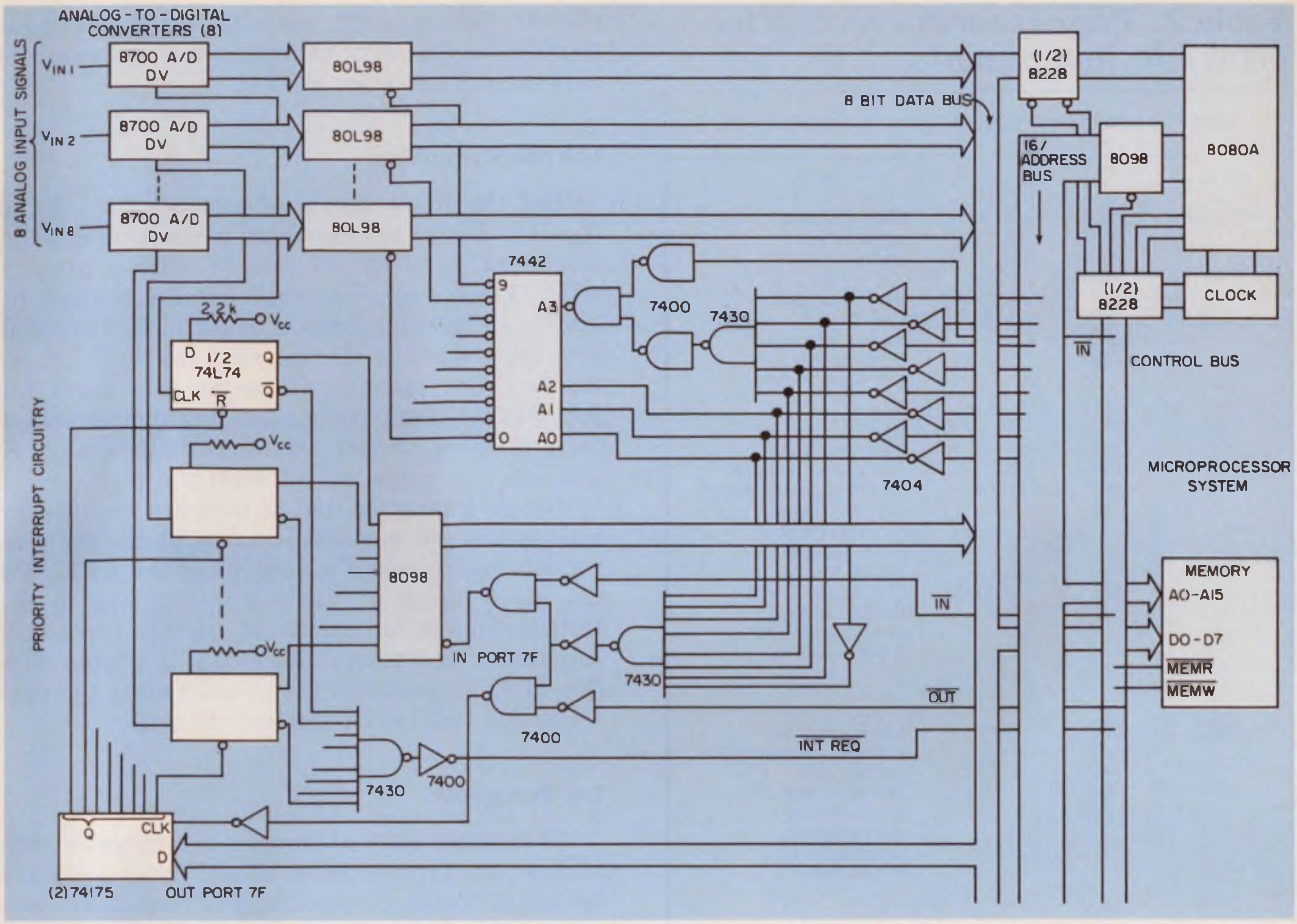
In systems with multiple analog inputs, many older designs use an analog multiplexer feeding a single, high-speed a/d converter. This approach is error-prone, of course, and requires complex interface logic. Now, with small low-cost monolithic converters, you can use a/d's for each analog line.

For example, the system in Fig. 3 has a battery of eight converters supplying data in parallel to the μP. The interface contains many of the same elements as the basic input port of Fig. 2. As before, feed the converter's data outputs to 80L98 buffers, which in turn drive the bus. The buffers' three-state feature allows you to make them inert selectively.

The decoding circuitry is slightly more complex. Apply the five high-order address lines as the inputs to a 7430 gate that enables a 7442 BCD-to-decimal decoder. To perform the final port-selection decoding with a 7442, select the appropriate a/d when an INPUT instruction is executed to one of the output ports, $F8_H$ to $FF_H$. Also, tie the converter's Initiate Conversion inputs high, so that the devices operate in the free-running mode.

Construct each of the eight interrupt-input ports of a flip-flop (1/2 74L74) with its D input wired high. Clock each flip-flop independently with the appropriate converter's Data Valid output. Gate the output of each flip-flop onto the line that requests the μP to interrupt (INT). Thus, you can request an interrupt whenever an a/d completes its cycle. Buffer the flip-flop outputs with an 8098 AND-tied to the data bus; enable this buffer, with the 7430 and 7400 gates, to respond to the input instruction at address $7F_H$. In this way, let the μP determine which flip-flop has caused an interrupt and which converter has completed its cycle.

Use an interrupt service routine (see Table 2) to save the contents of the working registers with a series of PUSH instructions. Then determine which port causes the interrupt with an input instruction to address $7F_H$. This instruction loads the status of each converter's Data Valid output from the 8098 into the accumulator. At this point, have the μP test the word, bit by bit, until it finds



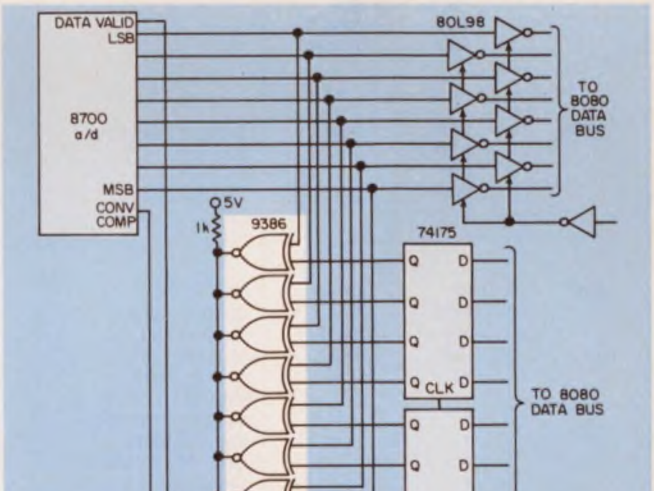

3. **This eight-port a/d converter system** is derived from the basic single-port interface. The maskable priority interrupt feature lets you program the microprocessor's servicing sequence for interrupt requests.

a ONE. Thus, the $\mu$P determines the address of the correct a/d input port and reads that port by means of an INPUT instruction. At the conclusion of the service routine, reset the flip-flop by sending a ZERO to the appropriate bit position of output port $7F_H$. Finally, restore the stack and reset the internal interrupt-enable flip-flop.

With this arrangement, then, the flip-flop tied to the second port can be set when one of the converters completes its cycle while another a/d port is being read. The second completed conversion generates an additional interrupt request signal—but the $\mu$P will not respond.

The $\mu$P's internal interrupt-enable flip-flop is automatically disabled by the first interrupt received—which locks out any further interrupts. You must reset the flip-flop with an EI instruction. End the first interrupt service routine by resetting the Status flip-flop and enabling the internal interrupt-enable flip-flop. Consequently you remove the source of the first interrupt. Then the second Status flip-flop causes a new interrupt which must be serviced in turn. Thus the $\mu$P will respond to each input port, even when several conversions are completed in a short time.

So far, the a/d ports have been equally im-




4. **To avoid wasting processor time,** monitor a slowly changing channel with this comparison scheme. Previously read data are latched into the 74175s by the $\mu$P. An interrupt request for this port is generated only when the converted data are different from those stored.

## Table 2. Priority service routine for eight interrupting ports

| Label | Instruction | Operand | Explanation |
|---|---|---|---|
| POLLED: | PUSH<br>PUSH<br>PUSH<br>PUSH<br>IN<br>MVI<br>STC<br>CMC | B<br>D<br>H<br>PSW<br>7FH<br>D, Ø | Save processor registers and status.<br>Read input port to find which caused interrupt. Set D to zero and Carry to zero. |
| LOOP 1: | RAL<br>INR<br>JNC | <br>D<br>LOOP1 | Determine which port caused interrupt by rotating accumulator left and testing for presence of Carry. Increment D each time. |
| | LXI<br>LXI | H, STABL<br>B, 3 | Load H and L with starting address of jump table and B and C with 3. |
| LOOP 2: | DAD<br>DCR<br>JNZ<br>PCHL | B<br>D<br>LOOP2 | Add B and C to H and L, decrement D and test for zero. Exit loop by transferring to appropriate jump command in jump table. |
| STABL: | JMP<br>JMP<br>JMP<br>JMP<br>JMP<br>JMP<br>JMP<br>JMP | ONE<br>TWO<br>THREE<br>FOUR<br>FIVE<br>SIX<br>SEVEN<br>EIGHT | Jump table consisting of 3-byte jump instructions. |
| RSTR: | POP<br>POP<br>POP<br>POP<br>RET | PSW<br>H<br>D<br>B | Restore registers and exit. |
| ONE: | IN<br>MOV<br>MVI<br>OUT<br>EI<br>•<br>•<br>•<br>•<br>•<br>JMP | ØF8H<br>B, A<br>ØFEH<br>7FH<br><br><br><br><br><br><br>RSTR | This is the service routine for port #1. It loads the priority mask with 1111 111Ø, enables interrupts and processes data. At conclusion, the program jumps to RSTR. |
| TWO: | IN<br>MOV<br>MVI<br>OUT<br>EI<br>•<br>•<br>•<br>•<br>•<br>JMP | ØF9H<br>B, A<br>ØFCH<br>7FH<br><br><br><br><br><br><br>RSTR | This is the routine for port #2. The priority mask is 1111 11ØØ which keeps port #1 from interrupting. |

portant. To assign the ports priorities, you have to make only a slight change in the program; no hardware changes are needed.

### The priority problem

Hold the Reset inputs of selected Data Valid flip-flops low to prevent those ports from causing interrupts. Load output port 7F with a priority mask. Begin each interrupt service routine by loading a different priority mask into the output port and resetting the internal enable-interrupt flip-flop. For example, if the priority mask for port 3 is 11111100, ports 1 and 2 cannot interrupt the processing of port-3 data; ports 4 through 8, however, can cause more interrupts.

You can guarantee that no data are ever lost by making a slight modification that places the conversion cycle under the control of the CPU. Tie the Reset inputs of the Status flip-flops to the Initiate Conversion inputs of the flip-flop's corresponding converters. Resetting a Status flip-flop after its port has been read causes the converter for that port to restart its cycle.

### The throughput

When either your $\mu$P processes a large amount of data or a large number of a/d input ports are connected to the bus, you might feed more data to the system than it can process. But if the analog inputs on some of the ports change slowly, you can add logic that increases the effective capacity of the system. Add a latching output port with the same address as its corresponding a/d input port (see Fig. 4). Then, after you read the input port, generate an output instruction to the same address. The data are thereby duplicated in the 74175 latches. A pair of 9386 quad, exclusive-NOR circuits with open-collector outputs compares the output word from the a/d with the word stored in the 74175 latches. The open-collector feature of the 9386 allows it to be collector-ORed; ONEs at all 9386 outputs signify that the data in the a/d latches match the data in the output ports. This condition means that there has been no change in the analog-input voltage, so there is no need to reprocess the data. When the a/d bits do not match the corresponding bits in the 74175, the output of the 9386s goes to ZERO. This output clocks the 7474 Status flip-flop, which in turn interrupts the $\mu$P. From this point the operation is unchanged. ■■

**References**


1. Schmid, H. and Mrozowski, G., "Mating Microprocessors with Converters," *Electronic Design*, Sept. 1, 1975, p. 76.
2. Nichols, A. J. and McKenzie, K., "Build a Compact Microcomputer," *Electronic Design*, May 10, 1976, p. 84.

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# Control 10 to 10,000 Hz digitally and get complementary output frequencies

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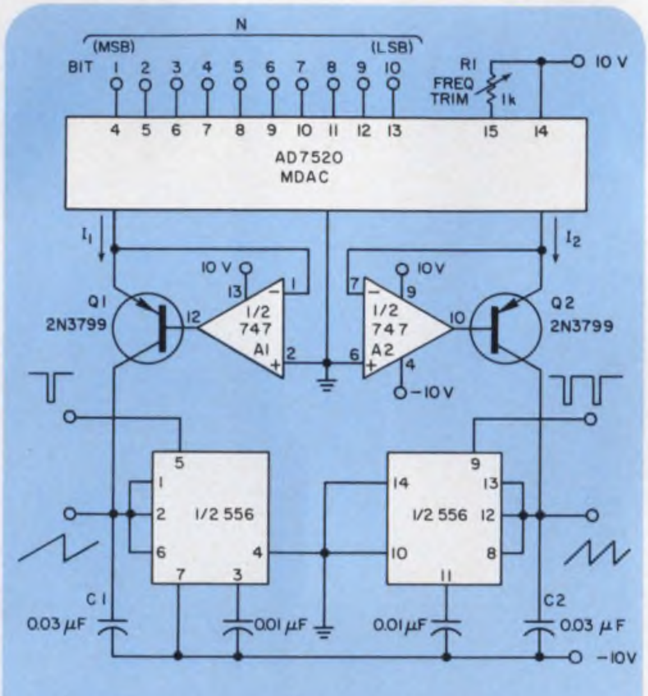
An AD7520 d/a converter provides an output current, $I_1$, proportional to N, and another current, $I_2$, proportional to 1023−N. The transistors $Q_1$ and $Q_2$ and op amps $A_1$ and $A_2$ not only charge capacitors $C_1$ and $C_2$, but also maintain a zero-voltage sink to absorb the d/a converter outputs. The timer circuits discharge the capacitors to 1/3 $V_{cc}$ whenever the voltage reaches 2/3 $V_{cc}$ at a frequency proportional to the currents $I_1$ and $I_2$. Since the charging current is proportional to the digital input, linear digital-to-frequency operation is achieved.

*D. R. Morgan, Senior Engineer, General Electric Co., Electronic Laboratory, Syracuse, NY 13201.* CIRCLE NO. 311




**Complementary frequencies proportional to digital inputs** are provided with only three DIP IC packages and two transistors.

# Watchdog circuit guards µP systems against looping

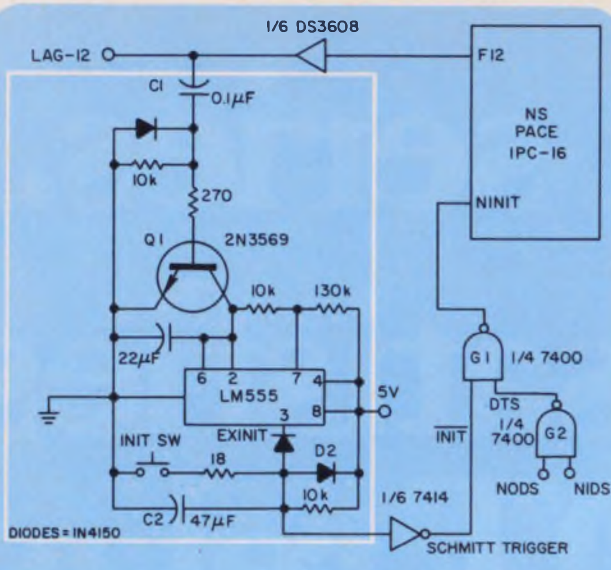
Lightning discharges or even man-made EMI can totally scramble commands and produce a looping condition within a mini or microcomputer's program. Component or peripheral equipment failure can cause the microprocessor system to hang up in a loop. And even though all due caution is exercised during program development, bugs may reside for years without being discovered.

Therefore, an automatic "watchdog" circuit is imperative in unattended systems and is quite useful in most other systems.

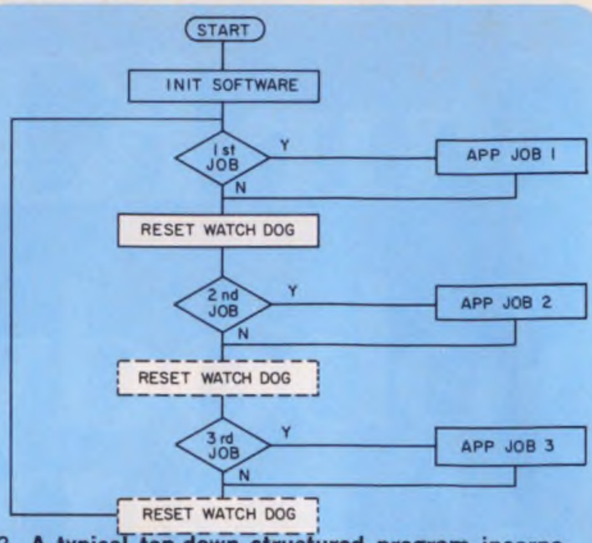
The watchdog circuit (Fig. 1) is built around an LM555 timer. Applied to National Semiconductor's PACE microprocessor, the timer is periodically reset by the µP's F-12 flag signal via capacitor $C_1$ and transistor $Q_1$. Should the flag signal fail to appear within the 555's timeout period, an output labeled EXINIT is generated. And should the system fail from other causes with F-12 high, coupling capacitor $C_1$ prevents a system lockup.

EXINIT "pulls down" $C_2$ and fires the Schmitt

*(continued on page 92)*




1. **Watchdog circuit monitors subroutine time.** Should an F-12 signal fail to appear within a predetermined limit, looping is indicated and the system is reinitialized.




2. **A typical top-down structured program** incorporates watchdog reset commands within the executive program. To accommodate the timing of different job loops, multiple watchdog resets (shown dotted) may be required. Tree-oriented logic requires watchdog resets at major branch points.

trigger as does the manual switch, INIT. Inverted by $G_1$, INIT, reinitializes the processor via the $\mu$P input, NINIT; DTS (data transfer strobe) to $G_1$ prevents an initialization during a data transfer, which prevents a short write cycle from producing errors.

With "top-down" programming, the resetting command for the watchdog is located in the executive program between subroutine junctions (Fig. 2).

The watchdog's timeout period might be critical, depending on how long the system user can wait before deciding that the system is looping. As a rule of thumb, the watchdog timer should be set 20% longer than the longest legal routine. A greater safety margin may be needed in systems not having crystal-clock timing.

In a large system with many relatively fast-response modules, the longest legal routine might take as long as 500 ms. But each loop might take only 10 ms to execute. Here, several reset commands can be distributed within the executive routine to allow an over-all shorter watchdog time.

Locating the watchdog reset command and setting the timeout period in "tree-oriented" program logic are more difficult and more critical. Parallel subroutines and greater programming difficulty allow a high probability of error and inadvertent program looping. In limited programs, the watchdog reset commands are located at the main branch points. On more extensive programs, the reset commands are integrated into several branch points located within the tree structure.

An ancillary software or hardware counting circuit, set for a predetermined number of NINIT-signal counts is a valuable checkout tool. If, say, three counts occur during a fixed time-period, a high possibility exists that the system is malfunctioning. Visual and aural indications can then be given, and the equipment shut down, especially when malfunctioning, can be dangerous.

Coding, of course, depends upon the device and program concept. For a PACE, the coding is:

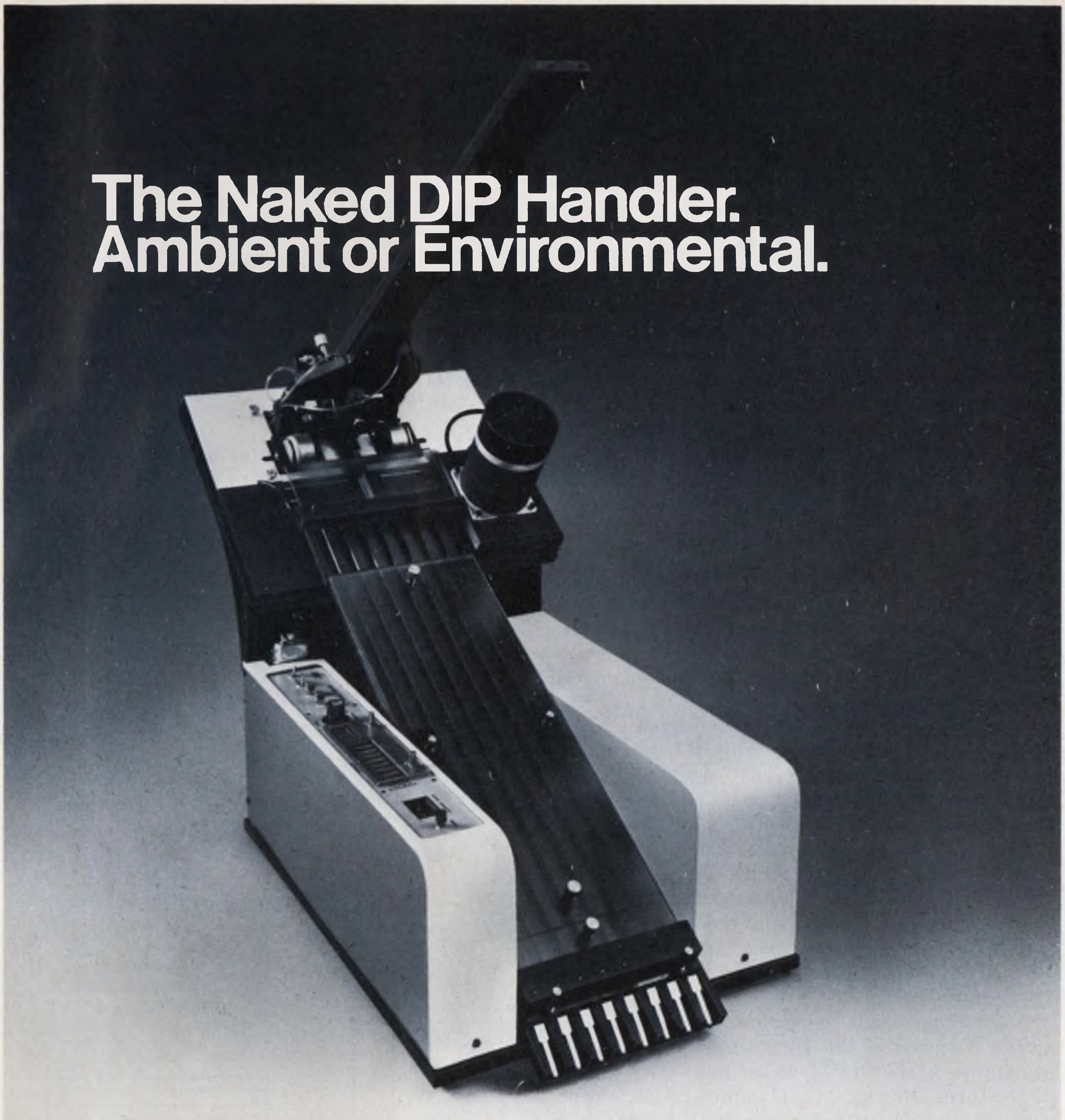
```
                   .TITLE WDRST,' WATCHDOG RESET VIR0 TPXVS101876A'

                   ; DEMONSTRATION OF CODE TO RESET WATCHDOG
                   ; TIMER USING F12 AS RESET SIGNAL

                   START:
        000C                 F12=12            ; ASSEMBLER ASSIGNMENT

   0000 3C00 A               PFLG  F12         ; TO RESET F12 IF HIGH
   0001 5C00 A               NOP               ; TIMING
   0002 3C80 A               SFLG  F12         ; STARTS RESET PULSE
   0003 5C00 A               NOP               ; TIMING
   0004 3C00 A               PFLG  F12         ; ENDS RESET PULSE

        0000       .END START

START   0000  T        F12      000C  A
NO ERROR LINES
SOURCE CHECKSUM = 5622
```

Ensure that nothing in the executive or any of the subroutines can alter the flag chosen as the reset signal. The designer may use both the editor and de-bug programs.

The watchdog circuit is useful also in system checkout. Routines and subroutines can progress automatically, with the watchdog calling attention to the loops as they develop. Time is saved not only when the watchdog reinitializes the system on random disturbances, but also when component failure or hidden faults are exposed in the operating program.

*Victor E. Shiff and Richard H. Parr, Engineering Department, Teleplex Corp., 33 Danbury Road, Wilton, CT 06897.*

CIRCLE NO. 312


The Naked DIP Handler.
Ambient or Environmental.

# Circuit allows program-halt and single-instruction mode on $\mu$P

The ability to halt program execution and then to proceed one instruction at a time is a valuable capability of any computer system. In a microprocessor system, this capability is normally implemented by controlling its run/halt input.

The Fairchild F8 $\mu$P, unlike most other 8-bit $\mu$Ps, doesn't have a run/halt input. Nevertheless, the circuit in Fig. 1 provides such a run/halt and single instruction capability for the F8.

With the circuit's switch, $S_1$, in the Run position, the F8 executes normally. When it is in the Halt position, instruction execution is effectively "halted." Then the momentary-contact switch, $S_2$, can be used to initiate a single CPU (central processor unit) instruction and then to return the $\mu$P to the halt state.

Although the processor can't directly halt execution, the system can be "halted" by forcing the CPU to execute a sequence of no-ops. And because the program counter is not contained within the F8 CPU chip, the counter isn't advanced during this no-op situation.

To halt the F8, an instruction-fetch request from the $\mu$P's output ROMC control bus is detected and translated by the control circuit into a system no-op. At the same time, a processor no-op instruction (2B hexadecimal) is placed on the data bus. The F8 CPU reads the data bus and executes the no-op instruction. After executing the no-op, the CPU's fetch-request for another instruction again translates to a no-op, and so on.

The instruction-fetch code of all ZEROs on the F8's ROMC output lines is detected with a simple NOR gate, $G_1$.

After appropriate synchronization, the control circuit translates the instruction fetch into a system no-op code (1C hexadecimal) with the use of the three OR gates, $G_2$, $G_3$ and $G_4$. Also, a processor no-op code (2B hexadecimal) is placed on the data bus by the control circuit's 74S241 three-state buffer, $IC_1$.

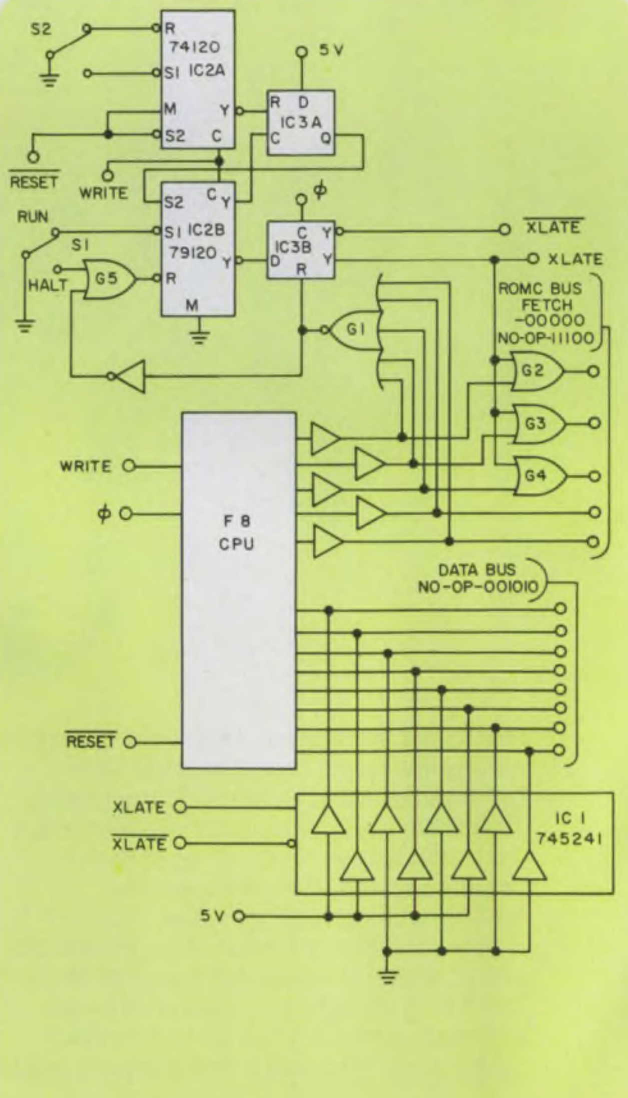
The control circuit's pulse synchronizer, $IC_{2a}$ and $IC_{2b}$, provides all the necessary synchronization. If $S_1$ is in the Run mode, $IC_{2b}$ passes pulses. The CPU clock occurs during a Write pulse, so $IC_{3b}$ is continually clocked LOW, thus clearing the Xlate signal to allow normal operation. When $S_1$ is placed in the Halt mode, $IC_{2b}$ continues to pass pulses until a negative transition of the reset input $G_5$ occurs.

A reset occurs when an instruction fetch is detected by $G_1$. When $IC_{2b}$ stops passing pulses, $IC_{3b}$ is clocked HIGH, thus setting Xlate and halting the processor.

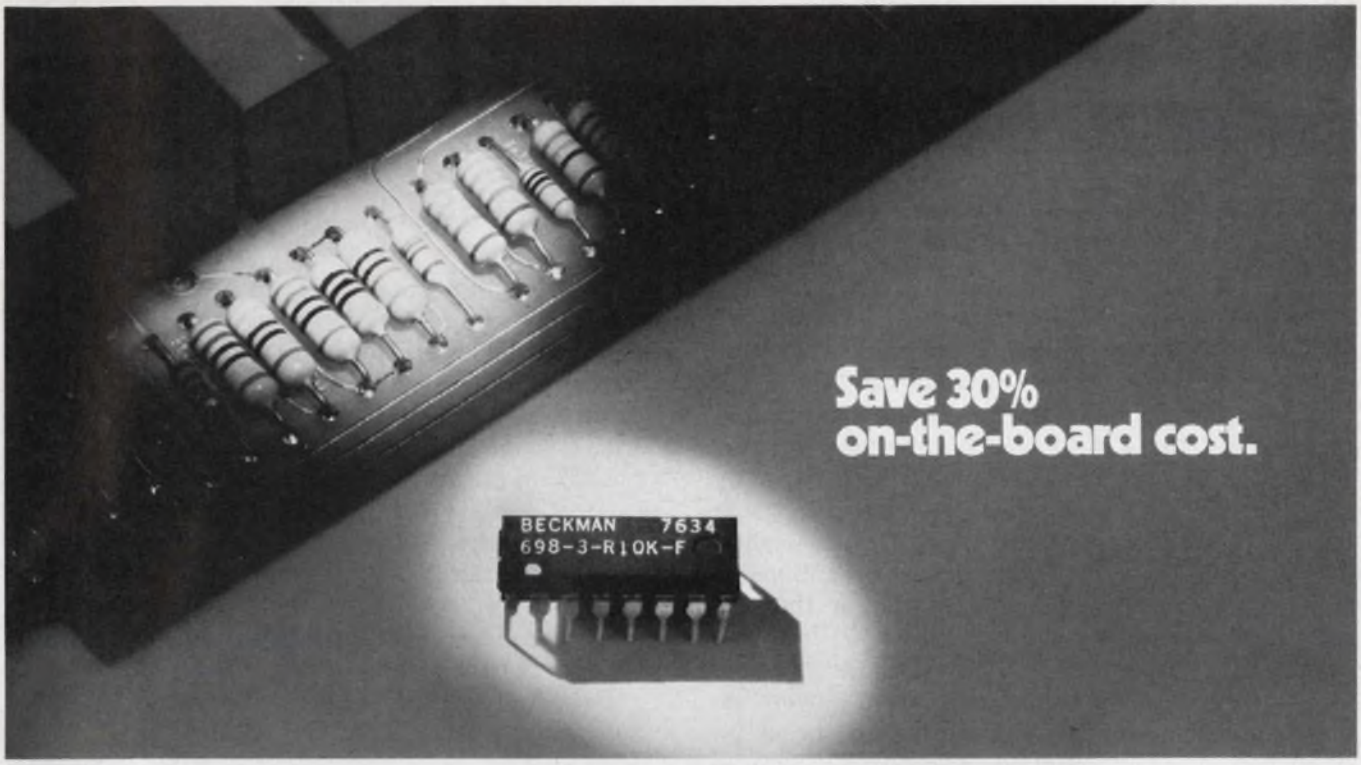
When the processor is halted, switch $S_2$ can single step the system. With $S_2$ pressed, $IC_{2a}$ passes one pulse, which resets $IC_{3a}$. Since $IC_{3a}$ is reset, $IC_{2b}$ passes the next Write pulse, which causes the F8 to begin normal execution. Execution continues until another instruction-fetch cycle is detected.

The Reset input of $IC_{2a}$ should be connected to the F8 CPU reset line to ensure proper system reset.

*Terry Dollhoff, Director of Computer Science, Acuity Systems Inc., 11413 Isaac Newton Square, Reston, VA 22090.* CIRCLE NO. 314




**1. A control circuit translates the instruction-fetch code** into a sequence of no-op's to obtain a $\mu$P-system "halt" and to allow single-instruction action.

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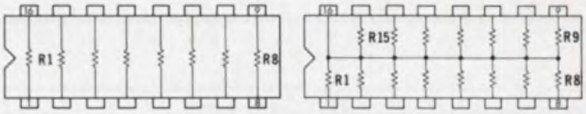


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CIRCLE NUMBER 46

# Simple solid-state relay circuit can be built with few components

A sensitive-gate triac such as the 2N6071B makes possible the construction of a simple, inexpensive solid-state relay where the triac gate is driven directly by an opto-isolator. No amplifier is necessary, nor is the circuit complicated by the need for a dc power supply (see figure).

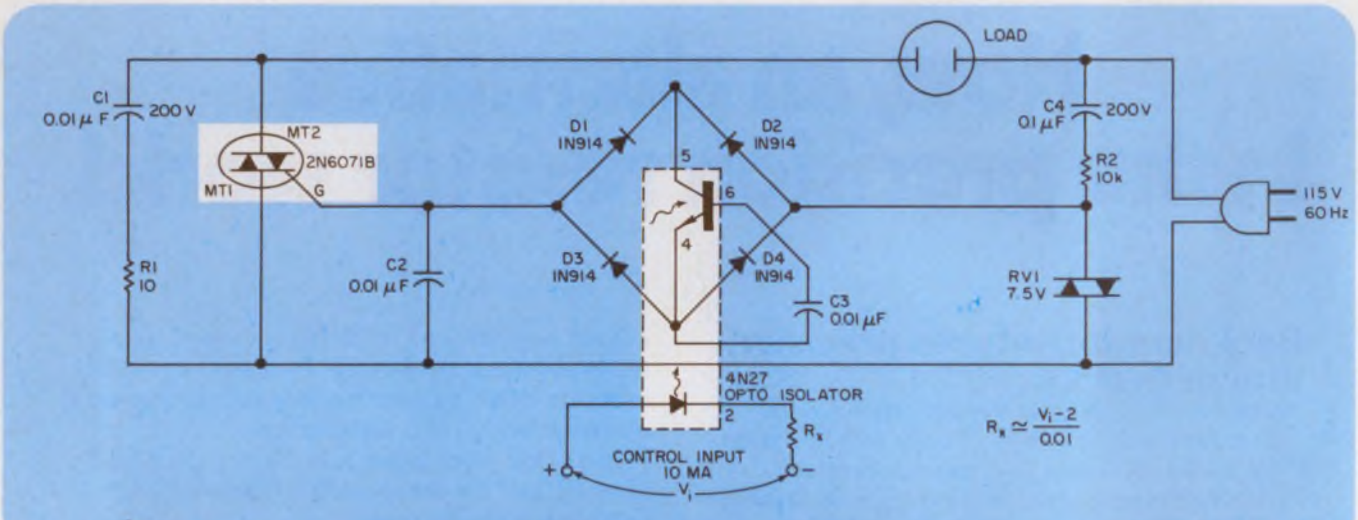
Current to trigger the triac flows directly from the line through capacitor $C_1$ and resistor $R_2$. The capacitor introduces a leading phase shift into the gate current to make the current maximum near the zero-voltage crossing of the line voltage. Resistor $R_2$ and varistor $RV_1$ limit the voltage applied across the opto-isolator transistor, and also protect the isolator from power-line transients and surges, especially any occuring when power is first applied. Varistor $RV_1$ can be any general-purpose type that limits voltage peaks to about 20 V.

Bridge diodes $D_1$ through $D_4$ (low-cost general-purpose types) route the gate current in the proper direction through the opto-isolator transistor. And components $R_1$, $C_1$, $C_2$, and $C_3$ prevent the triac from triggering for a half-cycle when power is first turned on. These components can be omitted if the half-cycle of power to the load can be tolerated.

The circuit can control ac circuits that draw about 2 A (nominal), although with proper heat sinking the triac can handle 4 A.

*Dale Hileman, Sphygmetrics, Inc., 6311 J DeSoto Ave., Woodland Hills, CA 91367.*

CIRCLE No. 313




**A solid-state relay** built with a sensitive-gate triac needs no amplification between opto-isolator and triac.

**IFD Winner of September 13, 1976**

**J. E. Buchanan,** Westinghouse Electric Corp., Defense & Electronics Systems Center, Friendship International Airport, P.O. Box 746, Baltimore, MD 21203. His idea "Build a Voltage-Controlled Oscillator with only One TTL-Inverter Package" has been voted the Most Valuable of Issue Award.

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# New method speeds $\mu$P software development

A radical technique that speeds up microprocessor software development has been introduced by Quarndon Electronics of Derby, England.

Known as direct assembly, the British technique combines the two separate, basic programs used in the conventional method of generating $\mu$P software:

- The Assembler, which converts mnemonic instructions and symbolic addresses into absolute machine code.
- The Editor, which allows assembly-language programs to be modified without re-entering the entire program.

In their place, a single Direct Assembler simultaneously converts each mnemonic instruction or each symbolic address to machine code as it is entered, and checks for syntax errors. Errors can be corrected on the spot before entering additional mnemonics. Standard monitor functions, such as breakpoints are also included.

Direct Assembler programs have been developed by Quarndon for the 8080 and 2650 systems run on Nova minicomputers. A resident 8080 Direct Assembler has also been developed that occupies only 3 kbytes of PROM.

Quarndon's resident Direct Assembler is used with a single-board 8080 microcomputer that doubles as the development system. Work is now in progress to produce resident Direct Assemblers for 2650 and 9900 systems.

## Demand for 3-D semi observation is answered

Observing, measuring and displaying three-dimensional semiconductors are now possible with a stereoscopic observation and measuring instrument that connects to a scanning electron microscope.

Developed by the Central Research Laboratory of Hitachi, Ltd., Tokyo, the instrument measures three-dimensional (3-D) images, magnified up to 500,000 times, to a maximum height of 300 Å and a maximum length and width of 30 Å.

The instrument has two 3-D-image memory devices, a time-sequential television with a PLZT electro-optical shutter, and a measuring unit. (PLZT is a piezoelectric material composed of lead lanthanum, zirconium and titanium.)

An object can be observed three-dimensionally with the scanning electron microscope because each eye views the object from a different angle. The specimen is tilted in the microscope column, and electron beams are directed at it from two different angles. As a result, *two* images are stored in the image-memory devices and shown on a television monitor. Each image is presented alternately at 1/60th of a second and synchronized by the PLZT shutter.

The 3-D measuring unit computes distances automatically and gives digital readings.

Unlike Hitachi's instrument, a conventional dynamic stereo microscope cannot tilt the specimen, but must deflect the two incident electron beams before the specimen can be viewed from different angles. But as a result, the resolution drops about 10,000 times to about 1000 Å.

Hitachi's instrument can even measure and display heights of less than one micrometer, such as scratches on a polished surface.

## Schottky-barrier anode device doesn't suffer

A planar, gallium-arsenide, Gunn-effect device by Fujitsu Laboratories, Kawasaki, Japan, does not suffer from the usual high electric-field layer near the anode that causes current saturation at high bias and incoherent oscillation. A Schottky-barrier anode contact in Fujitsu's device eliminates the high field.

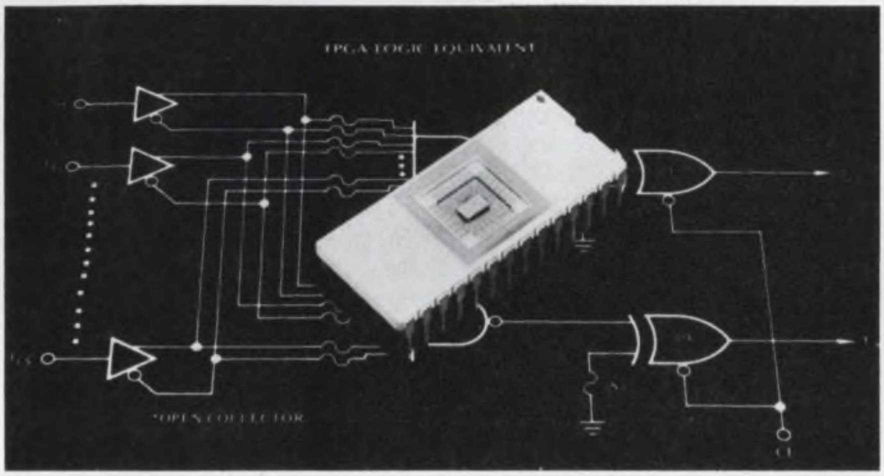
The device is formed by n-GaAs layers—grown on (100) crystalline-oriented surfaces of chromium-doped, semi-insulating substrates —whose carrier concentrations are 8 to 15 $\times$ $10^{15}$ $cm^{-3}$ with thicknesses of 3 to 5 $\mu$m. The cathode contact is formed from an alloyed gold-germanium-nickel film; the anode contact is an evaporated aluminum film. Straight, bar-shaped active areas, 35-$\mu$m long, are formed by mesa etching.

Measurements of the current/voltage (I/V) characteristic under dc-biased conditions show that the I/V curve is linear over a range of more than 15 V—better than the 5 V recorded for the earlier devices with ohmic-anode contacts.

While the earlier devices produce only noisy waveforms, the Schottky-barrier anode devices produce coherent waveforms with a typical period of 750 ps.

Because of its stable operation, Fujitsu's Gunn-effect device looks promising for very-high-speed logic applications.

# Programmable gate arrays add flexibility, cut complexity



*Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Napoleone Cavlan (408) 739-7700. P&A: See text.*

In addition to read-only memories and programmable logic arrays now used as low cost replacements for discrete logic, a new tool has become available to the logic designer—the programmable gate array (PGA). Developed by Signetics, this circuit contains nine 16-input AND/NAND gates, each with its own output.

Although the PGA and PLA seem alike at first glance, there are some major differences. The PGA is a one-level gate array that performs AND or NAND combinations, while the PLA is a more complex two-level array that performs AND/OR, NAND/OR and other dual combinations.

Each of the nine PGA gates has 16 inputs, but each of the 16 inputs can appear in either its true or complement form. And, any or all of the 16 inputs for each gate can be programmed for don't-care conditions by electrically disconnecting them from the gate input.

The output of each NAND gate goes into an Exclusive-OR gate, which can be programmed to behave as inverter to convert the NAND output to an AND. If the Exclusive-OR gate is left unprogrammed, the NAND gate output remains unchanged. Programming is done in much the same way as in PROMs and PLAs—zapping nichrome fuse links that were deposited on the chip during fabrication.

There are two versions of the PGA available—the 82S102 and the 82S103. The 82S102 has open collector outputs, and the 82S103 three-state outputs. Both versions have an output-enable control line that permits output strobing.

Two operating temperature ranges are also available. Units with an N prefix operate over a 0-to-75-C range while units having an S prefix function over −55 to +125 C. N-series units have a maximum propagation delay, input-to-output, of 30 ns, and a maximum input loading of −100 μA. S-series PGAs have a maximum delay of 40 ns and a maximum input current limit of −150 μA. Typical power dissipation for all units is about 600 mW.

All PGAs operate from a 5-V TTL power supply and are fully TTL-compatible on all inputs and outputs. For gate programming, however, the supply voltage must increase to 8.75 V and the output voltages must be brought to about 17 V. Fusing current must be limited to about 175 mA.

Available in plastic or ceramic 28-pin, 600-mil-wide DIPs, the arrays cost $7 each and up for the commercial plastic version in 100-unit quantities. Delivery is from stock.

**CIRCLE NO. 303**

## LED flashing circuit doubles battery voltages

*Lithic Systems, P.O. Box 869, Cupertino, CA 95014. Robert Hirschfield, (408) 257-2004. Less than $0.50 (lge. qty.); stock.*

The LS3909 monolithic LED flasher circuit is a direct second-source for the LM3909 from National Semiconductor. The flasher can blink 1.6-V LEDs from a battery voltage as low as 1.1 V, by use of a voltage-doubling technique. The LS3909 is available in 8-pin mini-DIPs, TO-100s, and individual chips.

**CIRCLE NO. 304**

## Motor controller handles brushless ac motors

*Photo-Therm, 110 Sewell Ave., Trenton, NJ 08610. Roman Kuzyk (609) 396-1456. $6 (1000-up); 4 wks.*

Control the loading of any brushless ac motor with the power controller. The circuit, housed in a 14-pin DIP, can turn off the motor upon overload (settable to 1% of load), provides line voltage operation, has zero-crossover firing for inductive loads and contains two delay circuits, one for overcoming starting surge and a second to override short-term overloads. A patented technique that measures the power factor of the motor is used by the IC.

**CIRCLE NO. 305**

INTEGRATED CIRCUITS

## IC does both f/v & v/f conversions to 100 kHz

*Intech/FMI, 282 Brokaw Rd., Santa Clara, CA 95050. (408) 244-0500. From $6.50 (100-up); stock to 4 wks.*

Capable of operating over a near-dc-to-100-kHz range, the A-8402 voltage-to-frequency or frequency-to-voltage converter requires only a 4-to-18-V supply. An analog input voltage of 0 to 10 V can be converted into a pulse train of 100 kHz, maximum. Key specifications include a ±0.05% maximum nonlinearity at 10 kHz, a ±200 ppm maximum tempco on gain, and a digital output compatible with DTL, TTL, and CMOS. The A-8402 operates over 0 to 70 C and an extended temperature range version (A-8402 ET1) is available for −25 to +100 C operation. The v/f/v converter is housed in a 14-pin ceramic DIP.

CIRCLE NO. 306

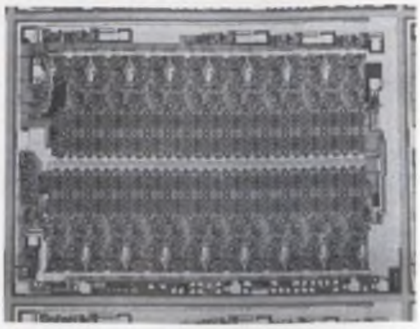
## Monolithic tachometers switch at desired speed

*National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5000. $1.65 (100-up); stock.*

By combining a frequency-to-voltage converter, a high-gain op amp and a comparator on a single chip, National Semiconductor has developed the LM2907 and 2917 monolithic tachometer speed switches. When the circuits are used with a floating transistor as an output, either a supply-referred load of 50 mA or a swing-to-ground for zero frequency can be handled. Both circuits are specifically designed to operate relays, lamps, and other components when the input frequency reaches or exceeds a selected rate. The main difference between the two devices is that the LM2917 includes an active shunt regulator to clamp the supply. The regulator is not included in the LM2907. The tachometer circuits are also available as 8-pin models (2908 and 2918). Models 2907 and 2917 have 14 pins. All units operate from 12 V and have a maximum frequency input of 10 kHz. Nonlinearity for a 10-kHz input is 1% maximum.

CIRCLE NO. 307

## FIFO memories operate at rates to 20 MHz



*Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. John Kosek (408) 739-3535. $28 (100-up); stock.*

A first-in, first-out memory, the 67401, is organized 4-bits wide and 64 words long. It is pin compatible with the Fairchild MOS 3341 FIFO, but at its typical speed of 20 MHz is about 20 times faster. The 67401 is suitable for synchronous or asynchronous operation, uses a standard 5-V power supply and is TTL compatible on all inputs and outputs. The memory is available in a standard, 16-pin, side-brazed package.

CIRCLE NO. 415

## Multidecade latched counter handles 8 digits

*LSI Computer Systems, 1235 Walt Whitman Rd., Melville, NY 11746. Alvin Kaplan (516) 293-3850. $8.15 (100-up); stock to 6 wks.*

A six-decade, dc-to-5-MHz up-counter, the LS7031, has a built-in 8-digit multiplexer. All counter outputs are latched and data are available in multiplexed BCD format. Two additional on-chip quad latches, in the two LSD positions, allow the latching of BCD data from off-chip prescalers, thus permitting a count rate well above 5 MHz. Digit strobes are guardbanded so they occur totally within valid BCD data. The multiplex scan counter is driven by an external clock or an on-chip oscillator whose frequency is determined by an external capacitor. Maximum multiplex frequency is 500 kHz. The MSB of decades 6, 7 and 8 are available for overflow and carry functions. The circuit operates from a single power supply, between +5 and +15 V dc and comes in a 40-pin DIP.

CIRCLE NO. 416

## High voltage display drivers handle 200 V

*Dionics, 65 Rushmore St., Westbury, NY 11590. (516) 997-7474. From $2.06 (1000-up); stock.*

The DI-300 and DI-500 families of monolithic high voltage display drivers offer programmable constant-current outputs. For example, the DI-302 level-shifted segment driver is a pin-for-pin replacement for the Sprague UDN-7183A, 7184A and 7186A but it also offers a programmable constant-current output of 0.1 to 2.5 mA. The DI-300 has the same programmable constant-current output. Both are housed in 18-pin DIPs and are designed for eight-channel displays. The level shifter portion of the DI-300 circuit has an operating voltage capability of 200 V; the DI-302 is rated for 125 V. The DI-500/505/510 series of level-shifted digit drivers feature full 200-V level shift capability. The DI-502/507/512 drivers have a 125 V capability. These devices are direct pin-for-pin replacements for the Sprague UDN6144A, 6164A and 6184A circuits, respectively. They also functionally replace the Signetics 585 Series. All DI-500 family types are available in 4, 6 and 8-line versions.

CIRCLE NO. 308

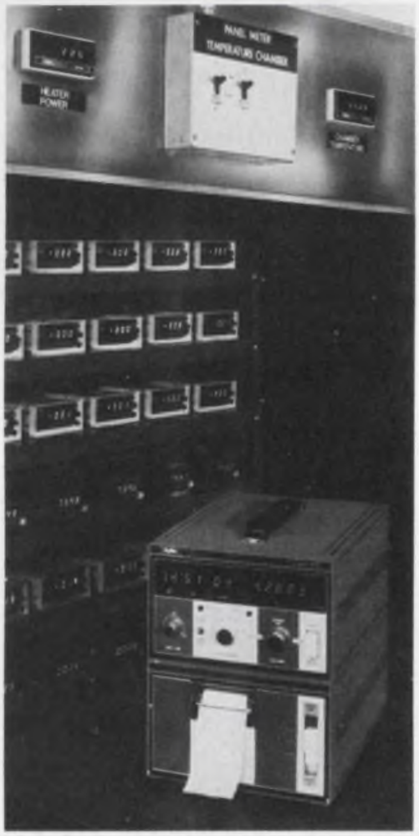
## ICs for remote control provide 31 functions

*Siemens AG, Zentralstelle fur Information, Postfach 3240, D-8520, Erlangen 2, Federal Republic of Germany. Joachim Ullmann.*

Two MOS ICs, the S556 and S554, can be used to form an infrared remote control system. The S556, when used with two to four LEDs, functions as the transmitter and the S554, with a photodiode, serves as the receiver. Up to 31 control functions are possible and binary coded outputs can easily be decoded. The 18-pin S556 draws only 10 $\mu$A; the receiver circuit comes in a 28-pin DIP.

CIRCLE NO. 309

# Data logger changes role with drop-in card modules



*Digitec/United Systems Corp., 918 Woodley Rd., Dayton, OH 45403. (513) 254-6251. See text.*

It's rare today to get more for less, but that's what the Digitec Datalogger 1000 gives you—more data logging capability for about 10% less dollars than its closest competitor, the Doric Scientific 200.

At $1995, the 1000 comes with 10 channels, field-interchangeable modules for multiparameter measurements (one at a time), an internal crystal clock that reads out real or elapsed time and a 20,000-count (4-1/2 digits) display. These features are just a sprinkling of what the 1000 offers.

By contrast, the 12-channel Doric 200 sells for $2290 with an optional clock, and displays just 3-1/2 digits. The 200 also appears to be less accurate than the Digitec unit.

The signal-conditioning modules (PC boards) of the 1000 aren't found on other units. The Digitec approach lets you go from dc to ac voltage, to true-rms, to dc autoranging or to temperature measurements (RTD, thermistor or thermocouple) at will. Extra modules range from $130 to $275 (temperature modules cost $175).

If you need more channels, the Digitec lets you expand up to 100; the Doric to only 24. Program time intervals are switch selectable on the 1000. Nine intervals are available, ranging from 1 min to 5 h, and you can choose from manual, continuous and automatic-cycle modes.

Single-point, repeat printing is also standard in the Digitec unit. This feature selects a data point of interest, continuously interrogates that point and displays and records—at a selected interval—all pertinent information. The displays of time, channel number and measured data are simultaneous—not time-shared as in other units.

Resolution of the 1000 is 1 $\mu$V dc, 10 $\mu$V ac and 0.01° for temperature. Systems dc accuracy—at 23 C and $< 85\%$ relative humidity—is $\pm 0.01\%$ of reading $\pm 0.005\%$ of full scale on the higher ranges; it gets slightly worse on the more sensitive scales.

With autoranging, another feature not found on the Doric unit, the 1000's accuracy again suffers slightly. Note that "systems" accuracy doesn't include items like thermal EMF or offset voltages contributed by scanning cards. Accuracy of the Doric 200 is listed as $\pm 0.1\%$ of full scale $\pm 5$ $\mu$V, with an additional tempco of $\pm 0.0025\%$ of reading/°C.

The Digitec's 60-Hz CMR isn't very high—only 80 dB versus the Doric's 59-Hz spec of 120 dB. However, Digitec specs CMR at 1000-Ω imbalance, the most accepted way, while Doric uses a 100-Ω value.

Optional features—alarms, BCD

*(continued on page 106)*

## INSTRUMENTATION

*(continued from page 104)*
outputs and more—further expand the 1000's capabilities. For its performance, the 1000 is surprisingly compact. The unit measures 8-1/2 × 11 × 14 in., and weighs but 22-1/2 lb. Delivery takes two weeks, starting Feb. 15.

For Digitec CIRCLE NO. 301
For Doric CIRCLE NO. 302

## Unit scales or corrects errors in count source


*Durant, 901 S. 12th St., Watertown, WI 53074. (414) 261-4070. From $400; stock-8 wks.*

Series 1100 scaler/error corrector alters a count received from a signal source (transducer) and compensates for error factors in the measuring system. The 1100 provides a metric output even though the input supplies American units. Series 1100 is not a counter itself, but is used to interface between the count source and a counter to scale pulses into usable engineering units, such as inches, feet or meters. Standard units have count speed to 6 kHz, five digits of preset for correction setting and are available in desk or panel mounting.

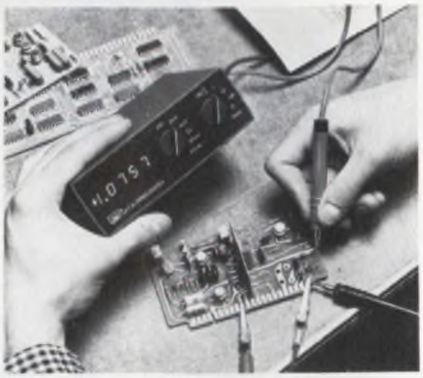
CIRCLE NO. 310

**Filler**

*We hear from Bob Pease of National Semiconductor that a National spy has just returned from Signetics with one of its secret processes. He says that, by making a NOR gate with Insulated Gate transistors, you get an IG-NORe gate which, of course, is the key to the Signetics Write-Only Memory.*

*Now that we have the secret, Pease confides, we can second-source the WOM and make more than twice the profits that Signetics did.*

## Miniature DMM reads true rms



*Data Precision, Audubon Rd., Wakefield, MA 01880. (617) 246-1600. $345.*

Model 248 provides true-rms measurement of ac volts and current. Measuring only 1-3/4 × 5-1/2 × 3-1/2-in. deep, the unit offers 4-1/2-digit resolution on all parameters, and it features 10-$\mu$V sensitivity dc and ac. Basic one-year accuracy is ±0.05% of input. Maximum crest factor is 5 at full scale ac voltage and current range input, and 2-1/2 at the 100% over-range level. The rms-to-dc conversion is accomplished with a calculating converter LSI module.

CIRCLE NO. 417

## Unit analyzes for electrical safety

*Bio-Tek Instruments, 500 Shelburne Rd., Shelburne, VT 05482. (802) 985-8014. $497; 4-8 wks.*

Model 250MA electrical safety analyzer performs all safety tests as described in the National Electrical Code, the NFPA 76BT and in AAMI Safe Current Limits. With simple pushbutton control, you can perform leakage-current testing, potential-difference testing, voltage measurement, ground-wire resistance measurement and power conduct-to-chassis resistance. Model 250MA also measures current consumption at the push of a button.

CIRCLE NO. 418

## Two models join generator line

*Marconi, 100 Stonehurst Ct., Northvale, NJ 07647. (201) 767-7250. 2015/1, $2250; 2015/2, $2250; 60-90 days.*

Two new AM/FM signal generators, based on the Model 2015, cover 10 to 520 MHz to meet the specialized modulation requirements of telemetry systems and narrowband mobile radios. Model 2015/1 is particularly suitable for use in the production and servicing of narrowband transceivers. It has full-scale deviation ranges of 2.5, 5 and 25 kHz. Model 2015/2 is a wide deviation version suitable for tests on wideband telemetry receivers. It features full-scale deviation ranges of 20, 100, and 500 kHz.

CIRCLE NO. 320

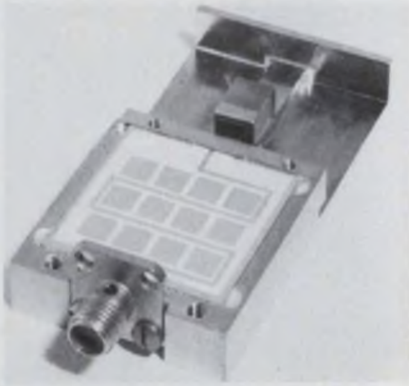
## Graphics package tells user what to do

*Julie Research Laboratories, 211 W. 61 St., New York, NY 10023. (212) 245-2727. $10,000.*

Computer graphics has been added to the company's LOCOST automated test systems. The graphics software uses pictures and alphanumeric display to direct the interconnection of cables and equipment; identify and direct the adjustment of internal controls; identify and direct the use of each panel control; describe in English any necessary keyboard action; and explain when and how to make any pertinent observations. The system uses alphanumerics and line art—including simplified three-dimensional drawings and flashing graphics elements—to show the operator what to do next.

CIRCLE NO. 321

## Laser beam modulated by acoustic signal

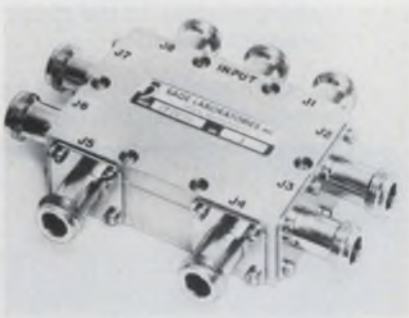


*Thomson-CSF Electron Tubes, 750 Bloomfield Ave., Clifton, NJ 07015. (201) 779-1004. $4325; 20 wks.*

What your microfiche or optical memory system needs is an opto-acoustic deflector and modulator. These devices use the optical interference between an acoustic wave and a laser beam on a lead-molybdate substrate. The result is a frequency-modulated light beam, which is also deflected in proportion to the acoustic frequency. Modulation efficiency up to 90% in the 150-to-300-MHz band has been attained.

CIRCLE NO. 322

## Divide your power and conquer

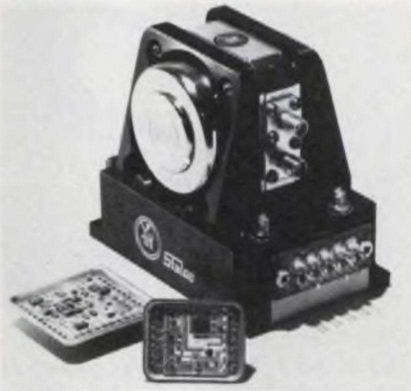


*Sage Laboratories, 3 Huron Dr., Natick, MA 01760. (617) 653-0844. $225; 45 days.*

If your problem is to divide 3.7- to 4.2-GHz power eight ways, you can conquer with the Model FP-2036. It features isolation of 25 dB min (30 dB typ), insertion loss of 0.6 dB max (0.4 dB typ) and unbalance of 0.25 dB max. The unit can handle 1 W, and is equipped with type N female receptacles.

CIRCLE NO. 323

## Track with a Staloc! A what?

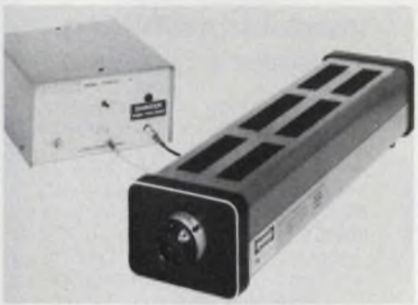


*Yig-Tek Corp., 1725 De La Cruz Blvd., Santa Clara, CA 95050. (408) 244-3240. From $2400; 120 days.*

A self-tracking automatic lock-on circuit, that's what. The Model L183 automatically centers any YIG bandpass or band-reject filter at the desired frequency differential from a cw reference, over the 2-to-18-GHz range. The new technique is similar to a phase-lock loop, and can be used for preselectors or remote tuning up to decade ranges. YIG driver and loop circuits are included. Drivers are also available separately for $400, 60 day delivery.

**CIRCLE NO. 324**

## HeCd laser radiates deep blue yonder



*Liconix, 1400 Stierlin Rd., Mountain View, CA 94043. (415) 964-3062. $3000; 30 days.*

The deep blue, 442-nm, light of the Model 4110 HeCd laser is ideally matched to silver-halide films and photoconducting materials. This lower-priced version of the 4100 lacks feedback control, but has extended tube life and very good environmental stability. A number of options are available. Inquire for volume discounts.

**CIRCLE NO. 325**

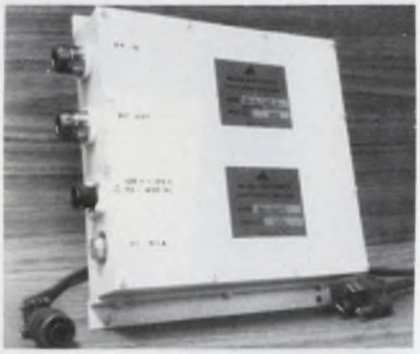
## Low-pass filter handles 15 kW pk

*Sage Laboratories, Inc., 3 Huron Dr., Natick, MA 01760. Tony Cieri (617) 653-0844. $800; 30 to 60 days.*

Can you use a low-pass rf filter with 50-dB min rejection from 1.28 to 11.0 GHz? The Model FF1922 measures 7/8 × 14-1/2 in., including HN connectors. It handles power levels of 15 kW pk, 500 W av in the transmission bands of 1026.5 to 1033.5 and 1085 to 1095 MHz. Passband VSWR is 1.25 max. Maximum insertion loss is 0.5 dB in the lower and 1 dB in the higher channel.

**CIRCLE NO. 326**

## Telemetry preamp for L-band sports 2.5-dB NF

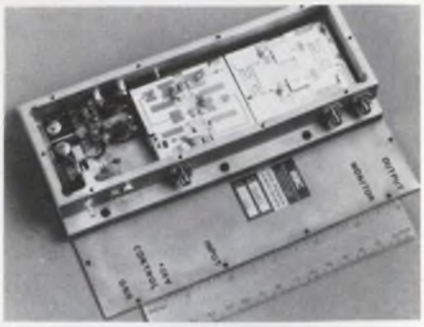


*Mu-Del Electronics, 2426 Linden Lane, Silver Spring, MD 20910. Irv Kuzminsky (301) 587-6087. $1095; 60 days.*

Packaged for an outdoor environment, the Model MDA-1415E consists of a low-noise solid-state preamplifier with a low-loss combline preselector bandpass, and a power supply. In the 1435-to-1540-MHz range it provides 29-dB gain with a 2.5-dB noise figure. Output is 10 dBm, and the unit measures 7 × 7 × 2 in. Higher gain and other frequencies are available.

**CIRCLE NO. 327**

## L-band Xistor amplifier gives 45 W swimmingly



*Microwave Semiconductor Corp., 100 School House Rd., Somerset, NJ 08873. Richard B. Moffet (201) 469-3311. See text; 90 days.*

For your seaworthy houseboat, the Model MSC91045 amplifier can provide communications via the Marisat system. With 45-W min (cw) from 1.62 to 1.66 GHz, the AM/PM conversion is still under 8°/dB. Small signal gain is 25 dB and over-all efficiency is 35%. The 7.5 × 3.4 × 1-in. unit is designed for marine environments. Price depends on a number of design alternatives.

**CIRCLE NO. 328**

## Flat broadband coupler is small and rugged


*Narda Microwave Corp., Plainview, NY 11803. (516) 433-9000. $175; stock.*

Available in 6 and 10 dB values, the Model 4246 covers 6.5-18 GHz with ±0.3 dB flatness. It uses the patented Narda Multi-Section coupling structure and handles power levels of 50 W cw, 3 kW peak. Operation to 105 C and storage to 125 C without degradation are guaranteed. The precision SMA female connectors mate in compliance with MIL-C-39012.

**CIRCLE NO. 329**

## X-band FET amplifier plugs into 110 V ac

*Aercom Industries, 1050F E. Duane Ave., Sunnyvale, CA 94086. Dick Hassett (408) 736-7600. $3650 (1 to 4); 45 days.*

The Model AT-12001-P offers small-signal gain of 30-dB min from 8 to 12.4 GHz with a noise figure of 7.5-dB max. The 2.65 × 6.1 × 2 in. FET amplifier gives +7-dBm min output, and plugs into 110 V ac, 50 to 400 Hz.

**CIRCLE NO. 330**

## Lightweight dummy load is leakproof

*Coaxial Dynamics, Inc., 12110 Enterprise Ave., Cleveland, OH 44135. (216) 671-3550. $148; stock.*

The Model 4260 dry coaxial load handles 200 W with less than VSWR typ., from dc through 512 MHz. Peak power capability of 1000 W, no need for cooling fluid and a weight of 6 lb make the unit especially suitable for field use.

**CIRCLE NO. 331**

## Gunn source aims at klystron oscillators

*PRD Electronics, 6801 Jericho Tpke., Syosset, NY 11791. Wally Weissman (516) 364-0400. See text; 90 days.*

The Model 917 Gunn oscillator provides 50 mW min of rf power, and is mechanically tunable over the industrial/medical 10.5 ±0.2 GHz band. Together with the Model-821 power-supply modulator, the oscillator serves as a general-purpose signal source, and can be substituted for klystron oscillators. The Model 821 provides 9 to 10 V dc at 900 mA, and an adjustable square-wave signal of 1000 ±100 Hz. The oscillator costs $350; the power supply, $325.

**CIRCLE NO. 332**

POWER SOURCES

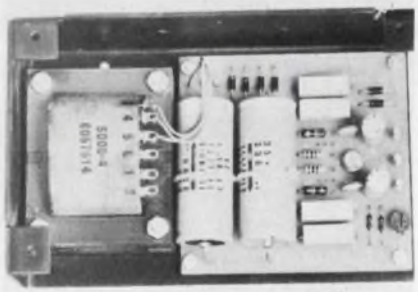
## Broad inverter line has been improved

*Nova Electric, 263 Hillside Ave., Nutley, NJ 07110. Ken Niovitch, (201) 661-3434. From $375; stock.*

The full line of more than 150 Nova inverters boasts three improved key specifications. Frequency regulation, from no-load to full-load is upgraded from 0.25 to 0.15%; voltage regulation, which was ±2% is now ±1%; and distortion has dropped from 6 to 5%. The line of inverters provides outputs of 115, 220 or 240 V ac, at 50, 60 or 400 Hz.

CIRCLE NO. 333

## Bipolar dc supply tracks over 12-15 V



*Century Electronics, 2688 S. La Cienega Blvd., Los Angeles, CA 90034. (213) 870-1083. From $32.95 (100 units).*

Bipolar dc supplies of the LBA series provide automatic tracking with balance errors as low as 1%. Of the over 200 standard models, the 15 LBA-1 is shown. It has 2% max tracking error, and is adjustable from ±12 to ±15 V with a single control. A model with less than 1% tracking error (15LBA-1A) is also available. The tracking supplies are rated for 1-A load current to 50-C ambient without derating. Other specs include 105 to 125 V, 47-to-63-Hz input, ±0.05% line/load regulation, 0.5-mV rms typical output ripple, and a temperature coefficient of ±0.02%/°C.

CIRCLE NO. 334

## Convection cooled UPS is quiet

*Clary Corp., 320 W. Clary Ave., San Gabriel, CA 91776. (213) 287-6111. From $1650.*

The Mini-UPS uninterruptible power system features a solid-state, convection-cooled design that cuts size and weight and eliminates audible noise generated by fans and blowers. The system is immune to input voltage variations of ±15%. Standard models have single-phase outputs and are available in 625-VA, 1.25, 2.5 and 5-kVA ratings. The unit mounts in a standard 19 in. rack or can be supplied in a stand-alone cabinet. A static-bypass switch and battery packs are available as options.

**CIRCLE NO. 335**

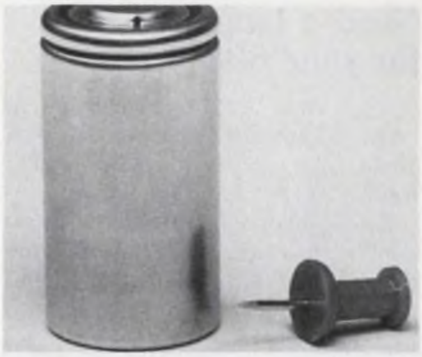
## Strappable switcher spans wide outputs


*Trio Laboratories, 80 Dupont St., Plainview, NY 11803. (516) 681-0400. From $355; stock.*

The 672 features a strappable input of 115 or 208-V nominal at 45 to 400 Hz and delivers 2 to 48 V dc. In this single-output 175-W switching-supply efficiency runs as high as 80% and the MTBF exceeds 40,000 h with only self-cooling. Overvoltage and overload protection are standard features along with remote sensing and adjustable output voltage.

**CIRCLE NO. 336**

## Sub-C cell capacity has been increased



*General Electric, P.O. Box 861, Gainesville, FL 32602. T. Traeger (904) 462-4746. See text; stock to 8 wks.*

The Super sub-C rechargeable cell delivers 1.4 A-h at 1.25 V. This addition to the company's 1.2 and 1.0-A-h line of sub-C, wound NiCd cells is priced at $1.47 per cell (10,000 qty). The 1.2 and 1.0 A-h units are priced at $1.25 and $1.15 for like quantities. The 1.62-in. high sub-C's have 0.875-in. diameters.

**CIRCLE NO. 337**

## Need a language tutor for your 8080 μP?

*muPro Inc., 424 Oakmead Parkway,, Sunyyvale, CA 94086. Jim Moon (408) 737-0500. From $975; stock.*

BSAL-80, a block-structured assembly language program for the 8080 family of μPs, is an assembler with a relocating or linking loader. It permits the user to write programs in high-level language syntax while retaining the flexibility and execution speed of assembly code. BSAL 80 comes in 8080-resident or standard Fortran-4 cross-assembler versions. Text manipulation is facilitated by an optional editor with automatic line numbering and a special command set ($275).

CIRCLE NO. 338

## Floppy-disc-storage drive has rugged parts

*Industrial Micro Systems, 633 W. Katella Ave., Orange, CA 92667. (714) 633-0355. $2350 (1-24).*

A floppy-disc-storage drive, the Model 61-0010, has a die-cast cartridge guide and base plate. The drive comes in a fully enclosed, portable or rack-mounted case. The unit stores 3.2 megabits per disc. The controller supports up to three drives. Communication goes through a three-wire, full duplex, 9600-baud communication interface. The signal levels are RS-232 or 20-mA current-loop levels. Power requirements are 115 V ±10% at 1.5 A.

CIRCLE NO. 339

## Spectrum analyzer system comes with mini

*EMR Telemetry Div., Sangamo-Weston, P.O. Box 3041, Sarasota, FL 33578. (813) 371-0811. $19,000.*

The Model 1510 digital real-time spectrum analyzer system comes with a DEC PDP-11/04 minicomputer. The analyzer operates on signals up to 25.6 kHz. The included software package computes octave and 1/3-octave spectrum analysis with ANSI Class III filter characteristics. The Model 1510 also does power-density analysis with automatic gain control. The hardware consists of a spectrum analyzer, computer and teletypewriter.

CIRCLE NO. 340

## Bug-killer offered for IBM System/3 programs

*Informatics Inc., 21031 Ventura Blvd., Woodland Hills, CA 91364. Janet Wharton (213) 887-9040. $199; stock.*

Called XREF, this enhancement program for Models 4, 6, 8, or 10 of the IBM System/3 generates an alphabetical list of field names, file names and indicators during compilation. XREF is completely compatible with Auto Report, Total, and other RPG software enhancements, and even runs on systems that use only disc source libraries.

CIRCLE NO. 341

## Self-sharpening cleaner picks up debris and bugs

*Data Devices International, 6301 De Soto Ave., Woodland Hills, CA 91364. Warren Sproul (213) 884-5500. From $9295; 8 wks.*

With the Century 22 automatic cleaner/evaluator you can remove loose oxide and debris from 1/2-in. mag tape (IBM hub) and check it for errors at the same time. Cleaning is accomplished with a self-sharpening, rotating cylinder and two self-sharpening grids, at speeds up to 360 in/s (forward or reverse). An interlock provides fail-safe operation. The head is guaranteed for 2000 h or 1 yr.

**CIRCLE NO. 342**

## Hard-disc drives operate with floppies

*Data General, Southboro, MA 01772. (617) 485-9100. See text.*

A series of cartridge-disc systems can be mixed with flexible-disc drives supervised by one controller. The series consists of Models 6045 (10 Mbyte), 6046 (20 Mbyte), 6047 (30 Mbyte) and 6048 (40 Mbyte). The Model 6045 consisting of cartridge-disc drive, integrated power supply, controller and cabling costs $9950. The unit needs a rack height of 10.5 in.

**CIRCLE NO. 343**

## Now you see the keyboard—now you don't

*Applied Digital Data Systems, 100 Marcus Blvd., Hauppauge, NY 11787. (516) 231-5400. $25 premium.*

If you need a CRT display terminal with a movable keyboard, the D-option of the Consul series provides this flexibility. Separation from the screen up to 2 ft is possible. Yet, when attached, the D-option adds only 1 in. to the depth of the standard TTY-compatible Consul terminals (Models 520, 580, 920 and 980.)

**CIRCLE NO. 344**

## Disc-memory system connects to minis

*Data Systems Design Inc., 1122 University Ave., Berkeley, CA 94702. (415) 849-1102. $2795-up; 2-4 wk.*

The DSD-210 diskette-memory system works with DEC's PDP-8 PDP-11 and LSI-11 minicomputers. The system is compatible with DEC's instruction set and IBM's 3740 disc-recording format. An 8-bit bipolar μP controls all data transfers, monitors read/write head positionings, and performs data-error checks. A self-test microcode verifies the system. The DSD-210 comes with single, double, or triple diskette drives.

**CIRCLE NO. 345**

## Digital cassette unit features remote control


*Techtran Industries, Inc., 580 Jefferson Rd., Rochester, NY 14623. (716) 271-7953. $950 (single qty); 45 days.*

The Model 815 digital cassette recorder features remote control of read, write, rewind, fast-forward and edit functions. It also has switch-selectable data rates of 110 and 300 baud, dual RS-232C plug-in interfaces, and a 20-mA terminal interface. The unit stores 145,000 characters on one Philips-style cassette. The 815 weighs 6 lb and measures 5 × 7.25 × 11 in.

**CIRCLE NO. 346**

## Portable terminals speak ASCII and APL


*Computer Devices, Inc., 9 Ray Ave., P.O. Box 421, Burlington, MA 01803. K. Stofer (617) 273-1550. From $1635 (see text).*

As an extra-cost option, the APL character set is available on several Miniterm models, in addition to the normal upper/lower case ASCII and numerics. Prices range from $1635 ($87 per month, if leased) for the read-only Model 1201, to $2435 ($135 per month) for the portable time-sharing terminal, Model 1203, with built-in coupler.

**CIRCLE NO. 347**

## Paper tape reader has only one moving part


*Facit-Addo, Inc., 66 Field Point Rd., Greenwich, CT 06830. Odd Bjerkmann (203) 622-9150. $325 (unit qty); stock.*

The Model-4030 paper-tape reader combines a small read-head with a simple design: only one part moves. With LED light sources the head handles up to 60% tape transmissivity. The basic unit contains control electronics, and is also available in a two-module (3-1/2 in.) rack panel. Another option includes a power supply and parallel SP-1 interface.

**CIRCLE NO. 348**

## Drum memory beats other drums' price

*Vermont Research, Precision Park, North Springfield, VT 05150. Evered W. Hinkley (802) 886-2256.*

Reduced cost and small size (12-1/4-in. high in a 19-in. rack) are the main attractions of the Model-4016 fixed-head drum memory. In addition to 4.2 megabytes of storage and 8.5-ms access time, the drum features speed detection and noncontact start/stop heads. All electronic circuits are external to the media enclosure. A wide choice of controllers is available.

**CIRCLE NO. 349**

PACKAGING & MATERIALS

## Spread your gold ink down to 0.0003 in.

*Engelhard Industries, Electro Metallics Dept., 1 Central Ave., East Newark, NJ 07029. Sanford Cole (201) 589-5000. From $150/oz; 2 wks.*

Four new gold inks, designated A2763, A3319, A3360 and A3362, yield a fired thickness of only 0.3 mil, thus covering up to 375 square inches per oz. The new inks also permit well-defined metallizing widths of 5 to 10 mils, as a result of their high-shear flow characteristics. The four inks differ only in printing and firing requirements, and some secondary final properties. Price depends on quantity and, of course, the gold price.

**CIRCLE NO. 350**

## SMA feedthrough has uniform impedance

*Cablewave Systems Inc., 60 Dodge Ave., North Haven, CT 06473. (203) 239-3311. $6.27 (500-up); stock.*

The SMA bulkhead feedthrough adaptor, type 705627-101, has a uniform impedance of 50 Ω throughout its length. The solder-in glass seal has the same impedance as the rest of the connector. This contrasts with other connectors that have a glass seal of about 44 Ω. The hermetic unit has a leak rate of $1 \times 10^{-8}$ cc/s at 1 atm. The center pin of the connector is attached to the glass seal by welding. The hermetic SMA bulkhead feedthrough adaptor has a max VSWR of 1.25:1, from 2 to 18 GHz. Both connector ends have female matings.

**CIRCLE NO. 351**

## Tool kit comes in small-sized case

*Specialized Products Co., 2324 Shorecrest, Dallas, TX 75235. (214) 358-4663. $77 (single qty).*

The Model SPC-199 contains more than 40 tools mounted in a simulated-leather black-zippered case measuring 11.5 × 10 in. The tools include several varieties of screwdrivers, nut drivers, wrenches, pliers, files, instrument oilers and alignment tools. Also included is a soldering iron.

**CIRCLE NO. 352**

## Conductive-plastic tray prevents static

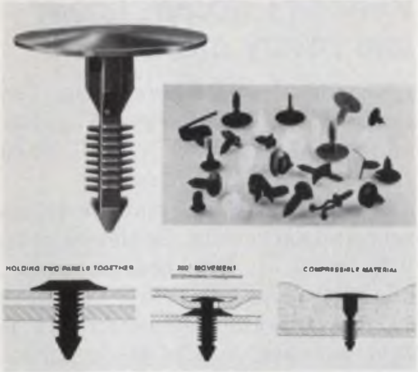
*Wescorp, 1601 Stierlin Rd., Mountain View, CA 94040. (415) 969-7717. $10 (1-24); 3 wk.*

A plastic parts tray, Model W5024-3, protects microcircuits from static electricity during a manufacturing operation. Called SCAT, for a sectioned, conductive anti-static parts tray, it is curved to fit a "lazy Susan" parts table. The tray has an outer semicircular length of 18 in. The inner length is 9 in. It is divided into three equal-sized compartments. The tray is made of opaque polystyrene mixed with graphite and is black in color.

**CIRCLE NO. 353**



## Christmas tree replaces screws?



*Illinois Tool Works, Inc., Fastex Div., 195 Algonquin Rd., Des Plaines, IL 60016. LeRoy Rysell (312) 299-2222. See text; stock.*

The versatile "Christmas tree clips" have molded flexible ribs that deflect as the clip is pressed into a hole, and spring back on the other side of the panel. These fasteners come in a wide range of sizes and shapes, for insertion in hard as well as pliable materials, and just about any kind of hole. Price depends on the specific model.

**CIRCLE NO. 354**

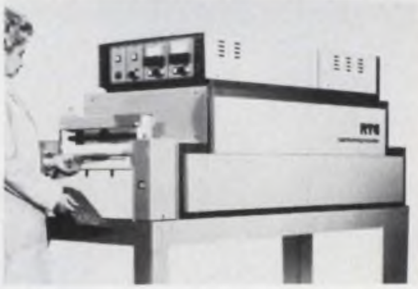
## Backplane holds twice the cards for LSI-11

*MDB Systems, Inc., 1995 N. Batavia St., Orange, CA 92665. (714) 998-6900. $295; 14 days.*

A backplane assembly holds twice as many cards as the version from DEC, for its LSI-11 μC. The backplane holds eight quad modules or 16 dual modules. The unit has 10 power-supply terminal posts. It also has full-length card guides and a prewired multilayer PC-backplane board.

**CIRCLE NO. 355**

## Radiant solder system outshines other units



*Radiant Technology Corp., 13906 Bettencourt St., Cerritos, CA 90701. Joe Romance (213) 926-6518. $6000.*

If you work with printed-circuit boards, but have no access to a large soldering machine, the Model F750 infrared solder system may be your answer. It fits on a table top and is relatively inexpensive, yet completely automates the process of fusing tin-lead to the copper conductors of printed-circuit boards, with widths up to 15 in. The operator simply places the prefluxed board on the conveyor at one end, and picks up the finished product at the other end.

**CIRCLE NO. 356**

## Bearings accept linear and rotary motion

*Linear-Rotary Bearings, Inc., 99 Urban Ave., Westbury, NY 11590. (516) 333-6678. 1-9 prices: $5.05 (LR-4) to $217 (LR-64).*

The LR series of rotary bearings accepts shafts with diameters from 0.25 to 4.0 in. The bearing design allows the shaft to rotate and move in the direction of length. It is said to have a life of 10-million inches of relative motion, compared to competitive models' life of 2 to 4-million in. The Model LR-4 can accept a 0.25-in-dia. shaft rotating at 3600 rev/min with a 14-lb load.

**CIRCLE NO. 357**

## A series of plastics conduct electricity

*Emerson & Cuming, Inc., 809 Washington St., Canton, MA 02021. (617) 828-3300. Sheets: $84-$239, bars: $8.40-$30.00.*

A series of five plastics, called Eccosorb HF, has a volume resistivity ranging from $10^3$ to $10^7$ Ω-cm. The plastics come in sheets measuring up to 12 × 12 × 1 in. Or they come in bars with cross-sections measuring up to 1 × 1 × 12 in. They can be used at frequencies from dc through microwave.

**CIRCLE NO. 358**

## Silicone tubing shrinks on exposure to air

*Insulation Systems Inc., 1233 Reamwood Ave., Sunnyvale, CA 94086. (401) 734-5190. See text.*

A line of silicone tubing, called No Heat, shrinks down when it is exposed to air. The tubing comes packaged in air-tight pouches or cans, and will start to shrink 5 min after exposure. It reaches its final diameter in 30 min. The silicone tubing is nonflammable and has a continuous operating range of −75 C to +175 C. The tubing is available with shrunk inside diameters of 0.062 to 1 in. One type, which costs $1.89/ft (500-up), shrinks to an inside diameter of 0.25 in.

**CIRCLE NO. 359**

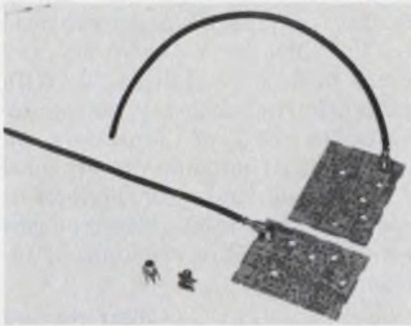
## Inexpensive fixture speeds PC assembly

*Cir-Pax Systems, 11535 Leo Rd., Fort Wayne, IN 46825. Andrew S. Gall (219) 627-3607. From $49.50; stock-2 wks.*

For prototype IC systems, this compact work station not only keeps your desk or bench neat, it speeds up assembly, too. The terminals provided fit holes with diameters of 0.055, 0.073, and 0.093 in. and the gripping fingers of the terminals hold component leads in the proper position. The assembly can then be turned over, and either hand or flow-soldered.

**CIRCLE NO. 360**

## Inexpensive connector snaps into PC boards



*Connector Corp., 6025 N. Keystone Ave., Chicago, IL 60646. Bill Paradise (312) 539-3108. 10¢ (small qty); stock to 5 wks.*

The Model 107E65-4 rf/audio connector snaps instantly into PC boards, and allows both parallel and right-angle connection. The clever design of the 107E65-4 prevents flux or solder from entering the contact area, and provides rigid mounting with three lugs. The connector protrudes less than 1/2 in. above the board.

**CIRCLE NO. 361**

## Neat epoxy adhesive sticks—up to 190 C


*Tra-Con, Inc., 55 North St., Medford, MA 02155. (617) 391-5550. From $25; 1 wk.*

Tra-Bond 2248 is a high temperature epoxy adhesive for bonding and staking applications. It comes in pre-dispensed "Bipax" packages that end the mess of mixing two-component systems. The dark brown, 100%-solids epoxy bonds to metal, glass, ceramics and plastics. After curing at elevated temperatures, the 2248 resists water and many solvents, and retains its mechanical and electrical properties up to 190 C.

**CIRCLE NO. 362**

MODULES & SUBASSEMBLIES

## True-rms converter handles dc to 2 MHz

*National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. Brent Welling (408) 737-5000. From $22.50; stock to 6 wks.*

The LH0091, a true-rms converter, computes the root-mean-square value of virtually any combination of ac or dc input signal from dc to 2 MHz. Performance is guaranteed to better than 0.2% accuracy to 30 kHz, with crest factors as high as 5. The frequency can be extended to 200 kHz for 1% accuracy and crest factors as high as 10. With external trim, accuracy can be adjusted to 0.05% of the reading. An uncommitted amplifier is provided for filtering, gain, or high-crest-factor configuration. The true-rms converter comes in two kinds of 16-lead DIPs.

**CIRCLE NO. 363**



## Accelerometers cover wide range


*Schaevitz Engineering, P.O. Box 505, Camden, NJ 08101. (609) 662-8000. From $539; stock.*

Five models of ASB-series closed-loop-servo angular accelerometers measure from ±50 rad/s² to ±1500 rad/s² full scale, with linearity to ±0.1% of full scale, hysteresis to ±0.02% of full scale, and resolution to ±0.0005% of full scale. These units are intended for measuring angular acceleration of roll, pitch or yaw in aircraft or aerospace control systems. They operate from standard dc supply voltage. Available options are 0.2-to-4.8-V telemetry output, and output-to-input isolation. An output-bias option permits operation around a nonzero level. Other output variations are: unipolar, limiting, bipolar (with single supply voltage) and low-impedance. These devices are 2.6 × 1.1 × 1.68 in.

**CIRCLE NO. 364**

## Set relay's delay with thumbwheels

*International Microtronics, 4018 E. Tennessee St., Tucson, AZ 85714. Dr. Otto Fest (802) 748-7900. $79; stock-to-4 wks.*

You set this solid-state time-delay relay with direct-reading thumbwheel switches. Series 280 Digilay times on-or-off delay modes from 1 ms to 999 s with accuracy and repeatability of ±0.5%. Power turn-on time is 30 ms and power-recycle time is 10 ms. An external frequency-modulation feature permits fine tuning of the oscillator's base frequency, or you can modulate the time delay with an external waveform. SPDT-relay, SPDT-reed-relay, and SPDT-triac options provide switching times ranging from 10 μs to 1 ms. The device operates from 12-V ±10% input power.

**CIRCLE NO. 365**

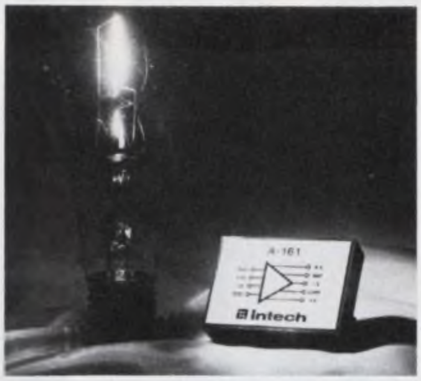
## Video sample-and-hold works faster

*ILC Data Device, Airport International Plaza, Bohemia, NY 11716. (516) 567-5600. From $395; stock.*

The Model VADC-150 is the fastest video sample-and-hold unit available. It features a 100-MHz small-signal bandwidth, 500-V/$\mu$s slew rate and 20-MHz sample rate and is intended for video a/d and pulse processing. The module's acquisition time can vary from 12 to 25 ns, depending on signal change; apterture time or aperture jitter is $\pm 60$ ps. The VADC-150 is a system-oriented modular device that provides TTL-compatible control inputs and a FET input impedance for video. Feedthrough attenuation is 50 dB at 10 MHz, linearity is 0.1% and the drift rate is 0.2 mV/$\mu$s. The unit meets the requirements of MIL-STD-202D. The modules are offered in two types, each having its own temperature range, the VADC-150-1 for $-55$ to $+85$ C, and the VADC-150-3 for 0 to $+70$ C.

**CIRCLE NO. 366**

## FET op amp delivers high output




*Intech/FMI, 282 Brokaw Rd., Santa Clara, CA 95050. (408) 244-0500. $95 (1-29); stock to 4 wks.*

FET inputs and a rated output of $\pm 35$ V at 150 mA are features of the A-161 modular op amp. It also boasts a min slew rate of 15 V/$\mu$s and bias current of less than 20 pA. The unit operates over a supply range from $\pm 12$ to $\pm 40$ V. In addition, the amplifier, connected as a unity-gain follower, can operate into a capacitive load of up to 1000 pF.

**CIRCLE NO. 367**

## Control small motors without spiking

*G.K. Heller, 7 Mayflower Pl., Floral Park, NY 11001. (516) 775-7170. $62 (singles); 3 to 4 wks.*

The TSX controller maintains the preset-speed of 1/40-HP permanent-magnet or shunt-wound dc motors with power transistors instead of triacs and SCRs. Therefore, you can use this controller close to sensitive electronic equipment without causing rf interference. The unit provides speed regulation within 1% for fluctuations in torque within the motor's rated limits, or variations in ac-line voltage from 100 to 130 V. The device is said to give you a wider range of smooth rotational-speeds than can be attained with SCR controllers. Standard features include full-wave field-voltage supply, full-wave-filtered armature supply, protection against transient voltages on both the input line and the dc output, a line-voltage correction circuit, and trimming adjustments for max and min speeds.

**CIRCLE NO. 368**

# How to get high

HIGH VOLTAGE

HIGH SPEED

HIGH CURRENT

HIGH PERFORMANCE

## Signetics' high technology products fit all markets.

We have a lot of things to talk about. From our broad line of analog products available to fill consumer, data processing, instrumentation and communication requirements—including new products, exclusive products, interface products, industrial products, military products, you name it. Right down to our special applications assistance which includes detailed literature and our experienced engineering staff that's always on-call to help you on a one-to-one basis.

Then there are the specific benefits offered by our analog products. In fact, when you see the high voltage, high current, high speed and high performance... you'll see why Signetics is "high on analog."

And, see how easy it is for you to take advantage of all the benefits for yourself.

So where do we begin?

**High voltage.** Just for example, there's the Signetics NE541 Class AB monolithic power driver that offers an operation up to 80 volts, low standby current, and a wide power bandwidth. Perfect for driving large audio output stages and similar applications. Signetics has many other analog products rated at high voltages to meet your latest requirements.

**High speed.** Signetics analog devices act faster to provide better performance when computer logic

# on analog.

| DIGIT DRIVERS (NE584 & 585) | POWER AMPLIFIER (NE541) | DIGITAL PHASE LOCKED LOOP (NE564) | DUAL COMPARATORS (NE521 & 522) | SERVO-AMPLIFIER (NE544) | HIGH VOLTAGE REGULATOR (78HV) | OP-AMPS (SE & NE535) | MULTIPLEXER (SD5301) | QUAD-TIMERS (SE & NE558 & 559) | COMPRESSOR/ EXPANDERS (NE570 & 571) |
|---|---|---|---|---|---|---|---|---|---|
| yes | yes | | | | yes | | | | |
| | | yes | yes | | | yes | | | |
| | yes | | | yes | yes | | | yes | |
| yes | yes | yes | yes | yes | yes | yes | yes | yes | yes |

and memory function faster with low signal levels. Signetics sense amps, dual comparators and other products turn on and off faster. Perfect for data recording and communication applications.

**High current.** Examine the NE544 servo-amplifier that is a linear one-shot, all purpose servo driver with all functions integrated into one, and you will see it is truly unequalled. You'll also see why Signetics is "high on current."

**High performance.** There's a whole list of high performance analog products available from Signetics. Multiplexers, quad-timers, compressor/ expanders, operational amps. They feature low input offset voltage, low input bias current, TTL compatibility, all logic on a single chip, economy, everything to make designing easier.

The more you know about analog, the higher you get on it. Don't wait. Start now by mailing the coupon.

**Attach this to your letterhead for fast response.**

☐ Send me the complete analog information and fact sheets.
☐ Have a Field Applications Engineer call me for a one-to-one appointment.

My application is ______________________

Name ______________ Title ______________

Telephone ______________ Mail Stop ______________

THINK Signetics

811 E. Arques Ave., Sunnyvale, Ca. 94086

 A subsidiary of U.S. Philips Corporation

CIRCLE NUMBER 86

## Amp lets you select gain and bandwidth

*Preston Scientific, Inc., 805 E. Cerritos Ave., Anaheim, CA 92805. (714) 776-6400. See text; stock to 30 days.*

Gain of the DX-series Model-A instrumentation amplifier can be set at any of seven levels by a front-panel rotary switch. Fixed gains of 10, 20, 50, 100, 200, 500 and 1000 are standard. A continuous fine-control lets you adjust gain-settings between selector levels, with a gain of 3000 max. A six-position front-panel switch lets you select bandwidths of 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz or "wideband." A critically damped 12-dB/octave filter determines the frequency response. In small quantities, the amplifier is priced at $295. Dual outputs (one filtered, one unfiltered) are optional at $35. The amplifier boasts the following characteristics: 0.05% accuracy; 0.005% linearity; 1 $\mu$V max one-sigma input noise. Tempco over the 0-to-50-C range is 1 $\mu$V referred to the input; 30-day stability is $\pm 3$ $\mu$V referred to input and $\pm 100$ $\mu$V referred to the output. Additional specifications include: output amplitude of $\pm 5$ or $\pm 10$ V with 100-mA max current on both ranges; output impedance of 1 $\Omega$; common-mode rejection (at 1000 gain) of 130 dB at dc, 120 dB at 60 Hz and 60 dB at 60 kHz; common-mode voltage of 10-V pk; slew rate of 1 V/$\mu$s; and settling time to $\pm 0.01\%$ of final value of 50 $\mu$s.

CIRCLE NO. 369

## Data-acquisition unit needs no baby sitter

*CSP, 209 Middlesex Tpk., Burlington, MA 01803. (617) 272-6020. From $4000; 120 days.*

Series-500 Analog Data Acquisition Modules (ADAMs) provide for crystal-controlled sampling (4.8 MHz) and processing of up to eight analog signals, without supervision from a host computer. All of the hardware (including up to eight sample-holds) and software necessary to accomplish data-acquisition and a/d conversion are incorporated within the ADAM. These modules digitize input signals into a normalized 16-bit floating-point format using the company's MAP's SNAP II Fortran-compatible language. Processing rate for standard units is 125 kHz with 12-bit resolution, while a higher-speed model offers a 250-kHz digitization rate with 10-bit resolution.

CIRCLE NO. 370

## Stable oscillator takes the punches

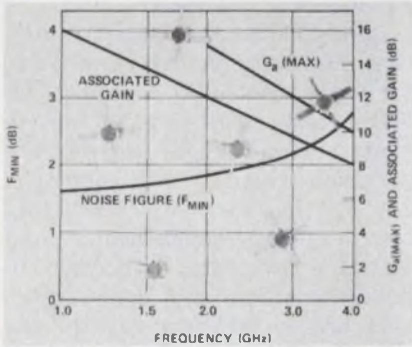
*Frequency & Time Systems, 182 Conant St., Danvers, MA 10923. (617) 777-1255. $2400 (1 up) stock.*

The Model 1000 quartz-crystal oscillator gives you stability: better than $1 \times 10^{-12}$ for averaging times of 1 to 1000 s, and better than $1 \times 10^{-10}$ per day for 30-day averaging. It boasts ruggedness: meeting MIL-STD-810C, method 514.2, for ground-launched missiles, cat.E, proc.4 and withstanding random vibration of 23.9 g rms from 20 to 2 kHz and peak-shock with a pyrotechnic spectrum of 2300 g at 1850 Hz. The unit has spectral purity: less than 118 dB of phase noise 1-Hz from the 5-MHz output. The oscillator's spectral purity and stability point to its use as a stand-alone basic-frequency source for multiplication up through the millimeter band. Modules can be specially ordered with lower phase noise, up to four TTL-compatible outputs and with output frequencies other than 5 MHz. Radiation hardened models are available. The 3 × 3 × 6.9 in. unit weighs 1.9 lb.

CIRCLE NO. 371

DISCRETE SEMICONDUCTORS

## Microwave transistors deliver low noise




*Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. (415) 493-1501. $49: HTXR-5103, $105: HTXR-6104 (10-24); stock.*

Two silicon bipolar transistors are suitable for low-noise amplifiers in the 1-to-4-GHz range. Model HXTR-6103, with a 2.2-dB (max) noise figure at 2 GHz and a 110 dB (min) associated gain, can replace the Fairchild FMT 4005. Model HXTR-6104 has a 1.6-dB (max) noise figure at 1.5 GHz and associated gain of 13 dB (min). Both devices are manufactured with ion-implantation techniques and titanium-platinum-gold metallization. Packaged in the hermetic HPAC-100 metal/ceramic packages, both devices can meet the requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

CIRCLE NO. 372

## Pnp power transistor complement of 2N3373

*Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036. (602) 244-3465. $2.59 (100-999); stock.*

A pnp power transistor, the 2N6609, rated at 16-A continuous maximum collector current and a $V_{CEO}$ of 140 V dc minimum, is a complement to the popular 2N3373 npn. The transistor features a dc safe operating area of 1.5 A at a $V_{CE}$ of 100 V. This 150-W capability is over three-times greater than the power-dissipation capabilities of earlier 16-A, 140-V pnp's. This performance has been achieved by including base ballasting with Motorola's standard epitaxial-base process.

CIRCLE NO. 373

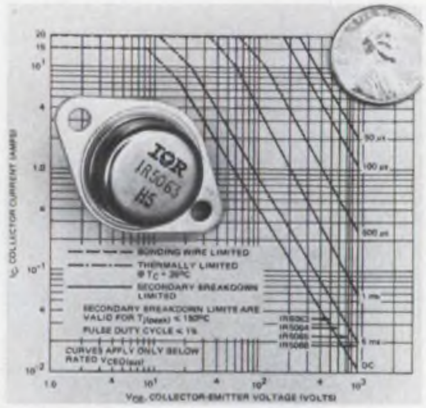
## LED numerical displays 0.5 and 0.3-in. high

*Spectronics Inc., 830 E. Arapaho Rd., Richardson, TX 75080. (214) 234-4271. $1.25: SPX-300, $1.45: SPX-500 (1000 up); 30 days.*

Two series of red, seven-segment LED displays feature 0.3-in. high (SPX-300) and 0.5-in. high (SPX-500) characters. The new devices offer wide viewing angles, continuous uniform segments and high contrast. And they are categorized for uniformity of luminous intensity. They are available in both common-cathode and common-anode configurations.

CIRCLE NO. 374

## Power Darlingtons rated to 1000 V at 125 W



*International Rectifier, 233 Kansas St., El Segundo, CA 90245. (213) 322-3331. $11.75 to $18 (100-999); stock.*

Very high-voltage monolithic Darlingtons with power ratings to 125 W, designated the IR5063 through IR5066 series, have collector-to-base ratings to 1000 V and collector-to-emitter ratings to 900 V. Peak collector current for all units in the line is 20 A. Hard-glass passivation of the silicon chip provides exceptional stability at high operating junction temperatures. Processing is triple diffused for high voltage with a wide safe operating area and fast switching. Small-signal current gain for all the Darlingtons is 8 at 0.5 A, 10 V. Thermal resistance, junction-to-case, is 1 C/W. Maximum power dissipation for all units is 125 W. Packaging is in a standard JEDEC TO-3 case.

CIRCLE NO. 375

## Snap-action thermostats sealed hermetically

*Protective Controls Inc., Husky Park, Frederick, MD 21701. (301) 663-5141. $6 to $6.50 (OEM qty); 2 to 8 wks.*

Series 5100 thermostats are hermetically sealed immersion-type snap-action bimetalic disc units. A new single-break switch design gives improved reliability as well as improved shock and vibration characteristics. The devices withstand 20 g's up to 2000 Hz and meet MIL-STD-202, condition D. Ratings are 3 A, 120 V ac; 1.5 A, 240 V ac; or 5 A, 30 V dc—100,000 cycles with SPST single-break (NC or NO) contacts. Quick-disconnect, spade or screw-type terminals are provided. The thermostats are factory calibrated within an operating range of —20 to 350 F.

**CIRCLE NO. 376**

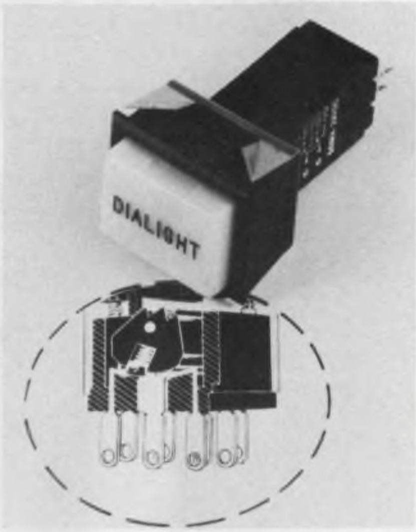
## PB switches assemble with contact blocks

*Alco Electronic Products, Inc., 1551 Osgood St., North Andover, MA 01845. (617) 685-4371. $3.85: operator, $2 to $3.85: blocks (1-9); stock to 6 wks.*

Called the Series 2000, these oil-tight pushbutton control switches mount in 7/8-in. dia panel holes popular in the industry. The switches use Snap-Bloc contact blocks that require no tools to assemble and have UL and CSA ratings of 10 A at 300 V ac nominal (3500 VA make; 360 VA break). Virtually, any combination of NO and NC contact blocks is available.

**CIRCLE NO. 377**

## PB lighted switches wipe gold contacts




*Dialight, 203 Harrison Pl., Brooklyn, NY 11237. (212) 497-7600. $1.65 (1000 up); 2 to 3 wks.*

Wiping-action with gold contacts provides reliable switching at low levels under a wide range of operating environments. The switches are part of Dialight's 554 series of low-cost computer-grade illuminated pushbutton switches and incorporate the same features as the 554 Series snap-action switches. Applications are typically for 1-to-100-mA (resistive) switched current at 1 to 30 V dc. A choice of momentary or tease-proof alternate action with SPDT or DPDT arrangement and solder-blade, quick-connect or PC-board terminals is available. T-1-3/4 incandescent lamps are used.

**CIRCLE NO. 378**

## Miniature crystals operate at 2 to 3 MHz

*Valtec, 75 S. St., Hopkinton, MA 01748. (617) 435-6831. $3.50 to $15; 6 to 10 wks.*

A series of miniature quartz crystals, the VM6 series, can operate in the 2-to-3-MHz range with a typical series resistance of under 200 Ω. The crystals are packaged in an HC-18/U holder with maximum dimensions of 0.53 × 0.435 × 0.183 in. This construction, previously only used for high-frequency crystals, permits use of the crystals in high-density mounting on PC boards.

**CIRCLE NO. 379**

# Application Notes

## Spectrum analysis

"Notes on Spectrum Analysis" discusses the important design and operational features concerning the use of all spectrum analyzers. A simple-to-follow question-and-answer format is used. Ailtech, Farmingdale, NY

CIRCLE NO. 380

## Optically coupled isolators

How isolators can be applied in circuits using thermocouples and transducers in equipment for patient monitoring, adaptive control systems and high-voltage current monitoring is covered in a four-page application note. Hewlett-Packard, Palo Alto, CA

CIRCLE NO. 381

## Machine controls

*Machine Controls in the Manufacturing System* discusses effective use of modern machine controls as significant factors in increased production, and describes how computer-numerical-control and programmable-control machines can be applied in automatic manufacturing systems. Allen-Bradley, Milwaukee, WI

CIRCLE NO. 382

## Ultra-isolation transformers

The protection of sensitive electronic equipment from ac line noise and transients is the subject of the *Noise-Suppression Reference Manual for Ultra-Isolation Transformers*. Topaz Electronics, San Diego, CA

CIRCLE NO. 383

## μP/display interface

Techniques for interfacing microprocessors to alphanumeric displays are described in a six-page application note. Burroughs, Electronic Components Div., Plainfield, NJ

CIRCLE NO. 384

## Semiconductor testing

A 16-page semiconductor testing handbook tells what preconditioning and testing can accomplish, the cost and risk factors, and guidelines as to the degree of testing that various ICs require to ensure against system failures. Microelectronic Testing Laboratories, Irvine, CA

**CIRCLE NO. 385**

## Data processing

*An Executive Guide to Dispersed Data Processing* describes in nontechnical language the dispersed processing concept and its signficance for the business executive. The 20-page brochure includes explanatory illustrations of functioning networks. Datapoint, San Antonio, TX

**CIRCLE NO. 386**

## Minicomputers

The advantages of using a minicomputer for small-business applications is described in nontechnical language in a 12-page brochure. Cincinnati Milacron, Lebanon, OH

**CIRCLE NO. 387**

## Surge-suppression circuits

A six-page application note shows how to design surge-suppression circuits to protect thyristors from load-induced faults. Westinghouse Electric, Semiconductor Div., Youngwood, PA

**CIRCLE NO. 388**

## Dry plasma

The use of dry-plasma methods for failure analysis of semiconductor devices is described in an application note. Tegal, Richmond, CA

**CIRCLE NO. 389**

## Reinforced thermoplastics

Wear and friction properties of internally lubricated reinforced thermoplastics for applications involving moving parts are covered in a 20-page study. LNP Corp., Malvern, PA

**CIRCLE NO. 390**

# New Literature


## Semiconductors

Complete data for hybrids and discretes for rf linear applications are covered in a 12-page catalog. It includes specifications, application block diagrams and reliability notes. TRW RF Semiconductors, Lawndale, CA

**CIRCLE NO. 391**

## Software directory

*Datapro Directory of Software* provides current, comprehensive and objectively prepared profiles on thousands of software products and their vendors and applications, along with an extensive survey of software users. Sample pages of the directory are available on request. Datapro Research, Delran, NJ

**CIRCLE NO. 392**

## Semi screening report

The third quarter *Screening Report Summary* on integrated circuits, transistors and diodes includes both a tabulation of detailed data on each lot processed by device type and part number. Continental Testing Laboratories, Fern Park, FL

**CIRCLE NO. 393**

## Data communications

Illustrations and descriptions of data communications products can be found in a six-page brochure. Tele-Dynamics, Fort Washington, PA

**CIRCLE NO. 394**

## Semiconductor packaging

Custom transistor and hybrid requirements are described in a four-page brochure. Transistor Specialtys, Peabody, MA

**CIRCLE NO. 395**

## Antennas

Technical, system design and product information for antenna and transmission line systems are covered in a 128-page catalog. Andrew Corp., Orland Park, IL

**CIRCLE NO. 396**

## Keytops

Included in a 16-page brochure describing keytops is an application guide and many photographs. Key Tronic, Spokane, WA

**CIRCLE NO. 397**

## Circuit boards

Sub-elements for making instant circuit boards, pre-etched general-purpose prototype and wire-wrap socket boards, and PC drafting aids for making circuit-board master artwork are described in a six-page catalog. Circuit-Stik/Centron Engineering, Torrance, CA

**CIRCLE NO. 398**

## Power-supply periodical

A periodical, *WATTS UP AT SCI*, provides information about power-supply concepts, applications and new-product developments. Semiconductor Circuits, Haverhill, MA

**CIRCLE NO. 399**

## Power supplies

Specifications, outline drawings and pricing of single, dual and triple-output miniaturized power supplies are given in a 20-page catalog. Acopian, Easton, PA

**CIRCLE NO. 400**

# Bulletin Board

**Wintek** has scheduled its three-day **"Hands-On Microprocessor Short Course with Take Home Microcomputer"** at nine locations in February and March, 1977. Tuition is $495. Course locations include Boston, Chicago, Dayton, Huntsville, Los Angeles, St. Petersburg Beach, Palo Alto, Philadelphia and Washington, DC.

CIRCLE NO. 401

**Mostek and Fairchild** have announced that **Fairchild's MOS/CCD Products Div. will second-source the Mostek MK 4027,** a 16-pin 4096-bit dynamic RAM, which has an access time of 150 ns.

CIRCLE NO. 402

**Texas Instruments** has lowered prices of **programmable control system components.** The single-unit price of an input module drops from $11 to $10, an output module from $13 to $12 and an interface module from $80 to $70.

CIRCLE NO. 403

Hundreds of **microcomputer programs** are available on paper tape and in listing form through a new expanded user's library announced by the **Microcomputer Systems Div. of Intel.**

CIRCLE NO. 404

**Motorola** is **second-sourcing the 2900 four-bit μP slice family** originated by Advanced Micro Devices.

CIRCLE NO. 405

Users of MSCS, PMS or CMSC network analysis programs for planning and control calculations can now obtain graphic reports (time-scaled networks, Gantt bar-charts and cost/resource graphs) automatically generated by **Systonetics' EZPERT** on a "pay-as-you-use" basis. This service is available throughout the U.S. via the McDonnell Douglas Automation (MCAUTO) computer network.

CIRCLE NO. 406

# Vendors Report

Annual and interim reports can provide much more than financial position information. They often include the first public disclosure of new products, new techniques and new directions of our vendors and customers. Further, they often contain superb analyses of segments of industry that a company serves.

Selected companies with recent reports are listed here with their main electronic products or services. For a copy, circle the indicated number.

**Bunker Ramo.** Information systems; electronic intelligence and ocean surveillance systems; connection and interconnection devices.

CIRCLE NO. 407

**Reynolds Metals.** Aluminum products.

CIRCLE NO. 408

**Control Data Corp.** Computer services.

CIRCLE NO. 409

**Hazeltine.** Electronic display systems; anti-submarine warfare systems; computer terminals and equipment; electronic identification and communications equipment; transportation control systems and color-analysis equipment.

CIRCLE NO. 410

**General Electric.** Products for generation, transmission, distribution, control and use of electricity.

CIRCLE NO. 411

**CTS.** Resistors and resistor networks, switches, microcircuits, quartz crystal products, loudspeakers, metal and plastic specialties.

CIRCLE NO. 412

**Basic Inc.** Refractory materials and chemical and electronic products.

CIRCLE NO. 413

**Burroughs.** Products that record, store, compute, process and communicate data.

CIRCLE NO. 414

# Electronic Design

ELECTRONIC DESIGN's function is:

- To aid progress in the electronics manufacturing industry by promoting good design.
- To give the electronic design engineer concepts and ideas that make his job easier and more productive.
- To provide a central source of timely electronics information.
- To promote communication among members of the electronics engineering community.

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- To refuse any advertisement deemed to be misleading or fraudulent.

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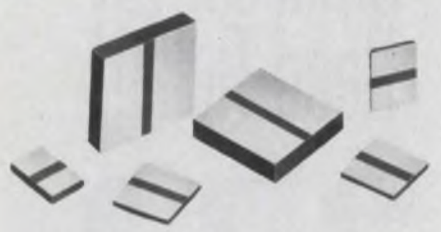
# quick ads

New and current products for the electronic designer presented by their manufacturers.

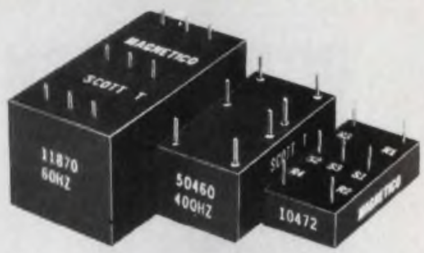


**CERAMIC CHIP CAPACITORS.** SPLIT-CHIP, is a new concept in ceramic chip capacitor technology. These new units have two broad electrodes on one face and eliminate conventional wrap-around end terminations. This new concept provides lower cost and easier assembly. SPLIT-CHIPS are available in five standard sizes from .040" x .030" to .130" x .090" and .015" thick and in all popular dielectrics and capacitance ranges. JOHANSON DIELECTRICS, INC., Box 6456, Burbank, Ca. 91510 213-848-4465

CERAMIC CHIP CAPACITORS **181**

**World's Smallest Displacement Transducer.** Make precision, noncontacting displacement measurements at points never before possible. This new transducer, 0.080" OD, gives accuracy of $<100$ $\mu$in. in a range up to 0.020". Temperature stable. Repeatability and resolution is better than 10 $\mu$in. Price $485, including associated electronics. Kaman Sciences Corporation, P. O. Box 7463, Colorado Springs, CO 80933. (303) 599-1500.

TRANSDUCER **184**




**Scott T Transformer.** 11870: 60HZ, 90v, L-L in. 1.1x2.1x1.1. 50460: 400 HZ, 90v, L-L in. 7/8x1-5/8x11/16. 50642: 400HZ, 11.8v, L-L in. 7/8x5/8-11/16. 10472: 400-HZ, 11.8v, L-L in. 3/4x1-1/2x3/8. All with 6v RMS sine & cosine output. MAGNETICO, INC., 182 Morris Ave., Holtsville, N.Y. 11742 516-654-1166.

TRANSFORMER **187**

**MEMODYNE INCREMENTAL LOW POWER DATA LOGGER Model 2221,** is ideal for remote or unattended collection of sporadic measurements. Features 16 channels, 0 to +10 volt analog input, 12 bit resolution, over 2 megabit capacity per 300 foot cassette. Standby current is less than 50 microamps. Available for line or battery operation. Unit price is $1670.00. Memodyne Corporation, 385 Elliott Street, Newton Upper Falls, Massachusetts, 02164. (617) 527-6600.

LOW POWER DATA LOGGER **182**


**ANTI-STATIC SYSTEMS FOR PRINTERS,** OCR COM and other machines. Static causes rapidly moving paper and film to jam. . . cause arc tracks on undeveloped film. . . attract and hold dust to photographic negatives causing imperfections on printed circuit boards. Numerous products, of interest to both OEM and user, are detailed in new 32 page catalog to solve these problems quickly, reliably and economically. Chapman Anti-Static Div., Portland Co., 58 Fore St., Bx 427, Portland, ME 04112. (207) 773-4726

ANTI-STATIC SYSTEMS **185**

**MAGNETIC SHIELDING** Take advantage of Eagle's 23-year background in shield design and production. Custom and standard models. Full service includes design, engineering, fabrication, heat treating, finishing, testing. Also wide selection of sheet and foil so you can form your own shields. For helpful design and cost data, request Bulletin E-77. Eagle Magnetic Co., Inc., Box 24283, Indianapolis, IN 46224. 317-297-1030.

MAGNETIC SHIELDING **188**

**FLOPPY DRIVE TEAM!** Now, drive motors and stepping motors specifically for flexible disc systems—both from EAD. The drive motor has excellent torque, precise repeatable speeds, 1/100 hp, 1500 rpm @ 50 Hz, 1800 rpm @ 60 Hz. Stepping motors are Size 18 and 20, with single or multiple start lead screw, 3- or 4-phase, 15° per step. Write or call: **Eastern Air Devices,** Holtzer-Cabot motors, Dover N.H. 03820, (603) 742-3330, TWX (510) 297-4454. Syn & Ind Motors • Gear Motors • Fans • Blowers.

DRIVE & STEPPING MOTORS **183**


**VIDEO CHARACTER GENERATOR.** Converts up to 16 parallel BCD digits at TTL levels into video signals for display on monitors or for insertion into a video signal. Fifteen fixed alpha-numeric characters can also be included. Horizontal and vertical positioning controls. Many formats available. Chrono-log Corporation, 2 West Park Road, Havertown, Pa. 19083 (215) 853-1130.

VIDEO DISPLAY GENERATOR **186**

**Free 32 Page Catalog**

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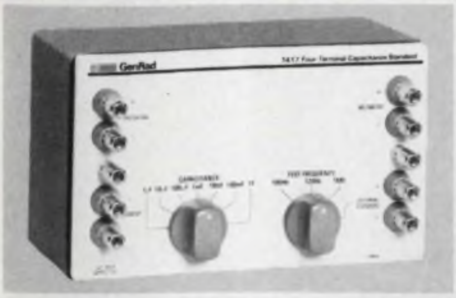
LENSE, PRISM CATALOG **189**

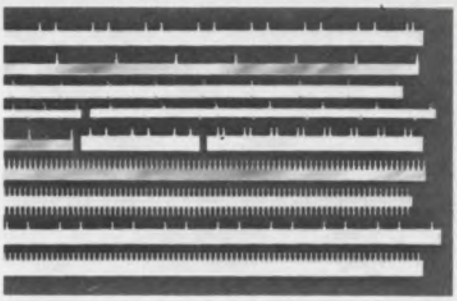



**New Capacitance Standard.** The GR 1417 is a four-terminal capacitance standard with direct reading accuracy of 0.025% at capacitance values of 1, 10 and 100$\mu$F, 1, 10 and 100 mF and 1F. This standard is calibrated for use at frequencies of 100 Hz, 120 Hz and 1 kHz but may be used over a frequency range from below 50 Hz to over 10 kHz. The GR 1417 also acts as a standard for dissipation factor. Gen-Rad, 300 Baker Ave., Concord, MA 01742 (617) 369-8770.

CAPACITANCE STANDARD **190**

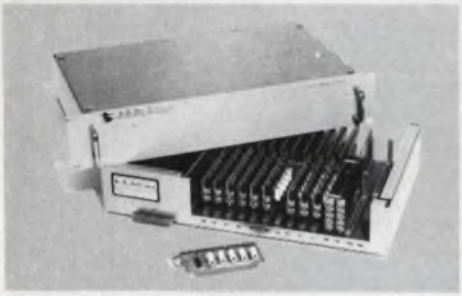

Free New '77 catalog contains over 34,500 quality power supplies from the world's largest manufacturer, Power/Mate Corp. Power Supplies for every application including submodulars, open frame, varirated, encapsulated, laboratory & system. All units UL approved and meet most military and commercial specs for industrial and computer uses. Power/Mate Corp., 514 S. River St., Hackensack, NJ 07601 (201) 343-6294

POWER SUPPLIES **193**



**MINI/BUS® BY ROGERS,** low-cost, low-inductance, high capacitance printed circuit board bus bars for noise reducing voltage distribution, are available in a variety of ready-to-ship designs. Prototype kits are also available from stock. Call or write Mini/Bus product specialist for a complete list. Rogers Corporation, Chandler, AZ 85224. Phone: (602) 963-4584. (EUROPE: Mektron NV, Gent, Belgium; JAPAN: Nippon Mektron, Tokyo.)

BUS BARS **196**



**DATA SWITCHING SYSTEMS** Whether you want a Multiplexer or Matrix to switch Low Level or High Frequency by Manual or Computer control we have a switch to meet your specifications. The systems are built up from a basic control unit into which can be plugged many different switching modules in the configuration you require. IEEE 488 interface available. For further information and a complete solution to your switching problems contact A.D. DATA SYSTEMS INC. P.O. Bx 9209, Rochester, NY 14625 (716) 381-2370

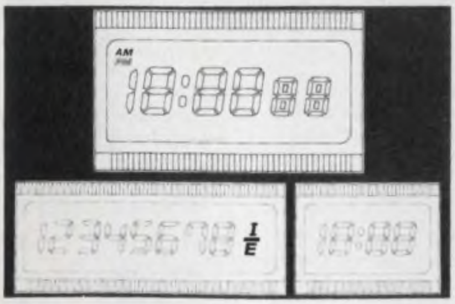
MATRICES **191**


**LOW COST TRIPLE OUTPUT DC-DC CONVERTER FOR MICROPROCESSOR FIELD.** Provides regulated +12V, +5V, and −5V from unregulated 4 to 6V input. Will operate from 4 cells for battery-operated applications. Over 80% efficient. Other outputs also available. Input filtered. Low output noise. 100% burn-in. Optional power strobing. Encapsulated in rigid case. Small (only 3.1" x 2.1" x 0.4"). Scientific Programming, Inc., 1499 Bayshore Hwy., Burlingame, Ca. 94010. (415) 692-1600.

MINIATURE DC POWER SOURCES **194**


**FLUORESCENT PHOTOELECTRICS.** TRAN-BAL INVERTER BALLAST; allows designer to utilize fluorescent lamp for long photoelectric light source by eliminating flicker associated with 60 Hz Operation. Models available for all lamps through 40 watts. Input voltage 12 to 48 v.d.c. The Bodine Co., 236 Mt. Pleasant Road, Collierville, TN (901) 853-7211

FLUORESCENT PHOTOELECTRONICS **197**



**SHARP LIQUID CRYSTAL DISPLAY.** We have a wide range of standard displays and can special design for a low design cost. Quick delivery on all displays. Contact:—Sharp Corporation, Semi Conductor Division, Overseas Marketing, 2613-3, Ichinomoto Tenri, Nara, Japan. Tel: (07436) 5-1321 Telex: 5522364 SHAPEL J

STANDARD/SPECIAL DISPLAYS **192**

**NEW MOTOR CONTROLS COST LESS!** KBGE AC Voltage Controls for motors, heaters and lamp loads. KBGE modules use high reliability triacs. Phase-controlled circuitry is rugged and compact (3" x 2" x 1"). Versatile for power on voltage control; many features. Samples: 120 VAC, \$18.; 240 VAC, \$20. Free data sheet D-162. KB ELECTRONICS, INC., 5801 Foster Ave., Brooklyn, N.Y. 11234 (212) 968-8000.

MOTOR CONTROLS **195**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CIRCUIT BREAKER **198**

# Advertiser's Index



**Advertisers in non-U.S. Edition*

# Product Index

**Information Retrieval Service.** New Products, Evaluation Samples (ES), Design Aids (DA), Application Notes (AN), and New Literature (NL) in this issue are listed here with page and Information Retrieval numbers. Reader requests will be promptly processed by computer and mailed to the manufacturer within three days.



## new literature



## application notes

# eliminate assembly problems & save 60¢ per connector*

## *labor savings attained with the Molex Dualcon™ crimp/snap-in 28 position connector

**The facts** ... A study conducted at a major west coast peripheral manufacturer clearly shows the labor and cost savings between the Molex 4338 crimp/snap-in connector versus a solder eyelet P.C. Connector. The evaluation was made on a fully loaded 28 position dual connector.

| OPERATION | SOLDERING METHOD | MOLEX 4338 CRIMP/STYLE |
|---|---|---|
| STRIP INSULATION | 5:37 | 5:37 |
| SHRINK TUBING ON WIRE | 4:40 | N/A |
| SELECT TERMINAL AND ATTACH WIRE | 10:17 | N/A |
| SOLDER WIRE TO TERMINAL | 3:44 | N/A |
| POSITION SHRINK TUBING | 1:53 | N/A |
| HEAT SHRINK TUBING ON FIRST SIDE | 1:00 | N/A |
| HEAT SHRINK TUBING ON SECOND SIDE | 0:16 | N/A |
| CRIMP WIRE TO TERMINAL* | N/A | 2:12 |
| SELECTIVELY LOAD TERMINAL | N/A | 7:27 |
| **TOTAL OPERATION TIME** | **27:27** | **15:16** |

**Using a $3.00 per hour labor rate ... it costs $1.38 per connector using the soldering method, versus 78¢ per connector, using the Molex crimp/style snap-in. A savings of 60¢ per connector ... or a 44% SAVINGS.**

*Based on 1200 crimps per hour

**The designer and manufacturing engineers answer to eliminating assembly operations, saving time and lowering cost**
**. . . The Molex Dualcon.**

The 4338 Series Dualcon is a new .156 crimp/snap-in dual readout edge connector for .062 P.C. cards. The snap-in type contact allows greater production flexibility and at the same time reduced labor/assembly man-hours **because you use only the contacts you need.**

**Literature and Information** — How much can you save on your present or future application? Ask your Molex Sales Engineer. For more information on the 4338 call or write MOLEX INCORPORATED, 2222 Wellington Court, Lisle, IL 60532. (Phone: 312/969-4550)

**Options:** The 5 Amp rated terminals are available with pre-tin gold over nickel, or selective gold plating and will accommodate 18—24, and 24—30 AWG. Solder loop and split eyelet type terminals are available. Inter-contact and on-contact polarizing keys are optional.

The connector housing is available with or without mounting flanges in 6, 8, 10, 12, 15, 18, 22, 24, 25, and 28 dual row positions.

Application tooling is available for hand termination, semi-automatic bench machines (available on lease or purchase terms) and fully automatic units for extremely high speed production.

molex . . . *Affordable Technology*

CIRCLE NUMBER 263

23 Part I approvals in 13 months . . .

# Acceptance of High Rel COS/MOS is climbing fast.

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| CD4009A | 05501 | CD4021A | 05704 |
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| CD4011A | 05001 | CD4023A | 05003 |
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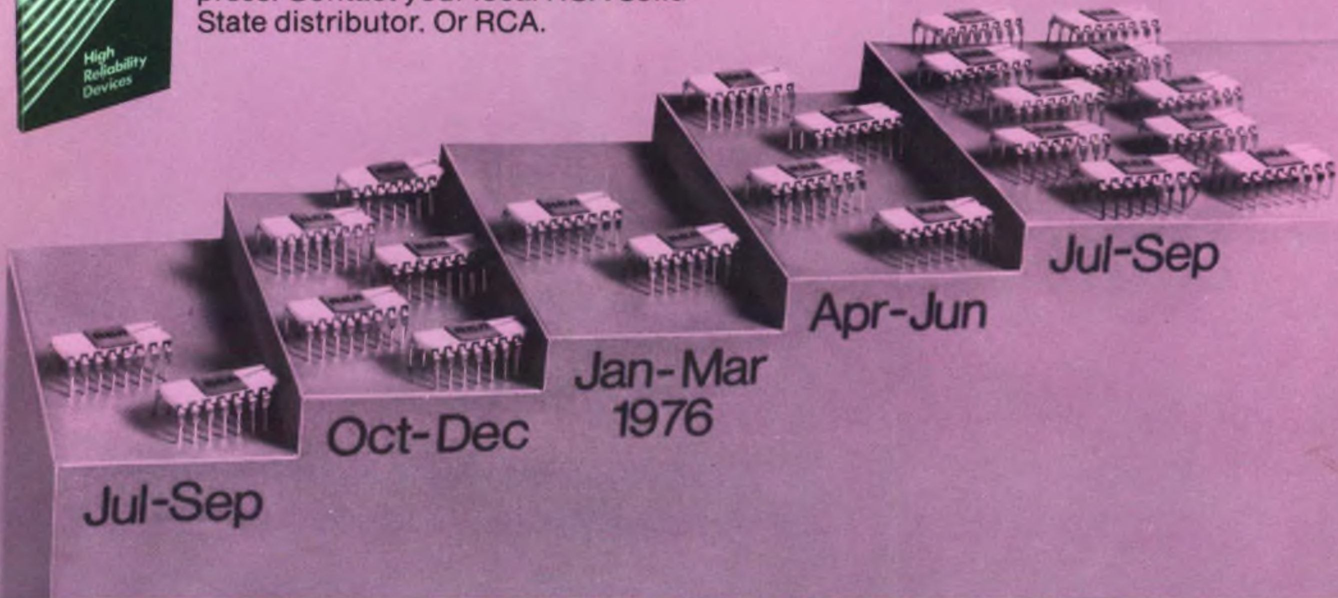
Write: RCA Solid State. Box 3200, Somerville, N.J. 08876; Sunbury-on-Thames, Middlesex TW16 7HW, England; Ste. Anne de Bellevue H9X 3L3, Canada; Fuji Building, Tokyo, Japan.

RCA

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