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for the Radio-Amateur

Especially Covering VHF,
UHF and Microwaves

VHF communications

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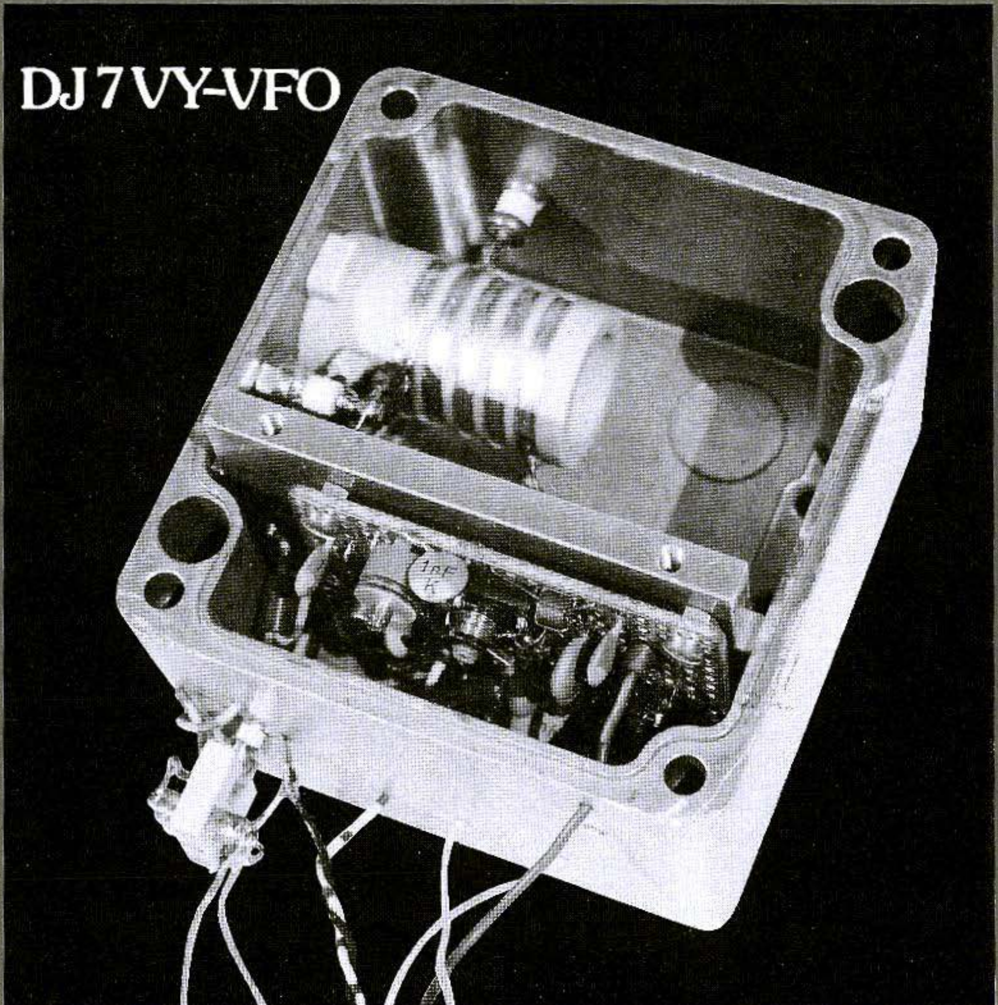

DJ 7VY-VFO

VHF communications

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Volume No.13 · Summer : Edition 2/1981

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Editorial

One often wonders why the Japanese manufacturers have had such success on the amateur radio market, and why this success is not enjoyed by European and US companies. What has happened to such companies as Hammerlund, Halicrafters, Johnson, Collins, and many other world-famous companies ?

The Japanese success is certainly not due to our industry not being able to produce high-quality electronic equipment, since there is very little japanese equipment used for professional communications. It is certainly not due to our low-standard demands, since especially the Europeans tend to demand (expensive) perfection, which they produce and export.

No, the Japanese have perfected the art of producing and exporting that type of equipment that is able to satisfy the majority: Average technology behind an attractive, shiny front-panel.

Let us not be blinded by this, and remember that our technology is by no means inferior. Just take a look at some of the descriptions published in this magazine over the last two years. Compare the noise figures and overload capabilities of the preamplifiers and mixers, the spectral purity of the oscillators, the effectiveness of the DJ 7 VY noise blanker, and many other things including modem demodulators for the various modes.

Surely it would not be much more expensive to produce superior equipment that is more reliable, easier to service, and with instructions one can read !

We consider that European and US amateurs are qualified enough to know the difference, and should be willing to pay the difference. Remember: »In life you only get what you pay for«. Anyway, who wants all these memories and other toys, I personally would prefer higher sensitivity and better overload characteristics, how about you ?

News on the Satellite Scene

According to the US NOAA and European ESA, two new satellite launches are to take place around the same time this magazine is published: Launch of NOAA 7 to replace the defective TIROS satellite which is planned for End of June, 1981, and the launch of METEOSAT II sometime in June, 1981, with first pictures to be expected in July. Lets hope that these will be as successfully launched as the last two INTELSAT V satellites launched recently.

Dr. Meinzer, DJ 4 ZC told me recently that OSCAR 9 is still scheduled for launch in 1982, and this will be especially interesting for us since it will include a 1296/432 MHz transponder, which is very exciting !

73 s ! DJ 0 BQ / G 3 JVQ

Low-Noise VHF-Oscillator with Diode Tuning, Digital Frequency Control, and Frequency Indicator

by M. Martin, DJ 7 VY

The following article is to describe a VHF-oscillator for 2 m receivers, which was introduced at the Weinheim VHF-Convention 1979. It represents a further development of the design described in (1), and is easy to construct due to the use of a standard, cast aluminium case, and the low amount of mechanical work. The sideband noise values are only slightly inferior to that of the variable capacitor version !

1. GENERAL

The large increase in the density of radio amateurs around large cities means that special attention must be paid in the conception of low-noise receive oscillators. Since the noise sidebands of the receive local oscillator will be transferred to all input signals during the conversion process, this means that a strong signal located 20 kHz from the selected receive frequency will considerably reduce one's sensitivity. This process is now to be explained with the aid of an example:

The receiver is assumed to possess a noise figure of 3 dB and a SSB-bandwidth of 2.4 kHz together with an oscillator sideband noise (SBN) of − 120 dB/Hz at a spacing of 20 kHz from the local oscillator signal. This represents normal values associated with equipment available on the market. It is assumed that a signal of 100 dB above noise is present at 20 kHz from the selected frequency. It will be seen from the receiver specifications that the minimum field strength that can be received with a noise figure NF of 3 dB will be $P_{\text{in min}} = -174 + 34 + 3 = -137$ dBm ≙ 31 nV into 50 Ω (− 174 dBm = theoretical noise threshold into 50 Ω, 34 dB ≙ 2.4 kHz to 1 Hz). The 100 dB-signal will be present with − 137 + 100 = − 37 dBm ≙ 3 mV at the 50 Ω input of the receiver. The noise sidebands which were modulated from the oscillator will have the following power values within a 2.4 kHz bandwidth at a spacing of 20 kHz: − 120 + 34 = − 86 dB down on the carrier value of − 37 dBm, corresponding to − 37 − 86 = − 123 dBm. Since the sensitivity threshold of − 137 dBm is blanketed with noise up to − 123 dBm (increase of 14 dB), this will mean that weak signals can no longer be received with this receiver which will then possess a noise figure of 17 dB ≙ 50 kTo !

This means that the available dynamic range of a receiver is not only limited by the large-signal handling capabilities of the input stages and the mixer, but also by the noise sidebands of the oscillator ! Both measures of quality should therefore stand in a reasonable relationship to another. If, for instance, the dynamic range of a receiver is limited to only 70 dB due to intermodulation, it is necessary for the VFO to possess at least a noise suppression ratio of 70 dB within a bandwidth of 2.4 kHz at a spacing of 20 kHz. This corresponds to a SBN-value of − 104 dB/Hz. This means that a value of − 134 dB/Hz will be required if the receiver has a dynamic range of 100 dB !

The better the SBN-value of the oscillator, the nearer the receiver can be tuned to a strong signal, assuming that this signal possesses a better noise suppression ratio. Unfortunately, this demand is not fulfilled by many standard crystal-oscillator circuits used in VHF-technology, and some controversy exists sometimes whether it is the transmitter that possesses this noise spectrum, or whether it is produced in the local oscillator of the receiver.

2. EXPERIMENTAL CIRCUIT

The circuit of the described oscillator is given in **Figure 1**. This oscillator possesses the following technical specifications:

Frequency range:	135 to 137 MHz
Output power:	approx. 0 dBm ≙ 1 mW ≙ 223 mV into 50 Ω at the center frequency

Power reduction at the band limits:
less than 3 dB

Harmonic and spurious signals:
$1/2\ f_0$: – 44 dB, $3/2\ f_0$: – 38 dB, $2\ f_0$: – 40 dB, all other signals more than – 60 dB down.

Voltage sensitivity:

U_D of T 1:	125 mV/kHz
U_D of T 2:	2.5 V/kHz
U_{tune} max.:	2.7 mV/kHz
$U_{D AFC}$:	60 mV/kHz

Noise ratio SBN:

– 135 dB/Hz at 20 kHz spacing at 135 MHz
– 143 dB/Hz at 20 kHz spacing at 137 MHz
< – 160 dB/Hz (!) at more than 500 kHz.

The VHF-portion of the oscillator is very similar to the design published in (1). It will be seen that the variable capacitor has been replaced by two varactor diodes. The effect of these diodes on the noise behaviour was examined in detail. The various types of coupling to the resonant circuit were measured together with their noise behaviour. The results are given in **Fig. 2**.

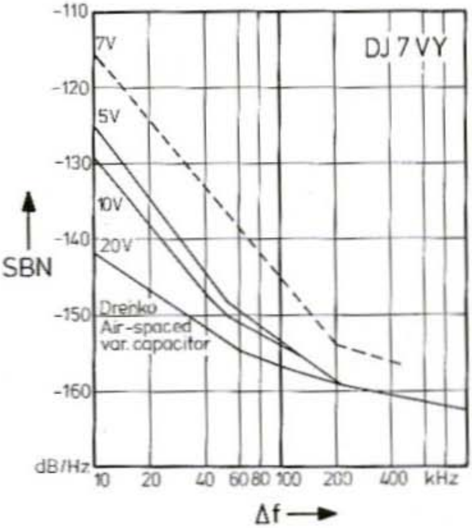


Fig.2: Noise of the VFO as a function of the diode voltage

It will be seen that the deterioration caused by the diodes will reduce on increasing the diode voltage. In excess of 20 V, no difference could be measured between this oscillator and the variable capacitor version. The dashed curve shows the SBN-values of two series-connected diodes coupled to the second coil winding. Even though the VHF-voltage is virtually identical to that of the two parallel-connected diodes connected to this winding, it will be seen that the deterioration is approximately 10 dB ! Due to the »hotter« coupling of the diode resistances, it seems that a considerably higher effect on the Q of the circuit exists than when using the lower coupling of the parallel-connected diode dissipation resistances.

The unloaded Q of the circuit without diodes was measured with the aid of an impedance meter HP 4815 A:

$$L = 0.32\ \mu H,\ \ C = 18\ pF,$$
$$R_p \text{ at } 64\ MHz = 36\ k\Omega;$$

the following will result with a probe Z_{pr} = 130 Ω:

$$Q_0 = R_p/Z_{pr} = 277\ !$$

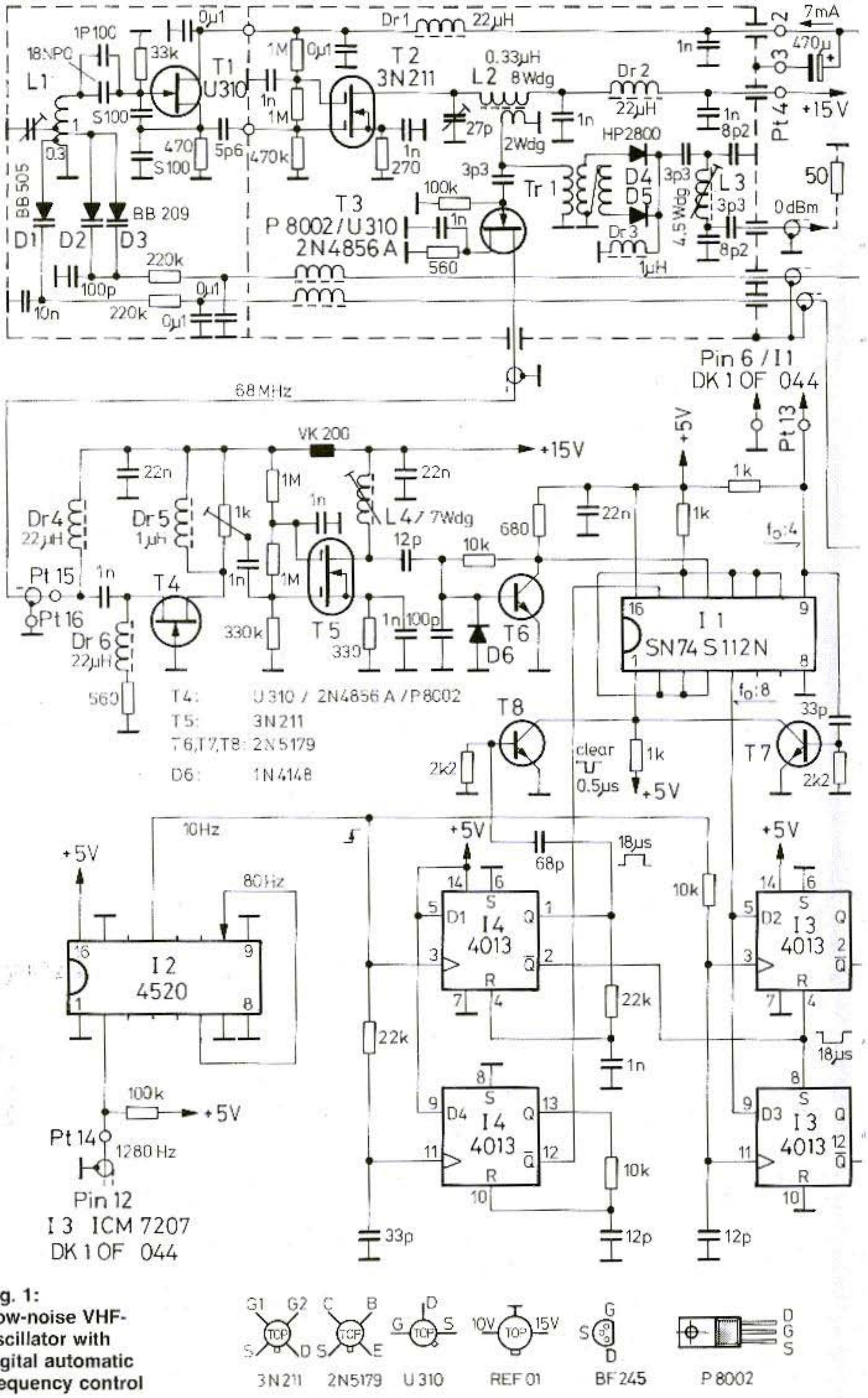
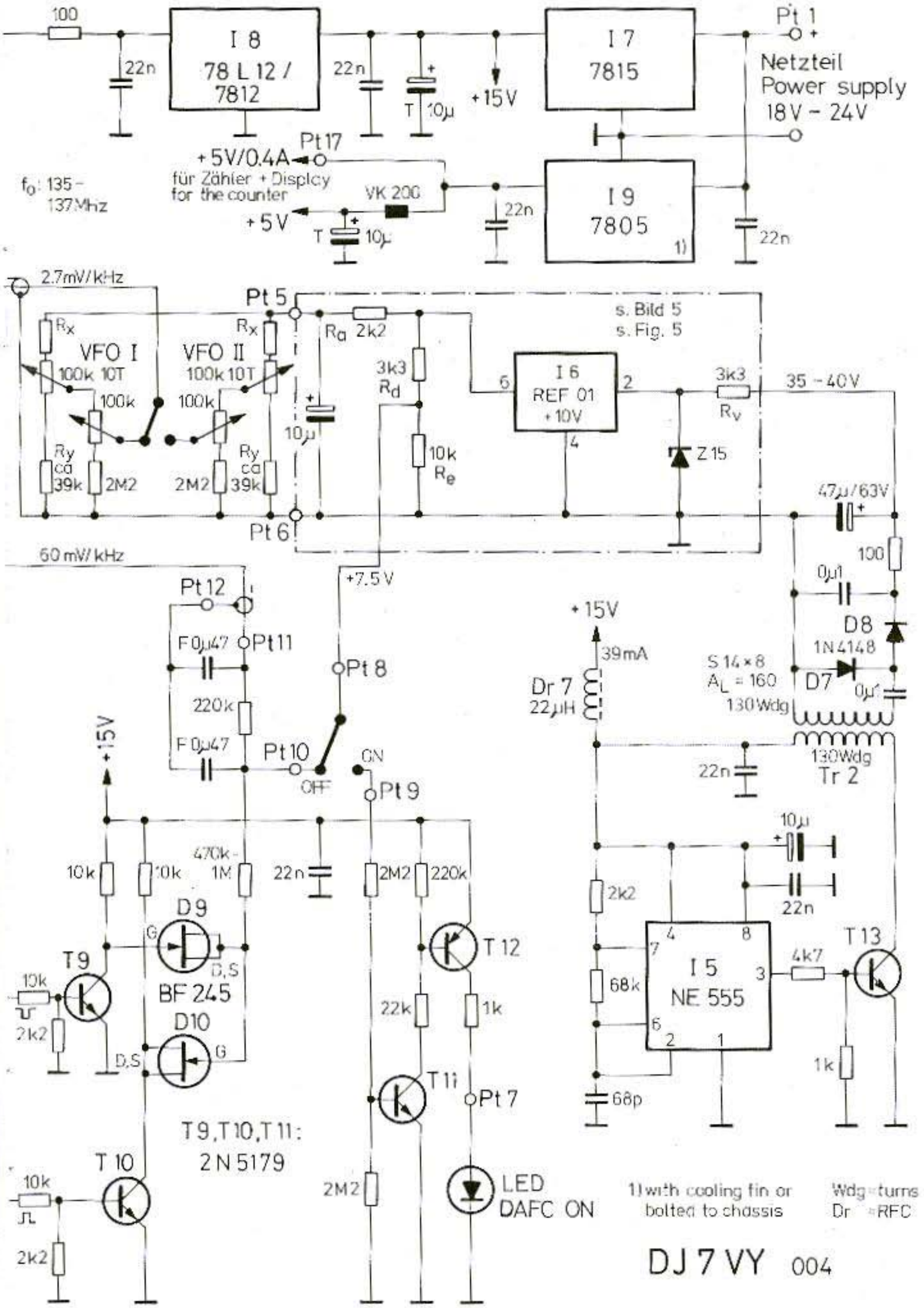


Fig. 1:
Low-noise VHF-oscillator with digital automatic frequency control



Pt 13: to pin 6 of I 1 on DK 1 OF 044 (136 : 4 = 34 MHz)

Disconnect the bridge from 5 to 6 of I 1
Connect pin 12 of I 1 to pin 6 of I 6
Disconnect bridge from 5 to 6 of I 6

Connect Y to pin 12 of I 2
Disconnect bridge from pin 12/I 1 to pin 12/I 2
Connect W to pin 13/I 1

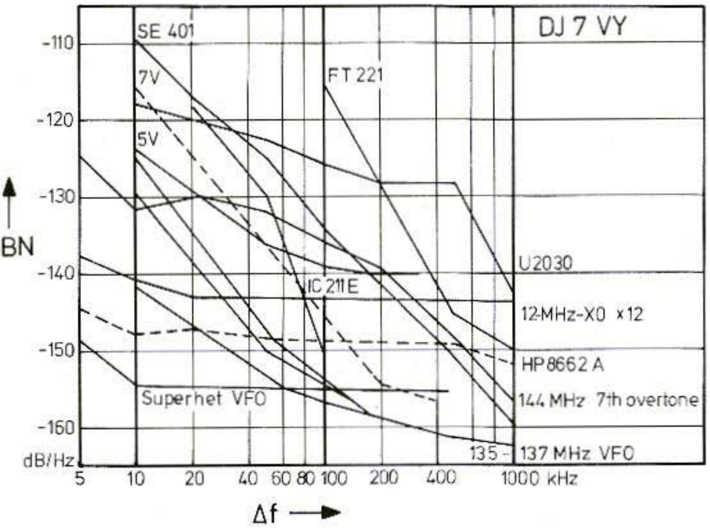


Fig. 3: Noise values of various different oscillators

A comparison to the noise values of other oscillators is given in **Figure 3**. It will be seen from the poor values obtained with some PLL-oscillators that the use of very small inductances having too great a coupling to the connected diodes severely limits their usability.

Furthermore, the frequency variation of the VFO as a function of the tuning voltage was determined. The lower curve in **Fig. 4** is valid for the circuit shown in Figure 1 and shows the lowest variation between the higher and lower limit of the tuning range. If the value is to be adjusted for minimum

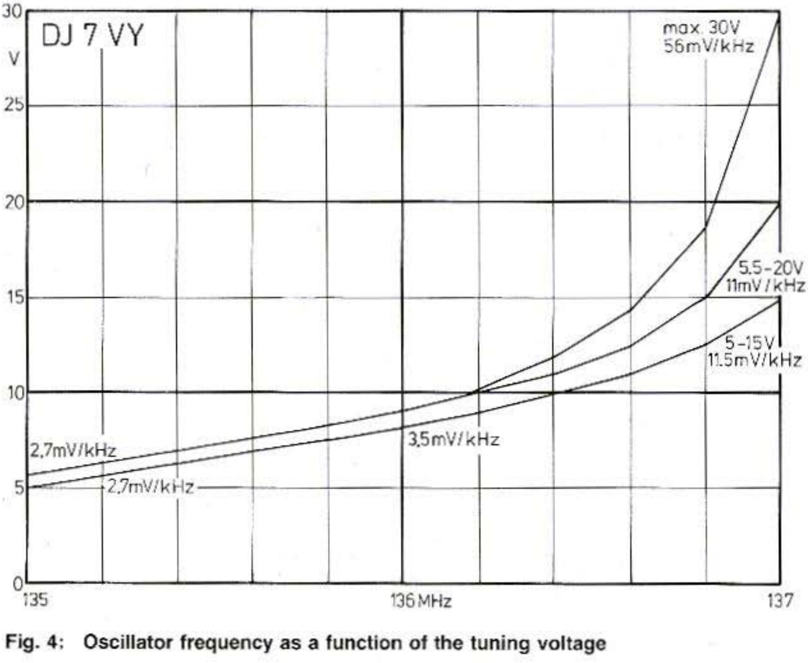


Fig. 4: Oscillator frequency as a function of the tuning voltage

noise in a narrow frequency range, attention should be paid that the tuning voltage is only variable between 20 and 30 V.

As can be seen in the diagram, a maximum voltage sensitivity of 2.7 mV/kHz results which places demands on the stability of the voltage stabilizer. If the wiper of the tuning potentiometer is set at one third of the maximum voltage, e.g. approximately 6.6 V of 20 V, and if the maximum permissible frequency drift should be less than ± 5 Hz, this means that the 20 V tuning voltage must be stable to within 81 µV ! It is not difficult to obtain this stability of ± 40 µV as a long-term value when using series-connected integrated stabilizers. This is quite different with respect to the short-term behaviour.

The low-frequency flicker-noise of the stabilizers in the range of 0.1 to 10 Hz amounts up to 300 µV with most types and can hardly be suppressed using low-pass filtering. In order to obtain a time constant of 0.01 Hz, one would require, for instance, 100 Ω and 200 000 µF (= 200 mF), and the charging of this electrolytic would take a considerable length of time.

The values exhibited by conventional stabilizers were measured with a sensitive oscilloscope and are given in **Table 1.** It was found that only type REF 01 possesses the required low-noise values.

78 L 15:	± 100 – 300 µV
78 L 10:	± 150 µV
723:	± 60 – 150 µV
CA 3085:	± 100 µV
MC 1461:	± 30 µV
MZF:	± 30 – 60 µV at I_Z = 5 mA
	± 200 µV at I_Z < 1 mA
REF 01:	± 10 µV

In order to obtain higher tuning voltages from a fixed voltage value of 10 V, a DC-amplifier was constructed using »low-noise« AF-transistors, by which the same flicker-noise was exhibited as by the measured voltage stabilizers.

For this reason, the tuning voltage was left at 10 V accepting the negligible reduction in quality.

The most simple manner of increasing the voltage, is to use a cascade of REF 01-stabilizers as shown in **Figure 5**. This is easily possible up to 20 V due to the higher conversion voltage (DJ 7 VY 004 is already prepared for this).

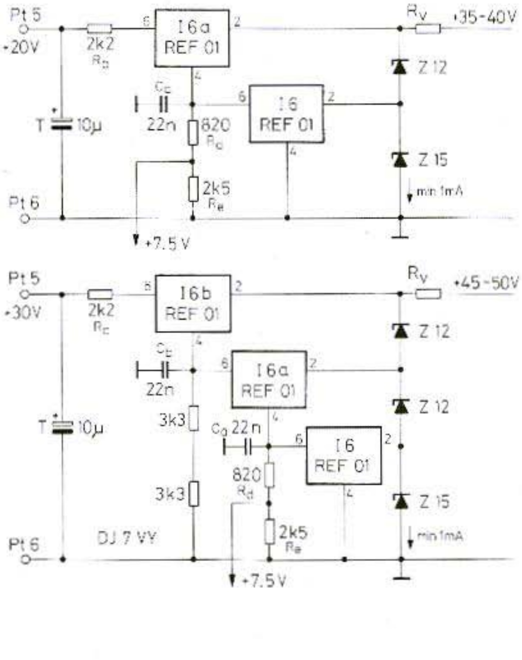


Fig. 5
Generation of an extremely low-noise tuning voltage using cascaded precision voltage stabilizers

The value of the dropper resistor R_d should be made so that at least 1 mA pass current flows through the lowest 15 V-zener diode. In the case of the 30 V version, the winding ratio should be increased correspondingly.

The stabilization factor amounts to a total of more than 10^6, since zener stabilization is provided previous to the REF 01, and since the DC-voltage converter is fed from a stabilized voltage source.

The long-term stability of the oscillator is obtained by using an improved, and simplified digital automatic frequency control circuit (DAFC) similar to (2). The reference frequency for this is obtained from a frequency counter to be described by J. Kestler, DK 1 OF, in one of the next editions of VHF COMMUNICATIONS.

This frequency counter is also used for the frequency readout of this oscillator.

3. CIRCUIT DESCRIPTION

3.1. Oscillator

The oscillator is equipped with the low-noise, high-current FET U 310 manufactured by Siliconix, and operates in a Clapp circuit in a frequency range of 67.5 and 68.5 MHz. Three taps are to be found on inductance L 1 that are made directly to the silver-plated windings of the inductance: The DAFC-diode BB 505 is connected at 1/3 turns, the two diodes BB 209 at one turn, and the air-spaced trimmer used for setting the upper frequency limit is connected at 1.5 turns. The main resonant circuit capacitor consists of the parallel-circuit of 18 pF/NPO plus 1 pF/P 100 which must be altered when altering the frequency range.

The buffer stage T 2 (3 N 211) is driven from the source of T 1. A resonant circuit together with low-noise Schottky diode doubler are to be found at the drain of the buffer. The 135 to 137 MHz signal from the doubler is passed via a bandpass filter for suppression of the frequencies $1/2\, f_0$ and $3/2\, f_0$. This means that when a tuned preamplifier is used, a spurious reduction of more than 100 dB will be present at 68 ± 9 MHz and 204 ± 9 MHz. Such spurious signals with a spacing of several MHz observed with premix-oscillators were not present.

The output power of the VFO can be brought to the required level for driving a high-level mixer by using a subsequent amplifier circuit similar to that given in (3), or the circuit given in **Figure 6**.

A portion of the 68 MHz signal is tapped off at high impedance before the doubler diode with the aid of T 3 and passed to the DAFC and counter circuit.

3.2. Digital Frequency Selection

After passing through the three buffer stages equipped with transistors T 3, T 4, and T 5, the 68 MHz signal is fed to switching transistor T 6, which triggers the double flipflop I 1. Integrated circuit I 1 divides the input frequency firstly by two, and this out-

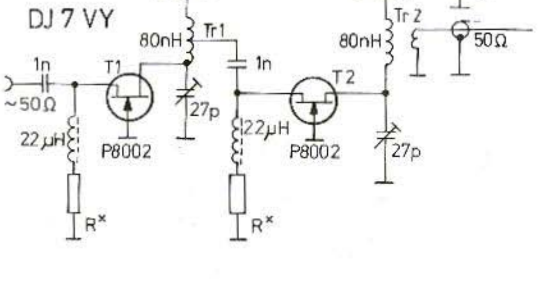


Fig. 6:
VFO-amplifier with an output power of 23 dBm (200 mW)

Gp = 18 – 24 dB according to tap
T 1, T 2: P 8000, P 8002 or
2 N 4856 A depressed into chassis.
Tr 1, Tr 2: ratio 3 : 1 to 4 : 1

R* select for a I_D of approx.
30 mA for T 1 and 40 - 50 mA for
T 2 (approx. 33 - 68 Ω).

put signal is fed to the input of the counter and secondly the signal is once again divided by two in switching transistor T 7, so that a frequency of 17 MHz appears at the Q-output (pin 5). This is interrogated via divider I 2 with a repetition rate of 10 Hz. The resulting high or low level is fed to the D-inputs of the two flipflops I 3, which then control the so-called charge pump. Since I 3 is not able to process a clock frequency of 17 MHz, the output state of I 1 will be maintained until I 3 has processed the signal. After this, a reset-pulse is passed via I 4 to I 1, and the process will be recommenced.

According to whether a high or low signal is fed to the charge pump, a charge pulse will be added or subtracted at the tuning diode via T 9 or T 10, which means that the frequency of the oscillator will be corrected up or down.

Basically speaking, the circuit operates as a 1 Bit-counter, whose output state fluctuates statistically with the bit-error in the case of a constant input frequency. On average, the states 'High' or 'Low' appear equally often. If the input frequency starts to drift, more high, or more low pulses will appear according to the direction of drift, and these allow the frequency to be maintained. The scanning rate and the frequency division ratio determine the frequency locking steps. The 1 Bit-counter can count to an accuracy of 10 Hz when using a 100 ms time base. Since the frequency division ratio is 136 : 17 = 8, this will mean that the frequency locking steps will be 80 Hz.

As soon as the DAFC is switched on, the oscillator frequency will drift by a maximum of ± 40 Hz and will remain at this position as long as the drift speed does not exceed the maximum frequency control speed, and the diode voltage does not run away too much from the mean voltage (approximately ± 3 V) during the control process.

The control speed is determined by the approximately 18 µs keying length of the charge pump (RC-link 22 kΩ / 1 nF at I 4), and by the value of the storage capacitor and its load resistance. It amounts to approximately 1.8 kHz per minute. If the tuning is changed with the DAFC switched on, the frequency variation will be far greater than this value and the charge pump will give a continuous chain of plus and minus pulses. However, as soon as the tuning knob is released, the next lock-in point will be reached, and the frequency will remain stable.

The circuit is extremely high-impedance between point 10 and ground. In the case of a period of 100 ms, and a charge-step of approx. 3 Hz, the voltage variation caused by positive or negative leakage currents on the two charge capacitors should not be greater than the frequency sensitivity of the control diode multiplied by the value of the steps: $60 \times 10^{-6} \times 2 = 0.18$ mV !

This results in a mean DAFC-voltage of 7.5 V when using the well-known charge equation:

$$Q = C \times U = I \times t$$

with

$$R_L = U_D/I$$

the minimal leakage resistance is thus

$$R_L = \frac{U_0 \times t}{C \times U} = \frac{7.5 \times 0.1}{1.8 \times 10^{-4} \times 10^{-6}} = 4.16\ \mathrm{G\Omega}$$

And the maximum leakage current will be 1.8 nA !

This means that all capacitors in the DAFC-circuit must be plastic-foil types, since only these types of capacitors provide a sufficiently high insulation resistance. For the same reason, diodes D 9 and D 10 are junction FETs, whose gate-diode leakage currents are typically less than 0.01 nA. The leakage currents of various diodes type BB 505 measured were found to always be less than 0.1 nA, and therefore fulfilled these demands.

The required amount of charge for the control of other scanning periods and frequency division ratios can also be determined for other oscillators using the previous equation. For example, a 5 MHz VFO is connected to point 15 via a transistor such as T 3 (RFC 5 and L 4 increase to 22 µH, and the 100 pF is deleted at the input of T 6). The scanning frequency is 20 Hz (pin 12 of I 2 instead of pin 13). This also results in 80 Hz when using a frequency division ratio of 1 : 4. The tuning sensitivity of the diode is assumed to be 300 mV per kHz. This means that a voltage step value at the charge capacitor of 1 mV results for a suitable step value of 3 Hz. The charge current amounts to $7/10^6 = 7\ \mu A$. The required keying length for 1 mV variation at 1 µF results from the following equation at a current of 7 µA :

$$t = C \times U/I, \quad \text{thus}$$
$$10^{-6} \times 10^{-3} / 7 \times 10^{-6} = 143\ \mu s$$

Instead of increasing the keying length by eight times, it is possible for the charge resistance to be decreased correspondingly to 120 kΩ. At higher scanning rates, the insulation demands will be lower, which can easily be realized in the case of the previous calculation.

The frequency limit of the DAFC amounts to approximately 100 MHz when using a 74 S 112 for I 1. In the case of frequencies below 30 MHz, a type 74 LS 112 can be used for I 1, and the 33 pF capacitor between T 7 and pin 9 of I 1 can be connected to pin 13 for lower division factors.

The frequency lock-in points then correspond to twice the scanning frequency.

3.3. The Counter

The signal supplied by I 1 is 1/4 of the VFO output frequency (34 MHz), which is processed further in the four-decade counter designed by J. Kestler, DK 1 OF. In order to delete the 1 : 4 frequency division for the counter without increasing the time base length, two of the dividers in the counting branch (I 1 and I 6) only use the 1 : 5 dividers, and the 1 : 2 dividers are avoided. Since I 1 cannot process 34 MHz with its 1 : 5 divider, it must be replaced by a 74 S 196. The two first digits of the 6-digit indicator are wired to »14«, and a »9« is programmed as intermediate frequency in the first counter decade. An exact description of this counter follows on the next pages in this edition.

3.4. Voltage Supply

The drain voltage of the oscillator transistor T 1 is stabilized twice, and the output voltage of the 78 L 12 is passed through a RC-lowpass filter for filtering out any noise components. Since the frequency sensitivity is 120 µV/Hz, the flicker-noise has a negligible effect here.

The tuning voltage is stabilized in a multiple stabilizer circuit: Oscillator I 5 drives the converter transistor T 13 which generates a DC-voltage of approximately 40 V on the secondary winding of Tr 2. The minus pole of this winding is only grounded to the VFO-case. This voltage is then stabilized to 15 V with the aid of a zener diode and fed subsequently to the low-noise, precision voltage stabilizer REF 01. The output voltage of this stabilizer is fed to the DAFC-diode D 1 via a voltage divider when switched off, and via an additional noise-filter to the tuning potentiometers.

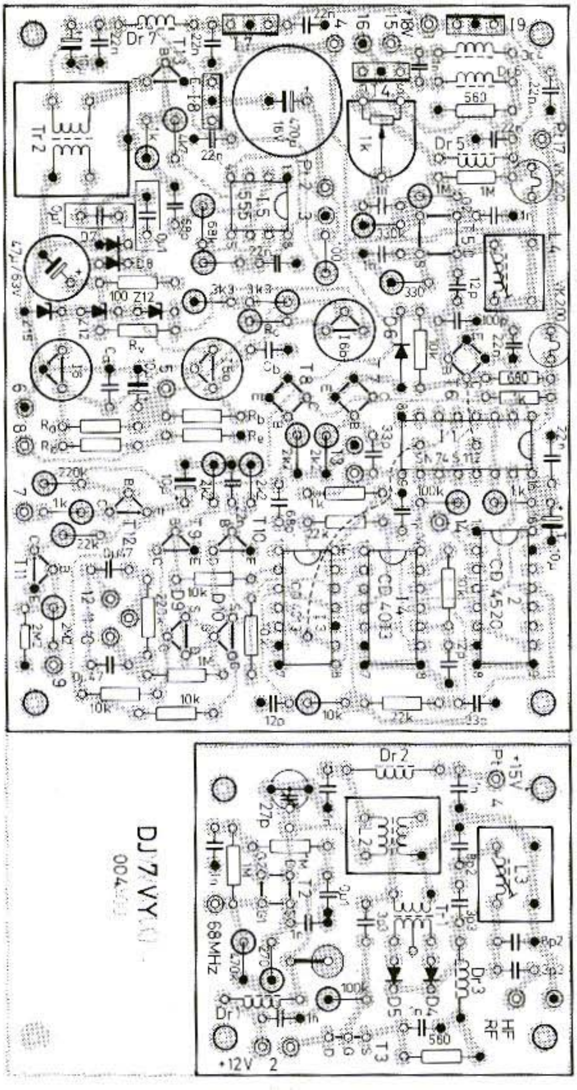
The lower frequency limit of the tuning range is determined by the fixed resistor connected in series with the tuning potentiometer. A second potentiometer allows the fine adjustment of the frequency. If the potentiometer circuit is built up several times, it is possible to switch the tuning voltage and use the circuit as if it were several separate VFOs.

4. CONSTRUCTION

The oscillator is enclosed in a cast-aluminium case type A 105 with the dimensions 75 mm x 80 mm x 52 mm. The DAFC is accommodated together with the tuning voltage supply and the oscillator buffer stages on the double-coated PC-board with through-contacts designated DJ 7 VY 004. The dimensions of this board are 140 mm x 75 mm (see **Figure 7**). The VFO-buffer circuit is sawn off before mounting the components.

The oscillator components are mounted on the 5 mm thick aluminium inner panel which is provided with M 3 threaded holes and screwed to the base and sides of the case. **Figure 8** gives the dimensions, and position of the components. This panel

Fig. 7: Component locations on PC-board DJ 7 VY 004 with through-contacts for accommodation of the oscillator buffer, DAFC, and tuning voltage generator



could also be made from 2 mm thick brass and mounted with brackets. PTFE-supports of 3.7 mm are pressed into position at the positions marked with a »T«, and PTFE feedthroughs of 3.7 mm are provided at the positions marked with »TD«.

Holes of 1 mm diameter are drilled into the plate for the ground connections, after which 1 mm dia. silver-plated wire is placed through them and flattened somewhat to provide a good contact. On the component side, this wire is shortened to approxima-

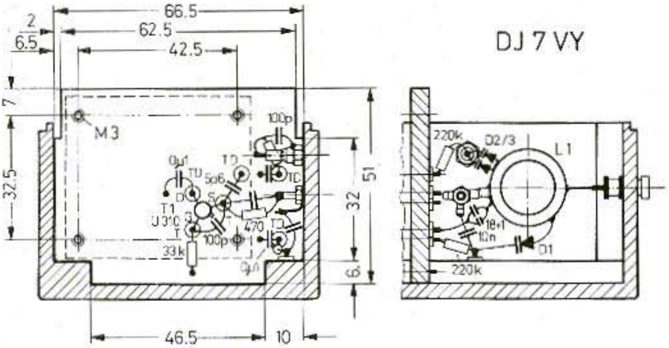


Fig. 8:
Support plate for the oscillator-components; cross-section through the oscillator

tely 2 mm and flatened like a rivet on the other side. Of course, when using a brass plate, it is possible for the ground connections to be soldered. The grounding of the inductance is made using a long M 3 solder tag, which may not be used as ground connection for the 470 Ω resistor and the 100 pF styroflex capacitor, since it is only »cold« at its base. A second solder tag must be provided for this, which is screwed to the same position (see **Fig. 9**).

The support for the tuning diodes is screwed into place 17 mm from the center point of the coil, and this should be spaced 25 mm from the base of the case. It is important that the leads of the 100 pF series-capacitor should be especially short at this position. If the main tuning capacitance is too small, and the air-spaced trimmer has too much capacitance, a reversal of the resonance can take place if the value of the capacitor is incorrect, or if the leads are too long. In this case, the output frequency will increase in a narrow range on varying the voltage, although the diode voltage is reduced, and then after approx. one Volt less return to a normal behaviour.

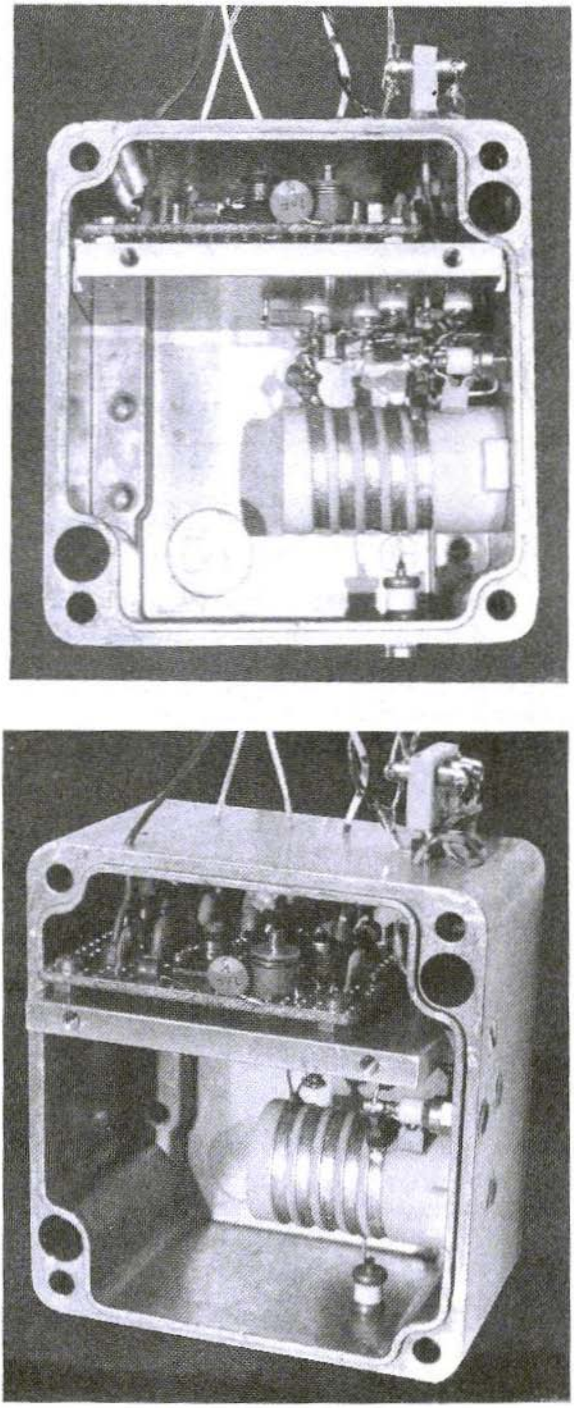
It seems that series resonance effects occur due to the parasitic capacitances and inductances, which will not occur when the disk capacitor is soldered into place correctly.

Attention should be paid when mounting the inductance that the DAFC-diode should be soldered firstly at 1/3 of the first turn, since this position is not accessible afterwards. The oscillator and buffer board are completed, wired together and mounted to the center panel of the case with the aid of 3 mm spacers, and the coaxial cable should be pulled out to the holes slowly. Caution: Do not forget the alignment holes for the trimmers at L 2 and for L 3 !

After completing the DAFC-board, the following changes must be made for use in conjunction with the counter board DK 1 OF 044:

1. Disconnect the bridge from pin 5 to pin 6 of I 1;
2. Exchange I 1 for a type 74 S 196;
3. Interconnect pin 12 of I 1 to pin 6 of I 6;
4. Disconnect the bridge from pin 5 to pin 6 of I 6;
5. Connect point Y to pin 12 of I 2;
6. Disconnect the bridge from pin 12 of I 1 to pin 12 of I 2;
7. Connect point W with pin 13 of I 1;
8. Connect point 21 to ground (division 1 : 100 is now 1 : 25);
9. Connect a diode from point 7 with its cathode to point 6;
10. Connect a further diode from point 7 with its cathode to point 3 (programming for 9 MHz IF);
11. Connect 10 kΩ from point 20 to + 5 V;
12. Connect point 19 to + 5 V;
13. Connect point 18 to ground;
14. Ground point 3, 4, 5, and 6 via 10 kΩ;

Fig. 9:
Photograph of the author's prototype using a Vero-board



15. Connect six resistors of 270 Ω for the fixed programming of the first two digits to »14« on the rear side of the indicator board to ground;
16. Solder 100 Ω for the decimal point at the third position on the right, or at the fourth position on the left to ground;
17. Connect pin 12 of I 3 on DK 1 OF 044 with the aid of coaxial cable to point 14 on DJ 7 VY 004;
18. Interconnect pin 6 of I 1 on DK 1 OF 044 to point 13 on DJ 7 VY 004;
19. The preamplifiers on the counter board need not be equipped !

It is now possible for the oscillator, readout, and DAFC to be switched on. If no faults have been made, a receive frequency in the 2 m band should be indicated immediately after connecting the supply voltages.

Note: The counter and DAFC-board should be enclosed in a metal case in order to ensure that no interference from the digital circuits is introduced into the signal path !

4.1. Special Components

T 1:	U 310 (Siliconix)
T 3, T 4:	U 310, P 8000, 2 N 4856 A BF 246 C, P 8002
T 2, T 5:	3 N 211 (Texas Instr.)
T 6, T 7, T 8:	2 N 5179, 2 N 709
T 9 - T 11:	BC 107, BC 143, BC 338, or similar NPN
T 12:	BC 177, BC 145, BC 327 or similar PNP
T 13:	BC 107 or similar (metal case!)
I 1:	74 S 112 (2 x JK-FF)
I 1 on DK 1 OF 044:	74 S 196
I 2:	4520 (2 x 4-Bit counter)
I 3, I 4:	4013 (2 x Dual Flipflop)
I 5:	NE 555 (Timer)
I 6:	REF 01 CJ (10 V control)
I 7:	7815
I 8:	78 L 12 or 7812
I 9:	7805

D 1:	BB 505
D 2, D 3:	BB 209
D 4, D 5:	HP 2800
D 6 - D 8:	1 N 4148 or similar
D 9 - D 10:	BF 246, BF 245 or similar, drain and source connected

100 kΩ 10-turn-potentiometer

Case: Type A 105, available from the publishers

Air-spaced trimmer: AT 5200, 10 pF, Tecelec Airtronic (may not be required, see alignment details).

Inductances and Filters

L 1:	Aged ceramic inductance, type 87-6228, Stettner
L 2:	0.33 µH = 8 turns of 0.3 mm dia. enamelled copper wire, two coupling turns at the center of the first winding. Core in central position for L_{max}. Special coil set with violet core, without cap and screening can.
L 3:	4.5 turns of 0.3 mm dia. enamelled copper wire in special coil set as for L 2, without cap and can
L 4:	7 turns of 0.3 mm dia. enamelled copper wire in special coil set with orange core, cap and can
Tr 1:	4 + 2 x 4 turns of 0.12 mm enamelled copper wire on a two-hole core, Siemens B 62152 - A 8 - X 17
Tr 2:	2 x 130 turns of 0.12 mm dia. enamelled copper wire wound in a potted core 14 x 8, $A_L = 160$

RFC 1, RFC 2, RFC 4, RFC 6, RFC 7: 22 µH
RFC 3, RFC 5: 1 µH

Use 1 mm dia. PTFE coaxial cable SM 50 for wiring the tuning voltage, the DAFC, and for the RF-signals between the VFO, and the board.

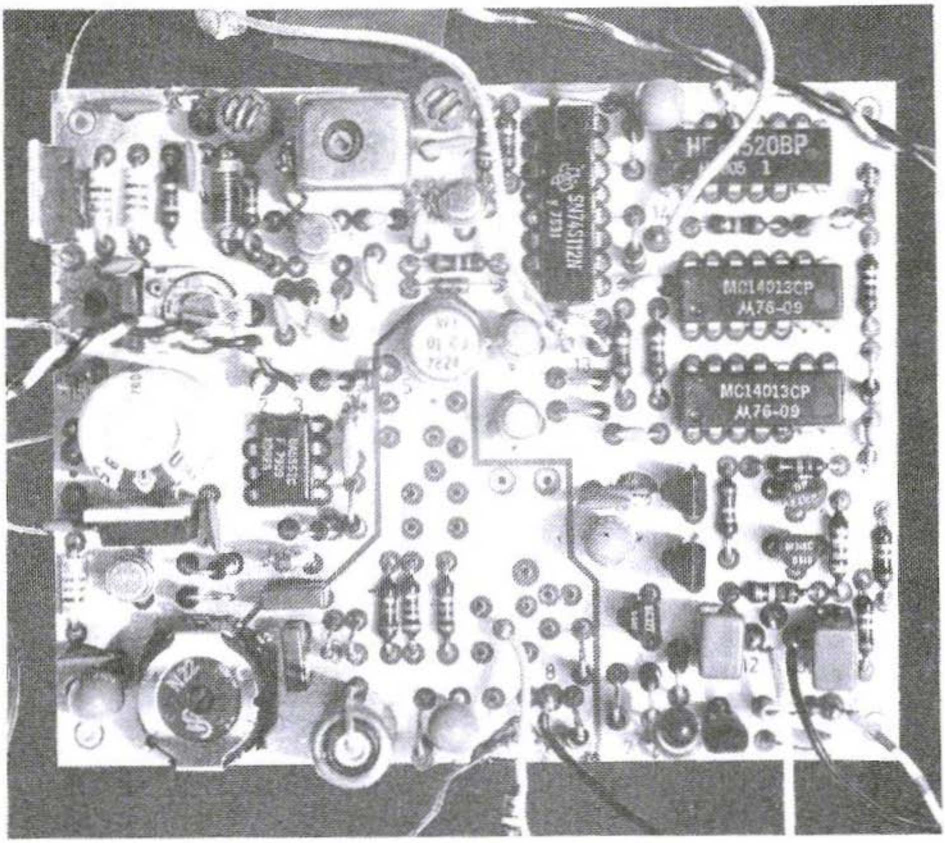


Fig. 10: Photograph of the author's prototype of module DJ 7 VY 004

5. ALIGNMENT INSTRUCTIONS

The only measuring equipment required for aligning the oscillator shown in **Figure 9** are a multimeter with RF-probe, and a receiver.

Firstly terminate the output of the VFO with the aid of a 56 Ω resistor, and measure the VHF-output voltage. The 145 MHz indicator is aligned for maximum with the aid of the drain-trimmer of T 2, and with L 3, and should amount to approximately 220 mV. The output voltage can be increased by reducing the source resistance of T 1. The drain current should, however, not be greater than approximately 10 mA, so that T 1 will not cause too much drift.

The required frequency range is set either with R_x, or the trimmer of L 1.

Firstly align the tuning potentiometer for maximum voltage with the DAFC switched off and the fine tuning set to a center position. The frequency should now be aligned to 146.1 MHz with the aid of the trimmer of L 1. In the case of an intermediate frequency of 10.7 MHz, it is preferable for the main circuit capacitance to be increased by 0.5 to 1 pF (1.5 to 2 pF in parallel with the 18 pF NPO) rather than adjusting this trimmer too far. If the trimmer is deleted, it is possible for the upper frequency limit to be set by providing a suitable dropper resistor R_x in conjunction with the tuning potentiometer.

After this, place the tuning potentiometer to the other stop and align the lower frequency limit to approximately 143.9 MHz with the aid of the dropper resistor R_y. A trimmer should not be used here since the aging of the contacts, and thus the resistance can fluctuate. Metal film resistors are most favorable !

Since the alignment of R_y also has an effect on the upper frequency limit of R_x, it is necessary for both values to be changed alternately. The alignment is made preferably using trimmer potentiometers, whose values are measured after completing the alignment and are then replaced by fixed resistors.

For alignment of the counter input circuit, the output trimmer of T 4 and L 4 should be aligned alternately so that the resonance of L 6 is at the center of the band and that the input voltage at the band limits is just slightly greater than the threshold of the counter.

The operation of the DAFC is now checked with the aid of a receiver. The VFO-signal can either be monitored itself, or the VFO used as receive oscillator tuned to a crystal-stable receive signal, and monitored in the SSB-mode. The frequency must remain stable after switching on the DAFC, which means the AF-beat tone should not change !

If the frequency drifts, the insulation of all lines to point 10 should be checked. If the fine tuning is now rotated very slowly, the control process can be monitored acoustically. When altering the tuning by approximately 20 Hz, the signal will return to the previous lock-in frequency after releasing the tuning knob. If the sudden tuning was greater than 40 Hz, the circuit will lock in at the next point 80 Hz away. The original frequency can be obtained by rotating slightly in the opposite direction. By carefully monitoring and rotating slowly, it is possible for the individual discrete lock-in frequencies to be heard.

In the case of a lock-in spacing of 80 Hz and an output frequency of 136 MHz, the tuning accuracy will amount to ± 10 Hz/136 MHz = 7.3×10^{-8} due to an assumed error of three subsequent charge surges. The lock-in spacing amounts to 5.8×10^{-7} ! It will be seen from these values that the reference frequency used for control must have a greater quality than this; this means that its drift specifications must be at least one order of magnitude better ! However, this is only possible when using very good temperature-compensated Xtal oscillators (TCXOs), or crystals mounted in an oven. The reference oscillator accommodated on PC-board DK 1 OF 044 can only be used with some limitations if a heating of the crystal and module ICM 7207 is avoided. It is better to use an external 5.24288 MHz oscillator using NPO capacitors, and to feed its output signal to pin 6 of the ICM 7207.

Another frequency in the range of 1 to 2 kHz with a required stability of 0.1 ppM can be injected to pin 14 of I 2 on the DAFC-board. The circuit will operate with any input frequency that is sufficiently stable. It is possible for it to be locked into a standard frequency transmitter such as DCF 77, whose transmit frequency need only be divided by $2^6 = 64$, in order to achieve a frequency stability of greater than 10^{-10} (a further IC type 4520 is required) ! It is also possible to lock in to the BBC on 200 kHz by dividing by $2^7 = 128$.

6. OPERATING INSTRUCTIONS

Since the oscillator can also be tuned with the DAFC switched off, and will lock in to the next lock-in frequency after releasing the tuning knob, the DAFC-switch is not absolutely necessary. It can be replaced by a push-button switch between points 8 and 10, and without the LED-readout. In this case, the DAFC-circuit will be set to a mean voltage after switching on the oscillator. After this, it will remain in its operating range during all »normal« temperature fluctuations. It is only when a frequency is to be maintained over a considerably long period that it is recommended to switch off the DAFC temporarily so that the commencement point of the correction voltage is at the center of the tuning range.

The previous frequency is not stored on changing the frequency of one tuning potentiometer to the other. Both frequencies are as stable as a crystal in their locked-in mode, however, not their actual spacing. This means that a slight frequency shift can occur on switching back to the original frequency since the DAFC-circuit has generated a different diode voltage after locking in to the other frequency. Furthermore, the gradient of the temperature coefficient is not necessarily equal at both positions.

In order to save current, the counter board can be switched off with the exception of the oscillator and clock generator. The operation of the DAFC will not be adversely affected.

7. IMPROVEMENTS

Thanks to its very good sideband noise specifications, this oscillator is extremely suitable for operation within a PLL-synthesizer system. However, special attention must be paid that no noise voltages are generated within the PLL-control loop itself, since this would then deteriorate the original SBN-values. The most favorable method is to use two loops, and two tuning diodes. The coarse tuning is made using a digital-analog converter with subsequent lowpass filter at a very low-noise level, and the fine tuning of the fast control frequency components is carried out with the aid of a loosely coupled diode.

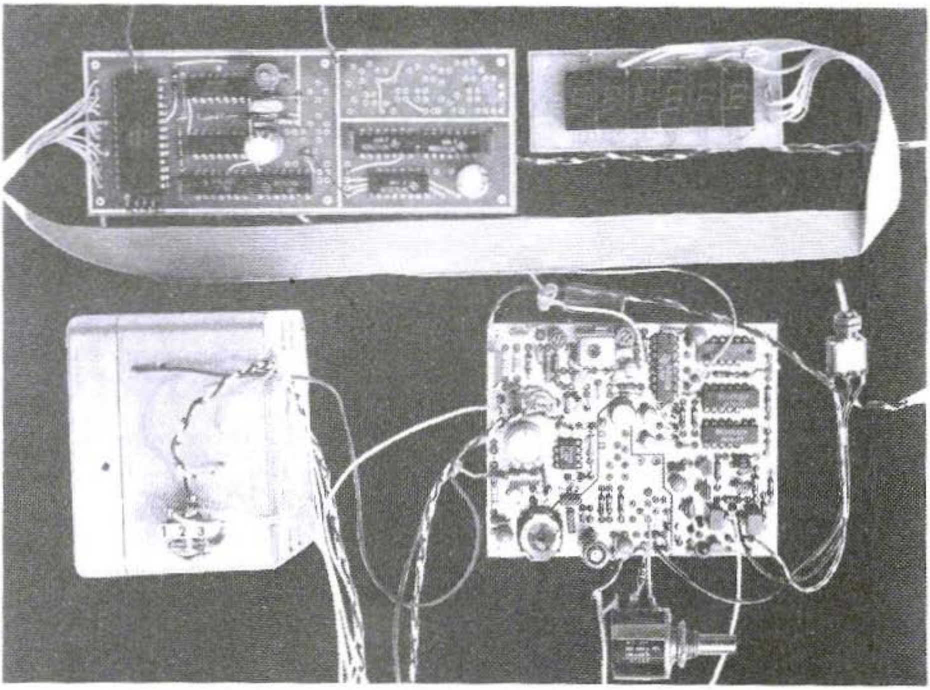


Fig. 11: VFO, DAFC, counter, and readout temporarily connected together

Our digital-circuit specialists are therefore called to realize this aim ! New, very »intelligent« PLL-components have just appeared on the market !

8. REFERENCES

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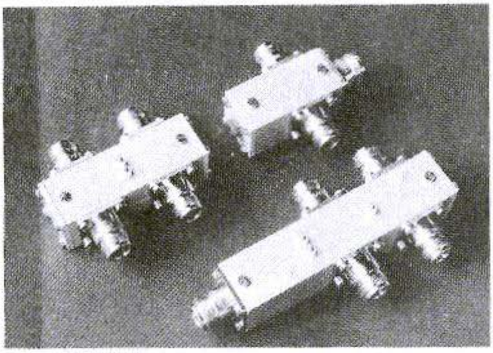
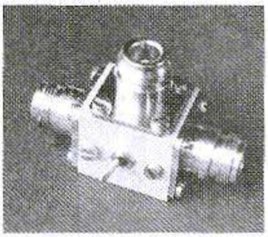
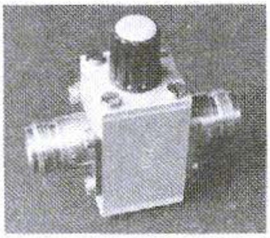
(3) M. Martin, DJ 7 VY: A Modern Receive Converter for 2 m Receivers Having a Large Dynamic Range and Low Intermodulation Distortions VHF COMMUNICATIONS, Edition 4/1978, pages 218-229

(4) J. Kestler, DK 1 OF: A Settable Up-Down Frequency Counter. This will be described in one of the next editions of VHF COMMUNIC.







A Settable Up-Down Frequency Counter

by J. Kestler, DK 1 OF

Modern communication technology places high demands on the accuracy of the transmit and receive frequencies. Radio amateurs, of course, often tune across the band, and find somebody to talk to, however, it is necessary to know the frequency exactly when making skeds on the VHF and UHF bands.

For this reason, digital frequency readouts are becoming very popular with commercial amateur radio equipment.

Home-made counters consisted previously of several individual integrated circuits that required a relatively large amount of room, and power consumption. These types of counters were not very suitable for installation in radio equipment.

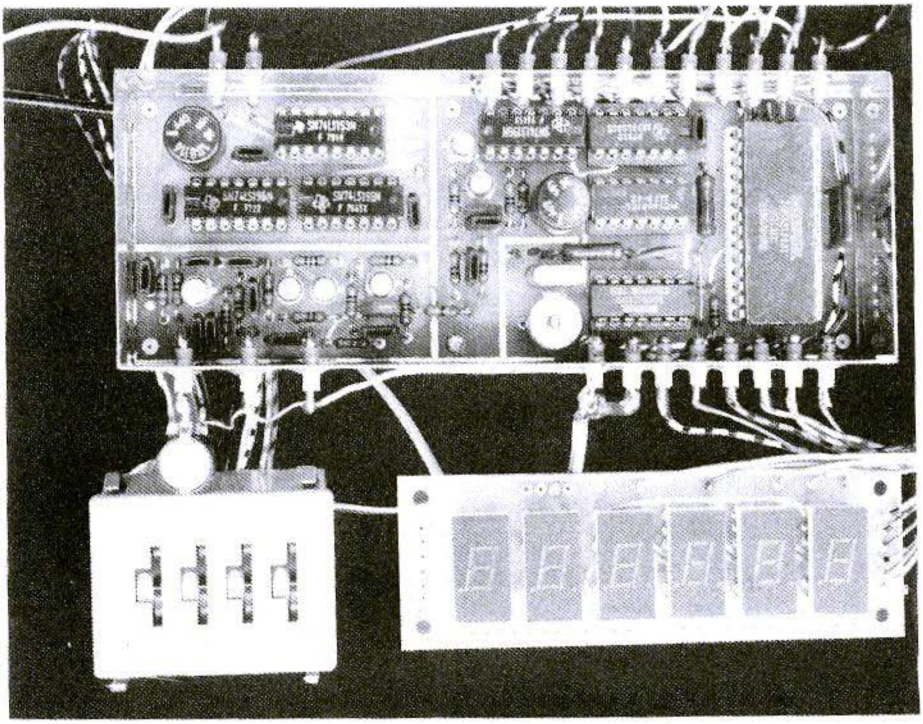


Fig. 1: Photograph of the author's prototype showing the maximum complement including high-impedance input amplifier and programming using digital switches

However, inexpensive, highly integrated MOS-circuits have been available for some time now that contain all important components and only require a few external components for operation.

The following article describes such a counter; it can be used for a large number of applications, and its four digits can be preset to any required values. This means that it is possible to measure the oscillator frequency of a receiver or transceiver, to preset the intermediate frequency and then indicate the receive or transmit frequency directly. The actual display has six digits; the two highest digits can be wired as required, for instance to 14X.XXX MHz for 2 m in equipment. The counter can count up or down, which means that it can be used also in equipment where the intermediate frequency is higher than the operating frequency. The frequency counter shown in **Fig. 1** is accommodated in a tin plate case of approximately 13.5 cm x 5 cm x 3 cm together with its preamplifier and prescaler, whose upper frequency limit is in excess of 40 MHz.

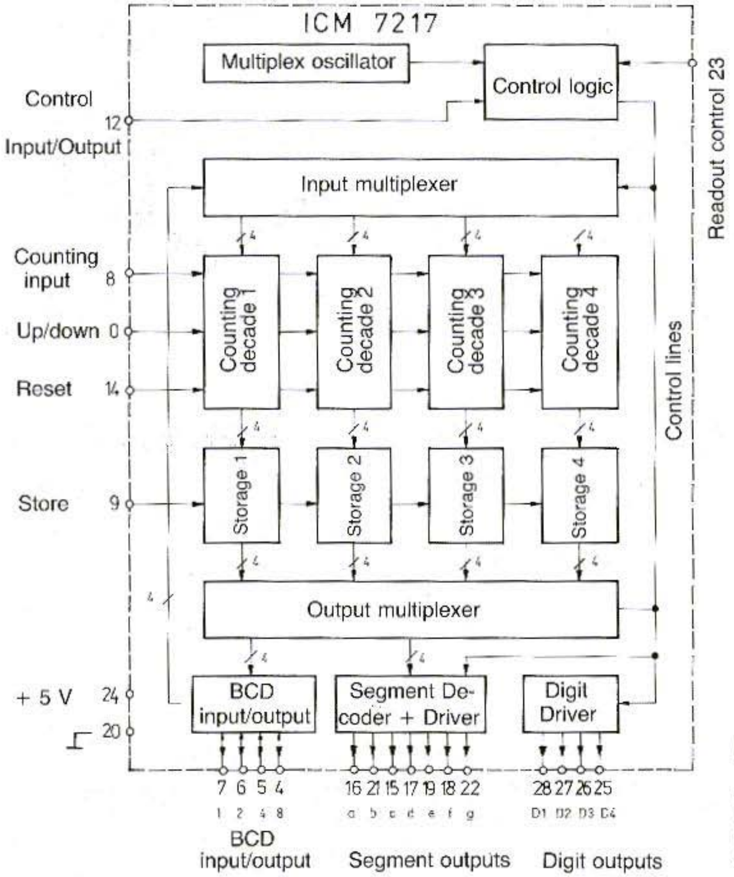


Fig. 2: The highly-integrated counter module ICM 7217 operates using a multiplex system

1. MOS-LSI-CIRCUIT ICM 7217

Figure 2 shows the simplified block diagram of the counter module used. As can be seen, a cascade circuit of four counting decades is used, which are fed with the input frequency via connection 8. A pulse fed to pin 14 (»reset«) resets all decades to 0. The counter can be switched to up or down operation via pin 10. If an impulse is fed to connection 8 (»store«), the four storages will then accept the momentary state of the counter decades. Up to here, there is no difference to the normal, descrete technology.

One feature of LSI-modules (large scale integration) is that the data inputs and outputs are not fed out individually due to the limited number of connection pins, but are multiplexed. In our case, this means that the output multiplexer interrogates stores one to four and feeds the actual storage contents in a cycle to the seven-segment decoder/driver, to which the parallel-connected segments a to g of the digital readout are connected. The control logic then switches on the required »part« of the display via the digit driver.

As was previously mentioned, it is possible for the counting decades to be programmed (»set«) so that the count does not commence at »0000«, but at any required number (this is the same as when adding the counting impulses to a preset number). The input multiplexer is used for this application and passes on the information from the BCD-input/output unit one after another to the 4 counting decades. The input/output unit can also be requested to output the contents of the four storages in sequence in a BCD-format by placing an order at pin 12. The association of the actual BCD »word« is determined by the digit-outputs; if, for instance, D 2 is at H-level (»high«), this will correspond to a BCD-output of the contents from storage 2.

Finally, the display can be controlled via connection 23; this allows the previous zeros to be suppressed, or for the display to be switched off completely. In this case, the operating current of the module amounts to less than 1 mA.

The following **Table 1** shows the operation of the individual control inputs of the module:

Input	Connection	Level	Function
Control	—	H	BCD-input
Input/Output	12	open	BCD-output
		L	Connections at high-impedance
Up/Down	10	H or open	Counts upwards
		L	Counts downwards
Reset	14	H or open	Counting
		L	Reset to 0000
Store	9	H or open	Storage remains unchanged
		L	Accept counter state
Readout	—	H	Readout switched off
control	23	Open	Previous zeros off
		L	Previous zeros on

Table 1: The control inputs of the ICM 7217 (H = + 5 V, L = Ground)

The LSI-circuit ICM 7217 also contains a number of further stages that are not necessary for the described application. For clarity, they have not been given in Figure 2. If further information is required, this can be obtained by ordering the manufacturer's data sheet.

2. CIRCUIT OF THE FREQUENCY COUNTER

The detailed circuit diagram of the counter is given in **Figure 3**. The input Pt 1 is followed by an emitter follower T 1, which feeds the switching transistor T 2 at low-impedance. A DC-feedback ensures that the operating points of the transistor are kept constant. Resistor R 1 determines the input impedance of the circuit. If a longer coaxial cable is to be used at the input, a resistance value in the order of 50 Ω should be selected. If the resistor is not provided, the input impedance will be in the order of 1 kΩ.

Since the counter module I 5 can only process relatively low frequencies, a ÷10-divider (I 1) is connected in front of it. The manufacturer of the ICM 7217 guarantees a maximum input frequency of 2 MHz; the three examples available to the author, however, counted up to in excess of 4 MHz without problems, which means that a frequency of up to 40 MHz can be fed to Pt 1. The maximum and minimum input levels were measured on the author's prototype and are given in **Figure 4**.

The required control signals for operating the counter are generated in integrated circuit I 3. The storage strobe pulse is taken from pin 2; connection 13 controls the counting gate I 4/4. The counting time is selectable via Pt 20/S 1. If S 1 is open, this will amount to 1 s, whereas it will be reduced to 0.1 s when the switch is on.

The reset impulse available at pin 14 is too short for the application described here. It is

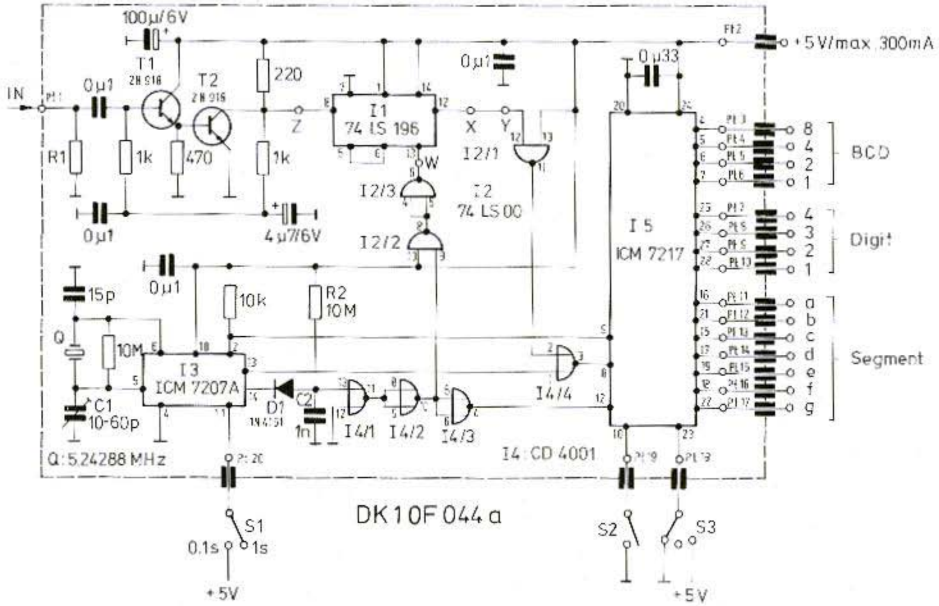


Fig. 3: This partial complement of the counter is sufficient for a number of applications

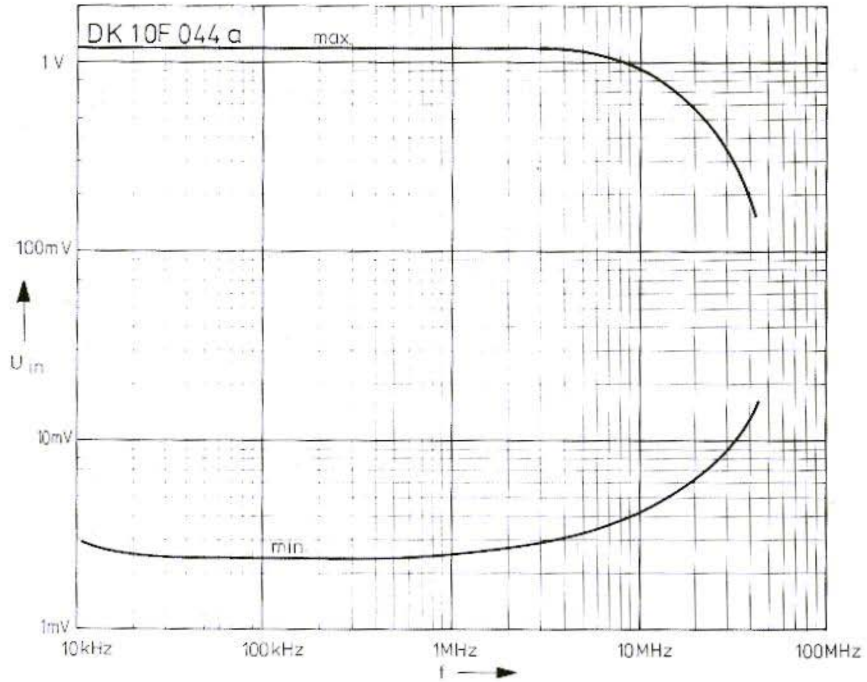


Fig. 4: Permissible input voltage range at Pt 1 for the counter shown in Fig.3

necessary for it to be available for at least a complete multiplex cycle, and for this reason, it is extended to approximately 10 ms with the aid of D 1, R 2, and C 2.

The prescaler I 1 is reset in synchronous during each counting cycle via the inverters I 2/2 and I 2/3, which suppresses a continuous jumping of the last decimal position. However, this only functions at relatively low input frequencies.

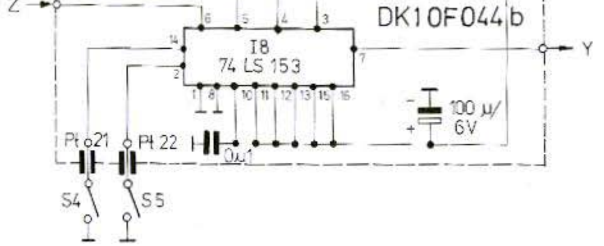


Fig. 5:
This circuit allows the resolution to be switched by 1 : 1000

Logic-level at Pt 20	 Pt 21	 Pt 22	Division by	Resolution	Readout	Max.Input Frequency
L	L	L	1	1 Hz	X.XXX kHz	4 MHz
H	L	L	1	10 Hz	XX.XX kHz	4 MHz
H	H	L	10	100 Hz	XXX.X kHz	40 MHz
H	L	H	100	1 kHz	X.XXX MHz	40 MHz
H	H	H	1000	10 kHz	XX.XX MHz	40 MHz

Table 2:
Variable frequency division ratios, and resulting resolution

Pt 20: L = S 1 off, H = S 1 on
Pt 21: L = S 4 on, H = S 4 off
Pt 22: L = S 5 on, H = S 5 off

In the previously described »Basic Complement«, the counter offers a resolution in the last digit of 10 Hz or 100 Hz, which is selectable with S 1, and the preselection is already taken into consideration by I 1, which means that the first digit possesses a valency of 10 kHz or 100 kHz. If the frequency counter is to be used universally, it is also necessary for the 1 MHz and 10 MHz positions to be indicated. This can be achieved by providing two further ÷10-dividers between point X and Y. **Figure 5** shows a circuit recommended for this.

The two decade counters I 6 and I 7 operate as prescaler and are also reset in synchronous in the same manner as I 1 via point W. Their inputs and outputs lead to I 8 (74 LS 153), which is a dual four-Bit demultiplexer, of which only one half is used. This allows the division ratio to be selected between 1 and 1000 in decades via the control inputs Pt 21 and Pt 22. This is indicated in Table 2.

A preamplifier with a high-impedance input and variable trigger threshold was provided in order to use the frequency counter for general measuring and test purposes. The circuit diagram of this preamplifier is given in **Fig. 6.**

Choke L 1 complements the output capacitance of T 3 and the input capacitance of T 4 to form a Pi-network, which allows the gain to be improved at the upper frequency limit. The most favorable value for R 3 is dependent on the spread of T 1; in the case of maximum gain (R 2 fully clockwise), a drain current of 2 to 3 mA should flow via Pt 24. The amplifier stages T 4 to T 6 are stabilized using a DC-feedback similar to that used for T 1 and T 2.

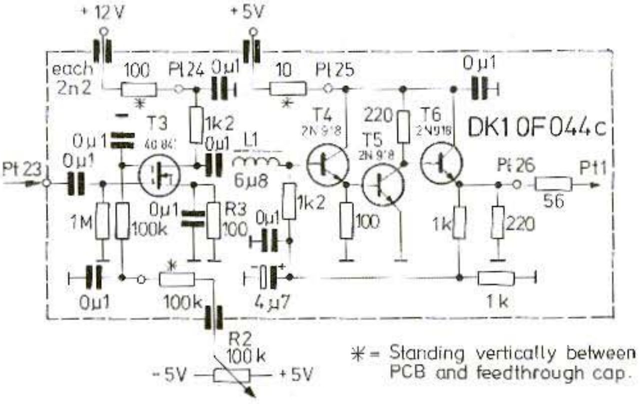


Fig. 6:
This high-impedance input amplifier increases the sensitivity of the counter and allows the frequency to be measured at any part of the circuit

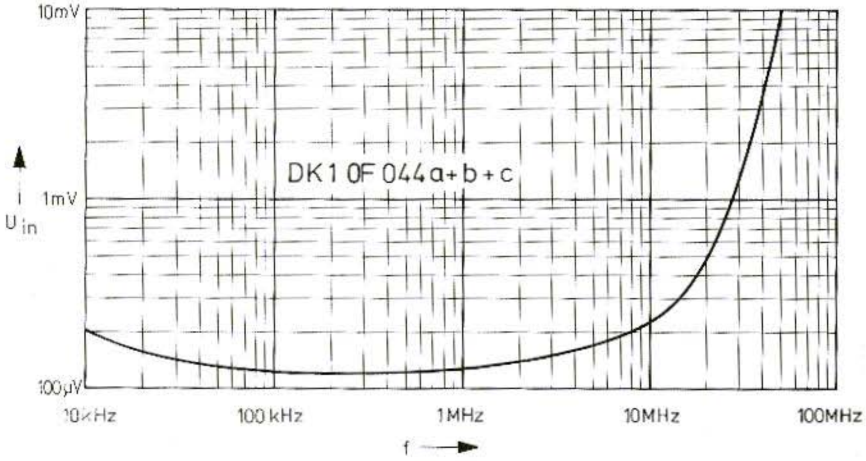


Fig. 7: Overall frequency response of the complete counter (Figures 3, 5, and 6): less than 1 mV is required up to 25 MHz

The frequency response of the input sensitivity of the overall counter is given in **Fig. 7**.

3. READOUT MODULE

Since the counter module I 5 already contains all decoder and driver stages, it is possible for conventional seven-segment digital readouts to be directly connected. Due to the multiplex operation, only 11 interconnection leads are required for the total number of 28 LED-segments. As can be seen in **Figure 8**, the segment connections a to g of the four lowest valency digits are connected in parallel. They are connected to corresponding outputs of the counter module (Pt 11 to Pt 17 in Fig.3); the common anode connections D 1 to D 4 are connected to the digit outputs (Pt 7 to Pt 10).

The anodes of the display modules A 5 and A 6 are directly connected to the supply voltage via connection A; the light-segments can be operated via external 270Ω dropper resistors (see **Table 3**).

The decimal points can also be operated via external dropper resistors (connections DP 1 to DP 6). Attention should be paid, however, that different resistance values are required due to the demultiplexed (A 1 to A 4) or DC (A 5, A 6) method of operation in order to ensure the same brightness.

Decimal No.	Required connections
0	a, b, c, d, e, f
1	b, c
2	a, b, d, e, g
3	a, b, c, d, g
4	b, c, f, g
5	a, c, d, f, g
6	a, c, d, e, f, g
7	a, b, c
8	a, b, c, d, e, f, g
9	a, b, c, d, f, g

Table 3:
Fixed wiring of required digits

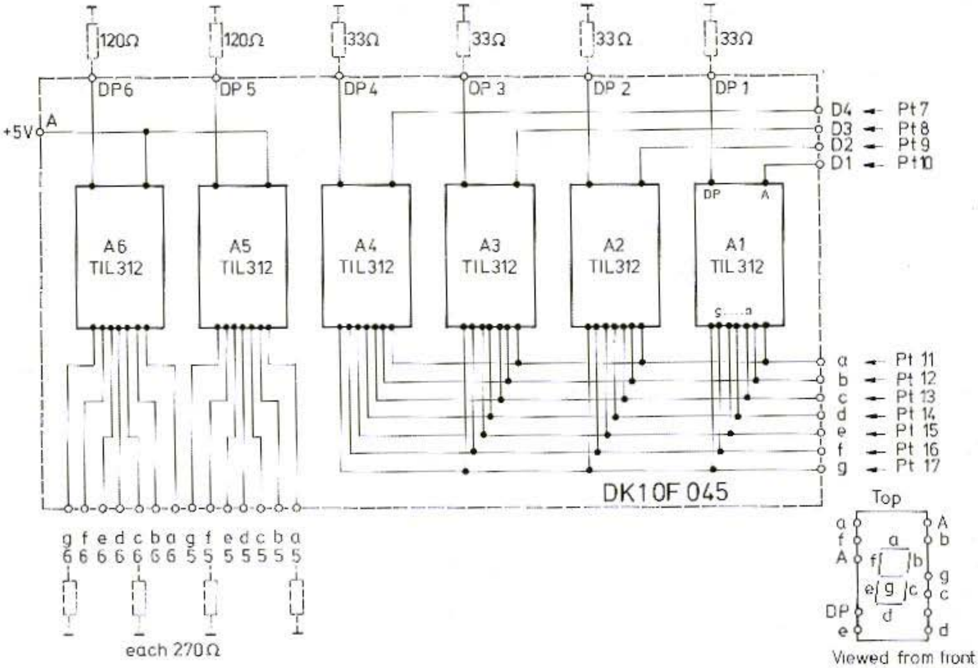


Fig. 8: **The first two digits of the 6-digit readout can be wired to any required number**

4. PROGRAMMING THE COUNTER

If the BCD-inputs of the counter module (Pt 3 to Pt 6 in Fig.3) remain disconnected, the count will be based on »0000«. The preselection of the individual decades is made – as previously mentioned – using a multiplex method. This means that if digit 4 (A 4) is to be set to a certain value, it is necessary for the associated bit series to be also entered to the BCD-inputs, if digit-output 4 is active (H). This can easily be achieved using a diode matrix as shown in **Figure 9**.

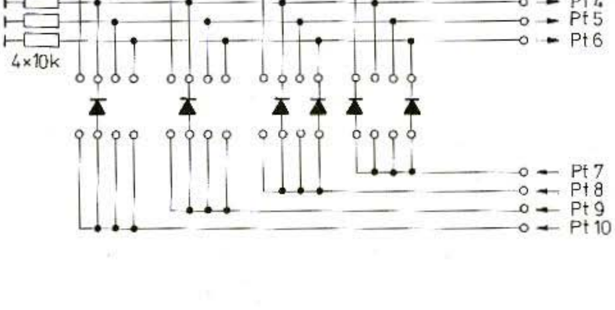


Fig. 9:
A fixed programming of the counter is made with diodes as shown in this example (example: 9544)

Preselection	Required diodes
0	–
1	A
2	B
3	A, B
4	C
5	A, C
6	B, C
7	A, B, C
8	D
9	A, D

Table 4:
Programming of the counter

Up to now, we have only spoken of an addition of the preselected number and the counting frequency. A subtraction can also be made easily by programming the complement instead of the constants. This is best explained with the aid of an example:

The counter is to provide a frequency readout for a medium-wave radio with an IF of 456 kHz (4-digit, last digit = 1 kHz). In the case of an input frequency of 1287 kHz, the oscillator will run at 1743 kHz. The program is made at the complementary value of the IF (10000 – 456) which is 9544. The readout is then:

Preselection:	9544
Oscillator frequency:	+1743
Readout:	11287

The carry-1 is, of course, not indicated so that a receive frequency of 1287(kHz) is indicated.

It is, of course, possible for the programming to be made with the aid of a digital switch as shown in **Figure 10**. If such a switch is used that possesses a longer connection board such as Contraves-type M 140 L, it is possible for the required diodes and resistors to be accommodated on this.

The previously described preselector circuits have the disadvantage that they are not grounded, and cannot always be driven by a grounded logic. This would, for example, be necessary on switching bands, if the frequency counter is used as readout for a shortwave transceiver.

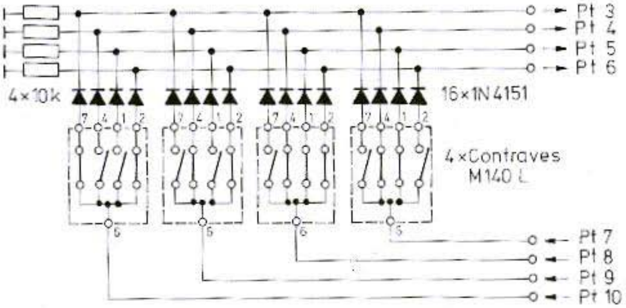


Fig. 10:
If the programmed value is to be changed, this can be made using a digital switch (4 positions)

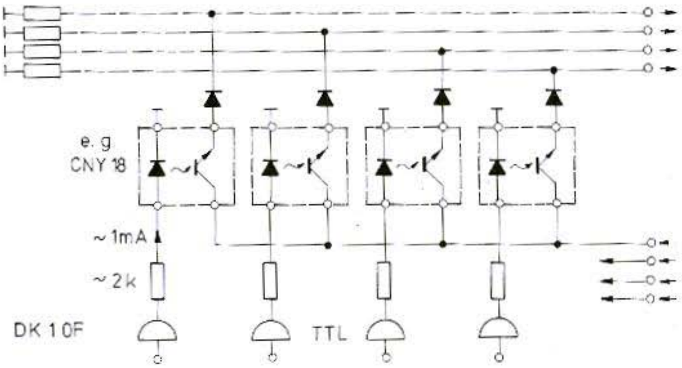


Fig. 11:
The counter can be electronically programmed with the aid of opto-couplers

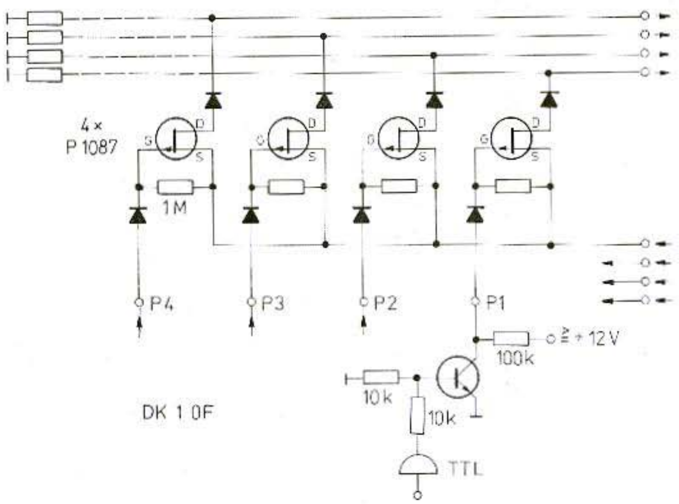


Fig. 12:
This circuit also allows the counter to be remote-controlled

One way of solving this problem would be to use an opto-coupler (LED and photo transistor in a common case) as indicated in **Fig.11**, or to use switching FETs as shown in **Fig.12**. Only one decade was shown in these drawings.

The programming inputs (P 1 to P 4) require a relatively high voltage for H-level (≧ 12 V) in order to ensure that the FETs are blocked. High-level logic (HLL) modules or MOS-switches with a supply voltage of 15 V can be directly connected.

5. CONSTRUCTION

Two double-coated PC-boards with through-contacts were developed for accommodating the frequency counter. The dimensions of PC-board DK1OF044 is 135 mm x 50 mm and can be enclosed in a metal-plate case. This case accommodates the circuits given in Figures 3, 5, and 6.

The screening panels shown as dashed lines in the component location plan **(Figure 13)** are not absolutely necessary.

When operating the frequency counter together with a transmitter or receiver, it is advisable to completely screen the whole frequency counter module and to bypass all connections with the exception of the counting input with the aid of feedthrough capacitors. **Fig.14** shows a frequency counter constructed in such a manner.

The readout board DK1OF045 has dimensions of 90 mm x 30 mm. It is only the seven-segment readouts that are mounted on this board **(Figure 15)**. Two connections are provided for the decimal points so that one can use the readout modules with left-hand or right-hand point.

SPECIAL COMPONENTS

I 1, I 6, I 7:	74 LS 196 N (Tex.Instr.)
I 2:	74 LS 00 N (Tex.Instr.)
I 3:	ICL 7207 A (Intersil)
I 4:	CD 4001 (RCA and others)
I 5:	ICL 7217 IJI (Intersil)
I 8:	74 LS 153 N (Tex.Instr.)
T 1, T 2, T 4, T 5, T 6:	2 N 918, 2 N 709, 2 N 5179
T 3:	40841, 40673 (RCA)
Q:	Crystal, 5.24288 MHz, HC-18/U, solder mounting
C 1:	Plastic foil trimmer 10-60 pF 10 mm dia.
L 1:	Ferrite choke, 6.8 μH spacing 10 mm

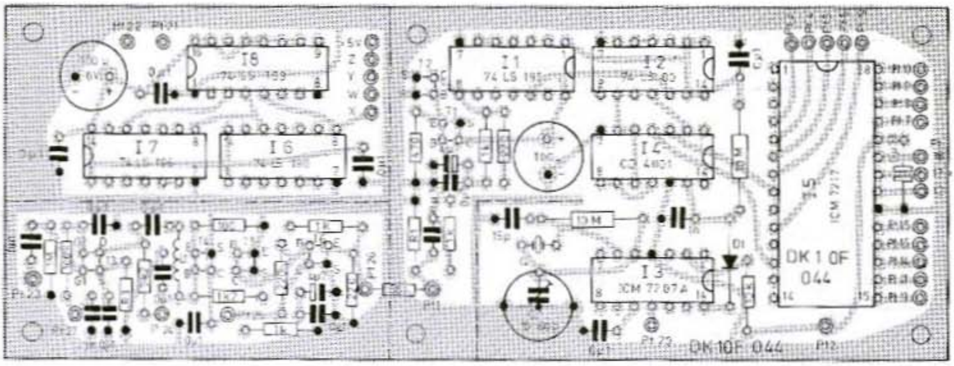


Fig. 13: Component locations on the double-coated PC-board DK 1 OF 044, with through-contacts

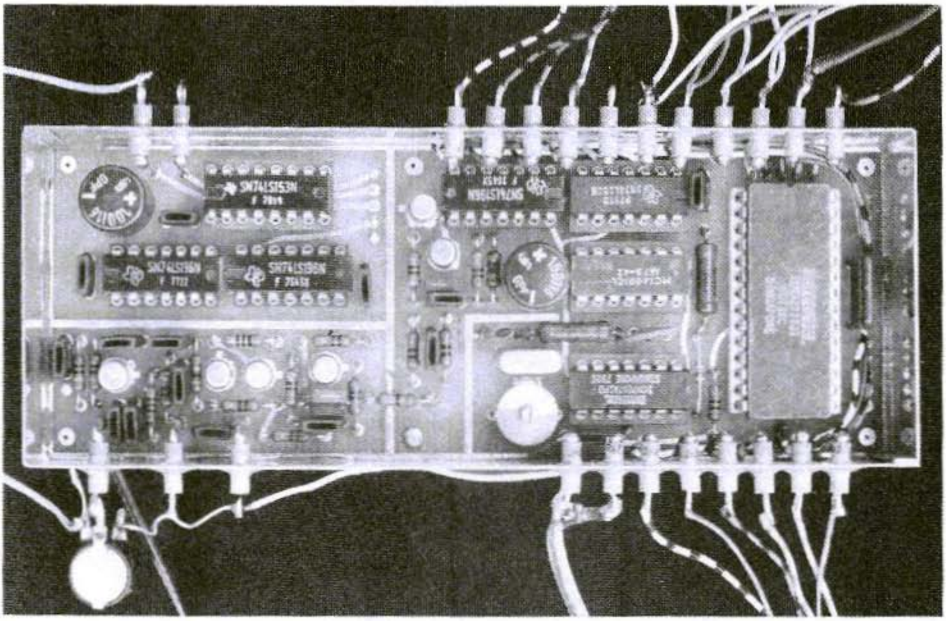


Fig. 14: A photograph of the author's prototype built into a metal-plate case and provided with feedthrough capacitors. This is suitable for installation in a receiver.

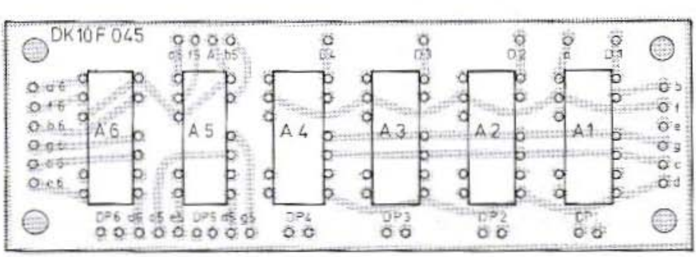


Fig. 15: Component locations on the readout board showing the conductor lanes on the conductor side

All capacitors with the exception of electrolytics: Ceramic disks or multilayer types

All diodes: 1 N 4151 or any other silicon
diodes

A 1 to A 6: Seven-segment readouts
TIL 312 (Tex.Instr.) or
MAN 72A (Fairchild) or
DL 707 *)

*) Type DL 707 has three anode connections that must all be connected !

Alignment and testing is limited to checking the drain current of T 3 to 2 to 3 mA with the aid of a suitable value of R 3.

The oscillator trimmer C 1 is adjusted most simply by providing a known frequency to the input and adjusting the trimmer for correct readout.

It should be noted that a crystal-controlled frequency of 1.28 kHz (keying ratio 1:1, CMOS-level) is available at pin 12 of I 3, which can be used, for example, for a digital AFC.

6. FINAL NOTES

Naturally, a suitable prescaler is necessary for VHF/UHF applications. If one uses the prescaler described in (1) with TTL-output, it is possible for transistors T 1, and T 2, as well as the associated components to be deleted, and for the output signal to be directly connected to point Z (Fig.3). If a longer coaxial cable is required between prescaler and counter (more than 20 cm), it would then be better to keep the stages T 1/T 2 (R1 = 56 Ω) and to provide a dropper resistor of approximately 1 kΩ at the input of the cable.

A seven-digit version of the described counter is in the process of development; if there is sufficient interest, further details will be given regarding this later.

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A Linear Amplifier for 1250 MHz Using the BFQ 68

by G. Sattler, DJ 4 LB

The transistor BFQ 68 was mainly developed for wideband amplifier applications in the frequency range of 40 to 860 MHz. However, this transistor is also suitable for power amplification in the 1250 MHz amateur band. Four transistors are connected in parallel in the SOT 122 case (metal/ceramic with screw stud), compared to two transistors in the case of the BFQ 34.

The manufacturer gives an output voltage of 1.5 V into 75 Ω for an intermodulation rejection of 60 dB at 800 MHz. This corresponds to an output power of 30 mW. At larger drive levels, it is easily possible to obtain approximately two Watts of linear RF-power output in the frequency range 1250 to 1300 MHz. This makes the described amplifier suitable for SSB applications in the 1296 MHz band, and ATV applications at 1252 MHz.

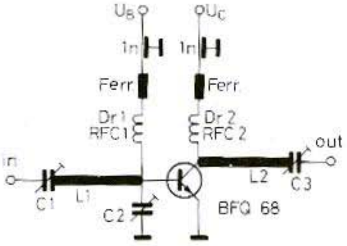

Fig. 1: This stage can provide an output power of approximately 1.7 W in the 24 cm band

CIRCUIT DESCRIPTION

Figure 1 shows the RF-circuit diagram of a linear amplifier equipped with the BFQ 68. It will be seen that this is not very different from that described in (1). **Figure 2** gives a recommended circuit for the supply voltages of the transistor BFQ 68.

An NPN-transistor connected as emitter-follower supplies the base voltage for the RF-power transistor. Two silicon diodes are connected in series; one compensates the temperature drift of the emitter-follower itself, and the other the temperature drift of the RF-power transistor. A constant quiescent collector current within 5% is obtained within an ambient temperature range of − 20 to + 60°C using the combination of four diodes (instead of a 7 V 5). The required value can be adju-

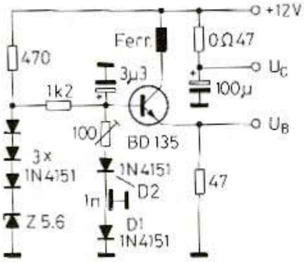

Fig. 2: Diode D 1 must be in thermal contact with the BFQ 68 transistor in order to keep the quiescent current constant. D 2 should be in contact with the BD 135

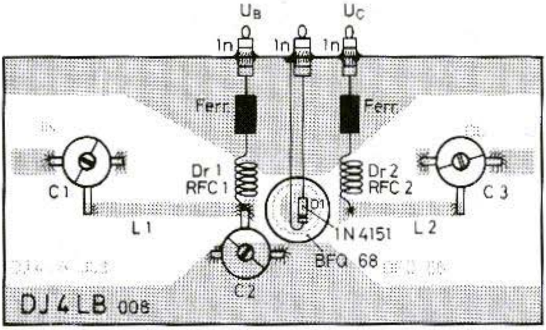

Fig. 3:
Solder the components to the conductor side of the board

sted using a resistor connected in series with the diodes and checking the voltage drop across the 0.47 Ω resistor.

MAJOR COMPONENTS

1 BFQ 68 (Philips)
1 BD 135, BD 137 or BD 437 (Siemens)
1 C 5 V 6 zener diode

C 1:	Plastic-foil trimmer, 22 pF (green), 7.5 mm dia.
C 2, C 3:	Plastic foil trimmer, 6 pF (grey), 7.5 mm dia.
RFC 1 and 2:	λ/4 chokes; 6 cm of thin enamelled-copper wire wound to 3 mm diameter

3 feedthrough capacitors; 1 nF
3 ferrite beads.

CONSTRUCTION

To aid reproducibility, the RF-circuitry is accommodated on a double-coated, epoxy PC-board designated DJ 4 LB 008. The dimensions of this board are 72 mm by 35 mm, which can be accommodated in a plate-metal case.

The component locations are given in **Fig. 3**. It is possible for the auxiliary bias supply circuit to be mounted on the case in some suitable position. Further constructional details are shown in the photographs given in **Figures 4 and 5**. Either BNC connectors or direct cable connection is possible.

MECHANICAL CONSTRUCTION

1. Case

Drill the holes at both ends of the box for the coaxial cable or BNC connectors. Drill three holes on one side for the feedthrough capacitors, and a hole for mounting the BD 135 transistor.

2. PC-Board

Drill a hole with a maximum of 7.5 mm diameter for the BFQ 68 transistor at the marked position. Saw two thin slots along the edge of the copper coating (one short and one somewhat longer) in the direct vicinity of the emitter connections and make through-contacts to the other side of the board as described in (1). File out the ends of the board suitable for mounting the BNC-connectors or coaxial cable. Finally fit the board into the case.

3. Assembly

Insert the PC-board with a spacing of approximately 1 mm to the lower edge of the case and solder on both sides. The heat sink should fit well to the flange of the transistor but need not touch the bottom of the case.

Before soldering the BFQ 68 into place, cut the base and collector connections so that they do not protrude over the wide ends of the striplines on the PC-board. Also shorten the emitter connections.

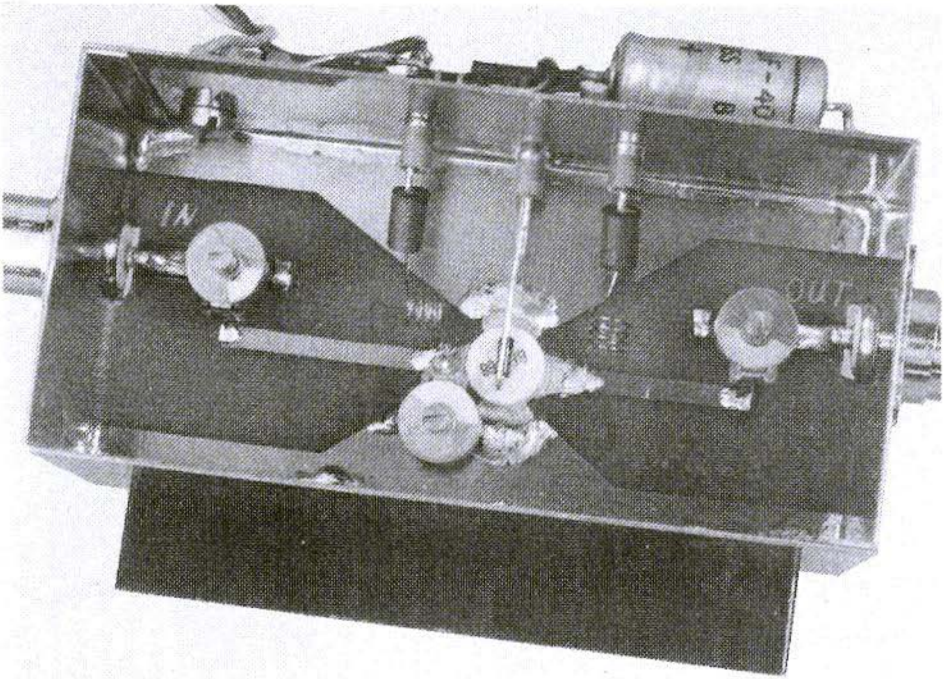

Fig. 4: Photograph of the author's prototype

Mount the silicon diode for temperature compensation: Solder the cathode connection wire to the case so that the diode touches the power transistor (use heat-conducting paste), and bend back the anode connection in a tight turn and solder to its feedthrough capacitor.

Do not forget the two ferrite beads at the cold end of the λ/4 chokes. Place a mica disc on the outside of the case before screwing the BD 135 transistor into place tightly. Finally screw the heatsink into place and pad any remaining spacing between heatsink and case to increase mechanical stability.

CONNECTION AND ALIGNMENT

1. The auxiliary circuit for generation of the base voltage should be checked separately. The DC-voltage at the output of the emitter-follower should be adjustable between 0.7 and 0.95 V.

2. Connect the auxiliary circuit to the actual linear amplifier. Terminate input and output of the linear amplifier with 50 Ω. Align the collector current of the BFQ 68 to approximately 300 mA. After this, measure the resistance

Output power	P_{out} (W)	0.5	1.0	1.5	2.0	2.5	3.0
Collector current	I_C (mA)	280	290	320	370	440	560
Power gain	V_P (dB)	8.5	8.1	7.7	7.3	6.5	5.8

Table 1

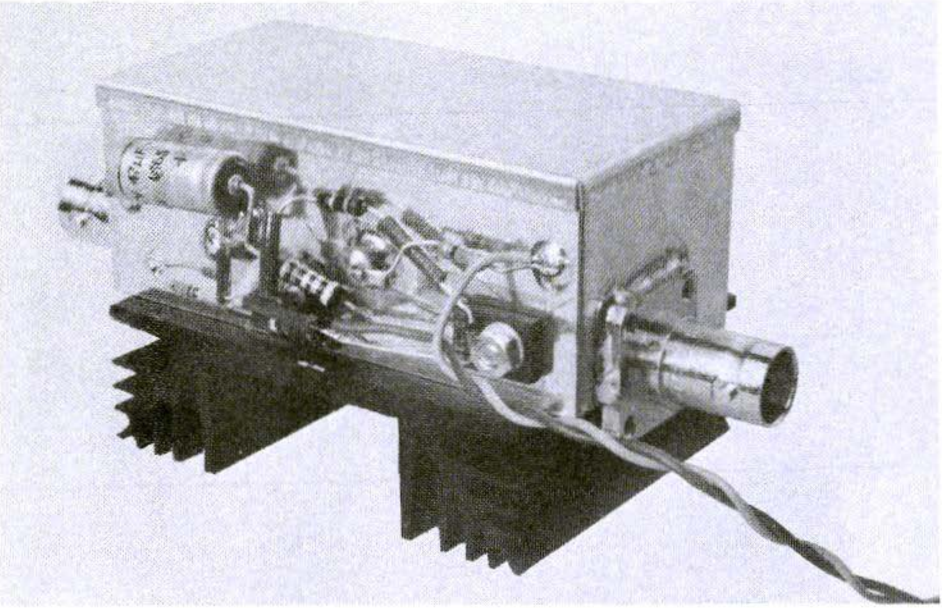

Fig. 5: Photograph showing the base-bias circuit from Fig. 2

value of the trimmer potentiometer and replace with fixed resistors to ensure that the expen-sive power transistor will not be destroyed by a cheap, defective potentiometer at later date.

3. Initial setting of the trimmer capacitors: C 1 fully inserted, C 2 30% capacitance, and C 3 20% capacitance. Drive the linear amplifier with a signal between 1250 and 1300 MHz, initially using an attenuator or long coaxial cable between exciter and input of the linear amplifier in order to protect the exciter (e.g. DF 8 QK 001) against too high a mismatch.

4. Alignment: Only increase the drive power until the wattmeter at the output just shows some indication. After this, correct the alignment of trimmers C 3 and C 2. Slowly increase the drive power, correcting the trimmer adjustments at each step. Never try and rotate the trimmer capacitors by 360° at full drive thinking that you may find a better setting ! The position of most favourable input matching is found by reducing the value of trimmer C 1 from maximum towards half capacitance, which will be indicated by a slight increase of output power. This can be checked with the aid of a reflectometer.

Table 1 gives values measured on the author's prototype with an operating voltage of 12 V. The maximum permissible collector current of 300 mA for continuous operation as given by the manufacturer, was exceeded during this measuring run.

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J. Dahms, DC 0 DA:
A Transistorized Linear Amplifier for 1296 MHz
VHF COMMUNICATIONS 11, Edition 1/79, pages 17-26

Constant-Amplitude PLL-SSB on the UHF and SHF bands

by O. Frosinn, DF 7 QF

Constant-amplitude SSB was introduced several years ago. In this method, a constant-amplitude SSB-signal is generated at IF-level, and subsequently mixed up to the required band. This phase-locked loop SSB was first introduced in VHF COMMUNICATIONS in (1). At that time, the main reason for using this mode was to avoid interference in neighbouring radio and television receivers.

The task of this article is to find a method based on this concept that allows a transmitter containing frequency multiplier stages to generate SSB. The basic fundamentals of such a system are to be described here.

There are three main possibilities of generating a transmit signal in the UHF and SHF bands (432 MHz, 1296 MHz, 2404 MHz, and 10 GHz).

1) Superheterodyne type transmitter
2) Frequency multiplier transmitter
3) Free-running oscillator

All modulation modes are possible in the case of a superheterodyne transmitter, whereas only FM and CW are possible when using a frequency multiplier system, and only FM will be possible when using free-running oscillators such as the Gunn-element oscillators used at 10 GHz.

This, of course, indicates that a superheterodyne method seems to provide the best possibilities. However, it is very difficult and expensive to manufacture the required linear power amplifier for the microwave frequencies. The alternative method described in (2) using a parametric up-converter also has disadvantages, namely the required, expensive power varactors (2 pieces !), the inavoidable conversion losses, and its tendency to unwanted oscillation.

Of course, frequency modulation can be used for short to medium paths, and a crystal-controlled transmitter equipped with frequency multipliers will be sufficient for this; if the signal was weak, it would be possible for it to be keyed in the CW-mode. However, if communication is to take place at higher path losses (troposcatter !) and when one's communication is to be made at low field strength, this will mean that SSB will be required even at these higher frequencies. This was underlined in an interesting experiment described in (3).

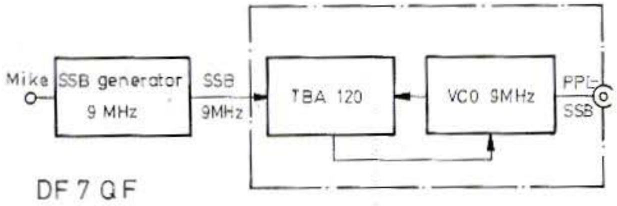

Fig. 1: Block diagram of a circuit for generating PLL-SSB as described by PA O EPS

1. PLL-SSB

As was mentioned in the introduction, phase-locked loop SSB was mainly used to avoid BCI and TVI. This signal sounds like an infinitely (100 %) clipped SSB-signal and will require more bandwidth than normal SSB. In order to maintain a constant amplitude, the suppressed carrier, which is normally approximately 30 dB down, is amplified in the pauses between words up to the full amplitude of the PLL-SSB signal.

A simple manner of generating such a signal is shown in the block diagram in **Figure 1**. The output signal is subsequently processed further in the usual manner by conversion and linear amplification.

2. MULTIPLIED PLL-SSB

Starting with the basic circuit given in Fig. 1, a method was experimented with that allowed a SSB-signal to be generated in a frequency-multiplier type transmitter. Frequency multiplication seemed possible since the signal had a constant amplitude, and the information was in the form of frequency modulation.

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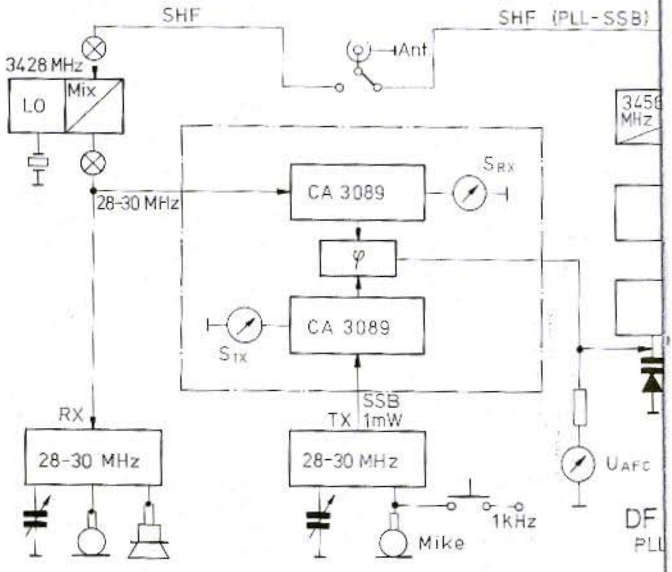

Fig. 2: PLL-SSB on the 9 cm band, using a 10 m transceiver

plified here, limited and fed to the phase comparator. At the same time, the SSB-signal from a 10 m transmitter is fed to the CA 3089 in the transmitter, which is also amplified, limited and fed to the phase comparator. The carrier suppression of the transmitter should not be too great in order to ensure that the phase-locked loop can lock-in in the pauses between words.

The control voltage from the phase comparator is fed via a low-pass filter to the varactor diode of the voltage-controlled crystal oscillator (VCXO).

This means that the voice frequency is not superimposed on the control voltage as interference, as is the case with PLL FM-transmitters, but the control voltage will be varied in time with the modulation. The low-pass filter is therefore only used for suppressing interference peaks, which are generated by the phase jumps in the phase comparator when driven with an SSB-signal.

As one can see, the transmit frequency in the SHF-band (in our case 3456 MHz) is dependent on the frequency of the 10 m transmitter and that of the local oscillator (LO) of the receive converter.

Here two examples:

1. LO correct, TX to 28.2 MHz:
   TX = 28.2
   LO = 3428
   SHF = LO + TX = 3428 + 28.2 = 3456.2
   RX = SHF − LO = 3456.2 − 3428 = 28.2
   VCXO = SHF ÷ 72 = 3456.2 ÷ 72 = 48.002777
2. LO has frequency shift, TX at 28.2 MHz:
   TX = 28.2 (Δ LO = 0.1 MHz)
   LO = 3428.1 (Δ LO = 0.1 MHz)
   SHF = LO + TX = 3456.3
   RX = SHF − LO = 28.2
   VCXO = SHF ÷ 72 = 48.004166

The transmit signal will therefore still appear in the receiver at the frequency of the transmitter, although the LO has a frequency shift of 100 kHz. However, the SHF-signal is incorrect to the value of these 100 kHz.

If the TX and RX are aligned to 28.0 MHz, it is necessary for the crystal in the VCXO to oscillate at 48.00000 MHz. This must be checked with a sufficiently accurate counter. A detuning of the TX by, for instance, 500 kHz and thus a frequency change at SHF by 500 kHz corresponds to a variation of the frequency of the variable oscillator by 500 ÷ 72 = 6.94444 kHz. These values in the range below 1 Hz mean that great demands are placed on the frequency generation with respect to frequency stability and accuracy.

3. OPERATING AND CONSTRUCTION DETAILS

A modified DJ 4 LB 003 circuit using a 96 MHz crystal was found to have too low a pulling range (only 10 kHz in the 13 cm band !) For this reason, the author decided to use the older circuit as described by DJ 9 ZR in (4). A 48.015 MHz crystal was used, and subsequently doubled so that a frequency multiplier chain based on the usual 96 MHz oscillator could be used. The pulling range was adjusted according to the alignment instructions given in (4), and could be monitored easily by listening to the signal at the third harmonic of 48 MHz x 3 = 144 MHz.

With the aid of the AFC-voltage from the CA 3089, a pulling range of 250 kHz was obtained on the 13 cm band, or 375 kHz on the 9 cm band. By the way, this VCXO provides a very clean, stable signal in the 13 cm band when fed with a stable DC-voltage !

The modules are then interconnected as shown in Figure 2, and fed with a variable DC-voltage of between 2 and 10 V via the AFC-input of the VCXO. Both meters S_{RX} and S_{TX} should indicate values in excess of S 9, and the needle of the transmit S-meter S_{TX} should increase by 20 to 30 dB during modulation. If the S_{TX} indicates too low a level, it may be necessary for the drive power in the 10 m band to be increased. This may mean that the carrier suppression in the SSB-mode may have to be reduced.

If the transmitter is switched to »FM«, the S_{TX}-meter should indicate the same value as when modulating in the SSB-mode. CW-transmission is possible in the SSB-mode by keying an audio generator.

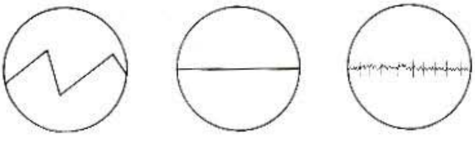

Fig. 3: Oscilloscope traces of the control voltage left: unlocked, center: locked-in, right: locked-in and modulated

As has been previously mentioned, the suppressed carrier should not be too greatly suppressed in the SSB-mode since the PLL-circuit requires a certain amount of signal in the pauses to remain locked in. On the other hand, the suppressed carrier should not be too strong, since it would take up too large a component of the output power. A compromise must be found experimentally. If S_{RX} indicates too low a level, this will mean that the coaxial relay will have too high an isolation. In this case, somewhat more power can be fed to the converter using a directional coupler. Of course, one can also provide an additional preamplifier stage in front of the 28 MHz receiver, which should not have too low a bandwidth.

After both S-meters indicate the correct level, the tuning voltage at the VCXO is varied between 2 and 10 V, to see whether the required tuning range results in the SHF-band. This is checked on the receiver.

The receiver is now adjusted to the transmit frequency, which can be heard in the receiver due to the unwanted coupling and inferior cross-talk attenuation in the PLL-module. The AFC-voltage is now taken from the PLL-module and fed to the VCXO: If the transmit frequency is within the pulling range of the VCXO and in the capture range of the phase comparator, the VCXO will be pulled to the correct frequency. At the same time, the field strength indicated on the S_{RX}-meter will increase considerably.

Fig. 3 shows how the control voltage appears in its unlocked, locked, and finally in locked and modulated state. If the PLL does not lock in, the transmit frequency should be tuned until the signal is captured, and then tuned to the required frequency (within the AFC-voltage range of 2 to 10 V).

It will be seen that this very simple circuit has several disadvantages:

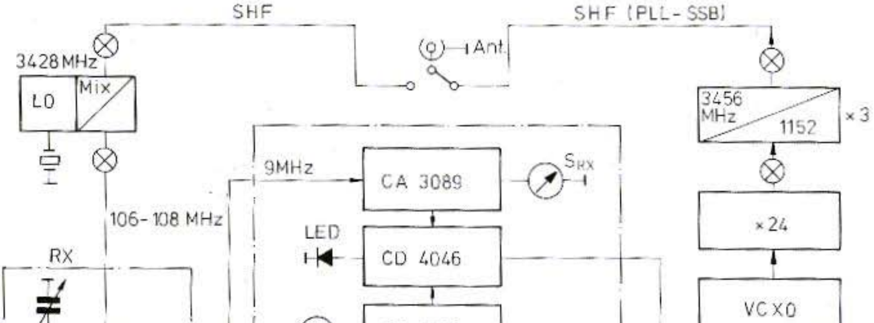

Fig. 4: PLL-SSB on the 9 cm band, using a 9 MHz IF

Capture and pulling range do not coincide; The circuit does not indicate the lock-in state.

It is possible, however, to monitor the value of the control voltage using a high-impedance voltmeter, and this should be done in practice. It would be even better if the value and state were monitored on a DC-coupled oscilloscope. In the case of a sufficiently stable construction of the modules, and some experience with this system, it is sufficient that the signal be monitored in the receiver, as well as monitoring the control voltage. In any case, this PLL-circuit is so simple and the expense so low in comparison to the advantage of being able to transmit SSB in conjunction with a frequency-multiplier transmitter that it is well worth experiment.

4. THE IF-METHOD

The circuit given in Fig. 2 was then extended to find a further method, which is shown in **Figure 4**. In this case, the phase comparison is carried out at the low, fixed IF of the receiver. However, it is necessary for the IF to be tapped off in front of the crystal filter, which means that a slight modification must be made to the receiver.

This circuit requires only a SSB-generation at the same frequency as the receiver IF, which is usually 9 MHz; the tuning of the output frequency in the SHF-band is made using the VFO of the receiver.

It is possible to use integrated MOS-circuits here (low current drain !), which means that an additional conversion of both frequencies to frequencies below 5MHz would be required when using the described 28 MHz method.

As can be seen in the block diagrams, any frequency multiplication factor can be used. When using a local oscillator frequency of 1152 MHz, it is only necessary to change antenna, converter and transmit multiplier !

5. SSB IN CONJUNCTION WITH A GUNN-OSCILLATOR

After successfully carrying out the experiments with frequency-multiplier transmitters (successful with exception of the efficiency), the next experiment was to attempt »locking-in« a Gunn-oscillator. It was found, unfortunately,to be too extensive to take the whole fixed transmit system to a 10GHz portable location.

A Gunn-oscillator as described by DL 6 MH in (5) was constructed and provided with an additional GaAs-varactor for electronic tuning. A PTFE-screw is used to tune the frequency to within the capture range of the PLL; after locking in, the Gunn-frequency is just as stable as that of the local oscillator in the converter or the SSB-transmitter. When using suitable Gunn-elements, an output power of several hundred mW can be generated in the 10 GHz band. **Fig. 5** shows a block diagram of the author's 10 GHz station.

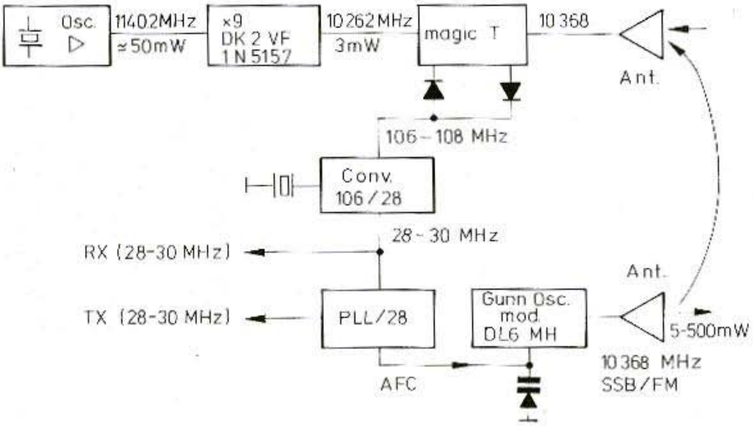

Fig. 5: PLL-SSB using a Gunn-oscillator for 10368 MHz

6. FINAL REMARKS

PLL-SSB appears »wider« than normal, converted SSB. However, this should be acceptable on the higher SHF-bands, especially since an incorrectly aligned varactor up-converter can also generate an unpleasant signal when not aligned with the aid of a spectrum analyzer ! Furthermore, it should be noted that the described method is not free of faults. The described circuits are given more as an incentive for further considerations and experiments, and are not by any means considered to be the final conclusion.

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Chokes for Contactless Tuning of Waveguide Modules

by E. Schäfer, DL 3 ER

Plungers are required for matching and tuning waveguide modules such as oscillators, detector probes, mixers etc. However, they are difficult to construct at home due to the close tolerances resulting when using the rectangular waveguide usually employed by radio amateurs together with the H_{10}-(TE_{10}-)wave. Since the currents of the H_{10}-wave run vertically in a rectangular waveguide, it is not necessary for the plunger to have contact to the narrow side of the waveguide; however, it is difficult enough to make good contact with the wider-side if a continuous variation is to be made without jumps.

It is also difficult to fix the tuning plunger after alignment. Soldering into place is not advisable, since a necessary realignment after changing a component would not be possible. Also locking with a screw is not suitable, since this could damage the contact surfaces.

The described contact-less choke system avoids many of these problems and can be easily manufactured.

The author is at present using such a system on the 24 GHz band for tuning of Gunn-oscillators, detectors, and mixers in rectangular waveguides type WR 42 and WR 28 (1). This system has not been tried at 10 GHz, however, the results obtained at the higher frequencies seem to indicate that it could be equally suitable for such applications.

OPERATION

A three-stage system of chokes is used, which are each $\lambda/4$ long. **Figure 1** shows how they are mounted in the waveguide. They remind one of coaxial low-pass filters with alternating high and low impedance $\lambda/4$ sections. The metallic portions do not touch the inside wall of the waveguide. A PTFE-collar (Part 2 in **Fig.2**) is provided behind the three choke

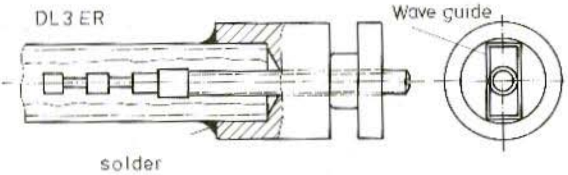


Fig. 1: Overall view of the choke system

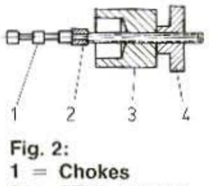
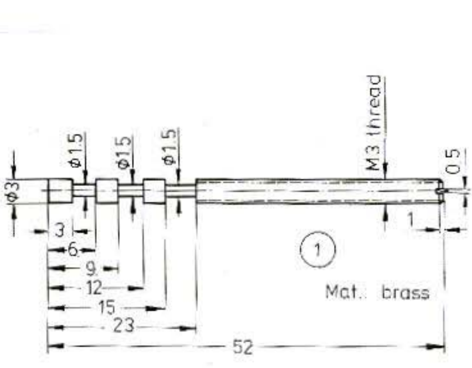
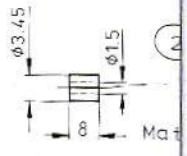
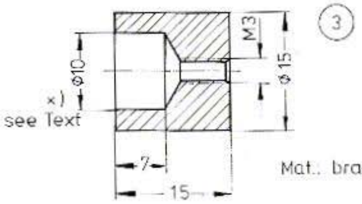
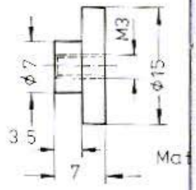


Fig. 2:
1 = Chokes
2 = PTFE support
3 = Guide bushing
4 = Fixing screw







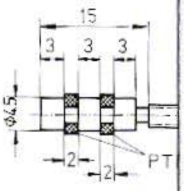


sections and is used as a support in conjunction with the threading in part 3.

A screw (part 4) is used to adjust and fix the plunger. The given dimensions **(Figure 3)** are suitable for the 24 GHz band when using a R 320 (WR 28 or WG 22) waveguide.

By the way, the length of the individual choke sections is not critical, and this system still works well at 33 GHz.

The whole choke system can be shortened by providing PTFE-discs at the high-impedance sections as shown in **Figure 4**. The velocity factor V ($V = 1 \sqrt{\varepsilon}$) is dependent on the relative dielectric constant ε, and will shorten the overall length from 23 mm to 15 mm in our ex-



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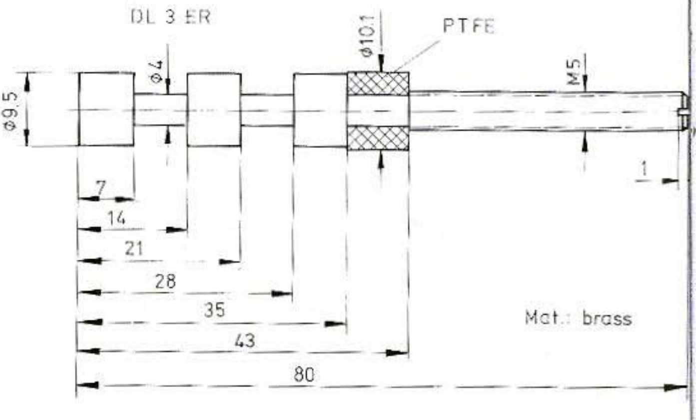

Finally, **Figure 5** shows the dimensions of a similar choke system for waveguide type R 100 (WR 90 or WG 16) at 10.3 GHz. The overall length of the choke system can be shortened from the 43 mm given in Figure 3 to approximately 32 mm by using two PTFE-supports. These discs should be 4.6 mm long and 10.1 mm in diameter. A length of 2 mm should be reduced to a diameter of 4 mm towards the threaded section after the end of the last choke section.

CONSTRUCTION TIPS

A lathe should be available for manufacturing the parts given in Figure 3. The 120° countersunk portion of part 3 is only provided to assist assembly. This part is soft-soldered to the end of the waveguide. The hole of 10 mm diameter (nominal) is matched to the outer diameter of the waveguide so that it fits tightly into part 3. When using different waveguides than R 320 (WR 28), the dimensions of part 3 should be made correspondingly larger. In the case of the 10 GHz band (waveguide R 100), this part can be provided with a threaded hole, and fitted as a rectangular brass block into the waveguide and fixed into place by soldering or using a screw (no electrical contact !). Anyway, the adjustment of the choke system is very stable and smooth due to the second support bearing provided by part 2. This is especially true when the slotted PTFE-collar (part 2) fits tightly in the waveguide. It may even be depressed somewhat so that there is no play at all. Since the diameter of the PTFE-collar is somewhat greater than the choke system, this ensures that no galvanic contact is made to the inside wall of the waveguide.

The surface of the choke system (part 1) should be smoothened after lathing using wet emery cloth (600) and subsequently polished with steelwool at a speed of 3000 r.p.m. This part will really be at its optimum if it is silver-plated; rub-on silver-plating is sufficient.

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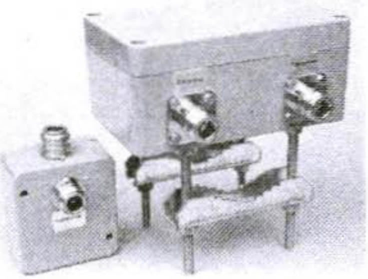


A New Method of Mounting and Feeding a Gunn Element Using a BNC-Connector

by K. Buchenrieder, DD 0 MQ

The following article is to describe a new method of mounting the active element in a 10 GHz transceiver. The Gunn element is held with the aid of a flange BNC-connector through which the operating DC-current is also fed. This technology represents a simple, mechanical solution and means that construction can be made using simple tools – hand-drill, fret-saw, and files – and using readily available parts (Figure 1).

DIODE-MOUNT USING A BNC-CONNECTOR

Figure 2 shows a drawing of the complete Gunn-oscillator; a cross section of the diode mount is given in **Figure 3**.

The Gunn-element (7) is held at the centre of the waveguide (5) with the aid of the grub screw (10), collar (6), and the BNC-connector (1). Two brass plates (4) and (8) are hard-soldered to the waveguide, so that this is strengthened enough to accept the grub screw, and the mounting screws (2). Four threads are cut in plate (4) for mounting the BNC-flange connector, and this must be done before soldering.

Since the grub screw possesses a hardened cutting edge, it is necessary for it to be softened firstly, using some form of flame (cigarette lighter is sufficient !). It is possible after this, for a hole to be drilled at the centre to accept the pin of the Gunn diode. The tubular piece (6) can be soft-soldered directly to the BNC-connector.

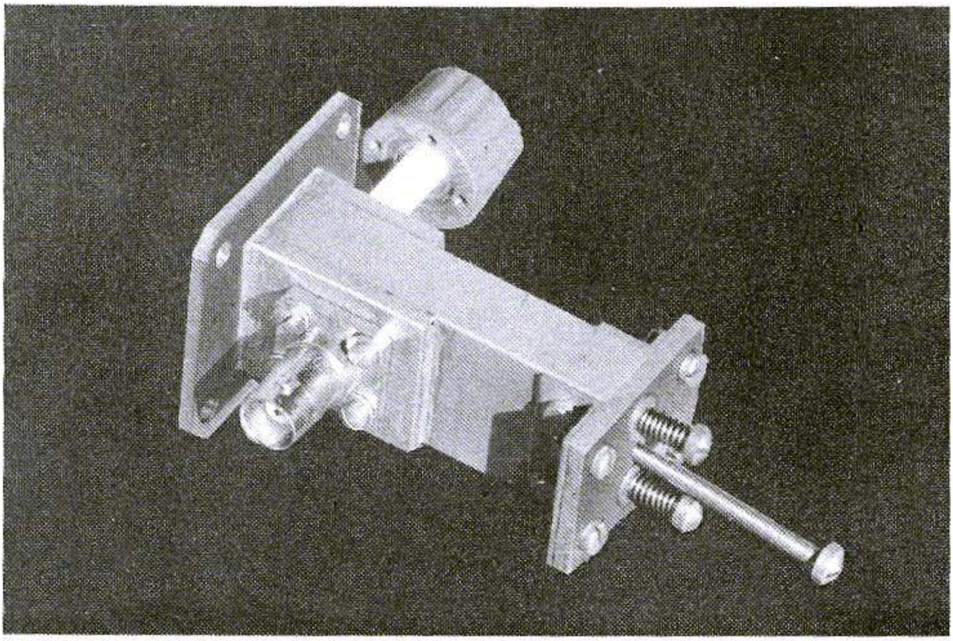


Fig. 1: Gunn-oscillator using a BNC-connector for mounting and feeding the Gunn-element

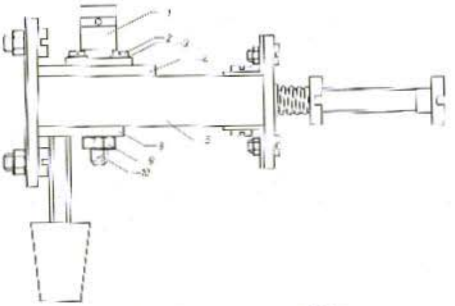


Fig. 2: The complete Gunn-oscillator described by the author

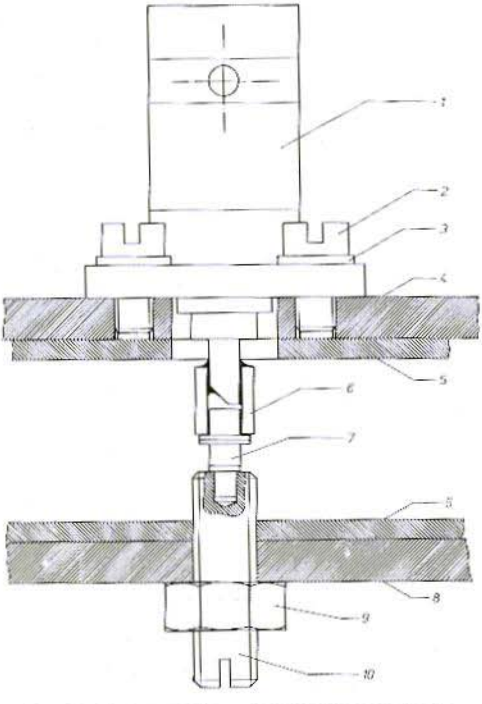


Fig. 3: Cross-section showing the new type of diode mount

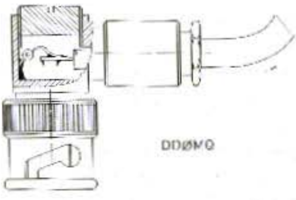


Fig. 4: The Gunn-oscillator is by-passed to prevent parasitic oscillation using a capacitor in the BNC-connector.

COMPONENTS (Figures 2 and 3)

(1)	50 Ω BNC-flange connector type UG-290 A/U
(2)	Cylinder-headed screw, brass, M 2.5 x 6 mm
(3)	Washer M 2.5; outer diameter 6.0mm; 0.5 mm thick
(4)	Brass plate 4 mm thick; same width as waveguide; length as required by the construction
(5)	Waveguide R 100 (WG-16)
(6)	Brass tube, outer diameter 3.0 mm; inner diameter 1.7 mm; Length appr. 5 mm. Available at model shops
(7)	Gunn element, e.g. type DGB 6844 A (15 mW), available from the Publishers
(8)	Brass plate, 4 mm thick, dimensions according to construction
(9)	Hextagonal nut M 4 (brass)
(10)	Grub screw with slot for screwdriver, and cutting edge M 4 x 10 mm

BY-PASSING THE GUNN OSCILLATOR

All Gunn-oscillators must be by-passed for frequencies lower than the operating frequency in order to avoid parasitic oscillation. This is made at the DC-voltage line. Values of 10 and 100 nF are usually used. The author found that a value of 3.3 nF was sufficient. This low capacitance value ensures that the higher modulation frequencies are not limited.

Since there are no possibilities for mounting this capacitor within the described oscillator, it was mounted in a right-angle BNC-connector, as shown in **Figure 4**. This means that the by-pass capacitor is very close to the Gunn-element, and that the interconnection to the modulator and power supply can be made in a coaxial manner.

A System for Reception and Display of METEOSAT Images

Part 8: The Control Module for the CRT

by R. Tellert, DC 3 NT

Part 7 of this article described the electromechanical FAX-machine, which is now to be followed by Part 8 that is to describe the electronic circuitry for the CRT. PC-board DC 3 NT 009 is also to be described in this description, and represents the last board of the system. This module generates the control signals for the CRT and for the film transport motor of the camera.

A few notes are to be brought to refresh your memory: The image is made in real time on the screen of a medium-sized TV-tube at a maximum of four lines per second. This unit is constructed so that the picture tube faces upwards, and is accommodated in a large, wooden case, which includes the EHT-power supply, as well as the output amplifiers for the X, Y, and Z-signals. The camera is mounted at the correct distance above the picture tube using a light-proof adapter (wooden case). Any camera can be used from a instant polaroid camera, up to a high-quality large plane film camera. If a series of images is to be taken automatically,one will require a motorized camera. Of course, it is also possible to build your own camera, as was done by the author. The elctronic circuitry, anyway, already provides circuits for controlling the film transport motor, as well as for determining the end of the film, and for selecting a predetermined number of images.

8. PC-BOARD DC 3 NT 009

This module is accommodated on the system board DC 3 NT 012 and is driven by the various previously published modules. The following signals are generated in the module:

- A sawtooth voltage for the X-deflection of the electronic beam
- A sawtooth voltage for the Y-deflection of the electronic beam
- A brightness signal for the beam with blanking during the fly-back of the beam, as well as blanking for the unwanted channel in the case of TIROS/NOAA transmissions
- The drive signal for controlling the relay of the film transport motor.

8.1. Design Considerations

The deflection voltages for the picture tube should exhibit the same amplitude for all possible image speeds (see Part 4, Table 1), so that the dimensions of the image are equal. Furthermore, the X-deflection voltage (line) should be able to quickly follow the wow-and-flutter of the tape recorder in the playback mode.

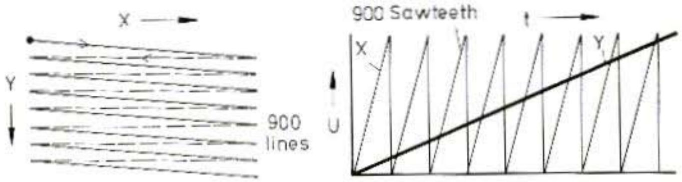


Fig. 67: Formation of the image and sawtooth voltages for deflection

Figure 67 shows how an image is built up schematically. It is assumed that an image comprises 900 lines. This means 900 sawtooth peaks are provided in the X-direction, and one sawtooth in Y-direction. These two different sawtooth voltages are generated from the so-called frame pulses supplied by module DC 3 NT 008, (Part 4 of this series of articles), and this is the main task of module DC 3 NT 009.

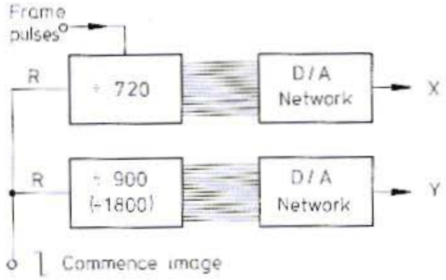


Fig. 68: Digital generation of the deflection voltages from the frame pulses

The speed switching is already contained in the frame pulses, which means that 720 pulses appear per line for each speed. In order to obtain the sawtooth voltage for the X-deflection, it is necessary to divide the frame pulses in some manner by 720, and by ÷ 720 x 900 in the case of the Y-deflection (with 900 lines per image).

Since the wow-and-flutter of the tape are corrected already in the frame pulses, the X and Y-sawtooth voltages can be generated in the circuit given in **Figure 68**.

This represents a clear digital concept and it will fulfill, theoretically, all demands. The weak point in realizing this in practice is in the digital-analog converters. Even when using expensive 10 Bit-D/A-converters, the Bit-jumps are not always identical. This leads to lines being generated in the image: Dark lines where the beam makes too large a jump, and bright lines where the beam is deflected less than required. One must assume that a bit corresponds approximately to an image point; with half a bit error of the D/A-converter, the exposure time for this image point would be 50% more – or less – and this difference will

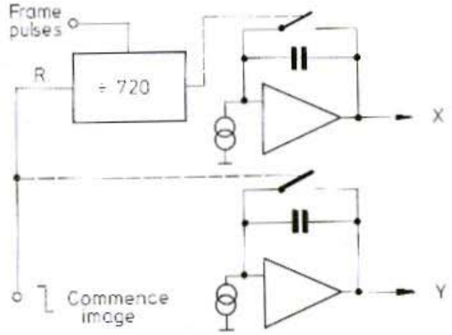


Fig. 69: The X and Y-voltages can also be generated using integrators

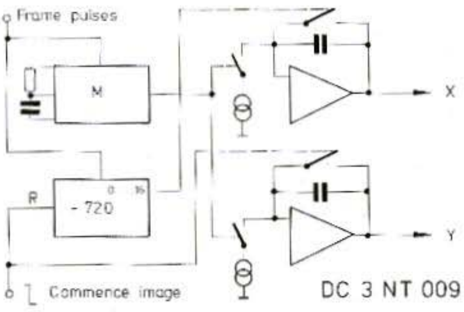


Fig. 70: The final combination of digital and integrator circuit

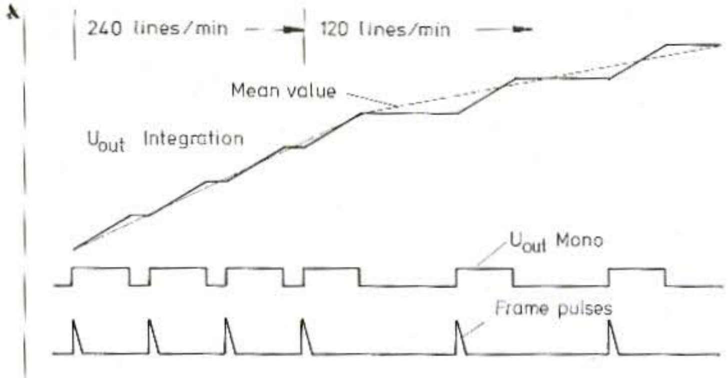


Fig. 71: Extract of a sawtooth voltage at two different speeds

be clearly visible, since the blackening of the film is the product of intensity and time.

The integrator principle shown in **Figure 69** avoids this disadvantage; its output voltage slope (≙ speed of the beam) is only dependent on the charging current and on the capacitance of the integrating capacitor. One demand is still not solved when using this system, and this is the demand of having the same image dimensions at all speeds, and the compensation of wow-and-flutter fluctuations when processing a tape-recorded signal.

A combination of the two methods is given in **Figure 70**. This satisfies all demands and is used in the described module. The operation is shown in **Figure 71**.

This Figure shows a small extract of the X or Y-sawtooth voltage, and for a speed of 240 lines per minute in the first half of the image, and 120 lines per minute in the second half. A monoflop is started with each frame pulse (the lowest line of the image); X or Y-voltages are only integrated during the delay of the monoflop. Each frame pulse therefore increases the X-output voltage by 1/720, or the Y-output voltage by 1/720 x number of lines. In the case of slower speeds than 240 lines per min., it is only the pauses between the frame pulses that are made longer.

8.2. Circuit Details

A counter type 4040 (I 1 in **Fig.72**) counts the frame pulses and resets the X-integrator I 8a (1/4 LM 324) after receiving 720 pulses. This is maintained until the counter state is 15, which serves as the fly-back for the beam. The beam remains black during this period.

This reset function is made by flipflop I 2a; it is reset at a counter state of 000, and at 016. This measure also ensures that a shutter is not required in the camera, since when no image is being written, counter I 1 and thus also flipflop I 2a are in a continuous reset position, and the picture tube will be dark. Information as to whether an image is to be recorded or not, is stored in flipflop I 5a. This IC possesses a start input, and four stop-inputs (I 4b) of equal priority.

Negative logic is used here, which means that the quiescent state of the inputs is $+U_B$; they are activated at 0 V (ground).

Flipflop I 5a controls the following 5 functions:

Reset of I 1 and I 2a
Reset of Y-integrators
LED »Mon« (image recording active)
Film transport after recording
Disable of manual film transport during image

Five stop-conditions exist for the flipflop I 5a:

Switch-on reset
External stop (connector strip, pin 11)
Film transport running
Film end-flipflop (F.E.) set
Y-integrator has reached end of image.

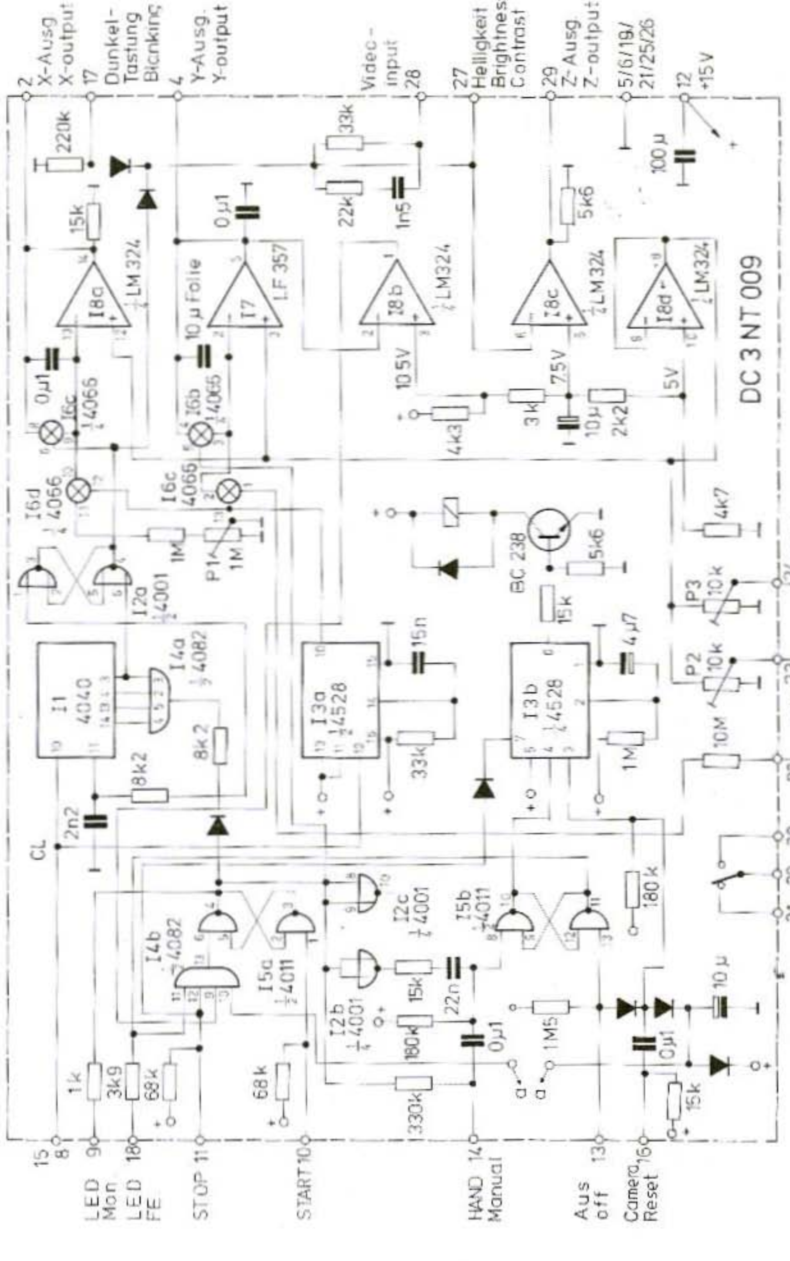


Fig. 72: The complete circuit diagram of module DC 3 NT 009

The control of the film transport motor also belongs to the logic part of module DC3NT 009. An operating voltage of 7 V was generated for driving the motor of a 35 mm camera. The motor also operates a contact, which will close when the film has been transported to the value of one image.

Furthermore, a pushbutton contact is required on the front panel of the unit that also transports the film by one image for each depression. This is required to bring the start of the film to the correct position after inserting a new film.

But, how can one determine the end of the film ? Of course, it is known that the film is fixed at the end of the roll. A monoflop and flip-flop are set in order to carry out film transport. The film transport motor is started with the aid of the monoflop I 3b. If the film can be transported, the previously mentioned contact on the camera will reset both the monoflop and the flipflop (I 5b). If, on the other hand, the film has ended, no pulse will come from the contact, and the motor will run as a short-circuit. This condition is limited in time due to the delay of the monoflop I 3b. After the delay, the motor will be switched off, however, the flipflop »Film End« will remain set. This ensures that no further exposure can be made due to a forced stop via I 4b. The film end flipflop can be reset using switch »Film End Off« via pin 13 of the connector strip.

The monoflop I 3b must, of course, run somewhat longer than the film transport time. The time delay of the monoflop can be generously dimensioned, since it only runs over its full period in the case of the last picture.

By the way, the whole of the described camera control is made in negative logic, since all input signals are made with the aid of switches or pushbuttons that make contact to ground.

Three different voltages are required in the analog portion of the circuit that are obtained using a voltage divider from the only operating voltage available of 15 V, (4k3/3k3/2k2/4k7). This results in:

+ 10.55 V for the image-end comparator (I 8b)

+ 7.1 V as operating point of the video signal amplifier I 8c

+ 5 V for the two integrators (I 7 for Y and I 8a for X).

The output voltage is equal to the input voltage (+ 5 V) in the reset states of the integrators. It will increase to + 10 V at the end of the slope. This end of the slope is determined by the charge current, which can be set for the X-deflection using trimmer potentiometer P 1. In the case of the Y-deflection, the end of the slope can be set using P 2 for an index of cooperation of 288, and with P 3 at 576.

The constant-current sources associated to each integrator are only resistors in our case; the current is constant because the voltage drop across them is constant. The non-inverted inputs of the integrators have a reference potential of + 5 V, as long as they are not saturated.

The Y-integrator (»Vertical«) must be designed for a relatively long integration time of approximately 200 to 400 seconds. In order to ensure that no expensive and large plastic foil capacitors of more than 10 µF must be used, a very low charge current was selected. This is the reason for the use of an operational amplifier with field-effect input. The type LF 357 used is a new development; for those readers having a 8007 available, this can also be used. All other operational amplifiers were combined using a previously used LM 324.

The video signal is amplified in I 8c. The positive or negative video signal is fed from pin 28 via a resistor and a RC-link to a summing point. The brightness potentiometer is also connected here via a 100 kΩ resistor on the system board.

The contrast control is connected between the summing point and output pin 29; this control determines the gain of I 8c. It is limited externally using a 15 kΩ resistor, which should be taken into consideration during the wiring, since the integrated circuit could become defective if a setting of zero contrast were selected.

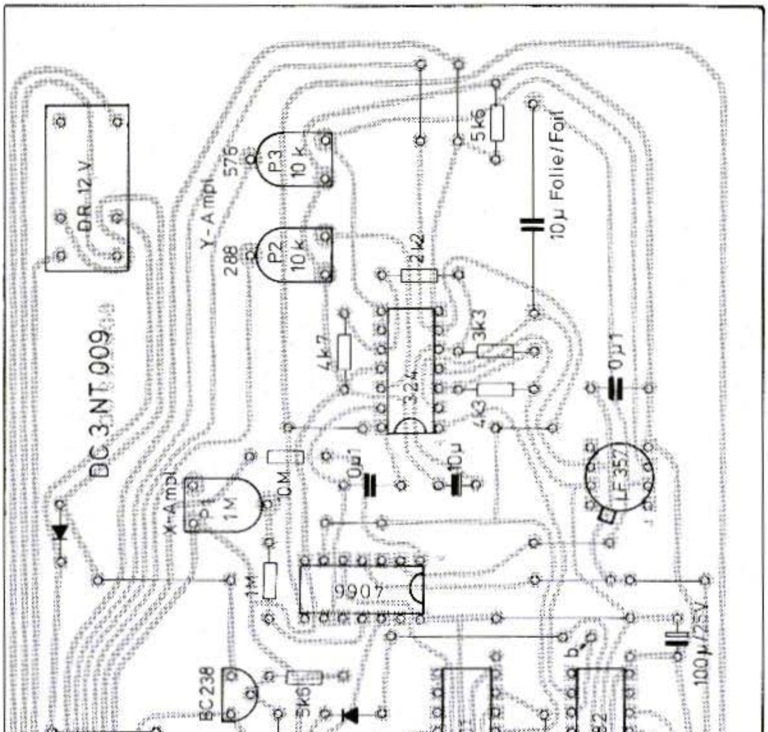


Fig. 73: PC-board DC 3 NT 009 is only single-coated – However 17 wire bridges will be required

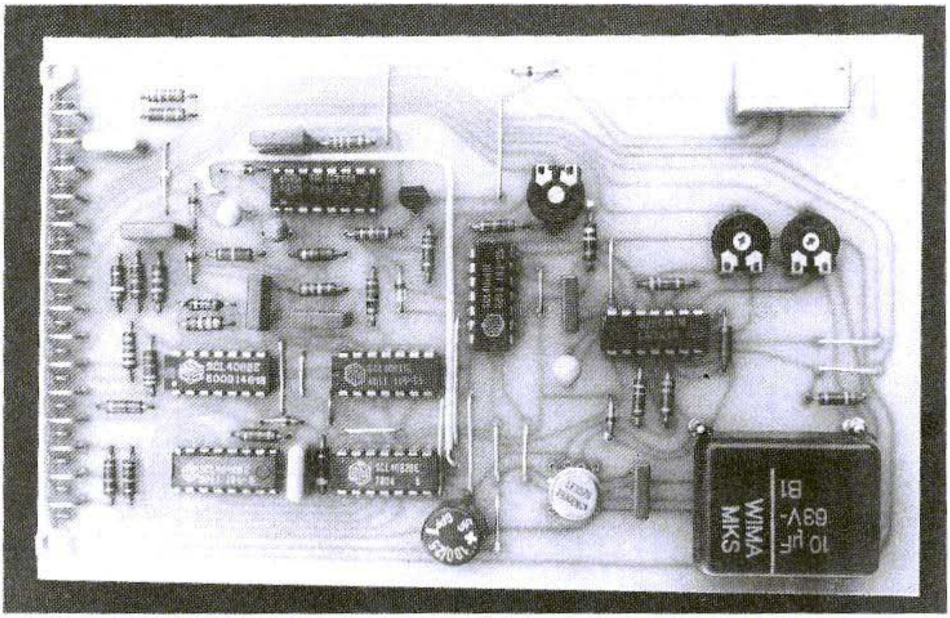


Fig. 74: **The photograph of the author's prototype shows the wire bridges, and the 10 µF integrating capacitor**

8.3. Components

I 1: 4040
I 2: 4001
I 3: 4528
I 4: 4082
I 5: 4011
I 6: 4066
I 7: LF 357 H (Siemens)
I 8: LM 324

1 NPN-AF transistor BC 413, BC 238 or similar

8 silicon diodes 1 N 4151, 1 N 4148 or similar

1 relay SDS – type DR 12 V

1 connector strip, 31-pole, (DIN 41617/Siemens)

Trimmer potentiometer with a spacing of 10/5 mm: 2 x 10 kΩ, 1 x 1 MΩ

Plastic foil capacitors with a spacing of 7.5 mm: 1 x 1n5, 1 x 2n2, 1 x 15nF, 1 x 22nF, 4 x 0µ1

1 plastic foil capacitor 10 µF/63 V, for a spacing of 27.5 mm

Tantalum electrolytics, drop type: 1 x 4µ7/25 V, 2 x 10 µF/25 V

1 alu-electrolytic, round, spacing 5 mm: 100 µF/ 25 V

All resistors: carbon type, for 10 mm spacing

Construction Details

Module DC3NT 009 is built up on a Europa-size board as the other plug-in modules. **Fig. 73** shows the component locations on this 160 mm x 100 mm PC-board. It is only single-coated to keep the costs as low as possible; however, this means that several wire bridges must be made. A total of 17 pieces are required, and these can be seen in the component plan, and also in the photograph of the prototype given in **Figure 74**. The only bridge that is longer, and which must be insulated, is the interconnection between points a and b.

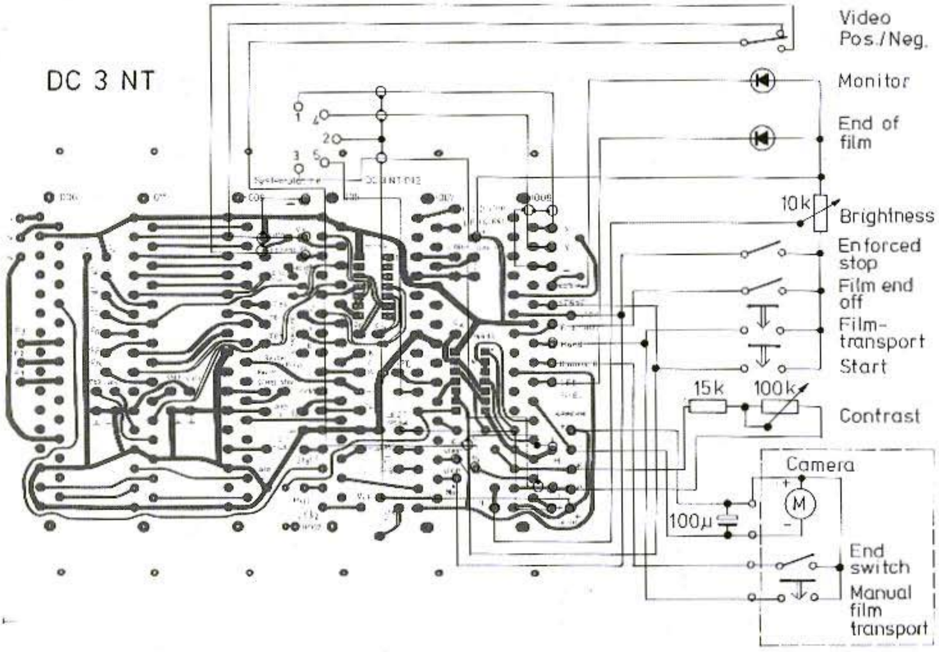


Fig. 75: This diagram shows the necessary interconnections between the system board and the control elements required due to the addition of DC 3 NT 009

The 10 µF plastic foil capacitor cannot be mounted perpendicular to the board, but must be placed horizontally on the board using double-adhesive tape, and connected using solder pins to the conductor lanes.

8.5. Connection and Alignment

PC-board DC3NT009 is plugged into the required position on the system board, which makes most of the interconnections to the other modules. The additional wire connections that must be made, are given in **Fig. 75**. These connections are mainly to the controls.

The only alignments that must be made, are the maximum amplitudes of the sawtooth voltage (end of slope). The start of the slope need not be aligned.

The final amplitude of the X-sawtooth voltage can be adjusted with the aid of an oscilloscope to +10 V; trimmer potentiometer P 1 is provided for this purpose, and a speed of 240 lines per minute should be selected.

The Y-integrator is somewhat more difficult to align: A digital voltmeter is connected to the Y-output and the time is then stopped in which the sawtooth voltage increases by 1 V. With an index of cooperation of 288, this should correspond to 45 seconds, and 90 seconds in the case of 576. At an index of cooperation of 288, P 2 should be adjusted, and P 3 in the case of 576.

This completes the description of this module, and the only part that must still be described are the picture tube with its output amplifiers, and EHT voltage generator.

A Simple Method of Switching the Direction of Circular-Polarized Antennas

by T. Bittan, DJ 0 BQ / G 3 JVQ

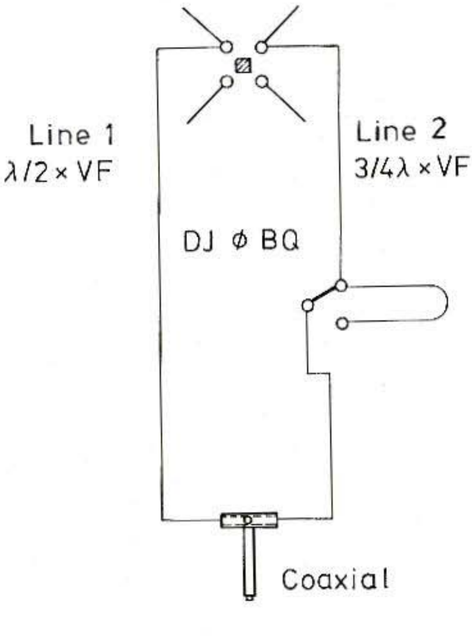
Several methods have been described for switching and selecting the required polarisation in conjunction with crossed Yagi antennas. These have been somewhat complicated and therefore somewhat difficult to construct. Also they were only described for use with 2 m antennas due to the problem of velocity-factor fluctuations along the two separate feeders that were required.

Since many operators of crossed Yagi antennas are mainly operating via satellites, they often only need to switch between clockwise and anticlockwise circular polarisation. For this reason, the author has designed a simple switching method that can be remote controlled from the station.

Due to the fluctuations of the velocity factor, it is important that the feeder lengths between matching transformer and antenna are as short as possible. The author recommends an electrical length of λ/2 for line 1, and 3/4 λ for line two. A λ/2 delay line is to be found in line 2 which shifts the delay in this line from λ/4 to λ3/4, thus switching the direction of polarisation from clockwise (direct) to anticlockwise (via delay line).

The only components that are required in addition to the coaxial cable is a relay with short contacts, and a matching transformer as offered by UKW-TECHNIK. The connection details are especially for the popular JAYBEAM range of crossed Yagi antennas, but can be modified for other similar antennas after taking the spacing between dipoles, and the phasing of the actual dipoles themselves into consideration.

In the case of crossed Yagi antennas with a λ/4 spacing between dipoles such as the 8 XY / 70 cm and 12 XY / 70 cm, the length of line 1 and 2 should be both λ/2 and not possess a phase difference of λ/4.



A Microcomputer for Amateur Radio Applications

Part 6: Power Supply and Rotator Interface

by W. Kurz, DK 2 RY

This article is to describe the power supply for the microcomputer, and an interface for driving a rotator. The latter has the task of feeding the calculated data via a port to the digital rotator control system DK1OF 038-041.

Before commencing the description, a short note regarding the previously described boards: In the case of board DK2RY 004, and DK2RY 005, a bidirectional bus driver was used (SN74 LS245). This driver was provided to ensure that a breakdown of the data could not occur. Subsequently, it was found that this measure was not necessary, since the IC only required a few µA in its non-active state. This means that a bridge can be made within the connection pins of the SN 74 LS 245, and this IC can be deleted.

6.1. The Power Supply

The power supply provides the following voltages: + 5 V / 5 A, - 5 V / 0.5 A, + 12 V / 0.5 A, and − 12 V / 0.5 A. Two C-core transformers with center-tap are used. Due to their large volume and weight, these are not accommodated on the PC-board, but are mounted separately in the case.

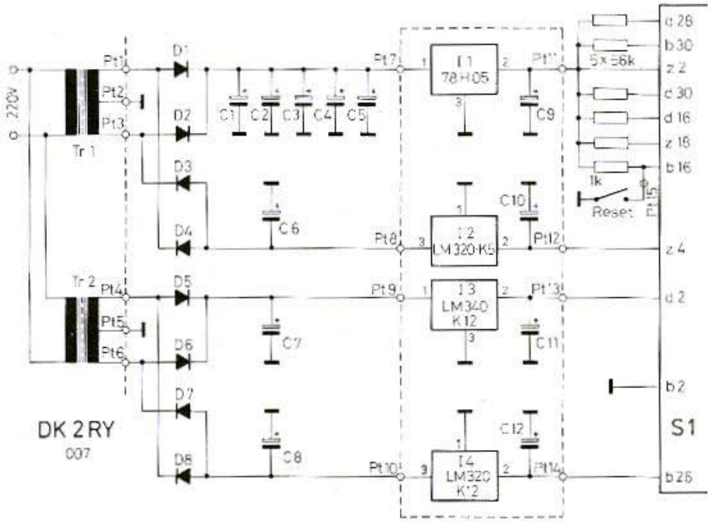


**Fig. 41:
The power supply of the microcomputer provides four different voltages;
the components shown within the dashed lines are not mounted on the PC-board**

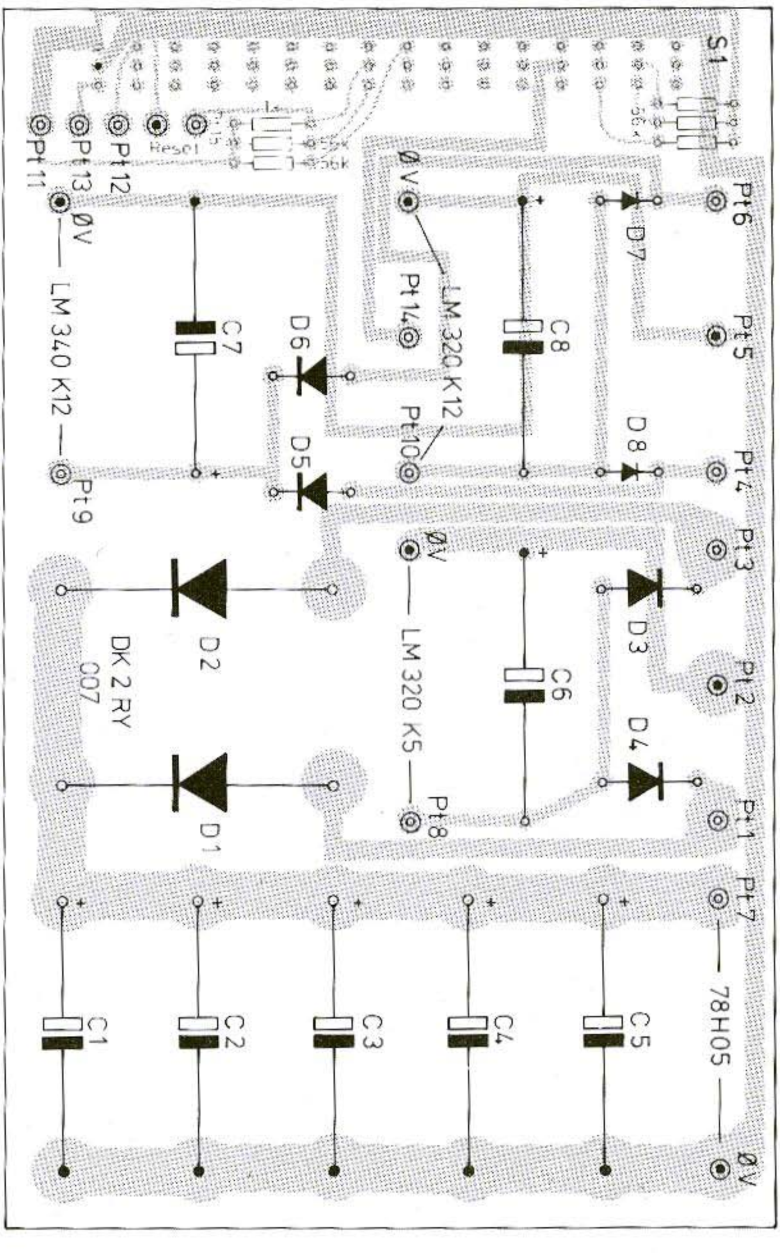


Fig. 42: PC-board DK 2 RY 007 for the power supply can also be connected to the bus

As can be seen **in Figure 41**, the AC-voltages are rectified using two rectifiers, and are then filtered. The resulting DC-voltages are stabilized in the integrated voltage stabilizers I 1 to I 4 and are fed to the bus. Bypass capacitors are soldered into place directly at the connection points of the voltage stabilizers to suppress any tendency to oscillation.

The 5 A fixed-voltage stabilizer type 78 H 05 manufactured by Fairchild is used for generating the stabilized operating voltage of +5V; all other voltage stabilizers are 1 A-types. These fixed-voltage stabilizers are mounted on a heat-sink on the outside of the case.

6.2. Construction of the Power Supply

The power supply (DK2RY 007) is built up on a 101.6mmx160mm single-coated PC-board as shown in **Figure 42**. The fixed-voltage stabilizers are screwed into place on a heat-sink and connected to the power supply board. It is important that the negative voltage stabilizers (LM 320-5K, and LM 320-12K) must be mounted in an insulated manner, whereas the positive stabilizers (78 H 05, LM 309K) are not insulated on the heat-sink.

A single-pole pushbutton switch is connected to the »reset« connections. This allows the whole computer system to be reset to zero. After placing all components into position and connecting all stabilizers, it should be checked to see whether the correct voltages are available at the correct positions (see **Table 1**). If this is the case, it is possible for the power-supply board tobeplaced into one of the strip-connectors on the bus-board (DK2RY 002).

Connection strip	Voltage
d 2	+ 12 V
b 2	Ground
z 2	+ 5 V
z 4	− 5 V
b 26	− 12 V

Table 1:
Operating voltages on the connector strip

6.2.1. Components

C 1 - C 6:	Electrolytic 2200 μF/16 V
C 7, C 8:	Electrolytic 1000 μF/40 V
C 9 - C 12:	Tantalum electrolytic 47 μF/25 V
I 1:	78 H 05 (Fairchild)
I 2:	LM 320-K 5 (Fairchild)
I 3:	LM 340-K 12 (Fairchild)
I 4:	LM 320-K 12 (Fairchild)

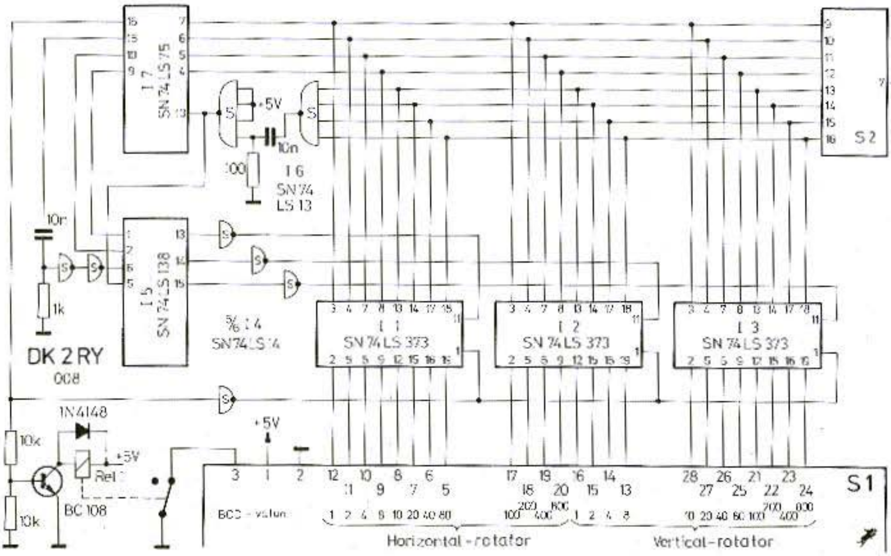


Fig. 43: This circuit represents the interconnection between the microcomputer and the digital rotator control described by DK 1 OF

D 1, D 2:	SSI C 1220 (Siemens) or similar
D 3 - D 8:	1 N 4001 or similar 1 A-rectifier
S 1:	48-pin connector strip C 74334-A80-A60
Tr 1:	Transformer 2 x 7.5 V/3.5 A type TR 65-75
Tr 2:	Transformer 2 x 15 V/0.6 A type TR 55-15

6.3. The Rotator Interface

As was previously mentioned, the rotator interface passes the calculated data to the digital rotator control. In principle, it would be possible for the digital rotator control to be directly connected to the three ports of the 8255 on board DK2RY 005. The author has, however, not done this in order to allow the interface to be used in conjunction with other microcomputers such as the PET 2001. Since these computers often only have one addressable port, the interface was designed so that it can be driven from one single port.

As is known, the angular values will have a word width of more than 8 Bit since they are required in BCD-code. For this reason, three latches type SN 74 LS 373 are provided in the rotator interface with which the calculated angles are stored **(Figure 43)**. Since the data is multiplexed, a further memory will be required into which the address of each latch is given into which it is to be written. A 4 Bit D-flipflop, type SN 74 LS 75 (I 7) is used as memory. It is only possible to write into this flipflop when the four highest-valency bits of the data word are at H-level. For this reason, they are interconnected via the Nand-gate of I 2. Circuit I 2 possesses two Nand-Schmitt triggers with four ports, each. The first is used as a normal Nand-gate. A RC-link differentiates the output signal, and passes it to the second Nand-Schmitt trigger. This generates a square-wave pulse with a duration of approximately 1 µs. During this period, it is possible to write into the D-flipflop.

The output signal 0 2 (WRITE STROBE) of the D-flipflop is also differentiated and passed to a Schmitt trigger. This forms a pulse of approximately 30 µs duration which is then fed to E 2 and E 1 of the SN 74 LS 138 (I 5). Circuit I 5 is therefore only active during this period, and it is only possible during this period to write into one of the three latches (I 1 to I 3). The address of the individual latch to be used is contained in the two lower-valency bits of I 7. Bit 3 of the I 7 provides the information whether the rotator interface is to be driven from the computer, or from the coding switches.

Output 0 3 of I 7 drives transistor T 1. If this output is at L-level, this will mean that the transistor is blocked, and that Reed-relay Rel1 will be in its rest position. It is now possible for the antenna direction to be selected using the coding switches. If, on the other hand, output 0 3 is at H-level, T 1 will conduct and energize Rel1. In this case, the computer will determine the antenna direction.

The output signals of I 3 are inverted and fed to the Strobe-input of the three latches, whereas output 0 3 of the SN 74 LS 75 activates the output amplifier of the latches via an inverter, or places them in a high-impedance state (tristate).

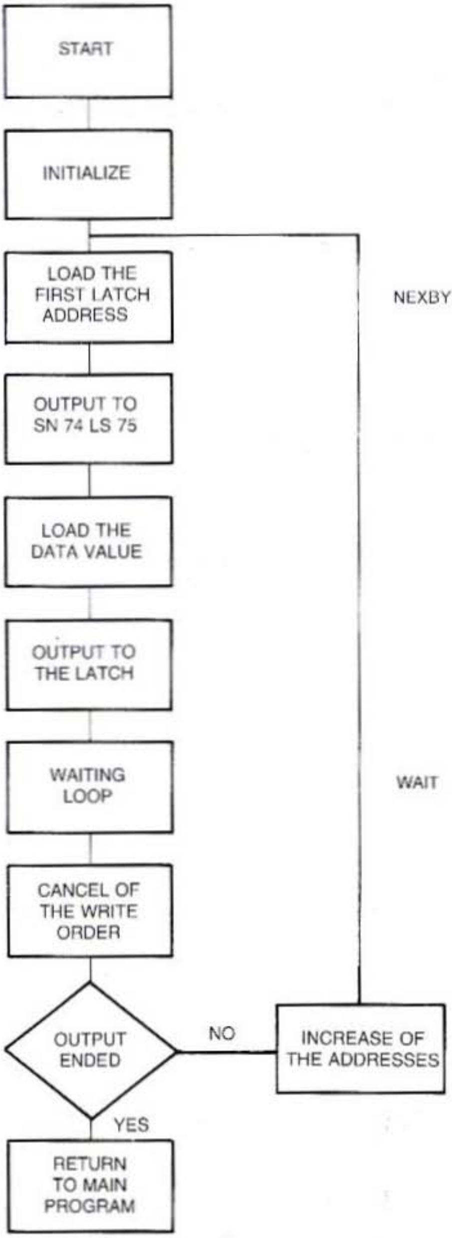
The states are summarized in **Table 2**:

Hexadecimal value at D 0 - D 7 of the 8255	Effect
E F H - 0 0 H	Data values for SN 74 LS 373
F 4 H	Write into I 1 Outputs active
F 5 H	Write into I 2 Outputs active
F 6 H	Write into I 3 Outputs active
F 7 H	Not used
F 0 H - F 3 H	Ignore write-order
F C H	Write into I 1 Outputs high-impedance
F D H	Write into I 2 Outputs high-impedance
F E H	Write into I 3 Outputs high-impedance
F F H	Not used Outputs high-impedance
F 8 H – F B H	Ignore write-order Outputs high-impedance

Table 2: State of the conditional bits and the resulting effects

For those readers using other microcomputer systems, it should be noted that the drive of the rotator interface is made in a 2-Digit BCD-code. This means that 2 BCD-digits are provided in an 8-Bit wide data word.

The following, simplified diagram together with program can be used as a base of a program for driving the rotator interface with a different computer than described here.



```
        PUSH HL
        PUSH BC

        LD HL, 2130
        LD BC, 03 F 4
        LDA, 00
        OUT E 8

NEXBYTE LDA, C

        OUT E 8

        LDA (HL)

        OUT E 8

        PUSH BC
        LDC, OF
WAIT    DCR C
        JNZ WAIT
        POP BC

        LDA, C
        AND F 3
        OUT E 8

        INC HL
        INC C
        DCR B
        JNZ NEXBYTE

        POP BC
        POP HL
        RTN
```

Program diagram for the drive of the rotator interface

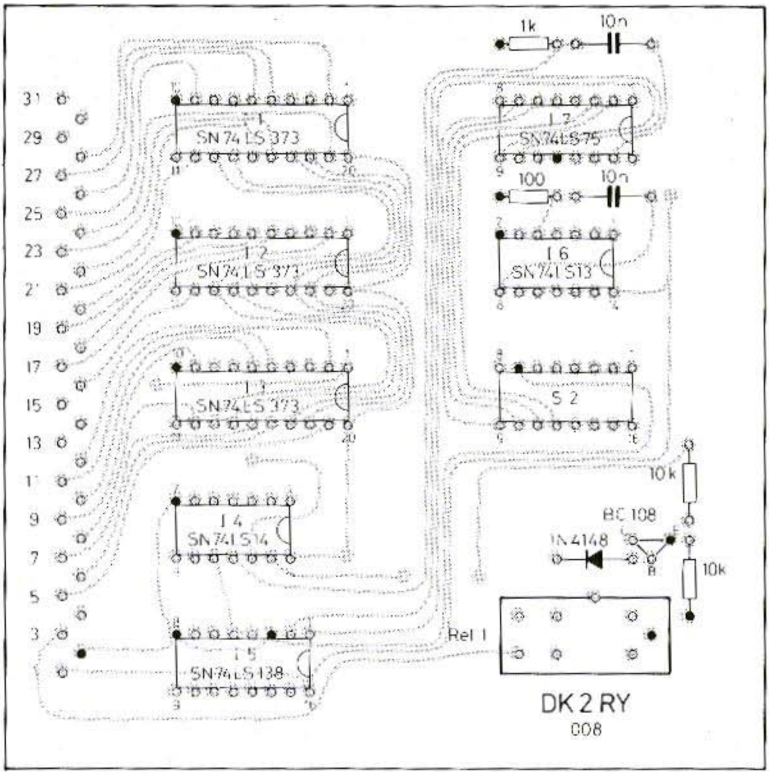


Fig. 44: PC-board DK 2 RY 008 for the rotator interface

6.4. Construction of the Rotator Interface

The rotator interface DK2RY 008 is accommodated on a 100mmx100mm large, double-coated PC-board with through-contacts **(Fig. 44)**. The completed board **(Figure 45)** is plugged into the digital rotator control using a 31-pin connector strip. The interconnection to the computer is made with the aid of a 16-pin DIL-connector and a flat-cable. The other end is also provided with a DIL-plug and connected to P 3 of the input-output unit DK2RY 005 (see **Figure 46**). The data connections on the connector strip are connected to the corresponding connections of the rotator control via cables **(Table 3)**.

6.5. Components for the Rotator Interface

I 1 - I 3: SN 74 LS 373 (TI)
I 4: SN 74 LS 14 (TI)
I 5: SN 74 LS 138 (TI)
I 6: SN 74 LS 13 (TI)
I 7: SN 74 LS 75 (TI)

S 1: 31-pin connector strip
C 42334-A55-A408 (Siemens)

Rel 1: Reed-relay RSD 5 (National)

DIL-connector 16-pin,
C 42334-A380-A16 (Siemens)

6.6. Connection of an Alpha-Numerical Keyboard

An alpha-numerical keyboard is not to be described here, since these are available inexpensively on the market. For this reason, the author is only to describe the connection of such a keyboard.

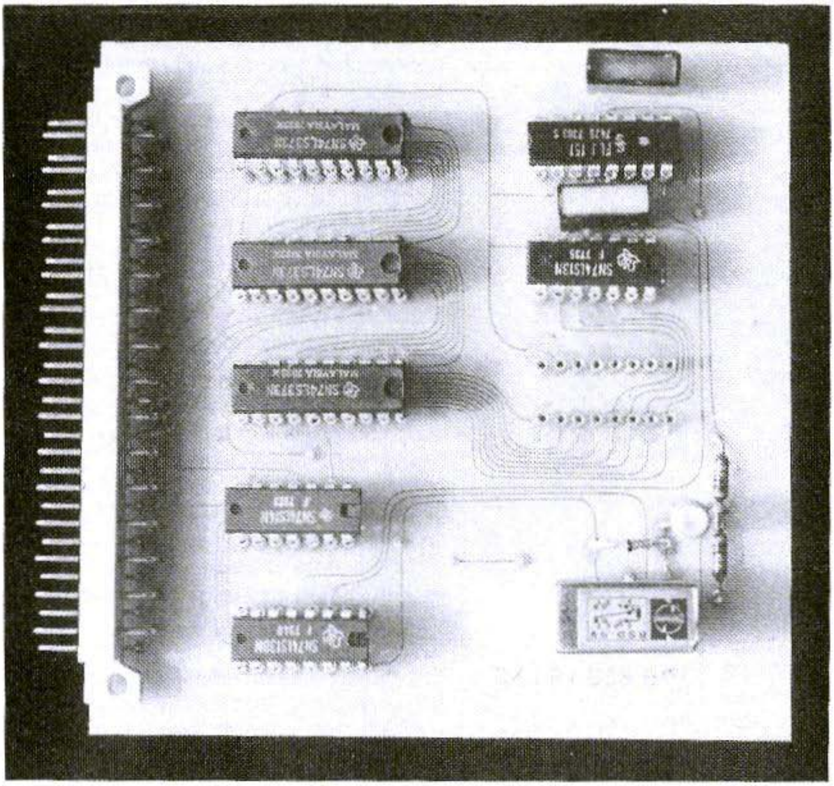


Fig. 45: The rotator interface is plugged into the rotator control as described by DK 1 OF

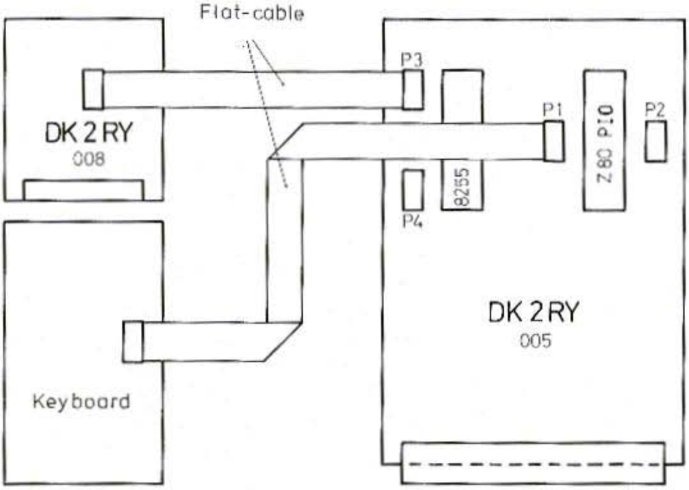


Fig. 46:
Two flat-cables are provided in addition to the bus

Connection Strip	Description		Connected to DK1OF038 pin
1	+ 5 V input		14
2	Ground		29
3	Output relay		Instead of S 1
4	-		-
5	BCD 80	Hor.	10
6	BCD 40	Hor.	11
7	BCD 20	Hor.	19
8	BCD 10	Hor.	20
9	BCD 8	Hor.	23
10	BCD 4	Hor.	24
11	BCD 2	Hor.	25
12	BCD 1	Hor.	26
17	BCD 100	Hor.	7
18	BCD 200	Hor.	6
19	BCD 400	Hor.	5
20	BCD 800	Hor.	4
16	BCD 1	Vert.	26
15	BCD 2	Vert.	25
14	BCD 4	Vert.	24
13	BCD 8	Vert.	23
21	BCD 100	Vert.	7
22	BCD 200	Vert.	6
23	BCD 400	Vert.	5
24	BCD 800	Vert.	4
25	BCD 80	Vert.	10
26	BCD 40	Vert.	11
27	BCD 20	Vert.	19
28	BCD 10	Vert.	20

Table 3:
Connections on the interface-board for digital rotator control.
(Vert. = Vertical rotator control;
Hor. = Horizontal rotator control)

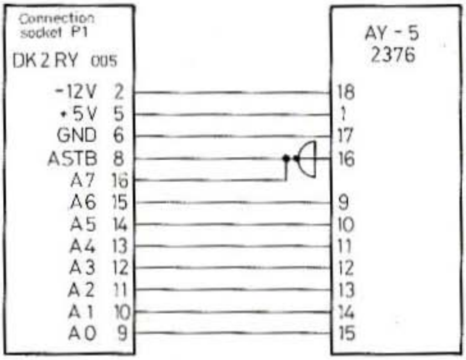


Fig. 47: Connection of a keyboard encoder

The operating voltages required for the operation of such a keyboard can be taken from connector P 1 on the input-output unit. The keyboard is connected using a 16-pin DIL-connector and flat-cable. It is important that the outputs of the keyboard coincide with those of the port, in other words, that the least significant bit is at A 0 of the port, the next at A 1, and so on to A 6.

Input A 7 of the port can be connected to a strobe, or grounded. An example is shown in **Figure 47**, which shows the connection of a keyboard-encoder type AY 5-2376.

It is also important that the strobe output of the keyboard goes from H to L when a key is suppressed; (it may be necessary to invert the strobe). Since the inputting of data and orders is made with the aid of an interrupt routine, and the interrupt is requested using the positive slope of the strobe-signal, the indication of the entered value will appear after releasing the key, and not on depressing it as is usually the case.

The author recommends that the required DIL-connectors used for the interconnection with flat-cables are ordered from Siemens. The following table gives a list of the order numbers:

DIL-connector, 16-pin	C 42334-A390-A16
Locking spring	C 42334-A390-C116
Flat-cable connector	C 42334-A368-A16
Flat-cable	V 45587-A161-A10
Coding bolt	C42334-A390-C2 (Packg. units: 50 pcs.)
Cable bracket	C 42334-A368-C5

These plugs and sockets can be coded and are therefore non-exchangeable.

FURTHER PUBLICATIONS

The next part of this article is to describe the TV-interface and represents the last article of this series. The task of the TV-interface is to display alpha-numerical signs (questions from the computer to the user, or the inputted values, data, and orders) on a conventional TV-receiver.

MATERIAL PRICE LIST OF EQUIPMENT
described in Edition 2/1981 of VHF COMMUNICATIONS

DJ 7 VY 004	**LOW-NOISE VHF OSCILLATOR WITH DIODE TUNING, DIGITAL LOCKING AND READOUT**		**Ed.2/1981**
PC-board	**DJ 7 VY 004**	**double-coated with thru-contacts**	DM 35.—
Semiconductors	DJ 7 VY 004	5 FETs, 2 DG-MOSFETs, 6 UHF and 2 AF transistors, 3 varactor, 2 Schottky, 3 switching diodes, 2 Schottky TTL-ICs, 3 CMOS ICs, 1 timer IC, 4 stabilizers	DM 169.—
Minikit	DJ 7 VY 004	1 ceramic inductance, 3 sp. coilsets, 1 two-hole core, 1 potted core set, 7 miniature ferrite chokes, 2 six-hole core chokes, 1 tubular cap. 18 pF NPO, 1 cap. 1 pF P 100, 2 styroflex cap. 100 pF, 1 metal case type A 105, 1 m PTFE 1 mm ∅ coaxial cable	DM 147.—
Kit	**DJ 7 VY 004**	**complete with above parts**	**DM 345.—**

DK 1 OF 044/045	**SETTABLE UP/DOWN FREQUENCY COUNTER**		**Ed.2/1981**
PC-board	DK 1 OF 044	double-coated, thru contacts	DM 26.—
PC-board	DK 1 OF 045	double-coated, thru contacts	DM 19.—
Semiconductors	DK 1 OF 044/45	1 ICM 7217, 1 ICM 7207, 5 low-power Schottky TTLs, 1 CMOS-IC, 5 UHF-transistors, 1 DG-MOSFET, 10 switching diodes, 6 digital readouts	DM 155.—
Minikit	DK 1 OF 044/45	1 miniature ferrite choke, 1 plastic foil trimmer, 16 cer.caps., 1 pl.cap., 2 tantalum electrolytics, 2 alu.electrolytics, 24 cer.feedthrough caps., 38 carbon resistors, 1 metal case	DM 49.—
Crystal	5.24288 MHz	HC-18/U	DM 16.—
Kit	**DK 1 OF 044/45**	**complete with above parts**	**DM 260.—**

DJ 4 LB 008	**LINEAR AMPLIFIER FOR 1250 and 1296 MHz**		**Ed.2/1981**
PC-board	DJ 4 LB 008	double-coated, etched one side, undrilled, without plan	DM 11.—
Semiconductors	DJ 4 LB 008	1 BFQ 68, 1 BD 437, 1 Z-diode, 5 diodes	DM 85.—
Minikit	DJ 4 LB 008	3 pl.trimmers, 3 feedthru caps., 1 tantalum and 1 alu.electrolytic, 3 ferrite beads, 1 trimmer pot., 4 resistors, 1 metal case, 2 BNC flange conn., 1 heatsink	DM 25.—
Kit	**DJ 4 LB 008**	**complete with above parts**	**DM 119.—**

DC 3 NT 009	**WEATHER SATELLITE SYSTEM / TV-MONITOR DRIVE**		**Ed.2/1981**
PC-board	DC 3 NT 009	single-coated, undrilled with plan	DM 20.—
Semiconductors	DC 3 NT 009	2 linear and 6 CMOS ICs, 1 transistor, 8 diodes	DM 35.—
Minikit	DC 3 NT 009	1 special relay, 1 conn. strip (31 pin), 3 trimmer pots., 27 carbon resistors, 9 pl.caps., 3 tantalum caps., 1 aluminium electrolytic	DM 47.50
Kit	**DC 3 NT 009**	**complete with above parts**	**DM 99.—**

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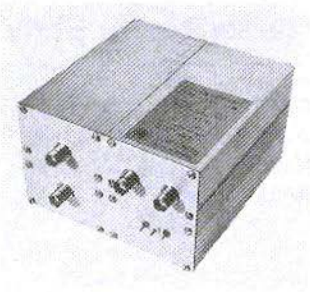

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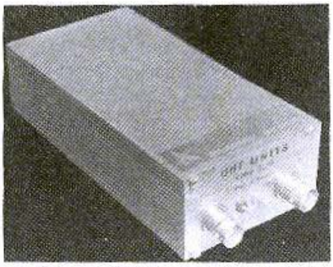

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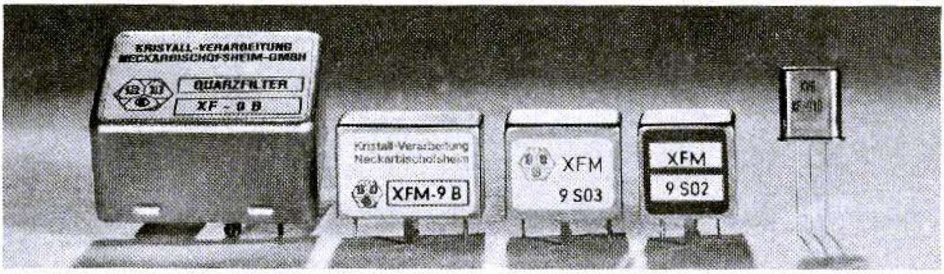

Case:	1	15	14	13	17

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		with impedance transformation			without impedance transformation		
		Type	Termination	Case	Type	Termination	Case
XF-9A	SSB	**XFM-9A**	500 Ω ‖ 30 pF	15	**XFM-9S02**	1.8 kΩ ‖ 3 pF	13
XF-9B	SSB	**XFM-9B**	500 Ω ‖ 30 pF	15	**XFM-9S03**	1.8 kΩ ‖ 3 pF	14
XF-9C	AM	**XFM-9C**	500 Ω ‖ 30 pF	15	**XFM-9S04**	2.7 kΩ ‖ 2 pF	14
XF-9D	AM	**XFM-9D**	500 Ω ‖ 30 pF	15	**XFM-9S01**	3.3 kΩ ‖ 2 pF	14
XF-9E	FM	**XFM-9E**	1.2 kΩ ‖ 30 pF	15	**XFM-9S05**	8.2 kΩ ‖ 0 pF	14
XF-9B01	LSB	**XFM-9B01**	500 Ω ‖ 30 pF	15	**XFM-9S06**	1.8 kΩ ‖ 3 pF	14
XF-9B02	USB	**XFM-9B02**	500 Ω ‖ 30 pF	15	**XFM-9S07**	1.8 kΩ ‖ 3 pF	14
XF-9B10*	SSB	—	—	–	**XFM-9S08**	1.8 kΩ ‖ 3 pF	15

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DISCRIMINATOR DUALS (see VHF COMMUNICATIONS 1/1979, page 45)

for NBFM	**XF-909**	Peak separation 28 kHz
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XF-9NB	500 Hz	8	60 dB : 6 dB 2.2	500 Ω ‖ 30 pF	1
XF-9P*	250 Hz	8	60 dB : 6 dB 2.2	500 Ω ‖ 30 pF	1

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