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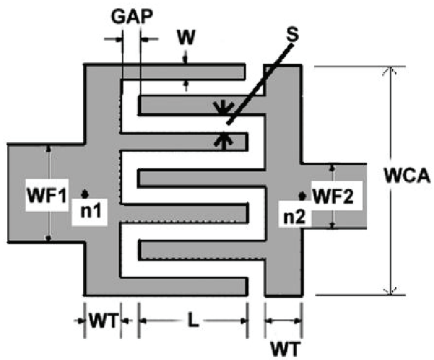


| Properties | Description | Units | Default | Range |
|---|---|---|---|---|
| N | Number of fingers | none | Required | ≥ 2 |
| W | Finger width | m | Required | > 0 |
| S | Finger spacing | m | Required | > 0 |
| L | Length of finger overlap | m | Required | > 0 |
| WT | Terminal strip width | m | Required | ≥ 0 |
| WF1 | Line width at port 1 | m | Required | > 0 |
| WF2 | Line width at port 2 | m | Required | > 0 |
| WCA | Capacitor width | m | N*W+(N-1)*S | ≥ N*W+(N-1)*S |
| GAP | Gap between end of finger and terminal strip | m | Required | > 0 |
| sub | Substrate name | none | Required | string |
| CoSimulator | Simulation engine | none | Circuit | Circuit, Planar EM |

## Ansoft Designer SV project: Using microstrip interdigital capacitors

*Gunthard Kraus, DG8GB*

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*Since issue 2/2006 there has been an advert for Monitoring Monthly on the inside back page of this magazine. When I contacted Kevin Nice to get the advert for this issue he told me that Monitoring Monthly has ceased publication. This is another victim of the current financial circumstances and the falling interest in our hobby. This magazine is secure, the only thing that will cause a problem is the lack of articles to publish. It is more and more difficult to find suitable articles. I am always looking for articles to fill the additional space available in this English version of the magazine because I carry less advertising than the German version (UKW Berichte). If you have a suitable article for this magazine please contact me, I can help format your article and offer small payment for your work.*

*This issue has some very interesting articles, in particular the insight into the design and development of interdigital capacitors by Gunthard Kraus will be extremely useful for those readers who design their own projects.*

*73s - Andy*

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*Aristoteles Tsiamitros, DD5FT*

# Cascade synthesis of active bandpass filters

**In my last article, cascade synthesis was applied to example active lowpass filters [6]. A practical guide to the design of bandpass filters follows using the same method.**

**This is carried out with the program SCILAB [7], by specifying lowpass-bandpass filter transformation to give component calculation.**

**The objective of the cascade synthesis is to split the system function of the bandpass filter into a product of two sub functions. The split is realised as partial filters. The product of the sub functions corresponds to the series connection of the partial filters that are decoupled from one another. Different solutions can be derived by appropriate selection of the type of filter for the partial filters.**

## 1.

## Introduction

The developer has to solve different mathematical tasks during the design of higher order active bandpass filters that

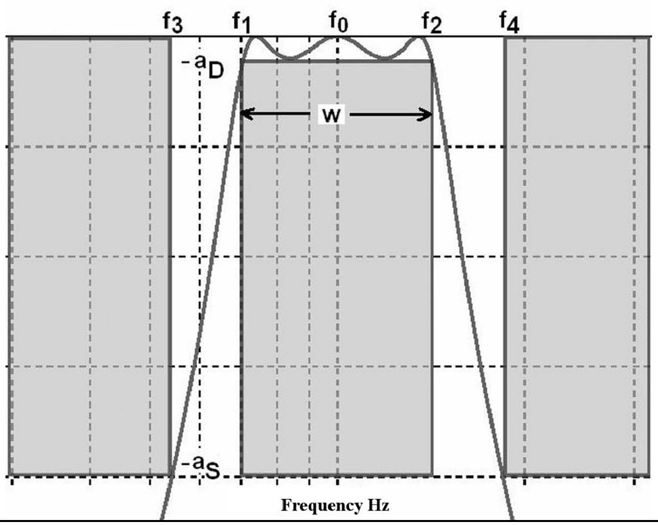



**Fig 1: Tolerance pattern for bandpass filters: Amplification in dB over the frequency range.**

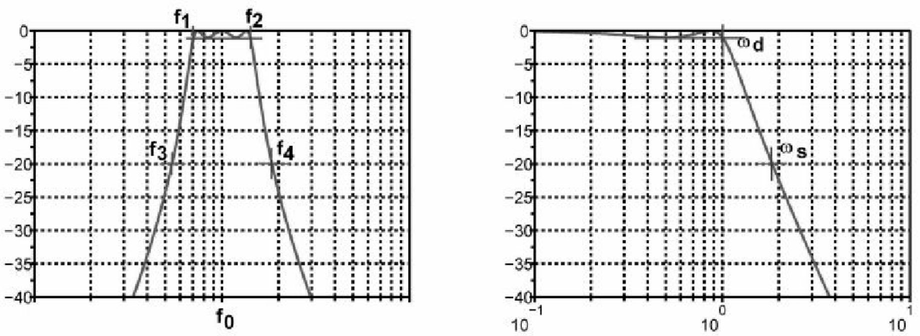



**Fig 2: Bandpass-lowpass filter transformation with: $\varpi_D = 1$ and $\varpi s = f_4 - f_3/f_2 - f_1$**

have a high cost of computation. It can be accomplished using lowpass-bandpass filter transformation the determining the high order roots of a polynomial degree afterwards. The free program SCILAB [7] is very helpful with these mathematical tasks as well as the lowpass-bandpass filter transformation where the pole positions of a system are computed. Filter design with SCILAB consists of a few procedures that are described in the following text before they are demonstrated in the next section by an example.

### 1.1. Individual steps

The design begins with the specification of the bandpass filter in the tolerance pattern (Fig 1). From this the pass and notch frequency of a reference lowpass filter can be determined (Fig 2). If its characteristics are specified (e.g. Butterworth, Tschebyscheff, etc.), the order and its system function can be determined afterwards. An all pole filter is used for the reference lowpass filter, whose system function has the form shown in Fig 3.

Using the lowpass-bandpass filter transformation (see sections 2 and 3) the system function of the bandpass filter required is finally determined. The system function of the filter from the example is shown in Fig 4.

The order of the bandpass filter is in each case is twice as high as the reference lowpass filter. By the transformation each pole position of the reference lowpass filter (see fig. 5) produces conjugate complex pairs of poles (see Fig 6). In addition the complex angular frequency appears in the numerator of the system function. The bandpass filter has zeros

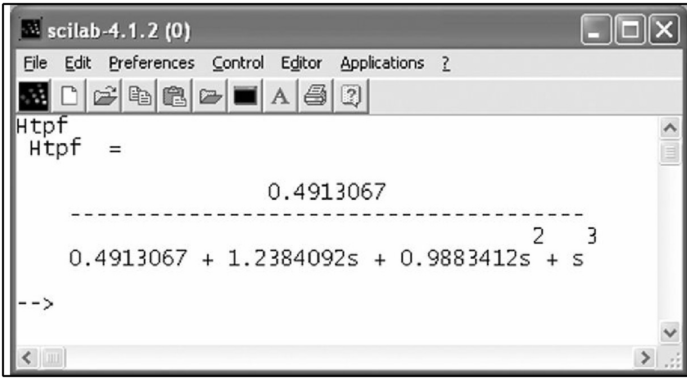



**Fig 3: System function of the reference lowpass filter.**

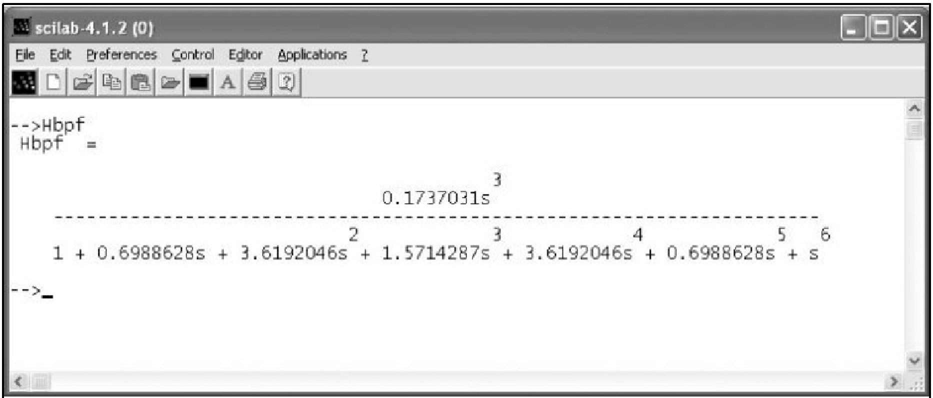



**Fig 4: System function of the bandpass filter.**

with s = 0; their number is equal to the order of the reference lowpass filter. The filter is realised as follows with the cascade technology. In filter synthesis using cascade technology the system function of the bandpass filter is a product of two sub functions. Degree split up is realised by partial filters.

A partial filter has two conjugate complex pole positions and 0, 1, or 2 zeros.

The system function of the partial filters has the following form:

$$H_{Teilfilter} = \frac{ks^i}{s^2 + as + b} \qquad i = 0,1,2$$

The zeros determine the type of filter, so that a partial filter can be implemented as lowpass (i = 0), bandpass filter (i = 1) or high pass filter (i = 2). The circuits for the individual partial filters can be selected according to the different criteria. Some examples can be found in the appendix.

In the next section there are two different solutions as examples. In the first all partial filters are implemented as band-

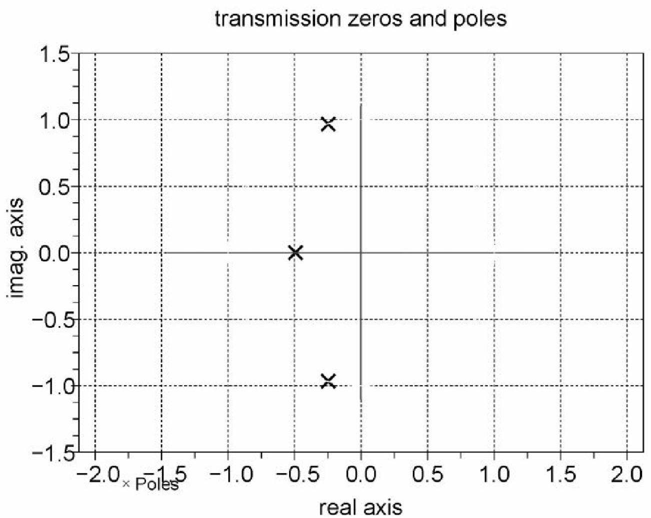



**Fig 5: Pole zero diagram of the reference of lowpass filter.**

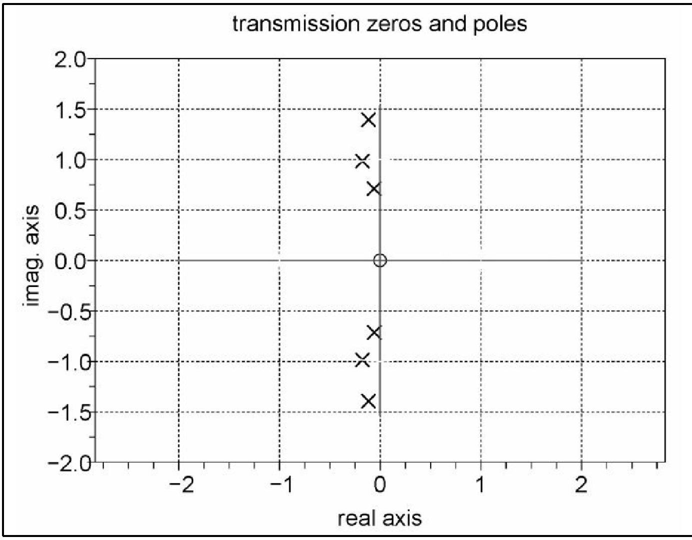
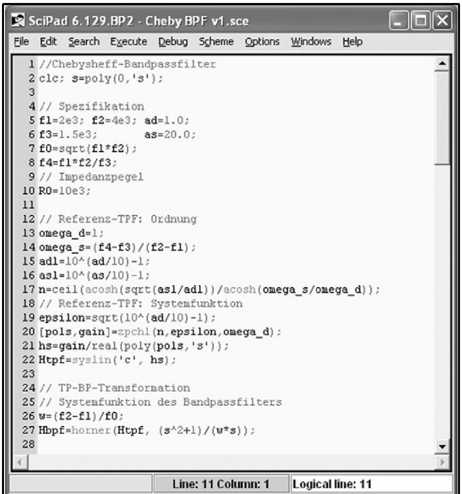



**Fig 6: Pole zero diagram of the bandpass filter.**

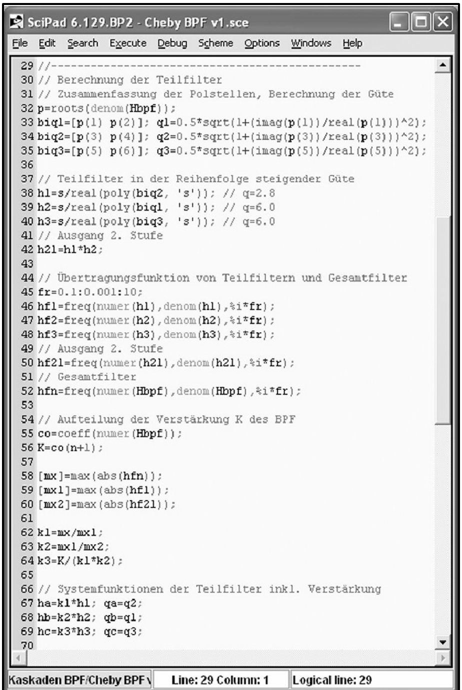
pass filters. In the second bandpass filters are derived from a series connected low-pass, band-pass and high pass filter.

The SCILAB script for the first solution is listed in Fig 7 to 10. The script for the second solution is largely identical. The partial filters are arranged in order of rising quality. The overall gain of the bandpass filter is divided in such a way that the maximum at the output of the



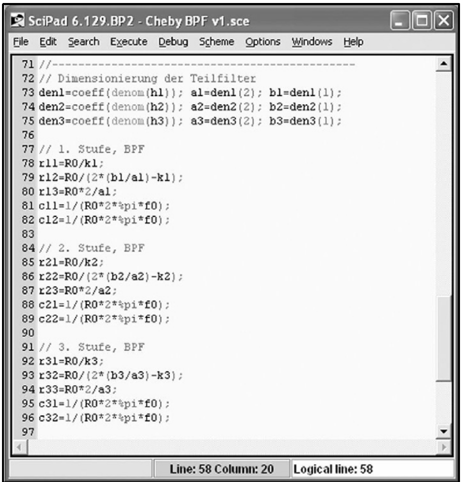

```
//Chebysheff-Bandpassfilter
clc; s=poly(0,'s');

// Spezifikation
f1=2e3; f2=4e3; ad=1.0;
f3=1.5e3;       as=20.0;
f0=sqrt(f1*f2);
f4=f1*f2/f3;
// Impedanzpegel
R0=10e3;

// Referenz-TPF: Ordnung
omega_d=1;
omega_s=(f4-f3)/(f2-f1);
ad1=10^(ad/10)-1;
as1=10^(as/10)-1;
n=ceil(acosh(sqrt(as1/ad1))/acosh(omega_s/omega_d));
// Referenz-TPF: Systemfunktion
epsilon=sqrt(10^(ad/10)-1);
[pols,gain]=zpch1(n,epsilon,omega_d);
hs=gain/real(poly(pols,'s'));
Htpf=syslin('c', hs);

// TP-BP-Transformation
// Systemfunktion des Bandpassfilters
w=(f2-f1)/f0;
Hbpf=horner(Htpf, (s^2+1)/(w*s));

```

**Fig 7: Determining the reference lowpass filter and the system function of the bandpass filter.**




```
//-----------------------------------------------
// Berechnung der Teilfilter
// Zusammenfassung der Polstellen, Berechnung der Güte
p=roots(denom(Hbpf));
biq1=[p(1) p(2)]; q1=0.5*sqrt(1+(imag(p(1))/real(p(1)))^2);
biq2=[p(3) p(4)]; q2=0.5*sqrt(1+(imag(p(3))/real(p(3)))^2);
biq3=[p(5) p(6)]; q3=0.5*sqrt(1+(imag(p(5))/real(p(5)))^2);

// Teilfilter in der Reihenfolge steigender Güte
h1=s/real(poly(biq2, 's')); // q=2.8
h2=s/real(poly(biq1, 's')); // q=6.0
h3=s/real(poly(biq3, 's')); // q=6.0
// Ausgang 2. Stufe
h21=h1*h2;

// Übertragungsfunktion von Teilfiltern und Gesamtfilter
fr=0.1:0.001:10;
hf1=freq(numer(h1),denom(h1),%i*fr);
hf2=freq(numer(h2),denom(h2),%i*fr);
hf3=freq(numer(h3),denom(h3),%i*fr);
// Ausgang 2. Stufe
hf21=freq(numer(h21),denom(h21),%i*fr);
// Gesamtfilter
hfn=freq(numer(Hbpf),denom(Hbpf),%i*fr);

// Aufteilung der Verstärkung K des BPF
co=coeff(numer(Hbpf));
K=co(n+1);

[mx]=max(abs(hfn));
[mx1]=max(abs(hf1));
[mx2]=max(abs(hf21));

k1=mx/mx1;
k2=mx1/mx2;
k3=K/(k1*k2);

// Systemfunktionen der Teilfilter inkl. Verstärkung
ha=k1*h1; qa=q2;
hb=k2*h2; qb=q1;
hc=k3*h3; qc=q3;

```

**Fig 8: Determining the system functions of the partial filters.**



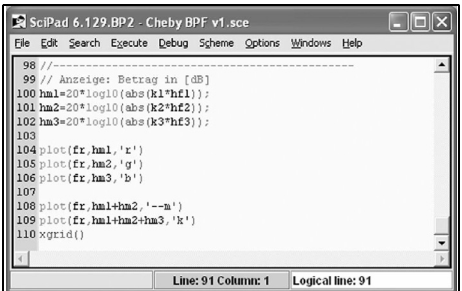
```
SciPad 6.129.BP2 - Cheby BPF v1.sce
File Edit Search Execute Debug Scheme Options Windows Help
//----------------------------------------------
// Dimensionierung der Teilfilter
den1=coeff(denom(h1)); a1=den1(2); b1=den1(1);
den2=coeff(denom(h2)); a2=den2(2); b2=den2(1);
den3=coeff(denom(h3)); a3=den3(2); b3=den3(1);

// 1. Stufe, BPF
r11=R0/k1;
r12=R0/(2*(b1/a1)-k1);
r13=R0*2/a1;
c11=1/(R0*2*%pi*f0);
c12=1/(R0*2*%pi*f0);

// 2. Stufe, BPF
r21=R0/k2;
r22=R0/(2*(b2/a2)-k2);
r23=R0*2/a2;
c21=1/(R0*2*%pi*f0);
c22=1/(R0*2*%pi*f0);

// 3. Stufe, BPF
r31=R0/k3;
r32=R0/(2*(b3/a3)-k3);
r33=R0*2/a3;
c31=1/(R0*2*%pi*f0);
c32=1/(R0*2*%pi*f0);

Line: 58 Column: 20   Logical line: 58
```

**Fig 9: Design of the partial filters.**

partial filters in each stage is equal to the maximum at the filter output. In this way the amplitude response in the pass band has the smallest fluctuations.

**Note:**

The literature [5] contains an algorithm that can be used to deal with the computation of the system function and the determination of the roots of the denominator polynomial. The algorithm computes the centre frequency and the quality of the partial filters from the pole positions of a reference lowpass filter. These are to be determined easily even without SCILAB. The partial filters can be designed from this, without further detours, by making the components a function of the quality for standardised circuits (centre frequency $\omega = 1$). The calculations can be made with a simple pocket calculator, a spreadsheet or with SCILAB.



```
SciPad 6.129.BP2 - Cheby BPF v1.sce
File Edit Search Execute Debug Scheme Options Windows Help
//----------------------------------------------
// Anzeige: Betrag in [dB]
hm1=20*log10(abs(k1*hf1));
hm2=20*log10(abs(k2*hf2));
hm3=20*log10(abs(k3*hf3));

plot(fr,hm1,'r')
plot(fr,hm2,'g')
plot(fr,hm3,'b')

plot(fr,hm1+hm2,'--m')
plot(fr,hm1+hm2+hm3,'k')
xgrid()

Line: 91 Column: 1   Logical line: 91
```

**Fig 10: The amplitude response of the partial filters and the bandpass filter.**

## 2. Example: Sixth order bandpass filter

This section shows an example using cascade technology to design a sixth order Tschebyscheff bandpass. The script for SCILAB divides roughly into four parts shown in Fig 7 to 10. Fig 8, 9 and 10 are for the special case of this example. The script must be adapted for other applications e.g. larger or smaller order filters.

### 2.1. Specification

A bandpass filter with the pass band $f_1$ = 2kHz to $f_2$ = 4kHz and the maximum attenuation in the pass band od $a_D$ = 1dB. At frequency $f_3$ = 1.5kHz in the stop band an attenuation of at least $a_s$ = 20dB as shown in Fig 1. The characteristic resistance of the filter $R_0$ = 10kΩ.

### 2.2. Reference lowpass filter

The centre frequency $f_0$ of the bandpass filter is the geometrical means of the edge frequencies $f_1$ and $f_2$ and/or the notch frequencies $f_3$ and $f_4$ at the selected stop band attenuation:

$$f_0 = \sqrt{f_1 \cdot f_2} = \sqrt{f_3 \cdot f_4} = 2.8284\,kHz$$

If the lower notch frequency f3 is given, the upper notch frequency is given by:

$$f_4 = \frac{f_1 \cdot f_2}{f_3} = 5.34\,kHz$$

For the standardised cutoff frequency of the reference lowpass filter $\omega_D$ = 1. The notch frequency is:

$$\omega_s = \frac{f_4 - f_3}{f_2 - f_1} \quad \text{as shown in Fig 2}$$

It is ϖs = 1.916.

Thus the definition of the reference low-pass filter is summarised:

- Pass frequency $\omega_D = 1$,
- Passband attenuation $a_D$ = 1dB
- Notch frequency $\omega_s$ = 1,916
- Stop band attenuation $a_s$ = 20dB.

Thus the filter order (n) of the reference lowpass filter can be computed:

$$n = \frac{a\cosh\left(\sqrt{\frac{10^{a_s/10} - 1}{10^{a_D/10} - 1}}\right)}{a\cosh\left(\frac{\omega_s}{\omega_D}\right)}$$

In the script (Fig 7) $f_0$ and $f_4$ are computed in the lines 7 and 8. The impedance of the bandpass filter is fixed in line 10 with $R_0$ = 10kΩ. The cutoff frequency $\omega_D$ and the notch frequency ws are determined in the lines 13 and 14. The attenuation $a_D$ can be use to calculate the filter order using the formula in line 17. It is n = 2.89. This value is rounded up by the function "ceil () " to n=3.

The system function of the reference lowpass filter Htpf (s) is calculated in line 22 and is shown in Fig 3. By inserting the function "plsz (Htpf) " in the script, the pole zero diagram of the reference lowpass filter shown in Fig 5 can be generated.

## 2.3. LP-BP transformation

A bandpass filter can be derived from a lowpass filter using the lowpass-band-pass filter transformation. But the complex angular frequency "s" becomes "s2 + 1 / w.s" in the system function for the lowpass filter. w is the relative range for the example:

$$w = \frac{f_2 - f_1}{f_0} = 0.707$$

Next the powers are simplified and new variables calculated (in the example the second and third power) for the terms in the numerator and denominator. This work can be left to SCILAB. The function "horner" in line 27 accomplishes the substitution and simplification; the result is shown in Fig 4.

The bandpass filter has three conjugate complex pairs of poles as well as three zeros at the origin, according to the term $s^3$ in the numerator of the system function. They are represented in the pole zero diagram in Fig 6, this diagram was produced by inserting the function "plzr (Hbpf)" in the script. The crosses in the diagram mark the pole positions and the circles mark the zeros. The filter order (highest power in the denominator of the system function) is 6. The highest power in the numerator is 3. The filter has 6 - 3 = 3 further zeros in the infinite as well as the three zeros at the origin.

## 2.4. Computation of the partial filters

In the line 32 of the script (Fig 8) the pole positions of the bandpass filter are computed and assigned to the variable p. The number of the pole positions on the screen is suppressed in the script by a semicolon at the end of the line. If p is entered in the input line of SCILAB then the pole positions are listed in complex form:

$p_1$ = -0.059 + j0.712

$p_2$ = -0.059 - j0.712

$p_3$ = -0.174 + j0.984

$p_4$ = -0.174 - j0.984

$p_5$ = -0.155 + j1.395

$p_6$ = -0.115 - j1.395

The partial filters are defined by the conjugated complex pole positions in the lines 33 to 35 using a matrix. The matrix

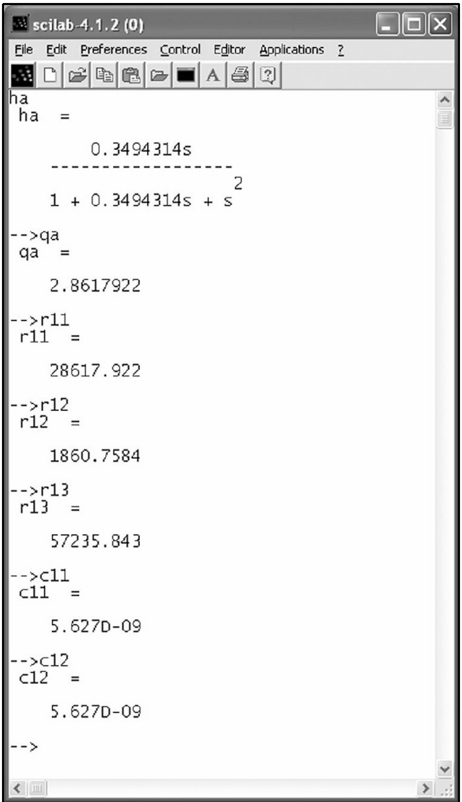



**Fig 11: System function, quality and components of one stage of the first solution.**

is used in lines 38 to 40 as parameters for the function "poly" that forms the system function of the partial filters $h_1$ to $h_3$. In addition in the lines 33 to 35 the pole qualities; $q_1 = 6.05$, $q_2 = 2.86$, $q_3 = 6.05$ are computed. They decide the sequence of the partial filters in the complete circuit. As mentioned the partial filters are connected in order of rising quality. The partial filter $h_1$ has the complex pole positions with the lowest pole quality "biq2". Therefore the sequence of partial filters from input to output of the complete filter is $h_1$, $h_2$, $h_3$. The numerators of the system functions in lines 38 to 40 determine the respective type of filter.

## 2.5. Allocation of attenuation

The system functions $h_1$, $h_2$, $h_3$ in lines 38 to 40 are not yet complete. The gain of stages $k_1$, $k_2$ and $k_3$ are missing. These gains are determined numerically from the amplitude responses of the partial filters. The system functions at the output of each stage are required. They are the product of the system functions of the preceded stages. The system function at the output of the second stage $h_{21} = h_1 \cdot h_2$. If the complete filter consists of more than three stages, $h_{31} = h_1 \cdot h_2 \cdot h_3$, etc. up to the penultimate stage $h_{(n-1)\,1} = h_1 \cdot h_2 \cdot h_3 \cdot \cdot \cdot h_{n-1}$. The product of the system functions of all stages is, of course, the system function of the complete filter from Fig 4.

The transfer functions of the individual stages $h_{f1}$, $h_{f2}$, $h_{f3}$ are calculated in lines 45 to 52, as well as the transfer function up to the output of the second stage $h_{f21}$ and the complete filter $h_{fn}$.

The transfer function is the evaluation of the system function along jω axis. The frequency limits from $f_r = 0.1$ to $f_r = 10$ are selected in line 45.

The frequency $f_r$ is normalised to the centre frequency $f_0$. The gain of the complete filter "K" is calculated in lines 55 and 56. The maximum at the output of the filter "mx" and the maxima at the output of the first and second stage "mx1" and "mx2" are calculated in lines 58 to 60 from the transfer functions. These maxima do not include the stage gain so that the maximum at the output of each stage must include the gain of the stages:

$k_1 \cdot mx_1 = mx$

$k_2 \cdot mx_2 = mx_1$

$k_3 \cdot mx_3 = mx_2$

etc. to $k_{n-1}$.

The gain of the last stage $k_n$ must be the product of the gain of the individual stages and is equal the overall gain "K" of the bandpass filter:

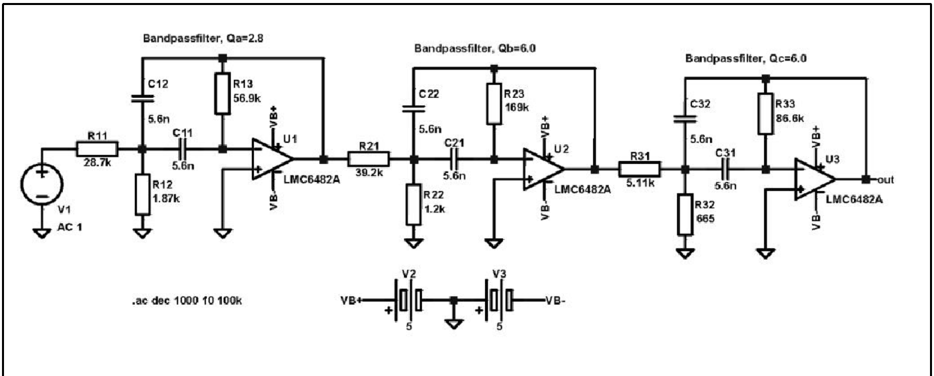



**Fig 12: Complete circuit of the bandpass filter for the first solution.**

$$k_n = \frac{K}{k_1 \cdot k_2 \cdots k_{n-1}}$$

The gain $k_1$, $k_2$ and $k_3$ for the three stages of the example are calculated in lines 62 to 64. The complete system functions of the partial filters and their quality are finally given in lines 67 to 69.

### 2.6. Designing the partial filters: First solution

If a zero is assigned at the origin of each of the partial filters a bandpass filter is defined. The circuit of a second order bandpass filter is shown in the appendix, Fig 18. Its system function from [1], was transformed for the case where $C_1 = C_2 = 1$. The component values are calculated using the formulae given in the text.

Fig 11 shows the system function of the first partial filter as well as its quality and component values. They were found individually using the input line of SCILAB, the variable name was input and <Enter> pressed. The remaining system functions and component values can be found using the same method, or removing the semicolon at the end of the appropriate lines will automatically show them. The

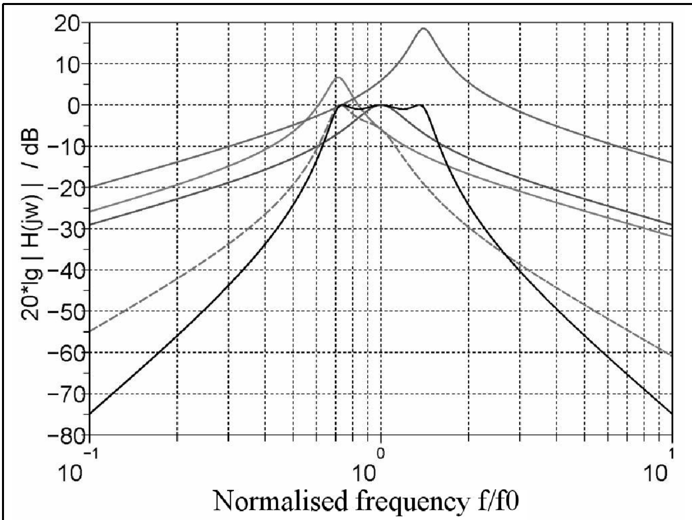



**Fig 13: Tschebyscheff bandpass filter. First solution: Amplitude response of the individual partial filters and at the output of the second stage**

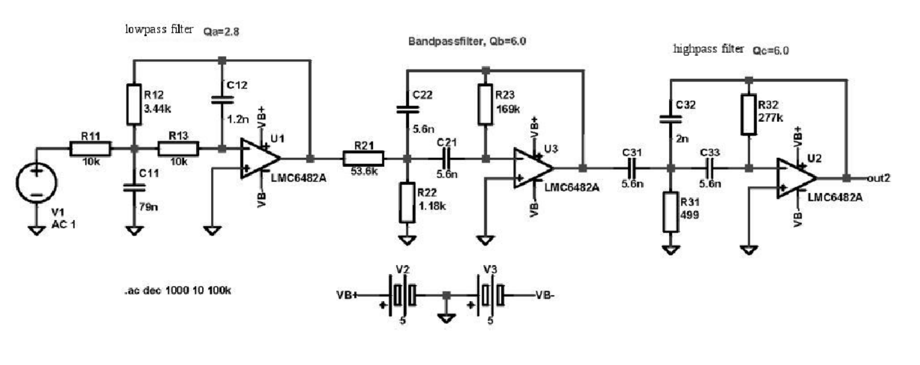



**Fig 14: Complete circuit of the bandpass filter for the second solution.**

complete circuit of the filter is shown in Fig 12. The amplitude responses are shown in Fig 13

**Note:**

To plot Fig 13 (and Fig 15) correctly the logarithmic frequency scale must be changed. To do this the SCILAB graphics editor "plot()" is used.. Click on "GED" to open the dialogue "Axes editor". In the "Object Browser" click "Axes". Under "Axis options" use the option "log" for the x axis. The dialogue has other attributes e.g. the legend for the axes; the font, size and orientation of the characters etc.

## 2.7. Designing the partial filters: Second solution

The first partial filter is a lowpass filters, the second partial filter is a bandpass filter the same as the first solution, and the third partial filter is a high pass filters.

The script for the second solution is a copy of the first script with the following lines changed. The zeros of the system functions (numerators $h_1$, $h_2$ and $h_3$) in lines 38 to 40 are change to:

- 38 h1=1/real (poly (biq2, "s")); // q=2.8
- 39 h2=s/real (poly (biq1, "s")); // q=6.0
- 40 h3=s^2/real (poly (biq3, "s")); // q=6.0

Further changes are necessary in the design of the filter stages. Lines 77 to 82 must be changed to the design equations for the lowpass in the appendix, chapter 5.1:

- 77 // 1. Stage, TPF
- 78 r11=R0;
- 79 r12=R0*k1/b1;
- 80 r13=R0;
- 81 c11= (2*k1+b1)/ (a1*k1*R0*2*%pi*f0);
- 82 c12=a1/ ((2*k1+b1) *R0*2*%pi*f0);

The second stage (lines 84 to 89) in both solutions is a bandpass filter. The script remains unchanged. The third stage must be changed for a high pass filter, lines 91 to 96 are changed to the design equations in the chapter 5.2:

- 91 // 3. Stage, HPF
- 92 c31=1/(R0*2*%pi*f0);
- 93 c32=1/(k3*R0*2*%pi*f0);

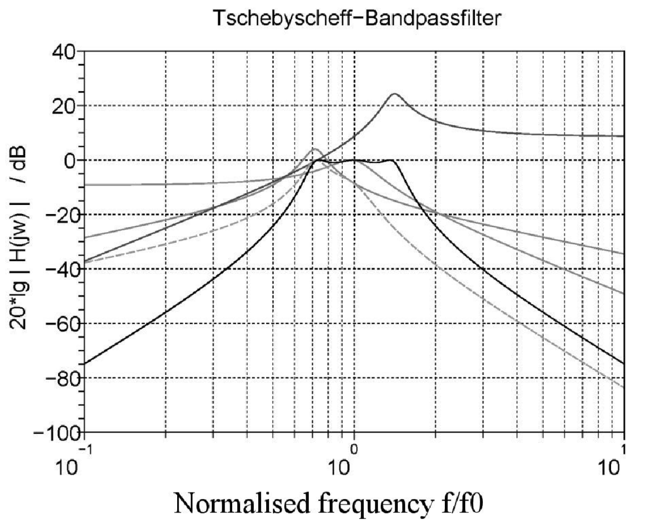



**Fig 15: Second solution: Amplitude response of the individual partial filters, output of the second stage and the complete filter.**

- 94 c33=1/(R0*2*%pi*f0);
- 95 r31=R0*a3*k3/(b3* (2*k3+1));
- 96 r32=R0* (2*k3+1) /a3;

The complete circuit of the filter is shown Fig 14. The amplitude response of the individual stages as well as the total filter is shown in Fig 15.

## 3. Summary

The design of active bandpass filters was presented using cascade technology with the help of the mathematical program SCILAB. The individual steps of the filter development were described by an example. The user has total control of the design for both the type of filter, and the special circuits of the partial filters themselves.

## 4. Literature

[1] Active filters and oscillators, Lutz V. Wangenheim, Springer publishing house, 2008

[2] Monolith technology; Chapter 13: Active filters, U. Tietze, Ch. Schenk, Springer publishing house, 12. Edition, 2002

[3] High Q Factor Circuits with Reduced Sensitivity, T. Deliyannis, Electronics Letters 27th Dec. 1968, volume. 4, No. 26, pp.577-579

[4] A Practical Method of Designing RC Active Filters, R.P. Sallen, E.L. keys, IRE Transactions, CT-2, 1955, p. 74-85

[5] Designers Guide to: Active bandpass filters, P.R. Geffe, EDN, April 5, 1974, pp. 46-52

[6] Example active low pass filters, Aristoteles Tsiamitros, DD5FT, VHF Communications Magazine 4/2008 pp 219 - 230

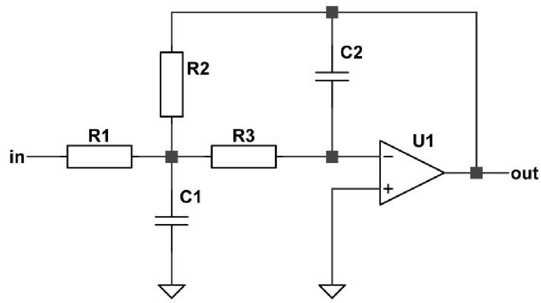



**Fig 16: Circuit of a 2nd order lowpass filter.**

[7] SCILAB homepage; www.scilab.org

[8] Engineering and Scientific Computing with SCILAB, C. Bunks, u.a., Birkhäuser, 1999

## 5. Appendix

The circuits in this section are only examples of second order active RC-filters that can be used as components to produce bandpass filters. Further configurations can be found in [1] to [4].

### 5.1. Second order lowpass filter

The system function is given in the following form:

$$H(s) = -\frac{k}{s^2 + as + b}$$

The circuit is shown in Fig 16. The component values are found as follows:

After definition of the resistors $R_1 = R_3 = 1$, the circuit specific system function is:

$$H_{RC}(s) = -\frac{\frac{1}{C_1 C_2}}{s^2 + \frac{1}{C_1}\left(2 + \frac{1}{R_2}\right)s + \frac{1}{R_2 C_1 C_2}}$$

Using both the system functions and the current transfer ratio (with s = 0) the remaining components are given as follows:

$$R_2 = \frac{k}{b} \qquad C_1 = \frac{2k+b}{ak} \qquad C_2 = \frac{a}{2k+b}$$

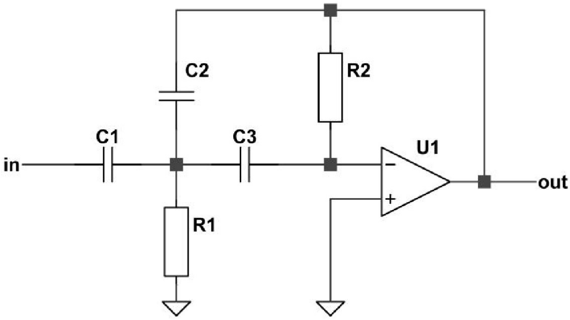



**Fig 17: Circuit of a 2nd order high pass filter.**

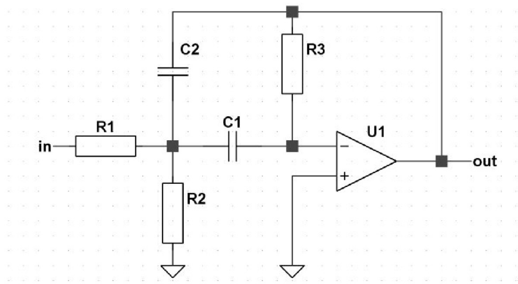



**Fig 18: Circuit of a 2nd order bandpass filter.**

## 5.2. Second order High pass filter

The system function is given in the following form:

$$H(s) = -\frac{ks^2}{s^2 + as + b}$$

The circuit is shown in Fig 17. The component values are found as follows:

After definition of the capacitors $C_1 = C_3 = 1$, the circuit specific system function is:

$$H_{RC}(s) = -\frac{\frac{1}{C_2}s^2}{s^2 + \frac{2+C_2}{R_2C_2}s + \frac{1}{R_1R_2C_2}}$$

Using both the system functions and the current transfer ratio (with s = 0) the remaining components are given as follows:

$$C_2 = \frac{1}{k} \qquad R_1 = \frac{ak}{b(2k+1)} \qquad R_2 = \frac{2k+1}{a}$$

## 5.3. Second order bandpass filter

The general system function is given in the following form:

$$H(s) = -\frac{ks}{s^2 + as + b}$$

The circuit is shown in Fig 18. The component values are found as follows:

After definition of the capacities $C_1 = C_2 = 1$, the circuit specific system function is:

$$H_{RC}(s) = -\frac{\frac{1}{R_1}s}{s^2 + \frac{2}{R_3}s + \frac{1}{R_3}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}$$

Using both the system functions and the current transfer ratio (with s = 0) the remaining components are given as follows:

$$R_1 = \frac{1}{k} \qquad R_2 = \frac{1}{2\frac{b}{a} - k} \qquad R_3 = \frac{2}{a}$$

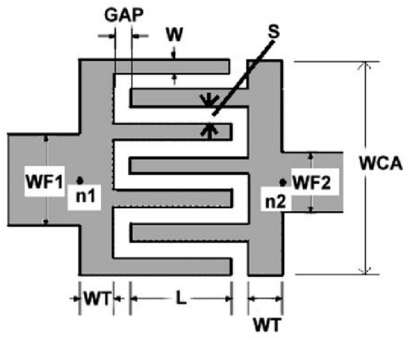
*Gunthard Kraus, DG8GB*

# Ansoft Designer SV project: Using microstrip interdigital capacitors

**Very small coupling capacitors are required for bandpass filters in the frequency range between 100MHz and 1GHz, often with values under 0.5pF. Implementing these interdigital capacitors in microstrip gives some advantages. This will be demonstrated in the following practical development.**

## 1. Introduction

As an introduction into microstrip interdigital capacitors (Fig 1), an extract from the on-line help of the CAD program




| Properties | Description | Units | Default | Range |
|---|---|---|---|---|
| N | Number of fingers | none | Required | ≥ 2 |
| W | Finger width | m | Required | > 0 |
| S | Finger spacing | m | Required | > 0 |
| L | Length of finger overlap | m | Required | > 0 |
| WT | Terminal strip width | m | Required | ≥ 0 |
| WF1 | Line width at port 1 | m | Required | > 0 |
| WF2 | Line width at port 2 | m | Required | > 0 |
| WCA | Capacitor width | m | N*W+(N-1)*S | ≥ N*W+(N-1)*S |
| GAP | Gap between end of finger and terminal strip | m | Required | > 0 |
| sub | Substrate name | none | Required | string |
| CoSimulator | Simulation engine | none | Circuit | Circuit, Planar EM |

**Fig 1: The famous interdigital capacitor. Easily to manufacture but because of the many measurements some work to design.**

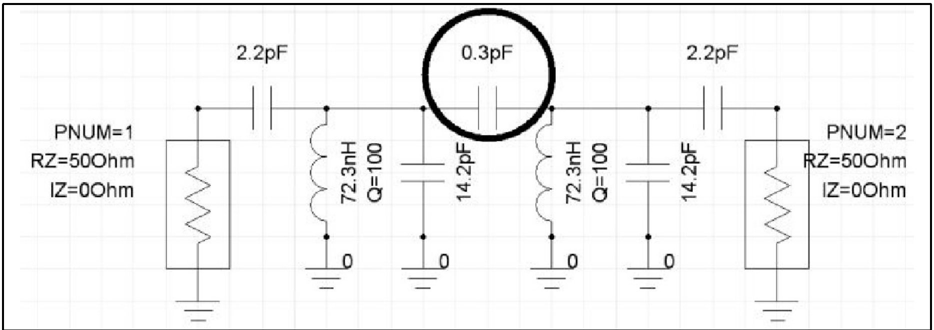



**Fig 2: The Ansoft filter tool supplies the finished circuit. The coupling capacitor to be investigated is marked with a circle.**

gives all the necessary explanation and details.

The design is not simple, however modern microwave CAD programs facilitate simulation; these should already contain this component in their component library as a microstrip model.

That is the case for the free Ansoft Designer SV software, this is the list of the advantages:

- After optimisation of the PCB layout very small tolerances are achieved leading to good reproducibility of filter parameters without additional components or assembly costs for quantity production.
- No discrete components need to be soldered. These would be difficult to obtain for such small capacitances and exhibit larger tolerances.
- Using high quality printed circuit board material with the smallest losses produces very high quality capacitors that are useful up to more than 10GHz.

## 2. The project, a 145MHz bandpass filter

A bandpass filter with the following data is to be designed, built and measured:

- Centre frequency: 145MHz
- Ripple bandwidth: 2MHz
- System resistance Z: 50Ω
- Filter degree: n = 2
- PCB size: 30mm x 50mm
- Tschebyschev narrow bandpass filter type with a Ripple of 0.3dB (coupled resonators)
- PCB material: Rogers RO4003, thickness: 32MIL = 0.813mm, $\varepsilon_r$ = 3.38, TAND= 0.001
- Housing: Milled aluminium
- Connection: SMA plug

**First design:**

- Filter coils NEOSID (type 7.1 E with shielding can, L = 67 - 76nH, single coil, quality Q = 100… 150, brass adjustment core)
- SMD ceramic capacitors 0805, NP0 material

The filter program contained in Ansoft Designer SV was used. The development of the circuit after the draft and a short optimisation is shown in Fig 2. The further work necessary to produce the finished PCB layout is described in the following article. A prototype was produced and tested using a network analyser to give the measurement results.

The design of the filter using Ansoft Designer SV giving all the steps leading to Fig 2 is shown in Appendix 1.

Appendix 2 contains guidance for successful control of the circuit simulation using Ansoft Designer SV.

It will also be helpful to download a copy of the authors tutorial on using Ansoft Designer SV. This is available free of charge in German or English from the web site [1].

To continue with the filter development; a look at the circuit of Fig 2 shows:

- The problematic coupling capacitor C = 0.3pf is identified by the black circle. The problem is not only the very small capacitance but also the high requirement for accuracy. A deviation of more than 1% gives a noticeable change in the transmission characteristics.
- It was optimised until all remaining capacitors can be realised using standard values, if necessary by parallel connection of several capacitors with different values.

## 3.

## Design procedure for interdigital capacitors with Ansoft Designer SV

### 3.1. Input problems

The component in the model library is under "Circuit Elements/Microstrip/ Capacitor/MSICAPSE". The layout of the interdigital capacitor in series connection is shown in Fig 1. Double click on the circuit symbol to access the list of the dimensions. At the end of the list there is a "MSICAP" button that opens the on-line help with an explanation of the individual inputs and dimensions. Experience is required to make these inputs but if the following rules are used then incorrect inputs will be avoided:

- Set the finger width W to 0.5mm. This ensures that the design does not become too large and under etching has less effect on the finger width when the PCB is made.
- The gap width S should not be TOO small otherwise the PCB manufacturer complains. A value of 0.25mm can be achieved even in your own workshop. On the other hand it should not be too large because then the capacitance value falls, requiring larger finger lengthens or more fingers.
- The number of the fingers and their length specifies the capacitance value. As an example, start with 4 fingers and vary the length of the fingers ensuring that they do not become too large. Set an upper limit of about 8 to 10mm. Instead of making the fingers longer simply increase the number of fingers.

With this data (and the PCB data) a draft design can begin BUT unfortunately the CAD program can make an analysis. That means that all the data and dimensions can be entered and the simulation started but the result will be an S-parameter file of the capacitor. It is only at this point that it is known if the capacitance of the draft capacitor is too large or too small.

Things become more difficult because the circuit diagram of the component has additional capacitors from each end to earth. These two unavoidable parallel capacitors detune the resonant circuits. How can these three capacitances be isolated to optimise the circuit, particularly if the filters are more complex and several interdigital capacitors are used?

### 3.2. Determination of the pure coupling capacitance

It is a challenge to determine the exact value of the coupling capacitor, but the two parallel capacitors are less difficult to deal with, just make the resonant circuit capacitors smaller in the simulation until the desired transmission curve

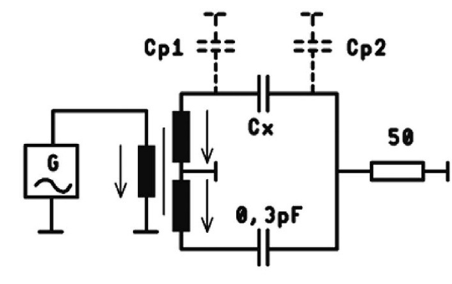



**Fig 3: Using an idea from crystal filter technology, this circuit is used to develop the exact value of the interdigital capacitor required.**

is achieved. The difference corresponds to the additional parallel capacitance contributed by the interdigital capacitor. Their value is not much different from the actual coupling capacitor.

Sometimes experience helps: e.g. crystal filters in a bridge connection presented a similar problem. In that case the housing capacitance was eliminated using a transformer circuit. The principle applied to the current problem is shown in Fig 3.

The voltage across the two secondary windings are the same magnitude but opposite phases. Thus the voltage, V, across the terminating resistor, RL, is zero if the two capacitors Cx and C2 are equal and in this case equal 0.3pF. The two parallel capacitances Cp1 and Cp2 do not play a role when the bridge is balanced thus only the value of Cx is being measured. Cp1 is parallel to the secondary winding of the transformer and cannot affect the balance of the bridge. Likewise Cp2 is in parallel with the 50Ω load resistor. In the balanced condition no voltage is developed across the parallel capacitor and the load therefore Cp2 has no effect on the circuit. This means that the value of interdigital capacitor can be simulated to be exactly the same as the known capacitor C2 and its parameters will then be known independent of the parallel capacitance values.

The simulation circuit shown in Fig 4 can be developed using Ansoft Designer SV. The transformer can be found in the component library under "Components/Circuit Elements/ Lumped/Transformers/TRF1x2" and the series connected interdigital capacitor under "Components/Circuit Elements/ Microstrip/Capacitors/MSICAPSE".

A microwave port with internal resistance of 50Ω feeds a broadband transformer with two secondary windings. The upper coil is connected to the output port by the interdigital capacitor. The opposite phase signal supplied by the lower coil is fed via a second capacitor to the output port.

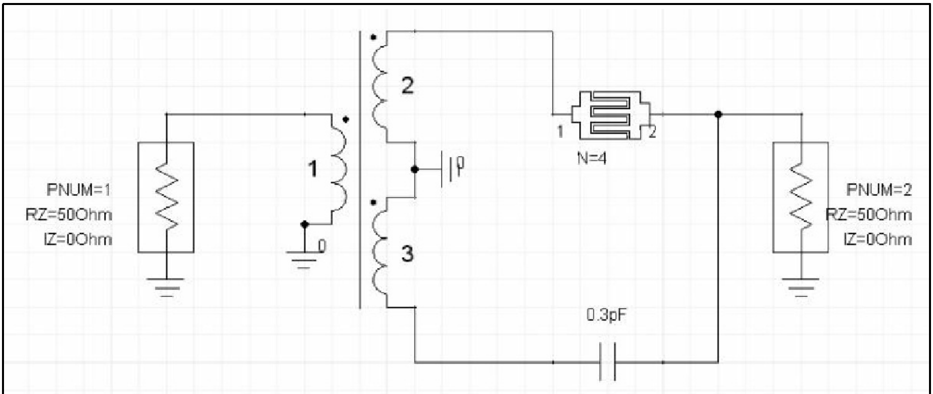



**Fig 4: Fig. 3 converted into a form for Ansoft Designer SV simulation.**

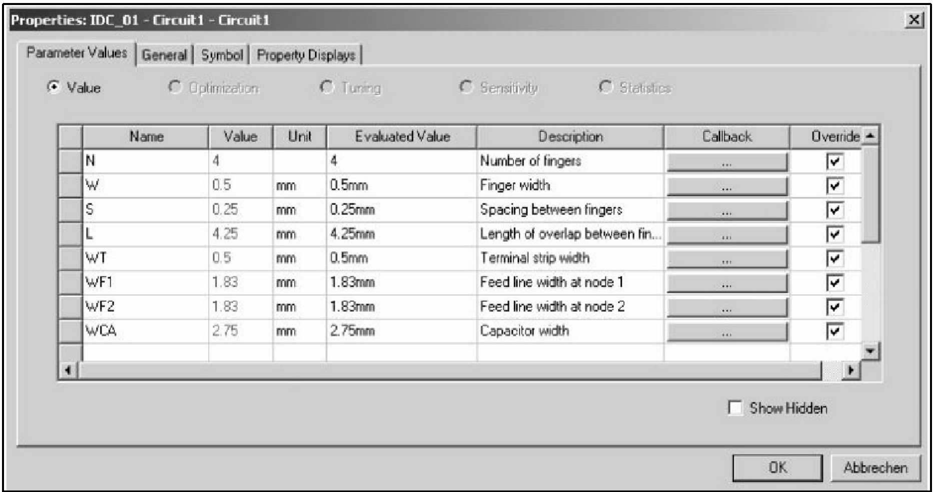



**Fig 5: Somewhat complex: the inputs required for the interdigital capacitor. Take care to examine each value. There is a line that is not visible but should not be forgotten (see text).**

**Importantly:**

This second capacitor must have the same value of 0.3pF (value of the inter-digital coupling capacitor required).

The important data for the simulation (and the later draft layout) is entered in the Property Menu of the interdigital capacitor. Double clicking on the symbol in the circuit diagram opens the menu; the entries required are shown in Fig 5.

However there are two important things that are not immediately obvious:

- There is a line missing from the window shown in Fig. 5, this can be found by scrolling down. This line to find is: GAP (between end of finger and terminal strip) = 0.25mm
- The total width "MCA" must be calculated by hand and entered into the relevant field. It should be noted that the units do not automatically default to mm so take care to enter this value otherwise the default will be metres and the simulation will be meaningless.

The above dimension is calculated as follows: MCA = 4 x Finger length + 3 x Gap width = 4 x 0.5mm + 3 x 0.25mm = 2.75mm

Finally the correct PCB material data must be selected. Scroll to the line "SUB" in the open Property Menu for the interdigital capacitor. Click on the button in the second column to open the menu "Select Substrate" and then click on "Edit". Fill out this form, as shown in Fig 6 for the RO4003 PCB material to be used: thickness = 32MIL = 0.813mm, dielectric constant εr = 3.38, tand = 0.001, copper coating 35µm thick and the roughness is 2µm. Once everything is correct click OK twice to accept the data and close the Property Menu.

Everything is now ready for the simulation. Programme for a sweep from 100MHz to 200MHz with 5MHz increments and look at the results for S21 (If you do not know the individual input steps necessary for Ansoft Designer SV they are described in appendix 2).

The finger lengths of the interdigital capacitor are varied and the simulation run again until the minimum for S21 is found. Now the bridge is balanced and

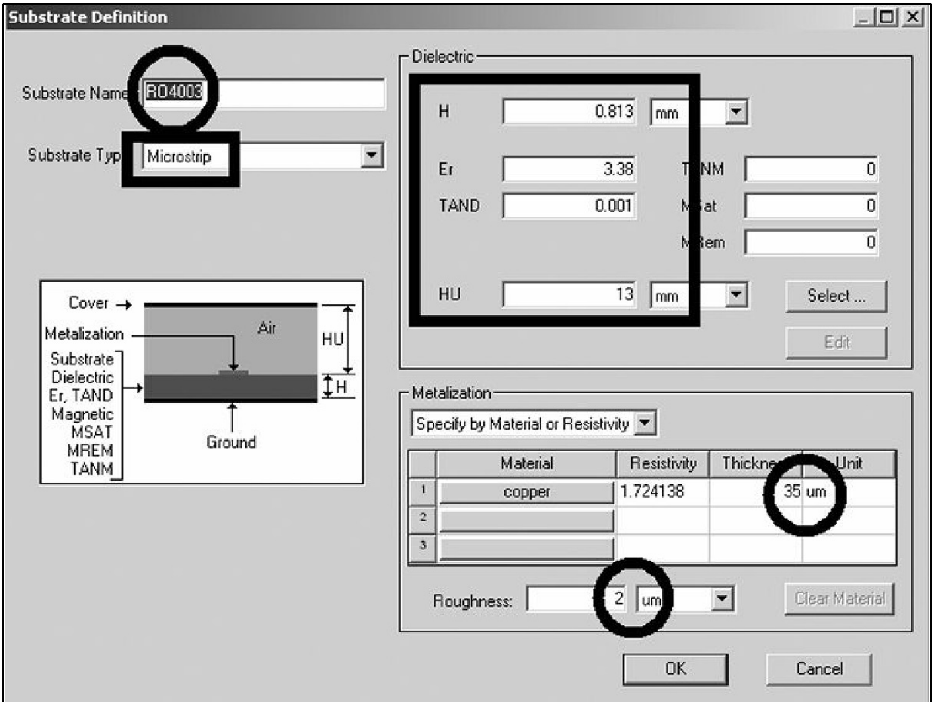



**Fig 6: The data for the Rogers R04003 PCB material are entered correctly into the Property Menu.**

the mechanical data for the interdigital capacitor with exactly the correct value can be transferred to the PCB layout. The optimised results are shown Fig 7. The finger length of 4.25mm gives a minimum for S21 and further refinement is not needed. It is interesting to see the results that the circuit will provide.

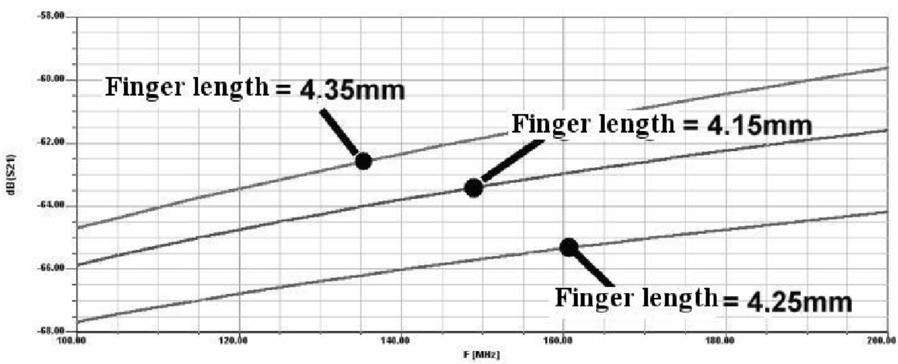



**Fig 7: The minimum is easy to recognise: a finger length of 4.25mm gives the correct value for the 0.3pF coupling capacitor.**

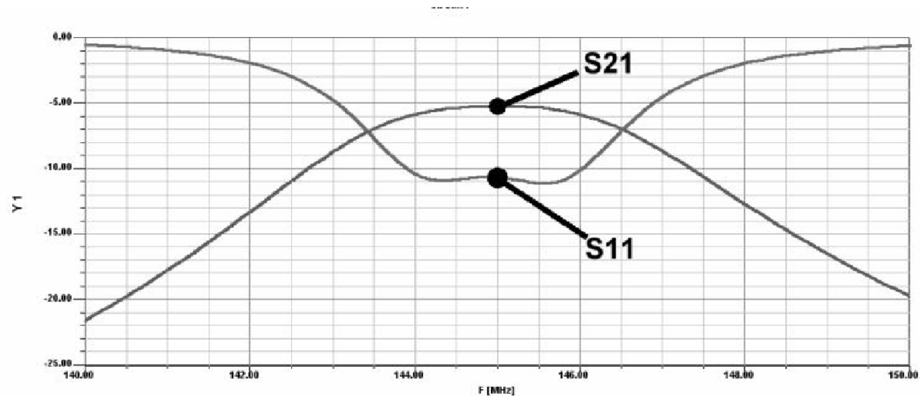



**Fig 8: This curve is the goal for this project.**

### 3.3. Completing the circuit

A new project is started with the circuit as shown in Fig 2 from the introduction (with discrete components) and the sweep adjusted from 140 to 150MHz in steps of 100kHz with S11 and S21 displayed. This result is shown in Fig 8. This is the starting point for the following actions, if these result in the same result the you can be quite content.

Replacing the 0.3pF coupling capacitor with the interdigital component that has been designed, this gives the simulation circuit shown in Fig 9. Naturally the results shown in Fig 10 are worse because the additional parallel capacitances of the interdigital capacitor have not been considered. The parallel capacitors in both resonant circuits must be reduced until the curves of Fig 8 are achieved. Fig 10 shows an additional surprise that apart from the expected shift of the centre frequency from 145MHz to 143.3MHz (caused by the parallel capacitance of the interdigital capacitor) the S11 curve has a diagonal dip. Trying to compensate this effect with different values of two parallel inductances is surprising because as S11 improves, S22 gets worse. This means that this interdigital solution has its peculiarities based on the frequency

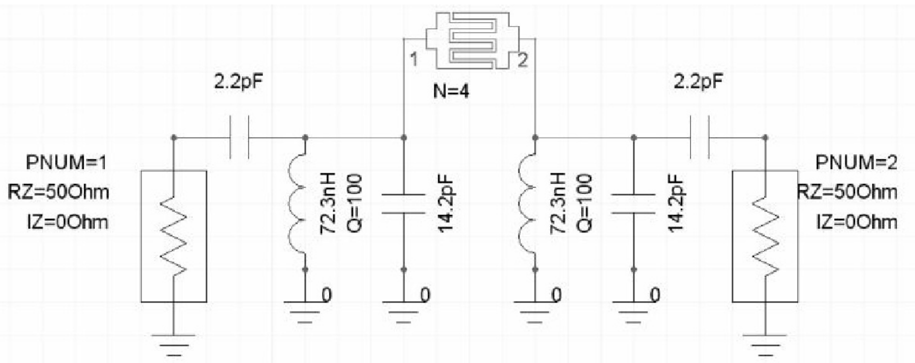



**Fig 9: The discrete 0.3pF coupling capacitor is replaced by interdigital capacitor.**

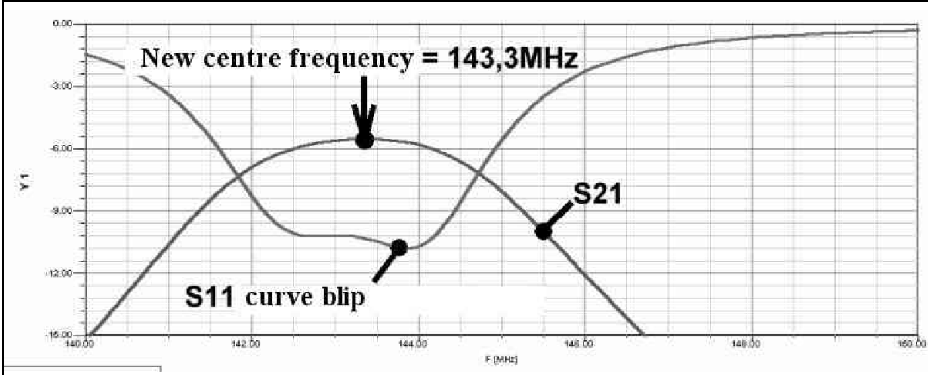



**Fig 10: The centre frequency has, as expected, moved lower and there is a diagonally dip in the S11 curve.**

response of the capacitors. Probably an alternative circuit diagram with only 3 capacitors can be imagined but the effect is more complex because it can be seen on the finished PCB. The effect can be lived with so the easy solution is just to move the centre frequency to the required value of 145MHz.

The parallel capacitors must be reduced to 13.8pf = 12pf + 1.8pf, using standard values that can be connected in parallel. The remaining adjustment is to fine tune the two coils using the adjustable cores. The new inductances of L = 72.3nH corresponds to the simulation result shown in Fig 10.

But this is not the conclusion because the PCB layout and its influence must be considered. Fig 11 shows the PCB layout that is principally a 50Ω microstrip line. It starts on the left (at the input SMA connectors) with a gap for the 2.2pF SMD coupling capacitor followed by the resonant circuit. The interdigital capacitor is in the centre and the right half is a mirror image of the left hand side. This corresponds to an additional conductor length of approximately 40mm for the circuit and this has the following consequences:

- Four additional sections of 50Ω microstrip line (with a width of 1.83mm for the given PCB data) must be added to the Ansoft Designer SV circuit if the simulation is to agree with the reality.
- The lengths of the pieces of line are 2 x 13mm = 26mm (from the SMA connector to the 2.2pF coupling ca-

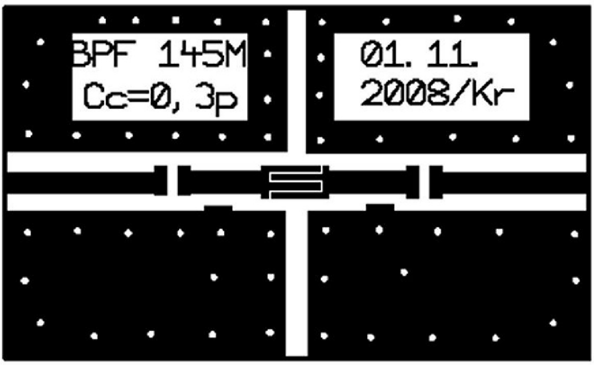



**Fig 11: The printed circuit board measures 30mm x 50mm made from Rogers RO4003 with a thickness of 0.813mm.**

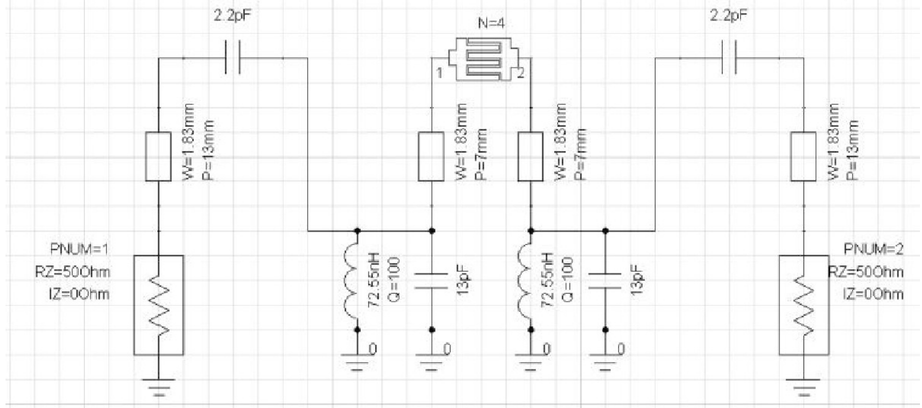



**Fig 12: The sections of microstrip line are included into the simulation to reflect the real circuit.**

pacitor) and 2 x 7mm = 14mm (from the resonant circuit to the interdigital capacitor).

Fig 12 shows the circuit. At these relatively low frequencies the microstrip line detunes capacitors so the parallel components must be adjusted again. Doing this gives the simulation results shown in Fig 13. The simulation of the wider frequency range from 100MHz to 200MHz is shown in Fig 14. Finally it is time to prepare the prototype PCB, the result after some hours of work are shown in Fig 15.

About 50 0.8mm hollow rivets were used for the plated through holes from the ground islands to the continuous lower ground surface. The SMD capacitors and coils are soldered and copper angles are screwed on to fit the SMA sockets. The adjustment cores of the coils are now easily accessible and from experience it is known that nearly no further adjustments are necessary when fitting the PCB into a machined aluminium housing.

The truth comes with the comparison of the curves of Fig 13 and 14 with the image that the network analyser produces from the prototype.

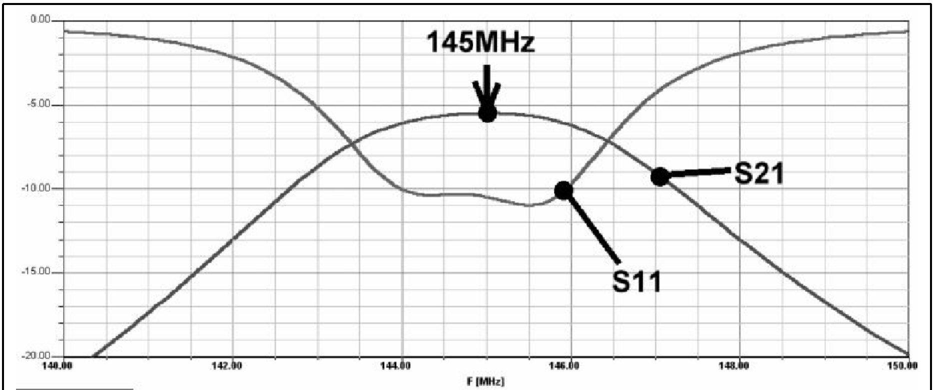



**Fig 13: If the results of measurement look the same as this simulation result the final goal will be achieved.**

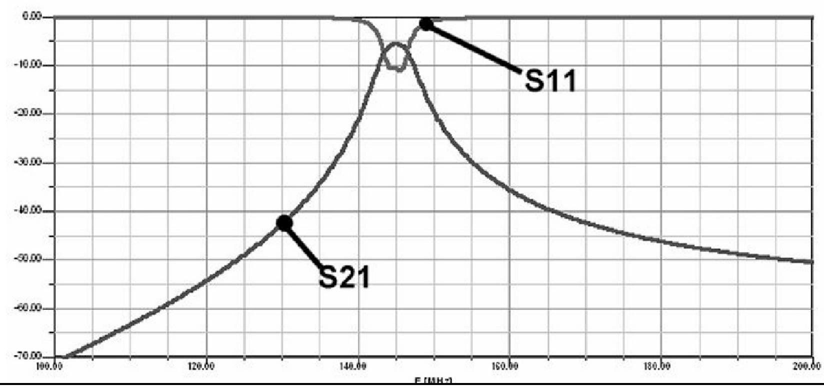



**Fig 14: The wider frequency range between 100MHz and 200MHz does not give cause for objection.**

By the way: the tear on the PCB that can be seen in Fig 15 was caused by human error. It is hard work fitting so many small rivets and takes some hours. But afterwards when finishing the PCB with a file in a hurry to see the results, too much pressure was applied. So you find out that RO4003 material can be drilled and milled but protests when it meets a stronger opponent. More care needed in future.

### 3.4. Results of measurement on the prototype

The measurements gave some unpleasant surprises shown in Fig 16, which is the S21 transmission curve (measured after correct alignment) and the simulation from Fig 13. The first mystery is that the attenuation has risen from 5.5 to 7dB at the centre frequency.

There are some doubts about the method devised to measure the value of the coupling capacitor even though the author is proud of the technique devised. So the best was to look for an owner of the APLAC simulation software (full version). APLAC has a text based command line simulator that can directly compute the value of an interdigital capacitor and the two "end capacitors". Entering the mechanical data for our capacitor design into APLAC and waiting for the result gave great relief because it gave a value of 0.29pF that is very close to the 0.3pF aimed at with Ansoft Designer SV. The interdigital capacitor is probably not the cause of the discrepancy but the sceptical

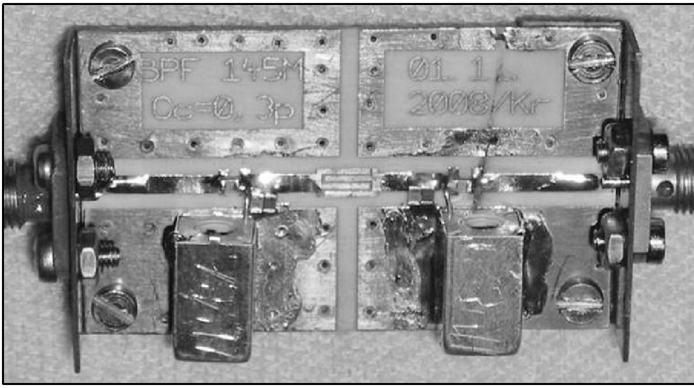



**Fig 15. The simulation converted into a prototype with SMA connectors. The circuit must now be measured on the network analyser.**

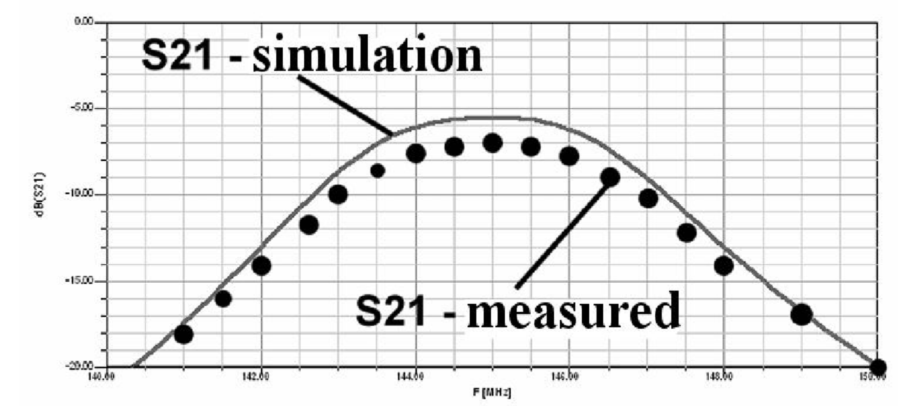



**Fig. 16: The measured S21 response shown with the simulation.**

developer leaves nothing to chance. The effect of changing the finger length by 0.2mm, and thus the coupling capacity, on the filter curve is shown in Fig 17. This gives the all-clear signal because the frequency range of the transmission curve only changes slightly but the attenuation is not affected.

This leaves the parallel coils as the possible problem (once again) because the NP0 material used in the SMD capacitors is above suspicion at these frequencies. Therefore the coil quality must be worse than shown on the data sheet (Q = 130) and the reason could be because the inductance is adjustable using a brass core. Eddy currents induced in the core oppose the magnetic field to reduce the inductance but unfortunately the quality falls. The quality Q = 130 specified, only applies when the core is fully unscrewed and thus almost ineffective, giving the maximum inductance value. There is no mention of this in the data sheet.

This explains everything but to double

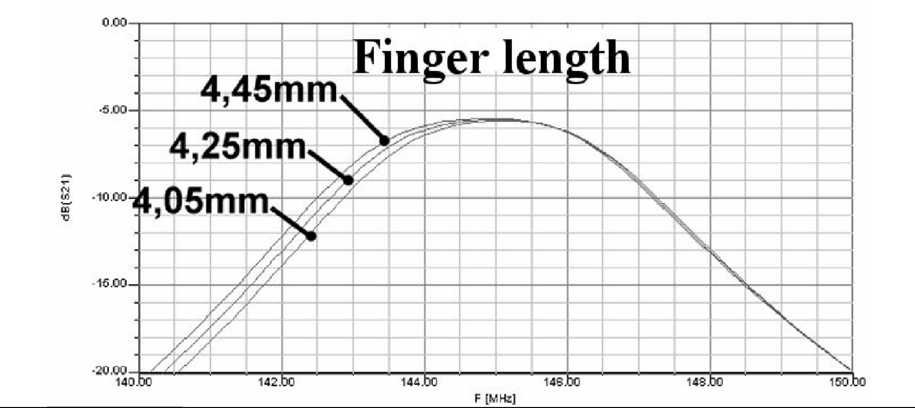



**Fig. 17: Different finger lengths and therefore different coupling capacitor values only move the centre frequency of the transmission curve but have no influence on the attenuation.**

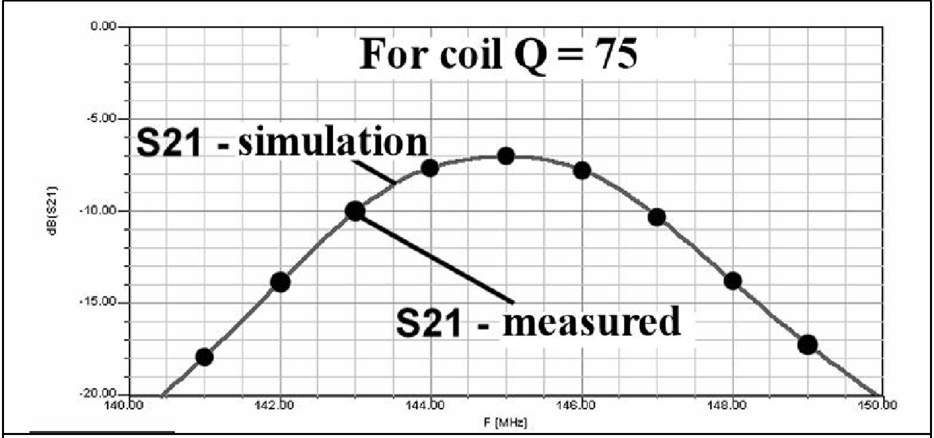



**Fig. 18: This proves the coils are the problem, the picture speaks for itself (see text).**

check a further simulation was performed. Fig 18 shows the proof because with Q = 75 the simulation follows the measured S21 curve accurately. The measurements also agreed with the wide frequency sweep shown in Fig 14.

### 3.5. Summary

Interdigital capacitors are a fascinating component; as long as the PCB process has an accuracy of 0.01mm they are a good component for problem free mass production. Only the coils were a problem, more tests would be required to find a better solution.

After the prototype was built and discrepancies noticed the simulations served as an analysis tool to determine the cause of the errors. This was all at no cost and was fun to do. The author wishes that this has inspired you to use Ansoft Designer SV for your own projects, the appendices give more information for filter design.

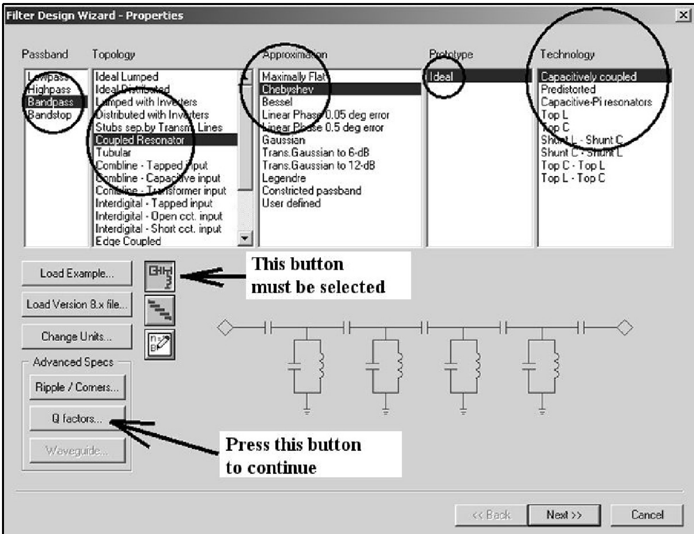



**Fig. 19: The start menu for the Filter Tools. Please set all values as shown.**

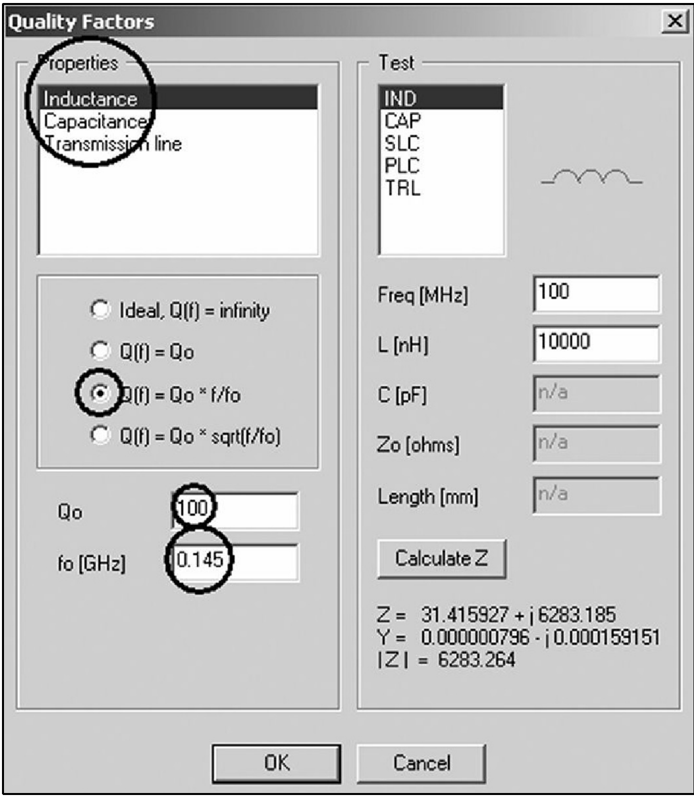



**Fig. 20: The coils need special attention (as always). The quality is set as shown.**

## 4.

## Appendix 1: Help for using the filter program in the Ansoft Designer SV

There is no need to continue searching the Internet for suitable CAD software for filter design, because Ansoft Designer SV deals with almost every filter type possible. The problem is how to find the correct selection:

To start the designer with a new file go to the “Project Open” option on the menu and click on “Insert filter Design”. Then use something like:

**Step 1 (see Fig 19):**

In the five menus (from left to right) select: “Bandpass/Coupled Resonator/Chebyshev/Ideal/Capacitively Coupled”.

Select the button for “lumped design” (button with circuit diagram). If everything is done click on “Q factors”.

**Step 2 (see Fig 20):**

The coil quality is set to Qmin = 100 at 100MHz (the filter quality rises linear with frequency). Click OK to return to the previous screen and then click “Next”.

**Step 3 (see Fig 21):**

Now for the serious entry of the filter data:

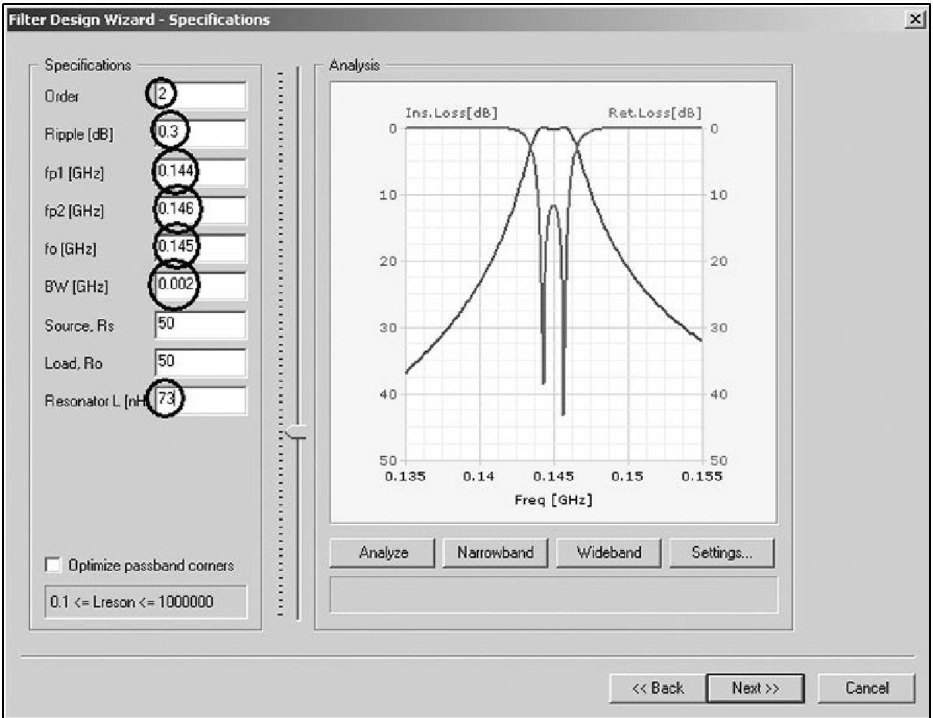



**Fig. 21: These are the settings for the filter and should be copied exactly (see text).**

| | |
|---|---|
| Order (filter degree): | 2 |
| Ripple: | 0.3dB |
| fp1 (lower cut off frequency): | 0.144GHz |
| fp2 (upper cut off frequency): | 0.146GHz |
| fo (centre frequency): | 0.145GHz |
| BW (Bandwidth) | 0.002GHz |

| | |
|---|---|
| Source, Rs (source resistance): | 50Ω |
| Load, Ro (load resistance): | 50Ω |
| Inductor L: (selected parallel inductance, all the same) | 73nH |

Press “Next” and the circuit is produced,

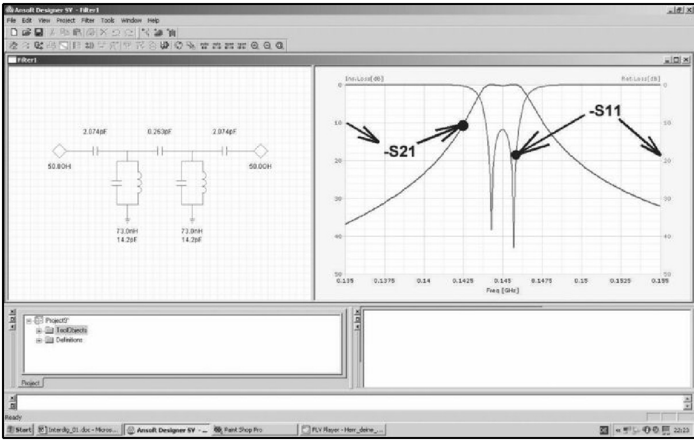



**Fig. 22: The circuit and the characteristics of the ideal filter.**

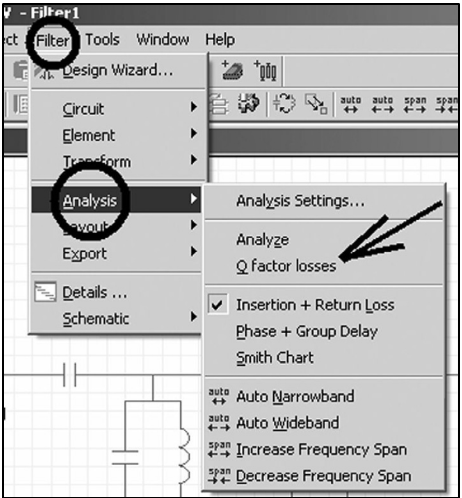



**Fig. 23: The addition of the filter quality will distort the characteristics.**

then select "Finish".

**Step 4:**

Click "Tile vertically" to produce a display of the circuit diagram and associated simulation of S11 and S22 as shown in Fig 22. The vertical axis is marked with "Insertion Loss (dB)" and "Return Loss (dB)". S11 and S22 are obtained by reversing the sign of these..

**Step 5:**

To show the effect of the coil quality Q = 100 select the view shown in Fig 23 by using the "Filter" menu from the Filter 1 window border and select "Analysis" then "Q Factor Losses". If a checkmark is set then Fig 24 shows the filter characteristics adjusted for the quality Q = 100.

Print the circuit an place it beside the PC because the next appendix needs the component values.

## 5.

## Appendix 2: Simulation of the circuit with the Ansoft Designer SV

Start a new project using the "Insert Circuit Design" option. The "Layout Technology Window" shows: MS-FR4 (Er=4.4), 0.060 inch, 0.5oz.copper,

At first place the two ports required. Initially they are interconnect ports, double clicking on their circuit symbols gives the chance to change them to Microwave Ports (Fig 25).

Now the remaining components can be found in the Project Window under the "Components/Lumped". For the capaci-

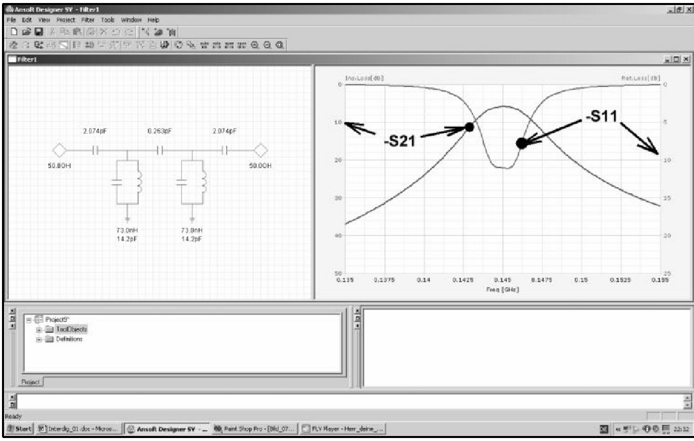



**Fig. 24: The filter circuit with a coil quality Q = 100.**

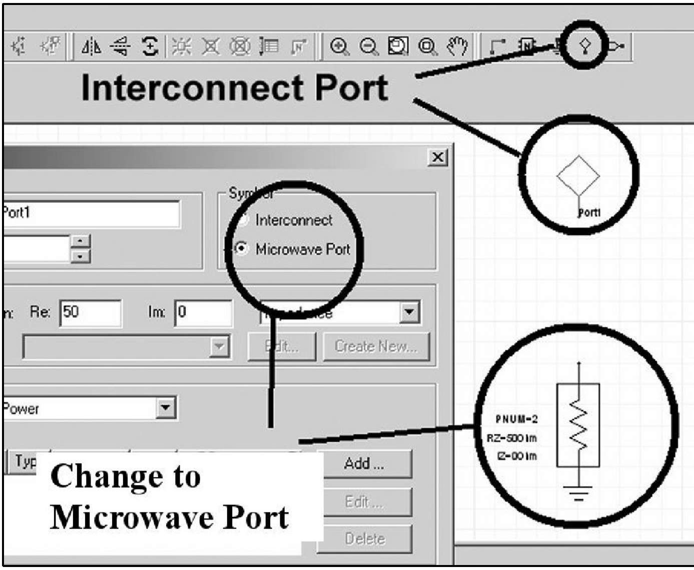



**Fig. 25: Do not forget to change the Interconnect Ports to Microwave Ports.**

tors a simple "Capacitor" is used but for the coils "INDQ" (Inductor with Q factor) should be used.

The circuit is drawn as shown in Fig 26 using "Wire" to connect the components and the component values added. Do not forget to double click on the coil symbols and set the quality to Q = 100 at 0.1GHz.

The PCB material should be changed to

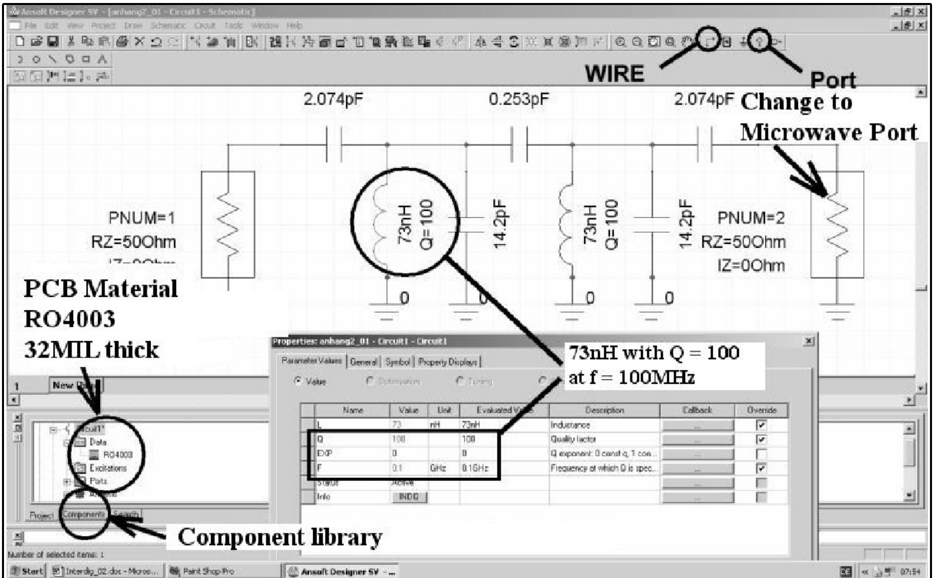



**Fig. 26: The simulation circuit shows all the correct components.**

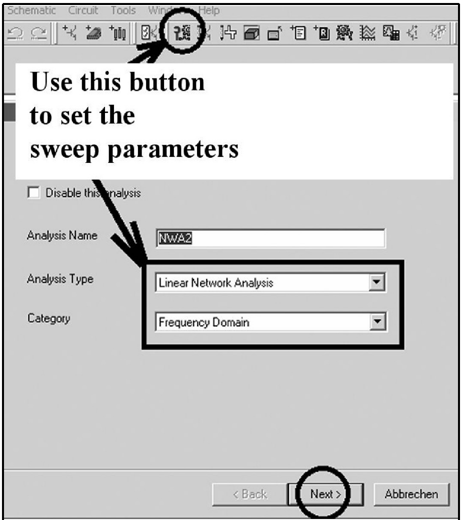



**Fig. 27: The sweep settings.**

"32MIL = 0.813mm thickness and R04003 material" as described in Fig 6.

Note: When a component is attached to the cursor it can be rotated by pressing "R". If the component is already placed it can be selected with a single mouse click and rotated by pressing "Control" and "R".

The circuit is stored under a suitable name and a sweep for 140 - 150MHz in 100kHz steps carried out as shown in Fig 27:

**Step 1:**

Click the setup button and continue with "Next".

**Step 2:**

Select "Add" on the next menu to show the sweep programming (Fig 28) and set the following:

1: Control "linear Sweep"

2: Sweep attributes (140MHz to 150MHz in 100kHz steps)

3: Press "Add"

4. Check the sweep values selected

5: Press "OK"

6. Lock the sweep programming with "Finish"

**Step 3:**

Pressing the simulate button starts the simulation but nothing is displayed until the create report button is pressed (Fig 29). Check that "Rectangular Plot" is selected; this can be changed on the pull down menu, e.g. Smith Chart representation.

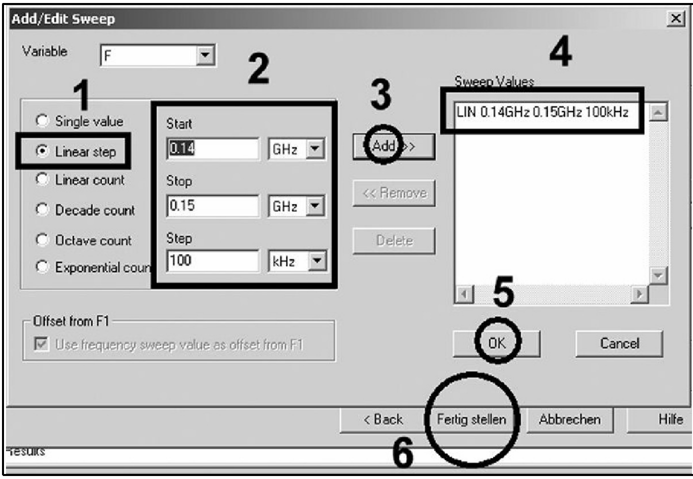



**Fig. 28: If everything is correct, the complete sweep can be programmed as this sample.**

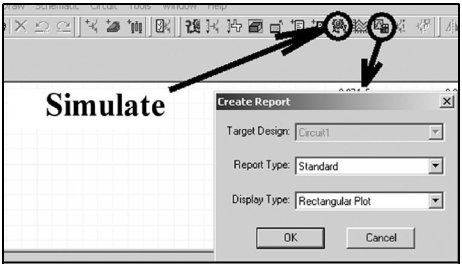



**Fig. 29: The display type can also be Smithchart. Also different forms of the representation can be selected.**

**Step 4:**

Use the "Traces" menu to add S-parameters to the list shown in Fig 30. Select S11 and then click "Add Trace". Use the same procedure to add an S21 trace and press "Done". The display shown in Fig 31 is now produced which is the same as Fig 8. Double clicking on the appropriate axis can change the axis divisions.

## 6. Literature

[1] www.elektronikschule.de/~krausg - is the main German web page and:

http://www.elektronikschule.de/~krausg/Ansoft%20Designer%20SV/English%20Tutorial%20Version/index_english.html - is the relevant English page

[2] www.ansoft.com

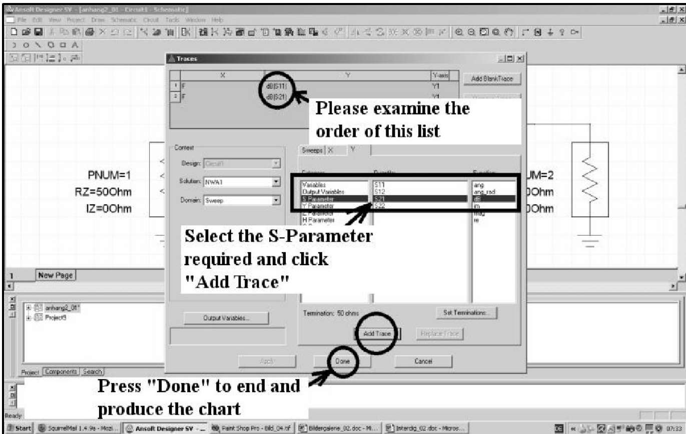



**Fig. 30: S11 and S21 are selected for presentation.**

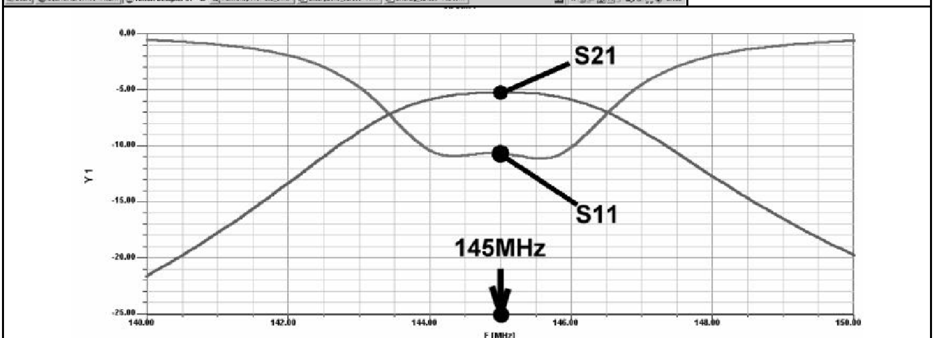



**Fig. 31: The simulation result.**

*Wolfgang Schneider, DJ8ES*

# Top loaded vertical DX antenna for 80m

**There is a lot of interest in the high frequency bands but they cannot offer the attraction of DX like the low frequency bands like 160m, 80m and 40m. One of the classic DX antennas for these bands is the vertical.**

## 1.

## Selection of an antenna suitable for DX

In the authors opinion there are only two types of antennas to be considered for the short wave bands like 80m. These are the classic dipole and the vertical. Of course there are many variants of this basic forms like dipoles e.g. the shortened form from W3DZZ. Available space and budget reduce the options that are practical.

The horizontal dipole is a wire antenna with the length related to the wavelength (40m, 80m or 160m). They are usually erected at heights of 8m to 12m above ground that is about λ/4 on 40m. On 80m or 160m this is much less than λ/4 that increases the angle of radiation.

The topic of radiation angle of wire dipoles is discussed in [1]. For DX dipoles should be at least λ/2 or more above ground. This is not practical under normal circumstances for the average radio amateur.

This only leaves the vertical antenna. This type of antenna is well suited for DX because it has a low radiation angle. But for every 1 metre of vertical wire a good earth is required and that is not so simple.

Nobody should think that a vertical antenna is space saving because a good efficient earth network requires a given surface area.

## 2.

## An earth network fundamental to the vertical antenna

A quarter wave vertical antenna must have an earth network suitable for high frequency use. This usually consists of as many radials as possible laid in a star shape. The radials are like the 2m ground plane that most people will have built at some time, they can be horizontal or bent. In this case the lengths required have to be considered in terms of their appearance and the space available plus other restrictions e.g. the XYL.

An earth network represents a reflecting

**Fig. 1: Top loaded λ/4 vertical antenna for 80m on field day for the Itzehoe club (MØ5).**

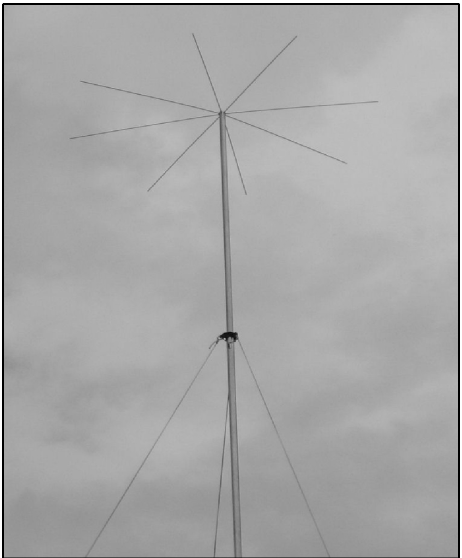


**Fig. 2: The top load made from thin aluminium rods is only visible in the close-up photograph.**

surface for the vertical antenna. To be useful it must use radials that are as long as possible. Commercial solutions use up to 250 individual radials buried under ground. They can lay on the ground and do not need to be the same length. The limiting factors are space and cost.

The requirements for an earth network are discussed in detail in [2] together with some practical solutions. My own measurements shown in Fig 9 definitely confirm these comments.

The actual antenna can consists of a vertical tubular structure, a mast, or simply a stretched wire. The antenna is isolated from earth. The length should ideally be $\lambda/4$. That corresponds to a length of approximately 10m for 7MHz, 21m for 3.6MHz or 42m for 1.8MHz.

The height of a 40m vertical is practical but it becomes more of a problem for the lower bands. There are some examples in

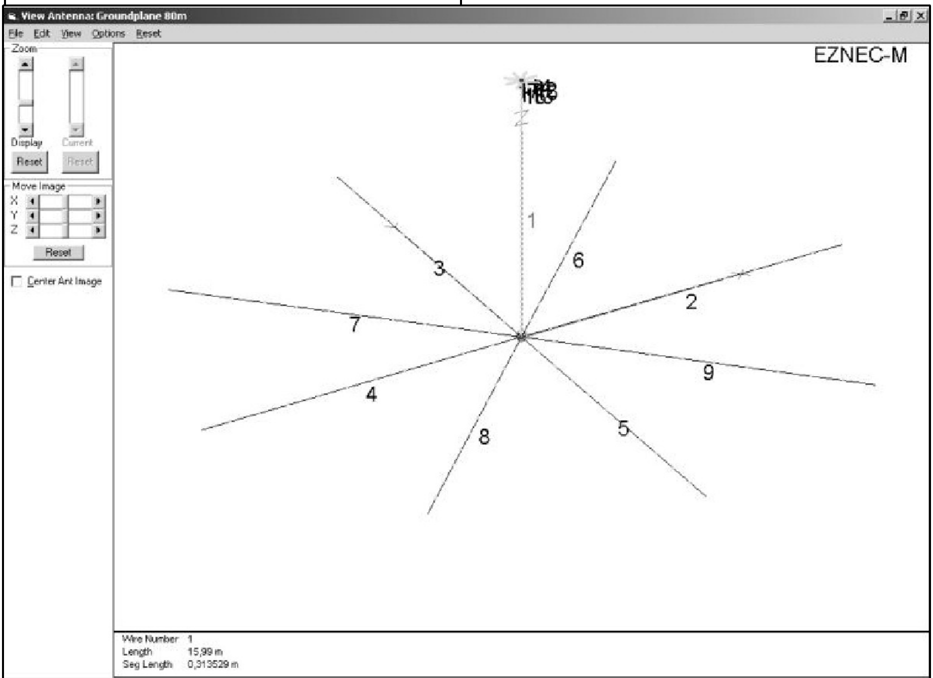



**Fig. 3: The top loaded vertical antenna simulated with EZNEC.**

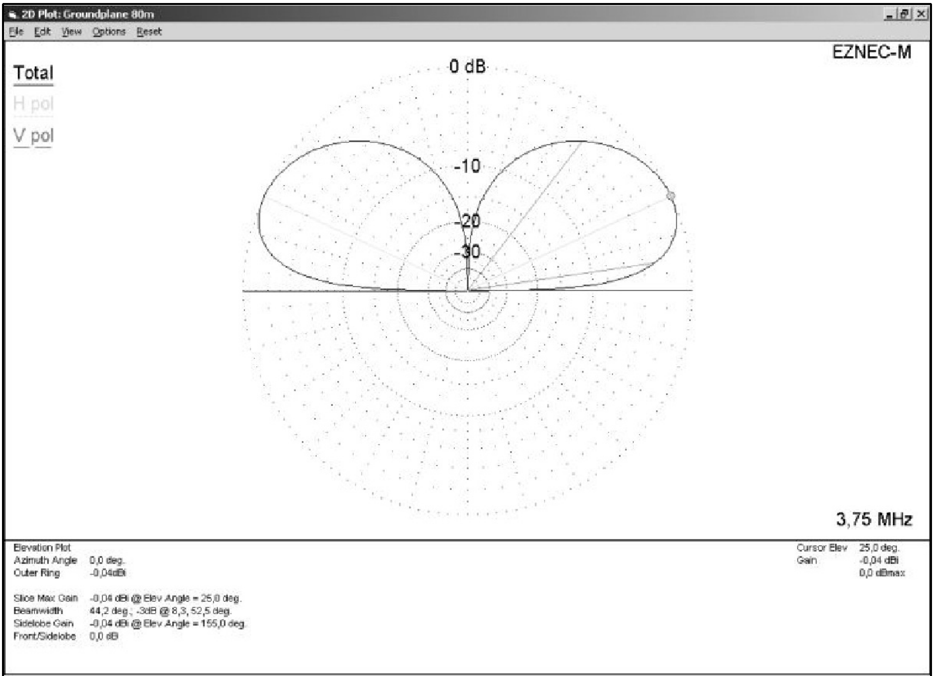



**Fig. 4: The radiation pattern shows an angle of radiation of approximately 25°, suitable for DX.**

[1] but for the normal radio amateur these remain a dream. Therefore alternatives must be considered.

Loading at the base of the antenna can electrically extend the antenna so that the mechanical length can be shorter for a given frequency band. This method introduces losses into the overall system.

Gerd Janzen, DF6SJ wrote a book on short antennas [3] dedicated to this topic and discusses the pros and cons of these antennas. He also presents different interesting alternatives. One of these alternatives is the vertical antenna with a top load. This is a shortened length antenna that is balanced with a top load. This smaller height is much simpler to realise. Of course this solution has losses compared to the ideal vertical antenna but it is very interesting because of the smaller size.

## 3. Simulation of top loaded vertical antennas

Today most electrical circuits can be simulated on a PC. Naturally this also applies to antennas. This not only saves money but also a lot of time, work and possibly frustration. Some designs do not work as planned at the first attempt.

The antenna simulation software EZNEC by Roy Lewallen, W7EL is available from [5]. After entering all parameters like the mechanical dimensions the software produces the results that can be expected from the antenna and the associated earth network (Fig 3). The radiation pattern of the vertical antenna is suitable for DX on 80m with a good angle of radiation at 25° (Fig 4). The

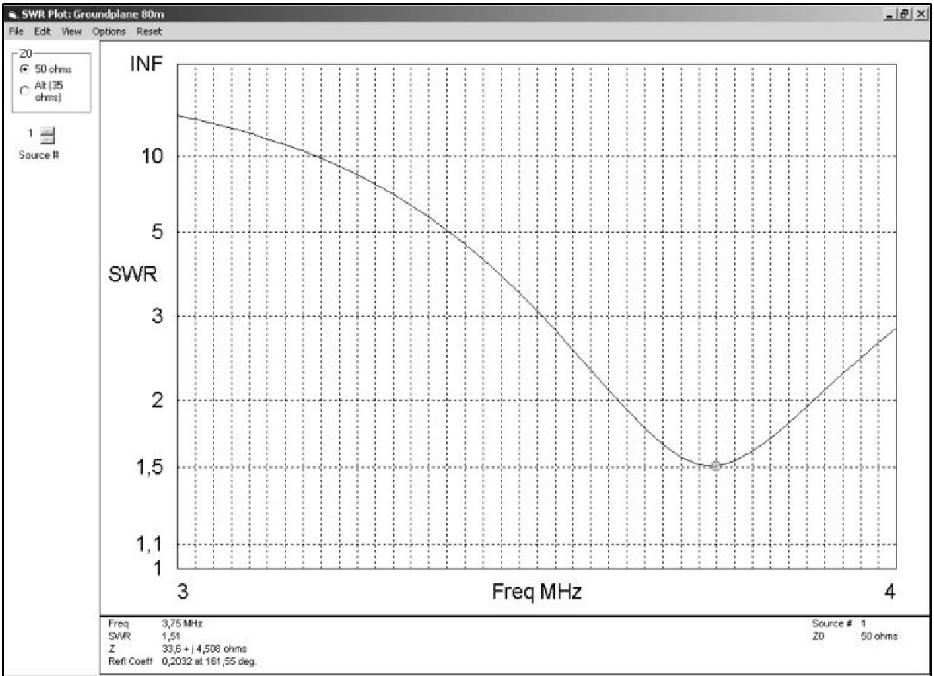



**Fig. 5: The SWR of this antenna, with ideal earth losses of 0 ohms, is approximately 1.5.**

**Fig. 6: The individual tubes are fitted into one another and secured with clips.**

horizontal pattern surrounds the antenna.

The radiation resistance of the antenna is approximately 32Ω. With an ideal earth network this would correspond to an SWR of 1.6 (Fig 5). In practice the earth losses have to be added. This lets the losses rise but the SWR approaches the ideal value of 1.

## 4.

## The mechanical construction

The vertical antenna with a top load for 80m consists of 3 aluminium tubes with diameters of 50, 45 and 40mm and the standard length 6m. The wall thickness of the tubes is 2mm. The tubes are fitted into one another and secured with a clip.

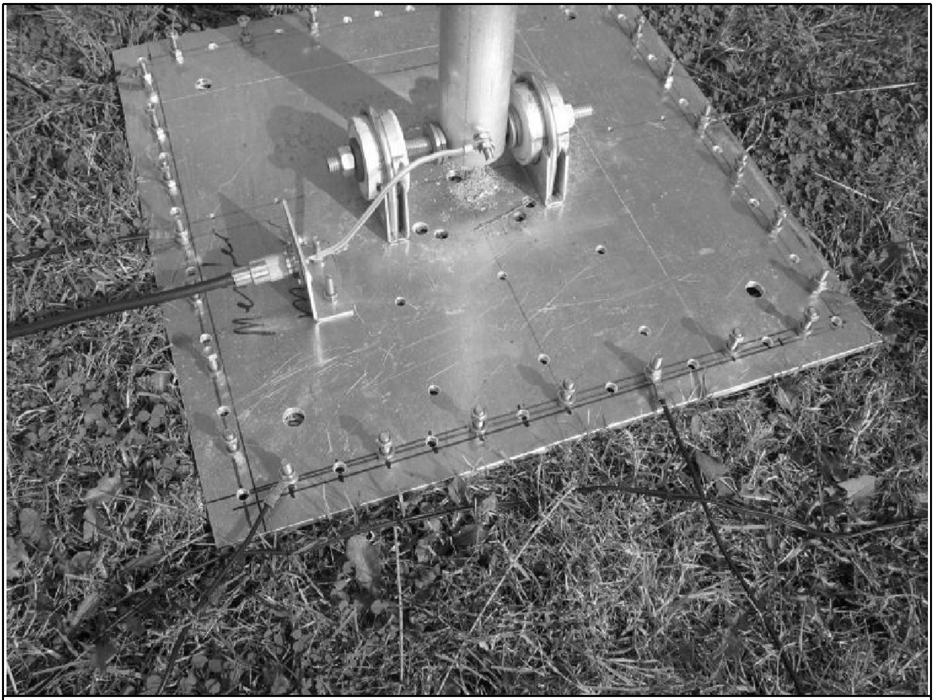


**Fig. 7: The mast base with connection for a great many radials.**

The pipes are pushed into one another and fixed with a clip. The lower and middle tubes have slits cut approximately 5cm long and the mating tube pushed in by 50cm as shown in Fig 6. This results in an overall length of 17m.

A hole is drilled in the lower tube for a tilting pin. The mast base shown in Fig 7 is an example, it is a 50cm x 50cm aluminium plate 8mm thick. The tilting joint is manufactured using two pieces of 52mm Polyimide secured by two 52mm clips with a 12mm bolt through the centre. 60 M6 x 20mm screws are fitted around the base plate for connecting the earth of 60 radial (that should be enough). This kind of mast mounting plate is ideal portable operation. When assembling such an antenna at home or elsewhere simpler alternatives can be used.

At the top of the vertical antenna the top load is made from 8 x 4mm diameter aluminium rods in a star shape. These have approximately 10mm of 4mm thread cut on the ends to secure them to the antenna as shown in Fig 8. Each rod is 1m long.

## 5.

## Operational experiences

The quality of the earth network is of critical importance for the efficiency of a vertical antenna. At least 120 radials with a length of 0.4λ would be ideal. But who has this much space in their garden? This is different when the antenna is used for portable operation e.g. for annual field day where the location is better.

The loss in the earth network is depend-

**Fig. 8: The assembly of the individual aluminium rods at the end of the tube for the top load.**

ent on the number of radials; this becomes clear in Fig 9. The measured values naturally depend on the local soil conditions. No generally advice can be given, however for an acceptable efficiency of the antenna at least 16 radials are necessary. The publication by Zander [2] deals with the size of an earth

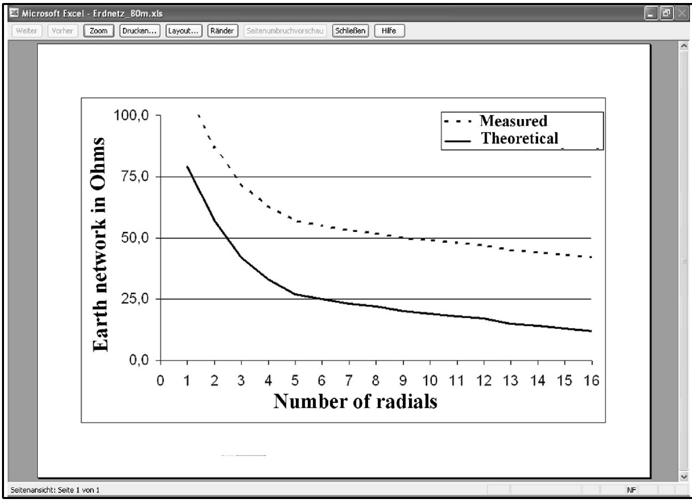



**Fig. 9: The losses in the earth network dependent on the number of radials (over 20m long).**

network.

Measurements of the top loaded antenna for 80m at different locations underline the impressive quality of this antenna. Depending on the earth network used, efficiencies between 70 and 85% are easily achieved. This corresponds to losses of only 1.5dB compared to the ideal quarter wave antenna.

In practice the above data was supported by the more than successful participation in various contests (e.g. cqww dxssb). The results speak for themselves.

## 6. References

[1] John Devoldere, ON4UN: Low Band DXing, Fourth edition, ARRL 2005

[2] Horst Zander, DJ2EV: RF earth for small vertical antennas, Funkamateur 7/98, P. 848

[3] Professor Dr.-Ing. Gerd Janzen, DF6SJ: Short antennas, Franckh´ publishing house, W. Keller & Co, Stuttgart, 1986

[4] Wolfgang Schneider, DJ8ES: The entrance on Low Bands - the experiences of a KW newcomer, Funkamateur, 10/06, P. 1169

[5] Roy Lewallen, W7EL: EZNEC Antenna Software, www.eznec.com

*Henning C. Weddig, DK5LV*

# DDS using the AD9951

**Circuit technology is progressing with new ranges of Integrated circuits. The AD9951 DDS has a far superior 14 bit digital to analogue converters than earlier direct digital synthesisers (DDS) like the AD9850 and AD9851 this is because it has a clock frequency up to 400MHz. This article describes a complete circuit using modern components.**

## 1. Introduction

Inspired by different publications and various digital frequency synthesis techniques [5-9] I decided to attempt my own design. After a thorough study of the data sheet [10] the actual work began on this modern direct digital synthesiser. The first prototype that was developed with an external clock showed the performance that could be achieved. This approached the data sheet values, so could this be improved with circuit changes?

## 2. Circuit description

The circuit of this Direct Digital Synthesiser (DDS) project consists of four modules.

The block diagram is shown in Fig 1 the modules are:

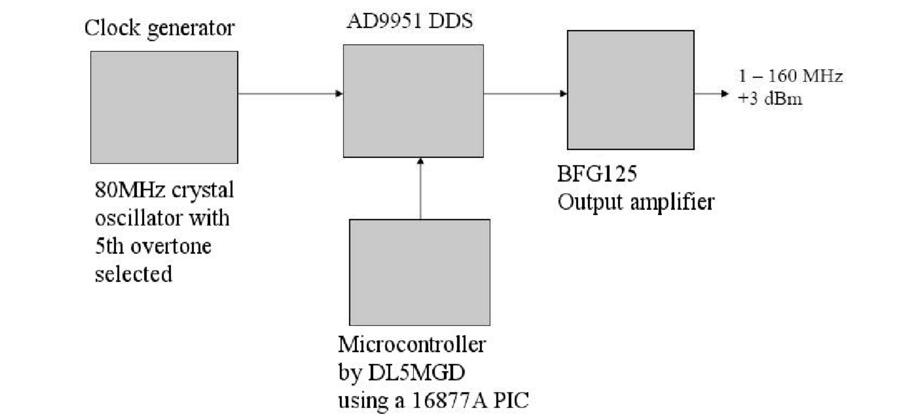



**Fig. 1: Block diagram of the Direct Digital Synthesiser (DDS).**

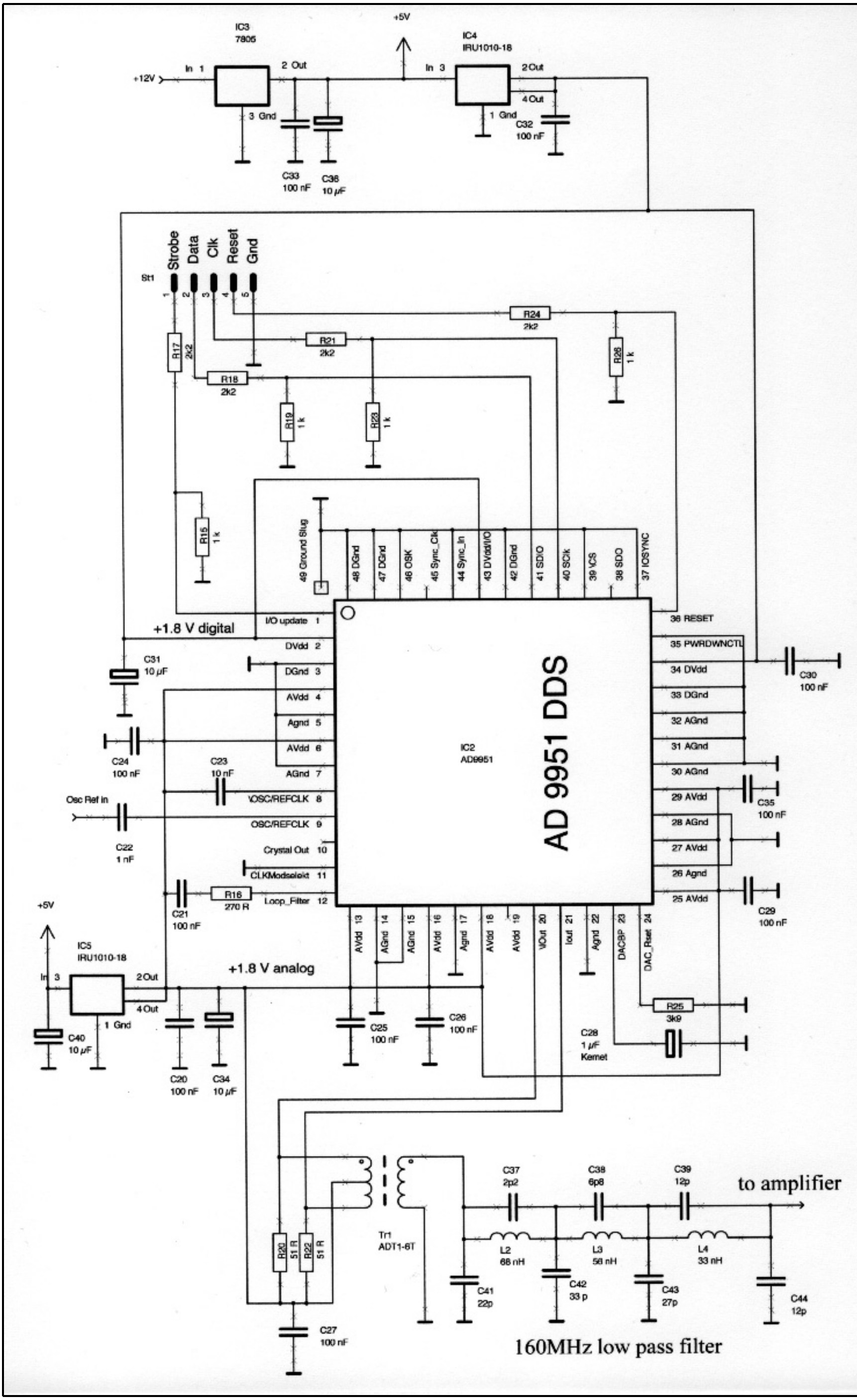



**Fig. 2: Circuit diagram of the Direct Digital Synthesiser (DDS).**

- DDS
- 400MHz clock pulse generator
- Microcontroller to control the DDS
- Output amplifier

## 2.1. DDS

The circuit diagram of the DDS module is shown in Fig 2.

The heart of the DDS printed circuit board is the AD9951 DDS integrated circuit from Analog Devices. It is a chip in a rectangular package (Thin Quad Flat Pack - TQFP/EP) with 48 legs on a 0.5mm pitch and a relatively large soldering surface (thermal pad) under the IC to dissipated the heat generated. Commercially manufactured double sided and plated through printed circuit boards were used for the prototype because the tracks are only 0.2mm wide. The soldering area for the thermal pad is connected to the earth surface by plated through holes.

### 2.1.1. Voltage supply

The supply voltages of 1.8V for the digital and analogue part of the DDS IC are produced using two IRU 1010-18 linear voltage regulators fed from the stabilised 5V supply as shown in [5]. The data sheet [13] shows that these can give a regulated supply with a maximum current of 1A and a maximum input voltage of 7V. According to the data sheet the operating power used by the DDS is typically 161mW, i.e. a current 89mA. Taking the quiescent current of the two linear regulators into account using a 5V supply [12] gives:

445mW - 161mW = 284mW.

Switched mode controllers, as suggested in [4], would improve the power dissipation performance and that may be meaningful for QRP equipment but it can produce unwanted spurious products.

The inputs for programming the internal DDS registers are designed for input voltages of 3.3V maximum, if pin 43 of the chip (DVDD_IO) is supplied with 3.3V. Because the microcontroller has a supply of 5V a third voltage regulator (5V to 3.3V) could be used for DVDD_IO or the high level from the microcontroller can be reduced using voltage dividers. Therefore DVDD_IO is connected to the 1.8V voltage regulator for the digital section. The digital signals; Clock, Data, Strobe and Reset from the external microcontroller, operated with 5V, are connected to the DDS data inputs by 2.2k/1k resistive voltage dividers.

### 2.1.2. Output connection

The Digital to Analogue Converter (DAC) outputs of the DDS are complimentary current outputs. An external resistor connected between the Rset pin (24) and ground controls the full-scale current. The value of the resistor is calculated as follows:

Rset = 39.19/Iout [Rset in kΩ, Iout in mA].

The best spurious free dynamic range is achieved with a maximum current of 10mA, which means a resistor of 3.9kΩ. From the data sheet the operating range of the DAC outputs is from the analogue supply voltage (AVDD) - 0.5V to AVDD + 0.5V. For a supply voltage of 1.8 V this gives the limits 1.3V to 2.3V, the maximum voltage swing is therefore 1Vpp = 0.35Veff. The two DAC outputs are current sources capable of supplying 1 to 10mA.

With these conditions the voltage developed across the load resistance can be between 1.8V and 1.3V relative to AVDD because the voltage rises by 0.5Vpp. Under these conditions a 50Ω load resistance can be used. Voltages outside of this range can cause substantial damage and can permanently damage the DAC.

The DAC signals should be coupled using a centre-tapped transformer feeding the load resistance as described in [10]. The resistance value is selected in such a way that the limiting values indicated

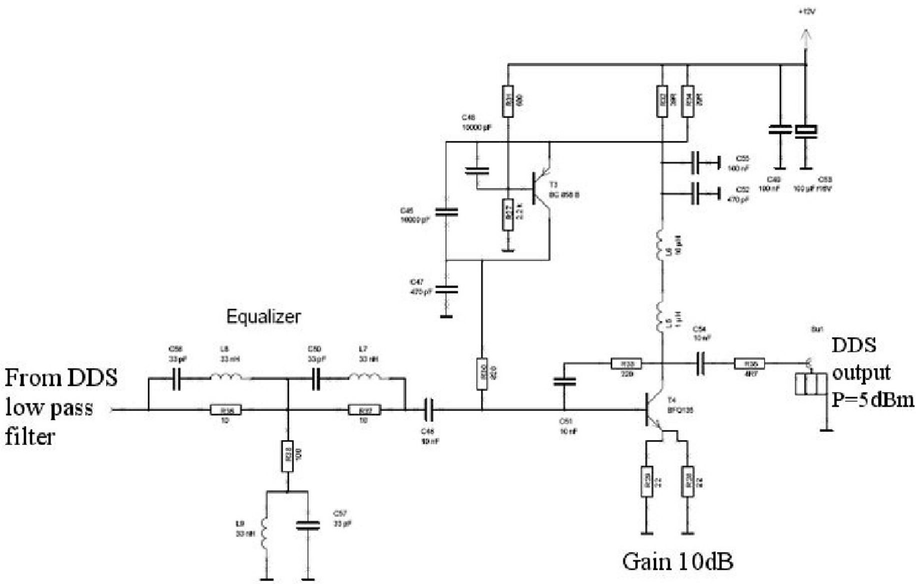



**Fig. 3: Circuit diagram of the output amplifier for the Direct Digital Synthesiser.**

above are not exceeded. The centre tap is connected to AVDD so that the DAC see a load resistance of 25Ω with a 50Ω load on the transformer. This method of connecting the DAC output has the following advantages according to [10]:

- Disturbances on supply voltage AVDD such as remnants of the clock pulse and other unwanted signals are effectively suppressed with a high symmetry transformer [10, page 48].
- The output voltage is doubled compared to using one DAC output.
- Reflections from a low pass filter following the DDS are effectively suppressed [10, page 47]

It is amazing that no transformers are used in the many circuits published for the well known AD9850 DDS. A fast operational amplifier, connected as a sum and difference amplifier, is shown in the circuit given in [3]. I0CG uses an unknown type of transformer from Minicircuit in [7, 8].

For the first attempts an ADT1-6 transformer was used, it is readily available and is suitable for a range from 10 kHz to only 125 MHz. In order to use the upper frequency range of the DDS the better transformer type T1-1T (80kHz to 200MHz) should be used. Both transformers are 1 : 1 but the T1-1T has a different housing. The voltage at the output of the transformer is twice the voltage across one half of the primary coils; this can be easily proved by measurement with an oscilloscope.

The latest implementation by Martein

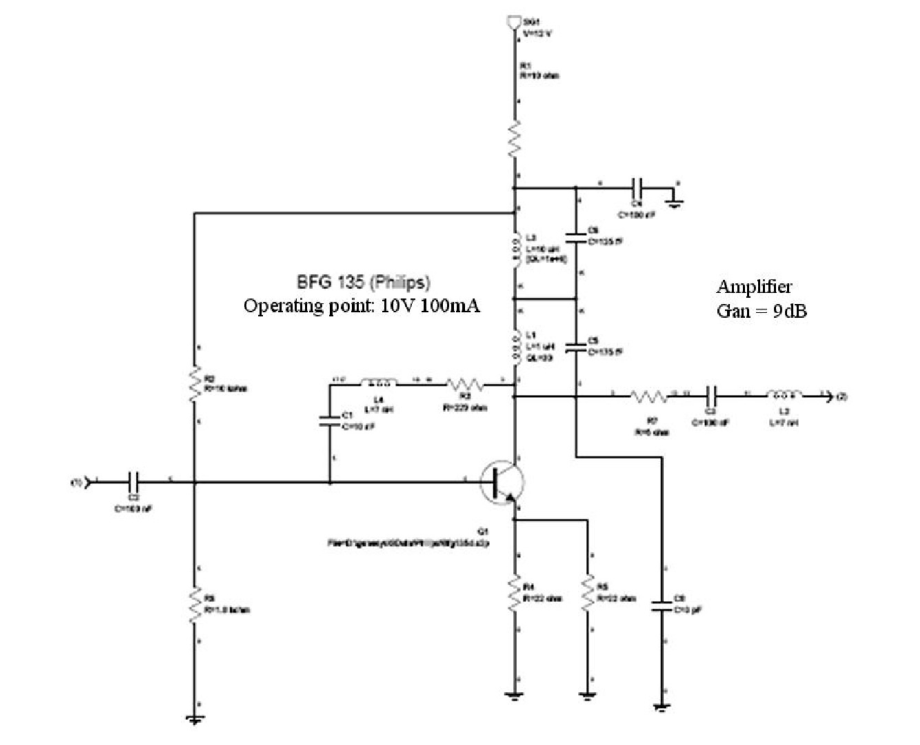



**Fig. 4: The simulation circuit of the output amplifier developed for use with Genesys.**

Bakker, PA3AKE [16] uses a capacitor (C28) on the DAC baseline-decoupling pin (DACBP pin 23) of the DDS. It filters the amplitude noise produced by the internal Band Gap reference that would otherwise modulate the DAC output. This pin is no longer present on new DDS components e.g. AD9912.

### 2.1.3. Low-pass

The seven pole elliptical low pass filter circuit and component values were taken from the Analog Devices evaluation board [12].

### 2.1.4. Output amplifier

The DDS supplies an output level of approximately -6dBm that is sufficient for many applications. Nevertheless a higher output level is desirable. Therefore an output stage was designed with the circuit diagram shown in Fig 3.

To maintain the harmonic suppression of approximately 60dB obtained from the DDS a linear amplifier was needed. Experience with MMIC amplifiers like the ERA 3 showed that these would not give sufficient harmonic performance. A test with a BFR96 amplifier had undesirable results; it suffered from wild oscillation in the UHF range and damaged the transistor.

A broadband amplifier using a BFG135 with negative feedback was developed and designed for stable gain of 10dB. With a current of 80mA it achieved the required 60dB harmonic suppression. The negative feedback circuit was designed with the commercial program "Genesys" version 8.1 (an Eagle product,

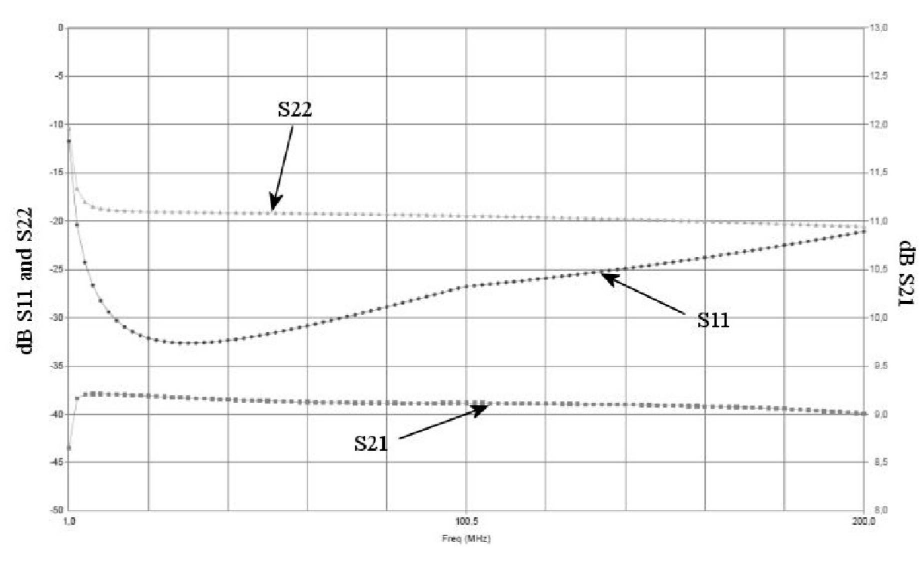



**Fig. 5: The simulation result showing the S-parameters S11, S22 and S21 for the output amplifier in the frequency range from 1 to 300MHz.**

now Agilent) with the simulation circuit shown in Fig 4. No DC voltage operating points can be examined with the basic version of the program that the author used so no operating point stabilisation was included in the simulation.

My first idea was to use a frequency varying negative feedback in order to compensate for the gain loss of the DDS output. This was done using a 100nH inductor in series with the feedback resistor and capacitor from the collector to base and a capacitor from emitter to ground. This circuitry seemed to work for the simulated frequency range of up to 200MHz. As the BFG135 has an ft of 6GHz the simulation frequency range must be extended in order to see if the circuitry is unconditionally stable (stability factor k > 1) even at higher frequencies. By doing so the simulation showed that for frequencies above 500MHz k is < 1. Therefore this compensation scheme is not feasible. By inspection of the test circuitry in the data sheet of the BFG135 [17] the feedback circuitry was changed (L2 set to 22nH, the cap from emitter to ground omitted and a small (10Ω) series resistor from the collector to the output included, see Fig 4. This gives a stable gain and stability factor over the frequency range up to 1GHz, see Fig 5.

In order to compensate for the sinc function, a bridged T-filter was designed. This filter is put between the lowpass filter of the DDS output and the input of the output amplifier. This circuitry gives a constant input and output impedance (like a diplexer at the output of a mixer). The attenuation is 4dB at low frequencies but as the attenuator is bridged at about 160MHz there is nearly no attenuation at higher frequencies. See Fig 6 that shows the frequency response of cascaded bridged T-filter and output amplifier. This circuitry is not implemented in the author's test PCB but is included in the updated PCB shown in this article.

The simulation up to 1GHz is shown in Fig 6. The gain above 500MHz drops so that no self-oscillation is expected.

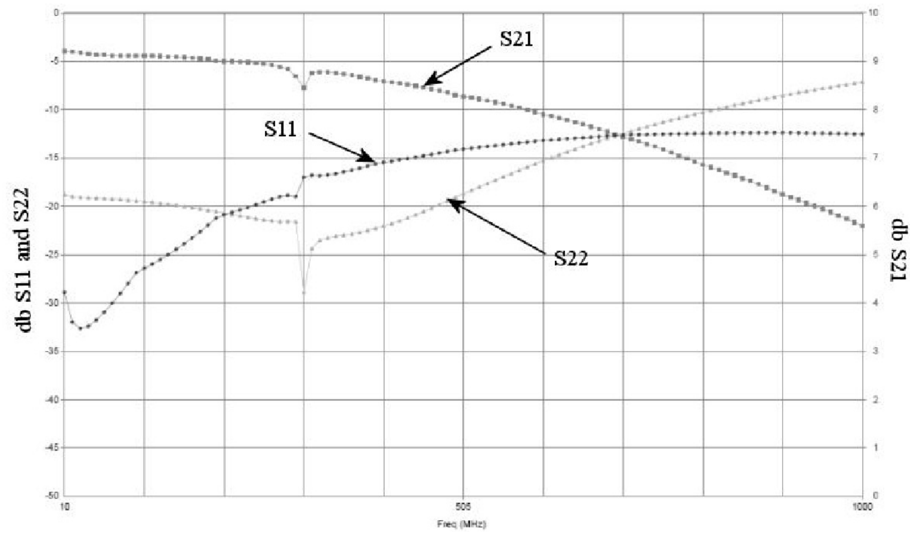



**Fig. 6: The simulation result showing the S-parameters S11, S22 and S21 for the output amplifier up to 1GHz.**

### 2.2. Clock production

The circuit diagram of the 80MHz crystal oscillator module is shown in Fig 7. Experiments with an external 20MHz clock and internal multiplication as shown in the data sheet [11] show that the best phase noise is obtained using an external 400MHz clock. The clock is generated from an 80MHz crystal oscillator with a TTL compatible output (Pout = +17dBm for the fundamental frequency). The fifth harmonic is selected using a two-pole helical filter. The filter is fed via a coupling capacitor because the TTL oscillator output has a DC offset. The prototype gave a measured output of –6dBm at 400MHz see Fig 8. Any frequency offset can be compensated using the software in the microcontroller [5].

When selecting harmonics of an oscillator the phase noise increases by 20 log N, where N is the harmonic number selected. Selecting the fifth harmonic increases the phase noise by 20 log 5 = 14dB for a fourth harmonic this would be 12dB. Attempts to select the fourth harmonic from a 100MHz square wave oscillator feeding a diode multiplier [14] failed. The fundamental could be filtered to give a sine wave to feed the diode multiplier [14] and the fourth harmonic selected using a low pass filter but the additional cost cannot be justified.

Fig 9 shows the measured phase noise of the crystal oscillator on the fundamental (80MHz) and fifth harmonic (400MHz). The degradation in phase noise was expected to be 14dB but was 20dB at 100kHz from the carrier. Since these measurements were taken at different times and with different power supply smoothing the results are difficult to evaluate.

The phase noise of a 100MHz crystal oscillator was also measured and it was worse than the 80MHz oscillator at the fundamental frequency therefore because of the higher price of this oscillator the 80MHz oscillator is more favourable. The good phase noise of the cheap crystal oscillator was a surprise.

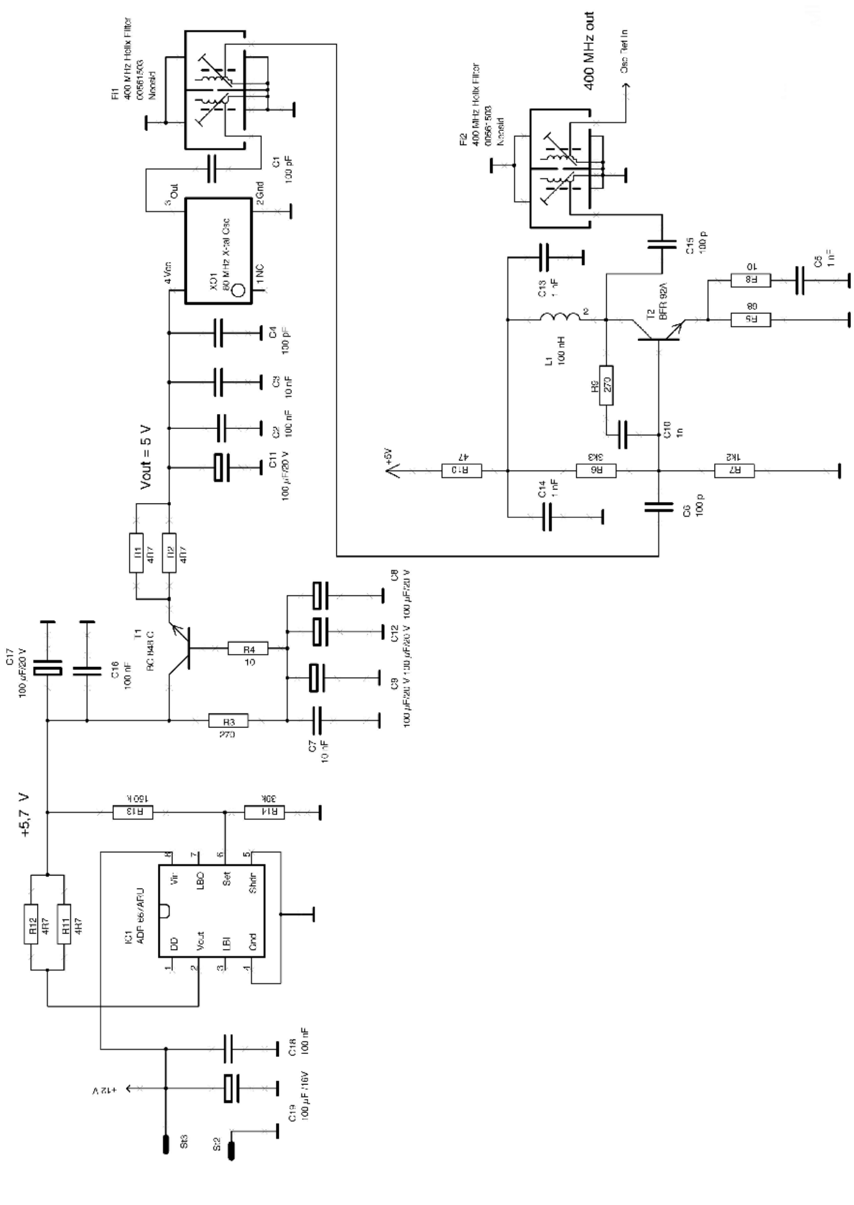



**Fig. 7: Circuit diagram of the 80MHz crystal oscillator modulator.**

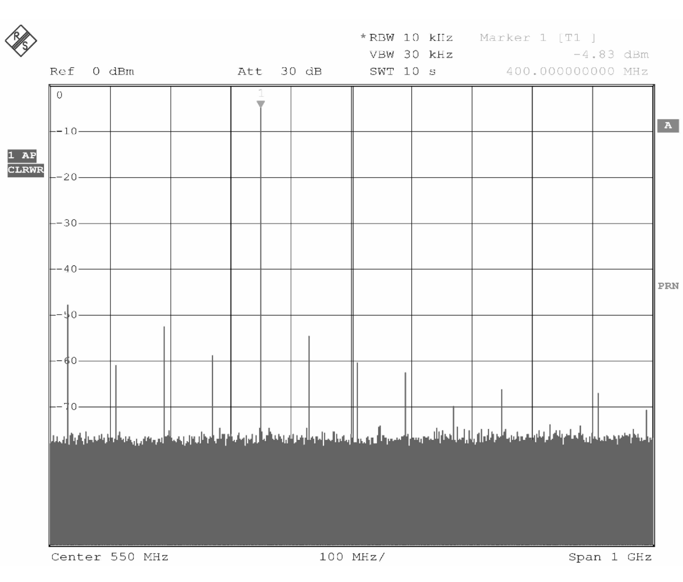



**Fig. 8: Output spectrum of the 80MHz crystal oscillator after a 400MHz two-pole Helix filters.**

However it must be mentioned that the phase noise of the oscillator is sensitive to noisy supply voltages. Therefore the supply voltage for the oscillator uses a low-noise low drop out voltage regulator and a filter. The filter consists of an NPN transistor emitter follower with high value electrolytic capacitors connected from its base to earth. The effective value of these electrolytic capacitors is increased by the current amplification factor of the transistor. With a current amplification factor of 100 the emitter capacitance is 100 x 300µF = 0.3mF. With this high capacitance value any noise voltages are effectively suppressed.

A capcitively loaded emitter follower can oscillate; this can be reduced with the 10Ω resistor in the base circuit. A resistor in the emitter circuit reduces the starting current flowing into the electrolytic capacitors. The current drawn by the crystal oscillator in the prototype was 60mA so two 4.7Ω of resistors (R1, R2) in parallel

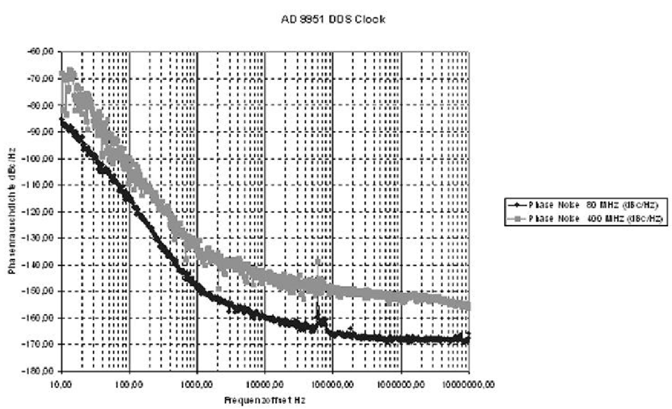



**Fig 9: Measured phase noise of the crystal oscillator on the fundamental (80MHz) and fifth harmonic (400MHz).**

**Table 1: Modifications to the source code that can be downloaded from [5].**

```
RESET:
    Bsf reset                ; Reset the AD9951, (high signal) so that all registers are in
                             ; a defined condition
    call wait_1ms            ; Reset goes "high" and remains there for the 1ms specified
                             ; by the subroutine
    bcf reset                ; Reset back to "low"
; ------Initialisation of the AD9951----------
    Init                            ; register cfr2 of the AD9951
    movlw    b `00000001`           ; address cfr2 in write mode
    movwf    daten                  ; call ser_aus
    movlw    b `00000000`           ; highest byte of the cfr2 (not used in the AD9951)
    movwf    daten
    call     ser_aus
    movlw    b `00000000`           ; second highest byte of the cfr2
    movwf    daten
    call     ser_aus
    movlw    b `00000110`           ; lowest byte of the cfr2 clock = 400MHz,
                                    ; internal multiplier switched off
    movwf    daten
    call     ser_aus
    bsf      strobe
    bcf      strobe
    return
; --- End initialisation of the AD9951-----
```

were used to minimise the voltage drop.

The frequency stability with temperature and ageing of the cheap crystal oscillator has not been investigated.

The oscillator signal can be fed to the DDS either symmetrically using a Balun or asymmetrical [11]. The oscillator inputs are internally connected to 1.35V therefore a coupling capacitor is required. When asymmetrical feed is used, pin 8 must be decoupled to AVDD with a 0.1µF capacitor. The oscillator output, Crystal Out, pin 10 can be switched off by setting an internal register (CFS2>9> = high). The data sheet for the DDS does not specify the Balun that can be used for symmetrically feeding the clock. The input level of the externally clock can be between +3dBm (890mVpp) and -15dBm (112mVpp) A high level is said to improve the phase noised but this is not quantified. For the maximum of the clock level the voltage is 1.35V + (0.89V)/2 = 1.795Vs. Because the harmonic suppression was not sufficient at 400MHz a buffer amplifier with another two-pole helical filter was developed.

## 2.3. Microcontroller

The microcontroller developed by Andreas Stefan, DL5MGD [5] was used to control the DDS. The firmware was modified for the current circuit; the modifications to the source code that can be downloaded from [5] are shown in Table 1. The second bit in the second highest byte of CFR2 is set high (b `00000010 `) making the Crystal Out, pin 10, inactive possibly giving better harmonic performance.

The first attempt to make this circuit on strip board failed so a ready-made PCB

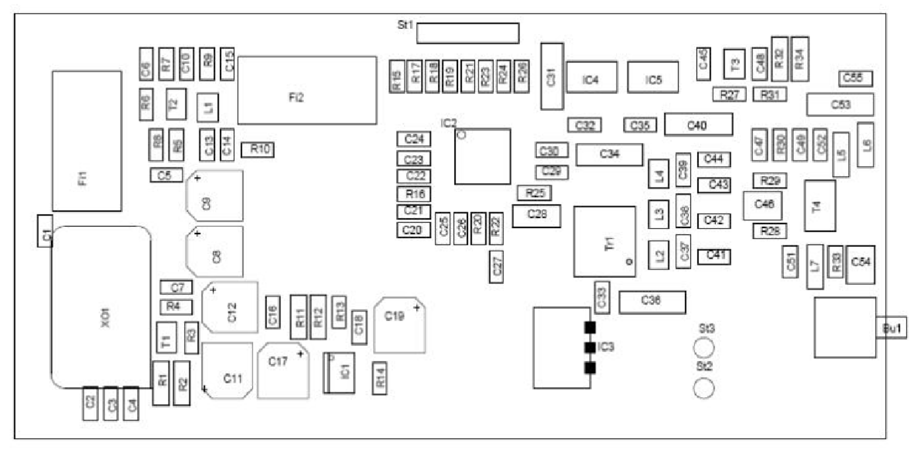


**Fig 10: Component layout of the DDS PCB.**

was purchased from Andreas and it worked first time. The circuit diagram of the microcontroller, operating instruction in English and the tiff files to make the single sided PCB is available from Andreas web site [5].

## 3. Construction

The component layout of the DDS PCB is shown in Fig 10, it is 55mm x 111mm and fits ito a standard tinplate enclosure. Fig 11 shows the SMD component side of the PCB and Fig 12 shows the lower side of the PCB. The prototype PCB was commercially manufactured and is shown in the photo Fig 13. The crystal oscillator can be seen at the bottom left followed by the noise suppression circuit needed for the oscillator. The two-pole helical filter is above the oscillator followed by the buffer amplifier and the second helical filter.

The square black block is the DDS with the broadband transformer below and then the low pass filter with coupling capacitor to the output stage. The PCB was designed for 1812 size SMD components.

The most difficult part when assembling the PCB is soldering the DDS IC. It is not only the 48 fine spaced legs that have

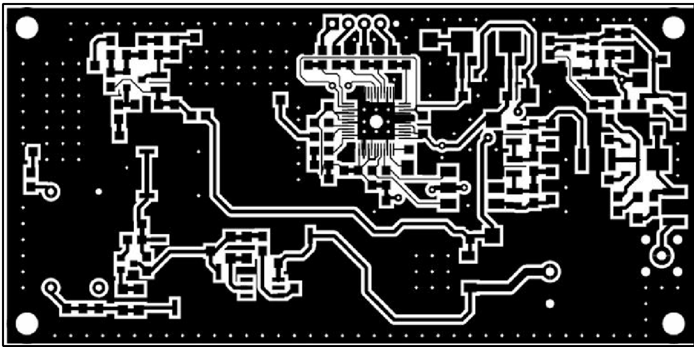


**Fig 11: SMD componet side layout of the DDS PCB.**

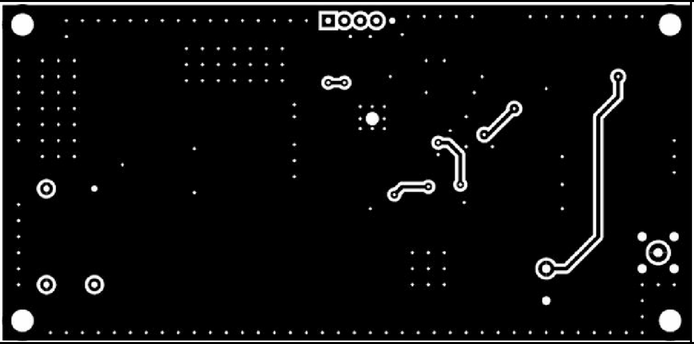


**Fig 12: Lower side layout of the DDS PCB.**

to be soldered but also the earth pad under the IC. Some amateurs drill an additional 3mm hole in the PCB under the IC so that it can be filled up with solder. The author uses the following procedure:

Coat the Pads of the printed circuit board with SMD paste, clamp the PCB on a table or in a vice, place the IC and align the legs to the pads of the PCB, heat the printed circuit board up from underneath with a hot-air blower until the tin solder contained in the paste melts. After the PCB has cooled surplus solder that bridges connections can be removed using de-soldering braid. Controlling this procedure is made much easier with a magnifying glass. Following this, fitting the remaining SMD components is child's play.

## 4. Measurements

The output spectrum and phase noise was measured up to 160MHz in the authors workshop starting from 10MHz, the lowest frequency usable on the E5052 analysers from Agilent.

### 4.1. Spectrum measurements

15 output spectrum plots of the DDS in 10MHz steps from 11 - 151MHz and

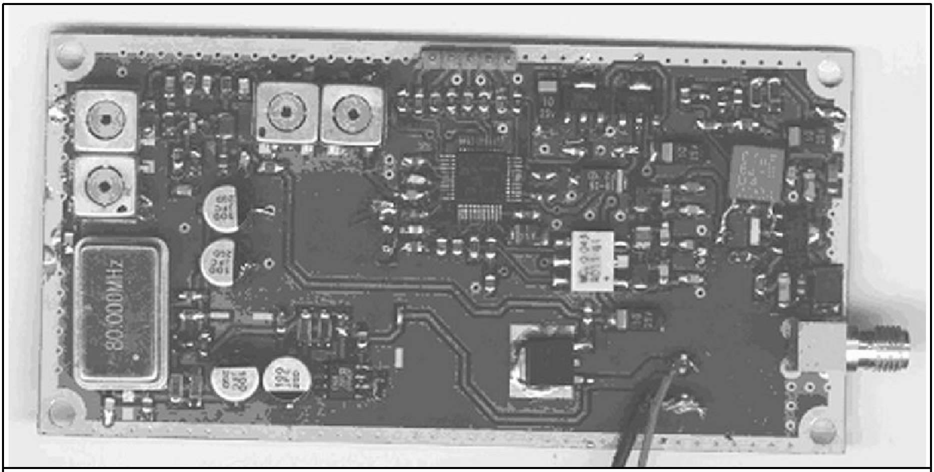


**Fig 12: Photograph of the prototype DDS PCB.**

159MHz were made, too many to print in this magazine, they are available on the magazine web site. The spurious level is a problem it is only suppressed by 42dBc up to 100MHz (¼ the clock frequency). The harmonics of the desired signal are suppressed by at least 60dB.

Despite low pass filters, leakage of the alias frequency can be seen when changing the frequency produced by the DDS. The alias frequency is about 100MHz away from the desired frequency. At an output frequency around 50MHz the signal and the alias frequency coincide. If the DDS is used as local oscillator for a short wave receiver with a high side intermediate frequency of 45MHz a birdie will appear on received signals of 5MHz that cannot be removed.

According to data sheet the spurious level should be suppressed by better than 70dBc. The reason for problem was examined; the transformer on the output of the DDS did not seem to be balanced as shown when it was replaced. The difference in the phase noise on the fundamental of the crystal oscillator and the fifth harmonic is 14dB and corresponds to the theory.

In a discussion at the end of the lecture given by the author during the UKW conference at Bensheim 2007 [15], a listener reported that he had noticed the spurious level problem when developing a commercial product. The reasons were insufficient decoupling and insufficient bonding of the thermal pad. Better soldering of the thermal pad gives better spurious levels because the DAC in the DDS chip is bonded to the thermal pad. Attempts by the author with 100nF and 1nF decoupling capacitors on the supply line made no difference. More control by the author when soldering the thermal pad is not possible. Therefore the middle plated through hole under the thermal pad PCB should be 2mm diameter. After soldering the legs of the DDS this large hole can be filled with solder to ensure a good earth connection.

### 4.2. Phase noise measurements

15 phase noise plots of the DDS in 10MHz steps from 11 - 151MHz and 159MHz were made, too many to print in this magazine, they are available on the magazine web site.

At low output frequencies (e.g. 11MHz) the DDS phase noise is approximately 20dB lower than those of the 400MHz clock. At first sight this result is amazing because the DDS can be regarded like a frequency divider to explain the phase noise improvement. The relationship of 400MHz to 11MHz the improvement should be 20 log (400/11) = 31.2dB however only approximately 20dB was measured. The difference is caused because the frequency divider is not noise free. At an output frequency of 131MHz the phase noise curve is not good. The phase noise curve also flattens out for higher carrier frequencies.

This means that the DDS is not suitable as a local oscillator for a large signal 2m receiver because the phase noise is too high even at some distance from the carrier. Because the DDS has better phase noise close to the carrier than a VCO, the combination of a DDS and a VCO may be considered. This is being investigated.

## 5.

## Conclusion

Since at the end of 2007 more DDS ICs in the same family with higher clock frequencies (1GHz) have become available from Analog Devices e.g. AD9910, AD9912. Signals up to 400MHz can be generated that can be used as an oscillator in 2m a transceiver. First publications appeared in Funkamateur Magazine also I0CG and WB6DHW have worked on a version. Because of the word length of the control data programming with an 8 bit controller is not easy.

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*John Fielding, ZS5JF*

# John's Mechanical Gem No. 6 Tapping holes in metal

**Many amateur constructors have the need to generate threaded holes for fastening an item. This requires the use of taps and the correct size pilot hole drill bit. We will focus on the iso-metric range of thread, as these are the most common in use today.**

## 1. Finding the correct hole for tapping.

Fortunately the metric series of threads has a logical way of specifying the thread pitch and the tapping drill size. For example, a M3 standard thread has a pitch of 0.5mm. Whereas we can look up in a table or mechanical engineering handbook for the correct tapping drill size there is a quicker method.

The exact tapping drill size is defined as the thread diameter minus the pitch, so for the M3 x 0.5mm tap we require a 2.5mm drill. This will give approximately 90% thread engagement, but it has been noted that as little as 60% thread engagement only decreases the tensile strength to about 80%. As the possibility of breaking small taps when tapping into some materials is a concern then we can slightly increase the tapping drill size to make the task less demanding.

Drill bits normally increment in 0.025mm steps for the smaller sizes but these are normally hard to obtain and expensive. The drill sets one purchases at the local hardware store normally increment in 0.5mm steps (1.5mm, 2.0mm, 2.5mm etc) but 0.1mm or 0.05mm steps are normally available at good tool merchants. For soft materials like aluminium the tapping drill can be closer to the nominal and for tougher materials, such as mild steel, the hole size can be slightly larger. A good average would be 2.7mm for the M3 x 0.5mm tap.

## 2. Types of taps

There are three different types of taps in common use; the first being what is known as "Hand-Taps" designed to be used by hand in a tap-wrench. The other two are more specialised and designed to be used in a tapping machine or CNC drilling and tapping machine. These are known as "Machine-Taps" and differ in construction to the hand-taps. Machine taps in general are stronger than hand

**Fig 1: A set of M3 hand taps and tap-wrench. The lower tap is the taper, the middle is the second and the top one is the bottom tap or plug-tap.**

taps and can withstand more torque. They also are unique in that normally only one tap is required to form a perfect threaded hole and can cut at high speed. The difference in cost between a machine tap and a hand tap is small and they are a better proposition for the home user.

Hand taps come in sets of three taps (Fig 1). These are known as “Taper, Second and Bottom”. The first tap used is the taper tap; this starts the threads but leaves them undersize. The second tap brings the threads to the correct size and form. The bottom tap (also known as a “Plug-Tap”) is used where the threads need to reach to the bottom of a blind hole.

Machine taps are available in several different types, some have the square top for use in a hand-tapping wrench and others have a plain shank to fit a collet chuck (Fig 2). The point of the machine tap is often formed in a spiral flute, which makes the tap stronger than a hand tap (Fig 3). For use in high-speed automatic tapping machines for materials such as mild steel the full spiral flute tap gives better threads.

Fig 2: A typical machine tap with the spiral tip.

Fig 3: A spiral flute machine tap for tapping tough materials

## 3.

## Lubrication

When tapping metal the tap should be adequately lubricated to prevent torn threads or jamming in the metal being tapped. Copper and bronze are the worst materials to tap and others less troublesome. A good all round lubricant is light mineral oil such as SAE-10 known as "3 in 1" or Sewing Machine oil. For aluminium some prefer to use paraffin/kerosene, methylated spirits or a proper tapping fluid such as Tapmatic™. For materials such as aluminium die-cast boxes often the hole can be tapped dry.

## 4.

## Starting the pilot hole

Drilling small holes in material such as aluminium and copper can be difficult, as the drill tends to grab and can break the fragile drill bit. It is best if the hole is started with a centre-drill (Slocombe drill) before using the tapping drill. Centre-drills come in several sizes the smallest being the BS-1 that is approximately 3.2mm in diameter (Fig 4). Copious lubrication will ensure the drill is cooled and less likely to grab and break.

## 5.

## Tapping by hand

This will be the most common application for home constructors. The taper tap should be entered into the hole and

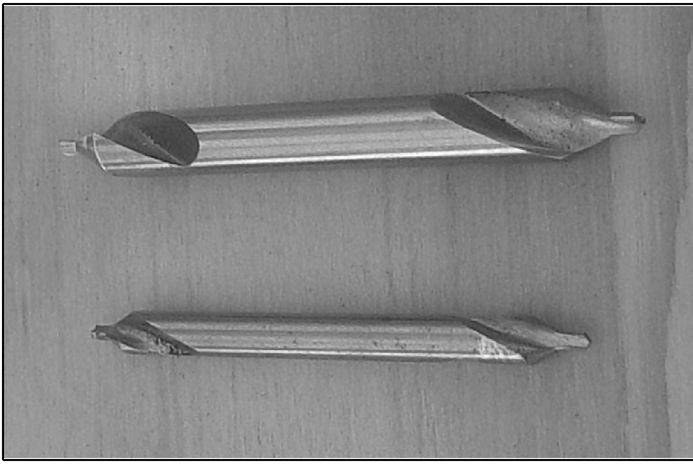

Fig 4: Small centre drills. BS-1 bottom and BS-3 above.

**Table 1: Recommended tapping drill sizes.**

| Screw size | Tapping drill mm |
|---|---|
| M2 x 0.4mm | 1.6 |
| M2.5 x 0.45mm | 2.1 |
| M3 x 0.5mm | 2.7 |
| M4 x 0.7mm | 3.4 |
| M5 x 0.8mm | 4.3 |
| M6 x 1mm | 5.1 |

aligned so it is perpendicular to the surface. Turn the tap-wrench two turns to start the threads and then back off by one turn to break away the swarf. Apply lubrication and turn the tap-wrench a further two turns, feeling for any undue resistance. If the tap starts to go tight then back off at least one turn and apply more lubricant. Small taps are fragile and easily broken! Having tapped the hole with the taper tap use the second tap to finish the threads to size. If the metal being tapped has the hole exiting the material then there is no further work to do apart from clearing away the swarf. If the hole is blind then use the bottom tap to finish the threads but be extra careful as the tap goes tight as it reaches the bottom of the hole. A broken tap can be very difficult to remove if it breaks off flush with the surface.

## 6. Suppliers

Some of the suppliers that I use on a regular basis are shown below, or consult your local Yellow Pages under "Machine Tool Suppliers".

**Chronos Engineering Supplies**

www.chronos.ltd.uk

Chronos Ltd
14 Dukeminster Estate
Church Street
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Tel: 01582 471900

Email: sales@chronos.ltd.uk

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*Gunthard Kraus, DG8GB*

# Internet Treasure Trove

## Microwave101

At first sight the title says nothing. Once you open the site you are greeted with by a complete collection of microwave documents including calculations and information etc. A lot of time is required to investigate everything.

Address:

http://www.microwaves101.com/index.cfm

## Microwave Detectors

Old things can be interesting and delightful. This information is over 30 years old but has been revised again and again plus presented as an Application Note by Agilent (formerly Hewlett Packard). It concerns the correct use of the detectors 423B and 8470B.

What makes this brochure so useful is the detailed cross section and exploded views of older plug e.g. BNC, N, ApC7 etc as well as the notes on correct handling them and the repair or exchange of such detectors. Some people will also find more memories in this Application Note.

Address:

http://cp.literature.agilent.com/litweb/pdf/00423-90103.pdf

## Basic Antenna Theory

For those who want to study the basics of antennas at a very scientific level should take a look at this university site.

Address:

http://farside.ph.utexas.edu/teaching/jk1/lectures/node81.html

## GLOBALSPEC

This site is for those who think they have missed something. It is a high quality engineering search engine that can seek out the maddest things. As an example try the result of this enquiry: Application Notes/Schottky Diodes.

Address:

http://application-notes.globalspec.com/Search?query=Schottky%20Diodes&show=appnotes&frmtrk=ofInterest

## OML

For those who find normal RF technology boring, they should take a look at the technology and problems for the frequency range above 50GHz. This homepage has lots of information on measuring instruments and good Application Notes. This is a completely different world.

Address:

http://www.omlinc.com/map.htm

## Plextek

More and more often manufactures are trying to present information on their new products to their customers and prospective customers. As an example Plextek are introducing a new mixer.

Address:

http://www.plextek.co.uk/papers/mixers2.pdf

For those who take a look will find some different and useful things. Click on "Technical Information" on the home page to get a choice between "Technical Paper" and "Downloads". Selecting Downloads there is a "Smart Antenna Demonstration" that can be downloaded.

Address:

http://www.plextek.co.uk/downloads.htm

## Amateur radio Astronomy/Western Australia

Radio astronomy always works on the edge of technical possibilities and is therefore worthwhile taking a look for any RF freak. These people begin with low frequencies (see the article on Schumann resonances) and do not stop at 10GHz. All the methods and devices are explained with no secrets. There is also plenty of interest to non astronomers.

Address:

http://wavelab.homestead.com/

## Ultra Low Power ELF/VLF Receiver Project

Having mentioned Schumann resonances, this continues in the same frequency range. In such receivers the same thought processes and the same technical work is required as in 10GHz project.

This is worth a look and it will inspire your imagination.

Address:

http://www-star.stanford.edu/~vlf/ulp_reciv/ulp.htm

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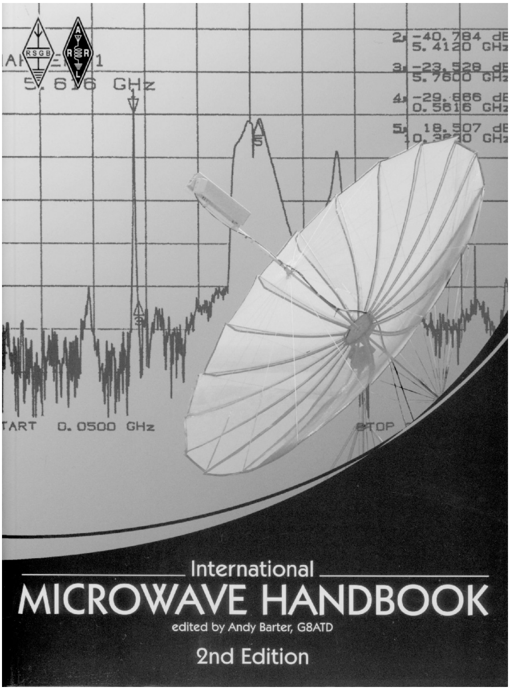
# The International Microwave Handbook 2nd Edition




The microwave bands are an excellent area for radio amateurs who want to experiment and construct their own equipment. The RSGB in partnership with the ARRL has produced this invaluable source of reference information for those interested in this area, along with excellent designs from around the world to fire the imagination. Material has been drawn from many sources including the RSGB journal RadCom and the ARRL publications QST & QEX. Alongside this material a truly international range of sources have been used including items from Germany, Denmark, New Zealand, Slovenian and many more.

The earlier chapters of the book provide invaluable reference material required by all interested in this exciting area of experimentation. Techniques and devices are covered in depth, leading the reader to understand better the wide range of equipment and techniques now available to the microwave experimenter. This book contains a wide selection of designs using the latest technology that can reasonably be used by radio amateurs and ranges from ones that can be reproduced by most radio amateurs to those that require a high degree of skill to make.

With the explosion in consumer electronics using microwave frequencies the opportunity to experiment has never been greater and this book is simply the.

**The handbook is available from The RSGB or ARRL**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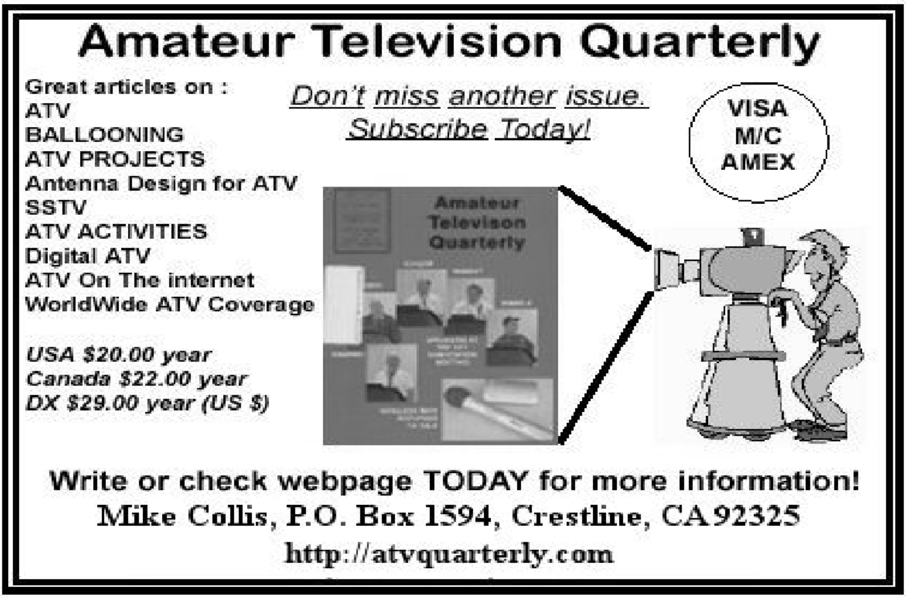
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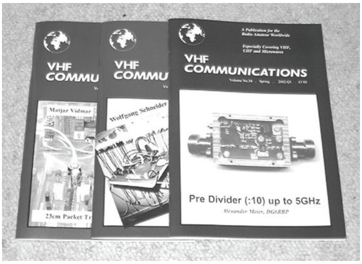


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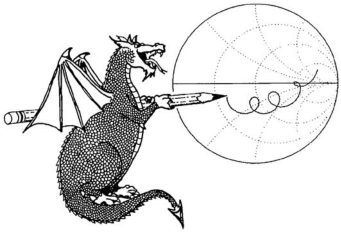

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