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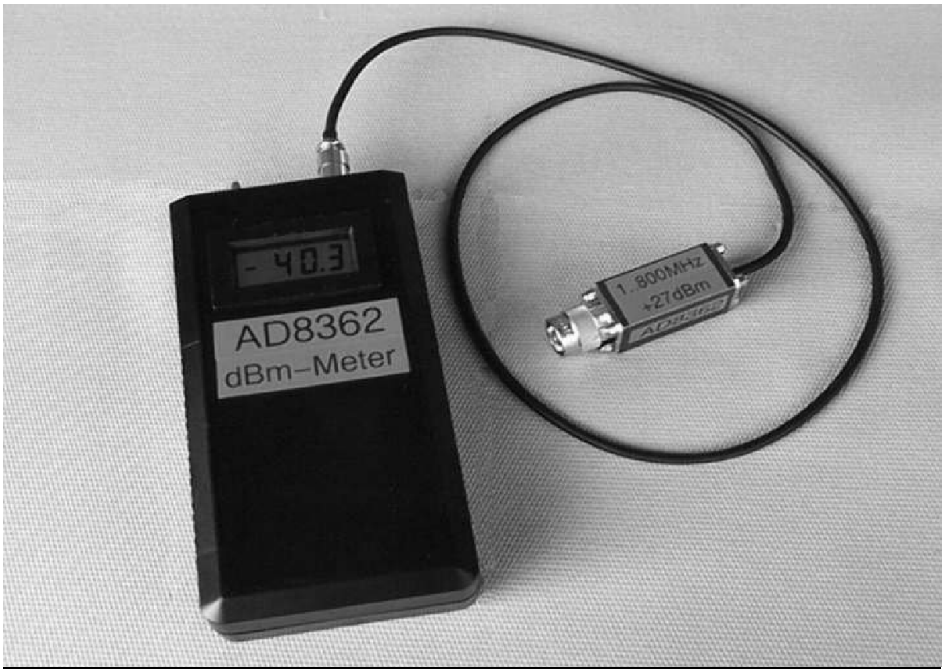

Wolfgang Schneider, DJ8ES

Low power radio frequency wattmeter using an AD8362 detector

Contents

Some interesting articles again including two approaches to PLL oscillators. The first uses a CPLD to provide the control logic, the second uses a microprocessor. Alexander Meier's microprocessor controlled PLL is still under development unfortunately his latest version was not ready in time to include in this magazine.

After requests for articles on CD from various places, I have produced the first compilation CD, see page 190 for details. I took them to Freidrichshafen and sold one, since then I have sold another four. From this sales rate I can only conclude that there is not a big requirement for such CDs. I would appreciate any feedback about future CD compilations.

73s - Andy

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Peter Arlt, DG4EAY

Simple PLL oscillator for receivers with 45MHz intermediate frequency

To assemble a DIY receiver you need (among other things) a stable VCO. It is a bonus if this VCO is also easy to copy, needs scarcely any SMD components and is also affordable. A project of this nature is described below.

This article describes a novel way to implement a PLL using a CPLD (Complex Programmable Logic Device). The magazine "Funk" in Germany published a series of articles on CPLDs in issues 6, 7 and 8 2004, these are referred to by Peter. Unfortunately these articles are in German, there are some similar articles that I have found [4], [5]. I have asked Peter if the full logic diagram implemented by his CPLD program is available, he does not want it published but can be contacted if required. Peter can also supply programmed CPLDs, PCB layouts and details of a version using a shaft encoder to set the frequency instead of thumb switches, please contact me for further information - Andy

1. Introduction

Assembling a DIY short-wave receiver (or any other receiver) is an interesting task for a radio ham or an electronics engineer. The description that follows does not cover a complete receiver, but merely the tuning oscillator. The aim was to develop a stable VCO that would be easy to copy. The price of such an oscillator is a factor that is just as important as the amount of mechanical work involved. It's true that today it is possible to assemble extremely stable free-running oscillators. However, this requires some expensive temperature compensation, and some mechanical knowledge is also required.

There are two main groups of oscillators – free-running units, that can be tuned by means of a variable capacitor (VFO) or capacitance diodes (VCO) and PLL controlled oscillators. The latter was chosen since this system is easier to copy and relatively low priced. The technical data for the prototype can be found in Table 1.

The entire circuit fits easily onto a 40mm x 100mm breadboard, but a special printed circuit board was also developed.

Table 1: Technical data of PLL

Frequency range	45,000.0 to 74,999.9MHz
Resolution	100Hz
Settling time	<1sec
Output	approximately +8dB
Supply	20v / 70mA, 5v / 150mA

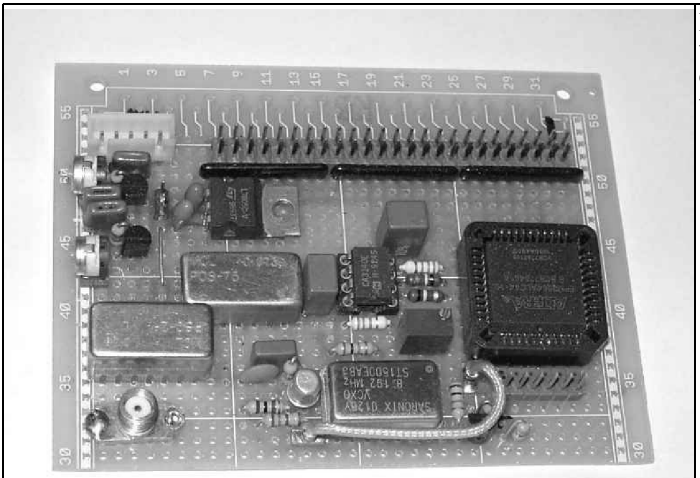

Fig 1: Picture of the completed PLL oscillator showing the CPLD chip.

The PCB and component layout are shown in Figs 7, 8 and 9.

Note: It should be clear that this relatively simple oscillator, it was not designed for high-end receivers. It is easily stable enough for simple short-wave receivers with SSB and CW, but not for bandwidths smaller than 100Hz. No data was measured regarding phase jitter or similar because the equipment required was not available.

2. Description

There are two affordable, state of the art options available. The first is to use a DDS, this was ruled out for various reasons:

- ease of copying; the components are in an SMD package with a pin spacing of 1/40 inch or less; this calls for suitable tools, good motor skills and "eyes like a hawk"; so errors are bound to happen with the assembly
- DDS components always need a micro-controller with appropriate programming in order to function.

My intention was to remain within the 1/10 of an inch pitch (2.54mm) and to dispense with any standard language programming. Another objective behind my approach was to avoid the complex frequency spectrum when a micro- controller is to be used. This either requires expensive shielding or can lead to considerable radiation into the receiver.

The second option is the discrete assembly of a PLL using logic modules. However, in order to avoid the extensive wiring which is required for many components, I selected a so-called CPLD; these are complex logical circuits with up to 5,000 gates on one chip. The basic facts about these components have been published in the relevant electronics magazines [6], so if you want to go into the subject further, that's the place to look.

Many of these CPLD modules can be supplied in PLCC packages with 44, 68 or 84 pins. Then again, there are suitable versions within the 1/10 of an inch pitch pins, which is important for ease of

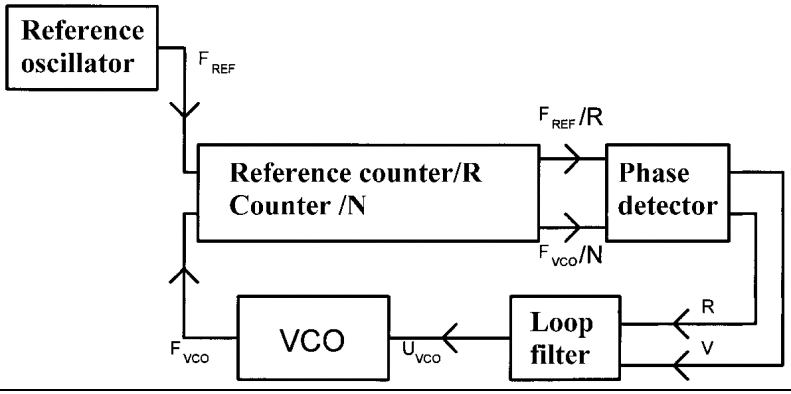

Fig 2: Block diagram of the digital section of the PLL oscillator.

copying. Components from Altera [1] were chosen, but there are many other manufacturers of similar components. The big disadvantage is the fact that the components are incompatible with one another. It is unfortunately not possible to replace, for example, a chip from Altera by a chip from Xilinx, although they offer the same range of functions and can also work with the same program.

The modules can be "programmed" in two ways: the first option uses a standard language such as VHDL, AHDL etc. The second (which is a lot simpler) uses a wiring diagram editor. Altera has an extremely comprehensive TTL library, which is freely available.

Anyone familiar with the 74xxx / 54xxx TTL range (now "well advanced in years") can very easily set up his/her own "personal" logic circuit, which is precisely what happened here.

An EPM30664ALC44-10 CPLD was used. This is a chip in a 44 pin PLCC housing with a 3.3 Volt operating voltage and space for 34 I/O pins, together with 64 macrocells (Fig 1). The entire digital section of the PLL was integrated in this fashion. The current consumption for the module is less than 100mA.

The JTAG programmer interface should be available, so that any program changes in the operating circuit can be enabled using the ISP (In System Programming). In the present case, this doesn't necessarily apply, since the chip is used to capacity and has exhausted its options, but for other chips (and especially for relatively large chips) ISP is very advantageous. In addition, many companies use this option for updates via the Internet.

3. Circuit diagram of digital section

3.1. Functions of CPLD

The following functional groups are accommodated in the CPLD (Fig 2):

1. A 6 digit, divide by N, counter
2. ROM for conversion
3. Counter control
4. Reference frequency generator
5. Phase detector

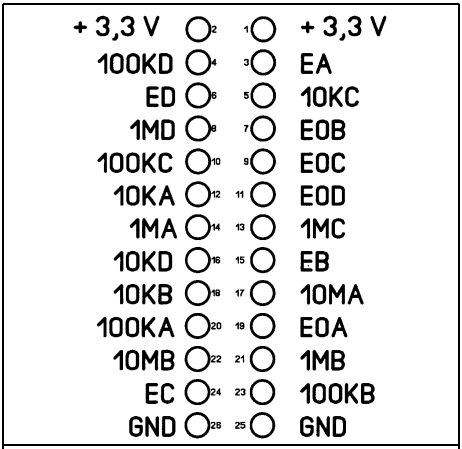

Fig 3: Pin connections for the thumbwheel switch connector.

Figs 3, 4 and 5 show design information for the CPLD.

3.1.1 Divide by N counter

It consists of 6 74190 pre-set decimal counters. These counters are connected in series – i.e. the output from the first counter is linked to the input of the second counter, the output of the second counter is linked to the input of the third counter, etc.

Each of these counters has 4 BCD pre-set inputs. This means that the counter can be pre-set via these inputs to a specific value within the range of 0 to 9 to determine its count ratio. Thus, the entire counter chain, we have ratios from decimal 0 to 999999. This project only requires the range from 450000 to 749999, the inputs of the counters with the highest values are permanently pre-set to 4, and the value 8 is set to 0, so that only count ratios of 4 to 7 are possible.

Tuning is carried out using BCD coded thumbwheel switches. Switches with an active logic outputs of "1" should be used.

CHIP "PLL45" ASSIGNED TO AN: EPM3064ALC44-10

Pin Name/Usage	Location	Dir.	I/O Standard	Voltage	I/O	User Assig
GND+	1					
IN81M	2	input	LVTTL			Y
VCCINT	3	power		3.3V		
EA	4	input	LVTTL			Y
E0B	5	input	LVTTL			Y
I100KD	6	input	LVTTL			Y
TDI	7	input	LVTTL			N
I10KC	8	input	LVTTL			Y
ED	9	input	LVTTL			Y
GND	10	gnd				
I1MD	11	input	LVTTL			Y
E0C	12	input	LVTTL			Y
TMS	13	input	LVTTL			N
I100KC	14	input	LVTTL			Y
VCCIO	15	power		3.3V		
E0D	16	input	LVTTL			Y
GND	17	gnd				
I10KA	18	input	LVTTL			Y
I1MC	19	input	LVTTL			Y
RESERVED	20					
RESERVED	21					
GND	22	gnd				
VCCINT	23	power		3.3V		
RESERVED	24					
EB	25	input	LVTTL			Y
I10KD	26	input	LVTTL			Y
I10MA	27	input	LVTTL			Y
I10KB	28	input	LVTTL			Y
E0A	29	input	LVTTL			Y
GND	30	gnd				
I100KA	31	input	LVTTL			Y
TCK	32	input	LVTTL			N
RP2	33	output	LVTTL			
VP3	34	output	LVTTL			
VCCIO	35	power		3.3V		
GND	36	gnd				
I1MB	37	input	LVTTL			Y
TDO	38	output	LVTTL			N
I10MB	39	input	LVTTL			Y
EC	40	input	LVTTL			Y
I100KB	41	input	LVTTL			Y
GND	42	gnd				
Fin	43	input	LVTTL			Y
I1MA	44	input	LVTTL			Y

Fig 4: Pin assignments for the Altera CPLD.

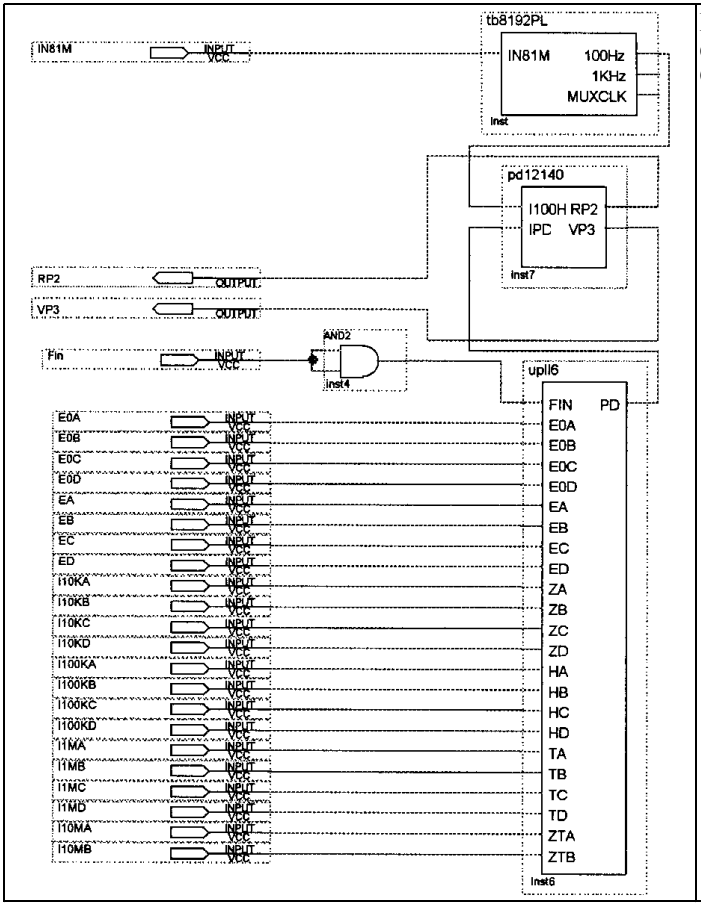

Fig 5: Block diagram of the CPLD.

3.1.2 ROM for conversion

In order to obtain a setting and/or display showing the correct frequency of 00,000.0 to 29,999.9MHz, a ROM must be internally connected in series with the counters with a conversion table that converts the range of 00 to 29 into the required range of 45 to 74.

One brief comment – this article is not intended to be concerned with the complex theory of phase locked oscillators. For more detailed information on this PLL circuit technology, look for specialist books [2] or search on the Internet.

3.1.3 Counter control

The counter control connects the counters together to produce the required frequency of 100Hz for the phase detector. This signal is not easy to see on a simple oscilloscope, since the rise time of the pulse is only a few nanoseconds. It can be checked using a frequency counter as a frequency of 100Hz. This signal is fed to the phase detector.

3.1.4 The reference frequency generator

A quartz crystal oscillator of 8,192.000MHz was used as the reference

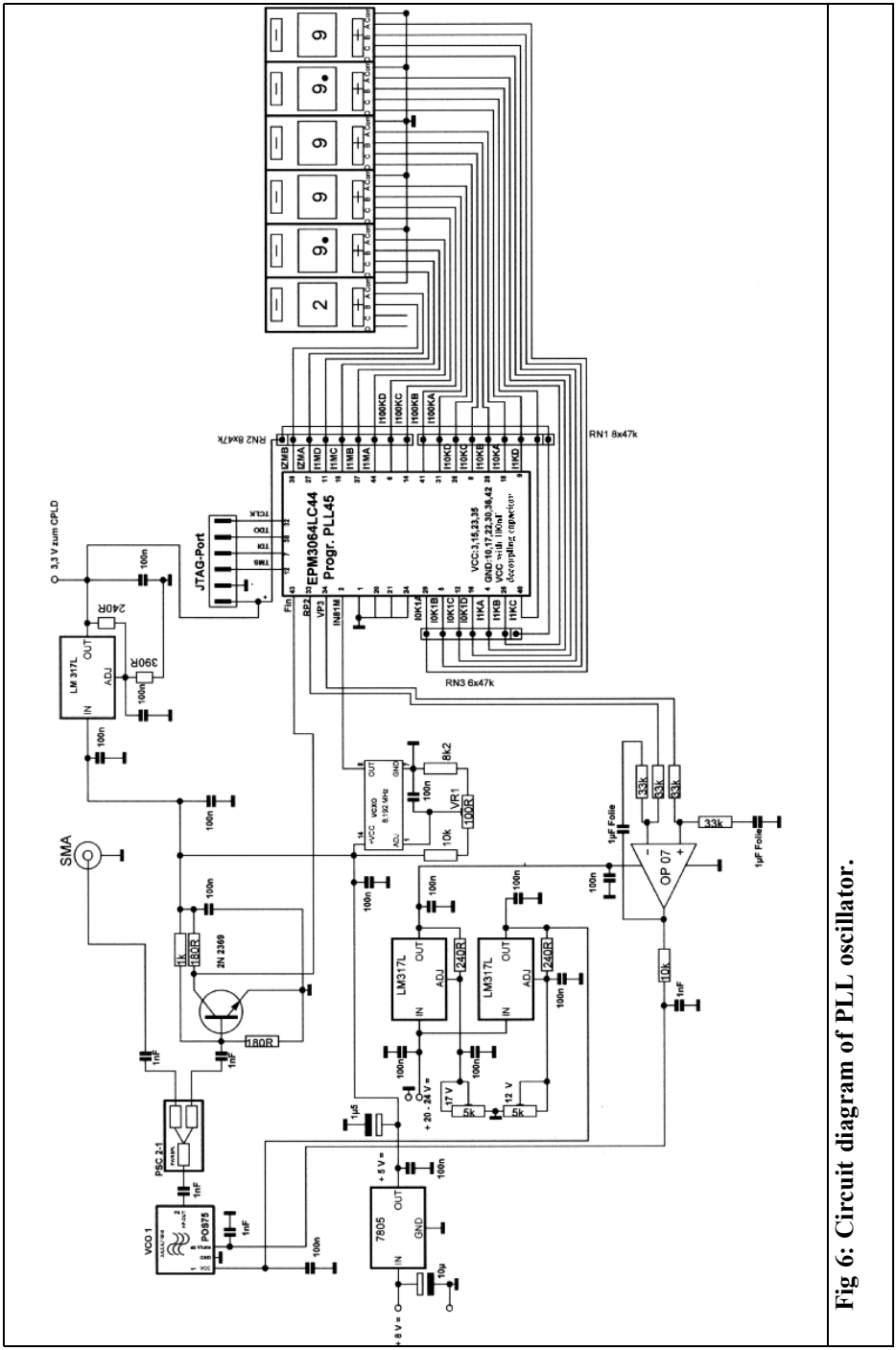

Fig 6: Circuit diagram of PLL oscillator.

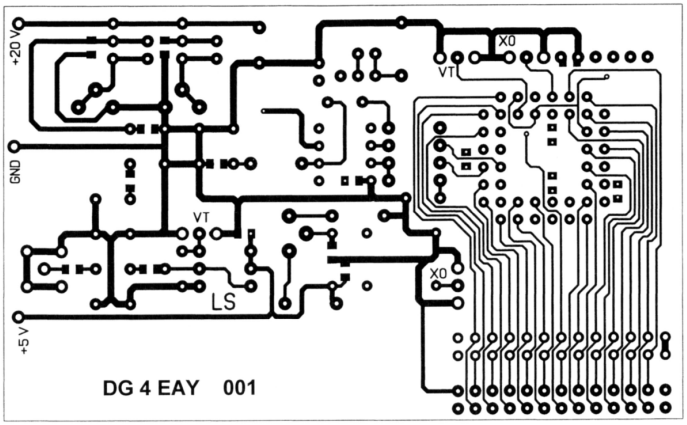

Fig 7: Bottom side of PCB for PLL oscillator.

frequency generator. An "even" frequency of, for example, 1MHz or 10MHz was not used, in order to avoid any unnecessary radiation into the receiver input. This would mean that signals of 1MHz, 100kHz, 10kHz etc. would be generated in the counters. These signals would generate spurii, due to the fast rise time of the pluses, which would be audible in the receiver at the corresponding interval, and would, in certain circumstances blank any signal input.

The reference frequency of 8,192.000MHz is divided down to 100Hz through a multi-stage counter chain, consisting of three counters: divide by 16, divide by 2, and divide by 10. This gives the required division of 81,920 and thus an output frequency of 100Hz. This 100Hz signal is likewise fed to the phase detector.

3.1.5 The phase detector

The phase detector compares the signals from the reference frequency generator and the counter control to generate a pulse trains, depending on the discrepancy. These pulses are converted into a voltage for the VCO in the loop filter described later. The phase detector used here is actually a phase/frequency detector. This means that both the phases and the frequencies of both input signals are compared and evaluated.

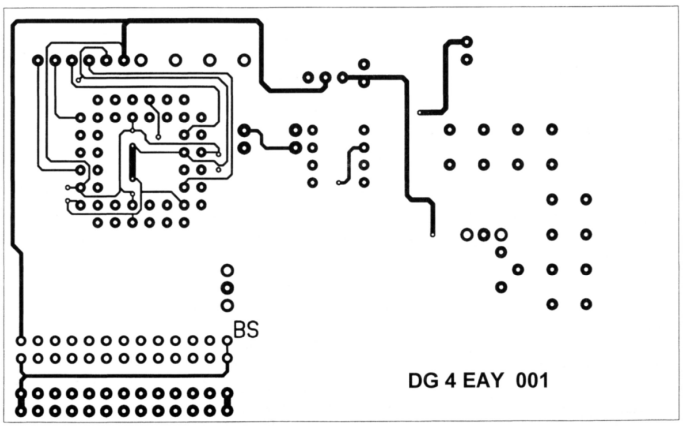

Fig 8: Top side of PCB for PLL oscillator.

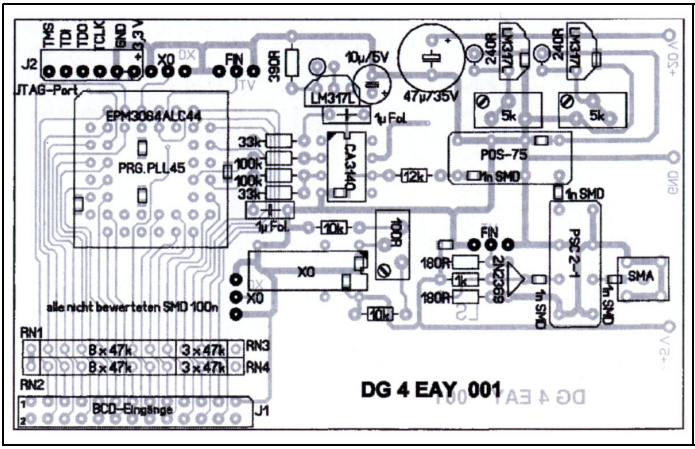

Fig 9: Component layout for PLL oscillator.

4. Circuit diagram of PLL oscillator

The circuit diagram of the PLL oscillator, including the CPLD and BCD coding switches, is shown in Fig 6.

4.1. Analogue section

The analogue section consists of two functions, the VCO and the loop filter.

4.2. Loop filter

The task of the loop filter is to generate the tuning voltage for the VCO from the "V" and "R" pulses from the phase detector. The loop filter used was designed empirically and can undoubtedly still be further optimised. One problem is the relationship between the frequency switching speed and adequate suppression of the phase pulse. An active filter using an operational amplifier is used. A passive filter would not be adequate for the voltage swing required for the VCO of approximately 11 volts.

4.3. The VCO

An industrially manufactured VCO from MiniCircuits is used. The frequency range is approximately 40 to 80MHz, with a tuning voltage of 1 to 17 volts. The output is approximately +10dBm to 50 ohms. This VCO has the ideal frequency range, high free-running stability, only slightly temperature dependent, together with a good phase jitter performance.

No doubt it would also be possible to build a DIY version of such a VCO, with similarly good parameters, but undoubtedly not with the favourable price / output ratio. I used a type POS75 in a plug-in housing, which costs about 20 Euros, one off. The supply voltage of the VCO is 12 to 15V max.

In order to avoid any loading effects on the VCO, the RF output of the VCO is fed to a power splitter. The RF signal is split into 2 outputs. One output is terminated at 50 ohms and feed the CPLD via a TTL converter. The other output goes to the receiver mixer, which must have an input resistance of 50 ohms. This power splitter does perform correctly unless it is terminated at 50 ohms. A PSC 2-1 splitter from Mini Circuits was used [3].

4.4. Power supply

Four controlled voltages are needed, and it makes sense not to generate them all

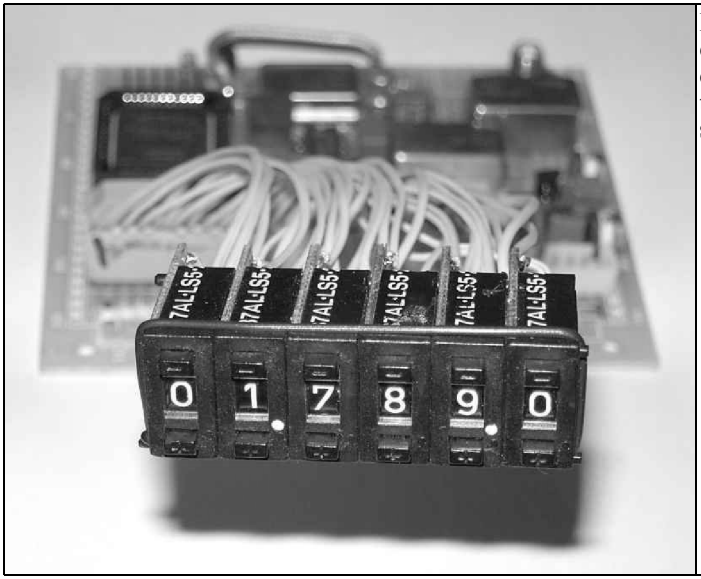

Fig 10: Picture of completed PLL oscillator showing the thumbwheel switches.

from a single basic voltage.

+ 16V, with as high a degree of stability as possible, is required for the operational amplifier in the loop filter. This voltage must be extremely stable, since any changes would have an immediate effect on the frequency, which again would lead to readjustment of the PLL. You must bear in mind how big (or preferably small) the voltage change in the tuning voltage is for a frequency change of 100Hz. With a total tuning range of 35MHz and a tuning interval of 100Hz, there will be a tuning voltage of 11/350,000 or approximately 30µV! And then, imagine a ripple voltage of only 1mV on the tuning voltage.

A second voltage of approximately 12 to 15 volts is needed for the VCO.

These two voltages can be generated from one voltage of approximately 20V, either from a power supply or else from a 5/24 V voltage transformer. Two LM317L's regulators are used with potentiometers for adjustment. Before connecting to the power supplies, first set and check the voltages.

The quartz crystal oscillator requires +5V at approximately 40mA.

The fourth supply voltage for the CPLD (3.3 volts) can be generated from the +5V supply. One LM317L is quite sufficient as a voltage regulator. The voltage is set using fixed resistors.

As already mentioned, the +5 volt supply should not be generated from the +20 volt supply. The power loss would be too great, generating too much heat. This would be very detrimental to the frequency stability of the oscillators.

5. Developments

As already noted, the chip used is pretty well used to capacity, which, above all, affects the number of macrocells. Subsequent changes are almost impossible, as

this would change the pin occupancy, which is in a specific relationship to the macrocells.

For relatively large CPLDs, it is possible, for example, to integrate a digital frequency display or a rotary encoder to provide the frequency input.

The basic point to make is that we should not believe that an "open air oscillator" can be used in a PLL and the PLL will just regulate it. True, this is correct in principle, but the continuous readjustment of the PLL would generate a very high degree of phase jitter, which would have the direct effect on receiving weak signals in a receiver. This behaviour is even more serious for a transmitter. I recommend that this circuit should not be used for a transceiver! For that there would have to be monitoring of the loop, i.e. a lock-detect circuit would have to be used, which would make it absolutely certain that the transmitter could not be operated with a loop that was not locked.

6. Appendix

6.1. The parts list

Semiconductors:
1 x EPM 3064LC44, (CPLD)
1 x 7805, 5V, fixed voltage regulator
3 x LM317L, variable voltage regulator
1 x CA3140, OP-Amp
1 x 2N2369, NPN trans.

Resistors:
2 x 180
3 x 240
1 x 390
1 x 1k
1 x 8.2k
2 x 10k
2 x 33k
2 x 100k

Trimmers
1 x 100
2 x 5k

Resistor arrays:
1 x 4k (6 units)
2 x 47k (8 units)

Capacitors:
1 x 10µF, electrolytic capacitor, 16V
1 x 1.5µF, electrolytic capacitor, 16V
2 x 1µF, foil
15 x 100nF, ceramic, 35V
4 x 1nF, ceramic, 35V

Special components:
1 x POS 75, VCO
1 x PSC 2-1, RF power splitter
1 x VCXO 8,192MHz,
6 x BCD switch
1 x JTAG port
1 x SMA socket

7. Literature

[1] www.altera.com

[2] PLL engineering, principles and use of frequency synthesisers, Georg Walz; Franzis Workbook 1989; Franzis Verlag Munich; ISBN 3-7723-5204-9

[3] Data sheets for components used www.minicircuits.com

[4]

http://fie.engrng.pitt.edu/fie96/papers/214.pdf

[5] http://www.qsl.net/g6uyj/jtag.html

[6] Funk magazine issues 6, 7 and 8 2004

Wolfgang Schneider, DJ8ES

Low power radio frequency wattmeter (dBm) using an AD 8362 detector

Although widely available, "useable" low power wattmeters for the mW range are still expensive. Whether it's a second-hand instrument from the surplus market or a new piece of equipment, you still normally need to pay a rather large three figure sum.

Fortunately there is the option of assembling a suitable measuring instrument yourself, with the help of modern integrated circuits such as the AD 8362 True-Power detector, in combination with a standard LCD voltmeter module. The readings obtained from such equipment are in no way inferior to those from commercial products.

1. General

Analog Devices has developed the AD 8362 module for measuring power over a wide frequency and power range. Thanks to special internal compensation measures, it can also be used over a wide temperature range.

The IC forms part of a whole family of power detectors which were originally developed for the ranges covering mobile telephones, the broadband distribution network and wireless-LAN applications in a frequency range going from 1MHz to more than 8GHz. They are normally used for regulating the transmit power in such systems.

2. Parameters of AD 8362

According to the manufacturer's specifications, the AD 8362 detector displays entirely linear behaviour over a very wide frequency range, going up as far as 2.7GHz. Our own measurements confirm the good characteristics of this integrated module, though natural resonances and other non-linearities, caused by the assembly, are visible in Fig. 6. These result from the circuit design selected, the construction used and from the circuit layout.

According to the data sheet, the best results are obtained with a 1:4 balun at the input. The circuit suggested here displays certain irregularities in the frequency response, so it cannot be used for frequencies below 10MHz and falls off above 1.9GHz by 1dB or more.

If all the advantages and disadvantages listed above are taken into account, and in view of the planned use of this

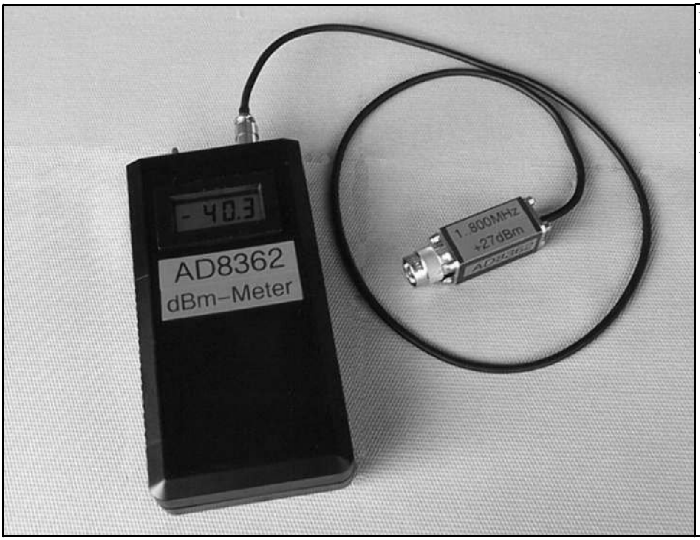

Fig 1: Photograph of the prototype wattmeter showing the measuring head and the display unit.

equipment as a radio-frequency low power wattmeter for amateur radio use, assembly for frequencies from 1MHz up to 1,000MHz is favoured. The prototype circuit proposed in this article is laid out accordingly.

3. Circuit description

The core of the measuring head (Fig 3) is the AD 8362 True-Power detector (IC1). The external wiring required for this module is essentially restricted to a few blocking capacitors (C2 to C6) and the input matching required by R4 (100 Ohms).

The 16dB input attenuator is used to establish the measurable input power range between -40dBm and +23dBm. This range of values can vary slightly, depending on the component tolerances. Thus, for example, our prototype (Fig. 1) displays power levels of between -37dBm (0.5µW) and +27dBm (500mW).

A display unit for dBm can be made very simply using a ready-made LCD voltmeter module. The output voltage of the

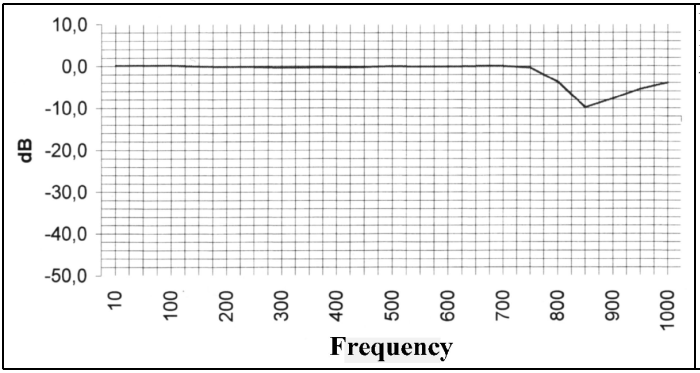

Fig 2: Frequency response in dB up to 1000MHz.

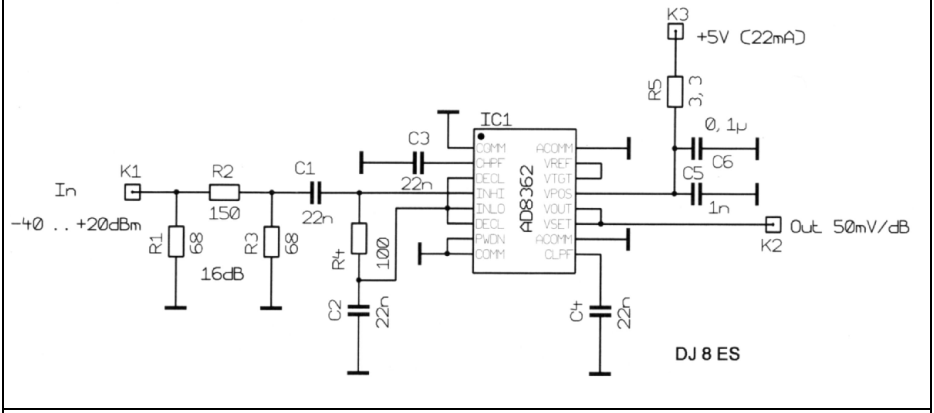

Fig 3: Circuit diagram of the measuring head using an AD8362.

measuring head is matched to the input voltage range of the LCD module (-200mV to +200mV) using an OP90P operational amplifier (IC1) with a downstream voltage divider. The amplification can be adjusted precisely by means of the 20kOhm precision trimmer (R6).

The offset voltage required (here approximately 40mV) for the zero point adjustment is obtained using a diode (potential difference 0.7V) connected to the trimming potentiometer, R7 (5kOhm).

The circuit for the display unit assembly (Fig 7) is operated directly from 9V (e.g. 9V battery). The 5V voltage regulator, IC2 (78L05) serves to generate the reference voltage for the zero point calibration and the operation of the measuring head.

4. Assembly instructions

The actual measurement detector is assembled on a 34mm x 34mm double-sided copper-coated epoxy printed circuit board, DJ8ES 068 (Fig 8).

Only SMD components can be considered because of their RF characteristics. They are all mounted on the topside of the board (Fig 9), while the underside

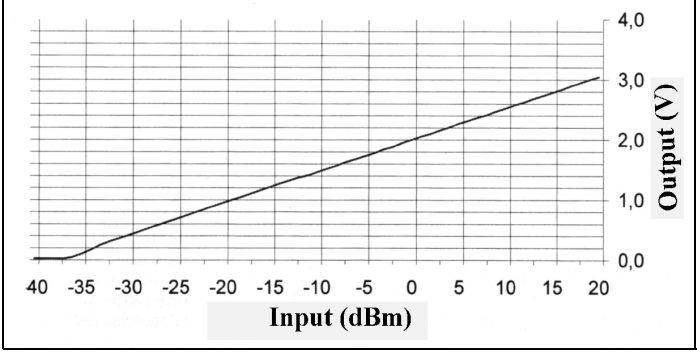

Fig 4: The output characteristic of the measuring head from -40dBm to +20dBm.

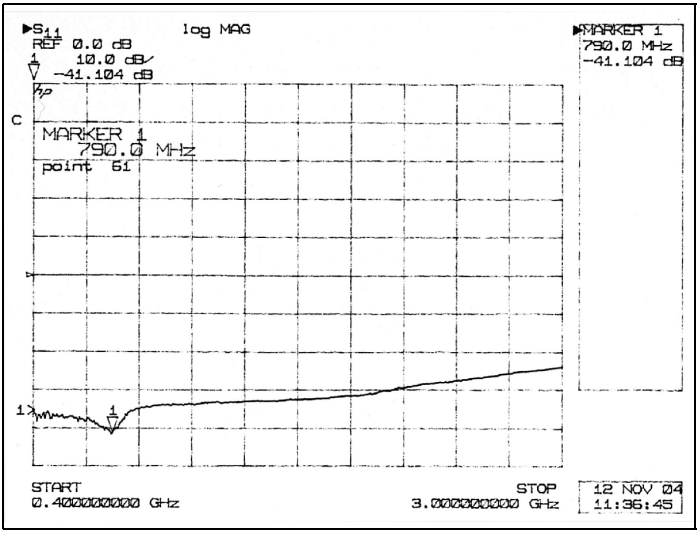

Fig 5: Even up to 3GHz the input sensitivity is approximately -40dB.

serves only as an earthing surface. Low inductance earth connections are made using feedthroughs at the relevant points.

A suitable tool should be used for mounting the SMD components such as a soldering iron with a fine tip, and 0.5mm solder. It pretty much goes without saying that the soldered points must be "clean".

The assembly can be incorporated in an appropriate housing, depending on people's individual wishes (e.g. from Mini-Circuits). The board must be cut to the required size before the components are mounted.

The electronics required for the display unit are assembled on a 52mm x 34mm single-sided copper-coated epoxy board, DJ8ES 069 (Fig 11).

In contrast to the detector, only wired components are used here (Fig 12). The components are mounted in no particular order.

4.1. Detector parts list

IC1	AD8362, Detector, SMD
C1- C4	22 nF, ceramic capacitor, SMD 0805
C5	1 nF, ceramic capacitor, SMD 0805

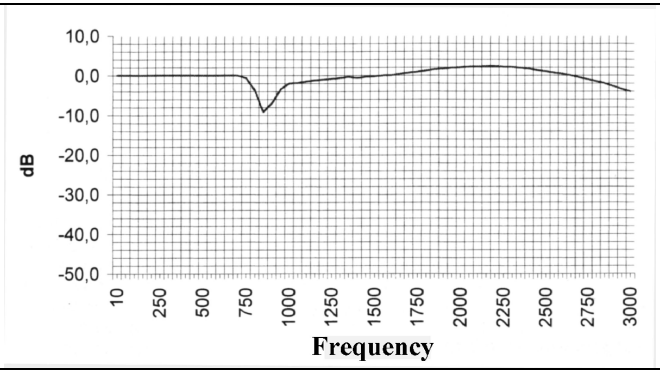

Fig 6: Some non-linearity is caused by resonances.

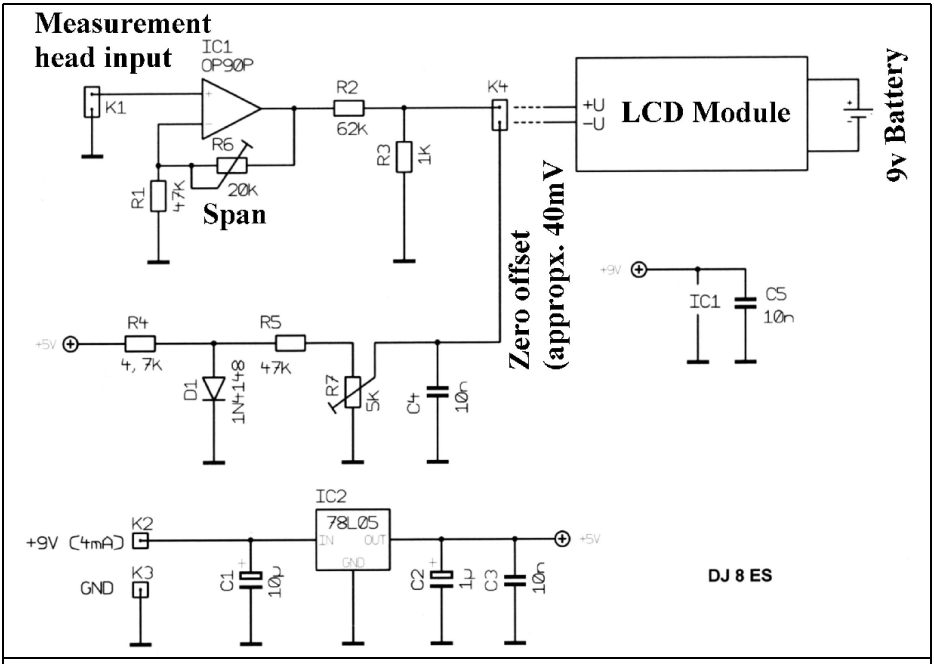

Fig 7: Circuit diagram of the display unit.

C6 0.1 µF/16 V, tantalum electrolytic capacitor, SMD

R1, R3 68 Ohms, SMD 0805
R2 150 Ohms, SMD 0805

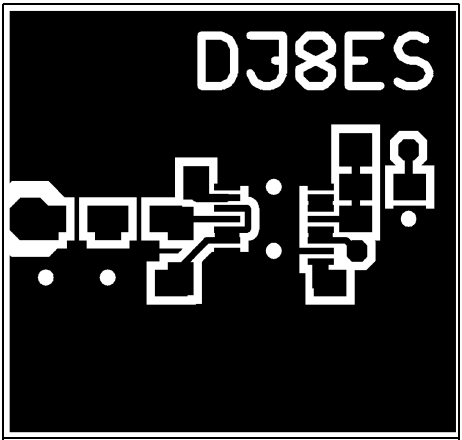

Fig 8: PCB layout of the measuring head.

R4 100 Ohms, SMD 0805
R5 3.3 Ohms, SMD 0805

1 x printed circuit board DJ8ES 068

4.2. Reading display parts list

IC1 OP90P, Operational amplifier
IC2 78L05, Fixed voltage regulator

D1 1N4148, Diode

Resistors 0.25W, RM 10mm:
R1, R5 47 kOhms
R2 62 kOhms
R3 1 kOhms
R4 4.7 kOhms

Precision trimmer:
R7 5 kOhms, Model 64 W,
R6 20 kOhm, Model 64 W,

C1 10µF/25V, tantalum, RM 2.5mm
C2 1µF/25V, tantalum, RM 2.5mm
C3-C5 10nF, ceramic capacitor, RM 2.5mm

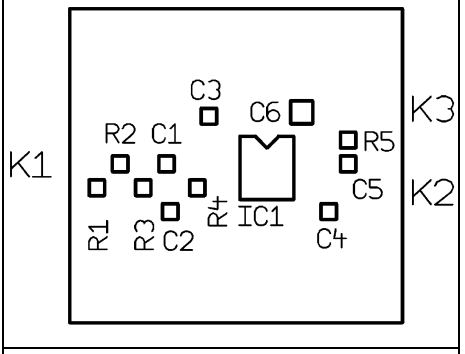

Fig 9: Component layout of the measuring head

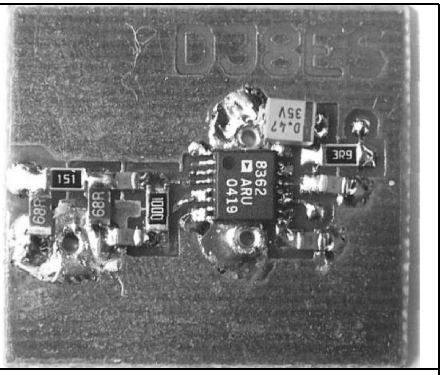

Fig 10: Picture of the completed measuring head.

K1, K4 Pin-and-socket connector 2-pin

K2, K3 Soldering iron 1 mm

1 x printed circuit board DJ8ES 069

5. Putting into operation and calibration

The measuring head itself does not require any special calibration. Once it has been put into operation, just check the current consumption (approximately 22mA) and the presence of an output signal. The output signal should display a slope of approximately 50mV per dB of input level. The characteristic curve in Fig 4 shows the behaviour of the specimen set-up.

The current consumption for the display assembly is only 4mA, or 26mA when the measuring head is switched on, from a 9V battery. An important point here is that the LCD voltmeter module is operated from its own battery.

First, the offset voltage (zero point adjustment) is set using R7 (5kOhms) to approximately 40mV. Then it's the turn of the trimmer for the slope, R6 (20kOhms). It must be approximately in the mid-position when the calibration

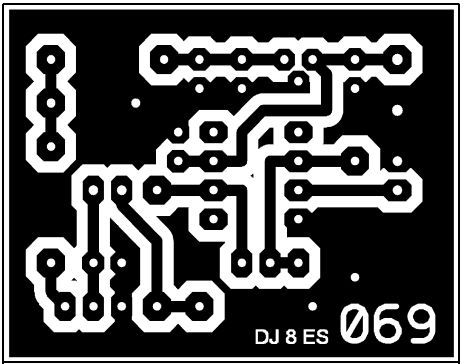

Fig 11: PCB layout of the display unit.

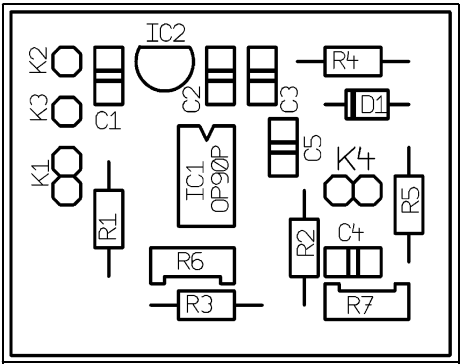

Fig 12: Component layout of the display unit.

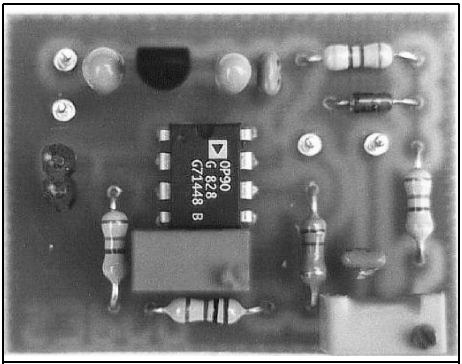

Fig 13: Picture of the completed display unit.

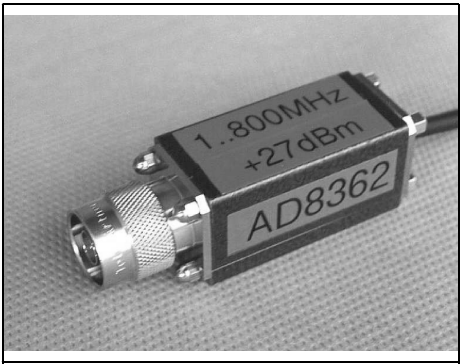

Fig 14: Picture of the enclosure used for the measuring head.

procedure begins.

The simplest way to calibrate the linearity is to use a switchable attenuator of, for example, 20dB. During the calibration procedure, the absolute value of the reading displayed is of no importance. It is only the difference between the two test levels that is relevant.

Finally, the offset for the input signal is precisely adjusted. The LCD display is set to 0 for a test signal with a level of 0dBm.

6. Outlook

The measuring instrument described above makes a low power radio-frequency wattmeter available (mW meter) for the power range from < 1µW up to 500mW, though in this version the display is shown only in "dBm".

Frank Peter Richter (DL5HAT) is currently working on a display unit with a 4 line LC display. This should make it possible to display the readings from the AD8362 measuring head in dBm, mW and mV. As a special feature, an additional plug-in attenuator (e.g. a directional coupler or a series attenuator) can be allowed for, operating in 0.1dB steps. This new display unit will be described here once the project has been successfully completed.

7. Literature

[1] Analog Devices: Data sheet AD8362, www.analog.com

[2] Logarithmic amplifier up to 500MHz with AD8307, Wolfgang Schneider, DJ 8 ES, VHF Communications 2/2000 pp 119 - 124

Prof. Gisbert Glasmachers

Non-linear distortions

A quality feature in demand almost everywhere today is amplifier with linear characteristics. It doesn't matter if we're talking about audio or video applications, the amplification of sensor signals, A/D and D/A converters or radio-frequency amplifiers, as technical progress advances the linearity has to keep getting better and better. This raises the question about which parameters most meaningfully describe the residual non-linearity and which measuring methods can be used to measure them. This article gives a summary of the various definitions of non-linearity and the measuring methods used.

1. Non-linearity and harmonics

A non-linear transmission characteristics distorts a signal. The inter-relationship can best be described in terms of the spectrum.

A pure sine signal with the frequency f_1 is applied at the input. In terms of the spectrum, this consists of an individual line (Fig 1, far left).

The amplified sinusoidal voltage, U_1, appears at the output, and likewise at frequency f_1. But there are also additional lines, U_2 at double the frequency, U_3 at three times the frequency, etc. These frequencies are described as harmonic oscillations or as harmonics. They represent the distortions in the output signal. Their amplitude decreases as the amplifier becomes more linear. An absolutely linear characteristic generates no harmonics.

The amplitudes of harmonics usually decrease as the ordinal number increases. Thus the third harmonic (U_3) is bigger than the fifth (U_5), which is bigger than the seventh, and so on.

It is also typical of non-linear amplifiers that the even-numbered harmonics have a smaller amplitude than the adjacent odd-numbered ones – e.g. $U_2 < U_3$. This is connected with the symmetry of the amplification characteristic. The output spectrum in Fig 1 shows this effect. In principle, the spectrum contains an infinite number of harmonics, but their amplitudes continuously decrease. At some point, they disappear into noise, or they can simply be ignored.

2. Mathematical inter-relationships

A linear characteristic is described by a linear equation.

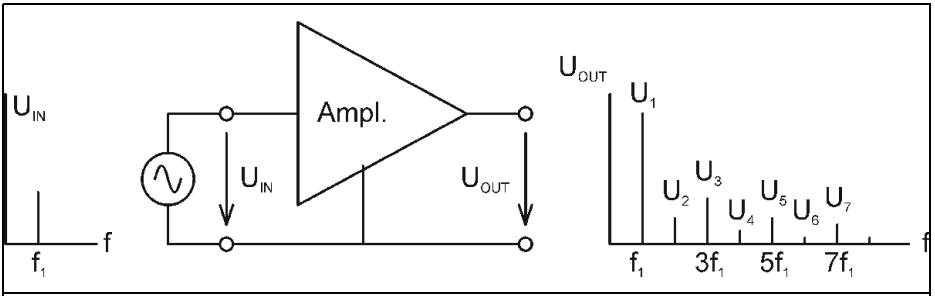

Fig 1: Sine wave input and outputs from an amplifier.

$$U_{OUT} = A_1 * U_{IN} \qquad [1]$$

where the term A_1 represents the voltage amplification A non-linear characteristic is described by a power function:

$$U_{OUT} = A_1 * U_{IN} + A_2 * U^2{}_{IN} + U^3{}_{IN} + \cdots \quad [2]$$

The series is infinite, but its members become smaller and smaller as the exponent becomes larger. For technical purposes, it is often interrupted after the third term. The first term represents the linear amplification known from equation [1], the second and all others describe the curvature of the amplification characteristic. On the assumption that the input voltage is a pure sinusoidal voltage, at the output we obtain:

$$U_{OUT} = A_1 * U_{IN} * \sin(\omega t) + A_2 * U^2{}_{IN} * \sin^2(\omega t) + A_3 * \sin^3(\omega t) \cdots$$

[3]

If a sine function is squared, we obtain:

$$\sin^2(\omega t) = 0.5[1 - \cos(2\omega t)] \quad [4]$$

If the third power is formed, we find:

$$\sin^3(\omega t) = 0.75\sin(\omega t) - 0.25\sin(\omega t) \quad [5]$$

It can be seen from equations [3] to [5] that the values generated are always integral multiples of the basic frequency, i.e. 2ω or 3ω. This explains the harmonics in the spectrum.

Another important characteristic of harmonics is that their amplitudes increase in line with the input voltage. With this in mind, let us initially look only at the first term from equation [2]. In the logarithmic representation, we obtain

$$U_{OUT}\,[dBV\,] = A_1\,[dB\,] + U_{IN}\,[dBV\,] \quad [6]$$

The second term from [2] becomes

$$U_{OUT}\,[dBV\,] = A_2\,[dB\,] + 2 * U_{IN}\,[dBV\,] \quad [7]$$

For the third term, we obtain

$$U_{OUT}\,[dBV\,] = A_3\,[dB\,] + 3 * U_{IN}\,[dBV\,] \quad [8]$$

If the three equations, [6] to [8], are plotted on a logarithmic scale, we obtain three straight lines with varying gradients - see Fig 2.

A gradient of 1:1 applies for the linear part of the characteristic line, 2:1 for the square term, 3:1 for the cubic, etc. One important result of the mathematical analysis can be stated here:

- The harmonic oscillations arise at twice, three times and four times the sinusoidal oscillation frequency
- Their amplitudes increase on a logarithmic plot with the double, triple

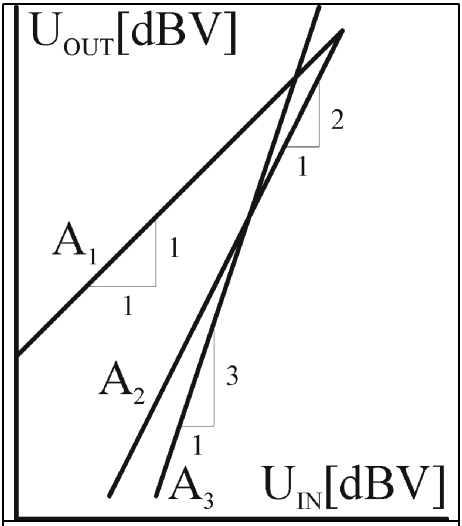

Fig 2: Logarithmic plot of equations [6] to [8].

and quadruple gradients.

We shall need these trends later, when we come to evaluate the spectra.

3. Total harmonic distortion

Total harmonic distortion (THD) is one of the oldest definitions of non-linearity. The equation for defining it is:

$$THD[\%] = \sqrt{\frac{U^2{}_2 + U^2{}_3 + U^2{}_4 + \cdots}{U^2{}_1 + U^2{}_2 + U^2{}_3 + U^2{}_4 + \cdots}}$$

[9]

We know that squared voltages, i.e. power levels, are added together. The total in the denominator includes all lines that are indicated in the output spectrum on the right in Fig 1. This corresponds to the actual power of the output signal. All harmonics, except for the fundamental, U_1, are represented in the numerator. So only the power of the harmonics is determined in this way. They alone are responsible for the distortions. When the roots have been worked out, THD describes the quotient of two voltages, which is normally expressed as a percentage.

4. Equipment for measuring total harmonic distortion

To measure the total harmonic distortion, we need a generator that produces a very pure sinusoidal oscillation. This is applied at the amplifier input as the signal source. The spectrum fractions of the output signal can be measured in various ways:

- Measurements using a spectrum analyser
- Measurements using an FFT analyser
- Measurements using filters and AC voltmeters

A spectrum analyser is basically an analogue measuring instrument that displays a voltage as a spectrum. Unfortunately, the price of such instruments is relatively high, so that they are beyond the means of most amateur radio enthusiasts.

An FFT analyser calculates the spectrum following the A/D conversion on a purely mathematical basis. Modern digital oscilloscopes usually also have a built-in FFT function. But this is of only limited use for measuring the total harmonic distortion, because the resolution of digital oscilloscopes - typically 8 or 10 bits - is simply not good enough for measurements of very good amplifiers.

The third measurement method can also be used with simple measuring instruments, provided you have high-quality

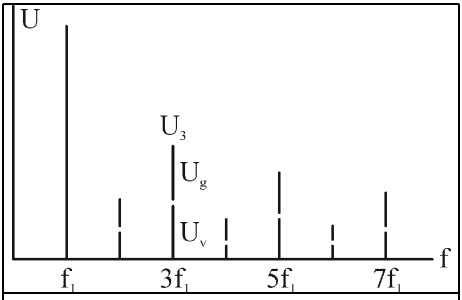

Fig 3: Output spectrum showing amplifier and generator elements.

filters available. A notch filter can be used to remove the fundamental from the spectrum. The residual voltage, which corresponds to the fraction from the harmonics, should be measured using a high-quality, wide-bandwidth AC voltmeter. Analogue instruments are often better than digital equipment for this purpose. For the audio range, there are also ready-made THD measuring instruments on the market. But a spectrum analyser is indispensable for higher frequencies. The total harmonic distortion is dependent on the output voltage and the frequency. So a complete description is not significant unless it is in the form of a group of curves.

5. Influence of sine generator

Generators that produce a perfect sinusoidal oscillation (in the mathematical sense) cannot be manufactured. Every oscillator generates harmonics. Unfortunately, these are also on the same frequencies that are generated by the nonlinear characteristics of the amplifier to be measured.

So the measurement result (see Fig 3 for the example of the third harmonic, U_3) contains a fraction, U_v, from the amplifier and a fraction, U_g, from the generator. This is true for all harmonics. But the two fractions cannot be separated by measurement. So it is not possible to measure the distortions of the amplifier in the strict sense. In order to keep errors of measurement small, we use generators with a very low total harmonic distortion. Such generators are available for audio purposes. For the radio-frequency range, we use another method of measurement.

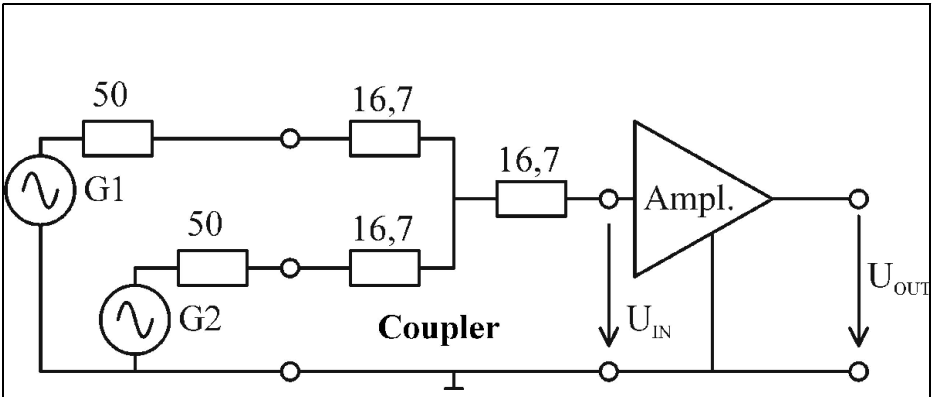

Fig 4: Measurement using the two tone method.

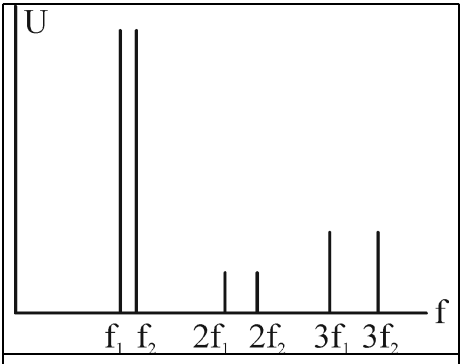

Fig 5: Spectrum showing outputs from two tone generator.

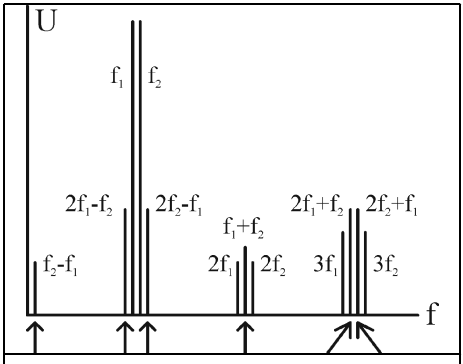

Fig 6: Spectrum at the output of the amplifier showing harmonics.

6. The intermodulation method

Instead of a single generator, we use two generators, G_1 and G_2, with slightly different frequencies, f_1 and f_2, which are fed to the amplifier's input through a coupler. The measuring rig can be seen in Fig 4. The total harmonic distortion of the generators has no influence on the measurement results.

The coupler consists of three star connected resistors suitable for radio-frequency work (each 16.7 Ohms). Thus there is an impedance of 50 Ohms at each terminal, provided that the generators and the amplifier are also adjusted to this value. The input voltage, U_{IN}, includes the sums of the two generator voltages and their harmonics. The associated spectrum, up to the third harmonic, can be seen in Fig 5.

This spectrum is now transferred to the output through the non-linear characteristic of the amplifier. We must forego any mathematical derivation here, and the result is represented directly as a spectrum, up to the third harmonic.

The spectrum (Fig 6) contains the two amplified input voltages at f_1 and f_2, together with a series of harmonic and non-harmonic lines. This effect is known as intermodulation. The harmonics are once again located at integral multipliers of the input frequencies, which here means $2f_1$, $3f_1$, $2f_2$, $3f_2$. They come from the generator *and* from the non-linearity of the characteristic line. They are therefore not suitable for an analysis. But there are lines that are caused exclusively by the amplifier's characteristic line. Arrows in Fig 6 identify these intermodulation products. We distinguish between close range interference and long range interference here.

The quadratic coefficient, A_2, in the characteristic equation [3] creates intermodulation products at f_{2-f1} and at f_{1+f2}. These lines are located at a significant distance from the two main lines, f_1 und f_2, in the spectrum, so we describe them as long range interference. The cubic coefficient, A_3, also creates long range interference at $2f_{1+f2}$ and $2f_{2+f1}$ and also close range interference at $2f_{1-f2}$ and at $2f_{2-f1}$.

Close range interference lies within the transmission band, while long range interference should be outside it. So the cubic terms should be seen as far more critical than the quadratic ones. Field effect transistors have a quadratic transmission characteristic consequently create only very slight close range interfer-

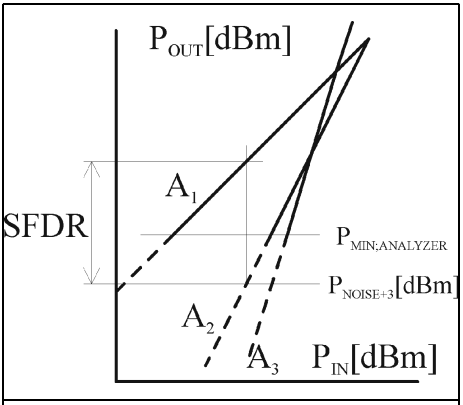

Fig 7: Measuring SFDR.

ence.

For analysis, there is a choice of lines. Thus, we can measure the quadratic distortions at f_{2-f1} or at f_{1+f2}. The result is identical. Even more choice is available in relation to the analysis of the cubic distortions.

7. Spurious Free Dynamic Range (SFDR)

This is an important criterion for describing an amplifier or converter. A dynamic range, by definition, has an upper limit and a lower limit.

Let us consider the output voltage of an amplifier. Its lower limit is defined as the point at which it has the same value as the noise voltage. A more conservative definition states that a signal is nonexistent unless it is least 3dB above the noise. This definition has been used as the basis of the following calculations. In the graphics and calculations below, the lower limit always appears as “noise + 3 dB”. The different definitions of the SFDR can make a numerical difference of approximately 2dB.

The upper limit is defined as the point at

$$U_{OUT,MIN}\ [dBV\ ] = U_{NOISE}\ [dBV\ ] + 3$$

which there is not a single harmonic exceeding the noise voltage + 3dB.

In Fig 7, we now have outputs depicted, instead of the voltages used up to now. This corresponds to the normal representation of readings on a spectrum analyser. However, Fig 7 would not differ in any way from a diagram showing voltages. It can be seen that, if the input voltage is increased (starting from zero), the fundamental frequency initially emerges from the noise with the amplification, A_1. This defines the lower limit of the dynamic range. If the input voltage is further increased, the next harmonic to appear is the second, A_2, followed by A_3. With the appearance of the first harmonics (i.e. in Fig 7 A_2), the spurious free dynamic range comes to an end. The SFDR can then be read off from the graph in dB's.

8. Problems in measuring the spectrum

Spectral lines (so-called "peaks") are visible only if they have a higher value than the noise background of the analyser, $P_{MIN;\ ANALYZER}$. This is primarily determined by the resolution bandwidth. The upper noise limit indicated in Fig 7, $P_{NOISE+3}$, is defined as the noise background of the amplifier, but not of the analyser. Since in very many cases the noise background of the analyser exceeds that of the amplifier, it is really not possible to measure the lower limit of the dynamic range directly. In Fig 7 the levels that cannot be measured are repre-

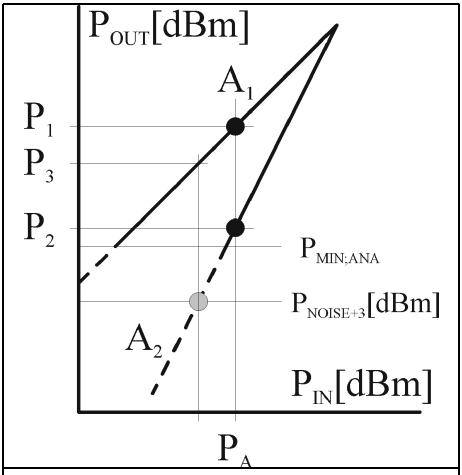

Fig 8: Extrapolating SFDR.

sented by a dotted line. If the noise power of the amplifier can not be measured directly using the analyser, either we must turn to other methods of measurement or we can calculate the noise power at the output using the bandwidth, B, of the amplifier, the amplification, V, and the noise factor, NF, which is assumed to be already known:

$$P_{NOISE+3}[dBm] = -171 + V[dB] + 10 * \log(B[Hz]) + NF[dB]$$

[10]

The next difficulty lies in the fact that it is usually also not possible to directly observe the emergence of the harmonics from the noise, because the analyser's noise level is too high. In this case, we can help ourselves by extrapolating the characteristic lines.

The procedure is clarified in Fig 8, initially only for the quadratic intermodulation products. At the input power, P_A, both the fundamental, P_1, and the second harmonic, P_2, can be measured at the output. But the deciding factor is the power P_3, because it defines the upper limit of the dynamic range. It is calculated as

$$P_3[dBm] = P_1[dBm] - \frac{P_2[dBm] - P_{NOISE+3}[dBm]}{2}$$

[11]

The procedure can also be applied in an analogous way to the cubical intermodulation products.

When specifying the measuring points, you should not select power levels that are too high. The essential rule is that at higher power levels more and more harmonics emerge from the upper noise limit, these arise in accordance with their ordinal number. Unfortunately, their frequencies sometimes lie precisely on the lines that are used for the evaluation of the second and third harmonics. We must therefore make sure that the measured harmonics have the correct gradient, namely 2:1 for quadratic intermodulation products and 3:1 for cubic intermodulation products.

9. Signal to Noise and Distortion (SINAD)

The signal to noise is generally used as the quality standard for a transmission system. The term is now expanded somewhat, in that we also add the distortions to the noise:

$$SINAD[dB] = P_{SIGN}[dBm] - (P_{NOISE} + P_{INTERMOD})[dBm]$$

[12]

The function initially increases as the output rises, because the signal increases and the noise remains constant. At higher power levels, the noise is then pushed into the background by the intermodulation products, so that the SINAD falls again.

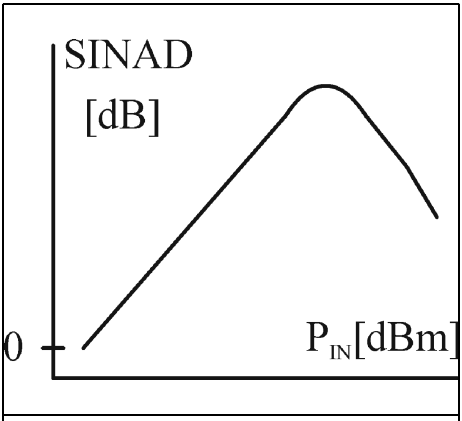

Fig 9: SINAD as a function of input.

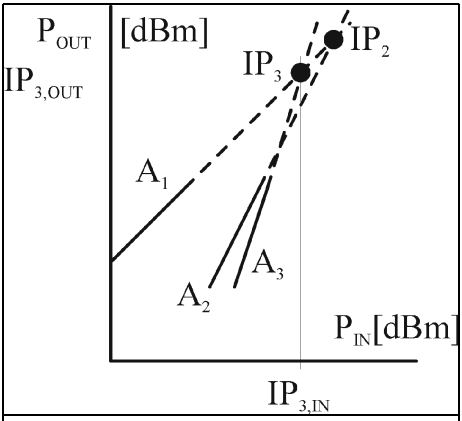

Fig 10: The intercept point.

10. Intercept Point (IP)

This refers to the virtual intercept points of lines in the diagram of the harmonics with the fundamental frequency. The inter-relationship is made clearer in Fig 10.

The logarithmic graph with the gradients of the fundamental frequency and the first two harmonics is already known from Fig 2. The intermodulation products are measurable in the range of the extended lines. At higher power levels, as already explained in Section 8, they are covered up by terms of a higher order. But the measurement curves can be extrapolated upwards (dotted lines). Intercept points then occur between the curves of the harmonics and the fundamental frequency. These are designated as IP_2, IP_3, IP_4 .etc.

The associated power level (or voltage) can be indicated (see Fig 10, which uses the example of IP_3) either at the input as $IP_{3,IN}$ or at the output as $IP_{3,OUT}$. Normally, as the level increases, IP_3 is reached first, before IP_2. So IP_3 represents the essential quality criterion. The intercept points lie far above the physically attainable levels. A numerical example: an amplifier with a maximum output of 10dBm can perfectly well display an IP_3 of 30dBm. The two standards, *SFDR* and *IP,* have the same value (from the pre-conditions). So one can be converted into the other:

$$SFDR[dB] = \frac{2}{3} * (IP_{3,IN} + 171 - 10\log B[Hz] - NF[dB])$$

[13]

11. Evaluation

All definitions presented previously register the non-linearity of amplifier characteristics. However, there are considerable differences as regards their usability.

SFDR describes the distortion-free range for a characteristic, starting from the noise level. The noise can be reduced through band restriction. Thus SFDR is also dependent on the user. It is well suited to the description of amplifiers that are operated at low levels (something like

distributing amplifiers or pre-amplifiers). In this way, all readings for the determination of the SFDR can be obtained at the lowest possible voltages. A/D and D/A converters are also best evaluated using SFDR.

The ***total harmonic distortion*** is usually defined at the rated power of a system. In principle, it takes in all harmonics. So it is a good evaluation criterion for the assessment of an amplifier at full power.

The ***intercept points*** describe the non-linearity at low power levels far below the operating limit, rather like SFDR. We are talking of virtual intercept points between the harmonics and the basic frequency. Don't be deceived by the big numbers. They don't say much about the power levels that an amplifier can actually achieve. In particular, it is not possible to show the level of the second and the third harmonics at medium and high power from the lines of the IP diagram. The readings for determining the intercept points are identical with those for the determination of the SFDR, but the noise is not taken into account.

SINAD is comparable to the familiar signal-to-noise ratio. It shows the maximum attainable interval between the signal and the combined complex of noise and intermodulation products. It is very well suited for the description of the maximum signal-interference at high power levels.

Alexander Meier, DG6RBP

Universal PLL oscillator module

This article describes a universal PLL oscillator module that generates a fixed frequency output signal between 2 and 7GHz, depending on the components used. The frequency is stabilised using a PLL. A micro-controller drives the PLL making the module independent so that can be used anywhere.

1. Introduction

There are numerous applications in measuring technology for fixed frequency oscillator modules. An example is a 4GHz local oscillator can be used with a mixer and a wideband 4 - 6GHz oscillator to mix down to a frequency range of 0.01 to 2GHz in a wobbler or synthesiser. Local oscillators can also be used in spectrum analysers to convert intermediate frequencies.

The universal oscillator module presented here consists of a tunable oscillator (VCO) with an output amplifier, a PLL circuit for frequency stabilisation, a quartz oscillator as reference and a micro-controller to drive the PLL.

Hittite [1] has numerous favourably priced VCO's in it's catalogue, ranging from 2 through to more than 7GHz, nearly all of which, thanks to standard housings and pin configuration, can be mounted interchangeably on the printed circuit board. In addition, due to the maximum input frequency of the ADF4107 PLL from Analog Devices [2], the module can be used to generate fixed frequencies of from 2 to 7GHz. A 20MHz quartz oscillator is used as reference frequency. A PLL oscillator module can be created at a lower cost than LO assemblies based on the multiplier principle.

2. Circuit description

Fig 1 shows the circuit diagram of the oscillator assembly. As an example, a circuit for an HMC 391 VCO is discussed here. This can be tuned from 3.9GHz to 4.45GHz. But in practice VCO's can be used slightly above or below the specified frequency limits.

The 6dB splitter, consisting of R10 to R12, splits the output signal (approximately +1 to +5dBm) of the MMIC VCO (U3) from Hittite. Part of

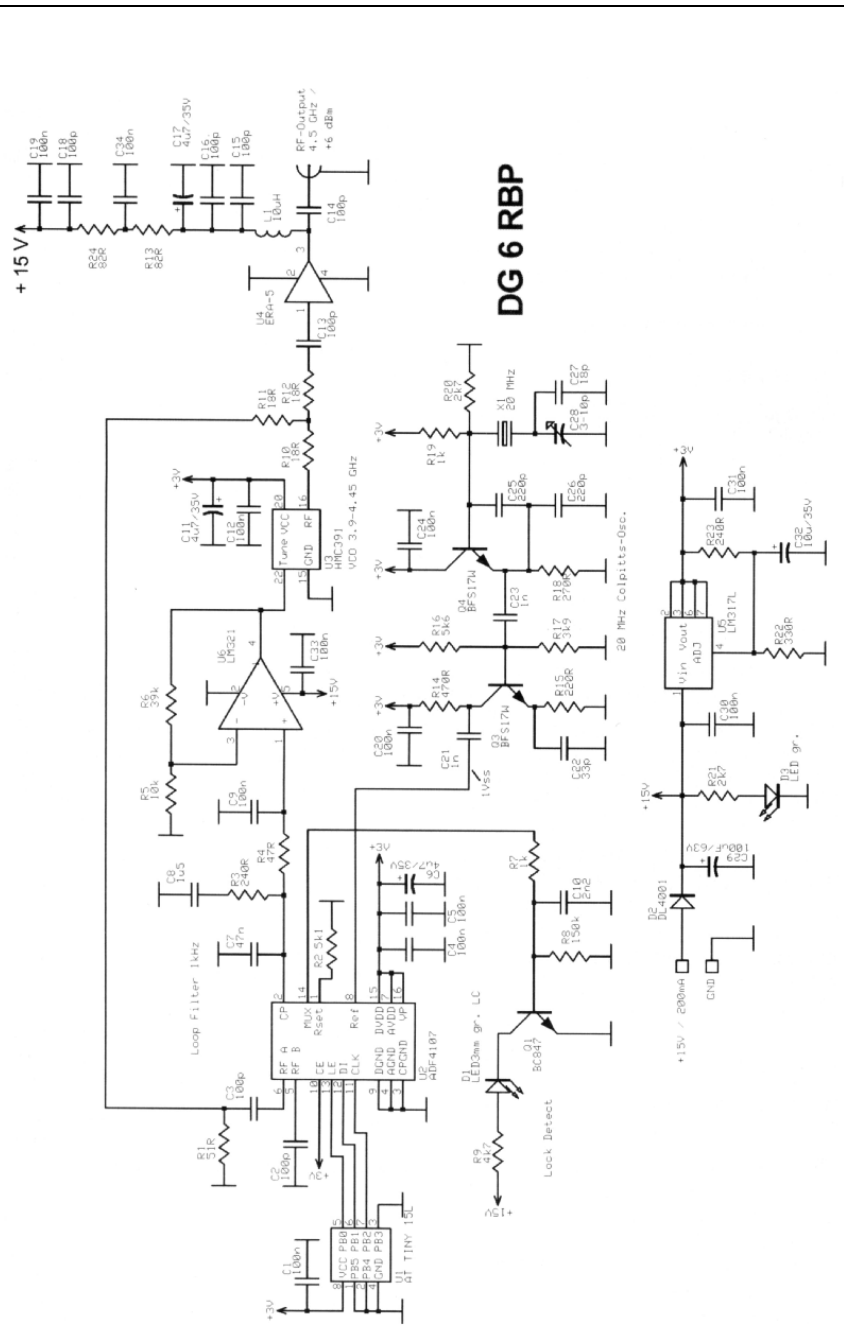

Fig 1: Circuit diagram of the universal pll oscillator.

the VCO output signal is amplified by approximately 10dB using an MMIC broadband amplifier (Gain Block U4), and is fed out as the output signal. The operating voltage is fed to the broadband amplifier through an inductance (L1) and the resistors (R13 and R24).

The second part of the VCO output signal is fed to the PLL (U2). The minimum input power required for the PLL depends on the frequency. According to the data sheet [2], it should be at least -5dBm. But normally the PLL is satisfied with far less.

The resistance, R2, determines the maximum current from the charge pump (pin 2). The four pole loop filter is connected to pin 2 and consists of C7 to C9, R3 and R4. The limiting frequency has been fixed at 1kHz with a 45° phase shift. The most convenient way to determine these values is with the help of the "ADI Sim PLL" PLL simulation software. The software can be obtained free of charge from Analog Devices [3].

A voltage of approximately 0 to 3V is generated at pin 1 of the operational amplifier (U6), which is proportional to the frequency deviation. This voltage is amplified by U6, so that the VCO can be tuned over its tuning range (V_{Tune}) from 0 to 10V.

After switch on, the PLL is programmed in a single operation, using the Atmel micro-controller AT Tiny 15L [4]. The module can thus be used independently, since the PLL does not have to be externally driven. The advantages of this micro-controller, apart from the compact construction (SMD housing, 8 pins), are the integrated oscillator and reset generator, which considerably simplify the external wiring. The software for the PLL has been programmed in Assembler and is stored in the controller's non-volatile memory. LED (D1) signals that the PLL is correctly locked.

The 20MHz reference oscillator consists of a simple Colpitts circuit (Q4). The exact frequency of the quartz oscillator can be tuned with a trimming capacitor (C28). The quartz oscillator is followed by an amplifier stage (Q3) to raise the voltage of the reference signal to approximately $1V_{ss}$.

The power supply required for the module is 15V (±5%). The circuit is protected against battery reversal with a diode (D2). An adjustable voltage regulator (U5) generates the supply voltage required for the VCO and the PLL (3V). Only the broadband amplifier is powered directly from the 15V supply voltage.

3. Alterations for other output frequencies

The following steps must be taken to alter the oscillator module for another output frequency:

1. Select a suitable VCO from Table 1. The corresponding data sheets can be found on the website of the manufacturer [1].

2. For an output frequency exceeding 4.5GHz, you are recommended to use different broadband amplifier, e.g. the ERA-2. The multiplier resistors R13 and R24 should be altered in this (R13, R24: 150 Ohms for ERA-2).

3. Change the software in the micro-controller (U1) for the desired output frequency.

4. The loop filter should be checked for the desired VCO and optimised, if required. Simulation software should be used for this [3].

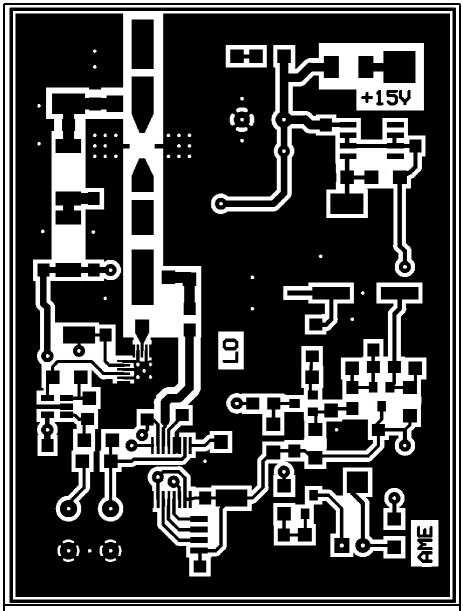

Fig 2: Bottom side of PCB for universal pll oscillator

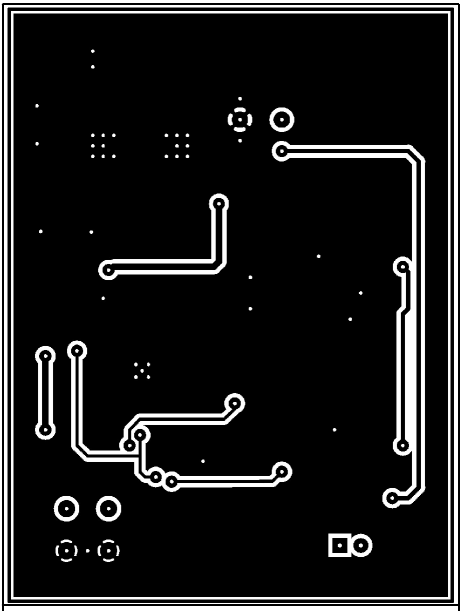

Fig 3: Top side of PCB for universal pll oscillator.

4. Assembly

The layout for the 71mm x 53mm printed circuit board is shown in Fig 2 & 3, and the component layout in Fig 4. The earth surfaces underneath the VCO and for the broadband amplifier must be made using through plating. We must advise against the use of self-etched printed circuit boards using compression rivets here!

To assemble the PLL oscillator assembly successfully, unfortunately expensive soldering equipment for the VCO is required. The tiny VCO is located in a housing measuring just 4 x 4mm with no connecting wires! The connection to the printed circuit board is provided through small soldering surfaces on the underside (!) of the component. These housings are being used more often for RF components because their RF characteristics are better. To mount the components, use a stencil to put some solder paste on the printed circuit board. Position the component and melt it on using hot air or (even better) a Reflow soldering unit. Unfortunately, it is just not possible to use a soldering iron. The VCO mounted on the printed circuit board can be seen in Fig 5.

Table 1: Hittite range of VCOs

VCO	Frequency in GHz	Output in dBm
HMC 384	2.05 - 2.25	3.5
HMC 385	2.25 - 2.5	4.5
HMC 386	2.6 - 2.8	5
HMC 388	3.15 - 3.4	4.9
HMC 389	3.35 - 3.55	4.7
HMC 390	3.55 - 3.90	4.7
HMC 391	3.9 - 4.45	5
HMC 429	4.45	4
HMC 430	5.0 - 5.5	2
HMC 431	5.5 - 6.1	2
HMC 466	6.1 - 6.72	4.5
HMC 505	6.8 - 7.4	11

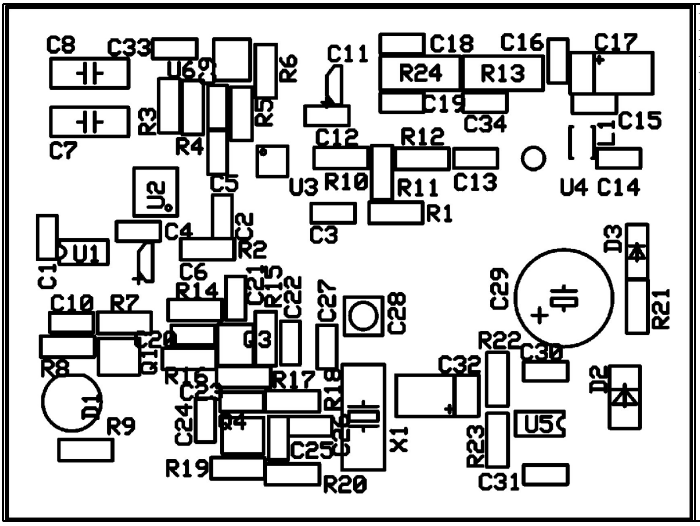

Fig 4: Component layout of universal pll oscillator.

Once the VCO has been mounted, the PLL (U2) is next. Like all other SMD components, this one can still be soldered, using a soldering iron with a fine tip, although the Reflow soldering process can be used. Then all the other components are mounted, in no particular order.

A fully assembled module can be seen in Fig 6. *Andy: It is revision 0 of this project, Alexander is working on revision 1 that will be available soon. The improvements included in rev. 1 will* be:

- *An external Reference can be used*
- *Less noise due to a better low noise op-amp*
- *Less noise due to a better power supply*
- *More power due to a gain block in sot-89 case*
- *Much cleaner spectrum due to improved pcb layout*
- *ISP Programming of the µController*
- *The pll oscillator can be controlled optionally by a external controller circuit.*

Revision 1 will be included in the new RSGB book - Microwave Projects 2 - that I am editing, due out in late 2005.

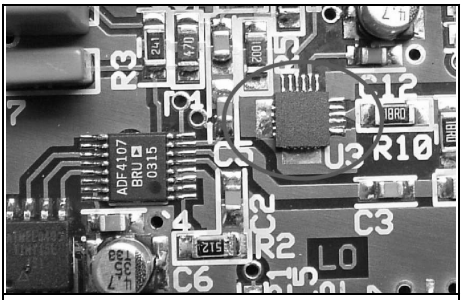

Fig 5: The VCO is small (4 x 4mm).

5. Parts list

R10-R12	18 Ohms, 1206
R4	47 Ohms, 1206
R1	51 Ohms, 1206
R13, R24	82 Ohms, 2512 (see Text)
R3, R15, R23	240 Ohms, 1206
R18	270 Ohms, 1206
R22	330 Ohms, 1206
R14	470 Ohms, 1206
R7, R19	1 kOhms, 1206

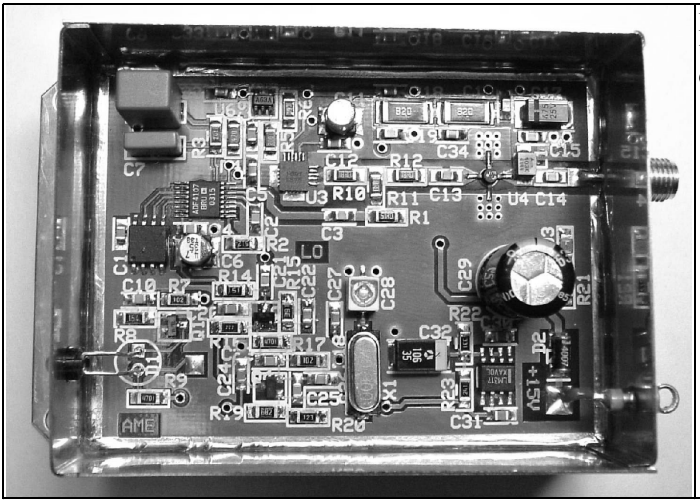

Fig 6: Completed universal pll oscillator.

R20, R21	2.7 kOhms, 1206
R17	3.9 kOhms, 1206
R9	4.7 kOhms, 1206
R2	5.1 kOhms, 1206
R16	5.6 kOhms, 1206
R5	10 kOhms, 1206
R6	39 kOhms, 1206
R8	150 kOhms, 1206
C27	18pF, 0805
C22	33pF, 0805
C2, C3, C13-C16, C18	100pF, 0805
C25, C26	220pF, 0805
C21, C23	1nF, 0805
C10	2.2nF, 0805
C7	47nF, MKS-2-5
C1,C4,C5,C9,C12, C19,C20,C24,C30, C31,C33,C34	100nF 0805
C8	1.5µF, MKS-2-5
C6, C11, C17	4.7µF / 35V, SMD Electrolytic capacitor
C32	10µF / 35V, SMD Tantalum
C29	100µF / 63V, Electrolytic capacitor
C18	3-10pF Trimmer, SMD
C35	Feedthrough capacitor, 1nF
L1	10µH SIMID 1210
D1	LED 3mm green
D2	DL4001
D3	LED green, 1206
Q1	BC 847C
Q3, Q4	BFS 17W
X1	20MHz, HC49 SMD, CL = 16 pf
U1	AT Tiny 15L, SMD, programmed
U2	AD4107, BRU
U3	VCO, seeTable 1
U4	ERA-5 (see Text)
U5	LM 317L, SMD
U6	LM 321, SMD
1	2 hole SMA flanged bush
1	DG6RBP PLL oscillator PCB
1	55 x 74 x 30mm tinplate housing

6. Calibration

Once the unit has been fully assembled, a functional test should take place. The module's output is connected to a spectrum analyser and the supply voltage is applied. The current consumption of the module should be approximately 150mA. The LED (D1) should light immediately

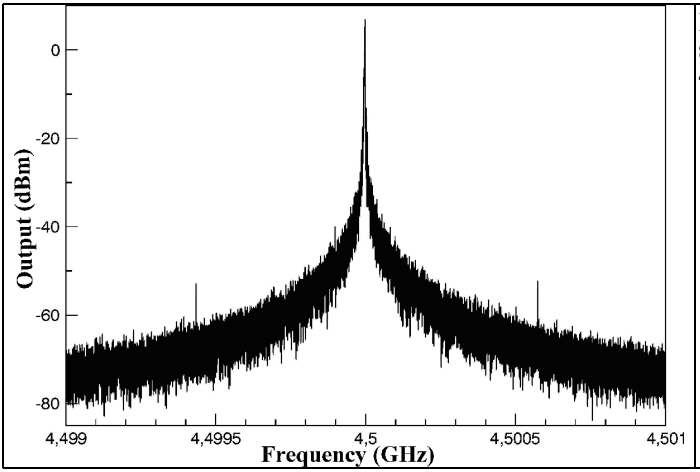

Fig 7: The output spectrum at 4.5GHz.

showing that the signal from the PLL is locked. A corresponding signal at the programmed output frequency can be measured using the spectrum analyser. Depending on the components (VCO, broadband amplifier), the output power will be approximately +5 to +10dBm.

Finally, connect the module to a frequency counter. The precise adjustment of the output frequency requires the use of the trimming capacitor (C28). If applicable, the capacitor (C27) can be adjusted a little towards the coarse setting for this purpose. The oscillator module is now ready for operation.

7. Measurements

The LO module used for the measurements was built in accordance with the circuit diagram (Fig 1) and programmed for an output frequency of 4.5GHz. The output spectrum is shown in Fig 7. Spurious readings are suppressed by approximately 60dB. The second harmonic is suppressed by approximately 20dB. There is an option for suppressing harmonics even further, using an additional low-pass filter. For example, the low-pass filters in the VLF series (Fig 8) from Mini-Circuits [5], are very suitable for this work, being very small, favourably priced and fitted with SMA connectors.

The phase jitter measurement can be seen in Fig 9. It is composed of elements from the VCO, the PLL, the loop filter, the reference frequency and the voltage supply! Above the limiting frequency of the loop filter (1kHz), the phase jitter from the VCO and the associated operational voltage is dominant. The phase jitter results for the oscillator module are certainly inferior to those for a multiplier LO, but they are more than sufficient for many applications in measuring technology but not for transverters!

Fig 8: VLF low pass filter from Mini Circuits.

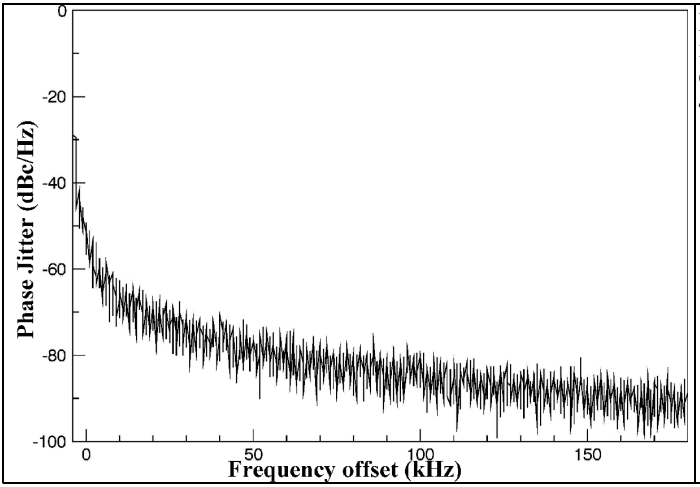

Fig 9: Phase jitter measurement of oscillator at 4.5GHz.

8. Literature

[1] Hittite Microwave Corporation, 20 Alpha Rd., Chelmsford, MA 01824, USA, www.hittite.com

[2] ADF4107 data sheet, Analog Devices, One Technology Way, Norwood, MA 02062-9106, USA

[3] ADI SimPLL, Analog Devices, Download from www.analog.com

[4] AT Tiny 15L data sheet, Atmel Corporation, 2325 Orchard Parkway, San Jose, CA 95131, USA

[5] VLF series low-pass filters, Mini-Circuits, Brooklyn, NY 11235, USA

Gunthard Kraus, DG8GB

Practical project: Stripline low pass filters for various frequency ranges

Part 2, continued from issue 1/2005

3.6

A 110MHz n=7 low pass filter

When something works too well, people get cocky. And that's why the next project had to be a 110MHz low-pass filter with a considerably steeper transition from the pass band to the stop band. Such a characteristic is very useful, especially to suppress the total harmonic distortion in signal generators or to improve the suppression of the image frequency suppression in receivers. But this should not increase the ripple effect in the pass band, the maximum ripple should not exceed 0.1dB. It would also be nice if the reductions of attenuation in the stop band above 1GHz could be reduced or eliminated.

Naturally, the filter program was used again, 3 inductors and 4 capacitors were needed for the basic circuit, with a degree of filtration of n = 7. This can still easily be accommodated in the standard aluminium housing. The calculated result from “fds” can be seen in Fig 23 and the designing of a new printed circuit board in Fig 24. I haven't included a photo of the completed filter, since only one coil and an SMD capacitor were used at this stage.

A simulation was carried out for all new components: a coil, a capacitor, two 4mm long 50Ω striplines, and two additional open-end extensions. These are the starting point for working with PUFF that can easily be recognised in Fig 25.

One rather unpleasant factor is the fact that at 100nH the inductors required still deviate markedly from their specification. As indicated by a brief simulation, naively using such 100nH coils leads immediately to a ripple effect exceeding 0.5dB in the pass band (The demands on the precision of components simply increase in line with the degree of filtration; try it out yourself, please do!). So adjustable inductors, available from NEOSID, were chosen. These have cap cores for frequencies of up to 200MHz. Their base is 7.5mm x 7.5mm and the housing is 10mm high so they can be fitted into the aluminium housing vertically or horizontally. An additional advantage, the very small windings should give a markedly higher self-resonant frequency, compared with the larger helical coils from the previous design.

With a coil Q of 100 (taken from the data sheet, and corresponding to a series resistor of approximately 0.7 at 100MHz), the simulation using PUFF generates the curve shown in Fig 26 (following a slight correction to the values - please compare component list F3 with the simulation

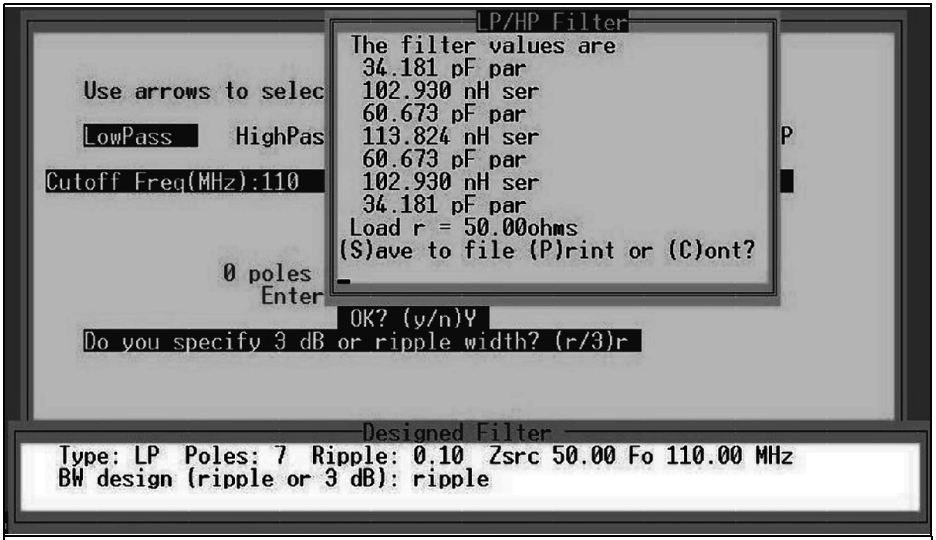

Fig 23: Filter components calculated by "fds".

result as per Fig 25!). The increasing attenuation at higher frequencies compared with the fifth order low pass filter (due to the greater number of components) can easily be seen. But this becomes really interesting with a display extended to cover 0 to -50dB (Fig 27), for in comparison with Fig 6 from Part 1 we can clearly recognise in the new design the higher number of peaks in S11 in the pass band, and the much steeper rise in attenuation of S21 in the stop band. At any rate, the gain in attenuation is a big fat 20dB at 200MHz!

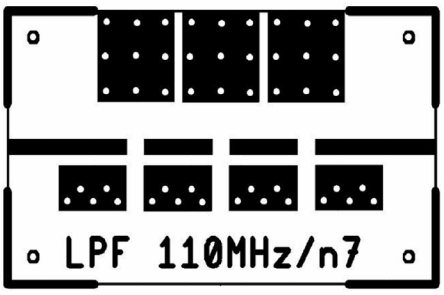

Fig 24: New PCB layout for the 110MHz filter.

Following the somewhat expensive prototype assembly, it was naturally exciting to see whether the prototype would behave in the way that might have been expected, based on the simulation. The end result (following quite a few attempts at calibration and a lot of frowning) can be seen in Fig 28. In fact, the choice was restricted to the following three options:

- Either the ripple was correct at low frequencies, but then it was excessive in the higher range...
- it was correct at high frequencies, but then it was too high at low frequencies
- the ripple was basically the same at any frequency, but clearly exceeded the limits laid down by the calculation.

Where did the error lie? Even unsoldering all the capacitors used and checking the measurements of the capacitances did not indicate any error in the mounting of the components. Well, everything became clear in the end, but it wasn't

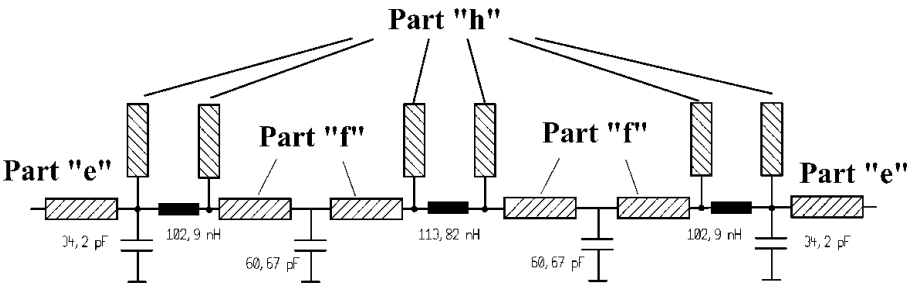

Fig 25: The start point for a PUFF simulation of the 110MHz n=7 low pass filter.

Part "e": Microstrip 50Ω / 14mm long, 1.83mm wide
Part "f": Microstrip 50Ω / 4mm long, 1.83mm wide
Part "h": Oneport "fr-50.s1p" (Open end extension for 50Ω microstrip)

exactly easy getting at the truth:

The permeability of the cap cores used is dependent on the frequency and decreases as the frequency increases. Consequently, either the inductance is correct between 80 and 100MHz but is then excessive at low frequencies, or we retune and then it is correct at low frequencies but it is too low at 100MHz. Such a sensitive little filter reacts to these relatively small discrepancies immediately. With hindsight it all seems very logical, but we have to find the error first!

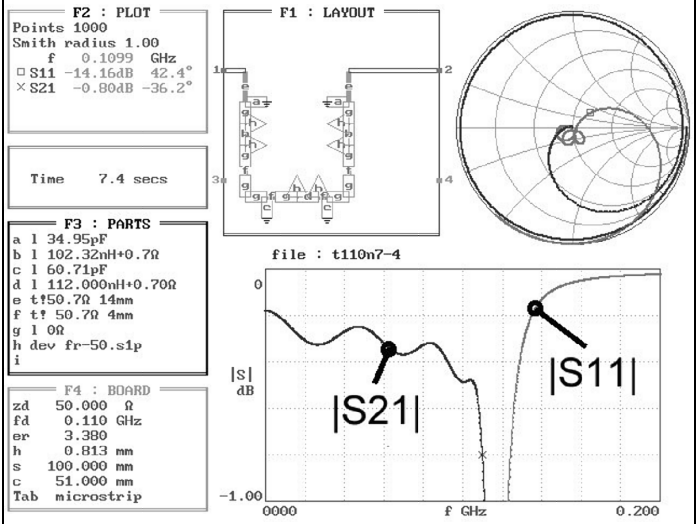

Fig 26: PUFF simulation results for the 110MHz filter. Slight adjustments in values from circuit in Fig 25.

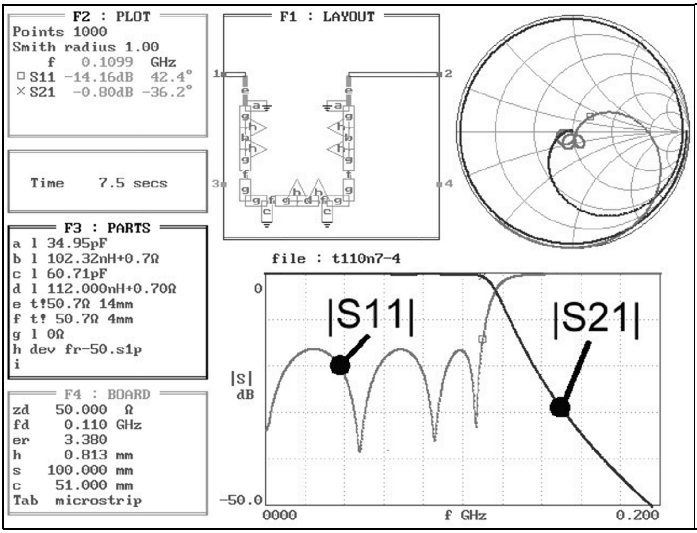

Fig 27: PUFF simulation results for 110MHz filter with range increase to -50dB. This clearly shows the maxima of |S11|.

In contrast, the effects of the improved attenuation constituted a pleasant surprise. Fig 29 shows that the markedly smaller coils do display much lower self-capacitance and thus there are hardly any problems until we exceed approximately

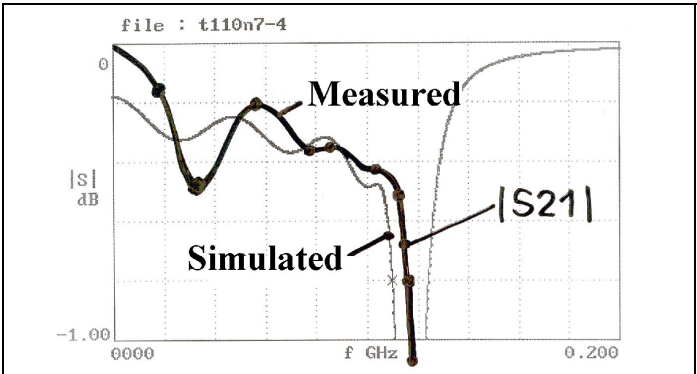

Fig 28: Measured results for 110MHz filter showing the best compromise in calibration.

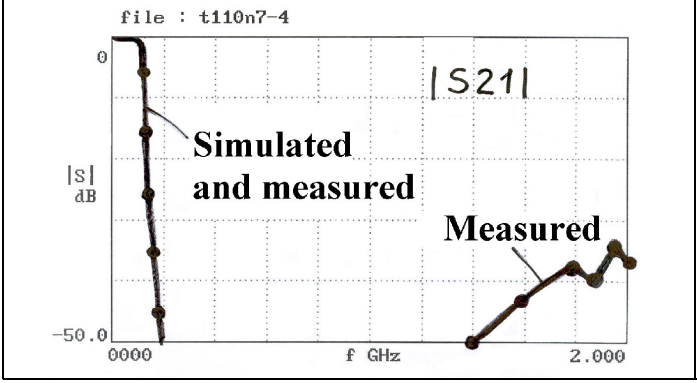

Fig 29: Measured results for 110MHz filter showing improvements in stop band due to use of smaller inductors.

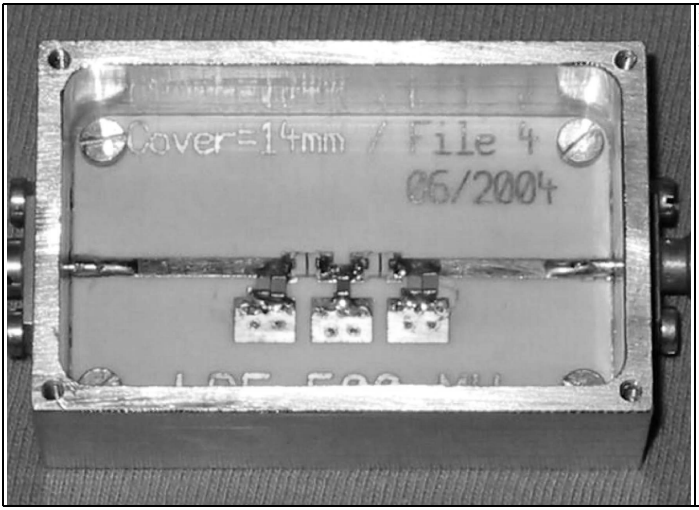

Fig 30: Picture of the version 1 500MHz filter using all SMD components.

1.8GHz. For a 110MHz low pass filter, that's decidedly satisfactory!

4.
Low pass filters for a cut-off frequency of 500MHz

A few preliminary comments are necessary before we begin:

For some reason, 500MHz is a difficult frequency for filter assembly. Pure stripline filters are fascinating, because once the development work is over there are no problems with copying or the precision of reproduction. Though at 500MHz the dimensions for corresponding striplines are still decidedly large, while discrete components are already slowly pushing up against their limits. The capacitors can be realised using SMD technology, but the values required fall and the discrepancies between the values and

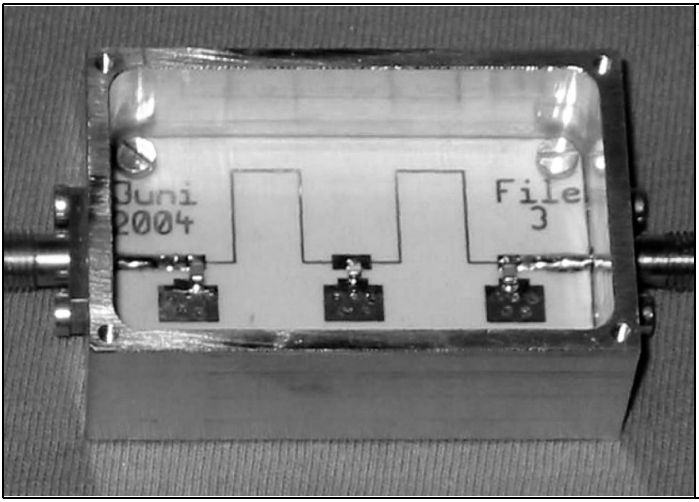

Fig 31: Picture the version 2 500MHz filter using SMD capacitors and stripline inductors.

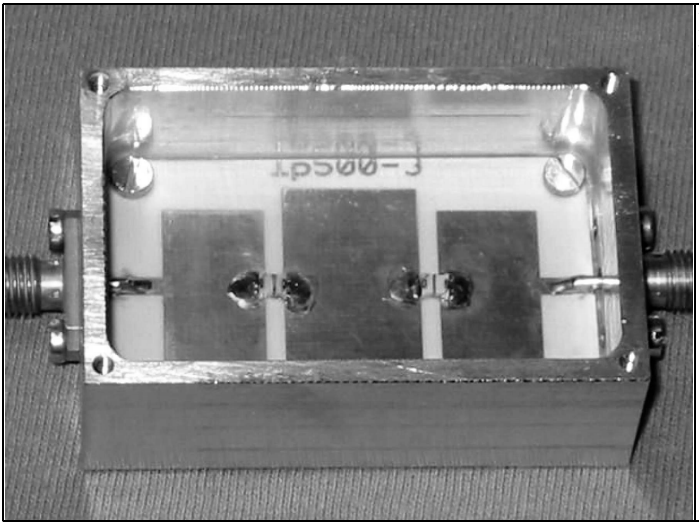

Fig 32: Picture of the version 3 500MHz filter using stripline capacitors and SMD inductors.

the standard series are significant. It's a similar story for the inductors; SMD fixed inductances display unpleasant tolerance values and/or falling levels of quality, and can no longer be kept within the limits required by the simulation. Also the use of adjustable designs looks decidedly bleak.

In order to get a feel for what was possible here, several different combinations were investigated and the pros and cons of each individual solution were estimated:

- Version 1, which uses SMD components for both the inductors and the capacitors, it can be seen in Fig 30.

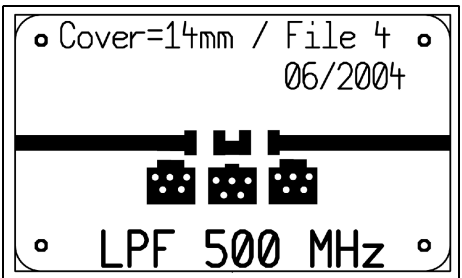

Fig 33: PCB layout for the version 1 500MHz filter.

- Version 2 combines SMD capacitors with printed stripline inductors it can be seen in Fig 31.
- Version 3: printed stripline capacitors in combination with SMD inductors are used in Fig 32.

4.1 500MHz n=5 low pass filter, version 1 with SMD components

First the component values are determined, using the "fds" filter program, with the filter data remaining unchanged right up to the cut-off frequency:

C1 = C3 = 7.3pF
C2 = 12.57pF
L1 = L2 = 21.8 nH

Naturally, we have to have a new board layout, since at the higher frequencies the connecting striplines between the individual components must be kept as short as possible, and precisely matching SMD pads must be used (Fig. 33). The associated simulation circuit, tailor-made for PUFF, can be seen in Fig 34. The open-end extensions for the SMD inductor pads were generated with the student version of APLAC as a S1P file (fr-2p83.s1p) and simply copied into the current PUFF file. (This procedure is

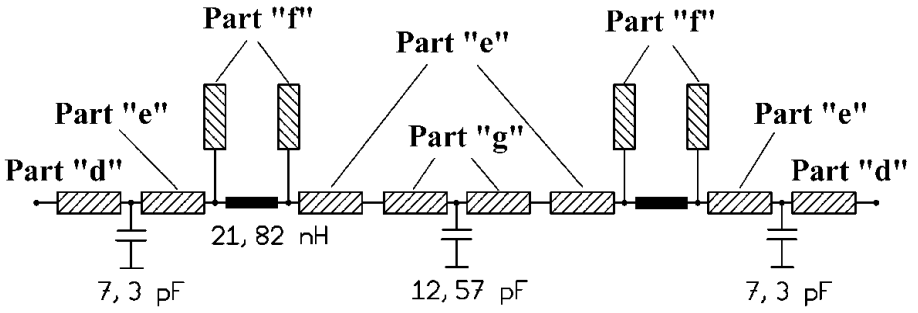

Fig 34: Circuit diagram of the version 1 500MHz filter used for PUFF simulation.

Part "d" Microstrip 50Ω / 19mm long, 1.83mm wide
Part "e" SMD microstrip pad 38.4Ω / 1.5mm long, 2.83mm wide
Part "f" Open end extension for SMD pad (Oneport "fr-2p83.s1p")
Part "g" Microstrip 50Ω / 1mm long, 1.83mm wide

described in Section 3.2 / Page 21 of Part 1 of this article in issue 1/2005).

A new conductor width of 2.83mm is required for the inductor pads on the printed circuit board and can be entered directly, using APLAC, into the attributes of the open stripline (component Mloc1). With PUFF, things aren't like that, so the characteristic line impedance associated with this width of SMD inductor pads was first determined as 38.4Ω. In actual fact, the line transition from 50Ω to 38.4Ω has to be taken into account four times to complete the circuit. The two conductor widths are not far apart, ignoring it at low frequencies would not cause a problem, but this no

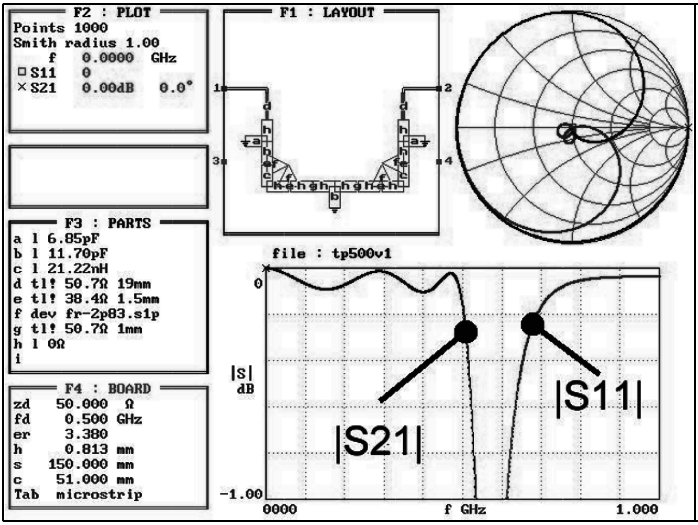

Fig 35: PUFF simulation of the version 1 500MHz filter.

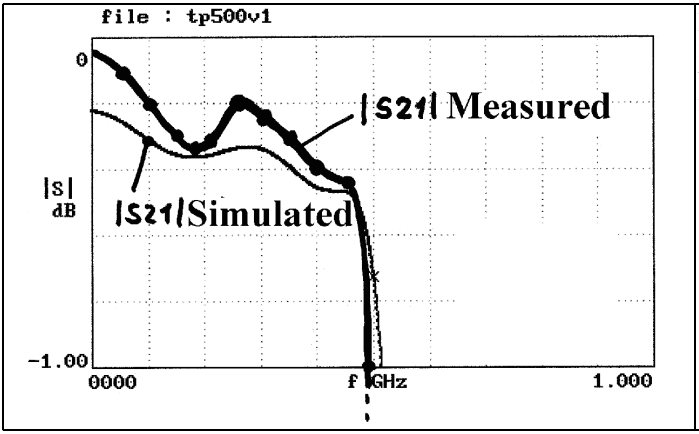

Fig 36: Measured results for the version 1 500MHz filter.

longer applies above 1GHz!

A trial comparison simulation using a full version of APLAC including all the participating effects showed that there is not that much of an influence on the result, therefore this factor need not be incorporated into the simulation.

At the start, when PUFF is used we suddenly receive an error message stating that the memory allocated is too small for such a big circuit with so many additional files. So there's only one thing left to do: Right click on the PUFF icon on the Windows screen and call up "Memory" in the properties menu. It is not until all the memory defaults have been set to the highest possible value (usually: 16,384 kilobytes) that this effect can be safely be said to have been eliminated. But this causes a longer loading time for the program and occasionally with longer simulation times.

Once this hurdle has been cleared, we move to optimisation. All influences from the pads, the connecting lines and the open-end extensions must be corrected through variations in the capacitors and inductors. If we compare the F3 components list of the end result shown in Fig 35 with the starting point of Fig 34, we can clearly see the differences.

The measurement using the fully assem-

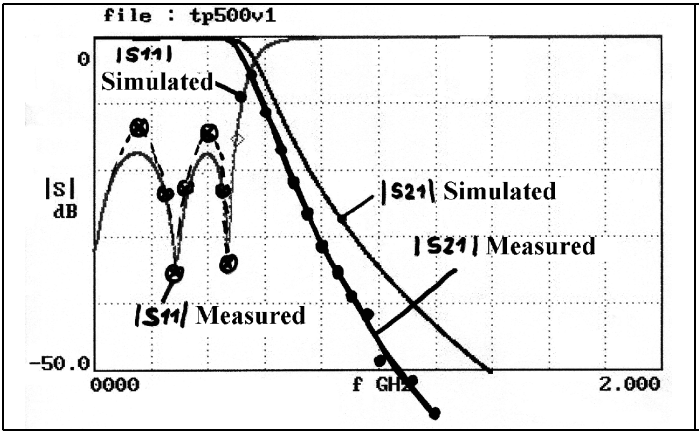

Fig 37: Measurement of the performance for the version 1 500MHz filter up to 2GHz. It shows the higher ripple in the pass band.

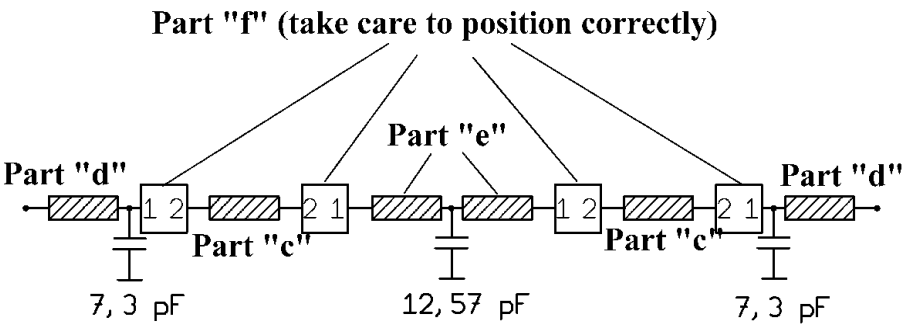

Fig 38: Circuit diagram of the version 2 500MHz filter used for PUFF simulation.

Part "c" Microstrip 120Ω / 32.7mm long, 0.25mm wide
Part "d" Microstrip 50Ω / 10mm long, 1.83mm wide
Part "e" Microstrip 50Ω / 2mm long, 1.83mm wide
Part "f" Twoport "st50-120.s2p" (transition from the 1.83mm wide 50Ω feeder to the 0.25mm narrow "inductor line" and vice versa).

bled prototype is really fascinating. Fig 36 shows the result for the pass band. The simulated curve is calculated for a series resistor of 1.3Ω in the inductors (corresponding to a quality of 50 to 500MHz). We can clearly see that the circuit reacts very sensitively to the fact that two SMD inductors have a standard value of 22nH, instead of the simulation value of 21.2nH - the cut-off frequency has actually slipped down by several percentage points and the Chebyschev ripple is bigger. Apart from the S21 curve at very low frequencies (where a lower inductor loss resistance is effective, but this cannot be simulated, except at great expense...), the correlation of theory and practice is still reassuring.

Finally, the display range was expanded to 0 to -50dB, so that both the S11 curve in the pass band and the attenuation behaviour up to 2GHz can be represented (Fig 37). It can very clearly be recognised that the higher ripple in the pass band is directly inter-related to a less satisfactory S11 value, i.e. higher reflection. Secondly, this higher ripple value once again leads to a steeper attenuation rise in the stop band. A brief test at 4GHz showed there was still 50dB attenuation, and that was satisfactory. These measurements were again carried out using the aged HP8410 network analyser. Two additional measurements had to be taken:

- A broadband directional coupler was connected in between the sweeper output and the network analyser input with a 10dB attenuation. Its output signal powered a microwave frequency counter. The sweeper was switched to manual and deliberately set to specific frequencies one after the other (as per the counter display). The current S11 and/or S21 value can be easily read off from the screen with the maximum sensitivity that can be selected on the network analyser being 0.25dB per division.
- The precision of measurement was increased by making an initial short circuit measurement without a filter in the frequency range between 100MHz and 2GHz. The inaccuracies

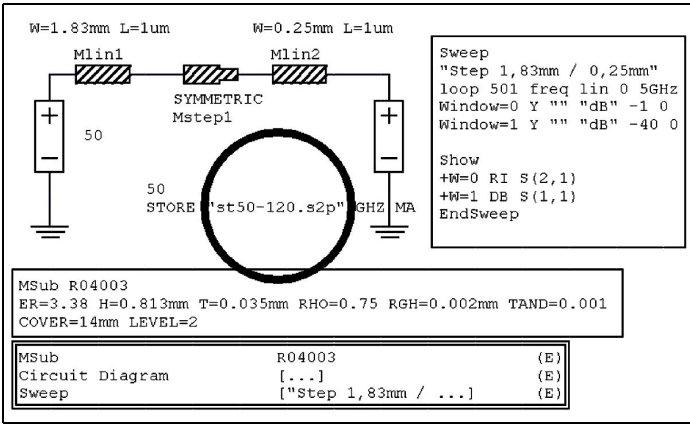

Fig 39: Using the free version of APLAC to simulate the step transitions.

of the measurement equipment were carefully entered in a table (for your information: from 100MHz to 500MHz, the maximum error at S21 was 0.25dB and even up to 1GHz it was still less than 1dB, not bad really for a measuring instrument of this age!). The measurement was then repeated with the low pass filter in the signal path. When the error had been manually corrected, the diagrams in Fig. 36 and Fig. 37 were plotted.

Here we can see again that successful results using such microwave developments do not depend entirely on having extremely modern but enormously expensive set of measuring instruments!

4.2. 500MHz n=5 low pass filter, version 2 with SMD capacitors and stripline inductors

The problem with the standard values of

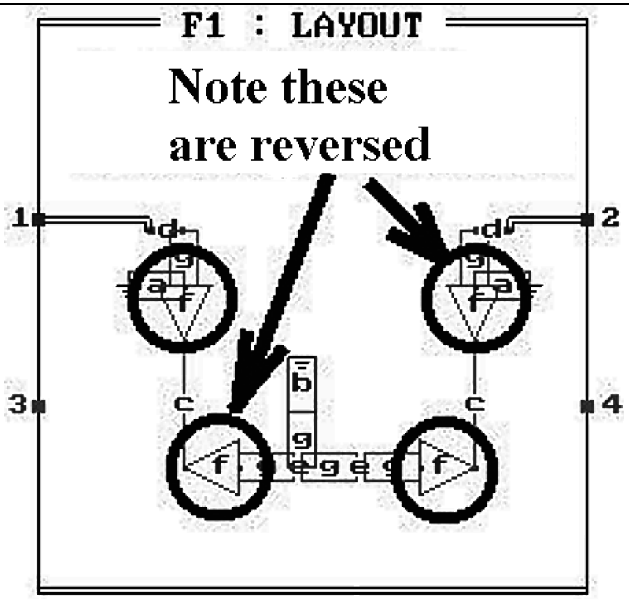

Fig 40: Position of the four part "f" components.

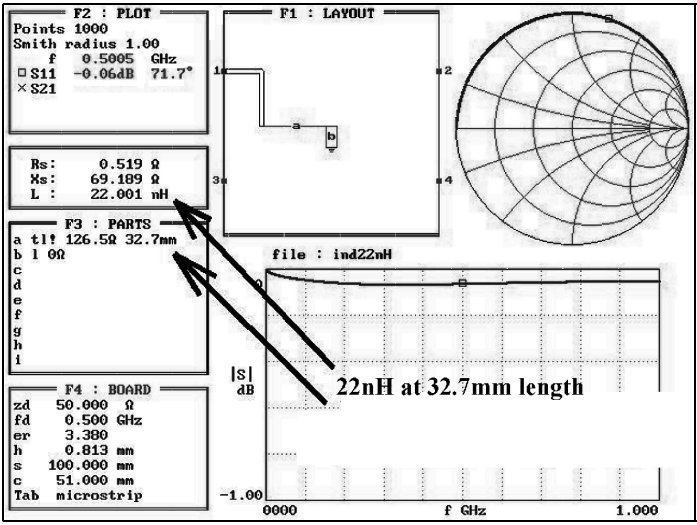

Fig 41: Result of PUFF simulation to find the length of line required for a 22nH inductor.

the SMD inductors, which do not match the requirements, was simply giving us no rest. So we contemplated thin striplines with a characteristic impedance of 120Ω as a replacement (width = 0.25mm). There were predictable disadvantages in the filter stop band (as the frequency increases, the attenuation rises only to a precisely predictable maximum and then falls again to almost zero when the "inductor line length" is in the order of λ/4), but the advantages in the pass band are even so very attractive:

- Precise repeatability for copying
- Precise fine calibration of the inductors is possible, following several drafts with different line lengths
- The quality that can be expected is rather higher than that for SMD inductors
- As a result, pre-set maximum ripple values can be maintained in the pass band, with very precise correlation of the simulation and the prototype.

Now PUFF comes back into the game. The starting circuit used for the PUFF simulation can be seen in Fig 38. In addition to the thin striplines, it also to contains four "steps" (transition from the 1.83mm wide 50Ω feeder to the 0.25mm narrow "inductor line" and vice versa). They were set up as per Fig 39, once again using the free student version of APLAC, and there is something else we should clarify here:

- The line lengths of the two lines in contact have been selected to be so short (1 micron each) that their influence on the result can be disregarded.
- The simulation result for zero to 5GHz was stored as an S-parameter file, with the appropriate attribute entry, at the right hand port (STORE "st50- 120.s2p" GHZ MA) and then copied into the current PUFF file.
- Great care must now be taken in setting up the PUFF circuit in field F1, since the order of the S-parameter files of the steps is a significant factor. The reason for this is very simple: its replacement circuit represents a simple LC low pass filter with only 2 components, and so it is important that the replacement capacitor always points to the wide 50Ω feed and the replacement inductance points to the narrow "120Ω

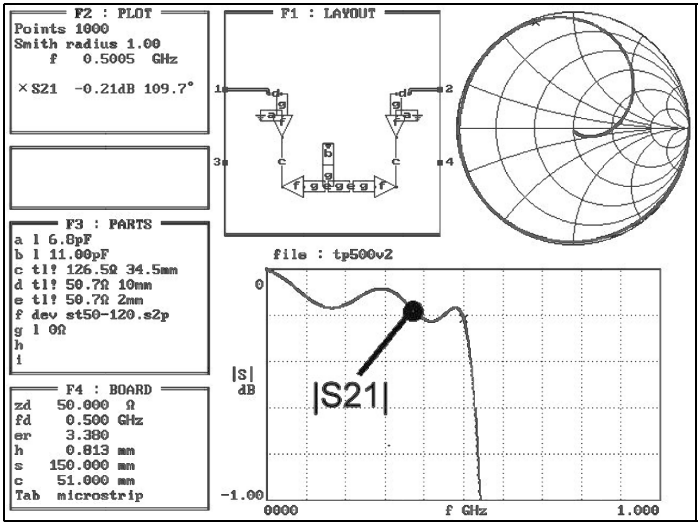

Fig 42: PUFF simulation of the version 2 500MHz filter.

inductor stripline“; only then does everything match. In Fig. 40 this can be recognised very easily in the four components identified with the letter “f“ (dev st50-120.s2p) taken from field F1.

If you're having difficulties with positioning, here's a trick that speeds things up enormously: first you draw the circuit in such a manner that all four steps point in the same direction. Then you dexterously move around, using the cursor keys, to delete each wrong step and then put it back in the right way round! It's done in a flash!

When the simulation circuit was being assembled, there was one question that had to be answered:

What is the initial length for the two “inductor microstrip lines"?

There is a very simple method where PUFF can offer first class service and show what it's capable of:

- Set up a simple circuit in field F1, where a line section is short-circuited at the end, and then determines its S11 value.

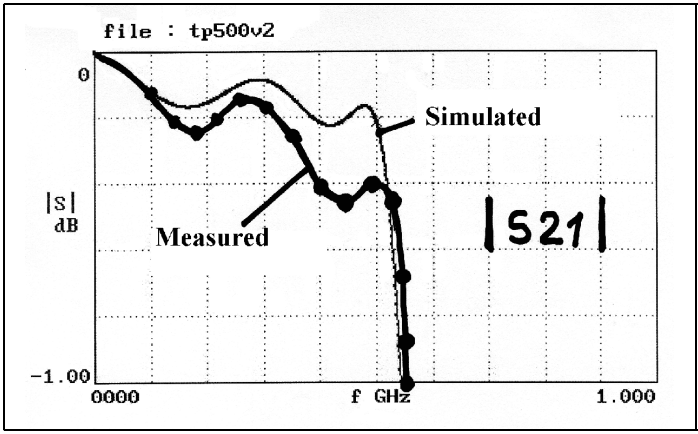

Fig 43: Measured results for the version 2 500MHz filter.

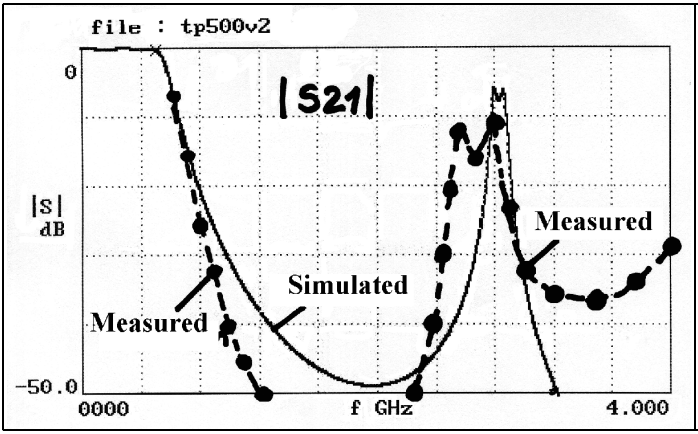

Fig 44: Measurment of the performance for the version 2 500MHz filter up to 4GHz.

- Following the calculation put the cursor on the "S11" line and press the equals sign. The replacement component values are immediately entered into the dialogue field at the current frequency (500MHz) and, since the line section behaves like an inductance at lengths below $\lambda/4$, the rest presents no complications. Repeat this procedure with various lengths in field F3 until the display shows 22nH, as desired, and a line length of 32.7mm is associated with it. Fig. 41 demonstrates this method very well.

Only now can a start be made on the actual circuit. The last simulation of the pass band can be seen in Fig 42. In Fig 43, we have the same simulation result again, but now together with the measurements on the prototype. We can be satisfied with the result, since the ripple is now markedly more uniform than in the previous version. The attenuation increases with the frequency, but we just have to accept this for the time being.

In Fig 44 the S21 simulation is shown together with the measurements up to 4GHz and for the value range from 0 to -50dB. The result was to be expected from this type of filter: first rate until you get past 2GHz, but then comes the dreaded collapse and departures from the simulation are unfortunately somewhat more serious than expected. Nevertheless, for such a wide frequency range it is easy to use and it is a great addition to your stock of components. Compared to version 1 it is better in the pass band, in the stop band it is worse at certain frequencies.

To end this section, Fig 45 shows the designed printed circuit board with the meandering folded lines (which would not fit into the housing any other way). By the way, documentation of S11 or S22 is superfluous because at the first maximum, theory and measurement correspond completely (approximately -16dB). Unfortunately, at the right hand maximum in the pass band, the theory predicts approximately -16dB, whereas only -14 to -15dB can be measured, which is nothing to worry about.

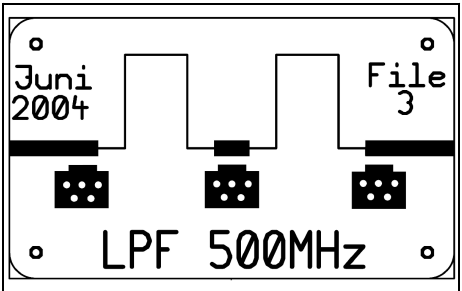

Fig 45: PCB layout for the version 2 500MHz filter.

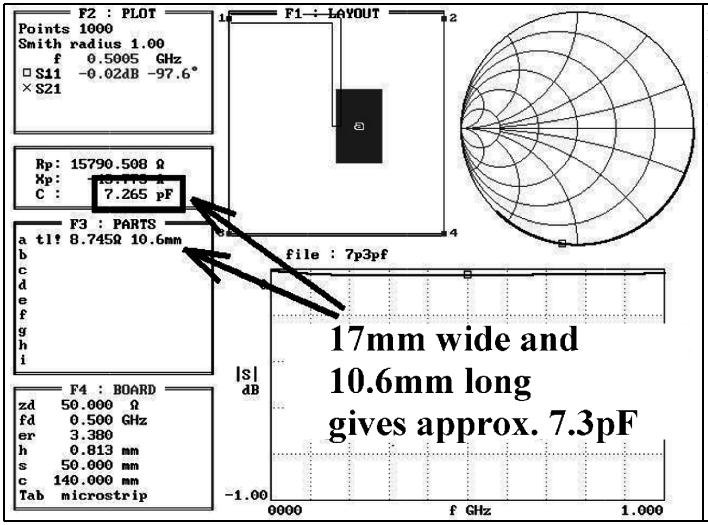

Fig 46: Result of PUFF simulation to find the dimensions of the 7.3pF capacitors.

4.3. 500MHz n=5 low pass filter, version 3 with SMD inductors and stripline capacitors

The advantages of this version are:

- Wide range with no reductions of attenuation in the stop band (as in version 1)
- All three SMD capacitors can be omitted. That makes this version easier to copy and reduces production costs.

While the creation of the printed capacitors is a puzzle, you have to live with the problem that it is difficult or almost impossible to obtain the precise inductance values proposed by the simulation. For this reason, the pre-condition has been somewhat altered: the filter circuit has to be optimised, using SMD inductances of 22nH to reduce the discrepancy with the standard value as much as

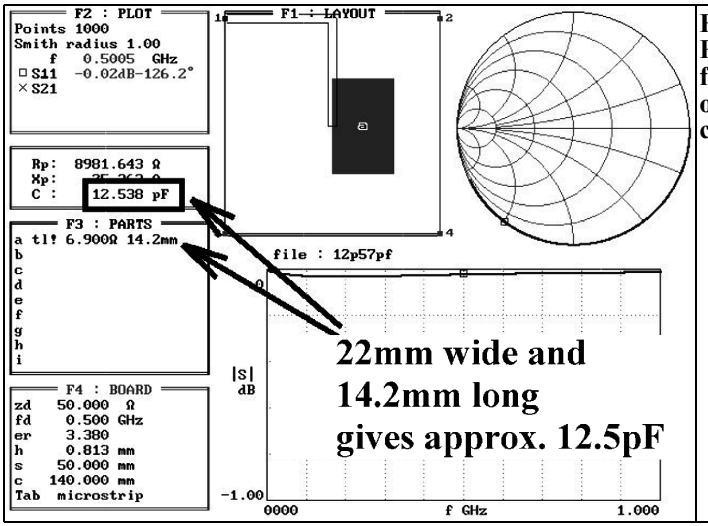

Fig 47: Result of PUFF simulation to find the dimensions of the 12.5pF capacitor.

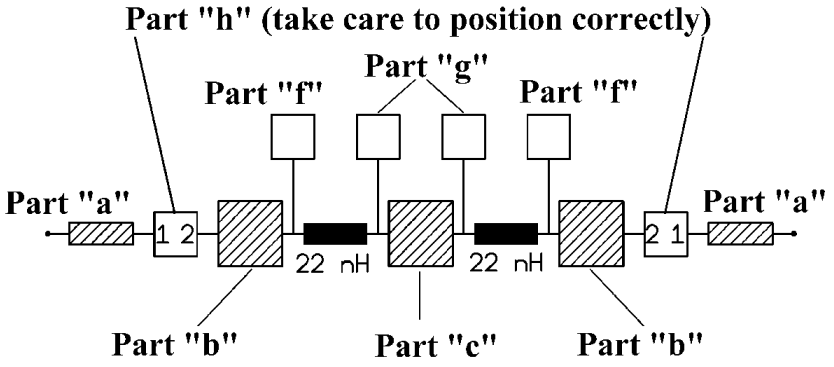

Fig 48: Circuit diagram for the version 3 500MHz filter used for PUFF simulation.

Part"a" Microstrip 50Ω / 6.4mm long, 1.83mm wide
Part"b" Microstrip 8.74Ω / 10.6mm long, 17mm wide
Part"c" Microstrip 6.9Ω / 14.2mm long, 22mm wide
Part "f" Oneport "17mm.s1p" (Open end extension for 8.74Ω)
Part "g" Oneport "22mm.s1p" (Open end extension for 6.9Ω)
Part "h" Twoport "s50-8p7.s2p" (transition from 50Ω and 8.74Ω)

possible - both for the cut-off frequency and for the ripple.

4.3.1. Designing stripline capacitors

As a reminder, and for comparison purposes, we repeat the requirements of the filter program:

C1 = C3 = 7.3pF
L1 = L2 = 21.82nH
C2 = 12.57pF

It is recommended that a wider line should be used for the central capacitor C2, because it is dangerous to obtain this capacitance - almost double the value of C1 – by just increasing the length. Firstly, there is a danger that it will not fit into the standard housing. Secondly, similar effects as in version 2 emerge in the stop band, since even thick striplines

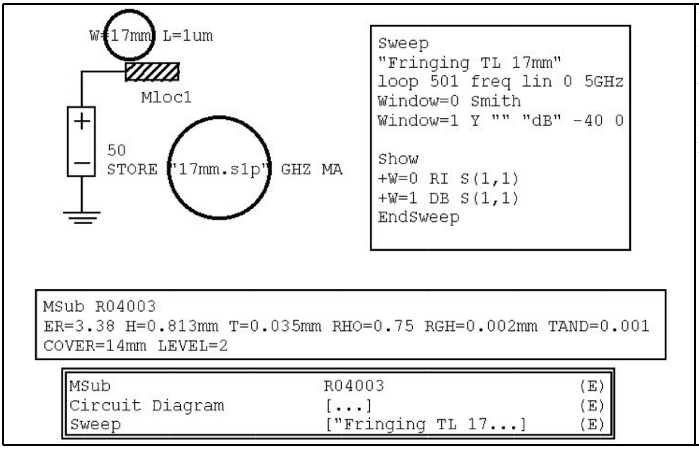

Fig 49: Using the free version of APLAC to generate the S-parameter file for the open end extension of a 17mm line.

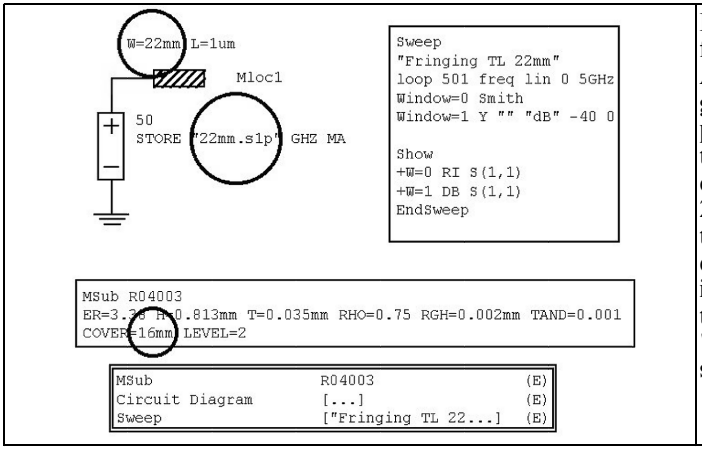

Fig 50: Using the free version of APLAC to generate the S-parameter file for the open end extension of a 22mm line. Note that the cover distance must be increased to 16mm to overcome a "feature" of the software.

cease to act like capacitors as the frequency increases and become genuine cables instead.

When these considerations were taken into account, and if we were careful to allow sufficient distance to the walls of the housing, the line width for C1 and C3 became 17mm, while that for C2 it was fixed at 22mm.

Initially, we used PUFF to determine the characteristic impedance associated with the width used. No great skill is required here, as we simply entered a section of 50Ω microstrip into a line in field F3. Then we briefly deleted the exclamation mark after "TL!....." and use the equals sign. The precise mechanical line data appears in the dialogue field.

If the characteristic impedance is reduced, the width increases, and we then fiddle about until we manage to obtain 17mm. It is a simple matter to determine the line length required for the capacitance specified: we work with an open circuit stripline section, simulate S11 and then use the keys (cursor on S11 in field F3, then press "Equals") to obtain the

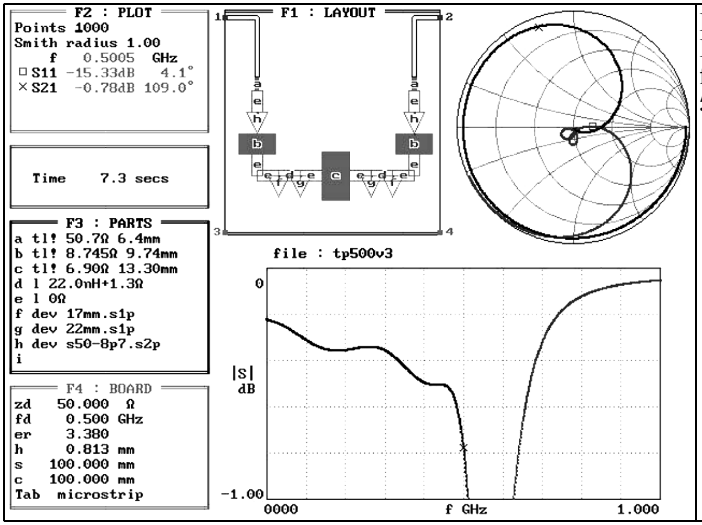

Fig 51: Result of PUFF simulation for the version 3 500MHz filter.

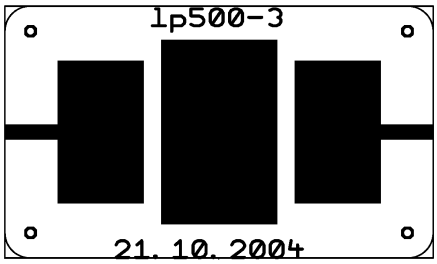

Fig 52: PCB layout for the version 3 500MHz filter.

relevant input capacitance. With a few variations of the line length, we can obtain required capacitances ranging from 7.3pF to 12.57pF (see Fig 46 for the two 17mm wide line sections and Fig 47 for the central capacitor with a conductor width of 22mm). But please don't forget to put the exclamation mark back behind the line entry in the appropriate line of field F3 before determining the length ("TL!...."). Otherwise the line will not be modelled realistically!

If we take a look at the PUFF simulation defaults in Fig 48, we can see immediately that APLAC must be used in order to determine the open end extensions for these wide lines, "17mm.s1p" and "22mm.s1p". Using the example of the 17mm wide line, Fig 49 is intended to demonstrate how simple it is and how helpful the free but performance-restricted student version of a modern microwave CAD program can be. As usual, the S1P file that is created is copied into the current PUFF file. However, if the open end extension procedure is also carried out in Fig 50 for the 22mm wide line, a problem occurs, there must be an important reason for this:

Modelling always applies only to a specific range of values as far as line, material and housing data are concerned. There is not always a warning when the limits are exceeded, for "Cover" = 14mm, this is the case, the calculated S-parameter file suddenly becomes a jerky sequence of gobbledegook. Unfortunately, no warning or error message is displayed referring to this, and so it is up to the developer to recognise this problem. Even an increase in the cover of 1 to 2mm is sufficient to put everything right again. This is the golden rule:

In cases like this, look at the curve for the S-parameter in the results diagrams, plotted against the frequency, and use your technical knowledge to determine whether this could really be true. At the end of the day, everything is based on the same principle - that you should never transfer any data blindly and without thinking. Always check first.

And here's a tip for professionals: as soon as you get two striplines with their narrow sides getting nearer and nearer to each other, a cross-talk effect will sometimes occur, in addition to the open end effect. Then we interpose a new component, namely a gap, in the simulation. It takes both effects into account and is naturally modelled and used as a "twoport". It is also available in APLAC as a ready-made component, but a check simulation using the full version shows that this is not necessary in the preceding example and it is sufficient to take the fringing into account. Nevertheless, we should mention this point for the sake of completeness.

Now it was time for the simulation and optimising result from PUFF assuming a quality level of Q = 50 for the SMD inductors at 500MHz, taken into account using a series resistor of 1.3Ω (Fig 51). After our previous experiences, no wildly exciting developments were to be expected while the completed prototype was being measured (see Fig 52 for the printed circuit board). So the result, in the form of a noticeably smaller transmission loss, was all the more baffling. In order to demonstrate this (and also to show the quality of the simulation), the measured values (Fig 53) were entered into a simulation diagram, in which the

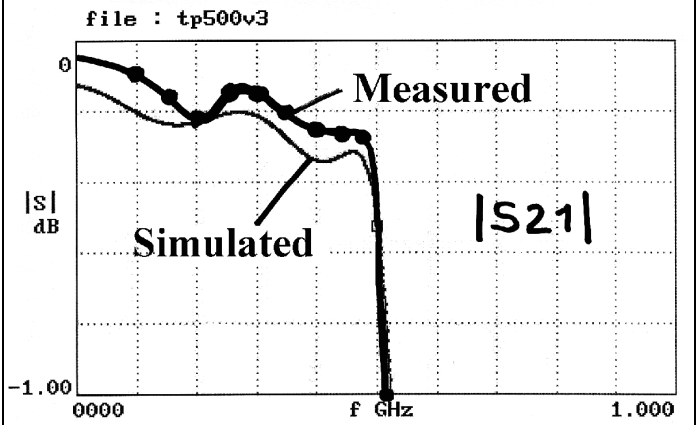

Fig 53: Measured results for the version 3 500MHz filter.

inductor loss resistance (corresponding to double the quality level, Q = 100) was halved. Obviously, the 22nH SMD inductors purchased for this development were better than expected, and the SMD capacitors used in the other versions were worse than expected.

The stop band curve is likewise somewhat steeper, but this is not connected with the higher component quality levels (Fig 54). If we take a good look at Fig 52, it is clear that the measured ripple somewhat exceeds the simulated value. Well, a worse ripple value would mean a steeper gradient for the attenuation in the stop band.

And finally, just a positive piece of news: even at 4GHz, the attenuation is still better than at 50dB.

To be continued.

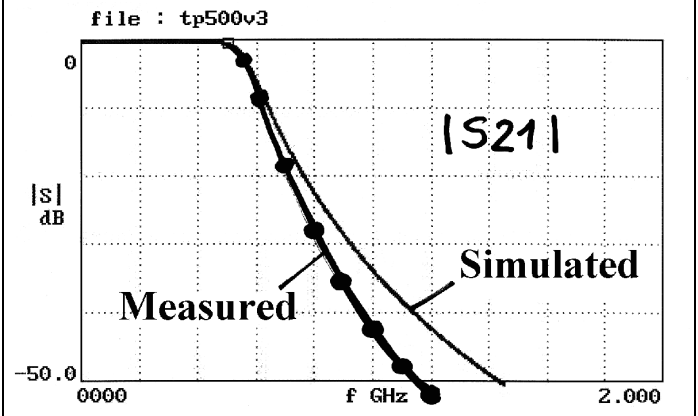

Fig 54: Measurement of the performance of the version 3 500MHz filter up to 2GHz.

Franco Rota, I2FHW

Franco's Finest: MGA62563 ultra low noise amplifier

1.0 Introduction

The purpose of this article is to demonstrate the specification of a new MMIC from Agilent (formerly HP) that has some very interesting performance in "no tune" applications. The MGA62563 has an ultra low noise performance associated with a high dynamic range in no tune circuits. It is an MMIC device fabricated with the GaAs-Fet E-pHEMT process, this process is already well known from the ATF54143 which is a single GaAs-Fet with a very high dynamic range.

This article will demonstrate that the performance of this no tune broad band MMIC are similar to a tuned GaAs-Fet.

2.0 The Choice

During many years of my working experience I have always had the need to supply RF amplifiers with low noise and broadband, of course with a good dynamic range. All the technicians know very well that the dynamic range is not compatible with low noise (or very low noise) performance.

Today the market can offer a very large choice of MMICs, I carefully examined the performance of many of them but only the MGA62563 from Agilent has the following performance:

- Very low Noise Figure: 0.8 - 1dB NF in the 30MHz to 2600MHz range
- Very good dynamic range: +32dBm OIP3
- High output power: +17.5 dBm P1dB
- Good input-output return loss: 10 to 20dB
- No tune: it needs only dc blocking capacitors and bias decoupling
- Power supply: single positive voltage (no negative bias)
- Unconditionally stable: K > 1 (no self oscillation)

and last but not least

- Ultra broadband applications

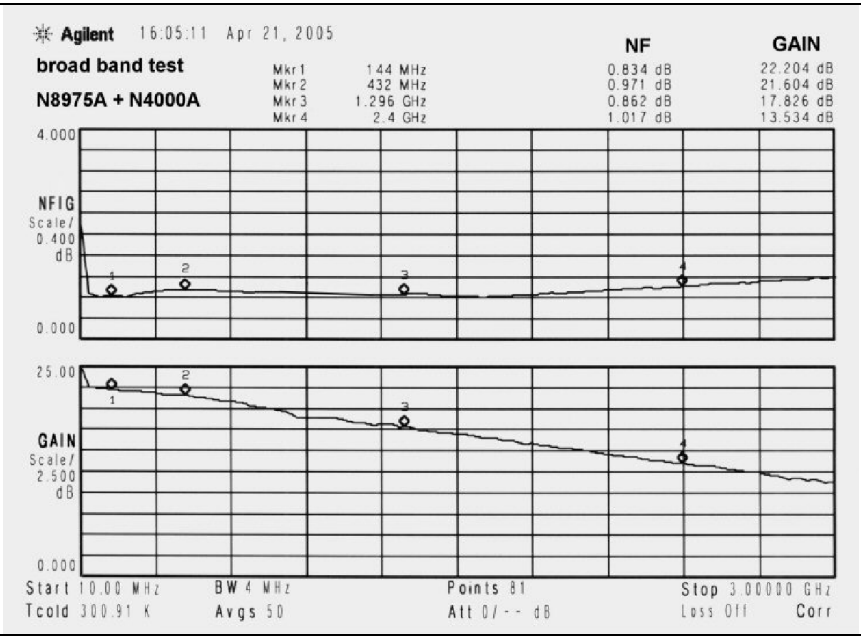

Fig 1: Plot of noise figure and gain for the MGA62563 up to 3GHz.

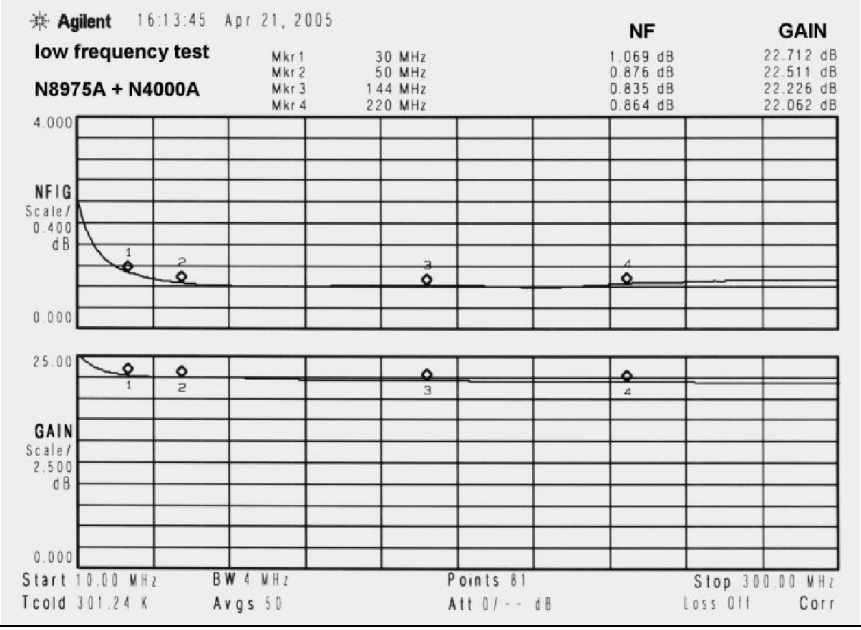

Fig 2: Plot of noise figure and gain for the MGA62563 up to 300MHz.

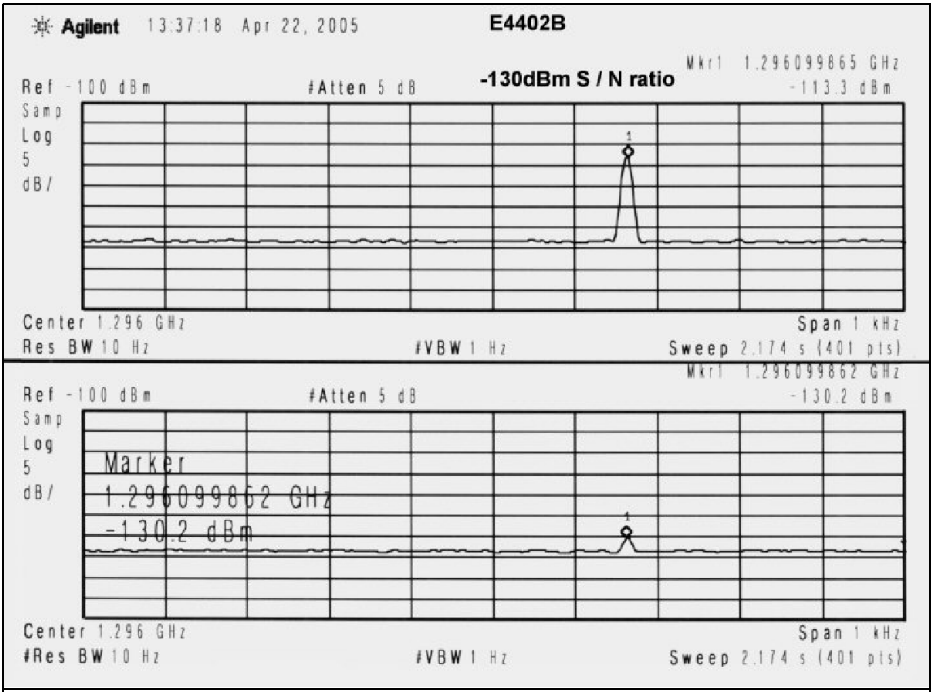

Fig 3: Plot showing the amplification of a 130dBm signal.

3.0

Performances Explanation

NOISE FIGURE - as you can see in Figs 1 and 2 there is the broadband and expanded low frequency band graph in order to show it at lower frequencies, the noise figure remains lower than 1dB up to 2GHz (typically 0.9dB) and 1.1dB @ 2.5GHz. The associated gain is appropriate for applications from 30MHz to 2.6GHz, see table 1. This is achieved without any special LC tuning or complicated circuits, it means that this MMIC is useful for a very big range of applications; you can use it as low noise preamplifier both for amateur and commercial applications.

As a last test I put this preamplifier in front of my spectrum analyser with an input signal of -130dBm (0.07µV). As you can see in Fig 3, the small signal of -130dBm is perfectly readable using the preamplifier.

DYNAMIC RANGE – with conditions of very low noise figure explained above, the device also has a high dynamic range.

Table 1: Noise figure and gain of the MGA62563 at various frequencies.

Frequency (MHz)	Noise Fig. (dB)	Gain (dB)
30	1.07	22.7
50	0.87	22.5
144	0.83	22.2
220	0.86	22
432	0.97	21.6
1296	0.86	17.8
2400	1.01	13.5

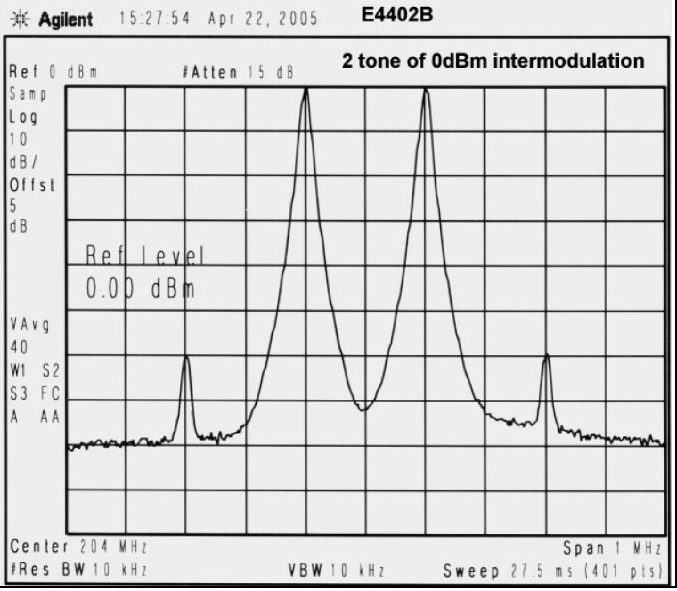

Fig 4: Plot showing the two tone test performance of the MGA62563.

You can see in Fig 4, a graph of two-tone intermodulation with two tones each 0dBm output power, the IMD level is -60dB. You can also see in Fig 5 graphs of single tone harmonic distortion, with 0dBm output level, the second harmonic

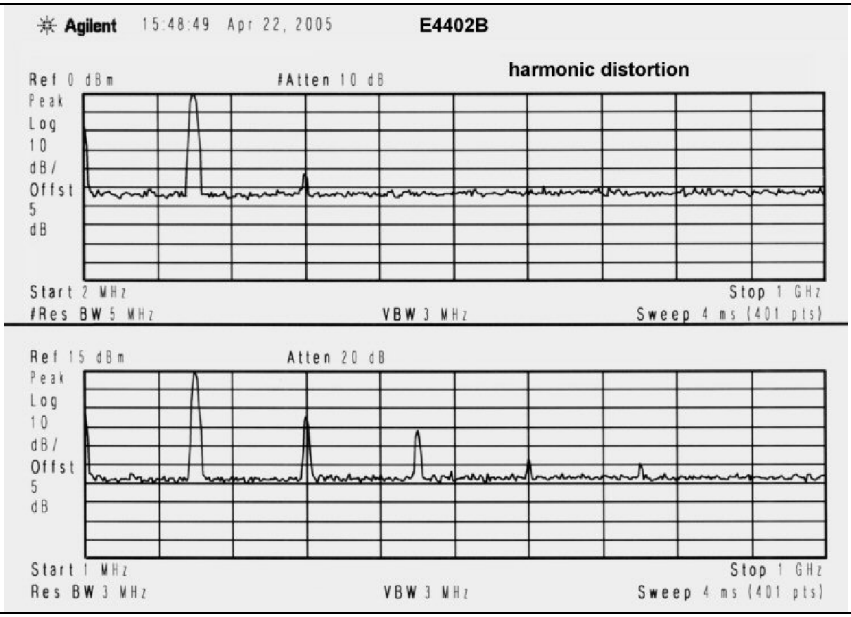

Fig 5: Plot showing the single tone test performance of the MGA62563 at two different input levels.

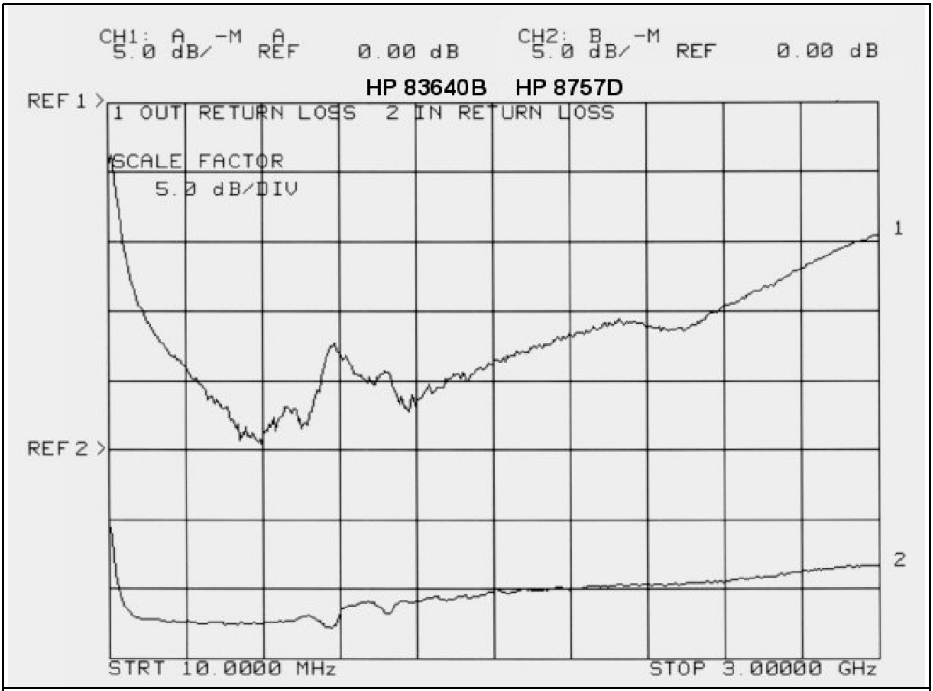

Fig 6: Return loss measurement of the MGA62463.

is -42dB and with +15dBm output level the second harmonic is -25dB.

The value measured for the output power 1dB compression point is in Table 2.

N.B. average value P1dB +17.5dBm = 56mW (a little transmitter)

IN-OUT RETURN LOSS - Typically an ultra low noise amplifier using a GaAs-Fet has a good noise figure but has a bad input return loss, this is known very well by EME fans. The MGA62563 has an average input return loss of 10dB and output return loss better than 15dB (see Fig 6).

If you put a filter (before or after) the amplifier you will not have any detuning of the filter because the return loss is moderately low. This is also very good as a moon bounce post amplifier in order to reduce self-oscillations, in fact the device is guaranteed for K > 1. In my lab I tested 3 devices all connected in cascade and I tried to obtain a self-oscillation by a mismatching but it was not possible.

4.0

No Tune Circuit

The circuit used for the above measurement is shown in the Fig 7, it is very simple and doesn't need any tuning components. The input dc blocking capacitor is not critical and I used a parallel capacitor, high Q ATC100A in order to reduce the ESR of a normal SMD capacitor for frequencies above 2GHz, this

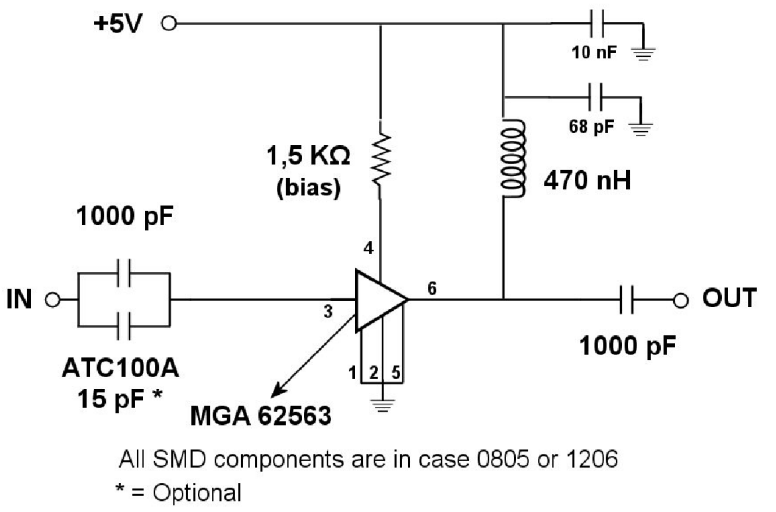

Fig 7: Circuit diagram of the test circuit used to make measurements on the MGA62563.

improves the noise figure by only 0.1dB, this means that it isn't indispensable.

The resistance of 1.5K. is for +5V/40mA power supply, you can adjust it if you want to improve or reduce the current, no large variations are been experienced between 30 to 50mA, so it means that the device is not critical and the performance remains stable within moderate power supply variations.

The choke coil and the dc blocking output capacitor are also not critical.

Table 2: 1dB compression point and output power of MGA62563 at various frequencies.

Frequency	P1 (dBm)	Psat (dBm)
50	+18	+19.5
150	+18.5	+20.5
500	+18	+20
1300	+17.5	+19.5
2000	+17	+19
2400	+16.5	+18.5

5.0 Conclusions

I believe that this MMIC will have a good future as ultra low noise preamplifier associated with high dynamic range. Considering the price, it is available around €3.00 each (a cup of coffee in UK and half a pizza in Italy) so it is affordable by anyone.

Good luck to everybody from I2FHW Franco Rota, www.rfmicrowave.it.

Gunthard Kraus, DG8GB

Internet Treasure Trove

145GHz amateur band

Variety is the spice of life – of course everyone knows this saying. Why shouldn't it sometimes be some completely different frequency ranges? So anyone who wants to take a trip to such high frequencies should begin by taking a look at this page.

Address:
http://www.mgef.org/145ghz.htm

136kHz amateur band

Anyone who, in contrast, is attracted by really low frequencies, will find an attractive little range of items here - circuits, antennas, ideas, etc...

Address:
http://home.online.no/~la8ak/L2.htm

Tele-Tech

They are a company that produces all kinds of things for RF technology, such as mixers, directional, other couplers and dividers. Not only is it interesting to glance at the specifications of the components (for example, there's a tiny little directional coupler which covers a range from 1MHz to 1GHz), but the application notes are of interest too.

Address:
http://tele-tech-rf.com/prodselection.htm

EM-Wonder

Those who like to simulate their circuits before testing the first prototypes will enjoy this site. Not only will they find links there to various SPICE model lists, but also data on something really splendid: a converter that generates an S-parameter file for simulation.

Address:
http://www.emwonder.com/spicemodels/

PlexTex

Some more people who are very active in

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Address:
http://www.plextek.com/technicalpapers.htm#

Broadband multi-function antenna suitable for incorporation into vehicles

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Address:
http://www.ubka.uni-karlsruhe.de/cgi-bin/psview?document=/2001/elektrotechnik/6&search=/2001/elektrotechnik/6

Tripod

Anyone looking for interesting programs for "fiddly little jobs" should make a note of this address and pay the site a visit from time to time. New items appear here at regular intervals.

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http://members.tripod.com/michaelgellis/software.html

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Here we have an online calculator, which can be used to determine all the important characteristics of a receiver if the various stage characteristics are entered. These characteristics are: overall amplification, total noise factor, spurious free dynamic range and noise floor in dBm.

Address:
http://members.tripod.com/michaelgellis/anadigic/Receiver.html

Directional Couplers

An easy-to-understand and accurately written introduction to the characteristics of directional couplers, including illustrations and formulae. Compiled as an online lexicon of RF technology by Bilkent University in Turkey.

Address:
http://www.ee.bilkent.edu.tr/~microwave/programs/magnetic/dcoupler/theory.htm

GlobalSpec - The Engineering Search Engine

There's not much explanation needed here: anyone needing links in connection with a problem or a term should try their luck here. Normally you end up with more information than you can use.

Address:
http://www.globalspec.com/

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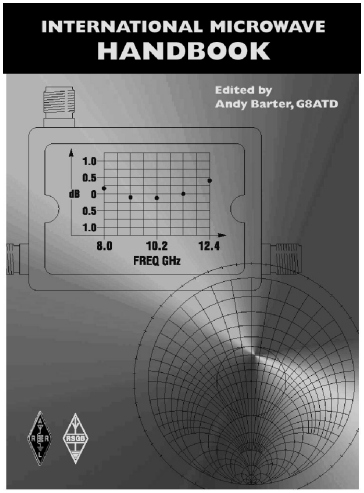

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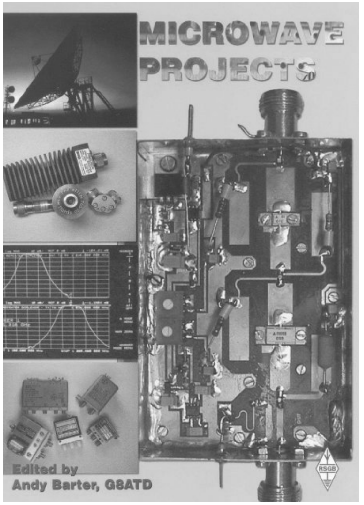

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