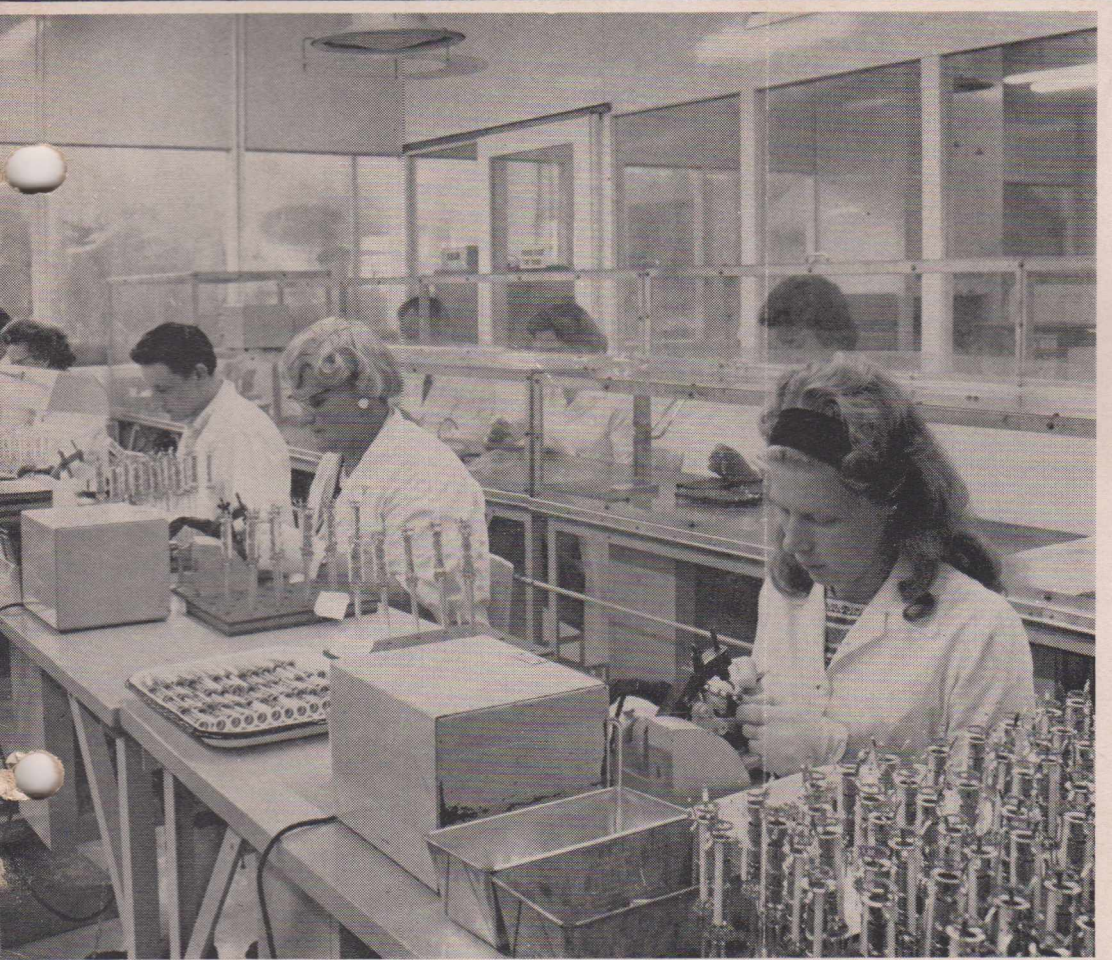
# RADIOTRONICS



## IN THIS ISSUE



*COVER:*

*View of Picture Tube Gun Section at A.W.V. plant, Rydalmere, N.S.W.*


**Vol. 31, No. 2** **April, 1966**

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# LINEAR AND DIGITAL INTEGRATED CIRCUITS

**We are proud to introduce a comprehensive range of integrated circuits of the single-chip, monolithic silicon, passivated, epitaxial construction.**

**The Linear Range covers requirements for application from DC to 100 Mc/s with the inherent temperature stability of the basic circuit permitting operation from —55°C to +125°C.**

**To mention but a few possible applications—do you need a D.C. Amplifier, Video Amplifier, R.F. or I.F. Amplifier, Wideband Amplifier and Discriminator, A.F. Amplifier, Schmitt Trigger, Comparator, Operational Amplifier, Sense Amplifier.**

**Digital Circuits in the range have extremely low power requirements (2.3 mW per gate) and, we believe, the highest commercially available speeds (3.6 nS.).**

## DIGITAL INTEGRATED CIRCUITS

Digital integrated circuits are supplied in 14-lead, hermetically sealed, ceramic and metal flat packages.

DIGITAL INTEGRATED CIRCUITS are aimed specifically at the growing number of applications that require either:

- extremely high-speed switching, or
- extremely low power dissipation

ULTRA-HIGH-SPEED ECCSL• (emitter-coupled current-steered logic) FAMILY is specifically designed for 3rd-generation data-processing and scientific computer applications in which high-speed operation is of paramount importance.

HIGH-SPEED ECCSL• FAMILY has been designed for use in military computer and control applications, and high-frequency digital communications equipment where high-speed and high-performance operation must be maintained over a wide temperature range (—55°C to +125°C).

LOW-POWER DTL FAMILY offers extremely low power dissipation in high-performance circuitry of Aerospace, Airborne, and Portable Digital Equipment where high-density equipment packaging requires low heat generation and low power drain.

EMITTER-FOLLOWER OUTPUTS in all the digital circuit families permit driving of relatively high-capacitance loads. In addition, all ECCSL digital families are capable of driving terminated transmission lines.

COMPREHENSIVE APPLICATION INFORMATION is given in associated application notes. These notes cover features; typical applications; logic functions; effects of power supply, temperature and loading variations; and other significant considerations for equipment designers.

FLAT-PACKAGE CARRIERS. Each RCA integrated circuit in a 14-lead flat package is shipped in an individual carrier. The carrier provides maximum protection against damage in handling and permits electrical testing of the circuit without removal from the carrier.

• Pronounced EXCEL

# BROAD-CAPABILITY LINE

RCA's broad, new line of integrated circuits are designed to cover a wide spectrum of your circuit requirements for both digital and linear applications. These new integrated circuits offer:

- single-chip, monolithic silicon, passivated, epitaxial construction
- hermetically sealed TO-5 style packaging, and ceramic and metal flat packaging
- digital circuit coverage includes both extremely low power (2.3 mW per gate), and highest commercially available speeds (3.6 ns)
- linear circuit coverage from DC to 100 Mc/s
- all circuits tested on computerized, automatic test equipment with parameter readout

# LINEAR INTEGRATED CIRCUITS

Linear integrated circuits are supplied in hermetically sealed, low-silhouette TO-5 style metal packages. Operational Amplifier types are available in both TO-5 package and 14-lead ceramic and metal flat package.

DIFFERENTIAL AMPLIFIER CONFIGURATION with built-in controlled constant-current source has been selected as the basic design unit for all RCA linear circuits.

APPLICATION VERSATILITY of the basic differential-amplifier configuration makes linear circuits extremely useful in a wide variety of applications—

- Push-pull amplifier
- DC amplifier
- Video amplifier
- RF amplifier
- IF amplifier
- AF amplifier
- Operational amplifier
- Sense amplifier
- Modulator
- Schmitt trigger
- AGC
- Limiter
- Squelch
- One-shot multivibrator
- Phase splitter
- Comparator
- AM detector
- Product detector
- Mixer

BASIC CIRCUIT permits easy access to internal circuit points and external circuit outboarding

INHERENT TEMPERATURE STABILITY of the basic circuit permits operation from —55°C to +125°C

TECHNICAL-ECONOMIC COMPATIBILITY of the differential-amplifier construction, and the reliable monolithic silicon epitaxial process, provide excellent performance, excellent economy

INHERENTLY MATCHED PAIRS of components offer excellent output-to-input isolation, no neutralization, and simplify feedback arrangements

COMPREHENSIVE APPLICATION INFORMATION is given in associated application notes. These notes cover operating characteristics at different voltages; effects of temperature and operating point on gain and frequency; detailed analysis of performance characteristics: cross-modulation, distortion, noise, phase compensation, etc.; practical circuit designs for limiters, detectors, 10-Mc/s narrow-band tuned amplifier, 3-stage video amplifier, etc.

# LINEAR INTEGRATED CIRCUITS

| Type | Equipment Applications | Circuit Applications | Max. Input Signal Volts | Device Dissipation mW | Gain dB 5.5 mc/s | Gain dB 10.7 mc/s |
|---|---|---|---|---|---|---|
| **WIDE BAND AMPLIFIERS** | | | | | | |
| CA3011 | — | Sound and FM IF Amplifier and Limiter, | +3 —3 | 120 | 66 | 61 |
| CA3012 | — | General RF and IF Wide Band Amplifier | +3 —3 | 190 | 66 | 61 |
| **WIDE BAND AMPLIFIER DISCRIMINATORS** | | | | | | |
| CA3013 | TV and FM | Sound and FM IF Amplifier, FM Detector, | +3 —3 | 120 | 66 | 60 |
| CA3014 | Receivers | AM and Noise Limiter, Audio Preamplifier | +3 —3 | 190 | 66 | 60 |

| Type | Equipment Applications | Circuit Applications | Max. Input Signal Voltage V | Device Dissipation mW | Input Offset Voltage mV |
|---|---|---|---|---|---|
| **OPERATIONAL AMPLIFIERS** | | | | | |
| CA3008 | Telemetry Data-Processing Instrumentation Communications | Operational Amplifier, Oscillator, Comparator, Feedback Amplifier, Narrow-Band and Band-pass Amplifier, Servo Driver, DC and Video Amplifier, Multivibrator, Balanced Modulator-Driver, Push-Pull Input | +1, —2 | 30 | 1.0 |
| CA3010 | | | +1, —2 | 30 | 1.0 |
| **RF AMPLIFIERS** | | | | | |
| CA3004 | Communications | Push-Pull Input and Output, Mixer, Limiter, Modulator, AGC, Detector, Wide and Narrow Band Amplifier, RF, IF, and Video Amplifier. CA3005 and CA3006 may also be used as cascode amplifier | +3.5, —3.5 | 26 | 1.7 |
| CA3005 | | | +3.5, —3.5 | 26 | 2.6 |
| CA3006 | | | +3.5, —3.5 | 26 | 0.8 |
| **VIDEO AMPLIFIERS** | | | | | |
| CA3001 | Video Systems Communications | Push-Pull Input and Output, Mixer, AGC and Schmitt Trigger, Modulator, DC, IF, and Video Amplifier (may be AC coupled) | +2.5, —2.5 | 60 | 1.5 |
| **DC AMPLIFIERS** | | | | | |
| CA3000 | Telemetry Data-Processing Instrumentation Communications | Push-Pull Input and Output, AGC, Mixer, Sense Amplifier, Modulator, Schmitt Trigger, RC-Coupled Feedback Amplifier, Crystal Oscillator, Comparator | +2, —2 | 30 | 1.4 |
| **IF AMPLIFIERS** | | | | | |
| CA3002 | Communications | Push-Pull Input, AGC, Product Detector, AM Detector, RC-Coupled Cascoded Amplifier, IF and Video Amplifier (may be AC coupled) | +3.5, —3.5 | 55 | — |
| CA3003 | | | Similar to CA3002 but features increased gain and reduced device dissipation | | |
| **AF AMPLIFIERS** | | | | | |
| CA3007 | Communications Sound Systems | Audio Amplifier, Audio Driver, Direct Coupling to Class B Audio Output Stage | +2.5, —2.5 | 30 | — |
| CA3009 | | | Similar to CA3007 but features improved frequency response characteristic, increased gain, greater dynamic voltage range, and greater versatility of application. | | |

# LINEAR INTEGRATED CIRCUITS

| Input Limiting Voltage μV | AM Rejection dB | AF Output mV | AF Output THD % | Noise Figure dB | Operating Temp. Range °C |
|---|---|---|---|---|---|
| | | | | | **WIDE BAND AMPLIFIERS** |
| 300 | — | — | — | 8.7 | —55 to +125 |
| 300 | — | — | — | 8.7 | —55 to +125 |
| | | | | | **WIDE BAND AMPLIFIER DISCRIMINATORS** |
| 300 | 50 | 188 | 1.8 | 8.7 | —55 to +125 |
| 300 | 50 | 220 | 1.8 | 8.7 | —55 to +125 |

| Input Bias Current μA | Gain dB | Common mode Rejection Ratio at 1 kc/s dB | —3dB Bandwidth | Input Impedance Ω | Output Impedance Ω | Associated Application Note | Type |
|---|---|---|---|---|---|---|---|
| | | | | | | | **OPERATIONAL AMPLIFIERS** |
| 5.3 | 60 at 1 kc/s | 94 | 300 kc/s | 14000 at 1 kc/s | 200 at 1 kc/s | ICAN—5015 | CA3008 |
| 5.3 | 60 at 1 kc/s | 94 | 300 kc/s | 14000 at 1 kc/s | 200 at 1 kc/s | | CA3010 |
| | | | | | | | **RF AMPLIFIERS** |
| 21 | 12 at 100 Mc/s | 98 | 100 Mc/s | 1200 at 100 Mc/s | 2200 at 100 Mc/s | ICAN—5022 | CA3004 |
| 19 | 16 at 100 Mc/s | 101 | 100 Mc/s | 1400 at 100 Mc/s | 2000 at 100 Mc/s | | CA3005 |
| 19 | 16 at 100 Mc/s | 101 | 100 Mc/s | 1400 at 100 Mc/s | 2000 at 100 Mc/s | | CA3006 |
| | | | | | | | **VIDEO AMPLIFIERS** |
| 10 | 19 at 1 Mc/s | 70 | 16 Mc/s | 60000 at 1.75 Mc/s | 60 at 1.75 Mc/s | ICAN—5038 | CA3001 |
| | | | | | | | **DC AMPLIFIERS** |
| 23 | 37 at 1 kc/s | 98 | 650 kc/s | 195K at 1 kc/s | 8000 at 1 kc/s | ICAN—5030 | CA3000 |
| | | | | | | | **IF AMPLIFIERS** |
| 20 | 24.4 at 1.75 Mc/s | — | 11 Mc/s | 100K at 1.75 Mc/s | 70 at 1.75 Mc/s | ICAN—5036 | CA3002 |
| | Similar to CA3002 but features increased gain and reduced device dissipation | | | | | | CA3003 |
| | | | | | | | **AF AMPLIFIERS** |
| 10.5 | 22 at 1 kc/s | 77 | 20 kc/s | 4000 at 1 kc/s | 60 at 1 kc/s | ICAN—5037 | CA3007 |
| Similar to CA3007 but features improved frequency response characteristic, increased gain, greater dynamic voltage range, and greater versatility of application | | | | | | | CA3009 |

# DIGITAL INTEGRATED CIRCUITS

| Type | Description | Features | Type | Logic Levels "0" V | Logic Levels "1" V |
|---|---|---|---|---|---|
| **ULTRA- HIGH-SPEED ECCSL* GATES (OR/NOR — POSITIVE LOGIC)** | | | | | |
| CD2150 | DUAL FOUR-INPUT GATE | • extremely high-speed switching (non-saturated transistor operation)—only 3.6 ns tpd (fan-out 1 + 10 pF)<br>• emitter-follower low-impedance outputs—permits large fan-out driving capability<br>• integral reference-threshold voltage supply—provides thermal and supply voltage tracking, plus good noise immunity<br>• capable of driving terminated 100-ohm transmission line—insures max. signal transmission without distortion | ECL | —1.6 | —0.76 |
| CD2151 | DUAL FOUR-INPUT GATE With "Phantom OR" Output Capability | | ECL | —1.6 | —0.76 |
| CD2152 | EIGHT-INPUT GATE With "Phantom OR" Output Capability | | ECL | —1.6 | —0.76 |
| **HIGH-SPEED ECCSL* GATES (OR/NOR — POSITIVE LOGIC)** | | | | | |
| CD2100 | DUAL FOUR-INPUT GATE | • high speed (result of non-saturated transistor operation)—6 ns tpd (fan-out 1 + 10 pF)<br>• wide operating temperature range —55° C to +125° C<br>• integral reference-threshold voltage supply—provides thermal and supply voltage tracking plus good noise immunity<br>• emitter-follower low-impedance outputs—permits large fan-out driving capability<br>• capable of driving terminated 300-ohm strip line—insures max. signal transmission without distortion | ECL | —1.55 | —0.75 |
| CD2101 | QUADRUPLE TWO-INPUT NOR GATE | | ECL | —1.55 | —0.75 |
| CD2102 | J-K FLIP-FLOP With Set-Reset Capability | | ECL | Scheduled for Announcement in 1966 | |
| CD2103 | DUAL FOUR-INPUT GATE With "Phantom OR" Output Capability | | ECL | | |
| CD2104 | EIGHT-INPUT GATE | | ECL | | |
| **LOW-POWER DTL GATES (NAND — POSITIVE LOGIC)** | | | | | |
| CD2200 | DUAL FOUR-INPUT GATE With Input Expander Node | • very low device dissipation—2.3 mW per gate<br>• wide operating temperature range —55° C to +125° C<br>• buffer circuit output—makes possible high capacitive-load driving capability<br>• high noise immunity—1.2V typ. at 25° C; 0.7V typ. at 125° C<br>• very low device dissipation — 8mW typ. | DTL | 0.1 | 3.4 |
| CD2201 | QUADRUPLE TWO-INPUT GATE | | DTL | 0.1 | 3.4 |
| CD2202 | DUAL FOUR-INPUT GATE-BUFFER | | DTL | Scheduled for Announcement in 1966 | |
| CD2203 | J-K FLIP-FLOP With Set-Reset Capability | • high noise immunity—clock lines, 1.5 V; all other inputs, 1.2V<br>• eight inputs: 2 DC Set, 2 Split Clock, 2 "J" Clock Steering, 2 "K" Clock Steering | DTL | 0.1 | 3.4 |
| CD2204 | DUAL FOUR-INPUT EXPANDER | Scheduled for Announcement in 1966 | | | |
| CD2205 | DUAL FOUR-INPUT GATE With "Phantom OR" Output Capability | Scheduled for Announcement in 1966 | | | |

* Pronounced EXCEL

# DIGITAL INTEGRATED CIRCUITS

| Operating Conditions | | | | | Typical Characteristics at $T_A$ = 25° C | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Temperature Range | Supply Voltage Range | Max. Fan-Out Per Gate Unloaded | Loaded with Terminated Transmission Line | | DC Input Current | Noise Immunity | Device Dissipation | Propagation Delay | | Associated Application Note | Type |
| | | | No. | Ω | | | | Speed | Load | | |
| °C | V | | | | mA | V | mW | ns | fan-out | | |
| **ULTRA-HIGH-SPEED ECCSL* GATES (OR/NOR — POSITIVE LOGIC)** | | | | | | | | | | | |
| +10 to +60 | —4.5 to —5.5 | 12 | 6 | 100 | 0.1 | 0.33 | 220 | 3.6 | 1 + 10 pF | ICAN-5025 | CD2150 |
| +10 to +60 | —4.5 to —5.5 | 12 | 6 | 100 | 0.1 | 0.33 | 175 | 3.6 | 1 + 10 pF | ICAN-5025 | CD2151 |
| +10 to +60 | —4.5 to —5.5 | 12 | 6 | 100 | 0.1 | 0.33 | 110 | 3.6 | 1 + 10 pF | ICAN-5025 | CD2152 |
| **HIGH-SPEED ECCSL* GATES (OR/NOR — POSITIVE LOGIC)** | | | | | | | | | | | |
| —55 to +125 | —4.68 to —5.72 | 12 | 6 | 300 | 0.05 | 0.32 | 88 | 5.6 | 1 + 10 pF | General Features of ECL discussed in ICAN-5025 | CD2100 |
| —55 to +125 | —4.68 to —5.72 | 12 | 6 | 300 | 0.05 | 0.32 | 120 | 5.6 | 1 + 10 pF | | CD2101 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2102 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2103 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2104 |
| **LOW-POWER DTL GATES (NAND — POSITIVE LOGIC)** | | | | | | | | | | | |
| —55 to +125 | +3.8 to +6.3 | 6 | — | — | —0.15 | 1.2 | 2.3 per gate | 100 | 6 + 60 pF | ICAN-5024 | CD2200 |
| —55 to +125 | +3.8 to +6.3 | 6 | — | — | —0.15 | 1.2 | 2.3 per gate | 100 | 6 + 60 pF | ICAN-5024 | CD2201 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2202 |
| —55 to +125 | +3.8 to +4.5 | 5 per Output | — | | —0.15 | 1.2 | 8 | 175 | 5 + 50 pF | ICAN-5024 | CD2203 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2204 |
| Scheduled for Announcement in 1966 | | | | | | | | | | | CD2205 |

* Pronounced EXCEL

# Frequency Multiplication Using Overlay Transistors

BY: R. MINTON and H. C. LEE

## INTRODUCTION

The "overlay" transistor can be used in frequency-multiplier circuits to generate watts of harmonic output power at microwave frequencies. The advantage of the use of overlay transistors in the generation of harmonic power is that frequency multiplication and power amplification can be realized simultaneously. In frequency-multiplier circuits, overlay transistors will provide power amplification at the fundamental frequency of the input driving power, and the nonlinear capacitance of the collector-to-base junction in these transistors will generate harmonics of the input frequency.[1] It is possible, therefore, for a single overlay transistor to provide both frequency multiplication and signal-power gain. Moreover, the use of an overlay transistor in a frequency-multiplier circuit extends the upper limit of the frequency range far beyond that possible from the same transistor in a power-amplifier circuit and well into the microwave region.

This paper describes the use and capabilities of overlay transistors in such applications. The operation and basic design considerations of overlay transistor frequency multipliers are explained, and the instability problems that may be encountered in such circuits are discussed. Circuit details and performance data are given for practical frequency doublers, triplers and quadruplers which use the RCA 2N4012 overlay transistor to generate watts of output power in the UHF and L-band ranges. The relative merits of common-base and common-emitter connections of overlay transistors in such circuits are compared.

## HARMONIC GENERATION IN OVERLAY-TRANSISTOR MULTIPLIERS

An overlay transistor used in a frequency-multiplier circuit operates simultaneously as a power amplifier to provide gain at the fundamental frequency of the input driving power and as a varactor diode to generate harmonics of the driving-power frequency. Fig. 1 shows the simplified equivalent circuit of an overlay transistor for this application. If the transistor collector-to-base capacitance, $C_{bc}$, were omitted, the circuit would be identical to the hybrid-pi equivalent circuit of a transistor power amplifier, which has been described extensively in literature.[2] In overlay transistors, however, the large area of the collector-to-base junction, together with the active area under the emitter, results in a relatively high collector-to-base capacitance. Because this capacitance is usually much larger than the capacitance $C_{b'c}$, it must be included in the equivalent circuit together with parameters defined by the hybrid-pi circuit.

The capacitance $C_{bc}$ varies nonlinearly with the transistor collector voltage in much the same way as that of a varactor diode with the voltage across the diode junction. It is this variable junction capacitance that makes possible harmonic generation in overlay transistor circuits. The nonlinear relationship between the collector-to-base capacitance $C_{bc}$ and the collector bias voltage in overlay transistors may be expressed as follows:

$$C_{bc} = K(\phi - V)^{-n} \qquad (1)$$

where K is the constant determined by the area and doping of the junction, $\phi$ is the contact potential, V is the magnification of the collector reverse-biased voltage, and the exponent n is a constant that is dependent upon the impurity distribution on both sides of the junction.

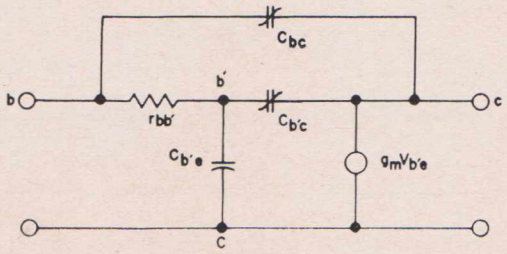



*FIG. 1.—Equivalent circuit of an overlay-transistor frequency multiplier.*

The plot of Eq. (1) given in Fig. 2(a) shows the variation in the collector-to-base capacitance, $C_{bc}$, as a function of the collector bias voltage, V. This form of capacitance-voltage curve is difficult to apply directly in the analysis of high-frequency, high-power transistor circuits. Because power is the product of current and voltage, it is more convenient to analyze such circuits in terms of the current and voltage swings in the transistor. The transistor current can be related to the collector-to-base capacitance if the charge, Q, across the junction is known. Because $dQ/dV = C(V)$, the charge Q can be determined as follows:

$$Q = \int C_{bc}\, dV \qquad (2)$$

With the capacitance $C_{bc}$ defined as in Eq. (1), the integration indicated in Eq. (2) can be performed, with respect to the voltage V, to obtain the charge. The resultant of this integration, plotted in Fig. 2(b), shows the variation in the charge Q as a function of the voltage V.

If a sinusoidal voltage, such as shown in Fig. 2(c), is developed by the amplifier section of the overlay transistor to drive the nonlinear capacitance $C_{bc}$, a highly distorted charge, or current, waveform is produced because of the non-linear charge-voltage characteristics of the capacitance. This waveform, shown in Fig. 2(d), contains components of the fundamental frequency and of harmonic frequencies. Output power at the desired harmonic is obtained when suitable selective circuits are coupled to the collector of the transistor. In an actual circuit, the driving voltage developed by the transistor

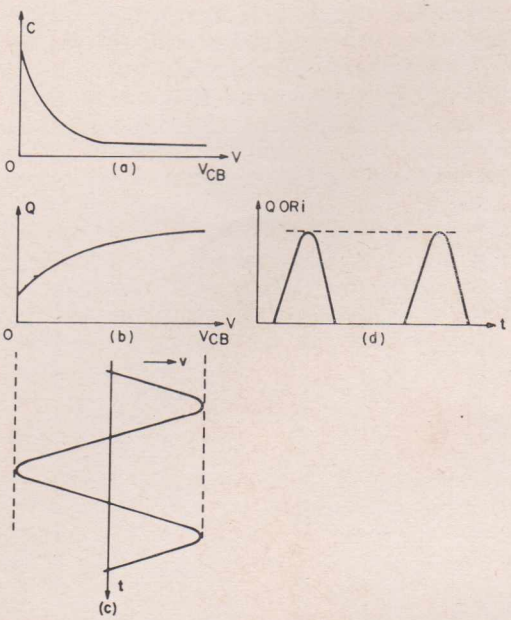



*FIG. 2.—Energy transfer relationships for an overlay transistor in a frequency-multiplier circuit: (a) Capacitance-voltage curve for the collector-to-base junction; (b) Charge-voltage curve of the collector-to-base junction; (c) Sinusoidal voltage developed by the amplifier section of the transistor to drive the nonlinear collector-to-base capacitance; (d) Distorted charge, or current, waveform produced by the nonlinear collector-to-base capacitance in the generation of harmonic power.*

contains both fundamental- and harmonic-frequency components.

Overlay transistors used in frequency multipliers may be connected in either common-base or common-emitter circuit configurations. In the common-base transistor frequency multiplier, harmonic generation is accomplished in essentially the same way as in a shunt-type varactor frequency multiplier, because the nonlinear collector-to-base capacitance of the transistor is connected in shunt with the input circuit. In the common-emitter transistor frequency multiplier, the nonlinear capacitance is connected in series with the input; the operation of the transistor circuit is then similar to that of the series-type varactor frequency multiplier.

Fig 3(a) shows the basic circuit configuration for the use of an overlay transistor in a common-base frequency doubler. A "T" matching network, or other type of matching section, must be used in the input of the doubler to set up a conjugate match across the emitter-base terminals of the transistor at the fundamental frequency of the input driving power. This conjugate match is required to obtain a maximum transfer of power from the driving source to the transistor. Because gain at the fundamental frequency is of primary importance, an idler circuit must be connected between the collector and base of the transistor. The idler loop, which consists of a simple series LC circuit, resonates with the transistor collector-to-base capacitance at the fundamental frequency and thus enhances the flow of fundamental current through the transistor. The idler circuit also develops the driving voltage required by the nonlinear collector-to-base capacitance for the generation of harmonic power. A suitable output circuit, which is series tuned to select output power at the second harmonic

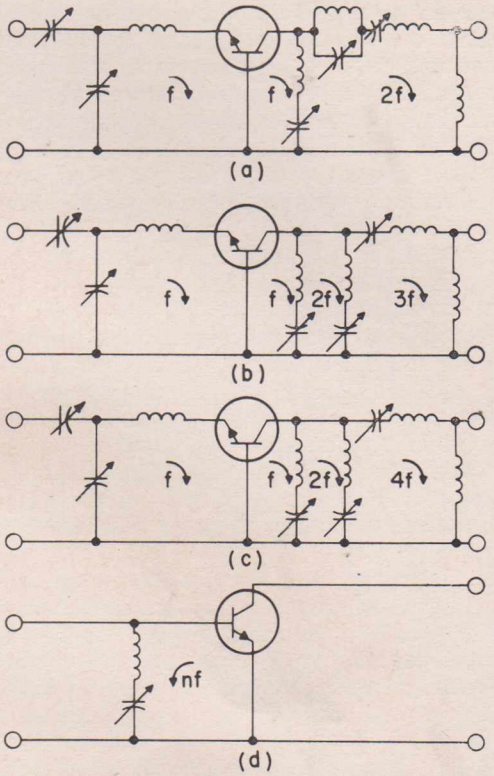



*FIG. 3.—Basic circuit configurations of overlay-transistor frequency multipliers: (a) Common-base frequency doubler; (b) Common-base frequency tripler; (c) Common-base frequency quadrupler; (d) Input-circuit arrangement for a common-emitter frequency multiplier.*

of the input frequency, completes the basic doubler circuit. In some circuits, an output trap must be added to restrict the flow of fundamental-frequency current in the output loop.

Figs. 3(b) and 3(c) show the basic circuits for the use of an overlay transistor in the common-base frequency tripler and quadrupler, respectively. These circuits are very similar to the common-base doubler, with the exception that an additional second-harmonic idler loop is connected in shunt with the transistor collector. The second-harmonic components produced by this idler loop beat with the fundamental-frequency components to generate additional harmonic outputs. In this way, the second-harmonic idler loop enhances the conversion efficiency.[3]

When an overlay-transistor frequency multiplier is used in a common-emitter circuit, an additional series resonant circuit must be incorporated in the input to provide a ground return for the nonlinear capacitance, $C_{bc}$, as shown in Fig. 3(d). Otherwise, the input, output, and idler circuits of common-emitter multipliers follow the considerations already described for the common-base multipliers.

## DESIGN OF OVERLAY-TRANSISTOR MULTIPLIERS

The design of transistor frequency multiplier circuits generally consists of the selection of a suitable transistor and the design of proper filtering and matching networks required for optimum circuit performance.

Transistors suitable for this application must provide the desired output power and gain at the fundamental frequency and must be able to convert the power from the fundamental frequency into power at the desired harmonic frequency. If a lossless circuit were coupled to a lossless nonlinear capacitance $C_{bc}$, power at the fundamental frequency could be converted into power at any harmonic frequency with 100 per cent. conversion efficiency, according to the energy relation derived by Manley and Rowe. In practice, however, the conversion efficiency is limited by the series resistance associated with the nonlinear capacitance and the circuit losses. It can be considered that the harmonic output power of a transistor multiplier circuit, as a given input power level, is equal to the product of the power gain of the transistor at the drive frequency and the conversion efficiency that results from the varactor action of the collector-to-base capacitance, $C_{bc}$. Conversion gain can be obtained only if the power gain of the transistor at the fundamental frequency is larger than the conversion loss.

In the design of such circuits, the input impedance at the fundamental frequency, as seen across the emitter-to-base junction of the transistor, as well as the load impedance presented to the collector at both the fundamental and harmonic frequencies, must be known. The knowledge of the collector load impedance at the harmonic frequency is required for the design of the output circuit. The knowledge of collector impedance at the fundamental frequency is needed in order to determine the input impedance of the transistor at that frequency so that the matching networks between the driving source and the transistor can be properly designed. The three impedances of course are inter-related and are functions of the operating power level, i.e., are determined by voltage and current swings. Once these impedances are established, the design of the matching networks is straightforward.[2,3] For the input circuit, a matching section having low-pass characteristics is preferred, and for the output circuit, a matching section having high-pass or band-pass characteristics is preferred. Such arrangements will insure good isolation between input and output circuits. As the desired frequency of operation increases to above 800 Mc/s, the design of transistor multiplier circuits requires the use of distributed circuit techniques. A fore-shortened quarter-wavelength coaxial cavity is found to be very useful.

## STABILITY AND BIASING CONSIDERATIONS IN OVERLAY-TRANSISTOR MULTIPLIERS

In general, the major problem of nonlinear devices is instability. Various types of instabilities can be incurred in transistor frequency-multiplier circuits. These include hysteresis, low-frequency oscillations, parametric oscillations, and high-frequency oscillations. These difficulties can be eliminated or minimized by careful design of the bias circuit, by the proper location of transistor ground connections, and by the use of common-emitter circuit configurations.

Hysteresis refers to discontinuous mode jumps in output power that occur when the input power or frequency is increased or decreased. It has been determined that this effect is caused by the dynamic detuning which results from the variation in the average value of the nonlinear junction capacitance with rf voltage. The tuned circuit will have a different resonant frequency for a strong drive input than for a weak drive input. It has been found experimentally that hysteresis effects are minimized and sometimes eliminated when the transistor is used in a common-emitter circuit configuration.

Low-frequency oscillations occur because the gain of the transistor at low frequencies is much higher than that at the operating frequency. This effect can be eliminated by placing a small resistance in series with the rf chokes used for the biasing circuit, as shown in Fig. 4.

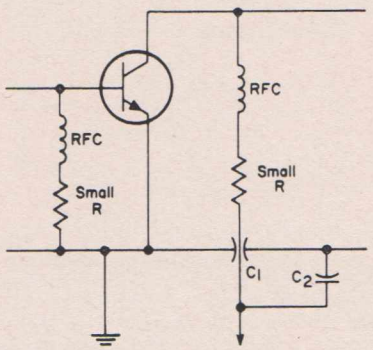



*FIG. 4—Circuit showing the biasing arrangement and bypass capacitances that are used to eliminate instabilities in common-emitter frequency multipliers.*

Parametric oscillations result because spurious low-frequency modulation is added to the harmonic output. This effect can be eliminated by carefully selecting the bypass capacitance, C2 in Fig. 4, to provide a low impedance to the spurious component in addition to that provided by the bypass capacitance C1.

Perhaps the most troublesome instability in transistor frequency-multiplier circuits is the high frequency oscillation. This type of instability is indicated by oscillations that occur at a frequency very close to the multiplier output frequency when the input drive power is removed. Common-emitter circuits were found to be less critical in this respect than common-base circuits. The high frequency oscillations were also found to be strongly related to the input drive frequency. This type of instability can be eliminated if the input frequency is kept below certain values. The input frequency at which stable operation can be obtained seems to depend on the method of grounding the emitter of the transistor. The highest frequency of operation can be obtained when the emitter has the shortest path to ground.

In practice, stable and reliable operation of transistors in frequency multipliers has been successfully obtained. The frequency multipliers discussed in the following section are all stable circuits.

## PRACTICAL TRANSISTOR FREQUENCY-MULTIPLIER CIRCUITS

The introduction of the RCA-2N4012 overlay transistor has led to the design of frequency-multiplier circuits which supply a minimum of 2.5 watts of harmonic output power, at frequencies up to 1 Gc/s, with conversion

gains greater than 4 dB. In a common-base power amplifier, which has a higher upper-frequency limit than a comparable common-emitter amplifier, a typical 2N4012 transistor provides unity gain at 850 Mc/s with an input driving power of 1 watt. With the same transistor used in a frequency-multiplier circuit, the upper limit of the frequency range over which signal power can be obtained is extended far beyond that of the power amplifier and well into the L-band range.

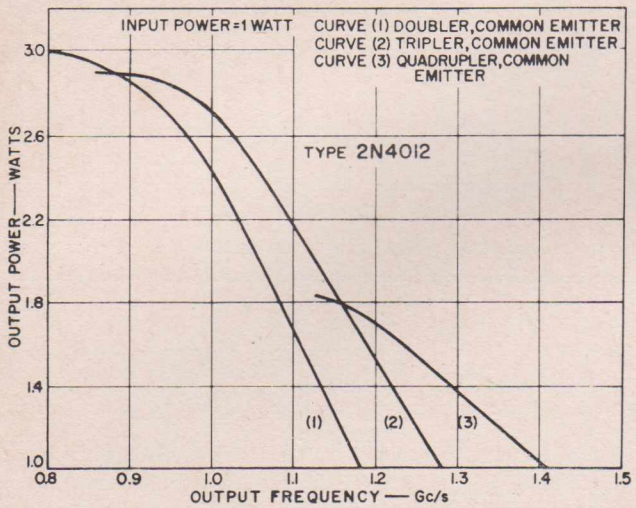



*FIG. 5.—Power-output capabilities of the RCA-2N4012 overlay transistor as a function of frequency when operated in common-emitter doubler, tripler, and quadrupler circuits.*

Fig. 5 shows the power-output capabilities as a function of output frequency for a typical 2N4012 transistor used in common-emitter circuit configurations for frequency doubling, tripling, and quadrupling. In a common-emitter doubler circuit, the transistor will deliver 3.0 watts of output power at 800 Mc/s with a conversion gain of 4.8 dB. In a common-emitter tripler circuit, the transistor will supply 2.7 watts of output power at 1 Gc/s with a conversion gain of 4.3 dB. In a common-emitter quadrupler circuit, the transistor will provide 1.7 watts of output power at 1200 Mc/s with a conversion gain of 2.3 dB.

It is of interest that the transistor frequency multipliers provide greater power outputs at higher output frequencies than the unity-gain output obtained from the transistor power amplifier at 850 Mc/s. When the frequency of operation is low enough so that the transistor can supply rf power with substantial gain, the output capabilities of the transistor frequency multipliers are essentially the same as those of the transistor power amplifier. For operation at the same output frequency and with the same input driving power, approximately equal amounts of output power will be obtained.

In the following paragraphs, circuit arrangements are shown and performance data are given for several practical frequency-multiplier circuits that use the 2N4012 transistor. These circuits include a 200-to-400-Mc/s doubler, a 400-to-800-Mc/s doubler, a 150-to-450-Mc/s tripler, a 340-to-1020-Mc/s tripler, and a 300-to-1200-Mc/s quadrupler. As mentioned previously, the design of multiplier circuits that have an output frequency of 800 Mc/s, or higher, requires the use of distributed-circuit techniques. All such high-frequency circuits described here use coaxial-cavity output circuits. These circuits are discussed first. The low-frequency circuits, which use lumped-element output circuits, are then described.

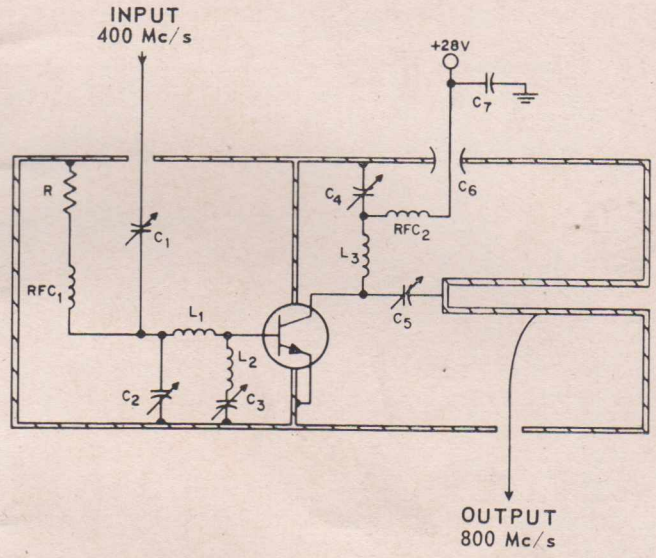



*FIG. 6.—400-to-800-Mc/s, common-emitter transistor frequency doubler.*

## 400-to-800-Mc/s Doubler

Fig. 6 shows the complete circuit diagram of a 400-to-800-Mc/s doubler that uses the RCA-2N4012 transistor. This circuit uses lumped-element input and idler circuits and a coaxial-cavity output circuit. The transistor is placed inside the cavity with its emitter properly grounded to the chassis. A "$\mu$" section (C1, C2, L1, L2, and C3) is used in the input to match the impedances, at 400 Mc/s, of the driving source and the base-emitter junction of the transistor. L2 and C3 provide the necessary ground return for the nonlinear capacitance of the transistor. L3 and C4 form the idler loop for the collector at 400 Mc/s. The output circuit consists of an open-ended $1\frac{1}{4}$-inch-by-$1\frac{1}{4}$-inch square coaxial cavity. A lumped capacitance, C5 (Johanson Type JMC 2954), is added in series with a $\frac{1}{4}$-inch hollow centre conductor of the cavity near the open end to provide adjustment for the electrical length. Output power at 800 Mc/s is obtained by direct coupling from a point near the shorted end of the cavity. The bias arrangement is the same as used in the circuit shown in Fig. 4.

Fig. 7 shows the output power at 800 Mc/s as a function of the input power at 400 Mc/s for the doubler circuit, which uses a typical 2N4012, operated at a collector supply voltage of 28 volts. The curve is nearly linear at an output power level between 0.9 and 2.7 watts. The power output is 3.3 watts at 800 Mc/s for an input drive of 1 watt at 400 Mc/s and rises to 3.9 watts as the input drive increases to 1.7 watts. The collector efficiency, which is defined as the ratio of the

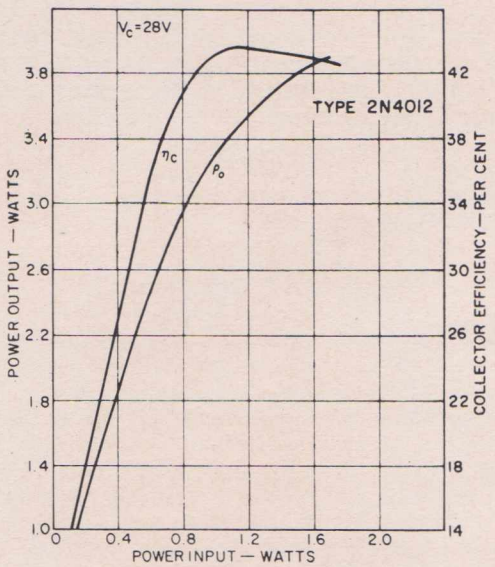



*FIG. 7.—Output power and collector efficiency as a function of the input power for the 400-to-800-Mc/s frequency doubler.*

rf output power to the dc input power at a supply voltage of 28 volts, is also shown in Fig. 7. The efficiency is 43 per cent. measured at an input power of 1 watt. The 3-dB bandwidth of this circuit measured at an output power of 3.3 watts is 2.5 per cent. The fundamental frequency component measured at an output power level of 3.3 watts is 2 dB down from the output carrier. Higher attenuations of spurious components can be achieved if more filtering sections are used.

The variation of output power with collector supply voltage at an input drive level of 1 watt is shown in Fig. 8. This curve is obtained with the circuit tuned at 28 volts.

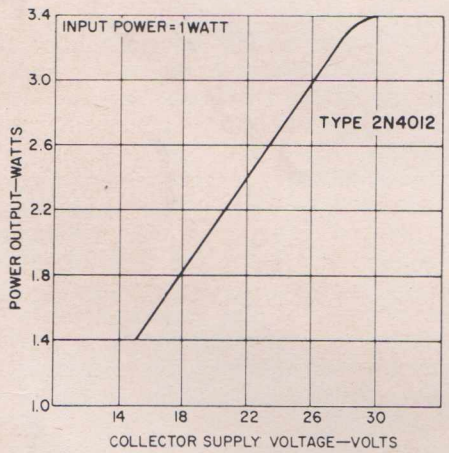



*FIG. 8.—Power output as a function of the collector supply voltage for the 400-to-800-Mc/s frequency multiplier.*

## 340-to-1020-Mc/s Tripler

The 340-to-1020-Mc/s tripler shown in Fig. 9 is essentially the same as the doubler described in the previous section with the exception that an additional idler loop, which consists of L4 and C6, is added in shunt with the collector of the transistor. This idler loop is resonant with the transistor junction capacitance at the second harmonic frequency (680 Mc/s) of the drive input.

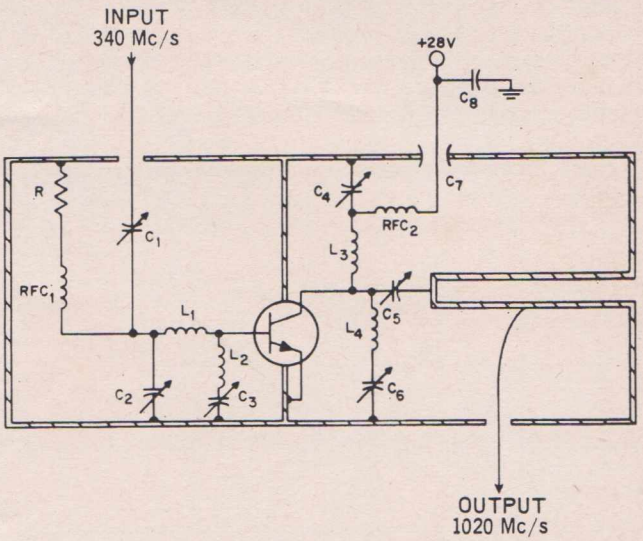



*FIG. 9.—340-to-1020-Mc/s, common-emitter transistor frequency tripler.*

Fig. 10 shows the output power of the tripler at 1020 Mc/s as a function of the input power at 340 Mc/s. This circuit also uses a typical 2N4012 transistor operated at a collector supply voltage of 28 volts. The solid-line curve shows the power output obtained when the circuit is retuned at each input power level. The dashed-line curve shows the power output obtained

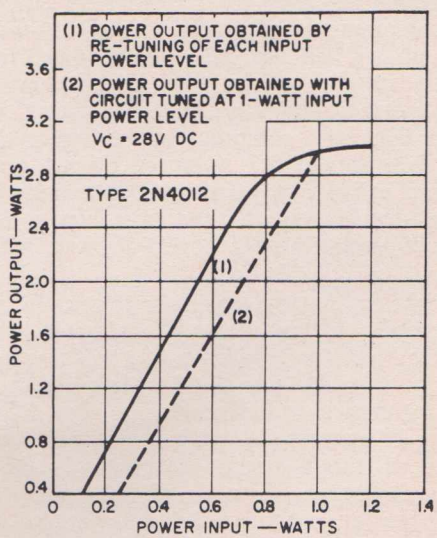



*FIG. 10.—Power output as a function of power input for the 340-to-1020-Mc/s frequency tripler.*

with the circuit tuned at the 2.9-watt output level. An output power of 2.9 watts at 1020 Mc/s is obtained with 1 watt of drive at 340 Mc/s. The 3-dB bandwidth measured at this power level is 2.3 per cent. The spurious frequency components measured at the output are as follows: at 340 Mc/s — 22 dB; at 680 Mc/s — 30 dB; at 1360 Mc/s — 35 dB.

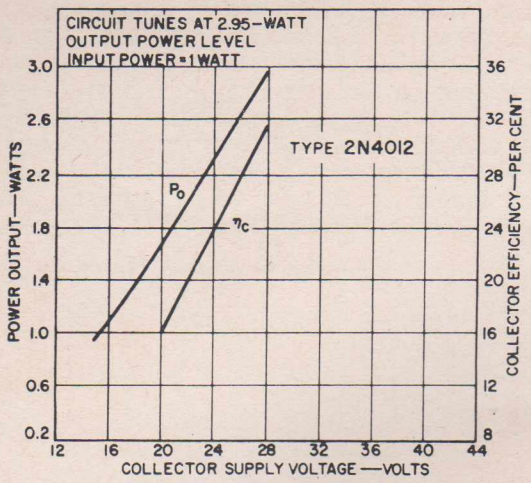



*FIG. 11.—Power output as a function of the collector voltage for the 340-to-1020-Mc/s frequency tripler.*

The variation of output power with collector supply voltage at an input drive level of 1 watt is shown in Fig. 11. The variation of collector efficiency is also shown. These curves are obtained with the circuit tuned at 28 volts.

The 2N4012 transistor in this tripler circuit with 1 watt of drive provides a minimum output of 2.5 watts, a median output of 2.8 watts, and a maximum output of 3.5 watts.

A 340-Mc/s amplifier that used the same circuit configuration and components as those of the tripler circuit shown in Fig. 9 was constructed in order to compare the performance between amplifier and tripler. The conversion efficiency for a large number of tripler units was then measured. The conversion efficiency of the tripler is defined as the 1020-Mc/s power obtained from the tripler divided by the 340-Mc/s power obtained from the amplifier at the same input power level (1 watt). The efficiency varies between 60 to 75 per cent., and averages at 65 per cent, which is comparable to a good varactor multiplier in this frequency range.

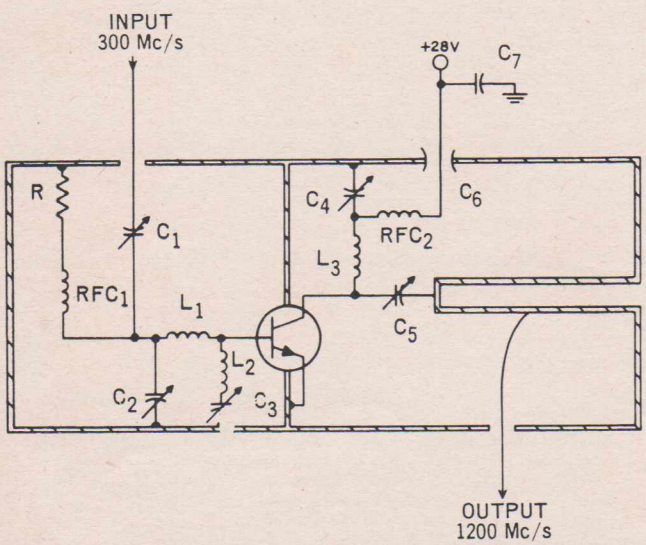



*FIG. 12.—300-to-1200-Mc/s, common-emitter frequency quadrupler.*

## 300-to-1200-Mc/s Quadrupler

The circuit diagram of a 300-to-1200-Mc/s quadrupler is shown in Fig. 12. This circuit is similar to the tripler circuit just described except for the reduced length in the output cavity. Table 1 compares the performance of the 2N4012 in the tripler and quadrupler circuits.

## Table 1

Tripler and Quadrupler Performance of a 2N4012 Overlay Transistor

| Transistor | Pin | Tripler $P_o$ ($f_o$ = 1020 Mc/s) | Quadrupler $P_o$ ($f_o$ = 1200 Mc/s) |
|---|---|---|---|
| 1 | 1 W | 3.0 W | 1.95 W |
| 2 | ↓ | 2.3 | 1.80 |
| 3 | | 2.8 | 1.70 |
| 4 | | 2.3 | 1.50 |
| 5 | | 2.9 | 1.30 |
| 6 | | 2.6 | 1.20 |

## 200-to-400-Mc/s Doubler Circuit

Fig. 13 shows the circuit diagram of a 200 to 400 Mc/s frequency doubler that uses the 2N4012 transistor. The input coupling network consists of a lumped-element

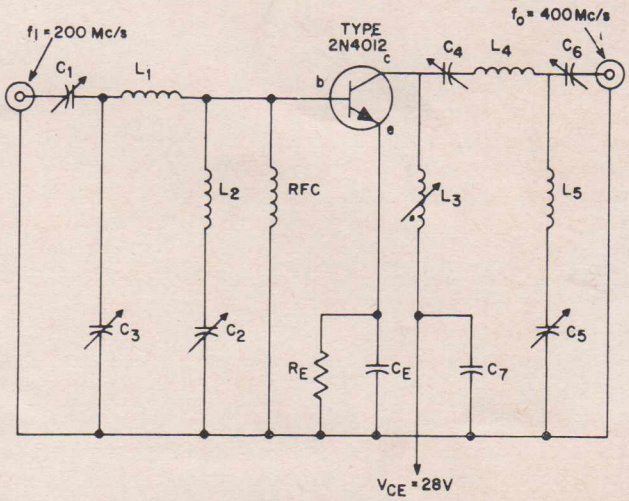



*FIG. 13.—200-to-400-Mc/s, common-emitter transistor frequency doubler.*

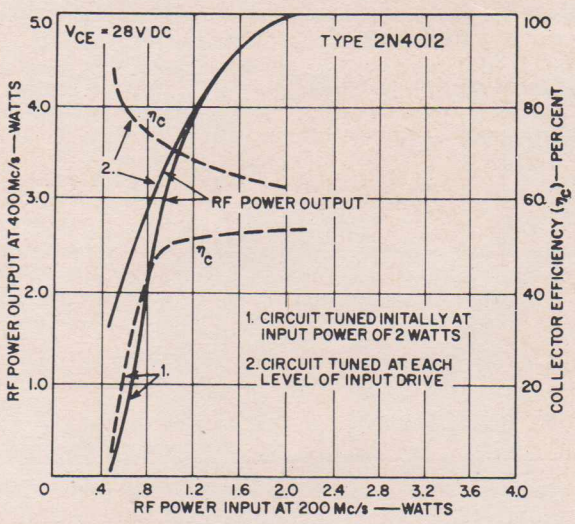



*FIG. 14.—Power output and collector efficiency as a function of input power for the 200-to-400-Mc/s frequency doubler.*

circuit (C1, C2, C3, L1, and L2). This circuit matches the impedance of the driving source to that of the base-to-emitter input circuit of the transistor at the input frequency of 200 Mc/s. The network formed by C2 and L2 provides a short circuit return path at 400 Mc/s for the harmonic output current. The collector output network consists of lumped elements C4, C5, C6, L3, L4 and L5. The network formed by lumped elements C4, C5, C6, L4 and L5 provides the proper load coupling to the collector circuit at 400 Mc/s. Fig. 14 shows the curves of power output from the doubler at 400 Mc/s for various input driving power levels at

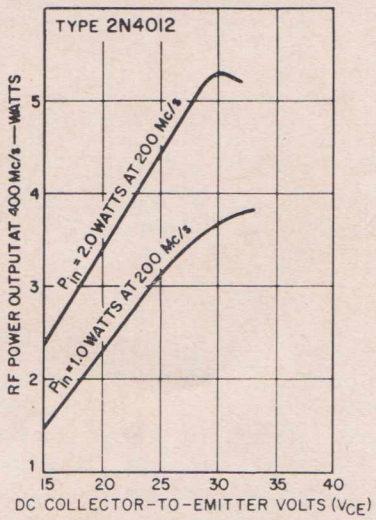



*FIG. 15.—Power output as a function of collector supply voltage for the 200-to-400-Mc/s frequency doubler.*

200 Mc/s. Fig. 15 shows the variation of power output at 400 Mc/s with dc supply voltage for input power drive levels of one and two watts at 200 Mc/s. The rejection of fundamental (200 Mc/s) and third-harmonic components in the output circuit were measured to be 25 dB below the 400 Mc/s power output of 3.3 watts.

## 150-to-450-Mc/s Tripler Circuit

Fig. 16 illustrates the use of the 2N4012 transistor in a 150-to-450-Mc/s frequency tripler. The input coupling network has been designed to match the driving gen-

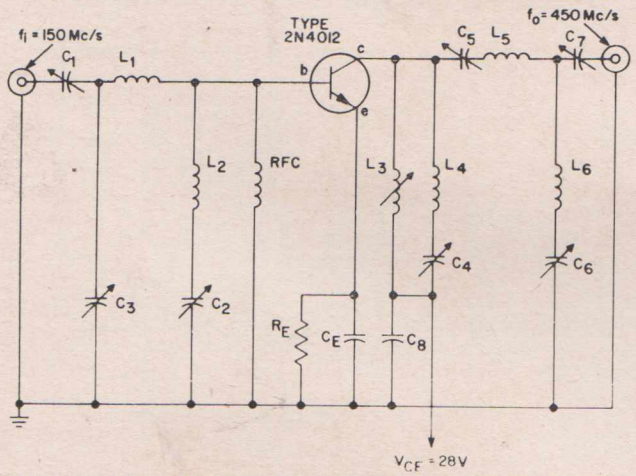



*FIG. 16.—150-to-450-Mc/s, common-emitter transistor frequency tripler.*

erator to the base-to-emitter circuit of the transistor. The network formed by C2 and L2 provides a short-circuit return for harmonic output current at 450 Mc/s. The idler network in the collector circuit, formed by L3, L4 and C4, is designed to circulate fundamental and second harmonic components of current through the voltage-variable collector-to-base capacitance, $C_{bc}$. The network formed by C5, C6, C7, L5 and L6 provides the required collector loading for 450-Mc/s output power.

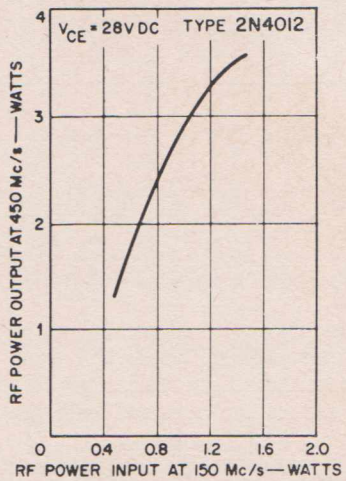



*FIG. 17.—Power output as a function of power input for the 150-to-450-Mc/s frequency tripler.*

Fig. 17 shows the 450-Mc/s power output of the tripler as a function of the 150-Mc/s power input. For one watt of driving power, 2.8 watts of output power was obtained at 450 Mc/s. The rejection of fundamental, second, and fourth harmonics was measured as 30 dB below the 2.8-watt, 450-Mc/s level. The variation of power output with supply voltage is shown in Fig. 18.

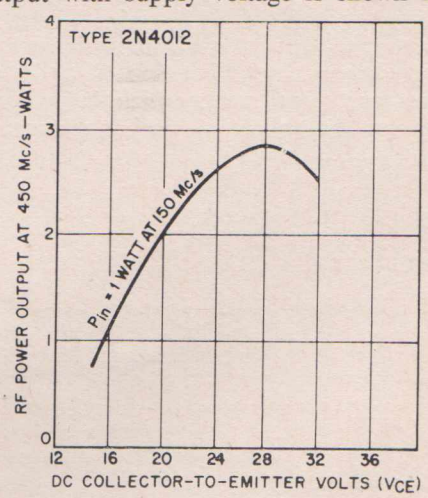



*FIG. 18.—Power output as a function of the collector voltage for the 150-to-450-Mc/s frequency tripler.*

## COMPARISON OF COMMON EMITTER AND COMMON BASE MULTIPLIER CIRCUITS

The performance data given in the preceding section were all obtained from frequency multipliers in which

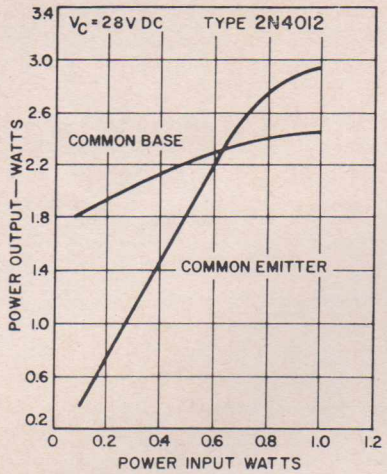



*FIG. 19.—Power output as a function of power input for common-base and common-emitter circuit configurations of a 340-to-1020-Mc/s transistor frequency tripler.*

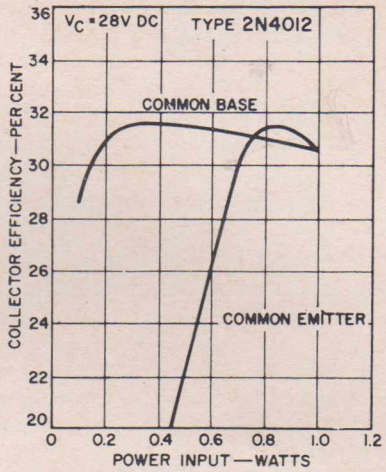



*FIG. 20.—Collector efficiency as a function of input power for common-base and common-emitter circuit configurations of a 340-to-1020-Mc/s transistor frequency tripler.*

the transistor is connected in common-emitter circuit configurations. When transistors are used in common-base circuit configuration, different results are obtained. Figs. 19 and 20 show the performance comparison between a common-base and a common-emitter tripler circuit using a 2N4012 transistor. At low power levels, the common base tripler provides higher gain and collector efficiency, whereas at high power levels, both higher gain and collector efficiency are provided by the common emitter circuit. At an input power of 1 watt at 340 Mc/s, the comon emitter tripler delivers 2.9 watts of power at 1020 Mc/s and the common base circuit, 2.4 watts. The collector efficiencies for both circuits are approximately the same, over 30 per cent. The 3-dB bandwidth measured in the common-emitter tripler is 2.3 per cent, as compared to 2.5 per cent. in a common-base tripler. The major difference in the two circuits is in that the output power of the common-emitter tripler saturates at a much higher input power level than that of the common-base circuit. This effect has also been observed in a straight-through amplifier. In addition, the common-emitter circuit is less sensitive to hysteresis and high-frequency oscillations as discussed in the early section.

## CONCLUSIONS

It is apparent from Fig. 5 that in a transistor frequency multiplier the order of multiplication has an important bearing on the amount of output power that can be supplied. For a given multiplier circuit, the highest output power is obtained at the frequency for which the product of power gain and conversion efficiency has the largest value. Fig. 5 shows that when an RCA-2N4012 overlay is used, maximum output power is obtained at 800 Mc/s from a doubler circuit, at 1000 Mc/s from a tripler circuit, and at 1300 Mc/s from a quadrupler circuit.

The data given in this paper have shown that the performance of overlay-transistor frequency multipliers is approaching that obtained from varactor frequency multipliers operated in the L-band. In comparison to the varactor circuit, however, the transistor multiplier is a simpler and less costly circuit and consumes smaller amounts of dc power.

(WITH ACKNOWLEDGEMENT TO RCA)

## REFERENCES

1. Canton, M., Sobol, H., and Ernst, R. L., "Generation of Microwave Power by Parametric Frequency Multiplication in a Single Transistor", *RCA Review*, Vol. XXVI, June, 1965.
2. Minton, Robert, "Design of Large-Signal VHF Transistor Power Amplifiers", RCA Application Note SMA-36, RCA Electronic Components and Devices, Harrison, N.J.
3. Lee, H. C., "VHF Power Sources Using Varactor Multipliers," RCA Application Note SMA-22, RCA Electronic Components and Devices, Harrison, N.J.

## ERRATA

In Radiotronics, July 1965, a circuit was shown for an input stage preamplifier intended for magnetic pick-up cartridges. Construction of a number of these units in the intervening period has shown that the isolation of $Q_I$ (Fig. 2, page 127) from low frequency components on the power supply allowed an insufficient margin of stability when no pick-up was connected to the input.

Accordingly it is recommended that users of this arrangement increase the time constant of the filter to the base of $Q_I$ by changing the 5.6 KΩ resistor to 15 KΩ and the 25 μF capacitor to 250 μF.

# A Hidden Clock in Every Bush

**The clock that is hidden in every bush speaks the language of atoms. Nuclear radiation meters are commonly used today in a carbon-dating process to determine the age of objects, a technique that has been of enormous assistance in such fields as archaeology. This is a typical story of carbon dating, complete with an interesting twist.**

Students of Heidelberg University recently cut down some bushes along the motorway to Frankfurt, and took their booty home to the laboratory. However, it was not a student's rag, but scientific work with a surprising result. Some pieces of good heartwood were cut out of the bushes and burnt under control. What the students needed was the carbon, which is an important constituent of all living matter. The examination of the carbon took some days and the result was: the bushes examined were three thousand two hundred years old, with an accuracy of plus or minus 180 years, according to the determination of their age by their $C^{14}$ content.

This result was naturally nonsense. In reality they could only have been a few years old at the most. But the method of age determination, which already proved excellent in many cases, indicated a "doctored" result. Nevertheless they were extremely pleased with their test. It proved the assumption that the air along the borders of the motorway was not exclusively fresh, natural air, but originated in large part from the exhausts of cars.

Now what has the determination of age got to do with exhaust gases? The plants absorb the carbon from the ambient air, principally the inactive carbon atoms $C^{12}$ and $C^{13}$, which, however, contains a tiny portion of the radioactive isotope $C^{14}$ caused by cosmic rays in the atmosphere. The change of $C^{14}$ concentration in plants allows conclusions to be drawn about their age.

In free air the ratio of $C^{14}$ to inactive carbon remains constant. Part of the $C^{14}$ decays constantly. Of a thousand $C^{14}$ atoms only 500, i.e. half, are present after approximately 5,000 years. A further 5,000 years later, again only about half are present, i.e. half of half. The figure is called the half-life. But in nature decaying atoms are always replaced by new ones so that an equilibrium is created.

However, in the course of time the carbon contained in the plants loses its $C^{14}$ content. Extremely sensitive measuring equipment is required to ascertain how much $C^{14}$ is still present. It can be detected by its radiation. Telefunken engineers have designed measuring equipment which can detect even the slightest traces of $C^{14}$. The ages of archaeological remains have been determined up to 20,000 years.

But to return to the bushes. They had absorbed carbon from petrol exhaust gases, carbon that was millions of years old. And that explains why their clocks were wrong.

### Material testing and protection against radiation

There are many natural clocks of this description. By means of the radiation from the hydrogen isotope tritium it can be determined whether a wine is ten years old or only one. Uranium reveals to us the age of rocks billions of years old. After hearing a radiation counter ticking, a scientist said: "In every stone, in every bush, there is a clock. But it ticks so softly that we need complicated measuring instruments to hear it."

Nuclear radiation meters are used for innumerable applications. Not only scientific investigations in chemistry, biology, medicine and physics are facilitated by these instruments. Their use is also constantly growing in industry for quality checks, non-destructive material tests and, above all, for protection against nuclear radiation. Typical examples are digital autoscalers, counting rate meters, reflecting cell probes and sample changers. How small the radiation quantities are and how sensitive the equipment, was shown during a demonstration of a radiation meter at an African university. The director of the demonstration had a brick brought from a building site near by. When he held the probe on the brick a real drum-fire of pulses started in the loudspeaker because tiny quantities of radioactivity are present in nature everywhere. The test instruments are so sensitive nowadays that harmless small quantities of radiation may be used for tests.

# Horizontal AFC Test Unit

**This is one of a number of articles being specially prepared for "Radiotronics", based on reports prepared in the AWV Applications Laboratory at Rydalmere, N.S.W. This article is based on AWV Applications Laboratory Report VR101, under the same title, by J. Van der Goot and R. Walton.**

**This instrument has been designed to assist in the evaluation of afc systems in television receivers. The unit allows the measurement of the "hold-in" and "lock-in" ranges of the system, in cycles per second, either side of 15,625 cps. Applications of this unit are found in the production testing and laboratory development of horizontal afc systems. The unit provides horizontal synchronising pulses which enable the evaluation of afc systems without the need to provide a composite video signal.**

## Principle of Operation

The unit consists of an oscillator, the frequency of which is variable approximately ± 3000 cps about a centre frequency of 31,250 cps. Pulses derived from the plate circuit of this oscillator are differentiated and their pulse repetition frequency is halved by a bistable multivibrator (binary counter). These pulses are then utilised to drive a monostable multivibrator which produces negative-going output pulses of adjustable width and amplitude to simulate horizontal synchronising pulses.

A sinusoidal output is derived from the variable oscillator and fed to a mixer stage to which is also applied a sinusoidal voltage derived from a crystal controlled oscillator operating at 31,250 cps. The output of the mixer is detected and applied to an audio frequency meter whose calibration has been adjusted to read half the applied frequency, thereby giving the actual deviation of the frequency of the output pulses either side of 15,625 cps.

The frequency of the variable oscillator can then be made equal to that of the crystal oscillator by adjusting its frequency to produce a zero beat as indicated by a neon lamp. The variable oscillator suddenly locks in on the crystal controlled oscillator when the difference frequency becomes approximately 8 cps. This will limit the measurement of afc performance to frequencies outside the range of 15,625 ± 8 cps.

The circuit diagram of the horizontal afc test unit is shown in two accompanying figures, one of which shows the oscillator section and the other of which shows the audio frequency meter section. Both sections are provided with their own power supply arrangements and are thus integral units in themselves. For example, arrangements could be made quite simply to utilise the audio frequency meter alone and so extend its utility. A further diagram shows the waveforms present in the unit, keyed to the measurement points keyed on the circuit.

## Performance

The basic performance of the test unit may be summarised as follows:

**Variable Oscillator.**

| | |
|---|---|
| Centre frequency .. .... | 31,250 cps. |
| Deviation, approximate | ± 3,000 cps. |

**Output Pulse.**

| | |
|---|---|
| Deviation, approximate | ± 1,500 cps. |
| Maximum width .. .... | 5.4 μsecs. |
| Minimum width .. .... | 4.3 μsecs. |
| Maximum amplitude .. | 4.0 volts |
| Minimum amplitude .... | zero volts |

The crystal oscillator is a standard circuit used in AWA equipment. The audio frequency meter is similar to that used in the AWA Series 8828 Audio Frequency Meters, with the modification mentioned. Clockwise rotation of the PRF controls decreases the output pulse repetition frequency. The purpose of the S/C button is to provide convenient means to remove the output pulses from the terminals by short-circuiting the output. This feature greatly facilitates some of the tests which are described later.

## Standard Tests

The International Electrotechnical Commission have defined three tests for the measurement of afc systems of television receivers. From their Publication No. 107, sub-section 6.2.3, dealing with synchronising range, lock-in range, hold-in range and following range, the synchronising range and its component properties are defined as follows:

"The synchronising range is the range over which the synchronisation signals are able to control the frequency of the time base circuits. When the synchronisation control knob is rotated through its range, for instance in a clockwise direction, a point is reached where the time base circuit is synchronised. Additional rotation produces another point where synchronisation is lost. By rotating the synchronisation control in an anti-clockwise direction, two more points are found. These points do not normally coincide with the points found previously."

"The lock-in range is the range between the two points at which synchronisation is obtained. The corresponding free-running frequencies are measured. (This may also be expressed as a $+\Delta f$ and $-\Delta f$ cps range on either side of the central oscillator frequency.)"

"The hold-in range is the range between the two points at which synchronisation is lost. The corresponding free-running frequencies are measured. (This may also be expressed as a $+\Delta f$ and $-\Delta f$ cps range either side of the central oscillator frequency.)"

"The following range is the range over which the transmitted line and field frequencies may vary before synchronisation is lost."

The more complete evaluation of afc performance requires the addition of tests to make a series as suggested below:

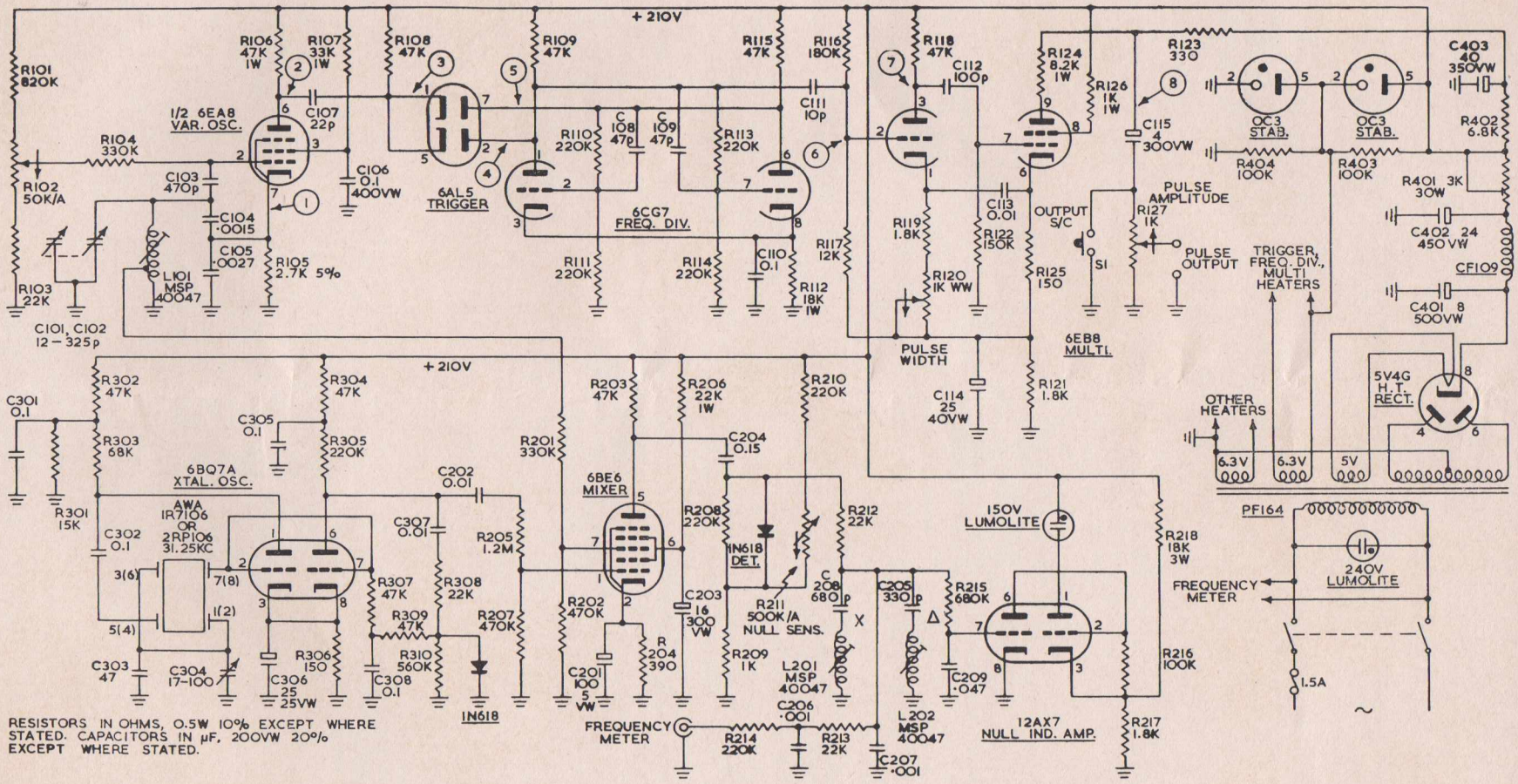
TEST 1. Measurement of lock-in and following range for variable synchronisation pulse repetition frequency and fixed horizontal oscillator frequency with the synchronising signal applied to the video amplifier.

TEST 2. Measurement of hold-in and lock-in range for fixed synchronisation pulse repetition frequency and variable horizontal oscillator frequency with the synchronising signal applied to the video amplifier.

TEST 3. Measurement of following and lock-in range as for Test 2 except that the receiver operates normally on a medium strength rf input signal containing the synchronising information.

TEST 4. Measurement of the free-running drift of the horizontal oscillator during "warm-up".

TEST 5. Measurement of the free-running frequency shift of the horizontal oscillator due to normal supply voltage fluctuations.


+210V
R101 820K
R102 50K/A
R103 22K
R104 330K
R105 2.7K 5%
R106 47K 1W
R107 33K 1W
R108 47K
R109 47K
R110 220K
R111 220K
R112 18K 1W
R113 220K
R114 220K
R115 47K
R116 180K
R117 12K
R118 47K
R119 1.8K
R120 1K WW
R121 1.8K
R122 150K
R123 330
R124 8.2K 1W
R125 150
R126 1K 1W
R127 1K
C101, C102 12-325p
C103 470p
C104 .0015
C105 .0027
C106 0.1 400VW
C107 22p
C108 47p
C109 47p
C110 0.1
C111 10p
C112 100p
C113 0.01
C114 25 40VW
C115 4 300VW
1/2 6EA8 VAR. OSC.
6AL5 TRIGGER
6CG7 FREQ. DIV.
6EB8 MULTI.
L101 MSP 40047
OUTPUT S/C
S1
PULSE AMPLITUDE
PULSE OUTPUT
PULSE WIDTH
OC3 STAB.
OC3 STAB.
R404 100K
R403 100K
R402 6.8K
R401 3K 3W
C403 40 350VW
C402 24 450VW
CF109
C401 8 500VW
TRIGGER, FREQ. DIV., MULTI HEATERS
5V4G H.T. RECT.
OTHER HEATERS
6.3V
6.3V
5V
PF164
240V LUMOLITE
FREQUENCY METER
1.5A
150V LUMOLITE
R218 18K 3W
R216 100K
R217 1.8K
12AX7 NULL IND. AMP.
L202 MSP 40047
C207 .001
C209 .047
R215 680K
C205 330p
C208 680p
R212 22K
R211 500K/A NULL SENS.
IN618 DET.
C204 0.15
C203 16 300 VW
R209 1K
R208 220K
6BE6 MIXER
R203 47K
R206 22K 1W
R210 220K
R201 330K
R202 470K
R204 390
C201 100 5 VW
C206 .001
R213 22K
R214 220K
FREQUENCY METER
+210V
R302 47K
R303 68K
R304 47K
R305 220K
C301 0.1
C305 0.1
C302 0.1
R301 15K
6BQ7A XTAL. OSC.
AWA IR7106 OR 2RP106 31.25KC
C303 47
C304 17-100
C306 25 25VW
R306 150
R307 47K
R308 22K
R309 47K
R310 560K
C307 0.01
C308 0.1
C202 0.01
R205 1.2M
R207 470K
IN618
RESISTORS IN OHMS, 0.5W 10% EXCEPT WHERE STATED. CAPACITORS IN µF, 200VW 20% EXCEPT WHERE STATED.
X 31.25 kc/s TRAP
Δ 62.50 kc/s TRAP

# Operating Instructions

Connect the instrument to a 240-volt 50 cps supply and allow it to warm up for a minimum of 5 minutes before taking measurements. It is important to stipulate the convention for $+\Delta f$ before going further. The convention that has been adopted throughout this article for the sign of the difference between the frequency of the horizontal oscillator and the incoming synchronising pulse repetition frequency is that $\Delta f$ is taken as positive when the free-running frequency of the oscillator is higher than the incoming synchronising pulse repetition frequency.

The various tests listed above will now be detailed in relation to the use of this test instrument.

TEST 1

This test consists of measurement of the following and lock-in ranges for the case where the synchronising pulse repetition frequency is varied and the horizontal deflection oscillator of the receiver has been adjusted to run free at a horizontal frequency of 15,625 cps. The detailed procedure is as follows:

1. With the receiver operating normally on a broadcast transmission observe the output of the synchronisation separator on a CRO. Display one or two horizontal synchronisation pulses on the CRO. Note the pulse amplitude and shape.

2. Render inoperative the if stages of the receiver, either by bypassing to earth the grid of the first and third if stages or by biasing the first (and second if applicable) if stage beyond cutoff.

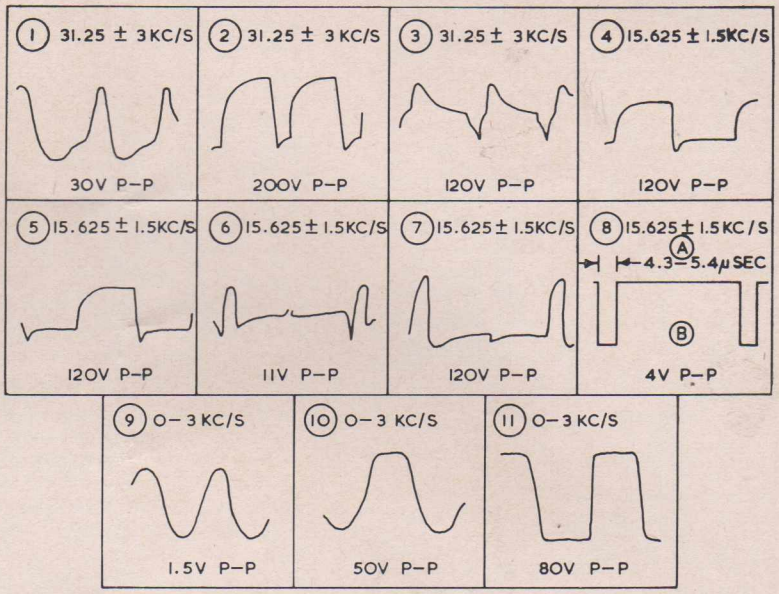
3. Render inoperative any noise gating or noise cancelling devices in the receiver.

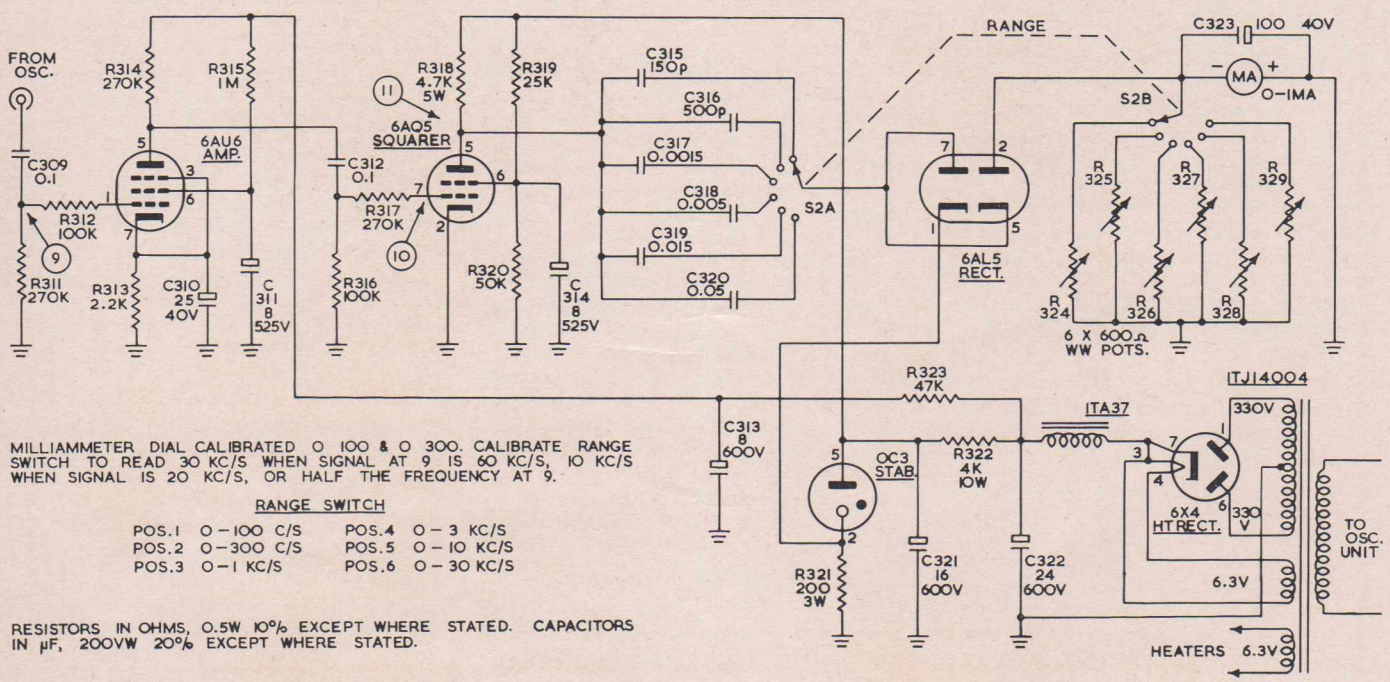
4. Connect the pulse output from the afc test unit to the grid of the video amplifier, adjusting the pulse width to agree with the ABCB standard.

5. Adjust the pulse amplitude until the amplitude and shape at the synchronising separator output are approximately the same as in step 1.

6. Adjust the pulse repetition frequency controls to produce a null on the null indicator. (This sets the synchronising pulse repetition frequency to 15,625 cps.) Then align the horizontal oscillator as outlined in the manufacturer's service data. The audio frequency meter should read very close to zero on the high frequency scales and may register up to 8 cps on the 100 cps scale.

7. Adjust the pulse repetition frequency controls clockwise (this decreases syn-




MILLIAMMETER DIAL CALIBRATED 0 100 & 0 300. CALIBRATE RANGE SWITCH TO READ 30 KC/S WHEN SIGNAL AT 9 IS 60 KC/S, 10 KC/S WHEN SIGNAL IS 20 KC/S, OR HALF THE FREQUENCY AT 9.

RANGE SWITCH

| | | | |
|---|---|---|---|
| POS.1 | 0-100 C/S | POS.4 | 0-3 KC/S |
| POS.2 | 0-300 C/S | POS.5 | 0-10 KC/S |
| POS.3 | 0-1 KC/S | POS.6 | 0-30 KC/S |

RESISTORS IN OHMS, 0.5W 10% EXCEPT WHERE STATED. CAPACITORS IN μF, 200VW 20% EXCEPT WHERE STATED.

chronisation pulse repetition frequency) until horizontal synchronisation is lost in the receiver. The scale of the audio frequency meter should be adjusted to keep the pointer within full scale deflection. The frequency reading corresponding to the point at which synchronisation is lost is the $+\Delta f$ hold-in range.

8. Adjust the pulse repetition frequency controls anti-clockwise until the receiver regains synchronisation. The frequency reading corresponding to oscillator lock-in is the $+\Delta f$ lock-in range. The determination of the point at which the oscillator locks in is facilitated by repetitively depressing the S/C button whilst adjusting the pulse repetition frequency of the synchronising pulses.

9. Adjust the pulse repetition frequency controls anti-clockwise from the null position until the receiver loses synchronisation. The frequency reading corresponding to the loss of synchronisation is the $-\Delta f$ hold-in range of the receiver.

10. Adjust the pulse repetition frequency controls clockwise until the receiver regains synchronisation. The frequency meter now indicates the $-\Delta f$ lock-in range of the receiver.

11. Realign the oscillator for normal operation.

TEST 2

This test comprises measurement of the hold-in and lock-in ranges for the case where the incoming synchronising pulse repetition frequency is fixed at 15,625 pps and the frequency of the horizontal oscillator is varied. Steps 1 to 6 inclusive of the detailed procedure are as for Test 1, followed by:

7. Adjust the core of the oscillator in the direction of increased frequency to the point where synchronisation is lost.

8. Short-circuit the grid of the synchrosation separator to its cathode and adjust the pulse repetition frequency controls anti-clockwise to reduce the number of slanting bars on the picture tube until none is visible. This is the point where the incoming synchronising pulse repetition frequency has been adjusted to equal that of the "off-frequency" horizontal deflection oscillator. The frequency meter now gives the $+\Delta f$ hold-in range.

9. Remove the short circuit from the synchronisation separator and adjust the pulse generator to produce 15,625 pps as previously outlined.

10. Adjust the core of the oscillator to decrease the horizontal sweep frequency until synchronisation is just regained. To locate the exact setting of the core at which this takes place, intermittently remove the synchronising pulses from the video amplifier by pressing the output S/C button and carefully adjusting the oscillator slug.

11. Short-circuit the signal grid of the synchronisation separator to its cathode and adjust the pulse repetition frequency controls anti-clockwise until the horizontal bars on the picture tube become almost stationary as before. The frequency meter now gives the $+\Delta f$ lock-in range.

12. Remove the short-circuit from the synchronisation separator and adjust the pulse generator to produce 15,625 pps as previously outlined.

13. Adjust the core of the oscillator in the direction of decreased frequency to the point where synchronisation is lost.

14. Short-circuit the signal grid of the synchronisation separator to its cathode and adjust the pulse repetition frequency controls clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $-\Delta f$ hold-in range.

15. Remove the short-circuit from the synchronisation separator and adjust the pulse generator to produce 15,625 pps as previously outlined.

16. Adjust the core of the oscillator to increase its frequency until synchronisation is just regained. To locate the exact setting of the core at which this occurs, intermittently removed the synchronising pulses from the video amplifier by pressing the output S/C button and carefully adjusting the oscillator slug.

17. Short-circuit the signal grid of the synchronisation separator to its cathode and adjust the pulse repetition frequency controls anti-clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $-\Delta f$ lock-in range.

18. Remove the short-circuit from the synchronisation separator and adjust the pulse generator to produce 15,625 pps as previously outlined. Realign the oscillator for normal operation.

TEST 3

The procedure here is the measurement of the "hold-in" and "lock-in" range for the conditions of Test 2 (i.e., where the incoming synchronising pulse repetition frequency is fixed at 15,625 pps and the frequency of the horizontal oscillator is varied). The receiver is operated under typical conditions with a medium to strong rf input signal. The actual free-running frequency of the oscillator is measured with the aid of the afc test unit. The detailed procedure is as follows:

1. Apply a medium to strong rf signal to the tuner input.

2. Render inoperative any noise gating or noise cancelling device in the receiver.

3. Adjust the core of the oscillator in the direction of increased frequency to the point where synchronisation is lost.

4. Render the if strip inoperative by applying an appropriate negative bias. Short-circuit the signal grid of the synchronisation separator to its cathode. Apply the pulses from the afc test unit to the grid of the video amplifier and rotate the pulse repetition frequency controls anti-clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $+\Delta f$ hold-in range.

5. Remove the bias from the if strip, remove the short circuit from the grid of the synchronisation separator and disconnect the pulse generator from the video amplifier.

6. Adjust the core of the oscillator to decrease its frequency until synchronisation is just regained. To determine the exact setting of the core at which this occurs, intermittently remove the synchronising pulses by switching the tuner to a vacant channel and carefully adjust the oscillator slug.

7. Render the if strip inoperative by applying an appropriate bias. Short-circuit the signal grid of the synchronisation separator to its cathode. Apply the output from the afc test unit to the grid of the video amplifier and rotate the pulse repetition frequency controls clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $+\Delta f$ lock-in range.

8. Remove the bias from the if strip, remove the short-circuit from the grid of the synchronisation separator and disconnect the pulse generator from the video amplifier.

9. Adjust the core of the oscillator in the direction of decreased frequency to the point where synchronisation is lost.

10. Render the if strip inoperative by applying an appropriate bias. Short-circuit the signal grid of the synchronisation separator to its cathode. Apply the output from the afc test unit to he grid of the video amplifier and rotate he pulse repetition frequency controls clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $-\Delta f$ hold-in range.

11. Remove the bias from the if strip, remove the short-circuit from the grid of the synchronisation separator and disconnect the pulse generator from the grid of the video amplifier.

12. Adjust the core of the oscillator coil to increase its frequency until synchronisation is just regained. To determine the exact setting at which this occurs, intermittently remove the synchronising pulses by switching the tuner

to a vacant channel and carefully adjust the oscillator coil.

13. Render the if strip inoperative by applying an appropriate bias. Short-circuit the signal grid of the synchronisation separator to its cathode. Apply the output from the afc test unit to the grid of the video amplifier and rotate the pulse repetition frequency controls anti-clockwise to reduce the number of slanting bars on the picture tube until none is visible. The frequency meter now indicates the $-\Delta f$ lock-in range.

TEST 4

Here the procedure involves the measurement of the frequency drift of the horizontal oscillator during warm up in the absence of synchronisation. The detailed procedure is as follows:

1. With the receiver operating normally on a broadcast transmission observe the output of the synchronisation separator on a CRO. Display one or two horizontal synchronisation pulses on the CRO. Note the pulse amplitude and shape.

2. Render the if strip of the receiver inoperative by applying an appropriate bias.

3. Render any noise cancelling or noise gating devices in the receiver inoperative.

4. Connect the output from the afc test unit to the grid of the video amplifier.

5. Adjust the pulse amplitude until the amplitude and shape at the synchronisation separator output are approximately the same as those observed in step 1.

6. Adjust the pulse repetition frequency controls to produce a prf of 15,625 cps (null) and then align the horizontal oscillator as specified by the manufacturer.

7. Switch off the receiver and allow it to cool to ambient temperature.

8. Remove the synchronisation pulses from the phase detector by short-circuiting the grid of the synchronisation separator to its cathode.

9. Switch on the receiver and measure the frequency of the oscillator with the aid of the afc test unit by varying the pulse repetition frequency so that it corresponds to the oscillator frequency. Rotate the pulse repetition frequency controls so as to reduce the number of slanting bars on the picture tube until none is visible. The audio frequency meter now indicates the frequency drift.

TEST 5

Test 5 involves the measurement of the free-running frequency shift of the horizontal oscillator circuit due to supply voltage fluctuations. This form of frequency shift follows the variations in the supply voltage rather quickly, but sufficient time should be allowed after the voltage change to permit the cathode temperature of the valves to stabilise.

The receiver should be adjusted for normal operation using the afc test unit as a source of synchronising pulses. The receiver should be prepared as indicated in Test 4 and the measurement commenced when the frequency of the horizontal oscillator has become sufficiently stable. A time interval of approximately one minute should be allowed from the moment the voltage is changed before a frequency measurement is made.

## *Note*

Due to coupling between the variable oscillator and the crystal controlled oscillator the former will lock with the latter when their frequencies are approximately 8 cps apart. The measurement of the frequency of deflection oscillators therefore is inaccurate for frequencies within the range of 15,625 $\pm$ 8 cps.

# PAL Demonstration in London

In response to an invitation by the Institute of Electrical Engineers, Dr. Walter Bruch recently held in London a public lecture with a subsequent discussion on the PAL colour TV system, which he developed as an organic extension and improvement of the American NTSC system.

Dr. Bruch, who has already demonstrated PAL in the U.K. several times, said that the development of the NTSC system was a great technical achievement at that time. But he emphasised that there are a number of factors which do not always ensure optimum picture quality in the practical application (transmission) of the NTSC system. Dr. Bruch explained that the PAL system he has developed embodies all the merits of NTSC and that the experience gathered with NTSC in the U.S.A. can be fully implemented in PAL due to the relationship between the two systems.

With the assistance of the BBC pictures were laid into the demonstration room over a cable link whilst the demonstration was taking place. By means of artificial distortions the better colour stability of PAL was shown in comparison with NTSC.

Just recently the British Radio and TV Manufacturers' Association recommended the general adoption of the PAL system in the future European colour TV services.

# Annual Index 1965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