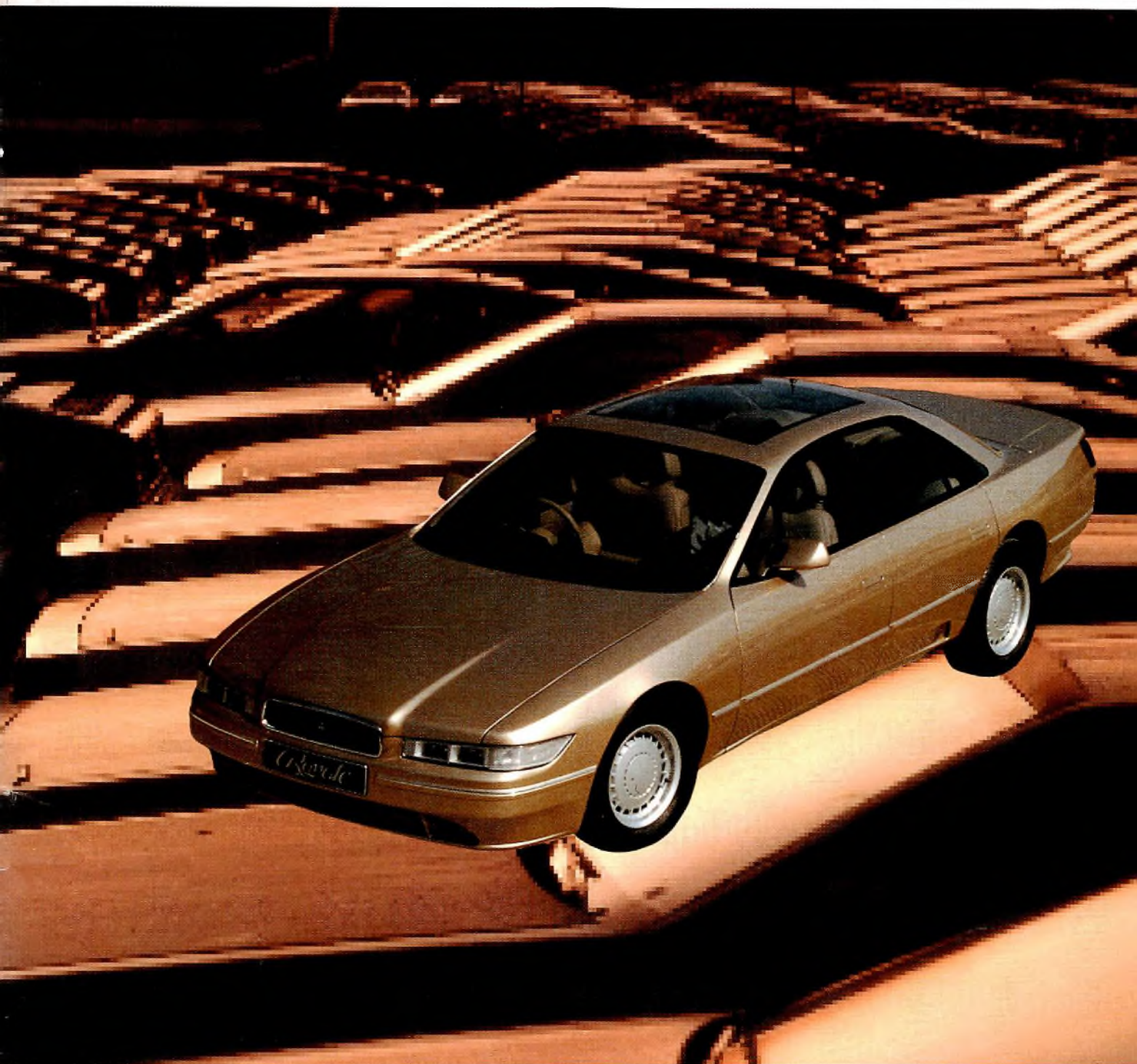


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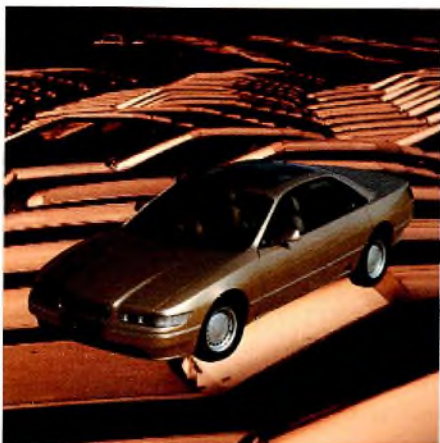
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In the hundred years since Carl Friedrich Benz introduced his single-cylinder, chain-drive 'Motorwagen' to the world, the role of the motor car has changed out of all recognition. In the early days, it was simply a bizarre means of getting around, and in that function it was often decidedly less reliable, and less comfortable than the horse-drawn carriages it supplanted. Contrast that with the state-of-the-art vehicles of today - vehicles like the 'Royale' shown here. A result of cooperation between Philips and IAD (International Automotive Design), the Royale incorporates among other things a CD-based in-car navigation system (CARIN), an office and communication system embodying cellular telephones, PC and facsimile machine, and a fully-integrated in-car entertainment system (with two LCD TV units). Car commuters of the future certainly won't lack creature comforts on their journeys, but as a break from the office, who knows, maybe taking a horse to work will come back into fashion.

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All-digital phase-locked loops using the 74HC/HCT297

WIM ROSINK

A phase-locked loop (PLL) is a control system that has already been in use for a long time for generating an output signal which is synchronized in frequency **and** phase to an input signal. For example, its use for the reception of radio signals in a 'homodyne' receiver was described by de Bellescize in 1932. The first widespread use of the PLL, however, was in TV sets for synchronizing the horizontal and vertical deflection oscillators with the transmitted sync pulses.

Initially, all PLLs were built with discrete components; they were extremely complex and their operation was entirely analog. Even after the introduction of transistors, they were still so complex that they were either impractical or too expensive for most applications.

The development of completely integrated single-chip PLLs changed this situation dramatically. All the advantages of analog PLLs can now be exploited by using just one IC and a few external components. Today, the superior noise immunity and tracking capability of PLL radio receivers allows them to be used for tracking weak signals from satellites and distant spacecraft. Other major applications are:

- Clock and data separation from complex data signals
- Frequency synthesizers and filters
- TV colour burst synchronization
- Motor speed control
- FM demodulators
- Doppler recovery
- Multi-standard self-adjusting computer monitors
- FSK decoding systems

Although some highly integrated PLLs such as our HCMOS 74HC/HCT4046 use a lot of digital circuitry, they're still semi-analog circuits and their operating parameters and stability are therefore inherently sensitive to component value spreads and to changes of supply voltage and temperature. Before clarifying the advantages of a totally digital PLL (DPLL) like our HCMOS 74HC/HCT297, it's useful to review PLL operating principles. Some PLL terminology is given in the Appendix.

THE BASIC ANALOG PLL

An analog PLL is, in principle, a feedback system for synchronizing the phase and frequency of an oscillator output with the phase and frequency of an incoming signal. Basically, it consists of a phase detector and a low-pass filter in the forward signal path, and a VCO in the feedback path. Figure 1 is the block diagram of a basic PLL.

Operating principles

With no signal applied to the input of a PLL using a simple phase detector as shown in Fig.1, the VCO operates at its centre frequency f_0 . When an input signal is applied, the phase detector compares the frequency and/or phase of the input signal with that of the VCO output. If any phase/frequency difference (error) is detected within the operating range of the phase detector, it generates an error signal $V_e(t)$ which is proportional to the phase

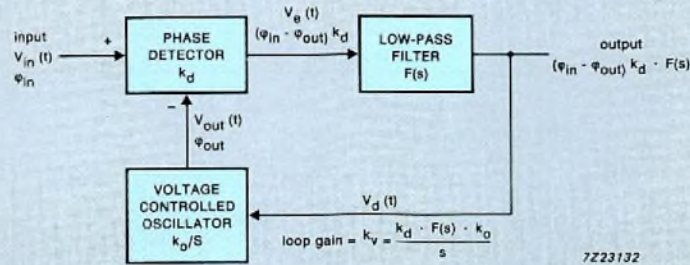


Fig.1 Analog PLL: block diagram

difference between the two signals. This error signal is usually a DC level modulated with AC components. The low-pass filter eliminates the AC components and delivers a signal $V_d(t)$ to control the VCO. This control signal forces the VCO to vary its frequency in a direction that reduces the phase/frequency error. The feedback nature of the PLL thus causes the VCO to synchronize (lock) with the incoming signal. Once locked, the VCO frequency is identical to that of the input signal and only has the minimum phase difference θ_0 required to generate sufficient error voltage V_d to shift the VCO frequency to the input frequency, thereby keeping the PLL in lock. This self-correcting capability of the PLL system allows it to track frequency changes of the input signal once it is locked.

The range of frequencies over which the PLL, once locked, can stay locked to an input signal is called the hold range, whereas the range of frequencies over which the PLL can acquire lock with an incoming signal is called the pull-in range (Fig.2). To ensure lock, the input frequency must not deviate beyond the pull-in range.

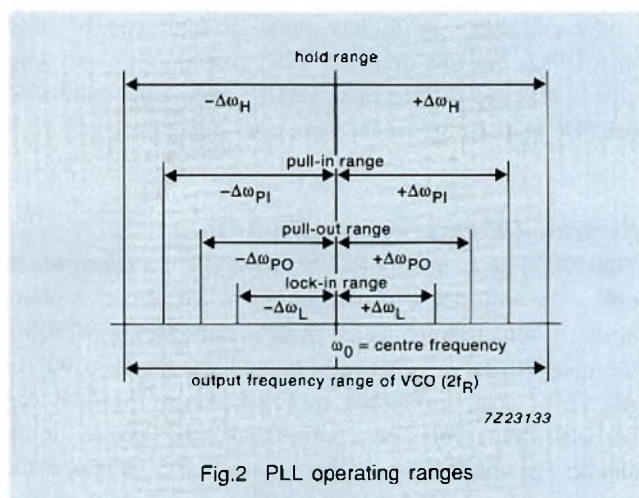


Fig.2 PLL operating ranges

Disadvantages

The VCO is the weakest link in an analog or semi-analog PLL. Changes of supply voltage and temperature affect both its centre and offset frequencies, thereby degrading the stability of the overall system. Also, changes of gain and conversion factors alter the system parameters.

Due to these effects and to spreads of external components, the centre frequency of a linear VCO can deviate by up to $\pm 20\%$. If the PLL system must have a narrow output frequency range (e.g. for FM demodulation or vertical scan synchronization), this deviation may well cause the pull-in range to shift sufficiently to exclude the input frequency. The only way to restore the correct pull-in range under these circumstances is to individually adjust the centre frequency of the VCO in each PLL to its correct value.

Our HCMOS 74HC/HCT297 allows a digital PLL to be implemented with very stable crystal-controlled clock pulse generators and digital circuitry instead of a VCO, thereby eliminating the possibility of such parameter changes. It also eliminates the need for individual circuit adjustments of the centre frequency.

A DIGITAL PLL USING OUR HCMOS 74HC/HCT297

Figure 3 shows the arrangement of a basic digital PLL (DPLL). Three of its four functional blocks are contained in the HCMOS 74HC/HCT297:

- Phase detector
- $\pm K$ counter with count-up and count-down sections
- Increment/decrement (I/D) circuit

The $\pm K$ counter, together with the I/D circuit, forms the digitally-controlled oscillator (DCO). The fourth functional block, a $\pm N$ counter is not incorporated in the 74HC/HCT297 because it is very application dependent.

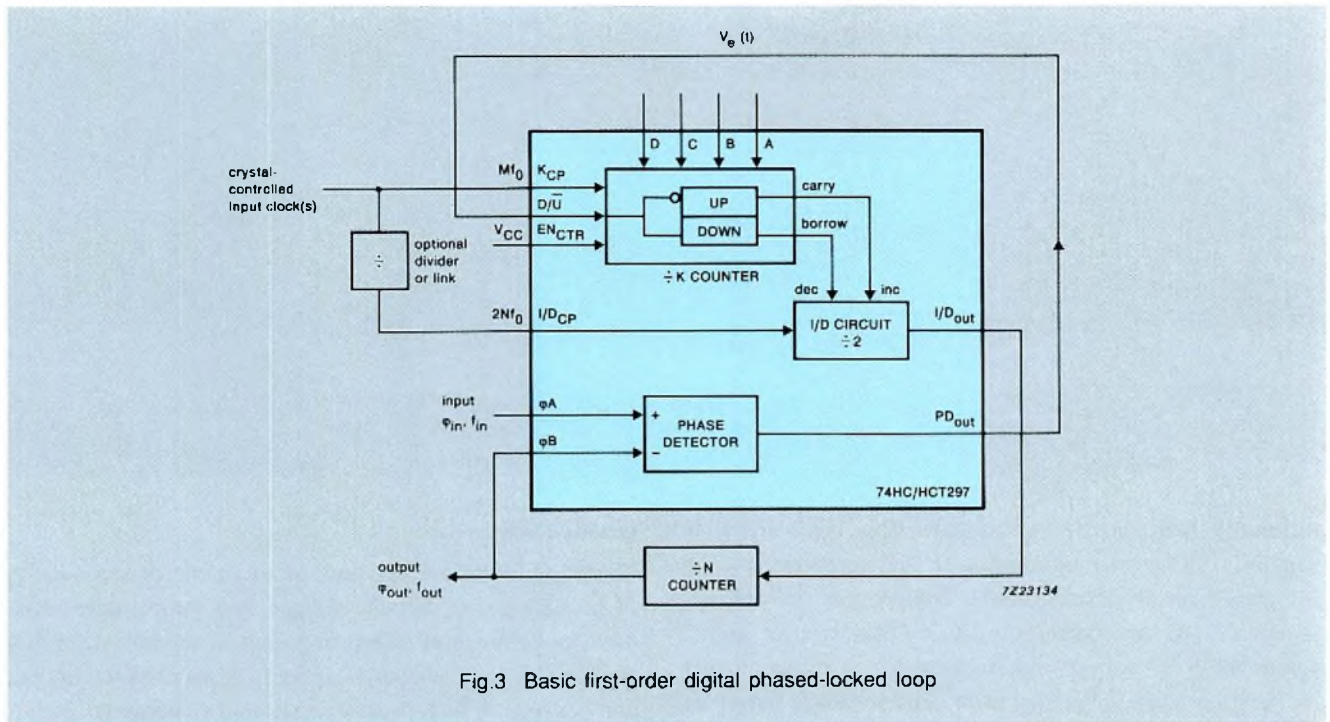


Fig.3 Basic first-order digital phased-locked loop

The 74HC/HCT297 offers all the well-known advantages of our HCMOS family of logic ICs and also has the following outstanding features:

- Digital design avoids analog compensation errors
- Easily cascaded to form higher-order loops
- Frequency range:
 - 30 MHz maximum at $V_{CC} = 4.5$ V for the $\div K$ counter clock
 - 20 MHz maximum at $V_{CC} = 4.5$ V for the I/D circuit clock
- Programmable bandwidth and centre frequency can also be varied dynamically
- Very narrow bandwidth attainable for high-Q loops
- Includes ripple cancellation features

The DPLL in Fig.3 requires a clock ($f_{KCP} = Mf_0$) for the $\div K$ counter and a clock ($f_{I/D} = 2Nf_0$) for the I/D circuit. In most DPLL applications however, the two clock frequencies can be the same and the clock inputs can then be connected together. Even if two different clock frequencies are required, they can be derived from the same source; one direct and the other via a divider.

The four functional blocks of the DPLL will now be discussed individually.

Phase detectors

Digital phase detectors require either a digital or a hard-limited analog input signal. However, most analog signals can be hard-limited without too much degradation

of the signal-to-noise ratio. The phase of such a square-wave input signal is $\sin(\omega_0 t + \phi_{in}(t))$ where ω_0 is the carrier frequency (equal to the DPLL centre frequency) and $\phi_{in}(t)$ is the time-varying phase of this frequency. For simplicity, the DPLL input signal will from now on be written as ϕ_{in} . Similarly, ϕ_{out} will represent the output signal.

The phase detector compares the phase of ϕ_{in} with that of ϕ_{out} and generates an error signal $V_e(t) = k_d \phi_e$, where k_d is the gain factor of the phase detector and ϕ_e is the phase error ($\phi_{in} - \phi_{out}$). So:

$$V_e(t) = k_d(\phi_{in} - \phi_{out})$$

The phase error for a DPLL is defined as zero when the duty factor of V_e is 50%.

Several types of digital phase detector can be used in a DPLL but the 74HC/HCT297 incorporates only two types, Exclusive-OR (EXORPD) and edge-controlled (ECPD) to perform all the necessary functions.

Exclusive-OR phase detector (XORPD)

The XORPD is a simple Exclusive-OR function which obeys the truth table shown in Fig.4. To obtain a phase error of zero (output signal with a duty factor of 50%), the phase difference between f_{in} and f_{out} must be 90° or $\pi/2$ (1/4 cycle) as shown in Fig.4. From Fig.4, it can be seen that, for correct feedback, the phase of f_{in} should lag that of f_{out} . Then, a lower f_{in} increases the average value of V_e , and the I/D circuit decreases f_{out} .

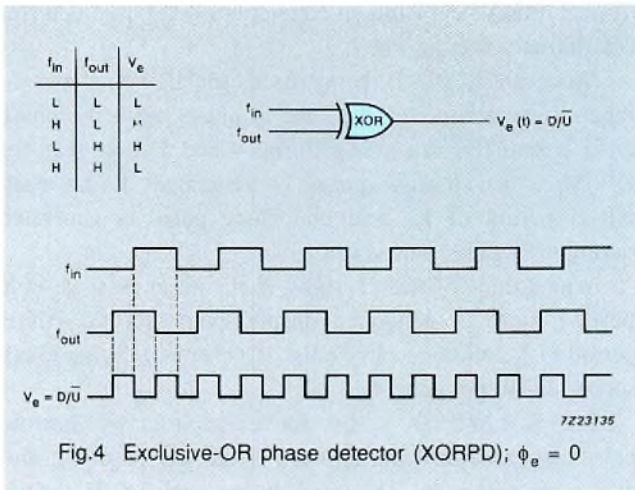


Fig.4 Exclusive-OR phase detector (XORPD); $\phi_e = 0$

For f_{in} outside the hold range, the duty factor of output signal V_e is 50% and f_{out} is equal to centre frequency f_0 .

The transfer function of the XORPD is shown in Fig.5. For convenience in later calculations, the output level range from the phase detector is defined as being from -1 when it's continuously LOW, to $+1$ when it's continuously HIGH.

When the phase detector output is zero (average value equal to half the supply voltage), the output waveform is a square wave with double the frequency of the input signal and a duty factor of 50%.

The gain factor (k_d) of the phase detector of a DPLL is expressed in terms of phase detector output per cycle of phase error. So, when the XORPD is being used, the value of k_d is 4 because the XORPD output is $+1$ for a phase error of $+90^\circ$ ($+1/4$ cycle), and -1 for a phase error of -90° ($-1/4$ cycle).

The phase error limits of the XORPD are $\pm 90^\circ$. If these limits are exceeded, the polarity of the loop gain reverses and the PLL goes out of lock.

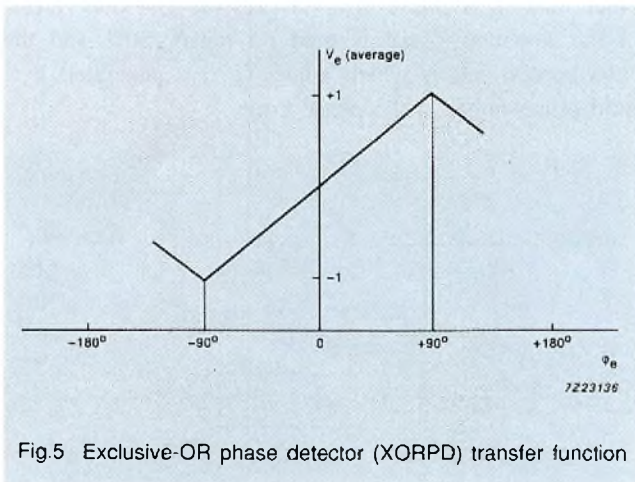


Fig.5 Exclusive-OR phase detector (XORPD) transfer function

Edge-controlled phase detector (ECPD)

The ECPD is a J-K flip-flop function obeying the Fig.6 truth table. For zero phase error output (output signal with 50% duty factor), the f_{in} and f_{out} input signals must be anti-phase ($1/2$ cycle or π radians phase difference) as shown in Fig.6(a).

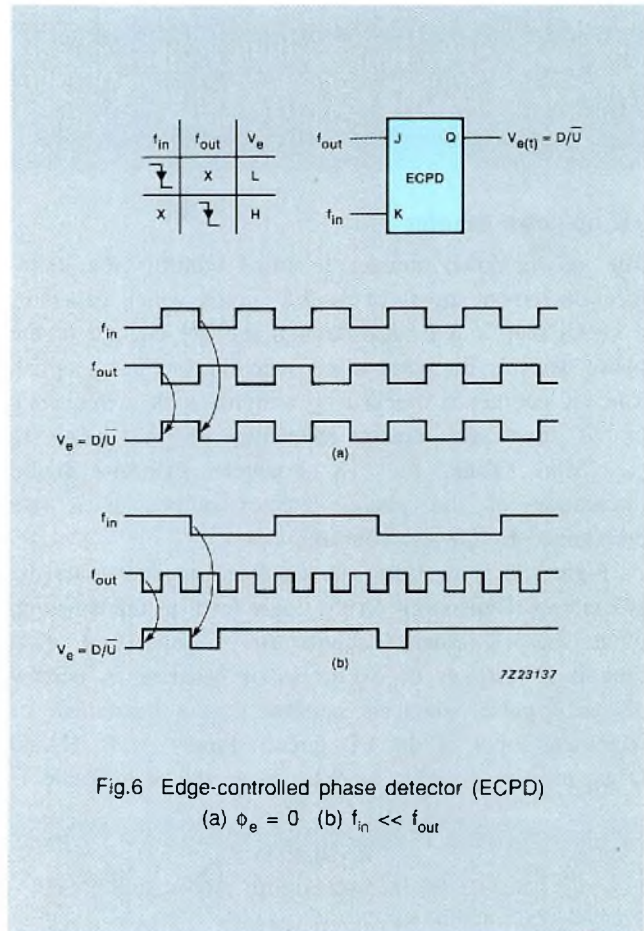


Fig.6 Edge-controlled phase detector (ECPD)
(a) $\phi_e = 0$ (b) $f_{in} \ll f_{out}$

The ECPD is also sensitive to any frequency difference between its input signals. With no signal at f_{in} , or with f_{in} lower than f_{out} as shown in Fig.6(b), the output frequency is decreased because V_e is HIGH for most of the time (high average value). For f_{in} higher than f_{out} , the output frequency is increased because V_e is LOW for most of the time (low average value).

Figure 7 shows the transfer function of the ECPD. When the inputs are anti-phase (phase error signal ϕ_e zero), the output waveform is a square wave with the same frequency as the input signal and a duty factor of 50%. The gain factor of the phase detector (k_d) is expressed in terms of output per cycle of phase error. It is therefore 2 because the output is $+1$ for a 180° ($1/2$ cycle) phase error. The phase error limits for the ECPD are $\pm 180^\circ$. If these limits are exceeded, the polarity of the loop gain reverses and the PLL goes out of lock.

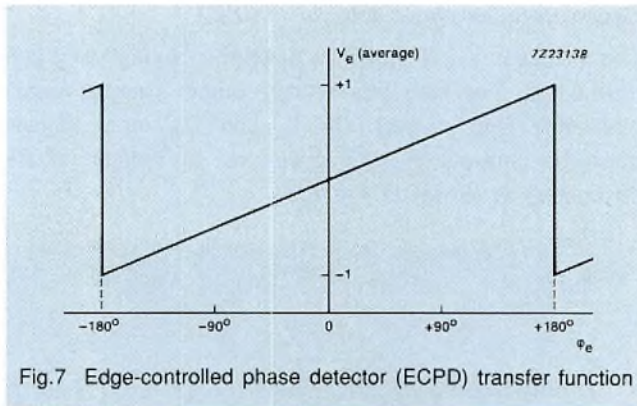


Fig.7 Edge-controlled phase detector (ECPD) transfer function

±K up/down counter

The ±K up/down counter in Fig.3 controls the increment/decrement inputs of the I/D circuit which generates a signal that is fed back through the ±N counter to the phase detector for comparison with the incoming signal. The ±K counter is clocked by a signal with a frequency of M times the centre frequency of the loop ($f_{KCP} = Mf_0$). Thus, the ±K counter performs digital integration of the phase detector output at a rate determined by the ±K counter clock.

Figure 8 shows the ±K counter together with the I/D circuit. Depending on the logic level at the down/up input, the ±K counter counts up or down and, each time it underflows or overflows, it generates a borrow or carry pulse which is applied to the decrement or increment input of the I/D circuit. Inputs A, B, C and D are used to program modulus K as shown in Table 1.

TABLE 1
Inputs for programming modulus K

D	C	B	A	mod.(K)	D	C	B	A	mod.(K)
L	L	L	L	inhibited	H	L	L	L	2^{10}
L	L	L	H	2^3	H	L	L	H	2^{11}
L	L	H	L	2^4	H	L	H	L	2^{12}
L	L	H	H	2^5	H	L	H	H	2^{13}
L	H	L	L	2^6	H	H	L	L	2^{14}
L	H	L	H	2^7	H	H	L	H	2^{15}
L	H	H	L	2^8	H	H	H	L	2^{16}
L	H	H	H	2^9	H	H	H	H	2^{17}

As explained in the description of the phase detector, the duty factor of the pulses at the down/up input of the ±K counter is 50% when the phase error is zero. Equal numbers of carry and borrow pulses are then generated at the same rate ($f_{carry} = f_{borrow} = Mf_0/2K$). If modulus K is made equal to M/2, one carry pulse and one borrow pulse is generated during each cycle of the output of a locked DPLL ($f_{carry} = f_{borrow} = f_0$). The waveforms for this mode

of operation when using an edge-controlled phase detector (ECPD) are given in Fig.9.

Since an ECPD is being used, the down/up and f_{in} inputs (waveforms 2 and 3) are in phase when the phase error is zero (Fig.6(a)). Waveforms 4 and 5 show that, for $K = M/2$, one borrow pulse is generated during each HIGH period of f_{in} , and one carry pulse is generated during each LOW period of f_{in} .

Waveforms 6 and 7 show that, when $K = M$, one borrow pulse is generated during every second HIGH period of f_{in} , and one carry pulse is generated during every second LOW period of f_{in} .

For $K < M/2$ ($K = M/4$ for example), two borrow pulses are generated during each HIGH period of f_{in} , and two carry pulses are generated during each LOW period. Because these carry/borrow pulses are added/subtracted to/from the input of the ±N counter, the duty factor of f_{out} deviates from 50% by up to $M/2KN$, causing ripple on the output. The amount by which the duty factor deviates is shown in waveform 3A of Fig.9. It can be calculated as $(1 \pm M/2KN)/2 = 0.5 \pm (M/KN)$ which, with $M = 2N$ becomes $(1 \pm 1/K)/2 = 0.5 \pm (1/2K)$.

If an XORPD is used, the frequency of the down/up input is double that of f_{in} (see Fig.4). If the phase error is zero and $K < M/4$, the ±K counter generates at least one carry pulse and one borrow pulse for each down/up input cycle. However, with an XORPD, carry and borrow pulses that occur during the same cycle of the down/up input cancel each other so they don't cause deviation of the duty factor of f_{out} . The maximum duty factor deviation of f_{out} is then reduced to $1/N$.

The stability of f_{out} can be considerably improved by using one of the ripple cancellation circuits discussed later during the description of a complete DPLL.

The carry and borrow pulses from the ±K counter are fed to the I/D circuit to increase or decrease its output frequency. If the input frequency to the DPLL is other than f_0 , a phase error is present. The duty factor of the down/up signal is then no longer 50% and the carry/borrow pulses which adjust f_{out} are generated in a ratio proportional to the phase error.

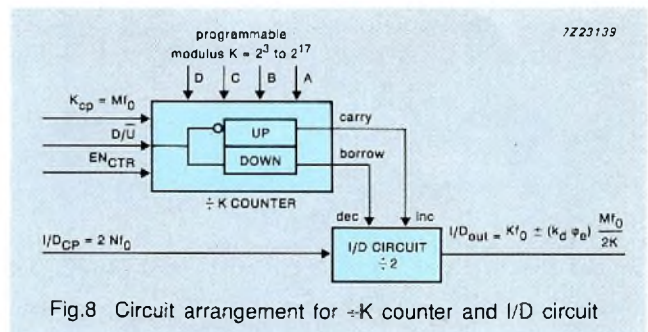


Fig.8 Circuit arrangement for ±K counter and I/D circuit

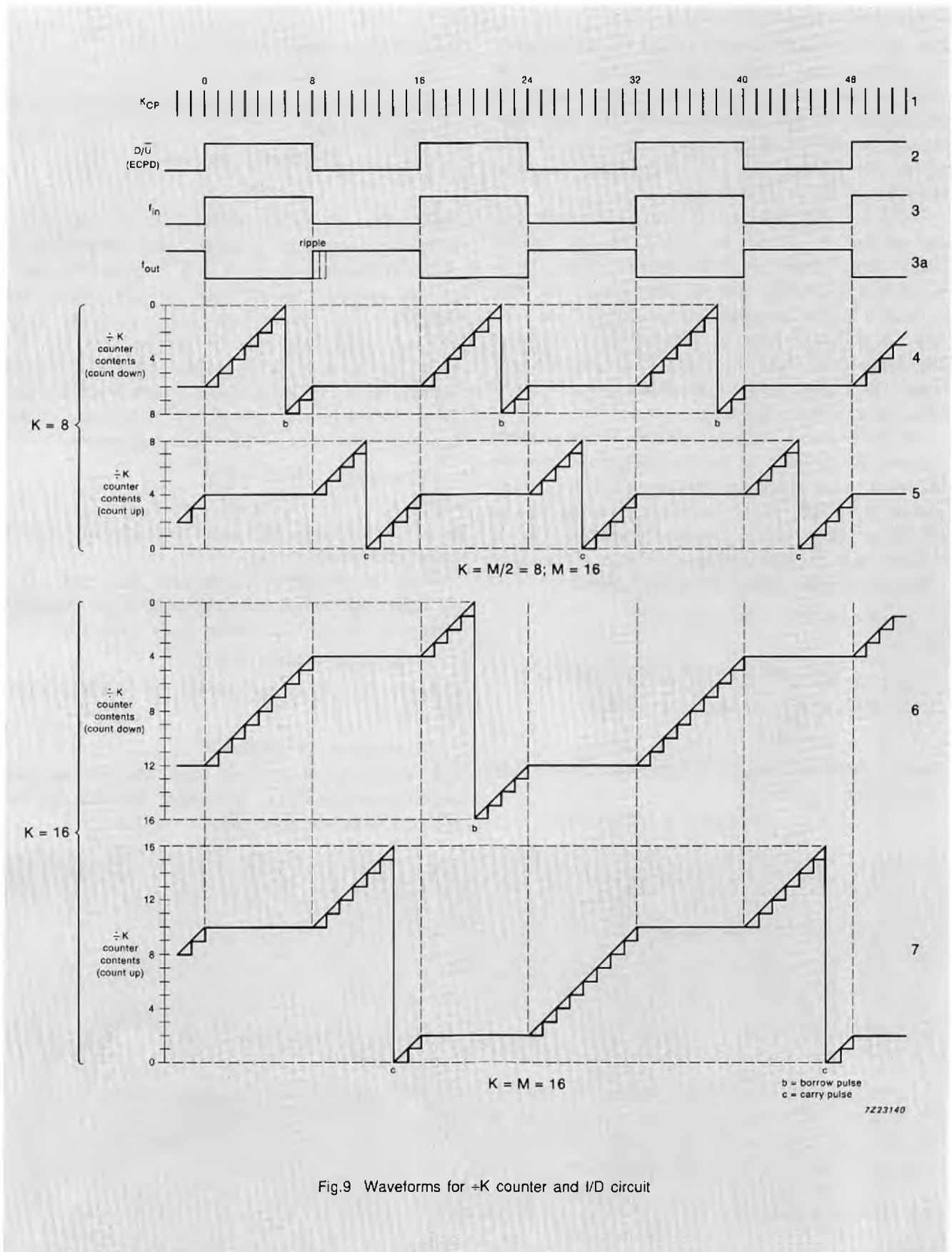


Fig.9 Waveforms for $\pm K$ counter and I/D circuit

Increment/decrement (I/D) circuit

The carry and borrow outputs of the $\pm K$ counter drive the decrement and increment inputs of the I/D circuit which is clocked at a frequency of $2Nf_0$, where N is the modulus of the feedback counter. In most applications, the I/D circuit clock frequency is equal to that of the $\pm K$ counter (the two clock inputs connected together) and $2N$ then equals M .

When the loop is locked, the carry and borrow outputs of the $\pm K$ counter are both LOW and the I/D circuit simply divides its clock frequency ($2Nf_0$) by 2. If the loop isn't locked, the $\pm K$ counter generates carry or borrow pulses depending on the sign of the loop error. If a borrow pulse is generated, the I/D circuit deletes one clock pulse (equal to half a cycle) from its output. If a carry pulse is generated, the I/D circuit adds half a cycle to its output.

At the limits of the phase detector operating range ($k_d\phi_e = \pm 1$), the limits of the frequency range from the I/D circuit are determined by the clock frequencies applied to the I/D circuit and the $\pm K$ counter ($f_{I/D\ CP}$ and $f_{K\ CP}$) and by the carry/borrow pulses from the $\pm K$ counter when its down/up input is held continuously LOW (carry pulses) or HIGH (borrow pulses):

$$f_{I/D\ out\ max/min} = f_{I/D\ CP}/2 \pm f_{K\ CP}/2K$$

So,

$$f_{I/D\ out\ max/min} = Nf_0 \pm Mf_0/2K = f_0(N \pm M/2K)$$

Or, if I/D_{CP} and K_{CP} are linked ($M = 2N$):

$$f_{I/D\ out\ max/min} = Nf_0(1 \pm 1/K)$$

Dividing these equations by N derives the limits of the output frequency range:

$$f_{out\ max/min} = f_0 \pm Mf_0/2KN = f_0(1 \pm M/2KN)$$

Or, with I/D_{CP} and K_{CP} linked ($M = 2N$):

$$f_{out\ max/min} = f_0(1 \pm 1/K)$$

With I/D_{CP} and K_{CP} linked ($M = 2N$) and K set to its minimum value (2^3):

$$f_{I/D\ out\ max/min} = Nf_0(1 \pm 1/K) = Nf_0(1 \pm 1/8)$$

Figure 10(a) shows the output from the I/D circuit under these conditions. A higher value for modulus K of the $\pm K$ counter (range 2^3 to 2^{17}) reduces the limits of the frequency range from the I/D circuit and therefore also reduces the hold range. A wider frequency range can only be derived from the I/D circuit by making $f_{K\ CP}$ higher than $f_{I/D\ CP}$. For example, by connecting a divider by 2 between K_{CP} and I/D_{CP} ($M = 4N$), and with $K = 2^3$, the limits of the frequency range from the I/D circuit increase to:

$$f_{I/D\ out\ max/min} = Nf_0(1 \pm 1/4)$$

Figure 10(b) shows the output from the I/D circuit under these conditions.

With a divider by 4 between K_{CP} and I/D_{CP} ($M = 8N$), and with $K = 2^3$, the limits of the frequency range from the I/D circuit theoretically increase to:

$$f_{I/D\ out\ max/min} = Nf_0(1 \pm 1/2)$$

However, the I/D circuit restricts the frequency range limits to:

$$f_{I/D\ out\ max/min} = Nf_0(1 \pm 1/3)$$

The conditions of $M = 4N$ and $M = 8N$ are not normally used in DPLL applications but they may be used if a wider operating range is required.

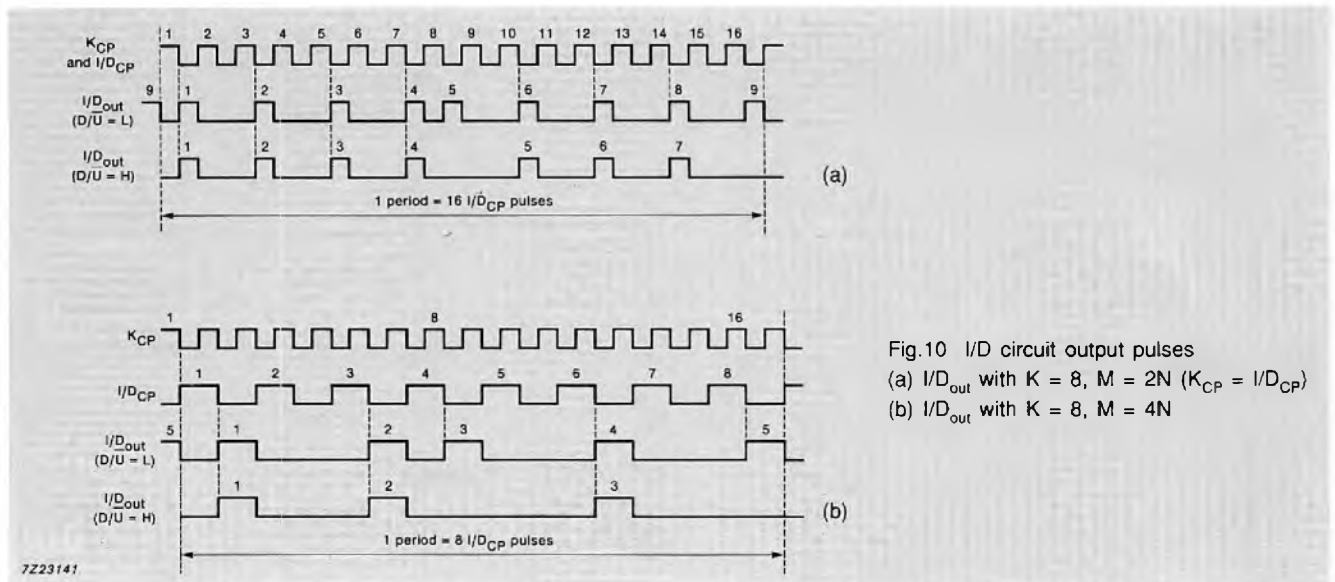


Fig.10 I/D circuit output pulses
(a) I/D_{out} with $K = 8, M = 2N$ ($K_{CP} = I/D_{CP}$)
(b) I/D_{out} with $K = 8, M = 4N$

±N counter

The output from the I/D circuit is the clock for an up-counting, ±N feedback counter. The most significant bit (MSB) from this counter is applied to the phase detector for comparison with the phase of the input signal as previously described in the section about the phase detector.

The complete DPLL

When the loop is locked to an input signal with a frequency equal to centre frequency f_0 and with phase ϕ_{in} , the output of the phase detector is a square wave with a 50% duty factor, and the ±K counter counts up and down by equal amounts. Equal numbers of carry and borrow pulses are therefore generated by the I/D circuit and the ±N counter adds/deletes them all to/from output signal f_{out} . The I/D circuit clock signal $f_{I/D CP} = 2Nf_0$ is now only divided by 2 in the I/D circuit and by N in the ±N feedback counter. The DPLL output ϕ_{out} with a frequency equal to centre frequency f_0 therefore remains in phase with ϕ_{in} .

If ϕ_{out} is not in phase with ϕ_{in} , the phase detector output is asymmetrical and the average value of the ±K counter output decreases or increases. The ±K counter then overflows or underflows and generates more carry pulses than borrow pulses or vice-versa depending on the sign of the phase error. The I/D circuit then adds/deletes pulses to/from the signal fed to the ±N counter, thereby incrementing or decrementing the phase of ϕ_{out} by $1/2N$ cycles for each carry/borrow pulse. This process continues until zero phase error is attained.

First-order DPLL equations

Figure 11(a) is the block diagram of a first-order DPLL. Figure 11(b) is its loop diagram. The ±K counter clock has a frequency Mf_0 and the I/D circuit clock has a frequency $2Nf_0$ as previously explained. The centre frequency of the loop is:

$$f_0 = f_{I/D CP} / 2N \tag{1}$$

The frequency of the ±K counter output is:

$$f_{K out} = (k_d \phi_e M f_0) / K \tag{2}$$

The frequency range of the I/D circuit output is:

$$f_{I/D out} = N f_0 \pm (k_d \phi_e M f_0) / 2K \tag{3}$$

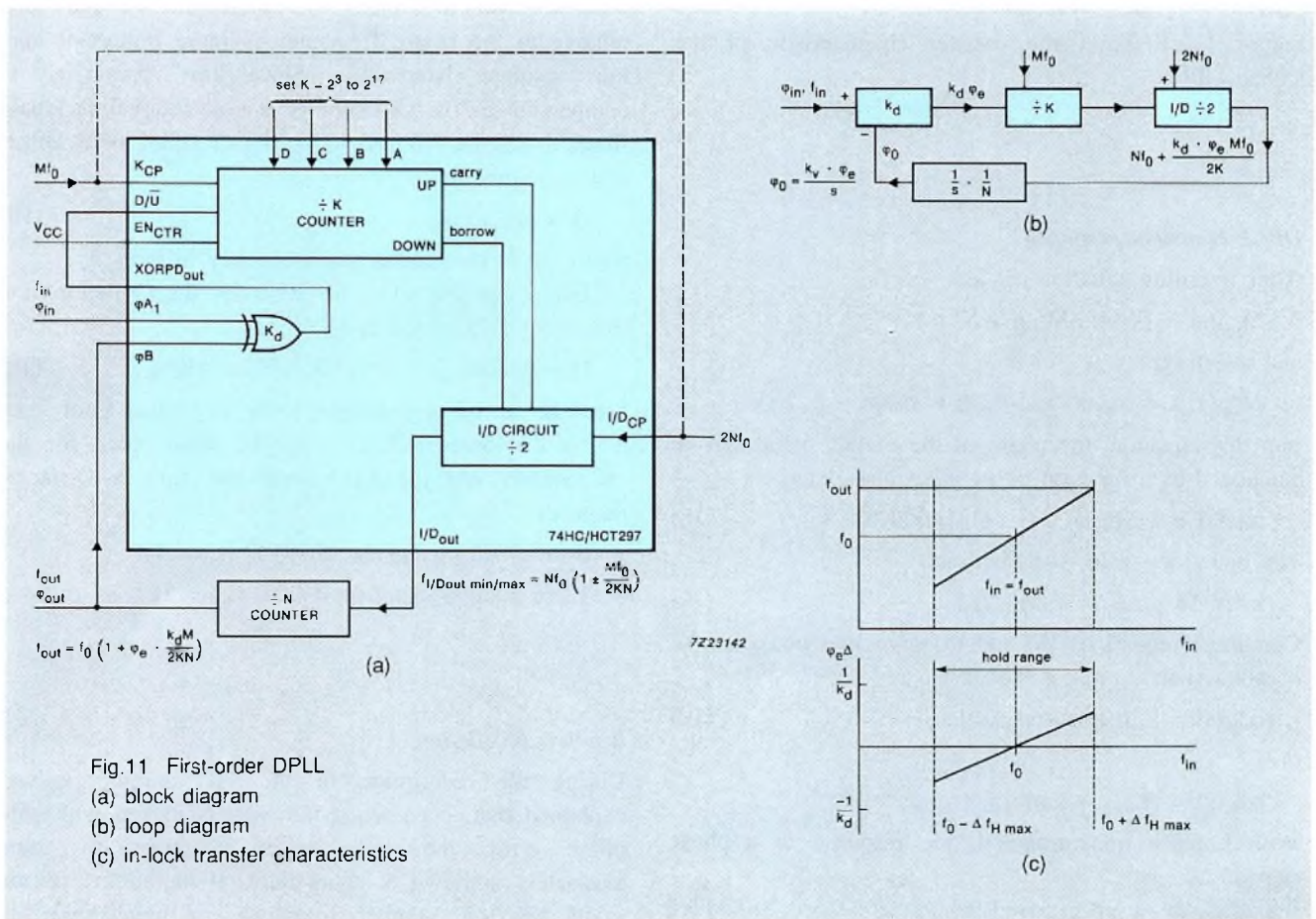


Fig.11 First-order DPLL
 (a) block diagram
 (b) loop diagram
 (c) in-lock transfer characteristics

The loop output frequency range is obtained by dividing equation (3) by N:

$$f_{out} = f_0 \pm (k_d \phi_e M f_0) / 2KN \quad (4)$$

The shift of the output frequency from the centre frequency as a function of phase error ϕ_e (in cycles) is therefore:

$$\Delta f_{out} = (k_d \phi_e M f_0) / 2KN \quad (5)$$

Since $k_d \phi_e = \pm 1$ at the limits of the hold range (see Figs 5 and 7), the hold range for $M/2KN \geq 1/4$ can be derived from equation (5) as:

$$\pm \Delta f_H = (M f_0) / 2KN \quad (6)$$

With the I/D_{CP} an K_{CP} clock inputs linked ($M = 2N$), the limits of the hold range become:

$$\pm \Delta f_H = f_0 / K$$

From this equation and equation (6), it's easy to see why the modulus of the $\pm K$ counter (K) is programmable; it allows the hold range to be adjusted. A low value for K widens the hold range and a high value for K narrows it.

When the DPLL is locked, $f_{out} = f_{in}$ and the phase difference (in cycles) between the two signals is ϕ_e which can be determined by rearranging equation (4):

$$\phi_e = 2KN(f_{in} - f_0) / k_d M f_0 \text{ cycles} \quad (7)$$

Figure 11(c) shows the transfer characteristic of the locked DPLL.

DPLL transient response

After rewriting equation (5) as:

$$\Delta f_{out}(s) = (k_d \phi_e(s) M f_0) / 2KN$$

and inserting:

$$\Delta f_{out}(s) / s = \phi_{out}(s) \text{ and } \phi_e(s) = \phi_{in}(s) - \phi_{out}(s)$$

into this equation, the phase of the output signal can be calculated as a function of an input phase step:

$$\phi_{out}(s) = k_d M f_0 (\phi_{in}(s) - \phi_{out}(s)) / 2KNs \quad (8)$$

The open-loop gain is defined as:

$$k_v = \Delta \phi_{out} / \Delta \phi_e = k_d M f_0 / 2KN \quad (9)$$

Combining equations (8) and (9) gives the phase of the output signal:

$$\phi_{out}(s) = k_v [\phi_{in}(s) - \phi_{out}(s)] / s \quad (10)$$

or,

$$\phi_{out}(s) = [k_v / (s + k_v)] \phi_{in}(s)$$

With Laplace transformation, the response to a phase step of $\Delta \phi_{in}$ is:

$$\phi_{out}(t) = \Delta \phi_{in} (1 - e^{-k_v t}) \quad (11)$$

So the DPLL responds to a phase step with a time-constant:

$$\tau = 1/k_v = 2KN / k_d M f_0$$

If $M = 2N$, τ becomes $K/k_d f_0$

This shows that adjustment of the programmable modulus of the $\pm K$ counter also influences the pull-in time of the DPLL. A low value for K (wide hold range) shortens the pull-in time and a high value for K (narrow hold range) lengthens it.

In the frequency domain, ϕ_{out} can be written as:

$$\phi_{out}(t) = \phi_{in} \sin \omega t [k_v / (j\omega + k_v)] \quad (12)$$

DPLL bandwidth

The -3 dB frequency of the first-order DPLL circuit can be expressed in general terms as being equal to the open-loop gain k_v as given in equation (9):

$$\omega_{3dB} = k_v = k_d M f_0 / 2KN \text{ rad/sec} \quad (13)$$

In many applications, $M = 2N$, and equation (13) can then be reduced to:

$$\omega_{3dB} = k_d f_0 / K \text{ rad/sec} \quad (14)$$

However, for a DPLL, the bandwidth of the loop relative to the centre frequency is more important than the absolute bandwidth. Since this parameter is comparable to the Q factor of a conventional bandpass filter, it can be referred to as the Q factor of a DPLL and is defined as:

$$Q = \omega_0 / 2\omega_{3dB} \quad (15)$$

where ω_0 is the loop centre frequency in rad/sec.

Using equation (14), for $M = 2N$ the Q factor of a first order DPLL system is:

$$Q = \omega_0 / 2\omega_{3dB} = 2\pi f_0 / (2k_d f_0 / K) = \pi K / k_d \quad (16)$$

Since K can be programmed to be any value from 2^3 to 2^{17} , a first-order DPLL using the same clock for the $\pm K$ counter and the I/D circuit can have a Q factor range of:

- 6 to 103000 using the XORPD ($k_d = 4$)
- 12 to 206000 using the ECPD ($k_d = 2$).

Ripple cancellation

During the description of the $\pm K$ counter, it was explained that, even when the loop is locked with zero phase error, the $\pm K$ counter continues to count alternately up/down at equal rates. If modulus K is too small, the $\pm K$ counter overflows or underflows too

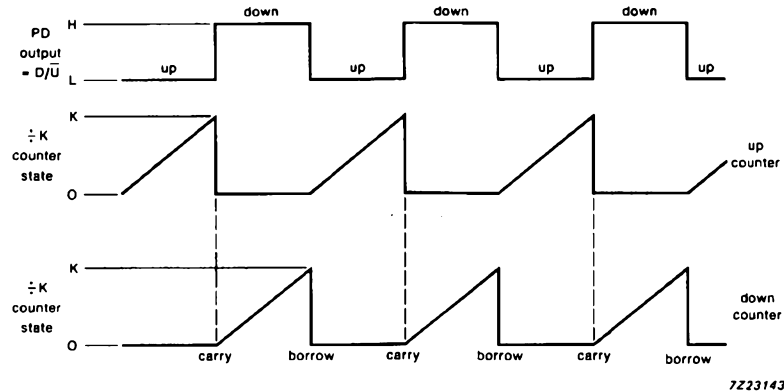


Fig.12 +K counter operation with a minimum K value for minimum ripple

often, resulting in repetitive generation of carry pulses followed by borrow pulses. This causes a duty factor deviation (ripple) on the output of the $\pm N$ counter if the ECPD is used. If the XORPD is used, carry and borrow pulses occur during the same half-cycle of f_{out} and cancel each other. However, the less significant bits from the $\pm N$ counter (not normally used in a DPLL) will still show duty factor or frequency ripple.

The duty factor deviation (ripple) can be reduced to $1/N$ cycles if modulus K is made large enough. The ripple frequency on f_{out} due to the carry/borrow pulses is equal to f_{out} if $K = M/2$. Figure 12 shows a situation with the minimum value of K to obtain minimum ripple. The values of modulus K to obtain minimum ripple are:

$$K > M/4 \text{ for DPLLs using the XORPD and with } f_{D/U} = f_{out}/2$$

$$K > M/2 \text{ for DPLLs using the ECPD and with } f_{D/U} = f_{out}$$

The circuits in Figs 13 and 14 show other simple ways to minimize ripple and ripple frequency by using only one external inverter. Both circuits use a feature of the 74HC/HCT297 that hasn't yet been mentioned; the enable input of the $\pm K$ counter.

The circuit in Fig.13 uses the XORPD. The MSB of the $\pm N$ counter is Exclusive-ORed with the input signal as previously explained in the description of the phase detector but, instead of the output from the phase detector driving the down/up input of the $\pm K$ counter, it drives its enable input. When the enable input is LOW, the $\pm K$ counter is inhibited from counting either up or down. The down/up input of the $\pm K$ counter is driven by the second MSB of the $\pm N$ feedback counter. With

this arrangement, the $\pm K$ counter can only count down when both its enable and down/up inputs are HIGH, and can only count up when its enable input is HIGH and its down/up input is LOW (see Fig.13). When the loop is locked (phase error of zero), the average value in the $\pm K$ counter remains constant. When the phase error is within the hold range of the phase detector, the $\pm K$ counter counts up or down by a number proportional to the phase error. For small phase errors ($f_{in} \approx f_0$), the output pulse rate of the $\pm K$ counter is very low so the frequency of the ripple on the output is reduced. The disadvantage of this circuit is that the input signal and the output from the $\pm N$ counter must have a duty factor of 50%.

In the circuit of Fig.14, which uses the ECPD, the duty factor of the input signal isn't restricted to 50%. However, a disadvantage of this circuit compared with the circuit using the XORPD is that the carry/borrow pulses are only generated during one half cycle of f_{out} . As previously explained, the frequency of the induced ripple is low but the ripple will cause a slight deviation on the duty factor of f_{out} .

Although the circuits of Figs 13 and 14 minimize the ripple and its frequency, they also approximately halve the hold range of the loop. The loop phase error limit ($\pm 90^\circ$ for the XORPD and $\pm 180^\circ$ for the ECPD) is reduced by a factor $1/[1 + (1/2K)]$ and the phase detector gain (k_d) is halved. Entering these value changes into equation (5) gives the new hold range:

$$\pm \Delta f_H = M f_0 / [1 + (1/2K)] 4KN = M f_0 / [2N(2K + 1)] \quad (17)$$

Which, for $M = 2N$ and $K \gg 1$ becomes:

$$\pm \Delta f_H \approx f_0 / 2K$$

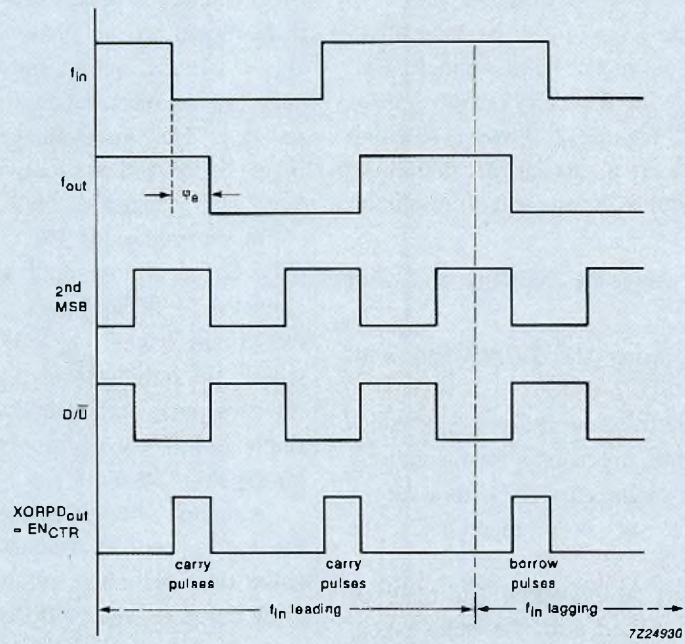
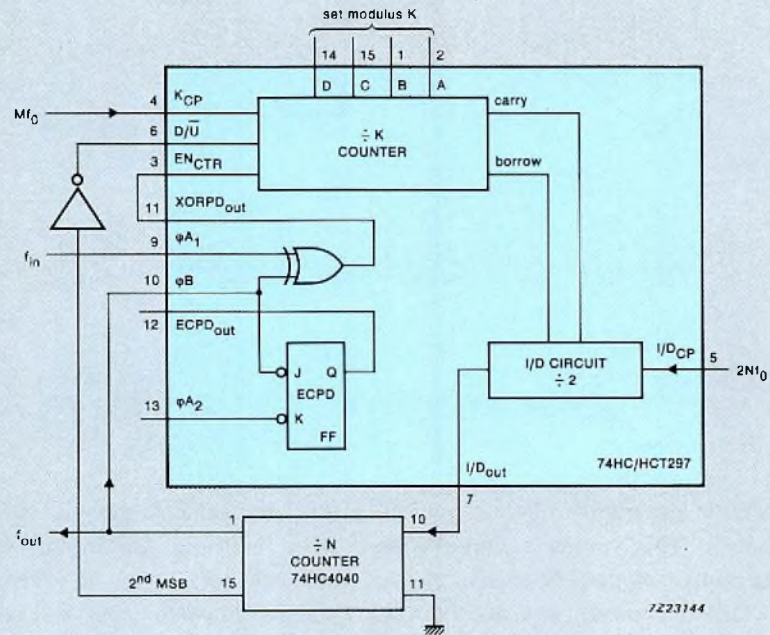


Fig.13 Ripple cancellation using the XORPD

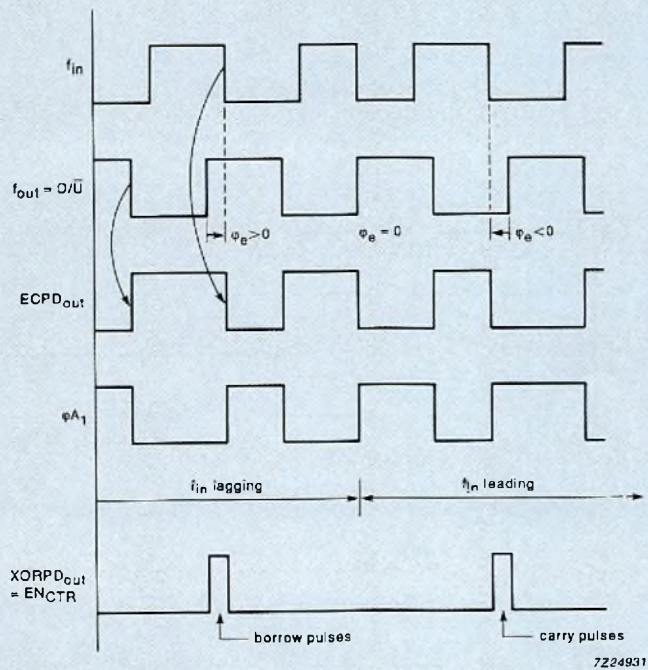
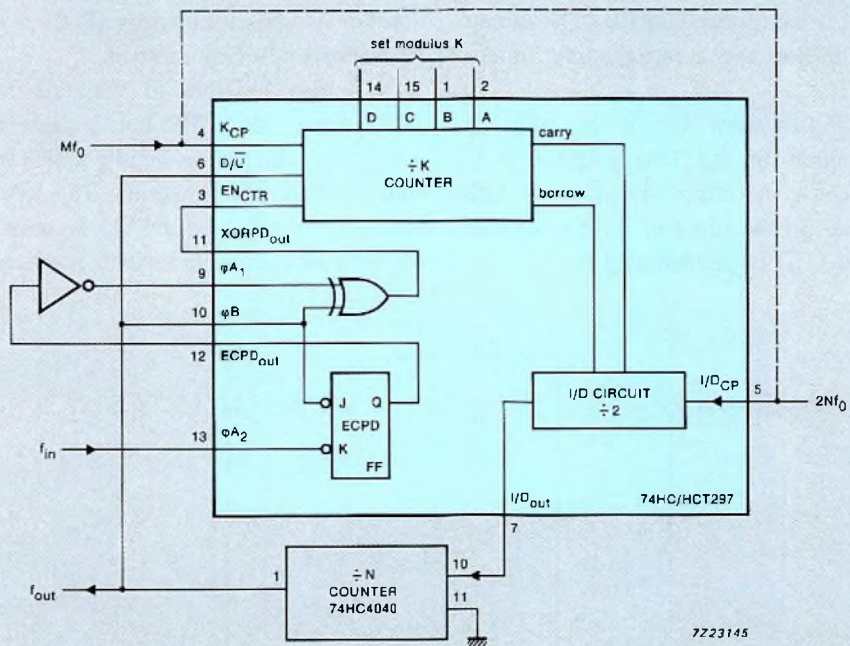


Fig.14 Ripple cancellation using the ECPD

DPLL APPLICATIONS

Lock detection

Figure 15 shows a simple lock detection circuit that is very suitable for a DPLL using the XORPD. The circuit needs only a D-type flip-flop and a retriggerable monostable multivibrator.

The waveforms in Fig.16 show that, if the DPLL is locked, the negated output of the D-type flip-flop is continuously HIGH because the phase of f_{in} always lags that of the output signal. So the input of the monostable is not triggered and the LED is permanently lit.

When the DPLL isn't locked (see Fig.17), the monostable is repeatedly triggered, and, if the time-constant is chosen correctly ($R_1C_1 > 4/f_{in}$), the LED will be permanently extinguished.

It's also possible to use this lock detector for a DPLL using the ECPD but, because f_{in} and f_{out} are then anti-phase when $f_{in} \approx f_0$, slight phase jitter can generate 'not locked' information. This means that, at the frequency where the DPLL is most likely to operate, the lock detection circuit will not function correctly.

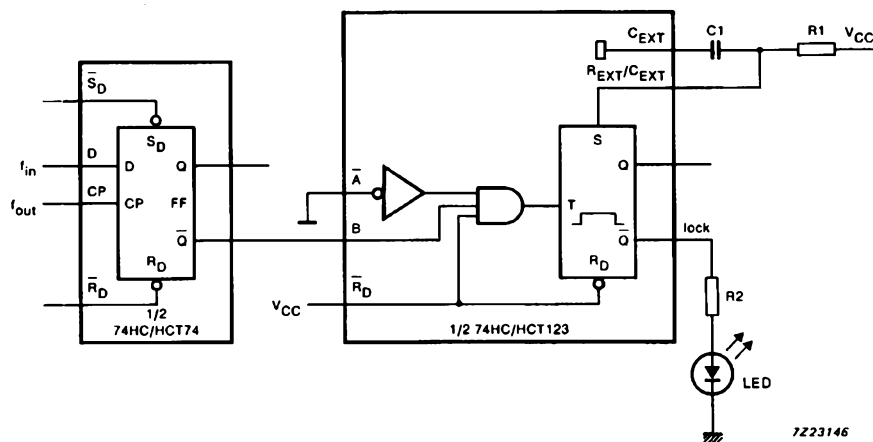


Fig.15 Lock detection circuit

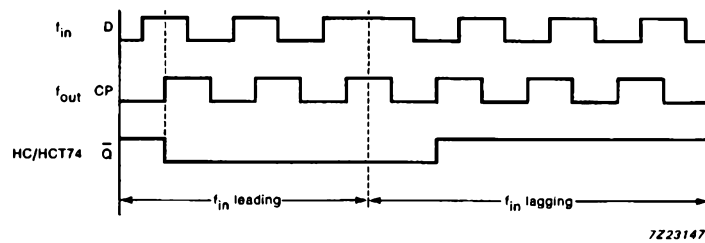


Fig.16 Lock detection waveforms for the 74HC/HCT74 flip-flop: in-lock (XORPD)

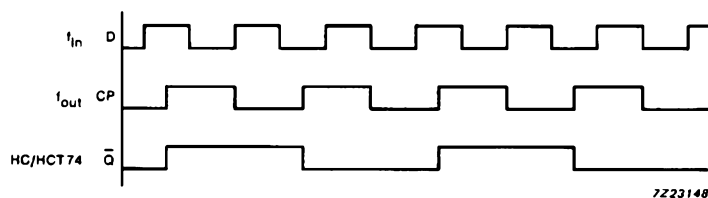


Fig.17 Lock detection waveforms for the 74HC/HCT74 flip-flop: out-of-lock (XORPD)

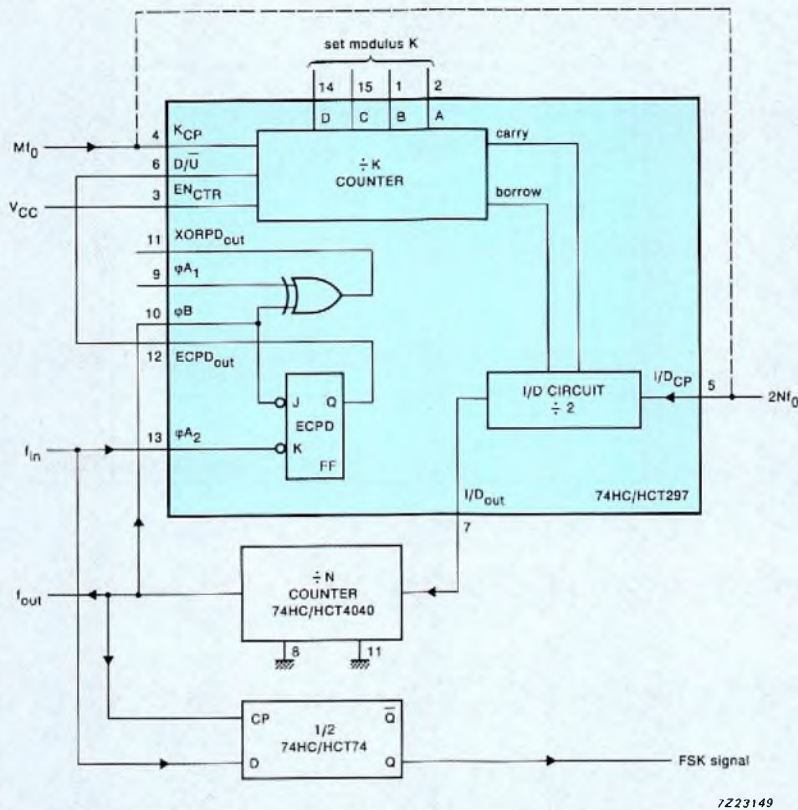


Fig.18 FSK decoding circuit with ECPD

FSK decoding with an ECPD

The circuit of Fig.15, when used with the ECPD, is however very suitable for decoding FSK signals with two frequencies which surround f_0 .

Figure 16 shows that the logic state of the D-type flip-flop output in the lock detection circuit depends on whether the phase difference between f_{in} and f_{out} is positive or negative. This feature allows the circuit to be used with the ECPD for decoding Frequency Shift Keyed (FSK) signals using frequencies f_1 and f_2 . If the centre frequency (f_0) is set so that f_1 is lower than f_0 and f_2 is higher than f_0 , f_1 creates a situation in which the phase of f_{in} is lagging, and f_2 creates a situation in which the phase of f_{in} is leading. So the negated output from the D-type flip-flop is a decoded version of FSK modulation applied to f_{in} because it is HIGH for f_2 and LOW for f_1 . Figure 18 shows the circuit of a complete FSK decoder.

Digital readout of phase data

The concept of latching f_{out} (the MSB of the $\pm N$ counter) with f_{in} can be extended to latching the entire contents of the $\pm N$ counter. A digital readout can then be obtained of the absolute phase error and the value of phase error signal ϕ_e , and therefore also of the frequency deviation $f_{in} - f_0$.

As previously described, there is a defined difference between the phase of f_{in} and f_{out} when the DPLL is locked. This phase difference is directly related to the information in the $\pm N$ counter when a HIGH to LOW transition of f_{in} occurs.

If the loop contains a $\pm N$ counter with parallel outputs, the information on these outputs can be latched in a register and used for computing purposes. A DPLL using the ECPD is most suitable for this purpose because it has a phase error limit of 180° and can make use of the entire contents of the $\pm N$ counter. For convenience, the following example will use a ± 16 counter (74HC/HCT93) in the feedback loop.

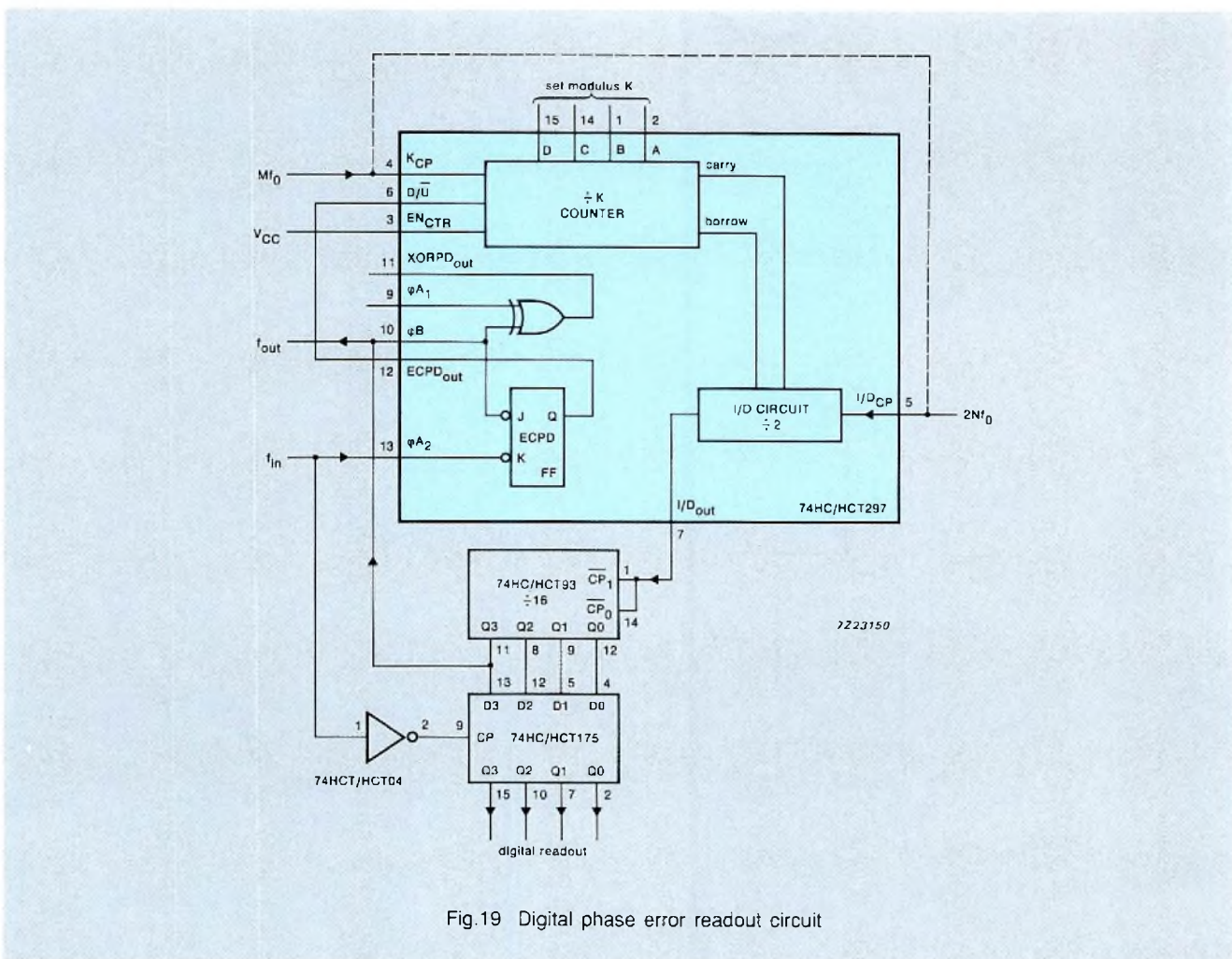


Fig.19 Digital phase error readout circuit

Figure 19 shows a circuit that can derive the phase difference between f_{in} and f_{out} as a 4-bit code. The falling edges of the f_{in} and f_{out} signals are used to measure the phase error, and the falling edge of f_{in} is used to latch the contents of the $\div 16$ counter into the register, the output of which is a 4-bit binary code that represents the absolute difference between the phase of f_{in} and f_{out} .

During the earlier description of phase detectors, it was explained that, for the ECPD, the phase error ϕ_e is zero when f_{in} and f_{out} are anti-phase. So the absolute phase difference between f_{in} and f_{out} always differs by half a cycle from the phase error ϕ_e . Figure 20 shows examples of this. Waveform 5 in Fig.20 shows an example where the absolute phase difference between f_{in} and f_{out} is between 15/16 and 1 cycle, but the phase error ϕ_e is between 7/16 and 8/16 cycle for the ECPD. Waveform 6 in Fig.20 shows an example where the absolute phase difference is between 13/16 and 14/16 cycle, but the phase error ϕ_e is between 5/16 and 6/16 cycle for the ECPD.

Figure 20 (waveform 7) shows an example in which the absolute phase difference between f_{in} and f_{out} is between 6/16 and 7/16 cycle, but the phase error ϕ_e is between $-2/16$ and $-1/16$ cycle for the ECPD.

Table 2 shows all the possible 4-bit codes from the register together with the associated absolute phase difference and phase errors ϕ_e .

The 4-bit codes in the Table are inverted data from the register which represents the absolute phase difference. Phase error ϕ_e is calculated by subtracting 1 from the MSB of the inverted outputs of the register. It's easy to see that the maximum difference between the calculated value of ϕ_e and its real value is an LSB (1/N cycle). Using $N = 16$, as chosen for this example, gives a result that isn't very accurate. However, a more accurate result can be obtained by increasing N to a higher value. The calculated phase error ϕ_e can be used to demodulate an FM signal or to calculate the real input frequency from:

$$f_{in} = f_0(1 + k_d\phi_e/K)$$

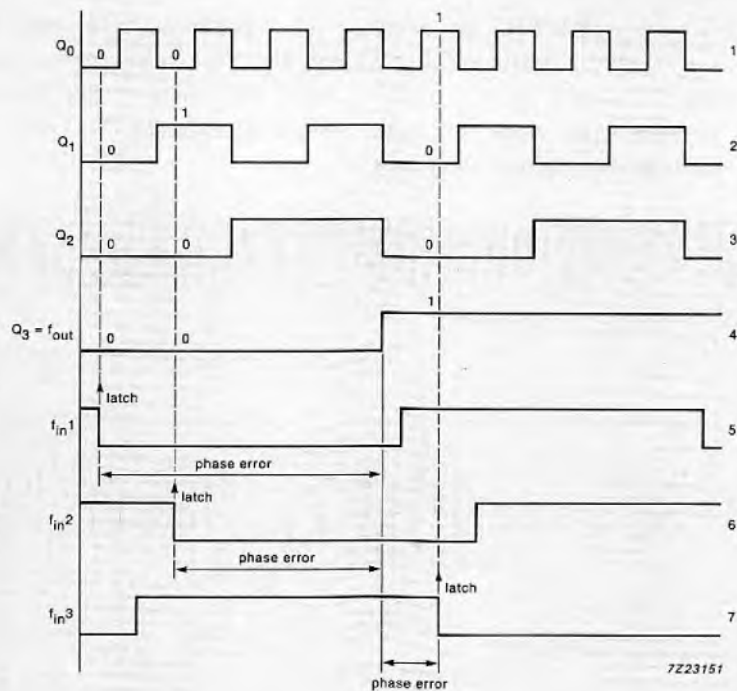


Fig.20 Digital readout from the register in Fig.18 for three values of ϕ_e . The data is latched at the falling edge of f_{in} . For f_{in1} , the phase error is $7/16$ to $8/16$ and the digital readout is 0000. For f_{in2} , the phase error is $5/16$ to $6/16$ and the digital readout is 0010. For f_{in3} , the phase error is $2/16$ to $1/16$ and the digital readout is 1001

TABLE 2
Four-bit codes representing phase difference and phase error

register output	absolute phase difference (cycles/16)	ϕ_e (cycles/16)
$Q_3 Q_2 Q_1 Q_0$		
0 0 0 0	15 to 16	7 to 8
0 0 0 1	14 to 15	6 to 7
0 0 1 0	13 to 14	5 to 6
0 0 1 1	12 to 13	4 to 5
0 1 0 0	11 to 12	3 to 4
0 1 0 1	10 to 11	2 to 3
0 1 1 0	9 to 10	1 to 2
0 1 1 1	8 to 9	0 to 1
1 0 0 0	7 to 8	-1 to 0
1 0 0 1	6 to 7	-2 to -1
1 0 1 0	5 to 6	-3 to -2
1 0 1 1	4 to 5	-4 to -3
1 1 0 0	3 to 4	-5 to -4
1 1 0 1	2 to 3	-6 to -5
1 1 1 0	1 to 2	-7 to -6
1 1 1 1	0 to 1	-8 to -7

Demodulation of phase modulated signals

Figure 21 is a block diagram of a 74HC/HCT297-based DPLL that can be used to demodulate signals which are phase modulated at a constant frequency. In this application, centre frequency f_0 should be equal to input frequency f_{in} . By using a strobe of constant frequency

(f_0), and phase-synchronized to f_{in} to latch the contents of the $\div N$ counter, phase errors can be read out digitally. Reference 4 describes the use of this kind of phase demodulation in Omega navigation receivers.

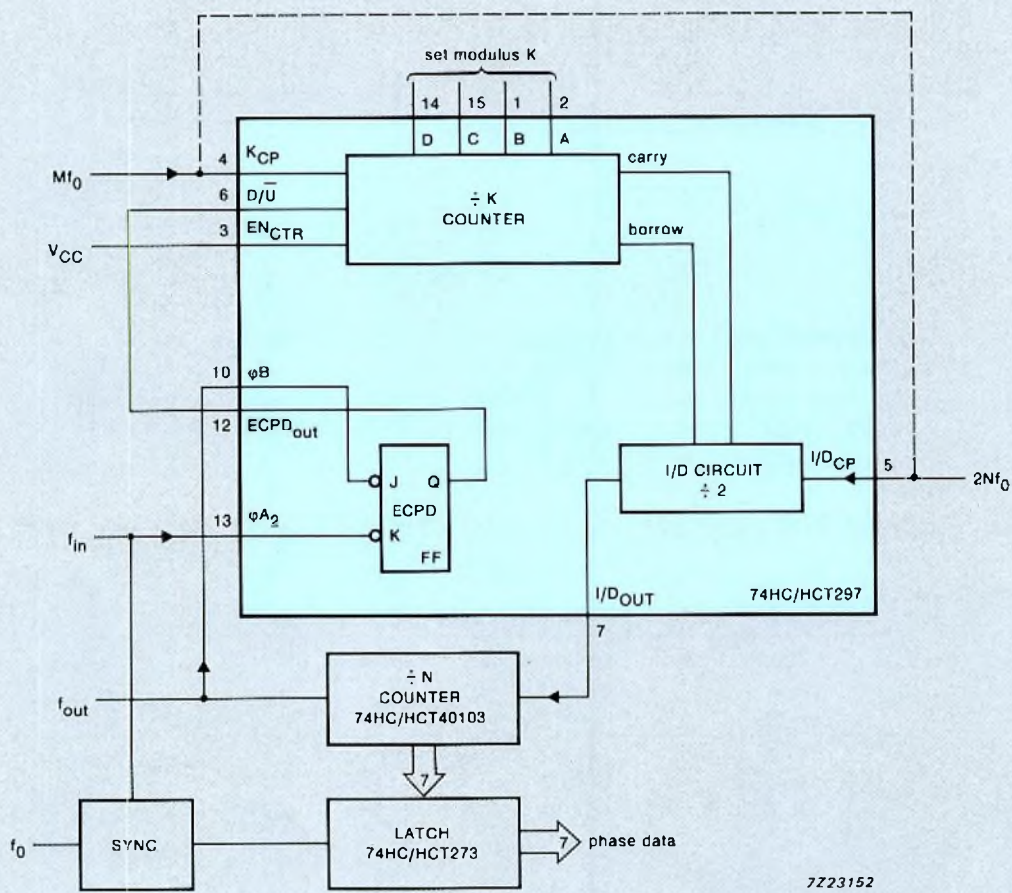


Fig.21 Digital phase-shift demodulator

Hold range extension

When both input signals to the phase detector are divided by the same modulus (L), the 3 dB frequency (ω_{3dB}) of the DPLL as given in equation (13) decreases by factor L . A circuit arrangement for doing this is shown in Fig.22.

If the ω_{3dB} frequency is now restored to its original value by decreasing K by factor L , equation (6) shows that the loop hold range is increased by factor L .

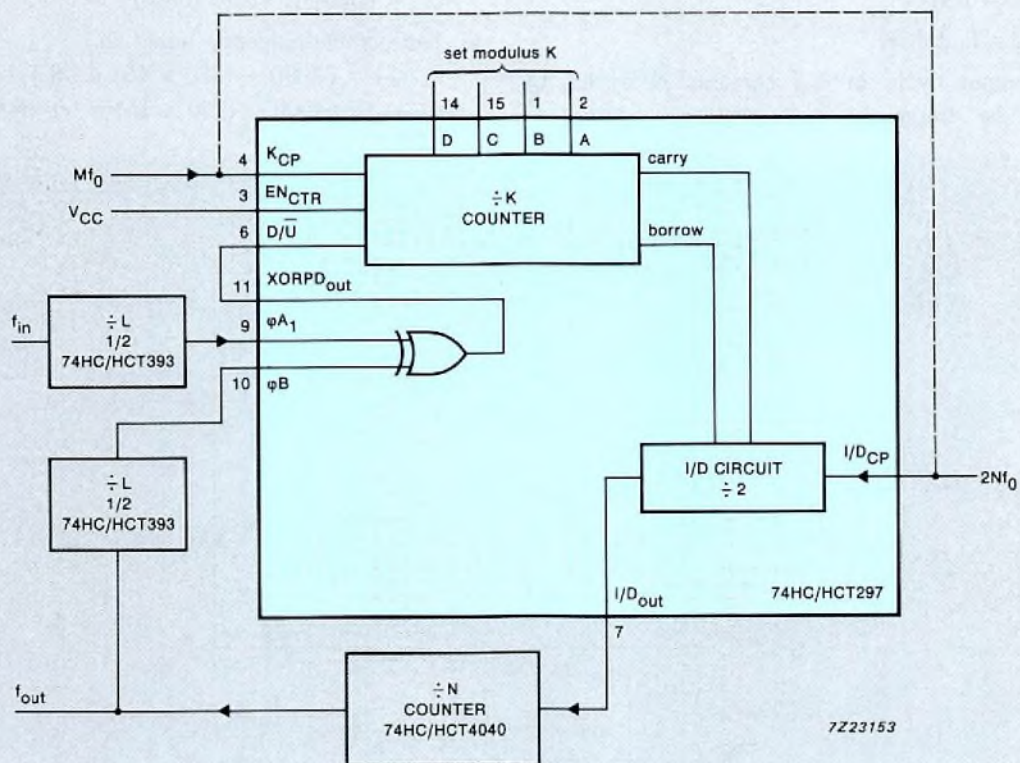


Fig.22 Hold range extension

DPLL used as a variable-frequency pulse generator

Because the output pulse rate of a DPLL is digitally-controlled, the DCO (+K counter plus I/D circuit) is very suitable for use as a pulse generator in which the output frequency can be varied in fixed increments around a centre frequency f_0 .

Figure 23 shows such a circuit in which the +K counter and I/D circuit clock frequencies are Mf_0 and $2Nf_0$ respectively. By applying pulses with variable duty factor and frequency to the down/up input of the +K counter, the centre frequency (f_0) range becomes:

$$f_{out \ max/min} = f_0 \pm Mf_0/2KN$$

Or, if the +K counter and the I/D circuit clock inputs are linked ($M = 2N$):

$$f_{out \ max/min} = f_0 \pm f_0/K$$

Since one output cycle of f_{out} contains N cycles of I/D_{out} , and the frequency is varied by adding or

subtracting pulses to/from the output, the output frequency can be varied in fixed increments of f_0/N . The total number of up/down increments is $M/2K$ or, for $M = 2N$, N/K .

As an example, consider a circuit in which centre frequency $f_0 = 64$ kHz, $N = 2^8 = 256$, $K = 2^4 = 16$, and the +K counter and I/D circuit clock inputs are linked ($M = 2N$):

- The frequency increment $f_0/N = 64000/256 = 250$ Hz
- The maximum number of up/down frequency increments is $N/K = 256/16 = 16$. So the output frequency range is:
 $f_{out} = 64000 \pm 250(0 \text{ to } 16)$
- The output frequency limits are:
 $f_{out \ max} = 64000 + (250 \times 16) = 68$ kHz
 $f_{out \ min} = 64000 - (250 \times 16) = 60$ kHz

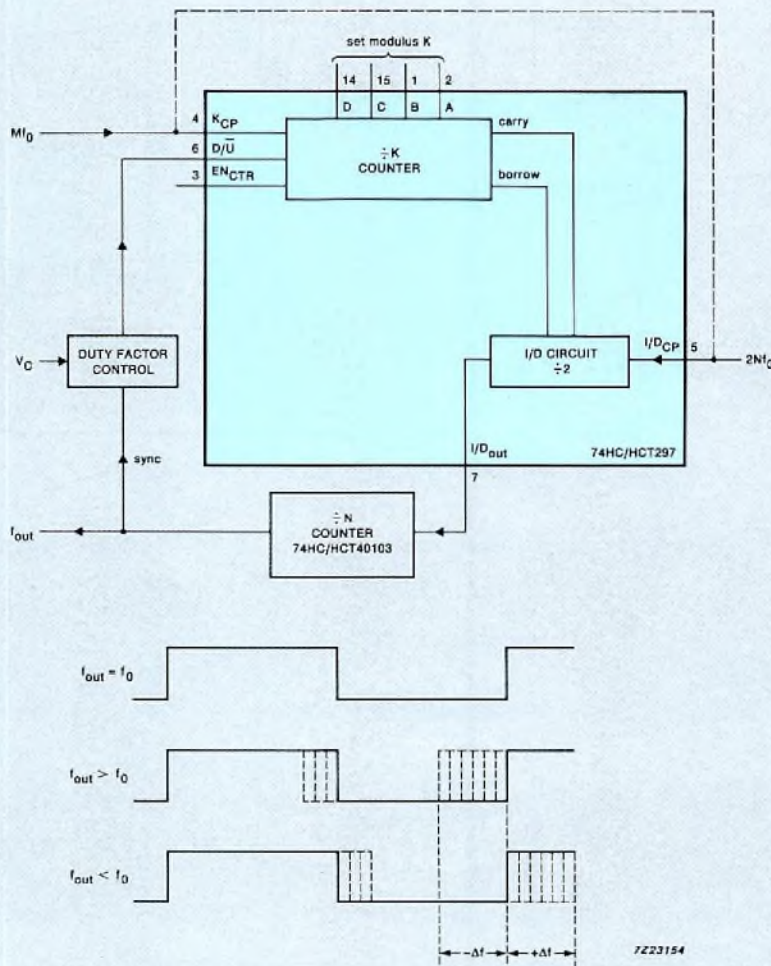


Fig.23 DCO used as a variable frequency pulse generator

Microprocessor control of centre frequency and bandwidth

Figure 24 is a block diagram of a DPLL in which the centre frequency and bandwidth are controlled in real-time by a microprocessor. To allow readout of the phase data and control of modulus N for the $\div N$ counter, the latter is divided into two parts; a programmable part for setting N and a fixed part for reading out the phase data. Such a circuit could be used to demodulate complex signals which contain several frequencies and several bandwidths.

The microprocessor can be made to read an out-of-lock condition so that its program can decrease modulus K to widen the hold range. Then, when a lock condition is read, phase error signal ϕ_e is used by the microprocessor to change modulus N , thereby altering the loop centre frequency until a minimum phase error signal (ϕ_e) is obtained. The microprocessor can then increase modulus K again to restore the narrower hold range.

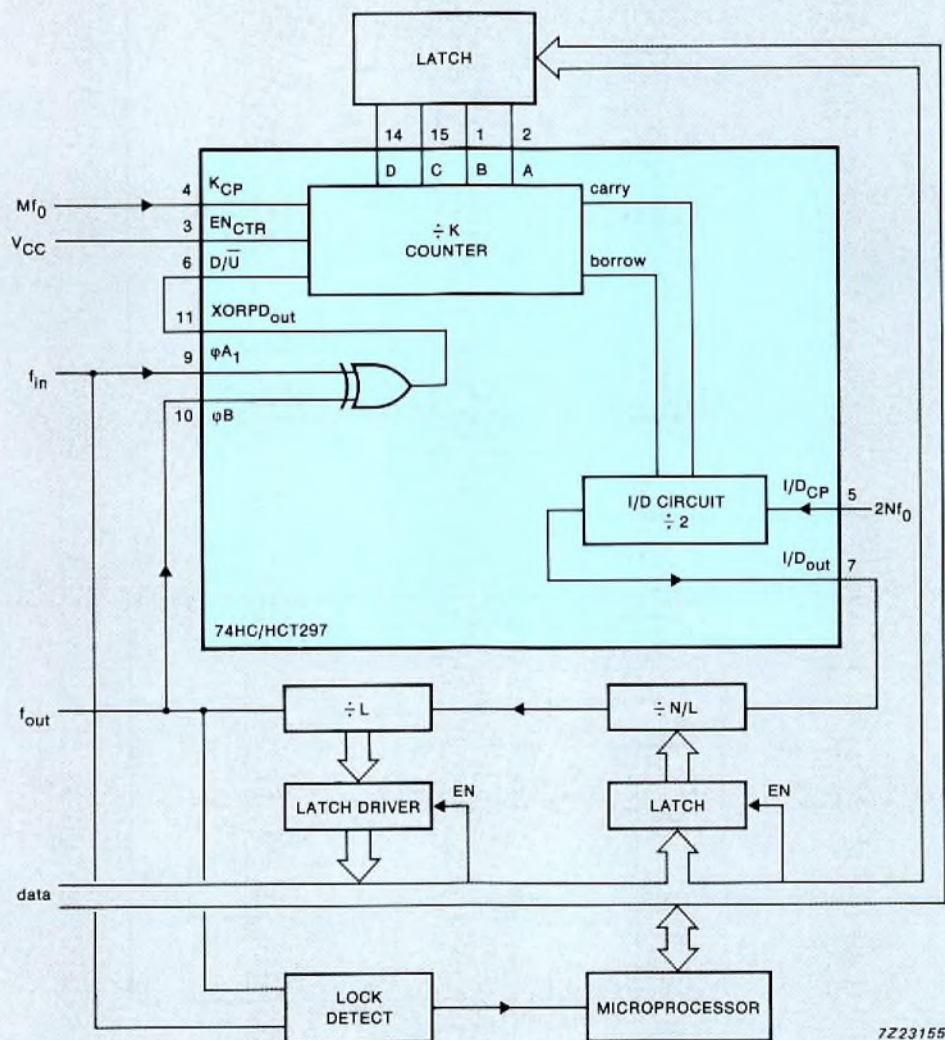


Fig.24 Microprocessor control of centre frequency and bandwidth

Second-order DPLLs

A higher-order analog PLL can be implemented by inserting a filter into the loop. A higher order DPLL can be implemented by cascading 74HC/HCT297 ICs as show in Fig.25 which is a block diagram of a second-order DPLL. Figure 26 is its loop diagram.

In principle, this second-order DPLL consists of two cascaded first-order loops, each using a 74HC/HCT297. The centre frequency of the overall DPLL is equal to

the loop 2 frequency and is therefore determined by the clock frequency of the I/D circuit of loop 2.

Since the output of the I/D circuit of loop 2 is used as a clock for the I/D circuit of loop 1, the output from the I/D circuit of loop 2 determines the centre frequency of loop 1. In fact, $f_{I/D\ CP}$ of loop 1 is derived from the output frequency of loop 2 and can be expressed as $2Nf_{out}$.

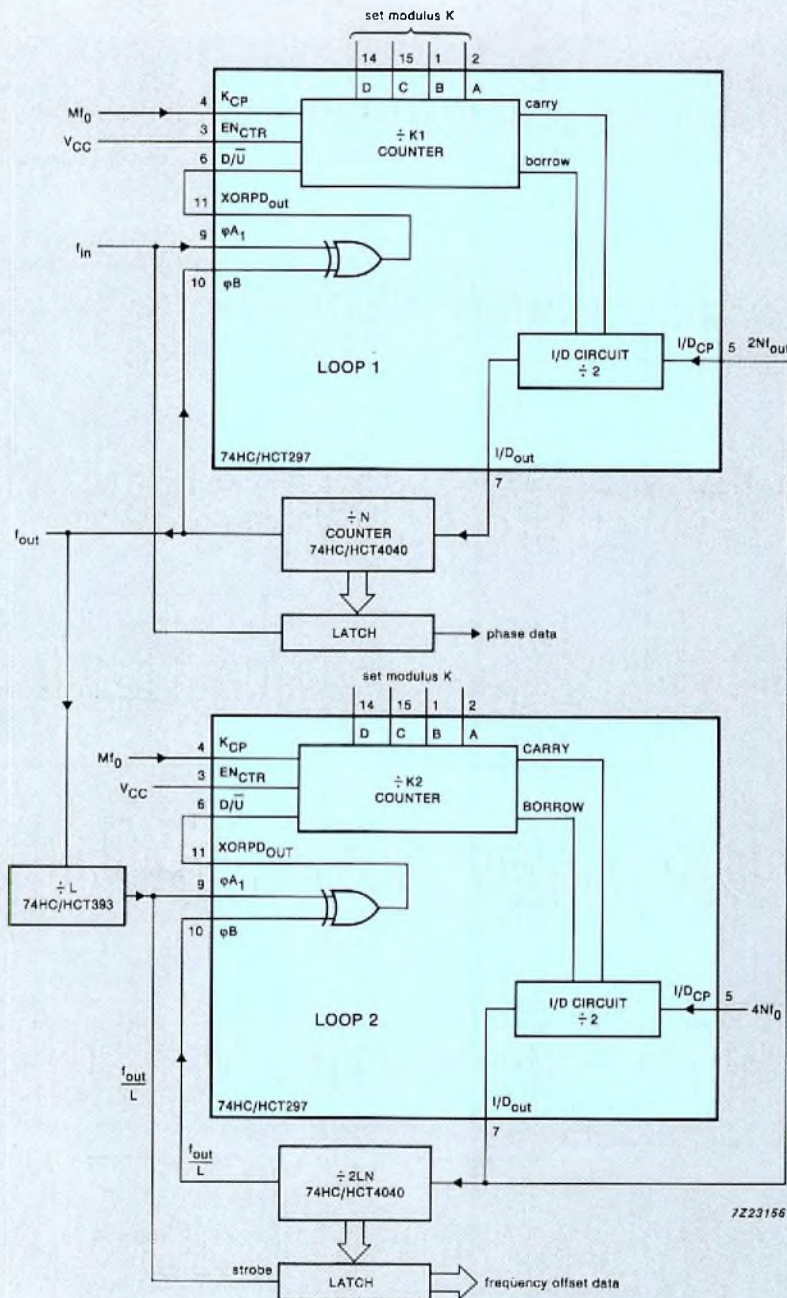


Fig.25 Arrangement of a second-order DPLL

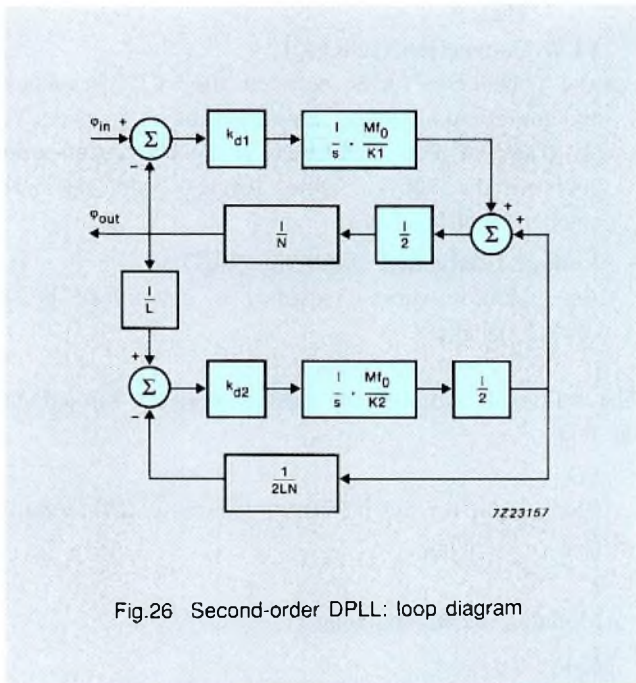


Fig.26 Second-order DPLL: loop diagram

Examination of Fig.26 shows that, if both loops are locked, the centre frequency of loop 1 is equal to that of incoming signal f_{in} . A second-order DPLL therefore tracks incoming signals within its hold range with a phase error of zero.

The hold range is determined by the components of loop 2:

$$\pm \Delta f_{H \max} = Mf_0/4K_2N \quad (18)$$

The phase error in loop 2 is proportional to the frequency difference between f_{in} and f_0 of loop 2:

$$f_{in} - f_0 = k_{d2}Mf_0\phi_o/4K_2N \quad (19)$$

So the frequency offset data can be obtained by latching the contents of the $+N$ feedback counter of loop 2 as previously described under the heading 'Digital readout of phase data'.

The transfer function for this second-order DPLL is:

$$H(s) = \phi_{out}(s)/\phi_{in}(s) = (\omega_1s + \omega_1\omega_2)/(s^2 + \omega_1s + \omega_1\omega_2) \quad (20)$$

where:

$$\omega_1 = k_{d1}Mf_0/2K_1N \text{ rad/sec} \quad (21)$$

and:

$$\omega_2 = k_{d2}Mf_0/4K_2LN \text{ rad/sec} \quad (22)$$

From the literature, the general equation for a second-order analog PLL using an active filter is:

$$H(s) = \phi_{out}/\phi_{in} = (2\zeta\omega_n s + \omega_n^2)/(s^2 + 2\zeta\omega_n s + \omega_n^2) \quad (23)$$

where ω_n is the natural frequency and ζ is the damping factor.

By comparing equations (20) and (23) expressions for the damping factor and natural frequency of a second-order DPLL can be derived:

$$\zeta = [\sqrt{(\omega_1/\omega_2)}]/2 \quad (24)$$

$$\omega_n = \sqrt{(\omega_1\omega_2)} \quad (25)$$

Reference 3 gives some information on the effects of damping factor and natural frequency on the performance of the loop.

APPENDIX - PLL TERMINOLOGY

The following is an alphabetically arranged list of PLL terms and the definitions used in this publication.

- Centre Frequency (ω_0, f_0)

The frequency at which the VCO operates if the input control voltage is half the supply voltage. Under this condition, the VCO frequency is in the centre of all the PLL operating ranges (see Fig.2). For an all digital PLL, the VCO operates half way between the minimum and maximum output pulse rate.

- Digitally-Controlled Oscillator (DCO)

In the DPLL, an Increment/Decrement (I/D) circuit and a programmable $\pm K$ counter form a digitally-controlled oscillator.

- Hold Range ($\pm\Delta\omega_H, \pm\Delta f_H$)

The range of input frequencies over which the loop, once locked, remains locked.

- Lock-in Range ($\pm\Delta\omega_L, \pm\Delta f_L$)

Within this range, the PLL acquires lock without skipping a cycle. Normally, the dynamic operating range of a PLL is restricted to the lock-in range. For frequency synthesizers, the term settling range is also used.

- Loop Noise Bandwidth (BL)

A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are strongly attenuated.

- **Low-Pass Filter (LPF)**
The low-pass filter in the loop permits only the DC and low-frequency signals to travel around the loop. It controls the pull-in range, noise and out-of-band signal rejection characteristics. It isn't used in a DPLL.
- **Natural Frequency (ω_n, f_n)**
The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. It can be determined experimentally by determining the modulation frequency that gives maximum output signal and phase error swing with an undamped loop.
- **Offset Frequency (ω_{min}, f_{min})**
The minimum frequency for the VCO.
- **Open-loop Gain (k_v)**
The product of the DC gains of all the loop elements between the phase error input signal and the output signal.
- **Output Frequency Range ($2\omega_R, 2f_R$)**
The maximum output frequency range of the VCO in a specific application or, for an all digital PLL, the difference between the minimum and maximum output pulse rate.
- **Phase Detector (PD)**
A circuit that compares the phases of two input signals and generates an output signal dependent on the relative phase difference. This error signal is fed to the low-pass filter. Some phase detectors have an output signal that also depends on the frequency difference. A phase detector that only checks for phase will drive the VCO to its centre frequency if f_{in} is much lower than f_0 . A phase/frequency detector will drive the VCO to its offset frequency.
- **Phase Detector Gain Factor (k_d)**
The relationship between the average output from the phase detector and the phase difference between its input and output. Its dimension is V/rad. For a digital PLL, it is expressed in terms of output per cycle of phase error.
- **Pull-in Range ($\pm\Delta\omega_{PI}, \pm\Delta f_{PI}$)**
Within this range, a PLL always acquires lock. The process may be rather slow and the time taken to acquire lock is called the pull-in time (t_p) or capture time.
- **Pull-out Range ($\pm\Delta\omega_{PO}, \pm\Delta f_{PO}$)**
This range of frequencies is the dynamic limit for stable operation of a PLL. A frequency step beyond this range causes the system to lose lock.

- **VCO Conversion Gain (k_o)**
The conversion factor between the VCO frequency and the control voltage. Its dimension is (rad/sec)/V, i.e. ($\Delta\omega/\Delta V$). For a DPLL, it is the conversion gain between the DCO output (cycles) and the $\pm K$ counter input level (± 1).
- **Voltage Controlled Oscillator (VCO)**
An oscillator whose frequency is determined by a control voltage

The following symbols are used extensively throughout the text:

- I/D_{CP}
Clock input for the increment/decrement (I/D) circuit ($f_{I/D\ CP} = 2Nf_0$)
- K
Modulus of the $\pm K$ counter
- K_{CP}
Clock input for the $\pm K$ counter ($f_{KCP} = Mf_0$)
- M
Multiple of the centre frequency to obtain the frequency of the $\pm K$ counter clock pulses
- N
Modulus of the $\pm N$ counter
- s
Complex operator
- sec
Second of time
- V_e
Output signal from the phase detector representing the phase error. For a DPLL, the range of V_e is from 1 to +1
- ζ
Damping factor of a second-order system
- Φ_e
Phase difference between f_{in} and f_{out}
- $\Phi_{in}, f_{in}, \omega_{in}$
Phase and frequency of the reference input signal to the phase detector
- $\Phi_{out}, f_{out}, \omega_{out}$
Phase and frequency of the output signal from the VCO
- $\omega_{3\ dB}$
The 3 dB bandwidth of the closed-loop gain (Φ_{out}/Φ_{in})

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PLL design program

Besides the PLL circuit 74HC/HCT297 (see article elsewhere in this issue), there are two other high-performance single-chip PLL circuits in Philips' High-Speed CMOS (HCMOS) range – the 74HC/HCT4046A and the 74HC/HCT7046A. Like the '297', both circuits have two digital phase comparators (EX-OR, and edge-triggered) with self-biasing input amplifiers. In addition, the 4046A has a third (edge-triggered) comparator, while the 7046A has improved lock-detection circuitry. Both circuits have an analog-controlled VCO which uses linear op-amp techniques to provide excellent frequency linearity over the whole control range.

To assist those designing with the '4046A' and the '7046A', a design program is available (Ref.1). The program which runs on an IBM PC or compatible (with MS-DOS) enables a complete HCMOS-based PLL including peripheral components to be designed and optimized fast. By eliminating the calculation drudgery associated with PLL design, the program invites experimentation, yet still reduces design time significantly.

The program is suitable for numerous applications such as FM and AM demodulation, frequency synthesis, FSK and PSK, and motor-speed-control to name but a few. It can also be used to evaluate and modify existing designs. To benefit from all of the program's features, a graphics card and printer are required, but these are not essential.

THE PROGRAM

The program starts by asking you to specify a few details about your system including some characteristics of the input signal, the supply voltage and the type of phase comparator you want to use. The calculations then start, using default settings which will always produce a stable loop design. During a calculation, on-screen messages inform you of progress, and may ask you to alter the value of parameters as the design proceeds. However, before any alteration is made, the effect on the other parameters is always described, and if you want, you can always return to the previous stage to reconsider your actions.

When the calculations are complete, the recommended values for the loop filter components and for the two bias components of the HCMOS circuit are displayed, together with the dynamic parameters of the complete phase-locked loop. The latter can then be optimized, although this isn't always necessary.

Optimization is an extremely useful feature of the program, allowing you to quickly tailor the dynamic loop parameters *exactly* to your specifications – a somewhat tedious process when done manually, owing to the interdependency of the parameters. Up to sixteen parameters can be altered individually, the new values of all dependent parameters being calculated in a few seconds.

After optimization, you can print the results and, if your PC has a suitable graphics card, generate a Bode plot of the open loop to examine the loop stability, returning to the optimization menu to make further modifications to the design as required.

With its interactive prompts and messages and an on-line 'help' facility, the program keeps the designer informed and in control at all times, and encourages the investigation of different routes to the design goal.

For many, the design program alone will be all that's needed before starting to prototype. For those requiring more insight into the theory behind the workings of the program, Reference 2 will be useful. As well as extensive application information on the '4046A' and '7046A', this reference contains worked design examples that include comparisons of predicted performance with the performance of real prototypes.

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MOSFETs control motors in automotive applications

ARTHUR WOODWORTH

The trend for comfort and convenience features in today's cars means that more electric motors are required than ever – a glance at Table 1 will show that up to 30 motors may be used in top of the range models, and the next generation of cars will require most of these features as standard in middle of the range models. Today, all these motors are usually controlled from the dashboard, requiring a lot of copper cable in the wiring harnesses – in some luxury models, for example, up to four kilometres of cable, weighing about 20 kg, is used. Such a harness might contain over 1000 wires, each wire requiring connectors at either end. Not only does this increase weight and cost, it can also create 'bottlenecks' at locations such as door hinges, where it becomes very difficult to accommodate large numbers of wires.

If, on the other hand, the motors were controlled by semiconductor switches located close to them, a lot of weight could be saved since these switches can be driven by much thinner, lighter wiring. And the use of multiplex wiring controlled by a serial bus could reduce weight even further.

In this article we discuss the use of such switches, and show how MOSFETs are better than bipolar switches for automotive applications. For example, MOSFETs have lower drive power requirements than bipolar switches, which need a constant bias. When active, bipolar switches consume and dissipate a lot more power than MOSFETs, making them less efficient. This is especially important when the energy source is a battery.

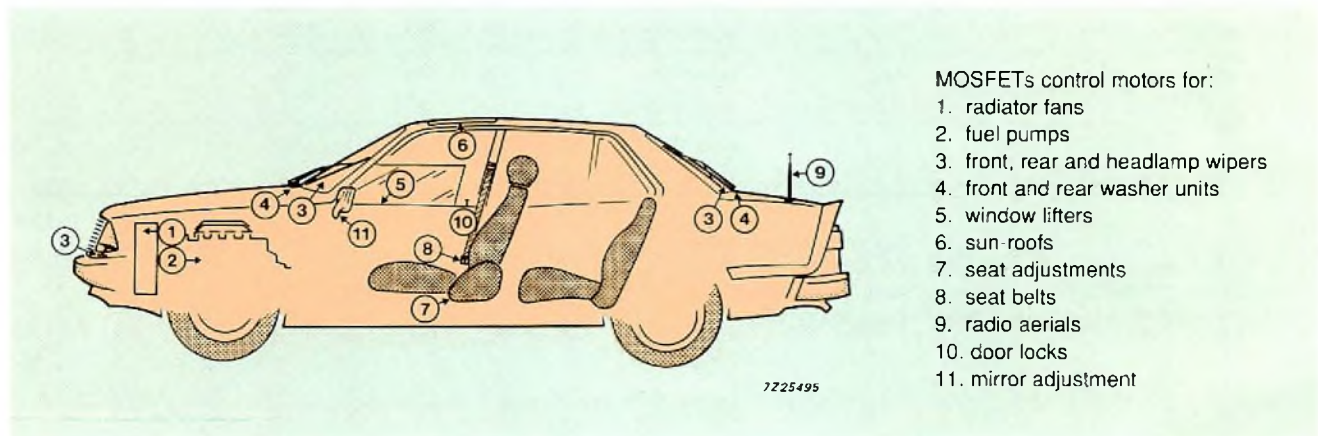


TABLE 1
Typical motor and switch requirements in a top of the range car

motor applications	typical power (W)	nominal current (A)	typical number of such motors	type of drive	typical number of switches per motor	proposed MOSFETs ¹⁾		comments
						standard BUK-	L ² FET BUK-	
air-conditioning	300	25	1	unidirectional, variable speed	1	456	556	Active suspension may also require such a high power motor
radiator fan	120-240	10-20	1	unidirectional, variable speed	1	455	555	These motors may go brushless, requiring 3 to 6 lower rated switches
fuel pump	100	8	1	unidirectional	1	453	553	
wipers: front			1-2			452/ 453	552/ 553	Reversing action is at present mechanical. This could be done electronically using 2 or 4 switches
rear	60-100	5-8	1	unidirectional, variable speed	1			
headlamp			2					
washers: front	30-60	2.5-5	1-2	unidirectional	1	452	552	
rear			1-2					
window lifter	25-20	2-10	2-4	reversible	4	452/ 455	552/ 555	
sun-roof	40-100	3.5-8	1	reversible	4	452/ 453	552/ 553	
seat adjustment (slide, recline, lift, lumbar)	50	4	4-16	reversible	4	453	553	
seat belt	50	4	2-4	reversible	4	453	553	
pop-up headlamp	50	4	2	reversible	4	453	553	
radio aerial	25	2	1	reversible	4	452	552	
door lock	12-36	1-3	6-9	reversible	4	451/ 452	551/ 552	
mirror adjustment	12	1	2	reversible	4	451	551	

¹⁾ These are meant for general guidance only. Specific applications should be checked against individual users requirements. In addition to standard and L²FETs, FREDFETs, SensorFETs and IPS might be considered. Also, a variety of isolated and non-isolated package options are available.

TYPES OF MOTORS USED IN MOTOR VEHICLES

Owing to the ever-present pressures of cost, weight and space associated with the automotive components market, designing electric motors with the required torque/speed characteristics for the application presents a difficult compromise.

Factors determining the motor design are:

- peak load current – also known as starting current or stall current, which is determined by the resistance of the motor, and which has a direct influence on the starting torque. In most applications, it's important that any switches used should be able to handle the peak current
- nominal load current – also known as working current, which is highly dependent on the application; the same motor may be used to drive a fan with one nominal current, and as a window drive with a completely different value (a motor for intermittent use will be optimized for maximum power output at its operating speed). In the latter case a higher current density is acceptable, which may lead to a three- or four-fold increase in power output.

There are four main types of DC motor which can be used in cars (see box). These types can be divided into commutator motors and brushless motors.

MOTOR DRIVE CONFIGURATIONS

Although the drive requirements for commutator and brushless DC motors differ, suitable transistors from our range of MOSFETs can be used for both.

Commutator motors

Figure 1 shows how a wound-field DC commutator motor or a PM DC commutator motor can be controlled by a switch in series with the DC supply. Traditionally, relays have been used, but they are not considered to be very reliable, particularly in high vibration environments. Semiconductors offer an attractive alternative, providing:

- low on-state voltage drop (acceptable levels are <10% of the supply voltage at maximum current – say <1 V)
- low drive power requirements
- immunity from vibration.

The power MOSFET scores on all counts, offering on-state resistances of a few m Ω and requiring only a few volts (at almost zero current) at the gate to achieve this.

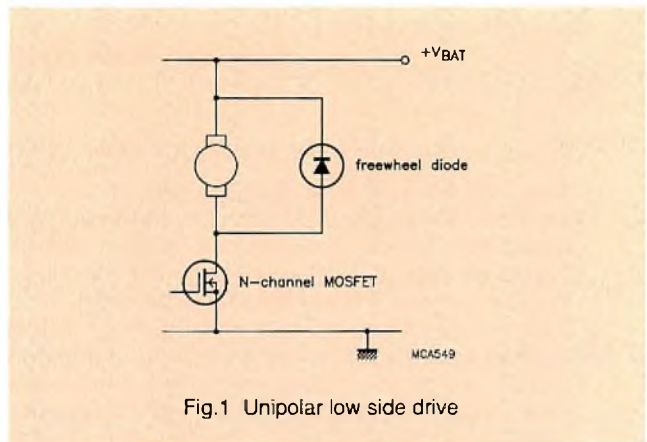


Fig.1 Unipolar low side drive

When a motor is switched off, it may or may not be turning. If it is, then the motor acts as a voltage source, and its kinetic energy is transformed into electrical energy and dissipated or returned to the supply, via a freewheel diode. If it is not turning, then the motor appears purely as an inductance and for a low-side switch (a switch connected between load and ground), the voltage transient developed will take the MOSFET into avalanche. Depending on the magnitude of the energy stored in the field and the avalanche capability of the MOSFET, external protection may or may not be required.

If $\frac{1}{2} L_m I_m^2 < W_{DSS}$, then no protection is required.

Reversing the polarity of the supply reverses the direction of rotation (e.g. for a sun-roof). This usually requires a bridge of semiconductors, see Fig.2. In this case the intrinsic source-drain diodes in the MOSFETs eliminate the need for external switching diodes. Note that the on-state voltage drop is across two devices in series; thus to maintain the same low value of voltage drop across the switches, the crystal area of each MOSFET must be doubled. This means that with four switches being used in a reversing bridge, eight times the crystal area is required compared with a unidirectional drive.

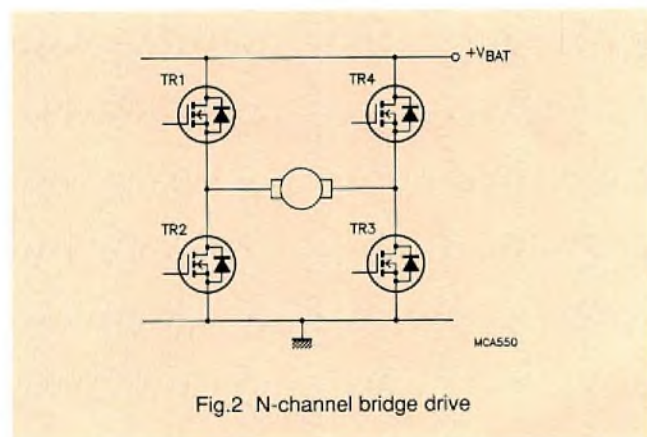
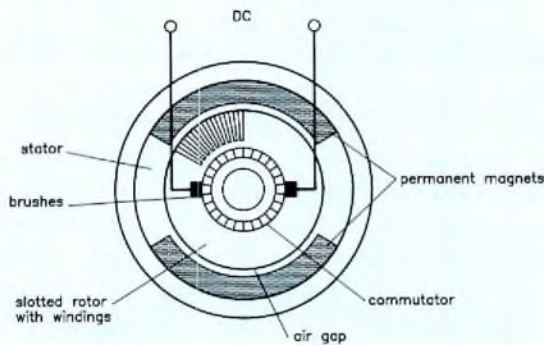


Fig.2 N-channel bridge drive

FOUR MOST COMMON MOTORS USED IN MOTOR VEHICLES

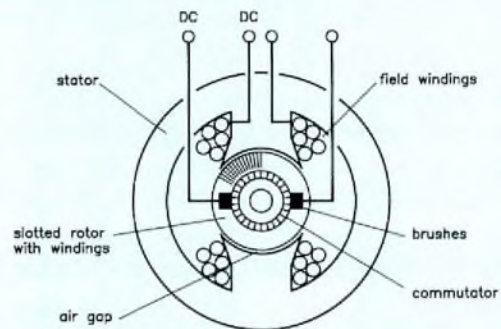
Permanent magnet (PM) DC commutator motor

These are the types most commonly used in cars. The permanent magnet forms the stator, the rotor consists of a slotted iron cylinder containing the copper windings. They're generally used below 5000 rpm, and they have a linear torque/speed characteristic. The graph shows typical curves relating torque, speed, current and efficiency. They have a lighter rotor and a smaller frame size than wound-field DC commutator motors, and a much lower inductance (typically 100 – 500 μ H). New materials (e.g. neodymium/iron/boron compounds) offer even more powerful fields in smaller volumes.



Wound field DC commutator motor

The stators of these motors have field windings, the rotor supply is fed via brushes and a multi-segment commutator. Although once widely used, they are being replaced mainly by PM motors. They are contained in characteristic square frames, and they may be series wound (with high torque at start-up but tending to 'run away' on no-load), shunt wound (with relatively flat speed/torque characteristics) or more rarely, compound wound.

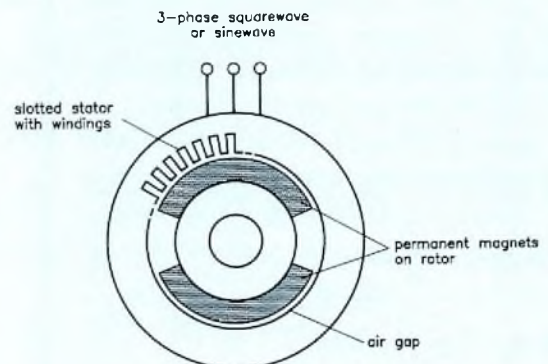
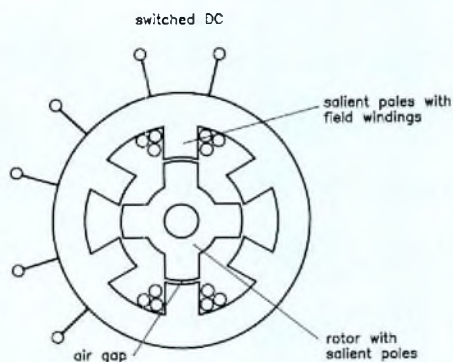


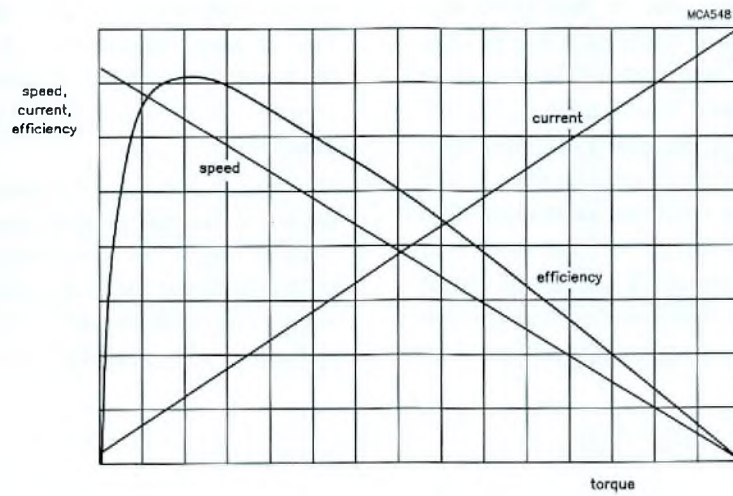
PM brushless DC motor

Although not yet extensively used in cars, these motors are under consideration for certain specialized functions e.g. fuel pumps where their arc-free operation makes them attractive. As their name suggests, they have neither mechanical commutator nor brushes, so there's no brush noise/wear and associated maintenance. Instead they have a wound stator and a permanent magnet rotor. They depend on electronic commutation and require a rotor position monitor, which may use magnetoresistive sensors, Hall effect sensors or induced signals in the non-energized winding. Thanks to their lightweight, low-inertia rotor they offer high efficiency, high power density, high-speed operation and high acceleration.

Switched reluctance motor

These motors are the wound-field equivalent to the PM brushless DC types. Although not widely used, they have been proposed for some of the larger motor applications such as radiator and air conditioning fans, where their high power/weight ratio makes them attractive. They can also be used as stepper motors in such applications as ABS and throttle control.





For a constant load, the speed of the motor can be controlled by a chopped voltage, which would control the voltage across the motor windings. In the case of the bridge, TR1 and TR4 might be used to control direction, while a chopping signal (typically ≥ 20 kHz) is applied to TR3 or TR2. When reversing the direction of rotation, it is necessary to arrange the gating logic so that it goes through a condition with TR1, TR2, TR3 and TR4 off to prevent short-circuiting the supply.

Switched field motors

PM brushless DC motors typically require six switches to generate the rotating field, see Fig.3. Simpler versions operating at lower power density in the motor are possible with three switches, which may be connected on the high- or low-side, see Fig.4.

Switched-reluctance motors may use as few as four or as many as twelve switches to generate the rotating field.

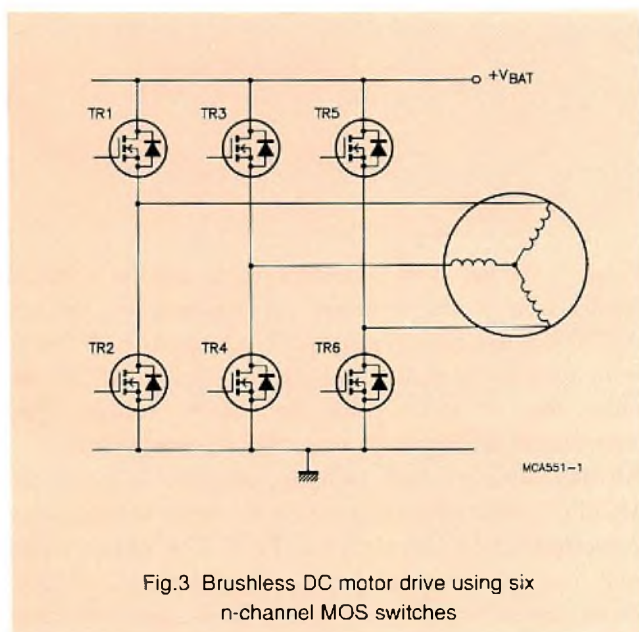


Fig.3 Brushless DC motor drive using six n-channel MOS switches

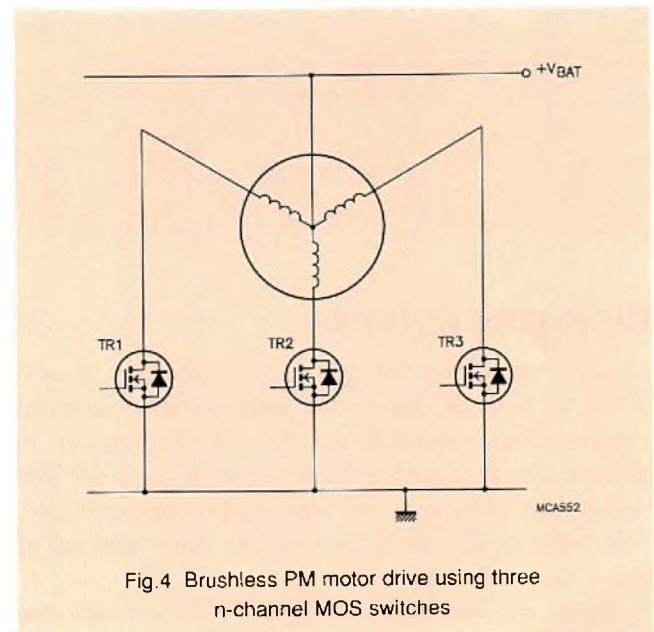


Fig.4 Brushless PM motor drive using three n-channel MOS switches

Figure 5 shows a four-switch version. For all switched-field motors, change of direction and speed are controlled by the timing of the field pulses. In the case of brushless DC motors these timing pulses can be derived from a dedicated IC, such as the Philips NE5570. Rotor position sensing is required (using e.g. magnetoresistive sensors) to determine which windings should be energized. Compared with a DC commutator motor, the power switches for a brushless motor have to be fast, because they must switch at every commutation. Pulse width modulation (PWM) speed control pushes up the required switching speed even further. Philips MOSFETs are designed so that both switch and in-built diode are capable of efficient switching at the highest frequencies and voltages encountered in automotive applications.

- **P-channel switches.** These simplify the drive circuit which only needs referencing to the positive supply, see Fig.6. Unfortunately P-channel switches require almost three times the silicon area to achieve the same low on-state resistance as N-channel types, which increases cost. Also, P-channel devices that can operate from logic level signals are not readily available.
- **N-channel switches.** To ensure that these are fully turned on, the gate must be driven 10 V higher than the positive supply for conventional MOSFETs, or 5 V higher for Logic Level (L²) FETs. This higher voltage might be derived from an auxiliary supply, but the cost of ‘bussing’ this around the vehicle is considerable.

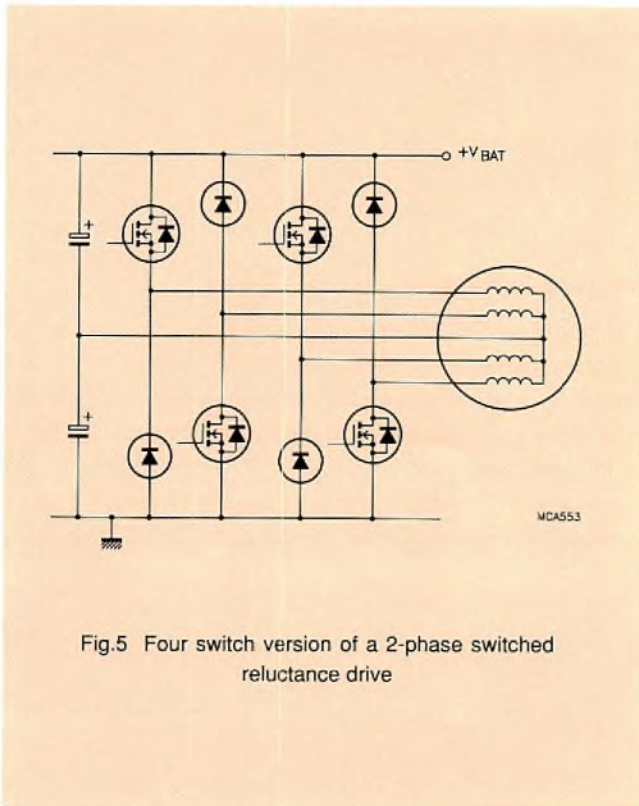


Fig.5 Four switch version of a 2-phase switched reluctance drive

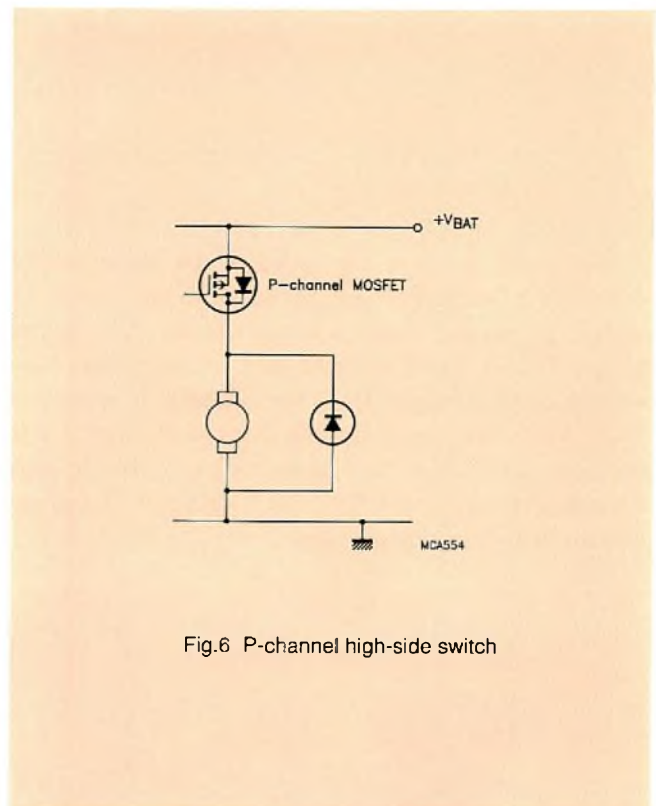


Fig.6 P-channel high-side switch

HIGH-SIDE DRIVERS

Often, in motor vehicles, there is a requirement for the switch to be connected to the positive battery terminal with the load connected via the common chassis to negative. Negative earth reduces corrosion and a low-side load is safer when loads are being worked on or replaced. Also, when bridges are being used, the upper arms are of course high-side switches.

There are two MOSFET possibilities for high-side switches:

Figure 7 shows how additional drive can be obtained locally from a charge pump. An oscillator (e.g. Philips AU7555D) free runs to generate a rectangular 12 V waveform, typically at around 100 kHz. A voltage doubler then raises this to about twice the battery voltage. This arrangement is suitable for both ‘DC’ or chopper drives. An alternative approach to bridge choppers is to use the MOSFETs themselves to generate the drive voltage using a bootstrap circuit, as shown in Fig.8. This circuit works well over a range of mark-space ratios from 5% to 95%. Zener diodes should be used in this circuit to limit transients which may occur on the auxiliary line.

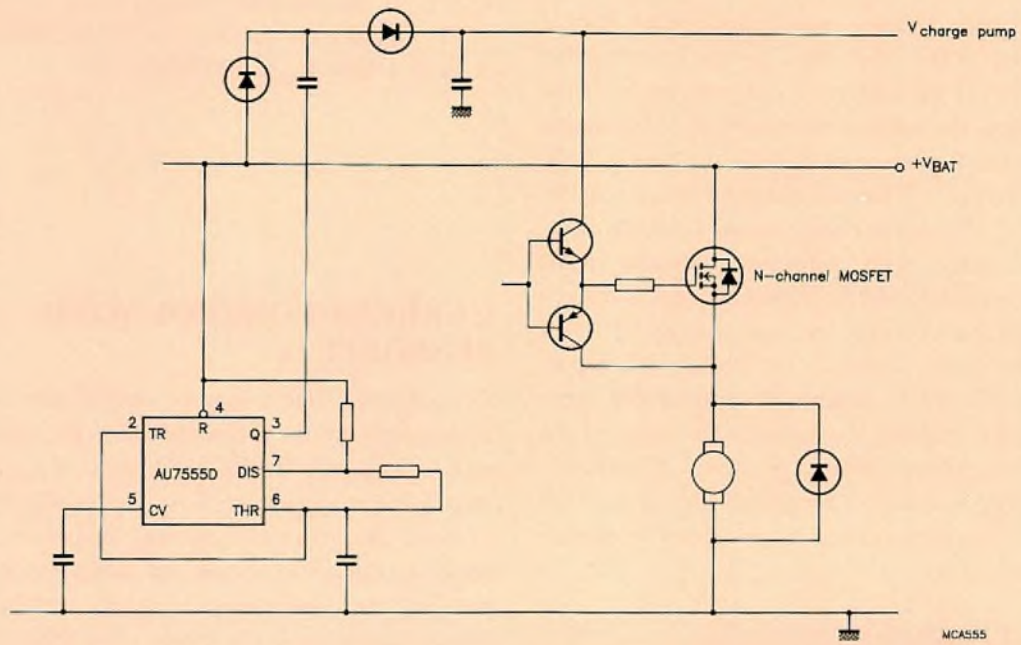


Fig.7 N-channel high-side switch with charge pump

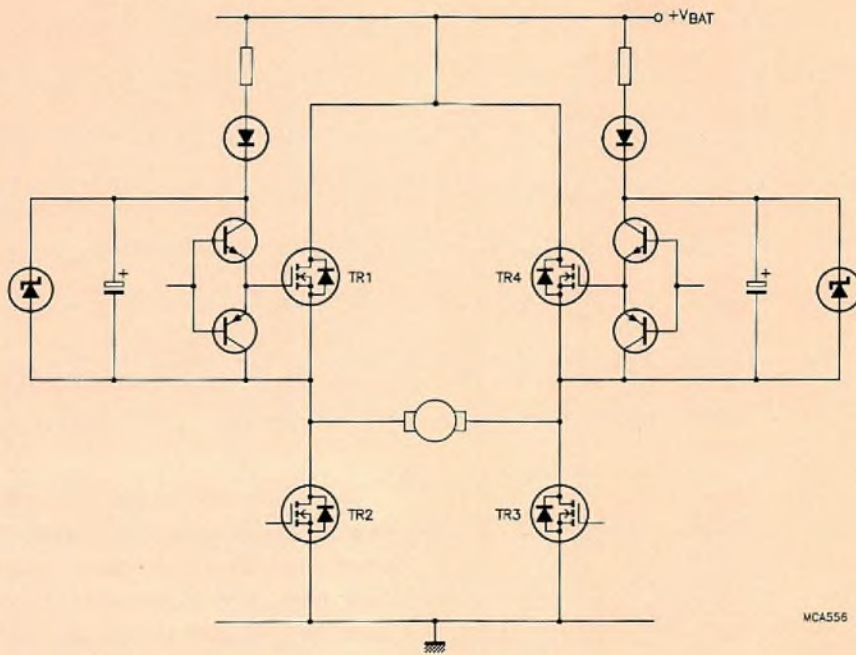


Fig.8 Bootstrap bridge drive

DEVICE REQUIREMENTS

Voltage

The highest battery voltage encountered under normal operation of a car is 16 V, but under jumper lead start this can rise to 22 V. If the battery is disconnected with the alternator running, the voltage can rise to 50 V (assuming external protection is present) or 60 V in the case of 24 V batteries (see Table 2). Thus the normal voltage requirement is 50/60 V. The power supply rail in a vehicle, however, is very noisy, with numerous inductive loads switching and generating voltage spikes and surges of both polarities, singly and in bursts, and with voltages of 100 V or more and durations of about 1 ms (Ref.2). It's important to choose MOSFETs capable of withstanding these stresses, either by ensuring V_{DS} exceeds the value of the transients or by selecting 50/60 V devices with sufficient avalanche energy capability to absorb the pulse. For transients exceeding these values it's necessary to provide external local protection.

TABLE 2
Conditions affecting automotive voltages
(12 V nominal supply)

voltage range	cause
>50 (60)*	coupling of spurious spikes
30 to 50	clamped load dump
22 to 30	voltage surge on cut-off inductive loads
16 to 22 (32 to 40)*	jump start or regulator degraded
10.5 to 16 (20 to 32)*	normal operation condition
8 to 10.5	alternator degraded
6 to 8 (9 to 12)*	starting a petrol engine
0 to 6 (0 to 6)*	starting a diesel engine
negative	negative peaks or reverse connected battery

* 24 V supply

Temperature

Ambient temperature requirements vary from -40 to +85 °C in the passenger compartment, and from -40 to +125 °C under the bonnet. All Philips MOSFETs shown in Table 1 have $T_{jmax} = 175$ °C.

CURRENT CONTROL WITH SENSORFETs

Occasionally, motors may be stalled; then the current is limited only by the series resistance of motor and switch and so a current five to eight times the running current will flow through the combination, possibly damaging one of them. The effect of increasing temperature, causing the series resistance of motor and switch to rise, gradually reducing the current can clearly be seen in Fig.9. Also, during maintenance the motor may become shorted out resulting in much higher current through the switch.

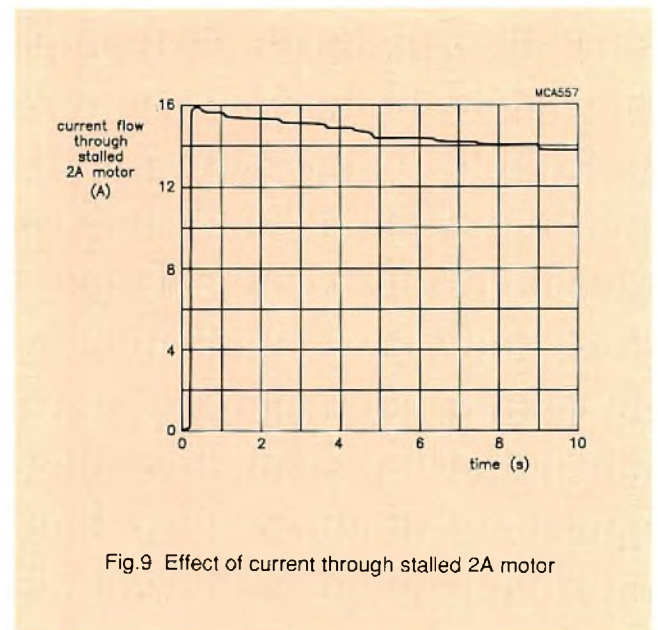


Fig.9 Effect of current through stalled 2A motor

While it would be possible to use series sensing resistors to detect overload current, these expensive, high power-dissipation components cause an undesired voltage drop during normal operation. If wire-wound resistors are used, their inherent inductance results in the generation of voltage spikes. Figure 10 shows the voltage drop across a 0.03 Ω wire-wound resistor in series with the source of a MOSFET monitoring the start-up of a motor. The inductive overshoot and ringing can clearly be seen.

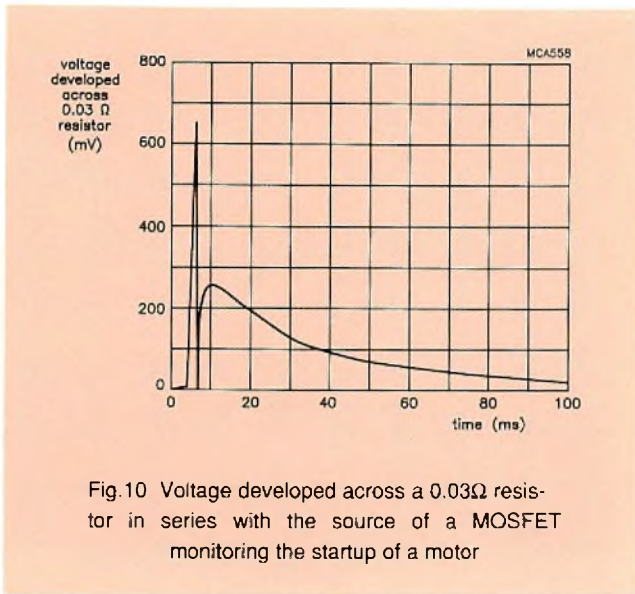


Fig.10 Voltage developed across a 0.03Ω resistor in series with the source of a MOSFET monitoring the startup of a motor

SensorFETs, on the other hand, such as the BUK793-50 or BUK795-50 can provide ‘loss-less’ current sensing. With these devices, a separate connection to a few of the source cells, called sensor cells, is made. Thanks to the inherently good cell matching, the sense current is a known proportion of the total. If this sense current is fed through a low-power resistor, the voltage across this resistor can, with suitable circuitry, be used to limit or shut down the sensorFET gate drive in the event of excessive current.

Pulse width modulation (PWM) drives for efficient switching

When a DC motor in a car is turned on, an initial surge current is drawn which again may be five to eight times the running current. However, for the starting torque to be unaffected it is important to allow a surge current of at least two to five times the running current for the start-up period of around 100 ms, see Fig.11.

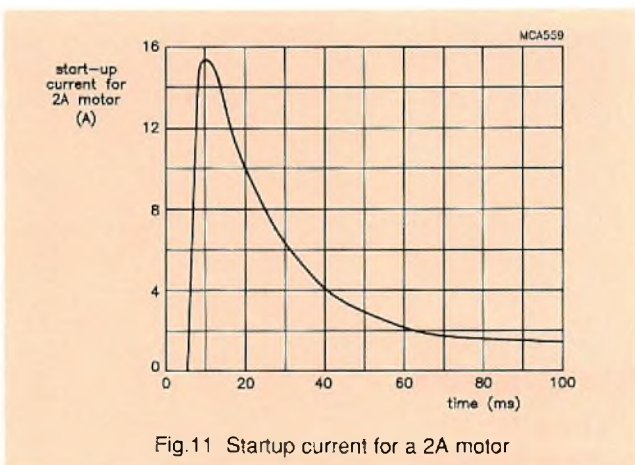


Fig.11 Startup current for a 2A motor

If a motor speed of less than the maximum is required, the mean current must be decreased. This can be done by using either a current-limiting resistor e.g. a MOSFET which is not fully turned on (see Fig.12), or by a PWM drive. Use of the non-saturated MOSFET as a resistor results in high power dissipation. A PWM drive, however, will switch the MOSFET fully on and off, minimizing dissipation. This may require some filtering to determine the mean value of the sense current, see Fig.13.

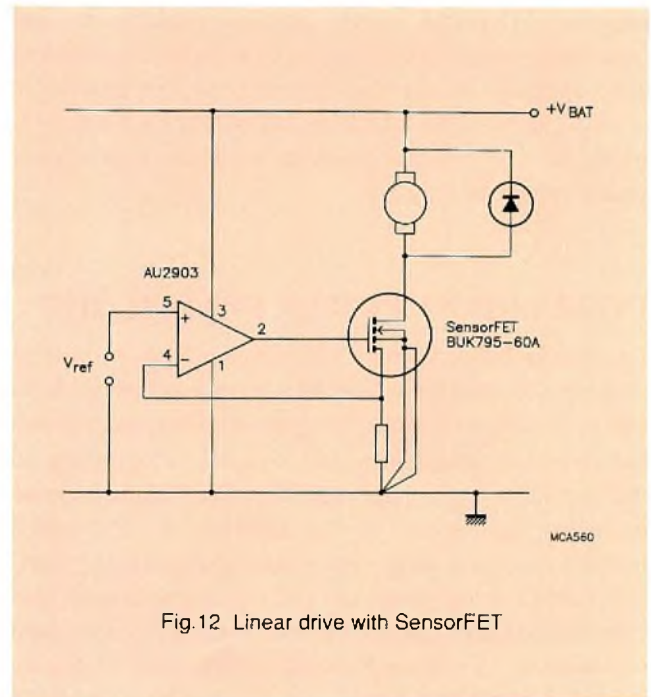


Fig.12 Linear drive with SensorFET

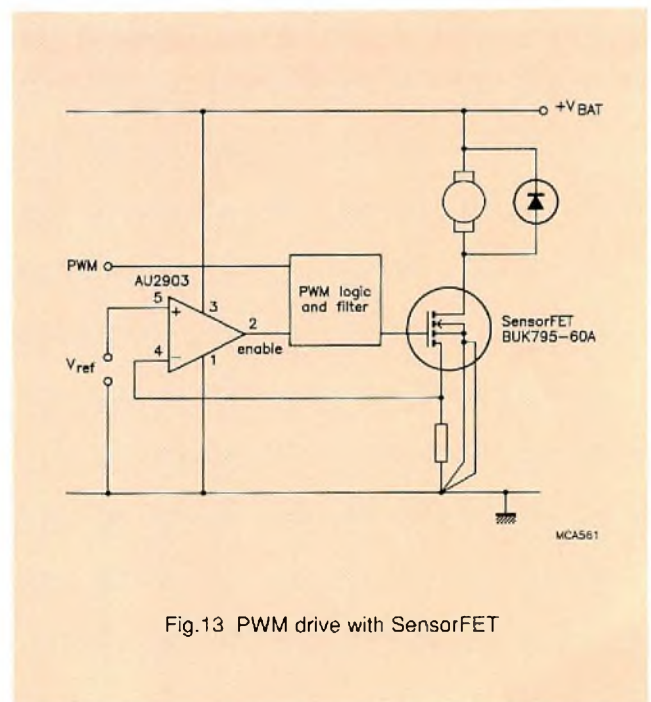


Fig.13 PWM drive with SensorFET

L²FETs

The battery voltage in a car is a nominal 12 V. This can vary from 10.5 V to 16 V under normal operation. It's important that the MOSFET switches be fully turned on at these voltages, bearing in mind that for high-side switches it may be necessary to derive the gate drive from a charge pump or bootstrap circuit. While a gate source voltage of 6 V is usually sufficient to turn a conventional MOSFET on, 10 V is required to achieve the lowest on-state resistance. Thus the margin between available and required gate drive voltage may be quite tight in automotive drive applications. One way to overcome this problem is to use L²FETs such as the BUK553-50A or BUK555-50A, which have a very low on-state resistance with a gate-source voltage of only 5 V.

INTELLIGENT POWER SWITCH (IPS)

An ideal high side switch to drive motor loads is one that could be switched on and off by a ground-referenced logic signal, is fully self-protected against short-circuit motors and excessive temperatures and is capable of reporting on the load status to a central controller. The Philips response to these requirements is the BUK196-50 IPS, which features on-board charge pump and level shifting, short-circuit and thermal protection and status reporting of such conditions as open- or short-circuit load. With an on-state resistance of 33 m Ω the BUK196-50 is capable of driving motors of up to 25 A, see Fig.14. The combination of IPS on the high-side and L²FET on the low-side enables a self-protected, reversible bridge to be designed that is compatible with standard TTL/CMOS logic levels, see Fig.15.

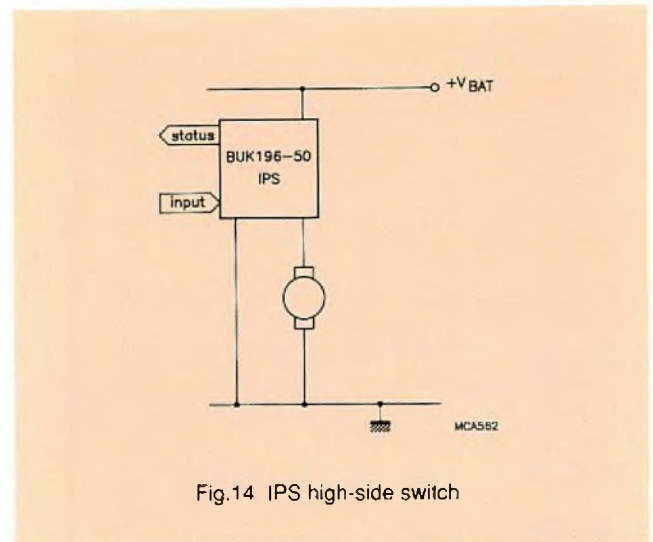


Fig.14 IPS high-side switch

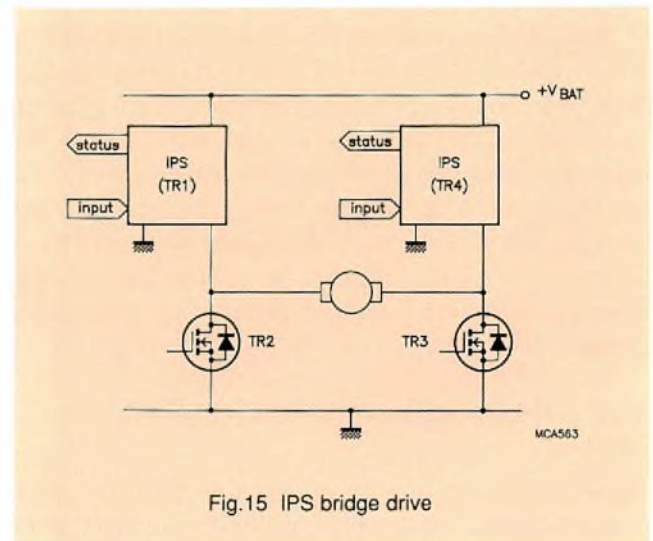


Fig.15 IPS bridge drive

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2. ISO-DIS-7637-1

Focusing semiconductor laser diodes in barcode readers

PETER CHALL

Barcodes are having an enormous impact on everyday life. From point-of-sale automation to inventory control in warehouses and retail outlets, they are an accepted way of coding product type, price, date of manufacture, and so on. The printed codes are optically scanned, either automatically (as in a supermarket checkout where products are passed over a "window" under which a laser seeks and scans the barcode), or manually with a hand-held scanner.

For barcode scanners, a focused spot of light must be able to resolve very small and sometimes poorly printed barcodes at a specified distance. The spot diameter must also remain within certain tolerances over a specified working depth. The actual focused distances and working depths will vary according to the application of the barcode reader. Figure 1 shows the basic principles of barcode scanning with a laser source.

In the past, helium-neon (He-Ne) lasers were in general use for reading barcodes. This, however, is rapidly changing. Today, semiconductor laser diodes with built-in focusing lenses offer compact, cost-effective, low-voltage, easy-to-use and above all, reliable alternatives to the bulky and fragile He-Ne laser. And with the recent introduction of visible light semiconductor lasers, the end for He-Ne lasers in barcode readers is in sight.

Thanks to our vast experience in using semiconductor laser diodes in Compact Disc and Laservision products, we can supply lasers with integrated optics that produce collimated and focused light beams for use in a whole range of applications, not limited to barcode scanners but also for laser printers, and systems for robotic guidance and triangulation measurement.



The laser collimator pen for use in barcode readers

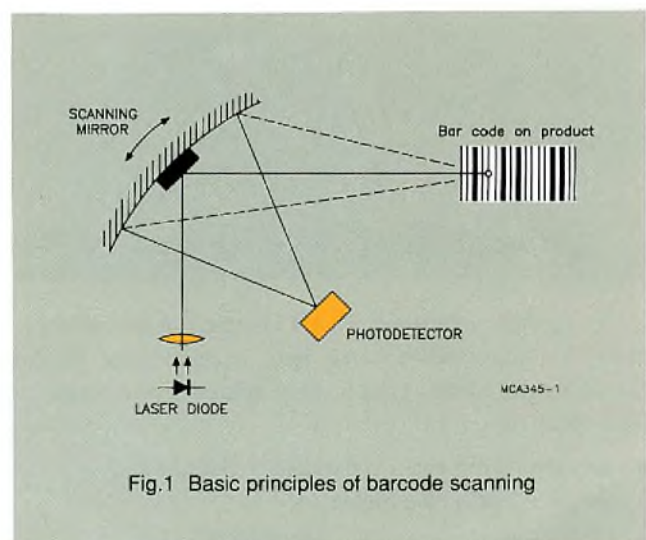


Fig.1 Basic principles of barcode scanning

This article summarizes an evaluation of our laser diode focusing system and demonstrates its suitability for use in barcode scanners. It shows how the focused spot diameter and beam profile can be guaranteed to within acceptable tolerances for the typical focusing distances and working depths used for such scanners.

Barcode scanners

In all laser scanning applications, a beam must be focused to the required spot size at the system's defined working depth. The dimensions of the spot must stay within well defined limits, determined by the spacing of the printed bars in the code.

In our integrated laser diode/aspheric focusing lens package, accurate control of the relative positions of the critical elements is possible, and therefore allows considerable flexibility in the choice of focusing distance, working depth and spot size.

The use of thermally-matched materials for the housing and lens minimizes temperature-related variations of spot size and focusing depth. The result is a highly temperature-stable device.

Focusing a laser diode

Before detailing the evaluation, we'll first outline a few basic principles of focusing a semiconductor laser diode. Figure 2 shows a typical scheme for a laser diode focused at a distance d . The diameter of the spot (ϕ) must remain within tolerance throughout a working depth range 2δ .

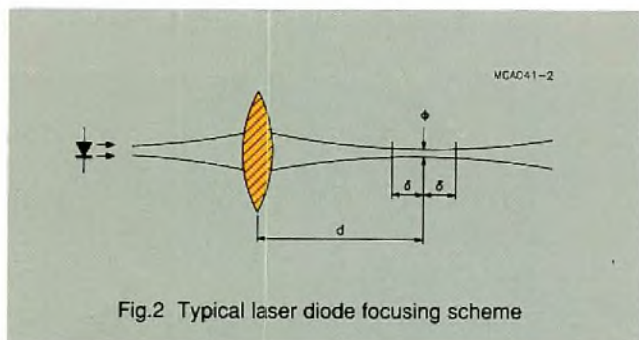


Fig.2 Typical laser diode focusing scheme

To further understand what's involved in this arrangement, it's necessary to take into account some typical characteristics of this type of laser source. For example, a laser diode has:

- an asymmetric beam waist ($2w_{\perp} \approx 0.5 \mu\text{m}$ and $2w_{\parallel} \approx 1.5 \mu\text{m}$) (see Fig.3)
- high emission angles ($\theta_{\perp} \approx 30^{\circ}$ and $\theta_{\parallel} \approx 10^{\circ}$).

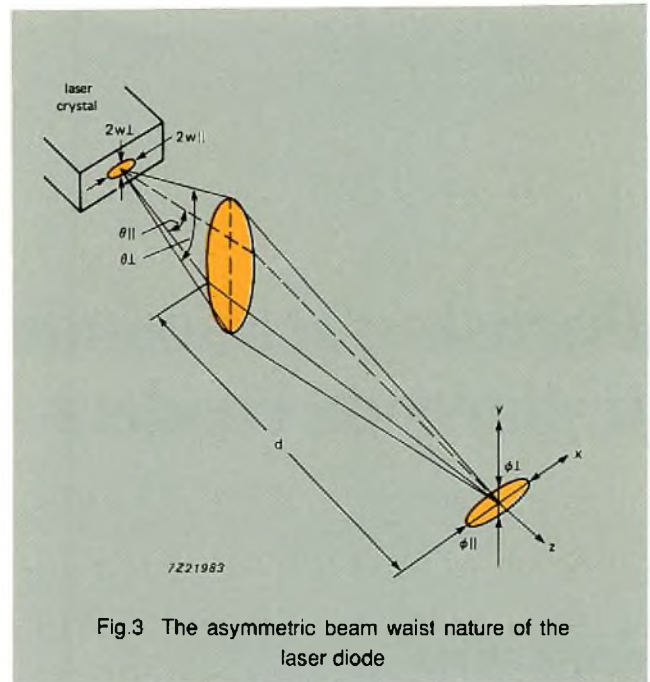


Fig.3 The asymmetric beam waist nature of the laser diode

A laser diode can be considered as a point source, and consequently the beam has a divergent spherical wavefront. A lens transforms this divergent wavefront to a convergent spherical wavefront (see Fig.4) and thereby alters the radius of curvature of the wavefront from R_0 to R_1 according to:

$$1/R_0 + 1/R_1 = 1/f$$

where f is the focal length of the lens.

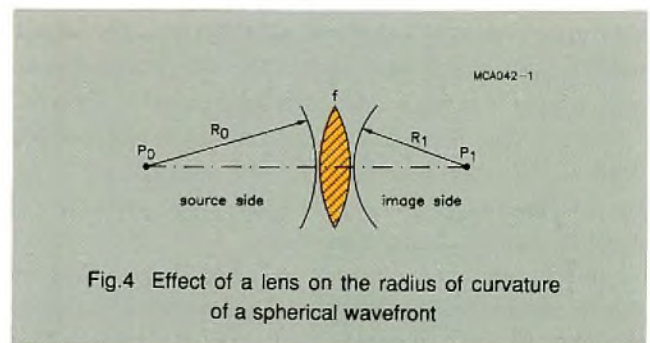


Fig.4 Effect of a lens on the radius of curvature of a spherical wavefront

The lens will also affect the amplitude of the light vector along the beam. The amplitude distribution of the light vector near the image point P_1 can be represented by the Fourier transform of the amplitude distribution in the exit pupil of the lens. For a spherical wavefront in this exit pupil, two specific amplitude distributions deserve special attention:

- homogeneous amplitude distribution leading to the so-called "Airy" spot P_1
- Gaussian amplitude distribution leading to a Gaussian amplitude along the image space.

Both distributions are possible depending on the numerical aperture (NA_1) of the lens (see Fig.5). A small NA_1 leads to beam truncation resulting in an Airy-like profile (see Fig.6), while a large NA_1 leads to a Gaussian-like distribution in P_1 . Two parameters are used to define the spot profile: the e^{-2} width – the width at intensity greater than $e^{-2} \times$ the intensity at the centre; and the full-width-half-maximum (FWHM) value – the width at intensity greater than half the maximum intensity value. Table 1 summarizes the equations determining the spot diameter and the focus depth of both intensity profiles.

Table 1

	Gauss	Airy
Spot diameter	ϕ	$1.22 \lambda/NA_1$
e^{-2} width/FWHM	1.7	≈ 1.6
Depth of focus*	$\approx 0.625\phi$	$\approx \lambda/2(NA_1)^2$

* Definition: 20% drop in intensity

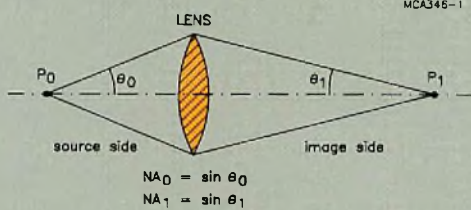


Fig.5 Numerical aperture (NA) for focusing a diode laser beam

Whereas the Gaussian distribution remains Gaussian all along the z-axis, the Airy distribution is only maintained near the image point P_1 . The change in this profile near P_1 is described by the Lommel functions (see Ref.1).

During the evaluation, the intensity profile of the focused laser diode beam is measured along two perpendicular axes and the e^{-2} width is found.

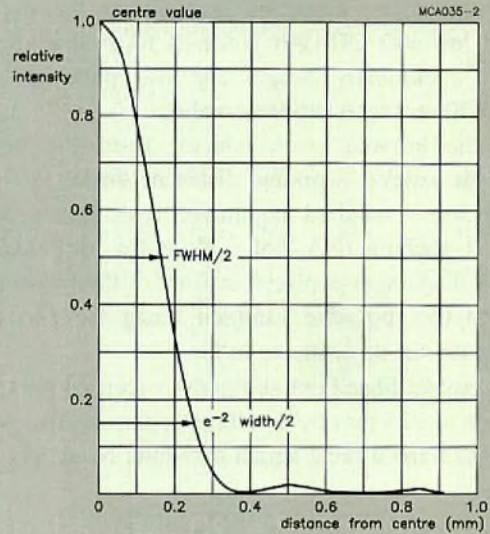
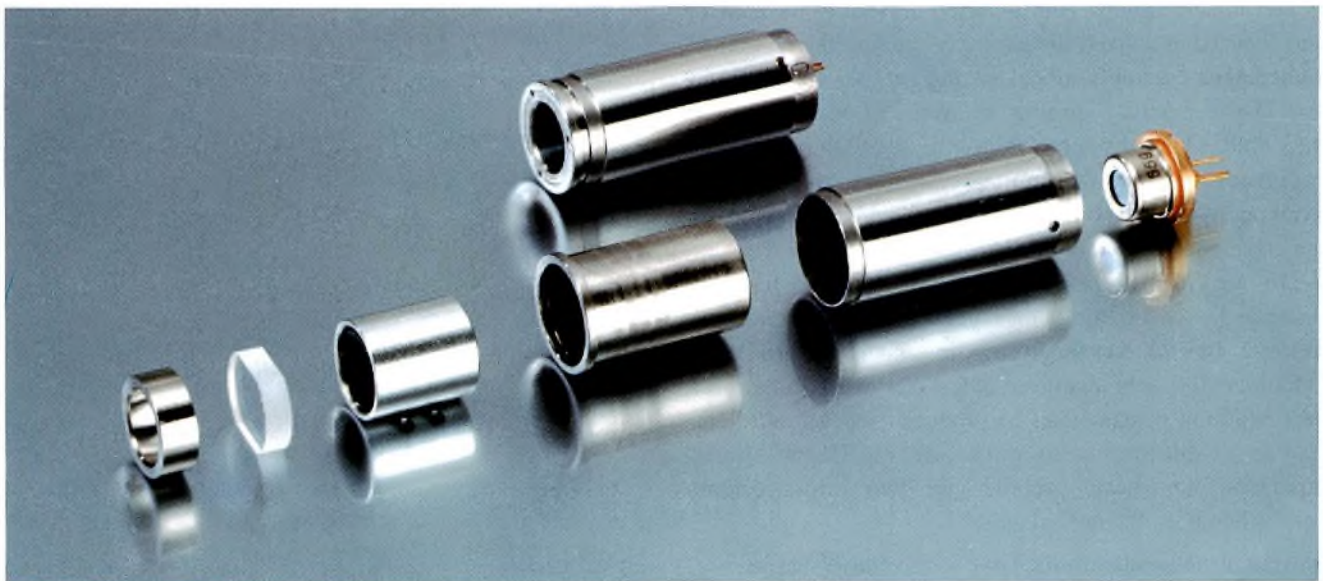


Fig.6 Typical Airy profile of a focused beam



The laser collimator pen assembly

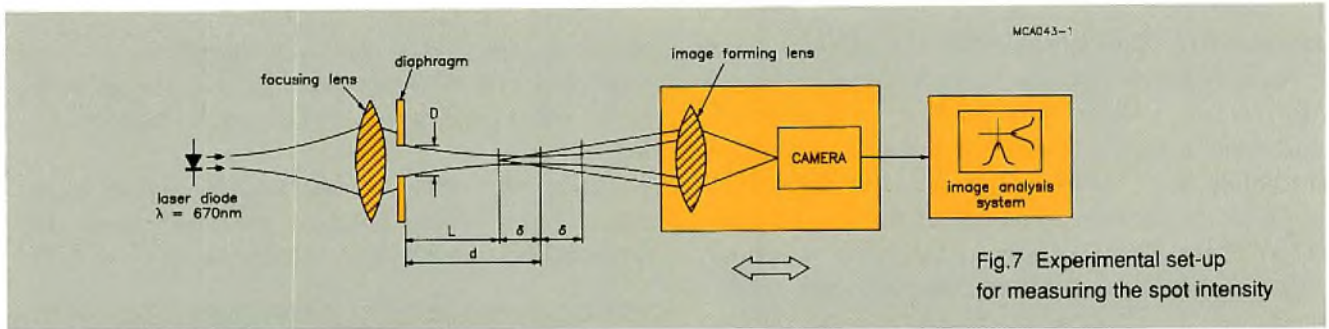


Fig.7 Experimental set-up for measuring the spot intensity

EXPERIMENTAL SET-UP

In this evaluation, emphasis is given to the use of a standard low-cost CD-laser diode as focused source (our CQL21). Preliminary results are also published for a visible (670 nm) laser diode assembly.

For the infrared semiconductor laser, the beam is focused at several working distances from 180 up to 600 mm by a standard collimator lens system with a numerical aperture (NA_0) of 0.25 and a focal length of 9 mm. A diaphragm is placed in front of the focusing lens to reduce the spot size variation along the z-axis. The experimental set-up is shown in Fig.7.

The visible diode laser assembly is focused typically at a distance of 225 mm by a collimator lens system with an NA_0 of 0.25 and a focal length of 9 mm. No diaphragm is used.

Intensity distribution measurement

The intensity distribution of the focused spot is measured by a camera linked to a special electronic image system for analog-to-digital conversion of the image. The stored "picture" of the focused spot is analyzed by a computer.

An image-forming lens is placed in front of the camera and focused at a fixed distance. By moving the combined camera/lens assembly along the optical axis of the laser, the beam intensity profile at various points can be measured. The distance from the exit pupil of the collimator lens (in the case of the infrared diode, the diaphragm) to the point in the beam being measured by the camera/lens assembly is L.

By varying L from a point in front of the focusing distance ($d - \delta$ in Fig.2) to a point beyond the working distance ($d + \delta$) and analyzing the intensity profile to determine the spot diameter (ϕ), a series of curves for each working distance can be produced. As a laser diode has an asymmetric beam waist (see Fig.3), the system measures the beam profile in two cross-sections perpendicular to the optical axis:

- in a plane parallel to the laser's active layer ($\phi_{||}$)
- in a plane perpendicular to the active layer (ϕ_{\perp}).

Typical examples of the measured profiles are given in Fig.8(a) for the infrared semiconductor laser, and Fig.8(b) for the visible semiconductor laser.

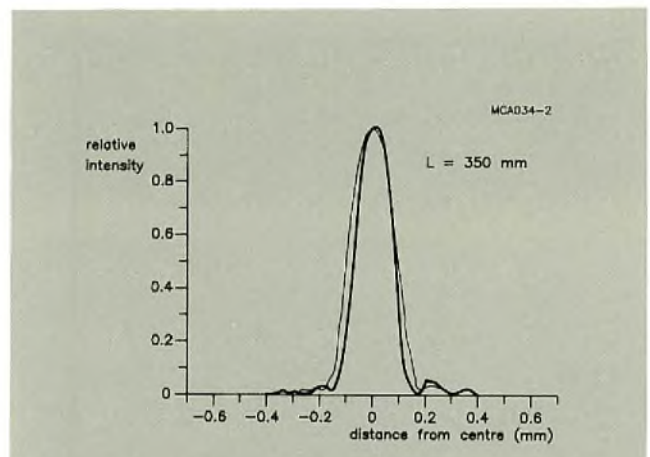


Fig.8(a) An example of a measured intensity profile for an infrared spot focused at working distance $d = 350$ mm, and measured at $L = 350$ mm. The thicker line is the profile in the plane perpendicular to the pn junction

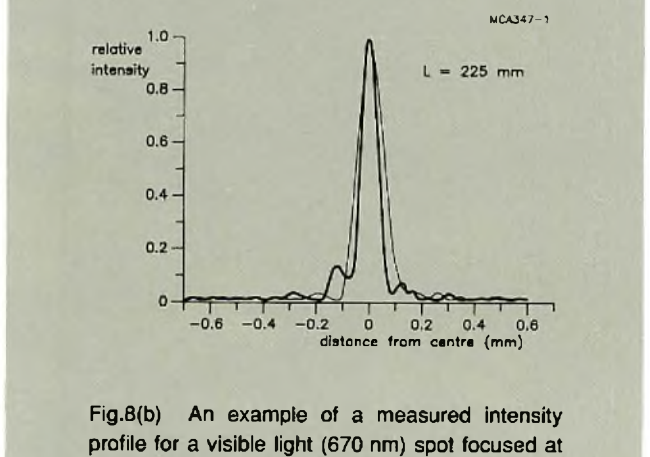


Fig.8(b) An example of a measured intensity profile for a visible light (670 nm) spot focused at working distance $d = 225$ mm, and measured at $L = 225$ mm. The thicker line is the profile in the plane perpendicular to the pn junction

Analysis of the results

Figures 9 and 10 show the spot diameter, ϕ , for the infrared semiconductor diode/focusing system at different focusing distances with two different diaphragms ($D = 1.5$ mm and $D = 2.0$ mm respectively). Indicated are the e^{-2} widths. The corresponding theoretical values of the Airy profiles (solid lines) are also shown on these graphs.

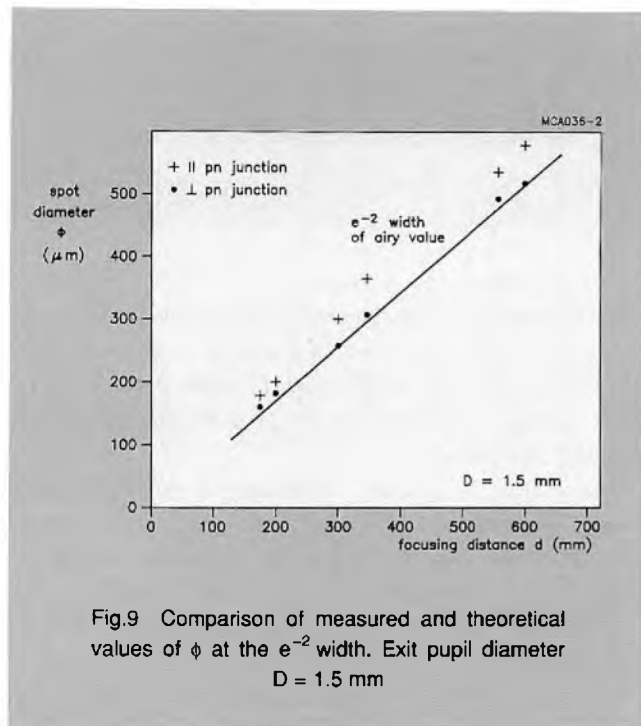


Fig.9 Comparison of measured and theoretical values of ϕ at the e^{-2} width. Exit pupil diameter $D = 1.5$ mm

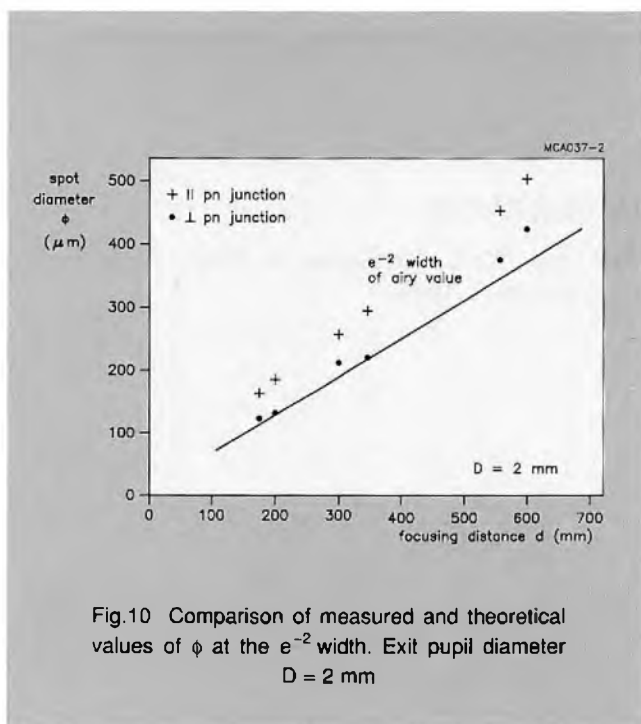


Fig.10 Comparison of measured and theoretical values of ϕ at the e^{-2} width. Exit pupil diameter $D = 2$ mm

For the exit pupil diameter $D = 2$ mm, the theoretical values of ϕ differ from the measured results in the plane parallel to the pn junction (by as much as 26%). This can be attributed to the relatively low emission angle of the laser in this plane (approximately 8° FWHM). Such an angle does not totally fill the exit pupil resulting in a lower effective diameter. For $D = 1.5$ mm, the measured results of ϕ in the parallel plane are closer to the theoretical values (within less than 12%).

In the plane perpendicular to the pn junction, the experimental values match the theoretical spot diameters. The far field angle of the laser diode in this plane is approximately 30° , and therefore the exit pupils for both $D = 1.5$ mm and $D = 2$ mm are completely filled.

Working depth

Based on initial customer indications of optimal working depths, focusing distances (d) of 180, 350 and 550 mm are analyzed in detail, and the working depth of the infrared semiconductor focusing system with $D = 1.5$ mm is taken as an example. The results are presented in Figs. 11, 12 and 13.

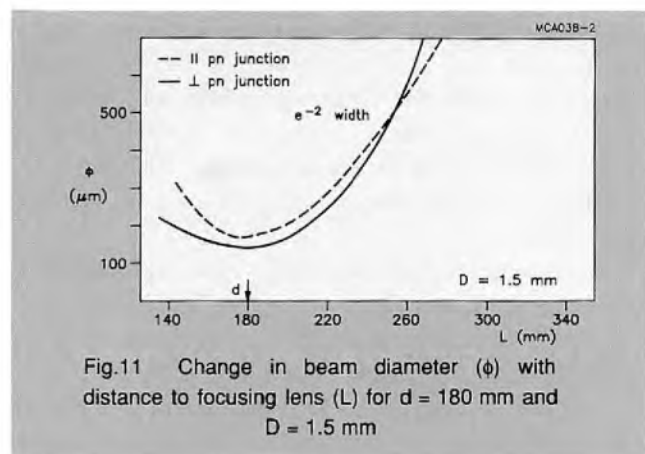


Fig.11 Change in beam diameter (ϕ) with distance to focusing lens (L) for $d = 180$ mm and $D = 1.5$ mm

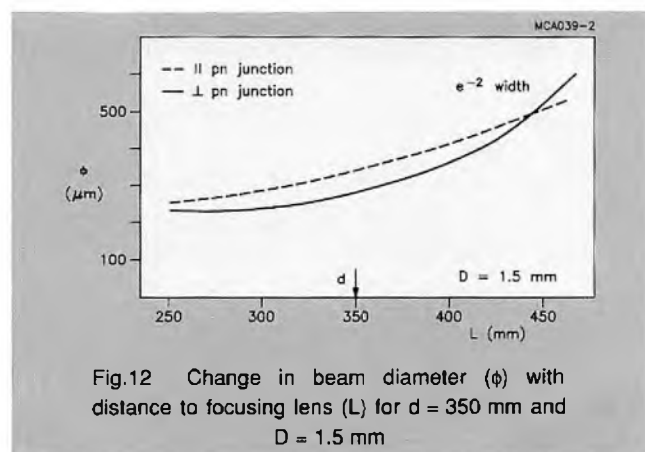


Fig.12 Change in beam diameter (ϕ) with distance to focusing lens (L) for $d = 350$ mm and $D = 1.5$ mm

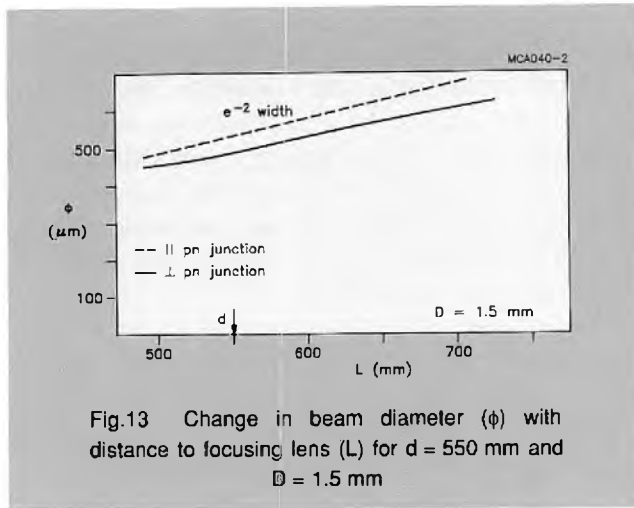


Fig.13 Change in beam diameter (ϕ) with distance to focusing lens (L) for $d = 550$ mm and $D = 1.5$ mm

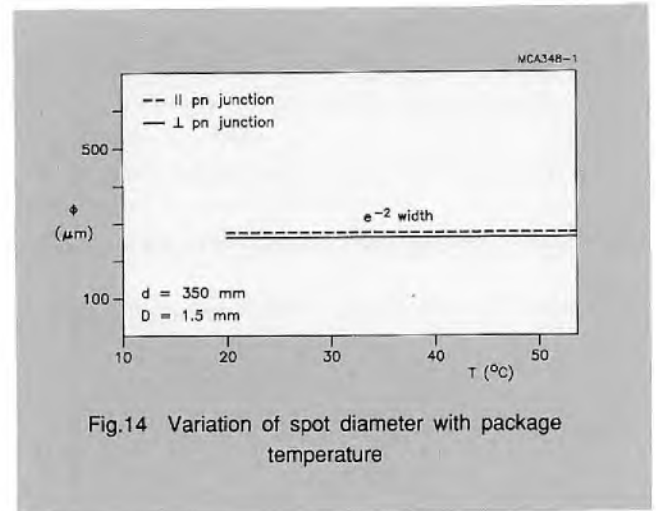


Fig.14 Variation of spot diameter with package temperature

The up-swings of the spot size around the focusing distance in Fig.11 ($d = 180$ mm) are a result of Fresnel diffraction. This diffraction mechanism causes wide variation of the intensity profiles along the optical axis. For focusing distances greater than 350 mm, these variations are much less pronounced (Figs 12 and 13).

CONCLUSIONS

With both infrared and visible semiconductor laser diodes, the focusing pen lens assembly has shown that it's eminently suitable for obtaining various spot diameters (whilst staying within acceptable limits) over a considerable variation in focusing distance. This makes the collimator focusing concept ideal for barcode scanning applications.

Semiconductor diode technology allows for production of a small and extremely rugged assembly, with both laser and lens in the same package. And by using thermally matched materials (stainless steel and glass), excellent temperature stability of the focusing system is achieved. This is also a key consideration in applications such as laser printers. Figure 14 shows the variation in spot diameter as a function of package temperature.

Semiconductor lasers are also very reliable. Experience with infrared lasers in consumer applications has indicated a life-expectancy of more than a million hours. And unlike He-Ne lasers, semiconductor laser diodes don't require a high voltage supply, and so are ideal for battery-powered portable equipment.

Low cost is another advantage of collimated laser diodes. Not only the lower initial cost of the device itself, but also the savings made in assembly (combined laser/lens, no extra optics, no special power supply) and in replacement costs (a much longer mean-time between failures).

It's also relatively easy to modulate a laser diode output (chopping) and tune the receiver amplifier to the chopping frequency to discriminate against excessive background light. This is difficult with He-Ne lasers.

REFERENCE

Born and Wolf, "Principles of Optics", 6th edition, Pergamon Press (1980).

Innovations in oscilloscope tubes

PAUL AERSSENS and KLAUS ZEPPENFELD

Oscilloscope tubes for bandwidths of more than 25 MHz use the technique of post-deflection-acceleration (PDA) to achieve optimum deflection sensitivity and screen brightness. The PDA technique combines high deflection sensitivity at low potential (2 kV) with the brightness provided by a high (16 kV) final screen voltage. The high voltage field is applied between the tube envelope (which has an internal conductive coating) and a mesh electrode. The mesh electrode is located concentrically within the tube envelope at the output end of the gun, between the deflection plates and screen. The beam is deflected in the conventional way by electrostatic plates.

Nowadays, PDA tubes use an aspheric (domed) mesh electrode system, which has the benefit (over previous flat-mesh systems) of a much greater scan magnification, brought about by the divergent lens effect. This allows the primary deflection angle between the deflection plates to be reduced, resulting in fewer deflection errors such as edge defocusing. In addition, the tube can be shortened, which is essential for small spot size, high writing speed and low plate capacitance (plate capacitance determines the bandwidth of the drive amplifiers).

This article discusses Philips' latest range of domed-mesh PDA tubes, the D14-370 family, which has been

perfected by continuous innovation and development over many years. Here are some of the major features of these tubes:

- optimized gun layout – resulting in a low-cost tube with a performance close to the theoretical limits
- frit-sealed tube envelope – providing the best glass tolerances available to allow all parts to be precisely aligned. This is of particular importance for PDA tubes where the alignment between the mesh electrode and the surrounding glass bulb is critical
- internal magnetic correction (IMC) – originally developed for Philips colour picture tubes, IMC enables us to manipulate the beam by superimposing a range of multipole fields at different locations inside the gun. This has two major benefits: firstly, by directing the beam exactly midway between the plates, it allows the plates to be closer together for improved sensitivity; secondly, IMC can be used to correct a number of imperfections in picture quality which in the past had to be corrected by external circuitry or could not be corrected at all.

GUN LAYOUT OPTIMIZATION

To make further advancements in oscilloscope tube performance, we went back to the basic principles of operation and used computer-aided-design (CAD) techniques to find the optimum design. A program was developed to determine the gun layout (Fig.1) for the highest performance, P (also known as the figure of merit) defined as the product of the X and Y sensitivities and line brightness. For our optimization procedure, P was more precisely defined as:

$$P = \frac{I}{D_x} \times \frac{J}{D_y} \times \frac{I_{beam}}{spot\ size}$$

where D_x and D_y are the X and Y deflection coefficients and I_{beam} is the beam current. The deflection coefficients were calculated by an automatic plate design program which set $D_x = 2D_y$, a usual side condition for oscilloscope tubes. The spot size as a function of beam current was determined by beam simulation with a focusing routine. $I_{beam}/spot\ size$ is a measure of line brightness and writing speed.

Thanks to magnetic correction facilities, standard safety margins for production tolerances resulting in beam off-centricity could be disregarded. This enabled the distance between the plates to be minimized for the best possible sensitivity.

Gun layout was optimized for a domed-mesh PDA tube with a post-magnification factor (m) of 4.5: the magnification by which the first focus plane, close to the mesh, is imaged onto the screen by the mesh lens. Note: a value of 4.5 is the maximum achievable by current mesh technology.

The program model included two important factors:

- cathode loading – significant for spot size mainly at low beam current
- space charge repulsion – the limiting factor for writing speed at high beam current.

Performance was calculated for deflection plates of different lengths and for different beam diameters. The results indicated that the sensitivity advantage of long deflection plates is balanced by the increased energy required to deflect the beam, due to the increased plate capacitance. The minimum length is set by the increase in angle of flare required to obtain sufficient scan. If the flare is too great then the effective plate distance is increased and sensitivity is reduced. For a domed-mesh tube, the required scan is small due to the high value of m. This implies that the optimum gun layout is short allowing a small spot and fast writing speed.

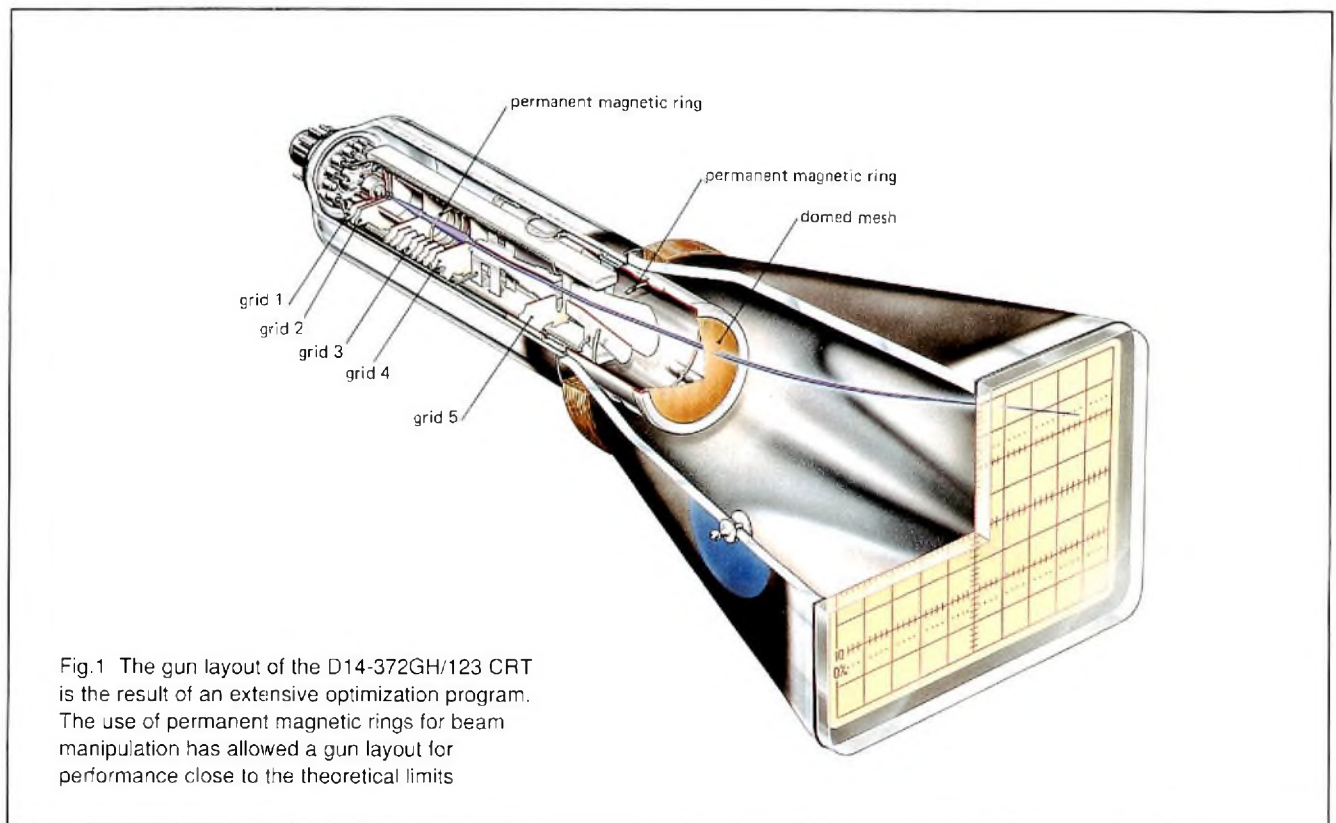


Fig.1 The gun layout of the D14-372GH/123 CRT is the result of an extensive optimization program. The use of permanent magnetic rings for beam manipulation has allowed a gun layout for performance close to the theoretical limits

This optimum layout is also independent of the gun voltage and has allowed the development of a standard gun for which the compromise between sensitivity and writing speed is determined by selecting the appropriate gun voltage rather than by using guns of different length. This is of great benefit to oscilloscope manufacturers as it facilitates standardization of the assembly line and greater product versatility.

What's more, space charge repulsion is insignificant in the high voltage region which means that, for a given value of m , the bulb length has negligible effect on performance. This has allowed the V-shaped bulb from the D14-360 mono-accelerator series to be used for the D14-370 PDA series without compromising performance.

ENVELOPE

To get the best possible alignment of glass parts, we applied the technique of frit sealing for envelope manufacture. The technique uses particles of crystallizing glass with a low melting point, to bond together the neck, cone and faceplate. This is done in a single heat treatment process at a temperature low enough not to affect the dimensional tolerances of the glass parts.

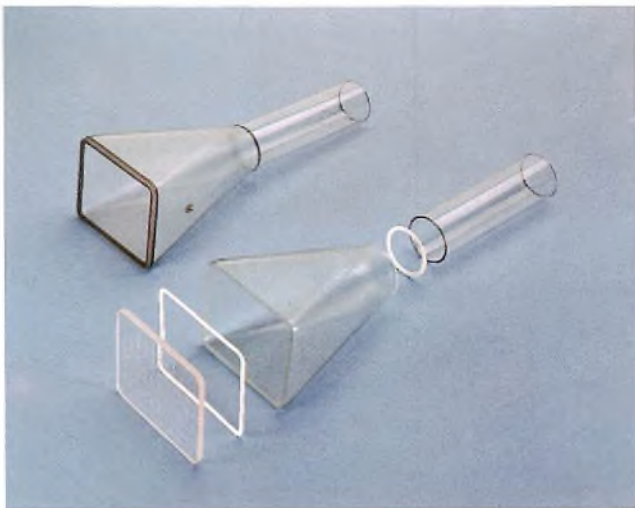


Fig.2 The tube envelope comprises three parts bonded together using frit seals

The resulting tube (Fig.2) has a smooth profile which facilitates mounting. An additional advantage is that the edges of the faceplate are not distorted by the frit seal allowing easy side illumination of the internal graticule.

INTERNAL MAGNETIC CORRECTION

Permanent magnetic rings

Internal magnetic correction (IMC) uses permanent magnetic rings to manipulate the beam. It can be used to reduce distortion in a CRT for the lifetime of the tube. First developed for static convergence correction in our colour TV tubes, permanent magnetic rings consist of thin wires of semi-hard magnetic material (Fig.3) located around the beam axis inside the tube. They are magnetized with several superimposed field configurations from outside the tube during the final test procedure. Experience gained in the television colour picture tube industry has shown that the magnetization withstands all conditions of operation and storage.

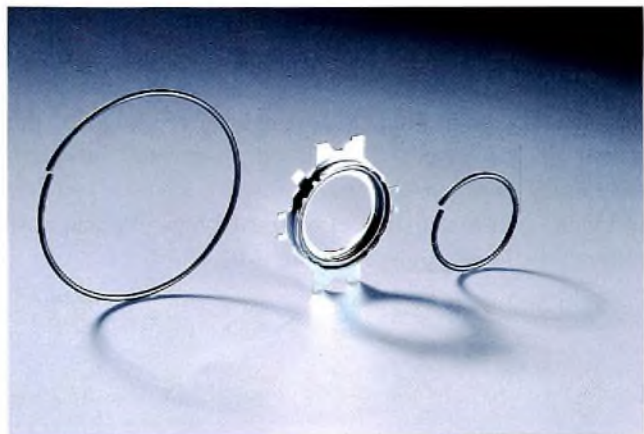


Fig.3 Permanent magnetic rings are made from semi-hard magnetic material. Grid 3 is shown with the ring mounted

Philips has long used permanent magnetic rings in oscilloscope tubes for spot shape and vertical line correction. Generally, two such rings are used:

- The first, located near the focus lens at grid 3, produces two dipole fields to improve brightness uniformity, and two quadrupole fields for astigmatism correction
- The second ring, between the X and Y deflection plates at grid 5, superimposes four different field configurations. Two dipole fields centre the beam. A quadrupole field, with poles diagonal to the X and Y axes, magnifies the vertical scan to increase sensitivity and improve calibration. A second quadrupole field, in line with the X and Y axes, rotates the vertical scan to optimize orthogonality (Fig.4(a)).

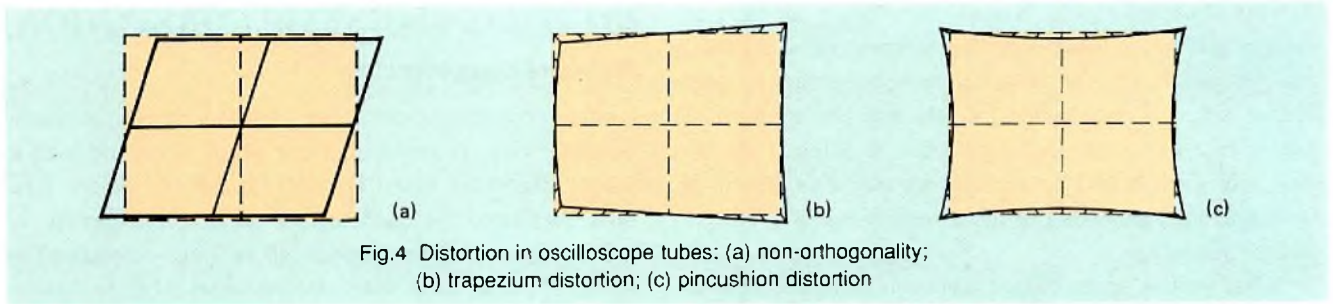


Fig.4 Distortion in oscilloscope tubes: (a) non-orthogonality; (b) trapezium distortion; (c) pincushion distortion

An additional ring for geometry correction

In PDA tubes, the alignment of the domed-mesh relative to the surrounding glass bulb is critical as any deviation from rotational symmetry will lead to geometry distortion of the final picture on the screen. In particular, tilting or eccentricity will result in trapezium or keystone distortion (Fig.4(b)), i.e. non-parallel horizontal or vertical lines displayed at the screen edges. This type of distortion cannot be corrected electrostatically and has been a limiting factor in measurement accuracy.

Geometry distortion can be quantified by measuring the accuracy with which a rectangle at the edge of the screen is displayed. Recent advancements in glass technology have enabled us to display an 80 × 100 mm rectangle with a deviation of only ±0.5 mm. We can now reduce this figure further by using IMC.

To correct trapezium distortion, two six-pole magnetic fields must be superimposed on the electron beam at the output from the deflection plates. This is done by means of a new larger magnetic ring clamped inside the cylindrical shield supporting the domed-mesh. Analysis has shown that a ring at this position can also take over the same functions as the ring formally at grid 5, when superimposed with similar fields.

Adding an octupole field to the new ring corrects pincushion/barrel distortion (Fig.4(c)). This obviates the need for an electrostatic geometry control electrode. Figure 5 summarizes the magnetic fields used in our latest range of PDA tubes.

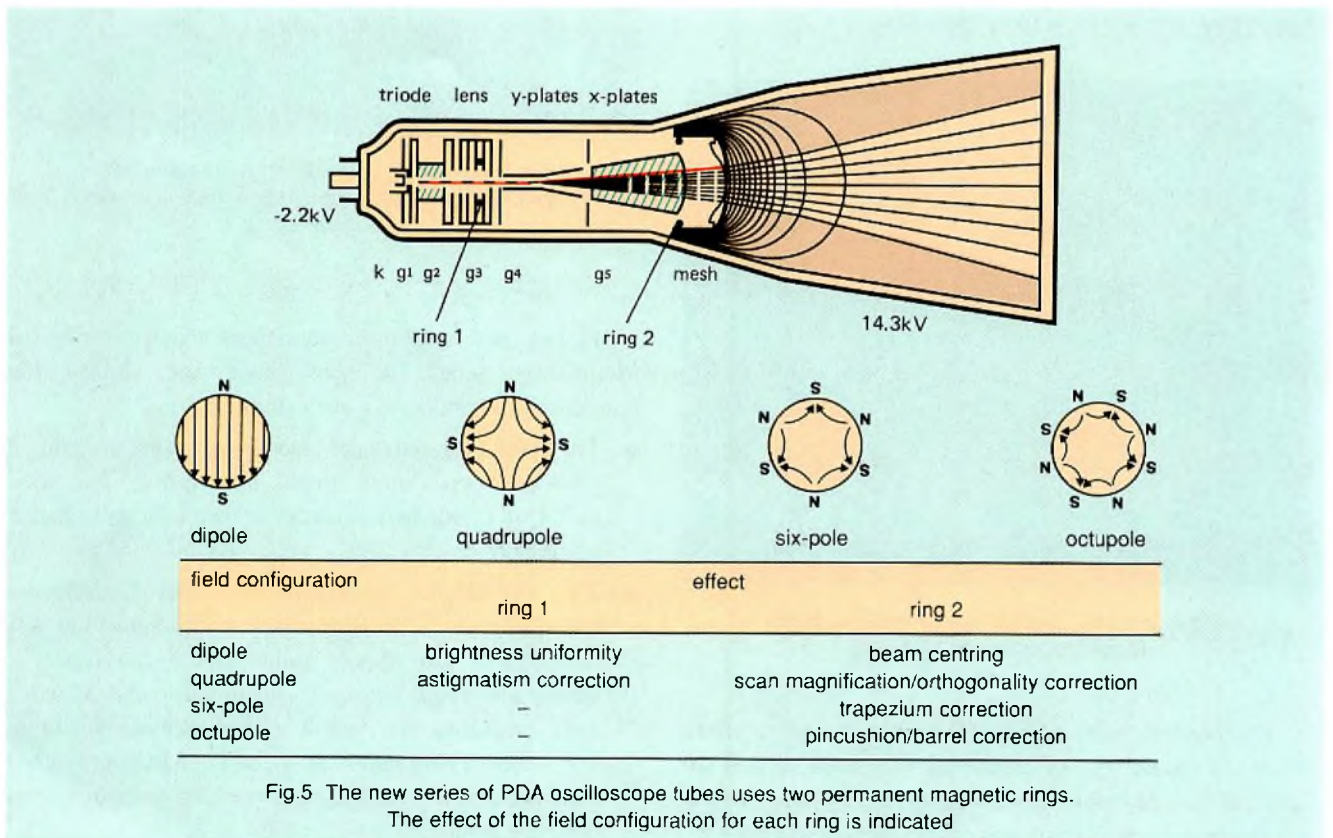


Fig.5 The new series of PDA oscilloscope tubes uses two permanent magnetic rings. The effect of the field configuration for each ring is indicated

SUMMARY

PDA tubes using a domed-mesh electrode have high sensitivity, increased brightness and low edge-defocusing. With the application of magnetic rings, the effects of tolerances on tube components have been eliminated, allowing the development of higher quality tubes which need fewer adjustments.

The use of CAD facilities has shown that the optimum oscilloscope tube has a short gun layout which implies a low deflector capacitance and short transit time, allowing the operational bandwidth to be increased. All these developments are embodied in our D14-372 which has a bandwidth of more than 100 MHz without side contacts. The side contact version D14-382 can operate at 200 MHz or more.

New chip-set reduces power consumption of radio pagers

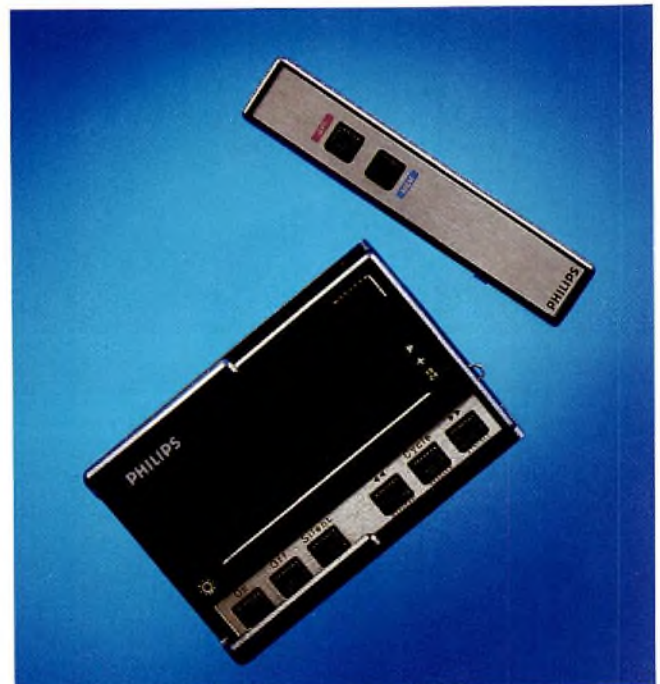
S. DRUDE and T. RUDOLPH

Radio paging systems are a fast-growing part of the telecommunications market since they offer a low-cost, fast-contact medium for people on the move. At present, paging systems are divided into two main groups. The oldest group are the short-range, on-site private systems used in hospitals and industrial plants to provide emergency contact with medical and maintenance staff. This group mostly incorporate a 'talk-back' facility which makes them more expensive than the newest group: wide-area, public paging systems.

This group of public paging systems are used to cover cities and counties. Eventually, it is proposed to link up the individual systems to provide global paging facilities via satellite. These public, wide-area paging systems do not offer a 'talk-back' facility in contrast with private paging systems, and therefore make very efficient use of the frequency spectrum. The infra-structure is simple because existing broadcasting stations can be used as base stations to cover a wide area, and a low-cost VHF or UHF battery-driven radio receiver can be used for the pocket receiver.

The user of these wide-area paging systems can select from two types of pocket receiver. The first type is the very simple 'beep-only' receiver to inform the user that someone wants to contact him or her. He or she then simply uses the nearest telephone to dial the pre-arranged telephone number. The second type is the display pager which offers the user a wide range of facilities. Firstly, it can display the telephone number he has to call and secondly, it can store telephone numbers so that, if the user is otherwise occupied, he can make the call when

it's convenient. The introduction of an alphanumeric display provides the user with the facility to receive and/or store complete messages. This latter facility gives the user a host of new options to enhance the value of the paging system, e.g. stock-market information, current gold price, sports results, and the latest news and weather information, all of which can be transmitted via the paging system. These interesting developments ensure that radio paging has an important role to play in the future of the telecommunications industry.



At present, three major system standards exist for wide-area paging systems:

- POCSAG (Post Office Code Standardization Advisory Group)
- RDS (Radio Data Systems)
- Golay (an earlier Motorola paging system).

POCSAG (also known as CCIR Radiopaging Code No.1) is becoming more and more accepted as the standard for city and nationwide paging systems, while RDS is being used to transmit broadcast information in Europe for future radio receivers.

Wide-area paging receivers must consume as little power as possible since they are battery-operated and inconvenient to recharge. Other important requirements are a high RF input sensitivity of the paging receiver, as it has to operate at long distances from the base station, and the provision of sufficient call/message storage and display capacity.

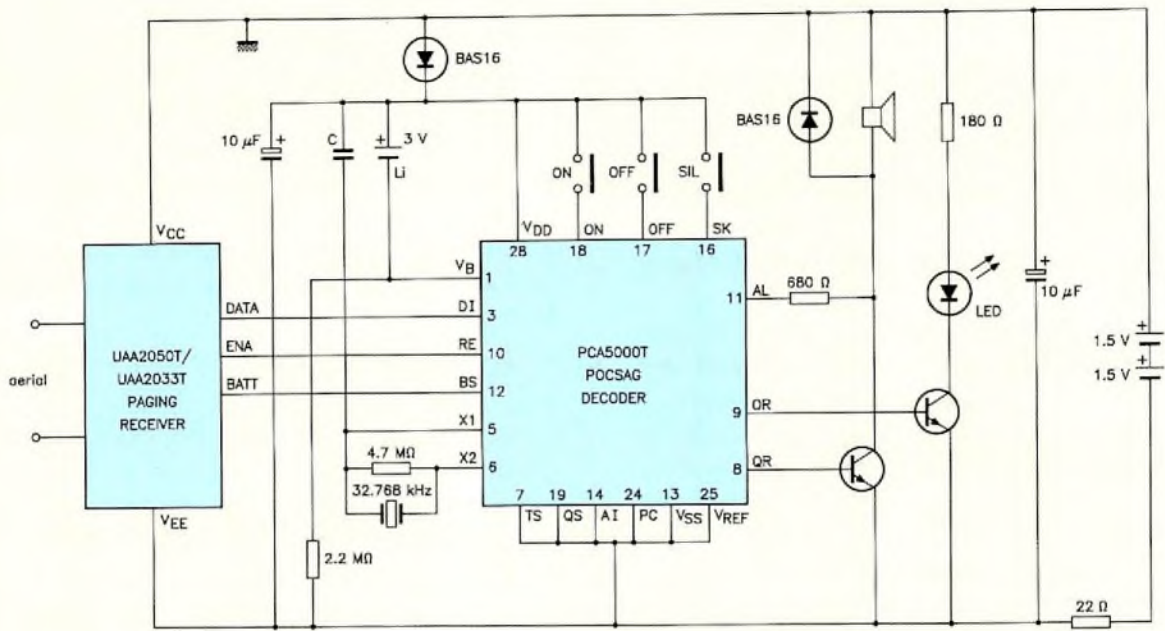
Philips has introduced three new ICs for POCSAG paging receivers; the bipolar UAA2050T low power digital UHF paging receiver, the VHF bipolar UAA2033T low power digital paging receiver and the CMOS PCA5000T paging decoder as shown in Fig.1. The UAA2050T and UAA2033T paging receivers are also compatible with the Golay standard, only an external filter has to be modified. These ICs have the following features:

- low DC supply voltages, between 1.9 and 3.5 V for the paging receiver UAA2050T (UAA2033T) and between 1.7 and 6.0 V for the paging decoder PCA5000T
- extremely low paging receiver current consumption, achieved by switching on the UAA2050T (UAA2033T) under the control of the PCA5000T for the minimum time during the data search phase and, when receiving data, to have a total duty factor of 4 in 17; this reduces the total system operating current to about 500 μ A
- in a display pager the PCA5000T also controls the 'sleep/active' period of the microcontroller; so the additional power consumed by the microcontroller is kept to a minimum
- the UAA2050T operates over a wide frequency range of 30 to 470 MHz with a typical input sensitivity of 0.17 μ V (EMF/2); frequency stability is provided by AFC with a capture range of 3 kHz (spurious signal rejection is >55 dB for a paging system with a channel spacing of 25 kHz)
- the UAA2033T operates over a frequency range of 30 to 174 MHz with a typical input sensitivity of 0.21 μ V, (EMF/2); frequency stability is provided by

AFC with a capture range of 4 kHz (spurious signal rejection is >55 dB for a paging system with a channel spacing of 25 kHz)

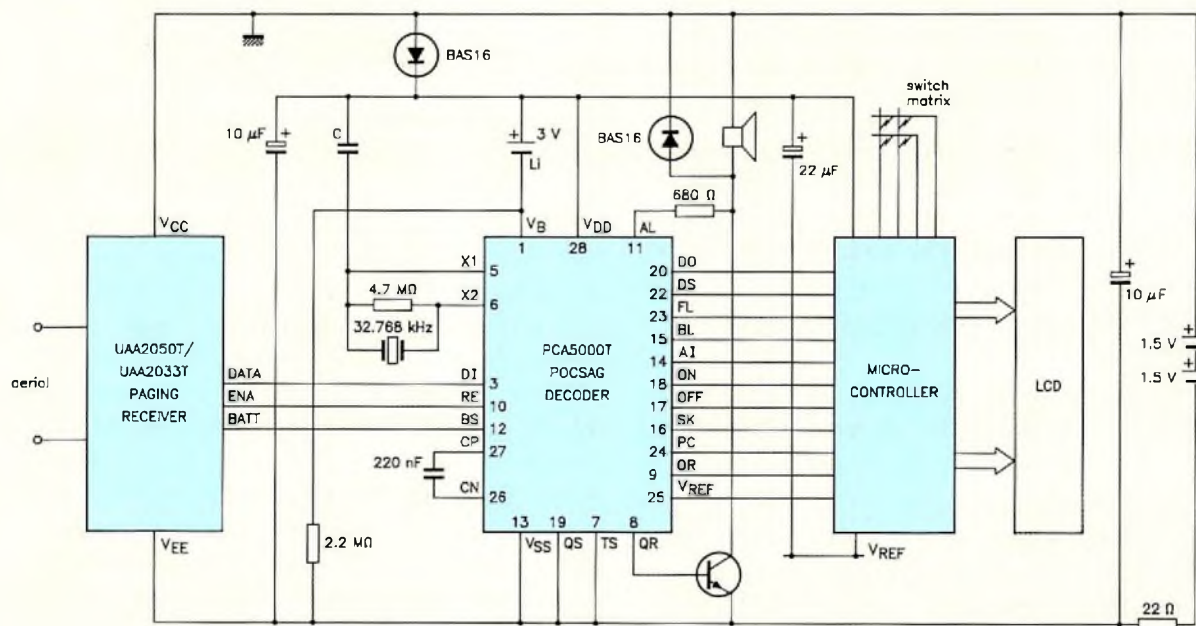
- the PCA5000T provides storage for two Receiver Identification Codes (RICs) so that the user can be paged under two different addresses (e.g. personal call or group call)
- the POCSAG codewords are checked by the PCA5000T for errors using a powerful polynomial error detection algorithm and the codeword errors are corrected using 4-bit burst or random distribution algorithms.
- the PCA5000T also provides a 16.384 kHz square-wave output (derived from the external 32.768 kHz oscillator) to provide timer/clock facilities; these activate the microcontroller to scan the keypad and update the time at regular intervals (using the event counter/interrupt system of the microcontroller)
- the PCA5000T incorporates an integrated voltage doubler circuit which allows the microcontroller and liquid-crystal display to be driven by an increased supply voltage
- when used together in a 'beep-only' pager, these ICs support a system call rate of 15 calls/s. When used together with a microcontroller in a display pager, they provide storage and display facilities for messages that are limited only by the external RAM storage capacity.

A general description of the operation of the two ICs in a POCSAG pager receiver is as follows. The input RF signal to the UAA2050T is a VHF/UHF carrier (30 to 470 MHz) and to the UAA2033T a VHF carrier (30 to 174 MHz) both with a frequency-shift keying modulation of ± 4.5 kHz. The transmitted data consists of an FM signal, with a positive frequency shift for a logic LOW and a negative frequency shift for a logic HIGH, at a bit rate of 512 bits/s. Applications for pager systems using a different frequency deviation and baud rate are possible using other external components. The UAA2050T (UAA2033T) mixes, filters and demodulates the input RF signal to generate unprocessed POCSAG data. The PCA5000T paging decoder periodically scans the data from the UAA2050T (UAA2033T). If a match is detected between the received data address codeword and one of the two user address codewords pre-programmed in the decoder RAM, the paging decoder decodes the subsequent message information. The paging decoder signals that valid information has been received by generating alert cadences and in a display pager, the numeric or alphanumeric data is displayed, on demand.



Beep-only pager application

MCA670



Display pager application

MCA659

Fig.1 UAA2050T (UAA2033T) and PCA5000T: the heart of POCSAG pagers

UAA2050T LOW POWER DIGITAL UHF PAGING RECEIVER

The UAA2050T is a very low power UHF (30 MHz to 470 MHz) paging receiver used in long-range digital paging systems which employ direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation, see Fig.2. The UAA2050T design is based on the offset receiver principle which provides better performance, decreases the power consumption and reduces the number of external components. The offset receiver mixes the received FM signal with a multiple of the local oscillator output to give a mixer output frequency equal to the frequency deviation \pm the frequency offset between the FM signal carrier and the local oscillator harmonic. The UAA2050T output is a fully-filtered and squared data pulse train intended to supply, for example, the PCA5000T paging decoder. The UAA2050T power consumption is controlled externally from the PCA5000T, using the scanning frequency of the POCSAG code format.

The RF signal from the antenna input (pins 19 and 20) is amplified by a preamplifier and then fed to the balanced mixer, see Fig.3, where the RF signal is mixed with the output from the quintupler. The local oscillator fifth harmonic is trimmed during quintupler alignment (pins 8 and 9) so that there is a 2.25 kHz frequency difference between the quintupler output frequency and FM signal carrier frequency. Therefore $5 \times$ crystal frequency - FM signal carrier frequency = 2.25 kHz.

During operation, when the FM signal carrier is FM modulated using a frequency deviation of ± 4.5 kHz the balanced mixer output is 2.25 kHz or 6.75 kHz, depending upon whether a logic HIGH or a logic LOW is received.

The mixer output is fed through a highly-selective 8 kHz band-pass IF filter consisting of a second order low pass active filter (pins 1 and 2) and a passive elliptic filter (pins 28 to 25) to remove unwanted FM mixing products and to provide channel selectivity. The filtered signal is amplitude-limited; to prevent overloading the limiter-amplifier, offset compensation is applied by the capacitors on pins 21 and 22. The FM signal is demodulated by a DFSK (Direct Frequency Shift Keying) demodulator to provide the 512 bits/s data pulse train and to generate the signal that automatically fine tunes the local oscillator using an AFC feedback loop to track the RF signal input frequency. Demodulation and AFC generation use the phase shift and multiply principle, the capacitor on pin 11 determines the demodulator phase shift characteristics. AFC frequency limits are ± 3 kHz, determined by the capacitors on pins 10 and 3. The raw data pulse train is passed through a low-pass data filter and finally through a limiter-amplifier to generate a logic-level output data pulse train with rise and fall times of less than 50 μ s. The component values shown in Fig.3 assume an FM signal carrier frequency of 469.200 MHz and an oscillator frequency of 93.84045 MHz. With an input sensitivity of 0.17 μ V (EMF/2), the bit error rate is 3 bits in 100. The data output signal is ($V_p - 0.7$) V minimum for a logic HIGH, and +0.5 V maximum for a logic LOW.

The UAA2050T operates from a supply voltage of between 1.9 and 3.5 V. It includes a battery low detector circuit which generates an output when the supply voltage is less than 2.0 V. The UAA2050T is in a SO28 mini-pack.

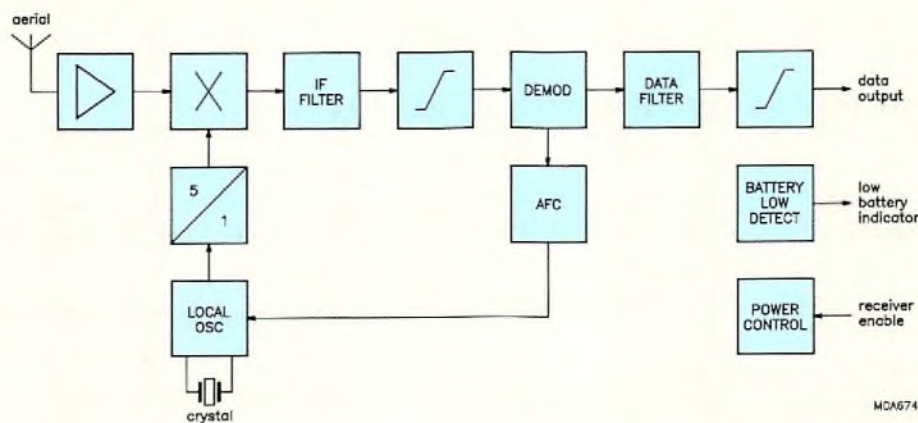


Fig.2 UAA2050T block diagram

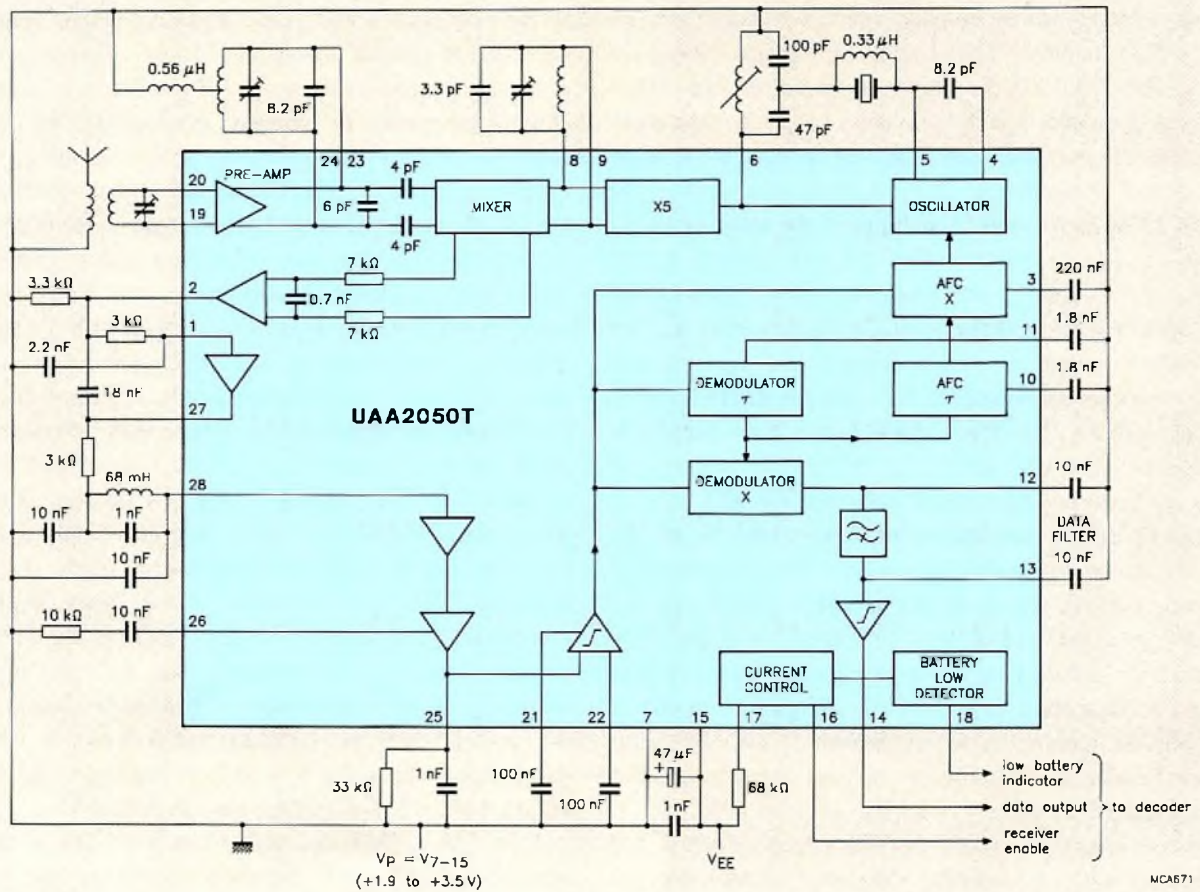


Fig.3 UAA2050T low power digital UHF paging receiver

UAA2033T LOW POWER DIGITAL PAGING RECEIVER

The UAA2033T is a low-cost VHF (30 to 174 MHz) paging receiver also based on the offset receiver principle and operating identically to the UAA2050T, see Figs 4 and 5. The UAA2033T has exactly the same facilities as the UAA2050T; the differences in construction and performance are:

- it doesn't include an integrated preamplifier, but still has a typical input sensitivity of 0.21 μ V (EMF/2) at an FM signal carrier frequency of 173.950 MHz
- it uses an oscillator and a frequency tripler so that the crystal frequency is given by:
 $3 \times \text{crystal frequency} - \text{FM signal carrier frequency} = 2.25 \text{ kHz}$
- the IF filters consist of passive components which are mostly external to the IC with only a few on-chip resistors; the UAA2050T incorporates some complete filters on-chip
- the AFC capture range is $\pm 4 \text{ kHz}$, maximum
- the typical DC supply current is 2.7 mA (for the UAA2050T, typically 3.0 mA)
- the battery low detector circuit generates an output when the supply voltage is less than 2.135 V.

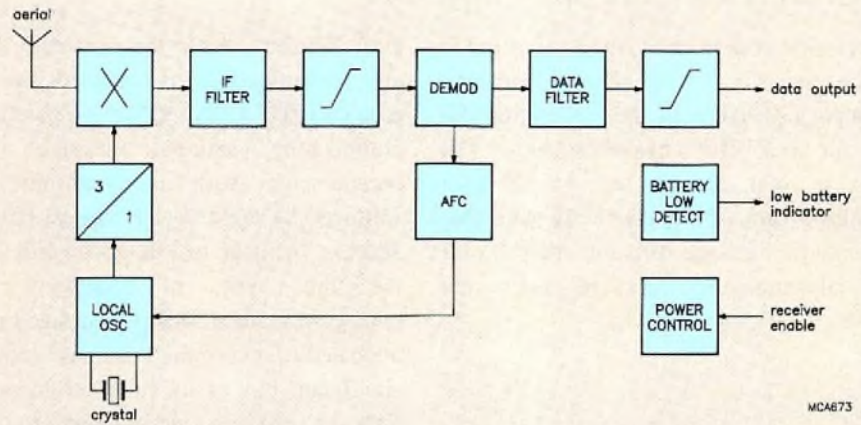


Fig.4 UAA2033T block diagram

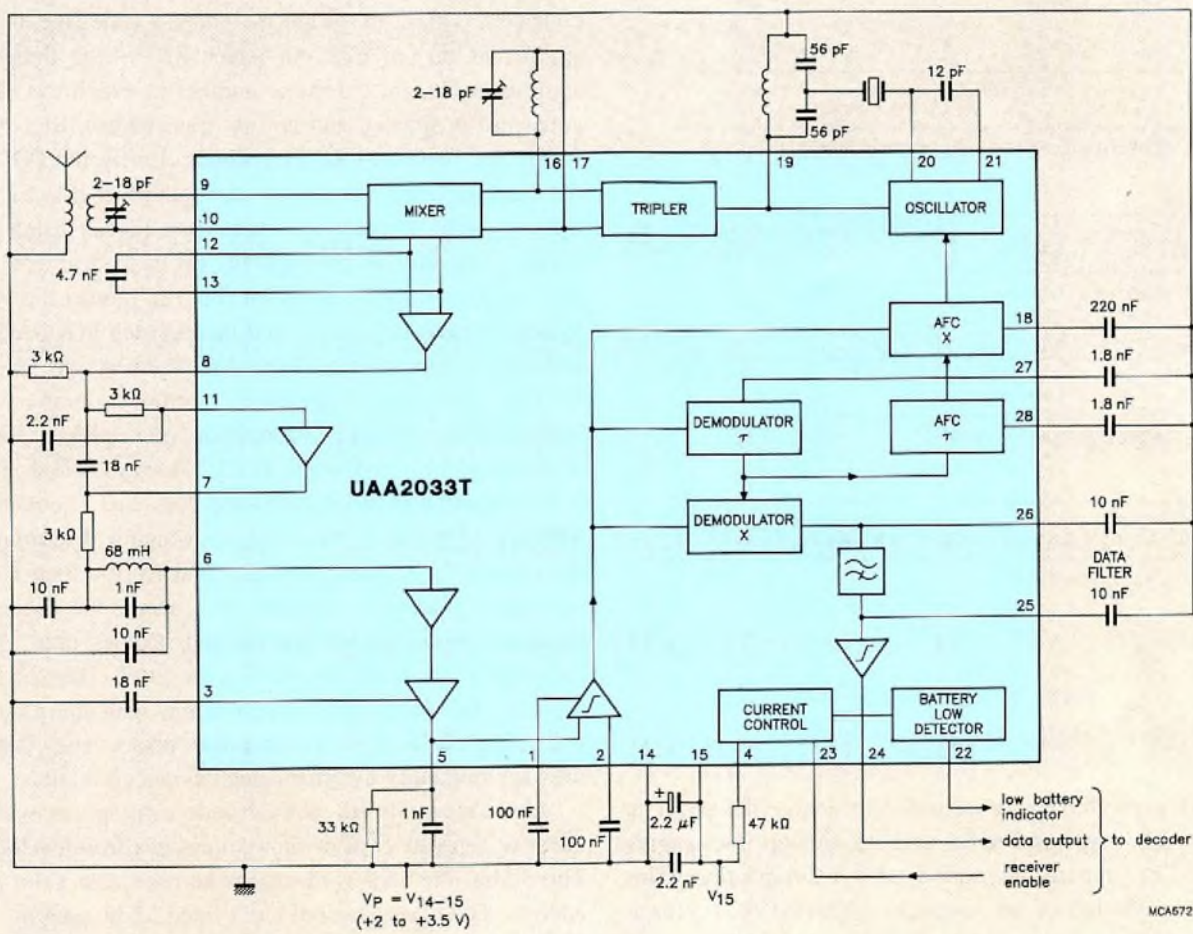


Fig.5 UAA2033T low power digital paging receiver

THE POCSAG CODE TRANSMISSION FORMAT

The POCSAG transmission code format is shown in Fig.6. The data transmission rate is 512 bits/s with an accuracy of 0.001%. The frequency deviation of the transmitted FM signal is ± 4.5 kHz for a 25 kHz channel spacing. The POCSAG code has a total capacity of 2×10^6 user addresses with a calling rate of 15 alert-only calls per second, 5 ten-digit numeric message calls per second, or 2 seventeen-character alphanumeric message calls per second.

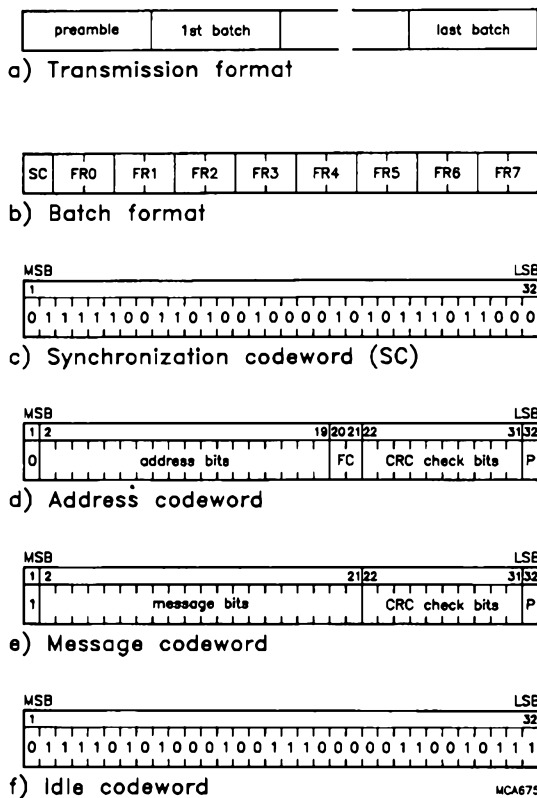


Fig.6 POCSAG code structure

Initially a preamble is transmitted to enable the pager to acquire bit synchronization and to set up the paging decoder to prepare for codeword synchronization. This preamble consists of bit reversals, 1010101010....., for at

least 576 bits. After the preamble, batches of codewords are transmitted as determined by the messages to be transmitted. Each 544-bit batch consists of synchronization, address, message and idle codewords, commencing with a synchronization codeword and followed by eight 64-bit frames. Each frame contains two address, message or idle codewords or any combination of the three types of codeword. The synchronization codeword is the 32-bit code defined in Fig.6. Each pager is allocated to one of the 8 frames according to the three least significant bits of its Receiver Identification Code (RIC). When a pager is programmed to have two RICs, they should have the same frame number since the frame number forms part of the address codeword and scanning two frames increases power consumption.

The address codeword selects a specific pager and classifies the call as tone (beep) only, numeric or alphanumeric. Bit 1 is always a logic LOW, which distinguishes an address codeword from a message codeword. Bits 2 to 19 are the address code (the 18 most significant bits of a 21-bit pager RIC – the three least significant bits are the frame number in which the address codeword is situated and are not transmitted). Bits 20 and 21 are the function bits (FC) which classify the POCSAG data as tone only, numeric or alphanumeric. Bits 22 to 31 are the cyclic redundancy check bits (CRC) using BCH (Bose Chaudhuri Hocquenghem) cyclic codes. The CRC bits, together with the parity bit (bit 32), protect the system against transmission errors and increase the POCSAG data call success rate by error detection and correction.

The message codeword contains numeric or alphanumeric message information and follows directly after the address codeword. Bit 1 is always a logic HIGH to distinguish a message codeword. Bits 2 to 21 contain the message information, the coding of which is determined by the system application. Messages that are too long for one message codeword continue by using the codeword positions in subsequent frames and batches until all the message information has been transmitted. Bits 22 to 31 are the CRC check bits, which again, with the parity bit (bit 32), check for transmission errors and improve message reliability by error detection and correction.

Idle codewords fill unused codeword spaces within a batch or separate two, or more, messages from each other. The 32-bit idle codeword cannot be used as a valid pager address. The idle codeword has a fixed 32-bit pattern.

PCA5000T PAGING DECODER

The PCA5000T is a fully-integrated CMOS, 512 bits/s, POCSAG decoder and page controller for 'beep-only' and display pagers. In the latter, the decoded POCSAG data is transferred over a serial interface to a microcontroller for processing and subsequent storage and display (Fig.1).

The PCA5000T features:

- 16.384 kHz reference clock output signal
- 512 bits/s POCSAG data processing using the Philips ACCESS synchronization algorithm
- 5 × 9-bit address RAM (with extra back-up lithium battery)
- 'beep' tone generator
- supply voltage doubler
- paging receiver and microcontroller scan activation control so that maximum power-down operation minimizes power consumption
- digital receiver data input filter
- serial microcontroller interface
- pushbutton control for 'beep-only' pagers
- Out-Of-Range output.

In both 'beep-only' and display pagers, call alert cadences are generated when a valid call or message is received and the pager is switched on. Status cadences are generated to inform the user of the current state of the pager as a result of user status interrogation. The decoder's 5 × 9-bit static RAM contains the two pre-programmed user addresses and special functions for silent override enable or disable, voltage-doubler enable and error-correction-algorithm selection. A built-in ACCESS algorithm ensures that the POCSAG data can be synchronized even without preamble detection and the pager current consumption is minimized by switching on the paging receiver only when searching for, or receiving POCSAG data. One of two error-correction algorithms is applied to the message codewords to minimize the call/message failure rate. The PCA5000T supply current is typically 15 µA. The IC is available in a SO28 mini-pack.

For both types of pager the internal status of the paging decoder is one of the following:

- OFF state. The paging decoder scans the ON, OFF and SILENT pushbuttons in a 'beep-only' pager and the operator's controls in a display pager, but signals are not decoded and the paging receiver is disabled to conserve power
- ON state. Received calls and messages are checked for validity and, when validity is confirmed, acoustic/message information is output to the beeper/microcontroller
- SILENT state. Operation is the same as the ON state, except that only special silent override calls cause alert cadences to be generated; if the pager is programmed as a 'beep-only' pager, up to four different calls are stored and the alert cadences are generated when the ON state is selected again.

POCSAG data decoding

The PCA5000T input data is passed through a digital low-pass filter, see Fig.7. A pulse sampling clock, in synchronism with the 512 bit/s data rate is generated by the clock recovery circuits from the filtered data to provide a reference for POCSAG data synchronization.

A serial data processor examines the data for validity using the Philips ACCESS algorithm. This is a five-stage algorithm to synchronize the POCSAG data as follows:

Stage 1: This is the power-on stage that's entered by selection of either ON or SILENT states. The paging receiver is switched on, and for up to 3 s scans for a preamble or a synchronization codeword. If a preamble is detected the algorithm enters stage 2 (preamble receive). If a synchronization codeword is detected, the algorithm enters stage 3 (data receive). If neither is detected after 3 s, the algorithm enters stage 5 (carrier off).

Stage 2: This is the preamble receive stage in which the paging decoder checks the POCSAG data bit-by-bit, for the preamble and the synchronization codeword. If a preamble or the synchronization codeword is not detected in 544 bits, the algorithm goes to stage 5. When a synchronization codeword is detected, the paging decoder enters stage 3.

Stage 3: This is the data receive stage in which the paging decoder is ready to accept data and scans the frame defined by its user addresses. The paging receiver is switched on 30 ms before the start of the allocated frame. In total, the pager is switched on for a duty factor of 1 frame in 8 and for the synchronization codeword, a duty factor of 4 in 17.

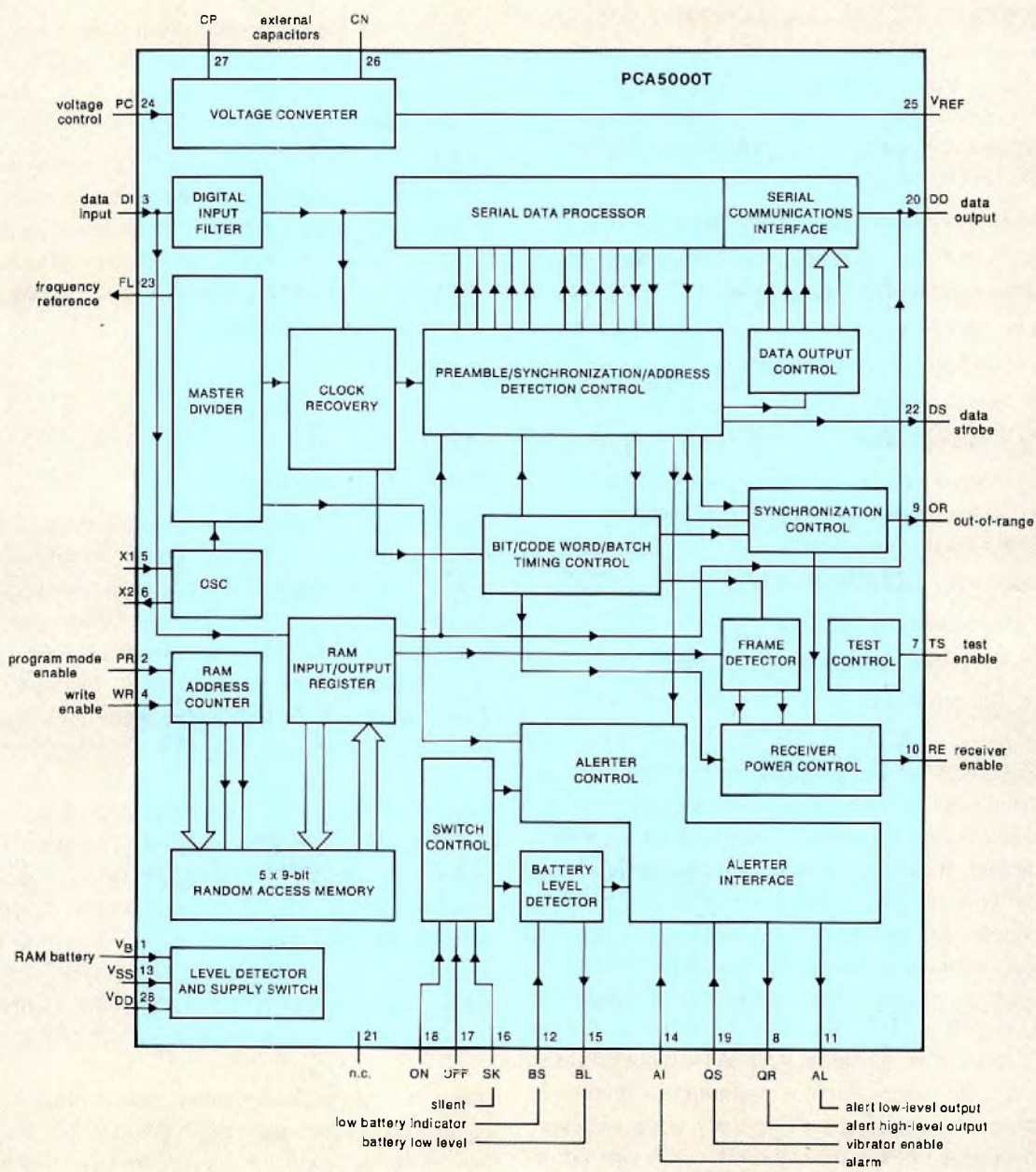


Fig.7 PCA5000T block diagram

Each codeword is now error-corrected as determined by the synchronization reference. When an address codeword is detected, the 18-bit address field is compared with the corresponding address codeword field stored in the paging decoder RAM. If the bits in the two fields are identical, the PCA5000T performs the following:

- stores a command to generate an alert cadence as determined by the function bits in the address codeword; the alert cadence is not generated until the complete message information has been received.

- enables the paging receiver to receive subsequent message codewords until a new address codeword (including idle codewords) is received, or the error correction algorithm fails to generate a valid codeword, or synchronization is lost
- transfers the message codewords belonging to the preceding address codeword to the microcontroller.

If no pre-programmed address is detected, the PCA5000T disables the paging receiver until 30 ms before the start of the synchronization codeword of the next batch. If synchronization is detected, the paging decoder remains in stage 3; if not, the ACCESS algorithm proceeds to stage 4.

Stage 4: This is the fade recovery stage. The PCA5000T continues to test for the synchronization codeword by enlarging the synchronization codeword window by one bit on each side for the next 15 batches in an attempt to regain synchronization. If a synchronization codeword is not detected, the ACCESS algorithm enters stage 5.

Stage 5: This is the carrier off stage. The paging decoder enables the paging receiver for 92 ms in 1125 ms to check if a preamble or synchronization codeword is present. The first 30 ms allow the paging receiver time to stabilize. In the following 62.5 ms, 32 bits of POCSAG data are examined at 576-bit intervals (equivalent to 1125 ms). When a preamble is detected, the ACCESS algorithm enters stage 2, or stage 3 if a synchronization codeword is detected.

Message Data Processing

After a valid address codeword has been detected, the paging decoder scans the next codeword position for a message codeword. If one is detected, the paging decoder receives the message codewords associated with the message until the next address codeword ends the message.

**TABLE 1
Function bits**

RIC	function bits	message type
A	00	numeric
A	01	tone only
A	10	tone only
A	11	alphanumeric
B	00	numeric*
B	01	tone only
B	10	tone only
B	11	alphanumeric*

* 4-bit burst correction possible

Error correction is applied to the message codewords. Normally, this is a single-bit correction but a 4-bit burst correction algorithm can be selected. In the latter, a compromise has to be made between call success rate and false call rate. The processing of the message data is

determined by the function bits (FC) of the address codeword and the RIC that's been called (A or B as shown in Table 1, refer also to Figs 6, 8 and 9). The processed message data is sent to the microcontroller to be converted into numeric or alphanumeric characters for display.

Decoder RAM

The static RAM of the PCA5000T stores two 18-bit address codes A and B, the three frame address bits (FR0-2) and six special function bits (SPF01-06), organized as five words of nine bits each, see Fig.9. The lithium back-up battery ensures data retention. As shown in Fig.8, the 21-bit receiver identification code (RIC) consists of the 18-bit address code plus 3 bits of the frame number (FR0-2) which must, therefore, be common to both user addresses.

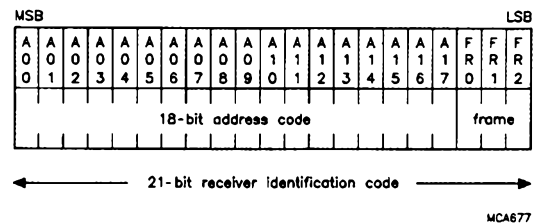


Fig.8 Receiver identification code (RIC) storage

The 6 special function bits are programmed to perform the following functions:

- SPF01: 0' beep-only' pager operation, silent call storage enabled and silent override for address B (function bits, FC = xx), voltage doubler disabled
 - 1 display pager operation, voltage doubler determined by SPF02, silent call storage disabled, 16.384 kHz output enabled
- SPF02: 0 enable voltage doubler (SPF01 = 1)
 - 1 disable voltage doubler (SPF01 = 1), alert cadence 1 when FC = 11
- SPF03: 0 1-bit error correction on message codewords
 - 1 4-bit burst error correction on message codewords with address B, FC = 00 or 11
- SPF04: user programmable
- SPF05: 0 silent override enabled on address B, FC = 01 or 10
 - 1 silent override enabled on address B, FC = 00 or 11
- SPF06: 0 silent override disabled on address A, FC = 10
 - 1 silent override enabled on address A, FC = 10

The silent override facilities are shown in Fig.10.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A 0 B	A 0 7	A 0 6	A 0 5	A 0 4	A 0 3	A 0 2	A 0 1	A 0 0
word 1	A 1 7	A 1 6	A 1 5	A 1 4	A 1 3	A 1 2	A 1 1	A 1 0	A 0 9
word 2	B 0 8	B 0 7	B 0 6	B 0 5	B 0 4	B 0 3	B 0 2	B 0 1	B 0 0
word 4	B 1 7	B 1 6	B 1 5	B 1 4	B 1 3	B 1 2	B 1 1	B 1 0	B 0 9
word 3	F R 2	F R 1	F R 0	S P F 0 6	S P F 0 5	S P F 0 4	S P F 0 3	S P F 0 2	S P F 0 1

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Fig.9 Receiver identification code (RIC) mapping

SPF 01	SPF 05	SPF 06	Silent override facility
0	X	X	Enable on address B, FC = XX
X	0	X	Enable on address B, FC = 01 or FC = 10
X	1	X	Enable on address B, FC = 00 or FC = 11
X	X	0	Disable on address A, FC = 10
X	X	1	Enable on address A, FC = 10

'X' = don't care
'0' = bit reset
'1' = bit set

MCA678

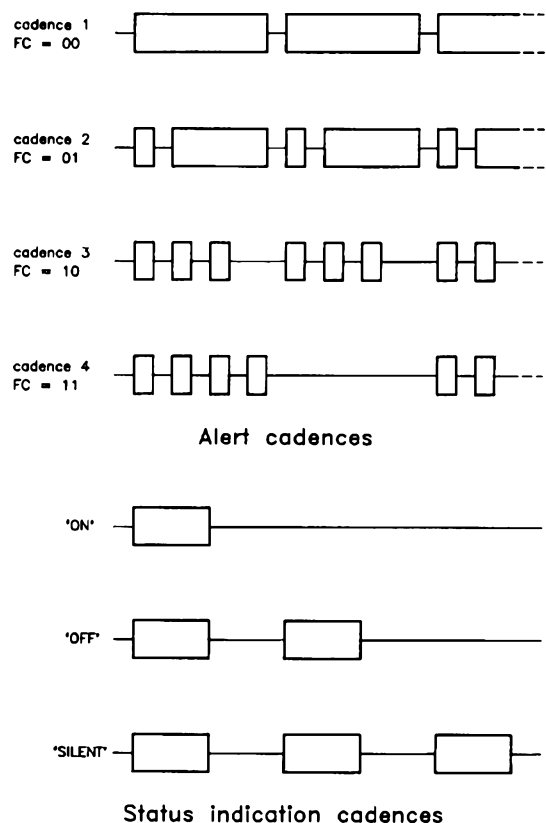
Fig.10 Silent override facilities

PCA500T audio and LED output signals

The paging decoder generates alert cadences by sending a 2 kHz square-wave modulated output signal to a magnetic or piezoceramic beeper, see Fig.11. The form of the alert cadence is determined by the two function bits in the address word. Alert cadences are generated if the pager is in the ON state and a valid call or message is received, if the pager is in the SILENT state and a silent override call is received, or if a 'beep-only' pager is switched from SILENT to ON and calls have been stored. In a display pager, alert cadences are generated only after the complete message has been received. During the first 4 seconds, the low intensity alert cadences are generated by energizing the alert low level output. For the following 12 seconds the alert high level output is energized to increase the alert cadence intensity. The increased intensity facility is not available if the vibrator option is in use. Alert cadence generation ceases after 16 seconds or, in a 'beep-only' pager, when the status is changed using the control pushbuttons or, in a display pager, when the status/reset selection is activated.

If the vibrator enable input is set to a logic HIGH, the vibrator control logic in the alerter interface switches a squarewave to the alert high level/vibrator output. High intensity alert cadences are inhibited and, if the paging decoder is in the SILENT state, no alert cadences are generated on receipt of calls. Instead, the alert high level/vibrator output is switched to a logic HIGH for the normal 16 seconds or until terminated by the user. Call storage in the SILENT state and silent override calls are inhibited.

The alerter interface provides information on the current state of the paging decoder as a result of user status interrogation. Figure 11 shows the status indication cadences. Status cadences are generated in the 'beep-only' mode when the internal state of the decoder is changed. Pressing the ON, OFF or SILENT push-button causes the status cadence of the present internal state to be generated (if no higher order alert cadences are being generated at the same time). The status cadence of the new internal state is generated after 1.5 seconds.



MCA679

Fig.11 Alert and status cadences

The battery level detector receives the low battery indicator signal from the paging receiver whenever ON or SILENT states are selected and the paging receiver is enabled. Each measurement is sent to the battery low level output. When four consecutive values from the paging receiver are a logic HIGH level, a continuous high level alert tone is generated when the paging decoder is programmed to 'beep-only' operation. When the battery low alert is reset, the battery low alert tone will not occur again until the pager is switched from the OFF state to the ON state.

The alarm input causes the PCA5000T to generate a continuous high-intensity alert tone, or, if the alarm input is pulsed, to generate a high intensity pulsed tone. Alarm tone generation overrides all other tone generation. Alert cadence generation has priority over battery low alert tone generation. Status indication cadences are always completed before generation of the alert cadence or the battery low alert tone.

The Out-Of-Range output is used to drive an indicator LED. When the ACCESS algorithm of the paging decoder is in stage 5 of the ACCESS algorithm (see POCSAG Data Decoding), the Out-Of-Range output is a logic HIGH for 62.5 ms in 1125 ms, i.e. a duty factor of 1 in 18.

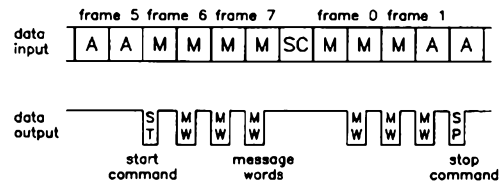
PCA5000T microcontroller interface output signals

The second interface of the PCA5000T is the serial microcontroller interface to convey the POCSAG message data to the microcontroller for processing and display. When the paging decoder has detected a valid address codeword, a serial data transmission commences with a start command word on the serial microcontroller interface. The start command word consists of 8 bits as follows:

- Bit 0: 0
- Bit 1: 1
- Bit 2: SPF03, as programmed
- Bit 3: SPF06, as programmed
- Bit 4: SPF05, as programmed
- Bit 5: 0 message on RIC A
1 message on RIC B
- Bit 6: FC 1, function bit 1,
as defined by the address codeword, bit 20
- Bit 7: FC 2, function bit 2,
as defined by the address codeword, bit 21.

When the start command word has been sent, the message fields of the message codewords are sent to the microcontroller in a 24-bit format, see Fig.12. The first 4 bits are always logic HIGH while bits 4 to 23 are bits 2 to 21 of the message codeword. The end of a message transfer is defined by the transmission of an 8-bit stop command word composed as follows:

- Bit 0: 0
- Bit 1: 0
- Bit 2: 0 message unsuccessfully terminated, erroneous, un-correctable codeword
1 message successfully terminated, address or idle codeword received
- Bit 3: 0 vibrator enable input at logic HIGH
1 vibrator enable input at logic LOW
- Bit 4: SPF04, as programmed
- Bit 5: SPF02, as programmed
- Bit 6: not defined
- Bit 7: not defined



a) Message output format

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0	1	SPF 03	SPF 06	SPF 05	RIC A/B	Address bit 20	CW bit 21

function code

b) Start command format

bit 0	bit 1	bit 2	bit 3	bit 4	message codeword bit 2 to bit 21 as received			bit 23
1	1	1	1					

c) Message word format

bit 0	bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7
0	0	ST	QS input	SPF 04	SPF 02	not used	not used

ST: successful termination

d) Stop command format

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Fig.12 PCA5000T/microcontroller interface communication

The end of a message transfer is also defined by a second start command word if the pager receives two successive calls. When this occurs, the presence of a start command word to define end of message transfer indicates successful message transmission and termination.

Figure 13 shows the microcontroller serial interface signals. The data strobe output from the paging decoder is the reference data clock for the microcontroller.

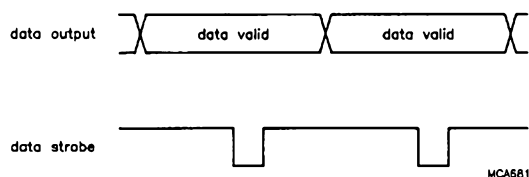


Fig.13 Microcontroller interface signals

Voltage doubler

The PCA5000T contains an integrated voltage converter to double the microcontroller supply voltage, V_{REF} , see Figs 1 and 7. If enabled by the special function bit SPF02 (see Decoder RAM storage) V_{REF} is equal to $2V_{cc}$, so that V_{REF} is -6 V maximum (Ref.3). The pager earth is the positive supply voltage V_{cc} in Fig.1. The output impedance of the microcontroller supply voltage is determined by the voltage converter control input, PC, so that if PC is high, a high impedance is inserted in the V_{REF} output, and if PC is low, a low impedance is inserted in the V_{REF} output. This shifts the logic LOW level for all the serial microcontroller interface signals accordingly. The doubled negative voltage level on V_{REF} enables the PCA5000T to operate directly in conjunction with CMOS microcontrollers and to drive different liquid-crystal displays.

If the power requirements of the external circuitry exceed the drive capability of the integrated voltage converter, an external power supply can be used. The drive capability is -150 μ A at $V_{REF} = -2.7$ V minimum, using a supply voltage of -2.0 V with PC = 0. With an external supply, the pump capacitor is removed from pins CP and CN and the external voltage source is directly connected to V_{REF} . Even in this case, the level-shifted interface logic signals are maintained.

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Abstracts

All-digital phase-locked loops using the 74HC/HCT297

Although some highly integrated PLLs use a lot of digital circuitry, they're still semi-analog circuits so their operating parameters and VCO stability are inherently sensitive to component value spreads and to changes of supply voltage and temperature. If the PLL system must have a narrow output frequency range (e.g. for FM demodulation or vertical scan synchronization), the pull-in range may be caused to shift sufficiently to exclude the input frequency. The only way to restore the correct pull-in range is then to individually adjust the centre frequency of the VCO in each PLL to its correct value. This article shows how our HCMOS 74HC/HCT297 IC allows an all-digital PLL to be implemented with very stable crystal-controlled clock pulse generators and digital circuitry instead of a VCO, thereby eliminating parameter changes and the need for individual circuit adjustments of the centre frequency.

MOSFETs control motors in automotive applications

There is increasing demand for low-cost, reliable electronic switching of motors in motor vehicles. Despite the wide variety of motor types and drive configurations there is a Philips power MOSFET solution available to suit it. The broad range of types includes L²FETs, sensorFETs, FREDFETs and devices with on-chip intelligence. The combination of low on-state resistance, ease of drive and ruggedness make them an attractive choice in the arduous automotive environment.

Focusing semiconductor laser diodes in barcode readers

Barcodes are now an accepted way of coding product type, price, date of manufacture etc. Though they were formerly read with He-Ne lasers, today's semiconductor lasers with built-in optics are taking over this task. Philips' long experience in producing lasers for CD and LaserVision products allows it to supply lasers with integrated optics for use in a whole range of applications, including barcode readers, laser printers and robotic guidance systems. This article evaluates Philips' laser-diode focusing system and demonstrates its suitability for use in barcode scanners.

Innovations in oscilloscope tubes

Advanced CAD techniques have been used to predict the performance of domed-mesh PDA oscilloscope tubes and determine the gun layout for optimum sensitivity and line brightness. Optimum layout was found to be short and independent of gun voltage, allowing the user to determine the compromise between writing speed and sensitivity. The manufacture of such an oscilloscope tube has been made possible with the development of internal magnetic correction (IMC), for extremely accurate beam control, and of new techniques for envelope manufacture, allowing the gun parts to be precisely aligned.

New chip-set reduces the power consumption of radio pagers

The radio pager ICs described in this article operate from a low supply voltage and consume minimal current to maximize operation time from one battery charge and minimize the size of pocket pager receivers. The heart of the pager system is the 512 bits/s PCA5000T decoder. In addition to decoding the received data in accordance with CCIR recommendation 584, radio paging code No.1 (POCSAG code), this IC minimizes the drain on the battery by optimizing the power down/up periods of paging receiver (UAA2033T or UAA2050T) and, for a display pager, also minimizing the power down/up periods of the microcontroller and LCD. When used in an alert-only pager, the two ICs support a call rate of fifteen calls a second. When used in a display pager, they support a call rate of five 10-digit numeric message calls per second, or two 17-character alphanumeric message calls per second.

Rein digital arbeitende PLL-Schaltung mit dem 74HC/HCT297

Obwohl bei einigen hochintegrierten PLL-Schaltungen viele digitale Schaltkreise verwendet werden, handelt es sich immer noch um halbanalog arbeitende Schaltungen, deren Betriebsparameter und VCO-Stabilität empfindlich auf Streuungen der Bauelementwerte sowie auf Änderungen der Versorgungsspannung und der Temperatur reagieren. Wenn das PLL-System einen kleinen Ausgangsfrequenzbereich hat (wie z.B. bei der FM-Demodulation oder Vertikalsynchronisation), kann sich der Fangbereich der PLL-Schaltung dann so weit verschieben, daß die Frequenz des Eingangssignals nicht mehr in den Fangbereich fällt. Die einzige Möglichkeit, den richtigen Fangbereich wieder herzustellen, besteht darin, die Mittenfrequenz des VCO auf den nominalen Wert einzustellen. Dieser Artikel beschreibt, wie sich mit unserem IC 74HC/HCT297 eine rein digital arbeitende PLL realisieren läßt, die hochstabile quarzgesteuerte Taktgeneratoren und digitale Schaltungen anstelle eines VCO verwendet, wodurch Parameteränderungen eliminiert werden und sich somit die Notwendigkeit eines Abgleichs der Mittenfrequenz der individuellen Schaltungen erübrigt.

Elektronische Steuerung von Fahrzeugmotoren über MOSFETs

Die Nachfrage nach preisgünstigen, zuverlässigen Schaltern für Kraftfahrzeug-Motoren nimmt ständig zu. Trotz der großen Vielfalt an Motortypen und den zahlreichen Ansteuerungs-Konfigurationen bietet Philips mit seinen Leistungs-MOSFETs in den meisten Fällen eine geeignete Lösung. Das umfangreiche Produktangebot umfaßt L²FETs, Sensor-FETs, FREDFETs und Bauelemente mit On-Chip-Intelligenz. Diese Elemente weisen einen geringen Durchlaßwiderstand auf, sind einfach anzusteuern und robust. Damit eignen sie sich hervorragend für den Einsatz unter den harten Bedingungen des Automobilbetriebs.

Fokussierende Halbleiter-Laserdioden in Strichcode-Lesern

Strichcodes sind heute ein gängiges Mittel zur Codierung von Produkttyp, Preis, Herstellungsdatum usw. Während sie früher mit HeNe-Lasern gelesen wurden, übernehmen heute Halbleiterlaser mit eingebauter Optik diese Aufgabe. Philips besitzt eine langjährige Erfahrung im Bereich der Fertigung von Lasern für CD- und LaserVision-Produkte und kann daher Laser mit integrierter Optik für zahlreiche Applikationen, einschließlich Strichcode-Lesern, Laserdruckern und Roboter-Führungssystemen, liefern. In diesem Artikel wird das Laserdioden-Fokussiersystem von Philips beschrieben und seine Eignung für die Verwendung in Strichcode-Lesern beurteilt.

Innovationen bei Oszilloskop-Röhren

Mit Hilfe moderner CAD-Techniken kann die Leistungsfähigkeit von PDA-Oszilloskop-Röhren mit gewölbter Netzelektrode gesteigert und das Strahlensystem so angeordnet werden, daß optimale Empfindlichkeit und Linienhelligkeit erreicht werden. Es stellte sich heraus, daß das optimale Layout geringe Länge hat und unabhängig von der Spannung des Strahlensystems ist und dem Anwender damit erlaubt, einen Kompromiß zwischen Schreibgeschwindigkeit und Empfindlichkeit zu finden. Die Herstellung einer solchen Oszilloskop-Röhre wurde erst möglich durch die Entwicklung der internen Magnetkorrektur (IMC), mit der der Strahl äußerst genau gesteuert werden kann, sowie durch die Anwendung neuer Techniken für die Röhrenkolben-Fertigung, mit denen die Teile der Elektronenstrahlröhre genau ausgerichtet werden können.

Neuer Chip reduziert die Leistungsaufnahme von Funkrufempfängern

Die in diesem Artikel beschriebenen ICs für Funkrufempfänger arbeiten bei einer niedrigen Versorgungsspannung und nehmen nur sehr wenig Strom auf, so daß die Betriebszeit mit einer Akkuladung maximiert und die Größe der Taschen-Rufempfänger stark verkleinert wird. Der 512-bit/s-Decoder PCA5000T bildet das Kernstück des Rufsystems. Dieses IC sorgt nicht nur für die Decodierung der empfangenen Daten gemäß der CCIR-Empfehlung 584, Paging-Code Nr. 1 bei Rufanlagen (POCSAG-Code), sondern minimiert auch die Belastung des Akkus, indem es die Ein- und Ausschaltdauer des Rufempfängers (UAA2033T oder UAA2050T) und – bei einer Display-Rufanlage – des Mikrocontrollers sowie der Flüssigkristallanzeige optimiert. Bei Verwendung in einer Alert-Only-Rufanlage unterstützen die beiden ICs eine Anruhfrequenz von 15 Anrufen pro Sekunde und bei Verwendung in einer Display-Rufanlage eine Anruhfrequenz von fünf Anrufen mit 10stelligen numerischen Meldungen pro Sekunde oder von zwei Anrufen mit 17stelligen alphanumerischen Meldungen pro Sekunde.

Boucles à verrouillage de phase entièrement numériques utilisant le 74HC/HCT297

Bien que certaines boucles à verrouillage de phase hautement intégrées utilisent de nombreux circuits numériques, il s'agit toujours de circuits semi-analogiques et de ce fait leurs paramètres de fonctionnement ainsi que la stabilité de l'oscillateur commandé en tension sont sensibles tant à la gamme des valeurs des composants qu'aux changements de la tension du secteur et de la température. Si le système de boucles à verrouillage de phase doit avoir une réponse en fréquence étroite (par exemple pour la démodulation FM ou pour la synchronisation du balayage vertical), il se peut que la plage de synchronisation se décale suffisamment pour exclure la fréquence d'entrée. Le seul moyen pour rétablir la plage de synchronisation correcte consiste à corriger individuellement la fréquence centrale de l'oscillateur commandé en tension pour chaque boucle à verrouillage de phase. Cet article montre comment notre circuit CMOS à haute vitesse 74HC/HCT297 permet de réaliser une boucle à verrouillage de phase entièrement numérique, dotée de générateurs d'impulsions pour l'horloge commandée par un quartz très stable et de circuits numériques au lieu d'un oscillateur commandé en tension, éliminant ainsi les variations de paramètres et ne nécessitant plus les réglages individuels des circuits de la fréquence de centre.

Contrôle de moteur électrique pour automobile grâce aux dispositifs MOS à effet de champ

La demande de systèmes de contrôle de moteurs électriques fiables et peu onéreux, pour application automobile, se fait de plus en plus importante. Malgré le grand choix de types de moteurs et de configurations de commande, Philips propose un dispositif MOS à effet de champ pour répondre à cette demande. La large gamme de types disponibles comprend des L²FETS, des SENSORFETS, des FREDFETS et des dispositifs de puissance intelligents. Leur faible résistance à l'état passant, leur commande aisée et leur robustesse en font une solution intéressante dans le difficile domaine de l'électronique automobile.

Réglage des diodes lasers à semiconducteurs pour les lecteurs de code à barres

Les codes à barres constituent aujourd'hui un moyen répandu de codage des types de produit, des prix, de la date de fabrication, etc. Si auparavant ils étaient lus avec des lasers He-Ne, ils le sont aujourd'hui par des lasers à semiconducteurs, dotés de caractéristiques optiques intégrées. L'expérience que Philips a depuis longtemps acquise dans la production de lasers pour disques compacts et produits Laservision lui permet de présenter des lasers dotés de caractéristiques optiques intégrées, pouvant être utilisés dans une large gamme d'applications, y compris les lecteurs de codes à barres, les imprimantes à laser et les systèmes de guidage de robots. Cet article évalue le système de réglage des diodes lasers Philips et démontre qu'il convient aux lecteurs de codes à barres.

Innovations en matière de tubes pour oscilloscopes

Des techniques de pointe en CAO ont été utilisées pour prévoir les performances des tubes pour oscilloscopes à post-accélération à grille bombée et pour déterminer le tracé du canon afin d'assurer une sensibilité et une luminosité de ligne optimales. On a découvert que le tracé optimal doit être court et indépendant de la tension du canon, ce qui permet à l'utilisateur de faire le compromis entre la vitesse d'écriture et la sensibilité. Ces tubes pour oscilloscope doivent leur réalisation tant au développement de la correction magnétique interne (IMC) pour un contrôle extrêmement précis du faisceau, qu'à celui de nouvelles techniques de fabrication de l'enveloppe, permettant un alignement précis des pièces constituant le canon.

De nouveaux circuits pour diminuer la puissance absorbée des systèmes d'appels radio

Les CI pour système d'appels radio décrits dans cet article fonctionnent avec une faible tension secteur et consomment un courant minimum pour maximiser le temps de fonctionnement des piles et pour réduire au minimum la taille des récepteurs de poche. Le décodeur PCA5000T de 512 bits/s est à la base du système d'appel. En plus du décodage des données reçues, conformément à la recommandation 584 du CCIR, code N°1 relatif aux appels radio (code POCSAG), ce CI garantit une utilisation maximale de la pile en optimisant la consommation du récepteur d'appels (UAA2033T ou UAA2050T) et dans le cas d'appel par affichage LCD, il réduit au minimum le courant du microcontrôleur. En cas d'appels d'urgence, les deux CI acceptent quinze appels par seconde. Pour des appels par affichage, ils enregistrent un taux d'appels de cinq messages numériques à 10 chiffres par seconde ou deux messages alphanumériques de 17 caractères par seconde.

Lazos enclavadores de fase (PLL) totalmente digitales usando los circuitos 74HC/HCT297

Aunque algunos circuitos PLL altamente integrados utilizan una gran parte de circuitería digital, aún tienen circuitos semianalógicos de modo que sus parámetros de trabajo y estabilidad del VCO son inherentemente sensibles a las dispersiones del valor de los componentes y a variaciones de la tensión de alimentación y temperatura. Si el sistema PLL debe tener un estrecho margen de frecuencia de salida (por ejemplo para demodulación de FM o sincronización del barrido vertical), el tiempo de enganche puede ser suficientemente largo como para excluir la frecuencia de entrada. La única forma de reestablecer el tiempo de enganche correcto es ajustar individualmente la frecuencia central del VCO en cada PLL a su valor correcto. Este artículo muestra cómo nuestros circuitos integrados HCMOS 74HC/HCT297 permiten implementar un PLL totalmente digital con generadores muy estables de impulsos de reloj controlados por cristal y circuitería digital en lugar de un VCO, eliminando así las variaciones de los parámetros y la necesidad de ajustes individuales de la frecuencia central.

Control del motor eléctrico del automóvil usando MOSFETs

Existe una creciente demanda por un encendido electrónico, fiable y de bajo coste del motor de los vehículos. A pesar de la amplia variedad de los tipos de motor y configuraciones de excitación, existe una solución con dispositivos MOSFET de potencia de Philips. La amplia gama de tipos incluye dispositivos L FETs, FETs sensores, FREDFET y dispositivos con inteligencia incorporada en el chip. La combinación de una baja resistencia en estado de conducción, facilidad de excitación y robustez los hacen especialmente atractivos para su utilización en las arduas condiciones del automóvil.

Enfoque de los diodos láser de semiconductor en lectores de códigos de barras

Actualmente los códigos de barras son una forma aceptada de codificar tipos de producto, datos de fabricación, etc. Aunque en un principio éstos eran leídos con láseres de He-Ne, actualmente están siendo reemplazados por los láseres de semiconductor actuales con óptica incorporada. Philips, que tiene una gran experiencia en la fabricación de láseres para dispositivos como CD (Compact Disc) y Laservisión puede suministrar láseres con óptica integrada para su uso en una amplia gama de aplicaciones, incluyendo lectores de códigos de barras, impresoras láser y sistemas de guía de robots. Este artículo evalúa el sistema de enfoque de diodos láser y demuestra que es adecuado para exploradores de código de barras.

Innovaciones en tubos de osciloscopio

Se han usado técnicas avanzadas de CAD para predecir el funcionamiento de los tubos de osciloscopio PDA de malla abombada y determinar la disposición del cañón para óptima sensibilidad y brillo de línea. Se ha visto que la disposición óptima debe ser corta e independiente de la tensión del cañón, permitiendo al usuario determinar el compromiso entre velocidad de escritura y sensibilidad. La fabricación de un tubo de osciloscopio de estas características ha sido posible con el desarrollo de la corrección magnética interna (IMC) para un control de haz extremadamente preciso, y de las nuevas técnicas para la fabricación de la carcasa, lo que permite que las partes del cañón estén alineadas de forma precisa.

Nueva familia de circuitos integrados que reduce el consumo de potencia de buscapersonas por radio

Los circuitos integrados para buscapersonas descritos en este artículo funcionan con una baja tensión de alimentación y consumen una mínima corriente con el fin de maximizar la duración de la batería y minimizar el tamaño de receptores buscapersonas de bolsillo. El corazón del sistema es un decodificador PCA5000T de 512 bits/s. Además de decodificar los datos recibidos de acuerdo con la recomendación CCIR 584, código de buscapersonas por radio N° 1 (código POCSAG), este circuito integrado minimiza el consumo de batería optimizando los periodos de potencia baja/alta del receptor buscapersonas (UAA2033T o UAA2050T) y, para un buscapersonas visualizador también minimiza los periodos de potencia baja/alta del microcontrolador y del LCD. Cuando se usa en un buscapersonas de sólo alarma, los dos circuitos integrados soportan una velocidad de llamada de quince llamadas por segundo. Si se usa en un buscapersonas visualizador, éste soporta una tasa de llamadas de cinco llamadas mensaje de 10 dígitos numéricos por segundo, o dos llamadas mensaje alfanuméricas de 17 caracteres por segundo.

Authors



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Peter Chall was born in Offenburg, Germany, in 1950. After graduating in physics from the University of Düsseldorf in 1977, he was contracted to the Deutsche Forschungs Gemeinschaft for research into the use of lasers for plasma analysis. In 1983 he returned to the University of Düsseldorf and was awarded a PhD for this research. Subsequently he joined Telefunken for development work in laser modules. Since 1986 he has lead the applications group for short wavelength diode lasers at Philips Components, Nijmegen, The Netherlands.



Arthur Woodworth was born in Manchester in 1945. He took a BSc in electrical engineering at Salford University in 1968 and later that year joined Mullard, Stockport (now Philips Components Ltd.) where he is now head of the Electrical Development Department responsible for the specification and evaluation of a wide range of rectifiers, thyristors, triacs and GTOs. He is currently specializing in the area of automotive products.



Stefan Drude was born in Düsseldorf, Germany, in 1957. He received his Diplom-Ingenieur degree in electrical engineering from the RWTH Aachen, in 1983, and joined the Valvo Application Laboratory the same year to work on various microcontroller applications including remote control, car radio and BTX. Since 1988 he had led a group working on pagers and other mobile communication systems.



Klaus Zeppenfeld was born in Halle, Germany, in 1940. After taking his doctorate in Physics at Hamburg in 1970 he joined Philip's Research Laboratories at Aachen and transferred to the Eindhoven Laboratory in 1973. Since 1977 he has been engaged in cathode ray tube development and is product manager for oscilloscope tubes at Heerlen, The Netherlands.



Wim Rosink was born in Delden, the Netherlands, in 1939 and graduated in electronic engineering from Enschede Polytechnic in 1959. After military service he joined the Application Laboratory of Philips Components, Eindhoven (PCALE) where he was first involved in the design of wideband amplifiers. In 1967 he became engaged in application work on devices for power control, especially for motor-speed control. Since 1988 he has provided application support for standard CMOS logic ICs and is currently Field Application Engineer for these products.

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