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Ever since the humble transistor radio appeared in the 1950s, Philips has spearheaded development of solid-state entertainment equipment. Colour TVs, radios, analogue and digital cassette recorders, digital TVs and CD players are just some of the items that have emerged. Now, however, the airwaves are so congested that broadcasters need to transmit at such high frequencies that their signals can only be radiated far enough by satellite-borne transmitters. This year sees the launch of the first satellite solely for the re-transmission of public radio, TV and teletext services. From its geostationary orbit 36 000 km above the earth, it will radiate multilingual news, sport and entertainment programmes to Western Europe. Once again Philips has met the technological challenge and, with Nordic VLSI and Plessey Semiconductors, has developed a DBS TV transmission decoder and IC set for handling signals encoded in accordance with any of today's European DBS TV transmission standards. The architecture of this advanced decoder, described on page 186, is such that it can also accommodate the requirements of any future TV services.

Contents

Two-chip modem for high-speed LAN systems

PRASANNA SHAH

Modems that employ the frequency-shift-keying (FSK) modulation technique are particularly suitable for LAN applications because of their high noise immunity and amplitude independence, which together yield a low bit-error rate. FSK modems are also relatively easy to construct and are, therefore, inexpensive in comparison with those employing more esoteric modulation techniques. Low-speed FSK modems have been available in ICs for some years but, until recently, FSK modems that could operate at speeds higher than 19200 bits/s were available only at the board level and employed many discrete and small-scale-integration (SSI) components.

Now, however, you can obtain a complete, high-speed modem in the form of two ICs: the NE5080 transmitter and the NE5081 receiver. These ICs can provide transmission rates as high as 8 Mbits/s, depending on the attenuation characteristics and the length of the cable used to connect the nodes.

For maximum error-free transmission rate, the coaxial cable should be kept short (since transmission rate falls with increasing cable length). Nevertheless, it's still possible to achieve a transmission rate of 500 kbits/s over a 30 000 m length of cable without any repeaters. You can adjust the sensitivity of the receiver to compensate for the cable length and for the noise level of the environment. For a signal-to-noise ratio of 20 dB, the typical error rate of a link using this modem is one in 10^{12} bits.

The NE5080 transmitter IC, which consists of six functional blocks (Fig.1), contains an on-chip voltage regulator that provides the current and voltage references used by the internal circuitry. It's possible to adjust the transmitter's centre frequency by selecting appropriate values for the tuning capacitor (C_O) and resistor (R_{CS}).

The TTL data-input circuits and their associated switch-driver circuits switch the current sources (I) into or out of the circuit according to the current value of the input bit.

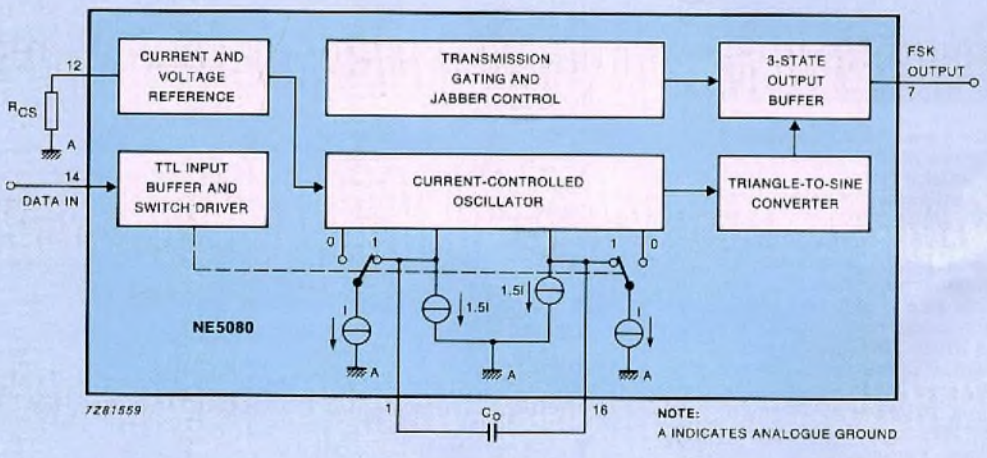


Fig.1 This FSK transmitter chip works at frequencys as high as 8 MHz. You can set the transmitter centre frequency by means of external trimming components

The switching process changes the total average current that charges or discharges C_O from 1.5I to 2.5I, or vice versa. The change in current causes the current-controlled oscillator to shift its output from one frequency to another in a manner that keeps the output phase continuous and eliminates sharp discontinuities in the output waveform. This Continuous-Phase FSK (CPFSK) technique has the advantage of confining most of the power to the main lobe of the spectrum; the consequent reduction of the power radiated into the sidebands reduces adjacent-channel interference (Ref.1).

The ratio of the two output frequencies is equal to the ratio of the average currents that charge and discharge C_O. The values of the current sources are fixed, and they normally yield a constant frequency ratio (f_0/f_1) of 1.666; however, by adding external components you can modify this ratio, which determines the bandwidth used by a particular channel.

The transmission chip's triangle-to-sine-wave converter circuitry converts the triangular output of the current-controlled oscillator to a sine wave with a total distortion of 2% or less. The transmission-gating circuits permit or prevent the transmission of data. The disable function not only puts the 3-state output buffer into the high-impedance state but also shuts off the current-controlled oscillator to prevent any feed-through to the output circuit.

The chip's jabber-control circuits are similar to its transmission-gating circuits, except that the jabber-control circuits provide a means of programming the length of the transmission. This feature acts as a failsafe that prevents a malfunctioning NE5080 transmitter or transmitter controller from tying up the network. To make use of the feature, you can connect an external capacitor from the chip's jabber-control pin (pin 3, not shown in Fig.1) to ground; an internal current source provides a small current to charge this capacitor. When the voltage across the capacitor reaches a preset threshold level, the jabber-control circuits disable the output buffer and shut off the oscillator. For point-to-point communications, which do not need the jabber-control feature, you can disable the circuitry by grounding pin 3.

Adjusting receiver sensitivity

The NE5081 receiver IC (Fig.2), like the NE5080 transmitter, contains an on-chip voltage regulator that provides all the voltage- and current-reference levels needed by the internal circuitry. The input-limiter circuits accept the incoming FSK signal and maintain their output amplitude at a constant level for all input-signal amplitudes ranging from 16 to 1100 mV (rms).

A phase shifter and a balanced analogue multiplier use a quadrature-detection scheme to demodulate the incoming data. To use the receiver IC, you need to select the values of the phase-shifter tank circuit (L_1 and C_1) to resonate at the centre frequency of the incoming carrier. To ensure good selectivity, the tank circuit must have a high Q factor. The balanced analogue multiplier accepts both the original amplitude-limited carrier signal and the phase-shifted derivative, and it generates signals containing both the baseband data and high-order harmonics.

A simple, second-order Butterworth lowpass filter eliminates the original carrier frequency and the high-order intermodulation products. The output of the filter contains only baseband data that is the equivalent of the original data applied to the transmitter at the remote end of the link. External resistors and capacitors allow adjustment of the filter's cutoff frequency.

A comparator determines the status of the input bit by comparing the output of the lowpass filter to a programmable reference threshold. By means of an external resistor, the threshold of the input-level-detection circuitry can be set to correspond to the minimum input-signal amplitude that is detectable above the noise. If the input signal amplitude falls below this preset threshold, the level-detection circuitry disables the receiver output buffers so

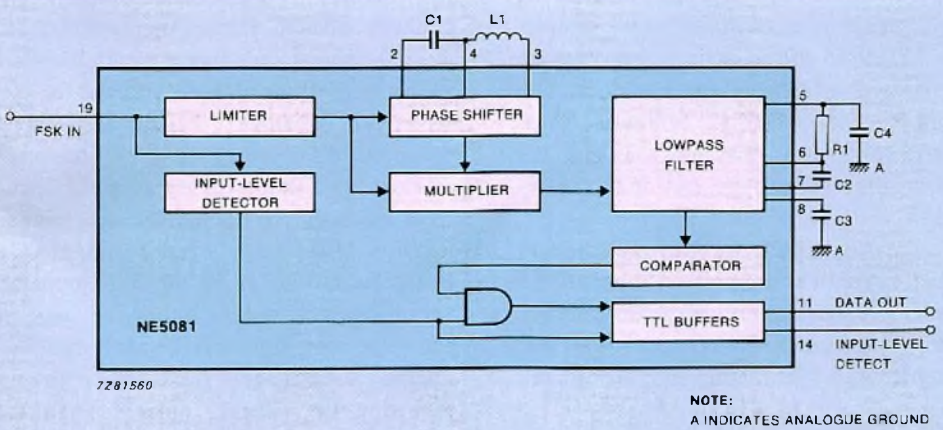


Fig.2 This FSK receiver chip uses quadrature detection. It automatically disables the output buffers when the input signal falls below a preset threshold

that noise will not be interpreted as data. The level-detection circuitry also generates a flag signal. When the flag is at logic 1, the input-signal amplitude is above the threshold, and the output buffers are presenting valid data.

The transmitter's high drive capability and the receiver's wide dynamic range allow the use of long lengths of cable (both coaxial and twisted pair) without any repeaters.

The receiver chip has built-in differential input circuits, so no extra components are needed at that end of the link. The transmitter chip has a single-ended output, so an inverting amplifier is needed to provide the inverted signal to the line. A single amplifier based on an opamp with a wide unity-gain bandwidth (Fig.3) is usually adequate for this purpose. However, if your inverting amplifier causes severe phase delay (which could impair the link's noise immunity or error rate), you'll have to add a matching non-inverting amplifier to drive the in-phase line and restore the phase balance.

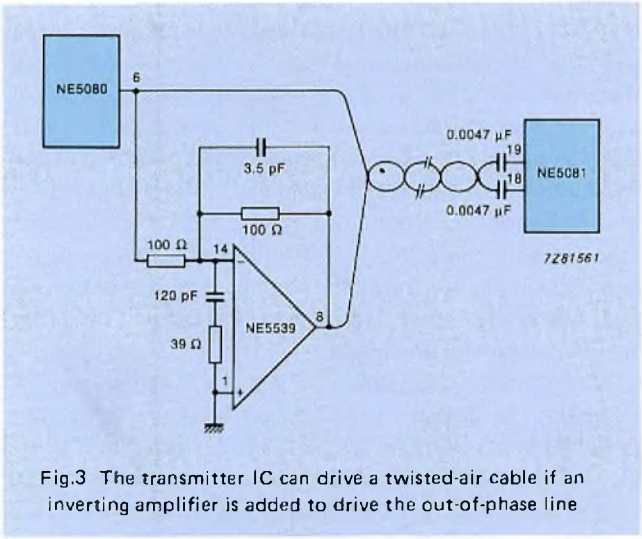


Fig.3 The transmitter IC can drive a twisted-air cable if an inverting amplifier is added to drive the out-of-phase line

Although a link employing these transmitter and receiver ICs has high inherent immunity to noise, some situations may require additional precautions. The ambient electrical-noise level in a factory environment, for example, is much higher than that of an office environment because of the EMI/RFI generated by heavy-duty machines. The bit-error rate of a link is a function of the S/N ratio. Thus, to improve the bit-error rate in a noisy environment, it's necessary to filter out the excess noise power at the receiver input.

Choice of active or passive filters for this purpose will depend upon the signal strength at the receiver input. If the signal strength is great, you can use an inexpensive passive LC bandpass filter. For low signal levels, an active filter will boost the in-band signal while attenuating the out-of-band noise.

If you elect to use a passive filter, keep the Q factor of the circuit as high as possible. To minimize the attenuation of the in-band signal, make sure that the Q factor is at least 35. The filter's characteristics will depend upon the spectrum of the transmitted signal.

Figure 4 shows a typical spectrum at the output of an NE5080 that is transmitting a pseudorandom data stream. The figure indicates the filter characteristics needed to eliminate the sidebands and out-of-band noise. You can use 2-, 3-, or 5-pole Butterworth passive filter for this purpose (Fig.5). Figure 6 shows the actual spectra obtained in a test of the chip's transmission of a pseudorandom data stream at 7.7 MHz, with and without the 5-pole filter. This filter attenuates the sidebands and the out-of-band noise by more than 40 dB, so it yields a much-improved S/N ratio and a lower bit-error rate.

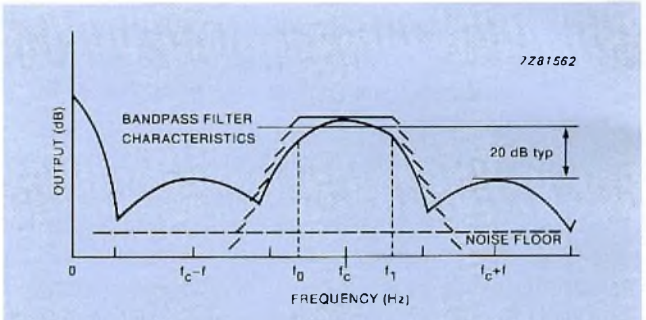


Fig.4 Sidebands are 20 dB below the main lobe in this spectrum of a typical NE5080 chip's transmission of pseudorandom data. The frequency ratio, f_1/f_0, is internally set to 1.666, but it can be modified by external components

When designing active filters for a high-frequency carrier, be sure to pick an amplifier with the widest possible unity-gain bandwidth: the NE5539, for example, is well suited to this application because of its 350 MHz unity-gain bandwidth (Ref.2).

You can extend the principle of filtering sidebands and out-of-band noise to create a multichannel frequency-division-multiplexed (FDM) system. The modem chip set can work over a wide range of centre frequencies (from less than 50 kHz to more than 20 MHz). Thus, it's possible to connect several transmitter/receiver pairs to the same coaxial cable to provide a multichannel FDM system. An appropriate filter at each transmitter output and receiver input can eliminate crosstalk between the channels. This capability is important for several reasons.

First, an FDM system makes efficient use of one of the most expensive components in any digital communications network — the cable. Second, you can use the same printboard layout for all of the FSK modems on the network; to change the centre frequency, you need only modify the values of a few resistors and capacitors. Third, you can upgrade the speed of any node on the network merely by removing the existing modem board and substituting a similar board that you've adjusted for the desired speed. You won't have to make any other hardware or software changes.

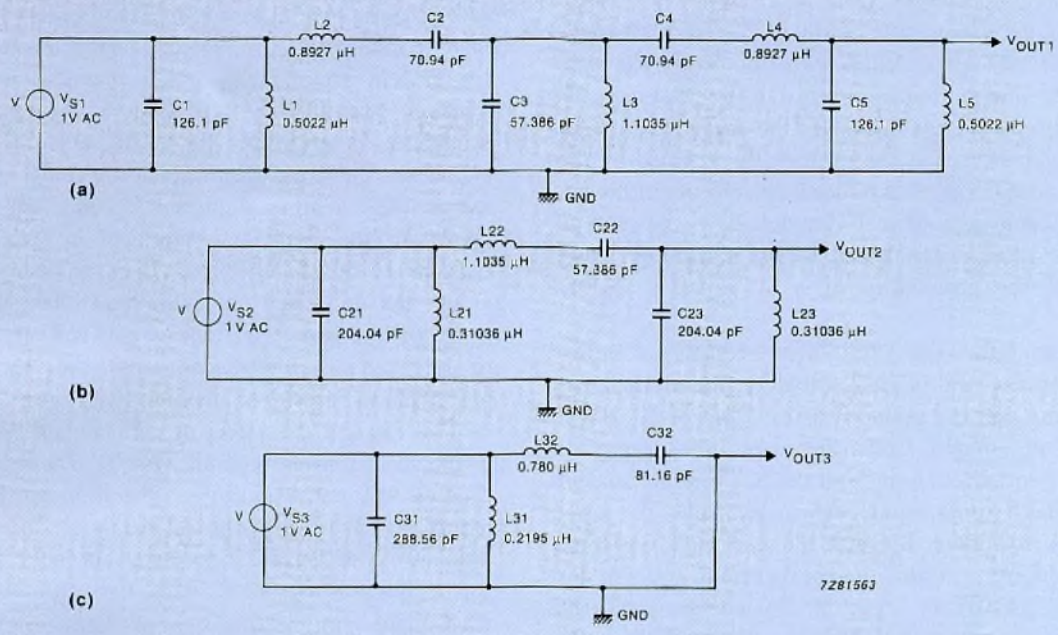


Fig.5 These Butterworth filters are tuned to 20 MHz. The 2-pole version (a) is often adequate for a frequency ratio of 1.666. For smaller ratios, you'll need the sharper cutoff of the 3-pole (b) or 5-pole (c) versions in order to eliminate the sidebands

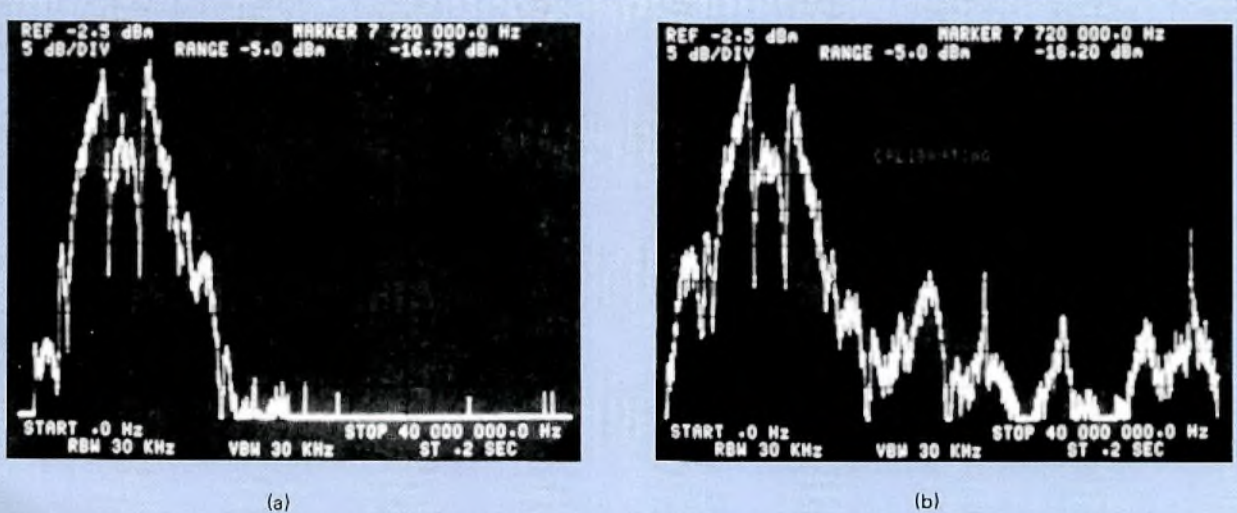


Fig.6 Sidebands have significant amplitude in the unfiltered output spectrum (a) of an NE5080 transmitting on a centre frequency of 7.7 MHz. Adding a filter (b) almost completely eliminates the sidebands

When you select the centre frequencies of the various channels in an FDM network, make sure that the higher channels avoid the harmonics of the lower channels. For example, the centre frequency of the first channel can be set to approximately 50 kHz, which will permit the channel to operate at a rate of 19.2 kbits/s. Because the frequency ratio (f_0/f_1) is 1.666, the band edges of this channel fall at 25 kHz and 75 kHz, so the total bandwidth is 50 kHz.

You can set the second channel's centre frequency at 455 kHz. The band edges of this channel fall at 250 kHz and 750 kHz, so the bandwidth is 500 kHz, which permits a data rate of approximately 192 kbits/s. You can centre the third channel at 5 MHz, yielding a data rate of approximately 2 Mbits/s, and the fourth channel at 21 MHz, yielding a data rate of about 8 Mbits/s. Careful filtering of the sidebands in each channel will ensure high data integrity and will improve the overall performance of the system.

Modifying the frequency ratio

Although the frequency ratio, f_0/f_1 of the NE5080 transmitter is internally set at 1.666, you can change the ratio by raising the lower frequency (f_0) or by lowering the upper frequency (f_1). As a result, the main lobe of the spectrum is narrower, and the bandwidth occupied by the channel is reduced. There's a tradeoff to consider, however. The reduced bandwidth of each channel allows the cable to accommodate more channels but results in a poorer noise margin; thus, the probability of a bit error is slightly increased.

The technique for raising the lower frequency is shown in Fig.7. When the data input is a logic 1, the input line is held at 5 V through the pullup resistor, R_{PU}, and the two diodes are reverse-biased. Under these conditions, capacitor C_0 is charged and discharged from the IC's internal current sources. When the data input goes to a logic 0, the input voltage drops to almost 0 V and the two diodes become forward biased. As a result, the total current available for charging and discharging capacitor C_0 increases, and the output frequency of the current-controlled oscillator falls.

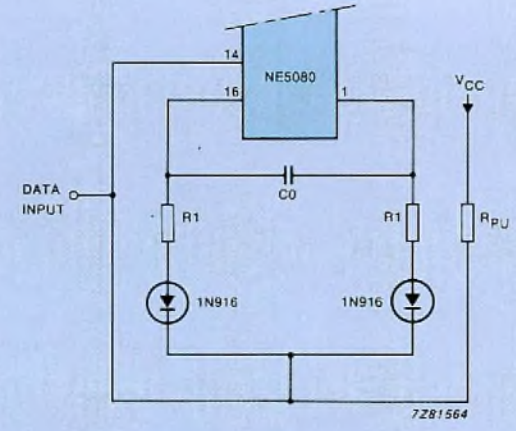


Fig.7 Capacitor C_0 determines the centre frequency of the NE5080. You can modify the frequency ratio by adding external components to raise the lower frequency or lower the upper frequency

The value of the two matched resistors (R_1) determines the amount of additional current available, and thus the f_0/f_1 ratio. It's essential that a close match be maintained between the two resistors to avoid excessive distortion at the FSK output. In selecting diodes for this application, consider their switching speed and capacitance; the 1N916 is fast and has a capacitance of only 2 pF, but even faster diodes with lower capacitance (such as the FD777) are available.

In making any modifications to Fig.7's circuit you'll have to take into account the stability of the ratio for a specific value of R_1 over a wide range of centre frequencies. It's evident from Fig.8 that a channel's deviation ratio remains constant for a fixed value of R_1 over a wide range of values for capacitor C_0. Note, however, that if you reduce the deviation from the centre frequency, you'll also reduce the maximum data rate for that channel. Likewise, increasing the frequency ratio will increase the possible data rates, but at the cost of extra bandwidth. If you reduce the frequency ratio, you'll also have to increase the Q factor of the receiver tank circuit so that the main lobe of the resonant circuit becomes narrower, thus corresponding to the main lobe of the modified transmitter spectrum.

You can see the effect of reducing the frequency ratio in the spectrum photographs (Fig.9). The main lobe grows progressively narrower, and so the filter must have a sharp cutoff to ensure that the sidebands are attenuated by at least 60 dB with respect to the main lobe. You'll need to use a Butterworth filter with five or more poles, or a Chebyshev or ripple filter that provides even sharper cutoff than the Butterworth type does.

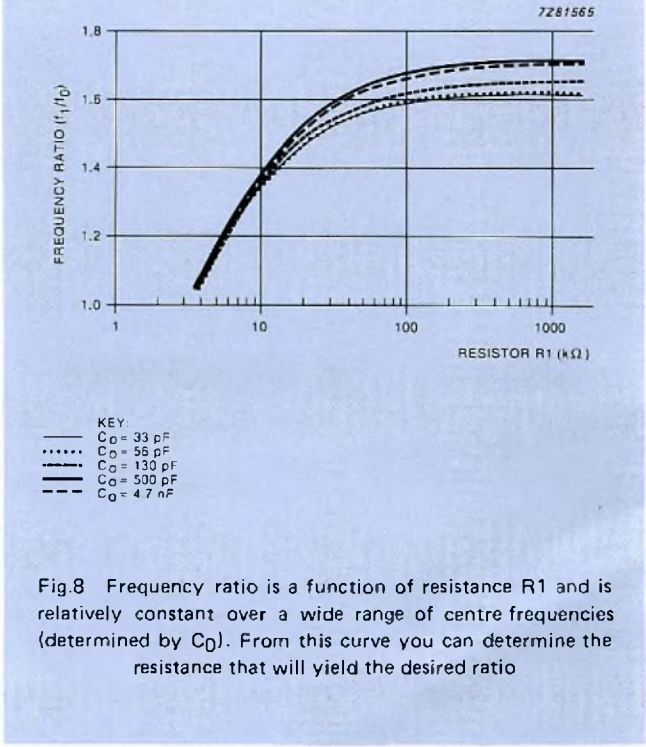
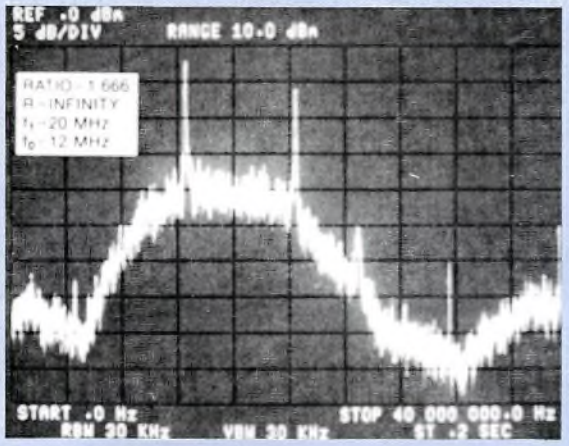


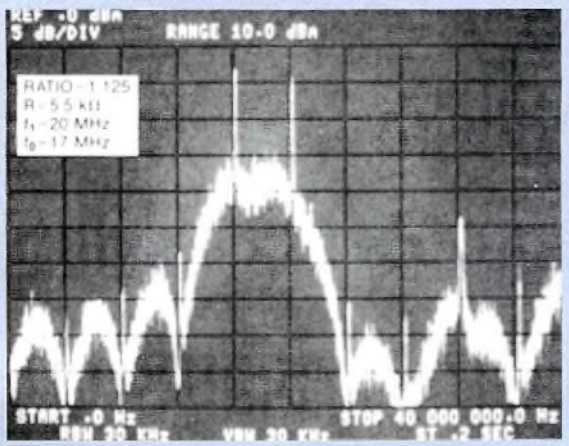
Fig.8 Frequency ratio is a function of resistance R1 and is relatively constant over a wide range of centre frequencies (determined by C_0). From this curve you can determine the resistance that will yield the desired ratio

If you use a 20 kΩ resistor in the circuit shown in Fig.7, you'll get a frequency ratio of 1.5, as the curve in Fig.8 shows. This ratio allows you to use a 30 MHz cable to accommodate six channels instead of four. If you reduce the ratio even further (for example, to 1.125), the same total bandwidth can accommodate many more channels.



(a)

(b)



(c)

Fig.9 The main lobe of the resonant circuit narrows as the frequency ratio is reduced. These photos show the effect of reducing the frequency ratio from the standard 1.666 (a) to 1.5 (b), and then to 1.125 (c)

A hybrid coil provides full-duplex capability

It's possible to make even more efficient use of cable resources. So far, all the applications discussed have required two cables for full-duplex communication (simultaneous transmission and reception by a given channel). However, full-duplex communication is possible over a single coaxial cable by adding a hybrid coil (Fig.10). The hybrid coil consists of 15 turns of 0.5 mm or 0.4 mm bifilar windings on a powdered-iron toroid core.

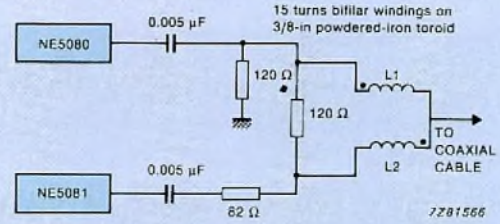


Fig.10 A hybrid coil permits full-duplex operation over a single coaxial cable. The back-EMFs induced in the hybrid windings cancel both the local transmitter signal at the receiver input and the received signal at the transmitter output, so that the signals do not interact

The sinusoidal signal from the NE5080 transmitter enters the hybrid at the dotted terminal of winding L_1. Because of the mutual inductance of the windings, the transmitter signal induces an equal and opposite signal in winding L_2, which cancels the transmitter signal that reaches the receiver through the 120 Ω resistor. Similarly, received signals entering the dotted terminal of winding L_2 create an equal and opposite signal in winding L_1. Hence, the incoming signal goes directly to the NE5081 receiver without interacting with the transmitted signal. The resistances shown in the schematic yield an effective termination resistance of 75 Ω.

The bit-error rate is the measure of data integrity within any data-communications network, so you should include a test of this parameter in your design procedures. A typical method of testing bit-error rate is to compare the bit stream applied directly to a bit-error-rate tester with the same bit stream that has passed through a modem link (Fig.11).

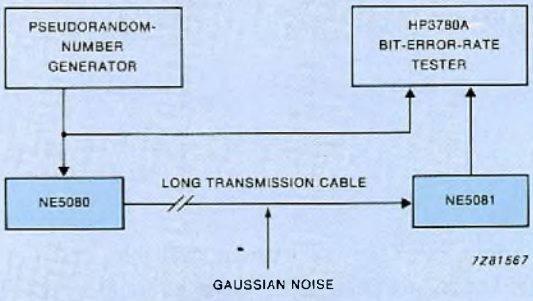


Fig.11 To determine a link's error rate – which is a function of its S/N ratio – you can use an error–rate tester to compare the bits sent with the bits received over the link, or you can examine the eye pattern at pin 8 of the NE5081 receiver

There's another quick and easy way to evaluate the performance of the link, a method that doesn't require a bit-error-rate tester. Simply connect the pseudorandom-number generator, the transmitter, the cable, and the receiver, to establish a data link carrying a pseudorandom bit stream. Then connect an oscilloscope to the receiver at pin 8, from which you can obtain an "eye" pattern (Fig.12). If the eye pattern looks clean, you can be fairly certain that the system is relatively noise- and error-free. A fuzzy pattern with small openings indicates excessive noise, which would probably lead to data errors.

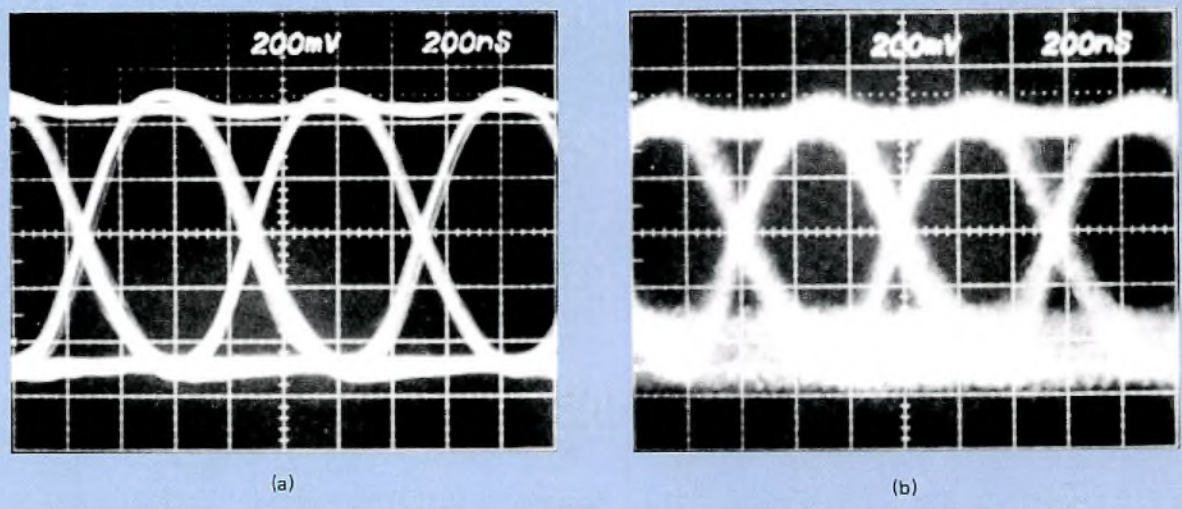


Fig.12 A clean eye pattern (a) indicates low noise. The horizontal width of the eye is a function of timing jitter; the vertical height is a function of the noise received. The fuzzy trace and small opening in (b) indicate excessive noise and an unacceptable high bit-error rate

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ACKNOWLEDGEMENT

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Multiple-step stress testing proves the reliability of solid aluminium capacitors

EVERT DEKKER and HELFRIED SCHMICKL

The technology of solid aluminium (SAL) electrolytic capacitors is backed by several decades of user experience. Because of their well-earned reputation for reliability, long-life and resistance to temperature extremes, they have secured a large share of the professional and industrial capacitor market. In comparison with more expensive tantalum capacitors their only disadvantage was that they were bulkier. This has been eliminated by new developments in aluminium etching (incorporated in our new 123 series) resulting in SALs which are half their previous size. This makes them comparable to tantalum capacitors of the same CV product. Moreover, the foil winding technique used in the 123 series promises SAL capacitors with CV products previously the exclusive domain of wet electrolytics.

Testing of solid aluminium capacitors has exposed no failure mechanisms. (A failure mechanism, as defined by IEC publication 271, is a physical, chemical or other process which ultimately results in failure). Wet aluminium electrolytic and solid tantalum capacitors, however, both display inherent failure mechanisms.

Determination and assessment of reliability in new components such as the 123-series capacitors is a time-consuming process when using conventional testing methods. Instead we use a technique of evaluating the useful life of components by applying a series of simultaneous stress tests, and increasing the levels of stress in stages to induce failure. This process, known as *multiple-step stress testing*, can achieve in weeks, results that would normally take months, or even years, of standard life-tests. To prove the validity of this form of testing, the results obtained from endurance tests of the earlier 121 series were compared with the results of multiple-step stress testing of components in this same series.

SOLID ALUMINIUM ELECTROLYTIC CAPACITORS

Solid aluminium electrolytics have no known inherent wear-out failure mechanisms; their use can increase overall system reliability. In addition, their electrical and thermal characteristics remain constant throughout a very long life. These characteristics are far superior to those of wet aluminium electrolytics and are comparable, indeed in many respects superior, to those of tantalums, see Table 1. A brief description of the construction of the 123-series capacitors is given in the panel on page 141.

Failure mechanisms

Tantalum, wet aluminium and SAL electrolytic capacitors have been available long enough for complete endurance tests to have been carried out. The failure mechanisms (where they exist) of each type have also been documented.

Field crystallization of the essentially amorphous tantalum oxide dielectric is the basic failure mechanism of solid tantalum capacitors (Ref.1). The growth of these higher conductivity oxide crystals during operation of the capacitors causes an increase in leakage current. The capacitor eventually short-circuits, and, since crystalline growth is primarily dependent on applied voltage, high voltage capacitors are more susceptible to failure. The effect of field crystallization can be minimized by using high-purity tantalum to reduce the number of crystallization nucleation sites (an impurity in the crystal grid).

For wet aluminium electrolytic capacitors, the failure mechanism is a gradual drying out of the electrolyte, reducing capacitance and increasing impedance until, eventually, the capacitor goes open-circuit.

TABLE 1
Comparison of electrolytic capacitor characteristics

	wet aluminium (Ta replacement types)	solid tantalum		solid aluminium	
		axial leads	radial leads	axial leads	radial leads
temperature range (°C)	−40 to +85	−55 to +125	−55 to +85/125*	−80 to +250	−80 to +175
effect of temp. derating on life and failure rate	significant	significant	significant	negligible	negligible
voltage derating above 85 °C	not usable	2/3 of U_R	2/3 of U_R	not required	40 V types only
effect of voltage derating on life and failure rate	negligible	significant	significant	slight	slight
inrush current	large	small	small	small	small
allowed reverse DC – level – duration	 1 V brief	 5% of U_R brief	 5% of U_R brief	 30% of U_R continuous	 30% of U_R continuous
guaranteed life (h) – at 85 °C – at 125 °C – at 155 °C	 2000 not usable not usable	 2000 2000 not usable	 1000/2000* not usable/2000 not usable	 8000 8000 5000	 5000 2000 2000
failure mechanism	drying out of electrolyte	field crystallization	field crystallization	none known	none known
failure rate (U_R, 125 °C, 0 Ω/V, 60% confidence)	10^{-6}/h (85 °C) ⩽2 kh	10^{-5}/h ⩽2 kh	3×10^{-5}/h ⩽2 kh	10^{-7}/h ⩽20 kh	5×10^{-7}/h ⩽10 kh

* depending on series.

The testing of SAL electrolytics has so far failed to reveal any failure mechanism, either short-circuit or open-circuit (Ref.2). In fact, these capacitors can actually improve with age, as the leakage current decreases during the life of the capacitor. This is in total contrast to both wet aluminium and solid tantalum electrolytics, which have intrinsic failure mechanisms that ultimately result in the breakdown of the capacitor.

Multiple-step stress testing of SALs

The first consideration for setting up a multiple-step stress test for a SAL electrolytic capacitor is to determine which stress factors affect the lifetime. For each stress factor, the maximum rated operational value (S_R), and the physical upper limit (S_U, above which the component will be subject to new failure mechanisms rather than failure due to accelerated ageing), are to be specified. The difference between S_U and S_R for each factor is divided into 10 equal steps.

For the duration of the first test period, the capacitors are subjected to all stress factors at their absolute maximum rated operational value, after which they are checked for conformity to specification. Each stress parameter is then increased to $S_R + 0{,}1\,(S_U - S_R)$ for the next test period and the capacitors are checked at the end. For the third period, the stress parameters are raised to $S_R + 0{,}2\,(S_U - S_R)$, and so on until they are tested at their physical upper limit (S_U) for the duration of the last (the eleventh) test period.

It is important that all stress parameters are increased at the same time for each step in order to cause an exponential increase of the test severity (see Appendix) and hence an exponential reduction of the lifetime. This is illustrated in the typical Weibull diagram of Fig.1.

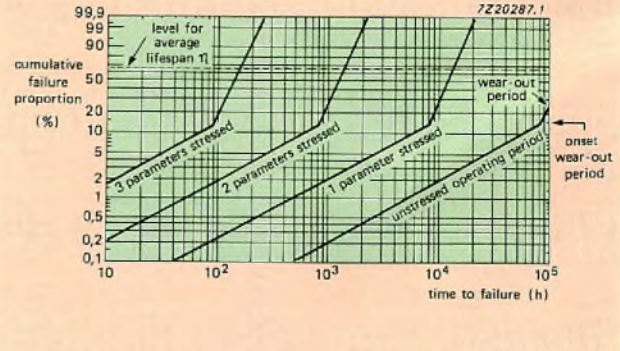


Fig.1 Typical Weibull diagram showing how lifetime decreases as the number of stressed parameters increases

TABLE 2
Electrical data for SAL electrolytics under test

	nominal capacitance	U_R	max. RMS ripple current at T_{amb} = 125 °C	max. leakage current at U_R after 1 min.	max. tan δ	max. ESR	max. impedance at 100 kHz
device [1] 2222 121 13331	330 μF	6,3 V	430 mA	150 μA	0,18	1,1	0,2
device [2] 2222 123 13102	1000 μF	6,3 V	760 mA	440 μA	0,18	0,36	0,2

When the life expectancy of a component is known from years of conventional life testing, that of a new component of like technology can be predicted accurately and quickly by multiple-step stress testing both components and comparing the results obtained. Additionally, any inherent defects in the new component design which could cause failure mechanisms can be identified early in development and eliminated.

To establish the life expectancy of the 123-series SAL, we tested a 1000 μF 123-series capacitor and a 330 μF 121-series capacitor according to the multiple-step stress test; the 121-series capacitor, for which there are 15 years of life-test results, being the reference. Both capacitors have the same case, the dimensions of which are shown in Fig.2. Electrical data for both samples are given in Table 2. The stress factors for the test are based on the supposed physical limits of the 123-series, and the full test schedule and measured results are given in Table 3.

The measured results show stability of all parameters with no trend toward deterioration. There were no complete failures and no evidence of a failure mechanism in either the 121-series reference capacitor or the 123-series test capacitor.

Two conclusions can be drawn from these results: the new 123-series capacitors are as reliable as the earlier and larger 121-series; and the supposed physical limits of the 123-series are not the real limits. In particular, a much higher ripple voltage can be superimposed on the DC voltage. Furthermore, the ripple current can be higher. This has been verified by a subsequent thermal and electrical analysis (Ref.3). Finally, the leakage current (specified as a function of the CV product) is the same as for the 121-series capacitors. This has all been included in the new product specification.

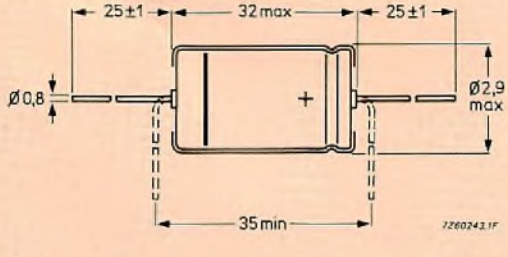


Fig.2 Case dimensions (mm) for the capacitors under test

Reliability and life expectancy of SAL electrolytic capacitors

Experience indicates that the stress parameters most likely to influence the reliability and useful life of SAL electrolytics are temperature and applied voltage. The results of the above tests on the 123-series capacitors show that it's permissible to go up to, and even exceed, the supposed limits of both these stress parameters without the capacitor failing. Therefore, it is reasonable to say that the true upper temperature limit for SAL electrolytic capacitors is above 175 °C. This is supported by field results taken at 250 °C (see Ref.10).

From the test results described here, and confirmed by simple endurance testing, at a temperature of 175 °C and a rated voltage (U_R) of 6,3 V, these capacitors have a predicted useful life greater than 2000 hours. Moreover, life expectancy falls exponentially with operating temperature (see Appendix). For example, at 125 °C and 6,3 V, the life expectancy is more than 50000 hours. Figure 3 shows the results on parameter values after 45000 hours endurance testing, comparing again the 121 and 123 ranges.

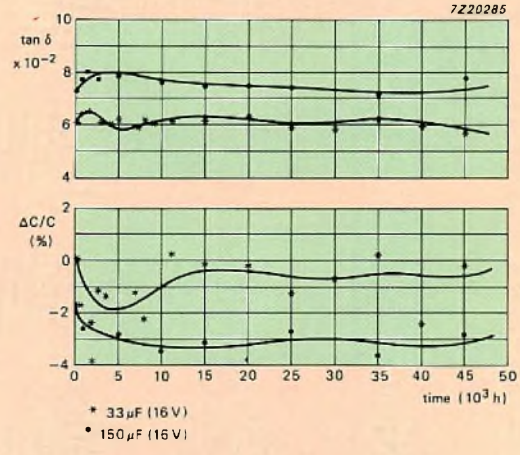


Fig.3 Results of endurance testing at 125 °C and rated voltage, for 121 series (33 μF/16 V) and 123 series (150 μF/16 V) capacitors.

TABLE 3

Multiple-step stress test results for axial solid aluminium capacitors

stress step		1	2	3	4	5	6	7	8	9	10	11	physical
time (h)		24	24	24	72	24	24	24	24	72	24	24	limit
stress factor	*device*[1])												
DC voltage (V)	[1]	6,3	6,8	7,3	7,8	8,3	8,8	9,3	9,8	10,3	10,8	11,3	28,8[2])
	[2]	6,3	6,8	7,3	7,8	8,3	8,8	9,3	9,8	10,3	10,8	11,3	11,5
ambient temperature (°C)	[1]	125	130	135	140	145	150	155	160	165	170	175	175[3])
	[2]	125	130	135	140	145	150	155	160	165	170	175	175
RMS ripple current (mA)	[1][6])	342	380	420	1240	1340	1440	1500	1500	1500	1525	1540	1370[4])
	[2]	940	1040	1140	1240	1340	1440	1540	1640	1740	1840	1940	1290
RMS ripple voltage (V)	[1]	1,5	1,65	1,8	5,24	5,61	5,9	6,0	6,0	6,0	6,0	6,0	12,4[5])
	[2]	1,24	1,34	1,47	1,65	1,77	1,9	2,1	2,1	2,2	2,38	2,56	0,1
peak ripple voltage (V)	[1]	2,1	2,3	2,5	7,4	7,9	8,3	8,5	8,5	8,5	8,5	8,5	17,5[5])
	[2]	1,8	1,9	2,1	2,3	2,5	2,7	3,0	3,0	3,1	3,4	3,6	0,2
sum of DC voltage + peak ripple voltage as multiplier on U_R	[1]	1,3	1,4	1,6	2,4	2,6	2,7	2,8	3,0	3,0	3.1	3,1	4,6
	[2]	1,3	1,4	1,5	1,6	1,7	1,8	2,0	2,1	2,1	2,3	2,4	1,8
measured results[7])													specification[8])
leakage current as multiplier on CV	[1]	0,006	0,006	0,005	0,004	0,003	0,003	0,002	0,002	0,001	0,002	0,002	
	[2]	0,025	0,024	0,024	0,017	0,017	0,015	0,013	0,012	0,012	0,018	0,018	0,1
ΔC as a % of initial capacitance at 100 kHz	[1]	−2,2	−2,7	−3,1	−7,3	−9,6	−11,0	−13,6	−14,9	−16,1	−15,7	−15,3	
	[2]	−2,2	−2,9	−3,3	−4,2	−4,4	−4,9	−5,2	−5,5	−5,7	−5,9	−6,2	10%
tan δ (dissipation factor as a % at 100 Hz)	[1]	4,4	4,5	4,8	6,6	9,8	9,0	9,9	9,5	10,0	9,8	8,6	
	[2]	17,2	17,2	17,0	16,8	18,6	18,2	18,5	18,4	18,2	18,6	16,5	22%
impedance at 100 kHz (mΩ)	[1]	93	94	91	83	87	82	84	86	90	92	80	
	[2]	150	147	141	132	138	136	139	134	137	141	128	240

[1]) Device type [1] – Axial lead solid aluminium capacitor series 121, 330 μF, U_R = 6,3 V.
Device type [2] – Axial lead solid aluminium capacitor series 123, 1000 μF, U_R = 6,3 V.

[2]) Voltage limit is 60% of the anode foil forming voltage.

[3]) Temperature limit: at 175 °C discolouration of the tin and insulation occurs, the capacitors can electrically go beyond this temperature.

[4]) Ripple current limit is derived from an inner temperature 20 °C higher than ambient.

[5]) Peak ripple voltage limit is the difference between limit value and applied value of the voltage.

[6]) For the 330 μF reference capacitor (device [1]), the ripple current setting was hampered by power supply limitations.

[7]) Average of six samples.

[8]) Specified requirements after 125 °C endurance tests. Wider margins apply for higher temperatures.

At 85 °C, the useful life of SAL electrolytics is so extended that it is no longer feasible to predict it. This has been confirmed by years of observation of solid aluminium electrolytic capacitors in the telecommunications industry, thus justifying the extremely low failure rate of 1×10^{-9}/h (1 FITS) specified for these components.

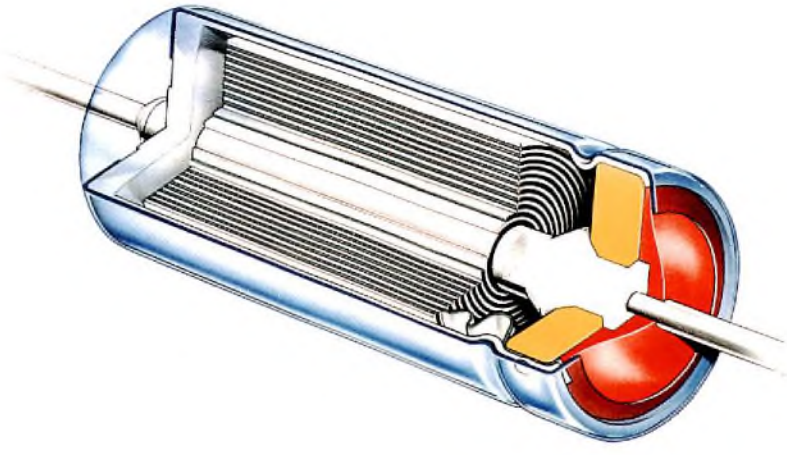
On the basis of these qualities, our SAL electrolytic capacitors have established an excellent reputation in aerospace electronics, in professional electronics, and recently, because of their resistance to high temperature and to polarity reversal, in automotive electronics.

SOLID ALUMINIUM ELECTROLYTIC CAPACITOR CONSTRUCTION

The 123-series SAL electrolytic capacitors are a development of the earlier bulkier 121-series. The higher CV product density of the 123-series is achieved through intensified etching of the aluminium-foil electrodes.

The internal structure of a SAL electrolytic has a capacitive element with five layers. Layer 1, the anode foil, is high-purity (99,99%) aluminium about 100 μm thick. It's layer 2, however, that determines the capacitance and other electrical characteristics. This layer is formed by the deep etching and oxidization of the aluminium foil of layer 1, the oxide lining the etched pits to form the dielectric. Layer 3 consists of low-resistivity manganese dioxide held in a glass-fibre web that also acts as a spacer. Layers 4 and 5 are similar to layers 1 and 2; layer 5 is the cathode aluminium foil, and layer 4 formed by the etching and oxidization of this foil (though less deeply etched than layer 2).

The cut-away view of the 123-series capacitor shows the basic construction. The anode and cathode foils, together with the glass-fibre web, are wound on a solid aluminium pin to which the anode foil is welded. The cathode foil connection is made by an aluminium strip welded at both ends; experience has shown that welding gives better reliability than any other form of connection.



Cut-away view of a 123-series solid aluminium electrolytic capacitor

APPENDIX

Theoretical considerations of multiple-step stress testing

From the number of failures in a given number of components over a period (under stated conditions of stress e.g. voltage, current, temperature), it is possible to gain data on the overall picture of reliability. Each component possesses its own reliability characteristic and some of the basic expressions for interpreting the data are as follows:

$R(t) = e^{-\lambda t}$ = reliability – the fraction of components that have not yet failed after elapsed time t (assuming constant failure rate λ).*

$F(t) = 1 - e^{-\lambda t}$ = cumulative failure proportion – the fraction of components that have failed after elapsed time t (again assuming constant λ).

It then follows that $R(t) = 1 - F(t)$.

Bathtub curve

A plot of reliability R and failure rate λ, against time t, results in a graph showing typical curves for the component (see Fig.A). The failure rate curve, known as a "bathtub" curve due to its shape, is in three distinct parts:

(a) early failures ($\lambda(t)$ decreasing)

(b) incidental failures ($\lambda(t)$ constant)

(c) wear-out failures ($\lambda(t)$ increasing).

The times at which early failures (caused largely by manufacturing faults) end, and wear-out begins are important as it is from these points that the typical useful life, and hence lifetime, are deduced and defined.

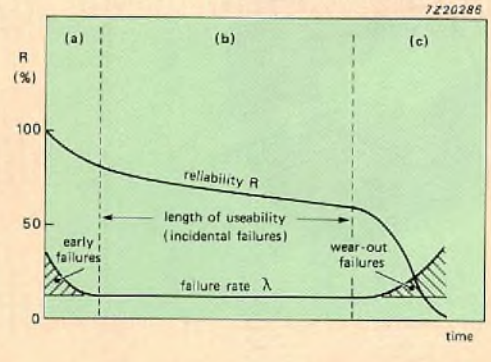


Fig.A Typical graph of component failure rate and reliability against time

* failure rate = the average number of component failures per component-operating hour (1/h). For high reliability applications, λ will be in the region 10^{-6}/h to 10^{-9}/h.

The period for which λ is constant (Fig.A, section (b)) is the operational section in which manufacturers' data on failure rates will apply and on which system designers will base calculations for overall system reliability. The overall reliability and failure rate in an electronic system are calculated from:

$$R_S = R_1 \cdot R_2 \cdot R_3 \ldots R_n$$

and

$$\lambda_S = \lambda_1 + \lambda_2 + \lambda_3 \ldots + \lambda_n.$$

From this, it is clear that the overall reliability and failure rate in an electronic system are most affected by the weakest single element present. Similarly, the overall reliability decreases as the number of elements in the system increases.

Weibull distribution functions

Although the name "bathtub curve" is pictorially descriptive, it's unsuitable for the exact determination of $\lambda(t)$, R(t), and the points at which the useful life starts and ends. A more accurate prediction can be made by applying the Weibull distribution function:

$$R(t) = e^{-(t/n)^{\beta}}$$

where β = Weibull "shape parameter", and $n = 1/\lambda$ is the average lifetime (in hours), defined as the length of time for which 1/e (36,7%) components are operational (for constant λ).

The Weibull function is transformed into a linear equation by taking the logarithm twice, thus:

$$\ln \ln (1/R(t)) = \beta \ln t - \beta \ln n.$$

A plot on Weibull probability paper with ln ln (1/R(t)) as ordinate, and ln (t) as abscissa, shows that the Weibull equation transforms the bath-tub curve into three straight lines of differing (β) gradients as shown in Fig.B.

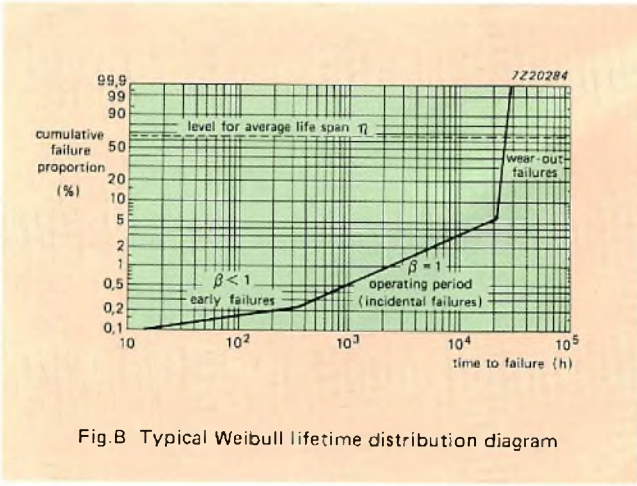


Fig.B Typical Weibull lifetime distribution diagram

With this Weibull lifetime distribution diagram, it is possible to accurately define the end of the period of early failures, and the onset of wear failures (from sections (a) to (b), and (b) to (c) respectively on the bathtub curve), by the two points of intersection of these three lines. Each section is defined as follows:

(a) $\beta < 1$ – early failure period ($\lambda(t)$ decreases)

(b) $\beta = 1$ – constant failure period ($\lambda(t)$ constant)

(c) $\beta > 1$ – wear-out failure period ($\lambda(t)$ increases).

In fact, it is not necessary to have $\beta = 1$ in section (b) as this occurs only when failures are determined totally by stochastic processes.

Arrhenius' law and accelerating factors

The reaction of most chemical processes increases exponentially as the temperature is increased. Temperature is therefore an accelerating factor. So if the operating temperature of a component under test is increased above its normal rating, the onset of wear failures occurs earlier and the average lifetime is shortened. Conversely, at a lower temperature, the lifetime can be expected to be longer.

The temperature influence can be described by making use of the analogy between the reaction constant of a process and the failure rate of a component, as both are defined as the decrease per unit time of the concentration of a species divided by the actual concentration of the species. Thus, from Arrhenius' law, the expression for the failure rate λ, at absolute temperature T, can be written:

$$\lambda(T) = Ae^{-B/kT}$$

where A and B are constants, k = Boltzmann constant and T = absolute temperature. The constant B is normally referred to as the activation energy of the process.

The information available cannot always be reduced to comply with Arrhenius' law, when the temperature is the only accelerating factor. The equations that describe test results fall apart even more when additional stress factors are involved. Parameters that reduce lifetime are, for example, vibration, humidity, pressure and, in particular for capacitors, the applied voltage.

Denoting the applied voltage by V, and general stress parameters by S_1, S_2, etc., the following equations apply (n, G, A_1, A_2, B_1, B_2, etc. are constants):

For integrated circuits the Eyring law (Ref.4):

$$\lambda(T,S) = A \exp.((-B+B_1S_1+B_2S_2+\ldots)/kT);$$

For ceramic capacitors (Ref.5):

$$\lambda(T,V) = A_1 \cdot V^n \exp.(-B/kT);$$

For solid tantalum capacitors (Ref.6):

$$\lambda(T,V) = A_2 \cdot V^n \cdot 2^{B3(T-B4)};$$

and for capacitors in general (Ref.7):

$$\lambda(T,V) = (A_3 \cdot V^n + A_4) \exp.(B_5T^G);$$

and

$$\lambda(T,V,S) = (A_5S_5+A_6S_6\ldots)\lambda(T,V).$$

Apparently, an adequate model is lacking to describe the failure mechanisms during actual testing. Probably a degradation process controlled by the Arrhenius activation energy is "polluted" by other unknowns that are applied to the components under test. These could be caused by the test process itself (e.g. handling, thermal gradients, influence by surrounding components, atmosphere). They could also derive from the production and handling history of the components, by which they may have already experienced some non-identified stresses before actual testing starts.

From all equations, however, it is clear that there is an exponential increase of failure rate with temperature (therefore the average lifetime decreases exponentially), and an acceleration of the increase by applied voltage and other stresses.

Thus the ageing process of a component or system is accelerated by the maximum possible amount if it is loaded with all known stress factors simultaneously (multiple-stress testing). The absolute level of the applied stress factors also influences the accelerated ageing process, so the lifetime period can be adjusted through both the number of, and the level of, the stress parameters applied.

This technique of applying several stress factors, and increasing the level of stress applied in stages, to accelerate the lifetime is known as *multiple-step stress testing*. The acceleration (or "time-lapse") factor can be calculated from the relationship between lifetimes under normal and under stressed conditions. This relationship is determined particularly accurately with the aid of the Weibull distribution graph.

However, to obtain correctly predicted results, the following conditions must be complied with:

1. The failure characteristic must remain the same.
2. The normal wear curve must be parallel to the accelerated wear curve on the Weibull graph. This is, in fact, verification of condition 1.
3. The failure analysis of all test batches must display the same fault mechanism.
4. The upper limits of the stepped stress parameters must not exceed conditions outside the operating area of the component (in the forbidden area, for example, boiling point) as this could induce new chemical processes that produce different fault mechanisms (Fig.C).

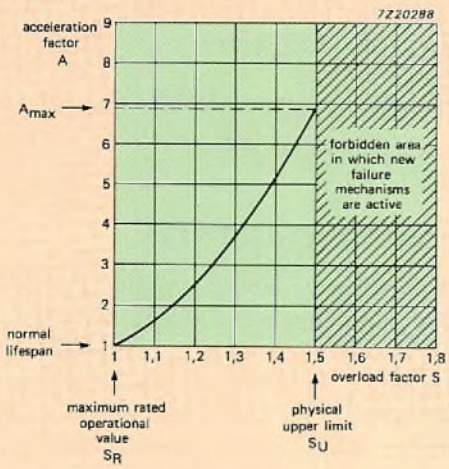


Fig.C The permissible overload area.

If conditions 1 to 4 are fulfilled, then the acceleration factor will be as follows:

$$\text{acceleration factor} = t_{ON}/t_{OA}$$

where t_{ON} = time of onset of wearout failures under normal conditions, and t_{OA} = time of onset of wearout failures under accelerated conditions. One disadvantage of this method is that the accuracy of prediction decreases as the acceleration factor increases.

To describe the above conditions in terms of the Weibull function, both the shape factor β and the point in time at which the first failure occurs must be independent of temperature (Ref.8). This is also necessary though not sufficient, in order to be able to apply Arrhenius' law. If the shape factor β in the operating period is not equal to 1, then the pre-exponential acceleration factor is difficult to identify. This is what happens for solid tantalum capacitors (Ref.9).

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Third-generation decoding ICs for CD players

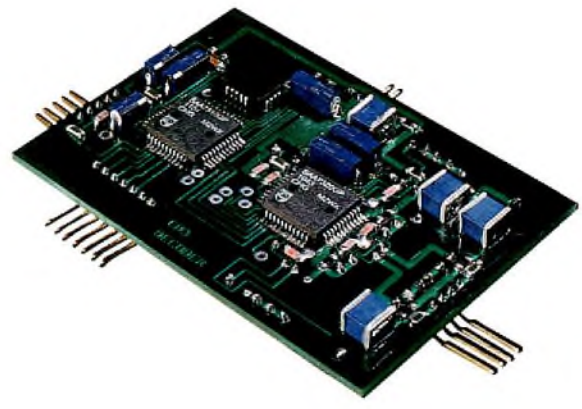
RAINER FINCK and DAVE SLOWGROVE

Since its introduction in 1984, our second-generation four-chip set for CD decoders (Ref.1) has won the acclaim of player manufacturers and listeners alike for the quality of the sound it can reproduce – for example, see Refs 2 to 6. With this chip-set, the first to make full use of the error-correction capability of the CD system's Cross-Interleaved Reed-Solomon code, and the first to discriminate between the errors on a disc (for more reliable corrections), sound reproduction reached levels of fidelity that even surpassed those available with our first-generation circuits. Indeed, the decoding system shown in Fig.1 has become the industry standard. What's more, the extremely high level of integration used has reduced the size of the decoding circuitry and the number of peripheral components in a CD player significantly, simplifying board design and lowering assembly costs.

Still higher levels of integration are used in a new CMOS chip set introduced in this article. Intended for use in players in the middle and low end of the market (for example, in audio stacks and portables), this third-generation chip set comprises just two ICs which together perform all the decoding functions and D/A conversion required in a CD player.

Besides retaining many of the benefits of our second-generation circuits, the new chip set:

- operates from a single (+5 V) supply
- consumes less power
- has an extended operating temperature range (–40 °C to +85 °C)
- has improved facilities for concealing data lost as a result of large external knocks, as commonly encountered by car players and portables. So there is less muting of the audio and hence fewer audible clicks.
- has a software-controlled inhibit of the data interpolation circuitry for CDI and CD ROM applications.
- has improved digital filtering (128 taps instead of 120).



Laboratory model of a complete Compact Disc decoder using the SAA7310 and SAA7320 CMOS circuits

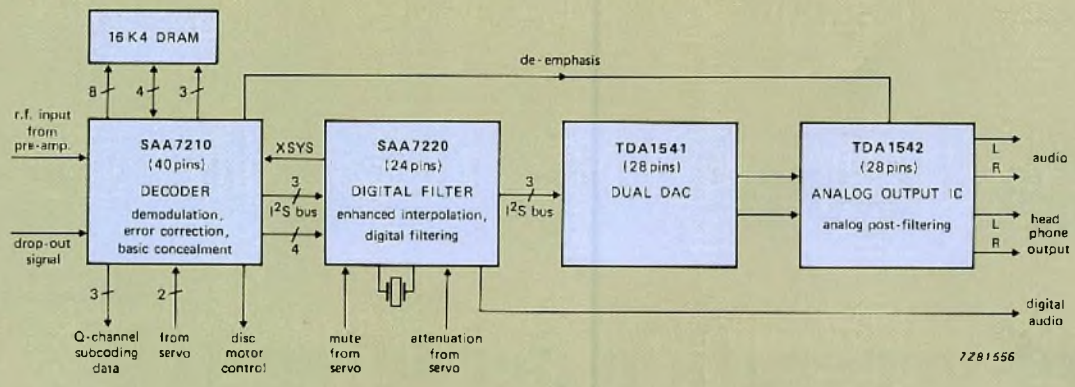


Fig.1 Second-generation CD decoder

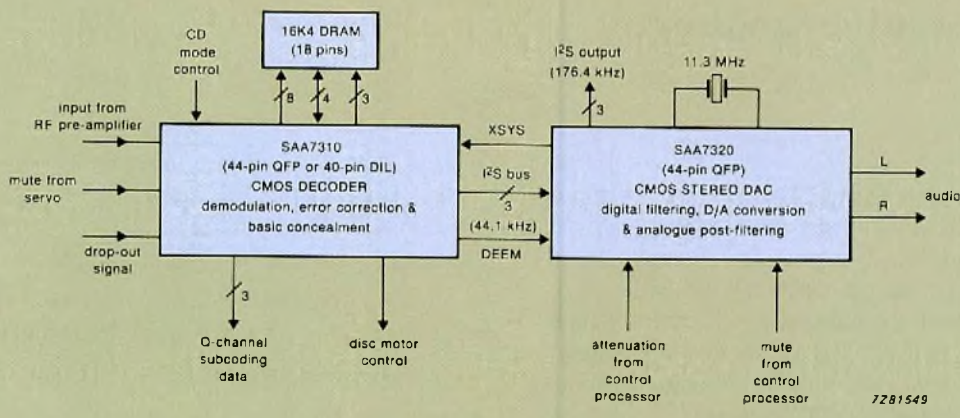


Fig.2 Third-generation CD decoder

Figure 2 shows the new decoding circuits. The SAA7310 (Ref.7) performs the same functions as the SAA7210 – demodulation, full error-correction, and basic interpolation of uncorrectable audio samples. In addition, it controls the new data interpolation inhibit and the data concealment procedure.

The SAA7320 (Ref.8) includes a phase-linear digital low-pass filter, two new-design high-linearity DACs and operational amplifiers for analogue post-filtering. The level of integration in the SAA7320 is the highest of any current CD circuit. Like the SAA7220 digital filter IC, the SAA7320 has facilities for attenuating the audio output by 12 dB, which can be used at the start of 'fast forward/fast reverse' commands and a search for a track, for example. In addition, the soft mute facility which can be used when moving to another track and during pauses is retained.

The data format between the SAA7310 and SAA7320 is according to the I²S (inter-IC sound) specification[1]), which allows combinations of second and third-generation ICs (such as the SAA7310, SAA7220 and TDA1541) to be used in a player, giving the player manufacturer maximum design flexibility, see Table 1.

Figure 3 is the circuit diagram of a complete CD decoder using the SAA7310 and SAA7320. As the figure shows, the circuit which includes on-chip stereo low-pass filtering requires only a few passive peripheral components.

[1]) I²S communication is a communication format for digital audio. The I²S bus is a 3-line bus comprising: clock, serial data line, and a control line used to select left and right channel words (Ref.9).

TABLE 1
Decoding ICs for CD players

	de-modulation	error correction	interpolation basic	interpolation enhanced	digital filtering	D/A conversion	application
1st generation	SAA7010	SAA7020	SAA7000	–	SAA7030	2 x TDA1540 plus discrete analogue low-pass filter	home players
2nd generation	SAA7210			SAA7220		TDA1541 plus TDA1542	home and full-performance players
3rd generation	SAA7310			–	SAA7320		portable and home players
2nd & 3rd generation	SAA7310			SAA7220		TDA1541 plus TDA1542	full-performance players

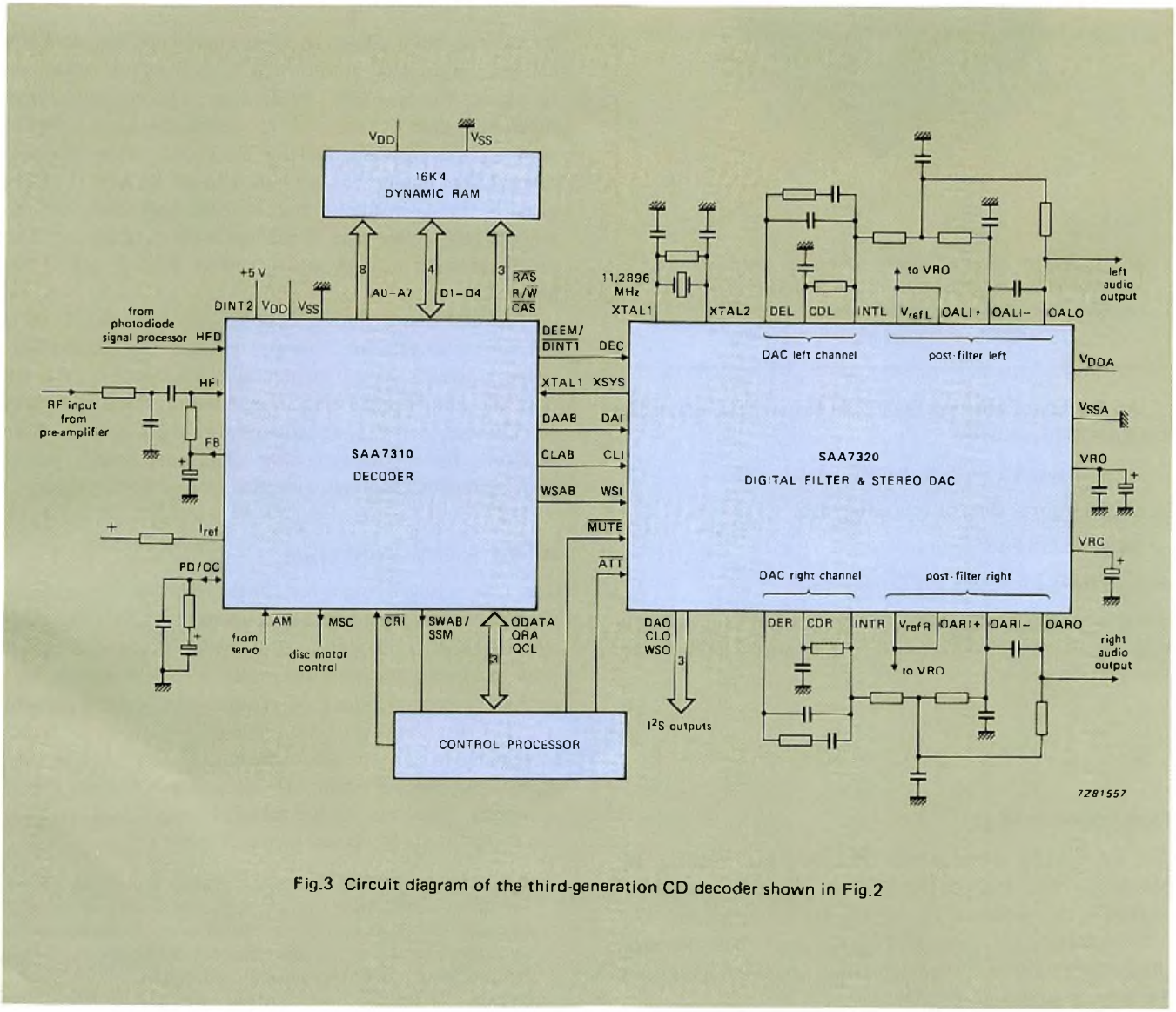


Fig.3 Circuit diagram of the third-generation CD decoder shown in Fig.2

SAA7310 DECODER

The SAA7310 performs all the functions necessary to decode an amplified and filtered version of the EFM (eight-to-fourteen modulated) data stream generated by the pick-up of a CD player. The SAA7310 is available in a 44-pin quad flatpack, or in a 40-pin DIL package suitable for upgrading an SAA7210-based decoding system. The pinning of the DIL version makes the SAA7310 virtually a drop-in replacement for the SAA7210.

The SAA7310, heart of a full-performance CD decoder, is available in a 44-pin quad flat-pack and in a 40-pin DIL package, the latter being pin-compatible with the SAA7210 to simplify upgrading of existing designs

All the features of the SAA7210 decoder are retained in the SAA7310, namely:

- fully integrated VCO in the demodulator PLL
- efficient processing of subcoding data
- adaptive error-correction
- operates with a large FIFO memory.

These and the new muting facility and selector for non-digital-audio applications such as CDI and CD ROM are summarized below.

Demodulator PLL

The SAA7310's demodulator PLL requires virtually no peripheral components. The VCO is a fully-integrated RC oscillator; it requires no peripheral components. The differential filtering circuitry of the PLL uses a self-balancing charge pump design that requires only one filter comprising just three components (Fig.4).

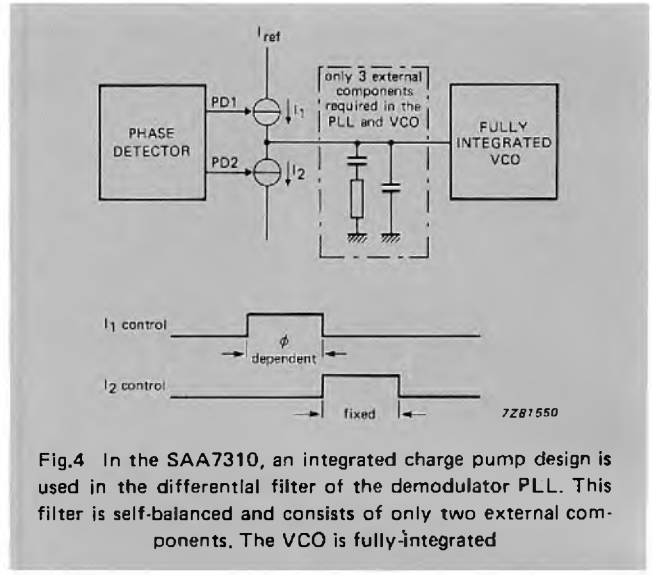


Fig.4 In the SAA7310, an integrated charge pump design is used in the differential filter of the demodulator PLL. This filter is self-balanced and consists of only two external components. The VCO is fully-integrated

Efficient processing of subcoding data

As well as the audio data, Q-channel subcoding data[1]) is derived continually in the SAA7310 from the incoming RF signal. The time spent by the control processor handling subcoding data is reduced by a handshaking protocol between the processor and the SAA7310. When the processor wants data, a request is sent to the SAA7310 which, when a full Q-channel frame is ready, acknowledges the request and enables the Q-channel serial data output. The processor sends a clock signal to shift the data out of the SAA7310.

The first negative-going edge of the clock signal resets the acknowledge signal thereby releasing the request line. If the processor doesn't require all the subcoding data, say only the number of a track (contained in the first sixteen bits), it can reset the request line after these bits have been received, thereby disabling the Q-channel output of the SAA7310 which resumes collecting new subcoding data.

Adaptive error-correction

The CD system's Cross-Interleaved Reed-Solomon Code (CIRC) enables up to four erroneous symbols[2]) (in a 32-symbol block) to be corrected if the CIRC decoder is given prior information about the position of the errors. This type of correction, where the position of an error is known, is called an erasure correction. When the positions of errors are unknown, up to two erroneous symbols can be corrected. A decoder with the maximum error-correction capability (like that of the SAA7310 and the SAA7210) can make the corrections shown in Table 2.

[1]) Besides the audio information recorded on a compact disc, information representing track numbers and playing times is recorded so that tracks can be played in any desired sequence and titles and elapsed playing times etc. can be displayed. This information is termed Q-channel subcoding data.

[2]) 14 bits.

TABLE 2
Error-correction possibilities of the CIRC decoder of the SAA7310

		erasure corrections				
		e=0	e=1	e=2	e=3	e=4
t corrections*	t=0	•	•	•	•	•
	t=1	•	•	•		
	t=2	•				

* detect and correct an error.

For optimum error-correction, only the following corrections of Table 2 are relevant:

t = 2 look for and correct two errors, positions unknown

e = 1, t = 1 make one erasure correction, and look for and correct one additional error

e = 2, t = 1 make two erasure corrections, and look for and correct one additional error

e = 3 make three erasure corrections

e = 4 make four erasure corrections.

In the SAA7310, adaptive error-correction discriminates between the errors found on a compact disc. This discrimination:

- enables more corrections to be made (for example, longer burst errors)
- makes the corrections more reliable.

As shown in Fig.5, these improvements are made by using additional error flags generated by the EFM decoder (using the bit run-length criteria to flag symbols likely to be in error) and by using multi-level error flags generated by the C1 and C2 corrector[1]).

With the error flags, several error-correction strategies are available, the strategy chosen depending on the type and number of error flags which are set by the defects on a disc.

Extensive testing with discs has shown that error-correction is significantly improved by using multi-level flags to signal symbols in error, three flags (two bits) being sufficient:

- hard error-flag (most reliable flag)
- medium error-flag
- soft error-flag (least reliable flag).

A no-error flag is indicated by setting both bits to zero.

[1]) Two Reed-Solomon codes C1 and C2 are used to correct erroneous audio samples, C1 being used to correct random errors in adjoining symbols, C2 to correct burst errors.

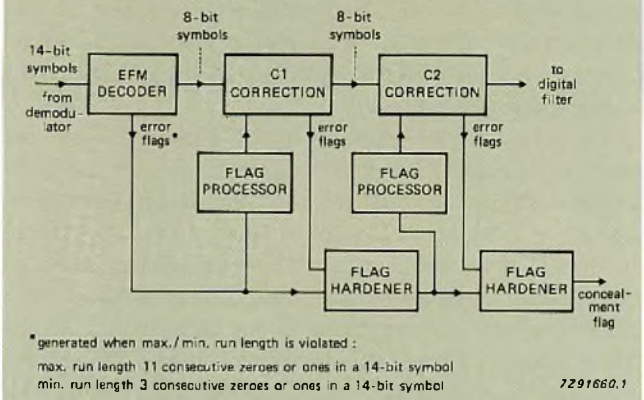


Fig.5 Symbols that violate the run length criterion are flagged 'likely to be in error' by the EFM (Eight-to-Fourteen Modulation) decoder. With this advance information, the C1 corrector can correct up to four erasures (symbols in error whose position is known). Although shown here as two correctors, C1 and C2 is a single corrector using sequential processing with the FIFO memory as buffer for de-interleaving 32-symbol blocks of data

With these flags, the best correction strategy is selected by a flag processor, see Fig.5. For example, when two symbols in a block of thirty-two are flagged with soft error-flags, it is best to attempt a t = 2 correction (rather than an e = 1 and a t = 1, or an e = 2, t = 1 correction). When two symbols are flagged with hard flags, it is usually better to attempt an e = 2 correction and to look for and correct another symbol in error with the remaining t = 1 capability. After a correction, the input flags are compared with the new flags produced by the corrector to update (harden) the flags for the next stage of processing. Flag hardening progressively improves the reliability of all flags, so that very reliable e = 3 and e = 4 corrections can also be made.

All the error-corrections routes (about 60) for CD audio applications are programmed in ROM in the SAA7310.

Large FIFO memory for car players and portables

Part of the memory used to de-interleave the error-correction data is used as a FIFO memory to remove variations in the demodulated-data rate due to, amongst other causes, the g-forces on car players and portables. In addition, this FIFO can be used to increase the allowable mechanical tolerances for the disc drive of a player. The SAA7310 is designed to operate with a 16K4 DRAM which can accommodate up to 64 frames. The FIFO is also used to store the increased number of error flags used in adaptive error-correction.

Additional mute

This feature was not incorporated in the SAA7210. Designed to improve the performance of car players and portables in particular, it enables the SAA7310 to reconstruct missing data when tracking is lost as a result of a severe knock to a player.

Should track loss occur, taking the 'additional mute' pin ($\overline{AM}$) of the SAA7310 LOW forces the data stream LOW before it enters the FIFO memory, that is, *before de-interleaving*, and the data is flagged as being in error. In general, the lost data can be reconstructed by the error-corrector or (after de-interleaving) by the interpolation circuitry, thus preventing any audible clicks in the audio signal. In the SAA7210, only a hard mute is available for use during track loss. This hard mute is retained on the SAA7310 ($\overline{MUTE}$ pin), but is not required in designs using the SAA7320 digital filter.

The additional mute circuitry can be controlled as the player designer wishes. One way is to use the $\overline{TL}$ track loss signal generated by our TDA5708 photodiode signal processor.

Digital audio, CDI and CD ROM selector

Another new feature of the SAA7310 is a mode selector (DINT2 pin) which prevents data being interpolated when the SAA7310 is used in CDI and CD ROM applications. For CD audio equipment, the DINT2 pin should be tied HIGH so that any uncorrectable audio samples from the error-corrector are reconstructed by a hold and interpolation circuit (see Fig.6), For CDI and CD ROM equipment, the DINT2 pin should be tied LOW to inhibit this concealment circuit.

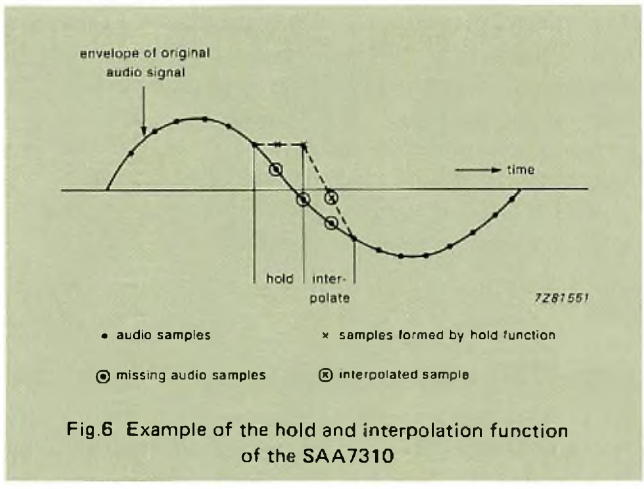


Fig.6 Example of the hold and interpolation function of the SAA7310

SAA7320 DIGITAL FILTER AND DAC

The type of low-pass filter in a CD player influences the quality of the sound reproduced significantly. To create true high-fidelity sound with no detectable colouration, our chip sets for Compact Disc players have, from the outset, used predominantly digital (FIR) filtering with four-times oversampling followed by low-order analogue filtering. The benefits of this approach are well-known:

- linear phase response (at a much lower cost than with all-analogue designs, and with no component adjustments necessary)
- flat pass-band
- optimum roll-off for excellent impulse response
- low noise
- long-term stability (no component ageing effects)
- smaller filter than discrete analogue designs.

In the SAA7320, there is again a four-times digital oversampling filter, now followed by another oversampling filter and a noise shaper which simplify the design of the digital-to-analogue converter – now a 1-bit converter operating at 11.2 MHz and providing 16-bit resolution, see Fig.7 and Ref.10.

The SAA7320 is available in a 44-pin quad flatpack.

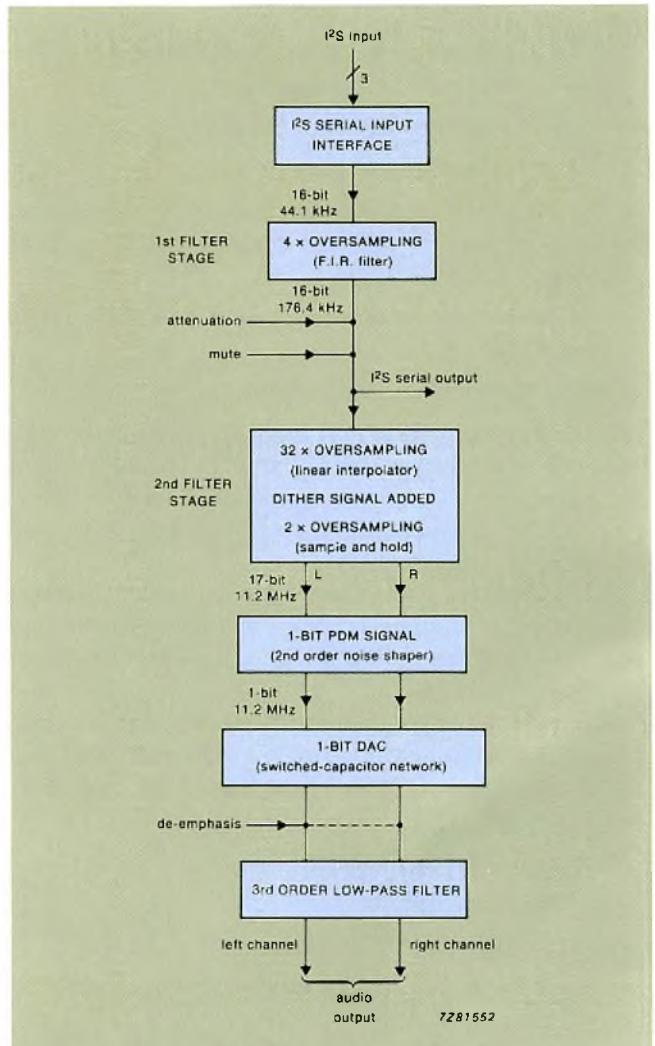


Fig.7 Data flow of the SAA7320

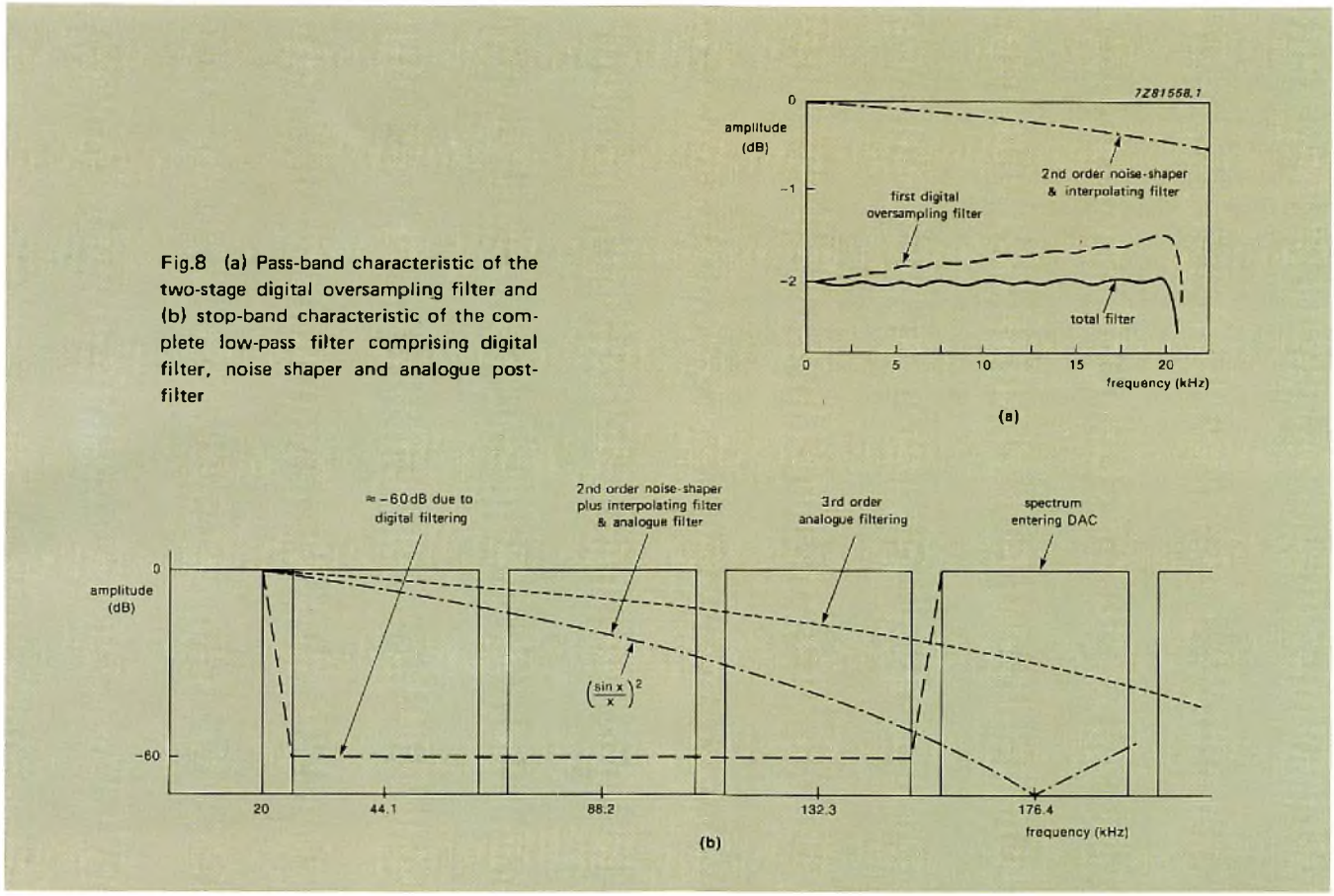


Fig.8 (a) Pass-band characteristic of the two-stage digital oversampling filter and (b) stop-band characteristic of the complete low-pass filter comprising digital filter, noise shaper and analogue post-filter

Digital oversampling filter

The 44.1 kHz sample rate of the 16-bit PCM input words is quadrupled in the first oversampling section of the SAA7320 – a finite impulse response (FIR) low-pass filter with 128 taps (eight more than the digital filter of the SAA7220). The filter has a 20 kHz bandwidth, a pass-band ripple of ±0.02 dB and a stop-band rejection of 60 dB above 24 kHz.

The second oversampling section is an interpolating filter based on an adder structure. The sample rate is increased another 64 times by the combination of a linear interpolator (32-times oversampling) and a sample-and-hold circuit (2-times oversampling). An internally generated out-of-band dither signal is used to prevent audible idling patterns of the noise shaper (see next section) at low input signal levels. The amplitude increases because of the dither signal, so an extra bit is needed, making the word length at the output of the linear interpolator 17 bits.

The frequency response of the digital filter contains compensation for the $(\sin x/x)^2$ roll-off due to the interpolator (–0.38 dB at 20 kHz) plus the roll-off due to the analogue post-filter (Butterworth characteristic). Figure 8 shows the contribution of each part of the filter to the complete frequency response. Owing to the digital oversampling filter, the analogue post-filter can be of simple design. Furthermore, because the SAA7320 has an I^2S output, it's possible to use only the four-times oversampling filter, leaving the design of the remainder of the player completely open.

Noise shaping and D/A conversion

In linear PCM audio systems such as Compact Disc Digital Audio, the noise spectrum of the digital audio samples can be reshaped to decrease the in-band quantization noise when the signal bandwidth is less than half the sampling rate, f_S (Ref.11). In the SAA7320, the use of oversampling, which spreads the noise over a wide bandwidth, and of noise shaping techniques lowers the in-band quantization noise to that equivalent to 16-bit resolution, from a 1-bit DAC operating at a sample rate of $256f_S$ (11.28 MHz).

The input signal for such a DAC is derived by passing the 17-bit oversampled and digitally-filtered PCM words through a quantizer which reduces the word length to 1 bit. A loop-filter that feeds the quantization error back to the input of the quantizer reshapes the 1-bit quantization noise, leaving only a small portion of this noise in the audio band.

As can be seen in Fig.9(a), the circuit of the 1-bit DAC is very simple. Its function is to modulate a DC voltage with the 1-bit data stream and the circuit is implemented using a switched-capacitor network. Figure 9(b) shows the timing diagram. During the first half of the sample period,

either C1 is charged by drawing a unity charge out of the summing node of the output opamp, or capacitor C2 is discharged by pushing a unity charge into the opamp. During the second half, C1 and C2 are discharged and charged respectively.

The linearity of this type of 1-bit DAC can be better than that of conventional DACs. This is partly because there is only one converter stage instead of many different stages (as in weighted-resistor or R/2 ladder designs, for example), so there is less dependence on component tolerances. In addition, this type of 1-bit converter doesn't suffer from the LSB inaccuracies of conventional 16-bit DACs, the main component of distortion at low signal levels, see Fig.10.

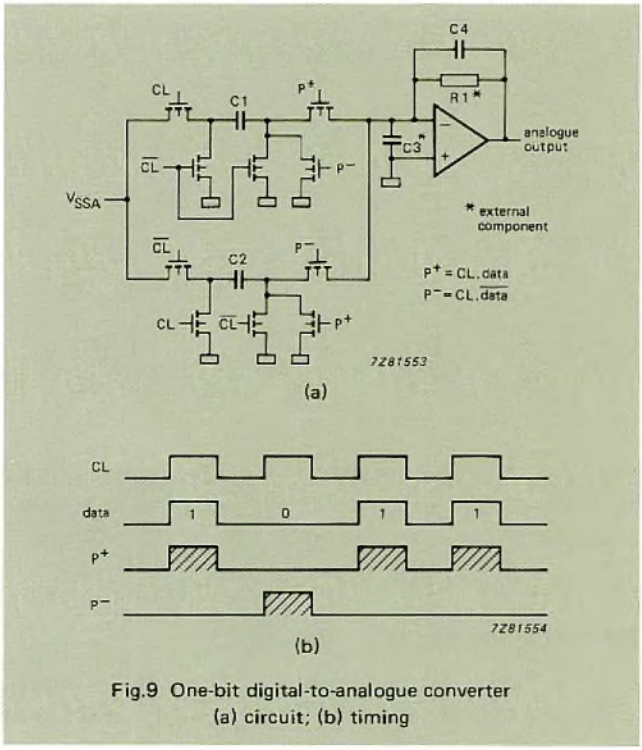


Fig.9 One-bit digital-to-analogue converter (a) circuit; (b) timing

Analogue post-filtering

In the SAA7320, two operational amplifiers per channel perform analogue post-filtering and current-to-voltage conversion. One opamp is used for the switched-capacitor network (and for some post-filtering), the other is used only for second-order post filtering. The main features of these opamps are high DC gain (90 dB), high slew rate (30 V/μs), and a low 1/f noise figure of −104.1 dB (relative to 0.7 V_{rms}).

For a flat frequency response, the filter section should be a third-order low-pass filter with a −3 dB cut-off at 60 kHz.

There is also a de-emphasis control input in the integrator stage so that the roll-off of the first filter stage can be changed by switching in an extra (external) feedback network when required.

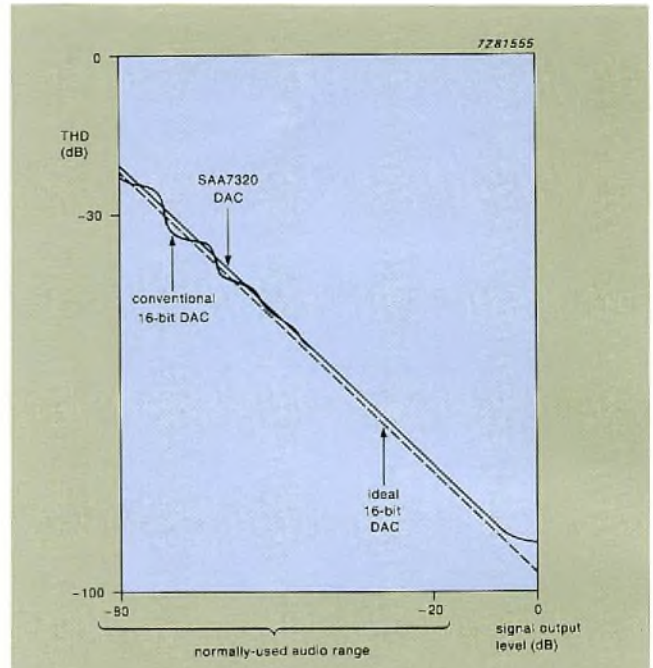


Fig.10 Superior linearity at low signal levels is one advantage of the SAA7320's 1-bit DAC over a conventional 16-bit DAC. In addition, a compact design allows two of the new DACs (two for stereo), the digital filter circuitry and the opamps of the analogue filter to the integrated on one chip

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Single-heterojunction GaAlAs – a new technology for infrared LEDs and optocouplers

MARIE CLAUDE BOISSY

Single-heterojunction GaAlAs technology was originally introduced to extend the range of visible LEDs, providing a brighter red than was obtainable from the usual GaAsP and (Zn- and O-doped) GaP types. We are the first to introduce this technology for infrared (IR) LEDs and optocoupler emitters which, until now, have been GaAs and GaAlAs homojunctions.

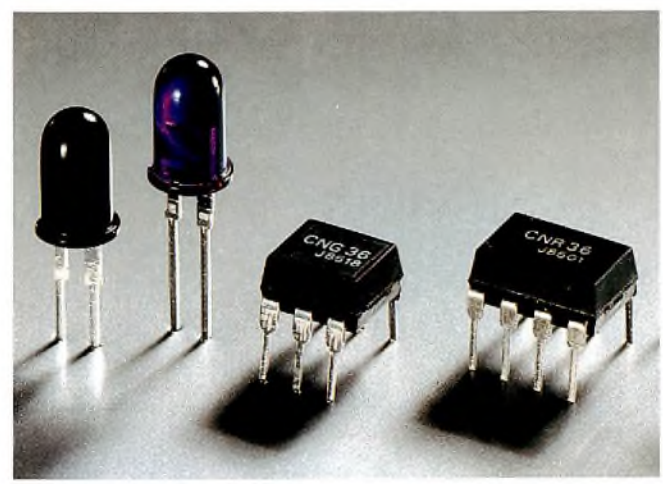
Generally, the forward current requirement for an optocoupler emitter is much lower than for an IR LED, the distance to the photoreceiver being considerably shorter. However, our new single-heterojunction GaAlAs IR diodes perform so well at both low and high forward currents that we can use the same emitter crystals in both IR LEDs and optocouplers. In comparison to GaAs and GaAlAs homojunctions, our new technology offers a few more advantages too:

- faster response and consequently higher operating speed
- more linear radiant intensity (I_e)/forward-current relation
- more stable operation (at low and very high currents)
- higher light output where it's needed – at low and high forward currents
- lower degeneration and better reliability.

The success of the new technology is best explained by considering its two aspects separately – the material and the structure.

GaAlAs – the ultimate semiconductor for IR LEDs and optocouplers

In recent years, GaAlAs has become one of the most well-known ternary compound-semiconductors used in optoelectronics. The reason is that its bandgap can be varied (by the Ga/Al ratio) to produce radiation at any desired wavelength between 650 and 900 nm, the visible red to near infrared range. With GaAlAs LEDs and optocoupler emitters, we've been able to choose the peak emitted wavelength to match the peak sensitivity of the photoreceiver, for a higher coupling efficiency.



By far the most popular photoreceivers are silicon photodiodes, photo-transistors and photo-ICs. They are high-speed receivers with a broad spectral response and well-developed technology (Si photoreceivers can be integrated, at low cost, with other circuit components to suit the application). However, their peak response is to 700-900 nm infrared radiation. So for any optical communication system using a Si photoreceiver (remote control television sets or optocouplers, for example), a GaAlAs source, tailored to operate at the receiver's peak sensitivity, produces a greater response in the receiver than any other source. At present we produce heterojunction emitters at two different emission wavelengths for the specific receivers used:

- 830 nm for coupling with general-purpose photodiodes and photo-transistors whose peak sensitivity is between 800 nm and 850 nm
- 740 nm for coupling with integrated photoreceivers whose peak sensitivity is between 700 nm and 750 nm.

For optocouplers with GaAlAs emitters, this means lower drive currents are possible than for those with GaAs emitters. Low enough that GaAlAs types can be driven directly from CMOS ICs.

Single-heterojunctions and homojunctions

Figure 1 shows the structure of a typical IR LED/optocoupler single-heterojunction emitter. The structure differs from a homojunction in that it has two epitaxial layers with different bandgaps:

- a tellurium-doped, n-type top injection layer – this has a 30% higher Al/Ga ratio than the bottom layer, resulting in a larger bandgap. This makes electron injection from the top to the bottom layer very efficient
- a zinc-doped, p-type bottom active layer – where the radiation originates. The aluminium content of this layer is chosen to yield the desired wavelength (the higher the aluminium content the larger the bandgap and the shorter the wavelength). As the photon energy equals the bandgap energy of the material, the larger bandgap injection layer is transparent to the emitted radiation.

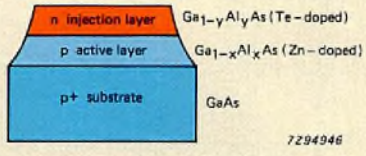


Fig.1 Schematic structure of single-heterojunction emitter

Unlike GaAs and GaAlAs homojunctions, single-heterojunction GaAlAs has an abrupt rather than a gradual p-n junction that is, moreover, between large and small bandgap layers. This results in a device which is inherently more stable and reliable than a homojunction. It provides high and constant injection efficiency over the whole range of drive currents and fewer non-radiative recombinations at the surface and in the space-charge region. This, in turn, gives a linear output-power/forward-current relation. Other technologies exhibit an efficiency peak at medium drive currents, but perform poorly at the low and high extremes of drive current.

A further advantage comes from doping with tellurium and zinc. Being respectively a shallow donor and a shallow acceptor, these give fast band-to-band radiative transitions. Competitors use silicon as both an n- and p-type dopant which, by contrast, produces deep donor and acceptor levels. Radiative recombinations are then due to slower pair transitions between deep levels, with a lower external quantum efficiency. Thus, our dopants are responsible for the high speed of our IR LEDs and optocouplers (50 ns switching time compared with 1 μs for homojunctions).

The fact that our heterojunction facilitates high speed at high currents is particularly important for IR LEDs which are usually driven by high pulsed forward currents in, for example, TV remote controls.

Fabrication

Fabrication is by a single-step liquid-phase epitaxy process on GaAs substrates. The substrates, held in large capacity graphite crucibles, are placed in a horizontal reactor and heated to about 850 °C in a hydrogen flow, to ensure temperature uniformity. Next, they're consecutively exposed to two melts, each consisting of Ga, GaAs, Al and the respective doping element (Zn for the first melt and Te for the second), while the temperature is gradually lowered.

The first melt comes into contact with the surface to form the p-type active layer. The melt is a saturated solution which when cooled, initiates lattice-matched crystallization, forming the first epitaxial layer. The active layer is allowed to grow to a thickness of about 20 μm. Later in the same cooling cycle, the second melt (with more aluminium added) similarly forms the n-type injection layer to a thickness of 10 μm. After completion of the epitaxy process, ohmic contacts are deposited and the wafers are sawn into discrete devices which are then securely bonded to lead frames.

Performance

Table 1 compares the performance of our single-heterojunction GaAlAs emitters with that of competitors' GaAs and GaAlAs homojunction emitters. The major advantage

of ours is a fast response, maximum emission being reached almost instantly after switch-on. Because of this, our single-heterojunction emitters can be used efficiently with very short duration pulses, in conjunction with very fast photosensors such as p-i-n photodiodes and complex photo-ICs. Homojunctions with Si doping, by contrast, never reach maximum efficiency if the current pulse duration is less than about $1 - 3\,\mu s$. Figure 2 shows the frequency response of a typical GaAlAs LED.

Measured at 20 mA, the luminous efficiency of the heterojunction IR LED is close to that of a standard Si-doped GaAs IR LED but, because of photon absorption in the GaAs substrate, only about half that of a Si-doped GaAlAs IR LED. However, this difference decreases significantly when the forward current is reduced from 20 mA to 2 mA. Indeed, the output-power/forward-current linearity of the heterojunction IR LED is far superior because there are fewer non-radiative recombinations at the surface and in the space-charge region than in Si-doped IR LEDs. This results in a higher efficiency under 0.5 mA, which is advantageous in optocouplers for CMOS-compatible applications.

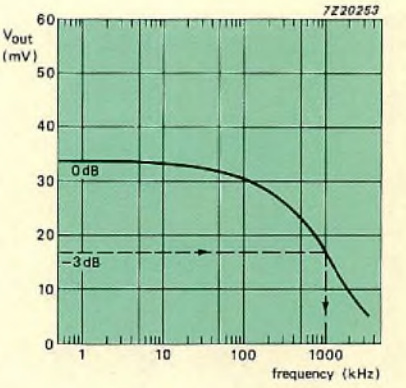


Fig.2 Frequency response of a typical GaAlAs IR LED (type CQW89A) as measured by a standard photoreceiver

Finally, as illustrated by the life tests (Figs 3 and 4), the reliability of GaAlAs heterojunction IR LEDs and optocoupler emitters is very high indeed. Even at 300 mA overstress, as required for British Telecom homologation, the stability is remarkable.

TABLE 1
Comparison of the three major technologies for IR LEDs and optocouplers emitters

	standard GaAs Si-doped	homojunction GaAlAs Si-doped	heterojunction GaAlAs Te & Zn-doped
response time (ns) at 20 mA	1000*	1000*	50
emission wavelength (nm)	930	880	740 or 830
efficiency (mW/A) at 20 mA	100**	150**	80
linearity	poor	poor	good
stability at low current	good	good	good
stability at high current	limited	limited	good

* increases at low current.
** decreases at low current and very high currents.

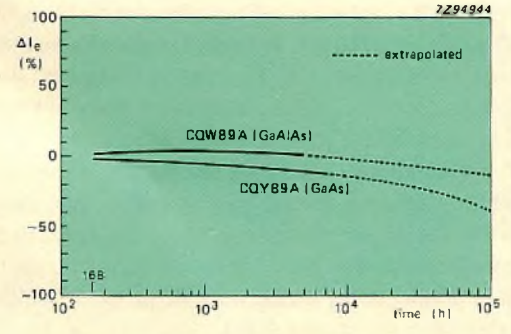


Fig.3 Variation of radiant intensity, ΔI_e, with time for typical GaAs and GaAlAs IR LEDs (respectively, 5 mm diameter CQY89A and CQW89A; I_F = 100 mA, T = 25 °C)

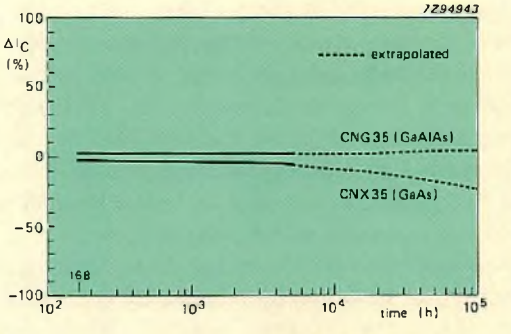


Fig.4 Variation of output current, ΔI_C, with time for typical GaAs and GaAlAs emitter optocouplers (respectively, CNX35 and CNG35; I_F = 10 mA, V_{CE} = 0,4 V)

Highly-accelerated humidity testing of CMOS ICs

WOLFRAM NACHBAUER

The effect of humid environments on complete, encapsulated integrated circuits is of critical importance in many applications. Moreover, defects in design or workmanship that result in increased susceptibility to humidity might lead to deterioration of performance or useful life. These aspects of structural integrity are traditionally explored by the 85 °C, 85% RH (relative humidity) test with appropriate bias. Test duration is usually 1000 h, which explores not only the hermeticity of the package, but also the effectiveness of the passivation, and the resistance to corrosion of internal bond pads and lead frame, as well as that of the external pins. Temperature-humidity-bias (THB) testing is of especial importance in the case of CMOS devices whose low dissipation and consequent small internal temperature rise in operation does not tend to reduce internal package humidity, as is the case with bipolar devices.

Improvements in plastic encapsulants, lead tinning and die passivation have greatly reduced the susceptibility of modern ICs to the effects of humidity. Where process or design problems do occur, the 1000 h duration of the 85/85 THB test prevents any early corrective action that would adequately protect the running production of both IC manufacturer and user. In fact, with state-of-the-art plastic-encapsulated CMOS ICs, THB testing has to be carried out for up to a year if useful numbers of failures are to be observed. A shorter test is clearly desirable.

One obvious route to an accelerated test is to increase temperature, since then failure mechanisms could be expected to accelerate according to Arrhenius' Law. However, there is a limit to the increase in temperature useable in practice set by the onset of new failure mechanisms like plastic degradation. Finally, humidity cannot be maintained at temperatures above 100 °C unless pressure is also increased, consequently, these accelerated tests are all performed in an autoclave ('pressure cooker').

Here we detail the results of investigations into several combinations of temperature and pressure that establish acceleration factors for the various failure mechanisms likely to be encountered. One set of test conditions that satisfies all the requirements for monitoring IC product quality has been selected and standardized, enabling us to detect incipient problems early, and to react quickly enough to avoid hazarding both our own and our customer's production.

TEST CONDITIONS AND FAILURE CRITERIA

Test conditions

In order to gather sufficient data for the accurate determination of acceleration factors, as well as to gain experience of various tests in practice, a number of sets of test conditions were selected for evaluation. These are listed together with the standard 85/85 THB test in Table 1. The 132,9/85 test has now been adopted as our standard test for the routine quality control of CMOS ICs.

Since CMOS ICs were used exclusively as test vehicles, dissipation during tests was negligible, and correction for humidity change between the package and chip unnecessary.

Failure definitions

All ICs were tested to the family specification both before and after humidity testing. Failures were divided into two categories:

- parametric failures, such as supply current leakage due to activated parasitic transistors or source-drain leakage in n-channels. Note, the failure criterion for source-drain leakage was not that given in the family specification, but a more severe in-house level.
- complete failures due to corrosion or excessive leakage.

Note that P410B, the encapsulating plastic used for the test vehicles, is no longer used in our IC production; it has been superseded by Nitto HC10-2, and Sumitomo 1100 HS; both more hermetic grades.

ACCELERATION FACTOR

Test results

Cumulative results from testing at 85/85 (THB) and 132,9/85 are given in Tables 2 and 3. The results given in Table 2 were obtained with HEF4000B CMOS logic IC test vehicles taken from the same diffusion and assembly batches; applied bias was 15 V. The results given include partial failures (failures as defined by the in-house test specification, but not outside the IC family specification).

Test vehicles for Table 3 were HCMOS ICs; applied bias was 6 V.

Analysis

Results from both tests are plotted onto the Weibull chart of Fig.1 (see Appendix 1) where the different HCMOS test durations are allowed for. Acceleration factors between 85/85 THB and 132,9/85 testing derived from Fig.1 are given for both HEF4000B and HCMOS ICs in Table 4 for 1%, 5%, 10% and 50% cumulative failure percentages.

Although the mean acceleration factor between the two test conditions appears to be about 30, comparisons between tests, even using the same type of test vehicles, proved difficult since different failure mechanisms were accelerated to a different degree. Accordingly, the behaviour of corrosion and parametric failures has been analysed separately.

TABLE 1
Standard THB and accelerated humidity test conditions

test conditions (°C/RH%)	pressure (atm)*	test chamber temperature (°C)	water vapour chamber temp. (°C)	relative humidity (%)	test equipment	notes
85/85	0	85	–	85	Brabender	Stand. MIL, IEC
108,7/85	0,19	108,7	104,0	85	Hirayama	
132,9/85	1,55	132,9	127,5	85	Hirayama	(Now standard at Philips)
151,1/85	3,25	151,1	145,2	85	Hirayama	

* kPa x 10^{-5}.

TABLE 2
Cumulative failures, HEF4000B (CMOS) series, plastic DIL

test conditions (°C/RH%/V)	sample size	test duration			
		170 h	500 h	1000 h	2000 h
85/85/15	670	0,6%	1,8%	4,6%	7,3%
		60 h	90 h		
132,9/85/15	620	7,1%	12,3%		

TABLE 3
Cumulative failures, HCMOS series, plastic DIL

test conditions (°C/RH%/V)	sample size	test duration					
		170 h	500 h	1000 h	2000 h	4000 h	
85/85/6	818	0,12%	0,37%	0,75%	1,4%	2,8%	
		60 h	120 h	180 h	240 h	300 h	360 h
132,9/85/6	1136	0,88%	2,9%	1,96%	3,5%	3,1%	6,5%

TABLE 4
Acceleration factors between 85/85 and 132,9/85

test vehicle	bias (V)	acceleration factor A at failure level			
		1%	5%	10%	50%
HEF4000 series	15	17	28	34	55
HCMOS series	6	22	27	31	45

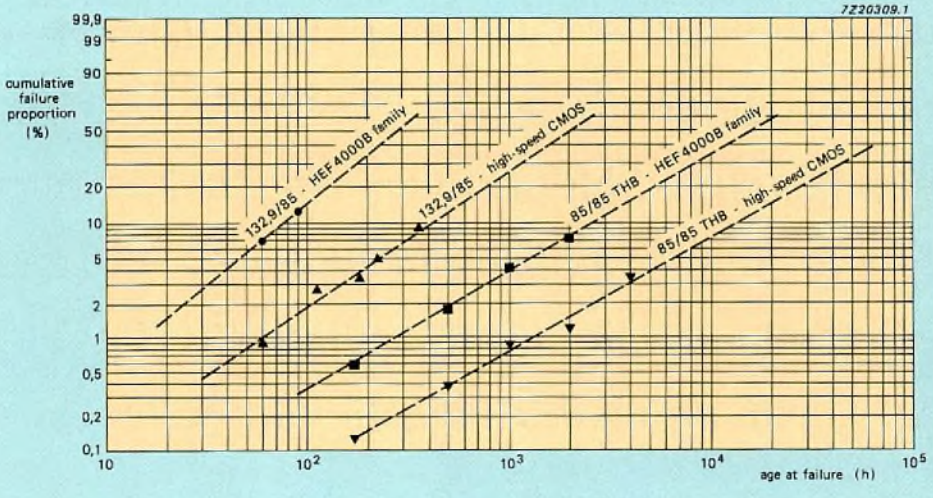


Fig.1 Weibull plot comparing 85/85 (THB) and 132,9/85 test results for both CMOS and HMOS devices in the older P410B plastic packages

TABLE 5
Corrosion failures

test conditions (°C/RH%/V)	test vehicles	sample size	test duration								
			170 h	500 h	1000 h	2000 h	3000 h	4000 h	5000 h	6000 h	7000 h
85/85/15	HEF4066BP	59	0	1	1	1	1	1	1	–	–
	HEF4519BP	60	–	0	0	0	0	0	0	0	0
			100 h	225 h	340 h	560 h	800 h				
108,7/85/15	HEF4066BP	60	0	0	0	1	8				
	HEF4519BP	60	0	0	0	0	0				
			30 h	60 h	90 h	150 h	210 h	270 h	330 h	390 h	
132,9/85/15	HEF4066BP	59	0	1	3	21	37	49	54	–	
	HEF4519BP	60	0	0	0	0	5	16	36	55	
			12 h	24 h	40 h	64 h	90 h	114 h			
151,1/85/15	HEF4066BP	60	0	8	34	43	55	59			
	HEF4519BP	60	1	5	6	14	29	49			

INFLUENCE OF FAILURE MECHANISM

Results obtained from tests carried out under all the conditions described in Table 1 have been combined with failure analyses of all observed failures. The data obtained allow the effect of test conditions on different failure mechanisms to be analysed and understood.

Corrosion failures

Table 5 gives the results obtained from tests carried out under all four sets of conditions for observed failures due to corrosion only. Using Weibull charts, the values of characteristic life η (time to 63,2% cumulative failure) and Weibull shape factor β have been determined. These are given for the three accelerated tests and for both test vehicles in Table 6.

Values of $\beta > 3{,}44$ imply a distribution whose maximum is shifted towards a longer time than that of a normal distribution. This may be due to the existence of more than one failure mechanism distributed about different characteristic life times. The test results themselves reveal shape factors that decrease with increasing test temperature.

Sorting the observed failures according to bias polarity and affected part, Table 7, reveals that failures occur predominantly on positively-biased bondpads and aluminium interconnect lines. Moreover, interconnect corrosion is more likely to occur where positive and negative lines are close together. This may be due to surface leakage, or the penetration of the nitride passivation layer by contaminants in the pastic encapsulant. Furthermore, Table 7 shows that bondpad corrosion is more likely at lower test temperatures, whereas interconnect corrosion becomes more common at higher test temperatures, as shown in Fig.2.

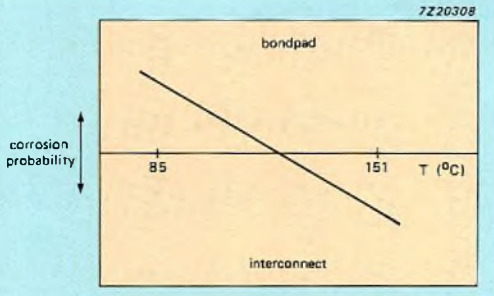


Fig.2 As temperature increases, so corrosion of the die metallization (interconnect lines) becomes more probable

TABLE 6
η and β for corrosion failures

test conditions (°C/RH%/V)	test vehicle			
	HEF4066BP		HEF4519BP	
	η (h)	β	η (h)	β
85/85/15	–	–	–	
108,7/85/15	1150	5,7	–	
132,9/85/15	210	2,8	330	6,1
151,1/85/15	57	2	90	2,4

TABLE 7(a)
Distribution of corrosion failure sites – 108,7/85/15 V

measurement point (h)	HEF4066 BP				HEF4519BP			
	bondpad		interconnect		bondpad		interconnect	
	+	–	+	–	+	–	+	–
560	0	0	1	1	0	0	0	0
800	4	2	2	0	0	0	0	0
sum	4	2	3	1	0	0	0	0

TABLE 7(b)
Distribution of corrosion failure sites – 132,9/85/15 V

measurement point (h)	HEF4066 BP				HEF4519BP			
	bondpad		interconnect		bondpad		interconnect	
	+	–	+	–	+	–	+	–
30	0	0	0	0	0	0	0	0
60	0	0	1	1	0	0	0	0
90	0	0	2	2	0	0	0	0
150	2	2	14	13	0	0	0	0
210	11	3	14	13	5	3	2	2
270	8	1	9	7	4	1	2	2
330	7	2	7	4	20	2	2	1
390	–	–	–	–	14	3	2	3
sum	28	8	47	40	43	9	8	8

TABLE 7(c)
Distribution of corrosion failure sites – 151,1/85/15 V

measurement point (h)	HEF4066 BP				HEF4519BP			
	bondpad		interconnect		bondpad		interconnect	
	+	–	+	–	+	–	+	–
12	0	0	0	0	0	0	1	1
24	0	0	6	5	0	0	4	2
40	2	1	25	16	0	0	1	0
64	8	1	6	6	3	0	7	3
90	12	7	10	9	16	3	3	2
114	4	0	2	1	20	9	4	2
sum	26	9	49	37	39	12	20	10

The dominance of interconnect corrosion at higher temperatures is thought to be due to the increased thermal stress in the plastic encapsulation causing cracks in the glass-over layer. It is through these cracks that contaminants in the plastic are able to reach the interconnect lines, accelerating the corrosion in areas of maximum potential gradient.

Dominance of bondpad corrosion at lower temperatures is probably due to moisture penetration along the lead-frame, while the preference for positively-biased pads may be due to chlorine contamination.

Activation energies (E_A) for corrosion failures vary from 1,6 to 1,8 eV for shorter tests to 1,0 to 1,07 eV for longer tests, Table 8. This is because the probability of corrosion failure increases with test time.

Parametric failures

Table 9 gives test results obtained under all the conditions listed in Table 1 for parametric failures only. Using Weibull charts, the values of characteristic life η and shape parameter β have been determined and are listed in Table 10. No reliable results for parametric failures could be derived for the 151,1/85 test due to the predominance of corrosion failures.

Characteristic life also decreased for parametric failures as test temperature increased, due to the effect of acceleration. The lower values observed for HEF4519 ICs is probably due to the thinner nitride layer (1,1 μm against 1,3 μm) used on these devices.

TABLE 8
Corrosion failure activation energy

	E_A (eV) at failure levels:			
	1%	5%	10%	50%
HEF4066BP	1,6	1,3	1,2	1,07
HEF4519BP	1,8	1,5	1,3	1,00

TABLE 10
Parametric failure η and β

test conditions (°C/RH%/V)	test vehicle HEF4066BP		HEF4519BP	
	η (h)	β	η (h)	β
85/85/15	340.000	0,7	85.000	0,4
108,7/85/15	32.000	0,75	10.000	0,5
132,9/85/15	230	1.5	2.000	0,7
151,1/85/15	–	–	–	–

TABLE 9
Parametric failure results

test conditions (°C/RH%/V)	test vehicle	test duration (h)								
		170	500	1000	2000	3000	4000	5000	6000	7000
85/85/15	HEF4066BP	1/58	1/58	1/58	1/58	2/58	3/58	4/58	–	–
	HEF4511BP	–	8/60	10/60	12/60	12/60	12/60	14/60	14/60	14/60
		100	225	340	560	800				
108,7/85/15	HEF4066BP	1/60	2/60	2/60	2/59	3/52				
	HEF4519BP	7/60	7/60	9/60	13/60	14/60				
		30	60	90	150	210	270	330	390	
132,9/85/15	HEF4066BP	1/59	4/58	4/58	*	*	*	*	*	
	HEF4519BP	3/60	5/60	5/60	7/60	11/57	11/57	12/48	13/15	
		12	24	40	64	90	114			
151,1/85/15	HEF4066BP	0/60	1/53	*	*	*	*	*	*	
	HEF4519BP	7/59	7/59	8/40	*	*	*	*	*	

* = corrosion dominant.

The comparatively small increase in shape factor observed with increasing test temperature is due to the transition from the early failure region to the constant failure rate region. Clearly, a higher test temperature than 108 °C is desirable to reduce the proportion of early failures.

Activation energies for parametric failures at various failure levels are given in Table 11. Again, there is no single activation energy.

TABLE 11
Parametric failure activation energy

test vehicle	E_A (eV) at failure level:			
	1%	5%	10%	50%
HEF4066BP	0,75	1,1	1,2	1,7
HEF4519BP	≪	<	0,36	0,92

THE PRODUCTION ACCELERATED HUMIDITY TEST

Advantages

From the results given so far, it will be apparent that 132,9 °C/85% RH with bias seems to be the most suitable test to replace the 85 °C/85% RH humidity with bias (THB) test as a standard, accelerated humidity test for the routine quality-control testing of CMOS ICs. Test temperature is high enough to reduce the influence of early failures seen at 108,7 °C, but not so high as to cause predominance of any single failure mechanism, as is the case at 151,1 °C.

Tests of 300 h duration (less than two weeks) are equivalent to 10 000 h (a full year) testing at 85 °C/85% RH, enabling us to gather data for product improvement quickly and to react to any defects in product or process fast enough to prevent the delivery of ICs likely to hazard our customers' own production.

Results

Experience with this test in production testing shows acceleration to be sensibly constant over many production batches. However, we have retained the traditional 85/85 THB test, not only to meet the requirements of both IEC and MIL Standards, but to demonstrate conclusively the advantages of the accelerated test over an extended period.

Tables 12 and 13 give the cumulative results obtained from production testing of HCMOS ICs using both the 85/85 and 132,9/85 tests on the same production batches during 1986. These results are plotted onto the Weibull chart of Fig.3. There it can be seen that projected to 30% cumulative failures the acceleration factor between the tests is close to 30.

Compared with the test results plotted in Fig.1, both lines in Fig.3 are shifted to the right, towards longer life. This indicates the improvement obtained from the change to HC10-2 encapsulant, and improved passivation. Note also that the scatter of the 132,9/85 results is much smaller than those for 85/85 testing. Inspection of Table 13 reveals that the incidence of failure becomes small after about 400 h testing, and that devices frequently survive 1500 h testing under these extreme conditions.

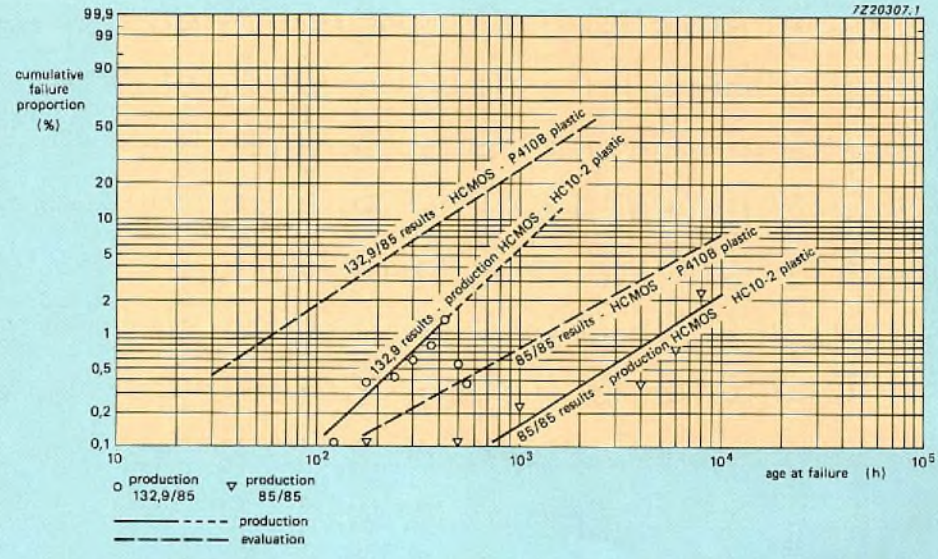


Fig.3 Weibull plot showing production 85/85 and 132.9/85 test results for HCMOS devices. Plots of HCMOS results in P410B plastic from Fig.1 are included for comparison. The production results are shifted towards longer lifetimes, indicating the improvements due to HC10-2 plastic encapssulants

TABLE 12 Research of 85/85 (THB) testing of production HCMOS ICs, 1986

	test duration (h)	sample size	cumulative failures		cumulative % failure	
			parameter	function	parameter	function
plastic DIL package:	170	855	0	1	0,00	0,12
	500	835	0	1	0,00	0,12
	1000	835	1	1	0,12	0,12
	2000	795	1	2	0,13	0,25
	4000	515	0	2	0,00	0,39
	6000	119	0	1	0,00	0,84
	8000	40	0	1	0,00	2,50
SO package:	170	630	0	0	0	0
	500	590	0	0	0	0
	1000	590	0	0	0	0
	2000	410	0	0	0	0
	4000	250	1	0	0,40	0
	8000	20	0	0	0	0

TABLE 13 Results of 132,9/85 (THB) testing of production HCMOS ICs, 1986

	test duration (h)	sample size	cumulative failures		cumulative % failure	
			parameter	function	parameter	function
DIL package:	60	1237	0	0	0	0
	120	997	0	1	0	0,10
	180	772	1	2	0,13	0,26
	240	672	1	2	0,15	0,30
	300	642	1	3	0,16	0,47
	360	612	1	4	0,16	0,65
	420	552	0	8	0,00	1,45
	480	532	0	3	0	0,56
	540	458	0	1	0	0,44
	600	398	0	0	0	0
	660	338	0	0	0	0
	720	338	0	0	0	0
	840	110	0	0	0	0
	960	110	0	0	0	0
	1080	90	0	0	0	0
	1200	90	0	0	0	0
	1320	90	0	0	0	0
	1440	30	0	0	0	0
	1560	30	0	0	0	0
SO package:	60	1022	0	3	0,00	0,29
	120	1022	1	3	0,10	0,29
	180	797	0	3	0	0,38
	240	737	0	2	0	0,27
	300	707	0	2	0	0,28
	360	460	0	0	0	0
	420	410	0	0	0	0
	480	380	0	1	0	0,26
	540	330	7	4	2,12	1,21
	600	330	8	5	2,42	1,52
	720	210	0	1	0	0,48
	840	50	0	1	0	2,00
	960	30	0	1	0	3,33

Derating

It is obviously important to be able to relate the results of laboratory testing of ICs to their performance in service. Where only temperature changes, the acceleration factor A is given by the standard Arrhenius expression:

$$A = \exp\ [E_A/k(1/T_1 - 1/T_2)] \qquad (1)$$

where T_1 is the lower (operating) temperature and T_2 the higher (test) temperature, E_A is the activation energy and k is Boltzmann's constant. This expression is tabulated for $T_2 = 132{,}9\ ^\circ C$ and various values of T_1 for selected activation energies in Appendix 2. For activation energies approaching 1 eV, the acceleration between 85 °C and 132,9 °C is close to the values found during the comparison tests.

Various models have been proposed that extend Eq. (1) where differing humidity levels have also to be allowed for (Refs 1 to 5). Such models generally add a humidity-dependent term to Eq. (1), as in Ref. 3:

$$A = \exp\ [E_A/kT(1/T_1 - 1/T_2) + 300\ (1/H_1 - 1/H_2)] \qquad (2)$$

Where H_1 and H_2 are the humidities corresponding to temperatures T_1 and T_2, respectively. This expression is tabulated for selected operating temperatures, activation energies and humidities in Appendix 3.

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APPENDIX 1: WEIBULL

During investigations into fatigue phenomena in metals, W. Weibull arrived in 1939 at the formula for a family of distributions named after him. The curve of the Weibull function, Fig. A1, varies according to the numerical values of the parameters used, especially shape factor β. When β is unity, the Weibull function reduces to the exponential distribution. When $\beta = 3{,}44$, the distribution is normal (Gaussian).

In practice, Weibull methods make it possible to determine in a straightforward way which distribution best fits a set of data. In practice, this is usually done using Weibull probability paper, as shown in Figs 1 and 3, in which the vertical axis is proportional to lnln 1/R(t) where R(t) is the instantaneous reliability. The horizontal axis is a log scale of time.

The Weibull shape factor β is the directional coefficient of the line that best fits cumulative failure, life points plotted onto a Weibull chart.

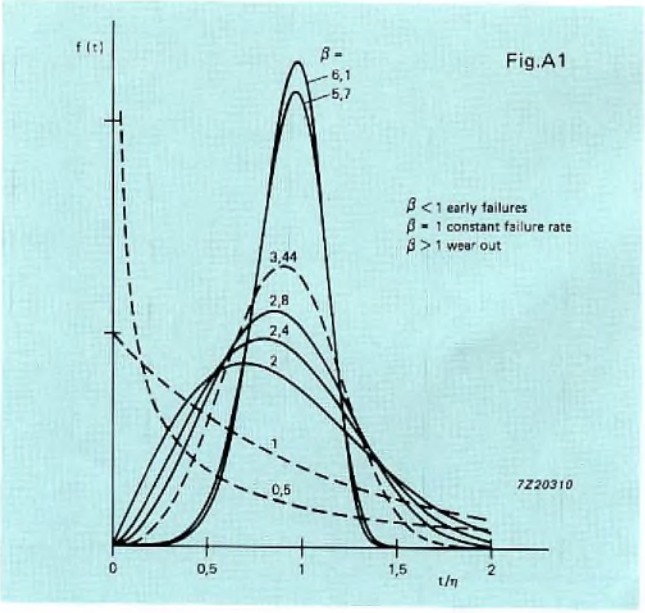


Fig.A1

APPENDIX 2: DERATING FACTORS FOR TEMPERATURE ONLY FOR VARIOUS ACTIVATION ENERGIES

(Note: Derating factors are the reciprocal of acceleration factors).

Activation energy = 0,5 eV
Test temperature = 132,9 °C

operating temperature °C	derating factor
40	0,0144
45	0,0192
50	0,0255
55	0,0335
60	0,0437
65	0,0566
70	0,0727
75	0,0927
80	0,1174
85	0,1476
90	0,1846
95	0,2294
100	0,2833
105	0,3481
110	0,4253
115	0,5171
120	0,6254
125	0,7529
130	0,9022

Activation energy = 1 eV
Test temperature = 132,9 °C

operating temperature °C	derating factor
40	0,0002
45	0,0004
50	0,0006
55	0,0011
60	0,0019
65	0,0032
70	0,0053
75	0,0086
80	0,0138
85	0,0218
90	0,0341
95	0,0526
100	0,0803
105	0,1212
110	0,1809
115	0,2674
120	0,3912
125	0,5669
130	0,8140

Activation energy = 1,5 eV
Test temperature = 132,9 °C

operating temperature °C	derating factor
40	0,0000
45	0,0000
50	0,0000
55	0,0000
60	0,0001
65	0,0002
70	0,0004
75	0,0008
80	0,0016
85	0,0032
90	0,0063
95	0,0121
100	0,0227
105	0,0422
110	0,0770
115	0,1382
120	0,2447
125	0,4268
130	0,7344

Activation energy = 2 eV
Test temperature = 132,9 °C

operating temperature °C	derating factor
40	0,0000
45	0,0000
50	0,0000
55	0,0000
60	0,0000
65	0,0000
70	0,0000
75	0,0001
80	0,0002
85	0,0005
90	0,0012
95	0,0028
100	0,0064
105	0,0147
110	0,0327
115	0,0715
120	0,1530
125	0,3214
130	0,6626

APPENDIX 3: DERATING FACTORS SHOWING THE INFLUENCE OF HUMIDITY ACCORDING TO EQ. (2)

Activation energy = 1 eV
Test temperature = 132,9 °C
Test humidity = 85%
Operating humidity = 25%

operating temperature °C	derating factor
40	0,0000
45	0,0000
50	0,0000
55	0,0000
60	0,0000
65	0,0000
70	0,0000
75	0,0000
80	0,0000
85	0,0000
90	0,0000
95	0,0000
100	0,0000
105	0,0000
110	0,0000
115	0,0001
120	0,0001
125	0,0001
130	0,0002

Activation energy = 1 eV
Test temperature = 132,9 °C
Test humidity = 85%
Operating humidity = 50%

operating temperature °C	derating factor
40	0,0000
45	0,0000
50	0,0001
55	0,0001
60	0,0002
65	0,0003
70	0,0004
75	0,0007
80	0,0012
85	0,0018
90	0,0029
95	0,0044
100	0,0068
105	0,0102
110	0,0153
115	0,0226
120	0,0331
125	0,0479
130	0,0688

Activation energy = 0,5 eV
Test temperature = 132,9 °C
Test humidity = 85%
Operating humidity = 50%

operating temperature °C	derating factor
40	0,0012
45	0,0016
50	0,0022
55	0,0028
60	0,0037
65	0,0048
70	0,0061
75	0,0078
80	0,0099
85	0,0125
90	0,0156
95	0,0194
100	0,0240
105	0,0294
110	0,0360
115	0,0437
120	0,0529
125	0,0636
130	0,0763

Activation energy = 2 eV
Test temperature = 132,9 °C
Test humidity = 85%
Operating humidity = 50%

operating temperature °C	derating factor
40	0,0000
45	0,0000
50	0,0000
55	0,0000
60	0,0000
65	0,0000
70	0,0000
75	0,0000
80	0,0000
85	0,0000
90	0,0001
95	0,0002
100	0,0005
105	0,0012
110	0,0028
115	0,0060
120	0,0129
125	0,0272
130	0,0560

New pinouts for ACL add reliability and simplicity to logic systems

ROB CROES and AD DE PAGTER

When the outputs of a high-speed logic IC change state, the short rise and fall times of the resulting signal can cause transients at the internal supply connections, thereby reducing the effective supply voltage to the chip and also causing transients at any unswitched outputs. This can degrade system reliability by reducing noise margins and speed, and causing loss of stored data and false switching. Since the amplitude of the transients increases in direct proportion to the number of outputs simultaneously switched in the same direction, this phenomenon is referred to as simultaneous switching noise. Although it also occurs in bipolar TTL circuitry, simultaneous switching noise is particularly severe in CMOS logic wherein the IC outputs can switch almost from one supply rail to the other.

It's a common belief that supply decoupling capacitors adjacent to each IC will eliminate simultaneous switching noise. However, this is not the case because the amplitude of the noise is related to the absolute inductance of the supply connection between the chip in the IC and the supply/groundplane on the PCB. Since multilayer PCBs provide excellent low-impedance supply/groundplanes, the noise can only be reduced by taking preventive measures during manufacture of the ICs. Supply line decoupling should be similar to that used for TTL systems operating at comparable speed.

As shown in Fig.1, when switching occurs, the discharge path for the sum of the load capacitances connected to any switched outputs of an IC includes the bonding wire and lead-frame inductance associated with the V_{CC} or GND connections. In the case of HIGH to LOW switching, the discharging total capacitance causes a transient current through the internal and external ground connections that lifts-up the internal ground above 0 V, thereby reducing the effective supply voltage to the chip and causing a voltage transient that increases the level at any unswitched LOW outputs. The peak amplitude of the transient (simultaneous switching noise) is directly related to the number of outputs simultaneously switched and is proportional to the dV/dt at the switched output(s), and to the inductance of the supply connections.

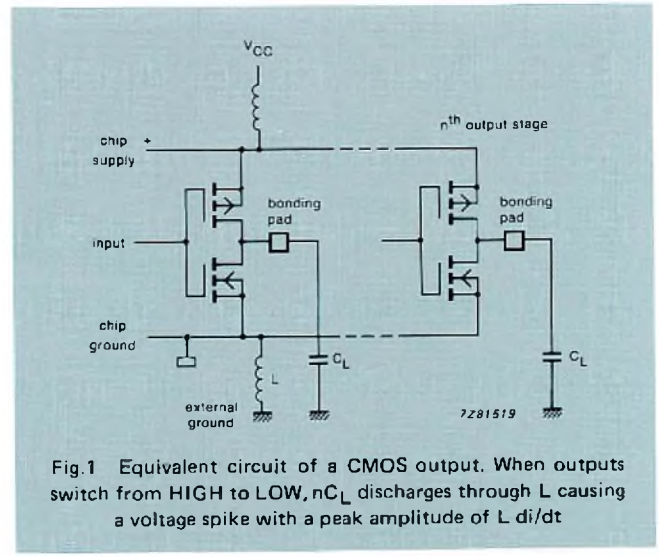


Fig.1 Equivalent circuit of a CMOS output. When outputs switch from HIGH to LOW, nC_L discharges through L causing a voltage spike with a peak amplitude of L di/dt

The first measure we've taken to reduce simultaneous switching noise in our ACL ICs is to use a modified output structure in which "distributed" transistors and edge-control circuitry control the di/dt of the output transistors during turn-on without reducing switching speed. A "distributed" transistor consists of many transistors which are turned-on sequentially to slow down the action but turned-off much more quickly. For ACL ICs with more than eight outputs, the output edge control circuitry is further tailored to keep the amplitude of the transients below the fatal level. The dimensions of the output transistors and output edge control circuitry are sufficient to maintain 24 mA output drive and to permit incident wave switching with 50 Ω or 75 Ω transmission line loads.

The second measure is relocation of the V_{CC} and GND pins to minimize the inductance of the associated lead-frame connections and bonding wires. In the early days of integrated logic circuits, manufacturers were forced to position IC supply pins at diagonally opposite corners of the package because of layout restrictions imposed by single-sided PCBs that were universally used at that time. However, in today's world of double-sided and multilayer PCBs and much faster logic, this can no longer be considered to be good engineering practice. The high inductance of the corner pins makes it the worst possible supply pin positioning from the point of view of achieving high performance.

For our ACL ICs, we've decided that optimum system reliability is far more important than pin compatibility with TTL, and we've relocated the V_{CC} and GND pins in the centre of opposite sides of the package where their inductance is minimum. Furthermore, ACL ICs with more than two outputs that can switch simultaneously have multiple parallel-connected V_{CC} and GND pins to reduce their inductance yet further. ACL ICs in 16-pin packages and with 3 or 4 outputs that can switch simultaneously have two V_{CC} pins and two GND pins; ACL ICs in 20, 24 or 28-pin packages and with 3 or more outputs that can switch simultaneously have two V_{CC} pins and four GND pins.

Figure 2 compares the reduced supply lead inductances for ACL ICs with the new pinouts with those of ICs with conventional pinning. It should be noted that the inductance shown for ACL ICs with multiple parallel-connected V_{CC} and GND pins includes mutual inductance. It is clear from Fig.2 that the inductance of the supply leads of ACL ICs in DIL packages is even less than that of ICs in the smaller SO packages with corner V_{CC} and GND pins.

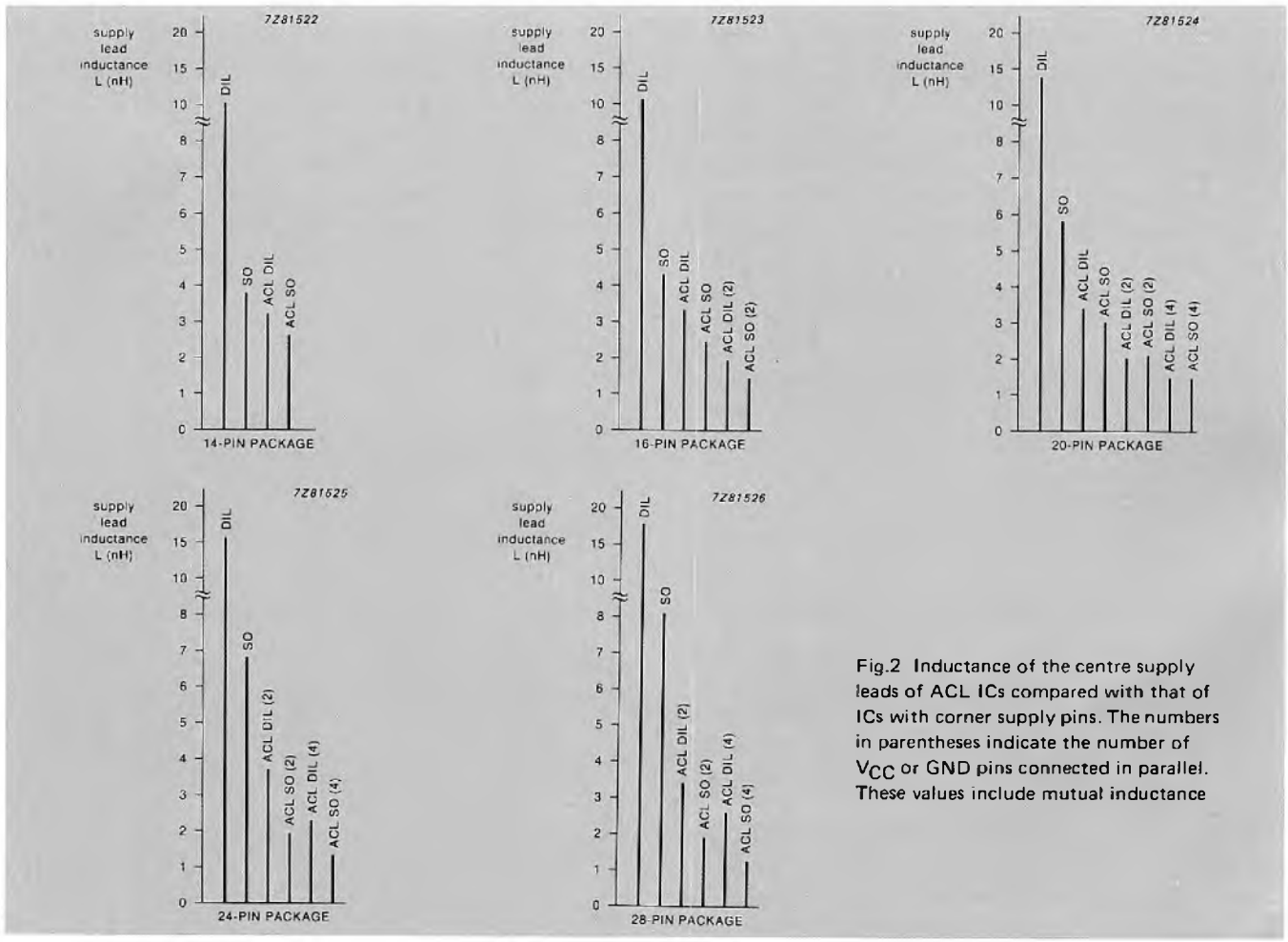
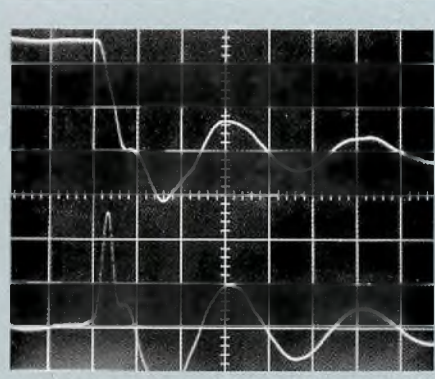
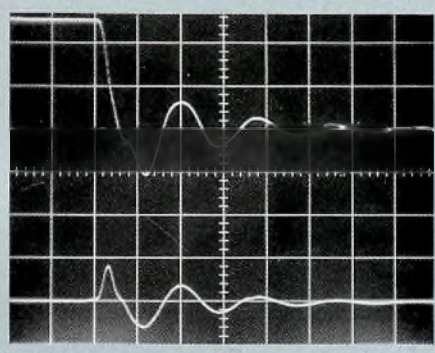


Fig.2 Inductance of the centre supply leads of ACL ICs compared with that of ICs with corner supply pins. The numbers in parentheses indicate the number of V_{CC} or GND pins connected in parallel. These values include mutual inductance

To confirm that reduced supply lead inductance results in considerable reduction of simultaneous switching noise, tests were performed on an ACL octal buffer/line driver (74AC11240) which has two V_{CC} pins and four GND pins centrally positioned, and on its corner supply pin counterpart (74AC240). The tests involved simultaneously switching seven of the eight outputs from HIGH to LOW whilst observing the simultaneous switching noise on the eighth (LOW) output. The results of these tests, shown in Fig.3, reveal that the initial peak amplitude of simultaneous switching noise (V_g) on the LOW output of the ACL IC stays well below the maximum LOW input switching level and is only about one-third of that for the same IC with conventional corner supply pins. So, the new pinning of ACL ICs eliminates the possibility of false switching. Since reduction of the effective supply voltage to the chip is also much less than that for the IC with corner V_{CC} and GND pins, the new ACL pinning also minimizes loss of speed and maintains the integrity of stored data.



(a) IC with corner supply pins



(b) IC with quad centre supply pins

Fig.3 Simultaneous switching noise comparison when 7 outputs of octal 74AC240 and 74AC11240 in DIL packages are simultaneously switched (V_{CC} = 5 V, T_{amb} = 25 °C). The noise is measured on the 8th output which is held LOW. Note that the frequency of the ringing in the upper picture is lower than that in the lower picture due to the higher total loop inductance between the output pin and the groundplane on the PCB ($V_g = V_{GND}$)

Figure 4 compares the amplitude of simultaneous switching noise for an ACL octal D-type transparent latch 74AC11373 with the new pinning for DIL and SO packages (lower two plots) with that of the same type of corner supply pin IC from two other manufacturers (upper three plots). It's clear that, in this case, the amplitude of simultaneous switching noise with the ACL IC in a DIL package is at least 40% lower than that of the same IC in a smaller conventional SO package.

We've also rationalized the positioning of the I/O and control pinning of ACL ICs as shown in Fig.5. The inputs surround the V_{CC} pin(s) on one side of the package, and the outputs surround the GND pin(s) on the other side. Any control pins are strategically placed at the corners of the package. This ACL flow-through architecture, which is used for all ACL ICs in both DIL and SO packages, minimizes the total inductance of I/O connections between the chip and the PCB (bonding wire plus lead-frame and output pin). It also facilitates positioning of supply decoupling components (supply pins closer together and opposite to each other), simplifies PCB design and fault-finding, and decreases the PCB area required for routing connections.

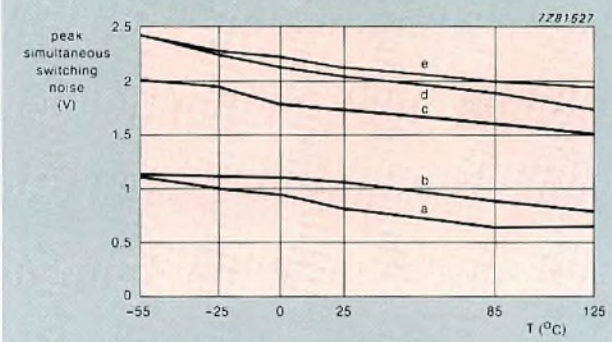


Fig.4 Amplitude of simultaneous switching noise for AC11373 ICs with the new pinning for SO and DIL packages (plots a and b) compared with that of AC373 ICs in corner supply pin packages from two other manufacturers (plots c, d and e) as functions of temperature. The amplitude of simultaneous switching noise with an ACL IC in a DIL package (plot b) is at least 40% lower than that of the same IC in a smaller SO package with conventional pinning (plot c). The measuring conditions were V_{CC} = 5 V, C_{load} = 50 pF, R_{load} = 500 Ω

plot a: 74AC11373 in SO package
plot b: 74AC11373 in DIL package
plot c: 74AC373 from manufacturer A in SO package
plot d: 74AC373 from manufacturer A in DIL package
plot e: 74AC373 from manufacturer B in DIL package

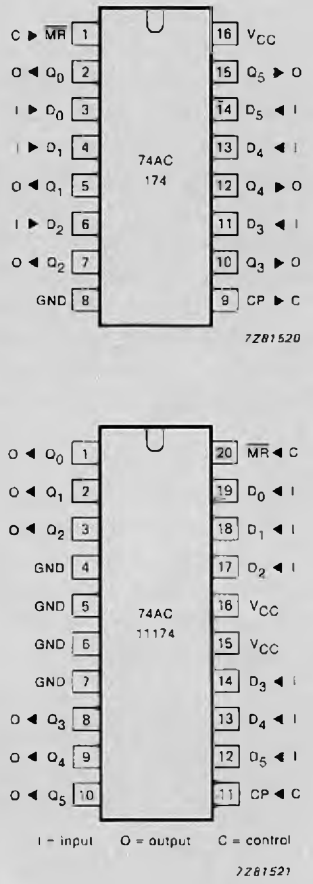


Fig.5 Flow-through architecture of the 74AC11174 ACL IC compared with that of the 74AC174 with conventional pinning

ACL PACKAGES

All ACL ICs are available in SO (small outline) packages as well as in 300 mil wide DIL packages, so you can use surface-mounting techniques to increase PCB packing density. ACL ICs with 14 ir 16 pins are in the narrower 150 mil (3.8 mm) SO packages packed on 16 mm tape on 13 in. reels (2500 ICs). ACL ICs with, 20, 24 or 28 pins are in 300 mil (7.6 mm) wide SO packages packed on 24 mm tape with 1000 ICs on a 13 in. reel. The body width of all the DIL packages (14 to 28 pins) is 300 mil (7.6 mm).

Video ADCs using folding and interpolation techniques

PIERRE PIVER

Demand for high quality ADCs for consumer products is increasing rapidly, especially those for video systems. Until now, however, none of the monolithic consumer ADCs available has had the required performance, and when composite video signals have to be converted, even professional "8-bit" ADCs are often down to 4 or 5 effective bits of resolution at the colour subcarrier frequency*. In addition, the latter dissipate lots of power, needs lots of external circuitry, and may be expensive to manufacture. Now, a range of ADCs incorporating a new A/D conversion technique has the required combination of 'professional' specification, low price and low dissipation. Originally developed for digital TV systems and MAC satellite TV, the circuits, which are manufactured in a standard 1.7 μm bipolar process, perform better than the best professional converters currently on the market. All the new converters have 8-bit effective resolution up to 8 MHz, yet dissipate less than 300 mW. Within the 5 MHz video band, every distortion component is below −60 dB. Samples of two 'flash' ADCs using this new design are available now – one dedicated for video applications, and the other for professional use. A second video converter incorporating the AGC and clamping functions and a second professional converter are in development. Main differences between the ADCs are operating temperature range, package and output configuration (see Table 2).

* The number of effective bits of resolution is a figure of merit that can indicate the high-frequency degradation of performance of an ADC, not apparent from manufacturer's commonly-published specs of integral and differential linearity. The number of effective bits of an ADC is $\log_2(\text{SNR}-1.78)/6.02$, where the SN ratio (SNR) is measured when a full-scale sine wave is being converted.

Whereas most high-performance ADCs are of the full-parallel 'flash' type, the new ADCs use a proprietary design that incorporates analogue pre-processing. As well as reducing power dissipation, chip size and 'kick-back' noise, pre-processing simplifies the distribution of signals around the chip. Although the specifications of full-parallel ADCs have improved steadily with improving technology, ADCs using analogue pre-processing techniques should always be able to achieve at least the performance of the full-parallel implementation manufactured using a comparable process.

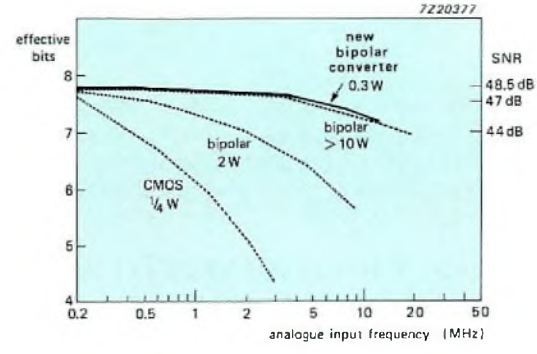


Fig.1 Eight-bit resolution up to 8 MHz, yet the new ADC dissipates less than a tenth that of the best professional full-parallel converter implemented in a similar process

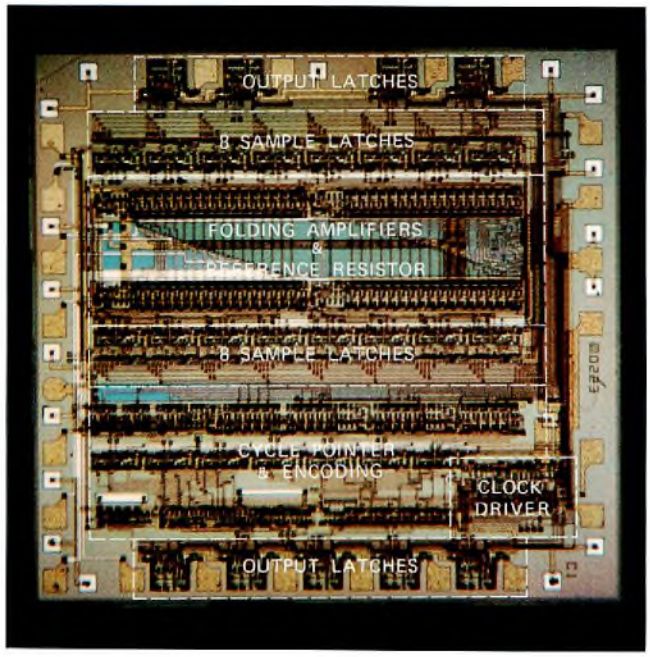


Fig.2 Photomicrograph of the new ADC chip. Drastic reduction of the number of comparators and latches required compared with that for a full-parallel flash ADC produces a compact layout occupying just 6 mm^2. The analogue circuitry is concentrated in one part of the chip, well away from the noise-generating digital circuits, so the analogue input lines can be extremely short, virtually eliminating differences in signal delay

TABLE 1
Specification of the new ADCs

max. clock frequency	50 MHz
f_{in} (7.5 effective bits*)	8 MHz
SNR (f_{in} = 0 to 5 MHz)	>47.5 dB
effective bits (f_{in} = 1 kHz)	7.8 bit
effective bits (f_{in} = 5 MHz)	7.6 bit
n-harmonics (f_{in} = 0 to 5 MHz)	<−60 dB
max. source impedance	75 Ω
input capacitance (typ.)	11 pF
output	ECL or TTL
dissipation (5 V supply)	<300 mW
chip area of the ADC	6 mm^2

* the input frequency at which the number of effective bits has fallen to 7.5, equivalent to an S/N ratio 3 dB worse than that of an ideal 8-bit converter. The number of effective bits (EB) is related to the S/N ratio (SNR) by

EB = $\log_2$(SNR-1.78)/6.02, where the S/N ratio is measured when a full-scale sinewave is being converted.

TABLE 2
8-bit ADCs for consumer and professional applications

	type	package	output	main applications
Consumer				
f_{clock}: ≥30 MHz; ambient temp. range: 0 to 75 °C	TDA8703	plastic DIL-24	TTL	video processing (de-scramblers, digital TV, MAC satellite TV, picture-in-picture, video communication, IF digitizing
	TDA8708*	plastic DIL-28	TTL	
Professional				
f_{clock}: 50 MHz ambient temp. range: −25 to +85 °C	TDE8713D*	ceramic DIL-24	TTL	image processing, medical electronics, radar, sonar, high-definition video, industrial control, test and measurement equipment
	TDE8715D	ceramic DIL-18	ECL	

* in development.

Suitable DACs for systems using these ADCs are the TDA8702 (consumer) and the TDE8712D (professional). Both DACs are in 16-pin DIL packages. Because of their small size and low power dissipation, the chips for the consumer converters (TDA8702, TDA8703 and TDA8708) are all suitable for encapsulation in SO packages.

REDUNDANCY IN CONVENTIONAL ADCs

In a conventional 8-bit full-parallel converter (see Fig.3), 255 comparators simultaneously compare the input signal with 255 reference voltage levels derived from a resistor ladder. At the sample clock, an array of 255 latches decides whether the output of each comparator is one or zero, and takes over this information. Digital circuitry translates the latched data into an 8-bit code. Only the position in the comparator array of the transition between ones and zeroes contains relevant information about the instantaneous level of the analogue signal. Therefore, full-parallel systems retain information that is redundant. For example, each sample latch only changes state once during a full-scale input ramp. Clearly, the use of the sample latches is not efficient. In the new converters, 'folding' and interpolation techniques drastically reduce the number of latches and comparators required.

TABLE 3
Components required for 8-bit full-parallel converters and for the new folding and interpolating converters

	conventional full-parallel ADC	folding and interpolating ADC
precision reference-resistor taps	255	64
comparators	255	64
interpolation-resistor taps	0	24
latches	255	16
gates	255	16
stages in encoding circuit	255	16
simple 3-bit coarse converter	0	1
clock-driver circuit fan-out	255	24
output buffers	8	8

one as in a full-parallel converter. In our design there are just 16 sample latches. Clearly, to prevent the output signals from affecting each other, the comparators whose outputs are combined must be sufficiently far apart in the comparator array. Because of the folding, the same sample latches can be used repeatedly, producing a repetitive latch-output-code (8 cycles over the entire input range), so a cycle pointer (3-bit coarse converter) is needed. The information generated by the cycle pointer is required to complete the 8-bit binary code describing the input signal. Because there are so few latches in a folding converter, the distance between the outer sample latches is much smaller than in a full-parallel converter, so clock distribution problems are simplified. Folding techniques not only reduce the size of the analogue-to-digital interface (23 lines instead of 255), but less encoding circuitry is required as well, cutting "kick-back noise".

Figure 4 illustrates the principle of folding when a slow ramp input signal is applied to the converter.

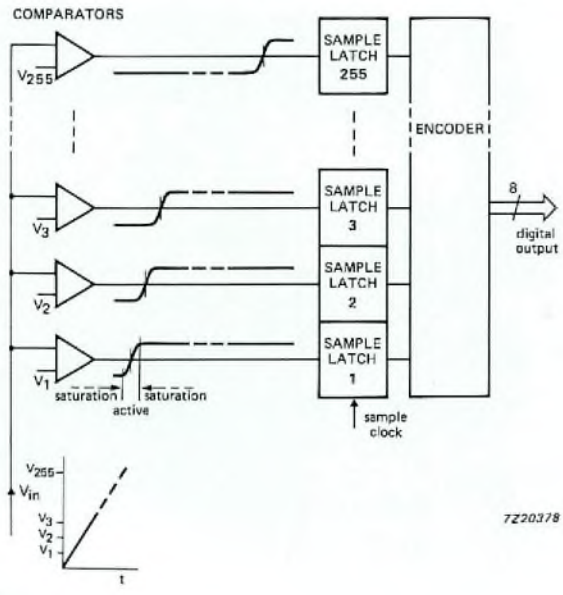


Fig.3 8-bit full-parallel flash ADC. At the sample clock, an array of 255 latches decides whether the output of each of 255 comparators is one or zero. The use of latches is not efficient — each has only to make one decision over the entire full-scale input range

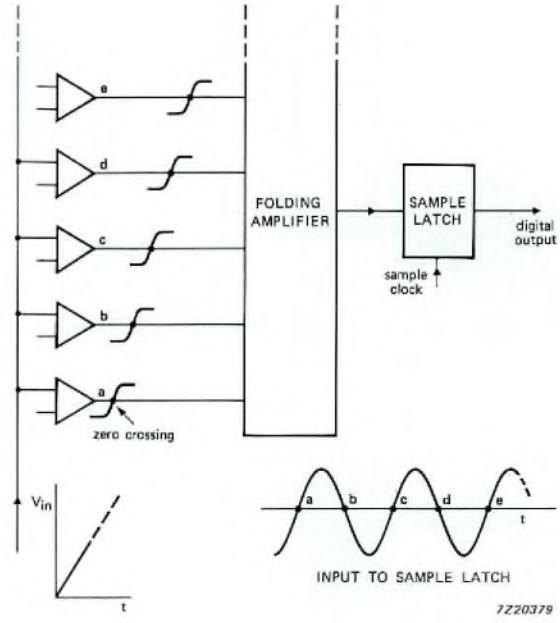


Fig.4 Folding the outputs of several comparators to one latch reduces the number of latches needed in an 8-bit converter to just sixteen. And interpolation techniques enable three out of every four comparators of a full-parallel design to be omitted without degrading the converter's accuracy

A measure that decreases the number of sample latches is the folding technique. Provided that at any moment no more than one of the comparators is in its transition range, the outputs of several comparators may be combined ('folded') and sampled by a single latch. In this way, one latch can handle several quantization levels instead of just

Although folding reduces the number of sample latches required compared with a full-parallel converter, the number of comparators is still large. However, it's possible to omit three out of every four comparators, and to recover the missing signals from the remaining output signals by interpolation without degrading the converter's accuracy.

The interpolation technique makes use of the fact that a comparator doesn't change state instantaneously when the input voltage exceeds the reference voltage. Instead, its output signal follows the input signal virtually linearly over a limited part of the transition range. Since only the zero crossing of each comparator input is important for a latch to make a correct decision about the status of each comparator, as long as the positions of the zero-crossings are unaltered by interpolation, the information in the comparator output signals won't be affected. In the new design, interpolation is implemented simply by inserting a ladder of resistors between the outputs of every fifth comparator (of the original 255-comparator array), and omitting the groups of three comparators in between, see Fig.5. The missing zero-crossing information is present at the taps of the ladder. Interpolation reduces the number of comparators and the number of reference taps from 255 to 64.

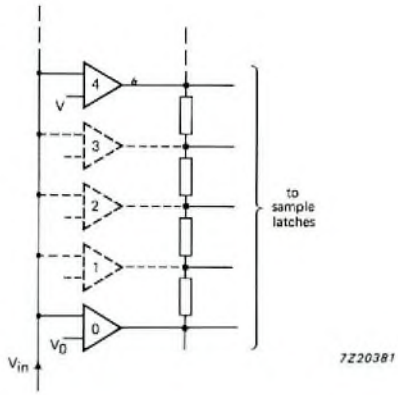


Fig.5 Interpolation by a simple resistor array

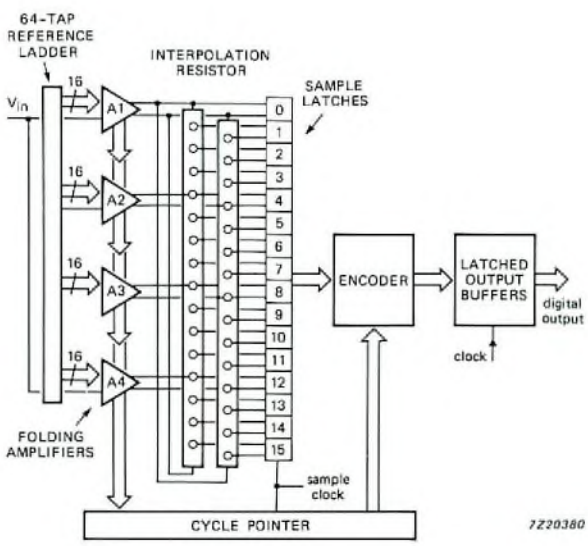


Fig.6 Block diagram of the new ADCs. In practice, interpolation takes place after the comparator output signals have been folded, not before as described in the main text

Reducing the number of taps improves the linearity of the comparator reference voltages in two ways. First, any physical contact to the reference resistor ladder material disturbs the homogeneity of the material which, with the manufacturing spread in the size of the contacts, degrades the linearity of the ladder. Second, in an interpolating ADC, fewer base currents flow through the reference resistor ladder. In a conventional converter, this cause of non-linearity of the reference voltages is strongly dependent on the current gain of the comparators' input transistors, and is not easily compensated. Therefore, conventional ADCs require a low-impedance reference ladder which consumes a large amount of power. In an interpolating ADC, the ladder impedance can be higher, reducing dissipation without affecting linearity.

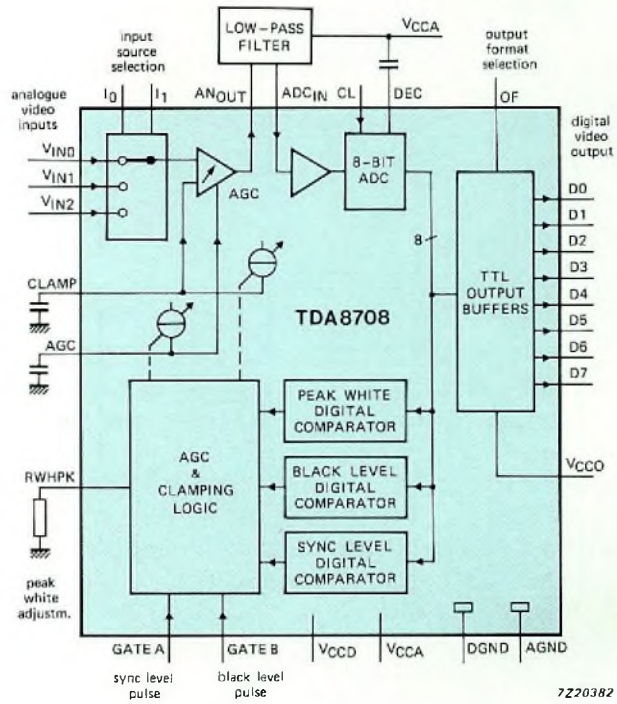


Fig.7 The TDA8708 incorporates the a.g.c. and clamping functions required for consumer TV applications

REFERENCE

Van de GRIFT, R. E. J., RUTTEN, I. W. J. M., and van de VEEN, M., 'An 8-bit video ADC incorporating folding and interpolation techniques', IEEE Journal of Solid-state Circuits, Vol. SC-22, No.6, Dec. 1987.

Enhanced computer-controlled teletext circuit SAA5243

JOHN KINGHORN

In the last few years, teletext has become an established feature in the domestic TV market. Over 15 million teletext TV receivers have now been produced, and the teletext facility is considered as a standard requirement for medium and top-range TV sets. As more countries start transmitting teletext, and as the features and quality of the service improve, the demand for teletext receivers will undoubtedly expand.

The Enhanced Computer Controlled Teletext (ECCT) circuit, SAA5243 (Ref.1), is designed to form the heart of a versatile and economical teletext decoder that takes full account of the increasingly complex requirements of the market. For improved recovery of the transmitted teletext data under poor signal conditions, a new video processor (VIP2): the SAA5231 (Ref.2), has been developed for use with the ECCT circuit. While catering for many diverse applications of teletext, these two circuits have been designed so that there are no system cost penalties for the standard mass-market television application.

FEATURES OF THE ECCT

- performs all the digital logic functions of a 625-line World System Teletext decoder
- microcomputer-controlled (via the I^2C bus) for flexibility
- 192 characters (12 x 10 dot matrix)
- covers all the major languages in Western Europe
- automatic selection of English, French, German, Italian, Spanish and Swedish character sets
- field flyback or full-channel data acquisition
- direct interface with up to 8 K bytes static RAM
- handles up to 4 simultaneous page requests
- 25th display row for software-generated messages
- cursor control available for videotex and telesoftware
- 7-bits plus parity, or 8-bit data reception
- accepts extension packets
- single 5 V power supply
- mask-programmable character sets for regions outside Western Europe
- slave sync operation option
- odd/even field output for de-interlaced displays.

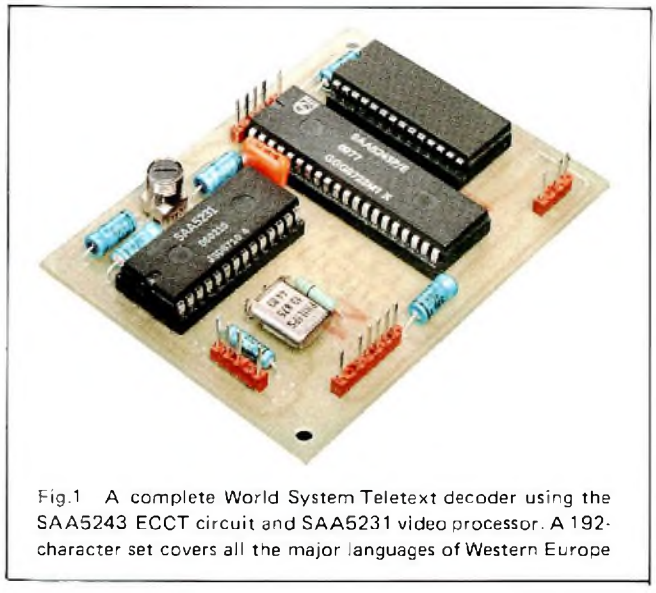


Fig.1 A complete World System Teletext decoder using the SAA5243 ECCT circuit and SAA5231 video processor. A 192-character set covers all the major languages of Western Europe

WORLD SYSTEM TELETEXT DEVELOPMENTS

Languages

The World System Teletext standard (Ref.3), previously known as UK Standard Teletext, has now been adopted in more than thirty countries, making the language requirements increasingly complex. Currently, individual languages or small groups of languages are catered for by mask-programmed variants of the character generator circuits of the decoder. Although this has been satisfactory for national broadcasting, the availability of 'national' broadcasts to an international audience via satellite transmissions and the trend towards international broadcasting make it desirable for teletext transmissions to be decoded correctly outside their country of origin. And as broadcasting becomes more international, teletext can be used to subtitle programmes in many languages simultaneously, making them comprehensible to a much wider audience – the desired translation being selected by the viewer and inserted in the normal picture, see Fig.2.

Some languages require many special characters, more than can be accommodated in the standard 96-character sets available with earlier teletext circuits. Spain is the first country in Europe to start a teletext service using an extended set of 128 characters. Other countries, for example Iceland, need a small number of special symbols which cannot be implemented economically in their own circuit variant owing to the relatively small home-market for TV sets. The best solution here is to include the special symbols in a standard device for a large group of languages.

Using a set of 192 characters, the ECCT circuit covers *all* the languages required in Western Europe. When controlled with suitable software, a teletext decoder using the ECCT circuit can be used anywhere in Western Europe with the correct characters displayed automatically.

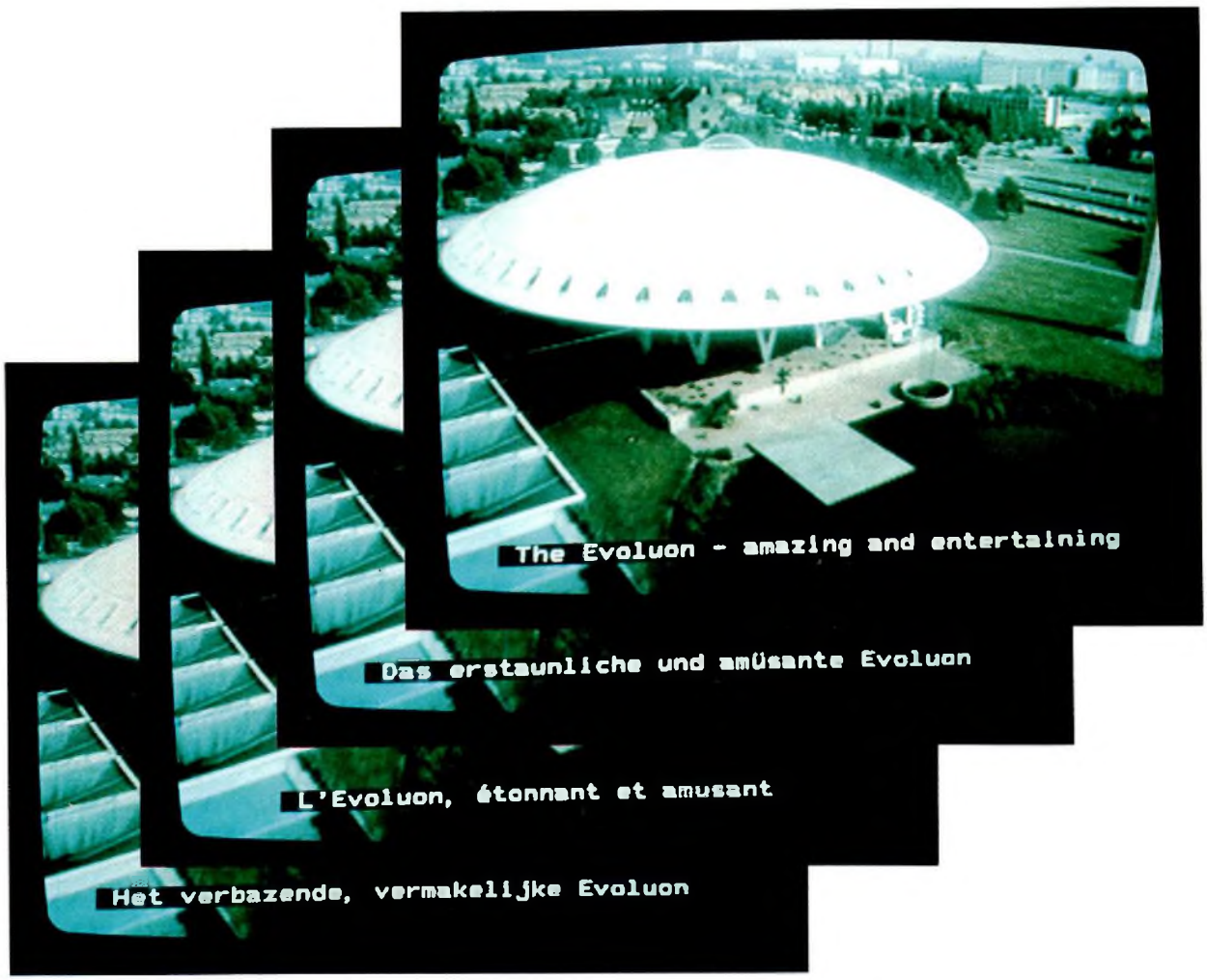


Fig.2 Multi-language subtitling makes more programmes comprehensible to today's international television audience

FLOF/Fastext

As teletext services mature, new features are being introduced to make it easier for the viewer to select the required information. A system known as FLOF (Full Level One Features) or Fastext (Ref.4) is now in service in the UK and Spain, with other countries expected to follow shortly. This gives easy selection of pages via coloured keywords (prompts) at the bottom of the screen which are used in conjunction with corresponding coloured keys on the remote control unit, see Fig.3. Instant access to pages can be provided by using additional memory. The ECCT circuit has all the facilities necessary to implement a Fastext decoder economically – multiple acquisition circuits, extension packet capture and a display row for broadcaster-generated prompt messages.

Fig.3 Full Level One Features (FLOF) or Fastext decoders using the ECCT simplify page selection and can provide instant page-access

VCR control

Another area of expansion for teletext is in the programming of VCRs. Such a programming system uses teletext pages containing programme schedules. The user selects the programmes to be recorded by moving a cursor on the screen to the required programme and pressing a "record this" button. This causes the necessary information to be loaded into the VCR automatically and the programme will be recorded when it is broadcast. In Germany, this system is known as VPV (Videotext Programmiert Videoheimgeräte), and a VPV decoder can be built using the ECCT circuit with suitable software to download the programme recording data into the VCR control circuit. The signals that switch the VCR recording circuits on and off are broadcast using the Video Programming System (VPS) format, so a VPS circuit is still needed to control the VCR. However, the necessary functions are now included in the broadcast teletext specification (Ref.3), which may be adopted in other countries. In this case, both the programming and control of the VCR could be performed with the ECCT and suitable software.

Data distribution

As well as these mass-market consumer applications, there is increasing interest in the use of teletext for data distribution. Subscription teletext services (for example, specialized financial information, control data and racing results) make use of teletext transmissions to convey data, and are not intended to be received on a normal teletext TV set. A degree of security can be achieved using encryption and access control methods, so that only those entitled to receive the data can do so. Decoders for such services (using the 'page format' transmission method) can be built using the ECCT with suitable software.

Another professional application for teletext technology is the distribution of data within an office or factory. Here, teletext is not broadcast, but is relayed through coaxial cable. Such systems can make use of full channel teletext data, where the entire channel is used for teletext and there is no accompanying TV picture signal. This allows a high data throughput of over 600 pages per second, giving fast access. These methods are particularly useful when a large number of receiving terminals are envisaged, since a full-channel teletext data inserter need occupy only one port on a computer, however many terminals are served. The ECCT can be switched (under software control) to accept full-channel teletext, with data inserted on any TV line.

Although a variety of applications can be catered for, the design of the ECCT circuit and VIP2 ensures there is no cost penalty for the normal mass-market application. In the design of the ECCT-based teletext decoder, two types of function have been distinguished:

– standard functions fixed by the broadcast specifications, for example, data slicing, sync generation and data acquisition – performed by dedicated circuitry in the VIP2 and the ECCT.

– functions that will vary depending on the application, for example, the control functions and displayed languages – performed by software in the decoder's control microcomputer.

Advanced decoders for professional applications are made mainly by using more sophisticated software than that used in decoders for the mass-market; often no hardware changes are required.

WORLD SYSTEM TELETEXT DECODER USING ECCT

Hardware

A simple World System teletext decoder using the ECCT is shown in Fig.1. It consists of three ICs and a few peripheral components. From the incoming composite video signal, the video processor extracts the teletext data, regenerates the teletext clock and produces the signal for synchronizing the text display to the TV syncs. The ECCT provides all the necessary digital hardware functions for a teletext decoder.

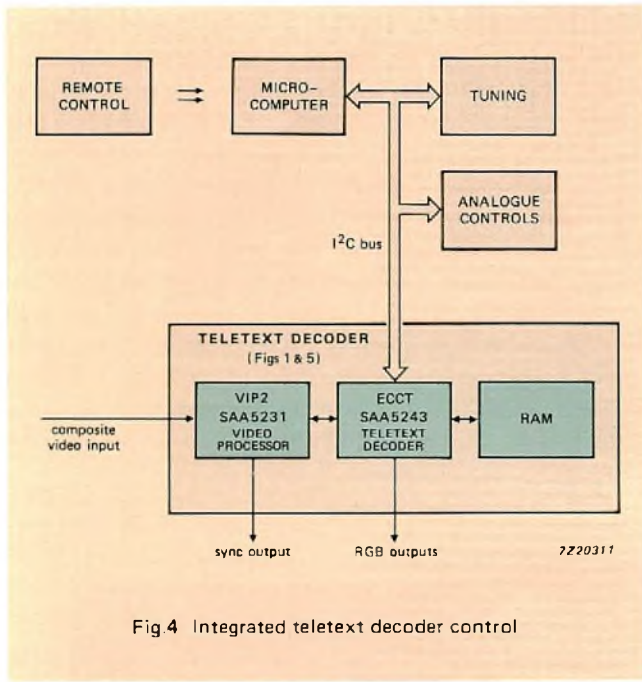


Fig.4 Integrated teletext decoder control

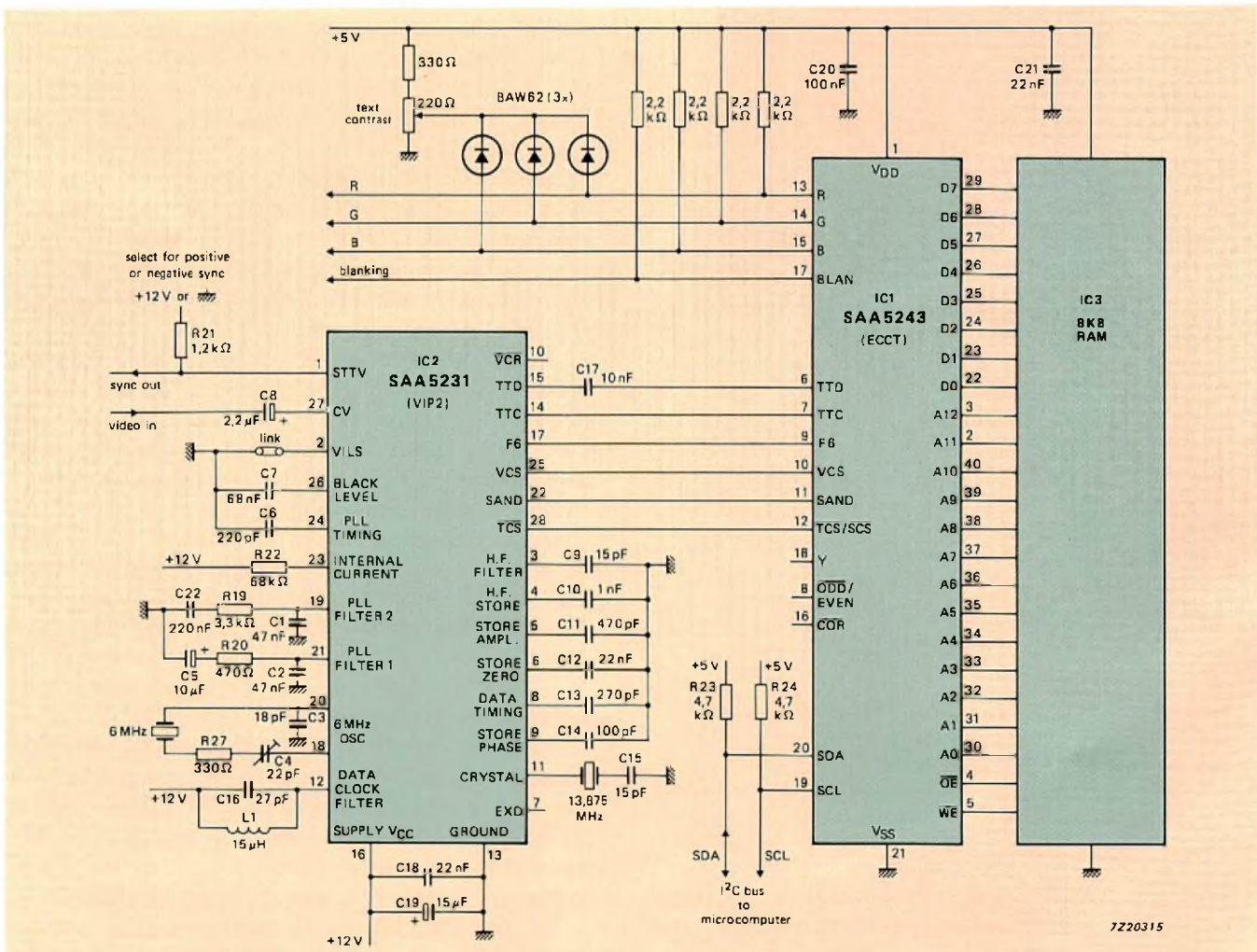


Fig.5 ECCT-based teletext decoder circuit diagram

It interfaces to a standard static RAM (typically 8 K byte) used as page memory.

As can be seen from Fig.1, this standard form of teletext decoder is small enough to be located on the main circuit board of a TV set – an approach that is becoming fairly common as teletext becomes a standard feature of a TV set. Putting the decoder on the main board eliminates the connectors, wiring and brackets of the conventional 'add-on' teletext decoder, and with careful board design, some of the peripheral components such as output buffers can be eliminated too. The ECCT is controlled via the 2-wire I^2C bus by the TV set's microcomputer, which, in addition, decodes signals from the remote control, and controls the tuning and analogue functions. In this approach, see Fig.4, the teletext facility is clearly designed as an integral part of the TV set. The circuit diagram of the complete teletext decoder is shown in Fig.5.

For more sophisticated systems, or where a variety of options are required in the TV set design, a modular approach may be preferred, see Fig.6. Here, a microcomputer is dedicated to the control of the teletext decoder, allowing higher performance with more independence from the rest of the set design. The hardware of the decoder itself is identical to that shown in Fig.5. This approach provides flexibility in design – modules for teletext, videotext and subscription teletext can be added as required (as long as the remote control decoding software can pass on all the necessary commands).

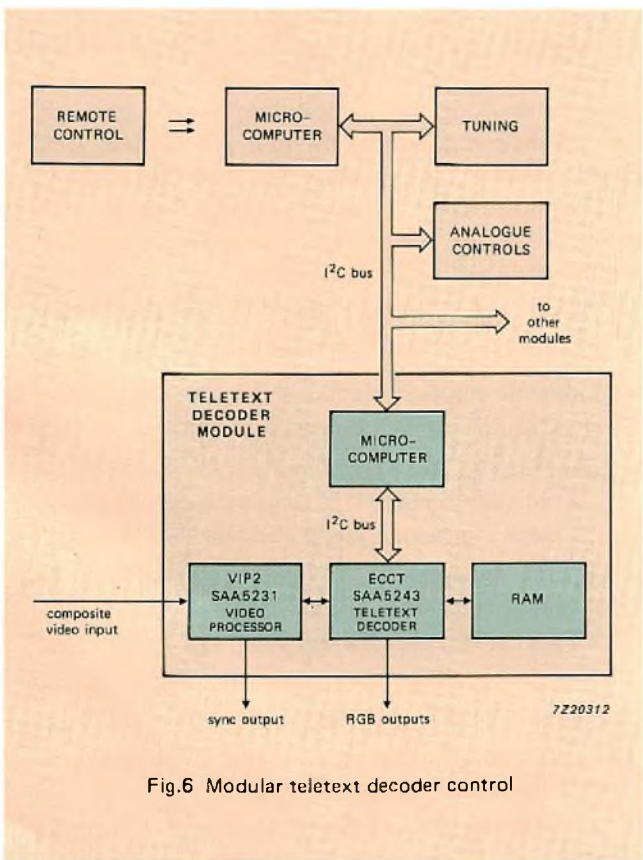


Fig.6 Modular teletext decoder control

Video Processor (VIP2): SAA5231

The SAA5231 is a 28-pin bipolar linear IC (see Fig.7) which extracts the teletext data from the composite video, regenerates the clock and synchronizes the text display to the tv syncs.

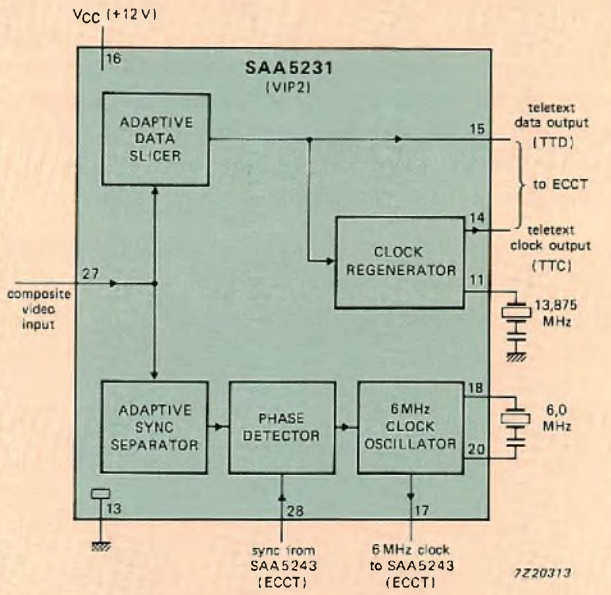


Fig.7 Video input processor SAA5231 (VIP2). Only the main functions are shown

The data detector of the VIP2 finds the slicing level for extracting the teletext data and compares it with the composite video to obtain sliced data. The slicing level is automatically altered to suit variations in data amplitude and low-frequency disturbances such as co-channel interference, while remaining relatively unaffected by echoes, data content, and noise. High-frequency losses in the signal are compensated, if necessary, to enlarge the "eye height" for improved data reception.

The teletext clock generator takes in the sliced data and generates a synchronized clock derived from a free-running crystal oscillator whose phase is shifted in a feedback loop until it is at the optimum point for latching the data. A PLL is not used as it would take too long to lock in; the circuit used can find the correct clock phase before the end of the clock run-in period. This type of regenerator produces less jitter than a tuned circuit and has no critically-adjusted components. In addition, missed clock cycles can't cause a loss of bit synchronization.

The 6 MHz clock for the character display is derived from a VCO. This clock is part of a PLL required to synchronize the teletext characters to the video signal; the PLL has been designed to allow the display to be locked to a VCR, for status messages, for example. The VIP2 includes a wide range adaptive sync separator for this PLL.

Enhanced Computer-Controlled Teletext (ECCT) circuit: SAA5243

The SAA5243, see Fig.8, is a 40-pin NMOS IC which performs all the digital logic functions of a 625-line World System Teletext decoder. Serial data and clock signals from the VIP2 video processor enter on the TTD and TTC pins respectively. After data capture, the data enters the page memory via a memory interface also used to direct data from the RAM to the character generator as required. The character generator provides the RGB drives for the video stages of the TV receiver or monitor. Outputs are provided for blanking and contrast reduction of the TV picture (BLAN and $\overline{\text{COR}}$), together with a monochrome text signal (Y) for driving a printer.

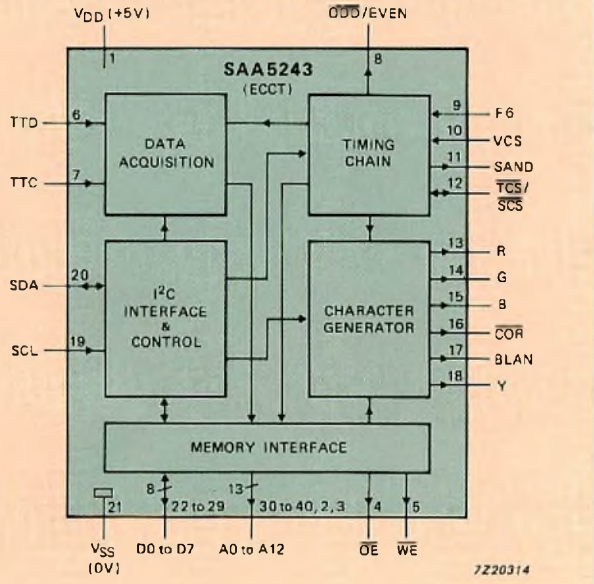


Fig.8 Enhanced Computer Controlled Teletext circuit (ECCT)

Timing chain

Timing signals for all of the ECCT are provided by the timing chain circuitry, which operates from a 6 MHz clock F6 from the VIP2. Line synchronization with the incoming signal is performed by a phase-locked oscillator in the VIP2, using the reference signal SAND from the ECCT. A composite sync waveform, VCS, from the VIP2 provides field synchronization for the data acquisition timing and also for the display timing when interlaced display is selected. The display timing circuit generates a composite sync waveform, TCS (with interlaced or non-interlaced format), used to drive the display timebases via the VIP2; alternatively, this pin can act as an input for a composite sync waveform to 'slave' the display timing circuits in the ECCT. To summarize, the main features of the timing chain circuitry include:

- operation from an external clock from VIP2
- display format – 625 lines/25 rows/10 lines per row
- can generate interlaced or non-interlaced (312/312 or 312/313 lines) composite sync
- double-height characters can be selected by the viewer
- software control of data entry period for normal field flyback and full-channel transmissions
- internal field sync integrator
- internal signal quality detector
- odd/even field output for de-interlacing circuits.

Data acquisition

The data acquisition section is enabled by a signal from the timing chain during lines 2 to 22 inclusive for field-flyback transmissions, or during all lines for full-channel transmissions. Serial data from the VIP2 is clocked into the TTD (TeleText Data) pin with the 6.9375 MHz TeleText Clock (TTC). The serial data stream is converted to 8-bit wide parallel data bytes, and a byte counter keeps track of the incoming data and allocates it to the correct function.

The data acquisition section can search for, store in memory and continuously update four pages simultaneously because there are four different acquisition circuits. If no extension packet processing is required, up to eight pages may be stored, although only four of them are continuously updated.

Each teletext page is numbered using seven digits – one for magazine, two for page number and four for sub-pages (rolling pages). The ECCT's acquisition circuits can receive pages by checking any combination of these seven digits, ignoring those not required by using a 'don't care' facility. Besides decimal page numbers for use with conventional teletext broadcasts, the full hexadecimal range of page numbers can be requested for maximum flexibility in specialized data distribution systems.

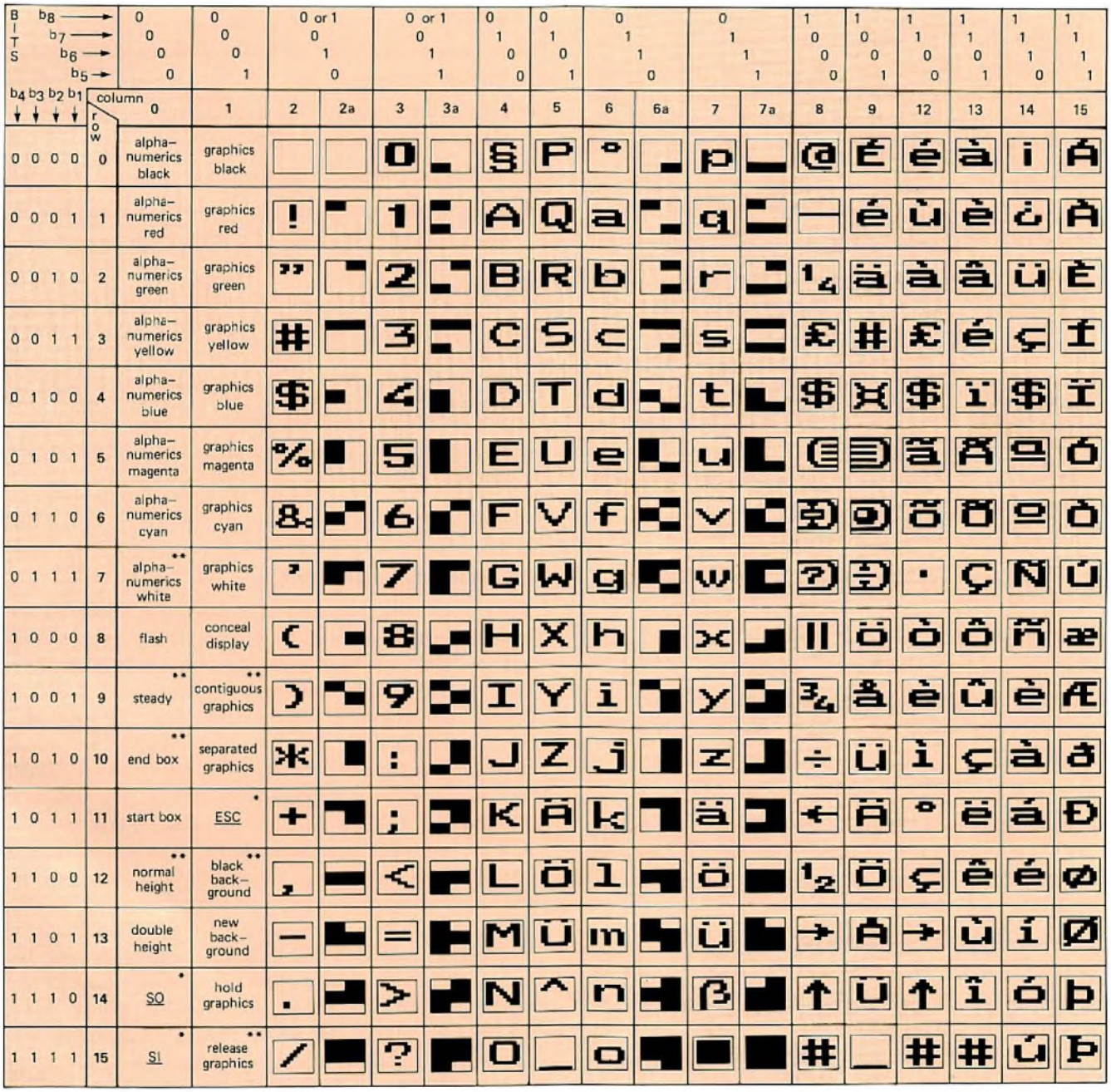
The main features of the data acquisition section are:

- accepts standard World System Teletext transmissions
- automatic selection of national character sets by decoding bits C12, C13, and C14 of the page header
- accepts up to 25 extension packets for processing by the control microcomputer. In this mode, each page requires 2 K bytes of memory, giving a maximum of 4 pages
- receives the following extension packets: X/24, X/25, X/26/0 to X/26/14, X/27/0, X/27/1, X/27/4, X/27/5, X/28/0, X/28/1, X/28/2, X/30
- can pass all transmitted control bits and addresses to a microcomputer for interpretation
- up to 4 simultaneous page requests are allowed in either field-flyback or full-channel mode
- software selection of field-flyback or full-channel data operation

- 'don't care' facility is available on magazine, page, and sub-code digits
- in field-flyback mode, automatic clearing of old page on first reception of new page, and clearing when page header bit C4 is set
- in full-channel mode, the clear functions are not available so pages should be transmitted non-row-adaptively
- central part of the page header rolls, in green, when the page in the display chapter is being looked for
- broadcast (rolling) time is always directed to the display memory
- 8-bit data reception option on all rows (for example, tele-software), or normal 7-bits plus parity (under software control)
- acquisition function may be switched off under software control.

Character generator

The ROM in the ECCT contains 192 characters, see Fig.9, each stored as a matrix of 12 dots horizontally and 10 dots vertically, improving legibility and display appearance compared with earlier circuits. The 192 characters are selected



* These control characters are reserved for compatibility with other data codes
** These control characters are presumed before each row begins

Fig.9 The ECCT code table

7Z96828.1

by character address decoding and the ten TV lines by ROM line address decoding. The ROM is accessed once per microsecond providing 12 outputs corresponding to the 12 dots in each line of a character. A 64 μs rate signal from the timing chain clocks a lines-per-row counter, which divides by ten (except when double-height characters are selected). The counter output is used to select the appropriate line of 12 dots in the ROM.

The outputs from the character generator for driving the video stages are R (red), G (green) and B (blue), pins 13, 14 and 15 respectively. The Y output (pin 18) is for controlling a printer and is active for the character foreground only, regardless of colours, and does not contain the flashing function. Blanking signals for the TV picture are supplied through the BLAN pin which is combined character, box, and full-screen blanking. Pin 16 ($\overline{COR}$) allows selective contrast reduction of the TV picture to enhance a mixed-mode display. All the character generator output pins are open-drain, making many different interfacing arrangements possible.

The main features of the character generator are:

- 12 x 10 dot matrix characters
- interlaced or non-interlaced display (software-controlled)
- serial attributes only
- 192 alphanumeric characters
- 6 national option character sets (English, German, Swedish, Italian, French and Spanish)
- 31-location auxiliary character set
- with suitable control software, all the major languages in Western Europe are covered
- Y output is foreground colour only
- BLAN output is combined character, box, and full-screen blanking
- $\overline{COR}$ output allows contrast reduction for superimpose or boxes (software controlled)
- user-selectable double height characters under software control. Large characters are then displayed quadruple-height
- double-height characters inhibited in row 23
- separate status row, always in single height, is available for software-generated messages. This may be displayed at the top or bottom of the screen (under software control)
- decoding for black foreground colour is provided
- internal cursor inverts background and foreground colours. It may be made to flash using a software loop in the control microcomputer.

Memory interface

The memory interface has 8 parallel data input/outputs (D0 to D7) and 13 address outputs (A0 to A12) which interface up to 8 K bytes of static RAM. The reading and writing of data to the RAM is controlled by the $\overline{OE}$ (output enable) and $\overline{WE}$ (write enable) signals. The RAM cycle is 500 ns with, in general, one write and one read cycle every microsecond. To summarize, the main features of the memory interface include:

- interface directly to 8 K RAM providing up to 8 stored pages in normal mode or 4 stored pages in extension packet mode
- 500 ns memory cycle time
- timings for static RAMs only, 200 ns access time is sufficient
- I^2C bus can address any RAM location for reading and writing
- address converter from row or column to 10 bits is included and addresses all 1024 locations
- all memory automatically cleared to 'space' at power-on
- separate address counters for display, data acquisition, and I^2C bus. I^2C bus address counters allow incrementing and presetting
- RAM locations not used for display or data acquisition purposes are available for use by the control microcomputer
- all RAM accesses (display, acquisition and I^2C bus) are synchronous with system clock
- all pages can be cleared, one at a time, under software control.

I^2C bus interface and control

The I^2C bus and control section are used to control the variable functions of the ECCT directly by altering the mode register bits, or indirectly via the external page memory. The I^2C bus slave transceiver accepts commands from the control microcomputer via the SDA (serial data) and SCL (serial clock) pins.

A command to one of the ECCT's mode registers follows the normal I^2C bus protocol (see Ref.5). The first byte contains the ECCT's slave address (0010001), with the R/W bit set to 0 to indicate 'write'. The second byte is interpreted as the register address required (R1 to R11), and the third byte is data to be loaded into that register. Subsequent bytes in the same I^2C transmission can be interpreted as data for the following register because the register address auto-increments. The register map for the ECCT is shown in Fig.10, with auto-increment being indicated by the arrows on the right of the diagram. The auto-increment allows several conditions to be set up by just one I^2C bus transmission. Register 11 is the address for accessing the external page memory. It is read/write as any

		D7	D6	D5	D4	D3	D2	D1	D0
Operating mode	R1	TA	$\overline{7+P}$/ 8 BIT	ACQ. $\overline{ON}$/OFF	EXTENSION PACKET ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0
Page request address	R2	–	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	R3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
Display chapter	R4	–	–	–	–	–	A2	A1	A0
Display control (normal)	R5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash/subtitle)	R6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	R7	STATUS ROW $\overline{BTM}$/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0
Active chapter	R8	–	–	–	–	CLEAR MEM.	A2	A1	A0
Active row	R9	–	–	–	R4	R3	R2	R1	R0
Active column	R10	–	–	C5	C4	C3	C2	C1	C0
Active data	R11	D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)

Fig.10 Register map of the ECCT. The arrows shown on the register map indicate that the register address auto-increments on the following I^2C transmission byte. TA (in register R1) and TB (in register R2) must be logic 0 for normal operation. All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold

RAM location can be read as well as written by the control software. All other registers are write only. The register bits have the following functions:

Register R1: Operating mode

D0, D1	interlace/non-interlace 312/313 line control
D2	text composite sync or direct sync select
D3	field-flyback or full-channel mode select
D4	extension packet enable
D5	data acquisition circuit enable/disable
D6	data reception select: 7-bit with parity check or 8-bit
D7	should be 0 for normal operation.

Regiser R2: Page request address

D0, D1, D2	defines the start column for page request data
D3	should be 0 for normal operation
D4, D5	selects one of four acquisition circuits
D6	selects the bank of 4 pages being addressed for acquisition.

Register R3: Page request data

D0 to D4	contains four groups of data (one for each acquisition circuit), allowing four simultaneous page requests, see Fig.11.

Register R4: Display chapter

D0, D1, D2	determines which of 8 pages is displayed.

Register R5 (normal) and R6 (newsflash/subtitle): Display control

D0, D1	picture on: inside (D0) and outside (D1) the boxed area
D2, D3	text on: inside (D2) and outside (D3) the boxed area
D4, D5	contrast reduction on: inside (D4) and outside (D5) the boxed area
D6, D7	background colour on: inside (D6) and outside (D7) the boxed area.

Start Column	PRD4	PRD3	PRD2	PRD2	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

X: bit not used.

Abbreviations:

MAG	magazine	page number
PU	page units	
PT	page tens	
MU	minutes units	page sub-code
MT	minutes tens	
HU	hours units	
HT	hours tens	

Fig.11 Register map for page requests. Register R3 contains four groups of data (one for each acquisition circuit) allowing four simultaneous page requests. The columns auto-increment on receipt of successive I^2C transmission bytes. When the DO CARE bit (PRD4) is set to 1, the corresponding digit for each group is taken into account for page requests. If the DO CARE bit is set to 0, each digit is ignored. This allows, for example, 'normal' or 'timed page' selection. If $\overline{\text{HOLD}}$ is set to 0, the page is held and not updated

Register R7: Display mode

D0, D1, D2	boxing function allowed on: row 0 (D0), rows 1 to 23 (D1), row 24 (D2)
D3	selects single or double height characters
D4	selects the top or bottom parts of the display
D5	used to reveal concealed areas of text
D6	cursor enable for reversing background and foreground colours
D7	determines whether row 25 is displayed below or above the main text.

Registers R8 to R11: Active chapter, row, column data

Registers R8 to R11 contain active chapter, row, column, and data information written to or read from the page memory via the I^2C bus.

To recap, the main features of the interface are:

- standard I^2C bus slave transceiver
- operates from 0 to 100 kHz
- acknowledge function
- position registers (R9 and R10) auto-increment after certain commands or may be directly addressed
- auto-increment between certain command registers as well as direct addressing
- all RAM locations accessible via the I^2C bus for reading and writing.

Software

The hardware of an ECCT-based teletext decoder is similar for many applications; it is the control software which determines the operating characteristics of the decoder, from the simplest stand-alone single-page decoder to a sophisticated multi-page decoder fully integrated into the design of the TV set. Software can interact with the programmable mode register bits in the ECCT or with the contents of the page memories. The I^2C bus interface allows the ECCT to be controlled by one microcomputer (as in Fig.4) or, in more complex systems, by several microcomputers, each performing a defined set of tasks (as in Fig.6). Other devices can be connected to the I^2C bus, depending on the facilities required, e.g. non-volatile memory, clock/calendar circuit, display driver, switching circuits, analogue control circuits. The way in which these devices are used depends entirely on the control software.

Many setmakers will prefer to write their own software to satisfy their own requirements. This also provides the opportunity to make a set different from that of other manufacturers. However, for those wishing to avoid the development costs of a custom design, a range of software packages for the ECCT is available.

Whatever the design of a decoder, the software is responsible for interpreting the commands from the remote control handset and controlling the corresponding ECCT registers in the desired way. For example, a control for double-height text may be desired. This could be implemented using three

buttons on the handset: 'large top', 'large bottom' and 'small'. Alternatively two buttons 'large' and 'small' could be used, with the 'large' command alternating between a 'large top' and 'large bottom' display. Another possibility would be to have only one button, giving sequentially 'large top', 'large bottom' and 'small' as a three-way toggle function. By writing the appropriate control software, the designer can make the ECCT operate in any of these ways.

In the simplest decoder, the control software deals with such functions and with requests for pages. It is also necessary to inform the user what is happening, so on-screen status messages must be generated, e.g. the requested page number, or the HOLD function. Within the constraints of the display, any message can be produced with appropriate software.

In the simplest decoder, only one page would be searched for at a time and only one acquisition circuit in the ECCT would be used. However, with the cost of standard RAM devices continuing to fall, a multi-page decoder giving the possibility of instant page access may be only marginally more expensive than a single-page decoder.

There are many ways of deciding which pages to capture, and again this function is set by the control software. For example, a user could store 'preferred' page numbers in non-volatile memory and request them in sequence by a 'next page' button. Another possibility would be for the broadcaster to determine which pages are associated with a given page, and to communicate this to the decoder by the 'linked page' extension packets (packets X/27). The decoder software can then read the associated page information from the ECCT memory, and make the appropriate page requests. Used in conjunction with an extra display row and coloured keys on the remote controller, this technique gives the FLOF/Fastext service now coming into operation in several countries.

As indicated earlier, the SAA5243E can display all the characters required for the major languages of Western Europe (Fig.12). Decoders for the more complex languages in Western Europe will require additional character-processing software. In some countries, extension packets X/26 are used to give supplementary characters, or to add accents to letters using the 'composition coding' technique. The X/26 packet information is received by the ECCT and stored in the extension packet area of page memory. Control software must read this data, interpret it and address the correct character via a software look-up table. This technique allows for many more languages than the English, German, Swedish, Italian and French national-option character sets selected automatically by the ECCT. With correct software, the following additional languages can be accommodated: Basque, Catalan, Danish, Faroese, Frisian, Gaelic, Greenlandic, Icelandic, Ladin, Portugese, Spanish and Welsh. These additional languages all rely on composition coding or supplementary characters transmitted via packets X/26 and will not be received correctly without the correct character processing software. Some other languages, such as Dutch, Finnish and Norwegian, use only the normal characters of a national option set and will be received correctly without character processing software.

For applications such as subscription teletext, telesoftware, VCR programming and videotex, clearly the software *and* the peripheral hardware of an ECCT-based decoder will have to be modified. For example, more memory, more powerful microcomputers and different interfacing to the decoder will usually be required compared with those for the mass-market application. Although designed for the consumer market, the price of enhanced computer-controlled teletext makes it attractive for other applications even when all its facilities are not used. For example, a simple VDU terminal could be constructed using the character generator without using the acquisition circuits. Or a high speed data distribution system for broadcast or cable networks could be provided using the acquisition circuits, without using the character generator.

Fig.12 All the characters required for the major languages of Western Europe can be displayed using the ECCT

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First multistandard decoder chip-set for DBS TV

INNOVATION THROUGH COOPERATION

It wasn't easy to meet the technological challenge of developing a DSB TV transmission decoder to handle signals encoded in accordance with any of the present European MAC packet standards (CMAC, DMAC and D2 MAC), and to also descramble and decrypt. It took the combined resources and expertise of Nordic VLSI, Plessey Semiconductors, and Europe's largest IC supplier, Philips. Nordic VLSI, with their unrivalled experience of MAC decoding designed the decoder and developed most of its 2 micron CMOS circuitry. Plessey Semiconductors will manufacture three of the full-custom VLSI CMOS ASICs at the heart of the decoder and also supply a teletext full-custom VLSI CMOS ASIC. To complete the decoder, Philips will develop the operating software (including decryption) and supply ICs from their extensive bipolar and MOS ranges to perform the analogue signal processing, computer control and data conversion functions.

This unique cooperation has led to the availability of the first-ever chip-set for constructing an advanced multi-standard MAC decoder which can enormously increase the market applicability of TV sets through its most innovative feature – multi-standard operation that meets all the requirements of today's European satellite TV market.

UNIQUE FEATURES OF A DECODER BUILT WITH THE CHIP-SET

- implements the full CMAC/DMAC/D2MAC packet standard
- can handle the standard MAC format for picture plus up to eight mono or four stereo sound channels
- is compatible with any TV set architecture
- a conditional access control feature allows descrambling and decryption of sound and vision signals (Pay TV) and teletext. This feature can handle several broadcasts simultaneously and meets the requirements of the new Part 6 of the EBU specification. Entitlements can be addressed over-air, via a smart-card or via a keyboard
- single- and double-cut conditional access descrambling of the vision signal as specified by the EBU
- very flexible packet multiplexing allows full-field sound/data transfer of up to 50 high-quality sound channels at a rate of nearly 20 Mbit/s
- all packet addresses in the selected data bursts are Golay decoded
- the configuration data can be changed without disrupting the service
- can handle teletext in accordance with the EBU specification during the frame interval or in the packet multiplex
- a second vision signal aspect ratio and decompression ratio will allow future high-definition TV (aspect ratio 16:9) to be accommodated whilst retaining compatibility with present standards (aspect ratio 4:3)
- linear or companded sound signals can be decoded
- processing of 1st and 2nd level error protection of the sound signal, including error concealment
- digital mixing allows simultaneous processing of stereo sound and commentary channels
- sound quality comparable with compact disc
- the decoder is software controlled.

MAIN FUNCTIONS OF THE MULTI-STANDARD MAC DECODER

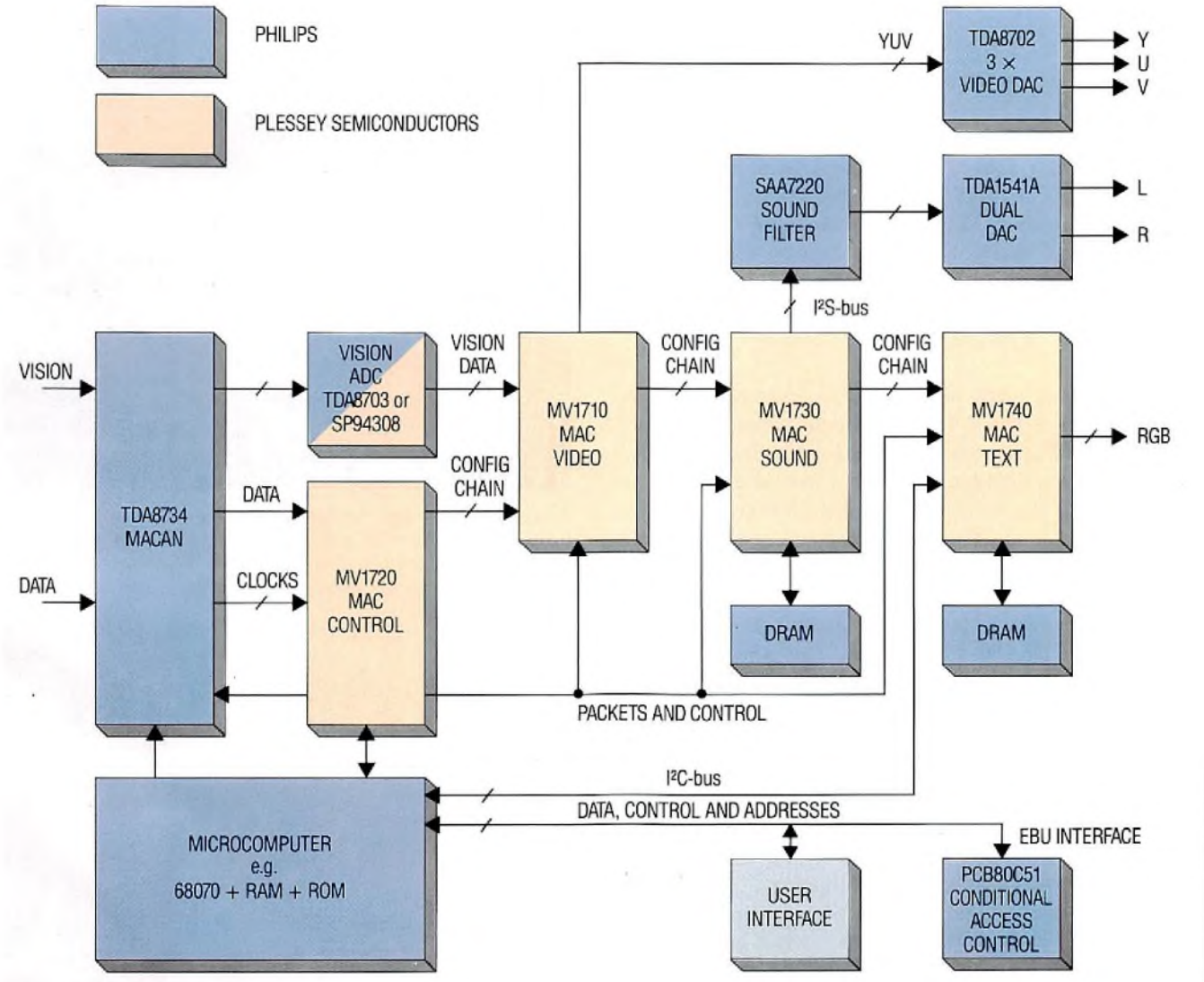
The main part of the decoder comprises four full-custom VLSI CMOS ASICs from Plessey Semiconductors; MAC control circuit MV1720, MAC video circuit MV1710, MAC sound circuit MV1730 and MAC teletext circuit MV1740. These are complemented by several Philips ICs; a MAC ANalogue (MACAN) circuit TDA8734 which performs analogue signal processing and includes functions such as data slicing, clock recovery and video clamping, a microcomputer comprising a microprocessor (e.g. the 16-bit 68070) plus RAM and ROM, and a conditional access control module incorporating a PCB80C51 8-bit microcontroller. Standard Philips ICs are also used for D to A and A to D conversion of the video signal (3 x TDA8702 and TDA8703 or Plessey SP94308 respectively), D to A conversion of the stereo sound signal (dual DAC TDA1541A), and for filtering the sound signal (SAA7220).

The conditional access control module handles both over-air and/or local addressing for decryption. It can either be detachable or can form a permanent part of the TV set. In either case, it's connected to the microcomputer via the EBU interface.

The user interface, in its minimum form, consists of pushbuttons and LEDs. A more advanced version would incorporate a keyboard for controlling menus and service identification data displayed on the screen of the TV set.

AN INNOVATIVE DESIGN THAT'S ALSO FUTURE-PROOF

In addition to being able to handle all of today's European DBS TV transmission standards, the architecture of this advanced multi-standard MAC decoder also facilitates extensions and will be able to accommodate the requirements of additional satellite TV services that may be defined in the future.



Block diagram of the multi-standard MAC decoder incorporating ICs from Philips and Plessey Semiconductors.

Research news

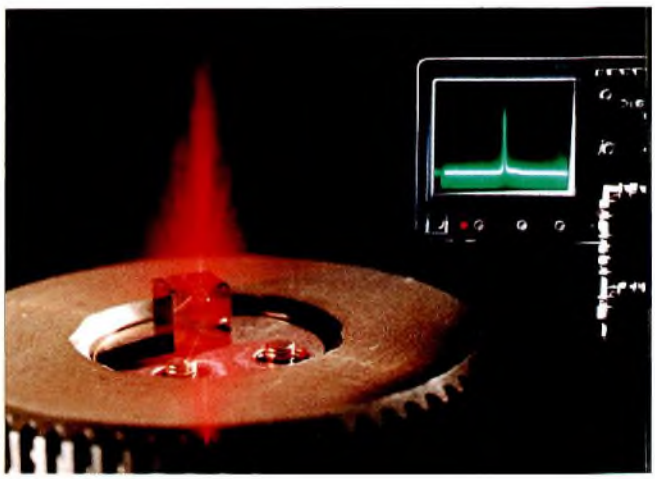
PHILIPS RESEARCH DEVELOPS SEMICONDUCTOR LASER THAT EMITS VISIBLE LIGHT

A semiconductor laser emitting light visible to the eye has been developed at Philips Research Laboratories. This laser, made of mixed crystals of aluminium, gallium, indium and phosphorus, emits light at a wavelength of 650 nm and is particularly suitable for digital optical recording, because of the high peak output power (more than 0.1 W). Contributions to this new development were made by researchers at the Philips Research Laboratories in Eindhoven and at the Laboratories d'Electronique et de Physique appliquee (L.E.P.), which are part of the Philips international research organisation.

Semiconductor lasers are used in professional products such as optical systems for telecommunication and data storage, as well as in consumer articles like the Compact Disc. For reading stored information, a semiconductor laser that emits light at a wavelength of about 800 nm is used at present. Reducing the wavelength can considerably increase the information density on a disc. This is why work is being carried out internationally on semiconductor lasers that emit light of sufficient intensity at about 600 nm. This is made possible by the specific choice of semiconductor material and the device structure.

The new semiconductor laser consists of a number of single-crystal layers of compounds of aluminium, gallium, indium and phosphorus of different composition and with different doping. These layers are deposited on a gallium arsenide substrate by vapour-phase epitaxy (VPE). The researchers at the two laboratories have now succeeded in optimizing the epitaxial deposition technology.

As a result, the materials obtained are of such purity and have such a perfect structure that the internal losses in the laser are minimal, so that light is produced with a high luminous efficiency.



A semiconductor laser operating at 650 nm. The actual laser is located at the front of a small 2-mm copper cube heatsink to ensure effective cooling. The oscilloscope image at the top right shows the spectrum of the radiated light

Abstracts

Two-chip modem for high-speed LAN systems

For local area networks a two-chip modem, incorporating the NE5080 transmitter and the NE5081 receiver, is available to allow communication over a coaxial cable at up to 8 Mbits/s. At 500 kbits/s, the cable can be as long as 30000 m without needing repeaters. By adding simple filters, it's possible to connect multiple modems to the same cable in a multichannel system.

Multiple-step stress testing proves the reliability of solid aluminium capacitors

Recent developments in solid aluminium (SAL) electrolytic capacitor manufacturing techniques have resulted in substantial increases in CV (capacitance x rated voltage) product density, making SALs comparable in size with miniature wet electrolytic and solid tantalum capacitors, and meeting today's high density circuit requirements. SALs, moreover, have no inherent long-term failure mechanisms, a fact already known from life tests on our 121 series and confirmed for our 123 series by multiple-step stress testing, a test procedure that produces in weeks what would take months or even years of standard life tests.

Third generation decoding ICs for CD players

Intended for use in players in the middle and low end of the market, two CMOS ICs (SAA7310 and SAA7320) together perform all the decoding functions, digital filtering and D/A conversion required in a CD player. The SAA7310 decoder retains all the features of its predecessor, the SAA7210. For CDI and CDROM applications, the SAA7310's interpolation circuitry can be turned off in software.
In the SAA7320, a four-times digital oversampling filter followed by another oversampling filter and a noise shaper simplify the design of the D/A converter – a novel 1-bit converter operating at 11.2 MHz and providing 16-bit resolution.

Single-heterojunction GaAlAs – a new technology for infrared LEDs and optocouplers

This technology, originally developed to provide brighter hyper-red LEDs, offers a significant improvement over rival GaAs and GaAlAs homojunction technology for infrared emitters. Advantages include higher operating speed, better reliability, linear radiant intensity/forward-current relation and a higher radiant intensity where it's needed (at low forward currents for CMOS driven optocouplers and high forward currents for the high-output IR LEDs used in remote controls).

Highly-accelerated humidity testing of CMOS ICs

The effect of humid environments on encapsulated ICs is of critical importance in many applications. Normal testing procedures to investigate these effects can take up to a year so clearly a shorter test is desirable. This article details results of investigations into several combinations of temperature and pressure that establish acceleration factors for various failure mechanisms likely to be encountered in CMOS ICs. One set of test conditions, the 132.9/85 test (132.9°C, 85% RH) has now been selected as our standard test for the routine quality control of CMOS ICs, enabling us to detect and eliminate incipient problems at an early stage.

New pinouts for ACL add reliability and simplicity to logic systems

The fast edges associated with high-speed logic like ACL can cause transients at the internal supply connections, reducing the effective supply voltage to the chip and causing transients at any unswitched outputs. This degrades system reliability by reducing noise margins and speed, and causing loss of stored data and false switching. To overcome this for ACL ICs, we've used edge-control circuitry to limit the di/dt of the output transistors during turn-on without reducing it during turn-off. The output drive current is maintained at 24mA to permit incident wave switching with 50Ω or 75Ω transmission line loads. We've also relocated the supply pins to the centre of opposite sides of the package to minimize their inductance. ICs with more than two outputs that can switch simultaneously have multiple parallel-connected Vcc and GND pins to reduce their inductance yet further.

Video ADCs using folding and interpolation techniques

A range of A/D video converters for consumer applications has been developed. A proprietary design incorporating analogue pre-processing slashes the number of latches and comparators required compared with full-parallel flash converters. Originally developed for digital TV systems and MAC satellite TV, the converters out-perform some of the best professional converters on the market. For example, each has an 8-bit effective resolution up to 8 MHz, yet dissipates less than 300 mW. Within the 5 MHz video band, every distortion component is below −60 dB.

Enhanced computer-controlled Teletext circuit SAA5243

The SAA5243 IC can form the heart of a teletext decoder that takes full account of the increasingly complex requirements of the teletext market. Although designed for the standard mass-market television application, the SAA5243 can also be used in high-speed data distribution systems for broadcast or cable networks, for example. Using a set of 192 characters, the ECCT circuit covers *all* the languages required in Western Europe. When controlled with suitable software, a teletext decoder using the SAA5243 can be used anywhere in Western Europe with the correct characters displayed automatically.

Zweichip – Modem für schnelle LAN-Systeme

Für lokale Netzwerke ist ein Zweichip-Modem mit dem NE5080-Sender und dem NE5081-Empfänger verfügbar, das die Datenübertragung über ein Koaxialkabel mit bis zu 8 Mbit/s möglich macht. Bei 500 kbit/s kann das Kabel 30000 m lang sein, ohne dass Verstärker erforderlich sind. Wenn einfache Filter hinzugefügt werden, können bei einem Mehrkanal-System mehrere Modems an das gleiche Kabel angeschlossen werden.

Beschleunigter Mehrstufen-Lebensdauertest beweist die Zuverlässigkeit von Trockenaluminiumkondensatoren

Neue Entwicklungen bei Fertigungsverfahren für Trockenaluminium-Elektrolytkondensatoren (solid aluminium electrolytic capacitor, SAL) haben zu einer erheblichen Steigerung des CV-Wertes (Kapazität x Nennspannung) geführt, so dass die SAL-Elkos in ihrer Grösse mit miniaturisierten Nasselektrolytkondensatoren und Trockentantalkondensatoren vergleichbar sind und die Anforderungen moderner Schaltungen mit hoher Packungsdichte erfüllen. SAL-Elkos weisen jedoch keine technologiebedingten langfristigen Fehler-Mechanismen auf. Dies zeigte sich bereits bei den Lebensdauertests für unsere Serie 121 und wurde durch den beschleunigten Mehrstufen-Lebensdauertest mit mehrfacher, gleichzeitiger Beanspruchung für unsere Serie 123 bestätigt. Mit diesem Testverfahren lassen sich innerhalb von Wochen die Ergebnisse erzielen, die bei gewöhnlichen Lebensdauertests erst nach Monaten oder selbst nach Jahren vorliegen.

Dritte Generation von Decoder-ICs für CD-Spieler

SAA7310 und SAA7320 sind zwei für den Einsatz in CD-Spielern der mittleren und unteren Preisklasse bestimmte CMOS-ICs, die zusammen alle im CD-Spieler benötigten Funktionen ausführen: Decodierung, digitale Filterung und D/A-Umsetzung. Der Decoder SAA7310 verfügt über alle Leistungsmerkmale seines Vorgängers SAA7210. Für CD-I- und CD-ROM-Anwendungen lässt sich die SAA7310-interne Interpolationsschaltung per Software abschalten. In der Digitalfilterschaltung SAA7320 wird eine hochlineare D/A-Umsetzung mit 16 bit Auflösung angewandt, realisiert mit digitalem 4-fach-Oversampling-Filter, einem weiteren Oversampling-Filter, einem Rauschbegrenzer sowie einem 1 bit-D/A-Umsetzer, dessen Abtastfrequenz 11.28 MHz beträgt.

Einfach-Heterosperrschicht-GaAlAs – eine neue Technologie für IR-LEDs und Optokoppler

Diese Technologie, die ursprünglich entwickelt wurde um besonders lichtstarke rote LEDs herzustellen, bietet gegenüber der bei Infrarotstrahlern mit GaAlAs-Homosperrschicht verwendeten bedeutende Verbesserungen: höhere Arbeitsgeschwindigkeit, grössere Zuverlässigkeit, lineares Verhältnis von Strahlstärke zu Durchlassstrom und ferner höhere Strahlstärkewerte dort, wo sie erforderlich sind (bei den geringen Durchlassströmen für CMOS-gesteuerte Optokoppler und bei den grossen Durchlassströmen für Hochleistungs-IR-LEDs in Fernbedienungen).

Wesentlich schnellerer Feuchtigkeitstest für CMOS-ICs

Der Einfluss von Luftfeuchtigkeit auf gekapselte ICs ist bei vielen Anwendungen überaus wichtig. Herkömmliche Testverfahren zur Untersuchung des Feuchtigkeitseinflusses können bis zu einem Jahr dauern, so dass ein kürzerer Test wünschenswert ist. Dieser Artikel beschreibt ausführlich die Untersuchungsergebnisse für einige Kombinationen von Temperatur und Druck, durch die verschiedene Fehlermechanismen, die bei CMOS-ICs auftreten können, beschleunigt werden. Wir haben als Standardtest für die routinemässige Qualitätsprüfung der CMOS-ICs eine bestimmte Kombination von Bedingungen (132.9°C, 85% rF) gewählt, so dass wir in einem frühen Stadium die beginnenden Probleme erkennen und beheben können.

Neues Design von ACL-ICs macht logische Systeme einfacher und zuverlässiger

Steile Flanken können zusammen mit Hochgeschwindigkeitslogik wie ACL zu Stromspitzen bei den internen Versorgungsanschlüssen führen, so dass die effektive Speisespannung des Chips herabgesetzt wird und Stromspitzen an allen nicht geschalteten Ausgängen verursacht werden. Die Zuverlässigkeit des Systems wird aufgrund von kleineren Störabständen und verringerter Geschwindigkeit reduziert, wodurch es zum Verlust von gespeicherten Daten und zu falschem Schalten kommt. Um dies bei ACL-ICs zu vermeiden, haben wir flankengesteuerte Schaltungen verwendet, die das di/dt der Endstufentransistoren während des Einschaltens begrenzen, ohne es beim Ausschalten zu reduzieren. Der Ausgangsansteuerungsstrom wird auf 24mA begrenzt, um Schaltsignale auf eine Last mit 50Ω oder 75Ω Wellenwiderstand geben zu können. Wir haben auch die Versorgungsanschlüsse zur Mitte der gegenüberliegenden Seiten des Gehäuses verlegt, um die Induktivität auf ein Minimum zu reduzieren. ICs mit mehr als zwei gleichzeitig schaltbaren Ausgängen haben mehrfach parallelgeschaltete Ucc− und Masseanschlüsse, um die Induktivität noch weiter zu verringern.

8-bit-A/D- Umsetzer mit Faltungs- und Interpolationstechnik

Es wurde eine Reihe von A/D-Videosignal-Umsetzern für Anwendungen in der Unterhaltungselektronik entwickelt. Durch einen speziellen Entwurf mit analoger Vorverarbeitung wird die Anzahl der erforderlichen Komparatoren und Auffangregister im Vergleich zu vollparallelen sogenannten Flash- Umsetzern erheblich verringert.

Die neuen Umsetzer, die ursprünglich für digitale Fernsehsysteme entwickelt wurden, sind leistungsstärker als einige der besten angebotenen professionellen Umsetzer. So haben sie z.B. bis zu einer Frequenz von 8 MHz eine effektive Auflösung von 8 bit, obgleich ihre Verlustleistung weniger als 300 mW beträgt, und jede bei der Umsetzung verursachte Verbesserungskomponente liegt innerhalb des 5 MHz-Videobandes under −60 dB.

Erweiterte computergesteuerte Teletext-Schaltung SAA5243 (ECCT)

Die integrierte Schaltung SAA5243 ECCT (Enhanced Computer Controlled Teletext) ist das Schlüsselbauelement eines modernen Videotextdecoder-Konzeptes, das die immer komplexer werdenden Anforderungen des Videotext-Marktes voll abdeckt. Das IC wurde zwar ursprünglich für Standard-Fernsehanwendungen entwickelt, lässt sich aber beispielsweise auch in kabelgebundenen Hochgeschwindigkeits-Datenverteilungssystemen für Fernsehen oder büro-interne Kommunikation einsetzen. Mit einem Zeichenvorrat von 192 Zeichen deckt die ECCT-Schaltung alle in Westeuropa benutzten Sprachen ab. Bei Steuerung mit geeigneter Software kann ein auf SAA5243 basierender Videotextdecoder in ganz Westeuropa eingesetzt werden, wobei die Bildschirmwiedergabe automatisch die richtigen Zeichen umfasst.

Modem deux puces pour réseaux locaux ultrarapides

Les réseaux locaux peuvent maintenant être équipés d'un modem à deux puces, incorporant l'émetteur NE5080 et le récepteur NE5081 et permettant la transmission par un câble coaxial de jusque 8 méga-octets/s. A 500 kilo-octets/s, le câble peut atteindre une longueur de 30.000 m sans utilisation de répéteurs. Par l'addition de simples filtres, il est possible de connecter des modems multiples au même câble dans un système multivoie.

Des tests accélérés, par augmentation simultanée des différents paramètres, démontrent la fiabilité des condensateurs aluminium à électrolyte solide "Alusolid"

De récents développements des techniques de fabrication des condensateurs Alusolid ont abouti à des accroissements appréciables de la densité (produit de la capacité par la tension nominale). Les dimensions de ces condensateurs sont devenues comparables à celles des condensateurs à électrolyte liquide miniatures et des condensateurs au tantale, répondant ainsi aux impératifs des circuits à haute densité. En outre, les condensateurs Alusolid ne sont pas affectés de mécanismes de défaillance à long terme, comme l'ont déjà montré les tests de durée de vie effectués sur notre modèle 121 et comme l'ont confirmé les tests accélérés pratiqués sur notre modèle 123. Il y a lieu de noter que la procédure de tests accélérés accomplit en quelques semaines ce qui nécessiterait des mois ou des années par les tests de durée de vie classiques.

Décodeurs de la troisième génération pour lecteurs CD

Destinés à être employés dans des lecteurs de milieu et de bas de gamme, deux circuits intégrés CMOS (SAA7310 et SAA7320) assurent conjointement toutes les opérations de décodage, de filtrage numérique et de conversion numérique/analogique nécessaires dans un lecteur CD. Le décodeur SAA7310 conserve toutes les fonctions de son prédécesseur, le SAA7210. La logiciel est conçu pour rendre inopérants les circuits d'interpolation du SAA7310 dans les applications CDI et CD-ROM. Dans le SAA7320, la conception du convertisseur numérique/analogique – un nouveau convertisseur 1 bit fonctionnant à 11.2 MHz et assurant une résolution de 16 bits – est simplifiée par l'emploi d'un filtre de suréchantillonnage numérique de facteur quatre, suivi par un autre filtre de suréchantillonnage et par un conformateur de bruit.

Hétérojonction unique au GaAlAs – une nouvelle technologie pour les diodes électroluminescentes infrarouges et les coupleurs optiques

Cette technologie, développée à l'origine pour réaliser des diodes électroluminescentes hyper-rouges plus efficaces, constitue une amélioration sensible par rapport à la technologie rivale à homojonction GaAs et GaAlAs pour émetteurs d'infrarouges. Ses avantages sont notamment une plus grande fiabilité, une relation linéaire entre intensité lumineuse et courant direct, et une intensité plus lumineuse élevée dans les cas où c'est nécessaire (aux courants directs faibles pour les coupleurs optiques commandés par CMOS, aux courants directs élevés pour les diodes électroluminescentes infrarouges de puissance élevés employées dans les télécommandes).

Test d'humidité ultra-accélérés pour circuits intégrés CMOS

Les effets de l'humidité ambiante sur les circuits intégrés encapsulés deviennent critiques dans de nombreuses applications. L'étude de ces effets par la procédure de test normale pouvant prendre jusqu'à un an, un test plus rapide est très souhaitable. L'article détaille les résultats de l'étude de plusieurs combinaisons de température et de pression qui déterminent des coefficients d'accélération pour divers mécanismes de défaillance pouvant affecter les circuits intégrés CMOS. Nous avons choisi un de ces ensembles de conditions, le test 132.9/85 (132.9°C, humidité relative 85%), comme test standard pour le contrôle de qualité de routine des circuits intégrés CMOS. Nous serons ainsi en mesure de détecter et d'éliminer les problèmes latents à un stade précoce.

Le nouveau brochage de sortie pour la famille ACL apporte fiabilité et simplicité aux systèmes logiques

Les fronts d'onde rapides produits par les circuits logiques ultrarapides tels ceux de l'ACL peuvent générer des transitoires aux connexions d'alimentation internes, réduisant ainsi la tension d'alimentation effective de la puce et générant des transitoires aux sorties non commutées. Ces transitoires diminuent la fiabilité des systèmes en réduisant les marges de bruit et la vitesse et en provoquant des pertes de données en mémoire et des commutations erronées. Afin de résoudre ce problème pour les circuits ACL, nous avons utilisé des circuits de contrôle de front d'onde pour limiter le di/dt des transistors de sortie lors de la mise sous tension, sans le réduire lors de la mise hors tension. Le courant de commande de sortie est maintenu à 24 mA pour permettre la commutation des ondes incidentes avec des charges de la ligne de transmission de 50 Ω ou 75 Ω. D'autre part, les broches d'alimentation ont été repositionnées au centre des deux rangées de broches du boîtier pour minimiser leur inductance. Les circuits intégrés comportant plus de deux sorties pouvant commuter simultanément sont équipés de broches V_{CC} et terre multiples, connectées en parallèle pour réduire encore plus leur inductance.

Convertisseurs analogiques-numériques vidéo 8 bits utilisant des techniques de repliement et d'interpolation

Une gamme de convertisseurs analogiques-numériques vidéo pour applications grand public à été développée. Une conception exclusive avec prétraitement analogique a permis de réduire considérablement le nombre des bascules et comparateurs nécessaires par rapport aux convertisseurs de type "flash". Développés pour les systèmes de télévision numériques et la télévision MAC par satellite, ces convertisseurs dépassent par leurs performances certains des meilleurs convertisseurs professionels existant sur le marché. Par exemple, chacun d'eux a une résolution effective de 8 bits jusqu'à 8 MHz, tout en dissipant moins de 300 mW. Dans la bande vidéo 5 MHz, chaque composant de distorsion est inférieur à −60 dB.

Le circuit télétext perfectionné SAA5243 à gestion par ordinateur

Le circuit intégré SAA5243 peut constituer le coeur d'un décodeur télétexte capable de remplir les fonctions de plus en plus complexes qu'exigent les besoins du marché. Bien que conçu pour des applications courantes en télévision grand public, le SAA5243 peut également être utilisé dans des systèmes ultrarapides de distribution de données pour la télédiffusion ou la télédistribution, par exemple. Ce circuit, qui utilise un jeu de 192 caractères, couvre *toutes* les langues d'Europe occidentale. A condition d'être géré par un logiciel approprié, un décodeur télétexte équipé du SAA5243 peut être utilisé n'importe où en Europe occidentale, avec visualisation automatique des caractères corrects.

Modem de dos chips para sistemas LAN de gran velocidad

Se trata de un dispositivo con transmisor NE5080 y receptor NE5081 para redes de cobertura local, que permite las comunicaciones por cable coaxial con velocidades de hasta 8 Mbits/s. A 500 kbits/s, la longitud del cable alcanza los 30 km sin necesidad de repetidores. Añadiendo filtros sencillos es posible conectar múltiples modems al mismo cable en sistemas multicanal.

Pruebas de vida de múltiples pasos prueban la fiabilidad de los condensadores de aluminio sólido

Los últimos avances en las técnicas de fabricación de condensadores electrolíticos de aluminio sólido (SAL, Solid Aluminium) han dado lugar a un aumento importante del producto CV (capacidad x tensión nominal), lo que los hace comparables en tamaño con los condensadores miniatura de electrolítico húmedo y tántalo sólido, y cumplen los requisitos de circuito de alta densidad actuales. No obstante, los condensadores SAL no tienen inherente mecanismos de fallo a largo plazo, hecho ya conocido de las pruebas de vida sobre nuestra serie 121 y confirmado por nuestra serie 123 mediante pruebas de esfuerzo de múltiples pasos, que es un procedimiento de prueba que produce en semanas los que obtendríamos en meses o incluso años de las pruebas de vida estándar.

Tercera generación de circuitos integrados decodificadores para lectores de disco compacto

Concebidos para funcionar en aparatos de media y baja calidad del mercado, los dos circuitos integrados CMOS (SAA7310 y SAA7320) relaizan todas las funciones de decodificación, filtrado digital y conversión de digital a analógica (D/A) de los lectores de disco compacto (CD). El decodificador SAA7310 conserva todas las características del anterior, el SAA7210. Para aplicaciones en CDI y CDROM, los circuitos de interpolación, del SAA7310 se pueden desactivar en el programa. En el SAA7320, un cuádruple filtro digital de sobremuestreo y un conformador de ruido simplifican el diseño del convertidor D/A – un nuevo convertidor de 1 bit que opera a 11.2 MHz y proporciona una resolución de 16 bits.

GaAlAs de heterounión sencilla: una nueva técnica para los diodos emisores de luz y los optoacopladores

Esta tecnología, desarrollada en principio para conseguir diodos emisores de luz hiperrojos más brillantes, ofrece considerables ventajas en comparación con la tecnología de homounión de GaAs y GaAlAs para los emisores de infrarrojos. Estas ventajas son: mayor velocidad de funcionamineto, mejor fiabilidad, mejor relación intensidad radiante lineal/corriente directa y más elevada intensidad radiante donde sea necesario (a bajas corrientes directas para dispositivos CMOS excitados por optoacopladores y corrientes directas elevadas para los diodos emisores de luz infrarroja de gran potencia que se emplean en los mandos a distancia).

Ensayos muy rápidos de humedad de circuitos integrados CMOS

El efecto de los ambientes húmedos sobre los circuitos integrados encapsulados es de importancia crítica en numerosas aplicaciones. Los procedimientos normales de ensayo para estudiar dichos efectos pueden durar hasta un año, por lo que obviamente se exigen ensayos de menor duración. En este artículo se detallan los resultados de las investigaciones con varias combinaciones de temperaturas y presiones que determinan los factores de aceleración con que se producen algunos mecanismos de avería en dichos circuitos. El ensayo 132.9/85 (132.9°C, 85% h.r.) se ha tomado por norma de los ensayos de control de la calidad de los circuitos integrados CMOS, lo que permite detectar y eliminar de raiz las averías incipientes.

Nuevos terminales de salida para ACL añaden seguridad y sencillez a los sistemas lógicos

Los flancos rápidos asociados a los circuitos lógicos de gran velocidad, como los ACL pueden causar transitorios en las conexiones internas de alimentación, reduciendo la tensión útil que llega al chip y produciendo transitorios en las salidas sin conectar. Esto degrada la seguridad del sistema al reducir los márgenes de ruido y velocidad y causa la pérdida de los datos almacenados y conexiones falsas. Para superar dichas dificultades en los circuitos integrados ACL se han empleado circuitos de control de flanco para limitar la di/dt de los transistores de salida durante el paso a conducción, sin reducirla en el paso a bloquear la corriente de excitación de salida se mantiene en 24 mA para permitir conexiones de onda incidente con cargas de línea de transmisión de 50 Ω a 75 Ω También se han cambiado las posiciones de los terminales de alimentación al centro de los lados opuestos del encapsulado para reducir al mínimo su inductancia. Los circuitos integrados con más de dos salidas que pueden commutar simultáneamente, tienen varios terminales de V_{cc} y de masa conectados en paralelo para reducir aún más su inductancia.

Convertidores A/D de video de 8 bits con técnicas de plegado e interpolación

Se ha desarrollado una gama de convertidores A/D de video para aplicaciones de consumo. Diseño patentado pre-procesado analógico reduce radicalmente el número de comparadores y registros en comparación con los convertidores de destello totalmente paralelo.
Diseñados en principio para los sistemas de televisón digital y por satélite MAC, sus prestaciones con superiores a las de algunos de los mejores convertidores profesionales del mercado. Por ejemplo, tienen una resolución útil de 8 bits hasta 8 MHz, pero con un consumo inferior a 300 mW. Dentro de la banda de imagen de 5 MHz, todos los componentes de distorsión quedan por debajo de −60 dB.

Nuevo circuito de teletexto controlado por ordenador SAA5243

El circuito integrado SAA5243 puede ser el corazón de un decodificador de teletexto que cumple las crecientes y complejas exigencias del mercado de teletexto. A pesar de estar concebido para aplicaciones normales del mercado de televisión pública, el SAA5243 se puede usar también en sistemas distribuidores de datos de gran velocidad para redes de radiodifusión o por cable, por ejemplo. El circuito ECCT lleva un juego de ciento noventa y dos caracteres, que cubre todos los idiomas europeos occidentales. Cuando es controlado mediante un software adecuado, un decodificador de teletexto que emplea el SAA5243 puede usarse en toda Europa Occidental con los caracteres correctos visualizados automáticamente.

Authors

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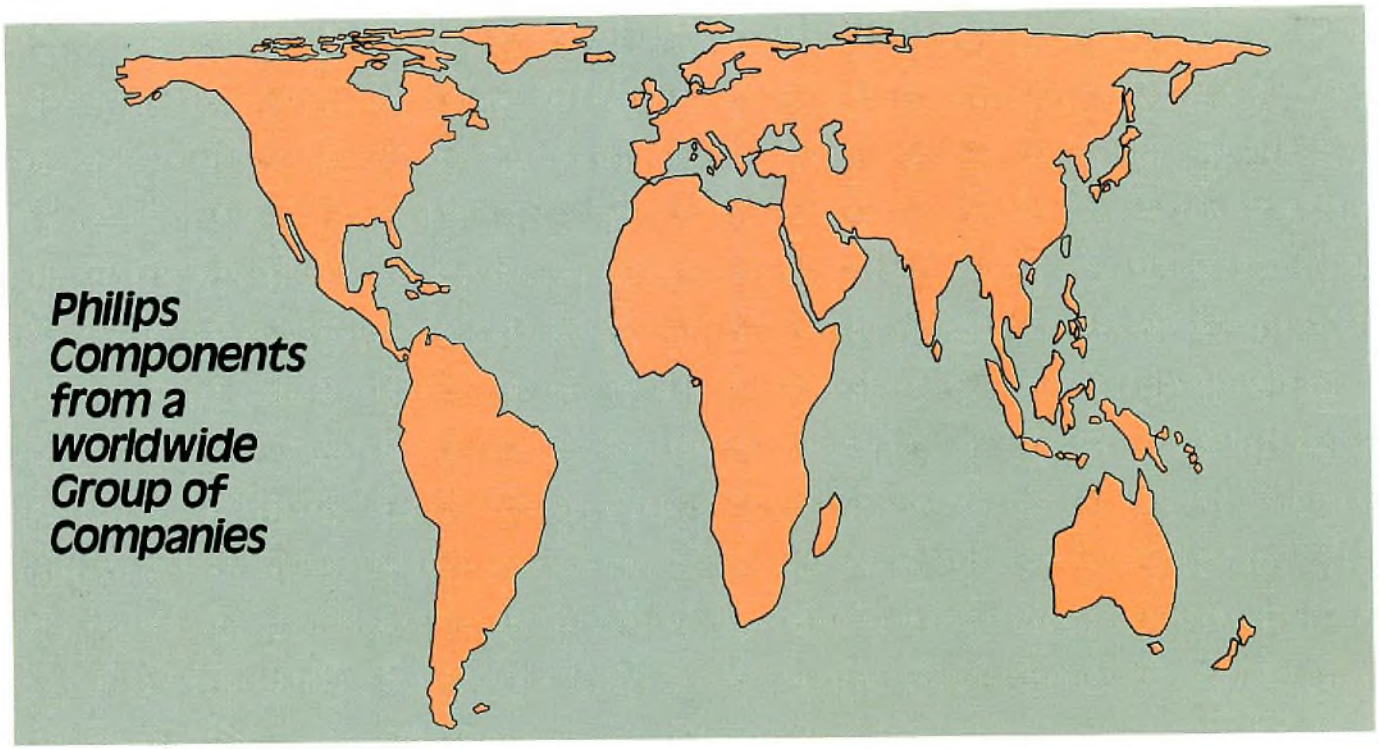

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