Electronic components & applications

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When Christopher Columbus set sail for the Indies in 1492, all he had to guide him were his compass, his knowledge of the heavens and his sailor's insight. In those days there were no official charts to aid him, no chronometers to help him calculate longitude, and the sextant was more than 100 years in the future! Contrast that with the host of electronic navigation aids available to the sailors of today. Like the crew of The Philips Innovator currently competing in the Whitbread Round the World Race. To help them on their voyage they have a Philips 'ap navigator' for coastal navigation, a Magnavox MX 4102 satellite navigator, and a facsimile receiver for supplying them with weather charts. For communication they have the latest Mariphone equipment plus telex facilities. No doubt all this would have greatly impressed Columbus. But if he'd possessed it, maybe he would have found his route to the Indies after all — and who knows, maybe America would still be undiscovered!

Astable multivibrators using HCMOS ICs

R. VOLGERS

74HC/HCT/HCU high-speed CMOS (HCMOS) logic ICs dissipate little power, have a wide operating voltage and temperature range and a low temperature coefficient of the input switching threshold voltage. This makes them ideal for constructing simple yet reliable astable multivibrators in which the operating frequency is determined by a single RC network. What's more, the high impedance of HCMOS inputs allows a wide range of switching time-constants (wide frequency range) to be selected without using high value capacitors which would increase the dynamic power dissipation. This article describes a basic astable circuit using two 74HC/HCU or two 74HCT inverting gates or buffers and derives simple formulae for accurately determining its operating frequency. It then develops the formulae to show how adding one resistor to the circuit makes the operating frequency and duty factor more independent of supply voltage variations and input switching threshold voltage spreads, and limits the input current. The article concludes by discussing the effect of temperature variations, the dynamic power dissipation and the range of external component values and supply voltage that can be used for the circuit.
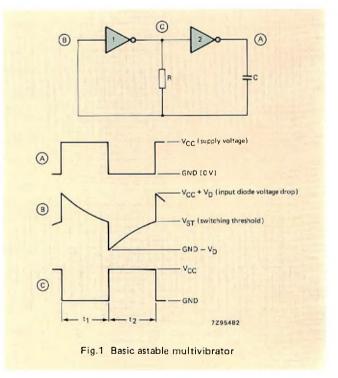
BASIC ASTABLE MULTIVIBRATORS

Figure 1 illustrates the circuit arrangement and waveforms for a basic astable multivibrator using two HCMOS inverters. When the supply voltage (V_{CC}) is applied to the circuit, the potential at points A and B will be of opposite polarity to that at point C (e.g. points A and B LOW, point C high). The capacitor then begins to charge and the potential at point B approaches the switching threshold voltage (V_{ST}) of inverter 1. When the voltage at point B reaches V_{ST}, the output of inverter 1 (point C) goes LOW, and the output of inverter 2 (point A) goes HIGH. Because the level change at point A is rapid, it is transferred to point B. However, point B is clamped within the limits $V_{CC} + V_D$

and $GND - V_D$ by the input protection network of inverter 1. The potential at point B now approaches V_{ST} again and, when it reaches that level, the circuit again changes state and the cycle repeats. The equations for switching periods t_1 and t_2 are:

$$t_1 = -RC \ln \frac{V_{ST}}{V_{CC} + V_D} \tag{1}$$

$$t_2 = -RC \ln \frac{V_{CC} - V_{ST}}{V_{CC} + V_D} \tag{2}$$

$$t_1 + t_2 = -RC \ln \frac{V_{ST}(V_{CC} - V_{ST})}{(V_{CC} + V_D)^2} \tag{3}$$

Fig.1 Basic astable multivibrator

Influence of supply and switching threshold voltage variation

For a circuit using a 74HC/HCU IC with $V_{ST} = 0,5\ V_{CC}$ and $V_D = 0,7\ V$, the switching period varies by +9% and −2,5% around the value at $V_{CC} = 5\ V$ over the supply voltage range 3 V to 6 V. This variation is due to the influence of the forward voltage drop across the input protection diodes of inverter 1 ($V_D = 0,7\ V$) which causes the value

$$\ln \frac{V_{ST}}{V_{CC} + V_D}$$

to vary with supply voltage variations even though V_{ST} is a constant percentage of V_{CC}. Since V_{ST} nom. is 0,5 V_{CC} for 74HC and 74HCU ICs, the peaks of the voltage at point B in Fig.1 are symmetrical around V_{ST}, resulting in a duty factor of 0,5 which is independent of supply voltage variations. However, the nominal switching threshold voltage is subject to a spread (0,3 V_{CC} to 0,7 V_{CC} for 74HC ICs and 0,2 V_{CC} to 0,8 V_{CC} for 74HCU ICs). This causes the total switching period to increase by a maximum of 10,5% for a circuit using a 74HC IC and 27% for a circuit using a 74HCU IC. The switching threshold voltage spread also causes the duty factor to spread between the limits 0,7 to 0,3 for a circuit using a 74HC IC, and 0,8 to 0,2 for a circuit using a 74HCU IC.
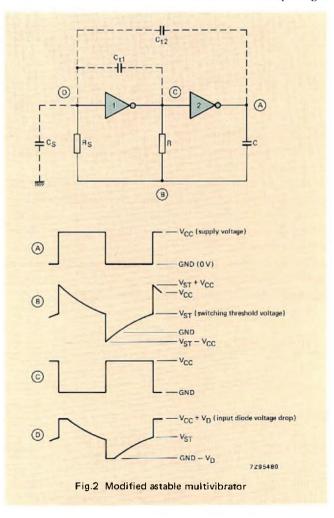
For a circuit using a 74HCT IC, the nominal V_{ST} is 1,3 V at $V_{CC} = 4,5\ V$, 1,415 V at $V_{CC} = 5\ V$ and 1,53 V at $V_{CC} = 5,5\ V$. The switching threshold voltage is therefore always below the midpoint of the total voltage swing at point B in Fig.1, and is not a constant percentage of the supply voltage. Because the supply voltage range for 74HCT ICs is only 4,5 V to 5,5 V, the value

$$\ln \frac{V_{ST}}{V_{CC} + V_D}$$

varies less over the supply voltage range than it does for a circuit using a 74HC/HCU IC, resulting in a switching period variation of ±0,8% around the value at $V_{CC} = 5\ V$ over the supply voltage range. However, because the voltage swing at point B in Fig.1 is asymmetrical around V_{ST}, the periods calculated with equations (1) and (2) are unequal, resulting in duty factors of 0,74 at $V_{CC} = 4,5\ V$, 0,75 at $V_{CC} = 5\ V$ and 0,76 at $V_{CC} = 5,5\ V$. Furthermore, the nominal V_{ST} of 74HCT ICs is subject to a spread of about ±0,5 V. With a 5 V supply, this causes a maximum switching period increase of 16% above the nominal value, and a duty factor spread from 0,8 to 0,6.

CIRCUIT MODIFICATION TO REDUCE SWITCHING PARAMETER VARIATIONS

Figure 2 shows the astable multivibrator circuit modified by the addition of resistor R_S in series with the input to inverter 1. This resistor increases the resistance between point B and the input to inverter 1, and thereby prolongs the discharge of capacitor C via the input protection network of inverter 1 each time the polarity of the charge on capacitor C reverses. If the value of R_S is high enough, the voltage at point B will reach the limits $V_{CC} + V_{ST}$ and $V_{ST} - V_{CC}$ before the voltage at point D reaches the switching threshold voltage. Since the waveform at point B now swings by $\pm V_{CC}$ around V_{ST}, it is always symmetrical about V_{ST} regardless of the value of V_{ST} or V_{CC}. If the value of R_S is too low, the peaks of the waveform at point B will be clipped; if it is too high and a buffered 74HC IC is being used, spurious oscillations or glitches may occur due to stray capacitance C_{t1} causing phase-shifted feedback around inverter 1. It is therefore preferable to use the unbuffered Hex Inverter 74HCU04 for this circuit. The optimum value for R_S is 2R. It will be shown later that increasing the value of R_S beyond 2R doesn't result in any further improvement of the performance of the circuit. The waveform at the input to inverter 1 (point D) is clamped by the input protection diodes to $V_{CC} + V_D$ for positive-going swings, and to $-V_D$ for negative-going swings, but resistor R_S limts the current flow through the input protection network during these periods. The presence of R_S therefore also reduces crosstalk to other inverters in the same package.

Fig.2 Modified astable multivibrator
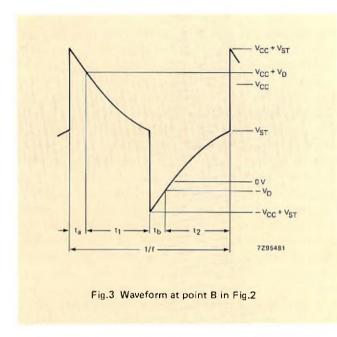
Fig.3 Waveform at point B in Fig.2

Figure 3 is a more detailed version of the waveform at point B in Fig.2. Period t_1 is still defined by equation (1), and period t_2 is still defined by equation (2). The equations for additional periods t_a and t_b are:

$$t_a = -\frac{K}{K+1} RC \ln \frac{K(V_{CC} + V_D)}{K(V_{CC} + V_{ST}) + V_{ST} - V_D} \quad (4)$$

$$t_b = -\frac{K}{K+1} RC \ln \frac{K(V_{CC} + V_D)}{K(2V_{CC} - V_{ST}) + V_{CC} - V_{ST} - V_D} \quad (5)$$

where $K = (R_S + R_I)/R$, and R_I is the input resistance of inverter 1 when one of the input protection diodes is conducting (about 125 Ω).

Since periods t_a and t_b increase with increasing supply voltage, and periods t_1 and t_2 decrease, the total switching period and duty factor of the waveform at point B in the modified circuit tends to be stabilized against supply voltage variations. Since t_a and t_2 increase with increasing switching threshold voltage, and t_1 and t_b decrease, the total switching period and duty factor also tend to be stabilized against spread of the switching threshold voltage.

If $K \geqslant 2$, periods $t_1 + t_a$ and $t_2 + t_b$ are:

$$t_1 + t_a = -RC \ln \frac{V_{ST}}{V_{CC} + V_{ST}}$$

$$t_2 + t_b = -RC \ln \frac{V_{CC} - V_{ST}}{2V_{CC} - V_{ST}}$$

The total switching period is therefore:

$$T = -RC \ln \frac{V_{ST}(V_{CC} - V_{ST})}{(V_{CC} + V_{ST})(2V_{CC} - V_{ST})} \quad (6)$$

Equation (6) shows that the switching period is no longer influenced by the forward voltage drops across the input protection diodes of inverter 1. For a circuit using a 74HC or 74HCU IC in which the nominal value of V_{ST} is $0.5V_{CC}$ for all supply voltages, equation (6) can be simplified to:

$$T = 2.2RC \quad (7)$$

For a circuit using a 74HCT IC in which the nominal V_{ST} is 1.3 V for $V_{CC} = 4.5$ V, 1.415 V for $V_{CC} = 5$ V and 1.53 V for $V_{CC} = 5.5$ V, equation (6) can be approximated by:

$$T = 2.4RC \quad (8)$$

Tables 1 and 2 verify the accuracy of equations (7) and (8) by comparing their results with calculations made with equations (1), (2), (4) and (5), and with measured results for a circuit in which $V_{CC} = 5$ V and $K = 2$ ($R_S = 2R$).

For a circuit using a 74HC IC, Fig.4 indicates the ratio of measured switching periods to those calculated with equations (1), (2), (4) and (5) for various combinations of R and C and with K = 2. The component value limits which will maintain the ratio acceptably close to unity are also shown.

Influence of supply voltage variations

Table 3 (74HC/HCU) and Table 4 (74HCT) compare the results of switching period and duty factor calculations made with equations (1), (2), (4) and (5) for $K = 10^{-3}$ (R_S short-circuit), $K = 2$ ($R_S = 2R$) and $K = 10$ ($R_S = 10R$), with supply voltage as a parameter. The Tables show that the influence of supply voltage variation on the switching period and duty factor of a circuit using a 7HC/HCU or 74HCT IC is almost eliminated when $K = 2$.
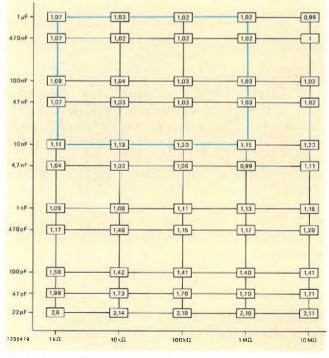

Fig.4 Ratios of measured to calculated switching periods, for a circuit using a 74HC IC, to indicate the validity of equations (1), (2), (4) and (5)

TABLE 1
Accuracy of formulae for 74HC/HCU ICs with
V_{CC} = 5 V, V_{ST} = 2,5 V and K = 2 (all times in μs)

RC	T calculated from formulae	T = 2,2 RC	measured T (74HC)	74HCU
1000	2174	2200	2177	2147
100	217	220	218	214
10	21,7	22	22,6	21,7
1	2,17	2,2	2,4	2,4
0,1	0,217	0,22	0,3	0,3

TABLE 2
Accuracy of formulae for 74HCT ICs with
V_{CC} = 5 V, V_{ST} = 1,415 V and K = 2 (all times in μs)

RC	T calculated from formulae	T = 2,4 RC	measured T
1000	2348	2400	2362
100	235	240	236
10	23,5	24	24,4
1	2,35	2,4	2,6
0,1	0,235	0,24	0,3

TABLE 3
Switching period and duty factor as functions of supply voltage with K as a parameter for 74HC/HCU ICs
(V_{ST} = 0,5 V_{CC}, RC = 100 μs)

			$K = 10^{-3}$		
V_{CC}	3 V	4,5 V	5 V	5,5 V	6 V
total switching period (μs)	181,645	168,685	165,986	163,749	161,866
deviation from value at 5 V	+9%	+1,6%	0	−1,3%	−2,5%
switching duty factor	0,5	0,5	0,5	0,5	0,5
			K = 2		
V_{CC}	3 V	4,5 V	5 V	5,5 V	6 V
total switching period (μs)	218,027	216,822	216,537	216,293	216,081
deviation from value at 5 V	+0,7%	+0,1%	0	−0,1%	−0,2%
switching duty factor	0,5	0,5	0,5	0,5	0,5
			K = 10		
total switching period (μs)	219,367	219,107	219,045	218,991	218,945
deviation from value at 5 V	+0,1%	+0,03%	0	−0,02%	−0,05%
switching duty factor	0,5	0,5	0,5	0,5	0,5

Influence of switching threshold voltage spread

Table 5 (74HC), Table 6 (74HCU) and Table 7 (74HCT) compare the results of switching period and duty factor calculations made with equations (1), (2), (4) and (5) for K = 10^{-3} (R$_S$ short-circuit), K = 2 (R$_S$ = 2R) and K = 10 (R$_S$ = 10R), with switching threshold voltage as a parameter. For a circuit using a 74HC IC, Table 5 shows that the influence of the switching threshold voltage spread on the switching period is reduced by 33% when K = 2, and the duty factor spread is reduced by 43%. For a circuit using a 74HCU IC, Table 6 shows a 33% reduction of the switching period deviation and a 40% reduction of duty factor spread with K = 2. For a circuit using a 74HCT IC, Table 7 shows a 29% reduction of switching period deviation and a 25% reduction of duty factor spread when K = 2.

TABLE 4
Switching period and duty factor as functions of supply voltage with K as a parameter for 74HCT ICs
(RC = 100 μs)

K = 10⁻³			
V_{CC}	4,5 V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53 V
total switching period (μs)	188,273	186,810	185,623
deviation from value at V_{CC} = 5 V	+0,8%	0	−0,6%
switching duty factor	0,74	0,75	0,76

K = 2			
V_{CC}	4,5 V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53 V
total switching period (μs)	234,022	234,855	235,562
deviation from value at V_{CC} = 5 V	−0,3%	0	+0,3%
switching duty factor	0,64	0,64	0,65

K = 10			
V_{CC}	4,5 V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53 V
total switching period (μs)	236,635	237,692	238,588
deviation from value at V_{CC} = 5 V	−0,4%	0	+0,4%
switching duty factor	0,63	0,64	0,64

TABLE 5
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HC ICs
(V_{CC} = 5 V, RC = 100 μs)

K = 10⁻³			
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	183,384	165,986	183,384
deviation from value at V_{ST} nom.	+10,5%	0	+10,5%
switching duty factor	0,73	0,5	0,27

K = 2			
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	231,812	216,537	231,812
deviation from value at V_{ST} nom.	+7%	0	+7%
switching duty factor	0,63	0,5	0,37

K = 10			
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	234,596	219,045	234,596
deviation from value at V_{ST} nom.	+7%	0	+7%
switching duty factor	0,62	0,5	0,37

Influence of temperature on switching period

Temperature variations have little influence on the switching period, and hence the operating frequency of astable multivibrators using 74HCMOS ICs. This is because the switching threshold voltage varies by only ±60 mV from its nominal value at 25 °C over the temperature range −40 °C to +125°C. This is far less than the ±200 mV variation for LSTTL ICs. The effect of the variation in switching threshold voltage is a spread of the total switching period. For a circuit using a 74HC/HCU IC with a 5 V supply and K = 2, the switching period increases by 0,02% at the two temperature extremes. For a circuit using a 74HCT IC, the switching period varies by ±1%.

Dynamic power dissipation

The average dynamic power dissipation of an entire IC package of inverters (or inverting gates), only two of which are used for an astable multivibrator is the sum of the following five terms. The first two terms apply to the inverters in the package which don't form part of the multivibrator. The sum of the last three terms is the dynamic power dissipation of the two inverters of the multivibrator.

$C_{PD}V_{CC}^2 f_i$ in which C_{PD} is the load imposed by internal capacitance and switching transient currents, and f_i is the frequency at the input.

TABLE 6
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HCU ICs
(V_{CC} = 5 V, RC = 100 μs)

$K = 10^{-3}$			
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	210,497	165,986	210,497
deviation from value at V_{ST} nom.	+27%	0	+27%
switching duty factor	0,83	0,5	0,17

$K = 2$			
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	256,202	216,537	256,202
deviation from value at V_{ST} nom.	+18%	0	+18%
switching duty factor	0,7	0,5	0,3

$K = 10$			
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	259,377	219,045	259,377
deviation from value at V_{ST} nom.	+18%	0	+18%
switching duty factor	0,7	0,5	0,3

TABLE 7
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HCT ICs
(V_{CC} = 5 V, RC = 100 μs)

$K = 10^{-3}$			
V_{ST}	0,93 V	1,415 V	1,9 V
total switching period (μs)	215,996	186,810	171,907
deviation from value at V_{ST} nom.	+16%	0	−8%
switching duty factor	0,84	0,75	0,64

$K = 2$			
V_{ST}	0,93 V	1,415 V	1,9 V
total switching period (μs)	261,231	234,856	221,700
deviation from value at V_{ST} nom.	+11%	0	−5,6%
switching duty factor	0,71	0,64	0,58

$K = 10$			
V_{ST}	0,93 V	1,415 V	1,9 V
total switching period (μs)	264,478	237,692	224,303
deviation from value at V_{ST} nom.	+11%	0	−5,6%
switching duty factor	0,70	0,63	0,57

$\Sigma(C_L V_{CC}^2 f_o)$ in which C_L is the load capacitance at the output, and f_o is the frequency at the output.

$(C_{PD} V_{CC}^2)/T$ in which C_{PD} is defined for the first term, and T is the total switching period for the multivibrator.

$(2C V_{CC}^2)/T$ in which C is the timing capacitance of the multivibrator, and T is its total switching period.

$X V_{CC}$ in which X is the average through-current from Table 8 and 9. This through current depends on the size of the input transistors of the particular IC and varies from one type of IC to another.

It is obvious from the fourth term that the dynamic power dissipation can be reduced by using a lower value for timing capacitor C, and therefore, higher values for R and R_S.

The last term is the additional average dynamic power dissipation of the first inverter used for the multivibrator. It occurs because the near-triangular waveform at the input to inverter 1 (point D in Fig.2) slowly approaches V_{ST} and causes the through-current indicated in Tables 8 and 9. Because of the shape of the waveform, inverter 1 is always operating in its linear region so that this term is independent of the operating frequency.

Component value and supply voltage limits

The astable multivibrator shown in Fig.2 will operate correctly as long as C is a bipolar capacitor with a value greater than 100 pF, and the value of R is between 470 Ω and 1 MΩ. The lower limit for the value of R ensure that R is much higher than the output impedance of the inverters (typically 40 Ω with a 4,5 V supply) so that output impedance spreads don't influence the switching period. However,

due to the influence of parasitic capacitances C_{t1} and C_{t2}, equations (7) and (8) will only remain valid when C is 10 nF or greater, and R is between 1 kΩ and 1 MΩ.

The previously mentioned spurious oscillations or glitches which can occur if the value of R_S is too large will have a frequency of $1/(2t_p)$ where t_p is the propagation delay of inverter 1. The impedance at the input to inverter 1 is then very high and sensitive to crosstalk. The spurious oscillations can be suppressed by using careful board layout to decrease parasitic capacitance C_{t1}, decreasing R_S, or increasing C_{t2} by connecting a low-value capacitor between point A and D. However, the best solution is to use the un-buffered Hex Inverter 74HCU04 which is specially made for linear applications and will make the oscillator less sensitive to spurious oscillations because it has lower gain than the HC04 or HCT04. Parasitic capacitance C_S is formed by board tracks and should be kept as low as possible to avoid any additional delay due to time-constant $R_S C_S$.

Although 74HC/HCU ICs can operate from a supply voltage as low as 2 V, it is recommended that a supply of at least 3 V be used for an astable multivibrator. This is because the threshold voltages of the input transistors can be as high as 0,9 V which would leave insufficient margin to operate in the linear region with a 2 V supply. The supply voltage range for astable circuits using 74HC/HCU ICs is therefore 3 V to 6 V. For circuits using a 74HCT ICs it is 4,5 V to 5,5 V.

TABLE 8

Average through-current for two inverters in an astable multivibrator using 74HC/HCU ICs

V_{CC}	74HC00	74HC04	74HCU04
	through-current (μA)		
3 V	150	130	600
4,5 V	700	450	2600
5 V	1050	650	3500
6 V	1800	1050	5600

TABLE 9

Average through-current for two inverters in an astable multivibrator using 74HCT ICs

V_{CC}	74HCT00	74HCT04
	through current (μA)	
4,5 V	700	450
5 V	1050	650
5,5V	1350	800

Crystal oscillators using HCMOS ICs

J. EXALTO

Crystal-controlled oscillators are widely used in clock pulse generators because of their excellent frequency stability and their wide operating frequency range. If they use an HCMOS IC as the active element, they have the additional advantages of low power dissipation and stable operation over a wide range of supply voltages and temperature. This article describes the design of several types of crystal-controlled oscillators based on the unbuffered HCMOS Hex Inverter 74HCU04.

The terms and definitions for crystal-controlled oscillators as specified by the IEC in their publication IEC 122-11 are listed in the Table.

CRYSTAL CHARACTERISTICS

Figure 1 is the equivalent circuit of a quartz crystal. The reactive and resistive components of the impedance of the crystal alone, and of the crystal with a series and a parallel capacitive load are shown in Fig.2.

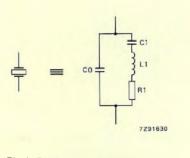Figure 2 shows that, with a specified value of load capacitance (C_L), the load resonance frequency (f_L) is the

same for a circuit with either a parallel or series capacitive load. It is therefore very important to use this value of load capacitance in the design of a crystal oscillator. However,
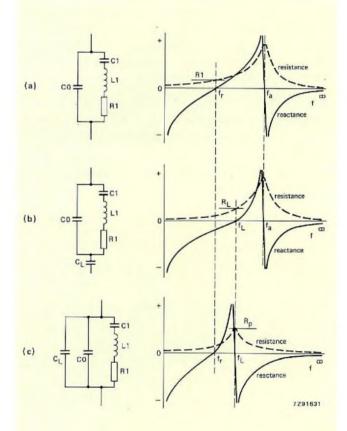

Fig.1 Equivalent circuit of a crystal

Fig.2 Reactance and resistance characteristics of a crystal,
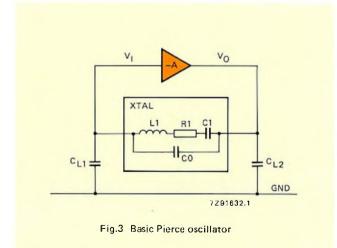(a) resonance, (b) anti-resonance, (c) load resonance

the preferred load capacitance should be partially adjustable so that compensation can be made for spurious capacitances caused by the pcb and the pins of the IC. Preferred values of load capacitance specified for fundamental frequency operation of various crystals at parallel resonance are 20 pF, 30 pF, 50 pF and 100 pF. Some countries still use 32 pF, but, since this is not a preferred value, its use is not recommended. The preferred values of load capacitance for overtone operation at series resonance are 8 pF, 12 pF, 15 pF, 20 pF and 30 pF.

The power dissipated in a crystal is called the "level of drive". Since the crystal characteristics become highly dependent on the level of drive if it is outside the range 1 pW to 1 mW, the crystal characteristics are usually specified at 0,5 mW. With a very low level of drive, as can occur during oscillator start-up, the characteristics can vary slightly, in particular, the resonance resistance R_r will increase about threefold. To overcome this, the loop gain of the oscillator circuit should be sufficient to prevent start-up problems, but not enough to overdrive the crystal.

HCMOS HEX INVERTER 74HCU04 IN CRYSTAL-CONTROLLED OSCILLATORS

The Pierce oscillator in which the crystal has a parallel load capacitance is the type most widely used in digital systems. As shown in Fig.3, it is basically a Colpitts oscillator in which the inductor has been replaced by a crystal. The advantages of this configuration are:

— good suppression of the third overtone (9×)

— lower power dissipation (level of drive) in the crystal than in a series-resonant oscillator due to the high ohmic loading

— the amplifier must provide 180° phase shift, so a simple inverter can be used.

The high input impedance of the 74HCU04 Hex Inverter makes it ideal for use in a Pierce oscillator. However, good power supply decoupling is necessary (see "Power supply decoupling" in the user guide of Data Handbook IC06N).

Although the 74HCU04 can operate from a supply voltage as low as 2 V, it is recommended that a supply of at least 3 V be used for a crystal-controlled oscillator. This is because the threshold voltages of the input transistors can be as high as 0,9 V which would leave insufficient margin to operate in the linear region with a 2 V supply. The supply voltage range for crystal oscillators using the 74HCU04 is therefore 3 V to 6 V.

Unfortunately, the output impedance of the 74HCU04 is too low to drive the crystal directly. The simple expedient of adding a resistor in series with the output causes additional phase shift resulting in an increase of loop gain and a decrease of the level of drive in proportion to the square of the frequency. This arrangement is therefore only suitable for lower frequencies (up to about 4 MHz). For higher frequency oscillators, the output impedance of the inverter must be increased with a series capacitor instead of a series resistor.

A 4 MHz crystal oscillator using the 74HCU04

Figure 4 illustrates a practical 4 MHz Pierce oscillator in which the crystal is operating at its fundamental frequency and is tuned by a parallel load capacitance consisting of C_{L1} and C_{L2} in series, together with stray capacitances. C_{L1} should be adjustable so that the capacitive load can be accurately set to the preferred load capacitance specified for the particular crystal being used. The loop gain of the circuit is:
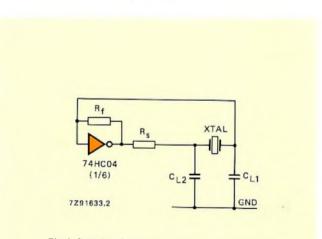
$$\frac{v_O}{v_I} = \frac{C_{L2}}{C_{L1}}$$

Fig.3 Basic Pierce oscillator

Fig.4 Practical Pierce oscillator using unbuffered inverter 74HCU04

For an economy range 4 MHz crystal (4322 143/144 04091), the specified C_L (C_{L1} and C_{L2} in series) is 30 pF and the specified resonance resistance (R_r) of the crystal is 75 Ω. At 4 MHz, a loop gain (C_{L2}/C_{L1}) of about unity is adequate, and so if there is no stray capacitance.

$$C_{L1} = C_{L2} = 60\,pF.$$

However, since there will always be some stray capacitance 56 pF capacitors should be used for C_{L1} and C_{L2}. Since C_{L1} and C_{L2} are equal, the total impedance as seen from the output of the inverter can be simplified to:

$$Z_L = \frac{X_{CL}^2}{R_r}$$

where $X_{CL} = -j/\omega C_{L2}$ and R_r is the specified resonance resistance of the crystal (75 Ω).

For optimal operation of a Pierce oscillator, the output impedance of the inverter should be the same as the total load impedance. The output impedance of the inverter should therefore be 5,9 kΩ. Since the output impedance of the 74HCU04 with a 5 V supply is only about 40 Ω, the preferred value for R_S in series with the output of the inverter is 5,6 kΩ. However, this value would cause too much phase shift, so a compromise value of 2,2 kΩ is used. Any value between 1 MΩ and 10 MΩ is suitable for R_f which provides d.c. bias for the output of the inverter.

Higher frequency crystal oscillators using the 74HCU074

In addition to the phase shift introduced by R_S in series with the inverter output, the inverter's propagation delay (t_p) also causes phase shift which can be expressed as:
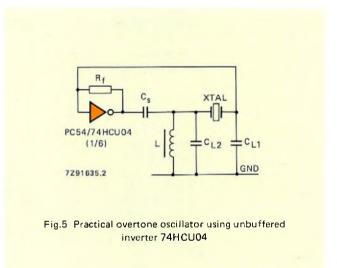
$$\text{Phase shift} = f_{osc} \times t_p \times 360°.$$

With a maximum propagation delay of 14 ns, a 4,5 V supply for the 74HCU04, and an oscillator frequency of 6 MHz, a further 30° phase shift would occur. This means that the Pierce oscillator circuit shown in Fig.4 is unsuitable for operation at high frequencies. Modifying the circuit by replacing R_S with a capacitor (C_S) of about the same value as C_L (half the value of C_{L1} or C_{L2}), allows the circuit to be used at a higher frequency.

An overtone crystal oscillator using the 74HCU04

Most crystal manufacturers supply crystals for operation at fundamental frequencies, third overtone crystals for operation in the frequency range 10 MHz to 75 MHz, and fifth overtone crystals for operation in the frequency range 50 MHz to 125 MHz.

Due to the high maximum operating frequency of HCMOS logic systems, it may be necessary to use a third overtone oscillator with parallel load capacitance as shown in Fig.5. A critical requirement for this type of oscillator is suppression of the fundamental frequency of the crystal. Two methods of suppression are used in the circuit of Fig.5.

— capacitor C_S, which should have a value close to that of C_L, presents a higher impedance to the fundamental frequency of the crystal than it does to the third overtone

— C_S/L resonates at slightly below the third overtone and traps the fundamental frequency.

Fig.5 Practical overtone oscillator using unbuffered inverter 74HCU04

Tuning L for maximum output voltage may affect the oscillator frequency slightly, but adjustment of C_{L1} will usually compensate for this.

Checking a prototype crystal oscillator design

The following simple checks will verify the quality of the design of a crystal-controlled oscillator using a 74HCU04 IC:

1. Test the oscillator under worst-case conditions (lowest supply voltage, worst-case crystal and highest operating temperature). A worst-case crystal can be simulated by adding series and parallel resistors.

2. Ensure that the circuit doesn't oscillate without the crystal.

3. Check the frequency stability of the oscillator over a supply voltage range greater than that which is likely to occur during normal operation.

TERMS AND DEFINITIONS FOR CRYSTAL OSCILLATORS (IN ACCORDANCE WITH IEC 122-1)

Adjustment tolerance — The permissible deviation from the nominal frequency at the reference temperature under specified conditions.

Ageing (long-term parameter variation) — The relation which exists between any parameter (e.g. resonance frequency) and time.

Note: such parameter variation is due to long-term changes in the crystal unit and is usually expressed in fractional parts per period of time.

Ageing tolerance — The permissible deviation due to time under specified conditions.

Anti-resonance frequency f_s — The higher of the two frequencies of a crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.

Level of drive — A measure of the conditions imposed upon the crystal unit expressed in terms of power dissipated.

Note: in special cases, the level of drive may be specified in terms of crystal current or voltage.

Load capacitance C_L — The effective external capacitance associated with the crystal unit which ddetermine the load resonance frequency f_L.

Load resonance frequency f_L — One of the two frequencies of a crystal unit in association with a series or with a parallel load capacitance, under specified conditions, at which the electrical impedance of the combination is resistive. This frequency is the lower of the two frequencies when the load capacitance is in series and the higher when it is in parallel (see Fig.2). For a given value of load capacitance (C_L), these frequencies are identical for all practical purposes and are given by:

$$\frac{1}{f_L} = 2\pi \sqrt{\frac{L_1 C_1 (C_0 + C_L)}{C_1 + C_0 + C_L}}$$

Load resonance resistance R_L — The resistance of the crystal unit in series with a stated external capacitance at the load resonance frequency f_L.

Note: the value of R_L is related to the value of R_r by the following expression:

$$R_L = R_r \left(1 + \frac{C_0}{C_L}\right)^2$$

Motional capacitance C_1 — The capacitance of the motional (series) arm of the equivalent circuit.

Motional inductance L_1 — The inductance of the motional (series) arm of the equivalent circuit.

Nominal frequency f_n — The frequency assigned by the specification of the crystal unit.

Operable temperature range — The range of temperatures as measured on the enclosure over which the crystal unit must function though not necessarily within the specified tolerances.

Operating temperature — The range of temperatures as measured on the enclosure over which the crystal unit must function within the specified tolerances.

Reference temperature — The temperature at which certain crystal measurements are made. For controlled temperature units, the reference temperature is the mid-point of the controlled temperature range. For non-controlled units the reference temperature is normally $25 \pm 2\,°C$.

Resonance frequency f_r — The lower of the two frequencies of the crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.

Resonance resistance R_r — The resonance of the crystal unit alone at the resonance frequency f_r.

Tolerance due to level of drive variation — The permissible deviation due to the variation of level of drive.

Tolerance over temperature range — The permissible deviation over the temperature range with respect to the frequency at the specified reference temperature.

Unwanted response — A state of resonance of a crystal vibrator other than that associated with the working frequency.

Working frequency f_w — The operational frequency of the crystal unit together with its associated circuits.
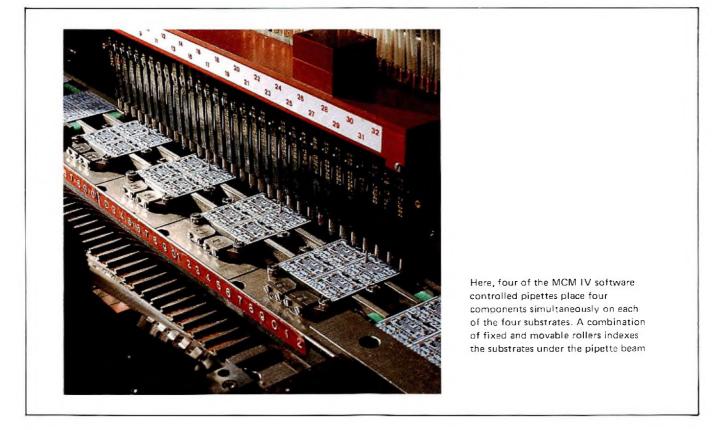
REFERENCE

Data Handbook C9; "Piezoelectric quartz devices"; ordering code 9398 124 90011.

Automatic placement machine for hybrid-circuit assembly

Answering the needs of large-scale manufacturers of hybrid circuits, MCM IV is the latest addition to the versatile MCM family of automatic placement machines for SMDs (surface-mount devices). Working an 80 hour week, the first of the new machines to be delivered is currently assembling hybrids at a rate of 1,2 million a year.

Developed in response to a customer's requirement to double hybrid-circuit production without taking up additional factory floor space, the MCM IV is based largely on concepts pioneered and proved in the MCM II, a machine which combines simultaneous and sequential placement under software control to attain high throughput. Unlike the MCM II, however, which is primarily for printed-circuit-board assembly, the MCM IV is designed specifically to work with standard ceramic substrates. Standard versions of the machine can have up to eight placement heads, each of which can place up to 1024 components in one machine cycle.

Here, four of the MCM IV software controlled pipettes place four components simultaneously on each of the four substrates. A combination of fixed and movable rollers indexes the substrates under the pipette beam

VERSATILE PLACEMENT HEAD

Central to each placement head is a movable beam carrying 32 pipettes that can pick up 32 components simultaneously and place them on substrates either simultaneously or sequentially, depending on the substrate layout and corresponding control software. The pipettes extract tape-packaged components fed from supply reels (also controlled by software), and transport them to their programmed positions on the substrates, rotate them to required alignments, and press them down onto solder-paste footprints screened in advance onto the substrates.

Four standard substrates at a time fit under the pipette beam, each served by a group of eight pipettes drawing from their own supply reels in a 32-reel, quick-change magazine. The beam moves under servo control so that any one of the pipettes in a group can place its component anywhere on the substrate it serves, with an accuracy of 0.2 mm in both x and y directions. The machine imposes no artificial grid restrictions.

The pipettes are spaced at a pitch of 10 mm and the walking-beam substrate transport mechanism can be programmed to advance the substrates 80, 160 or 320 mm at a time. For substrates having only one circuit each, the transport mechanism is programmed to advance 80 mm at a time so that successive groups of pipettes, working sequentially, can place up to 32 different component types. On substrates supporting two identical circuits, pipettes working simultaneously in pairs can place up to 16 component types. And on four-circuit substrates, pipettes working together in fours can place up to eight component types. The transport mechanism would then be programmed to advance 320 mm at a time so that all four substrates would move as a unit into and out of the placement-head working area.

In one machine cycle the pipettes can be charged up to 32 times. After that, all four of the substrates operated upon in that cycle must give way to four new ones. If two placement heads are fitted, the transport mechanism will then automatically position the first four substrates under the second head.

To avoid unnecessary constraints on substrate layout, any component can be rotated from its pick-up alignment by 90°, 180° or 270°, with an accuracy of 2°. Since selective rotation of individual pipettes would be unduly complicated mechanically, all are rotated together by the amount required for a given component, but only those actually placing that component are lowered to the substrate. After that, all 32 are again rotated together to the next alignment required.

MULTIFUNCTION PIPETTES

The basic design of the pick-and-place pipettes is an important feature that MCM IV shares with other members of the MCM family. It combines a central tube with an outer, mechanical chuck. The function of the tube is threefold: to monitor the presence of the component throughout the pick-and-place action, to hold it by vacuum during the last phase of that action, and to press it firmly onto its solder-paste footprint on the substrate. The chuck has equally important functions: it aligns the component with the x and y placement axes, regardless of tolerances in the original angle of presentation; and it exercises a positive, mechanical grip during transport of the component from the pick-up to the placement position.
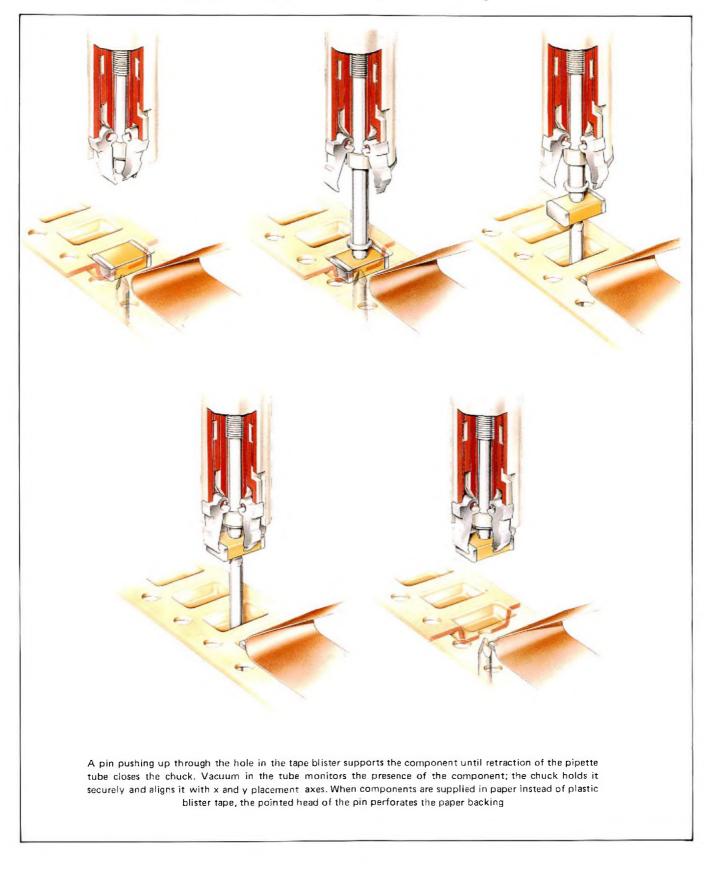
A pin rising from beneath the tape lifts the component out of its blister and presents it to the central tube of the pipette, which at this stage is under vacuum. The pin continuous to support the component until the jaws of the chuck, descending along the outside of the tube, close on it. The pin then retracts and the pipette carries the component to its placement position on the substrate.

Microphones mounted in turbulence chambers in each of the 32 vacuum lines monitor the presence of the components in the pipettes. If the initial presentation of any component is unsuccessful, the monitoring system triggers the corresponding tape feed to advance a new component into position so that the pipette can try again to pick it up. If, after two such "refires", pick-up is still unsuccessful, the machine cycle stops and the control panel alerts the operator and reports the pipette position at which the fault has occurred so that he can take remedial action. Likewise, if a component becomes dislodged before placement, the machine stops and notifies the operator of the fault and its position.

An important respect in which the MCM IV pipettes differ from those of other members of the MCM family is their action during the very last phase of component placement. MCM IV is designed to place components on solder-paste footprints whose limited adhesiveness must be relied upon to hold them securely in place until the solder paste is reflowed. The components must therefore be pressed firmly enough onto the footprints to give them reasonable assurance of sticking, yet gently enough not to risk damaging the comparatively brittle ceramic substrate. MCM IV pipettes meet this requirement by cushioning the final placement with air.

When a pipette reaches the position at which its component is to be placed, its central tube starts to descend and the chuck opens so that the component is held solely by vacuum. Then, as soon as the component touches the substrate, a valve in the placement head momentarily switches the connection of the tube from the vacuum to the pressure manifold, pushing the component down onto its footprint with a pulse of compressed air.

Reconnected to the vacuum manifold, the tube then retracts. If the microphone does not detect noise in the turbulence chamber, the control system interprets that as

an indication that the component has not in fact been successfully placed and is still attached to the tube instead of the substrate — as may happen, for example, if solder paste has not been properly screened onto the footprint. In this event too, the control system interrupts the machine cycle and alerts the operator.

A pin pushing up through the hole in the tape blister supports the component until retraction of the pipette tube closes the chuck. Vacuum in the tube monitors the presence of the component; the chuck holds it securely and aligns it with x and y placement axes. When components are supplied in paper instead of plastic blister tape, the pointed head of the pin perforates the paper backing

SUPPORT MODULES

In addition to the placement and transport modules, tape-reel magazines, and control electronics, MCM IV includes loading and unloading modules also under software control. The loading module, with a capacity of 600 substrates stored in quick-change cassettes, feeds substrates to the transport module in step with the action of the walking beam. In the event of feeding errors, sensors incorporated in the transport module detect vacant positions and signal the control electronics to adjust the placement program accordingly. At the far end of the transport module, the unloading module restacks the assembled substrates in cassettes in which they can then progress to reflow soldering. A reflow soldering station also may be initiated in the MCM IV-line.

Depending on the layout of the substrates, one MCM IV, requiring the attention of only one operator, can place from 25 000 to 200 000 components an hour.

MCM IV placement heads can be fed by 8 mm tapes in 32-reel magazines or, as here, 12 mm, 16 mm or 24 mm tapes in cassettes holding up to 20 reels

The multiple-station MCM IV includes a revolving stock turret to ensure an uninterrupted supply of substrates to the placement heads
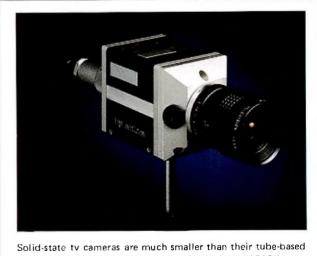
ACKNOWLEDGEMENT

MOS-XY, interline and frame-transfer sensors compared

M. COLLET

It wasn't so long ago that the solid-state imager was regarded as little more than a curiosity, something to be played with in the research labs of the world's big electronics companies, but no real threat to the tv camera tube. In those days the best that could be realized were relatively simple linear arrays that could do little more than display still images on a tv screen, good for a slide show but not much else. Two-dimensional high-resolution displays were just pie in the sky. But like the old adage of acorns and oaks, those early imagers have now grown into something really big. So big, in fact, that camera tubes are now under serious threat, and many types could well be completely supplanted within the next five years.

Already we find two-dimensional solid-state imagers replacing vidicons in CCTV installations and home video systems, and it won't be long before they hit the broadcasting market in the latest ENG tv cameras.

But the real future of the solid-state imager lies not merely as a replacement for the camera tube. It lies in applications for which camera tubes have never even been considered, and in a host of applications generated by its very existence. Character-recognition systems for computers and word processors are a prime example, as are home security systems, which thanks to the relatively low cost of the solid-state imager when in volume production, are likely to increase dramatically over the next few years. Then there are robot-vision systems, remote measuring systems and video slide-scanners, and in the slightly more distant future, home and office videophones and electronic *still-picture* cameras.

So let's take a closer look at the solid-state imager, and see if we can predict which of the many systems currently on the market is likely to be the major one of the future.

Solid-state tv cameras are much smaller than their tube-based counterparts. This camera contains Philips' NXA1010 frame-transfer sensor and is no more than 60 X 65 X 100 mm (excluding lens)
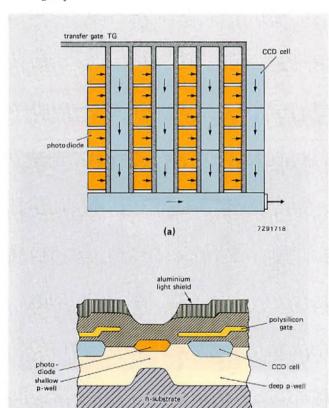
THREE SYSTEMS

If we neglect some less important examples, we find that there are three major systems jockeying for the lion's share of the market. These are the interline-transfer (IL) sensor, the x/y-addressed MOS sensor (MOS-XY), and the frame-transfer (FT) sensor. Let's look at each in turn.
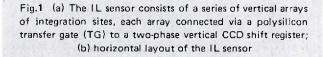
Interline-transfer (IL) sensor

The IL sensor (Fig.1), currently promoted mainly by NEC and Sony, was the first charge-coupled area image sensor to become commercially available. Basically it consists of a series of vertical arrays of integration sites, each array connected via a polysilicon transfer gate (TG) to a two-phase vertical CCD shift register. The number of transfer cells in each shift register is equal to the number of display lines in each field, and to half the number of integration sites. So the transfer cells are shared between the two fields and, by appropriate biasing of either one or the other set of gates controlling the vertical shift registers, each field can be read out separately to produce an interlaced picture frame.

The IL sensor has the advantage of requiring only half as many vertical transfer cells as there are pixels in the final tv picture, but it does require the same number of integration sites. The total integration time is thus a full-frame period and this can result in a somewhat poor response to fast moving objects.

X/Y-addressed MOS sensor (MOS-XY)

The MOS-XY promoted by Hitachi (Fig.2) consists of an x/y-addressed matrix of photodiodes with a MOSFET at each crossing point. The transistor gates in each row are connected via a polysilicon horizontal address line whose voltage is controlled by a vertical scan register. The transistor drains in each column are connected to aluminium sense lines, in turn connected to the video output via a series of MOSFETS controlled by a horizontal scan register.

(a)

(a)

(b)

Fig.1 (a) The IL sensor consists of a series of vertical arrays of integration sites, each array connected via a polysilicon transfer gate (TG) to a two-phase vertical CCD shift register; (b) horizontal layout of the IL sensor
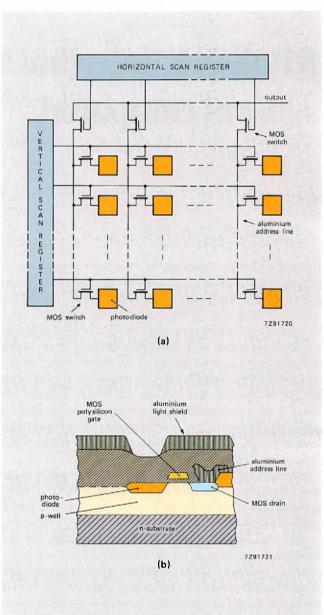

(b)

Fig.2 (a) The MOS-XY consists of an x/y- addressed matrix of photodiodes with a MOSFET at each crossing point. The transistor gates in each row are connected via a polysilicon horizontal address line whose voltage is controlled by a vertical scan register. The transistor drains in each column are connected to aluminium sense lines, in turn connected to the video output via a series of MOSFETS controlled by a horizontal scan register; (b) horizontal layout of the MOS-XY sensor

The vertical scan register selects the tv line to be read out by generating a positive pulse on the horizontal address line corresponding to that line, so raising the gate voltage of the MOS transistors and allowing the photocharge to pass to the aluminium sense lines. The horizontal scan register then sequentially connects each sense line to the video output to form the video signal. The outputs of each line are interlaced by the vertical scan register.

As with the IL sensor the MOS-XY requires as many photosensitive elements as there are pixels in the final tv picture. From a production point of view, however, it does have one advantage, it lends itself readily to manufacture using CMOS processes already established by Hitachi for its DRAMs, and this, of course, can provide significant cost savings.
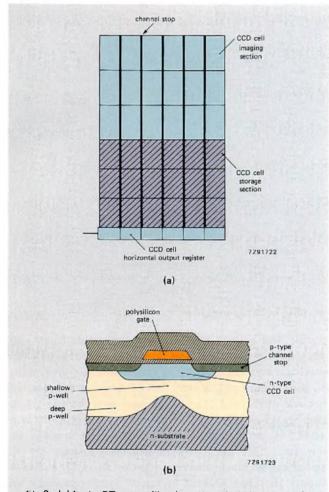

(a)

(b)

Fig.3 (a) In the FT sensor, illuminated vertical charge-transfer channels are operated with common electrodes to form a two-dimensional imaging area. During vertical blanking, charge generated in the imaging area over a field integration period is rapidly transferred into a shielded storage area located below the imaging area. During the horizontal blanking periods, this charge is shifted down a line at a time into a horizontal shift register where it is clocked out during each line period to form the video signal; (b) horizontal layout of the FT sensor

Frame-transfer (FT) sensor

In the FT sensor (promoted by Philips, Fig.3), charge-transfer channels are placed vertically side-by-side and operated with common electrodes to form a two-dimensional imaging area. During vertical blanking, charge generated in the imaging area over a field integration period is rapidly transferred into a shielded storage area located below the imaging area. During the horizontal blanking periods, this charge is shifted down a line at a time into a horizontal shift register where it is clocked out during each line period to form the video signal.

Since all the integrated charge is completely removed in each field, the FT sensor needs only half as many photosensitive cells as there are pixels in a complete frame, and the number of rows need equal only the number of display lines within a single field. The video information for the second interlaced field is obtained by electronically shifting the centre of each integration site by half a cell. In the latest four-phase devices (such as the NXA1010/1020), this is done by integrating the first field under, say, gates 2, 3 and 4, and the second field under gates 4, 1 and 2.

HOW DO THEY COMPARE?

When comparing these three systems, all of which are currently in use and enthusiastically promoted by their respective manufacturers, it's important to know on what basis we're talking. Should we, for example, consider devices of equal image area, and compare their sensitivity, resolution, cost. There are, after all, some arguments for this approach since the current most popular tv camera size is 2/3 inch, and it would be reasonable to expect the new cameras based on solid-state imagers to fall into line with this.

On the other hand, it may be argued that with a completely new technology at our disposal, we should optimize it to the full. After all, what's the point of having such potential for miniaturization, with all its accompanying advantages, if we allow ourselves to be constrained by limitations of the past.

Whatever the basis for comparison, a look at the factors governing size, cost and performance should provide some clear indications for the future.

Sensor layout and potential for miniaturization

The sensor layouts are shown in Figs 1, 2 and 3. In all cases the number of pixels has been chosen to be compatible with PAL and VCR (video cassette recorders). IL and MOS-XY sensors currently have 400 pixels per line and 600 photodiodes per column, the FT sensor has 600 pixels per line and 300 CCD cells per column in both the imaging and storage sections, which through interlacing yield 600 tv lines. The basic cells in all devices use a vertical anti-blooming

structure in which boron is diffused into the n-type sub-strate to produce p wells that allow excess-charge diffusion from the photosensitive areas into the substrate.

Looking at the horizontal layout of each device in turn, we find that for each column of pixels the IL sensor requires a channel stop, a photodiode, a transfer gate and a CCD shift register. The MOS-XY requires a channel stop, a photo-diode, a MOS polysilicon gate and drain, and an aluminium address line. The FT sensor, on the other hand, requires only a channel stop and a CCD shift register, and so makes far more efficient use of the area available for imaging. And on the basis of size alone, using the same degree of miniaturization in all devices, it would appear that the FT sensor comes out a clear winner by a factor of at least two.

Things aren't quite that simple, however, and to understand why we must look at the way the three sensors generate the composite video signal. As we've seen, the FT sensor has the advantage of a narrow pitch, and the IL and MOS-XY sensors have the advantage of a separate site for each pixel. This has led to the use of mosaic colour filters for IL and MOS-XY sensors, and to vertical stripe colour filters for the FT sensor.
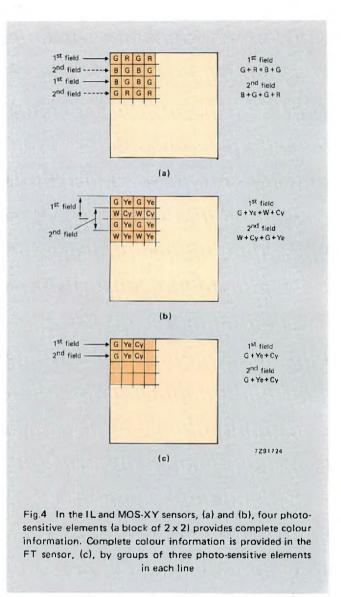
In the IL and MOS-XY sensors, four photo-sensitive elements (a block of 2 x 2, Figs 4(a) and 4(b)) provides complete colour information. The same is provided in the FT sensor by groups of three photo-sensitive elements in each line (Fig.4(c)). So the FT sensor needs 1,5 times as many photo-sensitive elements per line to produce the same number of colour pixels as the IL and MOS-XY sensors. This means that current devices referred to above (i.e. 400 x 600 elements for IL and MOS-XY sensors, 600 x 300 for the FT sensor) all produce lines of 200 colour pixels, so on this basis alone, all devices have the same horizontal resolution.

However, the narrower pitch of the FT sensor means for say an 8 mm image diagonal, these 200 pixels can be realized in $4\,\mu$m technology, rather than the $2\,\mu$m technology needed for current IL and MOS-XY sensors with 11 mm image diagonals. So an FT sensor of equivalent resolution to an IL or MOS-XY sensor is not only easier to manufacture, it also has a much smaller imaging area, and since it makes more efficient use of this area, its sensitivity is significantly higher.

If instead the FT sensor is manufactured in $2\,\mu$m technology, we can either halve the size of the chip yet still produce an FT sensor of equivalent performance to current IL or MOS-XY sensors, or we can double horizontal resolution.

So even allowing for the fact that the FT sensor requires more columns to produce the same colour video information as the IL and MOS-XY sensors, it comes out a clear winner on the basis of sensitivity-resolution-minia-turization.

What's more, if we're only interested in black/white imaging, the resolution of the IL and MOS-XY sensors will

Fig.4 In the IL and MOS-XY sensors, (a) and (b), four photo-sensitive elements (a block of 2 x 2) provides complete colour information. Complete colour information is provided in the FT sensor, (c), by groups of three photo-sensitive elements in each line

double, but that of the FT sensor will treble (since each photosensitive element then forms a complete pixel), thus making it even more attractive than it is for colour imaging.

A common criticism of the FT sensor has been that, because of its need of a storage section, it requires greater chip area than IL or MOS-XY sensors for equivalent image areas. As we've seen above, however, this neglects the important fact that for *equivalent performance* the FT sensor can be much smaller. To give an example: a state-of-the-art IL sensor realized in 1,5 to $2\,\mu$m technology will have a total chip area of around 39 mm², whilst an equivalent FT sensor (also realized in 1,5 to $2\,\mu$m technology) will have a total area (including storage section) of only 22 mm².

If on the other hand we manufacture the FT sensor in $3\,\mu$m technology, we'll end up with a sensor of around 38 mm², roughly the same as the 1,5 to $2\,\mu$m IL sensor. But we'll also have a sensor with roughly twice the sensitivity and, moreover, one that's much easier to manufacture.

Vertical resolution

Modern MOS-XY sensors use two address lines per column, thus allowing the use of neighbouring lines to construct the composite video signal for each tv line. This would only be possible in the IL sensor by including two CCD registers per column — requiring much greater packing density. The IL sensor therefore uses non-neighbouring lines to construct the composite video signal and so has poorer vertical resolution than the MOS-XY sensor. It does, however, have a lower noise level since the charges, being read out via CCD registers, are kept separate throughhout the signal path, in contrast to the MOS-XY, in which some charge mixing can occur within the aluminium address lines.
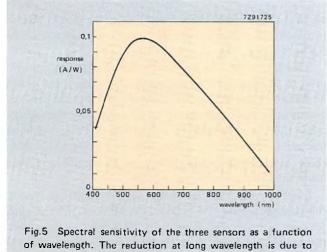
In these respects the FT sensor combines the advantages of both sensors since it uses neighbouring lines to construct the composite video signal, so its vertical resolution is comparable to the MOS-XY, and it reads out the charge via CCD registers and so its noise level is comparable to the IL sensor.

Sensitivity

Besides the effects of technology referred to above (i.e. $2\,\mu m$ versus $4\,\mu m$ technology), many other factors influence the sensitivity of the three sensors. For example, all three sensors use silicon for the photo-conversion process. If the correct dopant profiles and annealing treatments are used, silicon has a quantum efficiency of 1 for wavelengths between 300 and 1000 nm.

With a vertical anti-blooming structure, only electrons generated in the upper half of the p-well are collected, and for all sensors this causes quantum efficiency to decrease beyond 550 nm (Fig.5).

Furthermore, the refractive index step between silicon dioxide $(n = 1,45)$ and silicon $(n = 3)$ causes reflection losses, which can be limited by the proper choice of oxide thickness but only for a restricted wavelength range (450 to 500 nm).

Fig.5 Spectral sensitivity of the three sensors as a function of wavelength. The reduction at long wavelength is due to the p-well anti-blooming structure

Any parts of the imaging area covered with polysilicon suffer further losses due to reflection (which again can be optimized to some extent by proper choice of layer thickness) and absorption of short wavelengths (40% absorption at 450 nm, 80% at 400 nm). And of course, all regions covered by aluminium light shields will have zero sensitivity.

Combining all the above factors for equivalent sensors (i.e. realized in the same technology), we arrive at the quantum efficiencies given in Table 1. From this table you can deduce that for all visible wavelengths the IL sensor is less efficient than the MOS-XY and FT sensors.

Table 1
Quantum efficiencies of IL, MOS-XY and FT sensors

wavelength (nm)	IL	MOS-XY	FT
450	0,2	0,3	0,3
550	0,3	0,5	0,5
650	0,2	0,3	0,3

Noise

The noise produced by a sensor is just as important as quantum efficiency in determining its sensitivity. Here *noise* encompasses all factors contributing to spurious signals.

Thermal noise

Modern technology limits dark current to about $10\,nA/cm^2$ at $60\,°C$. This is equivalent to 7×10^3 electrons per charge packet in IL and MOS-XY sensors (2/3-inch camera format, 400 pixels per line), leading to a shot noise in the dark current of 80 electrons, and to 2×10^3 electrons per charge packet in the FT sensor (½-inch camera format, 600 pixels per line) leading to a shot noise of 40 electrons.

A second contribution to thermal noise is the noise introduced on resetting the CCD output node, which varies inversely with the square root of the output capacitance. For the IL and FT sensors, which currently have output capacitances of around 50 fF, this equals 90 electrons, and this number is likely to fall with improving design rules. For the MOS-XY sensor, the capacitance of the sense lines (around 1 pF) will always be the limiting factor and leads to a reset noise of around 400 electrons.

Since the output capacitance of both the IL and FT sensors is lower than that of the MOS-XY sensor, they are more susceptible to interference caused by spurious signals (frequency interference due to clock feed-through), but with proper camera design this will present no problem.

Finally, since most imagers use double source followers as output amplifiers, the thermal noise contributed by the amplifier should be the same for all. For an optimized amplifier design this lies at around 100 electrons.

Fixed-pattern noise

In silicon, the dark current is generated through transitions between localized energy levels between valence and conduction bands. These are known as recombination-generation centres and they're produced by impurities or crystal defects in the bulk of the material, or by what are known as *interface states* (imperfections at the interface between the silicon and the gate oxide). Because these are statistically distributed throughout the material, neighbouring pixels contain different numbers of them. The leakage current they produce gives rise to *fixed-pattern noise*. With current technology, this is dominated by interface states, which reach a concentration of around $10^9/(\text{cm eV})$. For minimum fixed-pattern noise, these interface states should be distributed as evenly as possible over the pixel area, which means that the standard deviation in the number of electron/hole pairs generated by these states should be a minimum.

In the IL sensor, roughly 1/3 of the pixel area contributes to fixed-pattern noise (the remainder of the area being covered by channel stops and CCD transfer cells whose contributions are averaged over each column). For 2/3-inch camera format and 400 pixels/line, the standard deviation in the number of electron/hole pairs generated is 660.

The MOS-XY sensor has roughly half the pixel area contributing to fixed-pattern noise, and for a 2/3-inch camera format and 400 pixels/line this gives a standard deviation of 800 in the number of electron/hole pairs generated.

Finally, in the FT sensor with 70% of the pixel area contribution to fixed-pattern noise, a ½-inch camera format and 600 pixels/line gives a standard deviation of 750.

Although on this basis the IL sensors appears to come out best, in reality the difference in these figure is insignificant and, for the dark current at least, there's no discernable difference in the fixed-pattern noise between the three sensors.

Shading

Shading is a gradual *long-range* change in sensitivity from one end of the sensor to the other due to dopant inhomogeneities, variations in RC times of gate electrodes and changes in the amplitude of the read-out register clocks after each line blanking period. Because all three sensors use similar dopant profiles (p-wells in high-ohmic n-substrates), none has a clear advantage in this respect, and as far as the other causes of shading are concerned, present state-of-the-art VLSI technology has virtually eliminated them.

Blooming

As we've already seen, all three sensors use a vertical p-well structure to prevent blooming of over-exposed pixels. Although the cross section shown is Fig.2 for the MOS-XY sensor is not optimal for vertical anti-blooming, it is possible to use the same double p-well structure as in the other two, so all three sensors have the same overexposure capabilities (of around several hundred times).

Smear

Smear is the continued build-up of photo-charge during the time it takes to shift out the integrated charge. Since this time is generally short compared with the integration period, smear becomes a problem only at high illumination intensities.

A customary way of indicating smear sensitivity is to give the ratio S of the smear signal (i.e. the signal generated while the photocharge is being shifted out) to the video signal when 10% of the image height is illuminated. For the FT sensor this equals $1/10 \, t_s/t_i$, where t_s is the time it takes to shift the integrated charge out and t_i is the integration time.
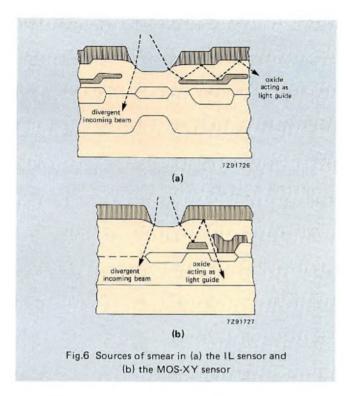
In the FT sensor, the charge packets are shifted quickly from the imaging region to the storage region during vertical blanking. For a 300 line sensor (NXA1010/1020), field transfer takes 0.47 ms, so S = 0.25%.

There are two ways to improve this figure: mechanical or liquid-crystal shutters (the latter applied on chip) which could conceivably reduce S to zero, or faster shift rates. Shift rates, however, are limited by the time constants of the polysilicon gates, but optimized technology might allow transfer rates as low as 0.05 ms giving S values of around 0.025%.

In the IL sensor, at the end of the integration period, all charge packets are shifted simultaneously into the vertical CCD shift registers where aluminium light shields protect them from smear. However, requirements of packing density and sensitivity limit the width of these light shields, so some light still reaches the CCD cells (Fig.6(a)). Although compared with the FT sensor only a fraction of this light contributes to smear, the integration time of the smear signal is substantially the same as that of the signal itself, so in practice S values for the IL sensor vary from 0.1% to 0.5%.

This figure can't be improved with shutters since they'd need to be closed during the integration period, but it can be improved by adding a storage section (at the expense of greatly increased chip area) and by improving the technology: thinner polysilicon gates for the CCDs and thinner insulation between polysilicon gates and light shields. With these latter developments, prototype IL sensors have been made with S values as low as 0.016%.

Smear in the MOS-XY sensor is very similar to that in the IL sensor. Here the drain of the MOS switches in each pixel must be shaded from light. This can't be done with the aluminium sense lines since their capacitance would then be too great. Instead, a second aluminium layer is used (Hitachi's MOS-XY sensor) giving S values of around 0.25%.

Fig.6 Sources of smear in (a) the IL sensor and
(b) the MOS-XY sensor

A thinner oxide layer between the aluminium layers
would minimize light leakage (Fig.6(b)) and reduce S, but
it would also increase the sense line capacitance. Future
developments, therefore, will probably see the S values for
MOS-XYs reduced to no less than about a half to a third
of current values.

Dynamic range

In the FT sensor, dynamic range is limited by the charge-
handling capacity of the vertical CCD registers. In the
MOS-XY, the charge-handling capacity of the aluminium
sense lines is practically without limit so the limitation is
instead imposed by the capacitance of the photodiodes. In
the IL sensor, either the vertical CCD registers (Sony with
MOS photosensitive elements) or the photodiodes (NEC)
limit the maximum signal. Table 2 compares (for 10 V
clocks) the maximum charge packets that can be handled
by 2/3-inch IL and MOS-XY sensors (400 pixels/line) and
by a ½-inch FT sensor (600 pixels/line).

Table 2
Maximum charge packets that can be handled

	storage (μm^2)	electrons/ ($\times 10^3$)	output (nA)
FT	45	360	690
IL (NEC)	80	400	510
IL (Sony)	90	720	920
MOS-XY	95	425	540

WHERE DO WE GO FROM HERE?

If we now summarise what we've discussed, we should be
able to arrive at some clear pointers for the future.

The main difference between the FT sensor on the one
hand, and IL and MOS-XY sensors on the other is the very
efficient use that the FT sensor makes of the imaging area.
This advantage can be used to produce superior resolution,
much improved sensitivity or smaller chip area.

Table 3
Sensor comparison — layout and cost factors

	IL	MOS-XY	FT
format	2/3-inch	2/3-inch	½-inch
pixels/line	400	400	600
pixels/column	600	600	300
chip area (mm^2)	85	85	66
design rule (μm)	2,5	2,5	3,5
dopant tolerances	———comparable———		

Table 4
Sensor comparison — consumer video cameras

	IL	MOS-XY	FT
triplets/line	200	200	200
lines to produce composite video	3	2	1
limiting horizontal resolution (MHz)	3,85	3,85	3,85
minimum scene exposure (lux)*	40	60	20
tolerance to overexposure	>100 ×	>100 ×	>100 ×
smear	0,15%	0,25%	0,25%

* f 1,4 S/N ratio 30 dB.

Table 5
Sensor comparison — professional applications
(black/white or three-chip colour)

	IL	MOS-XY	FT
limiting horizontal resolution (MHz)	3,8	3,8	5,8
minimum scene illumination (lux)*	20	30	10
tolerance to overexposure	>100 ×	>100 ×	>100 ×

* f 1,4 S/N ratio 30 dB.

The main differences between the MOS-XY sensor on the one hand, and the IL and FT sensors on the other are the MOS-XY sensor's initial cost advantage due the fact that it can currently be manuafctured using Hitachi's CMOS process established for its DRAMs, and the IL and FT sensors' superior sensitivity — thanks to their extremely low output capacitance. And with the possibility of producing the FT sensor with a smaller chip area, the potential cost advantage of the MOS-XY sensor is completely negated.

Moreover, with the enormous growth in image sensor applications over the next few years, the tremendous design flexibility of the FT sensor is bound to play an important role, and could well be the decisive factor in securing for it the supreme position.

Finally, it's probably true to say that, in most respects, the FT sensor combines and improves on all the good features of the other two sensors and inherits few of their bad ones. If we had to make a prediction, it would undoubtedly be that the FT sensor, with its inherent advantages is the most likely one to dominate the market in the future.

Whatever the outcome, the next few years are going to be very interesting ones indeed on the solid-stage imaging front.

ACKNOWLEDGEMENT

Controller IC contends with multiple protocols

JIM MAGILL

The need to transfer large amounts of data at high speed between several local workstations and large computer systems has generated a variety of message transaction schemes or protocols. While several protocols have evolved, development of dedicated controller ICs to handle them has not kept pace.

Now, a single-chip VLSI device, the SCN68562 Dual-Channel Universal Synchronous Communications Controller (DUSCC), Fig.1, incorporates circuitry for virtually all subsystems and functions required in advanced data communication systems. The chip provides interfacing to advanced DMA controllers and supports such interrupt structures as vectored, daisy-chained, priority, and masked using minimum external logic. In many applications, the DMA and interrupt interfaces are implemented easily through direct connections from the DUSCC's request and acknowledge lines to the control bus.

The DUSCC's two independent data communications channels permit substantial programming flexibility for handling multiple protocols. Because of variations in bit- and character-oriented protocols, a controller must provide a more encompassing solution for high performance data communication systems. For example, when the transmitter/receivers can be operated either as full-duplex synchronous or asynchronous channels, the chip can embrace a broad range of advanced bit- and character-oriented protocols, including HDLC/ADCCP, SDLC, X.25, X.75 link level, IBM Bisync, DDCMP, and X.21.

AN ARCHITECTURAL OVERVIEW

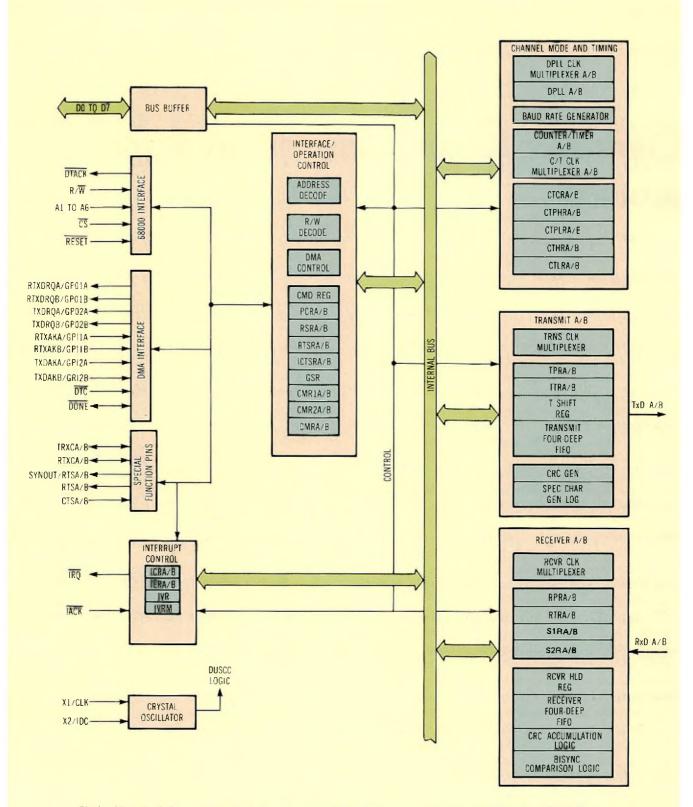Architecturally, the DUSCC has four major sub-sections: interface and operational controls, timing circuitry, channel receivers, and channel transmitters. The interface and operational control section handles transactions between the device and its various interfaces, coordinates activities between the other sections, and executes commands. Interface circuitry extends to a host processor, an interrupt structure, the DMA, and multifunction pins.
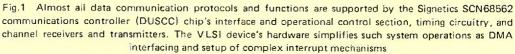
The host processor interface is dedicated to the complete set of control, data, and bus signals for the 68000 microprocessor. Eight DMA interface pins can be configured to provide individual DMA request and acknowledge signals for the individual transmitters and receivers. An additional control signal, $\overline{\text{DONE}}$, provides flow control. For example, it can signify the completion of a message sequence and the termination of DMA operation.
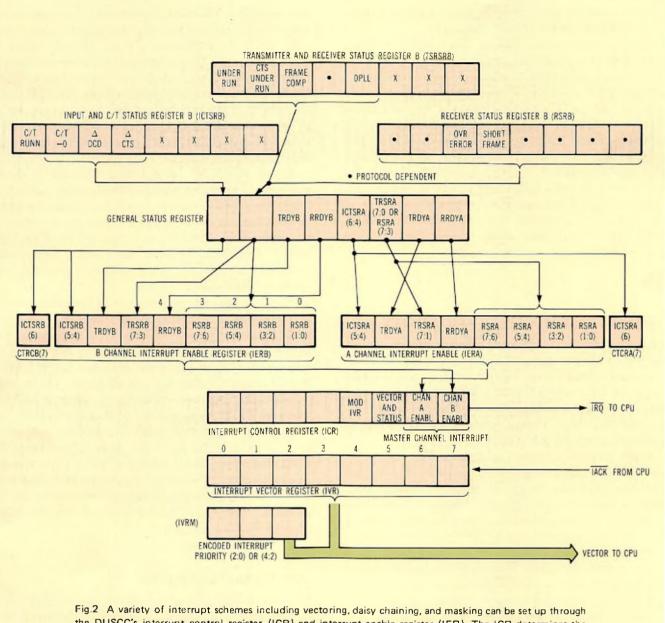
A triple set of registers configures each channel. The channel-mode configuration pair (CMR1 and CMR2) selects the channel protocol/transmission mode, message format, and error-check sequence. The system interface and pin configuration register (PCR) selects the function of the multifunction pins.
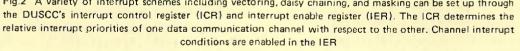
Each channel's interrupt structure is controlled through the interrupt control (ICR) and interrupt enable (IER) registers. (Figure 2 shows the interrelationship between these registers and the kinds of information stored.) Channels follow a fixed interrupt priority starting with receiver ready, transmitter ready, receiver or transmitter status condition, and finishing with external event or counter/timer ready. The relative priority of interrupts of one channel with respect to the other is selected through the ICR. These priority combinations are A before B, B before A, and alternating priority with either A or B as highest. Other bits in the ICR select vectored or nonvectored interrupt operation and vector format when the vectored mode is selected.

Fig.1 Almost all data communication protocols and functions are supported by the Signetics SCN68562 communications controller (DUSCC) chip's interface and operational control section, timing circuitry, and channel receivers and transmitters. The VLSI device's hardware simplifies such system operations as DMA interfacing and setup of complex interrupt mechanisms

Fig.2 A variety of interrupt schemes including vectoring, daisy chaining, and masking can be set up through the DUSCC's interrupt control register (ICR) and interrupt enable register (IER). The ICR determines the relative interrupt priorities of one data communication channel with respect to the other. Channel interrupt conditions are enabled in the IER

Interrupt masking can be performed either on individual groups or channel-interrupt conditions using the IER, or on an entire channel under control of the ICR. In addition to handling interrupt request and acknowledge signals, the DUSCC provides a mechanism for creating interrupt daisy chains using its X2/IDC pin to propagate the interrupt acknowledge signal. Most application timing functions can be derived from the DUSCC's internal timing circuitry. This section consists of independent 16-bit timer/counters and digital phase locked loop (DPLL) circuits for each channel, and a common crystal clock and baud rate generator.

Clock signals for the transmitters and receivers can be selected from an external source or from one of the internal sources mentioned above.

The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2/IDC pins or from an external clock connected to the X1/CLK pin. The oscillator's output provides the clock signal for the DUSCC's logic and other internal timing circuits.

The baud rate generator runs off the oscillator signal or on the external signal, generating 16 baud rates simultaneously. These signals are made available to the receiver,

transmitter, DPLL, and counter/timer. Since the 16 baud rates are available simultaneously, each receiver and transmitter can select its baud rate independently.

Each channel includes a DPLL that is used in synchronous mode to recover clock information from the received data stream. Each DPLL contains a 6-bit counter that is incremented by sampling a clock signal at 32 times the nominal data rate. The clock source can be from an external input, the receiver baud rate, the counter/timer, or the crystal oscillator. The DPLL uses the sampling clock signal together with the received data to construct a data clock that can be used as the DUSCC receiver data clock, transmitter clock or both. This results in a DPLL square wave output clock at a data rate that can be programmed to be sent out on a special pin. Users can select NRZ/NRZI, FM0. FM1, or Manchester as the encoding format of the received data.

TRANSMITTER/RECEIVER FLEXIBILITY

Dedicated hardware is integrated within the transmitter and receiver circuits to generate and detect special character sequences, to generate various error sequences and to handle many of the overhead tasks associated with advanced message formats. The large number of operational registers for each channel and the concise set of control commands allow easy setup and operation of the DUSCC.

Each transmitter channel consists of three major sections: clock multiplexer and control registers; first in, first out and shift register; and special character generation logic. After a channel is configured for a protocol/transmission mode, transmitter operation is refined by the contents of the transmitter parameter register (TPR) and the transmitter timing register (TTR).

The transmitter's clock source is selected from inputs to the transmitter-clock multiplexer. Inputs are the channel counter/timer, the other channel's counter/timer, baud rate generator, DPLL, or an external clock signal. The TPR selects the clock source and baud rate if the baud rate generator is chosen as the transmitter clock signal.

The transmitter accepts parallel character data from the data bus and loads the data into the transmitter FIFO register (TxFIFO), which consists of four 8-bit holding registers. Data is then moved to the transmitter shift register (TxSR), which serializes it according to the transmission format. The TxSR can also be loaded from special character logic or from the cyclic redundancy check/longitudinal redundancy check.

The transmitter-ready signal, TxRDY, indicates the status of the TxFIFO and is set either when an empty position exists in the FIFO or if the entire FIFO is empty. The user can choose the frequency of service requests because the DMA and interrupt service request follow the state of TxRDY.

The receiver architecture is basically similar to that of the transmitter. The receiver consists of a clock multiplexer and control registers, FIFO and shift register, receiver data path, and error accumulation logic. After a channel is configured for the transmission mode, receiver operation is refined by the contents of the receiver parameter register (RPR) and receiver timing register (RTR). The RPR selects the number of bits per character and controls operation of an external enable control line for all receiver transmission modes. The interpretation of the remaining bits in the RPR depends on the transmission mode selected.

Timing signals are selected from the receiver timing multiplexer. Its inputs are an external timing source, the baud-rate generator. channel counter/timers, and the DPLL output clock. The clock source and data rate selections of the baud-rate generator are made through the RTR. This register also selects the DPLL clock source from among counter/timers. external source, baud-rate generator, and crystal oscillator inputs.
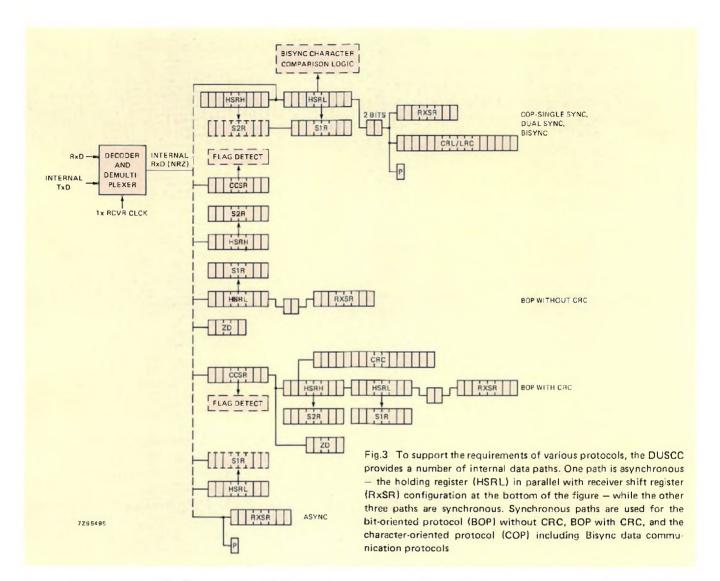
No single data path can support the diverse requirements of the various transmission modes efficiently. Thus, the DUSCC data path can be viewed as four separate paths — an asynchronous path and three paths to support the requirements of different protocols. Each data path is responsible for assembling characters into the receiver shift receiver (RxSR). After assembly, characters are sent to the receiver FIFO along with appropriate status information.

The receiver FIFO consists of four 8-bit holding registers with appended status bits. Data is loaded into the FIFO after a character is assembled; data is removed when a character is read. The state of the receiver FIFO (RxFIFO) is indicated by the receiver ready status signal (RxRDY). As in the operation of the transmitter, a user can choose when the RxRDY bit is set.

DOWN THE DATA PATHS

The asynchronous path of the DUSCC comprises the holding register (HSRL) and the RxSR in parallel. The HSRL path is active only if a character comparison option is selected. In this case, all incoming data is matched against the contents of the S1R register on a bit-by-bit basis to determine a character match. If a match is obtained, a flag in the receiver-status register is set. This feature can be used to generate an interrupt. If the character comparison option is not selected, character data is shifted only to the RxSR. After a character is assembled in the RxSR, it is loaded into the RxFIFO.

Synchronous data paths can be pictured as one of three parallel paths that become active in the following channel conditions: a character-oriented protocol (COP) with or without a block-check character (BCC); a bit-oriented protocol (BOP) without BCC and BOP with BCC. The COP path contains the two 8-bit holding registers (HSRH and HSRL) in series with the shift register, CRC accumulation

Fig.3 To support the requirements of various protocols, the DUSCC provides a number of internal data paths. One path is asynchronous — the holding register (HSRL) in parallel with receiver shift register (RxSR) configuration at the bottom of the figure — while the other three paths are synchronous. Synchronous paths are used for the bit-oriented protocol (BOP) without CRC, BOP with CRC, and the character-oriented protocol (COP) including Bisync data communication protocols

logic, two synchronizing flip-flops, and special Bisync comparison logic. Data entering this path is held first in either or both of the holding registers. During each bit time, data in the register (or registers) is compared with the contents of either the S1R register or the S1R and S2R registers. Comparison depends on the synchronizing pattern chosen — whether the pattern uses single or dual SYN characters. A match is indicated by the setting of a status bit in the receiver status register (RSR).

The BOP without a BCC path uses three parallel inputs to the character comparison (CCSR), HSRH, and HSRL registers, in series with the receiver register. In this arrangement, data is shifted into the three registers simultaneously. The holding pair of shift registers compare their contents with the S1R and S2R registers to determine if the correct station address has been received. All data entering this path is compared in the CCSR for the flag sequence. When a match occurs, the status bit in the RSR is set. Data entering the HSRL is assembled in character form in the RxSR and then transferred to the FIFO. Zero deletion occurs on all data received unless a flag or abort is detected.

In the case of the BOP with BCC data path, the CCSR, the holding registers, and the RxSR, are arranged in series. The CCSR remains active throughout a message frame and compares the incoming bit stream to determine the flag sequence. The address is compared using the 16-bit holding registers. As character data bits are shifted from the CCSR to the holding register pair, they generate the received BCC character according to the selected accumulation format of the CRC/LRC logic.

In Bisync mode, special comparison logic checks for control sequences and is active for both normal and transparent operation. Comparisons can be made either with EBCDIC or ASCII text messages as selected in the channel mode register. When detected, these sequences either cause a status bit in the RSR to be set or initiate special processing. This comparison logic makes the DUSCC a powerful tool for processing Bisync text. It frees the processor from searching for these special sequences and eliminates the need for additional processing associated with such sequences.

MINIMUM HARDWARE

An advanced two-channel data communication system can be implemented with the DUSCC. (The Table depicts the specifications for a typical data communication system supporting the different protocols.) Because so much of the hardware is already in the device, few additional parts are required.

Since the DUSCC provides separate DMA request and acknowledge signals for the transmitter and receiver, the full-duplex requirement for channel A is satisfied with a minimum of hardware between the DMA controllers and the DUSCC.

The complex vectored interrupt scheme for channel B is established by programming the interrupt control register for vectored interrupts and their formats. Separate interrupt vectors can be generated for the transmitter, receiver, and counter/timer by selecting bits in the interrupt control register. An interrupt masking can be performed through the interrupt-enable register. The interrupt interface involves simply connecting the interrupt request and acknowledge signals to the appropriate control bus signals. No additional hardware is necessary to complete this portion of the design.

A minimum of design is required to select the various interfaces for both channels. For channel A, five registers are used to select the channel interfaces and to set up the protocol requirements. Channel-configuration registers CMR1 and CMR2 establish the DMA structure and define operation of the data channel. External inputs are defined by the pin-control register and the address of the secondary station is stored in the S1R and S2R registers. Channel B is set up just as easily. But it requires additional programming of the interrupt control and enable registers to establish the interrupt structure.

Operating refinements for each channel are made through the transmitter and receiver parameter registers (TPR and RTR). These define the message format and select automatic features that are invoked under various transmitter and receiver conditions. The channel A transmitter, for example, is set up to terminate the BOP message automatically by sending an end of message sequence and then marking the data line when an underrun occurs. In similar fashion, channel B is set up to linefill with a sync pattern until another character is loaded into the transmitter when an underrun occurs. These actions do not require the intervention of the host processor.

Advanced dual-channel DMA		
	channel A	channel B
system interface	full-duplex DMA	vector interrupt separate vectors channel transmit/receiver, end of message characters, and mask off all other conditions
	Tx req on FIFO empty	Tx req on FIFO not full
	Rx req on FIFO full	Rx req on FIFP not empty
Tx clock	ext clock	ext clock
Rx clock	DPLL-Manchester encoded internal sampling clock	ext clock
protocol	bit-oriented protocol – secondary address CRC CCITT preset to 0's single control byte	bisync CRC-16 preset to 1's

Once the interfaces are established, transmitter and receiver operations are controlled and monitored through the command and the transmitter/receiver status registers. The DUSCC provides a set of commands that directly supports transmission of Bisync and BOP messages. Each command performs an action necessary to generate a message in the specific protocol. In Bisync, the first character of a message after the SYN pattern is an SOH, STX, or DLE-STX pattern. The send-DLE command not only sends the DLE-STX sequence, but the command can be appended to any character to transmit special control sequences as the protocol requires.

In BOP mode, the message frame after the flag character consists of 0 to n address bytes, followed by 1 or 2 control bytes. The sequence is transmitted by loading the data into the transmitter FIFO. After the last control byte, the transmitter switches automatically to the programmed character length. A feature of the transmitter is its ability to send the last character for a bit count less than the programmed character length by specifying a shorter character length in the output/miscellaneous register.

ACKNOWLEDGEMENT

Alloy bonding for power semiconductors

A. JONAS and D. ONCK

The die bond is crucial to the quality, and, hence, the true cost. of power semiconductors. Stresses in the bond due both to the nature of the bond itself, and to the temperature cycling experienced by the device in service, play a large part in the conformity and reliability experienced by the OEM (equipment manufacturer).

The demands of modern industry on device quality place a growing emphasis on the integrity of these die bonds. Moreover, these same demands require that any change in manufacturing technology be thoroughly proven before delivery commences.

The alloy bonding process, developed to contain the cost increases caused by the price of gold, has, therefore, been subject to extensive investigation. Devices now being delivered are of a quality equal to that obtainable with older processes, and ultimate quality promises to be even higher.

DIE BONDING PROCESSES

Traditionally, there have been two methods for bonding silicon dice to their mounting bases: hard soldering and soft soldering.

Hard soldering using gold-silicon eutectic is known as eutectic bonding (Ref.1). In this process, stress developed in the crystal due to the difference in thermal expansion between silicon and the copper header is relieved by the plastic deformation of the copper during cooling down from the bonding temperature. The process allows medium-sized dice to be hard soldered directly to copper; it has the advantages of excellent thermal fatigue performance and low thermal resistance in rectifiers, thyristors and triacs.

This low thermal resistance makes for improved SOAR performance of transistors. Hard solder never plastically deforms, so there is no fatigue failure mechanism for the joint between the die and mounting-base.

Soft solder (Pb-Sn) always plastically deforms to take up the stress caused by the thermal mismatch between silicon and copper. This keeps the stress in the die low, but means that the solder fatigues during temperature cycling.

The high price of gold forced us to look for a lower cost hard soldering process — a new process that must still meet the electrical performance and quality of the eutectic-bonding technology.

After exhaustive trials, we selected for production a bonding process using a tin-silver-antimony bonding alloy: this is known as *alloy bonding*. Tests on alloy-bonded devices demonstrated that they could meet the required standards of reliability and electrical performance. Subsequent production experience has amply confirmed our expectations.

ALLOY BONDING

The tin-silver-antimony alloy was chosen as the die-bonding medium to replace both eutectic bonding and soft-soldering in the majority of power-semiconductor applications. The tin and antimony provide the structural strength and the silver component improves the die-to-header or lead frame thermal resistance.

The die-attach process using this alloy includes a scrubbing phase in which the die is rubbed into the alloy to improve adhesion and eliminate voids. Bonding takes place at about 300 °C, significantly lower than for eutectic bonding. This not only makes the process easier to control but also reduces the stresses in the semiconductor die itself.

With eutectic bonding, the high stress imposed on the die limits the application of the process to dice less than about 4 mm square. With soft soldering, the stresses concentrated in the bond place excessive demands on the bond integrity itself. Alloy bonding results in stresses distributed throughout the structure, so that the advantages of a harder die bond can be extended to larger dice. Moreover, the improved stress distribution results in a more rugged device, reducing failures resulting from the attachment of devices to heatsinks.

PROCESS-CHANGE APPROVAL

If the ppm quality levels essential to economic equipment production are to be consistently achieved, no significant process change should be made without thorough investigation of the consequences. Accordingly, the alloy-bonding process has been subjected to a rigorous Significant-Change procedure that includes pilot production with full Quality investigation and consultation with major customers. Approval of the process was obtained at a formal Significant-Change meeting at which all relevant data, especially quality data, were reviewed in depth.

The Approval procedure was also used to prove the success of alloy bonding for each family of devices that was to use the process. Results of the associated tests are given for two types of device in the following sections.

ALLOY BONDING OF THYRISTORS AND TRIACS

The introduction of the alloy-bonded BT139 triac was, at first, viewed very critically. Much has been said about the high reliability of the eutectic-bonded version (Ref.2). It was decided, therefore, that before the new process was adopted it would have to prove that it could meet the normal acceptance criteria and match, or exceed, the electrical performance and reliability of the old process.

The majority of the tests chosen for the comparison can be classed as "extreme environmental" tests. Wherever possible, the tests have been continued until a significant number of devices have failed, to allow the distribution of failures to be compared. Test conditions and results are summarized in Tables 1 and 2.

Note that, owing to the 'learning curve', current production of alloy-bonded devices exhibits higher quality than that indicated by the Approval test results.

Drop test

For this test, each device is dropped three times from a height of 75 cm onto a maple-wood block. 100 devices of each type were tested. Only one device from each sample failed. Analysis revealed that, in each case, failure had been caused by a cracked die. (Failure rates in drop tests in current BT139 production devices are less than 0,4%).

TABLE 1	
Test conditions – BT139	
test	conditions
drop test	3 drops from 75 cm
pressure cooker	steam at 122 °C and 210 kPa
humidity with bias	50 V, 85 °C, 85% RH
rapid change of temperature	−40 °C → 120 °C
temperature cycling by liquid immersion	0 °C → 100 °C water
damp heat, cyclic	85% RH, 55 °C for 16 h, 85% RH, 25 °C for 8 H
thermal fatigue	16 A r.m.s., ΔT_j = 95 °C

Autoclave

This test checks the device for corrosion under extreme conditions of humidity and heat; 70 devices of each type were tested. Post-test measurements were performed within one hour of removal from test. No statistically-significant difference was observed between eutectic and alloy-bonded devices.

Humidity with Bias

20 devices of each type were biased to 50 V in a humidity chamber set to give 85 °C, 85% RH. None of the devices tested suffered degradation of characteristics after 168 h.

Rapid change of temperature

This is the standard cycling test performed between the permitted extremes of storage temperature; 50 devices of each type were tested. Two of the eutectic-bonded devices were leakage-current rejects after 15 temperature cycles.

Temperature cycling by liquid immersion

This is the cycling test required by CECC to release plastic-encapsulated devices. 50 BT139 devices of each type were tested; one eutectic-bonded device was found to have failed after 10 cycles.

Damp heat, cyclic

This test, also required for CECC release, was carried out on 100 devices of each type; no failures occurred in 20 days' testing.

Thermal fatigue

This test applies the maximum thermal conditions possible in practical applications. It is performed by mounting the devices on heatsinks and cycling the temperature between 25 °C and $T_{j\,max}$. This is done by alternating periods of self heating, using the maximum allowable device current, and periods of forced cooling, by turning off the current and passing cold water through the heatsinks.

TABLE 2
Summary of results

test	sample	failures	
		eutectic bonded	alloy bonded
drop test	100	1	
	100		1
bump test	20	12 after 10 shocks	
	20		0 after 10 shocks
mounting test	20	see Fig.1	
	20		see Fig.2
riveting test	50	1	
	50		0
autoclave	70	3	
	70		2
humidity with bias	20	0	
	20		0
rapid change of temperature in air	50	2	
	50		0
temperature cycling by liquid immersion	50	1	
	50		0
damp heat cyclic	100	0	
	100		0
thermal fatigue	45	see Fig.3	
	20		see Fig.4

Bump test

This is a special test that generates extreme shocks in the mounting tab: well in excess of those permissible in practice. Of the 20 eutectic-bonded devices tested, 12 were rejects after 10 shocks. None of the 20 alloy-bonded BT139s failed after 10 shocks; the test was continued on one device to 160 shocks, without failure occurring.

Mounting test

This test simulates the effect of fastening a device onto a concave heatsink. It consists of applying a continuous distorting force to the tab of a device supported along each side.

A sample of 20 devices of each type were tested and the observed distortions at failure were plotted on Weibull distribution paper, Figs 1 and 2. It was intended that each device would be bent until it failed, but 10 of the alloy-bonded BT139s did not fail at the 400 μm distortion available.

Fig.1 Weibull plot of cumulative failure percentage versus distortion on mounting eutectic-bonded BT139 triacs
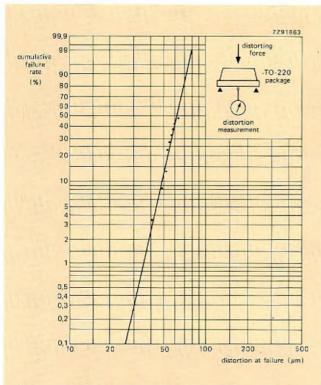
Fig.2 Weibull plot of cumulative failure percentage versus distortion on mounting alloy-bonded BT139 triacs. Compare with Fig.1

Fig.3 Weibull plot of cumulative failure percentage against number of thermal cycles for eutectic-bonded BT139 triacs
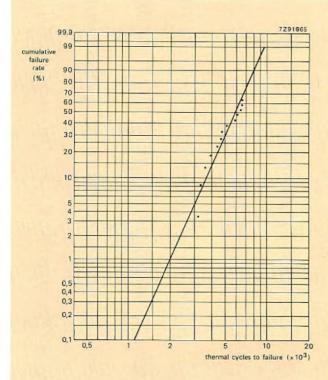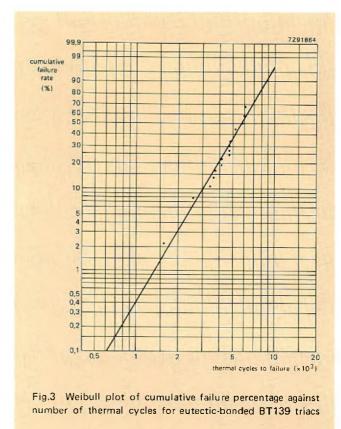

Fig.4 Weibull plot of cumulative failure percentage against number of thermal cycles for alloy-bonded BT139 triacs. Compare with Fig.3

Riveting test

This test is performed by fastening devices to an aluminium strip using pop rivets. Of the 50 devices of each type tested, only one (eutectic-bonded) device failed.

Note: this method of mounting is not recommended owing the large mechanical tolerances involved.

Measurements

In addition to the reliability tests, we performed a full electrical characteristic comparison. Figures 5 to 8 show the distribution of V_{T1}/V_{T3}, $R_{thj\text{-}mb}$ and I_{TSM} for a sample of each version of the BT139.

Conclusions

The results obtained from the drop test, the humidity with bias test, the autoclave test, thermal fatigue and damp heat cyclic tests demonstrate that alloy-bonded devices perform no differently from eutectic-bonded devices. The results from the bump test, mounting test, riveting, rapid change of temperature and temperature cycling tests indicate that alloy bonding improves reliability.

On the basis of these results we decided that alloy bonding was not only an acceptable process, but even preferable to eutectic bonding because of the more rugged devices it yielded.

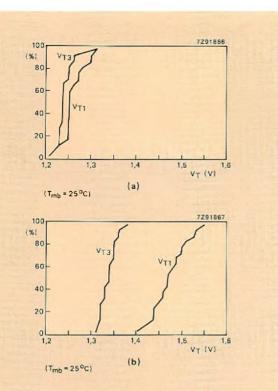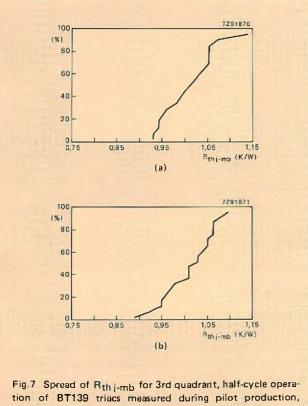Fig.5 Spread of ON-state voltages V_{T1} and V_{T3} for BT138 triacs measured during pilot production: (a) alloy bonded, (b) eutectic bonded
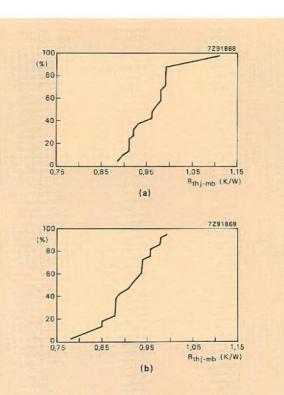

Fig.6 Spread of R_{thj-mb} for 1st quadrant half-cycle operation of BT139 triacs measured during pilot production, (a) alloy-bonded, (b) eutectic bonded

Fig.7 Spread of R_{thj-mb} for 3rd quadrant, half-cycle operation of BT139 triacs measured during pilot production, (a) alloy-bonded, (b) eutectic bonded
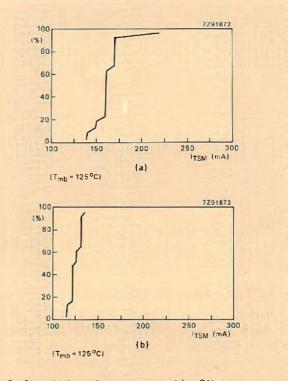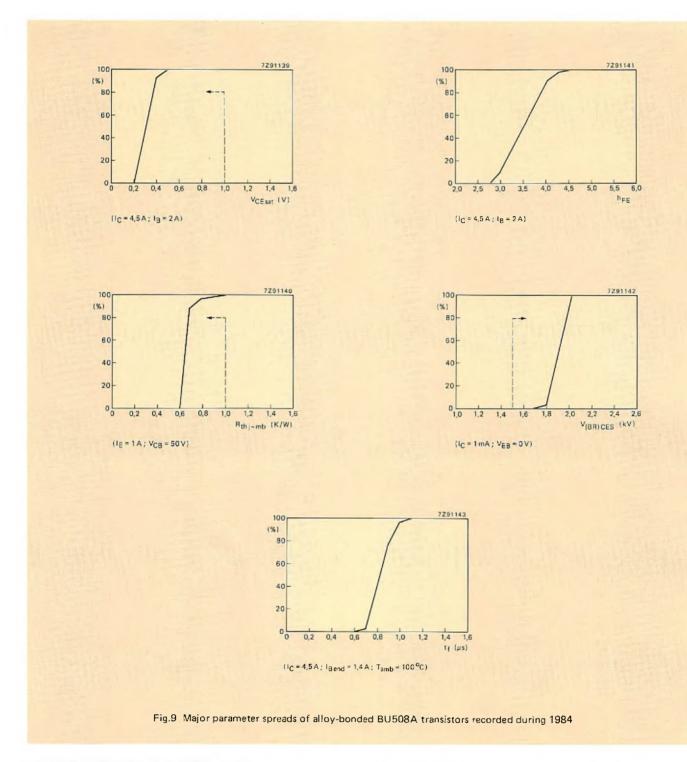

Fig.8 Spread of maximum, non-repetitive ON-state current for BT139 triacs measured during pilot production, (a) alloy-bonded, (b) eutectic bonded

Fig.9 Major parameter spreads of alloy-bonded BU508A transistors recorded during 1984

ALLOY-BONDED TRANSISTORS

A number of power transistor types with alloy die bonds are now in production. Of these, the BU508A was the first to be introduced as on alloy-bonded device. We therefore decided to compare the BU508A in the SOT-93 plastic encapsulation with the older BU208A soft-soldered TO-3 device that it is intended to replace. The quality of the production BU508A is examined in detail in a later section.

Test conditions

The endurance tests used in the comparison are detailed in Table 3, which should be read in conjunction with the device data given in the Data Handbook. Note that, in nearly every case, test conditions for the BU508A are more severe than those for the BU208A.

In addition to the endurance tests, a full programme of mechanical and environmental tests appropriate to each device envelope was performed. These are listed in Table 4.

TABLE 3

Comparative test conditions BU208A, BU508A

This table should be read in conjunction with the device data

	BU208A	BU508A
d.c. cut off	$V_{CB} = 750$ V, $T_{amb} = 100\,°C$	$V_{CB} = 750$ V, $T_{amb} = 125\,°C$
a.c. cut off	$V_{CB} = 1500$ V, $T_{amb} = 100\,°C$	$V_{CB} = 750$ V, $T_{amb} = 125\,°C$
dissipation	$P_{tot} = 8$ W, $T_{j\,max} = 115\,°C$	$P = 20$ W, $T_{j\,max} = 150\,°C$
thermal	$I_E = 6$ A, $\Delta T = 80\,°C$	$I_E = 6$ A, $\Delta T = 80\,°C$
practical circuit	$I_C = 4,5$ A, $V_{CE} = 1350$ V $T_{amb} = 55\,°C$	$I_C = 4,5$ A, $V_{CE} = 1350$ V, $T_{amb} = 55\,°C$
wet cut off		$V_{CB} = 500$ V, $T_{amb} = 55\,°C$ RH = 95%
V_{EB} cut off	$V_{EB} = 5$ V d.c., $T_{amb} = 125\,°C$	$V_{EB} = 5$ V d.c., $T_{amb} = 125\,°C$
high temp. storage	$T_{amb} = 115\,°C$	$T_{amb} = 150\,°C$
low temp. storage	$T_{amb} = -65\,°C$	$T_{amb} = -65\,°C$

TABLE 4

Mechanical and environmental tests used in the comparison exercise

BU208A	BU508A
pressure cooker test	
lead fatigue	lead fatigue
soldering heat	soldering heat
temperature cycling	temperature cycling
moisture resistance	moisture resistance

Stability and leakage current

Table 5 gives the results of the tests designed to reveal defects that could cause variations in device characteristics or increase leakage current during life. Overall failure rates to an upper confidence level of 60% are also given.

Given the more severe test conditions for the BU508A the results for the two devices are comparable. The difference between the calculated failure rates is due solely to the smaller number of device hours testing available for the BU508A, which widens the confidence band.

Power handling

Table 6 gives the results of the tests designed to investigate the reliability of devices when handling their rated power. Again, results are comparable, despite the more severe conditions under which the BU508A was tested.

TABLE 5

Results of stability and leakage-current tests

test	BU208A (failures/sample)		BU508A (failures/sample)	
	168 h	1000 h	168 h	1000 h
d.c. cut off (V_{CB})	0/540	0/110	0/120	0/120
a.c. cut off	0/500	0/130	0/100	0/180
d.c. cut off (V_{EB})		0/30		0/20
wet cut off		—		0/20
failure rate (60% UCL)	2×10^{-6}/h		$2,3 \times 10^{-6}$/h	

TABLE 6
Results of power-handling reliability tests

test	BU208A (failures/sample)		BU508A (failures/sample	
	168 h	1000 h	168 h	1000 h
dissipation	–	0/20	–	0/70
practical circuit	–	0/110	–	0/20
bottoming	–	0/10	–	0/10
storage, low temperature	–	0/30	–	0/50
stotage, high temperature	–	0/30	–	0/50
failure rate (60% UCL)	5×10^{-6}/h		5×10^{-6}/h	

TABLE 7
Structural-integrity test results

test	BU208A (failures/sample)	BU508A (failures/sample)
	(TO-3)	(SOT-93)
thermal fatigue	0/460 (720 cycles)	1/1258 (200 cycles)
mechanical and environmental	0/380	1/300
50 cycles, $-65\,^{\circ}$C to $+150\,^{\circ}$C	–	0/60

Structural integrity

Table 7 gives the results of the tests designed to explore device structural integrity. Again, results are comparable: the 60% confidence level thermal-fatigue reliability of the BU508A is slightly better than that of the BU208A.

Conclusions

These results show that BU508A (alloy-bonded in SOT-93) can be expected to be at least as rugged and reliable as the BU208A (soft-soldered in TO-3).

ALLOY BONDING IN PRODUCTION

Many power-semiconductor types are now produced with alloy bonding of the die to the lead-frame. The BU508A power transistor, and the BT139 triac have the longest production history of alloy bonding. Together, their production quality history gives a good indication of the potential of the process for good conformity and high reliability in other types of power device.

Power transistors

Reliability

Table 8 gives the results of our factory Quality Control Department's Group C testing of BU508A transistors during 1982 and 1983. These tests are carried out at stress levels corresponding to the combined Absolute Maximum ratings for the device. Despite the comparatively small number of device-hours' testing due to the short production history, it is evident that the devices come up to expectations. The thermal-fatigue results show a failure rate at 60% UCL of less than 2%/1000 h. As the confidence band decreases with more device-hours' testing, this value can be expected to decrease.

TABLE 8
Production Acceptance test results, BU508A, 1982/1983

test	duration	device hours (x 10³)	complete failures
dissipation	1 week	1,68	0
(operating life)	6 weeks	60	0
thermal fatigue	1 week	8,4	1
	6 weeks	70	0
cut off, d.c.	1 week	221,76	0
(high temp.)	6 weeks	408	3
cut off, a.c.	1 week	42	0
	6 weeks	280	0
cut off, wet	1 week	11,76	0
	6 weeks	130	0
storage, low	1 week	5,04	0
temperature	6 weeks	40	0
storage, high	1 week	5,04	0
temperature	6 weeks	40	0

Thyristors and triacs

Reliability

Table 9 gives the results of both d.c. blocking and thermal fatigue tests on alloy-bonded thyristors and triacs for 1982 to 1984. Note that the d.c. blocking test is an overstress test. By operating at 10 °C above maximum rated temperature, the effects of this test are effectively accelerated sixfold.

Conformity

The outgoing process average for inoperatives for 1984 was about 200 ppm. Figure 9 shows the spreads of major parameters measured on production devices during 1984.

The thermal fatigue test consists of repeated 2½ minute cycles: about 1 minute ON and 1½ minutes OFF. The end of the ON period is when the device junction temperature reaches $T_{j\,max}$; the end of the OFF period is when the junction temperature reaches 25 °C. Water cooling is used to speed the rate of cooling and so increase test severity.

Allowing for the effect of acceleration, the real failure rate revealed by the d.c. blocking test is about $4,4 \times 10^{-6}$/h with 60% confidence.

The thermal fatigue tests were prolonged beyond 1000 h until failure occurred. During this period, the first failures occurred at between 33 000 and 51 000 test cycles (1375 and 2125 h). The 1000 h failure rate revealed by these tests is $7,5 \times 10^{-6}$/h at 60% confidence. Results from production thermal fatigue tests are plotted on the Weibull chart of Fig.10.
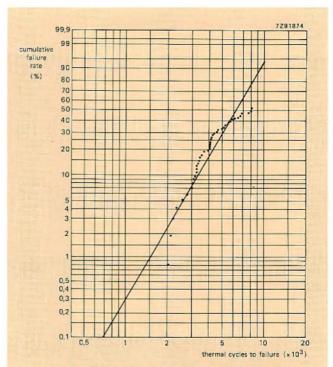

Fig.10 Weibull plot of cumulative failure percentage against number of thermal cycles for production BT138 and BT139 triacs during 1983, 1984 and 1985

TABLE 9
Production Periodic test results, alloy-bonded thyristors and triacs, 1982 to 1984

test	duration	device hours (x 10³)	complete failures	failure rate (60% UCL) (x 10⁻⁶/h)
d.c. blocking	1 week*	3180**	2	0,97
a.c. blocking	1 week*	2030**	0	0,45
high temp. storage	6 weeks	280	1	7,2
low temp. storage	6 weeks	440	0	2,09
thermal fatigue		(see Fig.10)		

* Accelerated test, 1 week is equivalent to 9 weeks at $T_{j\,max}$.

** Derated to $T_{j\,max}$.

Conformity

Figure 11 gives the process average for inoperatives for BT139 triacs during 1983 and 1984. As can be seen, the recorded (ppm) process average was zero for a number of months, reflecting the very high quality achieved by the alloy bonding process.

Figure 12 gives spreads of V_T, I_{TSM}, and T_{th} recorded during 1983. These should be compared with Figs.5 to 8.
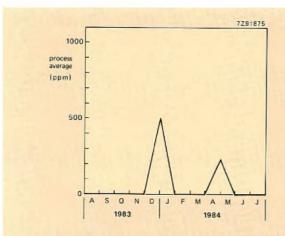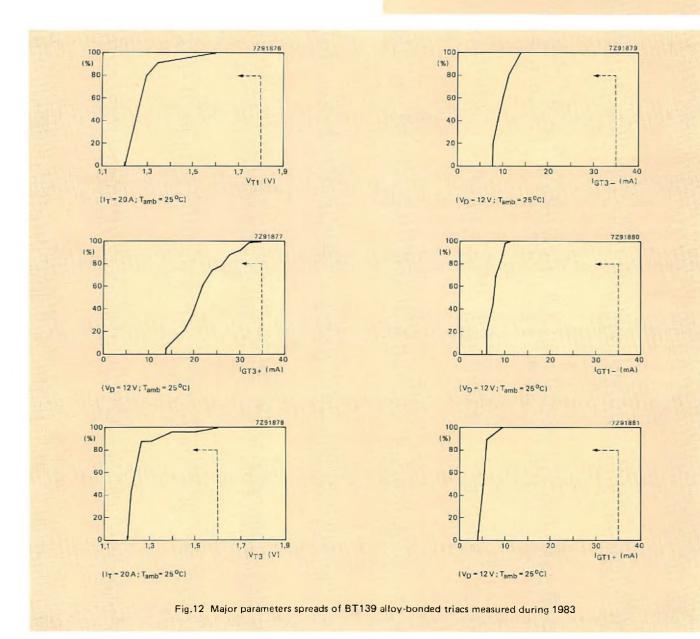

Fig.11 Process-average reject level for inoperatives for BT139 alloy-bonded triacs, 1983/84

Fig.12 Major parameters spreads of BT139 alloy-bonded triacs measured during 1983

CONCLUSIONS

The alloy bonding process was exhaustively tested before being used in production. The tests showed that, especially for larger dice, alloy bonding could be expected to be equal or superior to both the more expensive gold-silicon eutectic die bond and the conventional soft-solder die bond.

Subsequent production experience has confirmed the indications of the Release testing. It is evident that both the conformity and the reliability of power devices with alloy die bonds are high and can be expected to steadily improve.

References

1. LEENDERS, W. et. al. 1974. Titanium-gold: high-reliability transistor metallization. Electronic Applications Bulletin 32, 70-80 (No. 2).
2. 1979. Reliable thyristors and triacs in TO-220 plastic packages. Philips Technical Note No. 130.

VMEbus interface ICs for simpler asynchronous systems

S. BALIGA

The development of synchronous single-chip controllers for VMEbus-based systems vastly simplified the circuitry needed to coordinate bus traffic. However, as welcome as they were, these controllers could not perform as efficiently as the more complex multi-chip asynchronous ones. To simplify asynchronous systems, a family of bus interface ICs incorporating all the control logic for coordinating asynchronous bus traffic has been designed. The family comprises:

— a bus controller (SCB68175)

— an interrupt generator (SCB68154)

— an interrupt handler (SCB8155).

The bus controller, alone or with the two interrupt ICs, is for asynchronous operation in master-only configurations. It is compatible with 68000-based, or similar, bus masters and can be used in dual-port master boards by adding a dynamic RAM controller (74LS764). An error and retry scheme enables the 68175 to transfer data fast with minimum user-intervention. The 68175 resembles the 68172 VMEbus controller which it can replace in some designs.

The interrupt generator is for VMEbus and VERSAbus systems. It can assign up to seven priority levels to interrupts.

Finally the interrupt handler services interrupts received through a distributed multiprocessor system or generated locally.

These three ICs can reduce significantly the components needed in an asynchronous VMEbus system.

FROM MASTER TO SLAVE

Figure 1 shows a typical multiprocessing system comprising system master (master 1), master-slave and slave-only stations. A system arbiter determines which station has control of the bus at any time. For the system master and master-slaves, the bus controller chip SCB68175 coordinates data transfers over the system bus, or between the master and the slaves. Any master containing an interrupt handler SCB68155 can, in addition, receive and service interrupts generated by slaves having an interrupt generator SCB68154.
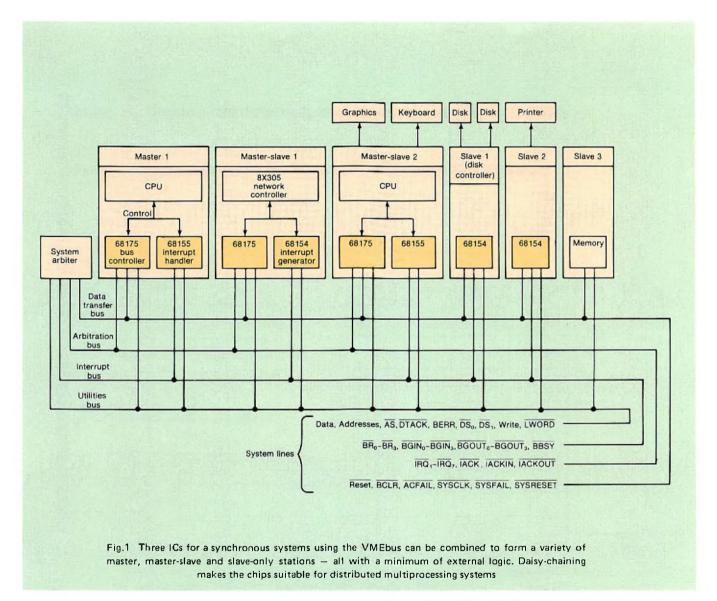
The system arbiter uses a priority arbitration scheme that recognizes up to four levels of bus request. It is usual to assign the system master third priority (by tying the controller's Bus Request output ($\overline{BR}$) to the system's $\overline{BR}_1$ line) to give the master-slaves higher priority. A master must vacate the system bus whenever a master with higher-priority requests the bus. For the system master, this requirement is met by merging bus request lines $\overline{BR}_2$ and $\overline{BR}_3$ with a local bus release-line from the CPU, at a NAND gate.

Since the system resources are available to all master-slaves, any peripheral can be accessed by a non-slave station. Therefore, a master can be interrupted by a request for information about a process that it did not initiate. To ensure time isn't spent acknowledging irrelevant interrupts, this system can be ordered to generate interrupt requests only on those lines to a station that can answer the request.

One of the master-slaves accesses an external network through the 8X305 microcontroller interface. This interface transfers data between the network and the system's global memory after it gains access to the system bus by means of its own bus controller.

Typically, the network's master-slave is given the second highest priority in the system by tying the output of its bus controller to the $\overline{BR}_2$ line. To ensure a master vacates the system bus whenever a higher-priority master requests it, the bus release line from the local CPU is merged with Bus Request $\overline{BR}_3$ at a NAND gate.

Fig.1 Three ICs for a synchronous systems using the VMEbus can be combined to form a variety of master, master-slave and slave-only stations — all with a minimum of external logic. Daisy-chaining makes the chips suitable for distributed multiprocessing systems

The user can access the multiprocessing system through an intelligent graphics terminal having the highest priority. The system master and master-slave 2 (Fig.1) allow graphics to be processed by the system. Graphics primitives are drawn in the master-slave's bit-mapped memory.

The slave-only stations allow the user to communicate with peripherals such as disks and printers. Slave 1 is accessed by both the master station and the graphics terminal, whereas slave 2 is a printer accessed only by the system master. The peripherals and system CPU exchange data through a local buffer, which eliminates the need for transfers through the global memory. The disk controller does not have to acquire the global system bus, so it doesn't require a 68175 bus controller.
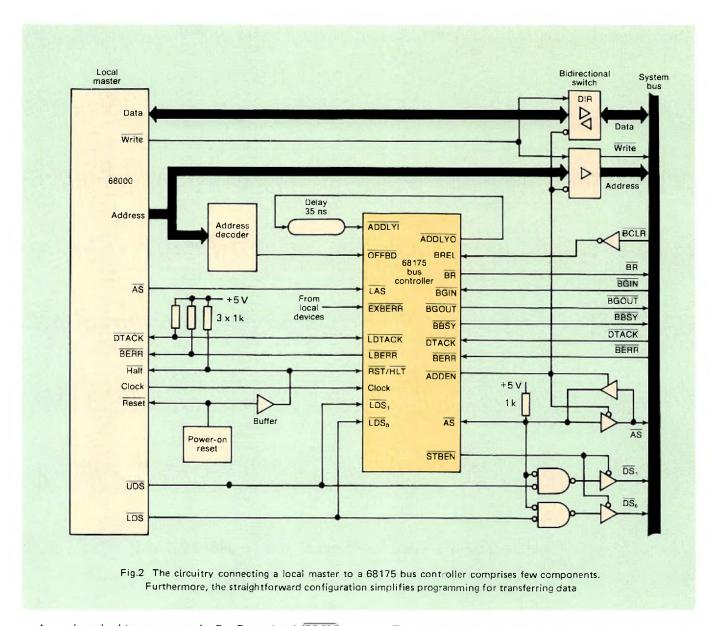
The memory slave responds only to data transfer cycles generated by the three masters. To make the system faster, an interrupt generator could be included in the memory slave to notify the master of reading and parity errors, for example.

68175 BUS CONTROLLER

Figure 2 shows the circuitry of a 68000 local master communicating with a 68175 bus controller. In a bus cycle, the address decoder initiates accesses to the system by bringing the Offboard signal ($\overline{\text{OFFBD}}$) LOW, see Fig.3. When the local master's Address Strobe ($\overline{\text{AS}}$) also goes LOW, the 68175 requests control of the system bus by asserting its $\overline{\text{BR}}$ line which along with the BR lines of all other 68175s in the system is monitored by the system arbiter to allow bus access to the requesting master.

All four bus request levels may have more than one requestor. The system arbiter selects a level and grants the associated requestor control of the bus. When there are several requestors with the same level, the daisy-chained Bus Grant lines are used to give one control. The system arbiter informs the master that it has control by pulling its Bus Grant In line ($\overline{\text{BGIN}}$) LOW. If no request is pending for a master given control of the bus, the daisy-chain signal is passed on via the Bus Grant Out line ($\overline{\text{BGOUT}}$).
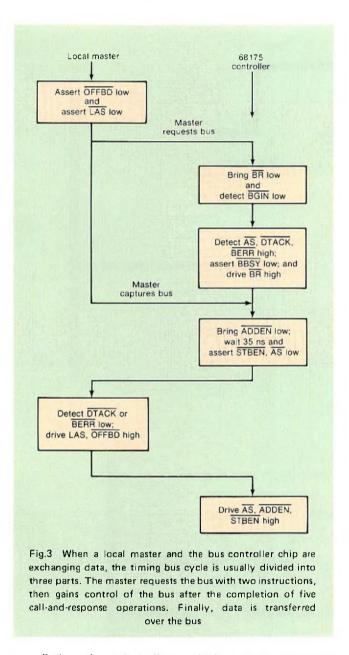
Fig.2 The circuitry connecting a local master to a 68175 bus controller comprises few components. Furthermore, the straightforward configuration simplifies programming for transferring data

An on-board arbiter prevents the Bus Busy signal ($\overline{\text{BBSY}}$) from being applied to the system bus if $\overline{\text{BGIN}}$ is received before $\overline{\text{BR}}$ was asserted. This eliminates bus contention during the $\overline{\text{BGIN}}\text{-}\overline{\text{BGOUT}}$ sequence. The bus controller can then take control of the bus as soon as the bus is free, that is, when $\overline{\text{AS}}$, Data Transfer Acknowledge ($\overline{\text{DTACK}}$) and Bus Error ($\overline{\text{BERR}}$) are all HIGH. Once in control, the bus controller determines the sequencing of the address, data and strobe signals for each bus cycle.

The transfer of data between a master and slave begins when $\overline{\text{AS}}$ is asserted. A 35 ns delay line connected between the device's Address Delay Out ($\overline{\text{ADDLYO}}$) and Address Delay In ($\overline{\text{ADDLYI}}$) ports gives the required address set-up time.

If the data cycle is terminated successfully, $\overline{\text{DTACK}}$ is received from the slave. The bus controller will then bring its own $\overline{\text{DTACK}}$ LOW. If the cycle is terminated by a bus error, the slave sends $\overline{\text{BERR}}$.

To terminate bus errors, the bus controller asserts both the Local Bus Error ($\overline{\text{LBERR}}$) and the Halt ($\overline{\text{HLT}}$) signal, allowing the local CPU to retry the bus cycle. If a second consecutive bus error occurs, the retry is terminated; only $\overline{\text{LBERR}}$ is asserted. The 68175 also allows a single-cycle retry for local cycles that terminate in an error via its external bus error $\overline{\text{EXBERR}}$ input. Local devices may drive the $\overline{\text{LBERR}}$ line LOW directly to by-pass the retry.

The termination of a bus cycle does not mean that the 68175 has relinquished control of the bus, since the Bus Release signal (BREL) determines the number of cycles awarded to the controller. In the simplest case, BREL can be tied HIGH, allowing a single cycle release-when-done operation, in which case the controller gives up the system bus at the end of the cycle. Therefore, a bus request must be initiated each cycle.

Alternatively, a DMA controller can assert BREL after a number of cycles set by the user. This option increases the

Fig.3 When a local master and the bus controller chip are exchanging data, the timing bus cycle is usually divided into three parts. The master requests the bus with two instructions, then gains control of the bus after the completion of five call-and-response operations. Finally, data is transferred over the bus

overall throughput, but allows a higher-priority master to request the system bus while multiple cycles are being run by the current master. It is therefore expedient to ensure that the higher priority master's waiting time is minimized.

For bus release-on-request, BREL should be combined with additional logic. The bus controller will ensure that $\overline{\text{BBSY}}$ will be asserted at least 90 ns before BREL is released, thus meeting VMEbus specifications. $\overline{\text{BBSY}}$ is ultimately used by the system's arbitration logic to resolve system bus requests, since arbitration can only begin when $\overline{\text{BBSY}}$ is HIGH.

68155 INTERRUPT HANDLER

The addition of a 68155 to boards already having a VMEbus controller gives complete interrupt-handling capability.

The 68155 handles interrupts according to priorities indicated by non-maskable interrupts and, within the same level, also assigns priorities to the six local interrupts — all before servicing the bus interrupts. Interrupt lines IRQ_1 to IRQ_7 are each assigned to a priority level; each interrupt's binary equivalent appears on lines IPL_0 to IPL_2 (Fig.4(a)). Interrupts are acknowledged by the assertion of the Interrupt Acknowledge signal ($\overline{\text{IACKDS}}$). If a bus interrupt is the highest-priority interrupt pending during an acknowledge, the interrupt-handler asserts its Bus Interrupt Acknowledge signal ($\overline{\text{BIACK}}$) used to generate the $\overline{\text{IACK}}$ signal. The user controls the interrupt handler through eight internal registers.
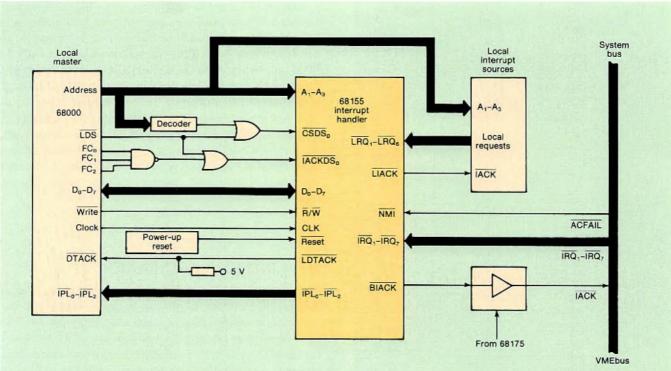
68154 INTERRUPT GENERATOR

The configuration for generating interrupts from a local master's instructions is just as straightforward, and the operation is almost identical. Under local CPU control, the 68154 generates interrupt requests on any of the bus interrupt lines (Fig.4(b)). It responds to an interrupt acknowledge sequence by supplying an interrupt vector as well as all handshake signals required to transfer this vector to the local master.

During an interrupt acknowledge sequence, only one of the seven possible VMEbus interrupt levels is acknowledged. An interrupt-driven system may support multiple interrupt devices. As before, a daisy-chained scheme is used to acknowledge a single interrupter. As soon as the system's $\overline{\text{IACK}}$ signal appears, the daisy chain starts at the first location in the system bus. The interrupt level acknowledged appears on system address lines A_1 to A_3. If the interrupt generator has recorded an interrupt request and receives an Interrupt Acknowledge In signal ($\overline{\text{IACKIN}}$), there is no need for it to pass the daisy-chain signal. However, if no interrupt request is pending on the level being acknowledged, it will pass the signal down the daisy-chain link to the next board via the Interrupt Acknowledge Out line ($\overline{\text{IACKOUT}}$).

The interrupt generator responds to the interrupt sequence only on receipt of the system $\overline{\text{DS}_0}$, $\overline{\text{IACK}}$ and $\overline{\text{IACKIN}}$. It also asserts the Buffer Enable signal ($\overline{\text{BUFEN}}$) so that the corresponding interrupt vector can be placed on the system bus. The generator supplies the seven most-significant bits of the interrupt vector, including the five most significant bits of its internal control register, R_0, linked with bus address lines A_2 and A_3.

Interrupts appearing at, say, the N level are generated by the local CPU, which writes a logic 1 to bit N of internal register R_1. An interrupt request then appears on $\overline{\text{IRQ}_N}$. When an interrupt is acknowledged, the appropriate bit in R_1 is cleared and the local CPU reads R_1 to determine whether the interrupt was acknowledged. To enable or disable an interrupt, the user sets bit 2 in the vector register R_2.
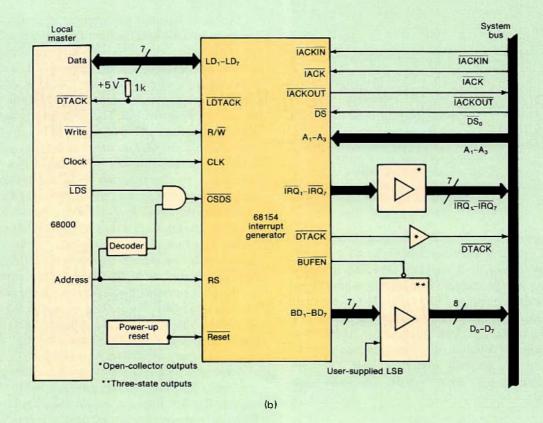
(a)

(b)

Fig.4 Communication between a local master and (a) the interrupt handler, or (b) the interrupt generator, is simple. In both cases, the sequence of bus operations is similar

Data flows between the interrupt generator and the local CPU via the local data bus in conjunction with the Register Select input (RS), Read/Write line (R/$\overline{W}$) and Chip Select ($\overline{CSDS}$) signals. The 68154 also generates the $\overline{LDTACK}$ signal which confirms the transfer of data between the local CPU and itself.

COMBINING THE POWER

Extremely efficient master boards can be made by using two or all three ICs. For example, a 68175 bus controller with a 68155 interrupt handler together create a subsystem that handles system bus requests and interrupt-acknowledge sequences completely, see Fig.5.

The 68155 can receive local interrupt requests while the subsystem is acknowledging a bus interrupt on the same level. The 68155 resolves arbitration disputes by gating all local interrupt requests through internal (transparent) latches that are activated during each interrupt acknowledge cycle.

The 68155 includes six local interrupts (LRQ_1 to LRQ_6) for the local CPU master board. The interrupts can be programmed in three ways — active-HIGH, active-LOW, or edge-triggered signals.

During an interrupt acknowledge sequence, vectors can be supplied in two ways. In the vectored mode, the chip places a vector on the local data bus and asserts $\overline{LDTACK}$. The vector is formed by linking the upper five bits of R_2 (the user-programmed local vector register in the 68155)

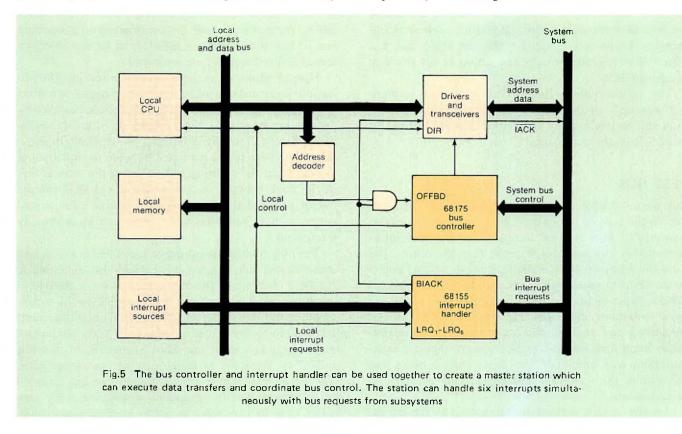with the level representing the pending local interrupt request.

In the second mode, the interrupting device places its own interrupt vector on the local data bus and asserts $\overline{LDTACK}$. The 68155's local interrupt mask register, R_3, lets the user enable local interrupts selectively. The state of the local interrupt requests is held in register R_4, and status register R_7 records the last interrupt to be acknowledged.

The Non-Maskable Interrupt line ($\overline{NMI}$) has the highest priority. The interrupt handler responds to an $\overline{NMI}$ request with a vectored interrupt cycle. In distributed interrupt-handling systems, two or more ICs may receive interrupt requests and request control of the system bus. To ensure that the handler with the highest pending interrupt gets control of the bus first, the VMEbus controller's $\overline{BR}$ lines are used to set priorities (Fig.1).

All data transfers between the local CPU and the interrupt handlers occur along the local data bus lines. The transfer is coordinated via the address bus, the Chip Select line ($\overline{CSDS_0}$) and R/$\overline{W}$.

ACKNOWLEDGEMENT

Fig.5 The bus controller and interrupt handler can be used together to create a master station which can execute data transfers and coordinate bus control. The station can handle six interrupts simultaneously with bus requests from subsystems

Manually testing the a.c. characteristics of ECL ICs

C. HAMELIN

When manually testing the a.c. characteristics of ECL integrated circuits, measurements accuracy depends largely on the accuracy with which the input waveforms can be initially set-up repeated. Unfortunately, digitally-controlled pulse generators which can automatically and accurately repeat waveforms once they have been set-up are very expensive and not yet widely available. The main factor contributing to measurement accuracy and repeatibility is therefore the ability of operators to adjust the analog controls of conventional pulse generators with sufficient accuracy to precisely duplicate the amplitude and d.c. offset of waveforms for each new set-up or for checking equipment drift.

This article outlines methods by which the accuracy and repeatedly of the measurement of the a.c. characteristics can be improved by eliminating as many variables as possible from the test set-up.

TEST JIGS

One major variable when manually testing a.c. characteristics is the type of test jig used. Every test engineer has his own idea of what an ideal test jig is, and it is difficult to say whether any one idea is better than the others. The main aim when designing a test jig, however, should always be to eliminate variables. For instance, a $50\,\Omega$ environment should always be maintained so that reflections which can cause waveform anomalies are reduced. This includes eliminating any unterminated stubs which are more than about 6 mm long because, at ECL speeds, they can cause reflections with amplitude and phase characteristics that can distort the wavefront and degrade the accuracy of measurements.
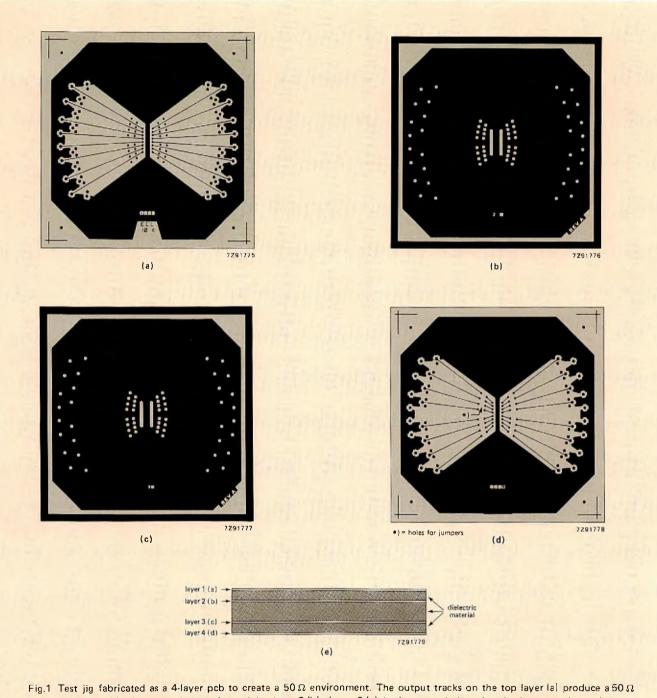
Another variable is the delay introduced by the test jig.

This is the delay contributed by the test jig over and above that of the DUT (Device Under Test). Although it is quite simple to design and construct a test jig that cancels the effects of its own internal delay, it will then necessarily be dedicated to one IC type or group of IC types having the same pinning for inputs and outputs. Since many test jigs of this sort would have to be constructed to test the full range of ECL ICs, this would be a rather expensive solution to the problem. Fortunately however, some compromises can be made which allow the construction of a common test jig that is completely satisfactory as far as cost-effectiveness and test integrity are concerned.

Figure 1 shows an example of such a test jig. The pcb has four layers and uses micro-stripline techniques to achieve a constant $50\,\Omega$ environment. Test jig delay is cancelled by deriving the input signal reference for the sampling oscilloscope directly from the DUT input pin as shown in Fig.2. Since the length of the pcb track between the input pin of the DUT and the reference output pad is the same as that of the track between the output pin of the DUT and the output pad, and the same length of coaxial cable is connected to both pads, the delay of the test jig is virtually transparent.

The only problem remaining is that there is a 6 cm long unterminated stub (unused input track) also connected to the DUT output pin. This causes aberrations on the output waveform which may or may not be visible on the oscilloscope display depending on their amplitude and their phase relationship to the actual output signal. These aberrations may appear as a slight overshoot or undershoot or subtle roll-off of the rising or falling edge of the output pulse. The signal may appear grossly distorted or not distorted at all except that the measured propagation delay may differ from its true value by a few hundred picoseconds.

(a) 7Z91775

(b) 7Z91776

(c) 7Z91777

*) = holes for jumpers   (d) 7Z91778

layer 1 (a)
layer 2 (b)
layer 3 (c)
layer 4 (d)
dielectric material
(e) 7Z91779

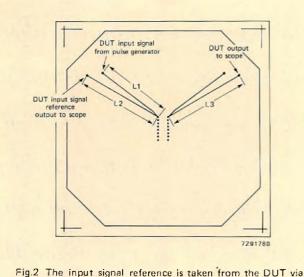Fig.1 Test jig fabricated as a 4-layer pcb to create a 50 Ω environment. The output tracks on the top layer (a) produce a 50 Ω micro-stripline with the ground-plane formed by layer 2 (b). Layer 3 (c) is the ground-plane for the input tracks on bottom layer 4 (d). Note the holes for the jumpers. In the cross-sectional view (e), the space between layers 2 and 3 merely provides rigidity for the test jig

This unwanted stub could be eliminated by simply cutting the unused input track, but this would prevent the test jig from being used for a different IC having an input pin at this location. In Fig.3, the input tracks incorporate discontinuities (A and C) across which jumpers can be fitted as appropriate for the specific DUT. Without a jumper, as in the case of an output pin, the unterminated stub is only about 6 mm long. Even at 100K ECL speeds, this stub is not long enough to delay the reflected signal sufficient to cause distortion of the waveform (the return-journey delay in the stub is much less than the transition time of the output signal).

With a jumper fitted, as in the case of an input pin, the line is terminated with the oscilloscope input impedance and, although there is a small break (less than 6 mm long) in the 50 Ω stripline, the impedance difference is so slight

Fig.2 The input signal reference is taken from the DUT via length L1. Since the two output tracks (L2 and L3) are the same length, jig delay cancels-out leaving only the delay through the DUT package and circuitry

Fig.3 The input track has a jumper (A) installed but the output track has no jumper (B), leaving a stub (C) less than 6 mm long

that is causes only slight distortion of the input signal to the DUT. Since the input signal reference to the oscilloscope is derived from a point after the jumper (directly at the input pin of the DUT), the oscilloscope and the DUT see the same signal and the DUT tends to ignore the minor aberrations at its input.

It is also very important to remember to use adequate bypass and filtration capacitance for the power supply because the extremely short rise and fall times associated with ECL cause extremely high instantaneous power factors during transitions. Bypass and filter capacitors must be positioned as close as possible to the DUT supply and ground leads.

MEASURING EQUIPMENT AND THE HUMAN FACTOR

As previously mentioned, pulse generator waveform variations probably have the greatest influence on the accuracy and repeatability of the measurement of a.c. characteristics. They are also the most difficult to control because operators can't accurately duplicate exactly the same set-up for each test session. The following procedures are recommended to eliminate as many of the operator and equipment variables as possible.

Setting-up the d.c. offset of the input signal

Many sampling oscilloscopes which have a digital readout can display precise values of amplitude, transition time and propagation delay but don't have provision for digitizing the d.c. offset of signals from ground. Also, because the
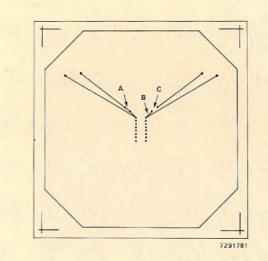
oscilloscope display is small, and because of the graticule resolution and parallax error, the eye cannot consistently resolve the d.c. offset to within less than 10 to 20 mV. However, an error of even 2 or 3 mV in the adjustment of the d.c. offset of the input signal will cause a propagation delay measurement error of several tens of picoseconds for a 10K ECL IC.
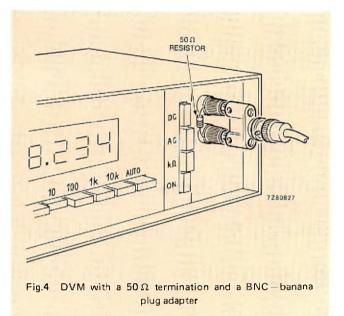
The repeatability of the d.c. offset setting for the input signal for 10K ECL ICs can be significantly improved by using a few additional pieces of standard laboratory equipment, including a high quality DVM (Digital Voltmeter) with a resolution of 1 mV or better. Although 100K ECL ICs are considerably less sensitive to input signal variations, it is advisable to use the same set-up precautions as those for 10K ECL ICs.

When setting the d.c. offset of the input signal with the aid of a DVM, a few assumptions have to be made. Firstly, it is assumed that a squarewave without d.c. offset with an amplitude A and a duty cycle of exactly 50% will cause a display of A/2 on a DVM when it is set to measure d.c. volts. Secondly, it is assumed that any d.c. offset added to the signal merely increases A/2. Finally, it is assumed that the bandwidth of the DVM is sufficient to prevent significant roll-off of the squarewave signal which could introduce non-linearities into the measurement. Although making these assumptions will decrease the accuracy of measurements, their repeatability will not be impaired as long as the same DVM is always used.

Bearing the foregoing assumptions in mind, adjust the d.c. offset of the input signal as follows:

1. Set the pulse generator output signal to a repetition rate of approximately 1 MHz with a duty cycle of exactly 50% (a frequency counter should be used for this).
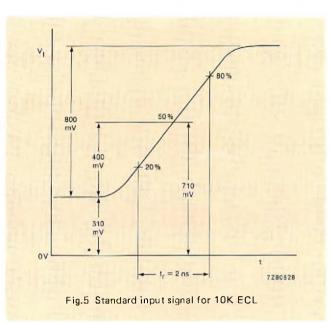
Fig.4   DVM with a 50 Ω termination and a BNC — banana plug adapter

Fig.5 Standard input signal for 10K ECL

2. Using a sampling oscilloscope with a digital readout set to measure volts, adjust the amplitude of the pulse generator output signal to 800 mV (for 10K ECL) with a d.c. offset of 0 V (i.e. the negative-going peak of the signal is 0 V and the positive-going peak is 800 mV).

3. Adjust the rise and fall times to 2 ns ± 0,2 ns between the 20% and 80% amplitude points (for 10K ECL).

4. Since the amplitude and transition time adjustments may interact, repeat steps 2 and 3 until satisfied with the adjustment accuracy.

5. Disconnect the 50 Ω coaxial cable from the input of the sampling oscilloscope and connect it to a DVM which is set to measure d.c. volts and has its input terminated with 50 Ω. In most cases, the latter can be accomplished with a BNC — Banana Plug adaptor with a 50 Ω precision resistor connected between the two DVM input terminals as shown in Fig.4. In any event, the 50 Ω termination should be as close as possible to the DVM input terminals. The DVM should read 800 mV d.c./2 = 400 mV.

6. The standard d.c. offset for a 10K ECL input signal is 310 mV (see Fig.5). This can now be set by adjusting the d.c. offset control of the pulse generator so that the DVM reads:

$$(800\,mV/2) + d.c.\ offset = 710\,mV$$

The accurately set input signal can now be connected to the test jig, but it should be periodically checked for drift throughout each test session. It may be necessary to use variations of this method to suit individual test requirements, but as long as the basic principle is followed, one of the major variables in testing the a.c. characteristics of ECL will be brought under control.

Effect of temperature on d.c. offset voltage

The bias voltage (V_{BB}) of 10K ECL ICs is temperature dependent. Furthermore, the temperature coefficient is not the same for all IC types due to internal power dissipation and various other characteristics, but it is approximately 1,1 mV/°C. This influences the amount of d.c. offset which must be applied to the input signal for measuring a.c. characteristics at ambient temperatures other than 25 °C. For example, if the IC were to be tested at 85 °C, the d.c. offset applicable at 25 °C (310 mV) would have to be increased to:

$$1,1\,(T_{amb} - 25) + 310\,mV = 376\,mV$$

From the formula in step 6 under the previous heading, this should cause a DVM reading of 776 mV.

100K ECL ICs have internal temperature compensation which virtually eliminates any drift due to variation of operating temperature. A d.c. offset of 310 mV can therefore be used over the entire temperature range for these ICs. However, as shown in the Table, the input pulse parameters for 100K ECL ICs differ slightly from those used for 10K ECL ICs, but the same principles apply to both families and the same measuring procedures and precautions apply.

Input pulse parameters for ECL ICs
(T_{amb} = 25 °C)

input pulse parameter	ECL family	
	10K	100K
amplitude	800 mV	740 mV
d.c. offset	310 mV	310 mV
t_r, t_f	2 ns	700 ps
repetition rate	1 MHz	1 MHz
duty cycle	50%	50%

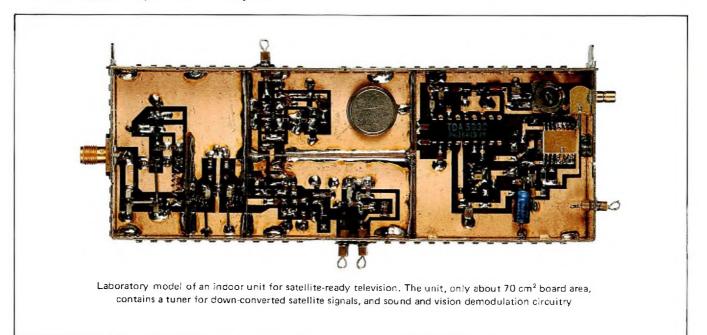# Indoor unit for satellite-ready tv

A. DOLSTRA

Regular Direct Broadcast Satellite (DBS) television services for most countries in Europe are scheduled to begin during 1987. Among the potential benefits of direct satellite broadcasting are the simultaneous nationwide availability of the service and the option of a wider bandwidth signal, the latter providing:

- improved picture quality

- additional sound channels for stereo or foreign language sound-tracks

- improved Teletext service with immediate access to individual pages.

We are developing components for all aspects of satellite tv reception, in consultation with manufacturers of DBS receiving equipment. By making the right components available in volume and on time, we aim to satisfy the needs of the emerging satellite-tv industry, giving set designers and manufacturers the option of producing satellite-ready tv sets now. It is anticipated that satellite-ready sets will accept a plug-in indoor unit to give full satellite tv reception when available, in addition to normal u.h.f. and v.h.f. broadcast tv and videotex. Of course, the circuitry of the indoor unit could be inside the set itself or, in a cable tv system, in the head-end station.

This article introduces suitable active components for the satellite tuner and i.f. amplifier of an indoor unit.

Laboratory model of an indoor unit for satellite-ready television. The unit, only about 70 cm² board area, contains a tuner for down-converted satellite signals, and sound and vision demodulation circuitry

INDOOR UNIT

Figure 1 shows the components of a satellite-tv receiving system. A down-converted satellite signal (950 MHz to 1750 MHz) from an outdoor unit enters an indoor unit comprising tuner, tuning control, and sound and vision processing circuitry.

The tuner of the indoor unit selects an f.m. channel and converts the signal to an i.f. of 479,5 MHz. After amplification, the i.f. signal is filtered by a surface acoustic wave (SAW) filter and demodulated before being applied to the sound and vision processing circuitry. This separates the audio and the video components of the baseband signal, the latter being processed further in the tv set to produce the RGB drive signals for the picture-tube.

Figure 2 shows a schematic of the tuner and demodulator of an indoor unit. Apart from the f.m. demodulator, the unit is substantially independent of the sound and vision processing format, e.g. D2-MAC, C-MAC or PAL. The performance of a typical indoor unit is given in Table 1. Table 2 gives a survey of the main r.f. active components used in the unit's tuner.

TABLE 1

Typical performance of an indoor unit for receiving DBS transmissions

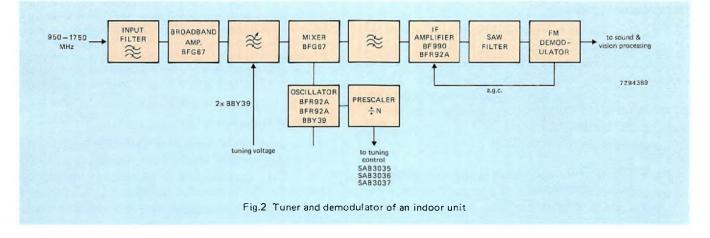|	
frequency range	950 to 1750 MHz
r.f. input operating level	−55 dBm to −25 dBm
intermediate frequency	479,5 MHz
noise figure	<12 dB
intermodulation distortion	−50 dB
input impedance	75 Ω

TUNER

Owing to the high gain of the outdoor unit, the noise figure specifications of the tuner can be relaxed. Consequently, the tuner is instead designed for minimum intermodulation distortion.

Surface mounted components are used in the tuner to minimize parasitic inductance and capacitance and to reduce the tuner's size.

Front-end

An input filter suppresses image frequencies and matches the input of a high-gain (about 10 dB up to 1,8 GHz) broadband amplifier designed around a BFG67 transistor. This transistor which has a transition frequency of 7,5 GHz is one of the most advanced wideband r.f. transistors available. Its fine electrode structure (probably the finest available with current manufacturing techniques) is obtained by using a modified planar-epitaxial process that needs just one mask to produce the base regions, completely eliminating alignment problems.

Another BFG67 is used in the mixer that generates the i.f. of 479,5 MHz. Such a high i.f. reduces the number of tuned filters needed. Furthermore, all image frequencies are outside the incoming down-converted signal band.

Fig.1 Components of a satellite-tv receiving system

Fig.2 Tuner and demodulator of an indoor unit

TABLE 2
Brief data on the main r.f. active components of the tuner of the indoor unit (typical values)

	encapsulation	power gain (dB)	noise figure (dB)	transition frequency (GHz)	diode capacitance at 1 MHz (pF)	capacitance ratio[1]
BFG67 transistor	SOT-143	10[2]	3[3]	7,5[4]	–	–
BFR92A transistor	SOT-23	15,5[5]	1,8[6]	5[7]	–	–
BBY39 varicap diode	SOT-23	–	–	–	1,8–2,0	>7,6

[1] 1–28 V.

[2] at 2 GHz; I_C = 15 mA, V_{CE} = 8 V, T_{amb} = 25 °C.

[3] at 2 GHz; I_C = 15 mA, V_{CE} = 8 V, R_s = 60 Ω, T_{amb} = 25 °C,

[4] at 500 MHz; I_C = 15 mA, V_{CE} = 8 V, T_{amb} = 25 °C.

[5] at 800 MHz; I_C = 14 mA, V_{CE} = 10 V, T_{amb} = 25 °C.

[6] at 800 MHz; I_C = 4 mA, V_{CE} = 10 V, R_s = 60 Ω, T_{amb} = 25 °C.

[7] at 500 MHz; I_C = 14 mA, V_{CE} = 10 V, T_{amb} = 25 °C.

A bandpass filter between the broadband amplifier and the mixer isolates the local oscillator signal from the antenna input, preventing interference to other satellite-tv indoor units. The filter is tuned using two BBY39 varicap diodes, chosen for their extremely low capacitance.

Frequency selection

The local oscillator frequency (1429 MHz to 2229 MHz) is applied to the mixer where it is used to tune the down-converted input signal. The oscillator uses a BFR92A transistor and BBY39 varicap diode. The BFR92A has very low feedback capacitance which prevents oscillations at unwanted frequencies. Another BFR92A transistor is used in the oscillator to buffer it from the mixer, thus isolating strong input signals from the oscillator.
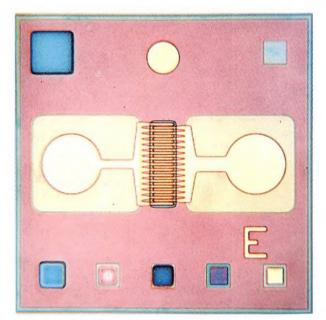
For compatibility with digital tuning systems, a prescaler can be included in the indoor unit. This prescaler converts the local oscillator frequency to a frequency within the range of a CITAC (Computer Interface for Tuning and Control) tuning system (SAB3035/36/37).

Intermediate frequency

The output of the mixer is bandpass-filtered and applied to an i.f. amplifier which provides about 30 dB gain. The i.f. amplifier incorporates a BF990 dual gate MOSFET and a BFR92A transistor. The dual-gate MOSFET makes it easy to incorporate automatic gain control, necessary to prevent the driver of the SAW filter being overloaded by strong input signals. The BFR92A transistor in front of the SAW filter provides good intermodulation performance even at high drive levels.

The selectivity of the tuner is set by the performance of the i.f. filter. A SAW filter with a centre frequency of 479,5 MHz and a 27 MHz passband suppresses adjacent channels.

The broadband amplifier and mixer of the satellite tuner described in the text use one of the most advanced wideband r.f. transistors available — the BFG67. The BGF67 chip (above) has an extra-fine interdigitated electrode structure (2,5 μm base-emitter finger pitch, 0,75 μm emitter-finger width) which minimizes noise and increases gain by minimizing collector/base area. The chip also has an extremely high transition frequency (typically 7,5 GHz) thanks to the use of shallow ion-implanted base and emitter regions and of very thin epitaxial layers (1,2 μm compared with 3 to 4 μm in equivalent devices)

F.M. demodulator

The f.m. demodulator behind the SAW filter has excellent threshold performance (carrier/noise <8 dB) owing to the use of a PLL. Available now for standard tv formats, the demodulator can be modified for future high-definition tv transmissions and multiplied analog component transmissions.

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'ACCORDION' IMAGE SENSOR IMPROVES RESOLUTION

An ingenious departure from the conventional mode of information transfer has made it possible to double the number of light-sensitive elements per unit area in a solid-state image sensor without necessitating a denser surface electrode structure.

In a solid-state image sensor the surface electrodes that govern the formation and transfer of charge packets set a limit to how small each light-sensitive cell can be (Fig.1). Although three electrodes per cell would be sufficient, four are generally used to simplify control and interlacing. In the standard $3,5\,\mu m$ process this results in fairly large cells. Some size reduction can be gained by adopting a three-layer electrode structure, but at the expense of sensitivity, particularly in the blue part of the spectrum.

The newly developed 'accordion' image sensor exploits the fact that only two electrodes per cell are actually needed for collecting the charges. By halving the number of electrodes required this makes it possible to double the number of
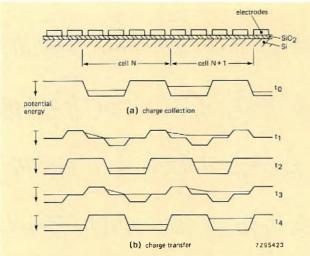
cells that can be formed in a given area. However, four electrodes per cell are still required for transferring the charges. So instead of stepping the image information as a coherent block from the image section to the storage section, it is transferred a line at a time. Starting at the bottom edge of the image section, each charge packet is spread out over the space occupied by two electrodes and separated from its neighbours by potential barriers two electrodes wide (Fig.2). The conventional transfer method can then be used. As they reach the bottom edge of the storage section the charge packets are recompressed so that a line of picture elements again occupies the space beneath two electrodes. Shifting them out a line at a time automatically creates the space required for stretching out subsequent lines of charge packets.

Using the accordion principle and the standard 3,5 mm process it has proved possible to fabricate image sensors with 604×588 light-sensitive elements in an area of $38,2\,mm^2$.

Fig.1 (a) Longitudinal section through one of the light-sensitive channels of a conventional frame-transfer image sensor (EC&A Vol.6 No.4, pp 226-229), showing the four electrodes per cell that govern charge-packet formation and transfer. The channels run from top to bottom of the image and the electrodes are horizontal strips spanning its width. Stop diffusions between channels divide each horizontal line of the image into a row of discrete picture elements. (b) Four-phase variation of the electrode potentials moves the charge packets in step with each other along all the channels at once so that picture information is stepped as a coherent block from the image section of the sensor to the storage section. There, each row of charge packets is read out sequentially during the next scan period to supply the video signal
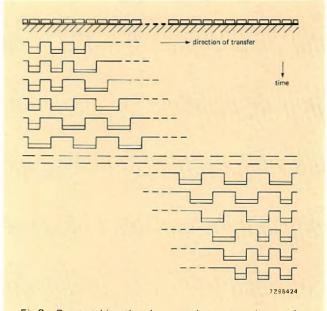

Fig.2 By stretching the charge packets out and squeezing them together again, like the bellows of an accordion, it is possible to transfer them using half as many electrodes. At top left, picture information leaves the image section and enters the storage section. There, charge packets that initially covered two electrodes are stretched out to cover four; the accordion is pulled open and transfer proceeds as in Fig.1. At bottom right, packets reaching the end of the storage section are again lodged under two electrodes: the accordion is squeezed shut
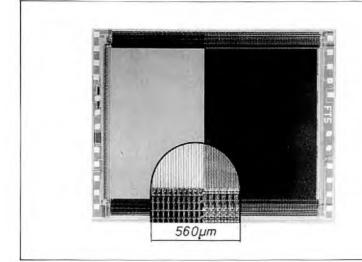
Fig.3 Accordion image sensor, with storage section on the left, image section on the right, control circuitry along the edges. The enlarged inset shows the transition from the image section to the storage section, where charge-packet streching is initiated

MOLECULAR-BEAM EPITAXY LEADS TO IMPORTANT ADVANCES IN SEMICONDUCTOR TECHNOLOGY

The ever-increasing complexity and range of operation of solid-state devices is ultimately based on corresponding developments in growth and processing techniques for semiconductor materials. The most important aspects involved are the control of dimensions, composition and purity of the material, in order to provide the required electrical characteristics. The best known example of this is, of course, to be found in silicon integrated-circuit technology, but similar progress is also occurring with devices fabricated from compound and alloy semiconductors formed from elements of groups III and IV of the periodic table, e.g. gallium arsenide, aluminium gallium arsenide and indium phosphide.

The single crystal starting material for device production is grown from a melt as large ingots, which are then sliced into thin wafers. Gallium arsenide devices, unlike silicon ones, are not in general made directly from these wafers. Instead, the wafers are used as substrates for the growth of very thin single or multiple-layer structures of gallium arsenide or related alloys. The orientation of the layers is determined by that of the substrate, a phenomenon known as epitaxy. Several quite distinct crystal-growth techniques have been developed to realize this. Two of these, known as vapour phase epitaxy (VPE) and liquid phase epitaxy (LPE), have become routine production methods. A third method, just emerging from the research stage, is known as molecular beam epitaxy (MBE). With this technology it is possible to grow layers with a 'thickness' of one atom.

With MBE, molecular beams of the constituent elements (gallium, arsenic, aluminium, phosphorus, indium), produced from effusion cells, impinge upon a heated substrate to produce the required epitaxial layer. The whole operation is carried out in an ultra-high-vacuum system. The growth rate and composition of the layer depend on the beam intensities,

which are in turn determined by the cell temperatures. The beam can also be switched off and on by the use of shutters. The system can be fully automated, with computer control of cell temperature and shutter operation, enabling pre-programming of complex, multi-layer structures. Growth rates are about one atomic layer per second, giving total growth times of a few hours. Since shutter operating times are about 0,1 second, abrupt changes in layer composition are possible, as well as a very accurate control of layer thickness. In this way MBE is well suited to grow structures containing many thin layers with very sharp interfaces (e.g. gallium arsenide/aluminium gallium arsenide).

The Philips programme on MBE started in the Research Laboratories in Redhill (U.K.) in 1970. There are now a number of MBE machines in use, some of them designed and built in the laboratory, the others commercial machines. In addition to the development of growth facilities, the laboratories have established a range of measurement techniques that allow rapid characterisation of the material. One of these is a valuable characterization technique that can be carried out during growth, called RHEED: Reflected High Energy Electron Diffraction. In this technique a beam of electrons with energy in the range 10-50 keV is directed at the crystal surface at extreme grazing incidence. A diffraction pattern is then produced on a fluorescent screen opposite the electron gun. Since the molecular beams are almost normally incident on the substrate, the geometries are quite compatible. The diffraction pattern contains information about the surface of the material and can be related to the topography and surface structure of the growing film. Another important feature of RHEED, which was discovered at PRL, is that it can be used to count individual atomic layers as they are being deposited. This gives a very accurate control of thickness.
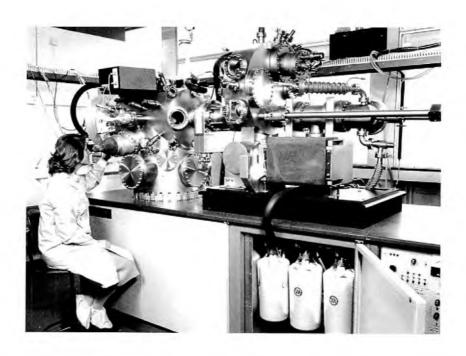
LASERS

With MBE one can make short wavelength semiconductor lasers which have important applications in optical recording and play-back systems. In a solid state laser diode the laser action relies on the existence in a semiconductor of a conduction band with relatively high energy and a valence band with relatively low energy. When a conduction-band electron recombines with a hole in the valence band a photon is emitted. The energy of the photon and hence the wavelength of the light depends on the energy difference between the conduction and the valence band. In a laser diode an excess of electrons is created in the conduction band together with an excess of holes in the valence band. If this excess is large enough, laser action can occur. Lasers emitting in the near infrared at 780 nm and 820 nm are currently used in Compact Disc players. When the active layer thickness is reduced to less than about 50 nm (about 200 atomic layers) effects occur that are not typical of bulk material. The reason for this is that when electrons are confined in a potential well of this width, new energy levels appear above and below the conduction and valence bands in the well. Recombination can now occur between these levels, producing laser emission at shorter wavelength than the normal band-to-band recombination process. Because of the existence of these new quantised states, the structure is known as a 'Quantum Well'; it forms the basis of a new type of solid-state laser device, which may operate in the visible part of the spectrum. The Philips Research Laboratories in Redhill have achieved laser operation at wavelengths as short as 707 nm using wells as thin as 13 nm. This is a significant advance in gallium-arsenide laser operation. It is expected that there will be many applications in optical data processing and display as this wavelength is in the visible range of the spectrum, whereas normal GaAs lasers emit in the infrared.

TWO-DIMENSIONAL ELECTRON GAS STRUCTURES

Electrons move faster in gallium arsenide than in silicon. This higher mobility of electrons in gallium arsenide has already given faster (i.e. higher frequency) electronic devices. Recently a structure has been developed that has the potential of producing even faster devices. It is based on a layer of aluminium gallium arsenide grown on top of high purity gallium arsenide. At the interface between these materials a two-dimensional cloud of electrons is formed in the gallium arsenide. This "electron gas" can have an electron mobility far exceeding that of normal, doped gallium arsenide. Not only have PRL achieve high purity gallium arsenide with a mobility greater than 100 000 cm²/Vsec, at low temperature, but they also have produced two-dimensional structures with low temperature mobilities of 1,5 million cm²/Vsec. This may lead to transistor structures capable of very high frequency operation, (approaching 100 GHz). The requirements for such high mobilities are high purity of the gallium arsenide, good quality interfaces and accurate control of layer thickness down to the atomic level. These can best be achieved with MBE.

Machine for molecular beam epitaxy in operation at Philips Research Laboratories in Redhill (G.B.)

Abstracts

Astable multivibrators using HCMOS ICs

74HC/HCT/HCU high-speed CMOS (HCMOS) logic ICs are ideal for constructing simple yet reliable astable multivibrators in which the operating frequency is determined by a single RC network. This article describes a basic astable circuit using two HCMOS inverting gates or buffers and derives simple formulae for accurately determining its operating frequency. It then develops the formulae to show how adding one resistor makes the operating frequency and duty factor more independent of supply voltage variations and input switching threshold voltage spreads, and limits the input current. The article concludes by discussing the effect of temperature variations, the dynamic power dissipation and the range of external component values and supply voltage that can be used for the circuit.

Crystal oscillators using HCMOS ICs

Crystal-controlled oscillators are widely used in clock pulse generators because of their excellent frequency stability and their wide operating frequency range. If they use a 74HCU high-speed CMOS (HCMOS) IC as the active element, they have the additional advantages of low power dissipation and stable operation over a wide range of supply voltages and temperatures. This article describes the design of several types of crystal-controlled oscillator based on the unbuffered HCMOS Hex Inverter 74HCU04.

Automatic placement machine for hybrid-circuit assembly

Answering the needs of large-scale manufacturers of hybrid circuits, MCM IV is the latest addition to the versatile MCM family of automatic placement machines for SMDs (surface-mounted devices). MCM IV is based largely on concepts pioneered and proved in the MCM II, a machine that combines simultaneous and sequential placement under software control. But unlike MCM II, which is primarily for p.c.b.s, MCM IV is designed specifically to work with standard ceramic substrates.

MOS-XY, interline and frame-transfer sensors compared

There are currently three major image sensors competing in the market: the interline transfer (IL) sensor, the x/y-addressed MOS sensor (MOS-XY) and the frame-transfer (FT) sensor. This article compares these sensors in terms of ease of manufacture, potential for miniaturization and performance. Of the three, the FT sensor seems without doubt the most promising with potentially higher resolution, greater sensitivity and smaller chip area.

Controller IC contends with multiple protocols

Because large amounts of data have to be transferred at high-speed between several local workstations and large computer systems, several message transaction schemes and protocols have evolved, but the development of ICs to handles them has not kept pace. Now, the SCN68562 Dual Universal Synchronous Communications Controller (DUSCC) incorporates virtually all the subsystems and functions required in advanced data communication systems. This article describes the DUSCC's architecture, its capabilities and its application. Since the DUSCC includes so much of the hardware required in communication systems, few additional parts are required, even in the more powerful systems.

Alloy bonding for power semiconductors

The high price of gold is stimulating research into new hard-soldering processes that are less expensive than eutectic bonding but that still meet the electrical performance and quality of the eutectic-bonding technology. This article reviews one of these hard-soldering processes known as alloy bonding that uses a thin-silver-antimony bonding alloy. Tests on alloy bonded devices demonstrate that they could meet the required standards of reliability and electrical performance, and subsequent production experience has amply confirmed expectations.

VMEbus interface ICs for simpler asynchronous systems

A bus controller, an interrupt generator and an interrupt handler have been developed to simplify the design of asynchronous VMEbus systems. The circuits incorporate all control logic for coordinating bus traffic. The bus controller is compatible with 68000-based (or similar) bus masters and can be used in dual-port boards. An error and retry scheme enables the controller to transfer data fast and with minimum user intervention. The interrupt generator can assign up to seven priority levels to interrupts. The interrupt handler can service interrupts received through a distributed multiprocessor system or generated locally.

Manually testing the a.c. characteristics of ECL ICs

The major problem when manually testing the a.c. characteristics of ECL ICs is the difficulty of initially setting up the input waveform and of repeating it at a later date. Unfortunately, digitally-controlled pulse generators that can automatically and accurately repeat waveforms once they've been set up are expensive, and the main factor affecting measurement accuracy and repeatability is the skill of the operator. This article outlines methods for improving the accuracy and repeatibility of measuring the a.c. characteristics by eliminating as many variables as possible from the test set-up.

Indoor unit for satellite-ready tv

To provide full DBS tv reception when it becomes available, future tv sets will require a tuner for the down-converted satellite signal (950 MHz to 1750 MHz) besides the normal u.h.f. and v.h.f. tuner. It's anticipated that the tuner, demodulator and sound and vision processing circuitry for the satellite signal will be in a small indoor unit that can be plugged into a 'satellite-ready' tv receiver, or in the case of top-of-range sets that can be incorporated in the receiver itself. Several components have been developed for the satellite tuner of such an indoor unit and these are introduced in this article. Of particular note is the performance of an advanced wideband r.f. transistor, the BFG67, in the broadband amplifier and mixer of the tuner.

Astabile Multivibratoren arbeiten mit integrierten H-CMOS-Schaltungen

Integrierte Logikschaltungen der High-Speed-CMOS-Reihen 74HC/HCT/HCU (H-MOS) eignen sich hervorragend für den Bau einfacher, aber zuverlässiger astabile Multivibratoren, deren Arbeitsfrequenz durch ein einfaches RC-Netzwerk bestimmt wird. Der Artikel beschreibt eine astabile Bassisschaltung, die mit zwei Inverter-gattern oder Buffern arbeitet, und leitet einfache Formeln zur Berechnung der Arbeitsfrequenz ab. Weitere Formeln zeigen, wie durch Hinzufügen nur eines Widerstands die Arbeitsfrequenz und das Tastverhältnis von Schwankungen der Versorgungsspannung und Streuungen der Eingangsschaltspannung unabhängig werden. Der Artikel schliesst mit der Beschreibung des Einflusses von Temperaturschwankungen der dynamischen Verlustleistung sowie der Dimensionierung externer Bauelemente und Versorgungsspannungen, die für diese Schaltungen geeignet sind.

Quarzoszillatoren, aufgebaut mit Integrierten H-CMOS-Schaltungen

Quarzgesteuerte Oszillatoren werden vielfach wegen ihrer hohen Frequenzstabilität und ihres weiten Arbeitsfrequenzbereichs in Taktgeneratoren eingesetzt. Wenn sie mit der Integrierten High-Speed-CMOS-Schaltung PC74HCU als aktiven Element arbeiten, bieten sie zusätzlich den Vorteil geringer Verlustleistung und stabilen Verhaltens über einen weiten Bereich der Versorgungsspannung und Umgebungstemperatur. Der Artikel beschreibt die Entwicklung mehrerer quarzgesteuerter Oszillatoren, die auf dem umgepufferten Hex-Inverter-Typ 74HCU04 basieren.

Bestückungsautomat für die Herstellung von Hybridschaltungen

Als Reaktion auf den grossen Bedarf an Hybridschaltungen bei Grosserienherstellern wurde die vielseitige und bekannte MCM-Familie der Bestückungsautomaten für SMDs (Surface Mounted Devices) um ein neues System, MCM IV, erweitert. MCM IV basiert weitgehend auf Techniken, die beim System MCM II erstmalig angewendet wurden und die ihre Bewährung in der Praxis bewiesen haben. Dabei wurden simultane und sequentielle Bestückung unter Software-Steuerung miteinander kombiniert. Im Gegensatz zum System MCM II, das vorwiegend für die Bestückung von Leiterplatten geschaffen wurde, ist MCM IV speziell für das Arbeiten mit Standard-Keramiksubstraten ausgelegt.

Vergleich von MOS-X/Y-, Interline- und Frame-Transfer-Sensoren

Zur Zeit stehen hauptsächlich drei Bildaufnehmer auf dem Bauelementenmarkt im Wettbewerb: der Interline-Transfer-Sensor (IL), der X/Y-adressierte MOS-Sensor (MOS-X/Y) und der Frame-Transfer-Sensor (FT). Der Artikel bietet einen Vergleich dieser Sensorarten hinsichtlich der Fertigung, der Miniaturisierungsmöglichkeiten und der Leistungsfähigkeit. Von den dreien erscheint der FT-Sensor am vielversprechendsten zu sein wegen der möglichen höheren Auflösung, grösseren Empfindlichkeit und kleineren Chipfläche.

Controller-IC beherrscht viele Protokolle

Da grosse Datenmengen mit hoher Geschwindigkeit zwischen lokalen Arbeitsstationen (work-stations) und grossen Computersystemen übertragen werden müssen, haben sich verschiedene Verfahren und Protokolle zum Austausch von Botschaften herausgebildet. Die Entwicklung von ICs zur Abwicklung dieses Datenverkehrs hat damit nicht Schritt gehalten. Der neue Zweikanal-Multiprotokoll-Controller SCN 68562 (DUSCC, Dual Universal Synchronous Communications Controller) enthält im wesentlichen alle in fortschrittlichen Datenübertragungssystemen benötigten Subsysteme und Funktionen. Dieser Beitrag beschreibt Architektur, Möglichkeiten und Applikation des Controller-IC. Da die Schaltung SCN 68562 einen sehr grossen Teil der in Kommunikationssystemen benötigten Hardware bereits enthält, werden nur wenige Zusatz-Bauelemente benötigt, selbst in leistungsfähigeren Systemen.

"Alloy Bonding" von Leistungshalbleitern mit Legierungen

Der hohe Goldpreis hat die Entwicklung neuer Lötverfahren gefördert, die trotz niedriger Kosten als beim eutektischen Bonden die elektrischen Anforderungen voll erfüllen, und die nahezu die Qualität des eutektischen Bondens haben. Dieser Aufsatz gibt einen Überblick über eines dieser Lötverfahren (bekannt als Alloy Bond Process), bei dem eine Zinn-Silber-Antimon-Legierung zum Löten verwendet wird. Prüfungen derartig gelöteter Muster zeigen, dass diese den geforderten Normen an Zuverlässigkeiten und elektrischer Funktion entsprechen, und die anschliessenden Produktionserfahrungen haben die Erwartungen vollauf bestätigt.

VME-Bus-Interface-ICs zur Vereinfachung asynchroner Systeme

Um den Entwurf von asynchronen VME-Bus-Systemen zu vereinfachen, sind ein Bus-Controller, ein Interrupt-Generator sowie ein Interrupt-Handler entwickelt worden. Die Schaltungen enthalten die gesamte zur Koordinierung des Bus-Verkehrs erforderliche Steuerlogik. Der Bus-Controller ist mit Bus-Mastern der S 68000-Familie (oder ähnlichen) kompatibel und kann auf Dual-port-Karten verwendet werden. Eine Error-and Retry-Prozedur versetzt den Controller in die Lage, Daten schnell und mit einem Minimum an Eingriffen der CPU zu übertragen. Der Interrupt-Generator kann den Interrupts bis zu sieben Prioritäten zuweisen. Der Interrupt-Handler kann Interrupts bedienen, die er von einem räumlich verteilten Multiprozessorsystem erhalten hat oder die intern erzeugt wurden.

Manuelle Prüfung des AC-Verhaltens von ECL-ICs

Das Hauptproblem bei der manuellen Prüfung des AC-Verhaltens von ECL-ICs besteht in der Schwierigkeit, die zu Anfang bei der Eingabe gewählte Wellenform festzulegen und sie zu einem späteren Zeitpunkt zu reproduzieren. Leider sind digital gesteuerte Pulsgeneratoren, die Wellenformen nach ihrer Festlegung automatisch und genau reproduzieren können, teuer, und die Messgenauigkeit sowie die Reproduzierbarkeit hängen weitgehend von der Geschicklichkeit des Bedieners ab. Der Aufsatz beschreibt Methoden zur Verbesserung der Genauigkeit und Reproduzierbarkeit von Messungen des AC-Verhaltens durch Eliminierung so vieler Einflussgrössen wie möglich aus dem Prüfverfahren.

Innenbaugruppe für satellitenempfangsfertige Fernsehgeräte

Für den FS-Satelliten-Direktempfang (sobald er angeboten wird) benötigen Fernsehgeräte der Zukunft' neben dem üblichen VHF- und UHF-Tuner einen Tuner zur Verarbeitung des herabgesetzten Satelliten-Signals (950 MHz bis 1750 MHz). Wir gehen davon aus, dass der Tuner, der Demodulator sowie die Schaltung für die Ton- und Bildsignalverarbeitung des Satelliten-Signals in einer kleinen Innenbaugruppe untergebracht sind. Diese Innenbaugruppe kann bei Fernsehgeräten, die für FS-Satelliten-Direktempfang vorbereitet sind, eingefügt (gesteckt) werden oder bei Geräten der Spitzenklasse bereits im Fernsehgerät eingebaut sein. Im vorliegenden Artikel werden einige Bauelemente für Tuner von Innenbaugruppen vorgestellt. Einen Schwerpunkt bildet ein leistungsfähiger Breitband-Transistor BFG 67 für den Breitbandverstärker und den Mixer mit Tuner.

Multivibrateurs astables avec des circuits intégrés HCMOS

Les circuits intégrés ultrarapides 74HC/HCT/HCU de logique CMOS (HCMOS) conviennent parfaitement à la construction de multivibrateurs astables simples et fiables, dont la fréquence de fonctionnement est déterminée par un seul réseau RC. Cet article décrit un circuit astable de base utilisant deux portes inverseuses HCMOS et donne des formules simples pour déterminer sa fréquence de fonctionnement avec précision. Le développement de formules montre comment l'addition d'une résistance rend la fréquence de fonctionnement et le coefficient d'utilisation plus indépendants des variations de la tension d'alimentation et de l'étalement de la tension de seuil de commutation d'entrée, et limite le courant d'emtrée. L'article détermine sur l'influence des variations de température, la dissipation d'énergie dynamique et les caractéristiques des composants extérieurs et les tensions d'alimentation des circuits.

Oscillateurs à quartz équipés de circuits intégrés HCMOS

Les oscillateurs pilotés par quartz sont largement utilisés dans les générateurs d'impulsions d'horloge en raison de leur excellente stabilité en fréquence et de l'étendue de leur gamme de fréquence de fonctionnement. Équipés d'un circuit intégré ultrarapide CMOS (HCMOS) 74HCU comme élément actif, ils présentent les avantages supplémentaires d'une faible dissipation d'énergie et d'un fonctionnement stable dans une gamme étendue de tensions d'alimentation et de températures. L'article décrit la conception de plusieurs types d'oscillateurs pilotés par quartz, basés sur le sextuple inverseur HCMOS 74HCU04 non "tamponné"

Machines de positionnement automatique pour l'assemblage des circuits

Répondant aux besoins des gros fabricants de circuits hybrides, la MCM IV est la dernière née de la famille MCM polyvalente de machines de positionnement automatique de CMS (composants pour montage en surface). La MCM IV est basée en grande partie sur le concept mis à l'épreuve sur la MCM II, machine qui combine le positionnement simultané et séquentiel sous contrôle de logiciel. A la différence de la MCM II, qui est destinée essentiellement aux circuits imprimés, la MCM IV est conçue spécifiquement pour opérer sur des substrats céramiques standards.

Les senseurs MOS-XY, interligne et à transfert de trame comparés

Trois principaux types de senseurs d'image se font actuellement concurrence sur le marché. Le senseur à transfert interligne (IL), le senseur MOS à adressage X/Y (MOS-XY) et le senseur à transfert de trame (FT). Cet article compare ces senseurs sous les aspects commodité de fabrication, potentiel de miniaturisation et performances. Il ne fait pas de doute que des trois, le senseur FT est le plus prometteur en raison de sa résolution potentiellement plus élevée, de sa sensibilité plus grande et des dimensions plus petites de la puce.

Un contrôleur de communication capable de traiter de nombreux protocols

Plusieurs systèmes et protocles de transmission de messages ont été élaborés pour pouvoir de transférer de grandes quantités de données à grande vitesse entre plusieurs stations de travail locales et de grands ordinateurs, mais le développement des circuits intégrés nécessaires pour les traiter a pris du retard. Une nouvelle réalization, le Dual Universal Synchronous Communications Controller (DUSCC) SCN68562, intègre pratiquement tous les sous-systèmes et fonctions que nécessitent les systèmes évolués de communication de données. L'article décrit l'architecture du DUSCC, ses possibilités et son emploi. Le DUSCC intégrant une grande partie des fonctions nécessaires aux systèmes de communication modernes, les circuits complémentaires sont peux nombreux même sur les appareils les plus puissants.

Soudure homogène de semi-conducteurs de puissance

Le prix élevé de l'or stimule l'étude de nouveaux procédés par brasure, qui sont moins coûteux que la soudure eutectique tout en rivalisant avec cette technologie pour la qualité et les caractéristiques électriques. Cet article est consacré à l'un de ces procédés de brasure appelé soudure homogène, qui utilise un alliage étain-argent-antimoine. Les tests effectués sur les dispositifs ainsi réalisés, montrent qu'ils satisfont aux normes requises de fiabilités et de caractéristiques électriques, ce qui a été amplement confirmé par les résultats obtenus ultérieurement en production.

Des systèmes asynchrones plus simples grâce à l'interfaçage de circuits intégrés par bus VME

Un contrôleur de bus, un générateur d'interruptions et un circuit de gestion d'interruptions ont été développés pour simplifier la conception de systèmes asynchrones VMEbus. Toute la logique de

commande nécessaire à la coordination du trafic de bus est incorporée aux circuits. Le contrôleur de bus est compatible avec les circuits de contrôle de bus de la famille 68000 (ou similaires) et peut être employé dans des cartes à double accès. Un programme par tâtonnement permet au contrôleur de transférer les données rapidement et avec un minimum d'intervention de l'utilisateur. Le générateur d'interruptions peut définir jusqu'à sept niveaux de priorité. Le circuit de gestion d'interruptions peut traiter les interruptions reçues par l'intermédiaire d'un système multiprocesseur réparti ou généré localement.

Contrôle manuel des caractéristiques en courant alternatif des circuits

Le problème principal soulevé par le contrôle manuel des caractéristiques en courant alternatif des circuits intégrés ECL est la difficulté du réglage de la forme d'ondes d'entrée et de sa répétition ultérieure. Malheureusement, les générateurs d'impulsions à commande numérique capables, une fois réglés, de répéter des formes d'ondes automatiquement et avec précision sont coûteux, et le principal facteur qui détermine l'exactitude et la répétabilité des mesures est l'adresse de l'opérateur. Cet article décrit des méthodes pour améliorer l'exactitude et la répétabilité de la mesure des caractéristiques en courant alternatif, et ceci en éliminent autant de variables que possible du montage de mesure.

Selecteur/démodulateur pour téléviseurs adaptés à la réception des émissions transmises par satellite

Pour assurer la réception des émissions de télévision retransmises par satellite, les téléviseurs de l'avenir devront être équipés, outre du sélecteur UHF et VHF conventionnel, d'un sélecteur pour le signal retransmis par le satellite et dont la fréquence a déjà été réduite par un convertisseur extérieur (950 MHZ à 1750 MHz). On prévoit que le sélecteur, le démodulateur et les circuits de traitement du son et de l'image seront logés dans un petit boîtier que l'on pourra raccorder un téléviseur adapté à la retransmission par satellite, ou qui sera incorporé au récepteur lui-même dans le cas des téléviseurs hauts de gamme. Cet article présente plusieurs composants développés pour le sélecteur incorporé à ce boîtier. L'amplificateur large bande et mélangeur du sélecteur est notamment équipé d'un transistor RF large bande évolué remarquablement performant, le BFG67.

Multivibradores astables con circuitos integrados HCMOS

Los circuitos integrados (HCMOS) de lógicas CMOS de alta velocidad 74HC/HCT/HCU son ideales para la construcción de multivibradores astables sencillos, pero fiables en los que la frecuencia de funcionamiento viene determinada por un solo circuito RC. En el presente artículo se describe un circuito astable básico que emplea dos puertas inversoras HCMOS o memorias intermedias y establece fórmulas sencillas para determinar su exactitud su frecuencia de funcionamiento. Nos da la fórmula para mostrar como la adición de una resistencia hace que la frecuencia, de funcionamiento y el factor de rendimiento sean mas independientes de las variaciones en la tensión de alimentación y de la amplitud de la tensión umbral en la conmutación, y limita la corriente de entrada. El artículo termina con un estudio del efecto de las variaciones de temperatura, la disipación de la energía dinámica y el margen de los valores de componentes externos y tensión de alimentación que pueden utilizarse para el circuito.

Osciladores de cristal con circuitos integrados HCMOS

Por su exelente estabilidad de frecuencia y amplio margen de frecuencias de funcionamiento los osciladores controlados por cristal se utilizan mucho en los generadores de impulsos de reloj. Si se emplea un circuito integrado (HCMOS) CMOS de alta velocidad 74HCU como elemento activo, entonces incorporan las ventajas adicionales de una baja disipación de energía y un funcionamiento estable en un amplio margen de tensiones de alimentación y temperatura. El presente artículo describe el diseño de varios tipos de osciladores controlados por cristal basados en el inversor 74HCU04 Hex HCMOS sin memorias intermedias.

Máquinas de colocación automática para montaje de circuitos Híbridos

Para satisfacer las necesidades de los fabricantes de circuitos híbridos a gran escala, el MCM IV es la última adición hecha a la familia MCM de múltiples aplicaciones de las máquinas de colocación automática para los dispositivos montados superficialmente. El MCM IV se basa ampliamente en conceptos introducidos y probados en el MCM II, una máquina que combina la colocación simultánea y secuencial bajo control 'software'. Pero a diferencia del MCM II, que se ha concebido principalmente para p.c.b.s., el MCM IV se ha diseñado exprofeso para empleo con substratos cerámicos normalizados.

MOS-XY, sensores de interlínea y transferencia de cuadro comparados

Los tres sensores de imagen más importantes que compiten en el mercado son: el sensor de transferencia de interlínea (IL), el sensor MOS direccionado por x/y (MOS-XY) y el sensor de transferencia de cuadro (FT). En este artículo se comparan la sencillez de fabricación, posibilidades de miniaturización y rendimiento de estos sensores. De los tres, el sensor FT es el que sin duda ofrece más perspectivas con una resolución potencialmente más alta, mayor sensibilidad y menor extensión del chip.

El circuito integrado controlador compite con múltiples protocolos

Debido a las grandes cantidades de datos que se transmiten a alta velocidad entre varias estaciones locales y grandes sistemas de ordenador, se han concebido varios esquemas de movimiento de mensajes y protocolos, pero el desarrollo de los circuitos integrados para su manejo no ha evolucionado al unísono. Ahora el doble controlador de comunicaciones sincrónas universales (DUSCC), el SCN68562, incorpora virtualmente todos los subsistemas y funciones necesarios en los modernos sistemas de comunicaciones de datos. En este artículo se describe la arquitectura de los dobles controladores de comunicaciones sincrónos universales, sus capacidades y su aplicación. Por incluir los DUSCC tanto 'hardware' requerido en los sistemas de comunicación, se necesitan pocas piezas adicionales, incluso en los sistemas más potentes.

Conexión aleadora para semiconductores de energía

El elevado precio del oro es un estímulo para la investigación de nuevos procesos de soldadura dura que resulten menos costosos que la unión eutéctica, pero sin perder el rendimiento eléctrico y la calidad que la caracterizan. En el presente artículo se pasa revista a uno de estos procesos de soldadura dura conocido como conexión aleadora que emplea una aleación ligante de estaño-plata-antimonio. Pruebas llevadas a cabo en dispositivos conectadas con esta aleación demuestran que podrían muy bien satisfacer las normas establecidas de fiabilidad y rendimiento eléctrico, y una posterior experiencia de producción tiene perspectivas ampliamente confirmadas.

Circuitos integrados de conexión en la barra colectora VME para sistemas asíncronos más sencillos

Para simplificar el diseño de sistemas asíncronos de barra colectora VME se han concebido un controlador de barra colectora, un generador de interrupciones y un transportador de interrupciones. Los circuitos incorporan toda la lógica de control para coordinar el tráfico de la barra colectora. El controlador de la barra colectora es compatible con barras colectoras maestras basadas en 68000 (o similares) y puede utilizarse en placas de doble puerta. Un esquema de errores y de reintento permite al controlador transferir los datos con rapidez y con un mínimo de intervención por parte del usuario. El generador de interrupciones puede asignarle hasta siete niveles de prioridades. El transportador puede dar servicio a las interrupciones recibidas a través de un sistema multiprocesador distribuido o generado localmente.

Comprobación manual de las características de c.a. de circuitos integrados ECL

El mayor problema que se presenta cuando se comprueban a mano las características de c.a. de los circuitos integrados ECL es la dificultad de ajustar desde el principio la forma de onda de entrada y de repetirla en fecha posterior. Lamentablemente, los generadores de impulso controlados digitalmente, capaces de repetir las formas de onda de modo automático y exacto una vez ajustadas son caros; el principal factor que influye en la exactitud de mediciones y en la repetibilidad es la pericia del operador. El presente artículo expone a grandes rasgos los métodos para mejorar la exactitud y repetibilidad en la medición de las características c.a. eliminando el mayor número posible de variables del ajuste de prueba.

Unidad interior para televisores aptos para recibir la señal procedente de satélites

Para posibilitar al máximo la recepción de la señal de tv DBS cuando se disponga de ella, los futuros televisores necesitarán un sintonizador para la señal de satélite convertida hacia abajo (de 950 MHz a 1750 MHz), además del sintonizador normal de u.h.f. y v.h.f. Se sabe de antemano que el sintonizador, el demodulador y los circuitos procesadores de sonido y visión para la señal de satélite se alojarán en una pequeña unidad interior enchufable a un televisor apto para recibir la señal de un satélite y en los aparatos más caros de la gama, incorporada en el propio receptor. Varios han sido los componentes diseñados para el sintonizador de satélite, por ejemplo una unidad interna, de los que nos ocupamos en este artículo. De particular importancia es el rendimiento de un moderno transistor de radiofrecuencia de banda ancha, el BFG67, en el emplificador de banda ancha y mezclador del sintonizador.

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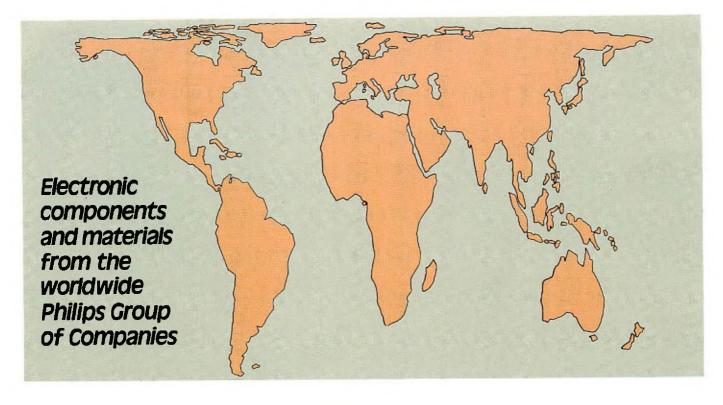Microwave devices
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