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Erected as a radio broadcasting tower in 1924 and now serving television as well, the Funkturm in Berlin marks the site of the biennial Funkausstellung at which manufacturers from all over the world display the latest in television, radio, and audio products. Digital control and, in particular, the use of microcomputers in both radio and television tuning systems as described in three articles in this issue of E.C. and A., are amongst the themes of this year's Funkausstellung.

Microcomputer-controlled tuning and control systems for TV

F. A. M. VAN DE KERKHOF

Since the introduction of voltage-controlled tuners, a wide variety of electronic tuning systems have been developed for television receivers. LSI technology has allowed digital control to be applied to the tuner and the analogue receiver functions at a price comparable with that of former electromechanical systems using variable capacitors and potentiometers.

Closed-loop digital systems provide accurate, drift-free tuning and incorporate easily programmed station memories. They can also provide on-screen and LED display of channel and station numbers, control of the analogue functions of the receiver and remote control facilities. These systems, however, although effective, are inflexible because they use a series of dedicated LSI circuits to perform a fixed set of control functions. Since the dedicated ICs must perform all the functions necessary to meet the requirements of different customers and markets, they tend to be costly and, in some systems, partially redundant.

The decreasing cost of microcomputers has led us to re-examine our concept of digital tuning and control of television receivers, and to develop a series of microcomputer-controlled integrated circuits to form a versatile modular Video Tuning System (VTS).

The heart of the VTS is an accurate and stable frequency-locked digital tuning loop (Fig.1) which is based on the same principles as the well proved DICS system (Ref.1). The digital code defining the required frequency is derived from a keyboard-addressed microcomputer and passed to the tuning loop via a 3-wire computer bus (CBUS). The basic tuning system can be extended to perform more control and display functions by simply connecting more ICs from the VTS series to the CBUS.

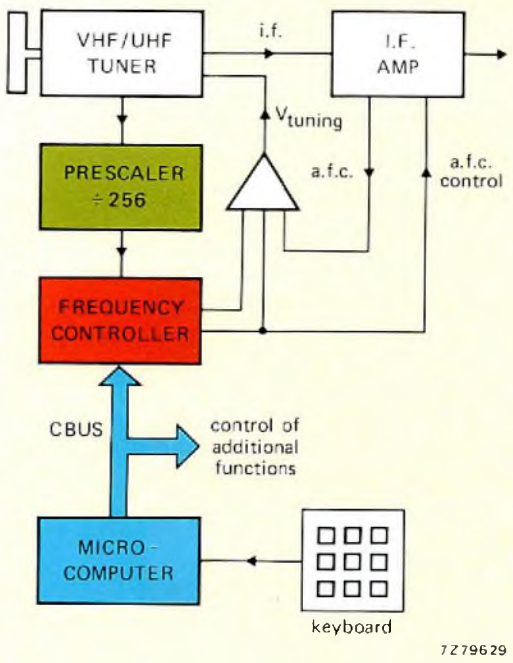

Fig.1 Basic microcomputer-controlled frequency-locked digital tuning loop for television receivers

In addition to direct access to TV channels, the VTS can also provide:

- programmable station memory (non-volatile RAM; i.e. CMOS memory with battery back-up or MNOS memory)
- stepping through channels or stations
- fine detuning with storage of detuning information
- search tuning
- 64-increment control of up to six analogue functions such as brightness, contrast, saturation, volume, tone and detuning
- display of analogue function settings
- LED display of station or channel numbers
- on-screen display of station and channel numbers
- muting
- infrared remote control
- control of teletext and viewdata circuits.
- timer and clock functions with LED and/or on-screen display.

The advantages of microcomputer-controlled systems over their dedicated LSI predecessors are:

- System development time is shorter.
- System flexibility simplifies design changes and updating.
- System is compatible with microcomputers from many sources.
- The most economic microcomputer can be selected to suit the complexity of the envisaged control system.
- Serial data on 3-wire CBUS only uses three ports of the microcomputer and the peripheral ICs. This results in compact layout and simple single-sided printed-wiring structure.
- The same remote control unit can be used to operate radio, audio and television equipment.

SURVEY OF THE INTEGRATED CIRCUITS OF THE VTS

Microcomputers

8021 For low-cost basic tuning systems.

8048 For medium-price receivers requiring a few functions in addition to the basic tuning facility.

8049 For top-class receivers incorporating teletext, viewdata, clock, timer, etc.

Tuner interface

SAB1009B A 70 MHz to 900 MHz wideband preamplifier for increasing the amplitude of the local-oscillator signal from the tuner to a level compatible with the SAB1046.

SAB1046 Prescaler for dividing the frequency of the tuner oscillator signal by 256 before it is applied to the frequency controller.

(The SAB1018, to be introduced later, will combine the functions of the SAB1009B and SAB1046.)

Frequency controllers

SAB3024 Computer Interfaced Tuning System (CITUS) which provides frequency-locked-loop digital tuning.

SAB3034 Analogue and Tuning circuit (A & T) which provides frequency-locked-loop digital tuning and 64-increment digital control of up to six analogue functions.

Analogue function control

SAB3013 Computer Controlled Analogue Memory (CCAM) which provides 64-increment digital control of up to six analogue functions.

Display controllers

SAA1060 Display/interface circuit for LEDs (DIFA-LED). Provides control of 16 LED segments with static drive or of 32 segments with dynamic (duplex) drive.

SAA1061 Output Port Expander (OPEX). Provides control of 16 LED segments with static drive.

SAB3016 Character On-screen Interface (COSI). Provides on-screen display of station and/or channel number or time of day. The display consists of two numerals, four numerals or two pairs of numerals separated by a colon. The numerals are displayed in 7-segment format on a rectangular background.

A Video Display Generator still in development will allow alphanumeric or graphical display to users' requirements: e.g. station lists, switching times, individual graphs and texts.

Remote control

SAB3011 Remote transmitter. Encodes keyboard entries and transmits the commands via infrared LEDs to the infrared receiver.

TDB1033 Infrared receiver. Provides differential amplification, pulse shaping and level control of signals received from the infrared transmitter via a photodiode.

SAB3042 Infrared Decoder (IDEC). Can be used to simplify the task of the microcomputer by demodulating and checking the validity of the commands from the infrared receiver. Can also accept five inputs matrixed to allow up to 31 commands to be issued from a local keyboard. In addition to a 3-wire bidirectional bus for connection to a microcomputer, the circuit also has IBUS outputs for controlling videotex systems, e.g. teletext and viewdata.

Timer/clock

A microcomputer-controlled timer/clock/calendar circuit is being developed.

TYPICAL APPLICATIONS

The basic VTS

Figure 2 shows a simple low-cost VTS based on an 8021 microcomputer and suitable for incorporation in simple television receivers such as those without a.f.c. circuits. The basic system performs the following functions:

- direct access to all CCIR channels by entering two digits on the local keyboard
- sequential stepping through the channels
- search tuning
- LED display of channel number

No a.f.c. is required. The system can be extended as follows:

- Remote control can be added by using the infrared transmitter SAB3011 and receiver TDB1033; the latter can be connected directly to the microcomputer.
- The computer-controlled analogue memory SAB3013 can be added to provide fine detuning, control of five analogue functions (e.g. volume, tone, brightness, contrast, and saturation), muting, and setting of all the analogue levels to mid-value at switch-on. If the receiver does have a.f.c., it is possible to reduce the cost of the system by using the SAB3034, which performs the dual functions of tuning and analogue control, instead of the SAB3024 and SAB3013.
- A non-volatile memory (MNOS or CMOS with battery back-up) can be added to provide preset station facilities and analogue levels set to user-selected values at switch-on.

A VTS for medium-price receivers

Figure 3 shows a more complex remotely controlled VTS based on an 8048 microcomputer and capable of performing the following functions.

- direct access to all CCIR channels
- presetting 20 or more stations (dependent on memory capacity)
- sequential stepping through the channels or stations
- search tuning
- selection of channels and stations by decimal key entry
- local and remote control
- fine detuning with storage of detuning information
- control of five other analogue functions with muting
- setting analogue levels to user-selected values at switch-on
- on-screen display of station and channel number.

The system can be extended as follows:

- Addition of SAB3042 simplifies the task of the microcomputer and allows straightforward interfacing with videotex circuits.
- The output expander SAA1061 can be used to provide a LED display instead of, or in addition to, the SAB3016 for on-screen display.
- The frequency and analogue function controller SAB3034 can be replaced with the frequency controller SAB3024 and the analogue function controller SAB3013. The system could then be used in television receivers without a.f.c.

Comprehensive VTS

Figure 4 shows a comprehensive VTS based on an 8049 microcomputer and intended for incorporation in top-class television receivers. The system includes all the facilities provided by the system shown in Fig.3 with the following additions:

- timer/clock circuit
- on-screen display of station/channel number or time of day.
- LED display of station/channel number or time of day.

If videotex is not required, a circuit for character and graphic displays could be added. A video display IC for this purpose is being developed.

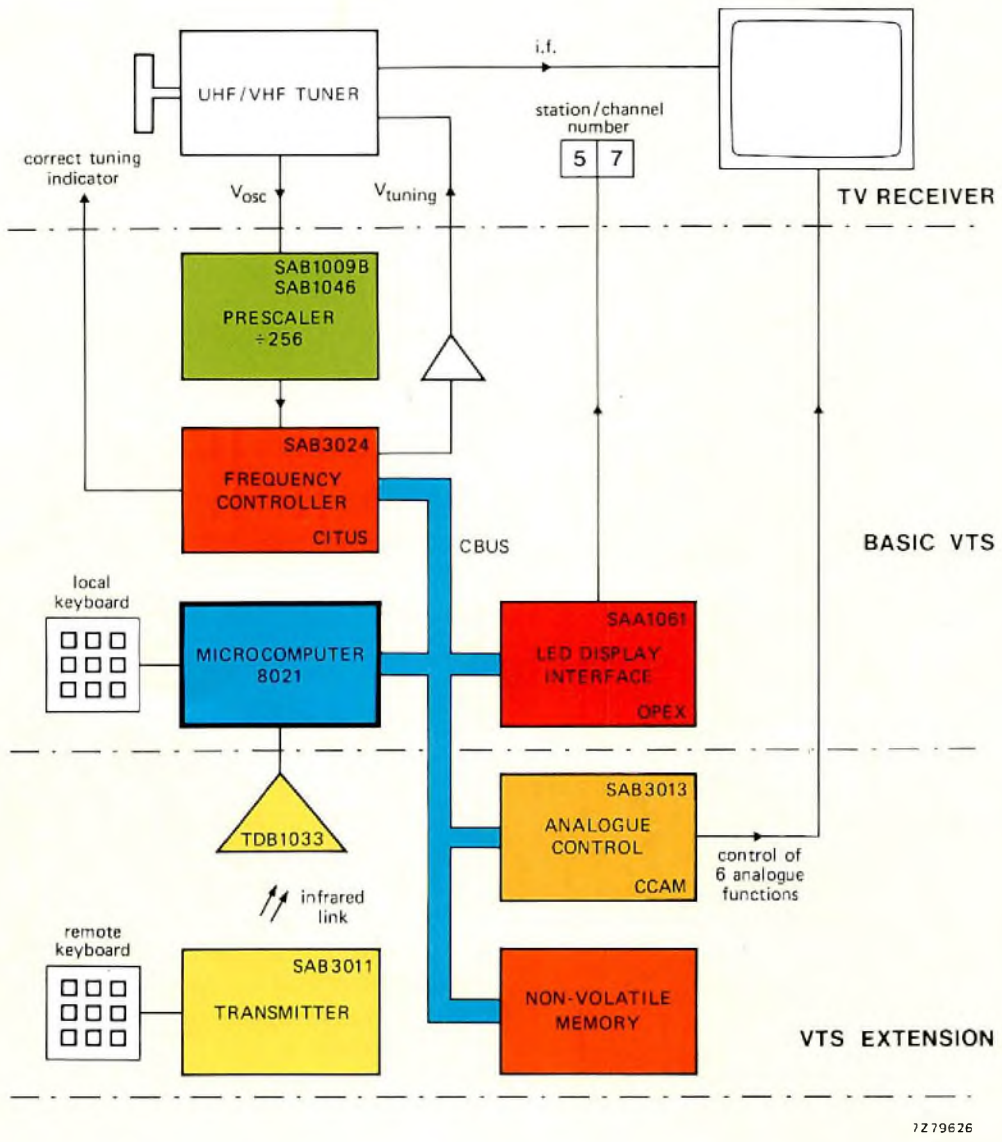

Fig.2 Basic VTS system with extension for station memory, analogue function control and remote control

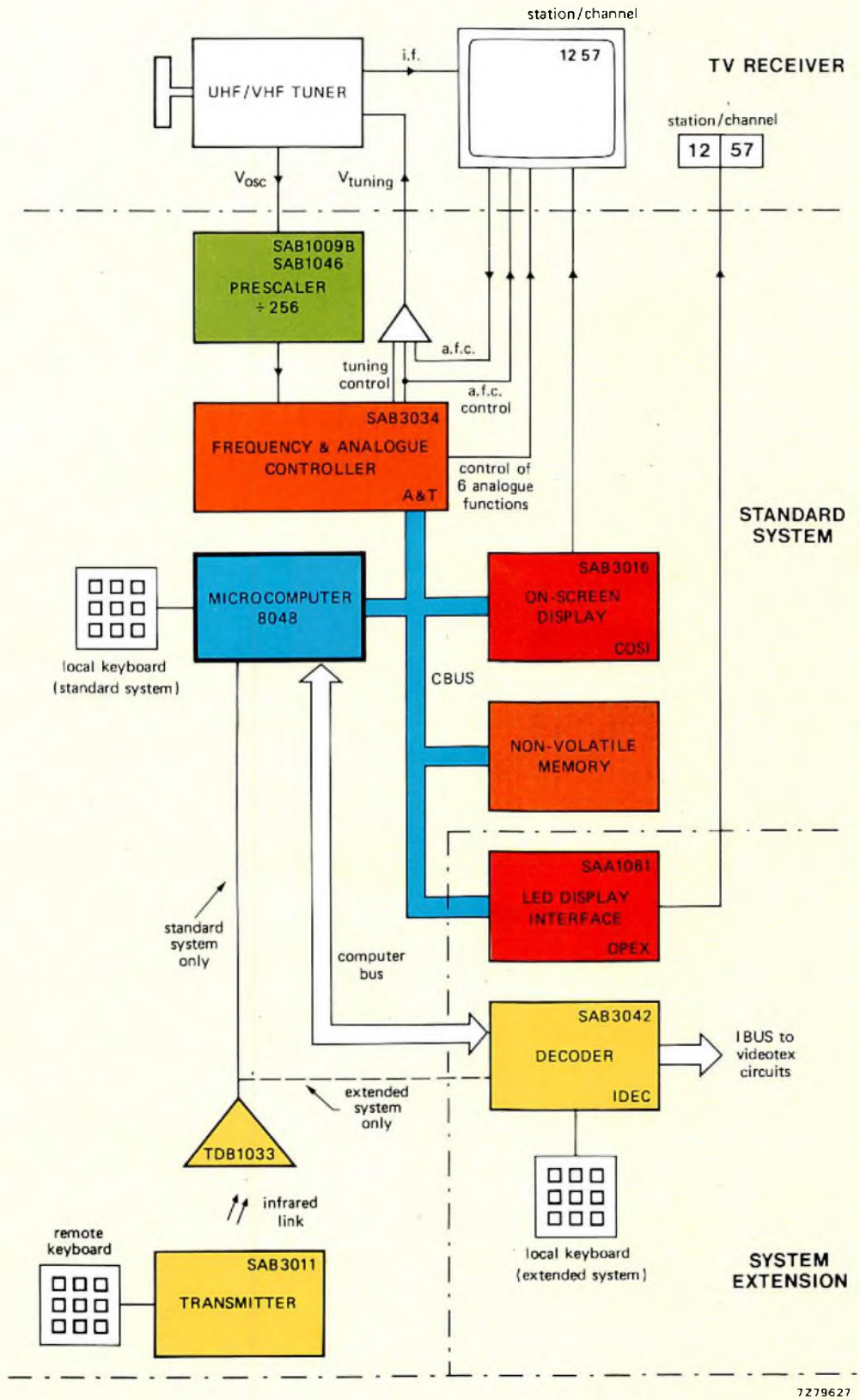

Fig.3 VTS system for medium-price receivers

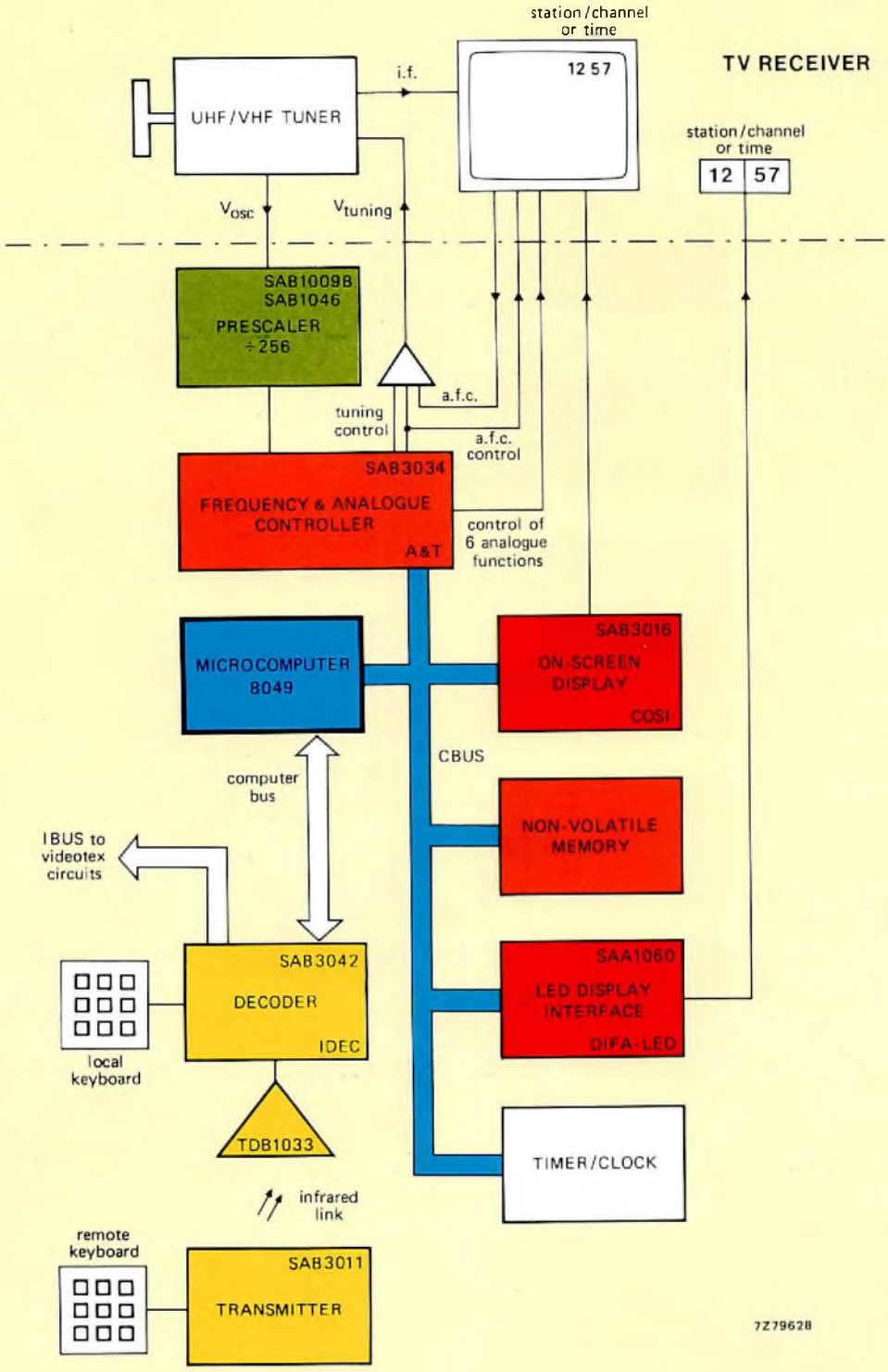

Fig.4 Comprehensive VTS system

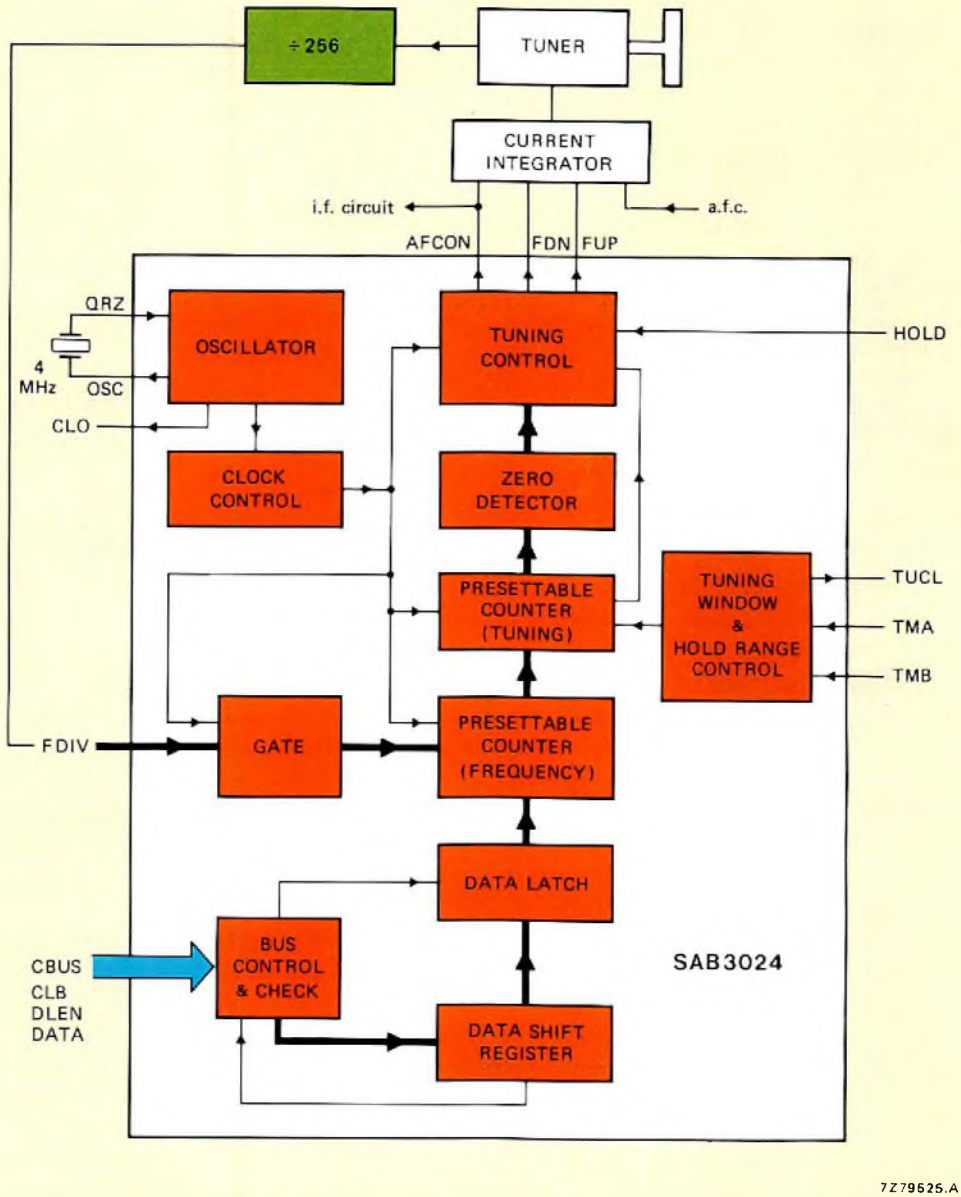

Fig.5 Frequency-locked digital tuning loop using CITUS circuit SAB3024

BRIEF DESCRIPTION OF VTS INTEGRATED CIRCUITS

Digital tuning with the SAB3024

The SAB3024 accepts commands from the microcomputer via the CBUS and performs the functions associated with frequency-locked-loop digital tuning. Figure 5 is a block diagram of the tuning control.

Receiver tuning data is transmitted from the microcomputer, via the CBUS, as 18-bit words which are loaded into the data shift register. Shortly after the end of each word, the data, if valid, is loaded into the data latch.

The 14 most significant bits of the data word define the required frequency and are loaded into the frequency counter. The cycles of the tuner local-oscillator waveform (divided by 256) at the FDIV input then decrement the frequency counter during a 4096 μs measuring period. The contents of the frequency counter at the end of this period define the tuning error as follows:

- counter has passed zero, frequency too high;
- counter has not reached zero, frequency too low;
- counter contents zero, frequency correct.

The remaining contents of the frequency counter are loaded into the tuning counter which is decremented to zero by clock pulses. The period during which the tuning counter runs is therefore proportional to the extent of the necessary frequency correction. The tuning control, in conjunction with an external circuit, generates FUP (increase frequency) or FDN (decrease frequency) pulses with a duration equal to the running time of the tuning counter. If the counter content was zero, neither FUP nor FDN pulses are generated but the AFCON output is set HIGH to switch on the receiver a.f.c., thereby allowing the tuning operation to be completed.

Since the frequency is measured by a 14-bit counter, the maximum tuning error is $f/2^{14}$. With an upper frequency limit of 1024 MHz, this results in a maximum tuning error of 62.5 kHz. This tuning window is narrow enough to allow the system to be used in TV receivers that do not incorporate a.f.c. The AFCON output can then be used to control a correct-tuning indicator. If a.f.c. is used, it will remain switched on by the AFCON signal as long as the tuning remains within a holding range of $\pm$62.5 kHz. Inputs TMA and TMB can also be addressed to give tuning windows of 250 kHz, 500 kHz or 1 MHz and corresponding holding ranges of 500 kHz, 1 MHz or 2 MHz by reducing the length of the frequency counter to 12, 11 or 10 bits.

The third and fourth bits of the data word define the rate at which the tuning counter is decremented and thereby control the duration of the FDN and FUP frequency correction pulses. Four durations can be selected for each tuning window width so that the characteristics of various tuners can be accomodated.

The first and second bits of the data word can be used to reverse the tuning direction information applied to the tuning control. This facility is included because, if the tuner local oscillator ceases to function, the divide-by-256 prescaler may oscillate at high frequency. In this event, the tuning loop will sense that the measured frequency is too high and will be unable to tune up. To overcome this condition, the FDN pulses must be changed to FUP pulses.

A HIGH level at the HOLD input will inhibit the tuning pulses and cause the AFCON output state to remain unchanged.

Digital tuning and analogue function control with the SAB3034

The SAB3034 performs frequency-locked-loop digital tuning and also provides digital control of up to six analogue functions. A block diagram of the system is given in Fig.6.

The digital tuning function is similar to that previously described for the SAB3024 except that the CBUS data comprises sixteen words containing up to 12 bits. Seven of the data words define the tuning window, the holding range, a frequency offset, the tuning speed, and the clock oscillator frequency. The clock frequency of 400 kHz may be derived from some microcomputers (e.g. the 8048) or may be generated from a 4 MHz crystal-controlled oscillator in the IC.

Eight of the data words control the level at the six analogue outputs and define whether they are enabled or disabled. The final data word defines the required tuning frequency in 10 bits.

The 12-bit frequency counter has an accuracy of 1024 MHz/2^{12} = 250 kHz, which is within the catching range of a.f.c. circuits. Frequencies up to 2^{10} MHz = 1024 MHz can be specified in increments of 1 MHz by the 10-bit frequency data word. The 2-bit offset frequency data word can be used to specify the last MHz of the required frequency in increments of 1 MHz/2^2 = 250 kHz.

The first six of the eight analogue function data words set the required values (0 to 64) into the six 6-bit analogue registers. The contents of the registers are converted into pulse-width modulated outputs with a frequency of 6.25 kHz and a duty factor proportional to the analogue value, as shown in Fig.7. External RC filters smooth the analogue outputs to obtain d.c. control voltages for the ICs in the television receiver. The remaining two analogue function data words simultaneously enable or disable all of the analogue outputs.

An internal power-on reset circuit sets all the analogue outputs to zero when power is first applied to the IC.

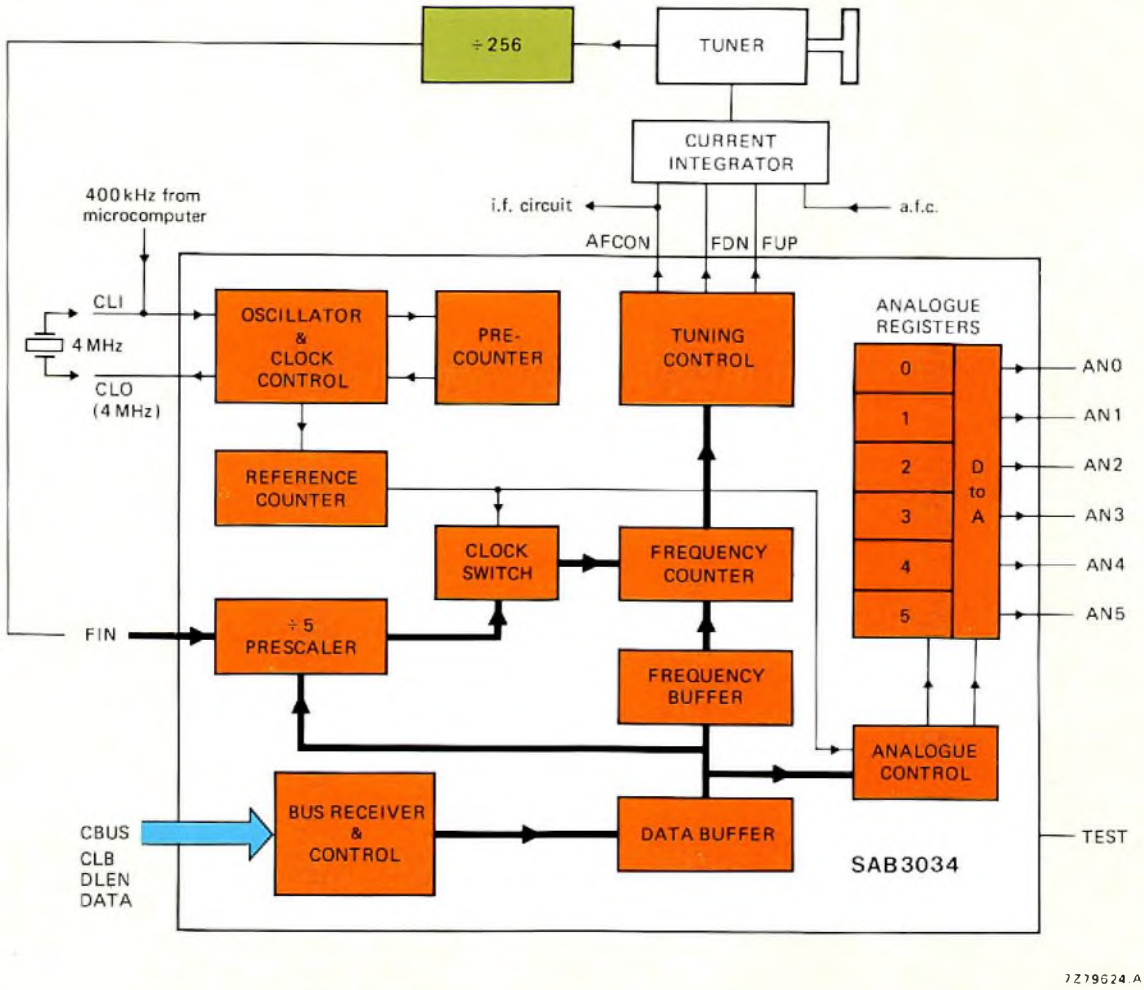

Fig.6 Frequency-locked digital tuning loop using A & T circuit SAB3034

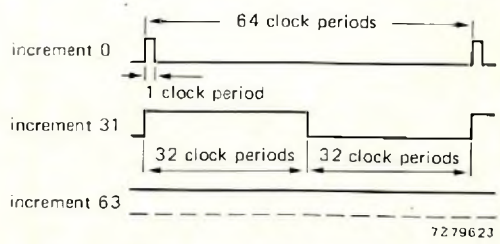

Fig.7 Pulse-width modulated analogue outputs from the SAB3034

Analogue function control with the SAB3013

The SAB3013 provides 64-increment digital control of up to six analogue functions. A block diagram of the circuit is given in Fig.8.

The circuit is controlled by six 11-bit data words, each preceded by a leading zero. The data is derived from the microcomputer via the CBUS. The two least significant bits of each word are coded to correspond with the system address code on inputs SAA and SAB. This allows up to four SAB3013 circuits to be used in a system. The next three bits of the data word are the address for the appropriate analogue latch. The six most significant bits of the data word are binary coded to represent the required increment (0 to 63) for the selected analogue function.

The data received from the CBUS is loaded into the data buffer. If the leading zero was LOW, DLEN is LOW (data complete), and twelve bits have been received, the data is transferred to the data latch on the trailing edge of the next clock pulse on CLB. Whilst the latch is being loaded, output BUSY becomes LOW to indicate that new data can be accepted from the CBUS.

The contents of the latches are converted into pulse-width modulated outputs with a cycle time of 64 clock periods and a duty factor proportional to the analogue value as shown in Fig.7. External RC filters smooth the analogue outputs to obtain d.c. control voltages for the ICs in the television receiver.

The circuit can be used with the internal 30 kHz to 1 MHz oscillator or with externally-generated clock pulses within the same frequency range.

An internal power-on reset circuit sets all analogue outputs to a duty factor of 0.5 (mid-value) when power is first applied to the IC.

LED displays with the SAA1060

The SAA1060 accepts serial data from the microcomputer via the CBUS and converts it into parallel data for directly driving 16 LEDs for bar-graph displays or 16 segments of LED numeral displays. For numeral displays the data input must be seven-segment decoded by the microcomputer. A facility is provided whereby the outputs can be time-division multiplexed so that 32 LED

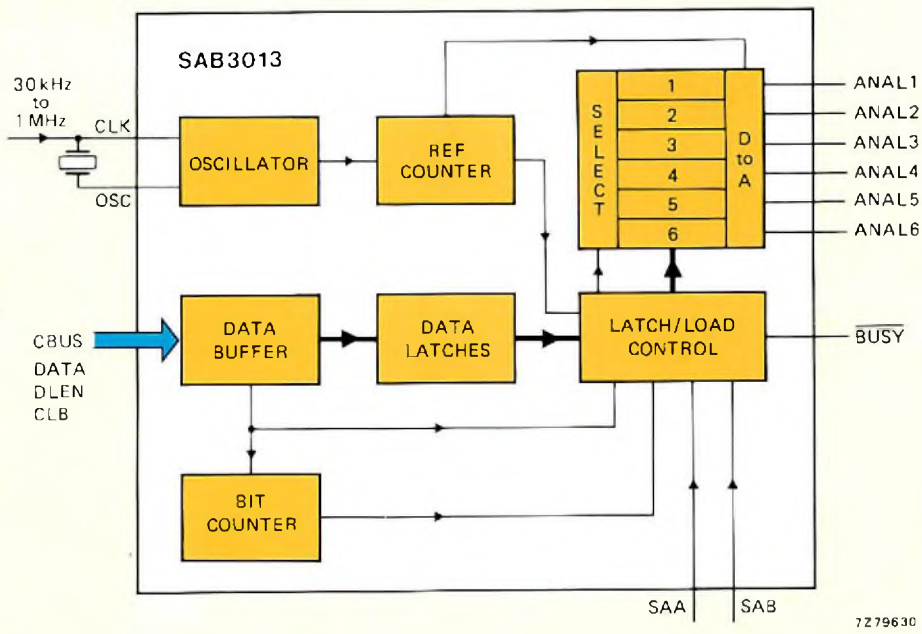

Fig.8 Computer-controlled analogue memory SAB3013

segments can be driven. A block diagram of the circuit is given in Fig.9.

Display data is transmitted from the microcomputer, via the CBUS, as 18-bit words comprising a leading zero, 16 bits of data and a register selection bit. The bus control stage checks the presence of the leading zero with DLEN HIGH during the first clock pulse. A check is also made to prevent data being accepted if there is interference on the CBUS. The shift register is then reset before the 17-bit data word is written in. The reset state of the first bit in the register is shifted into the last bit position. Correct length of the data word is then verified by checking the value of the last bit in the register. If the data is accepted, the bus control stage generates a 'valid' pulse which causes the load control stage to transfer the contents of the shift register to one of the data latches on the 19th clock pulse. Which latch is selected depends on the level of the load bit of the data word (bit 17): a HIGH level selects latch A, a LOW level selects latch B.

The state of the latches determines the state of the open-collector n-p-n output transistors in such a way that the display is blanked by HIGH data bits. Outputs Q_8 and Q_{16} are capable of sinking a maximum current of 80 mA. All the other outputs can sink a maximum of 40 mA.

Input LOEX determines whether the output data is derived directly from the selected latch (16 numeral segments in static mode), or whether the output data is derived alternately from the two latches in synchronism with transitions at the DUP input (32 numeral segments in duplex mode). When input LOEX is HIGH, the static mode is selected. When input LOEX is LOW, the duplex mode is selected.

When operating the circuit in the duplex mode, the contents of latch A are presented at the outputs when DUP is LOW; the contents of latch B are presented at the outputs when DUP is HIGH. If the DUP signal is derived from a 50 Hz mains supply, the interval between each data word must be at least 21 ms. During duplex operation with a sinusoidal display drive voltage, the current sinking capability of the outputs is 120 mA peak for outputs Q_8 and Q_{16}, and 60 mA peak for all other outputs.

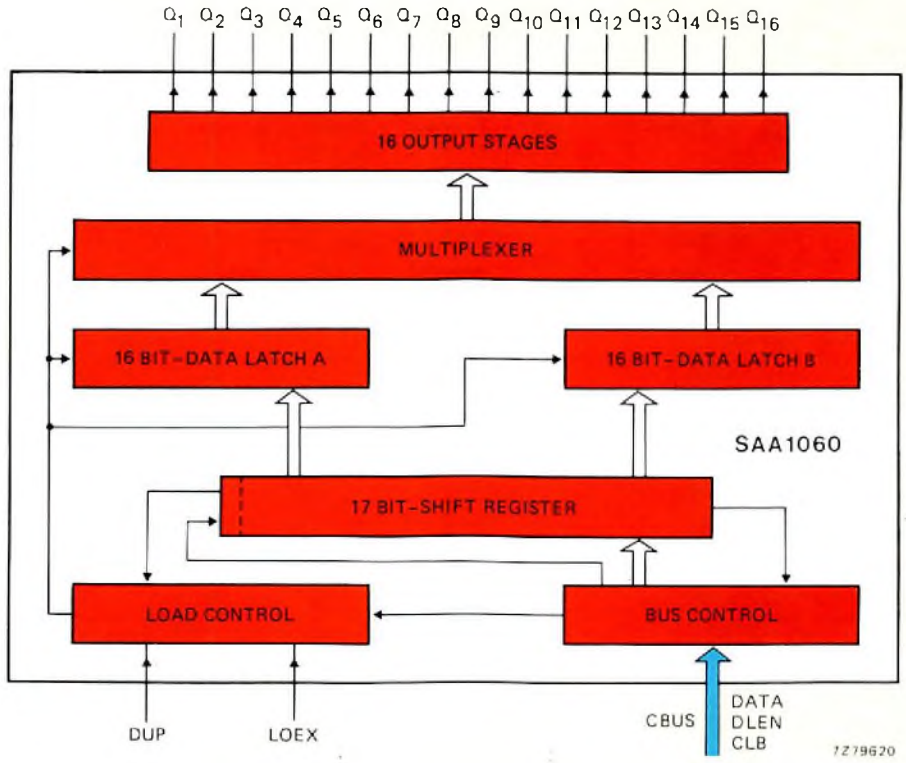

Fig.9 LED display/interface circuit SAA1060

LED display with the SAA1061 (OPEX)

The SAA1061 Output Expander (OPEX) functions in a similar manner to the previously described SAA1060 except that it can drive only 16 LED segments in static mode and the current sinking capability of the outputs is 15 mA per segment.

On-screen display with the SAB3016

The SAB3016 provides display of station/channel number or time of day at the top of a TV screen. The display consists of one or two blocks of two numerals, each block arranged within a rectangular background. One pair of numerals is used to display channel or station number; two pairs of numerals are used to display channel and station number; two pairs of numerals, separated by a colon, are used to display time of day. A block diagram of the circuit is given in Fig.10.

Display data, which is also compatible with the off-screen display circuits of the VTS, is transmitted from the microcomputer via the CBUS as a 17-bit word preceded by a leading zero. The first seven bits define the state of the seven segments of the left-hand numeral. Bits 9 to 15 define the state of the seven segments of the right-hand numeral. Bits 8 and 16 determine whether the numerals will be permanently displayed, flashing at 640 ms intervals or displayed for a period determined by an R-C network connected to the DISPL input of the circuit. Bit 17 indicates whether the transmitted data applies to the left-hand or right-hand pair of numerals. The state of input DOT determines whether or not two pairs of numerals will be separated by a colon.

The display format is shown in Fig.11. The width of the display (duration of blanking pulse IVID) is determined by the state of the MODE input (two numerals or four numerals) and by the 2.5 MHz crystal-controlled clock generator period $T = 400$ ns ($17T = 6{,}8\ \mu s$ for one pair of numerals; $34T = 14.6\ \mu s$ for two pairs of numerals)

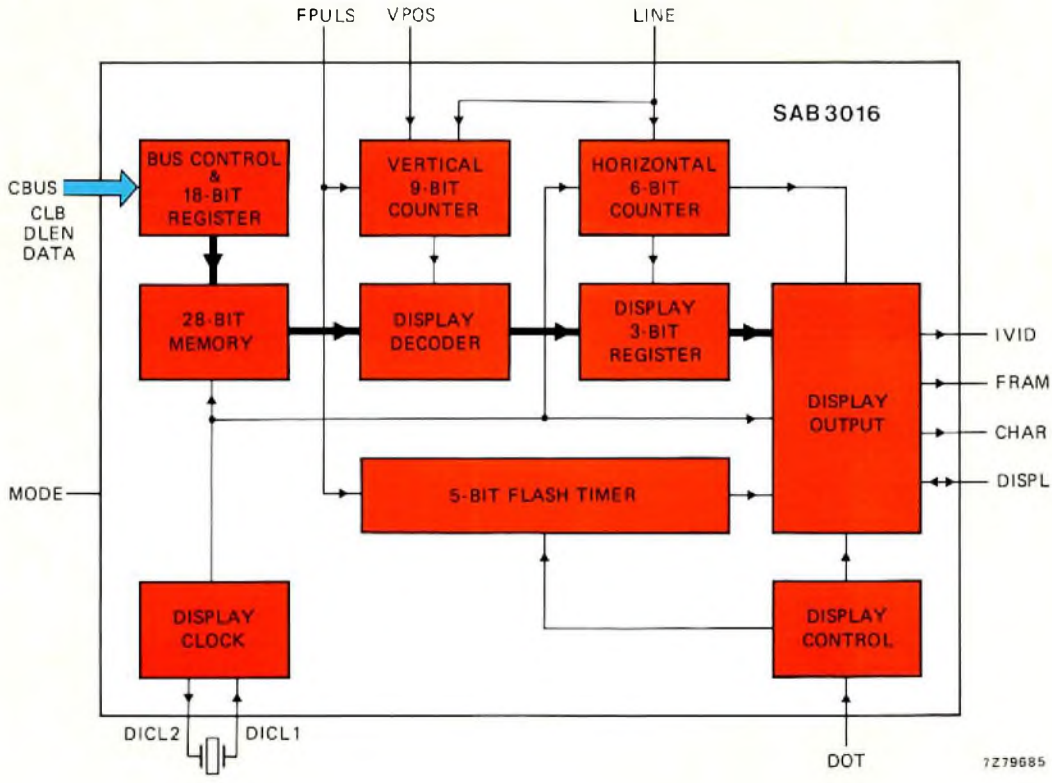

Fig.10 On-screen display circuit SAB3016

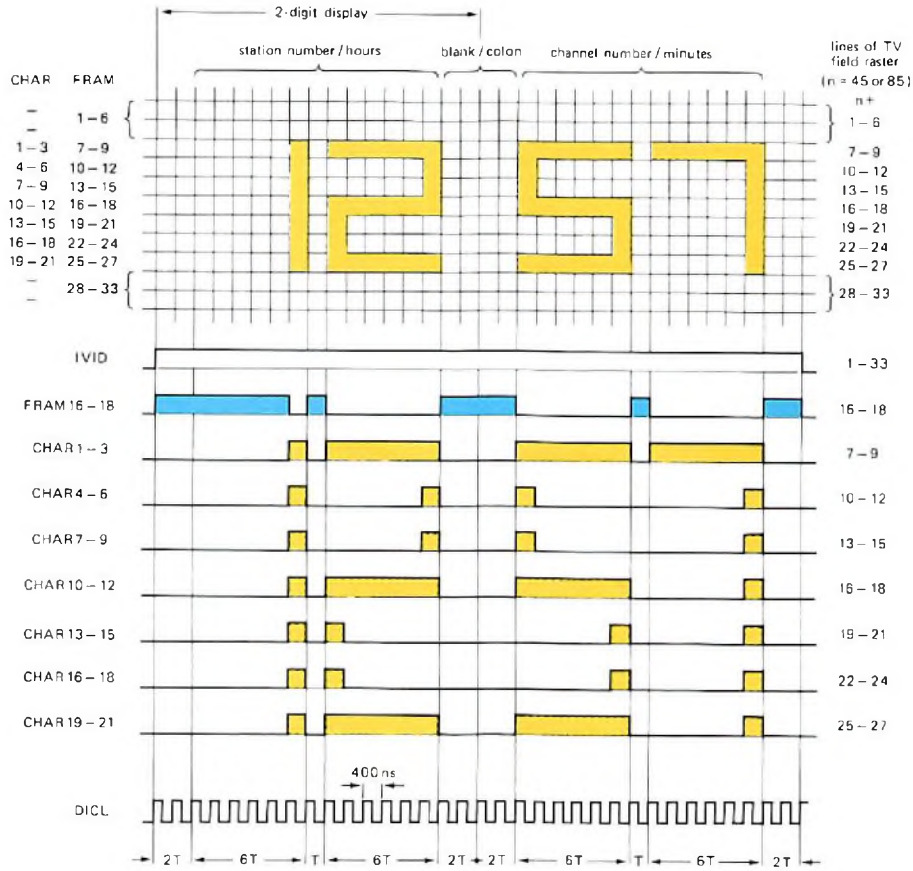

Fig.11 Display data from the SAB3016. The character rounding bits are omitted for clarity

compared with the time taken to scan the visible portion of a TV line (≈48 μs for a 625-line system). The vertical position of the top of the display is set to line 45 or line 85 by the state of input VPOS. The colour of the background block is controlled by output FRAM. The colour of the numerals is controlled by output CHAR. The display is synchronised with the television receiver scanning circuits by vertical and horizontal sync pulses applied to inputs VPULS and LINE. Typical displays are shown in Fig.12.

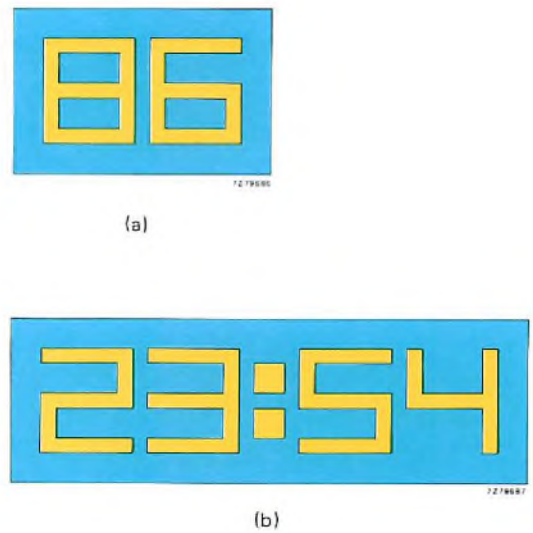

Fig.12 Typical on-screen displays with the SAB3016. (a) 2-digit channel number display. (b) 4-digits with colon for displaying time.

Basic remote control with SAB3011 and TDB1033

The SAB3011 is the infrared transmitter IC of the VTS. Since it must be battery-powered, CMOS technology is used to minimise power consumption. For the same reason, the circuit is made to assume a stand-by state when commands are not being transmitted. If a key-

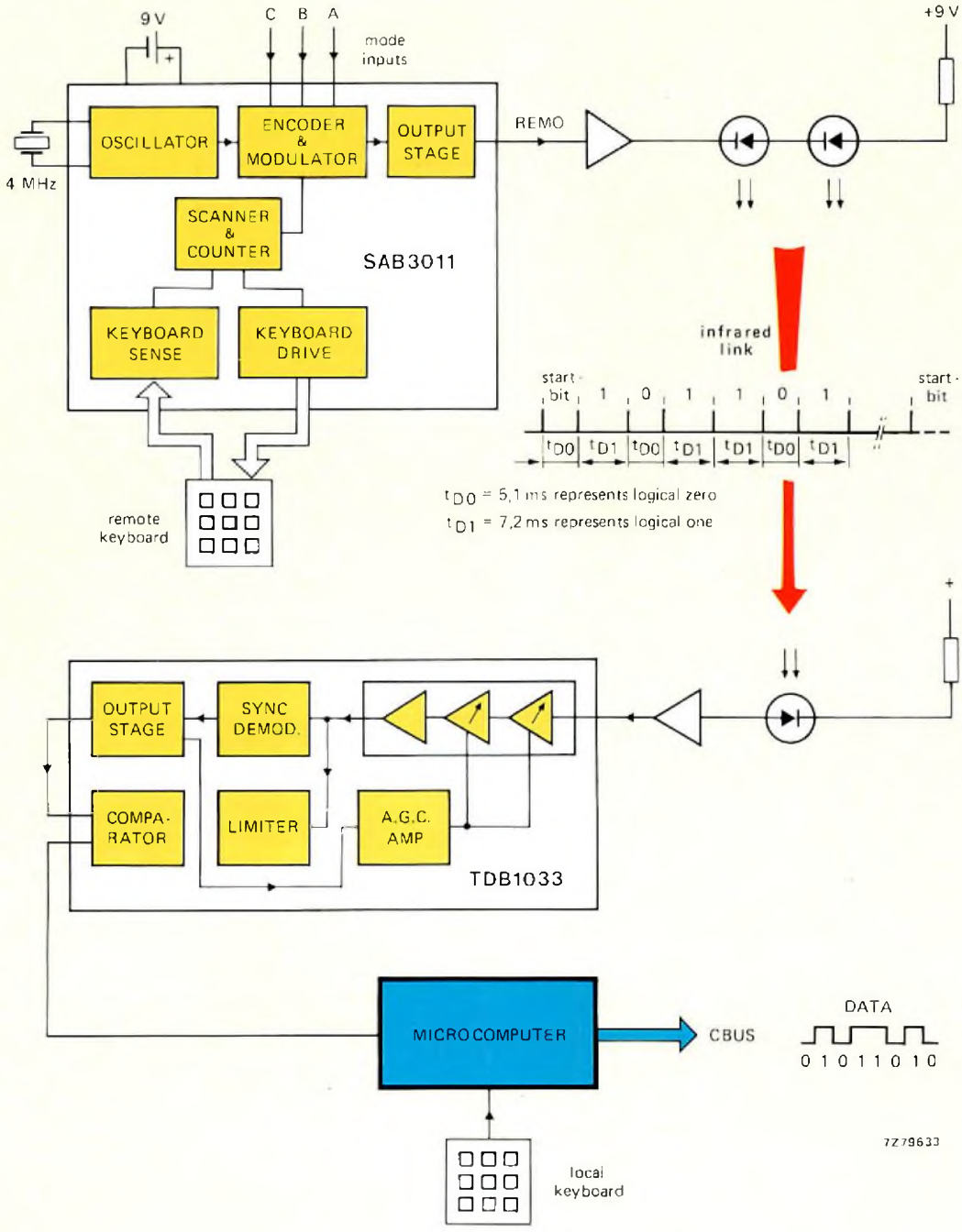

Fig.13 Basic remote control system for the VTS

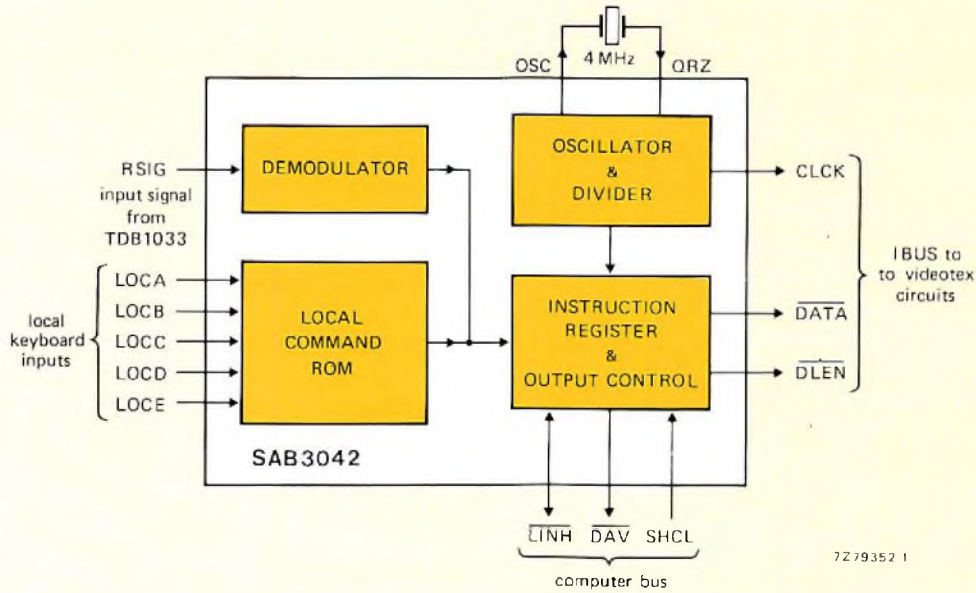

Fig.14 Block diagram of infrared decoder circuit SAB3042

board with 64 keys and one two-position switch is used, the SAB3011 can transmit 128 different command codes. It is therefore suitable for controlling more than one system, e.g. radio, television, hi-fi.

Figure 13 shows a block diagram of the SAB3011. In the stand-by state, the keyboard drive outputs are connected to the positive supply rail. When a key is pressed, current flows between the selected keyboard output and keyboard sense input, thereby starting the oscillator and initiating a keyboard scanning sequence. The scanning counter controls this operation in such a way that the value in the counter represents the code of the pressed key. The counter stops when it has located the pressed key, thereby memorising the key code. The output cycle is then started. The command word is transmitted at least twice and continues to be transmitted for as long as the key remains pressed. The command word consists of the 6-bit key code preceded by a start bit. The interval between the transmitted pulses indicates the state of the command word bits so that the word duration depends on the code being transmitted. Each pulse of the transmission shown in Fig.13 consists of a burst of six pulses lasting 154 μs. This prevents the execution of false commands due to background infrared radiation. The SAB3011 also has three MODE inputs which determine the mode of operation (infrared or ultrasonic) and the state of the start bit which precedes each command word.

The TDB1033 is the infrared receiver of the VTS. As shown in Fig.13, the incoming signal is detected by a photodiode and amplified by the differential input amplifier. The synchronous demodulator and a.g.c. circuits ensure rejection of spurious signals. The comparator provides a constant output level for a wide range of input amplitude. Although the TDB1033 is a bipolar IC, its output is MOS-compatible so that it can be directly connected to the T1 input of the NMOS microcomputer.

Remote control with the addition of SAB3042

The SAB3042 (Fig.14) demodulates the command words received from the TDB1033, checks their validity and provides an IBUS output for direct control of videotex circuits such as teletext of viewdata. The circuit also has a 3-wire, asynchronous, bidirectional computer bus for connection to the VTS microcomputer. Facilities are also provided for accepting commands from a local keyboard. If the SAB3042 is connected between the TDB1033 and the microcomputer in remote control systems such as that shown in Fig.13, the task of the microcomputer is much simplified because it need not validate incoming signals.

The RSIG input receives the pulse-position modulated signal from the infrared receiver TDB1033. When two consecutive, identical command words have been received, the command is judged valid, demodulated and stored in the instruction register.

Inputs LOCA, LOCB, LOCC, LOCD and LOCE allow commands to be received from a local keyboard. These have priority over remote commands. The assignment of the local commands is defined by an internal ROM. The required functions for a specific system can therefore be mask-programmed.

The IBUS outputs $\overline{\text{DATA}}$ and $\overline{\text{DLEN}}$ are normally HIGH; $\overline{\text{DLEN}}$ becomes LOW for the duration of valid data on the DATA line. If the $\overline{\text{DLEN}}$ line is already LOW prior to a command output, the command is delayed until the IBUS is available ($\overline{\text{DLEN}}$ HIGH). The command is then clocked out of the instruction register and along the $\overline{\text{DATA}}$ line in serial form.

The unidirectional computer bus lines $\overline{\text{DAV}}$ and $\overline{\text{SHCL}}$, and the bidirectional line $\overline{\text{LINH}}$ are normally HIGH. When a valid command is received at the RSIG input, $\overline{\text{DAV}}$ goes LOW. If the bus is busy, the microcomputer holds $\overline{\text{LINH}}$ HIGH to prevent the previous command stored in the instruction register from being changed before it has been transmitted along the bus. When the bus becomes available, the microcomputer sets $\overline{\text{LINH}}$ LOW and asynchronous clock pulses, derived from the microcomputer via the $\overline{\text{SHCL}}$ line, clock the instruction word from the instruction register onto the $\overline{\text{DAV}}$ line. The first seven bits of the instruction are the command word received from the keyboard. This is followed by two bits which indicate whether the command originated from the local or remote keyboard.

LITERATURE

1. DICS Digital tuning system for TV receivers, Technical Note 024. N.V. Philips' Gloeilampenfabrieken, Elcoma Marketing Communications, Eindhoven, The Netherlands. 1977.
2. Comprehensive remote control system for TV Technical Information 048. N.V. Philips' Gloeilampenfabrieken, Elcoma Marketing Communications, Eindhoven, The Netherlands. 1978.

Image intensifiers have reached the point at which the only limit to seeing in the dark is the statistical nature of light itself. Current developments are therefore concentrated on reducing their size and cost. The major advance in this direction is the incorporation of microchannel plates (channel electron multiplier plates) in second-generation tubes. These tubes attain the same intensification over a length of a few millimetres as their predecessors did over several centimeters.

This new tube, the XX1500, incorporates such a plate and, apart from shortness and lightness, offers the advantages of protection against bright sources and confining point highlights to the area in which they occur. The S25 photocathode has a spectral response suited to night-sky illumination, and computer control of its deposition ensures high sensitivity and consequently low noise. The 18 mm input and output windows are both fibre-optic, thus making lens design simpler. Fully automated deposition of the phosphor screen accounts for resolution at least 10% better than that of competing tubes. The P20 phosphor used is recognised as being the best suited to the scotopic eye.

The XX1500 costs about the same as earlier (first-generation) tubes and, in fact, makers of night-vision systems need only shorten the body of existing designs with 18 mm cascade tubes to gain all its advantages. Automatic gain control is included, as is provision for external adjustment of gain. With this tube objects can be clearly discerned at 800 metres under starlight conditions.

Single-phase rectifier circuits with CR filters

Part 2 - Design procedure

A. LIEDERS

INTRODUCTION

In the first part of this article (Ref. 1), a comprehensive set of equations was derived to describe the transformer-fed semiconductor rectifier and CR filter combination, and these equations are summarised here in Table 2. The use of the equations can, however, be time-consuming and therefore a set of nomograms, developed from the equations, is given here to provide a quick, simple, and accurate design aid for practical circuits. A step-by-step guide to using the nomograms is given later.

Both the equation-based calculation procedure and the nomograms require the circuit designer to make initial assumptions about the type of circuit to be used (Figs.1 to 4), output power, and so on, and to select suitable semiconductor rectifiers. If the design procedure given is then followed, circuit values are calculated to enable the designer to make an accurate choice of resistors and capacitors, and to check the suitability of the selected semiconductor rectifiers.

Finally, a comparison of theoretically derived circuit values with measured values for eight practical circuits shows that the equations (and nomograms) are an adequate description of real circuits and a significant improvement on previously used methods.

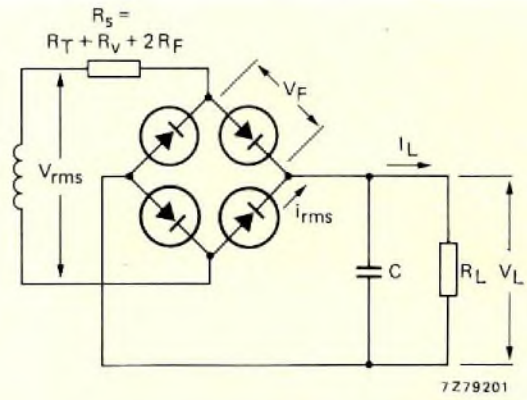

Fig.1 Bridge rectifier equivalent circuit showing elements and quantities used in calculations

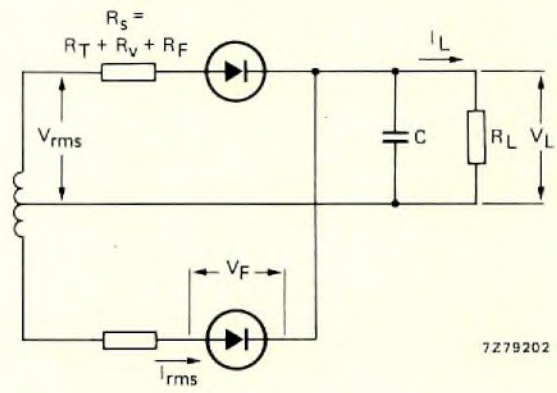

Fig.2 Full-wave rectifier equivalent circuit showing elements and quantities used in calculations

CALCULATION PROCEDURE

First define the required output characteristics V_L and I_L (and thus R_L), and set a limit on the ripple factor r. (These and other symbols used in this article are defined in Table 1.) (Note that the angular frequency $\omega = 2\pi f$ of the mains supply is known.) Next select a suitably rated

TABLE 1

List of symbols

Symbol	Definition
C	filter capacitor
D	rectifier diode
f	mains frequency
$I_{C(rms)}$	r.m.s. value of filter-capacitor ripple current
$I_{F(AV)}$	average forward current through diode
$I_{F(AV)\ max}$	maximum permitted diode average forward current
I_{FIM}	maximum inrush (surge) current
I_{FRM}	repetitive peak forward current through rectifier diode
I_L	load current
I_{rms}	r.m.s. value of diode current
$i_{1\text{-}2}$	instantaneous value of current through R_s during the period from 1 to 2
P_D	rectifier diode power dissipation
P_v	surge-limiting resistor power dissipation
Q	electric charge
R_F	diode forward resistance (as defined in Fig.1)
R_{FD}	diode forward resistance (as defined by traditional methods)
R_L	resistance of load
R_s	source resistance ($R_T + R_v + R_F$, or $R_T + R_v + 2R_F$)
R_T	resistance of power transformer seen looking into the secondary
R_v	surge-limiting resistance
r	ripple factor ($V_{C(rms)}/V_L$)
T	period of mains waveform
t	time
V_{CM}	peak value of ripple voltage in a doubler
$V_{C(rms)}$	r.m.s. value of filter-capacitor ripple voltage
V_F	diode forward voltage (as defined in Fig.1)
V_{FD}	diode forward voltage (as defined by traditional methods)
V_L	mean value of fluctuating rectified direct voltage
V_M	peak secondary voltage
V_{rms}	r.m.s. value of filter input voltage
V_{RWM}	crest working voltage of diode
v	open-circuit secondary voltage of transformer
v_L	instantaneous value of rectified voltage
v_n	rectified and inverted negative portion of input to filter for a doubler
v_p	rectified positive portion of input to filter for a doubler
v_1	minimum value of v_L
v_2	maximum value of v_L
x	$= \omega t$
α	half conduction angle
δ	phase lag between peak of sinusoidal input voltage waveform and half-point of conduction angle
ϕ	$= \delta - x$
ω	angular frequency of mains

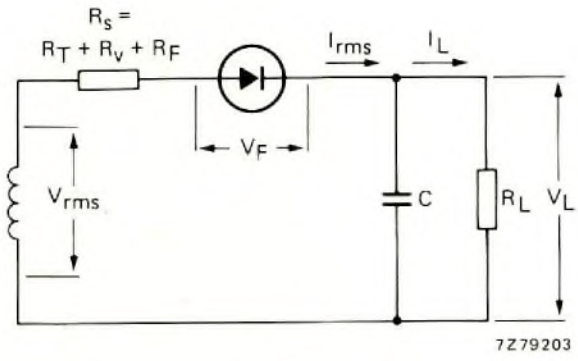

Fig.3 Half-wave rectifier circuit showing elements and quantities used in calculations

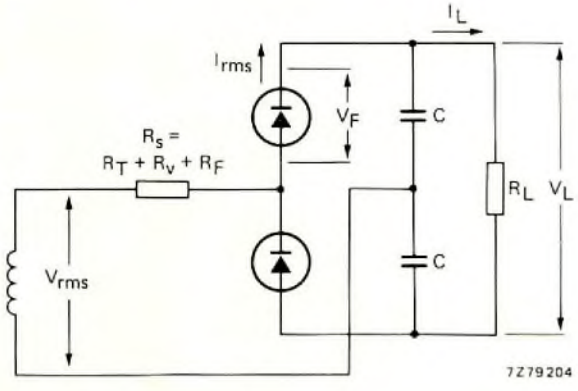

Fig.4 Symmetrical voltage doubler equivalent circuit showing elements and quantities used in calculations

diode, bearing in mind the type of circuit; that is, the diode average forward current $I_{F(AV)}$ equals I_L for half-wave and voltage doubler circuits, and equals $\frac{1}{2}I_L$ for full-wave and bridge circuits. The value of $I_{F(AV)}$ must be less than $I_{F(AV)\,max}$ for the diode, and I_{FRM} must be greater than $6I_{F(AV)}$. The value of V_{RWM} for the diode must be greater than $1.5V_L$ for bridge and doubler circuits, and greater than $3V_L$ for half- and full-wave circuits.

The values of V_F and R_F are now calculated from the maximum V_F against I_F curve in the published data, in the way shown in Fig.5b. V_F and R_F are given by:

$$V_F = 2V_{F2} - V_{F1},$$

$$R_F = \frac{2(V_{F1} - V_{F2})}{I_1},$$

where V_{F1} is the diode forward voltage drop at a current I_1 ($= 6I_{F(AV)}$), and V_{F2} is the diode forward voltage drop at a current $\frac{1}{2}I_1$. (I_1 is chosen to be $6I_{F(AV)}$ since this represents the typical value of the peak diode current during conduction. V_F and R_F may need to be recalculated if the diode peak current, calculated later, is not within ±10% of $6I_{F(AV)}$.)

To start the calculation, it is necessary to estimate the value of R_s. This includes R_F and the transformer resistance R_T, together with the value of any surge-limiting resistor R_v. The value of R_s is generally between 1 and 10% of R_L; it has a minimum value set by the surge current permitted through the selected diode. Once a good estimate has been made of R_s, calculation proceeds as follows.

1) Determine the value of A using Eq. 26 or 34 according to the type of rectifier circuit. From A, the value of a may be obtained from Table 2 in Part 1 (Ref. 1) or Nomogram 1; it is not easily calculated from Eq. 27 or 35.

2) The diode repetitive peak forward current I_{FRM} is given by Eq. 33 or 41. If the value of I_{FRM} obtained from this calculation differs by more than 10% from $6I_{F(AV)}$ (which has been used to determine R_F and

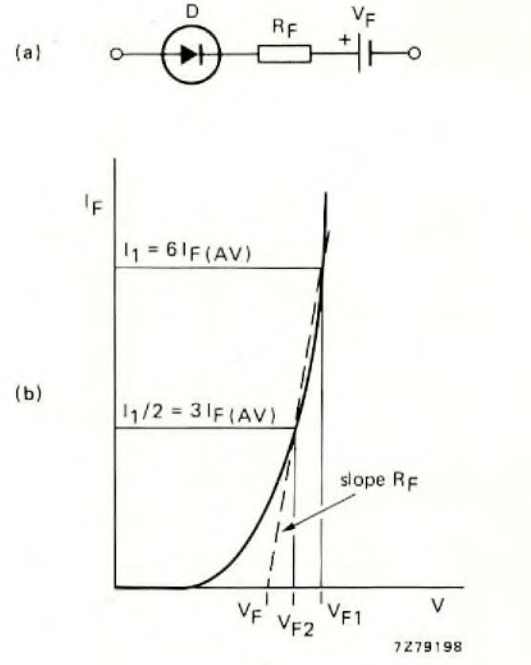

Fig.5 (a) Equivalent circuit of rectifier diode used as model for calculation purposes
(b) Method of determining parameters of equivalent circuit from published diode characteristics

$V_F = 2V_{F2} - V_{F1}$ $R_F = 2(V_{F1} - V_{F2})/I_1$

$I_{F(AV)}$ = Manufacturers Value ?

TABLE 2

Equations derived in Part 1

Unknown	Refer to Nomogram	Equations					
		Full-wave	Bridge	Equation number	Half-wave	Symmetrical doubler	Equation number
A		$A = \frac{2(V_L + V_F)R_L}{V_L R_s}$	$A = \frac{2(V_L + 2V_F)R_L}{V_L R_s}$	26	$A = \frac{(V_L + V_F)R_L}{V_L R_s}$	$A = \frac{(V_L + 2V_F)R_L}{2V_L R_s}$	34
a	1	$\tan a - a = \frac{\pi}{A}$		27	$\tan a - a = \frac{\pi}{A}$		35
C	2	$C = \frac{\frac{\pi}{2} - a}{r\omega R_L\sqrt{3}}$		31	$C = \frac{\pi - a}{r\omega R_L\sqrt{3}}$	$C = \frac{\pi - 2a}{r\omega R_L\sqrt{3}}$	39
δ	3	$\tan\delta = \frac{\pi - 2a}{A\omega CR_s \tan a}$		28	$\tan\delta = \frac{\pi - a}{A\omega CR_s \tan a}$		36
V_{rms}	4	$V_{rms} = \frac{V_L + V_F}{\sqrt{2}.\cos a\cos\delta}$	$V_{rms} = \frac{V_L + 2V_F}{\sqrt{2}.\cos a\cos\delta}$	29	$V_{rms} = \frac{V_L + V_F}{\sqrt{2}.\cos a\cos\delta}$	$V_{rms} = \frac{V_L + 2V_F}{2\sqrt{2}.\cos a\cos\delta}$	37
I_{rms}	5	$I_{rms} = \frac{AI_L}{2\cos a\cos\delta}\left[\frac{\ell + m + p}{2\pi}\right]^{1/2}$		32	$I_{rms} = \frac{AI_L}{\cos a\cos\delta}\left[\frac{\ell + m + p}{2\pi}\right]^{1/2}$		40
I_{FRM}	6	$I_{FRM} = \frac{AI_L(1 - \cos a)}{2\cos a}$		33	$I_{FRM} = \frac{AI_L(1 - \cos a)}{\cos a}$		41

Note: ℓ, m, and p are as defined below

$$\ell = a + \frac{\sin 2a\cos 2\delta}{2} \qquad m = 2\sin a\sin^2\delta\left(\frac{a\sin a}{3} - \frac{2(\sin a - a\cos a)}{a}\right) \qquad p = 2\cos a\cos^2\delta\,(a\cos a - 2\sin a)$$

V_F), I_{FRM} is used as the value of I_1 to calculate new values of $R_{1'}$ and V_F, and the subsequent calculations are repeated.

3) Determine the value of filter capacitor C from Eq. 31 or 39. Take the next larger standard value for use in further calculation.

4) Calculate tan δ, from Eq. 28 or 36.

5) The transformer open-circuit secondary voltage V_{rms} is now determined using Eq. 29 or 37.

6) The r.m.s. diode current I_{rms} is now calculated using Eq.32 or 40.

7) The crest working voltage that the diode must withstand is given by:

$$V_{RWM} \geq \sqrt{2}.V_{rms}, \qquad (55)$$

for bridge circuits, and by:

$$V_{RWM} \geq 2\sqrt{2}.V_{rms}, \qquad (56)$$

for half-wave, full-wave, and doubler circuits. (Note that, because of the CR filter, capacitive-load conditions apply.)

8) The maximum possible inrush (surge) current is:

$$I_{FSM} = \frac{\sqrt{2}.V_{rms} - kV_F}{R_s}, \qquad (57)$$

where k = 1 for half-wave, full-wave, and doubler circuits, and k = 2 for bridge circuits. The value of inrush current given by Eq. 57 is compared with the single-cycle surge characteristic of the proposed diode.

9) The power dissipated by the diode is:

$$P_D = \frac{V_F I_L}{q} + I^2_{rms} R_F, \qquad (58)$$

where q = 2 for full-wave and bridge circuits, and q = 1 for half-wave and doubler circuits. An additional allowance, for the power dissipated by leakage-currents when the diode is reverse-biased, is necessary. A means of determining this allowance is given in Ref. 2.

10) From the values calculated so far, check that the diode originally selected is adequately rated for the application. If not, another diode is selected and the calculations repeated.

11) The r.m.s. current through the filter capacitor is:

$$I_{C(rms)} = [2I^2_{rms} - I^2_L]^{1/2}, \qquad (59)$$

for full-wave and bridge circuits, and:

$$I_{C(rms)} = [I^2_{rms} - I^2_L]^{1/2}, \qquad (60)$$

for half-wave and doubler circuits. This current must be less than the ripple current rating quoted by the capacitor manufacturer.

12) Finally, check the dissipation of any surge-limiting resistor:

$$P_v = R_v I^2_{rms}. \qquad (61)$$

THE NOMOGRAMS

Nomograms have several advantages in calculations of this type. They save a great deal of tedious computation, as would be necessary with Eqs. 27, 32, 35, and 40; they provide rapid solutions to an accuracy adequate for engineering purposes; and they allow the effect of component tolerances and changes in circuit values to be appreciated quickly. Together, the nomograms designed from the equations derived in this article provide the four basic circuit values V_{rms}, I_{rms}, I_{FRM}, and C in the minimum of time. Starting with the dimensionless quantity A, computed from Eq. 26 or 34, the nomograms provide the values of factors B, D, F, K, and M. These are used in simple calculations to give the required basic circuit values.

Nomogram 1 gives the value of α in degrees or radians for subsequent use in the calculation procedure.

Nomogram 2 is the first nomogram required in the nomogram procedure that replaces the calculation sequence. It yields factor B from quantity A. Factor B is used to calculate the value of the filter capacitor C required to obtain a given ripple factor r:

$$C = \frac{B}{r\omega R_L} = \frac{B}{2\pi r f R_L},$$

where frequency f is in hertz and load resistance R_L in ohms. Use the nomogram appropriate to the type of rectifier circuit.

Nomogram 3 yields the value of factor D for calculating the value of tanδ for use in Nomogram 4:

$$\tan\delta = \frac{D}{\omega C R_s} = \frac{D}{2\pi f C R_s},$$

where C is the value of the filter capacitor in farads, f is in hertz and R_s in ohms.

Nomogram 4 uses the value of tanδ obtained from Nomogram 3 to determine V_{rms} by means of factor F:

$V_{rms} = F(V_L + V_F)$ for half-wave and full-wave rectifiers,

$V_{rms} = F(V_L + 2V_F)$ for bridge rectifiers,

$V_{rms} = F(V_L + 2V_F)/2$ for symmetrical doublers.

Nomogram 5 yields the value of factor K from which the value of I_{rms} can be calculated:

$I_{rms} = KI_L$ for half-wave and doubler circuits,

$I_{rms} = KI_L/2$ for full-wave and bridge circuits.

Nomogram 6 yields the value of factor M from which the repetitive peak forward current I_{FRM} can be calculated:

$I_{FRM} = MI_L$ for half-wave and doubler circuits,

$I_{FRM} = MI_L/2$ for full-wave and bridge circuits.

The six nomograms are given at the end of this article, on pages 226 to 230.

COMPARISON OF CALCULATED AND MEASURED VALUES

In order to check the accuracy of the calculation method, a number of practical rectifier circuits with CR filters were constructed and their properties measured. A power transformer of known resistance was used, and the filter capacitor was a polyester type whose value could be measured precisely. The characteristics of the rectifier diodes were individually determined using a curve tracer. All resistors used were also individually measured.

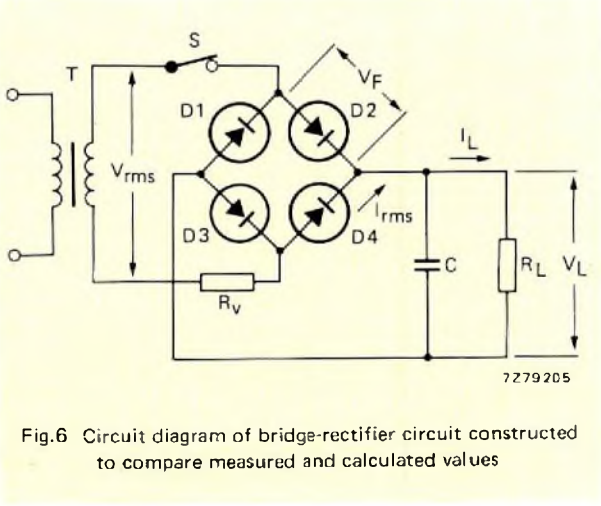

Fig.6 Circuit diagram of bridge-rectifier circuit constructed to compare measured and calculated values

Bridge circuit

A bridge circuit was the first one examined. The various components are identified in Fig. 6.

Power transformer	Input voltage variable, R_T = 4.94 Ω
Diodes D_1, D_2, D_3, and D_4	BAX13, V_F = 0.77 V, R_F = 5.75 Ω
Surge-limiting resistor	R_v = 3.28 Ω
Load	R_L = 497 Ω
Filter capacitor	C = 37.5 μF

The voltage applied to the primary of the power transformer was adjusted to give V_L = 10 V. By measuring the peak and r.m.s. voltages across R_v, the values of I_{rms} and I_{FRM} were determined. The peak-to-peak ripple voltage across R_L was measured, and from it the value of $V_{C(rms)}$ calculated. Angles a and δ were determined using an oscilloscope. The value of V_{rms} was measured with switch S open. The following values were measured.

V_{rms} = 9.5 V
I_{rms} = 26.7 mA
I_{FRM} = 91.6 mA
r = 0.0894
a = 34° (0.5934 rad)
δ = 10° (0.1745 rad)

Calculated values

Using the calculation procedure given earlier, the circuit can be designed from the following data.

V_L = 10 V
$I_L = V_L/R_L$ = 20.1 mA
R_F = 5.75 Ω
R_v = 3.28 Ω
ω = 120π rad/s (f = 60 Hz)
R_L = 497 Ω
V_F = 0.77 V
R_T = 4.94 Ω
C = 37.5 μF

The values required are V_{rms}, I_{rms}, I_{FRM}, r, a, and δ.

The source resistance is:

$$R_s = R_T + R_v + 2R_F = 19.7\ \Omega.$$

Now, the value of A is calculated:

$$A = \frac{2(V_L + 2V_F)}{V_L}\frac{R_L}{R_s} = 58.2.$$

From Nomogram 1, $a = 0.524$ rad ($= 30°$).

Since the value of C is given, Eq. 31 is used to determine the ripple factor r:

$$r = \frac{\frac{\pi}{2} - a}{\omega C R_L \sqrt{3}} = 0.086.$$

The next step is to calculate tanδ from Eq. 28:

$$\tan\delta = \frac{2\left(\frac{\pi}{2} - a\right)}{A\omega C R_s \tan a} = 0.224,$$

and thus $\delta = 12.6°$.

From Eq. 29, the required transformer open-circuit secondary voltage is:

$$V_{rms} = \frac{V_L + 2V_F}{\sqrt{2}.\cos a \cos\delta} = 9.65 \text{ V}.$$

The value of I_{rms} is given by Eq. 32:

$$I_{rms} = \frac{AI_L}{2\cos a \cos\delta}\left[\frac{\ell + m + p}{2\pi}\right]^{\frac{1}{2}}.$$

Now, $\ell = 0.91595$, $m = -0.0043215$, and $p = -0.90211$. (Note that the values of ℓ, m, and p have a large effect on the value I_{rms} and should be determined to five significant figures.) Thus:

$$I_{rms} = 26.94 \text{ mA}.$$

The value of I_{FRM} is given by Eq. 33:

$$I_{FRM} = \frac{AI_L(1 - \cos a)}{2\cos a} = 90.6 \text{ mA}.$$

The nomograms would give essentially the same results.

Alternative calculation method

A useful adaptation of Schade's method (Ref. 3) was made by Dayal (Ref. 4). Dayal presented design calculations and practical design procedures which are useful at high voltages. The results obtained using the method due to Dayal in low-voltage circuits are, however, not as accurate as might be desired; this is to be expected since it is a method adapted from work on valve rectifiers.

In order to compare Dayal's analysis and the analysis outlined in this article, the bridge rectifier circuit of Fig. 6 was also designed using Dayal's method.

The first obvious difference is in the determination of the idealised diode characteristics; Fig. 7 shows how this is done in Ref. 4. Using Dayal's method, the following

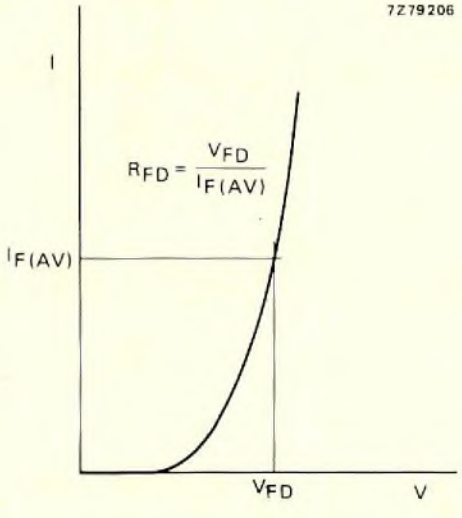

Fig.7 Determination of ideal diode characteristics according to method of Ref. 4

values are obtained for the BAX13 diodes. The average forward current is:

$$I_{F(AV)} = \frac{I_L}{2} = 10.05 \text{ mA}.$$

The forward voltage drop at this current is:

$$V_{FD} = 0.8 \text{ V},$$

and the forward resistance is:

$$R_{FD} = \frac{V_{FD}}{I_{F(AV)}},$$
$$= \frac{0.8 \times 10^3}{10.05} = 79.6\ \Omega,$$

so that the source resistance is:

$$R_s = R_T + R_v + 2R_{FD} = 167\ \Omega.$$

Following the instructions of Ref. 4, the next quantities to be derived are:

$$\frac{R_s}{R_L} \times 100 = 33.7\%,$$

and:

$$\omega R_L C = 7.03.$$

Using these values, the ripple factor is found from Fig. 16 in Ref. 4:

$$\frac{V_{C(rms)}}{V_L} \times 100 = 6.8\%.$$

The nomogram in Ref. 4 (Fig. 14) gives:

$$\frac{V_L}{V_{rms}\sqrt{2}} \times 100 = 55\%,$$

from which the required transformer open-circuit secondary voltage is:

$$V_{rms} = \frac{10}{55\sqrt{2}} \times 100 = 12.9 \text{ V}.$$

Next, the following values are calculated:

$$\frac{R_s}{2R_L} \times 100 = 16.8\%,$$

and:

$$2\omega R_L C = 14.$$

Then, from Fig. 17 in Ref. 4:

$$\frac{I_{rms}}{I_{F(AV)}} = 2,$$

and thus:

$$I_{rms} = 2 \times 10.05 = 20.1 \text{ mA}.$$

From Fig. 18 in Ref. 4:

$$\frac{I_{FRM}}{I_{F(AV)}} = 4.8,$$

and thus:

$$I_{FRM} = 4.8 \times 10.05 = 48.2 \text{ mA}.$$

Summary of results

Table 3 lists the results obtained by measurement and from the two methods of calculation. The calculation method outlined in this article is shown to give results that are sufficiently accurate for engineering purposes, whereas it is clear that some further development of the circuit designed by the method of Ref. 4 would be required.

Measurements on other circuits

The same calculation-and-measurement exercise described for the bridge rectifier circuit was performed on a number of other circuits. The details of these are given in Table 4.

In order to show the relative accuracy of the two methods of calculation, the percentage deviation from the measured results:

$$\frac{\text{calculated value} - \text{measured value}}{\text{measured value}} \times 100\%$$

of the various quantities calculated are plotted in Figs. 8 (r), 9 (V_{rms}), 10 (I_{rms}), and 11 (I_{FRM}).

CONCLUSION

The value of the required transformer open-circuit secondary voltage V_{rms} as calculated by the method presented in this article is very close to the measured value. Thus a transformer designed in accordance with these calculations will give the required in-circuit performance without modification. This will not usually be the case with a transformer designed according to the method of Ref. 4, especially at low voltages.

Furthermore, the values of I_{rms} and I_{FRM} obtained by the method of Ref. 4 are significantly lower than the values measured, or calculated by the method given in this article. Thus there is a possibility that a diode selected on the basis of the older method of calculation

TABLE 3

Comparison of measured and calculated values

Quantity	Measured value	Calculated values		Units
		New method	Ref. 4 method	
V_{rms}	9.5	9.65	12.9	V
I_{rms}	26.7	26.3	20.1	mA
I_{FRM}	91.6	90.5	48.2	mA
r	0.089	0.086	0.068	–
a	0.593	0.524	–	rad
δ	0.175	0.220	–	rad

TABLE 4

Values for other circuits constructed to test design methods

Circuit Type	No.	R_L Ω	V_L V	R_s (Ω) Method New	R_s (Ω) Method Ref. 4	C μF	Diode type
Half-wave	1	497	30	6.3	21.2	37.5	BY126
	2	497	30	59	74	37.5	BY126
Full-wave	3	497	30	7.3	32.4	37.5	2 X BAX17
	4	497	30	59.2	85.1	37.5	2 X BAX17
Bridge	5	497	10	19.7	167	37.5	4 X BAX13
	6	497	10	72.4	220	37.5	4 X BAX13
Doubler	7	1540	40	59	113	18.75	2 X BY126
Bridge	8 (see note)	60	120	2.125	3.73	3137	BY224

Note: The values for circuit 8 were calculated assuming a mains frequency of 50 Hz (all others at 60 Hz) and the use of an appropriate transformer.

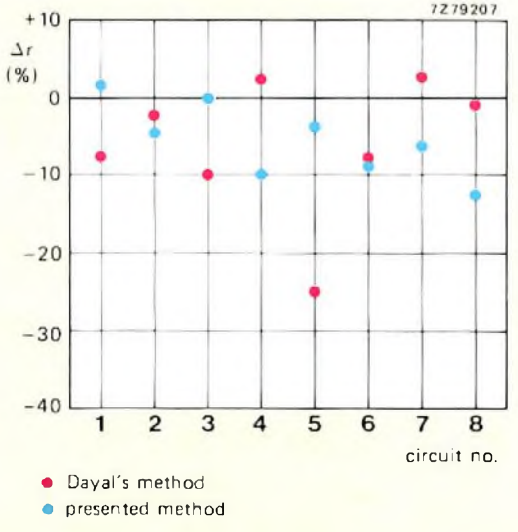

Fig.8 Deviation from measured value of ripple factor (r) calculated by method given in this article and method of Ref. 4

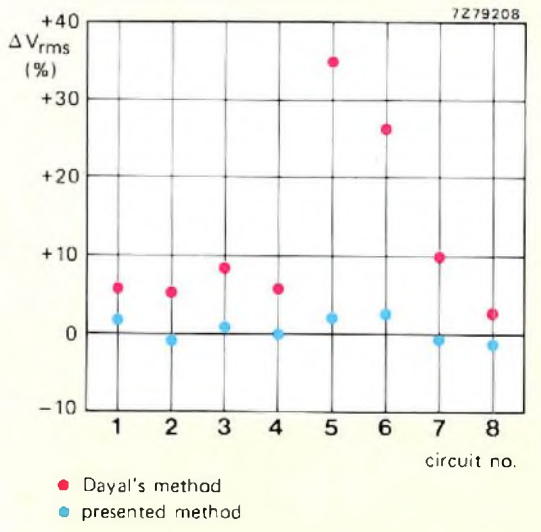

Fig.9 Deviation from measured value of V_{rms} calculated by method given in this article and method of Ref. 4

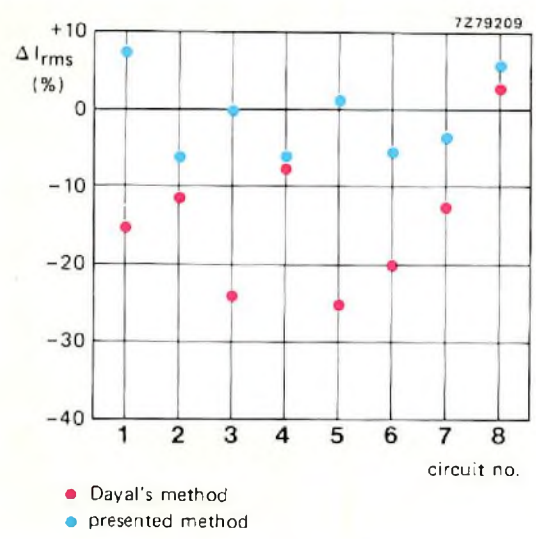

Fig.10 Deviation from measured value of I_{rms} calculated by method given in this article and method of Ref. 4

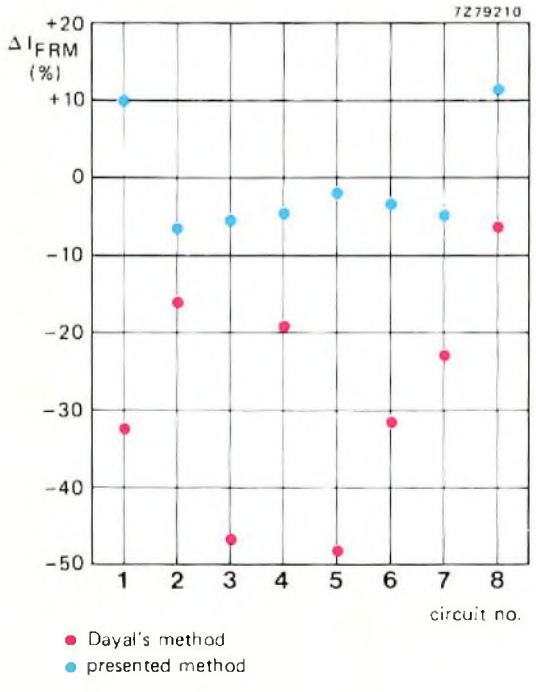

Fig.11 Deviation from measured value of I_{FRM} calculated by method given in this article and method of Ref. 4

might work outside its ratings, with a consequent loss of reliability and useful life.

It can, therefore, be said that the equations derived in Part 1 of this article (Ref. 1), and the nomograms and calculation procedure developed from them, are to be preferred for the design of semiconductor rectifier and CR filter circuits. That the adaptation of Schade's method, developed as it was for thermionic rectifiers, gives less accurate results, is not surprising in view of the differences between thermionic and semiconductor device characteristics.

ACKNOWLEDGEMENT

The author wishes to express his gratitude to P.E. Magyar of Application and Development Laboratory, IBRAPE, Sao Paulo, Brazil, for his helpful ideas and advice in the preparation of these articles; to B.G. Starr of Mullard Application Laboratory, Mitcham, UK for his careful study of the work and useful suggestions; to E.J. Hoefgeest of Elcoma Central Application Laboratory, Eindhoven, The Netherlands; and to all who helped in the publication of this work.

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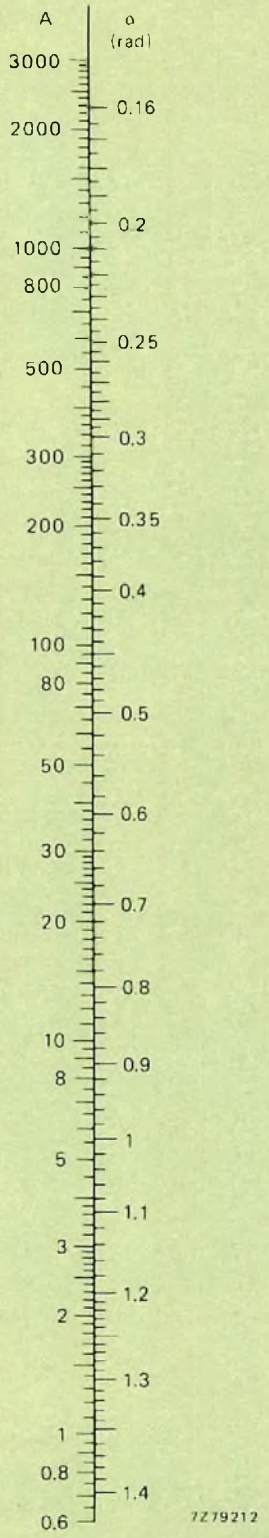
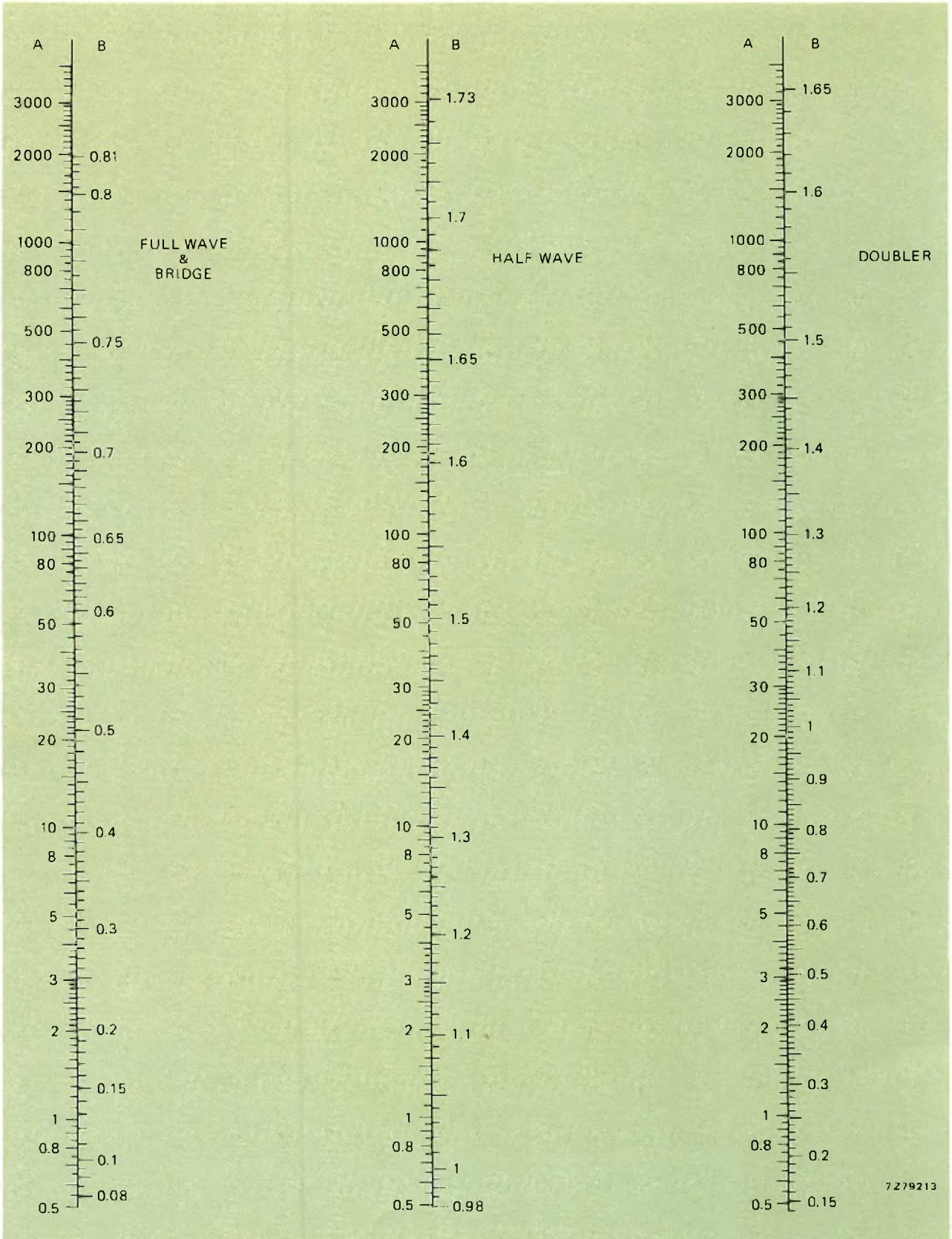
Errata
ECA Vol.1, No.3, May 1979
Single-phase rectifier circuits with CR filters

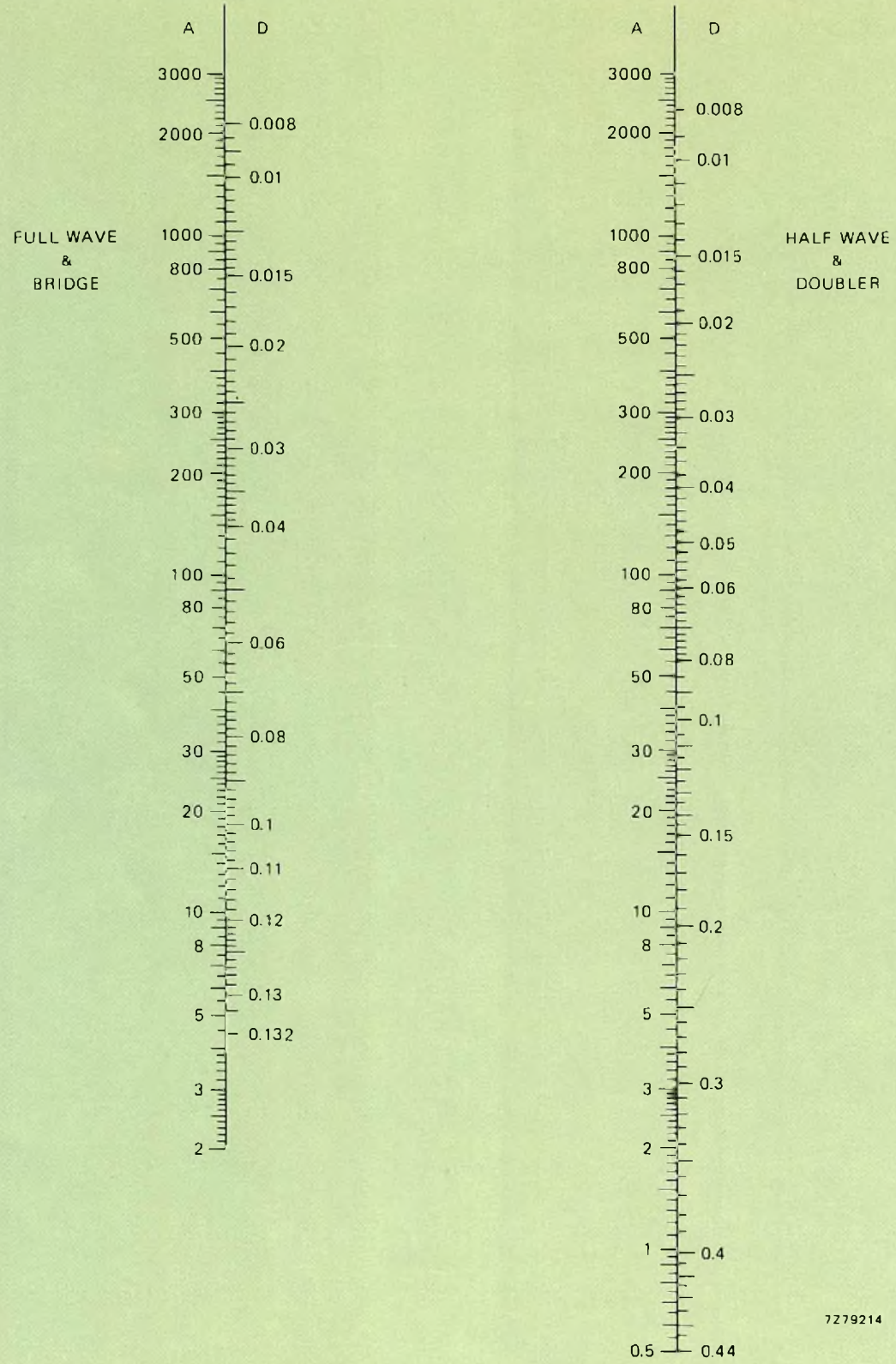
On page 153, right-hand column, the sentence starting on line six should read "Furthermore, even when the CR product of the filter network is not larger than the period of the mains-voltage waveform ..." On page 155, left-hand column, the first line should start "measured values."



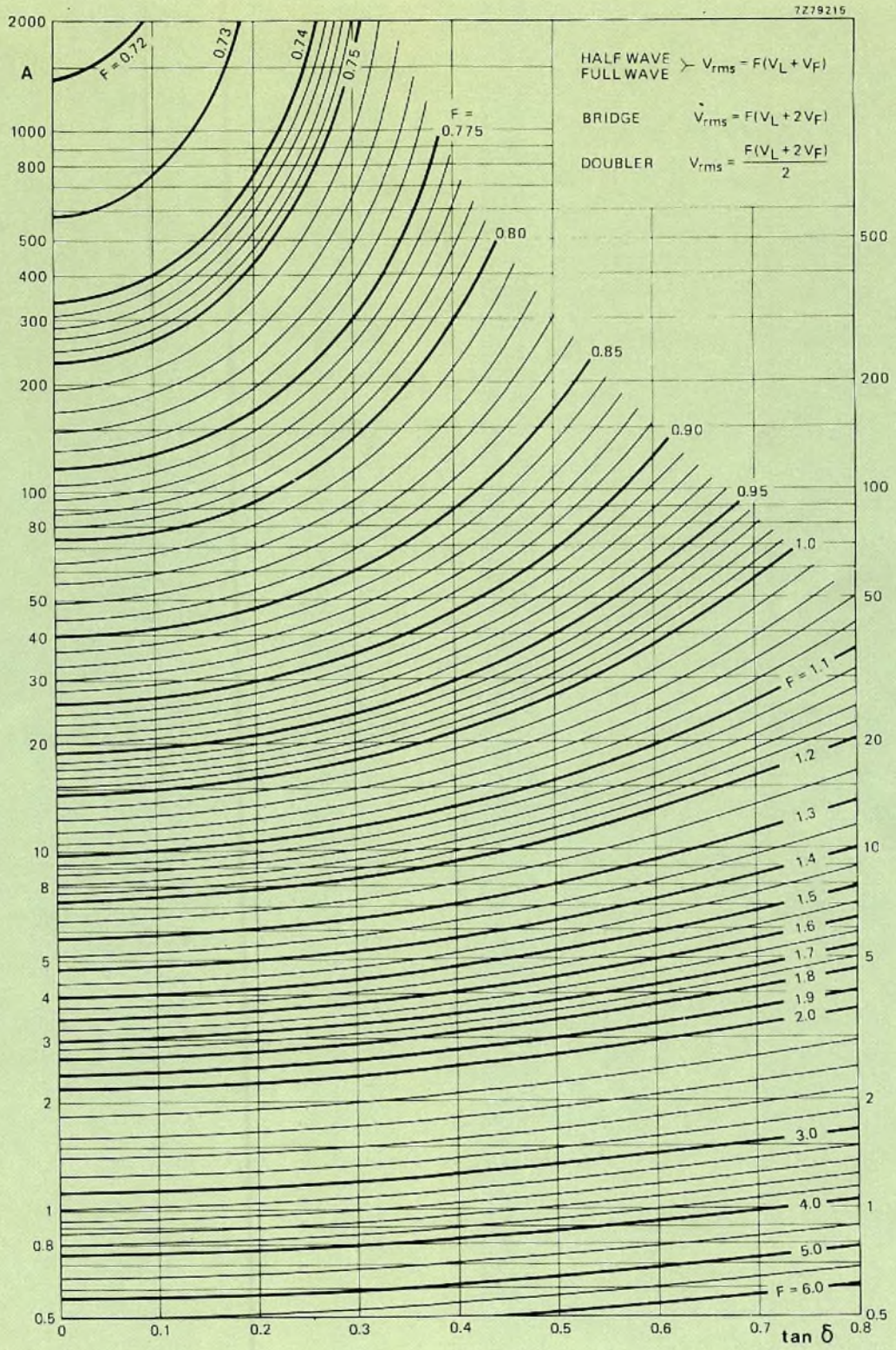
Nomogram 1 Value of half conduction angle α as function of dimensionless quantity A. .



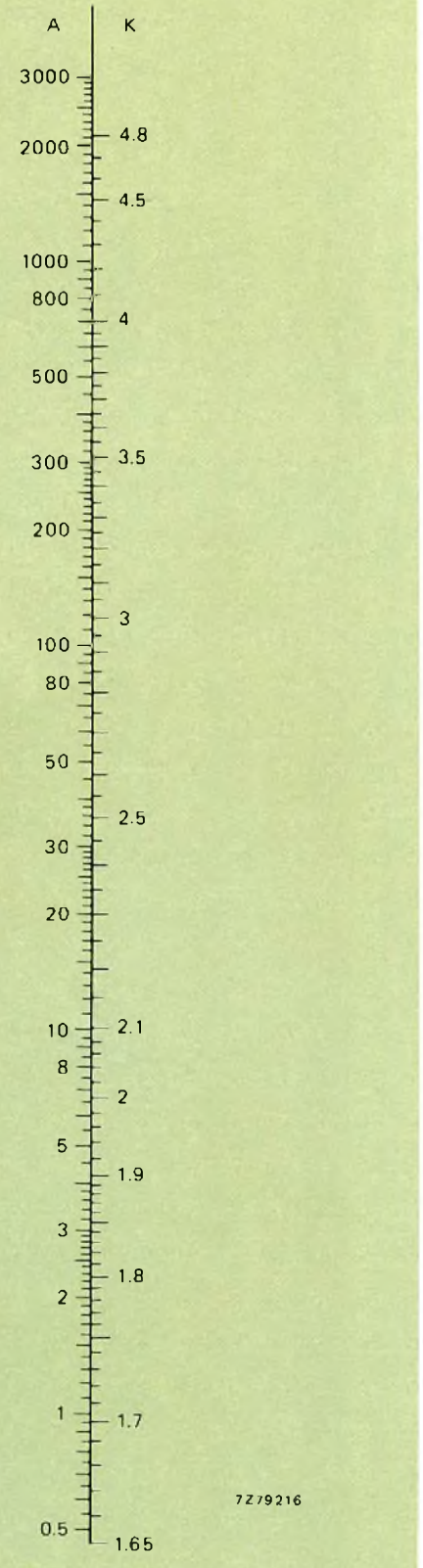
Nomogram 2 Nomogram for determining factor B from which value of filter capacitor C can be calculated $C = B/(r\omega R_L)$. Use scale appropriate to type of rectifier circuit



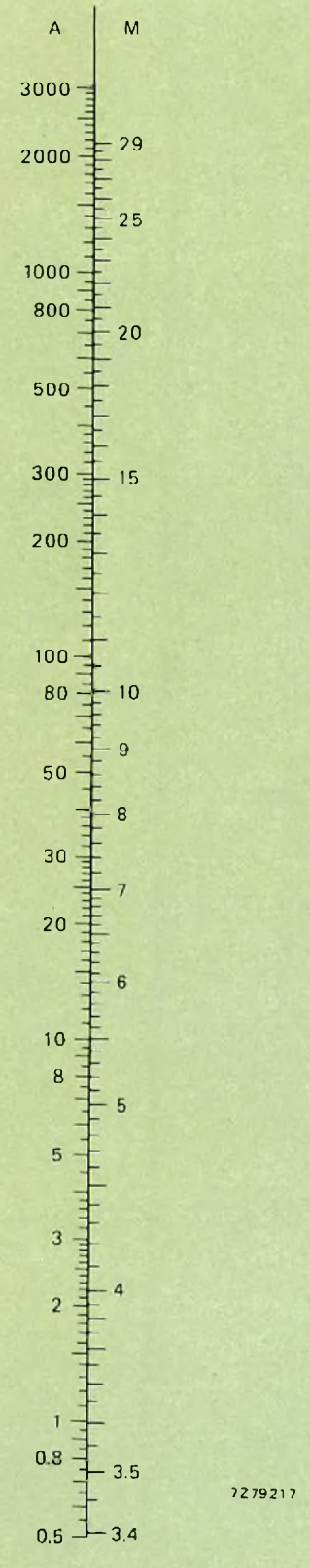
Nomogram 3 Factor D as function of quantity A.
From D, the value of tanδ for use in nomogram 4 can be determined:
$\tan\delta = D/(\omega CR_s)$. Use scale appropriate to type of rectifier circuit



Nomogram 4 Chart for determining factor F from quantity A and tanδ.
From F, the required value of V_{rms} can be determined:
$V_{rms} = F(V_L + V_F)$ for half-wave and full-wave rectifiers
$V_{rms} = F(V_L + 2V_F)$ for bridge rectifiers
$V_{rms} = F(V_L + 2V_F)/2$ for symmetrical doublers



Nomogram 5 Factor K as function of quantity A.
From K, the value of I_{rms} can be calculated:
$I_{rms} = KI_L$ for half-wave and doubler circuits
$I_{rms} = KI_L/2$ for full-wave and bridge circuit



Nomogram 6 Factor M as function of quantity A.
From M, the value of I_{FRM} can be calculated:
$I_{FRM} = MI_L$ for half-wave and doubler circuits
$I_{FRM} = MI_L/2$ for full-wave and bridge circuits

Digital control of radio and audio equipment

Part 2 - Voltage converter and memory for preset radio tuning

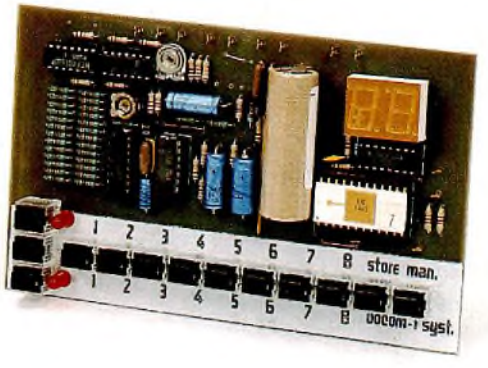
J. W. BEUNDERS

About ten years ago, a typical high-class European radio incorporated variable-capacitance diodes for tuning the f.m. waveband and had a few potentiometers for presetting selected stations. Since then, the increased number of f.m. broadcasts available to European listeners and the development of variable-capacitance diodes suitable for tuning the a.m. wavebands* has led to a demand for many more presets than were required hitherto. Since the restricted front-panel area of modern low-profile radios will often not accommodate a large number of electromechanical presets, we have developed a compact digitally-controlled preset tuning system which can be added to single or two-waveband radios with voltage-controlled tuning.

The preset tuning system is based on our monolithic voltage converter and memory (VOCOM) type SAA1089. The following are features of the system:

- Static operation.
- Long-term stability of preset frequencies.
- Presetting and selection of up to 16 stations without programme interruption.
- Three modes of operation: one waveband, 16 presets; two wavebands selected by VOCOM with 8 presets per waveband; two wavebands electromechanically selected with 8 presets per waveband.
- LED indication of waveband in use.
- Muting during presetting and selection.
- Conventional manual tuning and a.f.c. action retained.
- Typical standby current of only 0.5 μA.
- No interference because digital signal processing is only active during station presetting and selection.

* The recently introduced 8 V dual variable-capacitance diode type BB212.



Laboratory model of a VOCOM system

More extensive information for potential users is available in a separate publication. Requests for copies should mention this article, and the nature of the applicant's interest.

PRINCIPLES OF OPERATION

The VOCOM system is based on the principle of voltage synthesis. For presetting a station, the radio must firstly be manually tuned to the desired frequency. The manually-controlled tuning voltage level is then converted into a binary number and stored in a non-volatile RAM at one of 16 locations addressed by one of the pushbuttons on the VOCOM control panel. For selecting a preset station, the RAM is addressed from the control panel, and the binary number stored at the addressed location is converted into a voltage step by a DAC. This voltage increment is applied to the radio tuner instead of the manually-controlled tuning voltage. The selected RAM address (preset station number) is indicated by a 1½-digit, 7-segment LED numeral display driven via a standard decoder/driver IC.

The digital functions of the system are performed by a 24-pin DIL dedicated LSI circuit type SAA1089. The analogue and DAC functions are performed by standard integrated circuits. A simplified circuit diagram of the system is given in Fig.1.

Presetting a station

To preset a station, the system must first be set to manual operation by pressing the MAN button on the VOCOM control panel. This sets the reset/manual output (REM) from the SAA1089 to the HIGH state, thereby resetting the internal and external 12-bit counters and setting the electronic switch to the manual position. The radio must then be manually tuned and one of the numbered station pushbuttons on the VOCOM control panel pressed simultaneously with the STORE pushbutton. The muting output (MUN) then goes LOW, REM goes LOW and CLK pulses start to increment the internal and external 12-bit counters. The increasing content of the external counter is converted into an analogue staircase function by a resistor-ladder DAC and applied, via a buffer, to an external comparator. The buffered manual tuning voltage is connected to the other input of the comparator. When the staircase waveform from the DAC reaches the same level as the manual tuning voltage, the output from the comparator (ACN) goes LOW, CLK pulses cease and the content of the internal 12-bit counter (digital equivalent of the manual tuning voltage) is stored in the RAM location addressed by the control panel pushbutton. When the conversion is complete, the muting signal (MUN) reverts to the inactive state and the tuning voltage for the radio is now being derived from the DAC.

Making the memory non-volatile

Since the SAA1089 is a LOCMOS circuit, the RAM is volatile and must be supplied from a back-up battery to prevent erasure of its contents during power failure or temporary disconnection of the receiver from the supply. To ensure data retention, the V_{DD} terminal of the SAA1089 must be connected to a supply of at least 3 V (e.g. three NiCd cells). The diode in the supply line prevents the back-up battery discharging through the radio tuner circuits. The series resistor limits the charging current of the battery to about 10 mA at the maximum supply voltage (12.6 V).

Selecting a preset station

To select a preset station, the appropriate numbered station pushbutton on the VOCOM control panel is pressed. This applies a HIGH reset (REM) pulse to the internal and external 12-bit counters and sets the muting output (MUN) LOW. If the radio was previously tuned to a preset station, the electronic switch momentarily reverts to the manual position, but this is of no consequence because the receiver is muted. CLK pulses then increment the internal and external 12-bit counters. The increasing content of the internal counter and the content of the RAM at the addressed location are connected to an internal comparator. When they become equal, the comparator output inhibits further CLK pulses and the muting signal (MUN) reverts to the inactive state. Since the internal and external counters were clocked in unison, the content of the RAM has now, in effect, been transferred to the external counter. This binary number (digital equivalent of the required tuning voltage) is converted into an analogue voltage step by the resistor-ladder DAC and applied, via a buffer and the electronic switch, to the tuning voltage line of the radio tuner.

Operating modes

VOCOM has two basic modes of operation controlled by the state of the MODE input to the SAA1089. When the MODE input is LOW (mode 1), the system provides control of 16 preset stations for a single-waveband radio (mode 1A), or keyboard control of waveband selection and 8 preset stations in each band of a two-waveband radio (mode 1B). When the MODE input is HIGH (mode 2), the system provides control of 8 preset stations in each band of a two-waveband radio in which waveband selection is effected electromechanically instead of via the VOCOM control panel.

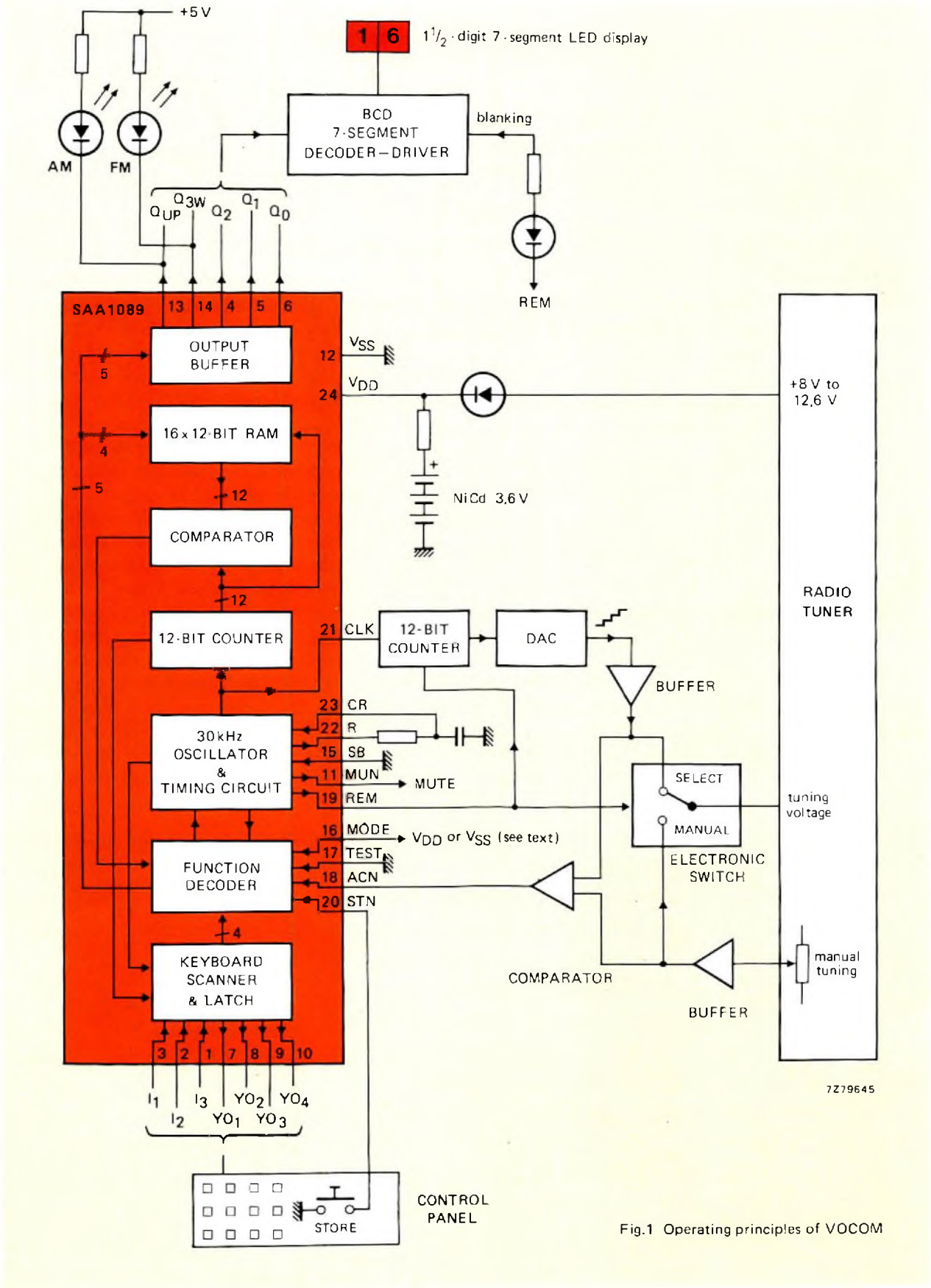


Fig.1 Operating principles of VOCOM

Pushbutton switch scanning

Figure 2 shows that the pushbutton switches on the VOCOM control panel are assembled on a 4 x 3 matrix as follows:

- 8 pushbutton switches (A to H) which address the upper part of the RAM (locations 9 to 16) or the lower part of the RAM (locations 1 to 8) in accordance with commands issued by switches J and K or TOG.
- MAN pushbutton switch which sets the system to manual tuning.
- Pushbutton switch J which routes the commands from switches A to H to the upper part of the RAM (locations 9 to 16).
- Pushbutton switch K which routes the commands from switches A to H to the lower part of the RAM (locations 1 to 8).
- Pushbutton switch TOG (toggle) which can be used instead of switches J and K to select the upper or lower group of locations in the RAM.

The functions of the pushbuttons on the VOCOM control panel for the three modes of system operation are given in the Table.

The three-state scan driver outputs YO_1, YO_2, YO_3 and YO_4 are normally LOW and the command inputs I_1, I_2 and I_3 are normally HIGH. When a pushbutton switch is closed, the resulting current flow causes the 30 kHz oscillator in the SAA1089 to start up. After a pre-determined debounce delay, the scan drive outputs change state one at a time and the resulting command inputs are decoded to detect the closed switch. If more than one switch is closed, only one will be detected because the decoding ensures the following order of priority:

D, C, B, A, H, G, F, E, TOG, K, J, MAN.

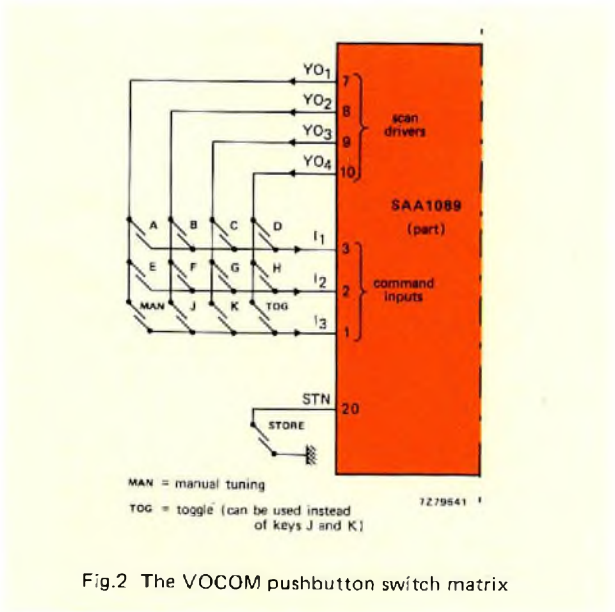


Fig.2 The VOCOM pushbutton switch matrix

APPLICATION INFORMATION

Basic VOCOM system

The circuit diagram of the basic VOCOM system is given in Fig.3. The DAC is formed by a 12-bit counter type HEF4040B with an external R-2R ladder network connected to its outputs. The 12-bit counter is incremented by the CLK pulses from the SAA1089. Since the reset connection of the counter (MR) is active HIGH, it is pulled up to V_{REF} via a 100 kΩ resistor, and held LOW during counting by the REM output from the SAA1089. The ladder network incorporates one additional R-2R section connected between the Q_0 output and the CLK signal. This arrangement allows 13-bit resolution of the counted number of clock pulses so that the output voltage from the DAC during presetting can be defined to within $\pm(V_{DD} - V_{SS})2^{-13}$, where V_{DD} = 8 V to 12.6 V. The output from the DAC is buffered by ¼ LM324 and fed to the input of an analogue voltage comparator type LM211. The manual tuning voltage from the radio is buffered by ¼ LM324 and applied to the other input of the comparator. The output from the comparator is connected to the ACN input of the SAA1089 so that it stops the voltage conversion process when the output from the DAC is equal to the manual tuning voltage from the radio.

Functions of the pushbutton switches shown in Fig.2

pushbutton in Fig.2	mode		
	1A	1B	2
A	1/9	1	1
B	2/10	2	2
C	3/11	3	3
D	4/12	4	4
E	5/13	5	5
F	6/14	6	6
G	7/15	7	7
H	8/16	8	8
MAN	MAN	MAN	MAN
J	UP	AM	not used
K	LOW	FM	not used
TOG	TOG	TOG	not used

MAN = manual
TOG = toggle for use instead of keys J and K

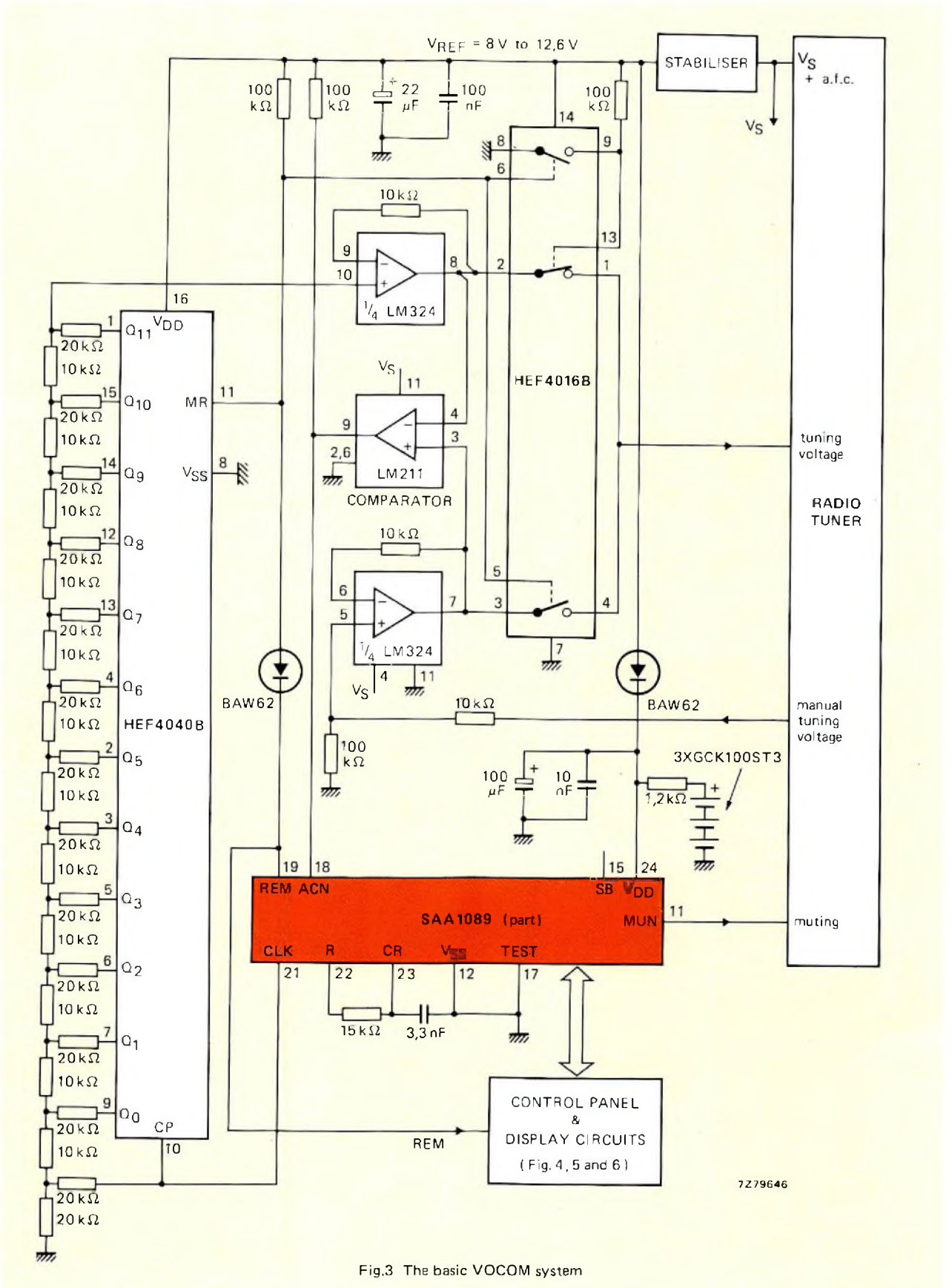


Fig.3 The basic VOCOM system

Three of the four switches in an HEF4016B are used as the electronic switch for changing the system from manual to preset operation. The required single-pole changeover function is achieved by applying the REM signal directly to the control input of the manual tuning voltage switch, and inverting the REM signal with a third switch before it is applied to the control input of the DAC output voltage switch.

The frequency of the oscillator in the SAA1089 is set to 30 kHz by the resistor and capacitor connected to pins 12, 22 and 23. Radiation from the oscillator does not interfere with the radio reception because whilst the oscillator is operational the radio is muted (i.e. during pushbutton switch scanning and voltage conversion).

Station number and waveband displays

The selected RAM address (station number) appears as a 4-bit binary code at outputs Q_0, Q_1, Q_2 and Q_{3W} of the SAA1089. This data is converted into 7-segment format by a BCD to 7-segment decoder/driver and used to drive a LED numeral display of the selected station number. The display is blanked during manual operation by connecting the REM signal to the brightness control input of the decoder/driver. Since the most significant bit of the display data (Q_{3W}) is LOW when the lower part of the RAM (locations 1 to 8) is being addressed, output Q_{3W} is also used to drive a LED indicator showing that a station from the lower group has been selected (mode 1A) or that the f.m. band is in use (mode 1B and mode 2). A fifth bit at output Q_{UP} goes LOW when the upper part of the RAM (locations 9 to 16) is being addressed. This output is used to drive a LED indicator showing that a station from the upper group has been selected (mode 1A) or that the a.m. waveband is in use (mode 1B and mode 2). The waveband data from open-drain outputs Q_{3W} and Q_{UP} are also passed to the radio where they effect the waveband switching in mode 1B operation. In mode 2 operation, Q_{3W} becomes an input which is used to route the keyboard-selected address to the upper or lower part of the RAM without using an additional keyboard switch. This facility allows VOCOM to be used in radios where the waveband switching is electromechanically controlled.

Control panel and display circuits

The VOCOM control panel and display circuits for the three modes of operation are given in Fig.4, 5 and 6. The functions of the display and control panel connections to the SAA1089 are listed in the table opposite.

Receiver put at the disposal of our Application Laboratory by courtesy of Telefunken Fernseh- und Rundfunk G.m.b.H. for incorporation of VOCOM.

Mode 1A (MODE = LOW) — 16 presets for single-waveband radio (Fig.4)

Q_{UP}	Active-LOW output for driving a LED to indicate selection of the upper group of stations (9 to 16).
Q_0, Q_1, Q_2, Q_{3W}	4-bit binary code of selected station number (1 to 16) drives 1½-digit, 7-segment common-cathode LED display via a decoder/driver. This display is blanked whilst the system is set to manual operation. Q_{3W} is also used as an active-LOW output for driving a LED to indicate selection of the lower group of stations (1 to 8).

Mode 1B (MODE = LOW) — 8 presets in each band of a two-waveband radio with waveband selection via VOCOM (Fig.5)

Q_{UP}	Active-LOW output for effecting selection of the a.m. band in the radio and for driving a LED to indicate selection of the a.m. band.
Q_{3W}	Active-LOW output for effecting selection of the f.m. band in the radio and for driving a LED to indicate selection of the f.m. band.
Q_0, Q_1, Q_2	3-bit binary code of selected station number (1 to 8) in the waveband in use. Drives 1-digit, 7-segment common-cathode LED display via a decoder/driver. This display is blanked whilst the system is set to manual operation.

Mode 2 (MODE = HIGH) — 8 presets in each band of a two-waveband radio with waveband selection via mechanical selector in the radio (Fig.6)

Q_{UP}	Active-LOW output for driving a LED to indicate selection of a.m. band.
Q_{3W}	Input from waveband selector in the radio, LOW = f.m., HIGH = a.m. Also used as an active-LOW connection for driving a LED to indicate selection of the f.m. band.
Q_0, Q_1, Q_2	3-bit binary code of selected station number (1 to 8) in the waveband in use. Drives 1-digit, 7-segment common-cathode LED display via a decoder/driver. This display is blanked whilst the system is set to manual operation.

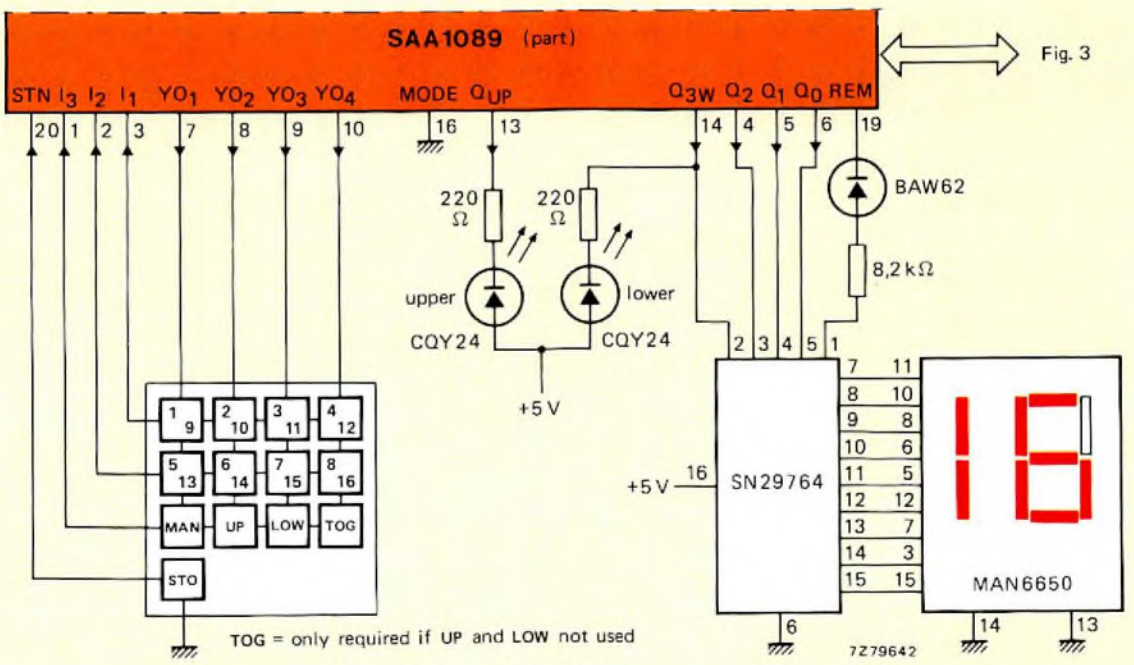


Fig.4 Control panel and display circuit for mode 1A

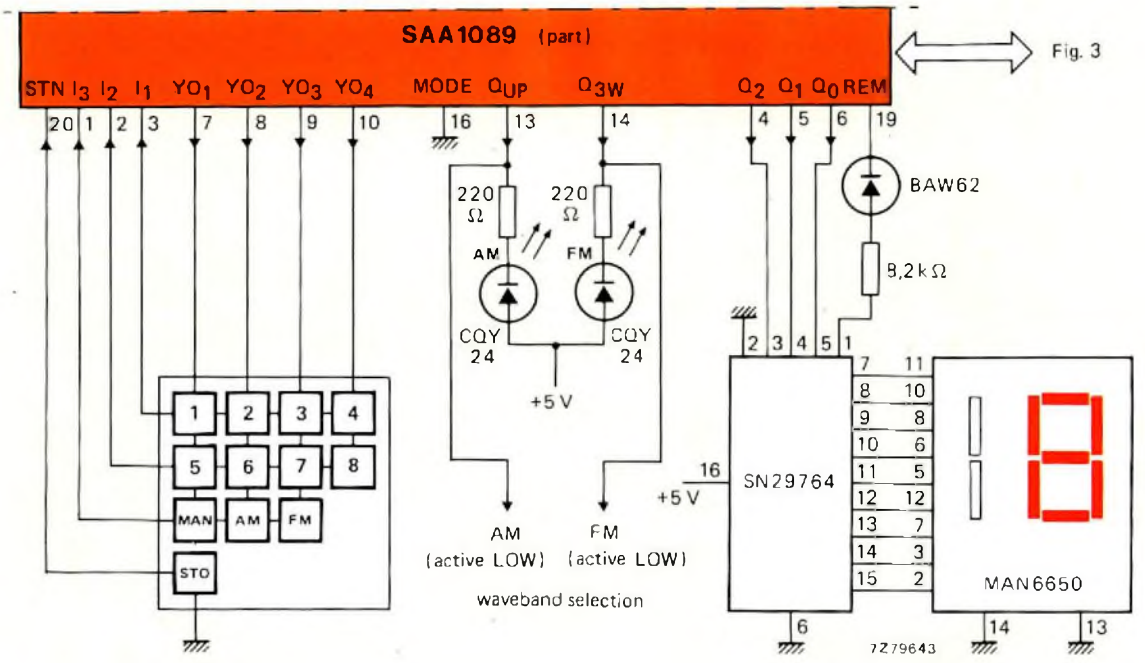


Fig.5 Control panel and display circuit for mode 18

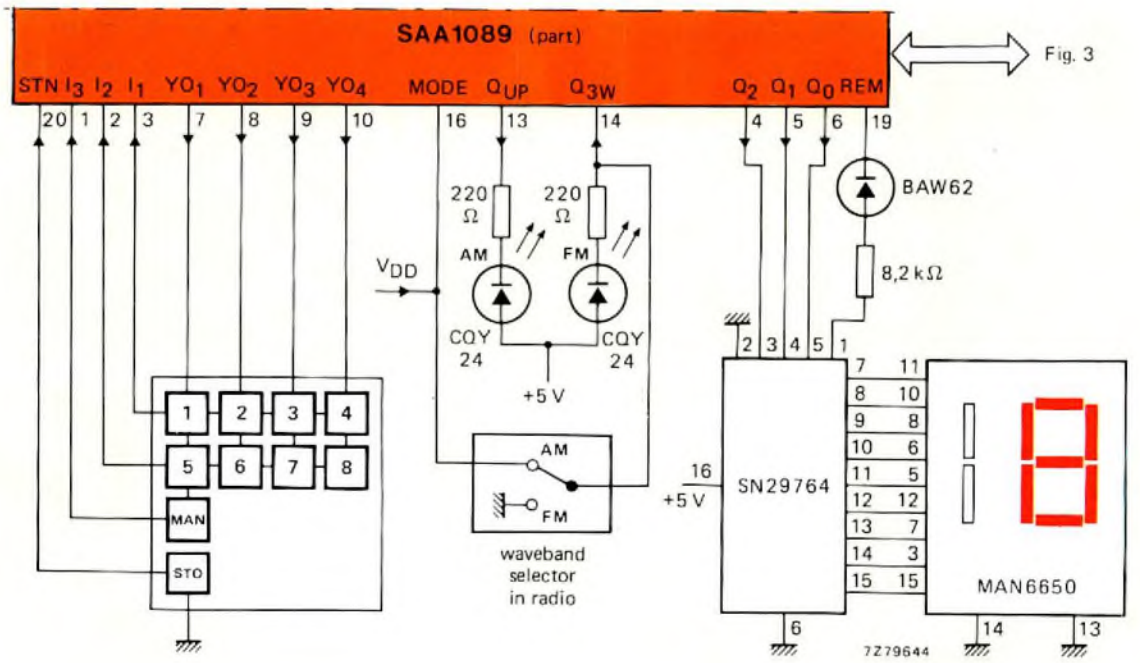


Fig.6 Control panel and display circuit for mode 2

Part 3 - Introduction to microcomputer-controlled radio tuning system

U. SCHILLHOF

LSI technology is now so advanced that the tuning, display and analogue control functions of radio receivers can be economically performed by mass-produced digital LSI circuits. Space-consuming and costly moving parts such as tuning capacitors, dials, meters, multiway switches and potentiometers can therefore be replaced by tiny but highly reliable electronic circuits which are digitally-controlled via a microcomputer. Moreover, digital control allows a receiver to be operated either by calculator-style pushbuttons on the front panel, or from a remote keyboard via an infrared digital data link.

The first two parts of this article described digital circuits which could be added to the r.f. section of a radio. The remaining parts will be devoted to the description of a new Radio Tuning System (RTS) which allows construction of all-electronic radios in which both the r.f. and a.f. sections can be digitally-controlled via a microcomputer.

One of the main advantages of the RTS is its modular construction from a series of LSI circuits, all of which are microcomputer-compatible. This allows a wide variety of control systems to be constructed to suit the individual requirements of manufacturers or different classes of equipment. This is illustrated by Fig.1 which shows a simple RTS, and Fig.2 which shows a more comprehensive system.

For the purpose of this description, the RTS will be divided into the following sections:

- tuning control with a frequency synthesiser,
- control of display and analogue functions,
- user controls and the microcomputer.

The first of these subjects is described in this issue. The other two will be described in future issues.

TUNING BY DIGITAL-CONTROLLED INDIRECT FREQUENCY SYNTHESIS

In the RTS, a phase-locked loop (PLL) maintains stable, accurate tuning in either the a.m. or f.m. broadcast bands. The local-oscillator signal from the tuner is passed to a frequency divider with a programmable division ratio. The output from the divider is compared with a stable reference frequency. The output of the comparator is then amplified and filtered before being used as the control voltage for the local-oscillator, thereby completing the control loop. The user changes the tuned frequency by keying-in the required broadcast frequency, which is converted into the appropriate division ratio by a microcomputer.

Additional features such as search tuning, manual tuning and station memory can easily be added to the system.

The components of the RTS associated with tuning control are:

SAA1059 A high sensitivity input preamplifier and dual-ratio frequency divider which can be connected to any local-oscillator via passive components.

SAA1056 A phase-locked loop frequency synthesiser which can be directly programmed with the binary-coded division ratio which is necessary to reduce the local-oscillator frequency for comparison with the reference frequency. The reference frequency generator in the SAA1056 can be programmed to achieve a tuning steps of 25 kHz, or 10 kHz for f.m., 5 kHz or 500 Hz for a.m.

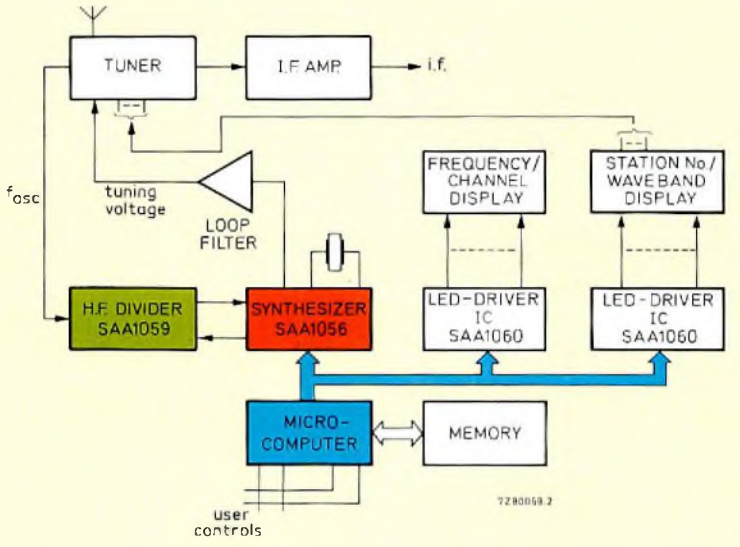


Fig.1 A simple RTS

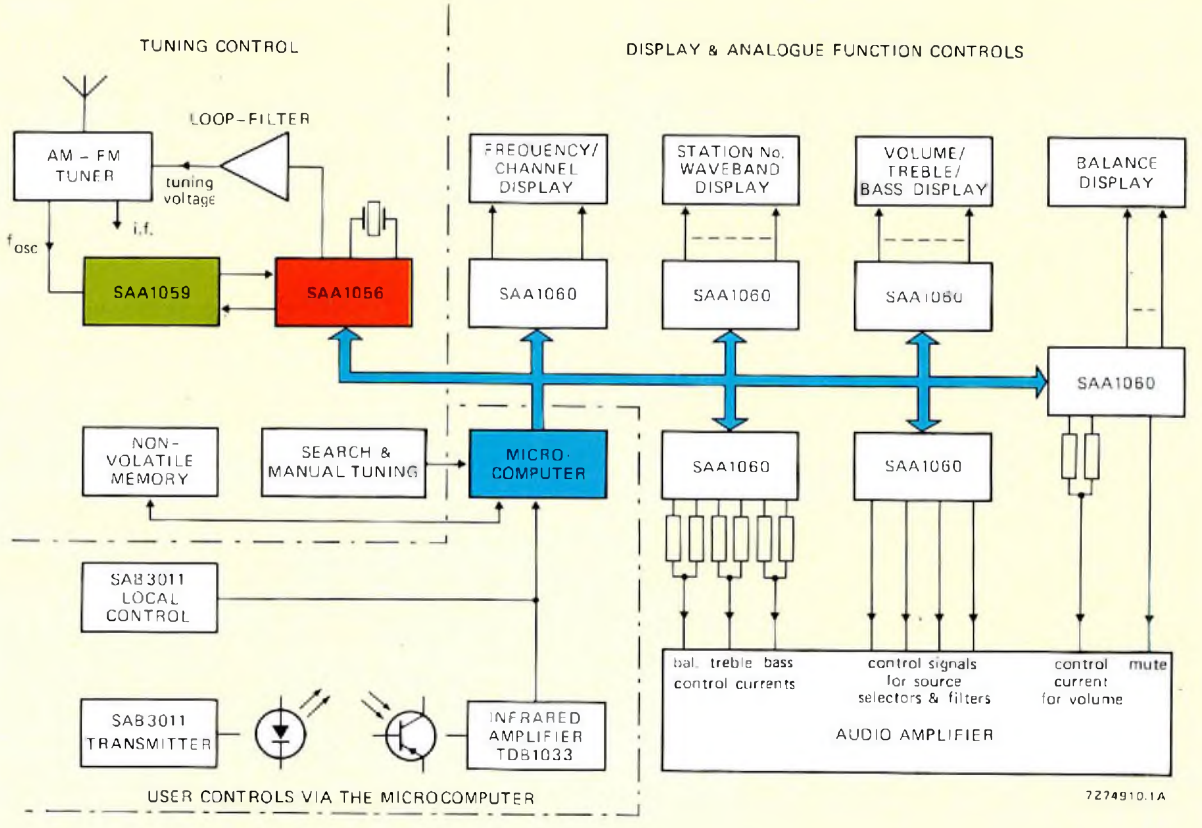


Fig.2 A comprehensive RTS

To support the tuning control section of the RTS, we have also developed a dual variable-capacitance diode type BB212 for a.m. tuning, and an a.m. band-switching diode type BB223. The BB212 will be described in a future issue.

Operating principles of frequency synthesis

A basic digitally-controlled PLL for radio tuning is shown in Fig.3. Each cycle of the signal from the voltage-controlled local-oscillator (VCO) decrements a preset counter so that it generates one output pulse for every N oscillator cycles. The resulting pulse train is applied to one input of a phase comparator. A pulse train from a crystal-controlled reference frequency generator is applied to the other input of the phase comparator. The phase comparator output, which is proportional to the relative phase of the two input signals, is passed through a low-pass loop filter to remove the high-frequency components and fed back to the VCO as the tuning control voltage. The loop is locked when:

$$f_{osc} = Nf_{ref}$$

It is apparent from this expression that the smallest increment by which the VCO frequency can be changed (tuning step) is f_{ref}. The reference frequency must therefore be low enough to achieve the required tuning accuracy. Unfortunately, however, the following restrictions limit the practical minimum value for f_{ref}.

- Conversion of the phase comparator output into the VCO control voltage is one of the most important processes in the digital PLL because any high-frequency variation of the tuning voltage will phase-modulate the VCO. The reference frequency must therfore be high enough to allow it to be adequately filtered out before it can reach the control input of the VCO.
- The time taken to change from one tuned frequency to another (acquisition time) is an inverse function of the loop bandwidth. Since the loop bandwidth is always narrower than f_{ref}, a short acquisition time necessitates a high reference frequency.

It is therefore essential that the reference frequency and loop filter parameters are optimum for the required frequency range of the PLL. At least two reference frequencies are required if the PLL is to be selective enough for use in a two-band radio. Typical tuning steps for a moderate performance receiver are 500 Hz for long and medium waves, 5 kHz for short-waves and 25 kHz for f.m. Higher performance f.m. receivers may require a reference frequency as low as 10 kHz. Or, in some rare cases, 5 kHz. A multi-ratio presettable divide-by-N_r counter is therefore interposed between the reference

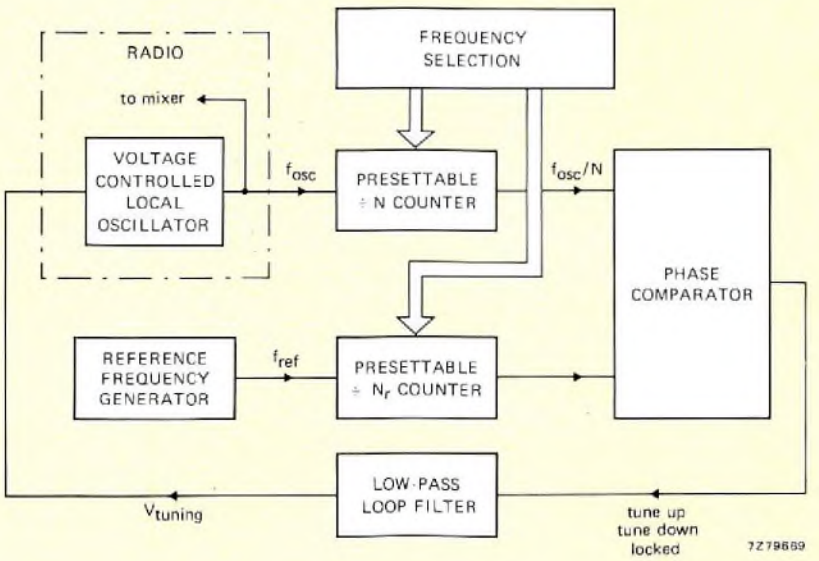


Fig.3 Basic digital phase-locked loop

frequency generator and the phase comparator. The required division ratio for the divide-by-N counter will then be:

$$N = \frac{f_{osc} N_r}{f_{ref}}$$

The highest ratio is required when the reference frequency is 5 kHz and the radio is tuned to the highest frequency in the f.m. band (108 MHz). In this case, the local-oscillator would have to be tuned to:

$$f_{osc} = f_{tuning} + f_{if} = 108 + 10.7 = 118.7 \text{ MHz}$$

The divide-by-N counter would have to be preset to:

$$N = \frac{118.7}{0.005} = 23740$$

The lowest ratio is required when the reference frequency is 500 Hz and the radio is tuned to the lowest frequency in the long-wave band (150 kHz). In this case, the local-oscillator would have to be tuned to:

$$f_{osc} = f_{tuning} + f_{if} = 150 + 450 = 600 \text{ kHz}$$

The divide-by-N counter would have to be preset to:

$$N = \frac{600}{0.5} = 1200$$

It is not practical to integrate conventional cascaded counters which can operate at speeds between 600 kHz and 118.7 MHz and can be preset to divide by any integer between 1200 and 23740. We have therefore designed an integrated digitally-controlled frequency divider that uses a technique known as 'pulse swallowing' to achieve the required performance.

The pulse swallowing frequency divider principle

The operating principles of the variable-ratio pulse swallowing frequency divider will be explained with the aid of Fig.4 and Fig.5.

The high-frequency two-ratio prescaler divides the frequency of the local-oscillator signal f_{osc} by either the upper ratio $N_U = 33$ or the lower ratio $N_L = 32$. The division ratio is controlled by the CMOD signal generated by the swallow counter. The swallow and program counters are preset to N_S and N_P respectively by two frequency-control data words derived from a microcomputer which computes the required ratio from the frequency keyed-in by the user. The frequency-control data words are stored in a latch. The two counters therefore count down from the preset numbers (N_S for the swallow counter and N_P for the program counter) to zero. Initially, the ratio control signal CMOD is HIGH and the prescaler divides by 33. When the swallow counter reaches zero, CMOD goes LOW, the prescaler division ratio changes to $N_L = 32$ and the swallow counter is inhibited from further counting. The program counter continues to count down to zero, at which time an output pulse is generated. The swallow and program counters are then reloaded with N_S and N_P respectively and the cycle repeats.

The equation describing the operation of the circuit is:

$$\frac{f_{osc}}{N} = \frac{f_{osc}}{N_U N_S + N_L(N_P - N_S)}$$

Inserting values for N_L and N_U and solving for N gives:

$$N = 33N_S + 32(N_P - N_S)$$

From this expression, it is obvious that the term $N_P - N_S$ must always be zero or positive. A condition of operation of the swallow counter is therefore $N_P \geq N_S$. The expression for N can be simplified to:

$$N = N_S + 32N_P$$

If all the possible integers of the division ratio are to be defined, it must be possible to step N_S through all values from 0 to 31 before changing the value of $32N_P$.

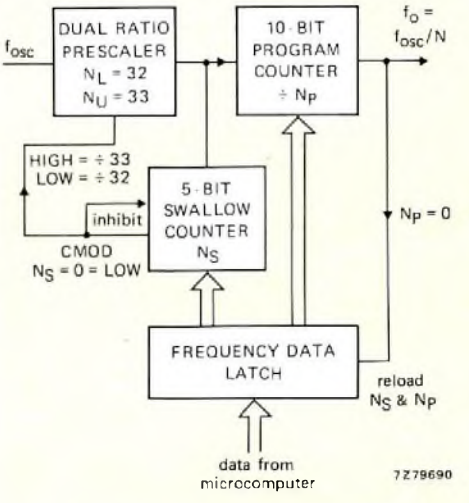


Fig.4 Pulse swallowing frequency divider

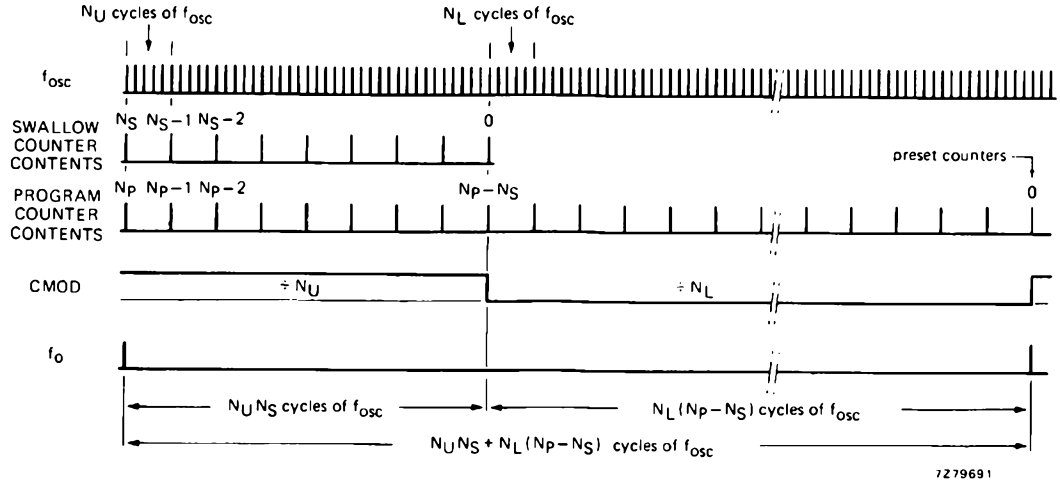


Fig.5 Operating principle of the swallow counter

To satisfy the condition $N_P \geqslant N_S$ during all the steps of N_S, the minimum value for N_P is 31. Since the program counter has a capacity of ten bits, the maximum value for N_P is $2^{10} - 1 = 1023$. The maximum and minimum division ratios are therefore:

$$N_{max} = N_{S\,max} + 32N_{P\,max}$$
$$= 31 + (32 \times 1023) = 32767$$

$$N_{min} = N_{S\,min} + 32N_{P\,min}$$
$$= 0 + (32 \times 31) = 992$$

The range of division ratios previously quoted as being necessary for tuning an a.m./f.m. radio (1200 to 23740) can therefore all defined.

Since multiplying or dividing by 32 in binary arithmetic is simply a matter of shifting the bits of the binary number five places to the left or right, it is very simple to programme the required division ratio for the swallow counter. This is best explained with numerical example. Assume a required division ratio of 9830. The 15-bit binary equivalent of this number is:

2^{14} 2^5 2^0

N = 0 1 0 0 1 1 0 0 1 1 0 0 1 1 0 = 9830

| 32Np | N_S |

The five least significant bits of the binary number are N_S:

2^4 2^0

N_S = 0 0 1 1 0 = 6

The ten most significant bits are 32Np:

2^{14} 2^5

32Np = 0 1 0 0 1 1 0 0 1 1 = 9824

Shifting the binary number for 32Np five places to the right (dividing by 32) gives Np:

2^9 2^0

Np = 0 1 0 0 1 1 0 0 1 1 = 307

The decimal numbers for N_P and N_S can be derived as follows:

Divide the required ratio by 32:

$$\frac{9830}{32} = 307.1875$$

The integral part of the result is Np = 307.

Multiplying the fractional part of the result by 32 gives $N_S = 0.1875 \times 32 = 6$.

The main advantage of this type of wide range presettable divider is that it requires only one high speed dual-ratio prescaler. The remaining circuitry operates at 1/32 or 1/33 of the local oscillator frequency. This reduces cost, saves power and allows more flexibility for circuit layout. Furthermore, since the lower ratio of the prescaler (32) is a power of 2, the counters can be directly programmed with the binary number representing the required overall division ratio. The ten most significant bits of the number address the Np counter; the five least significant bits address the N_S counter.

THE PRACTICAL FREQUENCY SYNTHESISER OF THE RTS

The microcomputer-controlled indirect digital frequency synthesiser previously described could be constructed from standard integrated logic circuits. Such a synthesiser would however be costly and would consume a lot of space and power. We have therefore integrated the high-speed divide-by-32/33 circuit on one chip (SAA1059), and the remainder of the lower-speed synthesiser circuits for the RTS on a second chip (SAA1056) as shown in Fig.6.

Programmable pre-scaler SAA1059

The SAA1059 is a multi-stage divider with an externally selectable division ratio of 32:1 or 33:1. Figure 7 is a simplified functional block diagram of the circuit.

The preamplifier ensures a high input sensitivity so that the signals from the local-oscillators in the radio can be connected to the RTS via passive coupling networks. The a.m. and f.m. local-oscillators can be simultaneously connected to the symmetrical inputs of the preamplifier without an input filter or a switch, provided that the unused oscillator is switched off in the radio. The pre-scaler incorporates two symmetrical output stages, one of which has open-emitter outputs and the other, open-collector outputs. Since the SAA1056 reacts to the trailing edges of the drive signal, open-collector output Q_{OC} is used in this application. Each of the four internal functional blocks has its own supply pin; pin 3 for V_{CC1} to the input preamplifier, pin 14 for V_{CC2} to the synchronising stage, pin 12 for V_{CC3} to the divider, and pin 10 for V_{CC4} to the output stages.

A timing diagram for the circuit is given in Fig.8. This diagram shows that the output signal Q_{OC} consists of a positive transition for every 32 or 33 input cycles (dependent on the state of count mode input CM33) and a negative transition 17 input cycles after each positive transition. The delay between the swallow counter in the SAA1056 receiving the required number of Q_{OC} positive transitions, and the change of division ratio from 32:1 to 33:1 must be less than the period of

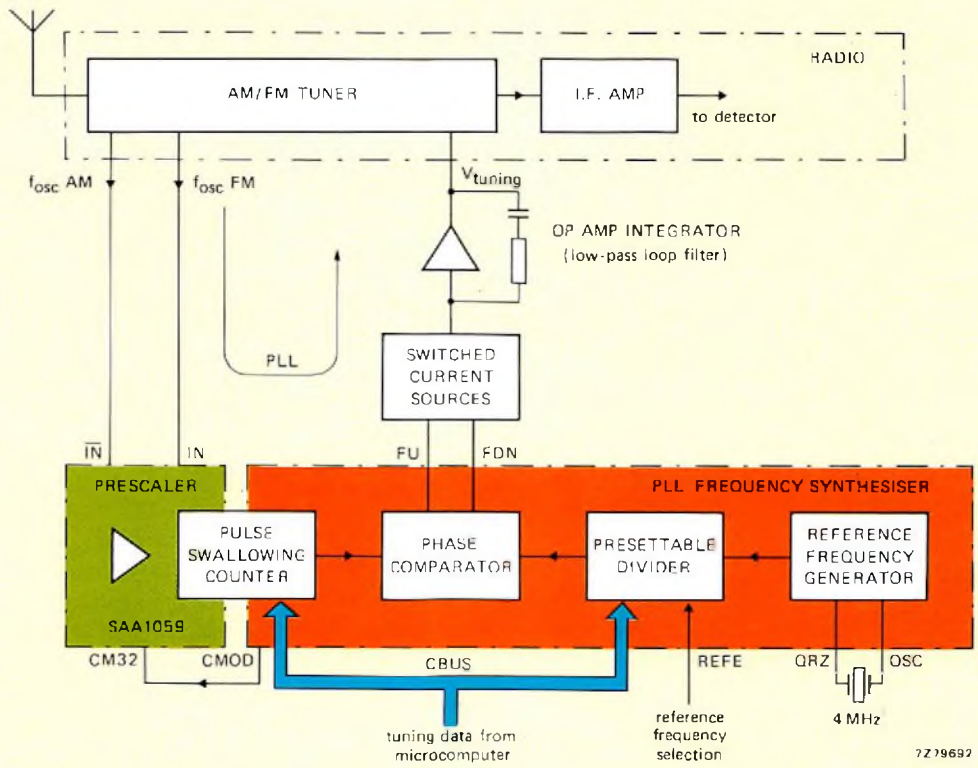


Fig.6 The RTS frequency synthesiser

one cycle (T) at output Q_{OC}. With the highest permitted input frequency (125 MHz), the period of the Q_{OC} output signal when dividing by 32 will be:

$$T = \frac{32}{125 \times 10^6} = 256 \text{ ns}$$

The typical set-up time (t_{su}) between receiving and executing command CM33 is 50 ns. The maximum allowable delay (t_d) between the swallow counter in the SAA1056 receiving the required number of Q_{OC} positive transitions and the issuance of command CMOD = CM33 is therefore:

$$t_{d\,max} = T - t_{su} = 256 - 50 = 206 \text{ ns}$$

The maximum delay specified for the SAA1056 is 150 ns.

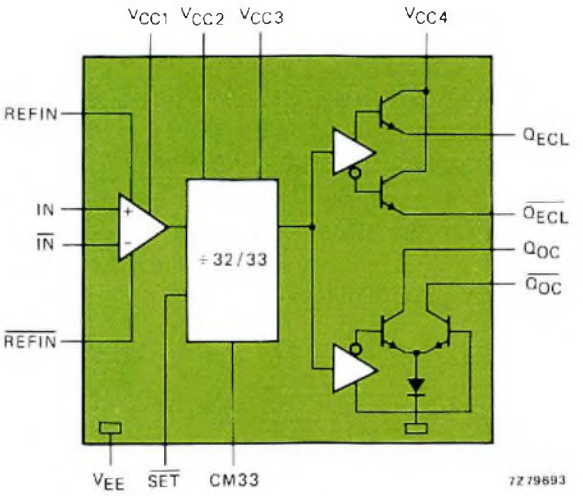


Fig.7 125 MHz programmable prescaler SAA1059

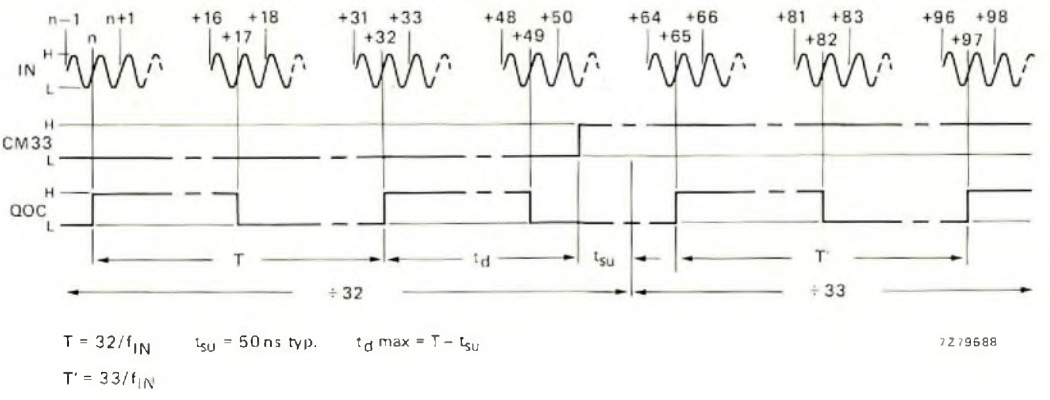


Fig.8 Timing diagram for the SAA1059 changing from ÷32 to ÷33 after a count of n + 32

PLL frequency synthesiser SAA1056

A functional block diagram of the PLL frequency synthesiser SAA1056 is given in Fig.9. The phase-locked loop tuning function of the upper five blocks shown in the diagram has already been explained. The functions of the remaining blocks will now be described.

The serial computer bus (CBUS) data comprises a 15-bit division ratio command word preceded by a reference-frequency defining bit and a leading zero on the DATA line, a data line enable (DLEN) signal and a train of clock pulse (CLB). Figure 10 shows the CBUS commanding a division ratio of:

$$N = 32N_P + N_S = (32 \times 307) + 6 = 9830$$

If the leading zero is present and DLEN is HIGH, the bus control circuit allows the data to be serially clocked into the shift register in synchronism with the falling edges of the CLB clock pulses. If sixteen bits of data have been received, DLEN goes LOW and the next clock pulse loads the data, together with externally applied reference-frequency bit REFE, into the 17-bit latch.

The single data bit (REFI) preceding the 15-bit division ratio command word and the externally applied REFE bit define the reference frequency divider ratio as follows:

REFI	REFE	Reference frequency divider ratio
1	1	160:1
1	0	400:1
0	1	800:1
0	0	8000:1

The required ratio for the reference-frequency divider is decoded and presented to the reference-frequency divider as 13 data bits. With the reference oscillator controlled by a 4 MHz crystal connected between QRZ and OSC, this results in a choice of reference frequencies as follows:

REFI	REFE	Reference frequency
1	1	25 kHz
1	0	10 kHz
0	1	5 kHz
0	0	500 Hz

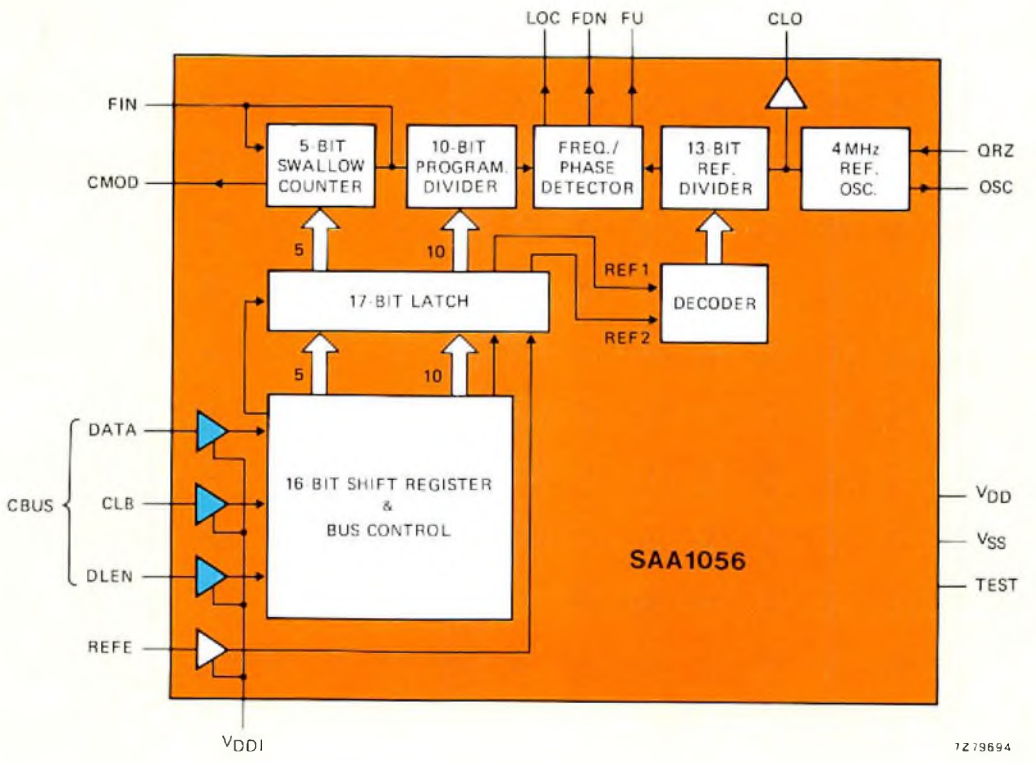


Fig.9 Functional block diagram of the PLL frequency synthesiser SAA1056

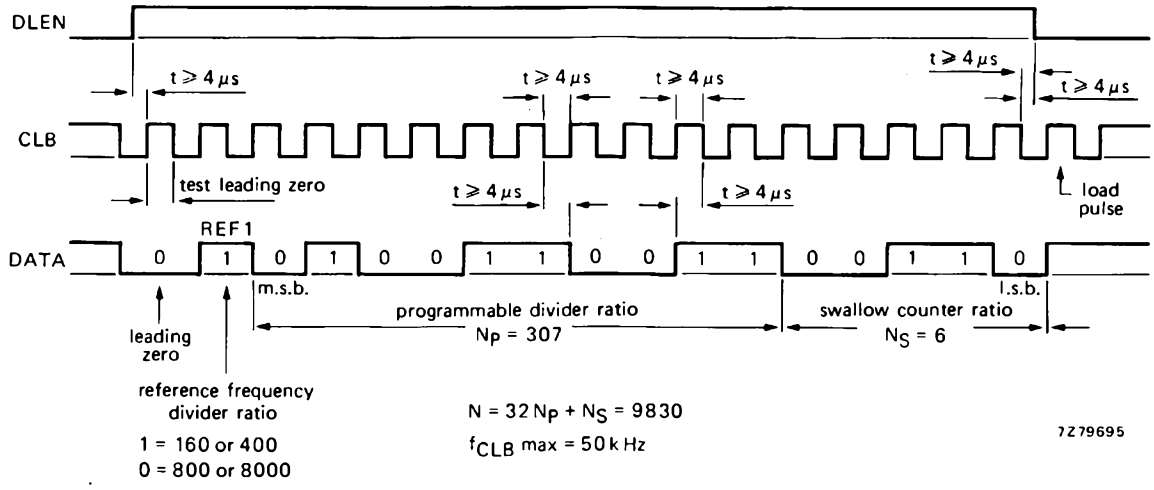


Fig.10 CBUS data to SAA1056 to define a division ratio of 9830:1 and a reference divider ratio of 160:1 or 400:1

One of the two higher frequencies is used for f.m. tuning; the 5 kHz reference frequency is for s.w. tuning. The 500 Hz reference frequency is for l.w. and m.w. tuning. The undivided output from the 4 MHz crystal-controlled oscillator is available at output CLO for deriving clock pulses for the CBUS if they are not available from the microcomputer.

The three CBUS inputs and the REFE input are connected to internal level shifters so that external interface circuits are not required between the SAA1056 (V_{DD} = 9 V) and the other RTS integrated circuits that have a 5 V supply.

Circuit interconnections

Figure 11 shows the SAA1059 and the SAA1056 interconnected in a practical digital frequency synthesiser. The width-modulated output pulses FU and FDN from the phase detector in the SAA1056 are used to switch current-sources which drive an active integrator (low-pass filter) to derive the tuning voltage.

If preset stations are required, the tuning data from the CBUS can be stored in a non-volatile memory (MNOS or CMOS with battery back-up).

Search tuning can also be incorporated in the RTS via the microcomputer. Such a system can be made to be selective so that it only responds to stereo broadcasts and/or stations above a certain signal strength.

The main features of the circuit in Fig.11 are:

- PLL tuning with crystal-controlled stability.
- Minimum wiring between ICs due to serial data transport and internal data format control.
- Simple passive coupling network between the receiver local-oscillators and the prescaler.
- Programmable reference frequency (minimum tuning step).
- Few peripheral components.

ACKNOWLEDGEMENT

The author wishes to thank the many engineers of the Valvo Application Laboratory in Hamburg for their contribution to the development of the RTS system described in this article.

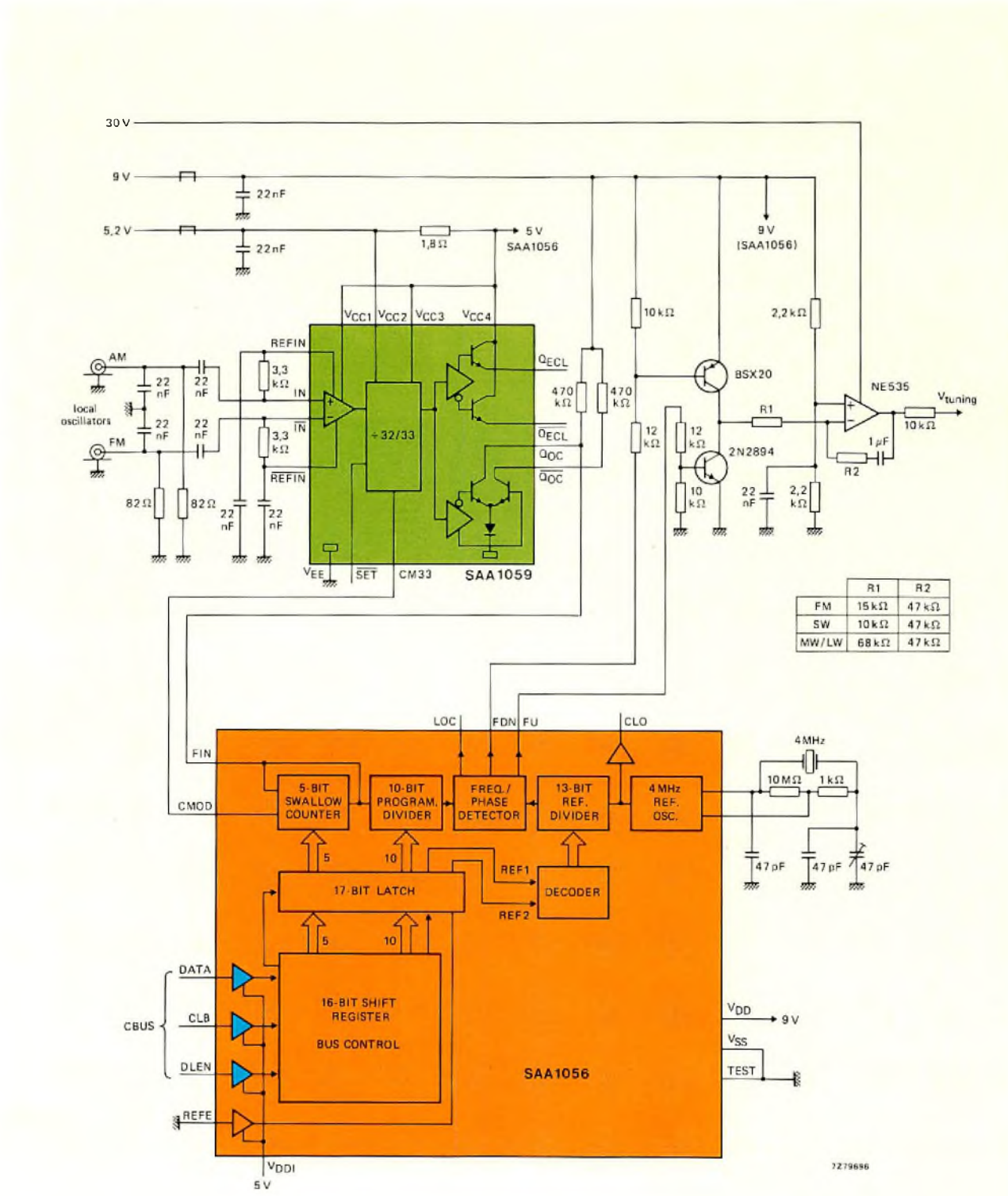


Fig.11 A practical digital frequency synthesiser

The 8X300 development and monitoring system (DMS)

E.D. van VELDHUIZEN

INTRODUCTION

All microcomputer systems consist of hardware and software. Generally, when designing a new system, a hardware prototype can be developed from a knowledge of the functional requirements of the system and the specification of the microprocessor selected. At the same time, the necessary software can be written. However, the software cannot be fully tested until the hardware is complete while, conversely, the hardware cannot be fully debugged until the system is finalised. To assist in the design of a new system, therefore, the engineer depends heavily on special development aids which enable him to develop and debug both software and hardware with the minimum cost in terms of time and effort. It is essential that development times are minimised to ensure a fast response to rapidly changing market requirements.

The 8X300 Development and Monitoring System (DMS) described in this article is a complete system intended specifically to assist in the design of systems using the 8X300 high-speed bipolar microprocessor. It provides the user with all the facilities for source code editing, program assembly, debugging, and for the production of final PROM programming tape.

THE 8X300

The 8X300 microprocessor is a fast bipolar device designed especially for high-speed real-time control applications; it has been fully described in an earlier article (Ref.1) but its main features are summarised below.

- 250 ns instruction cycle time
- eight general-purpose registers
- on-chip oscillator
- three-bus architecture:
  - address (13-bit)
  - instruction (16-bit)
  - data (8 bit tri-state)
- static operation
- low-power Schottky technology
- single +5 V supply

The architecture of the 8X300 is shown in Fig.1.

DEVELOPMENT OF AN 8X300 SYSTEM USING DMS

Fig.2 shows typical stages in the development of a microcomputer system, using the 8X300 DMS. As mentioned earlier, the hardware is based on the system requirements and the 8X300 characteristics. On the software side, a program is first written to enable a source tape to be produced and edited by means of the DMS. This source program is then translated by the assembler, and an object code tape, together with a listing, is produced. Any errors in the source code indicated by the assembler can be corrected by means of the DMS line-edit facility. With the hardware prototype connected to the DMS, the object code on paper tape is loaded into the RAM in the DMS, which acts as a program store for the system under development. The program is then executed by

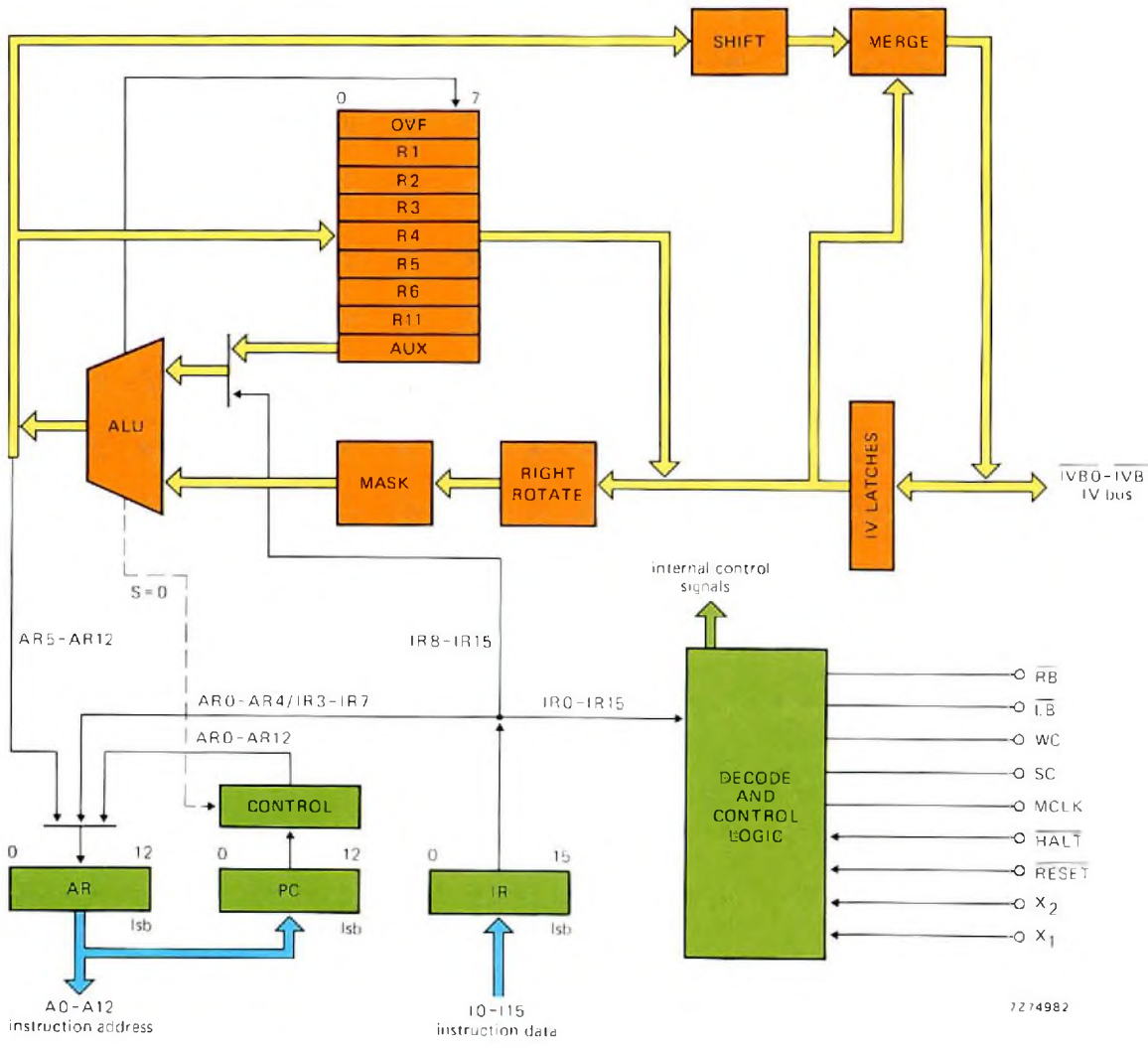


Fig.1 8X300 architecture

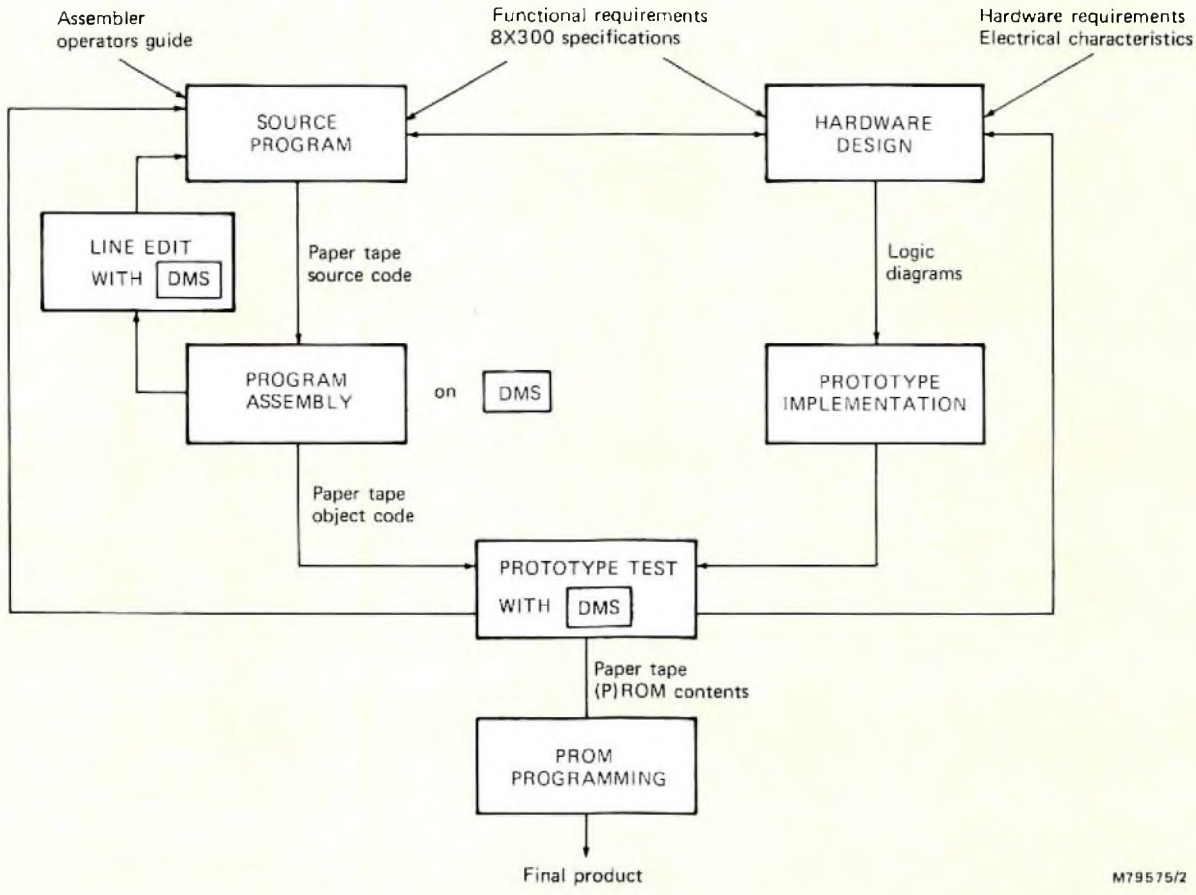


Fig.2 Typical stages in the development of an 8X300 system using the DMS

the prototype system and errors can be traced using the debugging facilities of the DMS; these include:

- run/single step instruction
- stop on breakpoint
- address trace
- display of contents of 8X300 registers and IV-bytes
- program dump.

When errors have been corrected, possibly by modifying the source code or hardware (or both), and the program runs correctly, the contents of the DMS RAM can be punched out in a format suitable for a PROM programmer. In this way, a PROM program tape is produced which can be used to create correctly programmed PROMs for insertion in production models of the system.

THE DMS SYSTEM

Most microcomputer development systems emulate the microprocessor used in the system being developed. However, in 8X300 systems, this approach would be extremely difficult, if not impossible, because of the relatively high speed of this microprocessor. The DMS therefore is designed to operate using the 'real' 8X300 in the prototype system. This offers the advantage that there are no differences in timing between the prototype operating alone and its operation when connected to the DMS.

Specific hardware (MSI TTL) monitors the actions of the 8X300 while the program being debugged is running. It compares addresses with that stored in the breakpoint register, traces addresses, stores the left-bank and right-bank IV-byte addresses, and controls the run,

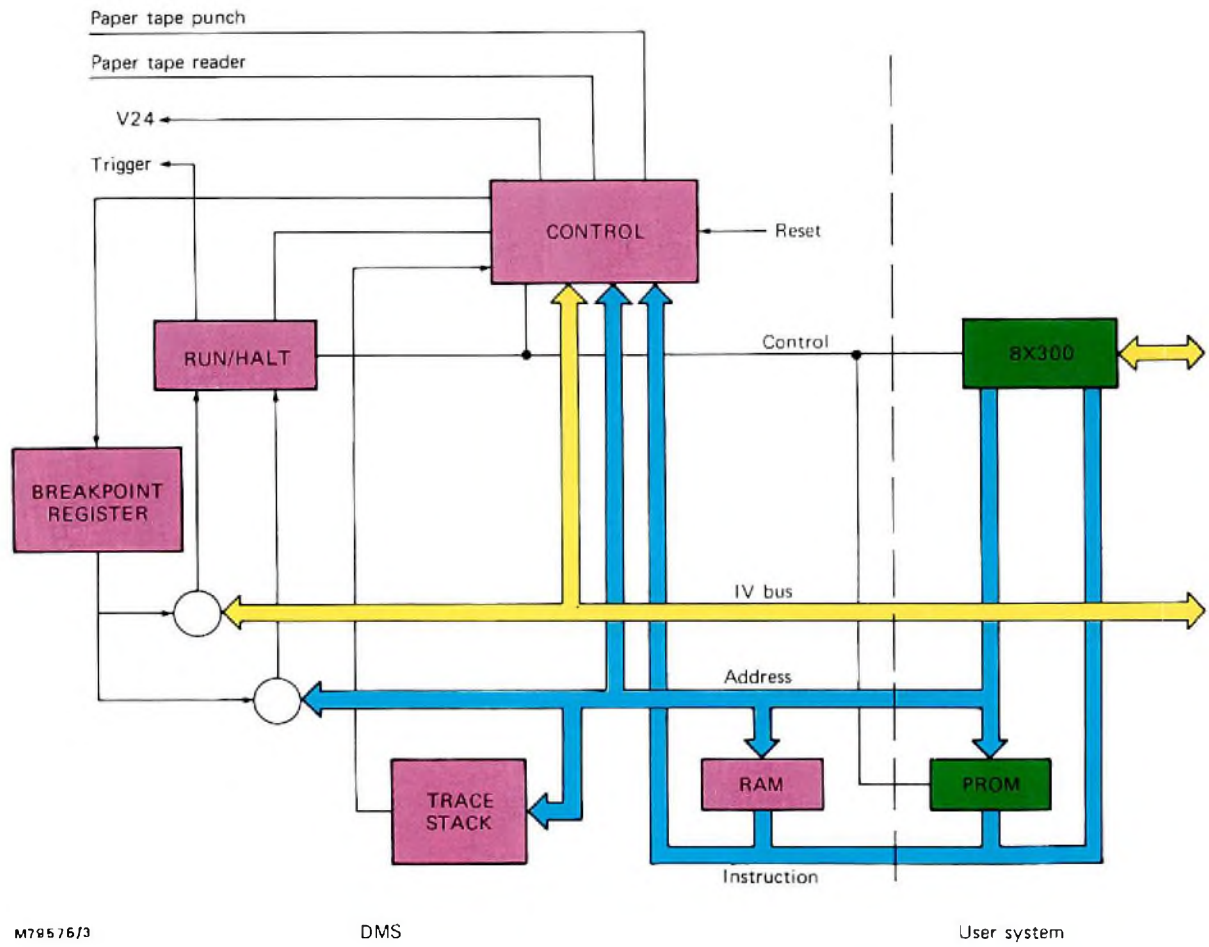


Fig.3 Functional diagram of DMS

halt, and single-step functions. All other control functions are performed by a Signetics 2650 microprocessor which executes operator commands and interfaces with the operator's communicating device via a V24 (RS232) interface or a 20 mA current loop serial interface. It also accesses the DMS RAM for program loading and modification; forces instructions on the 8X300 instruction bus to allow examination of the 8X300 internal registers and IV-bytes; stores and restores IV-byte addresses; and controls high-speed paper tape equipment.

DMS block diagram

Fig.3 shows the functional diagram of the 8X300 DMS. The RAM contains the program to be executed by the user's 8X300 system. (Note, however, that when using the DMS to test a non-prototype system, the 8X300 can also execute the program stored in the memory of that system.) When the program in the RAM has been finalised, the contents can be punched out on paper tape in a form suitable for a PROM programmer.

The trace stack is continuously loaded with the addresses of the last 15 instructions to have been executed. The addresses are written into the stack during full-speed running of the program. When the system is halted, the stack can be read and its contents displayed on a 'last-in first-out' basis.

The breakpoint register can be loaded with either an instruction address or an IV-byte address. When the contents of this register match the instruction address (or IV-byte address) in the program run, the run/halt circuitry will stop the 8X300 and/or provide a trigger

pulse. The trigger pulse is particularly useful when dealing with timing problems, and can be used to trigger counters or oscilloscopes. The run/halt circuitry will also perform in the single-step mode.

The user communicates with the DMS via a Teletype or VDU connected to the V24 interface. Further input/output connections are provided for high-speed paper tape punch and reader equipment.

The control section of the DMS governs the internal operation of the system. It controls the loading of the RAM, and interfaces with the operator's communication device and paper tape equipment.

Hardware and connections

The DMS is built on extended double Eurocard (220 X 233 mm) and can be conveniently mounted in a standard Eurocard rack. It provides all the control functions together with 1 K of RAM for the user's 8X300 program. It has been found that this amount of program storage is sufficient for most applications, but storage can be extended by the addition of an option card giving an additional 3 K of user RAM. This option card also carries the DMS assembler program in ROM (see later). The DMS operates from a single +5 V supply, although ±12 V supplies are required if the V24 interface is to be used.

Fig.4 is a schematic diagram of the DMS connected to its input/output peripherals and an 8X300 system under development. Connection to the operator's communication device is via a V24 or 20 mA current loop serial interface. A Teletype (providing keyboard input and printer output, as well as paper tape input and output) or a VDU terminal can be used, and one of four baud rates (110, 300, 600, or 1200) selected. A separate interface for high-speed punch and reader equipment is provided; this is particularly useful when a VDU is being used as the communicating device.

The connections between the DMS and the prototype system carry all the 8X300 interface signals: the instruction bus, address bus, IV bus, and control signals. In addition, a PROM-enable signal and possibly a user-halt signal, are required.

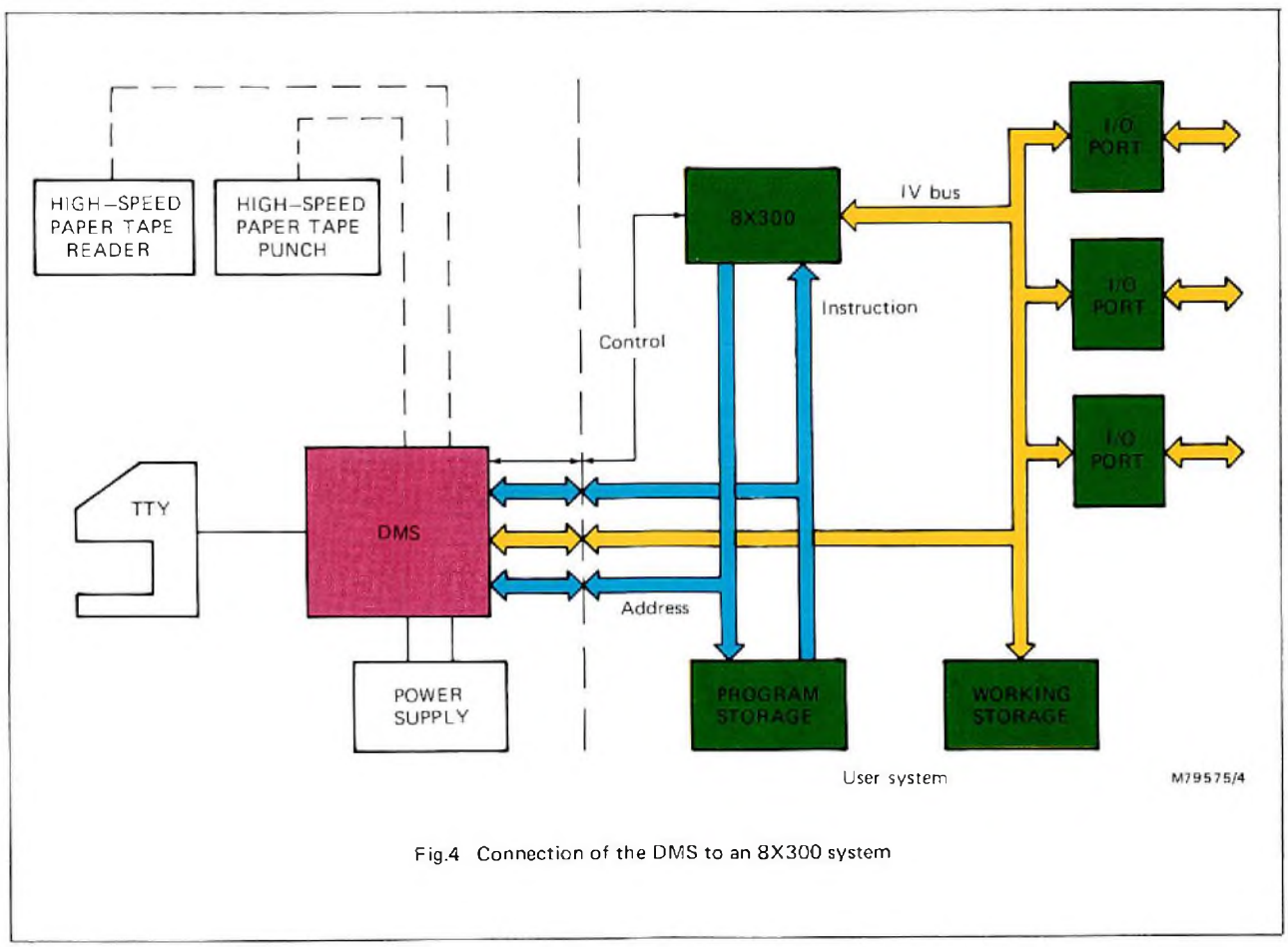


Fig.4 Connection of the DMS to an 8X300 system

DMS COMMAND SET

The DMS operates under the control of its ROM-resident monitor program which recognises a comprehensive set of commands from the operator. The command set is given in Table 1 and is divided into functional groups for use at different stages during the development of the system. Commands are entered via the operator's keyboard, each being followed by a CR (carriage-return) or LF (line-feed) character to indicate single-step or repeat execution. The DMS must be in the Wait state before commands are entered except for a small number of specific commands, such as Halt.

Load RAM

The DMS RAM can be loaded from a keyboard, Teletype tape reader, high-speed reader, or from the 8X300 system PROM. The program loaded can then be executed by the 8X300 system under test.

Edit

Assembly language source code can be entered and punched line-by-line on to paper tape. Existing source code tape can be read, edited from the keyboard, and new tapes generated.

Assemble

The source code tape generated during the Edit function can be read and the program assembled. The assembler will indicate the presence of any syntax errors, provide a listing of the source, and generate corresponding object code. The assembled object code is placed in the DMS RAM where it can either be executed or transferred to paper tape.

Alter

The contents of the RAM, and the 8X300 registers or IV bytes, can be examined and, if required, altered via the keyboard.

Breakpoint

A breakpoint can be set at which execution of the program is halted when a specific program or IV-byte address is reached. When the system halts, the data specified by the last Halt Display command is displayed. Alternatively, a trigger output can be requested, in which case the system does not halt.

Trace

When execution of the program is halted, entry of the Trace command causes the contents of the trace stack to be displayed; that is, the addresses of the last 15 instructions to have been executed.

Display

The contents of the RAM or the IV bytes can be displayed.

Halt Display

This defines the registers and/or IV bytes whose contents are to be displayed when the system is halted. Other commands in this group cause the system to ignore halts in the user-system, or to halt the system immediately.

Program switch

The operator can direct the system to execute either the program in the user PROM or that in the DMS RAM.

Start execution

Program execution can be started from any address in the program memory in either the single-step or run mode.

Dump program

The contents of the RAM can be punched out on either Teletype or high-speed punch equipment.

Generate PROM tape

The contents of the RAM can be punched on tape in one of three formats suitable for a PROM programmer.

Verify PROM tape

The tape generated for the PROM programmer can be read and compared with the contents of the DMS RAM to verify its accuracy.

Command source allocation

A command can be given at any time, directing the DMS to accept commands either from a tape input or from the keyboard.

Self-test

Commands are provided for checking the interface to the 8X300 system and to aid debugging of the DMS.

Fig.5 shows the print-out of a typical debugging run for a small program (the output device is a Teletype). The print-out is annotated to allow the reader to follow the program through. When debugging is complete, a PROM programming tape can be punched and verified against the contents of the DMS RAM.

TABLE 1

DMS command list

AI aaaaa **CR/LF,LF**	alter instruction/step address
AL aaa **CR/LF,LF**	alter left bank data/step address
AR aaa **CR/LF,LF**	alter right bank data/step address
AX aa **CR/LF,LF**	alter register data/step address
BS **CR**	clear breakpoint
BS aaaaa (T) **CR**	set breakpoint address (trigger-point)
BS L/R aaa (T) **CR**	set left/right bank breakpoint (trigger-point)
CH **CR**	accept commands from high-speed reader
CK **CR**	accept commands from keyboard
CT **CR**	accept commands from Teletype reader
DC aaaaa aaaaa **CR**	display contents of program memory
DH aaaaa aaaaa (text) **CR**	dump program memory to high-speed punch
DL aaa aaa **CR**	display left bank data
DR aaa aaa **CR**	display right bank data
DT aaaaa aaaaa (text) **CR**	dump program memory to Teletype
EHH **CR**	edit from high-speed reader to high-speed punch
EHT **CR**	edit from high-speed reader to Teletype punch
ETH **CR**	edit from Teletype reader to high-speed punch
ETT **CR**	edit from Teletype reader to Teletype punch
CTRL+B CR/LF	to enter new line
CTRL+C CR	punch contents of line buffer
CTRL+X CR	read next line and display
C **CR**	to copy n lines
GT **CR/LF**	go to current address and run/step
GT aaaaa **CR/LF**	go to address aaaaa and run/step
HC **CR**	continue at user-programmed halts
HD **CR**	clear halt display definition
HD X **CR**	halt display definition: all registers
HD Xaa ... Laa ... Raa **CR**	halt display definition: registers and IV bytes.
HS **CR**	stop at user-programmed halts
HT **CR**	stop execution
LH **CR**	load from high-speed reader
LK **CR**	load from keyboard
LT **CR**	load from Teletype reader
LU **CR**	load from user PROM
PD **CR**	program in DMS RAM
PU **CR**	program in user PROM
PT	punch PROM tape on Teletype
PH	punch PROM tape on high-speed punch
VT	verify PROM tape in Teletype
VH	verify PROM tape in high-speed reader
[BPNFw1 / BHLFw1 / HEXFw1] aaaaa aaaaa (text) **CR**	
SA **CR**	start assembly from Teletype reader
SAH **CR**	start assembly from high-speed reader
TI **CR**	test interface
TR **CR**	trace address
CTRL+I CTRL+O CR	I/O debug loop

w=word length I=LSB

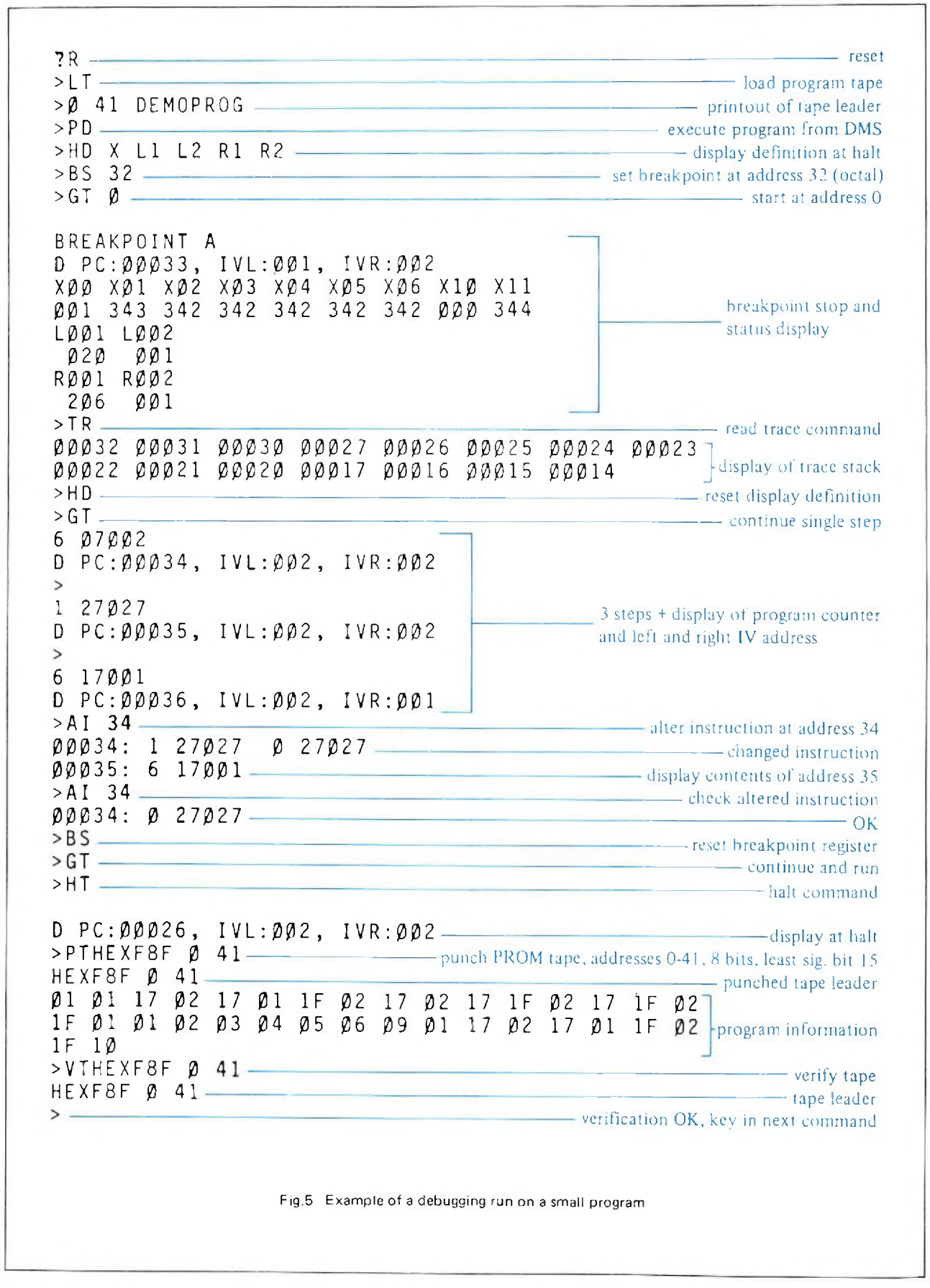


Fig.5 Example of a debugging run on a small program

ASSEMBLER AND CROSS-ASSEMBLER

An assembler is an important software tool which greatly simplifies the task of the programmer by its use of symbolic addresses, instruction mnemonics, etc, instead of laborious machine code. The DMS assembler, stored in ROM, is supplied on a separate card (the option card) which also contains an additional 3 K of user RAM. Some of the important features of the DMS assembler are:

- acceptance of source code on paper tape
- one-pass assembly
- symbolic addressing
- forward references
- expression evaluation
- symbolic representation of IV-bytes, or parts of an IV-byte
- subroutine call and return functions.

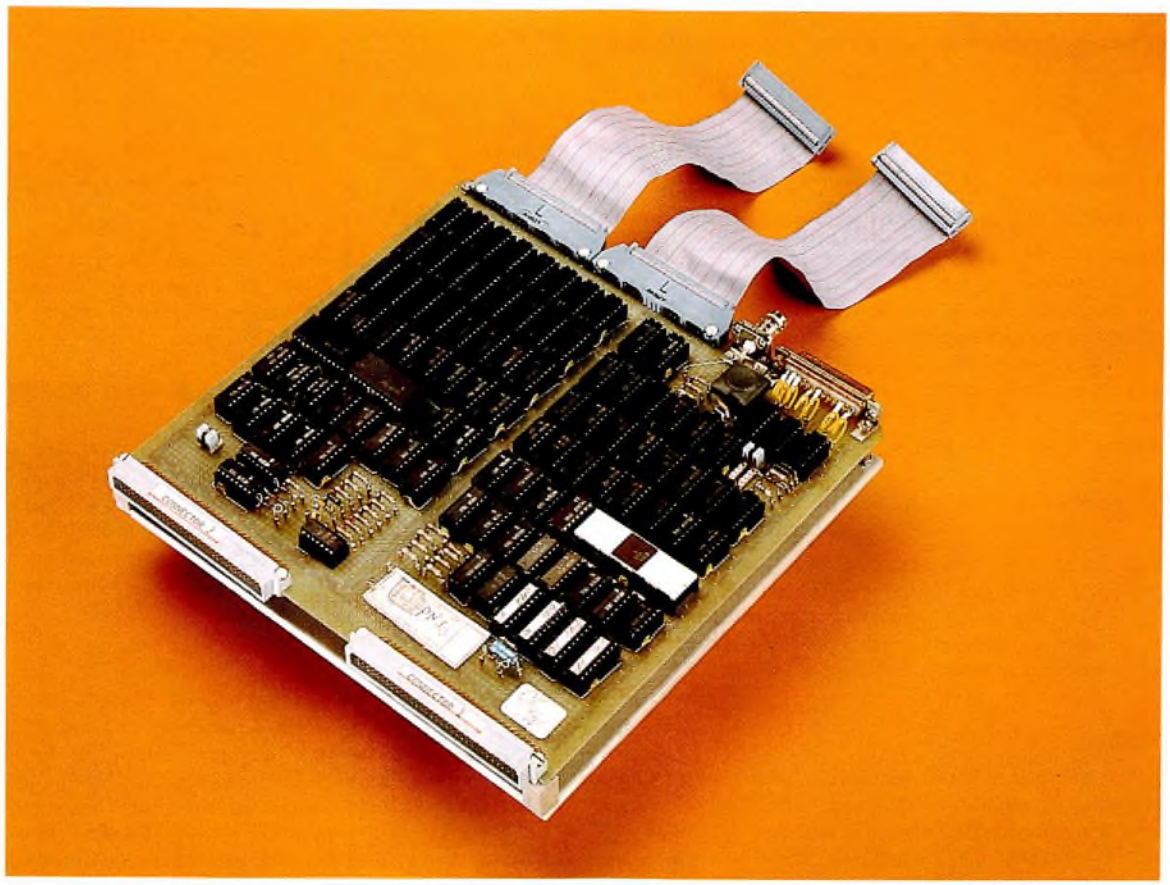
The facility to represent parts of an IV-byte symbolically enables the user to refer to single input/output lines by symbolic names. The subroutine call and return functions are valuable because the 8X300 has no special subroutine handling instructions.

If the user prefers to use a larger computer system to develop his software, or does not have the DMS assembler, he can use the 8X300 Microcomputer Cross-Assembler (MCCAP). This provides all the functions of the DMS with some additions, and can be run on most computers with a FORTRAN compiler. The MCCAP object tape output is suitable for input to the DMS.

REFERENCES AND ADDITIONAL INFORMATION

1. van VELDHUIZEN, E.D., 'The 8X300 – a high-speed control-oriented microprocessor', Electronic Components and Applications, Vol.1, No.2, Feb. 1979, pp.91 to 101.

Additional information can be found in 'The 8X300 System Design Manual' (ordering code 9398 602 60011) which describes the 8X300, ancilliary ICs, the instruction code, the DMS, the MCCAP, the 8X300 evaluation kit, as well as programming and application examples. Further information on the DMS is given in 'The 8X300 DMS user's manual' (ordering code 9398 607 00011).



The basic 8X300 Development and Monitoring System (DMS) on Eurocard with connections and wire links for interface and baud rate selection

Abstracts

Microcomputer-controlled tuning and control systems for TV

The described Video Tuning System (VTS) provides microcomputer-based control of the tuning and analogue functions of television receivers. The heart of the system is a stable frequency-locked digital tuning loop. Other facilities include on-screen and/or off-screen display of channel and/or programme number, preset stations, channel stepping, remote control, timing/clock functions, setting of sound and picture levels and control of videotex circuits.

Single-phase rectifier circuits with CR filters

Part 2 – Design procedure

This two-part article considers the semiconductor rectifier and CR filter combination. In this, the second part, a set of nomograms based on the equations derived in Part 1 is presented, and a step-by-step guide to the use of the nomograms in the design of practical circuits is given. Comparison of measurements made on eight different circuits with values derived using the equations printed in Part 1 shows good agreement. Furthermore, comparison of measured values with values calculated using traditional design methods shows the design method described in this article to be more accurate, particularly for low-voltage circuits.

Digital control of radio and audio equipment

Part 2 – Voltage converter and memory for preset radio tuning

This article describes a digital voltage converter and memory which provides up to 16 drift-free preset frequencies for f.m. or a.m./f.m. radios. Essentially an add-on circuit, VOCOM can be easily added to any existing radio design without disturbing the manual tuning a.f.c. facilities. LED display of selected waveband and program number is provided, and the system incorporates a back-up battery to ensure memory retention during temporary disconnection of the power supply.

Part 3 – Introduction to microcomputer-controlled Radio Tuning System

This is the first of a series of articles describing a versatile microcomputer-controlled Radio Tuning and control System (RTS). It explains how two new computer-bus compatible integrated circuits are used to achieve accurate, drift-free tuning with a phase-locked loop in an indirect frequency synthesiser.

8X300 DMS

In this, the second in a series of articles devoted to the 8X300 microprocessor, its application and support, the 8X300 Development and Monitoring System (DMS) is described. This is an inexpensive development aid intended to assist the engineer in debugging of both software and hardware at all stages of system development. The DMS command set is described and a brief example of a debugging run on a small program is given.

Mikrocomputer-gesteuerte Abstimm-und Bediensysteme für Fernsehempfänger

Das hier beschriebene Bedien- und Abstimmsystem VTS (Video Tuning System) steuert die Abstimmfunktionen und die analogen Bedienfunktionen von Fernsehempfängern auf Mikrocomputer-Basis. Den Kern des Systems bildet eine frequenzstabile geschlossene digitale Abstimmschleife. Zu den Leistungsmerkmalen des Systems gehören die Wiedergabe der Kanalnummer und/oder Programmnummer auf dem Bildschirm oder einer separaten Anzeige, Vorwahl und Speicherung von Stationen, schrittweise Kanalfortschaltung, vollständige Steuerbarkeit über die Fernbedienung, Timer/Uhr-Funktionen, Einstellung der Bild- und Tonfunktionen und Steuerung eines Videotex -Decoders.

Einphasen – Gleichrichterschaltungen mit RC-Filtern

Teil 2 – Entwurfsverfahren

Im zweiten Teil dieser Veröffentlichung über Halbleiter-Gleichrichterschaltungen in Verbindung mit RC-Filtern werden Nomogramme vorgestellt, die auf den im ersten Teil hergeleiteten Gleichungen beruhen; die Anwendung der Nomogramme beim Entwurf praktischer Schaltungen wird Schritt für Schritt erläutert. Ein Vergleich der an acht verschiedenen Schaltungen gewonnenen Messwerte mit den Rechenwerten aus den Gleichungen nach Teil 1 zeigt gute Übereinstimmung. Ausserdem ergibt sich aus dem Vergleich der Messwerte mit Rechenwerten aus herkömmlichen Entwurfsmethoden, dass das hier vorgestellte Entwurfsverfahren zu genaueren Werten führt, insbesondere bei Schaltungen mit niedriger Spannung.

Digitale Steuerung von Rundfunk- und NF-Geräten

Teil 2 – Spannungswandler und Speicher für Rundfunkempfänger mit Stationstasten

Dieser Beitrag beschreibt einen digitalen Spannungswandler und Speicher für bis zu 16 driftfreie Vorwahlfrequenzen in AM/FM-Rundfunkempfängern. Dieser als Zusatzschaltung konzipierte Baustein lässt sich leicht in alle bestehenden Rundfunk-Empfangsschaltungen einfügen, wobei die Eigenschaften von Handabstimmung und AFC nicht beeinflusst werden. Der eingeschaltete Wellenbereich und die Programmnummer werden mittels einer LED-Anzeige wiedergegeben. Zum System gehört eine Pufferbatterie, die die Aufrechterhaltung der Speicherdaten bei zeitweiligem Netzausfall sicherstellt.

Teil 3 – Eine Einführung in das Mikrocomputer-gesteuerte Rundfunk-Abstimmsystem RTS

Dieses ist der erste Beitrag einer Artikelserie, in der das vielseitige Mikrocomputer-gesteuerte Rundfunk-Abstimm-, Bedien- und Anzeigesystem RTS beschrieben wird. Hier wird zunächst erklärt, wie zwei neue Computerbus-kompatible integrierte Schaltungen in einem indirekten Frequenzsynthesizer mit Phasenregelschleife (PLL) zur exakten, driftfreien Abstimmung eingesetzt werden.

8X300-Kleinentwicklungssystem DMS

Im vorliegenden zweiten Beitrag einer Artikelserie, die dem Mikroprozessor 8X300, seiner Anwendung und seinen Systementwicklungs- Hilfsmitteln gewidmet ist, wird das 8X300-Kleinentwicklungssystem DMS (Development and Monitoring System) beschrieben. Dieses preiswerte Entwicklungshilfsmittel ist für die Unterstützung des Entwicklers bei der Erstellung und Prüfung sowohl der Software als auch der Hardware in allen Phasen der Systementwicklung ausgelegt. Der DMS-Funktionsvorrat wird beschrieben; als Beispiel wird ein Testlauf für ein einfaches Programm kurz behandelt.

Systèmes d'accord et de commande pilote par micro-ordinateur pour la télévision

Le système VTS d'accord vidéo décrit comprend la commande par micro-ordinateur des fonctions d'accord et de réglages divers des récepteurs de télévision. Le coeur du système est une boucle d'accord digital à verrouillage de fréquence stable. D'autres possibilités sont l'affichage sur écran et, ou hors écran du numéro de canal et, ou de programme, la présélection d'émetteurs, le choix pas à pas des canaux, la télécommande, les fonctions de synchronisation et d'horloge, le réglage des niveaux du son et de l'image et la commande de circuits vidéotex.

Circuits redresseurs monophasés avec filtres RC

2ème partie – Méthode de calcul

Cet article en deux parties est consacré à la combinaison d'un redresseur à semiconducteurs et d'un filtre RC. Cette seconde partie présente un jeu d'abaques basés sur les équations établies dans la première partie et décrit pas à pas l'emploi des abaques dans l'étude de circuits pratiques. La comparaison de mesures effectuées sur huit circuits différents et des valeurs calculées à l'aide des équations établies dans la première partie révèle une bonne concordance. De plus, la comparaison des valeurs mesurées et des valeurs calculées par les méthodes classiques montre que la méthode de calcul décrite dans le présent article est plus précise, en particulier pour les circuits à basse tension.

Commande digitale d'équipement radio et audio

2ème partie – Convertisseur de tension et mémoire pour accord radiophonique à présélection

Le présent article décrit un convertisseur digital de tension avec mémoire permettant la présélection et l'accord sans dérive sur 16 fréquences pour des récepteurs de radio FM ou AM/FM. De par sa nature un circuit essentiellement additionnel, le VOCOM peut aisément être ajouté à tout récepteur existant, sans perturber l'accord manuel ni le réglage automatique de fréquence. L'affichage de la gamme d'onde choisie et du numéro de programme se fait par diodes électroluminescentes et l'appareil comporte une batterie de réserve assurant la protection de la mémoire au cours du débranchement temporaire de l'alimentation.

3ème partie – Introduction au système d'accord radio commandé par micro-ordinateur

Cet article est le premier d'une série qui décrit un système polyvalent, de commande et d'accord radio commandé par micro-ordinateur. Il explique comment deux nouveaux systèmes intégrés compatibles avec bus d'ordinateur sont utilisés pour obtenir un accord précis et sans dérive avec une boucle à verrouillage de phase dans un synthétiseur de fréquence indirect.

8X300 DMS

Cet article, qui est le second d'une série consacrée au microprocesseur 8X300 et à ses applications, décrit le système 8X300 de développement et de surveillance (DMS). C'est un auxiliaire peu coûteux, destiné à aider le concepteur à mettre au point aussi bien le logiciel que le matériel dans toutes les phases du développement d'un système. Il décrit le jeu d'instructions du DMS et décrit brièvement l'opération de mise au point d'un petit programme.

Sistemas de sintonía y control controlados por microordenador para TV

El sistema de sintonía de video (VTS, video tuning system) descrito proporciona control, basado en microordenador, de las funciones de sintonía y analógicas del receptor de televisión. El corazón del sistema es un lazo de sintonía digital de frecuencia estable. Otras posibilidades incluyen visualización en pantalla y/o fuera de pantalla del número de canal y/o programa, emisoras preajustadas, salto de canal a canal, control remoto, funciones de temporización y reloj, ajuste de niveles de sonido e imagen y control de circuitos de videotex .

Circuitos rectificadores monofásicos con filtros RC

Parte 2 – Diseño.

Este artículo en dos partes considera la combinación de rectificador semiconductor y filtro RC. En esta segunda parte se presenta una serie de nomogramas basados en las ecuaciones deducidas en la primera parte y se da una guía paso a paso para el empleo de los nomogramas en el diseño de circuitos prácticos. La comparación de medidas efectuadas en ocho circuitos diferentes con valores deducidos empleando las ecuaciones indicadas en la primera parte muestran buena concordancia. Además, la comparación de valores medidos con valores calculados empleando los metodos de diseño tradicionales muestra que el método de diseño descrito en este artículo es más exacto, especialmente para circuitos de baja tensión.

Control digital de equipo de radio y audio

Parte 2 – Convertidor de tensión y memoria para sintonía de radio preajustada.

Este artículo describe un convertidor de tensión analógico/digital y memoria que proporciona hasta 16 frecuencias preajustadas sin deriva para receptores de radio AM o AM/FM. Puede añadirse fácilmente un circuito de esta clase a cualquier receptor de radio existente sin molestia para la sintonía manual y el c.a.f. Se dispone de visualizacion LED de la banda de onda y del número de programa, y el sistema incorpora una batería de retén (back-up) para asegurar la retención de memoria durante la desconexión temporal de la alimentación.

Parte 3 – Introducción al sistema de sintonía de radio controlada por microordenador.

Este es el primero de una serie de artículos que describen un sistema de sintonía y control de radio (RTS, Radio Tuning and control System) controlado por microordenador. Explica como se emplean dos nuevos circuitos integrados compatibles con bus de ordenador para lograr sintonía exacta y sin deriva con un lazo de efecto volante (phase-locked loop) en un sintetizador de frecuencia indirecto.

8X300 DMS

En este artículo, el segundo de una serie dedicada al microprocesador 8X300, su aplicación y soporte, de describe el sistem de desarrollo y monitorización (DMS, Development and Monitoring System). El DMS es un elemento económico de ayuda al desarrollo diseñado para la puesta en marcha (debug) de "software" y "hardware" en todas las etapas del desarrollo del sistema completo. Se describe el conjunto de mando del DMS y se da un ejemplo en la puesta en marcha y comprobación de un pequeño programa.

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