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Three New Pocket Calculators: Smaller, Less Costly, More Powerful

HP's second-generation pocket calculator family now includes a basic scientific model, a programmable scientific model, and a business model.

by Randall B. Neff and Lynn Tillman

IN 1972, HEWLETT-PACKARD INTRODUCED the HP-35 pocket scientific calculator,[1] the first in a family of calculators that eventually grew to include six members, from the original HP-35 to the sophisticated fully programmable HP-65.[2]

Now there is a second generation of HP pocket calculators. Currently this new calculator family has three members, designated HP-21, HP-22, and HP-25. The HP-21 (Fig. 1) is a basic scientific calculator that replaces the HP-35, the HP-22 (Fig. 2) is a business calculator, and the HP-25 (Fig. 3) is a programmable scientific calculator. State-of-the-art technology has been applied in the new family to achieve the major design goal of low cost with no sacrifice in reliability or quality.

Most parts are common to all three calculators, the fundamental differences occurring in the read-only memory (ROM) that contains the preprogrammed functions. In each calculator is an integrated circuit that is a small, slow, but powerful microcomputer. It executes microprograms that are stored in the ROM. When the user presses a key, a microprogram is activated to perform the function corresponding to that key.

The ROM comes in blocks of 1024 ten-bit words. Each block adds factory cost. But until all of the ROM has been allocated, features can be added, omitted, or modified and functions can be made more or less accurate without increasing factory cost at all. The firmware designer's challenge is to make these no-cost choices in some optimal way for each calculator.

HP-21 Scientific

The HP-21, the first calculator in the new family, was designed as a direct replacement for the HP-35. Because the HP-21 was to have 33% more microprogram ROM than the HP-35, everyone involved in the project wanted additional features and functions. New features were packed in until all the ROM was used. The HP-21 has all the functions of the HP-35 plus controlled display formatting, polar to rectangular conversions, radian mode in trigonometric calculations, and storage arithmetic.

One major change in these HP-21 family calculators from the HP-35 family is a shorter twelve-digit display. The HP-35 display had fifteen digits: two signs, ten mantissa digits, two exponent digits, and a decimal point. The new twelve-digit display was required because of the narrower plastic case of the

Cover: *The three pocket calculators in HP's second generation—the HP-21 Scientific, the HP-22 Business and Financial, and the HP-25 Programmable Scientific—are smaller and deliver more performance at lower prices than their predecessors.*

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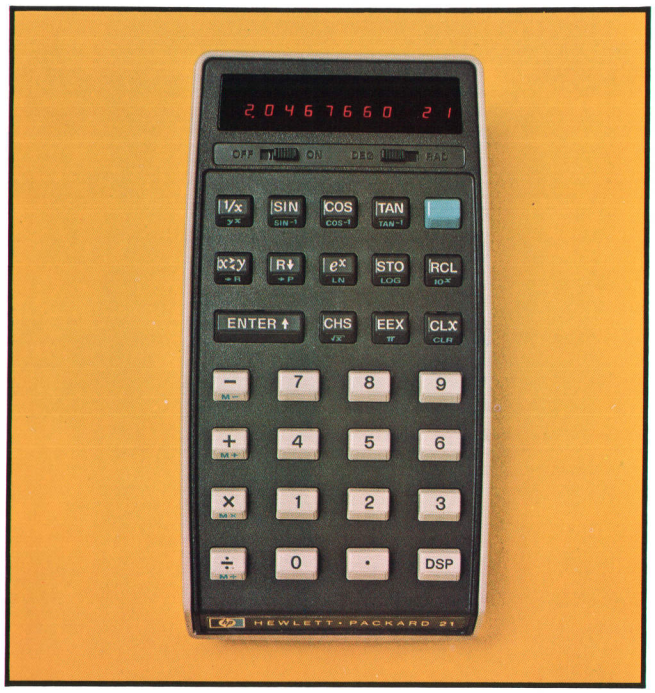


Fig. 1. *HP-21 Scientific Calculator*

new family.

In spite of the shorter display, there was still a requirement that the calculator have ten-digit precision. To meet this requirement, the decimal point was moved so that it appears next to a digit. Also, a decision was made to show a maximum of eight mantissa digits when an exponent is displayed, so two of the display digits do double duty, sometimes as mantissa digits, and other times as exponent sign and digit.

The HP-21 never gives a misleading zero answer. When the user has specified fixed notation and the non-zero answer of a function would be formatted as a zero, the HP-21 changes to scientific notation for that answer. When the HP-21 shows zero, it means the answer is zero to ten digits.

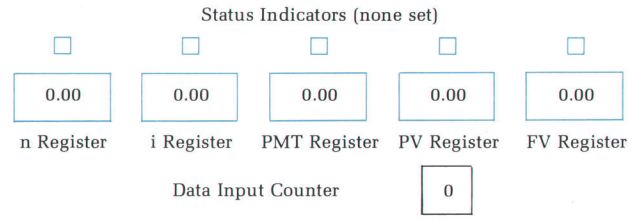
HP-22 Business

The HP-22, the business member of the new calculator family, was intended to be an "HP-70-Plus". Again, experience from programming the HP-70 and many new microinstructions allowed the product to grow functionally until it provided an array of mathematical, statistical, and storage capabilities in addition to the financial functions we had originally hoped to add.

The HP-22 is the first of our financial calculators to include e^x and ln functions on the keyboard. It is also the first of our financial calculators to provide linear regression and linear estimate. These functions, as well as arithmetic mean and standard deviation, are executed using data automatically accumulated with the $\Sigma+$ key. In combination, the arithmetic and statistical functions allow calculation of such things as exponential and logarithmic regression, power curve fit, and trend lines with uneven periods, a powerful set of computational tools for the financial analyst and forecaster.

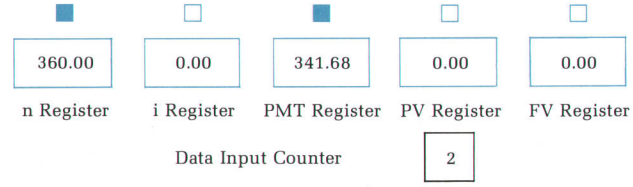
Greatly expanded storage is available to the user. There are ten user-addressable registers with storage arithmetic similar to that of the HP-25. There are also five financial storage registers—one associated with each of the basic financial parameters (n, i, PMT, PV and FV).* The basic functions defined by these five top row financial keys are the same as those in the HP-70 and HP-80.[4]

These registers combined with internal status indicators (one for each parameter) and an internal data-input counter form a flexible system for solving financial calculations. When the calculator is turned on, the system might be thought of as looking like this:



The financial functions require that the contents of exactly three of the financial parameter registers be specified as input data, that is, three status indicators must be set and the data input count must equal three.

When data is entered the associated status indicators are set and the data input counter is incremented. For example, if two items of data have been entered (say n = 360 and PMT = 341.68) the system might look like this:



If a status indicator is already set, entering data for that parameter will simply overwrite the previous register contents. For example, pressing n in the above situation would cause the 360.00 to be overwritten with whatever was in the display. The status indicator would remain set and the counter would remain at 2. Once three status indicators are set, pressing a financial key for which the status indicator is *not* set will trigger an attempt to execute that function.

* n: number of time periods; i: interest rate per period; PMT: payment amount; PV: present value or principal; FV: future value

Fig. 2. *HP-22 Business Calculator*

Say the system looks like this:

■	■	■	□	□
360.00	.75	341.68	0.00	0.00
n Register	i Register	PMT Register	PV Register	FV Register

Data Input Counter: 3

Pressing **PV** will cause calculation of PV in terms of n, i and PMT while pressing **FV** will cause calculation of FV in terms of n, i and PMT.

When a function is executed and an answer is calculated, the answer is stored in its associated register for possible later calculations. The status indicators and counter remain unchanged because the input parameters have not changed.

There is a reset function, which resets all five status indicators and resets the counter to zero, allowing a different combination of input parameters to be specified. However, the data remains in the registers and can be recalled using the **RCL** prefix key.

Besides the new flexibility in the basic financial functions some new functions have been added: %Σ (percent of sum), **ACC**(accumulated interest), **BAL** (remaining balance), and the annuity switch (**BEGIN** ◧ **END**).

A running total can be kept using the Σ+ key. The %Σ function can then be used to find what percent of that total any given number is.

Accumulated interest and remaining balance are also new. Just enter the loan amount PV, the periodic interest rate i, and the payment amount PMT. To find the accumulated interest between two periods, say from payment 13 through payment 24 enter the payment period numbers in storage registers 8 and 9 and press ■ **ACC**. If you then press ■ **BAL** the HP-22 will calculate the remaining balance on the loan after the payment indicated in register 9 is made (in this case after payment 24).

Annuities are often referred to as being "ordinary annuities" or "annuities due". These terms distinguish situations where periodic payments are made at the beginning of the period (for example, rents or leases are annuities due) from payments made at the end of the month (a mortgage, for example, is an ordinary annuity). The HP-22 features the annuity switch to make this distinction. Place the switch in the **BEGIN** position and any annuity calculations will be made assuming that payments occur at the beginning of the payment period. Place the switch in the **END** position and annuity calculations will be made assuming that payments occur at the end of the payment periods.

The HP-22 uses the same general solution techniques for the financial functions as the HP-80.[4] Execution of the equations involves numerous internal subroutine calls to +, −, ×, ÷, y^x, and ln (this is particularly true for the iterative solutions for i). This means that the standard round-off errors in these routines are compounded by the time the final solution is reached. To improve the final results given by the HP-22, improvements were made to the standard HP-21-family arithmetic subroutines. The y^x algorithm was extended to handle negative numbers to integer powers—for example $(-2)^2$ or $(-2)^{-2}$—and a subroutine was developed to calculate the expression $(1+y)^x$, which occurs frequently in financial equations.

HP-25 Programmable Scientific

The HP-25 was originally conceived as an advanced scientific calculator. It was specified as having 2048 microinstructions, twice as many as the HP-21. Also, it was to contain a new integrated circuit, a sixteen-register data storage chip. Because of improved microinstructions and experience gained by microprogramming the HP-21, the HP-25 finally appeared not only as a scientific calculator with many more functions than the HP-21, but more importantly, with 49 steps of user programming.

The real power of the HP-25 is its easy programming. The programming is based on key phrases rather than keystrokes. A key phrase is simply a sequence of keystrokes that together perform one function or operation. For example, both **f SIN** and **STO + 5** are key phrases, but they contain two and three keystrokes, respectively. The program memory contains numbered locations for 49 key phrases. When

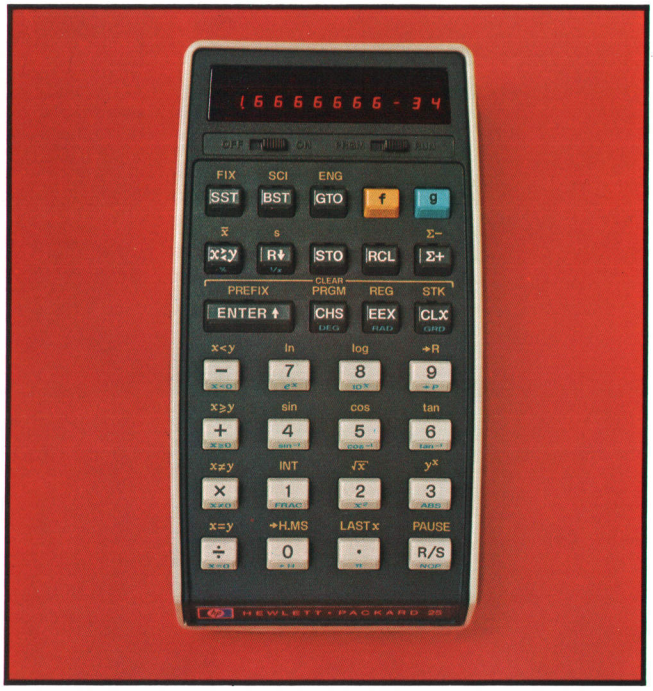


Fig. 3. *HP-25 Programmable Scientific Calculator*

the user writes a program, the calculator merges keystrokes into key phrases and stores the instructions in program memory.

Editing a program is particularly easy. In program mode, the display shows the step number and the key phrase stored there (see page 6). The key phrase is displayed as the row-column coordinates of the keystrokes that make it up. The digit keys are represented by a zero followed by the digit, and the other keys are described by a row digit followed by a column digit. For example, the f key is in the first row of keys and the fourth column, so its coordinate is 14. The key phrase f SIN appears as 14 04, and STO + 5 appears as 23 51 05.

One innovative feature of the HP-25 is the behavior of the SST (Single Step) key in run mode. This key was designed to help the user debug programs. It allows the user to execute his program one key phrase at a time. When the SST key is held down, the display shows the line number and the key phrase that is to be executed next. Releasing the SST key executes just that key phrase, and the numerical results appear in the display. This new feature makes debugging programs quite easy because the user can tiptoe through his programs, seeing both the key phrases and their results, one phrase at a time. The display when the SST key is held down includes the step number, so checking program flow and branching is easy.

The HP-25 contains a number of functions that make programming simpler. In program mode, the SST key and the BST (Back Step) key allow the user to step forward and backward through the program memory. Eight comparisons allow the program to react depending on the data in the calculation stack. Together with the GTO (Go To step number) operation, programs can branch and loop based on numeric results. A function that is new to pocket calculators is PAUSE. When encountered in a program, the calculator stops for a second, displays the most recent result, and then continues the program. This is useful when programming iterative functions because one can watch the function converge or diverge.

The HP-25 has line-number-based static programming. Key phrases go into numbered locations in memory, overwriting the previous contents. Branching in the program is to the step number of a phrase. This is in contrast to the HP-65 type of programming.[3] In the HP-65, keycodes shift around in the unnumbered memory as steps are inserted and deleted, and branching goes to label keycodes contained in the memory.

The HP-25 merges keystrokes into key phrases using a microcoded finite state machine. The machine carefully checks for undefined key sequences. When a valid key phrase is completed, an eight-bit code is fabricated. If the calculator is in run mode, the code is immediately decoded and executed. In program mode, the code is copied into the program memory and then decoded to generate the row-column display. The data registers used for program storage are 56 bits long. Each register can contain seven key phrase codes. Seven such registers comprise the program memory, so all together there are 49 key phrase locations.

The HP-25 contains a data storage integrated circuit with sixteen registers of 56 bits each (14 BCD digits). Seven registers are for user programming, eight are for user data, and one is used for the LAST x function.

Another innovative feature of the HP-25 is a new mode of formatting the displayed result, called engineering notation. This is a selectable format that makes calculated answers easier to understand. Imagine a problem that deals in physical units of measure, such as seconds. Say the answer to the problem in scientific notation is 5.00 −05. Now this is a valid answer, but not as clear as it could be. Setting the HP-25 into engineering notation gives the answer as 50.0 −06 which is easy to read instantly as 50 microseconds. Engineering notation forces the power-of-ten exponent to be a multiple of three and adjusts the decimal point to give the correct answer. If the above answer is multiplied by 10, it gives 500. −06 or 500 microseconds. Multiplying again by ten gives 5.00 −03 or five milliseconds.

Design Details

Several improvements in the instruction set of the

An Example of HP-25 Programming

A simple ecological model of interacting populations consists of rabbits with an infinite food supply and foxes that prey on them. The system can be approximated by a pair of nonlinear, first-order differential equations:

$$\frac{dr}{dt} = 2r - \alpha rf \qquad \text{(change in rabbits with time)}$$

$$\frac{df}{dt} = -f + \alpha rf \qquad \text{(change in foxes with time)}$$

where r is the number of rabbits, f is the number of foxes, and α is a positive constant to show how frequently rabbits and foxes meet. When $\alpha = 0$ there are no encounters; the rabbits keep breeding and the foxes starve. For a specific α, the probability of encounter is proportional to the product of the numbers of foxes and rabbits. A reasonable choice for α is 0.01.

One way to solve this problem numerically is a simple Euler method, solving equations of the form:

$$x_{n+1} = x_n + h \cdot f(x_n)$$

using a small step size h, where h represents a small increment of time. The equations become:

$$r_{n+1} = r_n + h \cdot (2r_n - \alpha r_n f_n)$$

$$f_{n+1} = f_n + h \cdot (-f + \alpha r_n f_n)$$

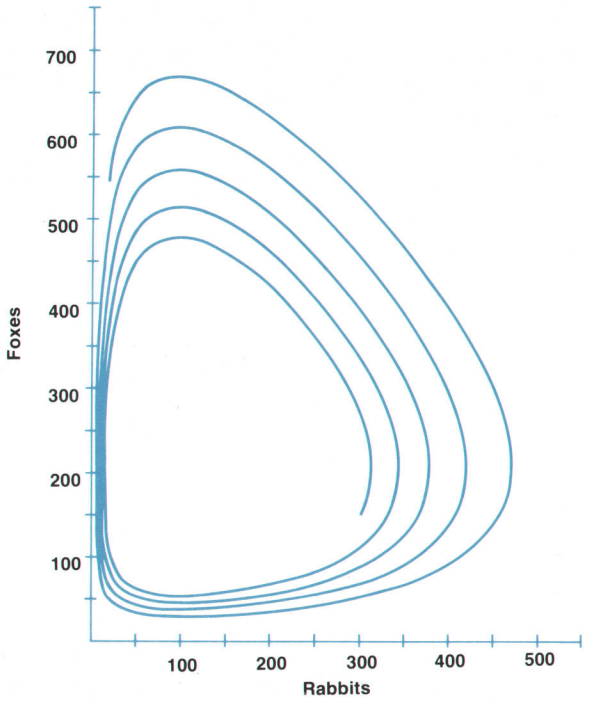
The features of the HP-25 make it ideally suited for problems of this type. The results can be plotted by hand on a graph of foxes versus rabbits. Note that the calculations give ten-digit floating-point numbers, but the display is always truncated to an integer.

Example:

$\alpha = 0.01$
$h = 0.02$
$r_0 = 300$
$f_0 = 150$

A plot of foxes versus rabbits is a circular loop with a period of about five time units (250 iterations). The rabbit minimum is 14, the maximum is 342 on the first loop. The fox minimum is 54 and the maximum is 478 on the first loop.

$r_0 = 100$, $f_0 = 200$ is a constant solution.



HP-25 Program Form

Title Rabbits vs Foxes Page ___ of ___

Switch to PRGM mode, press f PRGM, then key in the program.

LINE	CODE	KEY ENTRY	X	Y	Z	T	COMMENTS
00			f_0	r_0			rabbits ENTER↑ foxes
01	23 02	STO 2	f_0	r_0			save initial foxes
02	22	R↓	r_0			f_0	
03	23 03	STO 3	r_0			f_0	save initial rabbits
04	14 11 05	f FIX 5	r_0			f_0	change display format
05	24 02	RCL 2	f_n				start loop here
06	31	ENT↑	f_n	f_n			foxes
07	31	ENT↑	f_n	f_n	f_n		
08	24 03	RCL 3	r_n	f_n	f_n		rabbits
09	24 00	RCL 0	α	r_n	f_n	f_n	encounter factor
10	61	×	αr_n	f_n	f_n	f_n	
11	61	×	$\alpha r_n f_n$	f_n	f_n		number of meetings
12	23 04	STO 4	$\alpha r_n f_n$	f_n	f_n		save
13	21	x≷y	f_n	$\alpha r_n f_n$	f_n		
14	41	−	$\alpha r_n f_n - f_n$	f_n			change in foxes
15	24 01	RCL 1	h	$\alpha r_n f_n - f_n$	f_n		step size (time)
16	61	×	Δf	f_n			current change foxes
17	51	+	f_{n+1}				new number foxes
18	15 41	g x<0	f_{n+1}				if negative, then
19	00	0	0				change to 0
20	23 02	STO 2	f_{n+1}				save new number
21	24 03	RCL 3	r_n				rabbits
22	02	2	2	r_n			
23	61	×	$2r_n$				
24	24 04	RCL 4	$\alpha r_n f_n$	$2r_n$			number of meetings
25	41	−	$2r_n - \alpha r_n f_n$				change
26	24 01	RCL 1	h	$2r_n - \alpha r_n f_n$			step size
27	61	×	Δr_n				change in rabbits
28	24 03	RCL 3	r_n	Δr_n			
29	51	+	r_{n+1}				new number rabbits
30	15 41	g x<0	r_{n+1}				if negative, then
31	00	0	0				change to 0
32	23 03	STO 3	r_{n+1}				save new number
33	14 01	f INT	$\lfloor r_{n+1} \rfloor$				truncate to integer
34	24 02	RCL 2	f_{n+1}	$\lfloor r_{n+1} \rfloor$			foxes
35	14 01	f INT	$\lfloor f_{n+1} \rfloor$	$\lfloor r_{n+1} \rfloor$			truncate to integer
36	33	EEX	1. 00	$\lfloor f_{n+1} \rfloor$	$\lfloor r_{n+1} \rfloor$		
37	05	5	1. 05	$\lfloor f_{n+1} \rfloor$	$\lfloor r_{n+1} \rfloor$		
38	71	÷	$\lfloor f_{n+1} \rfloor / 10^5$	$\lfloor r_{n+1} \rfloor$			divide foxes by 10^5
39	51	+	$r_{n+1} \cdot f_{n+1}$				make double display
40	14 74	f PAUSE	$r_{n+1} \cdot f_{n+1}$				(Pause for 2
41	14 74	f PAUSE	$r_{n+1} \cdot f_{n+1}$				seconds
42	13 05	GTO 05					Loop
43							
44							
45							
46							
47							
48							
49							

REGISTERS
R0 α encounter factor
R1 h step size
R2 f_n foxes
R3 r_n rabbits
R4 $\alpha r_n f_n$ number encounters
R5
R6
R7

Note: the variables in the stack are incomplete. This listing does not include variables in the stack when they are no longer relevant.

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HP-25 Program Form

Title Rabbits vs Foxes Page ___ of ___

Programmer ___

STEP	INSTRUCTIONS	INPUT DATA/UNITS	KEYS				OUTPUT DATA/UNITS
1	Key in program						
2	Store α	α	STO	0			
3	Store step size	h	STO	1			
4	Input rabbits	r_0	↑				
5	Input foxes	f_0	f	PRGM	R/S		
	program loops, pausing						
	to give a dual display						
	of rabbits · foxes						rabbits · foxes
	for additional problems:		R/S				
	go to step 4						

HP-21-family microprocessor made life much easier for the microprogrammer. Three of the most useful improvements were 12-bit subroutine addresses, the digits-to-ROM-address instruction, and the data register instructions.

In the HP-35 microprocessor, the microinstruction address was only eight bits long. Each 256-word ROM would turn itself on or off as ROM-select instructions dictated. There was only one level of subroutine and the return address had only eight bits. The HP-21 microprocessor uses a twelve-bit address. A given ROM responds only when it sees an address it contains. Subroutines can be located on different ROMs and easily return to the correct next instruction. The new processor can save two twelve-bit subroutine return addresses. Two levels make it possible for one subroutine to call another.

A new processor instruction takes two calculated digits as the next microprogram address. This instruction is exactly like a computed GO TO instruction in some programming languages. This instruction made the HP-25 possible. It is used for both key phrase execution and key phrase display. The eight-bit key phrase code is broken down into groups of phrases such as GTO codes, STO codes, f, and g codes. Then the code is either used to generate a display (for the SST key) or is executed (run mode).

The data storage chip used in the HP-35 family required that a calculated address be sent from the processor to activate one register. Then the register could be written into or read from. When the HP-25 data storage chip was designed, this mode of operation was retained, because a calculated address is needed for STO, RCL, and programming. However, enough microinstructions were available to define separate instructions to read or write in each register. This simplified the HP-22 microprogramming by allowing any financial register to be accessed internally with a single microinstruction.

One change in the system design of the HP-21 family was putting the display segment drive in the ROM integrated circuit. Which segment to power is determined by an accessory ROM composed of sixteen words of seven bits each. The words 0 to 9 are used to generate the digits. One word, 15, is a blank. Three of the remaining words generate the letters E, r, and o, which the HP-21 family uses to spell "Error," telling the user that an operation is illegal. One remaining word generates the letter F. This is used by the HP-25 to spell "OF" when a storage register overflows. Since the display generator is a tiny ROM on the microcode ROM, it can be changed to create new characters for new calculators.

Acknowledgments

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Randall B. Neff

Randy Neff did the microprogramming for the HP-21 and HP-25. Born in Houston, Texas, Randy attended Rice University in Houston, receiving his BS and MS degrees in electrical engineering in 1972 and 1973. He joined HP's Advanced Products Division in 1973. A member of ACM, he's now a programmer in the integrated circuit laboratory of Hewlett-Packard Laboratories. Randy enjoys reading science fiction and working with wood. He's married and lives in Palo Alto, California.

Lynn Tillman

Lynn Tillman did the microprogramming for the HP-22 and its predecessor, the HP-70. With HP since 1973, she's now production engineer for the HP-22. Lynn received a BS degree in secondary education from the University of Texas at Austin in 1969. After teaching ninth-grade science for a year, she returned to the campus, this time at the University of California at Berkeley, and received an AB degree in computer science in 1972. Born in Mattoon, Illinois, Lynn grew up in Gallup, New Mexico, working weekends and summers in an Indian trading post. She's married, lives in Los Altos, California, and relaxes by producing handmade rugs and collecting glassware from the 1930's.

Inside the New Pocket Calculators

The HP-21 type of calculator isn't just a stripped-down version of older HP pocket calculators, but an entirely new design.

by Michael J. Cook, George M. Fichter, and Richard E. Whicker

THE HP-21 AROSE FROM THE NEED to follow its predecessor, the HP-35, with a lower-priced hand-held scientific calculator. The HP-35 was, in a way, a tough act to follow. Its low-cost successor couldn't be merely a stripped-down factory special, for it isn't possible to change part of the HP-35 design without destroying the integrity of the design.

Instead, the HP-21 required a totally fresh design with an integrity of its own, taking advantage of late refinements of technology in the areas of displays, integrated circuits, batteries, and assembly.

The HP-21, for the most part, uses the architecture of the HP-35 but requires fewer integrated-circuit packages to implement all the functions found in the earlier chip set (see Fig. 1). Two reductions in package count were obtained by combining the anode drivers with the ROM into one 18-pin plastic package and by incorporating all the arithmetic, register, and control circuits on a second chip in a 22-pin plastic package. Clock driving circuits are contained on each chip, thereby saving one more package.

Another improvement, both in cost and in appearance, is the use of a smaller, two-cell battery. The nominal 2.5-volt supply must be converted to four volts for operating the displays, resulting in some loss of efficiency, but since the bipolar display cathode driver now used does not require a converted voltage, the loss is nearly made up.

Arithmetic, Control, and Timing Circuit (ACT)

This circuit combines the functions of the first generation's arithmetic and register circuit, control and timing circuit, and clock driver circuit and includes several new capabilities. All of these circuits could not simply be put together unchanged because more pins would have been required than were on the package. To reduce this number, several pins are used for multiple functions. The cathode driver scans the key rows, so the ACT circuit needs only five lines to scan the key columns and one line to synchronize the cathode driver, instead of the previous design's eight lines for the key rows and five lines for the key columns. One line is used to send display data to the ROM and anode driver as well as to send addresses and receive instructions. The older design used ten lines for these functions.

The addressing structure has been changed to allow direct addressing of 4096 instructions. This means that at the end of a subroutine, control can pass back to the calling location from any location, instead of from only 255 locations. An additional level of subroutine nesting is included, so one subroutine can be called from within another. The number of status bits is increased to 16, and a four-bit register has been added to remember the display format requested by the user.

The original HP-35 stack is retained, but there are now two storage registers on the ACT circuit instead of only one. This is not readily apparent to the HP-21 user unless he needs to use the full stack and do transcendental functions at the same time. In the HP-35 the highest entry of the stack was lost, whereas in the HP-21 it is not lost. The stack registers are labeled X (display), Y, Z, and T. The storage registers are M and N. There are three working registers: A (= X), B, and C.

The ACT circuit also performs hexadecimal (modulus 16) arithmetic in addition to decimal. This function is used in display formatting in the HP-21 and HP-25, but may be of more interest to designers if the ACT circuit is to be used in instruments.

Data Storage Chip

This optional chip is used in the HP-22 and HP-25. To allow it to store programs, it was arranged that keycodes could be sent either to the ROM or to the A

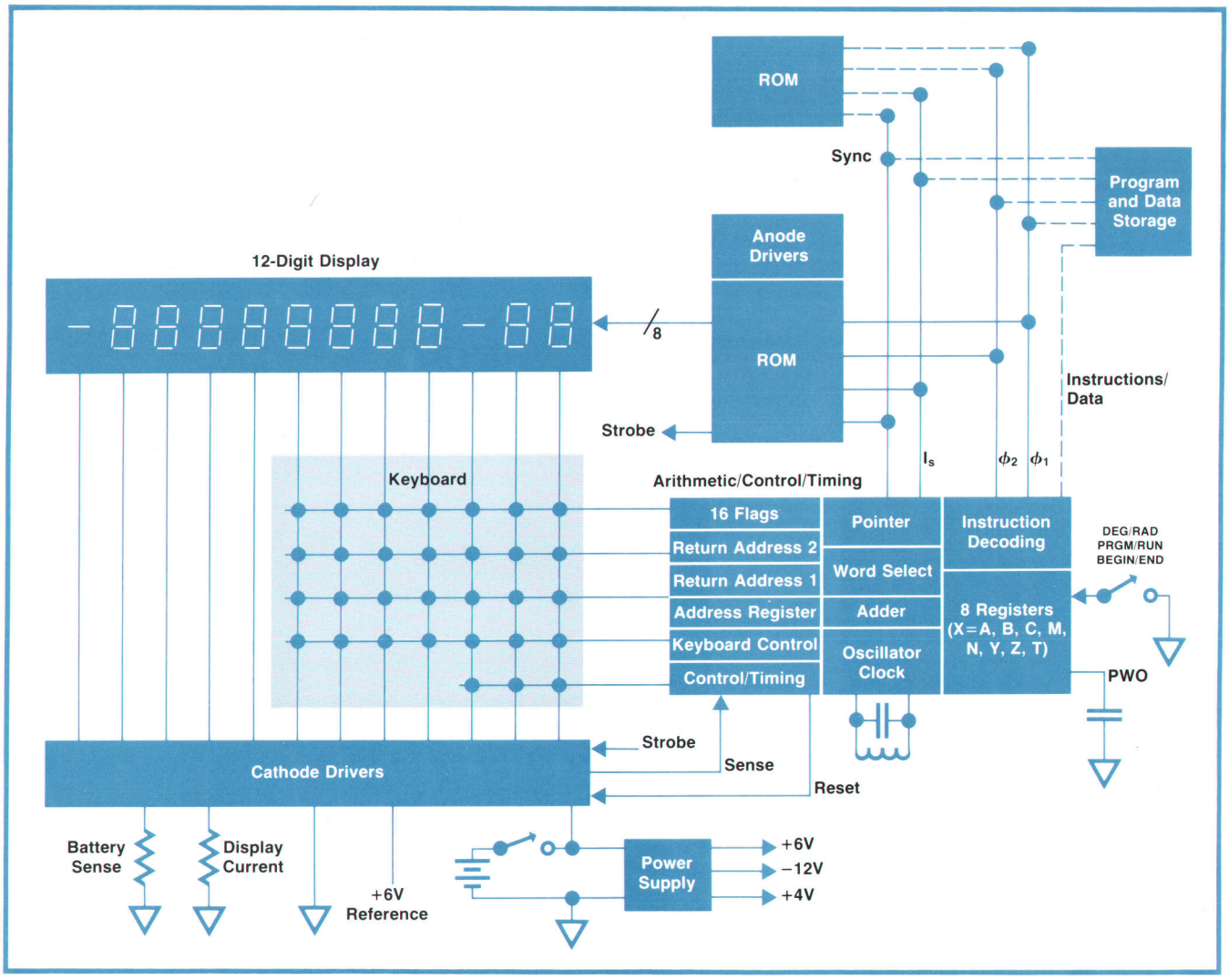


Fig. 1. *The three members of the HP-21 family differ in the amount of read-only memory and data storage they contain. Keys activate microprograms stored in the ROM, causing the arithmetic, control, and timing circuit to perform the indicated function.*

register on the ACT chip, and that the A register could send previously stored keycodes to the ROM. The C register communicates with the data storage registers, so by exchanging portions of the contents of the A and C registers, keycodes could be sent to and retrieved from the data storage registers. To aid in editing programs (i.e., sequences of keycodes), a circular shift function was added to the A register. This enables the data in the A register to be rotated without losing information.

The data storage chip is more versatile than its predecessor in that direct register addressing is possible, that is, the instruction itself contains the number of the register into which data is to be stored, or from which data will be retrieved. Previously a register number had to be built up in the C register, and then two instructions used, "C to data address" and either "C to data" or "data to C." These indirect data register addressing instructions are also still available.

ROM

The ROM consists of 10,240 bits of read-only memory, organized as 1024 words of 10 bits each. Four pages of microinstructions can be stored on one chip, and up to four chips can be addressed directly by the ACT circuit.

12-bit addresses are received on the instruction/address (I_S) line, least significant bits first. The two most significant bits enable one of four chips to output instructions onto the I_S line. Thus, up to 4096 microinstructions may be programmed in a maximum system. Unlike the HP-35 quad ROM, any 12-bit address sent to the ROM chip will be recognized, regardless of previous addresses.

Display Circuit

During each 56-bit word time, the ACT chip sends information to the ROM/display chip for displaying one digit. A character ROM in the display circuit con-

verts the input to seven-segment format and then multiplexes through the segments sequentially. With a 12-digit display, the duty cycle for each segment is 1/96 or about 1%. This requires a peak current of 30 mA to maintain an average current of 300 μA. This is a relatively high current for MOS and requires devices well over 100 mils (0.25 cm) wide.

To allow the use of multiple ROMs without duplicating the display function, a mask option can eliminate all power consumed in this portion of the chip. Typically, ROM 0 contains the display function and all other ROMs do not.

Five of the characters in the display ROM may be reprogrammed to any seven-segment character. Three of these characters generate E, r, and o to spell Error.

Packaging the New Pocket Calculators

by Thomas A. Hender

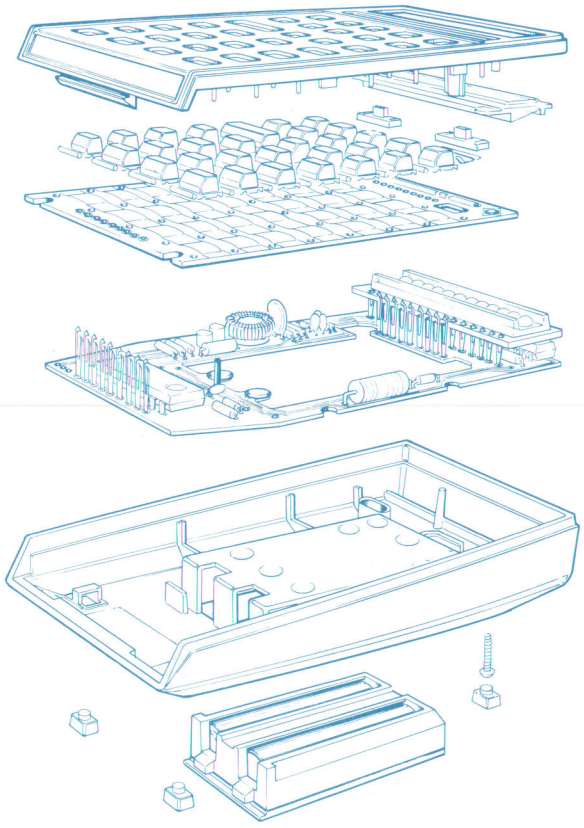
Objective: design a "shirt-pocket" calculator package for minimum factory cost, with reliability equal to or better than that of the HP-35 family. HP quality standards must be maintained.

Shirt-pocket size was achieved by reducing the number of keys from 35 to 30 (one less horizontal row) and by spacing the keys closer together. Spacing is the minimum deemed comfortable for the majority of users. Also, the display was reduced from 15 to 12 digits, and decimal points share positions with their digits.

The HP-21 uses only two rechargeable size AA NI-Cad batteries instead of the three required in the HP-35 family. This feature saves almost thirty grams of weight. The total weight of the HP-21 is 165 grams. Apart from the obvious weight saving accompanying its smaller size, the HP-21 package contains fewer parts: no backbone support, no key-spacing grid and no display window welding frame. Structural rigidity is designed into the monocoque or box shape of the battery compartment in the bottom case, and in the heat-staked egg-crate configuration of the top case and keyswitch printed circuit assembly (plastic posts on the top case fit through holes in the keyswitch printed circuit assembly; heat is then applied to deform the ends of the posts and rivet the two parts together).

Lower production costs of this package are mainly due to minimal assembly time, including testing. Only two screws fasten the HP-21 together—a reduction of ten from the HP-35. The display is an integral plug-in assembly. Modular construction eases handling and any necessary touch-up operations; for instance, there are no electronic components or soldering on the keyswitch printed circuit assembly.

The battery pack case doubles as part of the calculator's bottom outside surface, eliminating a separate battery-retaining panel. The battery jumper spring provides the force that holds the pack in the calculator, so latches are not needed. Battery terminals are automatically assembled into the logic board during fabrication. This feature eliminates the manual wiring and terminal fastening required in the previous generation's design. The ac terminal pins are mounted similarly. Electrical integrity is provided by a flow-soldering operation which connects all electronic components to the logic board. All keys except the blue prefix key are molded in two clusters, which are mechanically separated during loading into the keyboard bezel. This reduces the number of parts handled from thirty to three and minimizes assembly operator errors and fatigue. That this innovation works is largely because of the creative efforts of the plastic mold designers and craftsmen of the HP Manufacturing Division, whose continuing high standards of excellence contributed much to the success of the HP-21. The over-center breakaway tactile feel of our former calculator keys has been retained, and the molded design of the key-strip actuating surfaces on the undersides of the keys eliminates the control bumps needed on earlier models.



Acknowledgments

I want to express my thanks to Tom Holden and Craig Sanford for their fine assistance in the design and documentation of this package and to Denny Thompson and his group and to Bill Boller of the HP Manufacturing Division for seeing to it that necessary things were done on time. Finally, recognition is due to the cooperative people in production and to Gabe Bonilla and Cliff Planer of the model shop for their painstaking efforts, particularly during the concept phase of the project.

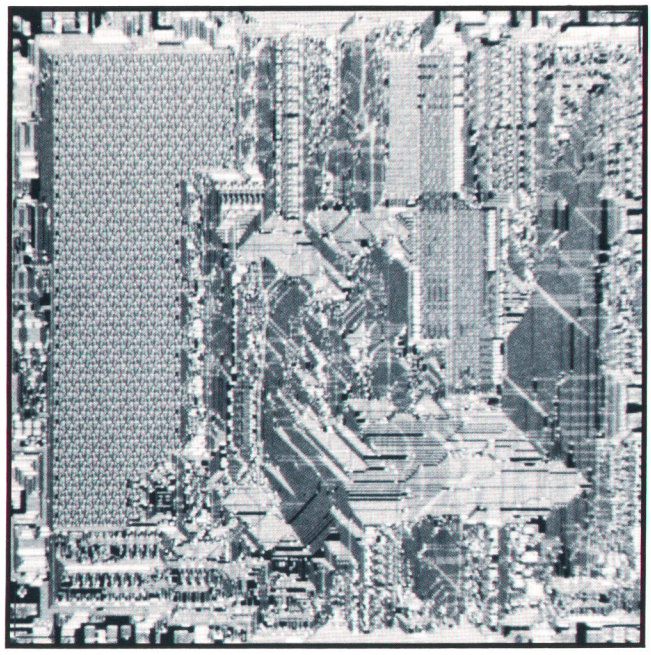


Fig. 2. *Arithmetic, control, and timing chip.*

Cathode Driver

In designing the cathode driver circuit for the HP-21 calculator, the main objective was to have a circuit with extremely low power consumption, a prime requirement for the HP-21 since only a two-cell battery pack is used. Functionally, the custom designed bipolar driver chip consists of a 12-bit shift register, twelve cathode drivers each with a current limiting feature, low-battery detection circuit, input buffer, and timing control gating. The 12-bit shift register turns on the twelve cathode drivers one at a time.

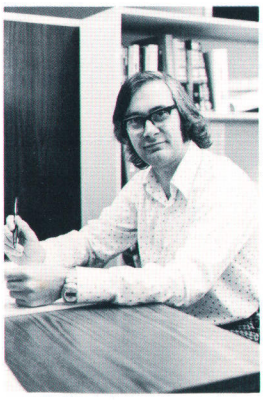
The LED digit display drive technique used in the HP-21 is different from that employed in the HP-35. In both cases the segment drivers (anode) and the digit drivers (cathode) are scanned one digit at a time, one segment at a time, but the HP-21 does it by switching dc voltages while the HP-35 uses an inductive charge-discharge method. When they are on, the anode drivers of the HP-21 are dc sources for the individual LED segments, while the anode drivers for the HP-35 drive each LED segment indirectly by first charging an inductor which then discharges through the LED segment. The HP-21 method requires significantly fewer components.

Acknowledgments

The authors would like to thank the following people for their contributions to this project: Bosco Wong for the design of the cathode driver chip, Les Moore for the assembly and debugging of the breadboard, Mark Linsky for the design of the power supply and recharger, Ed Liljenwall for the industrial design, and Ernst Erni and Chung Tung for their support throughout the project.

Richard E. Whicker

Rich Whicker, project leader for the HP-21 series, graduated from the University of Illinois in 1966 with a BSEE degree. For the next six years he did MOS logic design for a semiconductor company, then continued in that specialty after joining HP in 1972. Born in San Francisco, Rich now lives in Santa Clara, California. He's married and has three children, a daughter and two sons. For a change of pace from the job Rich plays piano, builds radio controlled models and, like a bus driver who goes for a drive on his holiday, works out electronic ideas of his own.



Michael J. Cook

Mike Cook developed the ACT chip for the HP-21 series. He joined HP in 1973 with an extensive background in the design of MOS LSI circuits. Born in Watford, Hertfordshire, England, Mike earned his BSc and MSc degrees in electrical engineering at the University of Southhampton in 1963 and 1966, then came to the United States to work for an aircraft company as a systems designer. Later he joined a semiconductor company, designing more than 50 MOS LSI circuits and serving briefly as MOS applications and marketing manager for that company in Germany. He speaks German and French as well as English and is a student of comparative linguistics. Mike is married, has three daughters, and lives in Cupertino, California. His interests include classical music, color printing, and sketching.

Correction

The article entitled "Active Probes Improve Precision of Time Interval Measurements" (Hewlett-Packard Journal, October 1975) understated the accuracy achieved by the Model 1722A Oscilloscope in time interval measurements. The accuracy of the Model 1722A for main time base settings between 100 ns/div and 20 ms/div is specified conservatively as ±0.5% of measurement ±0.02% of full scale for measurements less than 1 cm, and ±0.5% of measurement ±0.05% of full scale for measurements greater than 1 cm. Typical measurement accuracies are more than three times better than this. The time base calibration period has not been specified because it has not been a significant contributor to inaccuracy. Experience shows that yearly calibration may be sufficient for instruments maintained in a laboratory environment. The time base temperature coefficient is specified as ±0.03%/°C and short term stability is better than 0.01%.

Thomas A. Hender

Tom Hender was responsible for the product design and packaging of the HP-21 series. Born in Cobourg, Ontario, Canada, he served in the Royal (British) Navy during the second world war, then attended British Admiralty College (Devonport Division), graduating in 1947 with a BSc degree in mechanical engineering. His engineering career includes work on punched-card machines, line printers, point of sale terminals, and related peripheral mechanisms. He joined HP in 1973. Tom is married, has three daughters, and lives in San Jose, California. He serves his church as choir director and enjoys photography, chess, and model railroading.

George M. Fichter

George Fichter designed the read-only memory for the HP-21 series. A native of New York City (Brooklyn), he graduated from Stevens Institute of Technology with a BS degree in 1965, spent six years as a U.S. Air Force meteorologist; and then returned to school at the University of Washington, earning a BSEE degree in 1972 and an MS in computer science in 1973. He joined HP in 1973. George is married and has a son and a daughter. An accomplished musician, he plays French horn and experiments with computer music using an HP 2100 Computer. He's also learning to fly and hopes to get his private pilot's license this year. The Fichters live in Los Altos, California.

FEATURES AND SPECIFICATIONS

HP-21 Scientific Calculator

PREPROGRAMMED FUNCTIONS
- ARITHMETIC: +, −, ×, ÷
- LOGARITHMIC: e^x, ln x, log x, 10^x
- TRIGONOMETRIC: sin x, arc sin x, cos x, arc cos x, tan x, arc tan x
- OTHER: y^x, $\sqrt{x}$, 1/x, π, rectangular/polar coordinate conversion, degrees-radians mode selection
- REGISTER ARITHMETIC: addition, subtraction, multiplication, or division operations can be performed on data in storage register.

NUMERIC NOTATION
- FLOATING POINT: 10 digit mantissa and sign
- SCIENTIFIC: A sign and integer followed by up to seven possible decimal places. The exponent consists of a sign and two digits.
- MIXED FLOATING POINT AND SCIENTIFIC: Mixed numeric notation may be entered as data. After performance of any operation data reverts to floating point or scientific notation as applicable.
- ROUNDING TO LAST DISPLAYED DIGIT: Internal operations are calculated to within 10 digits.

DISPLAY
- NUMERIC AND DECIMAL POINT: Eight-segment, light-emitting diode (LED). Digit and decimal point are contained within a single eight-segment LED digit.
- SIGN: Eight-segment light-emitting diode
- 12-digit display including two sign digits
- MAXIMUM DISPLAY NUMBER: $\pm 9.9999999 \times 10^{\pm 99}$
- DISPLAY FORMAT: Fixed notation and scientific notation as specified
- SPECIAL INDICATIONS:
  - Overflow: All nines (9.9999999 99)
  - Underflow: Zero in scientific notation. In fixed notation automatically reverts to scientific notation for small numbers that would otherwise appear to be zero.
  - Low Battery: Inverted decimal points for 30 seconds to ½ hour before display blanks.
  - Improper Operation: "Error" written on display.

DYNAMIC RANGE: $9.999999999 \times 10^{99}$ to $1. \times 10^{-99}$ and 0.
NUMBER OF KEYS: 30, 1 on/off switch, 1 degree/radian switch
MEMORY REGISTERS: six total
- Four working registers in an operational stack
- One storage register
- One hidden register for trigonometric function computation

DATA ENTRY
- Exponent entry
- Negative number entry (CHS)

PACKAGING
- High-impact, contoured beige plastic (ABS) calculator case
- All solid state electronics
- Light-emitting diode (LED) display

SPEED: a one second maximum for all preprogrammed functions (200 kHz clock speed)
POWER
- RECHARGERS: European, 103-127 and 206-254 Vac 50-60 Hz; U.K. Desktop, 206-254 Vac, 50-60 Hz; United States, 90-127 and 180-254 Vac, 50-60 Hz. 5 watts, plastic box. Recharger warm to the touch in normal operation
- BATTERY: 350 mW derived from 2-cell quick recharge nickel-cadmium battery pack. Operating time 3 to 5 hours. Approximately 6 hours to recharge completely discharged battery pack when calculator is not in operation. Approximately 17 hours to recharge completely discharged battery pack when calculator is operating under maximum load (all 8's displayed). Battery pack must be in place for calculator to operate.

WEIGHT
- CALCULATOR WITH BATTERY PACK: 6 oz (170 grams)
- RECHARGER: 5 oz (142 grams)
- SHIPPING WEIGHT: 1½ lb (682 grams), approximately.

CALCULATOR DIMENSIONS
- LENGTH: 5⅛ in (13.02 cm)
- WIDTH: 2 11/16 in (6.83 cm)
- HEIGHT: 1 3/16 in (3.02 cm)

PRICE IN U.S.A.: $100.

HP-22 Business Calculator

FINANCIAL FUNCTIONS:
- n Number of periods
- i Periodic interest rate
- PMT Periodic payment amount
- PV Present value of money
- FV Future value of money
- 12× Converts yearly periods to monthly periods
- 12÷ Converts annual interest to interest rate per month
- ACC Computes accumulated interest between any two time periods of a loan
- INT Calculates simple interest
- BAL Gives remaining loan balance at any point in time
- %Σ Percent one number is of total
- % Calculate percentage of a number
- Δ% Percent of difference between two numbers
- BEGIN-END SWITCH: This switch is a special convenience which works in conjunction with the financial keys in calculating payments due at the beginning or end of the period for annuities, leases, loans and other transactions.

STATISTICAL FUNCTIONS:
- Σ+ Provides the number of entries and sums two variables
- Σ− Adjusts data, corrects an incorrect Σ+ entry
- L.R. Linear regression; linear functions between two points
- $\hat{y}$ Linear estimate
- $\bar{x}$ Mean or arithmetic average
- s Standard deviation

MATHEMATICAL FUNCTIONS:
- ln Computes natural logarithm (base e) of value in display
- e^x Natural antilog; raises e to value in display
- y^x Raises number in Y register to value in display
- $\sqrt{x}$ Square root of number in display

ARITHMETICAL FUNCTIONS:
- − Subtract
- + Add
- × Multiply
- ÷ Divide
- CHS Changes a positive number to a negative number

MEMORY REGISTERS:
- 10 separate addressable memories with full register arithmetic
- 5 financial registers
- 4 operational stack registers with stack roll-down for review

DATA MANIPULATIONS; DISPLAY CONTROL; STORAGE FUNCTIONS:
- x⇄y Exchange contents of the X and Y registers
- R↓ Rolls down the stack to review contents
- CLX Clears display
- CLEAR Clears display, stack and storage registers; resets financial status indication
- RESET Resets financial status indicators and clears only statistical data
- ENTER↑ Copies number displayed in X register into Y register; also separates numerical entries by moving entries up in operational stack
- RCL Recalls a number to the X register from a storage register
- STO Stores displayed value into one of the 10 storage registers
- [gold] Gold shift key; selects functions printed in gold on keyboard

DISPLAY:
- 10 significant digits (8 + 2 digit exponent displayed in scientific notation).
- Fixed decimal notation with automatic overflow and underflow into scientific notation
- Scientific notation with dynamic range of 10^{-99} to 10^{99}
- Automatic decimal point positioning and selective round-off
- Indicators for improper operations (Error in display) and low battery condition (lighted decimal points)
- Light-emitting diode (LED) display recessed for better contrast in harsh lighting

DESIGN SPECIFICATIONS:
- Operates 3 to 5 hours on rechargeable batteries (under 6 hours to recharge) or ac
- Specially designed recessed plug to prevent erroneous insertion of improper unit
- Solid state electronics with all critical connections gold-plated
- Tactile feedback keyboard. Positive contact action assures accurate entry of data.
- Heavy gauge compact case contoured to fit the hand
- Ultrasonically welded impact resistant case
- Plastic liquid-barrier shield under keyboard sealed to resist entry of moisture
- Keys are double injection molded to help prevent the legend from wearing off.

PHYSICAL SPECIFICATIONS:
- CALCULATOR LENGTH: 5⅛ in (13,02 cm)
- CALCULATOR WIDTH: 2 11/16 in (6,83 cm)
- CALCULATOR HEIGHT: 1 3/16 in (3,02 cm)
- CALCULATOR WEIGHT: 6 oz (170,1 g)
- RECHARGER WEIGHT: 5 oz (141,8 g)
- SHIPPING WEIGHT: approx 1½ lb (680 g)
- OPERATING TEMPERATURE RANGE: 32°F to 113°F (0°C to 45°C)
- CHARGING TEMPERATURE RANGE: 59°F to 104°F (15°C to 40°C)
- STORAGE TEMPERATURE RANGE: −40°F to 131°F (40°C to 55°C)

POWER REQUIREMENTS:
- AC: 100-127 V or 200-254 V, ±10%, 50 to 60 Hz, 5 watts
- BATTERY: 2.75 Vdc nickel-cadmium rechargeable battery pack

PRICE IN U.S.A.: $165

HP-25 Programmable Calculator

PROGRAMMING:
- Program writing capability
- Single step execution or inspection of a program
- Pause (to display intermediate result)
- Program editing capability
- 8 relational tests: x<y, x=y, x≠y, x<0, x≥0, x=0, x≠0
- Conditional branching
- Direct branching

KEYBOARD COMMANDS:
- TRIGONOMETRIC FUNCTIONS:
  - 3 angular modes (degrees, radians, grads)
  - Sin x
  - Arc sin x
  - Cos x
  - Arc cos x
  - Tan x
  - Arc tan x
  - Rectangular coordinates ⇆ polar coordinates
  - Decimal angle (time) ⇆ Angle in degrees (hours)/minutes/seconds
- LOGARITHMIC FUNCTIONS:
  - Log x
  - Ln x
  - e^x
  - 10^x
- STATISTICAL FUNCTIONS:
  - Mean and standard deviation
  - Positive and negative summation giving n, Σx, Σx², Σy, Σxy
- OTHER FUNCTIONS:
  - Integer (gives only integer portion of number)
  - Fraction (gives only fractional portion of number)
  - Absolute (gives absolute value of x)
  - y^x, $\sqrt{x}$, 1/x, π, x², %
  - Register arithmetic in all 8 addressable registers
  - Addition, subtraction, multiplication or division in serial, mixed serial, chain or mixed chain calculations.
- DATA STORAGE AND POSITIONING OPERATIONS:
  - Data entry
  - Stack roll down
  - x,y interchange
  - Data storage
  - Data recall
  - Change sign
  - Enter exponent

MEMORY:
- 4-register stack
- "Last x" register
- 8 addressable registers
- Program memory for storage of up to 49 steps

LIGHT-EMITTING DIODE DISPLAY:
- Displays up to 10 significant digits, 8 plus two-digit exponent in scientific and engineering notation, and appropriate signs. Three selectable display modes: fixed point (with automatic overflow and underflow into scientific), engineering, and scientific, with dynamic range of 10^{99} to 10^{-99}. Automatic decimal point positioning. Selective round-off; range 0-10 digits in fixed point; 0-8 digits in scientific; 0-8 in engineering notation. "Error" appearing in display indicates improper operation; low battery indicator.

GENERAL SPECIFICATIONS: Operates on fast-charge battery pack or ac. (Battery recharges in 6-17 hours.) Tactile feedback keyboard. Polyethelene liquid-barrier shield under keyboard. Compact case of high-impact plastic with recessed display. Recessed recharger/ac plug receptacle. Solid state electronics.

OPERATING SPECIFICATIONS:
- POWER: AC: 115 or 230 V, ±10%, 50 to 60 Hz, 5 watts. Battery: 500 mw derived from nickel-cadmium rechargeable battery pack.
- WEIGHT: HP-25: 6 oz (170 g) with battery pack. Recharger: 5 oz (142 g).
- SHIPPING WEIGHT: Approx 1.5 lbs (.7 kg).
- DIMENSIONS:
  - LENGTH: 5.1 inches (13.0 cm)
  - WIDTH: 2.7 inches (6.8 cm)
  - HEIGHT: 1.2 inches (3.0 cm)
- TEMPERATURE RANGE:
  - OPERATING: 32°F to 113°F (0°C to 45°C)
  - CHARGING: 59° to 104°F (15°C to 40°C)

PRICE IN U.S.A.: $195
MANUFACTURING DIVISION: ADVANCED PRODUCTS DIVISION
19310 Pruneridge Avenue
Cupertino, California 95104 U.S.A.

A New Microwave Link Analyzer for Communications Systems Carrying up to 2700 Telephone Channels

Multiplexed communications systems can operate at full capacity only when distortions are at a low level. This new instrument helps optimize the performance of wide-bandwidth systems.

by Svend Christensen and Ian Matthews

MICROWAVE LINK ANALYZERS, by detecting and displaying the transmission characteristics of microwave communications systems, help find the causes of distortion—distortion that unless corrected would degrade signal-to-noise ratio, reducing system capacity.

A new microwave link analyzer is designed to test communications systems that use an intermediate frequency (IF) of 140 MHz. A growing number of microwave links employ the 140-MHz IF which allows transmission bandwidths enabling transmission of up to 2700 voice channels simultaneously. The wide bandwidth, however, also makes a system more vulnerable to those forms of distortion that affect the higher modulation frequencies. Consequently, the new microwave link analyzer (MLA) was designed to include functions involving baseband test signals as high as 12 MHz.

As in earlier HP MLA's,[1] the basic measurement principle used in the new MLA, HP Model 3790A (Fig. 1), is to explore the passband of a frequency-modulated system with a low-level, high-frequency test signal superimposed on a high-level, low-frequency sweep signal (Fig. 2). Applied to the sys-

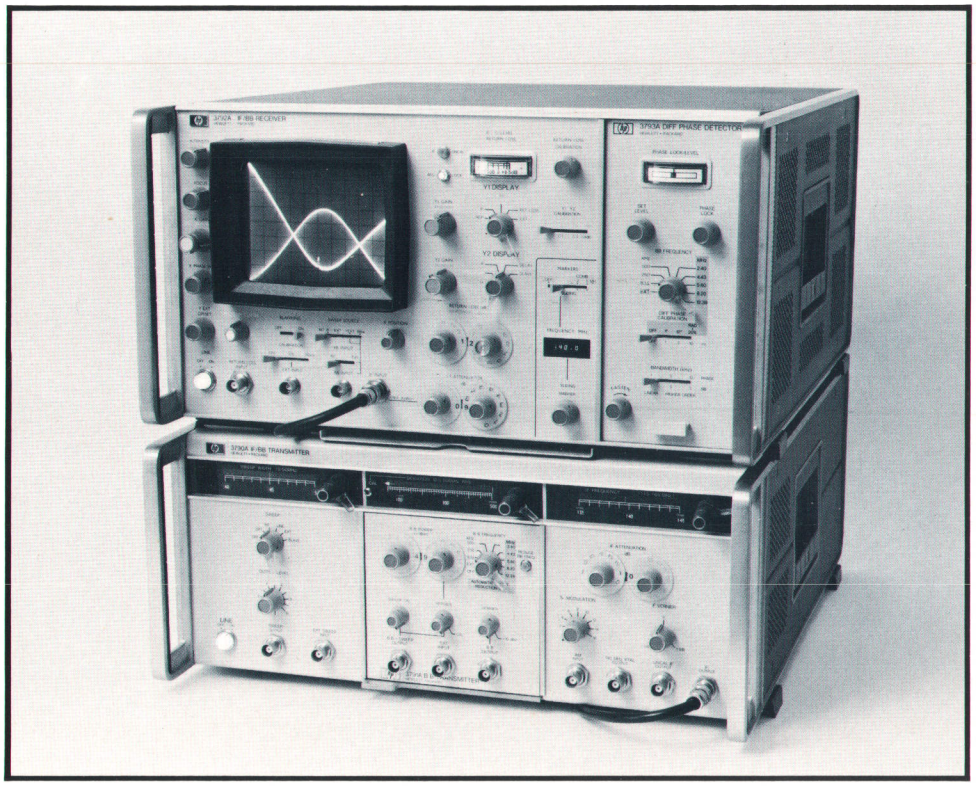


Fig. 1. *The new microwave link analyzer consists of a transmitter (Model 3790A, lower unit) that generates appropriate communications-link test signals, and a separate receiver (Model 3792A, upper unit) that measures the characteristics of the test signals after they have been passed through the device or system under test. Results are displayed as measured quantity versus frequency on the dual-trace CRT display. Measurements are made with this system either at the baseband level or at the newly-adopted 140-MHz IF level.*

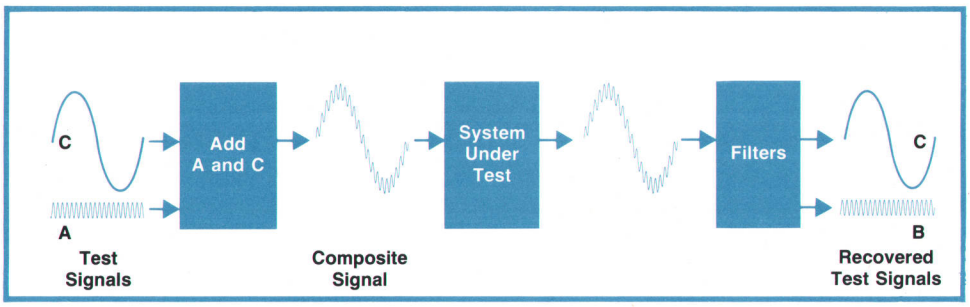


Fig. 2. *The MLA measurement principle. The composite signal frequency-modulates the system under test. Level variations in waveform B at the rate of C are processed and displayed as a plot of linearity or differential gain versus frequency. Phase variations in B with respect to A are processed and displayed as group delay or differential phase.*

tem under test, the low-frequency signal sweeps the high-frequency signal across the system's passband. Non-linearities and other distortions arising in the system affect the amplitude and phase of the high-frequency signal as it is swept. The disturbances in amplitude and phase are detected and displayed quantitatively at the receiving end of the system to provide a measure of the communication system's performance (Fig. 3).

The MLA makes several measurements to analyze a system's characteristics. These are:

Linearity
Differential gain
Group delay
Differential phase
IF amplitude response.

It also measures gain, attenuation, power, and return loss, and it can provide a spectrum display for measuring FM modulator and demodulator sensitivity by the carrier-null method.

Sources of Distortion

The disturbances in the received test signal result from three basic sources of distortion in a microwave link. One is imperfect voltage-to-frequency and frequency-to-voltage conversion in the modulators and demodulators. The other two are nonlinear phase response and non-flat amplitude response. Nonlinear phase response incorrectly *repositions* the phasor components of the FM signal and non-flat amplitude response incorrectly *reproportions* them, as discussed on pages 18 through 20. Preservation of the amplitude and phase of each phasor ensures the absence of AM in a pure FM signal. Any random upset of the critical phasor lengths and directions generates AM simply because the signal is no longer purely FM. If a signal distorted in this manner were passed through a device exhibiting AM-to-PM (amplitude modulation to phase modulation) conversion, PM would be produced which would be detected along with the wanted FM, degrading the signal-to-noise ratio.

Any of these distortions result in noise in telephone channels and impairment of television pictures.

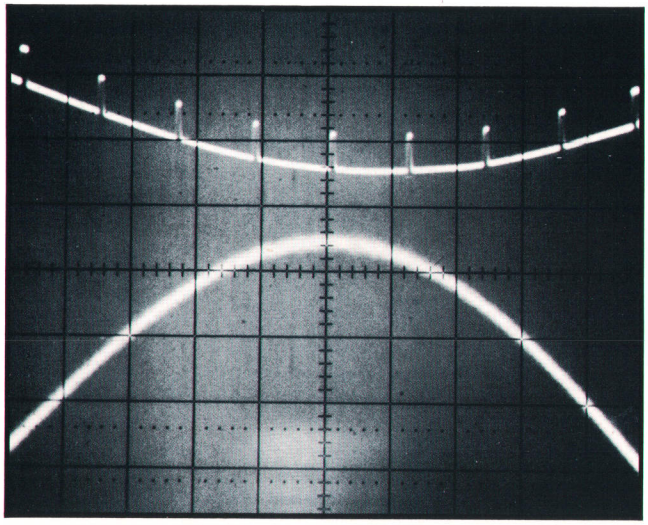


Fig. 3. *Typical display provided by the Model 3792A IF/BB Receiver, this one showing amplitude linearity (upper trace) and group delay as functions of IF frequency. The pulses on the upper trace are frequency markers.*

AM-to-PM Conversion

There are many influences that degrade a broadband communications system, some of which are well understood and readily corrected. The significance of AM-to-PM conversion, however, is not widely appreciated so it deserves special consideration.

To examine the effect of AM-to-PM conversion, consider an FM signal in which AM has been generated. If the modified signal were applied to a device whose phase response is sensitive to amplitude—TWT amplifiers and diode limiters are such devices—phase modulation would result from the amplitude modulation.

Two possibilities now arise. (1) If the AM had been generated by nonlinear phase response in a device, the phase modulation caused by AM-to-PM conversion would be in phase with the signal phase modulation and would affect the FM deviation. AM variations would then generate differential gain, the difference in system gain measured at two different frequencies. (2) If the AM had been caused by non-flat frequency response, the resulting phase modulation would be in quadrature with the signal phase modulation. In this case, AM variations would give rise to differential phase. These mechanisms are explained on pages 18 through 20.

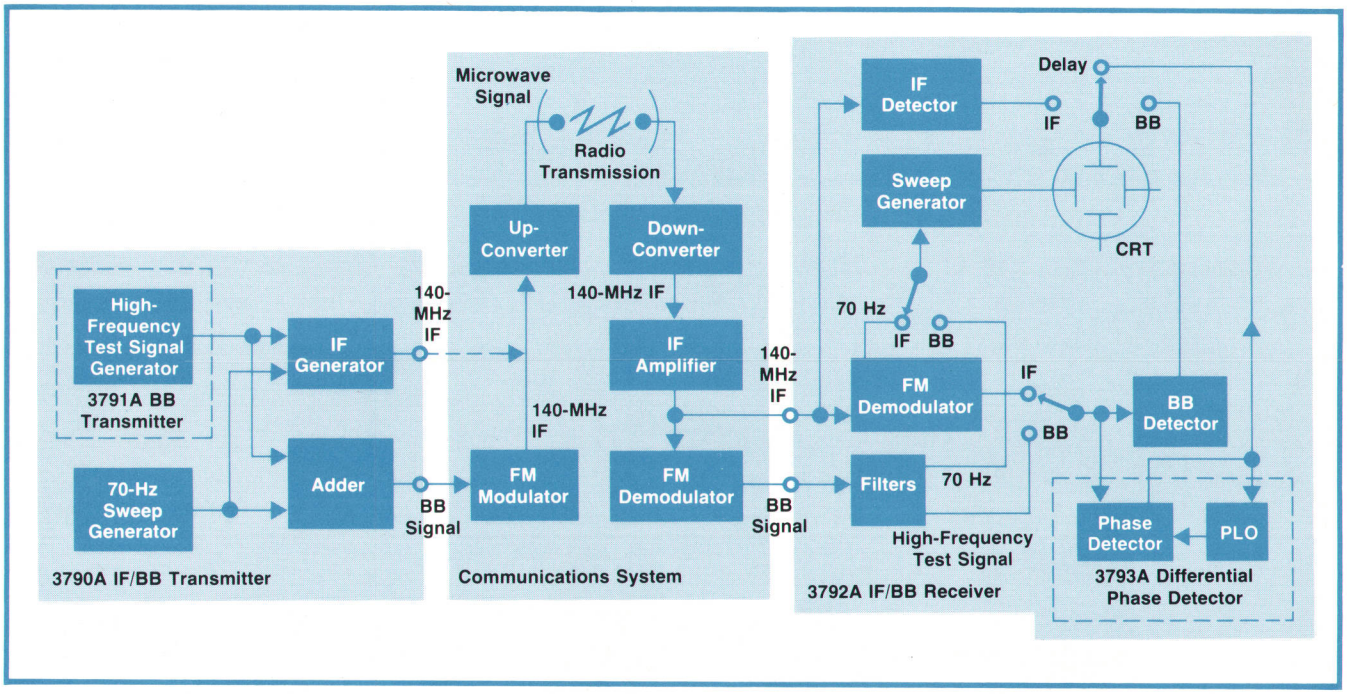


Fig. 4. *Simplified block diagram of the microwave link analyzer and a typical communications system. The analyzer can also measure the performance of modems and the other components of a system.*

AM-to-PM conversion is not the only contributor to differential gain. Nonlinear phase response generates AM with a corresponding decrease in signal PM, as shown on page 18. Analysis shows that the differential gain caused this way is proportional to the *fourth* power of the baseband frequency and so is much more significant in a 2700-channel system than in an 1800-channel system. When generated by nonlinear phase accompanied by AM-to-PM conversion, or non-flat amplitude response, differential gain is proportional to the *square* of the baseband frequency. For these reasons, it was considered important for the new MLA to have a test frequency at 12.39 MHz, the top end of the 2700-channel baseband.

Besides degrading signal-to-noise ratio in telephone systems, differential gain and differential phase have a pronounced effect on color TV transmissions. In the NTSC system used in North America, for example, color saturation is determined by the level of the color subcarrier, and hue is determined by the phase. To preserve the integrity of the color saturation and hue, it is important to minimize differential gain and phase occurring on the color subcarrier.

MLA Basics

The complete MLA system consists of two units with plug-ins as follows: Model 3790A IF/BB Transmitter with Model 3791A BB Transmitter plug-in, and Model 3792A IF/BB Receiver with Model 3793A Differential Phase Detector plug-in. A simplified block diagram of the MLA system and its application to a microwave communications link is shown in Fig. 4.

The low-frequency sweep signal is a 70-Hz sine wave originating in the IF/BB transmitter. To this is added one of eight low-level, high-frequency baseband test signals from the BB transmitter plug-in. This combined signal can be applied to the system under test at the baseband level in place of the multiplexed telephone signal.

Alternatively, the sweep and baseband signals can be used to generate a 140-MHz IF signal, swept up to ±25 MHz across the IF band by the 70-Hz sine wave and modulated over a narrow band by the baseband signal. This signal can be applied to the IF channel of the transmission system.

At the receiving end, either the demodulated signal or the IF signal may be applied to the receiver. If the IF signal is used, the sweep and baseband signals are recovered by a precision demodulator within the receiver.

Filters separate the high-frequency and low-frequency components of the baseband signal. The low-frequency sine wave is used for the horizontal sweep of the CRT display and the high-frequency baseband signal is rectified to derive a dc voltage proportional to the baseband signal level. This is applied to the vertical deflection of the CRT.

If measurements are made between the IF-in and IF-out ports of the transmission system, the CRT then

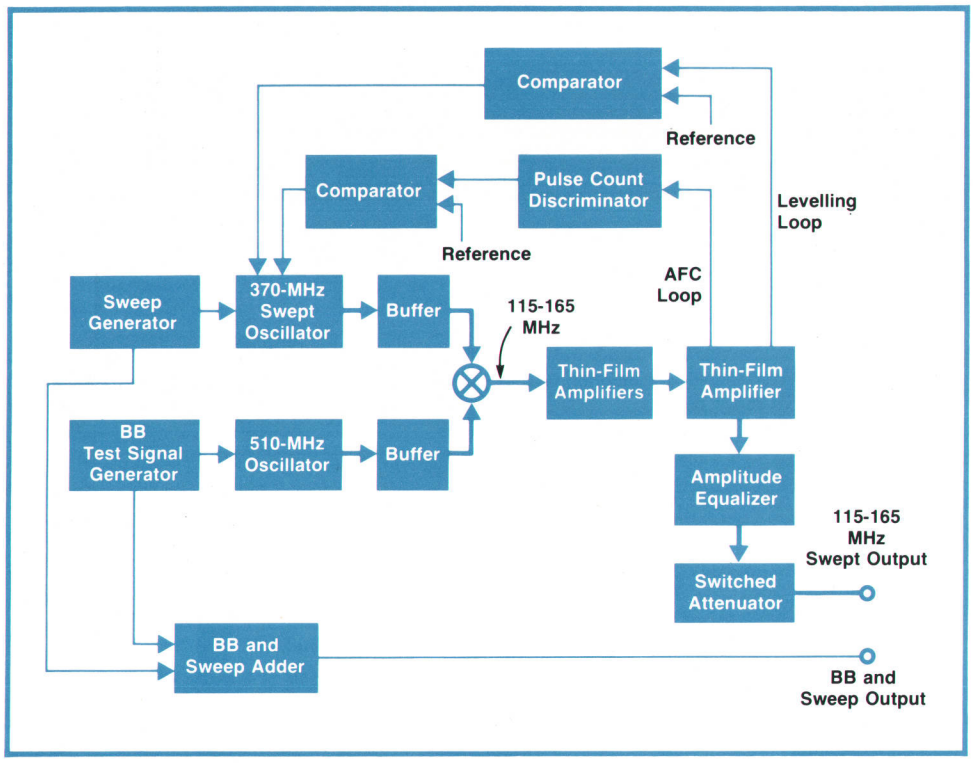


Fig. 5. *Block diagram of the transmitter. Low interaction between the sweep and high-frequency signals at the IF level is achieved by the use of two independent RF oscillators.*

displays IF differential gain or linearity. If measurements are made between BB-in and IF-out, it displays modulator linearity (allowing for IF response). Between IF-in and BB-out, it displays demodulator linearity. Between BB-in and BB-out, the display is of overall system linearity, if one of the lower-frequency test tones is used, or differential gain if one of the higher-frequency test tones is used.

The recovered high-frequency baseband signal is also compared in phase to a stable local oscillator that is phase-locked to the baseband signal average. The result of the comparison, a dc voltage, is applied to the CRT vertical deflection. The display then shows group or envelope delay if one of the lower-frequency baseband signals is used, or differential phase if a higher-frequency signal is used.

Driving the transmitter's modulator with the sweep signal alone enables measurements of IF amplitude response. Driving it with only a baseband test tone allows measurements of gain, attenuation and power.

The receiver is equipped with a meter that is used with an attenuator to give readings of average signal level, at either the IF or BB frequency. It is also used for readings of return loss when the facilities for that measurement are used (not shown in Fig. 4).

Technical Details

Bearing in mind the MLA measurement principle (Fig. 2), it is evident that the amplitude and phase of the high-frequency baseband test signal must not be disturbed by the high-level sweep signal during modulation. Low interaction is achieved by employing separate modulators for the two signals and forming a composite signal in a mixer.

The high-frequency test signal frequency modulates a 510-MHz oscillator and the 70-Hz sweep frequency modulates a 370-MHz oscillator, as shown in Fig. 5. The selection of oscillator frequencies was based on a computer-generated list of possible spurious mixer outputs, taking into account the receiver IF image frequency. Care was taken to prevent coupling between the modulation circuits for the two oscillators.

The two oscillator signals are applied to the mixer and the resulting difference frequency is the 140-MHz IF. Buffers between the oscillators and the mixer minimize the possibility of interaction so the IF modulation due to the high-frequency test tone is unaffected by the low-frequency sweep.

Following the mixer are two thin-film amplifiers having an amplitude flatness of 0.1 dB or better and group delay of less than 0.1 ns over a 50-MHz band of frequencies centered at 140 MHz. This performance is necessary to minimize distortion of the composite test signal. The first amplifier is located close to the mixer, presenting a resistive impedance to the mixer and a good match to the cable to the second amplifier. The second amplifier is located near the front panel so that the temperature-compensated levelling detector, which is on the amplifier substrate, can be close to the output connector.

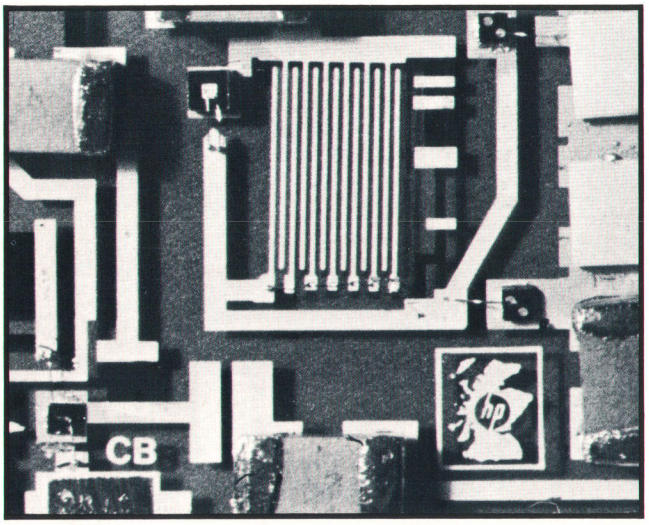


Fig. 6. *The amplitude response of the thin-film amplifier is adjusted by using a hand-held probe to remove the bonds that interconnect the arms of the thin-film interdigital capacitor (upper center).*

As would be required by any broadband amplifier that must have extremely flat amplitude response, means must be provided to allow compensation for production variances. This is accomplished by using a thin-film interdigitated capacitor, pictured in Fig. 6 and shown as C_c in the diagram of Fig. 7. To adjust amplitude response during production test of each amplifier, a hand-held probe is used to remove bonds to the digits one by one until the capacitance needed for the best response is obtained.

A broadband attenuator following the amplifier allows an output power range of +10 to −69 dBm in 1-dB steps with an accuracy of ±1 dB on all ranges (±0.5 dB at the +10 dBm output level).

Test Signal Generation

All the baseband test signals are derived from or locked to a 10-MHz master oscillator. The lower frequencies (83.3, 250, and 500 kHz) are derived by direct division of the master oscillator frequency. The higher frequencies (2.4, 4.43, 5.6, 8.2, and 12.39 MHz) are generated by an oscillator that has switchable crystals. This oscillator is phase-locked to the master by dividing its output down to 1 kHz and applying it to a sampling phase detector driven by the 10-MHz master oscillator. The resulting error signal phase-locks the switchable oscillator.

For the low-frequency sweep, a sine wave that has all harmonics >45 dB below the fundamental is synthesized by a 10-stage shift register. The input to the shift register is controlled by a flip-flop that loads the register with 1's when it is set, and loads it with 0's when it is reset. The outputs of all the shift-register stages are connected through weighting resistors to a summing point with the resistors chosen such that half a sine wave, from the trough to the peak, appears at the summing point as the shift register is loaded with 1's. When the first 1 appears at the output, the flip-flop is reset so 0's are then loaded, generating the other half of the sine wave. The first 0 appearing at the output then sets the flip-flop again for the next cycle.

The resulting waveform has a stepped appearance but the steps occur at the 1.4-kHz clock rate and are easily removed by low-pass filtering, leaving a low-distortion sine wave.

(text continued on page 20.)

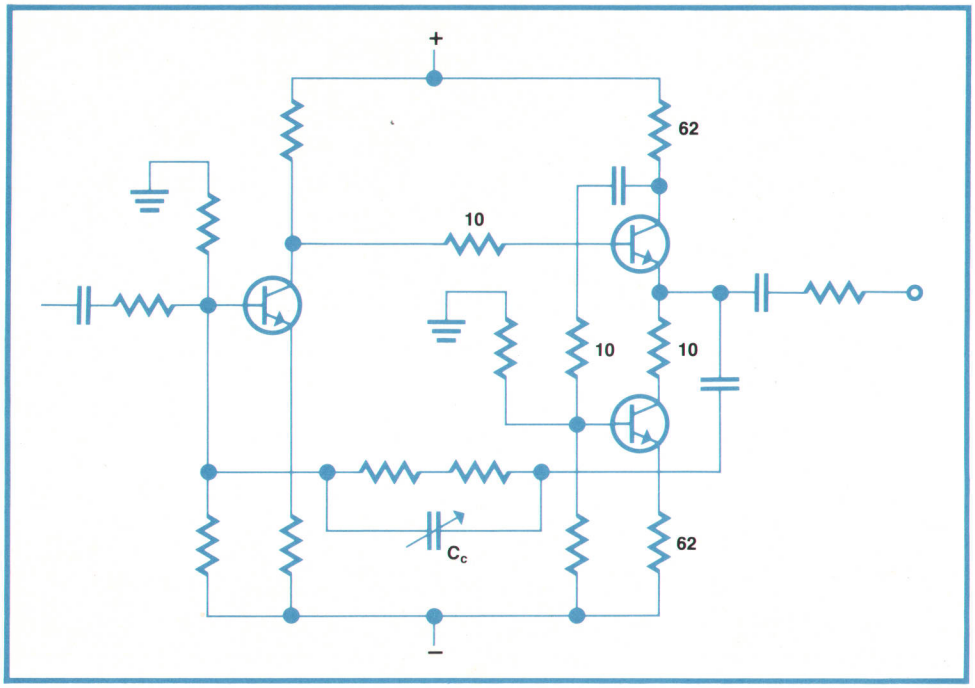


Fig. 7. *Circuit diagram of the IF amplifier output stage. Frequency response is optimized by adjusting feedback capacitor C_c. The final stage has a quiescent current of 45 mA giving +16 dBm output into 75Ω with second and third harmonic levels of −48 dB and −32 dB respectively at 165 MHz.*

The Detection of AM-to-PM Conversion by Means of High-Frequency Test Signals

There has been growing interest in recent years in distortions that can occur in wideband FM communications systems as a result of AM generated in a network being converted to PM in a nonlinear device that follows. The problem is, how to detect these so-called "coupled responses."

The following discussion, involving phasor diagrams and network phase and gain curves, deals with some physical mechanisms underlying the generation of differential gain and how it is affected by AM-to-PM conversion. A practical method for detecting AM-to-PM conversion is presented.

When a sweeping signal, centered for example at 140 MHz and carrying small-deviation frequency modulation (FM) at, say, 5.6 MHz is passed through an all-pass network such as a microwave-link group delay equalizer, the resulting plot of differential gain will be in the form of a "W". The network will have introduced AM and if in a device that follows AM-to-PM conversion occurs, the differential gain "W" will be asymmetrical. The appearance of asymmetry is the basis of this method of detecting AM-to-PM conversion.

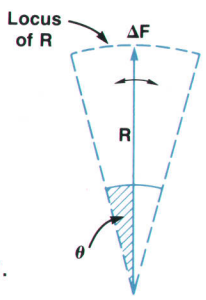


Fig. 1.

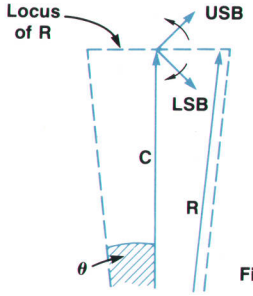


Fig. 2.

The Phasor Representation

Fig. 1 shows the phasor representation of a small-deviation FM signal. Since it is necessary to consider only phasor movements with respect to the carrier, rotation of the whole diagram counterclockwise at the carrier frequency has been stopped and only the back-and-forth oscillation at the modulating frequency remains. The maximum angular displacement, θ, of the signal phasor about its mean position is the phase modulation index. The maximum angular speed of the phasor determines the frequency deviation from the unmodulated carrier value. For sinusoidal modulation, maximum frequency deviation occurs at the central position. The locus of the tip of the phasor is the arc of a circle.

In Fig. 2, the first order lower sideband (LSB) is shown going backwards (clockwise) as time advances, while the upper sideband (USB) moves forward or counterclockwise, both rotating at the modulating frequency. The sum of the carrier phasor C and the two sidebands is the resultant R, also shown in Fig. 1. However for simplicity, the locus of the tip of the sweeping phasor R is now shown as a straight horizontal line.

Nonlinear Phase

Fig. 3a and 3b introduce the effect of nonlinear phase. In passing through a network having the phase curve shown, the sidebands are phase-shifted relative to the carrier by +8° and −10° respectively. A linear phase response that gives shifts of +10° and −10° would be equivalent to a pure time delay that would cause no distortion but when the LSB is given a counterclockwise displacement of 8°, the result is a tilting of

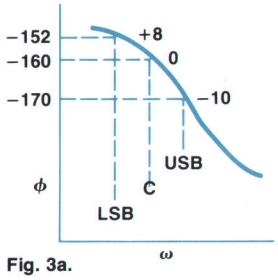


Fig. 3a.

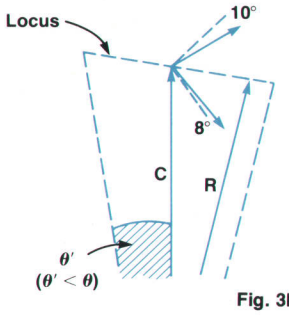


Fig. 3b.

the phasor locus and a slight reduction in the maximum phase deviation.

The phasor, still oscillating with a fixed period of *time* determined by the modulating frequency, now travels a slightly reduced angular *distance* and therefore moves with reduced *speed*. Since phasor speed is frequency deviation, *the peak frequency deviation is reduced*. Since a frequency discriminator, such as a microwave link demodulator, responds only to phasor speed or frequency deviation, the discriminator output is also reduced, giving rise to differential gain as the carrier frequency, ω, is swept.

Note that the maximum length and the maximum angular deviation of the resultant occur at the same time. The AM is in phase with the signal PM. If AM-to-PM conversion were to occur, with the PM in phase with the AM as it would be in a diode limiter, the generated PM would be in phase with the signal PM and would therefore affect its value; that is, AM variations would cause differential gain in an FM system. This is accounted for by the fourth term of equation 1, given later.

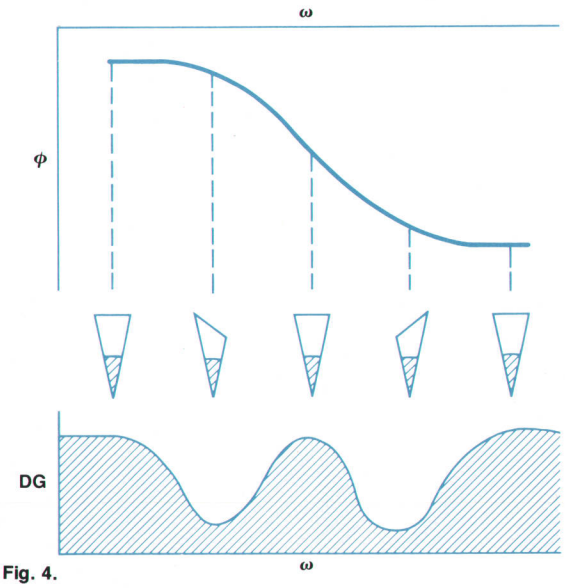


Fig. 4.

The Network Phase Curve

Fig. 4 is a plot of differential gain as the FM signal carrier frequency is swept over the phase curve of an all-pass network. At regions of maximum phase curvature, the phase and frequency deviations are reduced giving a dip in demodulated output. At the point of inflection of the phase curve, where the carrier and first order sidebands can lie on a straight line, there is

no phase distortion of the first order sidebands, no tilting of the phasor locus, and no reduction in phase or frequency deviation. Second order sidebands would not lie on the straight line and so would be phase-distorted, causing a slight reduction in the central peak of the differential gain curve.

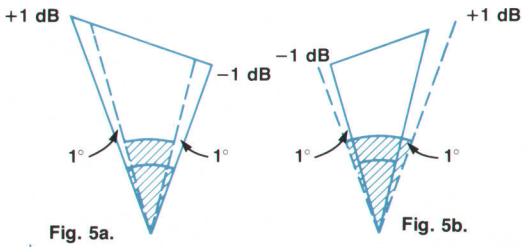


Fig. 5a.

Fig. 5b.

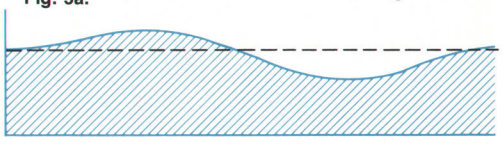


Fig. 5c.

AM-to-PM Conversion

In Fig. 5 the askew triangles of Fig. 4 are enlarged and the effect of +1° per dB of AM-to-PM conversion is added. Fig. 5a shows a 1-dB increase in phasor length on the left. This is a *positive* increment of AM and so 1° is *added*, giving a counterclockwise shift. On the right of Fig. 5a the phasor length is reduced by 1 dB. This is a *negative* increment and so 1° is *subtracted*, giving a clockwise shift. The overall result in Fig. 5a is an increase in phase deviation and frequency deviation. The phase and frequency deviations are decreased in Fig. 5b by a similar argument. The differential gain (DG) resulting from AM-to-PM conversion is shown in Fig. 5c.

In Fig. 6, the differential gain contributions of Fig. 4 and 5 are added, giving the asymmetrical "W" form typical of an all-pass network followed by a device that gives AM-to-PM conversion. This appearance of asymmetry is the basis for detecting the presence of AM-to-PM conversion.

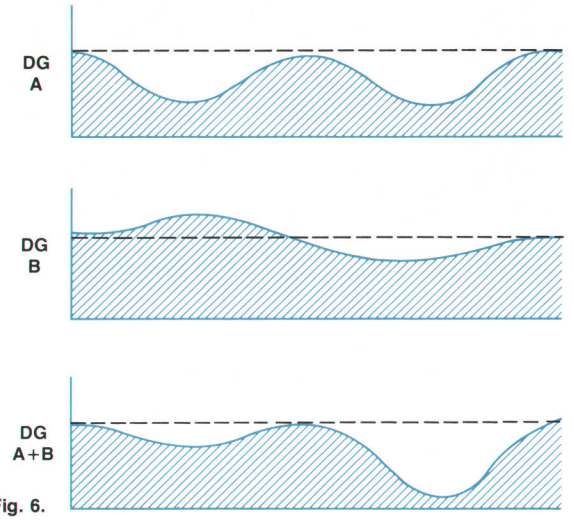


Fig. 6.

The Effect of Network Gain Slope

In Fig. 7 the effect of a gain slope alone is dealt with. There is no phase distortion, only changes in phasor lengths. The USB is attenuated relative to the LSB. When the USB and LSB are in line and in opposition they no longer cancel exactly so an elliptical locus results.

Note that since the maximum length of the resultant occurs

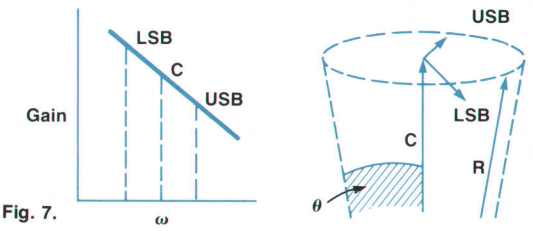


Fig. 7.

at zero angular deviation, the AM is in phase quadrature with the signal PM. In this case, PM resulting from AM-to-PM conversion is in phase quadrature with the signal PM and shifts the phase of the signal PM, leaving the signal phase-modulation index unchanged. AM variations resulting from non-flat gain therefore give rise to differential phase but not differential gain. This is shown analytically by the second term of equation 2.

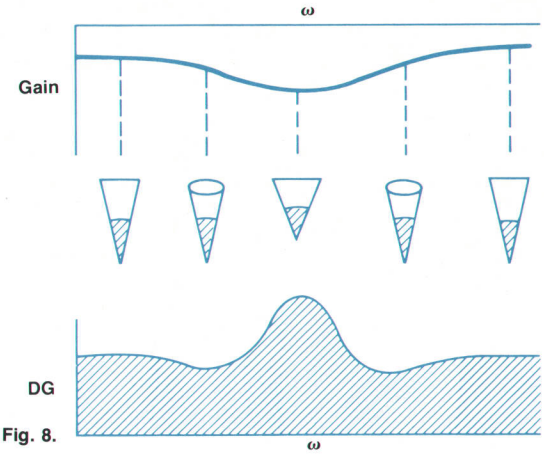


Fig. 8.

Network Gain Dip

Fig. 8 shows a gain dip in an all-pass network resulting from component loss. At the center of the gain dip, the carrier is attenuated relative to the sidebands, which are themselves of equal amplitude. The phasor triangle is compressed giving an increase in phase deviation and therefore in frequency deviation. The network gain dip gives a differential gain peak that is symmetrical about the center of the gain dip. Analytically, the gain dip is accounted for by the second term of equation 1.

The test for AM-to-PM conversion is not invalidated by the gain dip provided that the latter coincides with the center, or inflection point, of the network phase curve. This is the point of maximum group delay. No asymmetry is introduced. An off-center gain dip, however, will cause asymmetry in the absence of AM-to-PM conversion. AM-to-PM conversion in a test item is then indicated by a change in the asymmetry.

Quantitative Results

Two methods have been used to quantitatively relate the AM-to-PM conversion coefficient with differential gain symmetry. One is analytical while the other is a computer simulation of the network, AM-to-PM conversion, and FM signal, giving, as output, a plot of differential gain. A brief review of the first method is given here.

Terms of the following equation have already been published and discussed.[1,2] Here the terms, separately and in combination, are plotted for a typical network to show their contribution to differential gain. The plots are seen to have the same form as those predicted by the phasor diagram approach (Fig. 9).

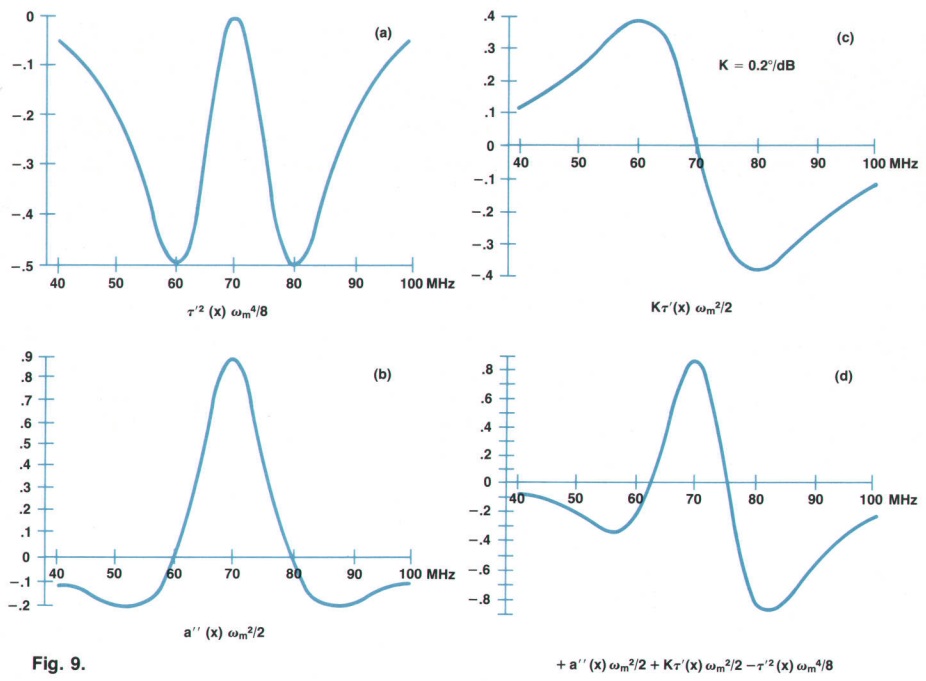


Fig. 9.

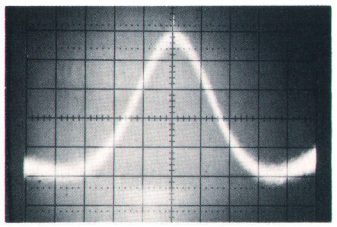


Fig. 10(a). *Differential gain display generated by an all-pass network with no following AM to PM conversion. The "W" form arising from the phase curve is superimposed on a central peak due to the network gain dip which itself results from component loss.*

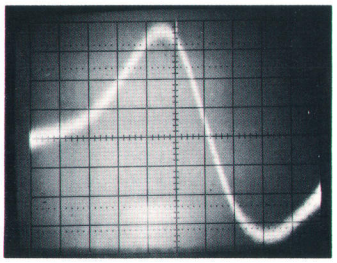


Fig. 10(b). *Differential gain display having the two contributions of (a) with the additional asymmetrical contribution arising from AM to PM conversion. The appearance of this asymmetry is the basis of the method for detecting AM to PM conversion.*

$$DG(x) = 1 + \alpha''(x)\,\omega_m^2/2 + K\tau'(x)\,\omega_m^2/2 - \tau'^2(x)\,\omega_m^4/8 \quad (1)$$

$$DP(x) = \tau(x)\omega_m - K\alpha'(x)\omega_m \cdots\cdots \quad (2)$$

where

DG(x) is the baseband differential gain characteristic

DP(x) is the baseband differential phase characteristic.

$\alpha(x)$ is the normalized amplitude response of the network

$\tau(x)$ is the group delay of the network

x is the swept carrier frequency

K is the AM-to-PM conversion arising in the system under test

$\omega_m/2\pi$ is the test frequency

', '', are the first and second derivatives.

The example is taken of an all-pass network having a parabolic group delay response of 7 nsec over ±10 MHz centered at 70 MHz, and having a gain dip of 0.45 dB centered at 70 MHz. A computer program evaluates a'' and τ' from the network singularities, and generates the plots shown in Fig. 9. Fig. 9(b) and (d), without and with AM-to-PM conversion respectively, should be compared with the photographs in Fig. 10 (a) and (b) which show differential gain displays on a Microwave Link Analyzer.

Ian Matthews

References

1. R. Coackley, "Characterization of Microwave Radio Links," National Telecommunications Conference, Houston, Texas, December 1972.

2. "Differential Phase and Gain at Work," Hewlett-Packard Application Note 175-1.

Receiver Circuits

The main function of the IF/BB receiver is to derive from the input signal information that can be used for quantitative display of disturbances in phase and level of the baseband signal, disturbances that arise from nonlinearities in the system under test. If the system under test supplies the baseband signal to the receiver, the low-frequency sweep and the high-frequency test signal are separated by straightforward filtering and appropriately amplified for detection and use by the display.

In the IF portion of the receiver, the amplifier following the input attenuator is a thin-film type to minimize the distortion that would arise from non-flat group delay and amplitude response. The input common-base stage presents a return loss of better than 38 dB to the input attenuator and serves as a buffer to the thin-film balanced detector that follows. The response of this detector is flat within 0.02 dB over an input range of 115 to 165 MHz.

The heart of the IF portion is the tracking demodulator, shown in Fig. 8. To provide useful measurements, this must be more linear than any demodulator likely to be encountered in a communications system.

High demodulator linearity is achieved in effect by heterodyning the incoming signal with a frequency-following local-oscillator signal to give a nearly-constant difference frequency of 17.4 MHz. The difference frequency is applied to the frequency discriminator and the discriminator output is used as an error signal to control the local oscillator, maintaining the 17.4-MHz difference.

The gain around the frequency control loop is 80

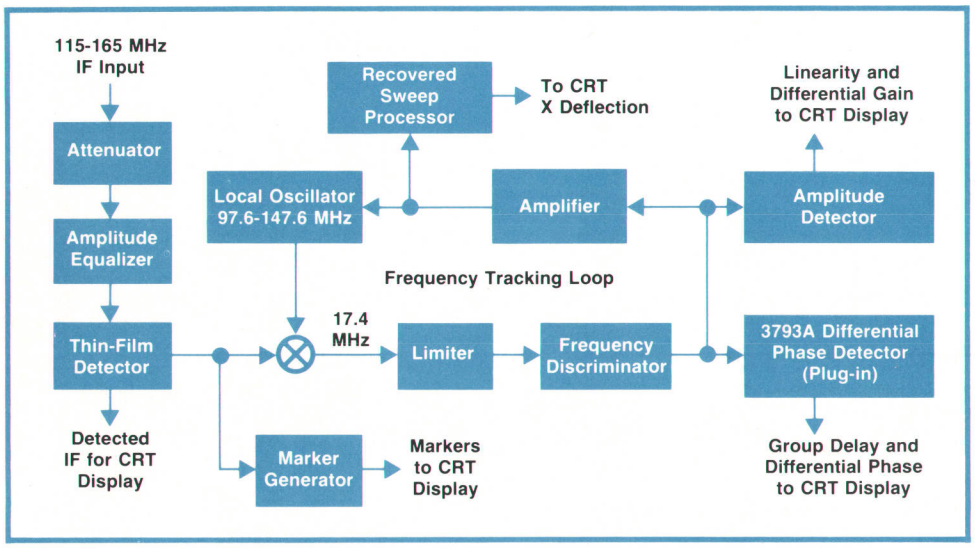


Fig. 8. *An IF signal is processed through a tracking demodulator in the receiver, recovering the high-frequency test signal with high fidelity.*

dB so a 50-MHz frequency variation of the IF signal is reduced to 5 kHz at the discriminator input. This residual sweep is small enough to give, in effect, a demodulator of high linearity since discriminator nonlinearities are not being traversed by the 17.4-MHz IF. The baseband test signal is thus faithfully reproduced at the discriminator output. Baseband test signals as high as 5.6 MHz are recovered with low distortion by this method.*

Precision Sweep

The control signal applied to the tracking-loop's local oscillator is, of course, comparable to the 70-Hz sweep but because of nonlinearities in the oscillator's frequency/voltage characteristics, it is not a pure sine wave. A pure sine wave is required, however, to maintain a linear frequency scale for the horizontal axis of the CRT display. Therefore, a sine wave is synthesized in a separate circuit and phase-locked to the 70-Hz error signal.

The sine wave is synthesized in the same manner as in the transmitter but with the phase-lock error signal controlling the clock oscillator. However, precise synchronization is required so the display's horizontal axis can be related to frequency. The question now arises, where on the recovered sweep waveform is synchronization to be accomplished? Because of the nonlinearities of the waveform, the only points where voltage can be precisely related to frequency are at the maximum and minimum values (waveform points B and D in Fig. 9).

Pinpointing the location of these points is difficult, however, because of the near-zero rate of change around these points. Instead, two points where the steep-rising parts of the waveform intersect a dc voltage are detected (points A and C). The time interval between the two points is measured and half this value is used to locate the time of occurrence of point B. The zero-level axis was arbitrarily chosen for points A and C although any other level could have been used because of the symmetry of the waveform about B.

As shown in the diagram, a limiter squares the recovered sweep waveform to delineate points A and C more sharply, and the squared waveform gates clock pulses to a counter. When the waveform terminates the count, the result retained in the counter is shifted one place as it is transferred to a storage regis-

* If either the 8.2- or 12.39-MHz test signals is used, an external wideband demodulator must be employed if IF-to-IF or BB-to-IF measurements are to be made.

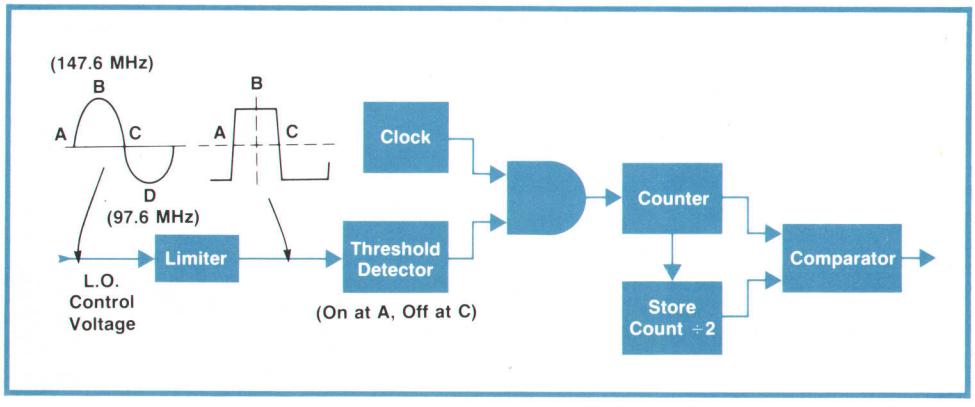


Fig. 9. *Recovered-sweep processor precisely locates the peak B of the recovered 70-Hz waveform by measuring the time between points A and C and dividing by two.*

ter, effectively dividing the count by two. On the next cycle, the stored count is compared to the instantaneous count in the counter and when the two are equal, a trigger pulse is generated. The stored count is then updated.

Phase-locked to this trigger is the sine wave generated by the shift-register synthesizer.

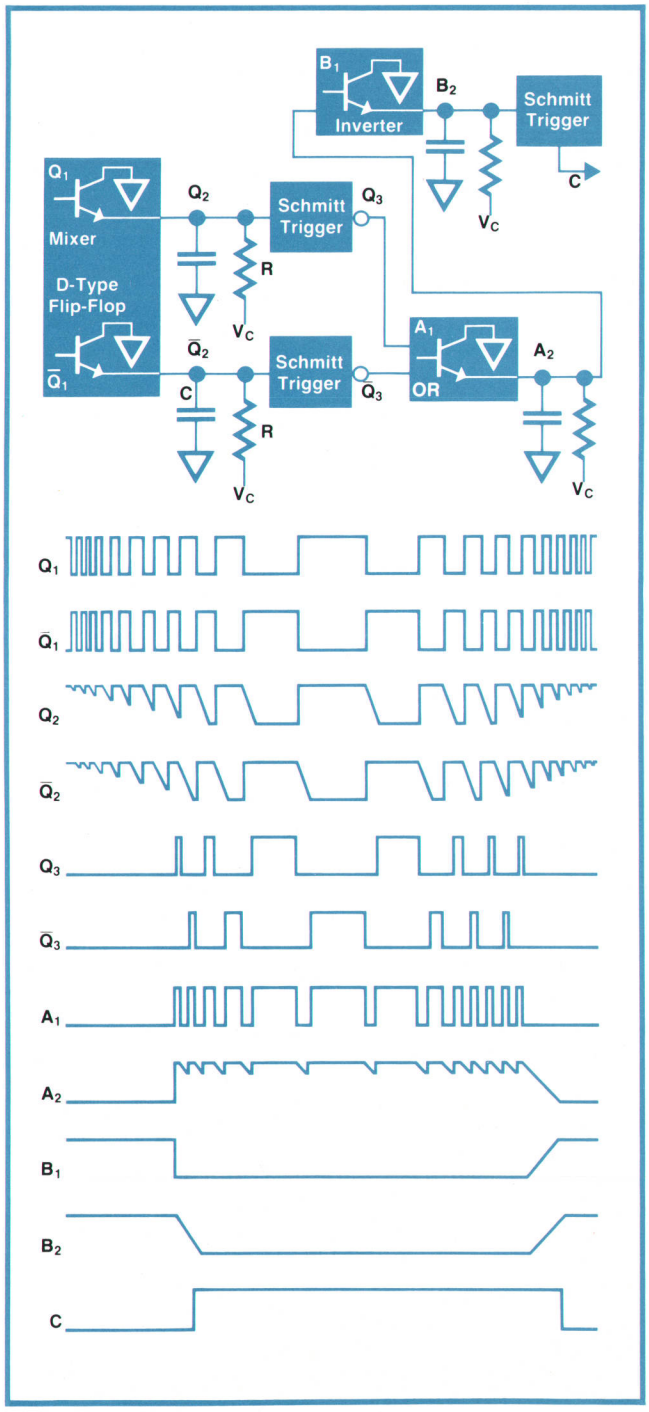


Fig. 10. *Marker generator uses a D-type flip-flop as a mixer to derive a pulse that spans the zero beat between the incoming signal and a reference.*

Markers

For calibrating the frequency scale of the CRT display in terms of IF frequency, two types of markers are provided. One type is a crystal-controlled frequency comb that puts pulses on the CRT trace at either 2-MHz or 5-MHz intervals. The other is a single marker that can be moved along the trace to identify the frequency of any point on the frequency scale. The control that positions this marker has a four-place digital readout that gives precise indication of marker frequency over a range of 115 to 165 MHz.

The marker generation technique is based on the detection of zero beats between the incoming signal and a locally-generated signal of known frequency. The circuit design was influenced by two factors: (1) marker generation must not be affected by the FM signals' sidebands, and (2) marker width should not be affected by a change in sweep width. The first factor is dealt with by substituting a local oscillator signal for the incoming IF and phase-locking the oscillator to the IF signal. The bandwidth of the frequency control loop is restricted so the local oscillator tracks the sweep but not the relatively high-frequency FM.

Marker width control, the second factor, is accomplished in the circuit shown in Fig. 10. This uses an ECL D-type flip-flop as a mixer with the incoming signal applied to the D input and the locally-generated reference applied to the clock input. The normal output of such a circuit in the vicinity of a zero beat is shown by waveform Q1 and $\overline{Q1}$ in Fig. 10. The flip-flop outputs, however, drive capacitors (C) that are charged quickly by transistor pull-up, but that discharge more slowly through resistors (R), thus giving the waveforms Q2 and $\overline{Q2}$. Hence, the Schmitt trigger circuits are triggered only when the width of the Q1 and $\overline{Q1}$ pulses is wide enough to allow the voltage on C to fall to the trigger level.

The Schmitt trigger outputs (Q3 and Q3) are OR'd to get waveform A1, which also drives a capacitor circuit obtaining waveform A2. This waveform is inverted and smoothed (B1) and used to drive the output Schmitt trigger. The Schmitt output is a single pulse that spans the zero beat.

Marker width is controlled by varying the voltage V_C, which controls the rate of capacitor discharge. A steeper discharge for C causes the first Schmitt circuits to trigger both earlier and later in the zero-beat cycle, widening the output pulse.

The automatic marker width control varies V_C to keep the marker width constant at 2 mm of display for IF sweep widths from 10 MHz to 50 MHz. Below 10 MHz, the markers widen, reaching 10 mm typically at a 3-MHz sweep width.

When the instrument is used in the spectrum display mode to check the modulation index of an FM signal by the carrier-null method, the phase-lock loop

is opened and the local oscillator is controlled by an internally-generated sweep-voltage. The LO signal is mixed with the incoming FM signal and the result is low-pass filtered, giving a display of the spectrum of the incoming signal. The markers can also be added to this display.

Phase Detector

Measurements of group delay and differential phase are made by phase-comparing the high-frequency test signal, separated from the sweep signal in the receiver, to the output of a crystal-controlled oscillator. To avoid the effects of slow drift, the crystal-controlled oscillator is phase-locked to the test signal, the bandwidth of the loop being restricted to 10 Hz so as not to affect the wanted phase information which occurs at 70 Hz, the sweep rate.

As shown in the block diagram of Fig. 11, the output of the 1-MHz crystal oscillator is divided down to match the frequency of the lower test frequencies (83.3, 250, and 500 kHz) for phase detection. The higher test frequencies are heterodyned down to 250 kHz for comparison with the phase-locked oscillator frequency divided by four. The oscillator used for the down-conversion uses switched crystals for stable frequency control.

The phase display is calibrated by switching in a fixed delay on alternate sweeps. The CRT then displays two phase traces, with the vertical separation determined by the amount of added phase.

The calibrated phase delays are achieved with switched RC networks. Since frequency deviation and phase modulation are not changed by mixing the higher test frequencies down to 250 kHz, the phase calibration steps hold for all these frequencies in terms of degrees or radians. The lower frequencies are passed directly through the phase delays without mixing and are therefore given in nanoseconds of delay.

Amplitude displays are calibrated by switching a precision attenuator into the signal path on alternate sweeps.

Acknowledgments

The need for a 2700-channel measurement capability was foreseen by David Ford, product manager, and Mike Crabtree, radio group manager, and confirmed by Roger Brownhill's market research. Mike, along with Colin Appleyard, project leader until his promotion to group leader, defined the product. Product design was by Owen Livingstone. The precision sweep generator was contributed by Andy Batham. Ian Harrison worked on the test-signal oscillators as well as dealing with many of the lab prototype problems. Brian Woodroffe helped with the product transfer administration and Hugh McNab handled the transfer to production. Thanks are particularly due the members of the Thin-Film Lab for their ready and energetic cooperation.

Reference

1. R. Urquhart, "A New Microwave Link Analyzer with High-Frequency Test Tones," Hewlett-Packard Journal, September 1972.

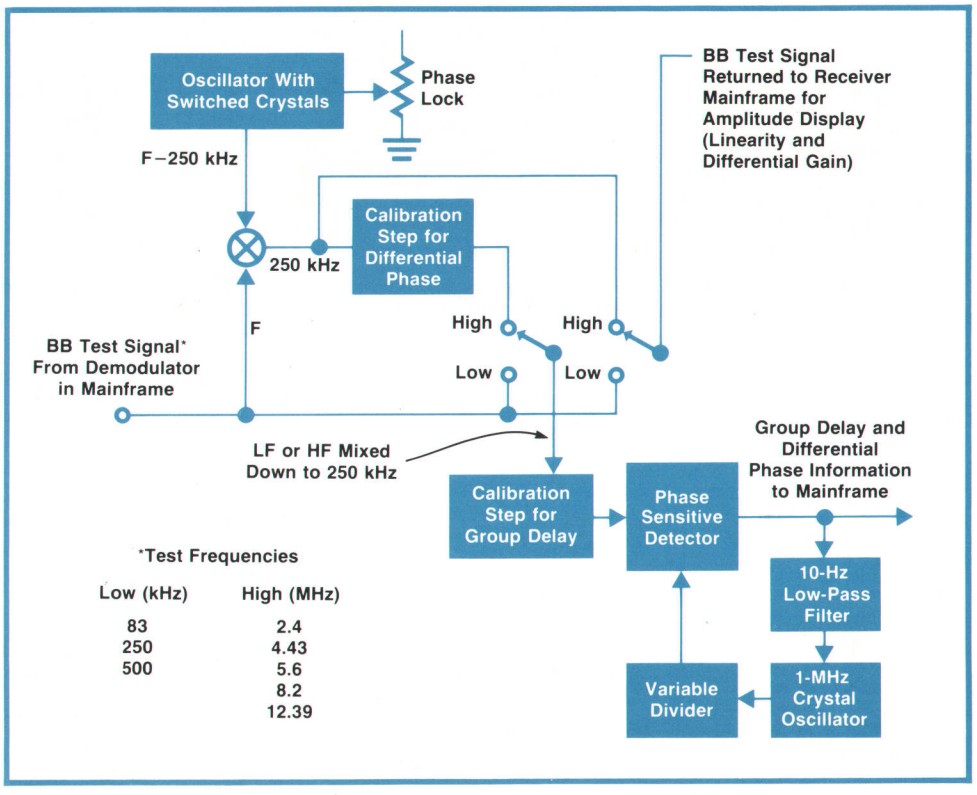


Fig. 11. *Block diagram of the phase detector in the Model 3793A Differential Phase Detector plug-in. Phase comparisons are made against a stable, 1-MHz, crystal oscillator that is phase-locked to the average phase of the incoming signal.*

ABRIDGED SPECIFICATIONS

HP Model 3790A/3792A Microwave Link Analyzer

MEASUREMENTS:
Group Delay
Modulator linearity and sensitivity
Demodulator linearity and sensitivity
Differential Phase
Differential Gain
IF Amplitude Response
IF Return Loss
BB Return Loss
Frequency spectrum
Power, gain, and attenuation

SWEEP FREQUENCIES: 70 Hz, line or EXT (40-100 Hz)

BASEBAND FREQUENCIES: 83.333, 250, 500 kHz, 2.4, 3.58 (4.43), 5.6, 8.2, 12.39 MHz, EXT 80 kHz to 15 MHz with demodulation to 5.6 MHz.

BASEBAND DEVIATION: 0.5 to 500 kHz rms.

SPECTRUM MODE: ±25 MHz centered between 135 and 145 MHz.

IMPEDANCE: 75Ω

POWER: 110, 120, 220, 240V, +5%, −10%, 48-66 Hz. 150 VA (3790A) + 190 VA (3792A).

TEMPERATURE (operating): 0 to 50°C

WEIGHT (with plug-ins): 3790A, 18 kg (39.25 lb); 3792A, 22.5 kg (49.25 lb).

DIMENSIONS: 3790A, 425 mm W × 172 mm H × 457 mm D (16.75 × 6.75 × 18 in); 3792A, 425 mm W × 216 mm H × 457 mm D (16.75 × 8.5 × 18 in).

PRICES IN U.S.A.: 3790A/3791A, $11,065
3792A/3793A, $10,965

MANUFACTURING DIVISION: HEWLETT-PACKARD LTD.
South Queensferry
West Lothian,
Scotland

SWEPT FREQUENCY (back-to-back)

Measurement Capability	IF Range (MHz)	Range	Maximum Sensitivity	Maximum Inherent Slope		Maximum Inherent Noise (rms)			
				BB-BB	IF-IF	BB Freq	BB-BB at −40 dBm	IF-IF	
IF Response	115 to 165	0 to ±3 dB via Y1 0 to ±3 dB via Y2	0.025 dB/cm	—	±0.05 dB at +5 dBm, ±0.1 dB from +5 to +10 dBm at input to 3792A.	—			
BB Linearity & Differential Gain	125 to 155 115 to 165	0 to 50%	0.25 %/cm	0.1%	0.2% 0.4%	—			
Group Delay	125 to 155 115 to 165	200 ns	0.25 ns/cm	0.1 ns	0.2 ns 0.5 ns 1 ns at 83 kHz	83.333 kHz 250 kHz 500 kHz	1.2 ns 0.4 ns 0.2 ns	0.6 ns 0.2 ns 0.1 ns	200 kHz rms dev.
Differential Phase	125 to 155 115 to 165	18° or 31.4% rad.	0.5°/cm	0.1°	0.2° 0.5°	2.4 MHz 4.43 MHz 5.6 MHz 8.2 MHz 12.39 MHz	0.2° 0.2° 0.2° 0.4° 0.4°	0.1° 0.1° 0.1° † †	500 kHz rms dev.
IF Return Loss	115 to 165	10 to 49 dB (Accuracy depends on hybrid used)	1 dB/cm	—	1 dB	—			

Ian Matthews

Ian Matthews joined HP Ltd. in 1968 following eight years in microwave radio link development in Canada and the U.S.A. He contributed to the Model 3710A MLA and to the 510-MHz oscillator, thin-film components, and attenuator of the Model 3790A before taking on project leadership. Ian earned a BSc degree with honors in physics from Aberdeen University and a MSc degree in digital techniques from Heriot-Watt University. He has also done graduate work at Stanford University, California. Married with two daughters aged 8 and 10, he enjoys family camping, hill walking, and golf.

Svend Christensen

As a student, Svend Christensen did summer work at HP Ltd., Scotland, and then on obtaining his degree (Teknikum Ingeniør) from the Teknikum, Sønderborg, Denmark, returned full-time in 1973. First he undertook the development of the MLA marker circuits and then became involved with the MLA systems aspects, also contributing to the design of the 140-MHz programmable attenuator. He is now engaged in new product investigation. Scottish weather permitting, Svend's leisure activities include golfing, cycling, and photography. He is married and has two daughters, 3 and 5.

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