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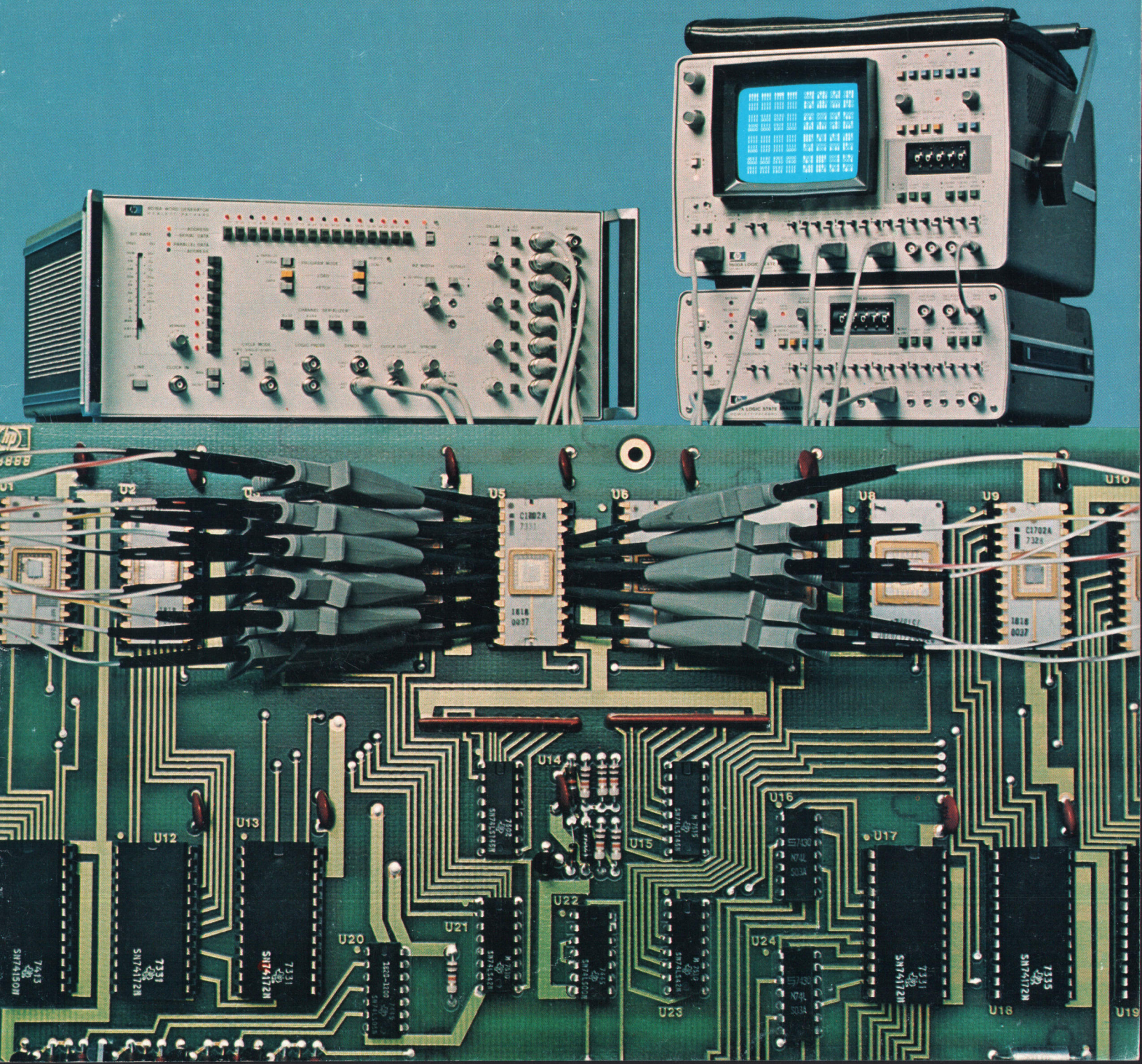


The Logic State Analyzer, a Viewing Port for the Data Domain

A new logic state analyzer has expanded capabilities that speed the location of the sources of problems in digital systems and broaden the range of problems that can be resolved with this class of instrument.

by Charles T. Small and Justin S. Morrill, Jr.

ENGINEERS DEVELOPING DIGITAL systems—especially those that involve microprocessors—now find themselves more concerned with word flow than with waveforms. But until recently, it was considerably more difficult to perceive word flow within an operating system than it was to view waveforms.

This situation was improved two years ago when a new kind of instrument, the parallel-mode logic state analyzer, was introduced.[1] The first of these instruments, the Hewlett-Packard Model 1601L, monitored data buses or other multinodal locations in a digital system, "captured" a sequence of digital words as it occurred there, and displayed the sequence as a table of 1's and 0's.

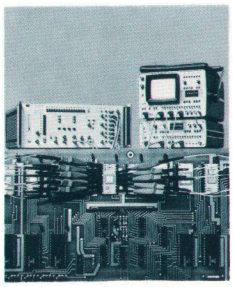
With the insight provided by this instrument, it became much easier to trace data flow and track down problems in digital systems. Digital designers who have had the opportunity to use this instrument now find it indispensable for analyzing and troubleshooting the digital systems on which they are working.

New Directions

Two years' experience with the Model 1601L has uncovered a number of additional capabilities that such an instrument might have. These capabilities have now been incorporated in a new logic state analyzer, Model 1600A, which works with or without a companion instrument, Model 1607A.

Basically, the Model 1600A (Fig. 1) works like the earlier Model 1601L: digital data appearing in parallel on several different lines is monitored through a multi-probe system and clocked into the instrument in synchronism with the clock or other pulses from the system under test. When a preselected trigger word appears on the data lines, the instrument stores the trigger word and the next 15 words and then displays the stored data in tabular form. Digital delay may be introduced making it possible to view the 16 words that occur as many as 99,999 clock periods after the trigger. Alternatively, the instrument may be set to store data continuously and then stop acquiring data when the trigger occurs. The 15 words leading up to the trigger word are thus captured for study.

Data acquisition and display cycles may alternate repetitively, or data may be acquired once and then displayed continuously until the RESET pushbutton



Cover: *Multichannel is the byword as new test instruments are developed in response to the accelerating rush to digital electronics. Described in this issue is the latest logic state analyzer, which gives a multiport view of what's happening in an operating digital system, and an eight-channel word generator for supplying the multichannel bit patterns needed for digital testing.*

In this Issue:

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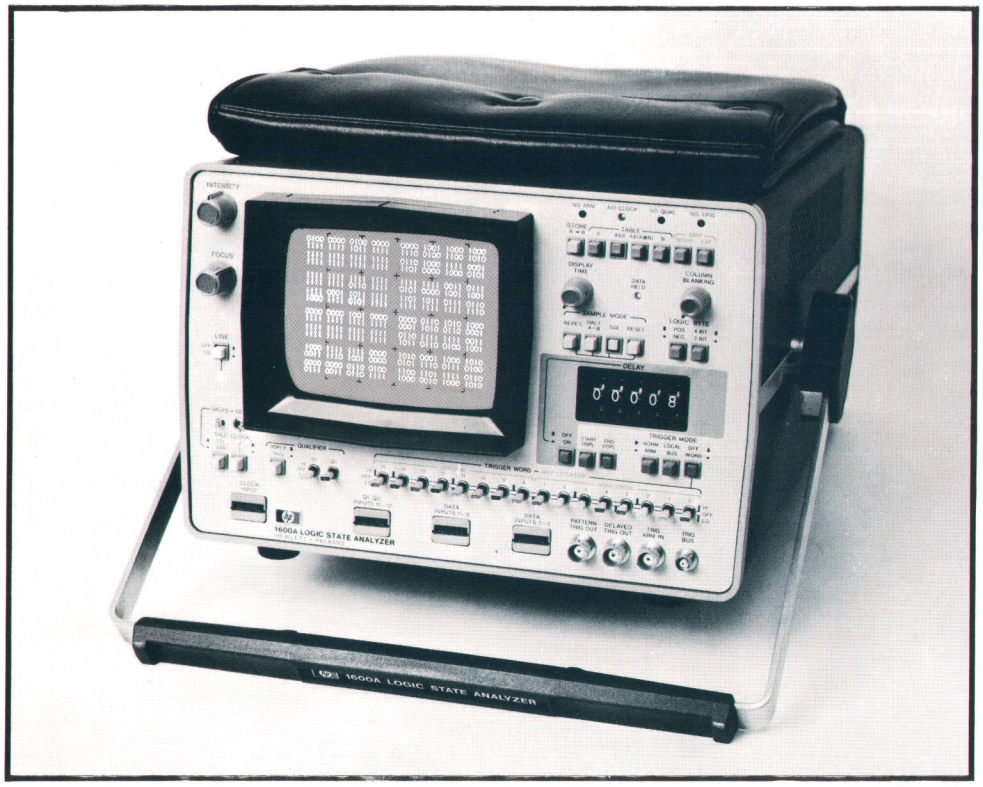

Fig. 1. *Model 1600A Logic State Analyzer monitors digital data appearing on as many as 16 lines and displays the data as words of 1's and 0's in tabular form running from top to bottom on the left half of the display. The right half of the display is used for data stored in an auxiliary memory or for data acquired by a companion instrument, the Model 1607A.*

is pressed, initiating a new data acquisition cycle.

The trigger may be any of the words in the data stream. A front-panel switch register enables the user to select the word that serves as the trigger. It is thus possible to view any part of an executing digital program by using the first word of the sequence as a trigger. The delay capability may be used to page through long sequences. Or, the digital sequence leading up to an unallowed state caused by a fault may be examined, using the unallowed word as the trigger.

The trigger word also causes the instrument to generate an output pulse that can serve as a trigger for an oscilloscope or other instruments in a test set-up. This makes it possible to view the waveforms that occur at a defined point in time with respect to the trigger word.

To provide flexibility in applications of the instrument, data may be clocked in on either the positive-going or negative-going edge of the clock pulses, the data may be interpreted as either positive-true or negative-true logic, and the logic threshold is adjustable. The miniature probe system developed for the Model 1601L, which facilitates making the many closely-spaced connections to the circuit under test, is also used with the new logic state analyzer (Fig. 2).

Branching Out

The new Model 1600A Logic State Analyzer broadens this basic capability by being able to look at 16 lines simultaneously, four more than the 12-bit capability of the earlier Model 1601L. When working with Model 1607A, Model 1600A can look at and display data appearing at 32 points (Fig. 3).

Two qualifier inputs have been added. When used in the QUALIFIER DISPLAY mode, these make it possible to be selective in clocking data into memory. For example, when monitoring a multi-use bus that has time-multiplexed addresses, instructions, and data, only the information pertinent to a particular operation need be stored for display.

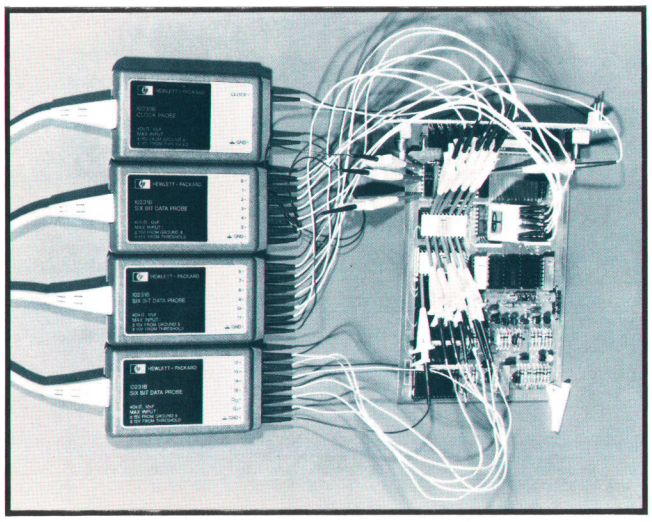

Fig. 2. *Miniature probes facilitate connections to closely-spaced test points. The probes are connected through short leads to input circuits within the pods to minimize circuit loading.*

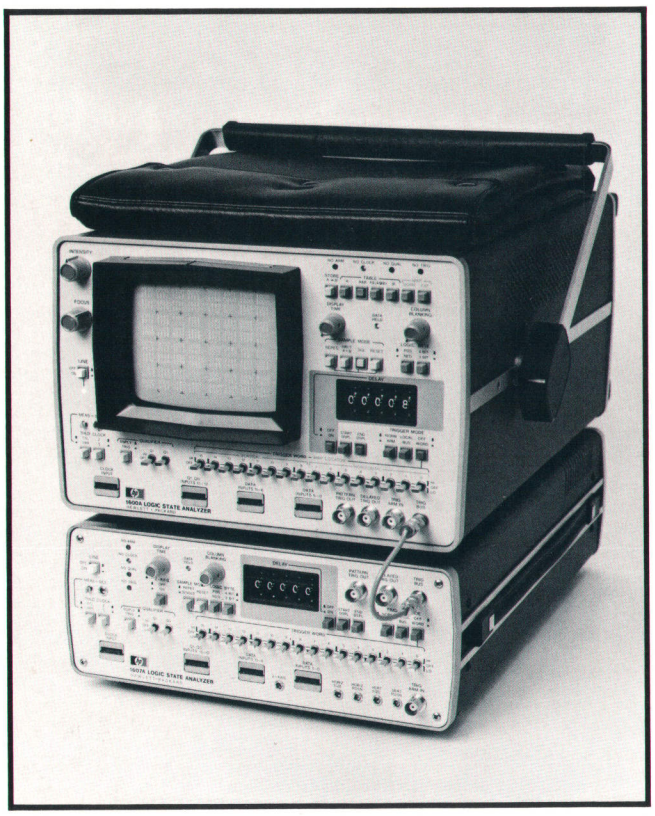

Fig. 3. *Models 1600A and 1607A Logic State Analyzers work together to monitor and display 32-bit words, or work with independent clocks to examine the interaction between two digital machines. The combination of the two instruments is known as the Model 1600S. Model 1607A has most of the capabilities of Model 1600A and can work by itself using an oscilloscope or CRT monitor for the display.*

The two qualifier inputs may also be used with the trigger word, in effect giving an 18-bit trigger word.

Data may be clocked in at rates up to 20 MHz. This speed allows tests to be conducted at the full operating rate of most digital systems, thereby uncovering faults caused by circuit response—faults that do not occur when a system is tested by single-stepping it at a slow rate.

Positioning of the trigger word on the display has been made more flexible in the new instrument. As before, in the START DISPLAY mode, the trigger word appears at the top of the displayed table and the next fifteen words follow below. In the END DISPLAY mode, the trigger word appears at the bottom with the previous fifteen words above. In either case, the trigger word is brightened to show its position. Now the digital delay may be used with the END DISPLAY as well as the START DELAY mode, making it possible to display events both prior to and immediately following the trigger word. The word at the top of the display is the word that occurs fifteen clock periods before the trigger word minus the selected delay. If the delay is less than fifteen, the trigger word appears brightened part way down the display.

Another added display mode is known as partial display. This occurs automatically whenever the rate of the clocks qualified by the DISPLAY qualifiers is below 60 Hz. If the instrument is in the START DISPLAY mode, the display shows the trigger word as soon as it occurs (or the first word following the selected delay) and fills in each successive word as it is clocked in. Previously the user had to wait for sixteen words to accumulate before the display would show what had occurred.

In the case of partial display in the END DISPLAY mode, each word is entered at the bottom of the display, pushing the others up. When the display is full, each new word entering at the bottom pushes the top word off the display. This continues until trigger conditions are met.

An "arm" mode is now provided for the trigger. In this mode, the instrument does not respond to the trigger word unless armed by a pulse at its ARM input. This prevents the data acquisition cycle from being initiated until some other event occurs.

Dual Data

Model 1600A has an auxiliary memory for storage of data. A front-panel pushbutton (STORE A → B) transfers the data stored in the main memory (A) to the auxiliary memory (B). The contents of each memory may be displayed separately or both may be displayed side by side for comparisons.

To make it easier to compare stored data with new data, a comparison mode [A & (A⊕B)] may be selected. The contents of the A memory are then displayed on the left half of the display while the right half shows how the contents of B differ from A—bit positions where the two memories are identical are displayed as 0's, and bit positions where they differ are displayed as 1's (Fig. 4). In addition, the 1's are brightened to make them easier to identify.

To help find elusive errors, the instrument may be operated in a HALT A≠B mode in which the A memory acquires the data in repeating data acquisition cycles until there is a difference between the contents of memories A and B. The instrument then reverts to the single-cycle mode and stops acquiring data when the current cycle is completed.

Map Display

A more comprehensive view of the operation of digital machines is provided by a new capability in Model 1600A. This is the MAP mode.

When operating in the MAP mode, the new logic state analyzer presents a digital word simply as a dot on the CRT display. The position of the dot is determined by the word, one half of the word giving the x-axis position and the other half giving the y-axis po-

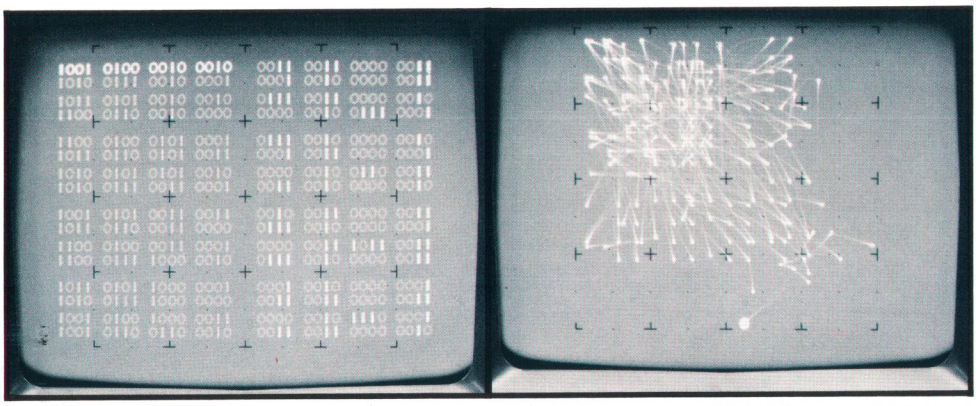

Fig. 4. *(Left) In the* COMPARISON *mode, 1's in the array on the right half of the display show where bits displayed on the left half differ from a stored sequence.* **Fig. 5.** *(Right) In the* MAP *mode, digital words are presented as dots on the display, each word having a unique position. Vectors trace the digital sequence from word to word. The cursor at bottom is a small circle positioned by the* TRIGGER WORD *switches.*

sition. Consequently, each word has a unique position on the CRT display.

In addition, the instrument traces lines from dot to dot as it steps through a sequence of digital words so each sequence of words generates a characteristic pattern (Fig. 5). Once familiar with the patterns generated by particular sequences of words, the user can instantly recognize whether or not a particular pattern is correct without having to do a state-by-state study of the tabular listing.

The MAP mode also gives an indication of the relative frequency of occurrence of any state—the more often a state repeats, the brighter its dot. In looking at memory address lines, for example, this mode gives a highly visible indication of which memory addresses are most often used and which are not used at all.

Map Expansion

A display of 65,536 dots would be difficult to interpret so an EXPAND mode can be used with the map. In the NORMAL MAP mode, only the six most significant bits of each half of the word are used for positioning, bits 10 through 15 for the vertical position and bits 2 through 7 for the horizontal position. Bits 0, 1, 8, and 9 do not affect the positioning. In effect, 4096 dot positions are displayed.

The EXPAND mode displays one of 16 area subdivisions expanded to full screen. Bits 0, 1, 8, and 9 then affect the dot position. The area to be expanded is selected by a cursor, a small circle positioned by the trigger-word switch register (Fig. 5). Positioning the cursor anywhere within one of the sixteen areas, outlined by marks fixed permanently on the CRT faceplate, selects that area for expansion.

When the map is expanded, the cursor can be positioned over any dot of interest. This dot then becomes the trigger word when the instrument is switched back to the TABLE DISPLAY mode.

Accessory Logic State Analyzer

Model 1607A Logic State Analyzer (Fig. 3) is functionally similar to Model 1600A but it does not have the auxiliary memory, the map mode, nor a CRT display. It has X, Y, and Z outputs, however, so it can use almost any CRT monitor or oscilloscope for its display. This arrangement is attractive in some situations because the oscilloscope can also be used for time-domain analyses, once Model 1607A working in the data domain has pinpointed the problem.

Model 1607A can work with Model 1600A to form a logic state analyzer with 32 data channels. Data entered by way of Model 1607A is presented on the right half of Model 1600A's CRT display. The resulting display may show words 32 bits wide, or data may be presented on part of the display while corresponding addresses or other signals are presented on the remaining part.

When used with the 1600A, Model 1607A adds some special capabilities to the combination. For example, the two instruments may operate with independent clocks but in a "bus trigger" mode such that triggering does not occur until trigger conditions are met in both instruments simultaneously. This mode might be used, for instance, when two digital machines communicate with each other but without synchronization of their clocks. Machine I is in state M when it transmits data over the interconnecting bus to Machine II, and Machine II must be in state R to receive the data. The bus trigger mode then detects when states M and R exist simultaneously so the state flow of Machine II can be monitored immediately following the receipt of data.

The Model 1607A may also supply the "arm" signal for the Model 1600A so triggering of the 1600A can be inhibited until some other trigger word is first detected by the 1607A.

Technical Details

The design of the new logic state analyzers involves three general areas:

1. Trigger recognition and delay;
2. Data acquisition;
3. Data display.

Although conceptually the trigger recognition and

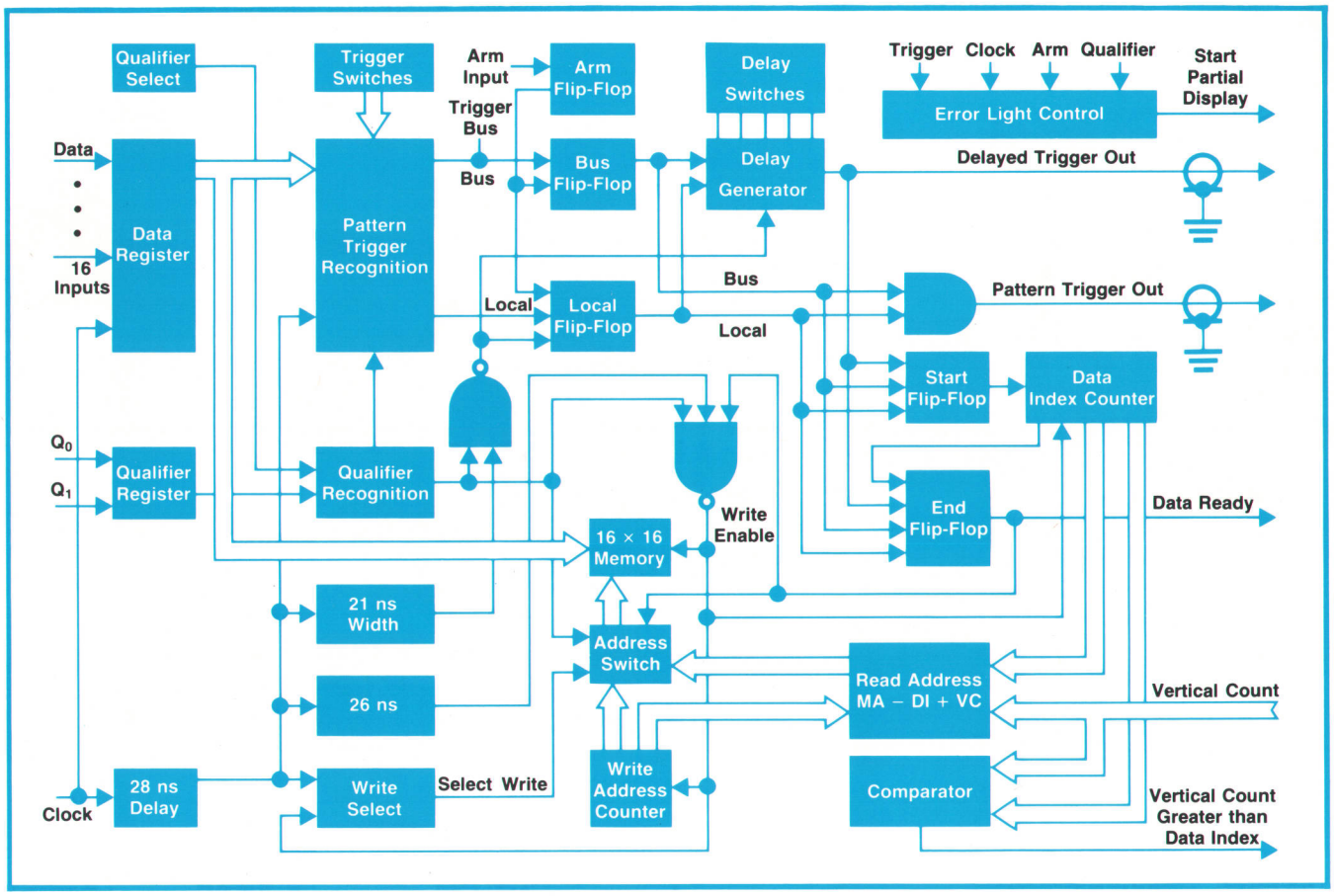

Fig. 6. *Block diagram of the data acquisition circuits. Not shown, for brevity, are the internal gates that determine which of several inputs will trigger a device, for example the "end" flip-flop.*

delay circuits are closely involved with data acquisition, they function independently. The trigger recognition circuit generates an output pulse whenever the trigger word is clocked in, assuming the instrument is armed, regardless of what the rest of the instrument is doing. These pulses are useful for synchronizing other test equipment, such as a time-domain oscilloscope, and they can also be totaled by a counter, giving the instrument the capabilities of a breakpoint register. Following each trigger, a delayed pulse is also supplied at a separate output connector on conclusion of the selected delay interval.

When the data acquisition circuits are enabled, the trigger recognition circuits control data storage. Beginning with a word determined by the trigger word and the mode selected (START DISPLAY, END DISPLAY, etc.), each subsequent qualified word latched into the input data register is stored in memory.

When 16 words have been stored, control is passed automatically to the display circuits, which then display the data stored in memory. When the SINGLE mode is selected, the data is displayed continuously until the RESET button is pressed. In the REPETITIVE mode, the data is retained on display for a period determined by the DISPLAY TIME control (200 ms to 5 s), after which control is passed back to the data acquisition circuits. New data is then stored upon the next occurrence of the trigger word.

A hierarchy of warning lights assists the operator in setting up the instrument. Whenever the average clock rate or the qualifier, trigger, or arming rates fall below 5 Hz, the appropriate warning light turns on. The lights are ranked as follows: clock, qualifier, and trigger. For example, if there were no clock and no trigger, only the NO CLOCK light would turn on. NO ARM, however, has precedence over NO TRIGGER but is independent of the other warning lights.

Data Input

Data is entered by way of pods that can be placed close to the point of measurement. Each of the miniature circuit probes connects through a 30-cm length of wire to a pod, six probes to a pod (Fig. 2). This arrangement minimizes capacitive loading of the circuits under test.

The pods contain trigger circuits that decide whether the voltage sensed by each probe represents a "0" or a "1". The threshold is fixed at +1.5V for TTL circuits, or it can be switched on the instrument front panel to VARIABLE, and is then adjustable over a range

of ±10V.

The digital word sensed by the probes is latched into the input data register by the input clock pulses (see the block diagram, (Fig. 6). This occurs on every clock pulse, regardless of the state of the qualifiers, the ARM input, or the selected display mode. Clock pulses are supplied from an external source, usually the system under test, and are subject to the same threshold recognition criterion as the data.

The pattern recognition logic looks at the input data register continuously, and when there is a match between the input data and the front-panel TRIGGER WORD switch register, the "local" flip-flop is triggered, initiating the data acquisition sequence if the instrument is in the LOCAL mode. The "trigger bus" line also attempts to rise, but will not do so if it is held down by any other instrument on the trigger bus. Each instrument connected to the trigger bus drives the bus with an open-collector circuit so the bus cannot rise until trigger conditions are met simultaneously by all bus-connected instruments. If the instrument is in the BUS mode, data acquisition is not initiated until the trigger bus rises.

The use of two trigger-generating flip-flops makes it possible to have two instruments bus-connected so data acquisition in one is dependent on trigger conditions being met in both instruments simultaneously, while the other, operated in the LOCAL mode, acquires data any time its own trigger conditions are met.

Generation of a trigger also starts the delay generator. The pattern trigger output remains true until the delay generator produces the delayed trigger pulse. If zero delay were selected, the delayed trigger would occur simultaneously with the pattern trigger.

TRIGGER ARM, if selected, disables the local and trigger bus flip-flops until an arming input sets the arm flip-flop. Then when trigger conditions are met, a pattern trigger output is generated and the arm flip-flop is reset.

Qualifiers

The QUALIFIER inputs may be used in either of two ways. When qualifying trigger words, the qualifiers effectively become part of the trigger word, making it 18 bits wide. The two qualifier bits, however, are not stored or displayed.

When qualifying the display, the qualifiers control the entry of data: words can be clocked into memory only when qualifying conditions are met. Similarly, the delay generator counts only those clock pulses that coincide with the qualifiers.

The Data Acquisition Cycle

When the display circuits relinquish control of the instrument, they issue a data acquisition command. This resets the trigger and delay generators and, if the instrument is in the START DISPLAY mode, resets the data index counter and the "start" and "end" flip-flops (Fig 6). The next qualified clock pulse switches the memory address lines to the address counter.

Occurrence of the trigger word sets the start flip-flop. This enables the data index counter, which is then incremented by each write pulse. The trailing edge of the write pulse also increments the address counter.

Each digital word latched into the input data register is written into memory at the address indicated by the address counter. This continues until the 16-state data index reaches full count, which resets the end flip-flop, gating off the write-enable pulses and stopping the loading of data into memory. The end flip-flop also sets the "data ready" line true, indicating to the display section that data is complete and ready for display.

When the instrument is operated in the END DISPLAY mode, the start flip-flop is preset, allowing the data index counter to run. When the data index counter reaches terminal count, it enables the end flip-flop. Data is acquired until the next occurring trigger, which stops data acquisition immediately and switches memory control to the display section.

The count in the data index counter at any instant indicates how many good words are in memory. The address counter points to the next address in memory to be accessed. The difference between these two counts is the address of the first word of the current data sequence. During the display cycle, the difference is added to the count in the display section's vertical counter. The result is the address of the next word to be read out of memory for display.

Generating the Table Display

Whenever the data acquisition circuits set the data ready line true, the display circuits take control of the memory and read out and display the memory contents.

Read out is serial, with memory addressing controlled by two four-bit counters (Fig. 7). The "vertical" counter indicates the word to be read and the "horizontal" counter, working through a 1-of-16 multiplexer, selects the bit within that word to be displayed.

The horizontal counter is driven by an internally-generated 50-kHz clock. When it reaches state 15, it increments the vertical counter and then resets. In this fashion, every bit address in memory is polled.

The CRT beam is positioned by digital-to-analog converters driven by the counters. The vertical counter digits are weighted so a wider step occurs on every other vertical address, spacing the lines on the CRT in pairs for easier reading. A still wider step occurs on every fourth line.

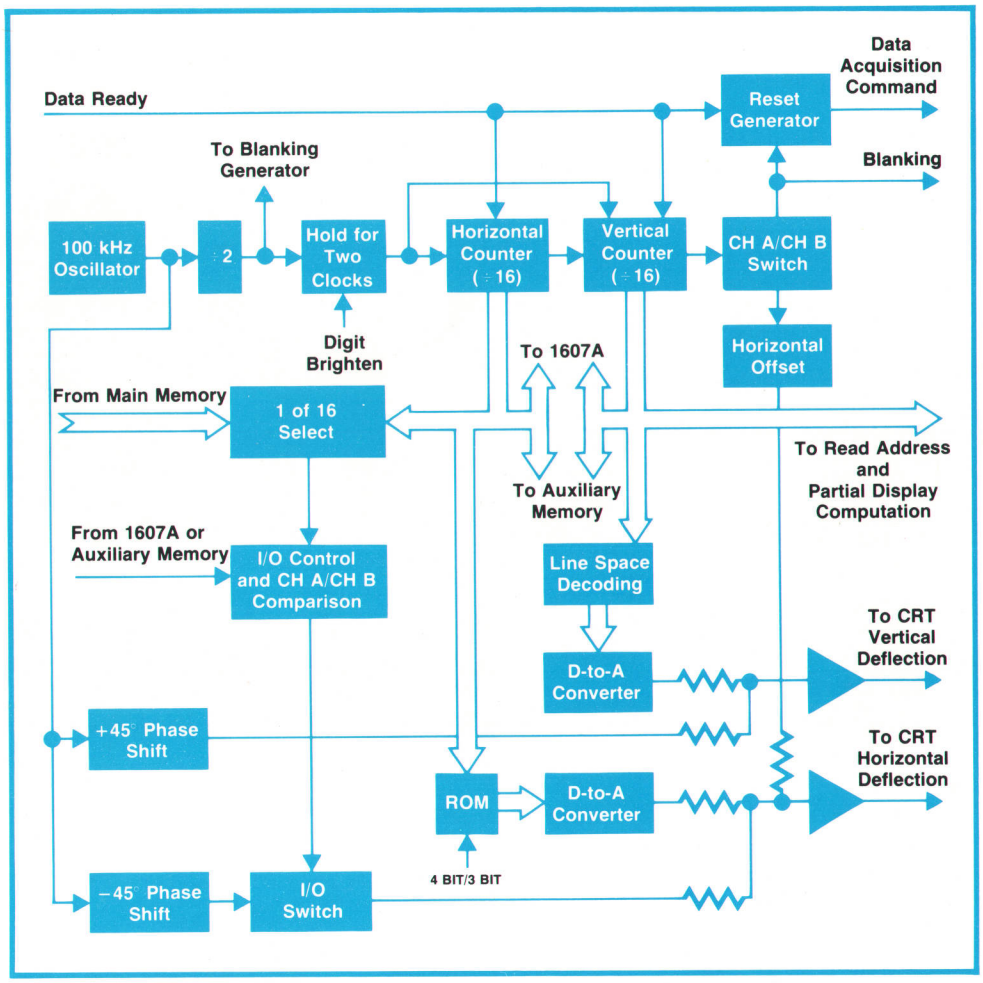

Fig. 7. *Block diagram of the display circuits configured for display of the table of 1's and 0's. When operating in the* REPETITIVE *mode, display cycles repeat until the* DISPLAY TIME *control (not shown) allows the reset generator to issue a data acquisition command. In the* SINGLE *mode, data acquisition is initiated only in response to the front-panel* RESET *button.*

A different method is used for spacing the columns to give the operator a choice of grouping by three's, for octal words, or by four's for hexadecimal words. This is accomplished by using the contents of the horizontal counter to address a ROM, which reads out digital words that generate the appropriate horizontal deflections when applied to the D-to-A converter.

Digits are written on the CRT by adding low-level 100-kHz sine waves to the deflection voltages. The sine waves are shifted 90° with respect to each other so the deflection voltages trace a small ellipse when a "0" is indicated for display. When a "1" is indicated, the sine wave to the horizontal circuits is gated off. Both sine waves are turned off when the instrument displays dots in the MAP mode.

The 100-kHz signal is divided by two to derive the 50-kHz clock for the horizontal counter. It also derives a 50-kHz square wave that blanks the CRT beam for 10 μs while it moves to a new position, and then unblanks it for 10 μs while the digit is written. When a digit is to be brightened for the trigger word or the A & (A $\oplus$ B) mode, the clock input to the counters is interrupted for two clock periods so the digit is written five times before the circuits step to the next digit.

When data from the auxiliary memory is to be displayed, the contents of the vertical and horizontal counters are combined as an eight-bit address for addressing the 256×1-bit RAM. A dc offset voltage is then added to the horizontal deflection to position the auxiliary display to the right of the main display.

Data from a 1607A is displayed on a 1600A by switching the 1600A's horizontal and vertical counters to interrogate the memory in the 1607A. The value of each bit interrogated is returned to the 1600A for display (a multiconductor I/O bus interconnects the two instruments).

Generating the Map Display

When the instrument is operated in the MAP mode, the 16-bit word in memory addressed by the vertical counter is applied directly to the D-to-A converters (Fig. 8). Bits 2 through 7 are applied to the horizontal axis and bits 10 through 15 to the vertical axis. Each word thus appears as a dot at a particular location on the CRT display.

No blanking signals are supplied between dots so the CRT beam traces a line as it moves from dot to dot. To make the lines visible, the display clock rate is slowed to 25 kHz and RC networks are switched into the deflection amplifiers to slow the transient re-

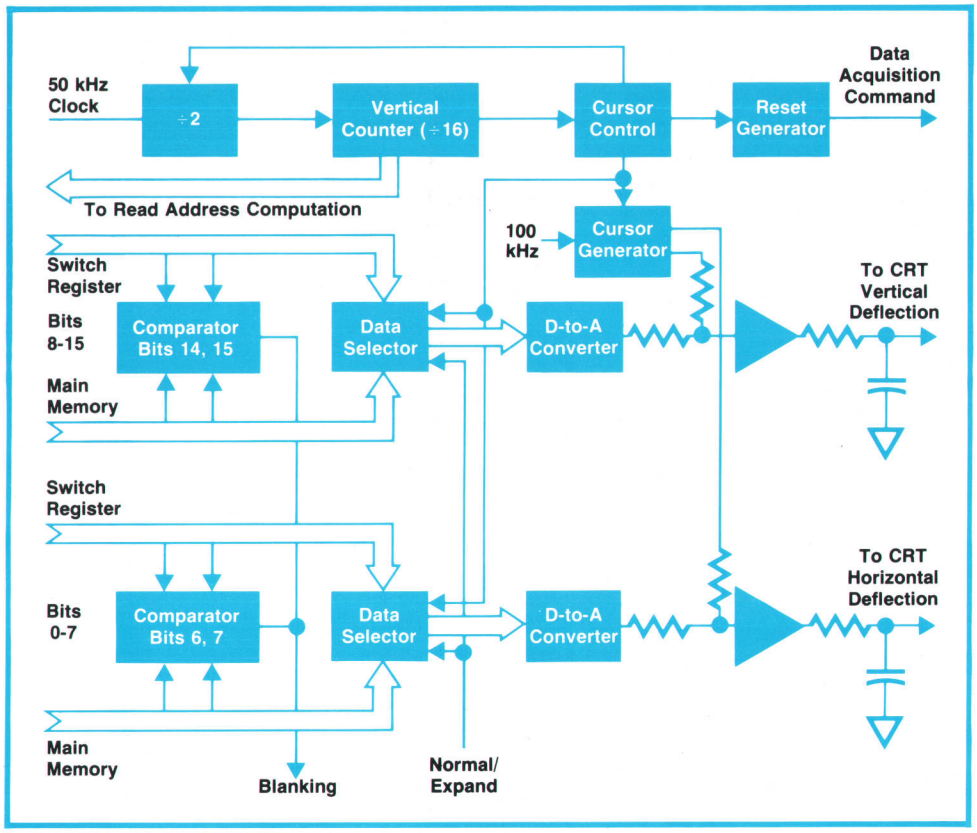

Fig. 8. *In the MAP mode, the clock pulses (divided by 2) go directly to the "vertical" counter so addresses are read out at a 25 kHz rate. When the vertical counter reaches terminal count, the data selectors switch to the front-panel switch register and a cursor is traced at the address indicated.*

sponse. The RC response characteristic retards the CRT beam as it approaches the next position, brightening the trace there to give an indication of direction.

The address of a particular dot can be determined with the MAP LOCATOR cursor. When all 16 words stored in memory have been displayed, the digital-to-analog converters are switched to the front-panel switch register, which provides the digital information for positioning the CRT beam. The phase-shifted 100-kHz sine waves are then added to the deflection voltages, the CRT beam is unblanked, and a small circle is written at that position.

In the EXPAND MAP mode, the D-to-A converters are switched to bits 0 to 5 (horizontal) and 8 to 13 (vertical). The CRT is blanked, however, until bits 6, 7, 14, and 15 of the word being read out of memory agree with the corresponding bits of the front-panel switch register. Hence, only those words lying within the same sector as the cursor are displayed. If two successive words are not in the same sector, the direction vector is blanked to prevent the presentation of misleading lines.

If the instrument is mapping in the repetitive mode, memory control is returned to the data acquisition circuits following the generation of the cursor. A new sequence of 16 words is then acquired and displayed. The short display cycle (200 ms) and the persistence of the CRT phosphor cause the map to appear as a

Inside the Model 1607A Logic State Analyzer

The Model 1607A Logic State Analyzer was designed with a dual purpose in mind: (1) to serve as an extension of the Model 1600A Logic State Analyzer and (2) to function independently as the logic state input for laboratory oscilloscopes.

Data acquisition is performed in the Model 1607A Logic State Analyzer in exactly the same way that it is in the Model 1600A. However, to make the 1607A compatible with as many CRT displays and oscilloscopes as possible, there are some differences in the way the display section works. For example, an extra state is inserted following state 15 in the horizontal counter. This adds 20μs to the retrace time to allow sufficient settling time for oscilloscopes that have limited horizontal bandwidth.

The amplitudes of the X, Y, and Z outputs are adjustable to accommodate the input settings of the associated oscilloscope. This allows the user to switch back and forth between time-domain and data-domain displays with a minimum of readjustment. Also, since the z-axis input of most scopes is on the rear panel and is not switchable, a switch for disabling the z-axis signal is provided on the front-panel of Model 1607A.

Another problem in compatibility concerned the trigger-word intensification. Because of the non-linear characteristics of the z-axis in most scopes, and also because of defocussing effects, it was difficult to define a universal brightening scheme. Therefore, trigger-word brightening is accomplished by writing the trigger word four times before proceeding to the next word. This is done by intercepting the horizontal counter carry bit four times before incrementing the vertical counter.

Thomas Saponas

composite of several 16-word sequences.

Blanking

Some 23 variables are involved in determining whether or not to blank the CRT beam, making this the most complex function in the display circuit.

In addition to those blanking signals already mentioned, a blanking signal is generated for unused columns to the left of the most significant digit. This signal is generated by a comparator. Whenever the output of the D-to-A converter connected to the horizontal counter exceeds a voltage set by the COLUMN BLANKING control, the comparator blanks the beam.

When channel B is displaying data stored in the auxiliary memory, column blanking in both channels is controlled simultaneously. Blanking for the partial display mode is achieved by comparing the count in the vertical counter to the count in the data acquisition section's data index counter. The beam is blanked whenever the vertical count exceeds the data index count because data in memory from that point on is "old" data not wanted on the display.

When the instrument is not in the partial display mode (qualified clock rate >50 Hz), the channel A display is blanked until 16 words are in memory and the trigger word is detected.

There are some differences in the blanking of channels A and B. When channel B displays data from a 1607A, column blanking, partial-display blanking, and so on for channel B are controlled by the 1607A, except in the A&A⊕B mode (channel B displaying differences between 1600A and 1607A data). In this case, channel B column and row blanking is controlled by both the 1600A and 1607A to prevent more bits being displayed than are actually being compared.

Acknowledgments

The 1600S design group was led by Bill Farnbach, who contributed significantly to the instrument design. Product design was by Roger Molnar. Many of the operating concepts were provided by section leader Chuck House and customer requirements were provided by product managers Dick Cochran and Bruce Farly.

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Charles T. Small

Chuck Small joined HP in 1966 as a production test technician. Two years later, he transferred to the pulse generator design group, building and debugging prototypes, and in 1972 he moved to the logic state analyzer group where he contributed to the design of Model 1601A. He then undertook the design of the data acquisition portion of Model 1600A. Chuck has an AE degree from the Portland (Oregon) Community College and is doing further academic work at the University of Colorado. Chuck does some woodworking, argues hi-fi matters with colleagues, and is a model railroader (HO gauge). He and his wife have one daughter, 3.

Justin S. Morill, Jr.

Justin Morrill joined Hewlett-Packard in 1972 after getting his Master of Electrical Engineering degree at Rice University (Houston, Texas) where he had also obtained a Bachelor of Arts in Science and Engineering. Before becoming involved in the Logic State Analyzers, he worked on applications of storage CRT's. In his spare time, Justin enjoys the customary Rocky Mountain hiking and backpacking, sometimes packing his 1-year-old son, and he also photographs old mining towns, getting there in his four-wheel-drive vehicle. Justin is also a woodworker.

SPECIFICATIONS

Models 1600A and 1607A Logic State Analyzers

Clock and Data Inputs

REPETITION RATE: 0 to 20 MHz
INPUT RC: 40 kΩ shunted by ≤14 pF
INPUT BIAS CURRENT: ≤30 μA
INPUT THRESHOLD: TTL, fixed at approx +1.5V; variable, ±10 Vdc.
MAXIMUM INPUT:
LEVEL: −15 to +15 Vdc
SWING: 15 V peak from threshold
MINIMUM INPUT:
SWING: 0.5 V +5% of p-p threshold voltage
CLOCK PULSE WIDTH: 20 ns at threshold
DATA PULSE WIDTH: 25 ns at threshold
DATA SETUP TIME: time data must be present prior to clock transition, 20 ns
HOLD TIME: time data must be present after clock transition, 0 ns

Pattern and Delayed Trigger Outputs

HIGH: ≥2 V into 50Ω (line driver interface)
LOW: <0.4 V into 50Ω (line driver interface)
PULSE DURATION:
DELAYED TRIGGER: approx 25 ns (RZ format) at 1 V level
PATTERN TRIGGER: approx 25 ns in RZ format at 1 V level with delay set to zero or off. With delay on and not set to zero, pattern trigger output starts on receipt of a pattern trigger signal and ends when the delay ends.

Trigger Arm Input

IMPEDANCE: 50Ω
LEVEL: low state, 0 V to <0.4 V; high state, 2 V to <5 V
PULSE WIDTH: 15 ns minimum at 1.5 V level
ARMING CONDITIONS: If arming pulse positive edge occurs <45 ns after a clock, triggering occurs on same clock cycle. If arming pulse positive edge occurs >75 ns after a clock, triggering occurs on next clock cycle.

1607A X, Y, and Z Axes Outputs

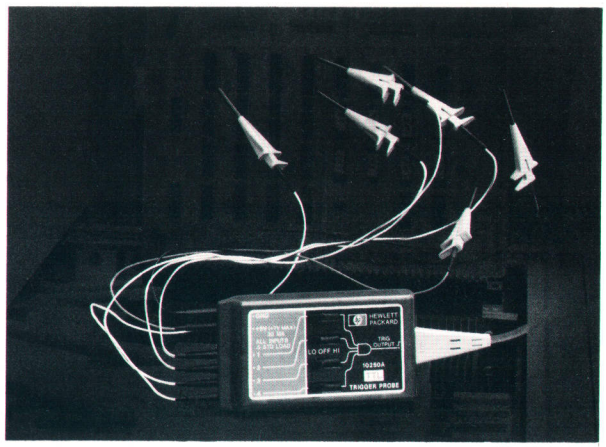
X and Y Axes: <0.6 V to >6 V p-p, ±8 V max into ≥100 kΩ
Z-AXIS: 0 to 10 V p-p into ≥1 kΩ "
DISPLAY INTERFACE REQUIREMENTS: The 1607A interfaces with any oscilloscope or display with the following input parameters.
X AND Y INPUTS: 0.1 to 1 V/div deflection factors; dc coupled input; and >500 kHz bandwidth
Z-AXIS INPUT: dc coupled with positive blanking; full blanking must occur with <10 V input at 10 mA

General

DISPLAY RATE: variable from <200 ms to >5 s (1600A), <50 ms to >5 s (1607A)
POWER: 100, 120, 220, 240 Vac; −10% +5%; 48 to 440 Hz; 120 VA max
DIMENSIONS: 284 mm (W) × 460 mm (D) × 197 mm (1600A) or 121 mm (1607A); (11.2 × 18.1 × 7.8 or 4.8 inches).
WEIGHT:
MODEL 1600A: 12.7 kg (28 lb)
MODEL 1607A: 6.4 kg (14 lb)
ACCESSORIES SUPPLIED: three 10231B data probes and one 10230B clock probe
PRICES IN U.S.A.:
MODEL 1600A Logic State Analyzer, $4000
MODEL 1607A Logic State Analyzer, $2750
MODEL 1600S includes a 1600A and 1607A with Trigger Bus and Data Cables, $6800
MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
1900 Garden of the Gods Road
Colorado Springs, Colorado 80907

Oscilloscope Triggering on Digital Events

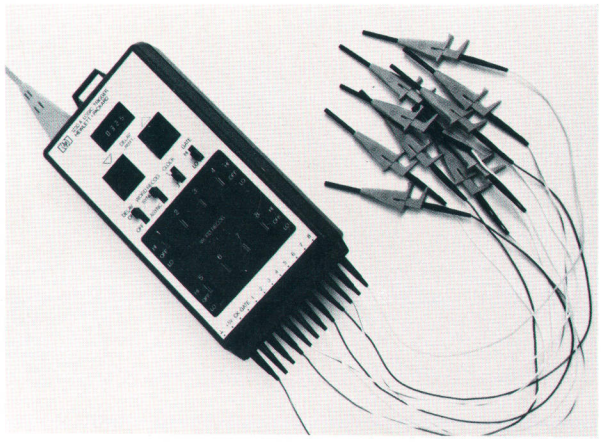
By presenting digital signals in the time domain, oscilloscopes can help find the sources of problems caused by propagation delays, transient spikes, noise, ringing, and inadequate pulse amplitude in digital systems. Isolating a short segment of a long digital sequence for detailed analysis, however, is very difficult if not impossible with a conventional scope. One of the advantages of the logic state analyzers is their ability to provide the trigger recognition needed for oscilloscope analysis of digital sequences. A number of other accessories have been developed to facilitate this use of an oscilloscope.



Four-Channel Monitoring

The most basic of the trigger recognizers are the HP 10250-series Trigger Probes. Each of these monitors up to four digital channels and whenever the bits appearing simultaneously in the data streams match the pattern established by the probe's switches, the output goes high, providing a trigger suitable for an oscilloscope or other instrument.

Three are offered. Model 10250A has trigger levels suitable for monitoring TTL circuits, Model 10251A operates with CMOS circuits, and Model 10252A with ECL circuits. They are powered by the device under test through separate connections and can operate at bit rates up to 10 MHz.



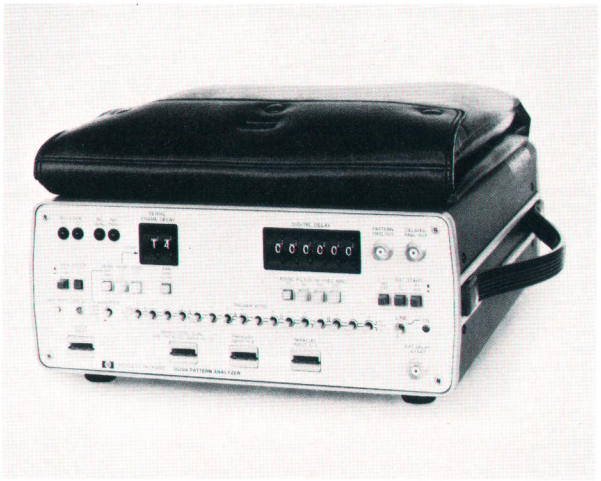
Eight-Channel Monitoring and Delay

The Model 1230A Logic Trigger augments this basic recognition capability by adding digital delay, making it possible to move the observation "window" up to 9998 clock pulses downstream from the recognition word. It can also monitor up to eight data streams simultaneously and works either asynchronously, as do the 10250-series Trigger Probes, or synchronously when connected to a system clock.

This device also has a ninth input (GATE) that can be used as a qualifier to prevent a trigger output until some other event occurs. The GATE input also enables two or more Logic Triggers to be operated in parallel for trigger recognition of wider words.

A handy method of setting the delay has been devised: holding down a pushbutton causes the delay interval, indicated by a LED display, to increase. Holding down another pushbutton causes the delay to decrease. Pressing both buttons at once immediately resets the delay to 1 bit.

A level lower than +0.8V is interpreted as a logic "0" and levels higher than +2V as logic "1's". Maximum bit rate is 15 MHz. It is powered by an external 5 V and draws 300 mA.



Sixteen-Channel Monitoring, Parallel or Serial

The most versatile logic trigger is the HP Model 1620A Pattern Analyzer. This instrument operates with either parallel or serial data streams. When operating in the parallel mode, it monitors up to 16 lines and generates triggers in exactly the same way as the Models 1600A and 1607A Logic State Analyzers, using the same kind of probe pods and bit-recognition circuits.

Model 1620A works at bit rates up to 20 MHz. Unlike the Logic State Analyzers, however, it can also work in an asynchronous mode without input clock pulses—an output trigger is generated whenever the data in all selected channels simultaneously matches the front-panel switch register. To prevent transients from generating false triggers, filters prevent the generation of a trigger until the input data has been held for a selected time.

The serial mode is useful for triggering on specific portions of long digital sequences like those encountered in disc memories. In the serial mode, Model 1620A generates a trigger when a sequence in the incoming bit stream matches the pattern set on the front-panel switch register.

The serial mode has a qualifier input (there are no qualifier inputs in the parallel mode). This allows pattern recognition to be suppressed until the qualifier input goes true. In addition, the viewing "window" can be delayed with respect to the qualifier. The delay prevents bit-stream comparison until the number of clock pulses indicated on the FRAME DELAY control has occurred after the qualifier goes true.

Unravelling Problems in the Design of Microprocessor-Based Systems

The debugging of a microprocessor-based system is expedited considerably by an instrument that provides an appropriate disclosure of what's going on inside the system.

by William E. Wagner

AS LOW-COST MICROPROCESSORS COME into widespread use, a whole new range of applications is opening up for the electronic design engineer. So is a whole new range of problems.

The designer of a microprocessor-based system is faced with the need for unravelling problems in four general areas: (1) hardware, (2) software, (3) combinations of software and hardware, and (4) information transfer to and from peripheral devices, that is, across an I/O port. To assist in the design and fabrication of these systems, many manufacturers of microprocessors offer diagnostic-simulators ranging in complexity from a few simple switches to massive kilobyte minicomputer systems. These, however, are designed for the express purpose of assisting the design engineer in the use of microprocessors of the particular manufacturer. Such systems concentrate on software debugging with minimum attention paid to the hardware. Adaptability is not an inherent trait of these machines.

Fortunately, the development of general-purpose measurement tools has been keeping pace with the needs of the design engineer. First there was the Hewlett-Packard Model 5000A Logic Analyzer, that provided means for examining the content of serial data streams, then the Model 1601L Logic State Analyzer that did the same for parallel logic streams, and now the Model 1600S Logic State Analyzer, described in this issue, that expands on the capabilities of the earlier instruments.

It is the purpose of this article to illustrate the usefulness of the Model 1600S by examples of typical applications. These examples are drawn from the author's experience with one of several designs of systems using microprocessors.

An Information Processing System

The design example concerns an information processing system that accepts hexadecimal data either from a keyboard or a tape input and displays alphanumeric data on a CRT terminal.

Four basic elements were required to implement the system (Fig. 1): a microprocessing unit (MPU) that provides the necessary data manipulation, a read-only memory (ROM) that contains executive control, a 4-kilobyte random-access memory (RAM) for temporary data storage, and a peripheral interface adapter (PIA) that provides communications with the keyboard, tape unit, and CRT display.

Interconnections among these modules is made by three buses: an 8-bit bidirectional bus for data transfer to and from the MPU, a 16-bit address bus, and a control bus. The control bus includes a request-for-interrupt line (IRQ), a READ/WRITE signal that signifies the direction of data to or from the MPU, and a MASTER-ENABLE signal that results from the logical ANDing of the phase-2 clock with VMA (valid memory address), a signal generated by the MPU.

The system prototype also included a ROM that had a diagnostic program with the following capabilities: examine and change, if required, the contents of any memory location in RAM, load data into RAM from tape, transfer memory to tape, set and remove program breakpoints, and display the contents of the MPU registers when a breakpoint is encountered.

Debugging the System

Before first turn-on of a new system, a dc continuity check is made and driving functions, e.g., the two-phase clock, are checked as a prelude to assembling the entire system. All I/O devices not mandatory for the start up are either removed or disabled.

These things having been done for our example system, start-up could then be examined. The start-up procedure for the particular microprocessor used is as follows:

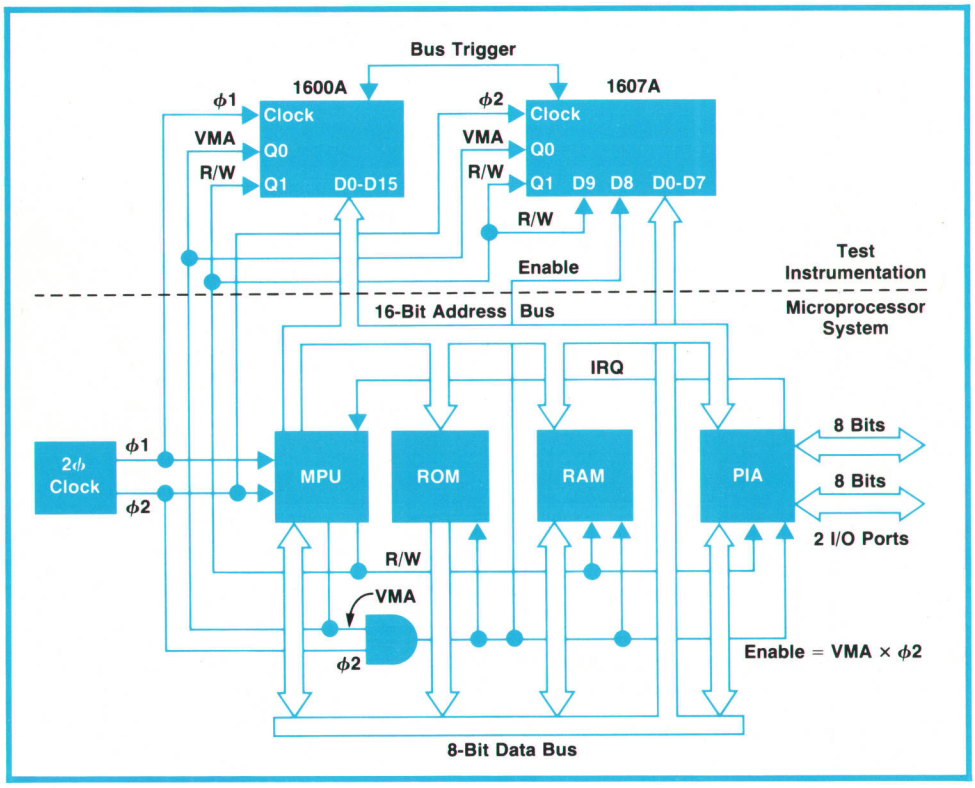


Fig. 1. *Microprocessor-based system is shown in block diagram form below the dotted line. Connections to test instrumentation above dotted line are shown.*

1. The MPU reads the data at memory location FFFE (hexadecimal notation) and internally transfers that 8-bit byte of data to the most significant bits of the 16-bit program counter.

2. The microprocessor then reads memory location FFFF and transfers that byte to the least significant bits of the program counter.

3. The microprocessor then begins execution of the program at the address to which the program counter is pointing.

The Model 1600S Logic State Analyzer was connected to the system in the manner shown in Fig. 1. The trigger word was set to FFFF to show how the system operates after the start-up procedure.

The result of the initial start-up is shown in Fig. 2. The trigger word FFFF is shown at the top of the columns displaying the 16 address bits on the left. The word immediately following, however, is 0000, which is not the word that is supposed to be there. Furthermore, the columns on the right, which show the ENABLE bit and the eight data bits, are all zeroes. Here is an indication of the source of the problem: since the ENABLE signal never reaches the logic-1 state, none of the circuit elements external to the microprocessor become enabled, specifically the ROM, so valid data never appears on the bus.

The remaining addresses on display indicate that the microprocessor is sequentially reading every address starting with 0000. Switching the logic state analyzer to the MAP mode (Fig. 3) confirms that the microprocessor does indeed step through every address looking for an instruction other than NOP (no operation), and never finding one.

Since the ENABLE pulse was at fault, an oscilloscope was used to examine the inputs to the ENABLE AND gate. Here it was found that both VMA and the $\phi 2$ clock reached the logic-1 state simultaneously, yet the output remained at logic 0. Obviously, the gate was defective.

This problem, easily corrected, seems elemental but without the insight provided by the logic state

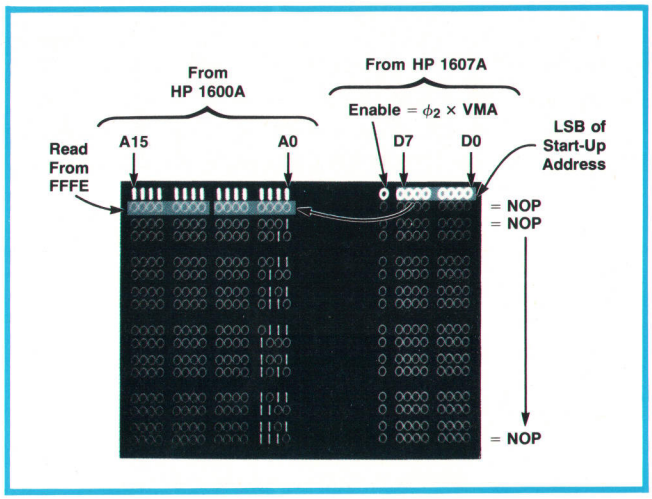


Fig. 2. *Logic State Analyzer display of the initial start-up routine of the system of Fig. 1. Unused channels 9 through 15 on the right half of the display are blanked by the column-blanking control on the Model 1607A.*

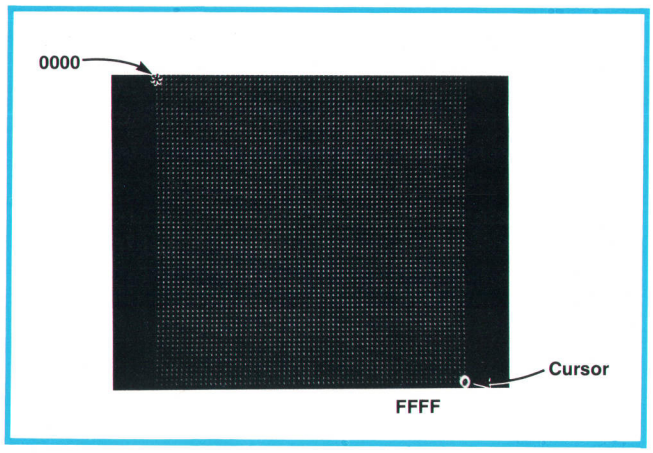


Fig. 3. *Map display of the address sequence following initial start-up of the system of Fig. 1. Uniform appearance of dots indicates that the system is stepping through every address (exposure was for two seconds to allow gaps caused by load-then-display sequence to be filled in).*

analyzer's simultaneous display of many channels, it would have taken much longer to track it down.

This example also illustrates another useful trait of the logic state analyzers: they often reveal information about a system that would otherwise remain undetected. In this case, the logic state analyzer revealed that the microprocessor interpreted 00 on the data lines as NOP (no operation). The manufacturer's literature specified that 02 would be interpreted as NOP but it said nothing about 00.

Closed Port

The next problem encountered involved an interaction between the software and the machine's hardware. This particular machine was structured to minimize the time between a request for interrupt service and the response to that request by use of the command "wait for interrupt" (WAI). It was found, however, that once the microprocessor entered the wait state, it would refuse to respond to external conditions satisfying the criteria for interrupt service.

To track down the problem, a short test program was entered into RAM storage by way of the diagnostic. It had two steps: (1) set the stack pointer to a known address, and (2) execute WAI.

The result is shown in Fig. 4. The trigger word for the logic-state analyzer was set at 0200, the address of the hexadecimal word 8E, as shown on the data bus portion of the display. This instructs the MPU to set the stack pointer (LDS). The next two addresses load the two bytes of the address 07FF, the highest location in RAM, into the stack pointer register.

The next address in the program (0203) places the wait-for-interrupt (WAI) command, 3E, on the data bus. It so happens that this particular MPU has a "look-ahead" feature that places the next address from the program counter on the address bus while the MPU is executing the current instruction. Thus, 0204 appears on the address bus as the MPU starts execution of the WAI command, but it is not used. The READ/WRITE line then goes to the logic-0 or "write" state.

We can now trace the operation of the WAI as the contents of the seven registers internal to the MPU are loaded into the memory stack, beginning with 07FF and stepping down from this location. It is noted, however, that when the contents of the seven registers are loaded in memory, VMA goes to the logic-0 state and as a result, so does ENABLE. Here, then, is the source of the problem. The peripheral interface adapter requires a clock pulse to transfer data across the I/O ports. This clock pulse was provided by ENABLE but since ENABLE was no longer present, there was no way for an interrupt request to be transferred across the port! Clearly, a modification of either the hardware or the software was in order.

It was decided to modify the software by implementing the WAI command step-by-step. The resulting subroutine transfers the contents of the MPU registers into memory and then enters a tight closed loop, as shown in Fig. 5a. The loop consists simply of one instruction: "branch always" (hex 20). This causes the program to loop back on itself. Branch always is a double byte word with the first byte being the instruction and the second byte being the relative offset that tells the microprocessor how far and in what direction to move in the program. Since the move is backwards, and since the system does not respond to negative numbers, the offset is expressed in two's complement form, and because the microprocessor has the built-in look-ahead feature, it has to move back two steps.

As a result of this software change, VMA returns

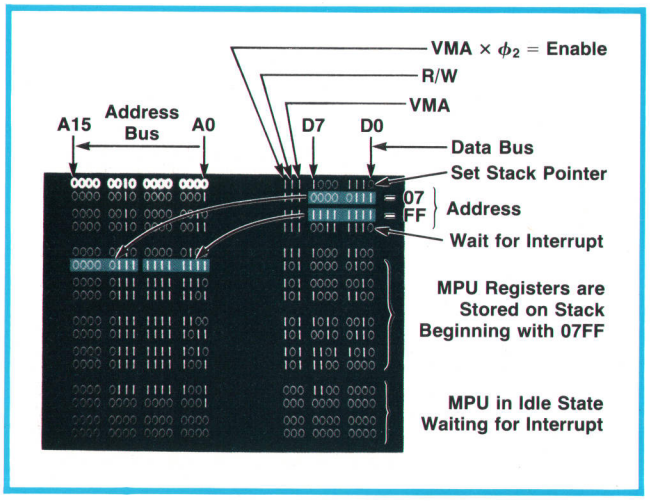


Fig. 4. *Logic State Analyzer display of the test program used to find a problem in the request-for-interrupt routine.*

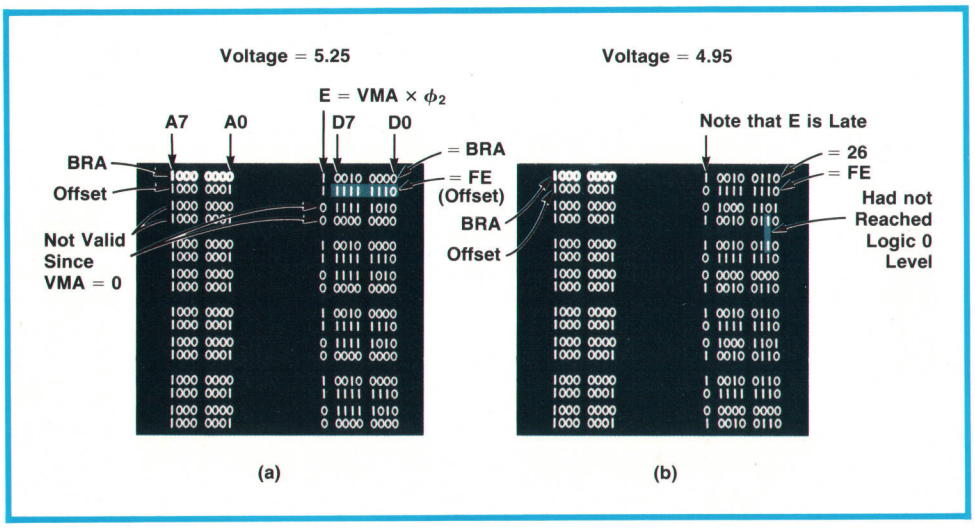


Fig. 5. *Revised wait-for-interrupt loop executes properly when the supply voltage is 5.25 volts (a). Incorrect information appears on the data bus (b) when the supply voltage drops to 4.95 volts.*

to the logic-1 state. Therefore the ENABLE signal was present for clocking the PIA when the criteria for interrupt were established in the external system.

Voltage Sensitivity

It was found that occasionally, for no apparent reason, the MPU would exit the new WAI loop without an INTERRUPT being generated. This was traced to a hardware dependence on voltage—the system would fail in a random unpredictable fashion if the supply voltage dropped lower than 4.95 volts.

Operation at 4.95 volts is shown in Fig. 5b. A clue to the problem lay in the fact that the MPU appeared to operate properly even though the data bus had erroneous information. The key factor here was that the logic-state analyzer had been set to clock in the data bus on the rising edge of the $\phi 2$ pulse. When the instrument was reset to clock in data on the falling edge of $\phi 2$, the correct data, as shown in Fig. 5a, then appeared on the display. What would this indicate?

If the data was valid on the falling edge of $\phi 2$ but not on the rising edge, this indicates that the data is still in a transitional state on the rising edge.

An examination of the ROM circuits disclosed the source of the problem: the two-state NMOS-to-TTL buffer between the address bus and the ROMs used a CMOS inverter, a device whose propagation delay is notoriously sensitive to the operating voltage. This buffer was replaced by a "bus extender", a single-stage device whose propagation delay is not so sensitive to voltage. That cured the problem.

Weak Pulse

As a final example, a problem was encountered in

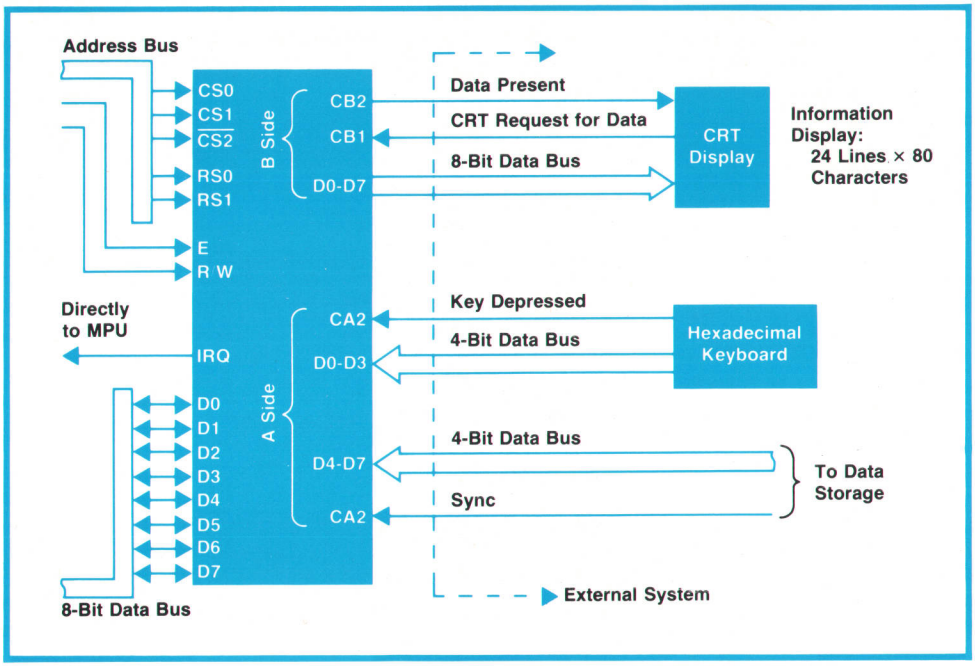


Fig. 6. *Interconnection of peripheral interface adapter and external devices.*

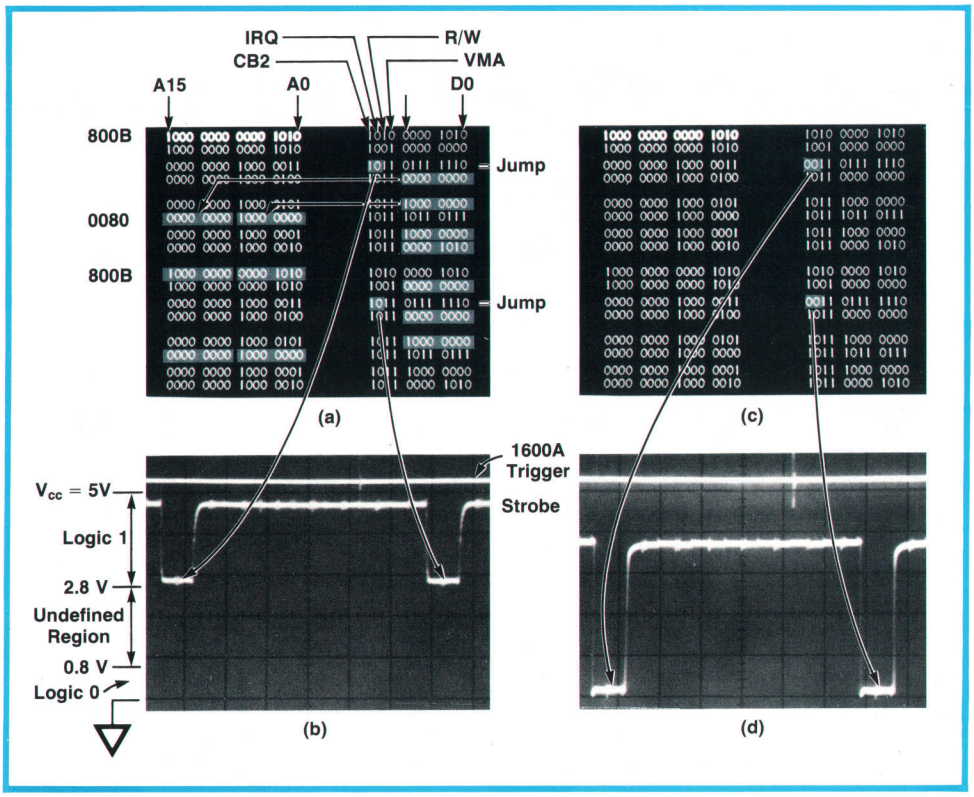


Fig. 7. *Logic State Analyzer display of the CRT display interrupt routine (a). A repetitive store operation results (see text). Oscilloscope examination of the CB2 pulse (b) shows insufficient amplitude which was corrected (d) by removal of a solder bridge. System then operates correctly (c).*

the interaction of the microprocessor with the CRT display. A request from the display for data would be entered into the peripheral interface adapter thereby generating an interrupt. When the interrupt service routine determined that it was the CRT that requested service, the appropriate data would be placed on the data lines and latched into the PIA. It was found that the data was never displayed.

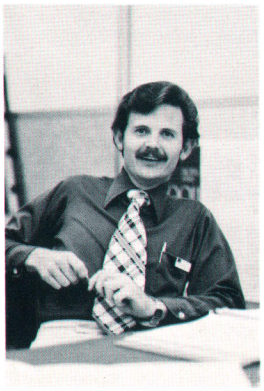
The PIA had been programmed to generate a "data present" pulse delayed in time by one ENABLE pulse following the write command to the PIA. The pulse was the strobe that informed the display terminal that a new byte of data was available. This did not happen when the system was running.

The logic state analyzer was connected as before with the CB2 (data present) line added to the display (Fig. 6). The trigger word was set for address 800A, which is the location of the data register corresponding to the input port on the CRT display terminal.

Tracing the sequence of a CRT test program in Fig. 7a, a loop is noted beginning at address 0080, which is the command to store the contents of accumulator A (STA A) at address 800A. As Fig. 7a shows, the program immediately jumps back to address 0080 and it continues this way, repetitively storing the contents of the A accumulator in the memory location reserved for the PIA. An examination of the CB2 line in Fig. 7a discloses that it fails to go low for one ENABLE cycle following the instruction WRITE to location 800A. This identified the problem.

An oscilloscope was used to observe the CB2 line. The scope was triggered by the trigger output of the Logic State Analyzer, with 800A being the trigger word. The result is shown in Fig. 7b. The upper trace is the trigger pulse and the lower trace is the CB2 pulse. A negative-going pulse does indeed appear on the CB2 line, but it is of insufficient amplitude to establish the logic-0 state.

A few minutes examination of the circuit board revealed a small solder bridge which, when removed, resulted in the pulse as shown in Fig. 7d. This cor- the fault, as shown in Fig. 7c.



William E. Wagner

Some experiments in acoustic radar while a student at Arizona State University led Bill Wagner to a job at an electronics company before he finished his academic work. That evolved into a position as an applications engineer with the company's microprocessor group. He joined Hewlett-Packard as a product support engineer in 1975 and is continuing his academic efforts at Colorado State University. Among his hobbies, Bill includes hiking, classical music, and mathematics. More of an avocation than a hobby is his fascination with pipe organs, having so far built seven from scratch, including rolling the pipes in the traditional manner.

A Multichannel Word Generator for Testing Digital Components and Systems

This instrument supplies eight 32-bit serial words simultaneously at clock rates up to 50 MHz or, conversely, 32 8-bit parallel words. Versatile outputs adapt the generator to a wide range of tests involving digital components, assemblies, and data buses.

by Arndt Pannach and Wolfgang Kappler

SIGNAL SOURCES HAVING BUT ONE or two output channels often fall short of providing realistic test signals for today's complicated circuits. Providing stimuli for testing digital components and assemblies is primarily a multichannel affair. A mixture of binary data and pulse-type signals—address, data, clock, flag, enable, strobe, to name a few—usually is required. Because these signals are not always identical in form, digital device testing has generally required an array of interconnected pulse generators and digital pattern generators, or a dedicated automatic system.

Described here is an instrument (Fig. 1) designed to meet the requirements for testing the new breed of digital circuits. It provides multichannel bit patterns and supplies them with the flexible clocking, delay, and control of output parameters needed for general-purpose testing. It has eight data channels plus clock, strobe, and two sync outputs.

There are no restrictions other than length on the bit patterns that can be generated by this instrument. The user is thus free to use whatever patterns he needs to do worst-case testing of his devices. A 32-bit word may be selected individually for each data channel and stored as the digital pattern to be generated for that channel. Alternatively, data may be entered as 8-bit parallel bytes, the instrument thus having the capacity to store 32 8-bit bytes. The serial

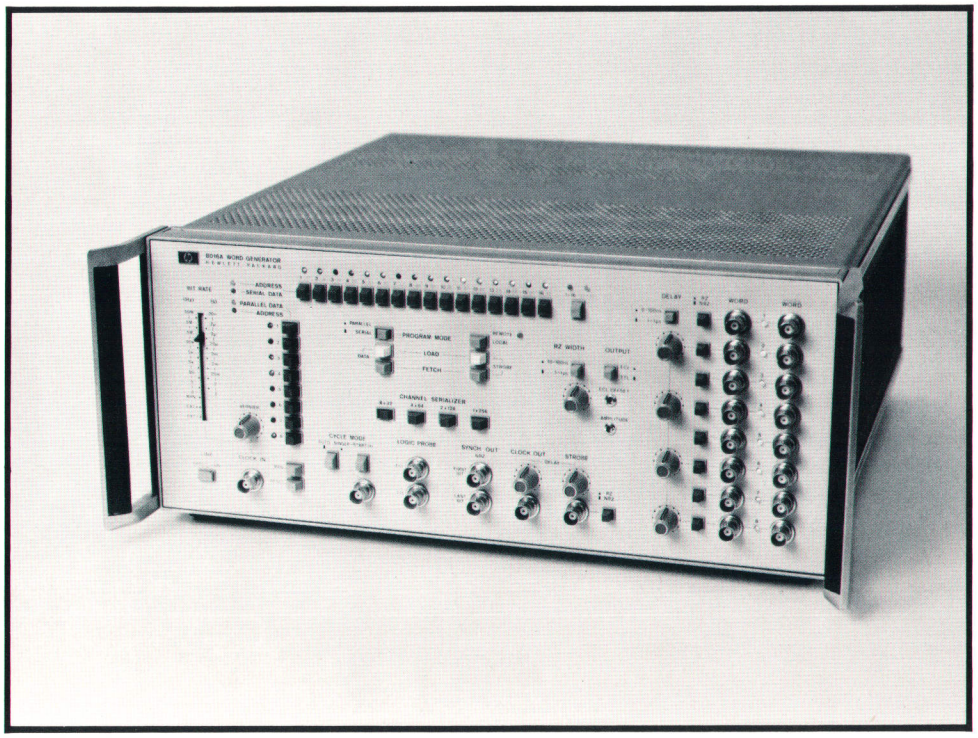


Fig. 1. *Model 8016A Word Generator has eight output channels, each supplying an independently-selectable 32-bit digital word at bit rates up to 50 MHz. Operator control of the output pulse parameters broadens the range of applications for this instrument.*

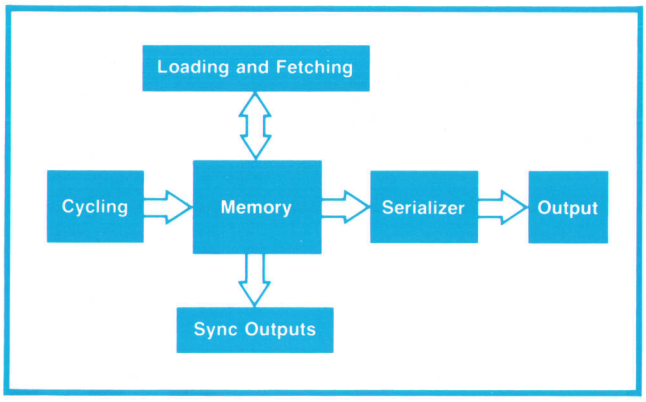


Fig. 2. *Basic block diagram of the Model 8016A Word Generator. The use of a programmable memory gives complete freedom in the choice of bit patterns.*

words are useful for testing shift registers, tape drives, and communications links. Parallel words are needed for testing LSI devices like memories, arithmetic logic units, digital subassemblies, and data buses.

Serial words may also be cascaded to give longer patterns. For example, the instrument may be set to give four 64-bit words simultaneously, or two 128-bit words, or one 256-bit word.

In either the parallel or serial mode, digital test patterns are supplied by the new word generator at clock rates up to 50 MHz, enabling tests of the majority of devices at their maximum rates.

Data Loading and Fetching

The central building block of the instrument is a high-speed semiconductor memory, as shown in Fig. 2. The memory content is read out nondestructively to supply the bit patterns to the output circuits.

A major question facing the designers of this instrument was: how should the data be entered? The front-panel had to be organized in a way that would make operation as self-explanatory as possible. It would have to provide a convenient means of entering 256 bits of new data while being able to tell the user what was already in memory.

The use of 256 front-panel switches was considered too cumbersome so a matrix scheme was adopted. As shown in Fig. 3, the instrument's memory is accessed by a 16-bit row register and an 8-bit column register. Each bit in either register is controlled by a data-setting/resetting pushbutton and its status is displayed by the adjacent LED indicator. The LED is illuminated if the bit is a logic "1".

A serial word is set into the row register. Pressing the LOAD pushbutton transfers the selected word into the memory channel selected in the column register, as shown in Fig. 3a. When more than one channel is addressed, the data is loaded simultaneously into all selected channels.

Pressing the FETCH DATA pushbutton results in a nondestructive readout, transferring the data in any addressed channel back into the row register. The fetched data is then displayed on the LEDs.

To further reduce the number of pushbuttons, each memory channel is divided into two 16-bit subunits. Another pushbutton determines whether the 16 bits in the row register are to go into the 1-16 or 17-32 positions in the memory. If all 32 bits of a channel need to be loaded or fetched, the load or fetch operation is performed twice.

In the parallel mode, an 8-bit byte is entered into the column register and the desired column address is entered in the row register, as shown in Fig. 3b. As in

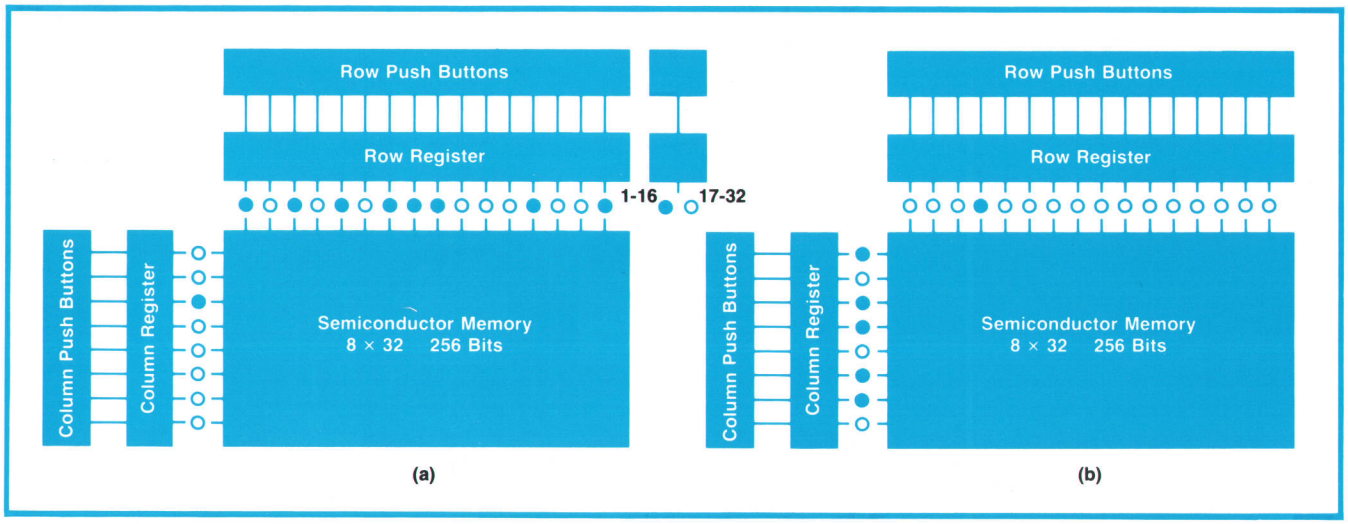


Fig. 3. *X-Y coordinate organization of the switches simplifies the manual loading and recall of data. In the SERIAL mode (left), a serial word is set up in the row register and the channel address is selected in the column register. In the PARALLEL mode (right), a parallel word is set up in the column register and the byte address is selected in the row register.*

the serial mode, loading and fetching are implemented by the LOAD and FETCH pushbuttons.

Data may also be loaded by way of a card reader, a calculator, or a minicomputer. With an optional circuit card and connector installed, the new word generator is compatible with the HP Interface Bus and can function as a bus "listener" to accept bit patterns from external devices (see box). A marked-card reader working through the bus proves to be a fast and convenient way to load the memory, especially if the test patterns have to be changed frequently. The card reader is particularly advantageous for testing on the production line, not only because of the speed of entry (2 seconds per card), but also because human error is avoided in loading the data.

Clocking and Cycling

The bit rate may be controlled by an internal clock generator over a range of 0.5 Hz to 50 MHz. It may also be controlled by an external source of clock pulses over a range of 0 to 50 MHz. The external pulses may be of either polarity. Internal controls permit selection of the trigger threshold and input impedance, enabling direct triggering from TTL (1kΩ input) or ECL (50Ω) circuits.

Words may also be read out one bit at a time with a front-panel pushbutton. This allows time for the user to verify the truth tables of tested circuits with a logic probe (power for HP logic probes is provided at front-panel connectors). As a further convenience, when the instrument is in the manual mode the column LEDs light up to show the bits present at the output at any instant, and the row LEDs show the address of the bit pattern present at the output.

Three modes of word cycling are provided. In the AUTO cycle mode, words are generated repetitively. In the SINGLE cycle mode, one complete word is generated in response to an externally-supplied trigger or to each actuation of the START pushbutton. A GATED cycle mode is enabled by an internal switch. In this mode, words are generated continuously as long as an externally-supplied gating signal is at a logic high, a feature that is useful for external start-stop operation. Regardless of when the gating signal goes back to a logic low, the word sequence is always completed.

Flexible Outputs

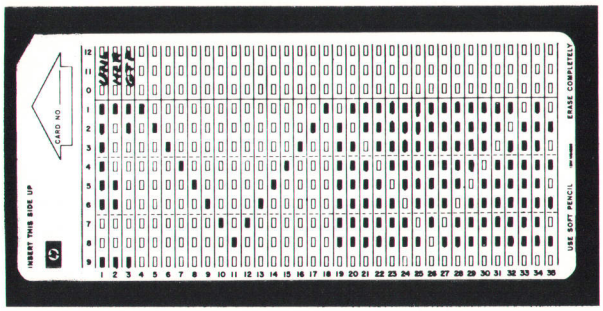
Pulse parameter flexibility was given the new word generator so the testing requirements of a variety of devices can be met. This flexibility also contributes to the simulation of worst-case conditions.

Each data channel (and the strobe channel) has an assigned NRZ/RZ pushbutton switch. In the NRZ format, most often used to simulate address and data signals, each logic "1" maintains its high level for the full duration of the clock period (Fig. 4). In the RZ for-

Word Generator Operation with the HP Interface Bus

Digital patterns can be loaded into the Model 8016A Word Generator by way of the HP Interface Bus (HP-IB), thus making it relatively easy to include the Word Generator in automatic test systems.*

An example of the ease of programming the word generator is shown below. This is a mark-sense card used by a card reader to program the 8016A to accept new bit patterns. The same commands could just as easily be entered by a calculator or computer.



The first command (UNL) on the card "unaddresses" all listeners on the bus so other instruments in the system will not attempt to respond to the commands for the word generator. The second command (MLA) addresses the 8016A. When thus addressed, the 8016A responds to information on the bus. Otherwise it would ignore it. In the case shown, the address is "1" coded in ASCII. Internal switches enable the user to select any address between 0 and 9 for the 8016A.

The third command on the card (GTP) is the instruction to load data in the parallel mode. The data then follows. The 8-bit bytes are marked in columns 1 through 8 on the card, which correspond to the 8 data channels in the instrument. Column 9 indicates whether the information is a command or data; no mark indicates data.

When it receives the GTP (go to parallel) command, the word generator stops its current readout, loads the data from the card and it restarts data generation when byte 32 has been loaded. If less than 32 bytes are to be loaded, the start-generation command (SDG) must follow the last byte.

In the serial mode, the data immediately following the load-in serial command (GTS) is interpreted as a channel number. The 32 bits for that channel are entered in the next four 8-bit bytes and the number following is interpreted as another channel address. Channels can be entered in any order, but the start-data-generation command (SDG) must be used to restart data generation.

The STROBE word is entered similarly using the strobe-byte-follows command (SBF). The 8-bit byte immediately following SBF assigns the strobe word to one or more segments of the serialized data and the strobe word follows in the next four 8-bit bytes.

The SDG command initiates a new readout. When the instrument is in the SINGLE CYCLE mode, it runs through one complete word-generation cycle in response to the SDG command, then stops. When in the AUTO cycle mode, the instrument generates words repetitively until receipt of a load command.

*D.W. Ricci and P.S. Stone, "Putting Together Instrumentation Systems at Minimum Cost," Hewlett-Packard Journal, January 1975.

mat, each logic "1" maintains its high level for only part of the clock period, returning to zero before the start of the next clock period. The RZ format permits generation of pulse-like signals such as clock and enable pulses. The pulse width for all channels operating in the RZ mode is determined by a single control that has a span of 10 to 1000 ns in two ranges.

Each data channel has two outputs, one for the true data and one for the complement. The output level is selectable, giving levels appropriate either for driving TTL circuits or for driving ECL circuits. All output ports have a 50Ω source impedance simplifying the interface to the tested circuits; reflections from impedance mismatches in the external signal path are absorbed and thus do not distort the waveforms.

Controllable Delays

To simulate real operating conditions, the signals in the even-numbered channels, and also in the clock and strobe channels, can be delayed up to 1000 ns with respect to signals in the odd-numbered channels (Fig. 4). These delays permit the user to explore critical timing conditions, as in analyzing the performance of data buses and interface cards.

The delays are not only useful in simulating worst-case conditions, but they are also mandatory in certain situations, such as writing data into a semiconductor memory where the write pulse is applied a prescribed period of time after the address and data have been applied.

Auxiliary Outputs

The word generator has four auxiliary outputs in addition to the eight data outputs. The CLOCK output supplies pulses at the actual bit rate, producing RZ pulses with logic levels determined by the selected logic mode (TTL or ECL). The pulses may be varied in width by the master RZ WIDTH control and may be separately delayed from 0 to 1000 ns with respect to the nondelayable data channels.

Two framing pulses are provided, the FIRST BIT trigger, which occurs only on the first bit of the data sequence and the LAST BIT trigger which occurs only on the last bit, whether or not channels are serialized. These pulses are always in the NRZ format.

The STROBE output performs two functions. When channels are not serialized, the STROBE functions as a ninth 32-bit channel that can be loaded and fetched the same as the data channels. Having nine channels makes it possible to supply three octal words in parallel to external devices. When channels are serialized, the strobe channel can be assigned to read out simultaneously with any of the 32-bit serialized segments that make up the data stream (Fig. 5). This mode is useful as a source of framing pulses or qualifiers to be used with the main data channels. It can also be used as a movable sync pulse to obtain a jitter-free oscilloscope display of any part of a long data stream.

Technical Details

A more detailed block diagram of the Model 8016A Word Generator is shown in Fig. 6. The memory is composed of a bank of 16×1-bit ECL RAMs, with two RAMs for each channel. To obtain bit rates as high as 50 MHz during readout, the RAMs are divided into two groups with the odd-numbered bits stored in one group and the even-numbered bits stored in the other. Readout from the two RAM groups is multiplexed to form single data streams. The RAMs thus operate at a maximum speed of 25 MHz but the data streams are interleaved to produce output patterns at bit rates up to 50 MHz.

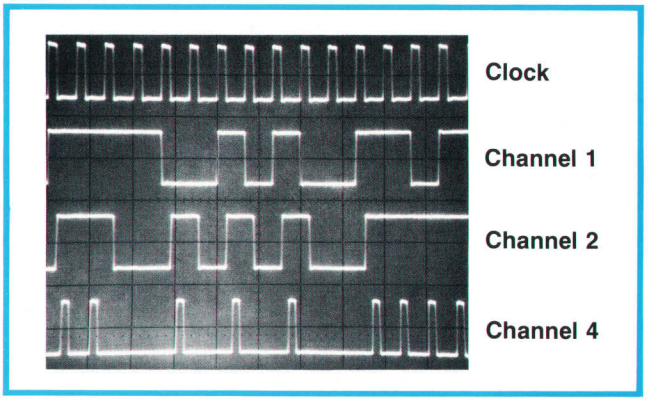


Fig. 4. *Typical pulse trains provided by the Model 8016A Word Generator. The top trace is the clock output. The middle traces are channels 1 and 2 in the NRZ format and the bottom trace is channel 4 in the RZ format. Channels 2 and 4 are delayed with respect to channel 1. (Oscilloscope settings: vertical, 2V/div; horizontal, 200 ns/div.)*

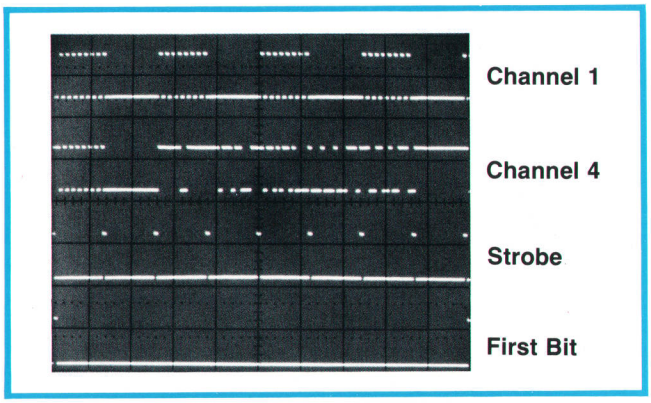


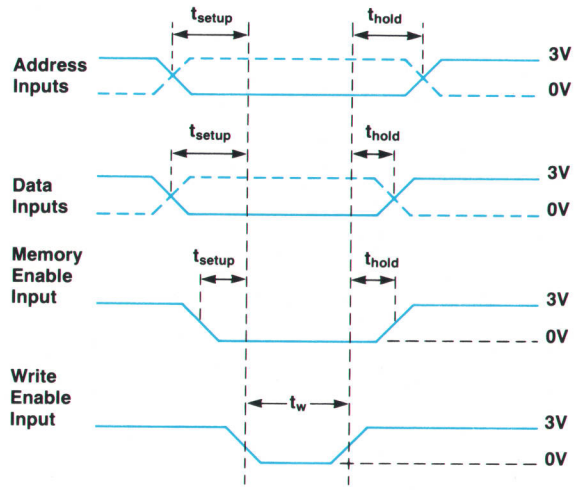
Fig. 5. *Operation in the serialized mode. Channel 1 (top trace) outputs its pattern repetitively, in this case eight 1's alternated with 0's followed by a string of sixteen 0's. Channel 4 outputs channels 1,2,3, and 4 in series. The STROBE word is assigned to all four channels producing a word-framing pulse for dividing the serial stream into 16-bit words. The FIRST BIT trigger occurs only on the first bit of the serialized data stream.*

Problem Solutions with the Model 8016A Word Generator

The development and test of digital ICs and the design and test of logic systems at the module level (PC boards), the unit level (peripherals), and the system level can all benefit from the capabilities of the Model 8016A Word Generator. The unrestricted choice of digital patterns provided by this instrument allows selection of the necessary test patterns, worst-case patterns, and invalid patterns for thorough checkout of a device's behavior. The variable interchannel delays, besides enabling tests of minimum set-up and hold times, also make it easier to identify the sources of crosstalk and "glitches". Varying channel delays one by one helps identify the channel that is the source of the problem.

Testing ICs

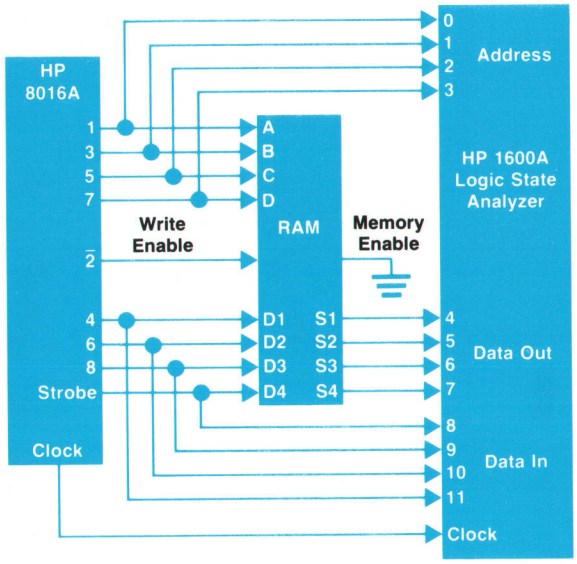
Although the advent of large-scale integrated circuits intensified the need for multichannel signal sources to permit functional tests, the need for electrical parametric tests remains. The effects on circuit performance of bias voltages, pulse amplitudes, signal delays and so on must be evaluated to be certain that a device meets its specifications. For example, testing a semiconductor random-access memory (RAM) requires that address, data, memory-enable, and write-enable signals all be applied with appropriate delays, as shown in Fig. A. A typical RAM is guaranteed to operate properly as long as the setup and hold times are no less than the minimum values specified by the manufacturer.



(A)

The Model 8016A Word Generator can supply the required combination of signals with interchannel delays adjusted to the specified setup and hold times for the device under test. With the 8016A supplying the appropriate signals, operation of the device can be checked with an oscilloscope or logic state analyzer. Actual limits may then be measured by reducing set-up and hold times until device operation fails.

A typical measurement set-up is shown in Fig. B. This illustrates a test of a RAM consisting of 64 TTL flip-flop memory cells organized in a matrix that provides 16 four-bit words. Memory operation is such that when the WRITE ENABLE input is true, information on the data input lines is read into the memory cells specified by the address lines. When the WRITE ENABLE pulse is



(B)

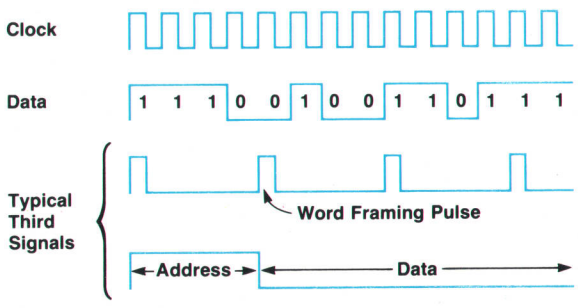
false, the data in the addressed cells is read out. The 8016A Word Generator supplies the address, the data, and the WRITE ENABLE pulse with appropriate delays. The Model 1600A Logic State Analyzer can verify device performance by displaying the address alongside the data read into that address, and also the data read out.

The 8016A is likewise useful for testing serial devices, such as shift registers, disc memories and terminals. Many serial devices actually need three inputs: data, qualifier, and clock. The 8016A supplies a clock signal and serial patterns up to 256 bits in length. The STROBE channel may be used as a qualifier; programming it to generate a string of 1's in the NRZ format effectively creates a wide gating pulse (Fig. C). It may also be used to supply word framing pulses, as shown in Fig. 5, page 20.

With the help of the Model 8016A, many of these tests can be performed economically on a wide variety of devices at incoming inspection stations or for component evaluation.

Design of an Interface

Designing and troubleshooting a computer or bus-system interface for a data terminal, magnetic tape storage unit, card reader, or other peripheral can be simplified by using the Model



(C)

8016A to simulate the interface signals. This can also be more economical than tying up a computer or a data bus system to serve as a test bed. Such systems transfer data on a one-shot basis and the transfer is fast. The single-step capability of the Model 8016A bypasses this problem.

As an example, the HP Interface Bus option for the 8016A itself was designed with the aid of a prototype 8016A supplying the HP-IB commands and data. The interface was first analyzed statically by going through a program stored in the 8016A one step at a time. At each step, logic states in the interface card were examined with a logic probe.

Once static operation was correct, bus commands were applied by the 8016A at high rates to analyze dynamic operation. The use of pattern repetition rates suitable for oscilloscope display —usually not possible with a data bus system—and the variable interchannel delays simplified analysis of interface timing margins. At that time, there was no convenient means other than the 8016A of simulating signals that made troubleshooting the interface so fast and thorough.

On the Production Line

The Model 8016A also effects savings in time and equipment in semiautomatic test equipment on the production line. For example, it is now used to check out the Model 1620A Pattern Analyzer (see page 11).

Functional tests of this instrument are made first. These include a check of its ability to respond to digital patterns, both serial and parallel, at 20-MHz bit rates. Then electrical parameters such as pulse-width sensitivity and data-channel set-up time with respect to the clock are verified.

Digital patterns for thoroughly checking the 1620A are stored in a calculator and transferred to the 8016A on the HP-Interface Bus as needed. The operator controls the sequence of patterns with the calculator and adjusts pulse widths and channel delays while monitoring the instrument under test.

In this case, one Model 8016A replaced an array of pulse and word generators that had been used to provide the necessary functional and electrical stimuli. Not only did this simplify the setup, but it also provided the multichannel signals with less skew and jitter than could be provided by interconnected generators.

These examples represent a small sample of the kinds of applications that can benefit from use of the Model 8016A Word Generator.

Jürgen Buesen

When the LOAD button is pressed while the instrument is in the SERIAL mode, a six-state algorithmic state machine (ASM) generates the necessary control signals for sequentially interrogating the row-register flip-flops and loading bits serially into the selected channel(s) in memory. When the instrument is in the PARALLEL mode, the ASM scans the row register for addresses and loads the contents of the column register in parallel into the main memory.

The channel serializer is a multiplexer that sequentially gates channel outputs into a common path. The channel that outputs the serialized data is indicated by illumination of a LED adjacent to its output connectors. The other channels continue to output their bit patterns repetitively (see Fig. 5). For example, with the serializer in the 2×128 mode, channel 4 outputs the bit patterns of channels 1, 2, 3, and 4 serially, and channel 8 outputs 5, 6, 7, and 8 while channels 1, 2, 3, 5, 6, and 7 output their 32-bit patterns repetitively.

Data Delay and Width

The output circuit for one of the delayable channels is shown in Fig. 7. The RAM-sync flip-flop resynchronizes the data from the memory and its output is applied in the NRZ format to the D input of the

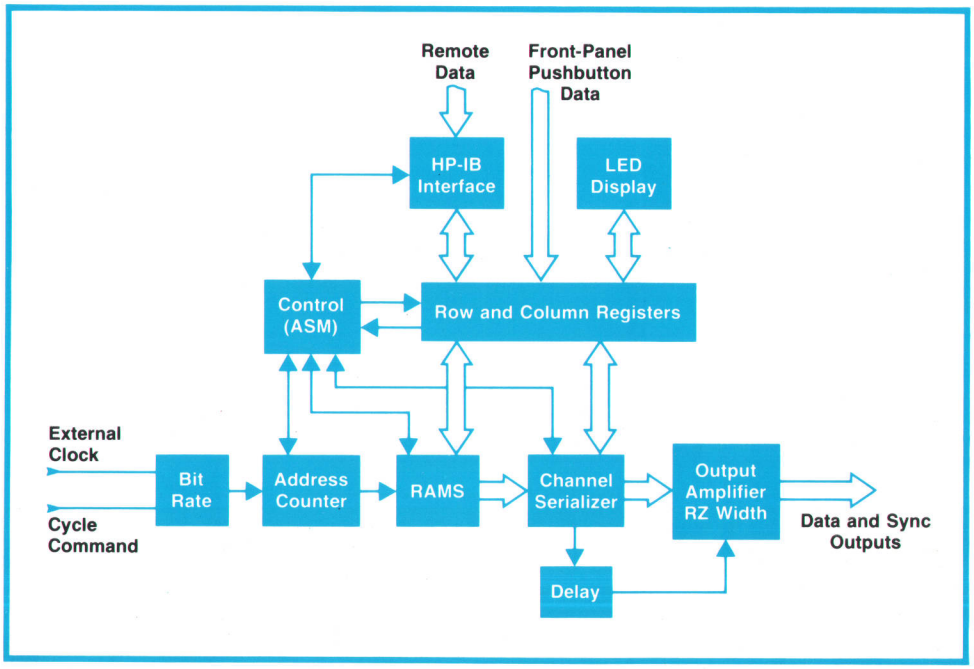


Fig. 6. *Word Generator architecture.*

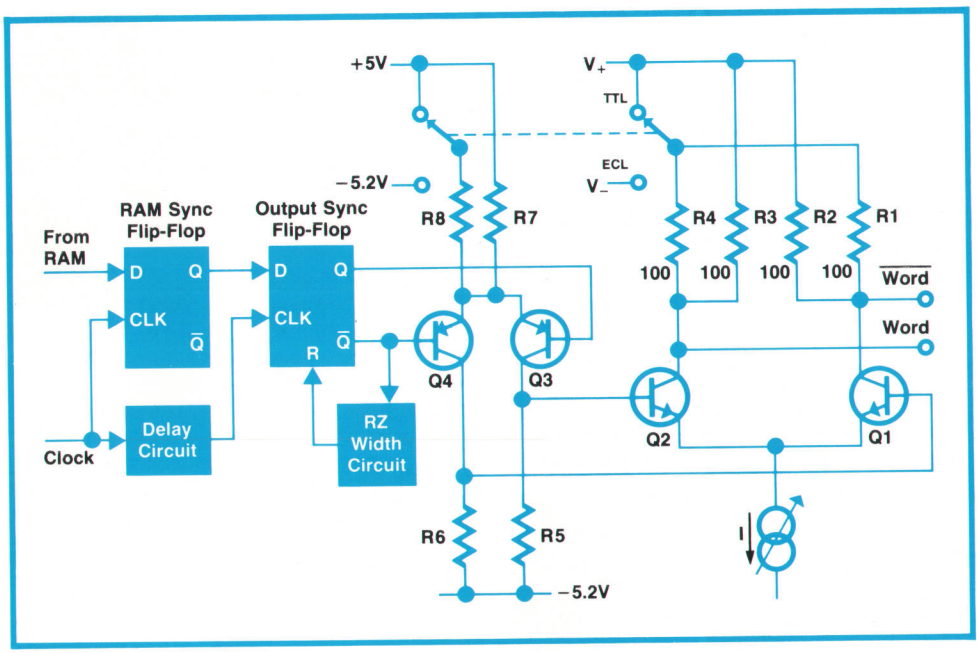


Fig. 7. *Output circuit for one of the delayable channels. The output stage has switchable dc levels and adjustable signal amplitudes to match drive requirements of tested circuits.*

output-sync flip-flop. The clock for this flip-flop is delayed, however, by a monostable multivibrator, thus delaying the output of this flip-flop according to the corresponding DELAY control.

For the nondelayable channels, a common clock signal is supplied in parallel to the output sync flip-flops. This assures low skew in the timing of the output pulses (less than ±1 ns). A small fixed delay in the common clock signal allows the delayed channels to be adjusted to zero relative delay.

When the RZ mode is selected for a channel, the transition caused by a "1" data bit at the $\overline{Q}$ output of the output-sync flip-flop triggers the RZ-width circuit, a monostable multivibrator. The trailing edge of this multivibrator's pulse resets the output-sync flip-flop to derive the RZ pulse.

The nondelayable channels (channels 1, 3, 5, and 7) use a common RZ-width circuit with FET switches to interrupt the flip-flop reset signal where RZ operation is not desired. The RZ width for all channels is controlled by a single potentiometer that in turn supplies a dc voltage to current-control transistors in all of the RZ-width circuits.

Output Circuits

Data from the output-sync flip-flop in each channel is fed through a driver stage to the output stage, a non-saturating differential amplifier (Fig. 7). The output impedance looking back into the instrument is determined by the load resistors in the collector circuit of each transistor. Two resistors are used.

In the TTL mode, both resistors are connected to a variable positive voltage, V_+. This voltage is adjusted by a front-panel screwdriver control to give an open-circuit amplitude range of 2 to 5 V for the output pulse tops. The current source in the emitter circuit tracks this voltage so $V_+ - I \times 50\Omega = 0$, thus maintaining the output pulse baseline at 0 V throughout the amplitude range. Transition times are ≤3 ns in this mode.

In the ECL mode, one of the resistors is connected to a negative voltage V_- and the current source is reduced to 40 mA. At the same time, one of the resistors in the emitter circuit of the driver (Q3, Q4) is switched to a negative voltage, reducing the drive pulses. This method of reducing output amplitude retains the clean waveform that was obtained in the TTL mode. Transition time in the ECL mode is ≤2.5 ns (10% to 90% amplitude).

The voltage V_-, offset from V_+ by −5 V, tracks V_+ to give control of the level of the ECL logic high over a range of −0.9 to +1.1 V. The current I is separately varied to give control of the logic low, giving a range of 0.3 to 1 V for the logic swing.

Timing

The internal rate generator is a ramp type commonly used in pulse generators. A constant current charges a capacitor until the capacitor voltage reaches a trigger level that turns on a discharge circuit, quickly discharging the capacitor and starting the next cycle.

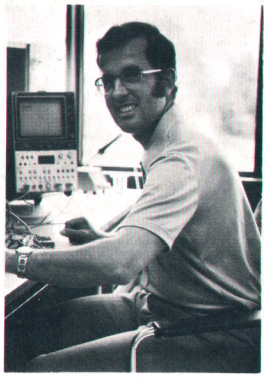
In the Model 8016A, the repetition rate, controlled by the charging current, has a basic range of 5 to 50 MHz. All the slower ranges are obtained by decade dividers. The dividers generate a gate that allows one rep-rate pulse out of 10 (or 100, or 1000, or up to 10^7) to pass, assuring low jitter at all repetition times.

Acknowledgments

Günter Riebesell developed the bit rate generator and the output circuits. The delay generator circuits were designed by Herbert Schuler. Sigurt Krass contributed to the HP-IB card and Horst Link was responsible for the mechanical design.

Special thanks are due R&D Manager Jörn Kos for overall guidance of the project, to Jürgen Buesen for help in defining the instrument, and to Walter Stahlecker and Herman Hinton for marketing inputs.

Wolfgang Kappler



A graduate of the University of Stuttgart (Diplom Ingenieur), Wolfgang Kappler joined HP in 1965, going to work on pulse generators. He subsequently became project leader for the 8057A Noise Generator and the 8006A Word Generator before becoming project leader for the 8016A Word Generator. When time permits, Wolfgang enjoys hunting in the Black Forest. He's married and has one son and one daughter.

Arndt Pannach

At HP since 1969, Arndt Pannach initially designed calculator peripherals like tape readers and typewriter couplers. He then set up a thin-film laboratory for production of very fast logic circuits. He is now group leader for word and data generators. Arndt graduated as a Diplom Ingenieur from the University of Stuttgart. A member of the HP GmbH R and D soccer team, he also enjoys skiing in the Alps and hiking with his family (two girls 6,3 and a boy, 2).

SPECIFICATIONS

Hewlett-Packard Model 8016A Word Generator

NUMBER OF CHANNELS: 8 data channels plus 1 strobe channel.
NUMBER OF BITS PER CHANNEL: 32 (fixed).
Data can be loaded in parallel or serial form depending on the position of the PROGRAM MODE switch.
CHANNEL SERIALIZER: Permits cascading of output channels to form longer words.
8 words on 8 channels, each 32 bits long;
4 words on 4 channels, each 64 bits long;
2 words on 2 channels, each 128 bits long;
1 word on 1 channel, 256 bits long.
BIT RATE:
INTERNAL: 0.5 Hz to 50 MHz in eight ranges. Vernier provides continuous adjustment within ranges.
EXTERNAL: dc up to 50 MHz or manual triggering.
RECYCLING:
AUTO MODE: data is recycled continuously.
SINGLE CYCLE (2 modes): a) One word generated for each cycle command. b) Words generated as long as a cycle command is active. Last word always completed. If channels are serialized, serialized word (64 bits, 128 bits, 256 bits) is always completed.
CYCLE COMMAND:
AMPLITUDE: ≥ +2V, ≤ +10V.
WIDTH: ≥12ns.
INPUT IMPEDANCE: 1kΩ.
MANUAL RESET:
AUTO CYCLE: All channel outputs set to "0". Next clock pulse after RESET generates byte number one.
SINGLE CYCLE: All channel outputs reset to word pause. Word pause controlled by rear-panel switch, can either be "ZERO" or "LAST BYTE".

Data Outputs

Two separate outputs per channel, one for normal and one for complement. The level of all output signals is controlled by a TTL-ECL switch. Adjusts for amplitude and offset.
TTL (across 50Ω): HIGH LEVEL variable from 2.5V to 1V. LOW LEVEL ≤ +0.2V. Transition times, ≈3.0ns (First/Last Bit Trigger = 4.0ns).
ECL (across 50Ω): HIGH LEVEL OFFSET variable from −0.9V to +1.1V. Amplitude variable from 0.3V to 1.0V. Transition times, ≈2.5ns (First/Last Bit Trigger = 4.0ns).
SOURCE IMPEDANCE: 50Ω.
DELAY: Four channels can be separately delayed between 0 ns and 1 μsec in two ranges with reference to channels 1,3,5 or 7. Ranges are common to all delayable channels. Channels have individual vernier controls.
DELAY JITTER: 0.1% + 50ps.
FORMAT: RZ or NRZ, separately selectable for each data channel and strobe channel.
RZ WIDTH: 10 nsec to 1 μsec in two ranges. Vernier provides continuous adjustment within ranges. Range switch and vernier is common to all channels.
WIDTH JITTER: ±0.2% +50ps.
SKEWTIME: Skewtime of undelayable channels (1,3,5,7) with reference to channel one: ± 1ns.

Auxiliary Outputs

FIRST BIT: Simultaneous with first bit of a frame. Format is NRZ.
LAST BIT: Simultaneous with last bit of a frame. Format is NRZ.
CLOCK: Delivers one pulse per bit. Format is RZ. Clock pulse may be delayed between 0 ns and 1 μs with respect to channels 1,3,5 or 7.
CLOCK PULSE WIDTH: controlled by RZ-Width control.
STROBE WORD: Separate LOAD and FETCH pushbuttons. Length, 32 bits. Can be assigned to any or all words within a serialized word frame. The strobe word may be delayed between 0 ns and 1 μs with respect to channels 1,3,5 and 7.
AMPLITUDE OF AUX. OUTPUTS: TTL or ECL voltage levels variable by front-panel control.
SOURCE IMPEDANCE: 50 ohms.
PROBE POWER:
ECL: −5.2V dc ± 10%, 80mA.
TTL: +5V dc ± 10%, 100mA.

General

OPTIONS:
OPTION 001, REMOTE PROGRAMMING: Bit pattern can be programmed by any controller that is compatible with the HP Interface Bus.
OPTION 002, CARD READER: permits loading 8016A memory from punched or marked cards via option 001 input.
PRICES IN U.S.A.: 8016A, $6400.
Opt 001, $550; Opt 002, $660.
MANUFACTURING DIVISION: HEWLETT-PACKARD GmbH
Werk Böblingen
Herrenberger Strasse 110
D-703 Böblingen, Württemberg
West Germany

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