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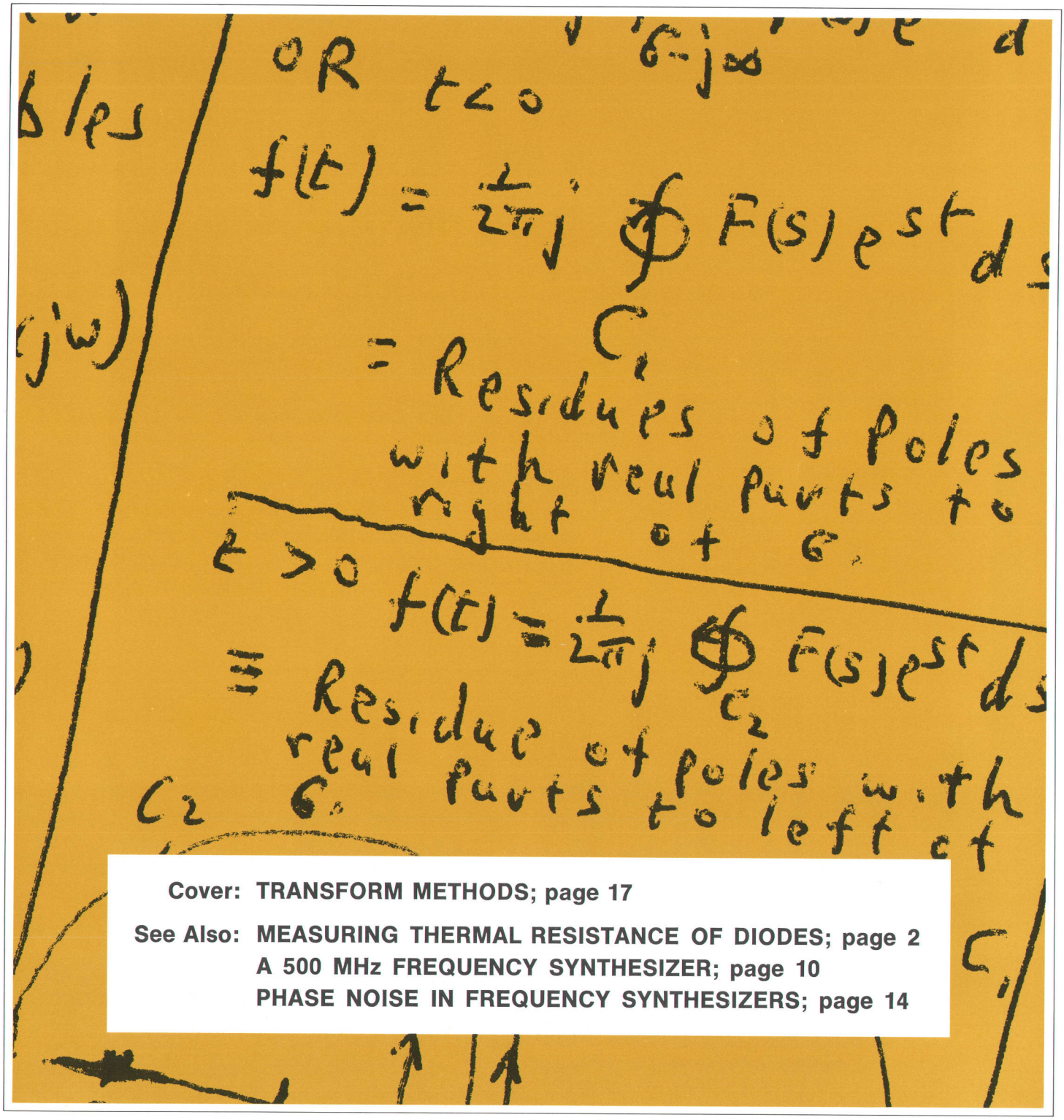

Cover: TRANSFORM METHODS; page 17

See Also: MEASURING THERMAL RESISTANCE OF DIODES; page 2
A 500 MHz FREQUENCY SYNTHESIZER; page 10
PHASE NOISE IN FREQUENCY SYNTHESIZERS; page 14

OCTOBER 1967

A System for Measuring the Thermal Resistance of Semiconductor Diodes

A fast, automatic system for accurately measuring junction-to-case thermal resistance of semiconductor diodes.

By Norman R. Galassi and Bernard S. Siegal

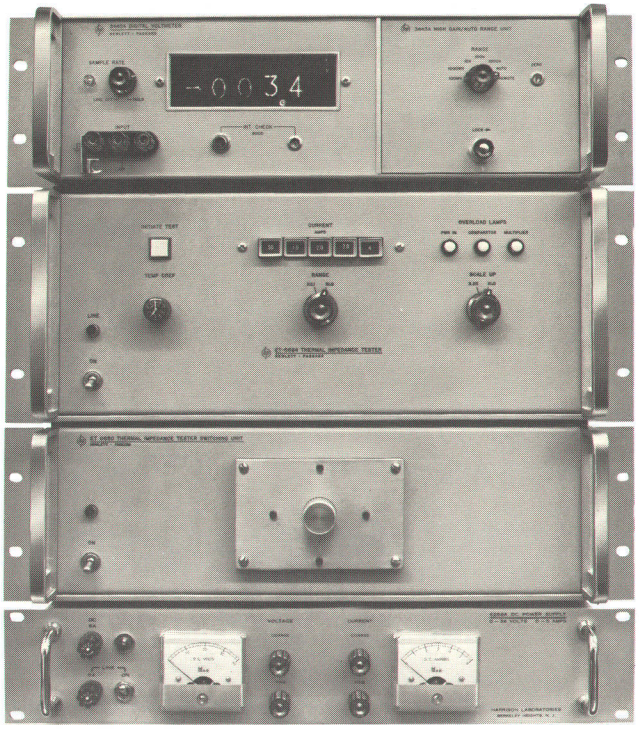

Fig. 1. *This complete thermal resistance measurement system speeds evaluation of diodes. In production, it allows fast checking for packaging faults. The diode under test is placed in the heat sink located in the center of the rack second from the bottom.*

THERMAL RESISTANCE OF SEMICONDUCTOR DIODES is one of the more important parameters specified on a diode data sheet. Knowing the guaranteed thermal resistance of a particular type of diode, a designer can determine if this diode will survive its own internally generated heat when used in the equipment he designs.

The problem in making a determination, however, is that many published specifications are not guaranteed and often inaccurate, even if unintentionally. Inaccuracy arises because of a lack of standardization of measurement of thermal resistance, and because inaccuracies creep in due to rudimentary methods of measurement.

Attempts have been made to standardize the measurement of thermal resistance. The Department of Defense and the Joint Electron Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) have published material toward this end. One such technique, called 'Method 4081 of MIL-STD-750A,' gives only an outline of a thermal resistance test. Another publication, the 'Technical Report on the Measurement of Thermal Resistance' of JEDEC describes several measurement methods and explains the sources of error.

However, details to implement these methods are not fully described. Different manufacturers are using different techniques which lead to differences in their pub-

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lished specifications. Therefore, as a safety factor, designers often reduce the rating from published specifications by 50 to 90%. Diodes with small thermal time constants (e.g., some step-recovery diodes) are the biggest problem since they heat and cool so rapidly that accurate measurements are difficult. To resolve these problems, Hewlett-Packard Associates has developed a system shown in Fig. 1, whose accuracy can be demonstrated. In addition, the system speeds measurement time from the 3 to 10 minutes now required to about 10 to 20 seconds.

For most circuit applications, the total thermal resistance that a device presents to its surroundings consists of several separate thermal resistances as expressed in Equation 1.[1]

$$\theta_{ja} = \theta_{jc} + \theta_{cs} + \theta_{sa} \tag{1}$$

where

θ_{ja} is the total thermal resistance of the heat path from the diode junction to its surroundings,

θ_{jc} is the thermal resistance of the heat path from the diode junction to the diode case,

θ_{cs} is the thermal resistance of the heat path from the diode case to the heat sink (mica washer, etc.), and

θ_{sa} is the thermal resistance of the heat path from the heat sink to the surroundings (ambient).

The total thermal resistance (θ_{ja}) is the quantity that the circuit designer needs to know. Generally the semiconductor manufacturer has direct control only over the junction-to-case thermal resistance (θ_{jc}), and this is the parameter usually specified on the data sheet.

The thermal resistance of any diode or heat sink is defined as the ratio of the steady state temperature difference between the particular points of interest on the device to the power causing the temperature rise.[2] This is expressed by:

$$\theta_{jc} = \frac{T_j - T_c}{P_a} \tag{2}$$

where

θ_{jc} is the thermal resistance of the particular heat path under consideration (junction to case),

T_c is the temperature of the cooler end of the path (case),

T_j is the temperature of the hotter end of the path (junction),

P_a is the power applied to cause temperature rise.

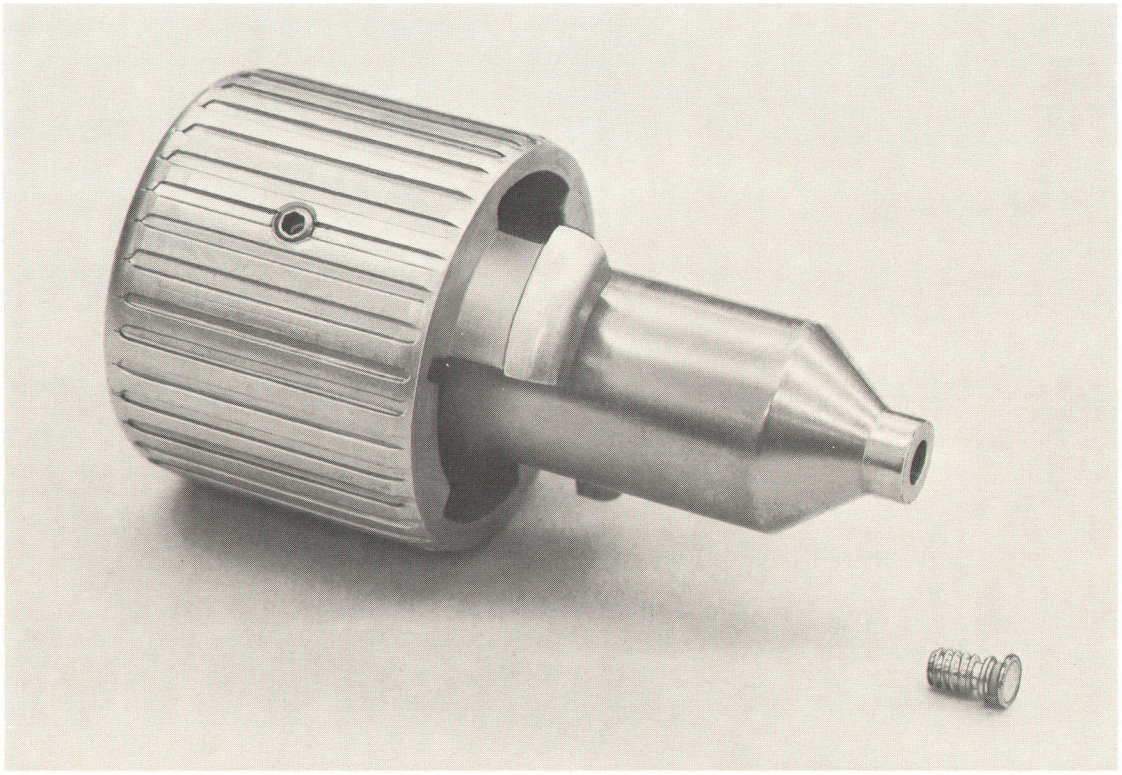

Fig. 2. *The large thermal mass of the diode holder keeps the case temperature substantially constant during the measurement. The diode, right, is inserted into the small threaded hole.*

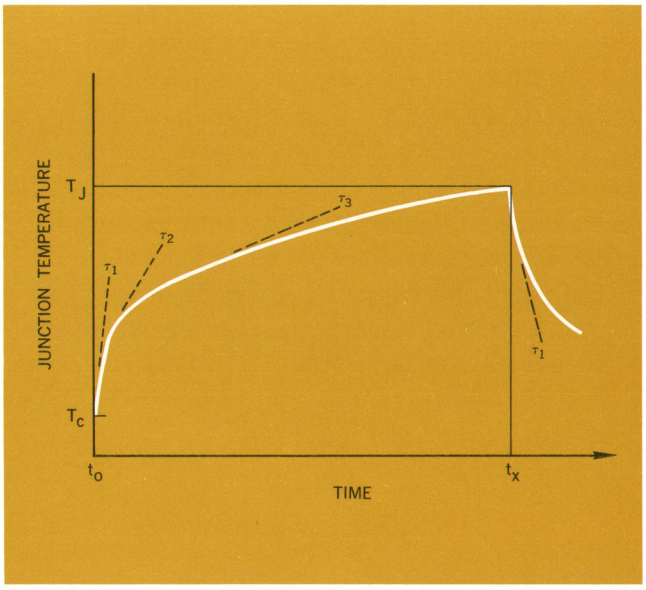

Fig. 3. *A typical plot of junction temperature as a function of time. Heating power is applied at* T_o *and removed at* T_x. *The slope of several thermal time constants,* τ_1, τ_2, τ_3, *are shown. These may vary from about 100 μs to 10 to 20 seconds.*

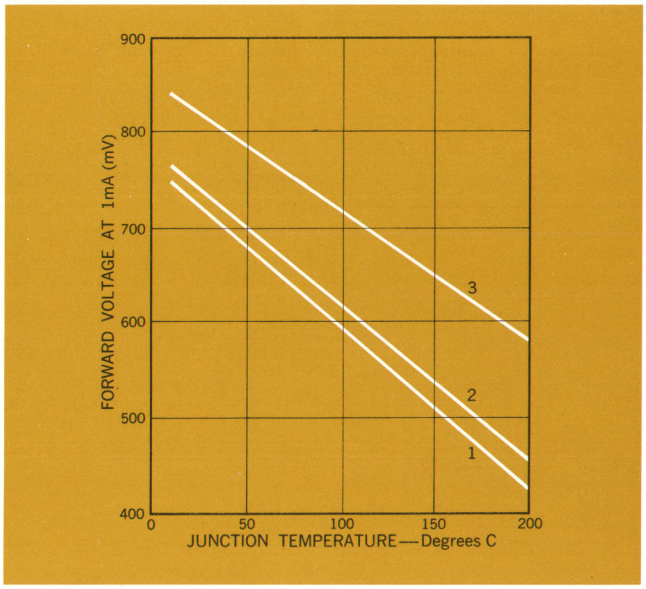

Fig. 4. *Typical plots of temperature coefficient* K *(forward voltage at 1 mA) for two types of step recovery diodes. Curves 1 and 2 are for diodes of the same type from different lots and show that* K *is essentially the same, but forward voltage can differ. Curve 3 is for a different type of diode, and both* K *and forward voltage differ from Curves 1 and 2.*

Measuring Thermal Resistance

In order to determine θ_{jc} for diodes, it is clear from Equation 2 that three quantities must be measured:

T_c, the case temperature,

T_j, the junction temperature,

P_a, the power applied to the diode under test in order to raise the junction temperature.

To measure the junction temperature, it is practical to monitor a temperature-sensitive parameter. In semiconductor diodes, the forward voltage drop at a small fixed forward current (0.01 to 5.0 mA) is an excellent parameter to monitor since it is fairly linear with temperature and is repeatable.

If the diode under test is mounted in a fairly good 'infinite' heat sink ($\theta_{cs} + \theta_{sa}$ small), Fig. 2, the junction temperature before the heating power is applied will be the same as the case temperature. The case temperature changes little during junction heating.

It is extremely important to remember that the steady state temperature difference is used in calculating thermal resistance. Most diodes exhibit several separately identifiable thermal time constants, Fig. 3.[3] This requires that the power be applied for a time much longer than the largest time constant of the diode so that the steady state condition is reached before the junction temperature is measured. In addition, it is necessary to interrupt the heating power to measure forward voltage at the forward current used to determine junction temperature. This must be done quickly after interrupting the heating power; the time interval must be small with respect to the shortest thermal time constant of the diode under test.

To measure junction temperature by using the forward voltage of the diode under test we must first measure the temperature coefficient of forward voltage of the diode under test. The temperature coefficient is:

$$K = \left.\frac{T_2 - T_1}{V_{fm2} - V_{fm1}}\right|_{I_{fm} = \text{constant}} \qquad (3)$$

where K is the temperature coefficient (°C/mV)

T_1 is the lower test temperature (usually 25°C),

T_2 is the higher test temperature (greater than the highest that could be reached during the measurement of θ_{jc}),

V_{fm1} is the forward voltage at I_{fm}, T_1,

V_{fm2} is the forward voltage at I_{fm}, T_2, and

I_{fm} is the fixed forward measurement current.

While there is a fairly large ($\pm 10\%$) variation in the

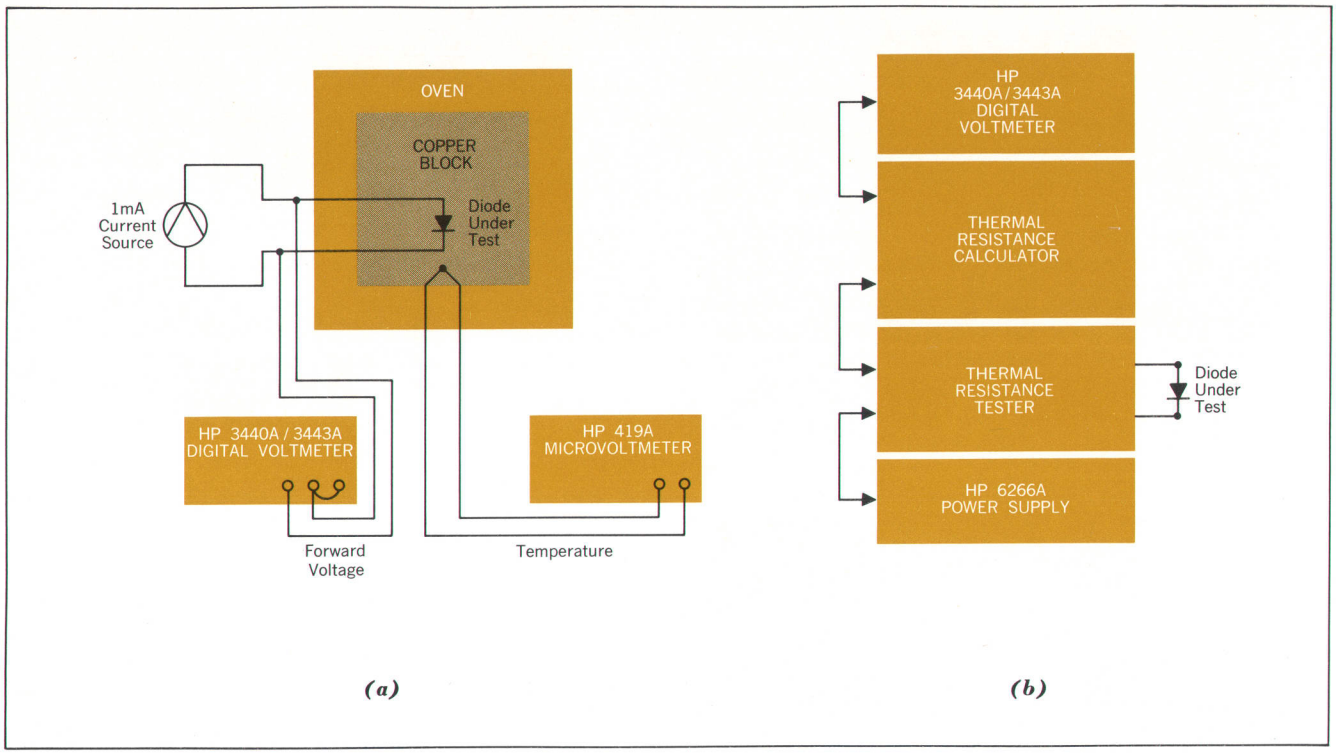

Fig. 5. *Temperature coefficient measurement system* ***(a)*** *is used for characterizing new diode types or spot checking during production if desired. The system* ***(b)*** *(pictured in Fig. 1) determines thermal resistance in about 10 to 20 seconds per diode, which enables fast measurement of large quantities of diodes.*

absolute value of the forward voltage at a fixed temperature and forward current for diodes from different lots (batches), the temperature coefficient is relatively constant ($\pm 3\%$) from lot to lot for diodes of the same type (number), Fig. 4. This allows us to measure the temperature coefficient of a sample of diodes of a given type and use the average value of the temperature coefficient in the thermal resistance calculations for that type diode.

To heat a semiconductor diode, a known fixed forward current is applied to the diode and the resultant forward voltage measured. The dc power thus applied is:

$$P_a = I_{fh} \times V_{fh} \tag{4}$$

where

P_a is the heating power applied to the diode,

I_{fh} is the heating current applied to the diode,

V_{fh} is the forward voltage of the diode at I_{fh}.

The measurement of the thermal resistance of diodes then requires three steps.

1. Determine the temperature coefficient of forward voltage (K) at the measurement current (I_{fm}) over the specified temperature range (T_1 and T_2 specified).
2. Measure the required parameters — V_{fmj}, V_{fmc} and V_{fh} at a predetermined I_{fm} and I_{fh}.

where

V_{fmj} represents the forward voltage corresponding to the temperature of the junction heated and

V_{fmc} represents the forward voltage corresponding to the temperature of the case.

3. Calculate the thermal resistance by:

$$\theta_{jc} = \frac{(V_{fmj} - V_{fmc})K}{V_{fh} \times I_{fh}} \tag{5}$$

Thermal Resistance Measurement System

As shown, the measurement of diode thermal resistance consists of measuring several different quantities, then calculating the thermal resistance of the diode under test. This can be a very time consuming task, taking as long as three to ten minutes per diode. If an adequate characterization of the temperature coefficient is first made, Fig. 5(a), the system described in this article can calculate the thermal resistance of an average diode in between 10 and 20 seconds. This makes the thermal resistance calculation system quite useful for evaluating packaging techniques, package uniformity, and product quality in R & D, production, and Quality Assurance. This system has the following pertinent specifications:

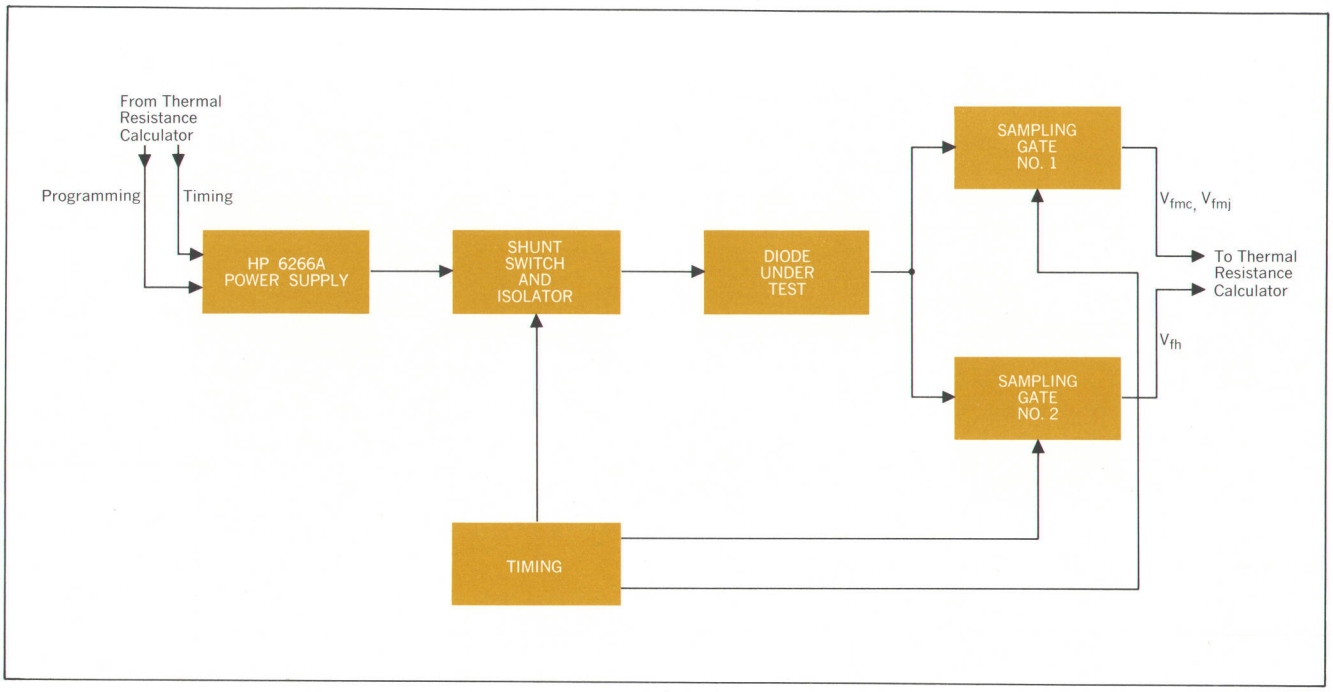

Fig. 6. *The thermal resistance tester portion of the measurement system contains the diode under test. Programming and timing of the power supply, left, is controlled by the thermal resistance calculator and sequencer section.*

- Heating current (I_{fh}) capability: 0.05 to 5.0 amps (Power capability to 40 watts — dependent on the diode
- Measurement current (I_{fm}): 1.0 mA
- Measurement duty cycle: 1.0%
- Accuracy: +8, −10%

The HPA thermal resistance measurement system consists of three main subsystems:

- The Temperature Coefficient Measurement System
- The Thermal Resistance Tester (measurement circuits)
- The Thermal Resistance Calculator

Temperature Coefficient Measurement System

In practice samples of diodes can be measured on a periodic basis to insure that the proper value of K (as defined in Eq. 3) is used in measuring the thermal resistance.

The temperature coefficient measurement system used for this measurement, Fig. 5(b), consists of an oven, a block of large thermal mass (on which the diodes are mounted), a constant current source for supplying I_{fm}, a temperature measurement system, and a forward voltage readout, such as an HP 3440/3443 DVM. The diodes to be measured are mounted in the block and placed into the oven. The oven temperature is adjusted to the specified T_1, and the forward voltage V_{fm1} is measured on all of the diodes at I_{fm} and T_1. The oven temperature is then adjusted to the specified T_2, and the forward voltage V_{fm2} is measured on all of the diodes at I_{fm} and T_2. The temperature coefficients are then determined using Eq. 3, and the average value is calculated for a number of sample diodes.

Since we have found the temperature coefficient K to be fairly constant over a wide range of temperatures, it might be more practical to use constant temperature water baths at 0°C and 100°C to make temperature coefficient measurements on large quantities of diodes.

Thermal Resistance Tester

The thermal resistance tester, Fig. 6, performs the measurement of V_{fmc}, V_{fmj}, and V_{fh}. V_{fmc} and V_{fmj} are measured during a 10 μs interval when the heating current is interrupted and only I_{fm} flows through the diode under test. V_{fh} is measured during the time the heating current is applied to the diode under test. These functions are performed by four main sections:

1. *Shunt switch.* The shunt switch, Fig. 7(a), removes the heating current I_{fh} from the diode under test and the blocking diodes isolate it so only the 1.0 mA measurement current I_{fm} flows. Thus, V_{fmc} and V_{fmj} may be measured during the 10 μs interval. The shunt switch turns off I_{fh} for a 10 μs interval at a 1.0 kHz rate (1.0% duty cycle).

2. *Sample gates.* The sample gates, Fig. 7(b), are used to measure V_{fmc}, V_{fmj}, and V_{fh}. V_{fmc} and V_{fmj} are measured by Sampling Gate No. 1, but at different points in time (determined by the Thermal Resistance Calculator). Sampling Gate No. 2 is used to measure V_{fh}.
3. *Timing circuits.* The timing circuits synchronize the sampling gates with the shunt switch so they switch on and off at the proper times, Fig. 8.
4. *Heating current source.* The heating current source supplies the heating current I_{fh} to the diode under test. The heating current source consists of an HP Model 6266 Power Supply programmed to supply a predetermined current at a time determined by the Thermal Resistance Calculator.

Thermal Resistance Calculator

The Thermal Resistance Calculator, Fig. 9, acts as the main control unit for the Thermal Resistance Tester, current source, and DVM in addition to performing the operations required to solve Eq. 5. It consists of seven subsections:

1. *Two sample and hold circuits.* One circuit samples V_{fmc} (before the current source is turned on) and stores the value in analog form. The second sample and hold circuit samples V_{fmj} (after variable delay interval after the current source is turned on so steady state T_j is reached) and stores the value in analog form.
2. *The subtraction circuit.* Performs the operation $V_{fmj} - V_{fmc}$ on the outputs from the sample and hold circuits.
3. *The power calculator.* Performs the operation V_{fh} times the programmed I_{fm} to obtain P_a. The value of P_a is converted into digital form by the HP Model 3440/3443.
4. *The division circuit.* Performs the operation:

$$\frac{\theta_{jc}}{K} = \frac{V_{fmj} - V_{fmc}}{P_a}$$

This is accomplished using a multiplying digital-to-analog converter and a comparator to divide $(V_{fmj} - V_{fmc})$ in analog form by P_a in digital form.

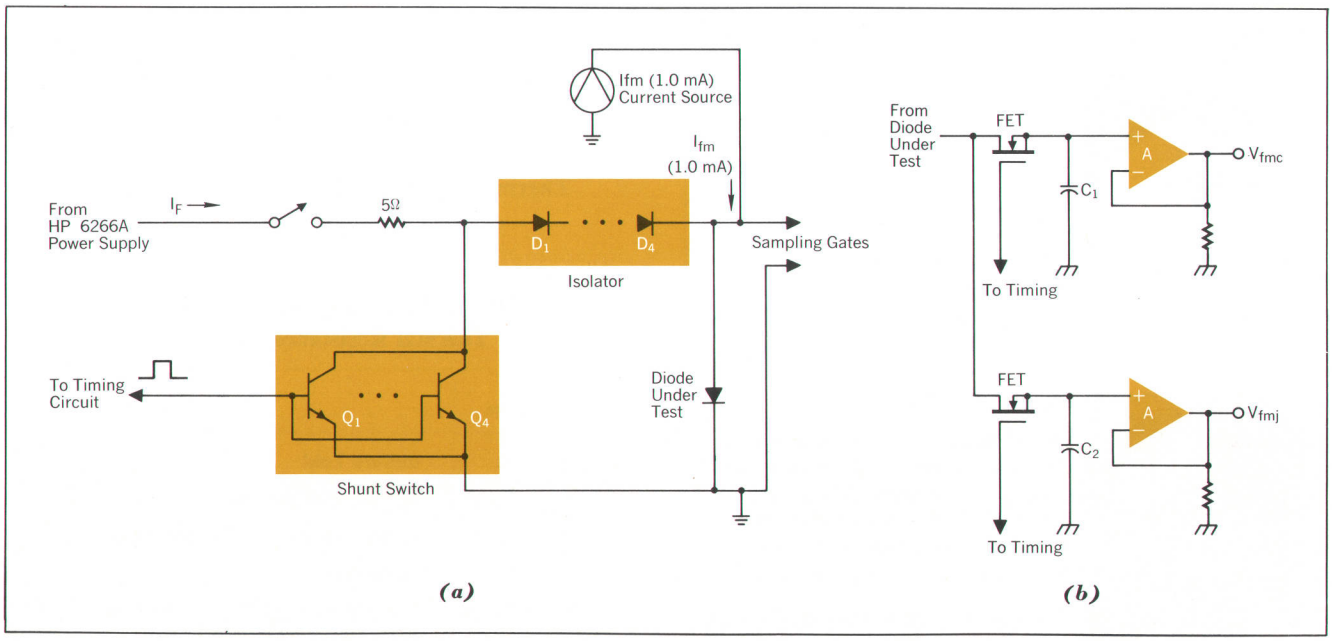

Fig. 7. *The shunt switch* **(a)** *of the thermal resistance tester section removes the heating current* I_{fh} *from the diode under test. The blocking diodes isolate the diode under test from the shunt switch so only the measurement current flows through it. Transistors* Q_1 *through* Q_4 *should be capable of switching 1–2 amperes each in less than 0.5 μs, and the diodes* D_1 *through* D_4 *should have a minority carrier lifetime of less than 0.2 μs at 5 amperes.*

During the measurement interval, the sampling capacitors in the sampling gates **(b)** *are connected to the diode under test through the FET's, which have a low 'on' resistance. The capacitors retain the value of the voltage sampled since the FET's have a high 'off' resistance at other than the measurement interval, and the high-impedance buffer amplifiers isolate the measurement circuitry from the capacitors.*

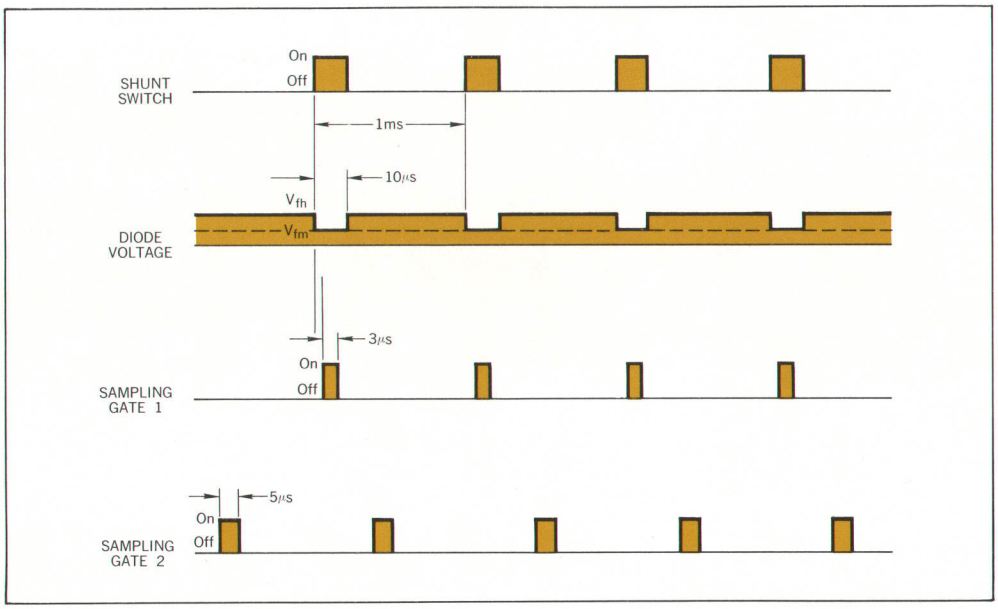

Fig. 8. *Timing diagram of the thermal resistance measurement. Sampling Gate #1 samples* V_{fm} *and it can be delayed as long as 6 μs from the turn-on time of the shunt switch. This delay permits diodes with a long minority carrier lifetime adequate time to reach* V_{fm} *from* V_{fh}. *Sampling Gate #2 samples* V_{fh}.

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Norm Galassi worked part time for Hewlett-Packard while attending San Jose State College. After receiving his Bachelor of Science in Electrical Engineering in 1965, he joined Hewlett-Packard Associates as a production process engineer.

In 1966 he joined the HPA Test and Evaluation Group and he is presently responsible for design and fabrication of production test equipment.

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Bernard S. Siegal

Bernie Siegal is a 1963 graduate of Cornell University with the degree of Bachelor of Electrical Engineering. He received his Master of Science in Electrical Engineering from San Jose State College in 1966.

Previous to joining Hewlett-Packard Associates in 1966, Bernie was engaged in research and development on microwave tubes. At HPA he is a semiconductor applications engineer.

Bernie is a Member of IEEE and is presently attending Stanford University on the Hewlett-Packard Honors Cooperative Program.

5. *The timing circuits.* These circuits time all other circuits in the Thermal Resistance Calculator as well as the power supply and the DVM, Table I.
6. *The programming circuits.* These circuits program the power calculator as well as the power supply and the DVM.
7. *The digital readout.* This consists of an HP Model 3440/3443 DVM. The DVM first reads the value of the power input to the diode under test, converts it into digital form, and returns this data to the Thermal Resistance Calculator. The DVM then

TABLE I Time Sequence of Operation of Thermal Resistance Calculator

Time	Action
T_0	*Initiate Test*
T_1	*Sample and hold* V_{fmc}
T_2	*Apply* I_{fh} *to the diode under test*
T_{TD}	*Time delay**
T_3	*Sample and hold* V_{fmj}*; calculate* $V_{fmj} - V_{fmc}$*; calculate power*
T_4	*Read power on DVM*
T_5	*Calculate* $\theta = \frac{V_{fmj} - V_{fmc}}{K P_a}$; *Turn off* I_{fh}.
T_6	*Read* θ *on DVM*

* The time delay between T_2 and T_3 can be set between 1 and 30 seconds to allow the diode under test to reach thermal equilibrium before the thermal resistance is calculated.

reads the thermal resistance with a scale factor of 1.0 mV = 1.0°C/watt.

Errors

The main sources of measurement error are:

- Errors due to variations in the temperature coefficient K (estimated to be $\pm 3\%$).
- Errors due to thermal time constants caused by:
  a. Errors in measuring T_j before steady state is reached. These can be reduced by adjusting the variable time delay TD.
  b. Errors due to junction cooling during the measurement interval. These could be as large as -5% for a device with very short constants (100 μs) and close to zero for a device with long time constants.
- Errors due to inaccuracies in the Thermal Resistance Calculator circuits which could be $\pm 2\%$ for temperature rises of at least 60°C at the junction during testing.
- Errors due to T_c (case temperature) drift during the measurement of T_j which could range from 0% to $+3\%$ for a well designed heat sink.

Adding these gives a probable overall accuracy of $+8$, -10%.

Acknowledgments

The authors would like to thank Charles Forge, semiconductor application engineer, for his helpful suggestions and assistance; Marc Nilson, who constructed the first version of the Thermal Resistance Tester and took much of the data, and Dave Jacoby, who constructed the final version of the Thermal Resistance Tester and the Thermal Resistance Calculator. ■

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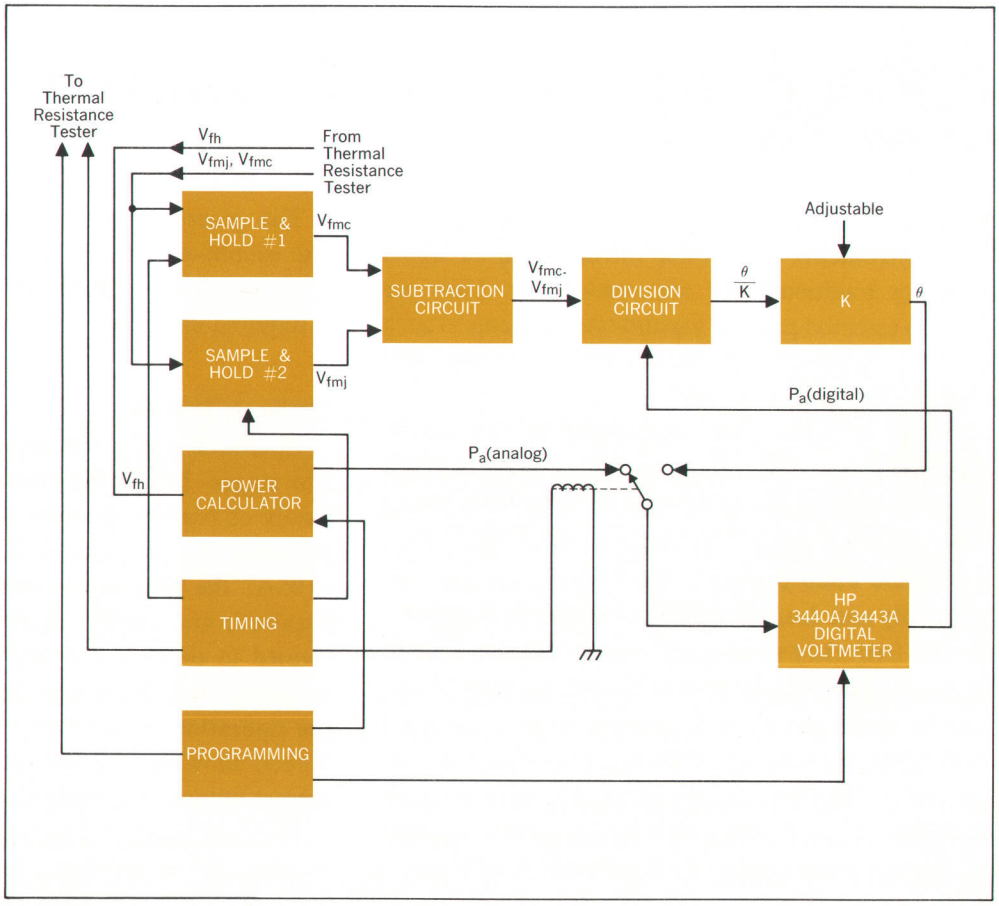


Fig. 9. *Thermal resistance calculator and sequencer programs and times the rest of the system. The relay switches the DVM input between* P_a *and* θ *circuitry.*

Fig. 1. *Pushbutton bank on the HP Model 5105A Frequency Synthesizer permits selection of high-quality signals up to 500 MHz in steps as fine as 0.1 Hz increments.*

Digital Frequency Synthesizer Covering 0.1 MHz

By Alexander Tykulsky

FREQUENCY SYNTHESIZERS have become highly versatile instruments since their introduction as signal sources for traditional HF communications. They are applied as essential parts of sophisticated systems in such areas as spectroscopy, advanced radar, space communication and automated testing.

For some time, there has been a need for high quality synthesized microwave signals capable of being switched rapidly. Suitable synthesizers, until recently have barely reached the VHF range. The use of auxiliary multipliers has been the usual expedient for bridging the gap, but this is costly and does not lead to optimum performance.

A new frequency synthesizer, the HP Model 5105A, (Fig. 1) represents a step toward better frequency coverage of the active spectrum. Frequency range is extended to 500 MHz, an increase of ten times the range of previous HP synthesizers. Design techniques used produce these higher output frequencies with less noise than could be obtained by multiplying up from lower frequencies.

The generation of signals in the microwave range is also simplified, since by starting at the higher output frequencies offered by the Model 5105A, less multiplication is required and phase noise is appreciably less.

Synthesis System

Operation of the synthesis system is accomplished in two stages. In the driver unit (HP Model 5110B), a family of fixed frequencies is derived from a frequency standard. In the variable frequency unit (HP Model 5105A), the fixed inputs from the driver are selected as required, and further arithmetic operations are performed to produce the desired frequency. Fixed filters are used, and frequency changes are effected only by the operation of solid state switches. The method is 'direct,' allowing no possibility of an uncontrolled or incorrect output. A simplified diagram is shown in Fig. 2.

The technique of generating a finely-resolved signal by means of an iterative sequence of mixer-divider units

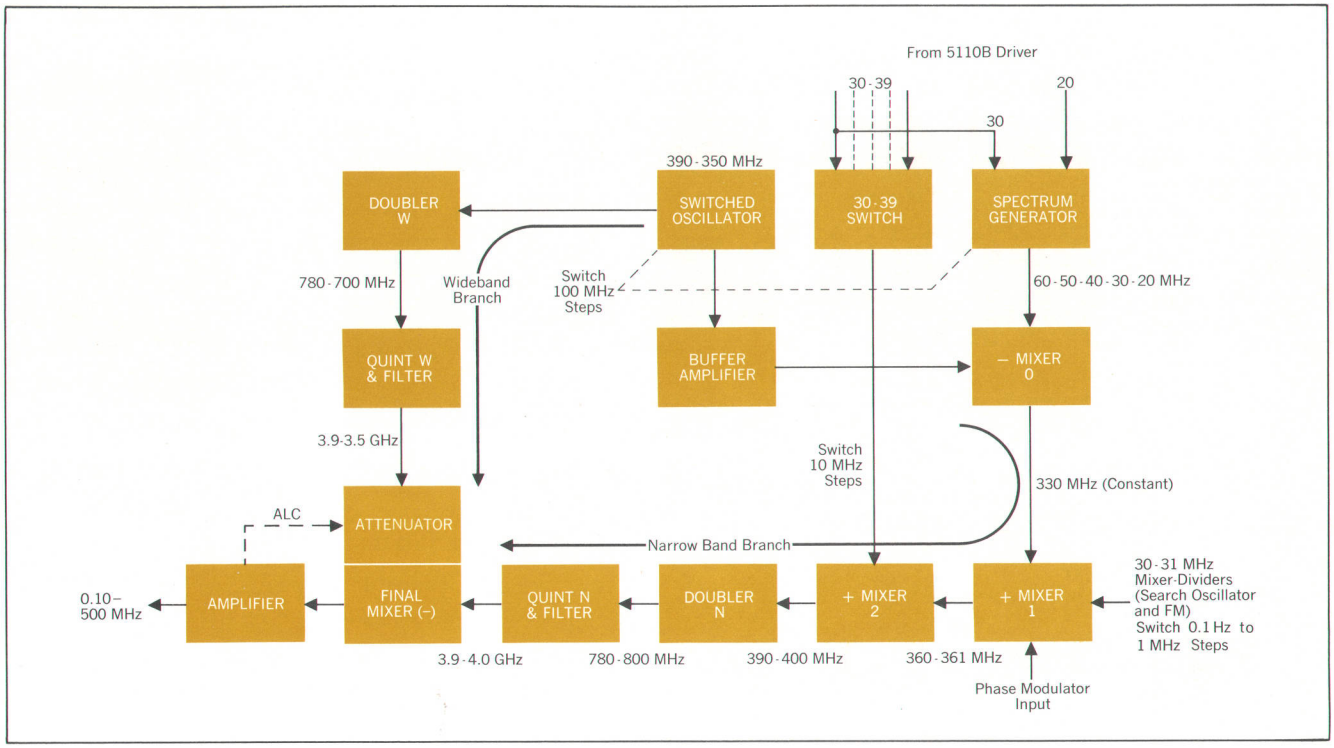


Fig. 2. *Output from the switched oscillator is processed, carried through two branches and difference mixed in the output mixer. Any frequency excursion occurring in the switched oscillator is cancelled out.*

z to 500 MHz in 0.1 Hz Steps

is borrowed from the HP Model 5100A.[1] The signal so generated, covering 30 to 31 MHz in decimal steps from 0.01 Hz to 100 kHz, is added into the N (narrow band) branch of the synthesis system at Mixer 1 and is multiplied by 10 in a doubler and quintupler. As a result the coverage contributed by the mixer-divider units as seen at the output is increased to 10 MHz and the steps range from 0.1 Hz to 1 MHz. A search oscillator is included in the mixer-divider sequence to provide continuous tuning coverage or FM.

A signal in the 30 to 39 MHz range, selectable in 1 MHz steps, is added into the same branch at Mixer 2 and contributes 10 MHz steps at the output. One stripline oscillator of a set of five (covering 390 to 350 MHz in 10 MHz steps) is switched on as required. Simultaneously the spectrum generator is switched to provide a complementary signal so that the difference (330 MHz) required to activate the N branch is always present. The switched oscillator frequency is multiplied by 10 in the doubler and quintupler of the W (wide band) branch, resulting in the 100 MHz step of the synthesizer.

Finally, a difference is taken in the Final Mixer and this difference signal is amplified and leveled.

Drift Cancelling

Non-synthesized signals (not quartz crystal derived) from the switched oscillators can be used because the synthesis system is in a drift cancelling arrangement. Cancellation of frequency errors is accomplished by channeling the frequencies through two paths as shown in Fig. 2. Since any UHF oscillator frequency excursion is carried through both paths, it cancels out in the output mixer. There is a difference in transmission time through the two paths, however, and the correlation is not perfect for rapid variations. The potential problem is avoided by using oscillators which have no appreciable high frequency modulation.

[1] Victor E. Van Duzer, 'A 0-50 Mc Frequency Synthesizer,' **Hewlett-Packard Journal**, Vol. 15, No. 9, May 1964.

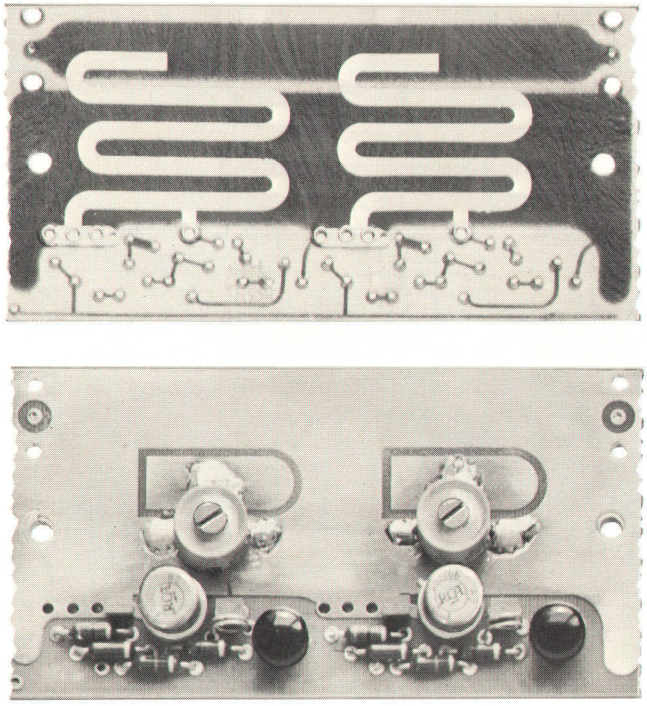


Fig. 3. *Two of the switched oscillators are shown here (the two-layer board is disassembled). They were designed for low noise by placing the active element (a transistor) at a relatively low impedance point on the resonator and designing the resonators as folded transmission lines in a rigid structure to reduce microphonics. In addition, no high impedance point is brought out of the structure and oscillator switching is arranged so that resonator Q is not degraded.*

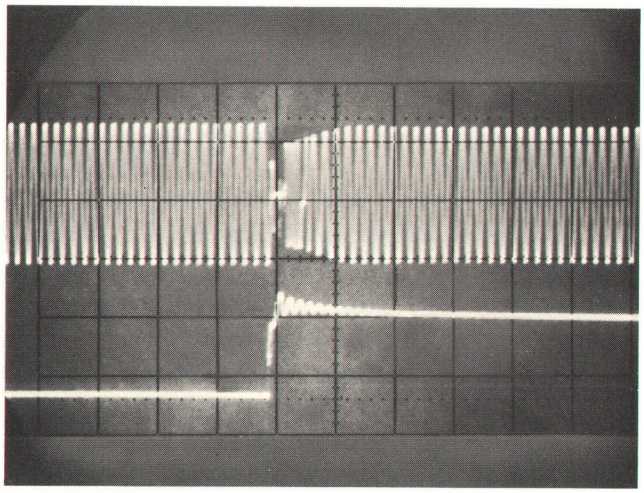


Fig. 4. *Typical performance in switching from 399 to 401 MHz. Lower trace is the switching signal. Sweep speed is 5 μs per division indicating switching speed is less than 20 μs. In photo, the signals are beat with 400 MHz.*

Switched Oscillators

Exploitation of the drift cancelling scheme depends on the availability of easily switched, high quality oscillators (Fig. 3).

Resonators are tapped transmission lines folded within the laminated boards. Tuning is accomplished by isolating portions of one ground plane. Output coupling results from the proximity of the resonators to the 50 Ω output strip line. No high impedance point is brought outside of the ground planes. The resulting compact structure yields the necessary high spectral purity, low microphonic susceptibility, and good long-term stability.

Output Circuit

Output level is detected at an internal point directly on the output transmission line and compared to a reference voltage. Control current is developed through a temperature compensated dc amplifier and applied to the PIN attenuator associated with the final mixer.

This method of leveling, while permitting efficient use of the amplifier output capability, makes the output power dependent upon the VSWR introduced by the combined effect of the load, transmission line, and connectors. At the calibrated output level of 0 dBm and with an ideal load, the flatness of output over the frequency range and for specified environmental conditions is ±1 dBm. Harmonic distortion is typically less than 4%.

External manual control of the leveling reference provides an output capability of approximately −6 to +6 dBm. A metering circuit indicates normal operation of the leveling circuit.

Spurious Outputs

Non-harmonically related spurious signals are more than 70 dB down from the desired signal. Spurious signals close in to the desired signal tend to occur in PM sideband pairs. Those more than a few MHz away tend to be single, additive signals.

Switching Speed

Programmed switching may be obtained by use of the three remote control connectors in the back panel of the variable frequency unit. Switching speed is nominally 20 μs, depending upon the frequencies involved. One example using the switched oscillators and spectrum generator is shown in Fig. 4.

Phase Modulation

Phase modulation is accomplished at Mixer 1 by controlling the tuning of the output circuit. The usable modulation rate extends from 0 to more than 1 MHz, with

the deviation typically down 1 dB at 1 MHz. Variation of deviation with output frequency is less than 2 dB. Harmonic distortion is a function of modulation depth —at 1 radian 5% is typical. Sensitivity is nominally 3 radians per volt.

Phase Noise

Spectral plots of phase noise at 50 and 500 MHz are shown in Fig. 5. Also shown are the results to be obtained by multiplying the HP Model 5100A in noiseless multipliers (× 10). It is clear that while the HP Model 5100A is to be preferred below 50 MHz, the HP Model 5105A is preferable to multiplication (by 10) of the HP Model 5100A. The advantage comes from the smaller magnification of independent noise originating in the filters of the driver unit. This is made possible by the use of the drift canceling scheme.

Solid State Modules

The design is based upon a large variety of solid state circuits, ranging from diode switches to S-band quintuplers. Modular construction is used throughout to achieve the required isolation between circuits, to facilitate extensive production testing, and to simplify servicing.

Acknowledgments

Many people contributed to the development of the HP Model 5105A/5110B, particularly Roland Glaser, Bob Maldewin and Fred Wolcott. ■

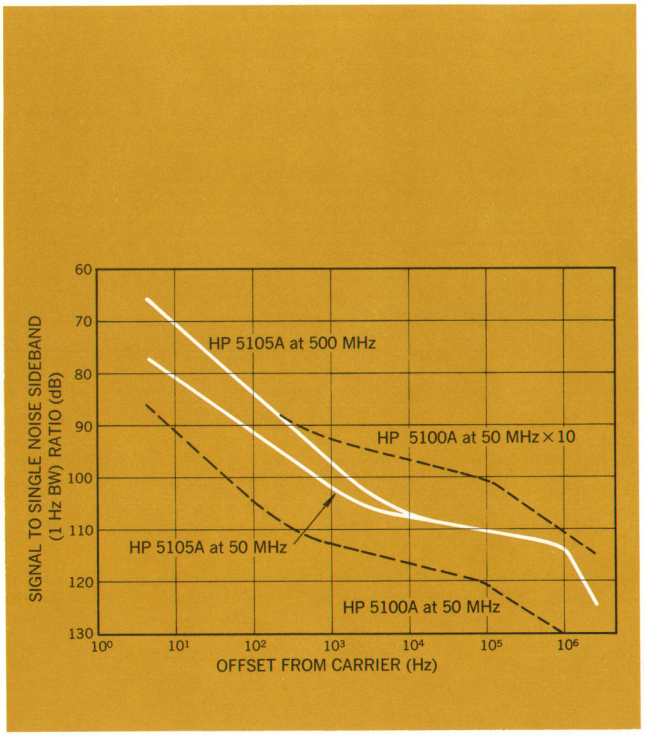


Fig. 5. *Comparison of spectral distribution of phase noise sidebands of the 50 MHz Model 5100A and the 500 MHz Model 5105A. The lower frequency synthesizer provides improved noise performance at the lower frequencies, while at higher frequencies the Model 5105A shows substantially better noise performance than can be obtained by multiplying the lower frequency by ten.*

SPECIFICATIONS

HP Model 5105A Frequency Synthesizer*

OUTPUT FREQUENCY: 0.1 to 500 MHz.

DIGITAL FREQUENCY SELECTION: 0.1 Hz through 100 MHz per step. Selection by front panel pushbutton or by remote switch closure. Any change in frequency may be accomplished in 20 μs typically.

OUTPUT VOLTAGE
FIXED: 0 dBm ±1 dBm into a 50-ohm resistive load.
VARIABLE: −6 dBm to +6 dBm into a 50-ohm resistive load, typical at 20°C.

SEARCH OSCILLATOR/FM: A search oscillator provides continuous variable frequency selection with an incremental range of 1.0 Hz through 10 MHz. Manual, or external voltage (−1 to −11 volts) control with linearity of ±5%. Maximum sine wave rate (external) is 1000 Hz.

PHASE MODULATION: (50Ω rear panel input) ±3 radians maximum deviations; dc — 1 MHz rate. Typical sensitivity: ±3 radians per volt. Linearity depends upon deviation amplitude.

SIGNAL-to-PHASE NOISE RATIO: Measured in a 30 kHz band centered on the signal (excluding a 1 Hz band centered on the signal) is greater than:

Output Frequency—MHz	1	50	100	500
Ratio—dB	48	48	48	40

SIGNAL-to-AM NOISE RATIO: (Above 100 kHz): Greater than 74 dB in a 30 kHz band.

RMS FRACTIONAL FREQUENCY DEVIATION (with a 30 kHz noise bandwidth):**

Averaging Time	Output Frequency			
	1 MHz	50 MHz	100 MHz	500 MHz
10 milliseconds	1×10^{-7}	2×10^{-9}	1×10^{-9}	6×10^{-10}
1 second	2×10^{-9}	4×10^{-11}	2×10^{-11}	1×10^{-11}

SPURIOUS SIGNALS: Non-harmonically related signals are at least 70 dB below the selected frequency.

HARMONIC SIGNALS: 25 dB below the selected frequency (applicable to fixed output when terminated in 50 ohms).

WEIGHT: Net, 75 lbs. (34 kg). Shipping, 133 lbs. (60 kg).

PRICE: $9,150.00

* Requires 5110B Driver.

** Note: When the 5110B Driver utilizes an external frequency standard, this will affect the stability and spectral purity of the output. Performance data stated above are based on internal frequency standard or indicate synthesizer contribution to over-all performance with external standard.

HP Model 5110B Synthesizer Driver

OUTPUT FREQUENCIES: Provides 22 fixed frequencies for the 5105A Frequency Synthesizer: 3.0 through 3.9 MHz in 0.1 MHz steps (50 mV + 1, −3 dB) 30 through 39 MHz in 1MHz steps, 24 MHz, and 20 MHz (100 mV ±1.5 dB), 50-ohm system. 1 MHz buffered output (1 volt ±1.5 dB into a 50-ohm resistive load) available at rear panel connector.

INTERNAL FREQUENCY STANDARD
TYPE: 1 MHz Quartz Oscillator.
AGING RATE: Less than ±3 parts in 10^9 per 24 hours.
STABILITY: As a function of ambient temperature: $\pm 2 \times 10^{-10}$ per °C from 0°C to +55°C.
As a function of line voltage: $\pm 5 \times 10^{-11}$ for a ±10% change in line voltage (rated at 115 or 230 volts rms line voltage).

RMS FRACTIONAL FREQUENCY DEVIATION:

Average Time	1 MHz Output Frequency
10 milliseconds	6×10^{-10}
1 second	1×10^{-11}

SIGNAL-to-PHASE NOISE RATIO:* >85 dB.

SIGNAL-to-AM NOISE RATIO:* >80 dB.

HARMONIC SIGNALS: >40 dB below the output (with proper termination).

* In a 30 kHz band centered on the carrier, excluding a 1 Hz band centered on the carrier.

PHASE-LOCKING CAPABILITY: A voltage control feature allows 5 parts in 10^8 frequency control for −5 to +5 volts applied externally.

EXTERNAL FREQUENCY STANDARD
INPUT REQUIREMENTS: 1 MHz or 5 MHz, 0.2 V rms minimum, 5 V maximum across 500 ohms. Stability and spectral purity of 5105A Frequency Synthesizer will be partially determined by the characteristics of the external standard if used.

GENERAL (Applies to 5105A/5110B)

OPERATING TEMP. RANGE: 0 to +55°C.

WEIGHT: Net, 54 lbs. (24 kg). Shipping, 67 lbs. (30 kg).

POWER: 115 or 230 volts ±10%, 50 to 400 cycles, 35 watts each unit (independent supplies).

PRICE: $4,350.00

MANUFACTURING DIVISION: HP FREQUENCY & TIME
1501 Page Mill Road
Palo Alto, California 94304

Phase Noise in Frequency Synthesizers

A FREQUENCY SYNTHESIZER OPERATES on the signal provided by a frequency standard to produce a desired frequency which reflects the accuracy and stability of the standard. In effect, the frequency of the standard is multiplied by a selectable synthesis factor — a rational number usually based on the decimal system. The ease and speed of selecting the synthesis factor, the resolution and range of available output frequencies, and the spectral purity of the output signal are usually the critical characteristics of the instrument.

Circuits performing the necessary arithmetic operations introduce random amplitude and phase variations. Amplitude modulation tends to be reduced by subsequent non-linear, compressive circuits; phase modulation however, remains, and is usually enhanced. Synthesizer noise, then, is mainly random phase modulation.

The total phase noise of a synthesizer includes the noise originating in the frequency standard. A useful model, Fig. 1(a), shows a simple synthesizer as the combination of an ideal multiplier and a phase noise modulator acting on the output of a frequency standard. This results in a total modulation made up of two parts which can be treated separately: The frequency standard noise multiplied by the selected synthesis factor, and the system noise $\phi_s(t,F)$. The system noise results from the combined effect of the arithmetic circuits (mixers, multipliers, etc.). The importance of a noise source depends on its magnitude and the multiplication which follows.

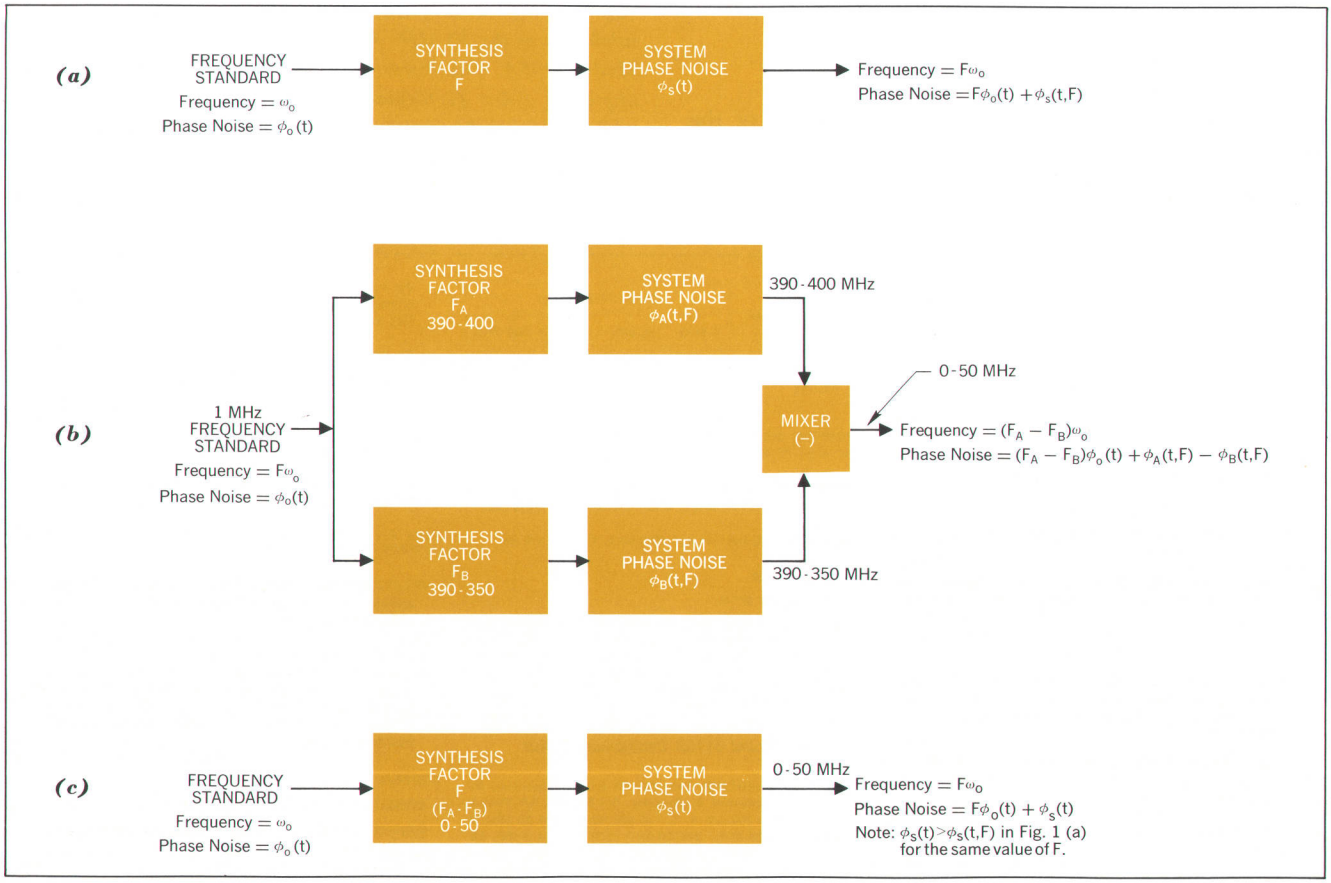


Fig. 1. *Synthesizer noise models. Narrow band system* ***(a)*** *is a basic form of a typical synthesis system. The wideband system* ***(b)*** *is a combination of two narrow-band systems. The wideband system simplified* ***(c)*** *in which* $\phi_S(t) = \phi_A(t,F) - \phi_B(t,F)$ *and is virtually independent of the synthesis factor* F. *The numbers given are examples only.*

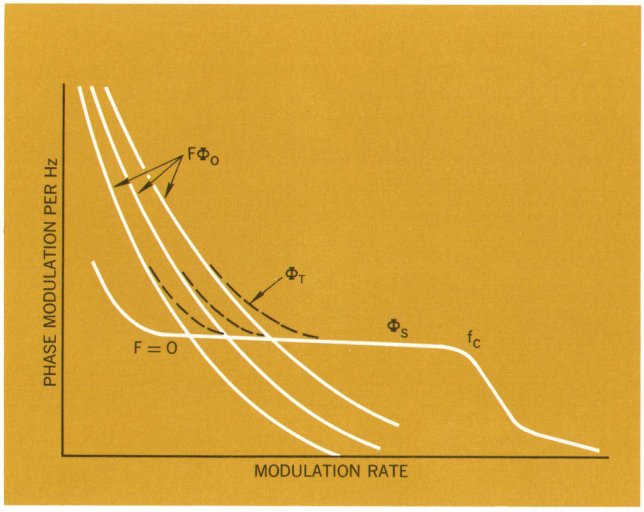


Fig. 2. *Distribution of phase noise components. These curves also illustrate the sideband distribution if the ordinate is considered to be two times the single sideband to carrier ratio, and the abcissa represents offset from carrier.*

Wideband output ranges are most readily obtained by down-converting the outputs of two higher frequency sub-synthesizers* each of which operates over a practical, small percentage bandwidth. The larger synthesis factors of each branch lead to greater system noise than would be expected from a non-heterodyne technique.

An example of a wideband synthesizer is shown in Fig. 1(b). The total phase noise modulation, $\phi_T(t)$, to be expected is

$$(F_A - F_B)\phi_0(t) + F_A\phi_A(t) - F_B\phi_B(t)$$

where the first term is directly related to the frequency standard, and the last two terms constitute systems noise. F_A and F_B are the selected sub-synthesizer factors, and $F_A - F_B$ is the overall synthesis factor. For simplicity, the model of Fig. 1(b) can be represented as shown in Fig. 1(c) and the system phase noise can be written

$$\phi_T(t) = F\phi_0(t) + \phi_S(t)$$

Typical spectral distributions for the model of Fig. 1(c) are shown in Fig. 2, where $\Phi_0(f)$, $\Phi_S(f)$ and $\Phi_T(f)$ are the Fourier transforms of the corresponding time functions.

Noise derived from the frequency standard becomes significant as F is increased, and then predominates at very low modulation rates. The best frequency standard available, consistent with the cost of the synthesizer, clearly should be used. Generally, a crystal filter is employed as part of the standard to improve the spectral purity.

System noise is virtually independent of F and is the major contributor at rapid modulation rates. Location of the corner, fc, (Fig. 2) is dependent upon the narrowest filter bandwidth in the system. In systems where very fast switching is not required, the corner fc may be moved in by the use of a phase lock loop as a narrow band filter, but at the cost of some increase of close-in noise.

The proper design of mixing circuits is a critical problem. Low signal levels lead to poor signal-to-noise ratios and phase noise. High signal levels may introduce spurious modulation at discrete frequencies — an equally undesirable result. Mixers applied at the end of a synthesis sequence introduce less noise since no multiplication follows.

Drift cancelling offers another opportunity to reduce system noise. The high sub-synthesizer frequencies are obtained by adding coherent signals into each branch. The non-coherent noise is reduced (since its synthesis factor is smaller) while the coherent noise is canceled in the output.

The sub-synthesizer factors for Fig. 3 are about one-sixth of those shown in Fig. 1. The system noise will also be about one-sixth — if the noise associated with the oscillator cancels. A differential group delay through the filters in paths A or B makes the cancellation imperfect. The net effect of the oscillator phase noise can be seen at final mixer. Arriving through path A the phase is $\phi_D(t + \tau)$, where ϕ_D is oscillator noise, t is time and τ is group delay due to the filters. Through path B the phase is $\phi_D(t)$. The mixer output shows the phase difference:

$$\phi_D(t + \tau) - \phi_D(t)$$

This equals $\tau\dot{\phi}_D(t)$ if τ is sufficiently small. Writing $\Phi_D(f)$ as the Fourier transform of $\phi_D(t)$, $j2\pi f\Phi(f)$ is the spectrum of $\dot{\phi}_D(t)$, and $j2\pi f\tau\Phi_D(f)$ is seen at the mixer output.

It can be seen that if the synthesizer system noise is to be minimized $\Phi_D(f)$ must be small, particularly for large values of f.

This reasoning also explains the need for a sharp filter in the frequency standard output. In Fig. 1(b), assume a probable differential delay, τ, between sub-synthesizers A and B. Then an additional noise modulation $\tau F_B\dot{\phi}_0(t)$ appears in the output and this leads to the additional spectral component $j\tau F_B 2\pi f\Phi_0(f)$. For sufficiently large

* Sub-synthesizers in this context are the synthesis systems, separate but related, contained within a frequency synthesizer.

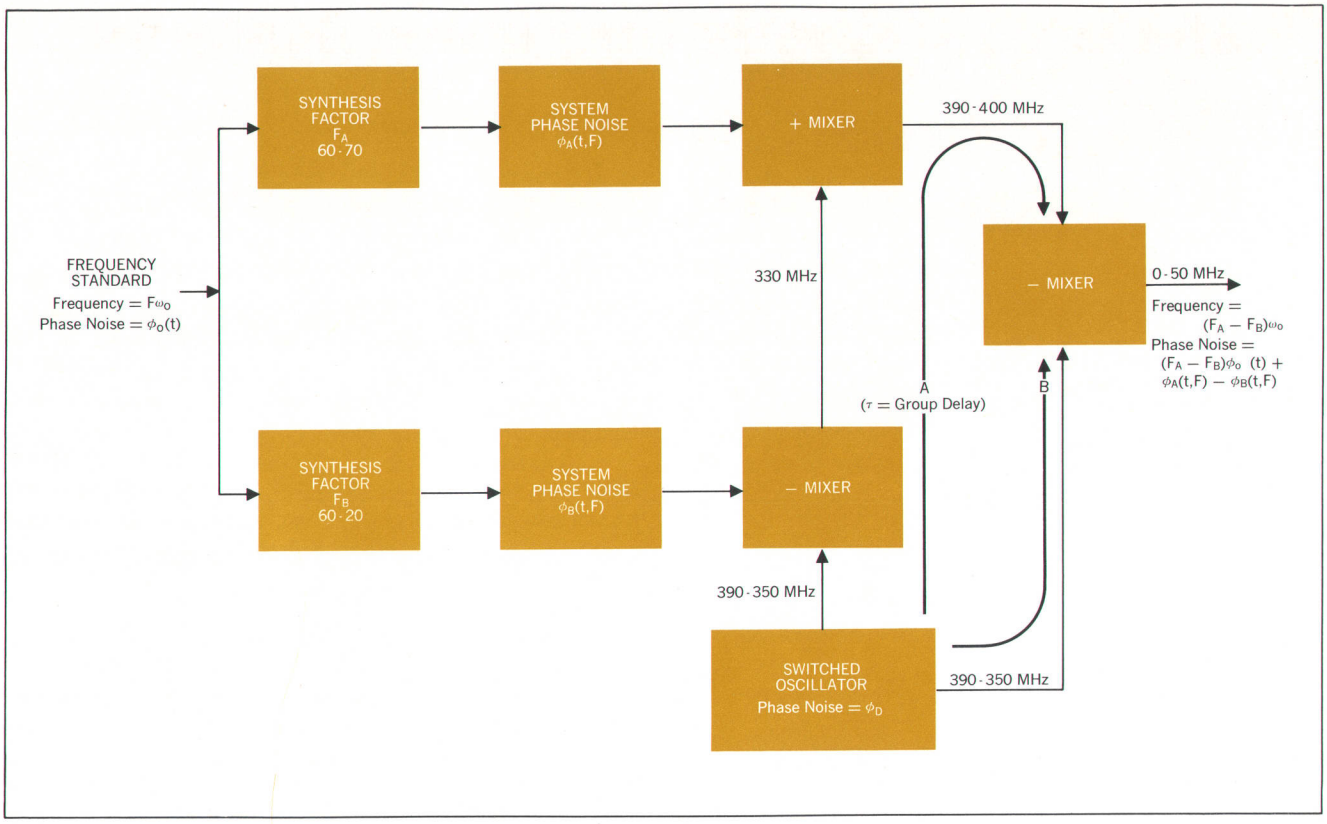


Fig. 3. *Noise model for a wideband synthesizer employing drift cancelling. System noise is less than in Fig. 1(b) since* F_A *and* F_B *are smaller leading to smaller values of* ϕ_A *and* ϕ_B. *The numbers given are examples only.*

values of *f*, this component becomes overriding and must be reduced by filtering.

Many different synthesis schemes can be devised to obtain a given set of numerical results, but the performance of each is unique. Choice of a suitable design is a compromise involving consideration of discrete spurious outputs, switching speed, size, cost and other characteristics in addition to phase noise. ■

Al Tykulsky, left, earned his Bachelor of Science in Electrical Engineering from CCNY and his MSEE from Rutgers University. Previous to joining Hewlett-Packard in 1962 he worked in the television and communications fields on the design of synthesizers and related test equipment. He holds patents relating to single-sideband generation, duplex communications, a pattern generator and a sweep oscillator.

Al designed the UHF section of the Model 5100A Frequency Synthesizer and was responsible for the design of the new Model 5105A. He has developed techniques for phase noise measurements of synthesizers and other sources used in laboratory and production testing.

Bob Maldewin, right, joined Hewlett-Packard in 1960 and participated in the development of the HP Model 5100A Frequency Synthesizer. Among other contributions, he is responsible for design details and fabrication processes of the Model 5105A stripline oscillators, the stripline output mixer and the PIN attenuator.

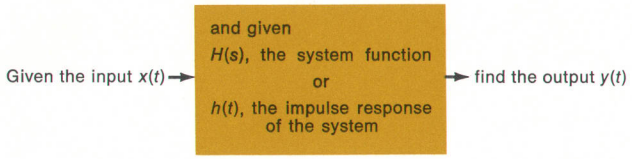
Transform Methods for Linear Systems

By Michael O'Flynn

Professor of Electrical Engineering, San Jose State College

This is a highly condensed collection of reference material on transform methods. Formulas for direct and inverse Fourier, Laplace, and Z-transforms are given in compact tabular form, with examples of how they are used to find system responses for several types of inputs.

Transforms are powerful tools for solving linear time-invariant system problems, such as



Depending upon the system and the excitation, the most convenient transforms to use might be Fourier transforms, one- or two-sided Laplace transforms, or one- or two-sided Z-transforms. These transforms are treated in many textbooks (such as references 1 and 3 in Bibliography), and no attempt has been made to give an exhaustive treatment here. To the author's knowledge, however, there is nothing in the literature equivalent to Table I, which is a comprehensive collection of the defining formulas for all of these transforms and their inverses. The arrangement and notation of this table are designed to demonstrate the similarities and interrelationships between the different transforms. A feature of the treatment of inverses is a logical progression from the fundamental inverse formulas to their equivalents in terms of complex variables (contour integrals, residues, Laurent series).

Table II applies transform methods to the problem of finding the output of a linear system for five types of input signals. In each case the transform used is the most appropriate one for the type of input.

These tables can be used as a reference by anyone working in the field of linear systems or — along with a textbook — by students of linear system theory. As an aid to the student, Table III lists the impedances of the basic network elements R, L, and C for the five classes of inputs.

Classes of Inputs

In the tables and discussion that follow, five classes of inputs are considered. They are:

i) A damped sinusoidal input $x(t) = Ae^{-\sigma_0 t}\cos(\omega_0 t + \phi_0)$

ii) A periodic input $x(t) = \sum_{n=0}^{\infty} A_n \cos(n\omega_0 t + \phi_n)$

iii) An aperiodic input which has a Fourier or a Laplace transform.

iv) A sampled input $x^*(t)$ known only at specified points.

v) A random input, where $x(t)$ is a member of an ergodic random process for which the autocorrelation function $R_x(\tau)$ and its Fourier transform $S_x(j\omega)$ are known.

As an example of the use of the transforms, the aperiodic case (iii) will be discussed in detail. The sampled case (iv) is similar to the aperiodic case except that Z-transforms are used instead of Laplace transforms. The first two cases, i.e., periodic and damped sinusoidal inputs, are well known.

For random inputs (case v) the problem can be restated as follows: Given the input autocorrelation function $R_x(\tau)$ and the system function, find the output autocorrelation function $R_y(\tau)$. With this modification, the problem is similar to the aperiodic case.

Inverses by Complex Variable Methods

The problem of finding the output of a linear system whose input and system function are known may be regarded as an exercise in finding inverse transforms. Inverses can be found either by looking them up in a table of transforms, or directly, by computing them using the inverse formulas given in Table I. The direct approach requires a knowledge of complex variables and contour integration, but it gives more insight into the physical meaning of the solutions.* For example, the inverse expressions contain full information about the natural frequencies of the system.

Linear System Output for Aperiodic Input

The output of a linear system for an aperiodic input $x(t)$ is

$$y(t) = \frac{1}{2\pi j}\int_{\sigma-j\infty}^{\sigma+j\infty} H(s)X(s)e^{st}ds.$$

Here the Laplace transform has been used. $H(s)$ is the system function and $X(s)$ is the transform of the input $x(t)$.

If the one-sided Laplace transform is used, and if Jordan's Lemma is satisfied (usually this means simply that $H(s)X(s)\to 0$ as $s\to\infty$) then

$y(t) = 0, t < 0$

$y(t) =$ sum of the residues of the poles of $H(s)X(s)e^{st}$, $t > 0$.

The complete response $y(t)$ consists of two parts. One is the *forced response* $y_f(t)$, in which only the input frequencies appear. [The input $x(t)$ is often called the *forcing function.*] The other part of $y(t)$ is the *transient response* $y_{tr}(t)$.

* If a transform has an infinite number of poles (e.g., a discontinuous function, such as ⊓⊓) it may be difficult or impossible to apply the complex-variable formulas. In such cases, time-domain analysis may be simpler than transform methods.

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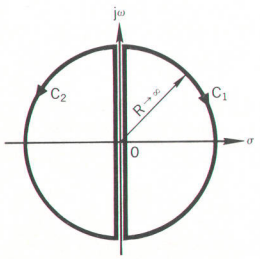
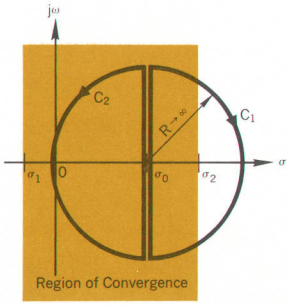
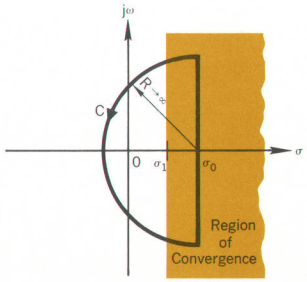
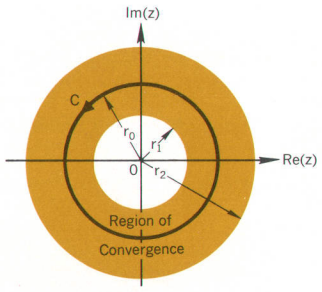
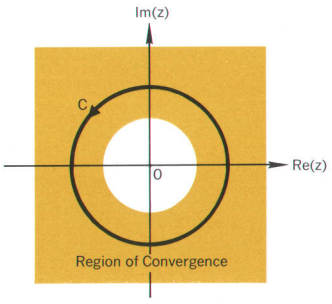
Table I Definitions of Different Transforms with their Inverses

Fourier Transform	Laplace Transform (Two-sided)	Laplace Transform (One-sided)	Z-Transform (Two-sided)
$F(j\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt$	$F(s) = \int_{-\infty}^{\infty} f(t)e^{-st}dt$	$F(s) = \int_{0}^{\infty} f(t)e^{-st}dt$	$f^*(t) = \sum_{n=-\infty}^{\infty} f(n)\delta(t - nT)$
$F(j\omega)$ is defined for ω real and exists if	$s = \sigma + j\omega$	$s = \sigma + j\omega$	$F(z) = \sum_{n=-\infty}^{\infty} f(n)z^{-n}$
$\int_{-\infty}^{\infty} \lvert f(t) \rvert dt$ exists	$F(s)$ exists if	$F(s)$ exists if	or
	$\int_{-\infty}^{\infty} \lvert f(t)e^{-st} \rvert dt$ exists	$\int_{0}^{\infty} \lvert f(t)e^{-st} \rvert dt$ exists	$F(z) = F^*(s)\big\rvert_{z = e^{sT}}$
	This integral exists in some allowable region of convergence $\sigma_1 < \sigma < \sigma_2$	This integral exists in some allowable region of convergence $\sigma > \sigma_1$	This exists in an allowable annulus of convergence $r_1 < \lvert z \rvert < r_2$
$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(j\omega)e^{j\omega t}d\omega$	$f(t) = \frac{1}{2\pi j}\int_{\sigma_0 - j\infty}^{\sigma_0 + j\infty} F(s)e^{st}ds$	$f(t) = \frac{1}{2\pi j}\int_{\sigma_0 - j\infty}^{\sigma_0 + j\infty} F(s)e^{st}ds$	$f(n) = \frac{1}{2\pi j}\oint_C F(z)z^{n-1}dz$
which may be evaluated directly or from tables	$\sigma_1 < \sigma_0 < \sigma_2$	$\sigma_0 > \sigma_1$	where C is a circle of radius r_0 such that $r_1 < r_0 < r_2$.
or	For $t < 0$	For $t > 0$	For $n \geqq 0$
$f(t) = \frac{1}{2\pi j}\int_{-j\infty}^{j\infty} F(j\omega)e^{j\omega t}d(j\omega)$	$f(t) = \frac{1}{2\pi j}\oint_{C_1} F(s)e^{st}ds$	$f(t) = \frac{1}{2\pi j}\oint_{C} F(s)e^{st}ds$	$f(n)$ = sum of residues of $F(z)z^{n-1}$ inside C.
$= \frac{1}{2\pi j}\int_{-j\infty}^{j\infty} F(s)e^{st}ds\Big\rvert s = j\omega$	$= -\left(\begin{matrix}\text{Sum of residues of}\\ \text{poles with real parts}\\ \text{to right of } \sigma_0.\end{matrix}\right)$	= Sum of residues of poles of $F(s)$.[C encloses all poles of $F(s)$.]	For $n < 0$
For $t < 0$	For $t > 0$,	Note: As a consequence of the definition of the one-sided transform an acceptable σ_0 is automatically to the right of the poles of $F(s)$.	$f(n)$ = sum of residues of $F(z)z^{n-1}$ outside C.
$f(t) = \frac{1}{2\pi j}\oint_{C_1} F(s)e^{st}ds$	$f(t) = \frac{1}{2\pi j}\oint_{C_2} F(s)e^{st}ds$		Note: the formula for $f(n)$ is the formula for the coefficients of the Laurent series for $F(z)$ (see Appendix).
$= -\left(\begin{matrix}\text{Sum of residues of}\\ \text{poles in right half}\\ \text{plane.}\end{matrix}\right)$	= Sum of residues of poles with real parts to left of σ_0.		
For $t > 0$	Note: Residues are defined for counterclockwise contours. Contour C_1 is clockwise. The integral around C_1 is, therefore, *minus* the sum of the residues of the enclosed poles.		
$f(t) = \frac{1}{2\pi j}\oint_{C_2} F(s)e^{st}ds$			
= Sum of residues of poles in left half plane.			
			

	Z-Transform (One-sided)
	$f^*(t) = \sum_{n=0}^{\infty} f(n)\delta(t - nT)$ $F(z) = \sum_{n=0}^{\infty} f(n)z^{-n}$ or $F(z) = F^*(s)\big\|_{z = e^{sT}}$ This exists in an allowable region of convergence outside a circle centered at the origin.
	$f(n) = \frac{1}{2\pi j}\oint_C F(z)z^{n-1}dz$ where C encloses all the poles of $F(z)z^{n-1}$ $f(n) =$ sum of the residues of $F(z)z^{n-1}$ Note: the formula for $f(n)$ is the formula for the coefficients of the Laurent series for $F(z)$ (see Appendix).



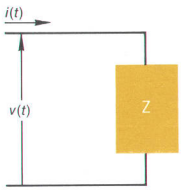


Table III
Impedance Table

Type of Input $i(t)$	Transformed Input	Impedance of Network Element: $Z(s) = \frac{V(s)}{I(s)}$		
		R	L	C
i) Damped Sinusoidal $A\,e^{-\sigma_0 t}\cos(\omega_0 t + \phi_0)$	$A\,e^{j\phi_0}$	R	$Ls\big\|_{s=-\sigma_0+j\omega_0}$	$\frac{1}{Cs}\big\|_{s=-\sigma_0+j\omega_0}$
Special Cases a) Sinusoidal, $\sigma_0 = 0$	$A\,e^{j\phi_0}$	R	$Ls\big\|_{s=j\omega_0}$	$\frac{1}{Cs}\big\|_{s=j\omega_0}$
b) Exponential, $\omega_0 = 0,\ \phi_0 = 0$	A	R	$Ls\big\|_{s=-\sigma_0}$	$\frac{1}{Cs}\big\|_{s=-\sigma_0}$
c) dc case, $\sigma_0 = 0,\ \omega_0 = 0,\ \phi_0 = 0$	A	R	$Ls\big\|_{s=0}$ short circuit	$\frac{1}{Cs}\big\|_{s=0}$ open circuit
	phasor notation			
ii) Periodic $\sum_{n=0}^{\infty} A_n\cos(n\omega_0 t + \phi_n)$	Same as case i) using superposition. Each harmonic has an impedance associated with it as in (i) (a).			
iii) Aperiodic $i(t)$	Fourier Transform $I(j\omega) = \int_{-\infty}^{\infty} i(t)\,e^{-j\omega t}dt$ if integral exists	R	$Ls\big\|_{s=j\omega}$	$\frac{1}{Cs}\big\|_{s=j\omega}$
	Laplace Transform $I(s) = \int_{-\infty}^{\infty} i(t)e^{-st}dt$	R	Ls	$\frac{1}{Cs}$
iv) Sampled $i^*(n)$	System functions for sampled data systems are usually computed first as ratios of Laplace transforms and then converted to Z-transforms.			
v) Random $i(t)$ Autocorrelation Function $= R_i(\tau)$	Power Spectral Density $S_i(j\omega) = \int_{-\infty}^{\infty} R_i(\tau)e^{-j\omega\tau}d\tau$	$\sqrt{R^2}$	$\sqrt{\lvert L^2s^2\rvert}\big\|_{s=j\omega}$	$\sqrt{\left\lvert\frac{1}{C^2s^2}\right\rvert}\big\|_{s=j\omega}$
		Note: $S_v(j\omega) = \lvert Z(j\omega)\rvert^2 S_i(j\omega)$		

Only the poles of $X(s)$ contribute to the forced response. The poles of $H(s)$ give the natural frequencies of the system and contribute to the transient response. If we denote the poles of $X(s)$ as $s_1, s_2, \ldots, s_n$ and the poles of $H(s)$ as $S_1, S_2, \ldots, S_m$, and assume zero initial conditions, the response $y(t)$ is

$$y(t) = y_f(t) + y_{tr}(t)$$

$$= \sum_{i=1}^{n} r_i + \sum_{i=1}^{m} R_i$$

where r_i denotes the residue of pole s_i in $H(s)X(s)e^{st}$ and

R_i denotes the residue of pole S_i in $H(s)X(s)e^{st}$.

If the poles of $H(s)$ and $X(s)$ are all *simple* and *distinct*, and if the poles of $H(s)$ do not cancel the zeros of $X(s)$ or vice versa, then all residues will be of the form

$$r_i = \hat{r}_i e^{s_i t} \text{ and } R_i = \hat{R}_i e^{S_i t}$$

See the Appendix or reference 2 for methods of computing residues.

If the initial conditions are not zero the complete response can be obtained to within m arbitrary constants. Again assuming simple, distinct poles and no pole-zero cancellation, $y(t)$ will be

$$y(t) = \sum_{i=1}^{n} r_i + \sum_{i=1}^{m} A_i e^{S_i t}.$$

The constants A_i are determined from the initial conditions, which are usually given as values of $y(t)$ and its derivatives at $t = 0$.

For many forcing functions and for most systems, the forced response $y_f(t)$ is the steady-state response. Examples of aperiodic inputs for which this is true are step functions, ramp functions, and suddenly applied periodic functions.

However, if the time constants of the natural frequencies — poles of $H(s)$ — are greater than the time constants of the input frequencies — poles of $X(s)$ — then the forced response will decay to zero faster than the transient response. In some systems, such as those made up of only L and C, and no R, the transient response will not die out at all. The transient response, therefore, may actually be the total steady-state response. ■

Table II Input-Output Relationships for a Linear System. *System Function* $= H(s)$

Type of Input	Transform of Input	Transform of Output	Output
Damped Sinusoidal $x(t) = A\,e^{-\sigma_0 t}\cos(\omega_0 t + \phi_0)$	$X(s) = j\pi A\,[e^{j\phi_0}\delta(s - s_0) + e^{-j\phi_0}\,\delta(s - s_0{}^*)]$ $s_0 = -\sigma_0 + j\omega_0$	$Y(s) = H(s)X(s)$	$y(t) = \frac{A}{2}[H(s_0)e^{j\phi_0}e^{s_0 t} + H(s_0{}^*)e^{-j\phi_0}e^{s_0{}^* t}]$ $= Re[H(s_0)\,A\,e^{j\phi_0}e^{s_0 t}]$
In phasor notation:	$X_T = A\,e^{j\phi_0}$ It is understood that this means $x(t) = Re[A\,e^{j\phi_0}e^{s_0 t}]$	$Y_T = H(s_0)X_T$	$y(t) = Re[H(s_0)X_T e^{s_0 t}]$
Periodic $x(t) = \sum_{n=0}^{\infty} A_n \cos(n\omega_0 t + \phi_n)$	Transform of the nth harmonic $X_n(j\omega) = \pi A_n[e^{j\phi_n}\delta(\omega - n\omega_0) + e^{-j\phi_n}\delta(\omega + n\omega_0)]$	By superposition $Y(j\omega) = \sum_{n=0}^{\infty} H(j\omega)\,X_n(j\omega)$	$y(t) = \sum_{n=0}^{\infty} Re[H(jn\omega_0)\,A_n e^{j\phi_n}e^{jn\omega_0 t}]$
In phasor notation:	$X_n = A_n e^{j\phi_n}$	$Y_n = H(jn\omega_0)X_n$	$y(t) = \sum_{n=0}^{\infty} Re[H(jn\omega_0)\,X_n e^{jn\omega_0 t}]$
Aperiodic $x(t)$	$X(j\omega) = \int_{-\infty}^{\infty} x(t)e^{-j\omega t}dt$ if integral exists, or $X(s) = \int_{-\infty}^{\infty} x(t)e^{-st}dt$	$Y(j\omega) = H(j\omega)X(j\omega)$ or $Y(s) = H(s)X(s)$	$y(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty}[H(j\omega)\,X(j\omega)]e^{j\omega t}d\omega$ or $y(t) = \frac{1}{2\pi j}\int_{\sigma-j\infty}^{\sigma+j\infty}[H(s)X(s)]e^{st}ds$
Sampled $x^*(t) = \sum_{n=-\infty}^{\infty} x(n)\delta(t - nT)$	$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$	$Y(z) = H(z)X(z)$ where $H(z) = \sum_{n=-\infty}^{\infty} h(n)z^{-n}$ where $h(n)$ = unit pulse response	$y(n) = \frac{1}{2\pi j}\oint_C H(z)X(z)z^{n-1}dz$
Random $R_x(\tau)$ = Input Autocorrelation Function	Input Power Spectral Density $S_x(j\omega) = \int_{-\infty}^{\infty} R_x(\tau)e^{-j\omega\tau}d\tau$	$S_y(j\omega) = \lvert H(j\omega)\rvert^2 S_x(j\omega)$	Output Autocorrelation Function $R_y(\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty}[\lvert H(j\omega)\rvert^2 S_x(j\omega)]\,e^{j\omega\tau}d\omega$

Appendix. Complex-Variable Formulas

1. $\oint_C f(z)dz = 0$ if $f(z)$ is analytic on and inside the closed contour C.

2. $\oint_C g(z)dz = 2\pi j \sum$ [residues of poles of $g(z)$ inside C].

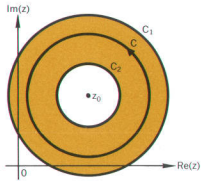
   If $g(z)$ has an nth-order pole at z_0 then

   residue of $z_0 = \frac{1}{(n-1)!}\left[\frac{d^{n-1}}{dz^{n-1}}\left\{(z - z_0)^n g(z)\right\}\right]_{z = z_0}$

3. If $f(z)$ is analytic on C_1 and C_2 and in the region between them, then $f(z)$ can be represented in that region by a Laurent Series.

$$f(z) = \sum_{n=-\infty}^{\infty} A_n(z - z_0)^n$$

where $A_n = \frac{1}{2\pi j}\oint_C \frac{f(z)}{(z - z_0)^{n+1}}\,dz.$



C is any curve between C_1 and C_2 and enclosing z_0.

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