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Load Lines In Transistor Amplifier Design

By the Engineering Department, Aerovox Corporation

GRAPHICAL constructions are of considerable aid in designing electron tube circuits. Load lines drawn across the plate current-vs-plate voltage family of curves yield circuit constants and important operating data. This relatively simple procedure eliminates many tedious calculations.

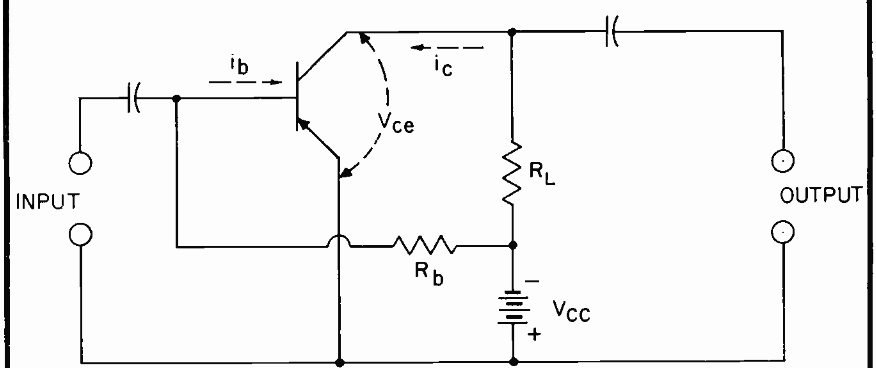
Graphical constructions are equally useful in the design of transistor amplifier circuits. Similar advantages are obtained. In transistor work, load lines are constructed on the collector $v_c i_c$ family of curves to determine operating point, load resistance, distortion, collector current swing, and base current values. The technique is similar in every respect to that employed in tube work.

This article will show, by illustrative examples, how to use the load line technique in transistor amplifier design.

DETAILED PROCEDURE

Figure 1 shows the circuit of a typical common-emitter, RC-coupled transistor amplifier stage. The common-emitter, also sometimes called the *grounded-emitter*, is widely used because it affords high power gain, high voltage gain, 180-degree phase reversal similar to a tube, and good frequency response.

When the constants of this circuit, especially the load resistance (R_L), collector supply voltage (v_{cc}), and collector-to-emitter voltage (v_{ce}) are chosen in such a way that the internal parameters of the transistor determine largely the operating point of the amplifier, inefficient operation, high distortion, or poor instability usually result. By proper choice of the operating point with respect to the transistor characteristics and supply voltage, low-distortion class-A performance easily is obtained safely within the transistor maximum ratings.



COMMON-EMITTER AMPLIFIER WITH SERIES BASE RESISTOR

FIGURE 1

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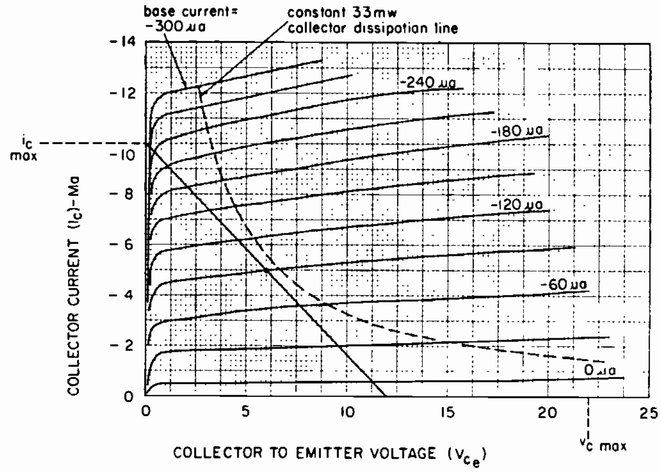
For graphical construction, the first requirement is to obtain a set of collector EI curves, such as those in Figure 2, for the transistor chosen. For common-emitter operation, the family contains a separate curve for each of several typical base-current values and is a plot of collector-to-emitter voltage, v_{ce}, versus collector current, i_c. If such a set of curves is not available in the transistor manufacturer's literature, the operator must plot a set by making a series of common-emitter d-c measurements on the particular type of transistor which is to be used in the amplifier. The procedure is to set the base bias current at a given level (zero base current is one such level) and to vary the collector current (supplied by a constant-current supply) while observing the corresponding voltage between collector and emitter.

In the graphical construction, follow this procedure: (1) Label the points of maximum collector current and maximum collector voltage on the graph. Figure 2 is a family of curves for the Raytheon CK721 transistor. The maximum collector current, from the manufacturer's data sheet, therefore is —10 ma, as labelled in Figure 2, and the maximum collector voltage is —22 volts. (2) Draw across the curves a plot showing the current and voltage intersects for the maximum dissipation (P_c), in watts recommended by the manufacturer. In the case of the CK721, $P_c = 33$ milliwatts and is represented by the dashed line which bends across the collector family in Figure 2. At any point of intersection of this line with abscissae and ordinates, the product $v_c i_c = 0.033$. In determining the points for the dissipation curve, voltages may be selected along the horizontal axis and corresponding current values calculated ($i_c = P_c/v_c$), or current points may be selected along the vertical axis and corresponding voltage values calculated ($v_c = P_c/i_c$). The area of the graph below and to the left of this curve encloses all points which are within the dissipation rating of the transistor. All points in the area above and to the right of this curve represent overload and must be avoided. (3) Select the operating point of the transistor (that is, collector voltage and collector current) and the supply voltage. (4) Mark the operating point on the graph. Example, see the dot at the intersection of the 6-volt and 5-milliampere lines in Figure 2. (5) Construct a load line from the supply voltage point on the horizontal axis,



COMMON-EMITTER COLLECTOR FAMILY WITH LOAD LINE CONSTRUCTION (RAYTHEON CK721 TRANSISTOR).

FIGURE 2

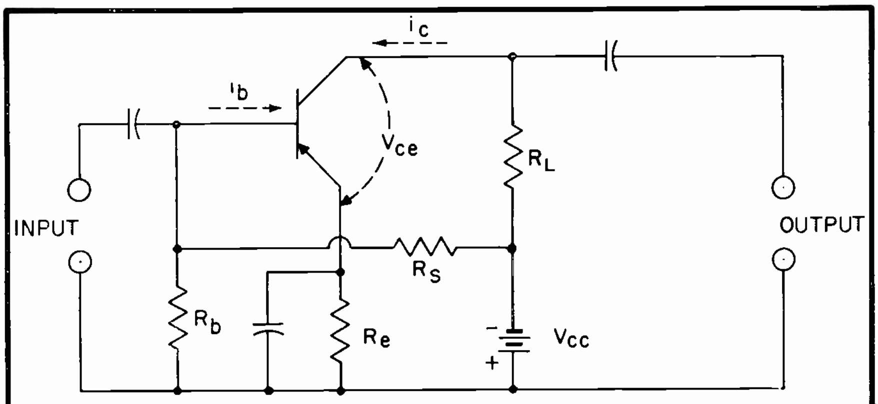
through the operating point, to the vertical axis. This is the solid line in Figure 2. (6) Determine the required load impedance, R_L, by computing the slope of the load line. ($R_L = dv_c/di_c$).

Several facts are evident from an examination of Figure 2, a typical example of transistor load line application. (a) The operating point has been selected at $v_{ce} = 6$ v, $i_c = 5$ ma. (b) With a supply voltage of —12 v, the load line extends from —12 to —10. ma. The load resistance accordingly is dv_c/di_c = (0—12))/(0—0.01) = 1200 ohms. (c) The entire load line is seen to be within the dissipation rating of the CK721, being 3 milliwatts lower than the constant dissipation curve at the point of closest proximity. (d) The base current level which will bias the transistor for the 5 ma. collector current at the operating point is seen to be 90 microamperes.

In the preceding example, the supply voltage was assumed fixed. The operating point was chosen, and the required load resistance determined from the slope of the load line. It is easily seen that different procedures might stem from other combinations of known and unknown factors. For example, the operating point and load resistance might be given and the required supply voltage left to be determined, or the load resistance and supply voltage might be specified and the operating point placed at any satisfactory position along the resulting load line.

It is desirable that the collector signal-voltage swing encompass as much of the collector characteristic as is feasible. This will insure maximum output voltage. Thus, with the operating point set at 6 v, 5 ma in Figure 2, the collector signal voltage may swing down the load line to the 0 μa base-current curve and up the load line to the 210 μa base-current curve without encountering the severe bending at the left ends of these curves. However, it is obvious that the upper swing traverses a larger number of base-current curves that the lower swing, because of the progressively closer spacing of the curves at the higher base current levels. The assymetry of signal waveform due to this condition may be minimized by limiting the swing to the region of more nearly equal base-current curve spacing, when low distortion is a more important objective than maximum output.

The collector current at the operating point is a function of the base bias current, i_b. Reference to Figure 2 shows that i_b must be 90 microamperes when $R_L = 1250$ ohms and $v_{cc} = 12$ volts. This base bias current may be obtained from a separate battery or from v_{cc} through a series dropping resistor, R_b in Figure 1. Base bias also may be obtained from a voltage divider (R_s/R_b), operated from v_{cc}, and an emitter series resistor, R_e, as in Figure 3. The required value of series resistor, R_b, in Figure 1, may be determined from the simple relationship $R_b = v_{cc}/i_b$, where R_b is in ohms, v_{cc} in volts, and i_b in amperes. For the 90-microampere base current indicated in Figure 2, $R_b = 12/(9 \times 10^{-5}) =$



COMMON-EMITTER AMPLIFIER WITH BASE-BIAS STABILIZATION NETWORK

FIGURE 3

133,500 ohms. In this calculation, the internal base-to-emitter resistance r_{be}) of the transistor is ignored, since its magnitude is very small with respect to R_b.

There is some objection to using series-resistor base bias in the common-emitter circuit in the way shown in Figure 1, because the high external resistance, R_b, in the base circuit tends to free the transistor for rather wide shifts of the operating point resulting from the effects of temperature on the internal parameters of the transistor. The base biasing scheme illustrated in Figure 3 overcomes this difficulty, stabilizing the operating point against temperature changes as well as against variations between individual transistors. In this arrangement, the supply voltage, v_{cc}, is reduced by the divider network, R_sR_b, and this lower potential is presented to the base of the transistor. Resistor R_e in series with the emitter then limits the base current to the desired bias value. R_e is bypassed heavily to minimize the effects of degeneration. Current through the R_sR_b leg is chosen high enough that resistances R_s and R_b may be made small with respect to the internal resistances of the transistor. This circuit satisfies the condition for stability that any external resistance in the base lead must be small and any external resistance in the emitter lead be made as high as possible.

MAXIMUM POWER OUTPUT

For maximum power output, a condition extremely important in the operation of conventional transistors since their power output capabilities normally are low compared to tubes, the load line should enclose as large an area as possible within the maximum current, voltage, and power dissipation ratings of the transistor.

Figure 4 illustrates the condition for maximum power output, although not necessarily at low distortion. The known supply voltage value, v_{c1}, as located along the horizontal axis. A load line then is drawn from v_{c1} to the vertical axis so as to be tangent to the constant collector dissipation curve at a single point, P. The load line intersects the current axis at i_{c1}. Both i_{c1} and v_{c1} are seen to lie within the maximum ratings ($i_c$max and $v_c$max). The slope of this line (v_{c1}/i_{c1}) yields the load resistance.

CLASS-B POWER AMPLIFIERS

Graphical constructions are particularly serviceable in large-signal systems design, of which the class-B power amplifier is a typical example.

The use of load lines in the determination of driving and output conditions, load resistance, and operating characteristics of transistorized class-B amplifiers has been covered in the article *Class-B Transistor Amplifier Data* which appeared in the January 1955 issue of the RESEARCH WORKER. To avoid repetition here, the reader having need of these data is referred to that issue.

REFERENCES

For additional information concerning the application of the load line technique to the design of transistorized circuits, the reader is referred to the following publications.

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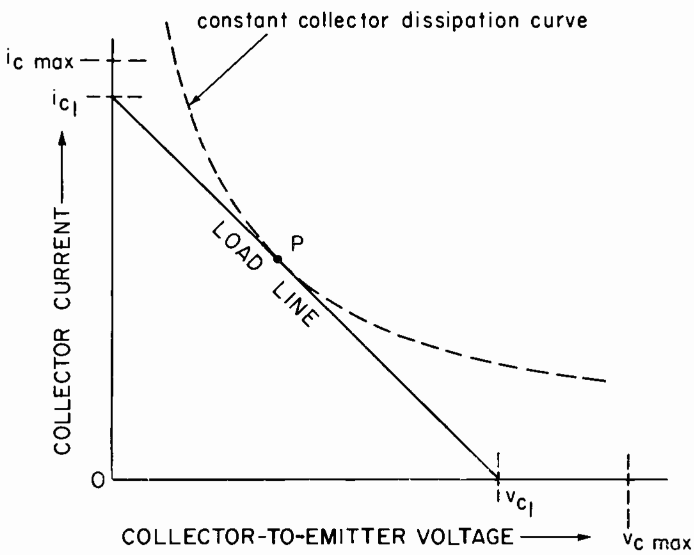

CONDITIONS FOR MAXIMUM POWER OUTPUT

FIGURE 4

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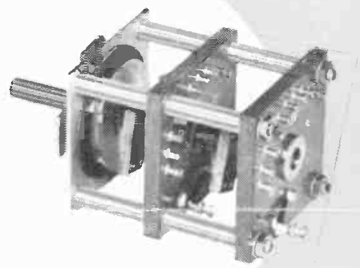

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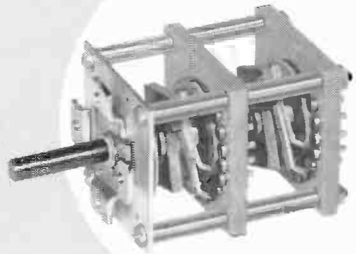

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