RCA

BROADCAST AND COMMUNICATIONS PRODUCTS

MAINTENANCE

TR-4 Television Tape Recorder

VIDEO SYSTEM

RADIO CORPORATION OF AMERICA

IB-31818

ELECTRONIC RECORDING PRODUCTS

MAINTENANCE

TR-4 Television Tape Recorder

VIDEO SYSTEM

RADIO CORPORATION OF AMERICA
BROADCAST AND COMMUNICATIONS PRODUCTS, CAMDEN, N. J.

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VIDEO SYSTEM DESCRIPTION

Introduction

The function of the video system is to convert the incoming composite video signal to a frequency modulated signal for recording on magnetic tape, and on playback to convert the tape FM to the amplitude modulated format originally applied to the input.

The video system, shown in the simplified functional diagram, figure 1, consists of the following modules:

No.	*Name*
A1	Video Input
A2	Modulator
A3-A6	Record Amplifier
A11-A14	Playback Amplifier
A15	FM Switcher
A16	Limiter
A17	Limiter
A18	Demodulator Output
A20	Horizontal AFC
A21	Video/FM Control
A22	Video Output
B21	Sync Logic
B22	Vertical Advance
2A1	Video Preamplifier

To simplify the functional description of the video system, the latter will be divided into two subsystems, (1) video/FM, and (2) signal processing. The video/FM subsystem description will include all but the five modules shown in the signal processing group, except for the Video/FM Control (module A21) which functionally is part of both subsystems. The signal processing subsystem description will cover the five modules forming this subsystem.

Video/FM Subsystem

(Refer to the block diagram, figure 2.)

Record Mode

Composite video is applied to the Video Input (module A1). Here the level of video is set and the video is then distributed to two outputs. One goes to the Modulator (module A2) and the other goes to the CRO and picture monitor. Sync is separated from the incoming video and fed to the Modulator and the Reference Generator (module B18). The latter is part of the Headwheel Servo system.

In the Modulator, the recording standard, monochrome or color, is selected and the signal is clamped at the sync tip level. With this selection, the proper

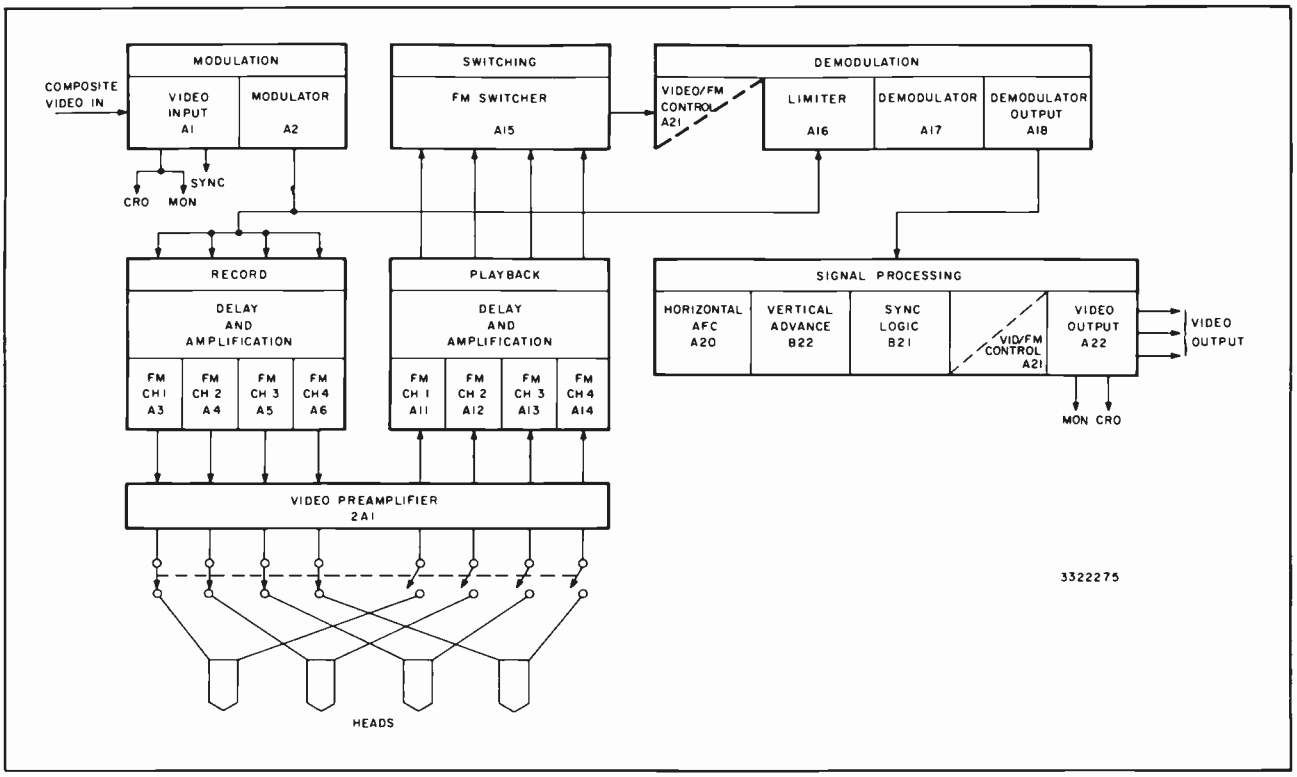


Figure 1—Simplified Video Functional, TR-4 Tape Recorder

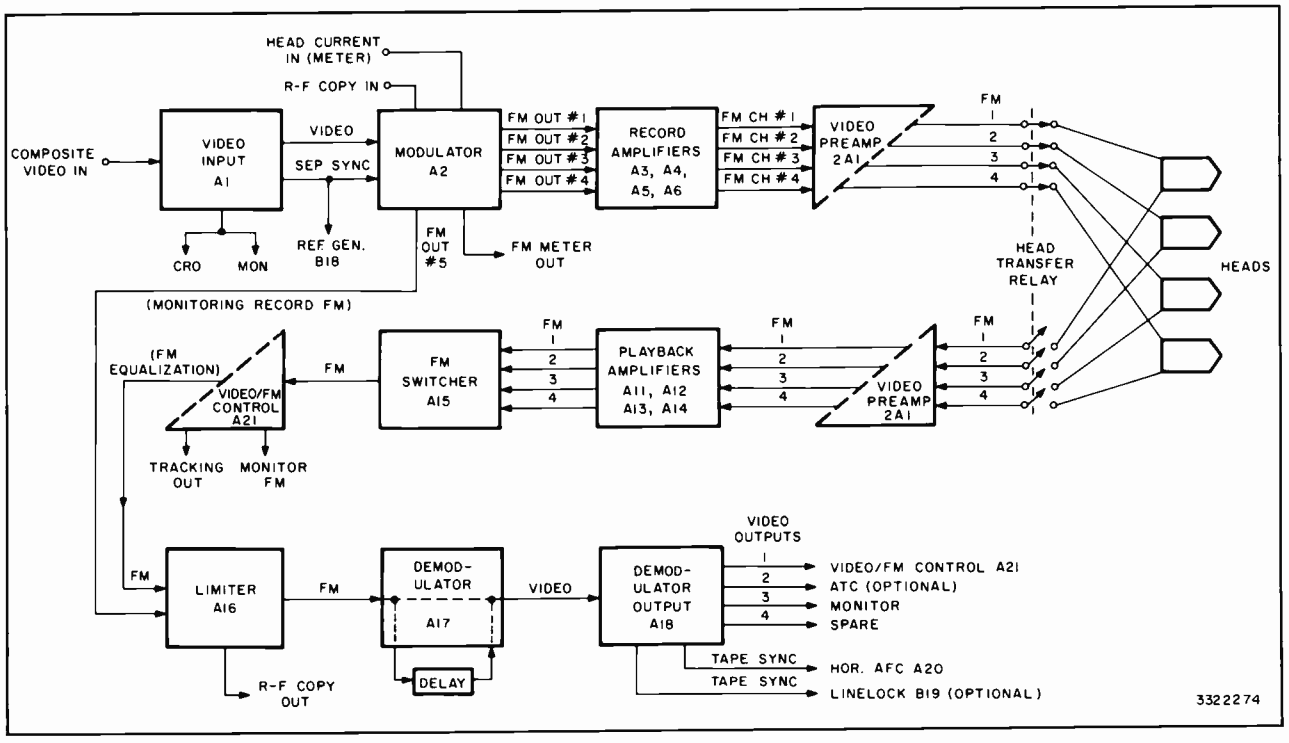


Figure 2—Block Diagram, Video/FM Subsystem

amount of pre-emphasis is added to the signal, and the deviation of the FM signal ultimately derived in the Modulator is established. R-F Copy switching facilities, which disable the frequency modulation conversion circuits, are provided so that the output of another player/recorder can be fed through the FM amplifier output circuits of the Modulator to be re-recorded. Included on this module is a sync tip frequency metering circuit.

The FM output of the Modulator drives five separate output lines. Of the first four outputs, one each goes to a Record Amplifier (modules A3-A6). The fifth output goes to the Limiter (module A16) and is used for monitoring the FM output of the Modulator when recording.

The four Record Amplifier (modules A3-A6) are identical and each contains an adjustable delay line. The signal entering a Record Amplifier passes through the delay line which is adjusted to compensate for errors in the mechanical displacement of the magnetic heads from exactly 90 degrees around the circumference of the headwheel. The signal then passes through amplifiers which increase the magnitude of the signal current to a level suitable for driving the heads. A level control on each module enables optimum adjustment of the signal current of each channel.

The output from the Record Amplifiers is coupled through the head transfer relay on the Video Preamplifier (module 2A1) to the slip rings on the headwheel. A metering circuit on this module enables the record current of each head to be evaluated on a multimeter.

Playback Mode

The output of each head is coupled by the head transfer relay to one of the four preamplifier circuits on the Video Preamplifier (module 2A1). The preamplifier circuits furnish the proper impedance match between the heads and the four Playback Amplifiers (modules A11-A14) to which the four playback signals are fed.

The four Playback Amplifiers are identical. Besides the amplifier circuits to provide the desired gain, each has an adjustable delay line and an equalizer circuit. The former serves the same purpose as those on the Record Amplifiers i.e., to compensate for errors in head quadrature. The equalizer circuit permits equalization of each channel on an individual basis to compensate for variations in the frequency response of the heads. The gain of each amplifier can be adjusted so that the level of the FM output of the four channels is the same.

Following the Playback Amplifiers is the FM Switcher (module A15). Here in this module the four channels are combined into one continuous output which is fed to the FM equalization section of the

Video/FM Control (module A21). The FM equalizer circuit permits adjustment of overall equalization to compensate for the loss of high frequency components in the FM signal during the head to tape transfer. The output of the equalizer circuit goes from the Video/FM Control module to the Limiter (module A16).

After entering the Limiter, the signal passes through several stages of limiting where symmetrical clipping of the positive and negative peaks take place. From the Limiter the signal is fed to the Demodulator (module A17). Included on the Limiter is a switching circuit that enables the r-f copy output to be inserted in parallel with output going to the Demodulator. This makes it possible to feed the output signal simultaneously to another recorder for re-recording.

In the Demodulator the video information in the FM signal is detected. The resulting output is a signal that is a replica of the original video modulating signal. From this module the signal goes to the Demodulator Output (module A18).

The Demodulator Output module is a video distribution amplifier that includes post-emphasis and sync separation. The post-emphasis circuit restores the video components to the same level that they were before pre-emphasis. The video is then amplified and fed to four outputs for distribution. One output goes to the video control section of the Video/FM Control (module A21); one goes to the monitor switcher; another serves as a spare and the last is for use with the optional ATC system. Sync that has been stripped from video is fed to the Horizontal AFC (module A20) and is also available for the optional Linelock (module B19).

The Demodulator Output is the last in the chain of modules making up the video/FM subsystem.

Signal Processing Subsystem

(Refer to the block diagram, figure 3.)

The function of the monochrome signal processing subsystem is to restore all components of the video signal to insure that the output signal is a standard video signal suitable for transmission. The video signal is clamped to set the proper dc level, new blanking is added, present sync is removed and new added. When the video signal enters the processing modules, the sync pulse may be deformed with noise spikes and switching transients during the blanking interval. The signal processing subsystem provides a video output signal with a clean and adjustable black level and a clean horizontal sync interval. The processing includes complete regeneration of horizontal sync, horizontal and vertical blanking, and reinsertion of the vertical interval. The clean horizontal interval eliminates mis-

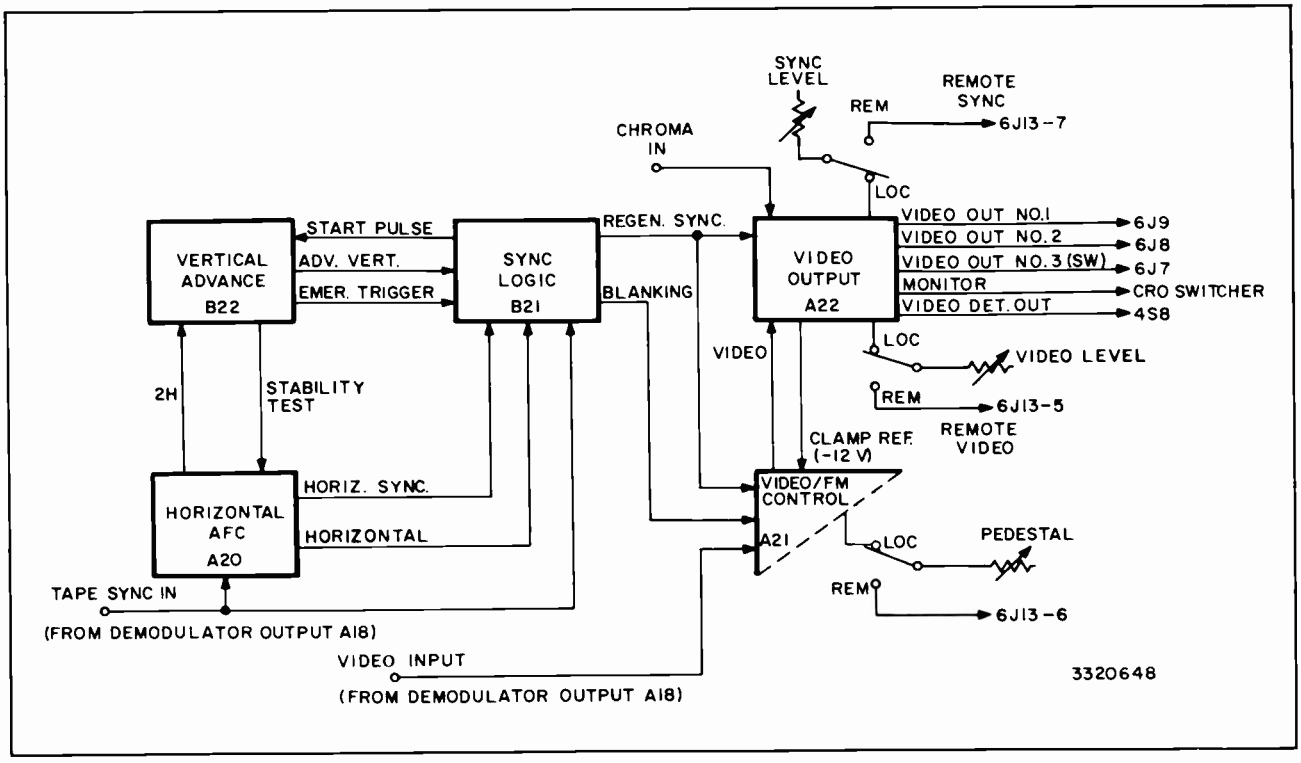


Figure 3—Block Diagram, Signal Processing Subsystem

clamping in stabilizing and transmitter amplifiers, which tends to occur due to the noise in the area below black level.

The three pulse-forming modules, Horizontal AFC (A20), Vertical Advance (B22), and Sync Logic (B21), form a sync timing and regeneration system. These modules are closely interlinked functionally to produce blanking, gated horizontal sync, and regenerated sync. The blanking pulses needed for both monochrome and color tape recording systems are regenerated from the sync pulse. The remaining two modules, Video/FM Control (A21) and Video Output (A22), handle the video component. Within these two modules, all signal elements are combined to form the new outgoing composite video signal.

The Horizontal AFC module regenerates horizontal blanking and horizontal sync, both of which are supplied to the Sync Logic module. The Horizontal AFC module generates a 31.5 kc square wave which is used to automatically control the phase and frequency of the new 15.75 kc signal with respect to tape sync reference. The 31.5 kc square wave is also used to drive the Vertical Advance module.

The Vertical Advance module generates a 3.5H pulse and an emergency trigger pulse. The 3.5H pulse is used as a trigger in determining the leading edge of vertical blanking, which is generated in the Sync Logic module. The emergency trigger pulse insures continuation of precise timing of the vertical blanking interval, should there be any interruption in the normal 3.5H trigger action.

The video signal from the Demodulator Output (module A18) is applied to the Video/FM Control module. Here it is amplified to a level suitable for stable clamping. Blanking is added and the video signal is then fed to the Video Output module. A means for remotely controlling the pedestal level is provided on the Video/FM Control module.

The Video Output module combines the video signal and the regenerated sync to form the composite video signal. This signal is available at four separate outputs, three of which are external and one of which is used internally to feed the CRO monitor. A switching circuit that enables either local or remote control of both video and sync levels is included on this module.

International Version

The Sync Logic, Vertical Advance and Horizontal AFC modules used in the international model of the TR-4 have been modified to conform to the line rates for international standards, in addition to the 525-line standard. Although certain circuits were expanded and switching facilities added, the international modules are similar in principle to their counterparts in the domestic model.

Most of the modifications in the three pulse-forming modules consist of simple time constant changes in order to obtain the correct pulse widths needed for the different TV standards. The only major changes are in the start pulse generator circuit of the Sync Logic module and in certain areas of the counter chain in the Vertical Advance module. The start pulse generator in the Sync Logic module is capable of producing a start pulse that is suitable for both 405- and 625-line standards. The Vertical Advance module contains the circuitry necessary to change the timing of the 3.5H pulse so that it is compatible with 405- and 625-line standards. The desired line rate, 405/525/625, is selected by means of the TV STANDARDS switch on the front panel of the Vertical Advance module. In the Horizontal AFC module, the modifications consist of changes in the time constant components in the 2H master oscillator and the horizontal square wave multivibrator circuits, plus a starting circuit for the 2H oscillator.

Following the description of each of the domestic standards pulse-forming modules, the circuit details peculiar to the international modules are discussed. Where necessary, simplified schematic diagrams and waveforms are included.

MODULE DESCRIPTIONS

Video Input (Module A1)

General

The Video Input module amplifies and distributes the applied composite video signal to two outputs and supplies sync that has been stripped from the incoming video to two outputs. This module contains a video distribution circuit and a sync separator circuit.

As shown in the block diagram, figure 4, the incoming video is passed through two emitter followers then to a variable gain control stage. From here the signal is fed through an impedance matching common base amplifier, then through two more amplifier stages to a series output amplifier. The video output of the series amplifier is fed via two sending-end terminated lines to the Modulator (module A2) and to the monitor.

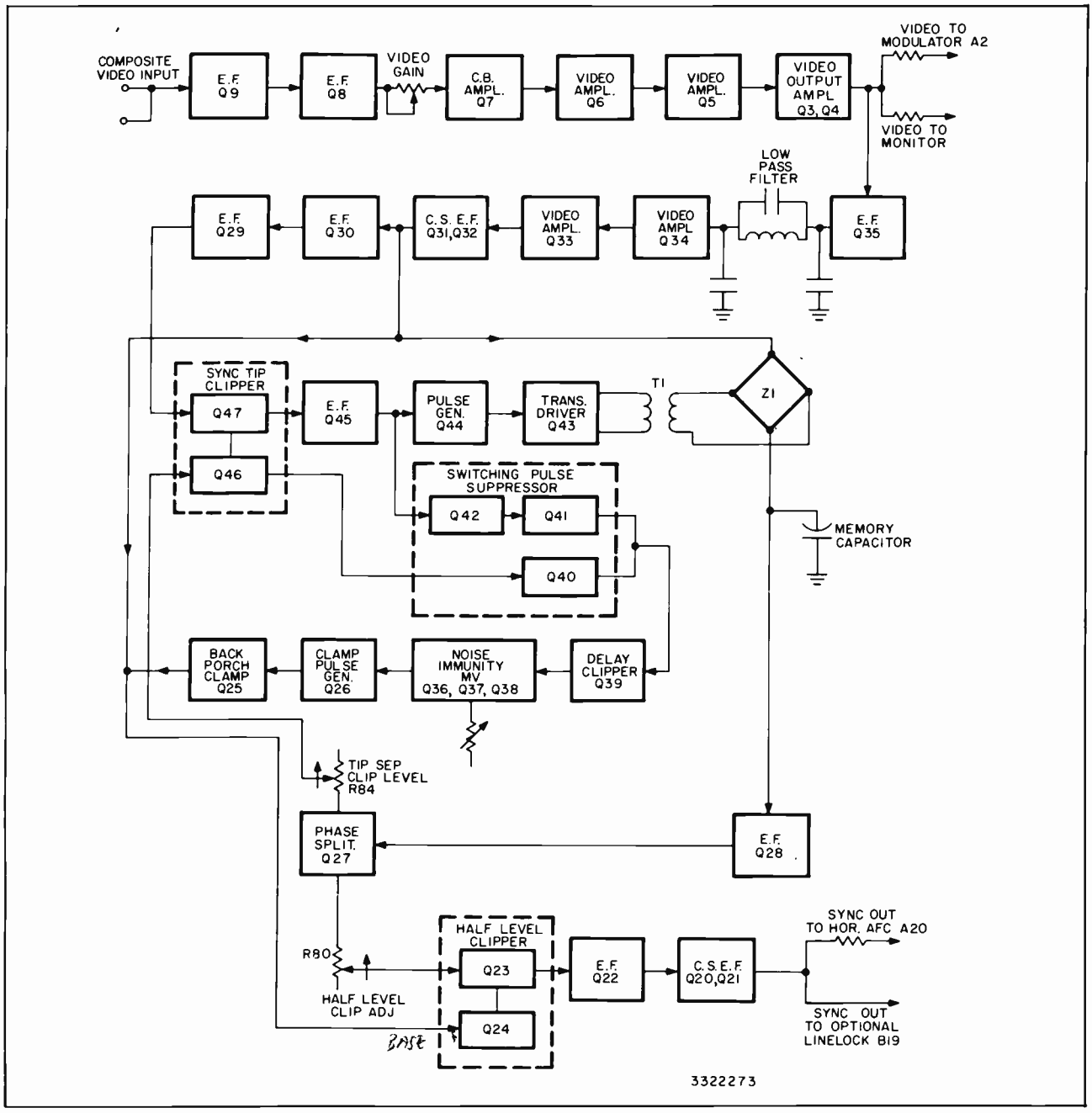


Figure 4—Block Diagram, Video Input Module

This stage also supplies video to the sync separator circuit.

The sync separator circuit extracts sync from the video signal without introducing any timing errors. This is accomplished by insuring that clipping occurs at one half the level of the sync pulse, regardless of the video input level, switching spikes, dropouts, or noise.

The video input to the sync separator is applied to an emitter follower, then through a low pass filter which removes high frequency components in the video and noise, then continues through two stages of amplification to a complementary symmetry emitter follower. From here the signal is fed through two emitter followers to the input section of the sync tip clipper. Two other outputs are also taken from the C.S.E.F. One goes to the diode quad and the other goes to the half level clipper.

The half level clipper consists of two transistors. Video is applied to one transistor and at this point the

back porch of the signal is clamped to ground. A dc reference voltage from a phase splitter is applied to the other transistor. This voltage is maintained at exactly one half the level of the incoming sync by the output of the diode quad, which serves as a sync sensing circuit. The half level clipper is designed so that one transistor conducts throughout that portion of video more positive than the half level of sync, and the other transistor conducts throughout that portion of video more negative than the half level of sync. This switching action between the two transistors produces a negative sync pulse that is timed precisely with the half level point of sync. This insures that the sync pulse ultimately available at the C.S.E.F. output stage for driving the output lines will be of constant width, regardless of variations in the level of the input signal.

The output of the diode quad determines the output of the phase splitter which is used as a reference for the half level clipper and the sync clipper. The diode quad keying pulses are produced by the pulse generator. The latter is triggered by pulses derived in the sync clipper. The keying pulses are applied out-of-phase to the diode quad. When the quad is keyed on, video passes through and the memory capacitor on the output side of the quad charges to the level of the sync tip.

The memory capacitor is connected to an emitter follower which has a high input impedance, thus preventing the capacitor from discharging during the intervals between keying pulses. The output of the emitter follower is fed to the phase splitter which provides two oppositely phased outputs that are proportional to the capacitor voltage. One output is taken across potentiometer R80 and fed to the half level clipper. The voltage across this potentiometer is half that of the sync tip. The other output is taken across potentiometer R84. The voltage across this potentiometer establishes a dc reference for the video input to the sync tip clipper that is just below the black level of the lowest sync pulses.

The back porch clamp insures that the sync timing contained in the composite video is accurately reproduced by the sync separator. The switching pulse suppressor, delay clipper, and noise immunity multivibrator all contribute towards this end.

The switching pulse suppressor generates a modified sync pulse which is slightly wider than normal sync. This modified sync pulse is called a "push out" pulse. This pulse occurs during the horizontal sync and equalizing pulse intervals and, in effect, pushes out any switching transients appearing in the sync or equalizing pulses.

The noise immunity multivibrator eliminates noise from the switching pulse suppressor, during the active scan time of the video signal, and divides by two during the 9H interval. The multivibrator triggers the clamp pulse generator at the trailing edge of modified sync.

The clamp pulse generator produces a high amplitude pulse whose width is accurately controlled. This pulse keys the back porch clamp and the latter, in turn, clamps the back porch of the video input to the half level clipper, during every horizontal blanking interval. During the 9H interval, however, clamping occurs at the black level interval after every equalizing pulse and during every serration of vertical sync. The width of the clamp pulse is rigidly controlled to prevent clamping near the edges of sync.

Circuit

Video Distribution Amplifier

Composite video is applied to pins 17 or 18 on the Video Input module (see figure 5) via one of the two coaxial input jacks 16J1 or 16J2, which are on the record connector panel on the rear of the TR-4. These jacks are connected together at a point within the module so that the input signal can be looped through the TR-4 or terminated at the unused jack.

The input signal is coupled through C14 to the base of Q9, an emitter follower. The output on the emitter is direct coupled to the base of Q8, another emitter follower. These two transistors form the input stage which is designed to accommodate high voltage tube equipment. The feedback circuit between Q8 and Q9 presents a high input resistance that makes possible the use of a voltage input coupling capacitor of reasonable size without sacrificing low frequency response.

The feedback signal from the emitter of Q8 to the base of Q9 is fed through R29, C12, C11, and R26. This signal is in phase with, and almost equal in Q9. Because the amplitude of the signal voltage at each end of R26 is almost identical, very little current amplitude, to the input signal applied to the base of flows through this resistor. Thus the *apparent* input resistance is very high, being over ten times the actual value of R26. Resistor R18 in series with the R26 provides isolation and both resistors in conjunction with R16 form a voltage divider returned to −20 volts, which furnishes dc bias to the base of Q9.

From the emitter of Q8, the signal is fed across R28, R20, the VIDEO LEVEL potentiometer, and R19 to the emitter of Q7, a common base amplifier. The

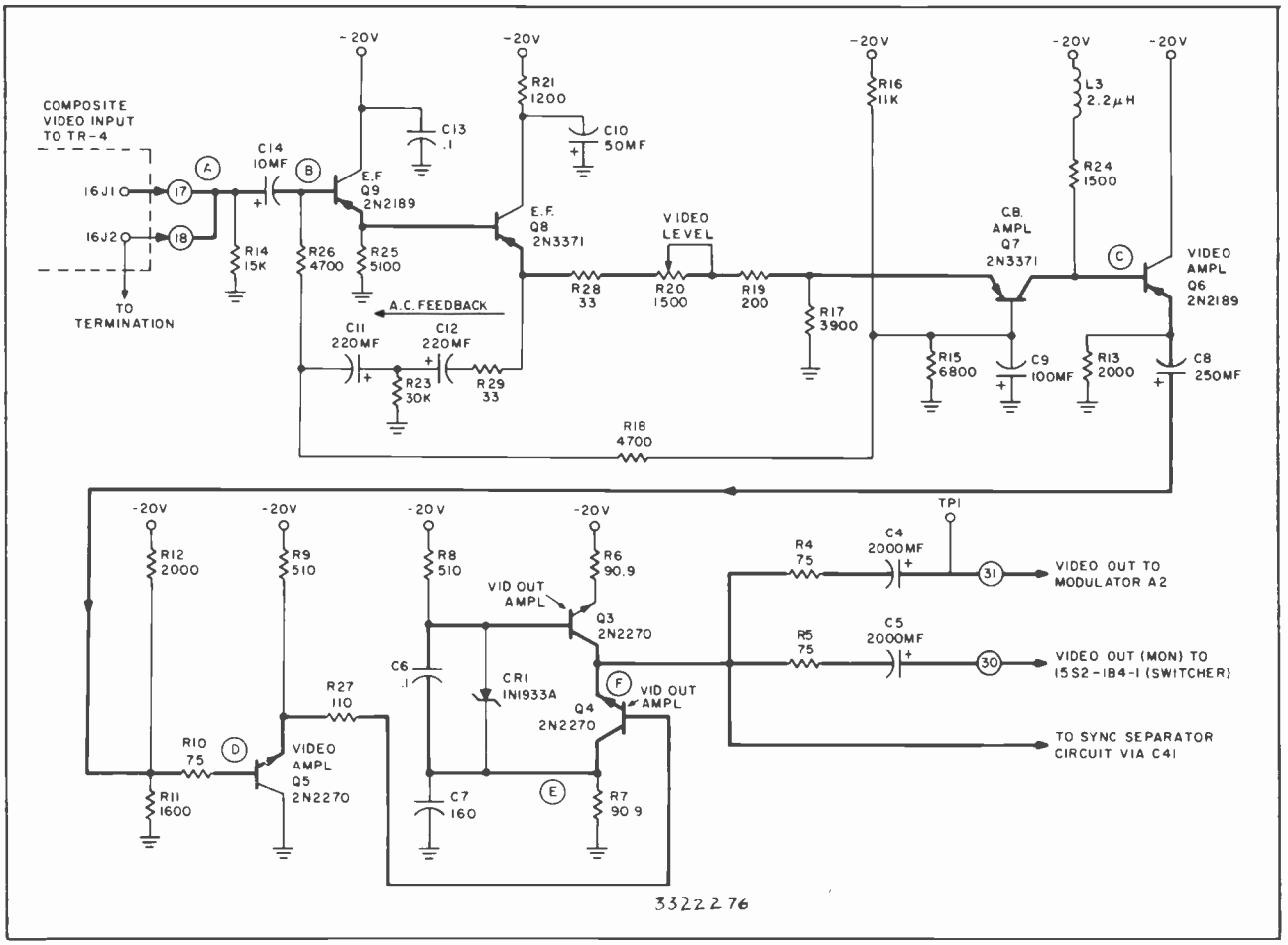
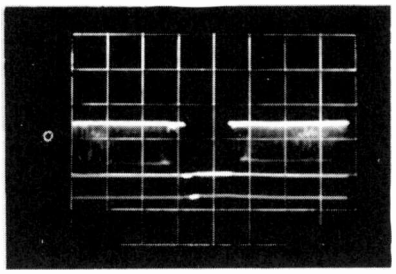
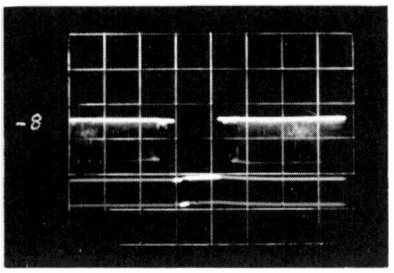


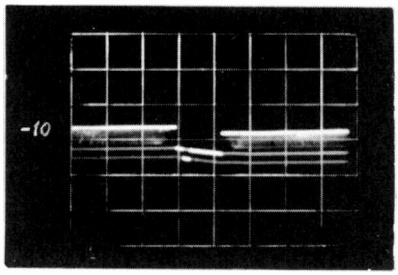
Figure 5—Video Amplifiers, Gain Control, and Output Circuits



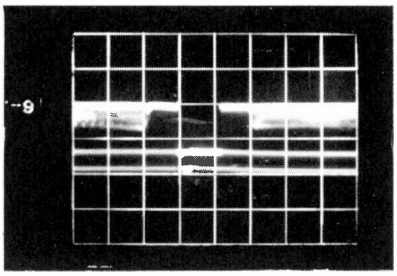
A. Input Side of C14, 1 ms/cm, .5v/cm



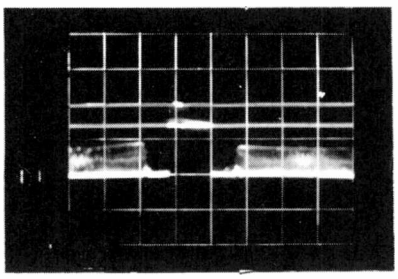
B. Q9 base, 1 ms/cm, .5v/cm



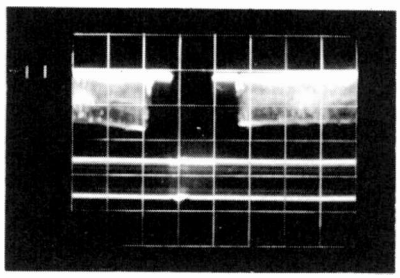
C. Q7 collector, 1 ms/cm, .05v/cm



D. Q5 base, 1 ms/cm, 1v/cm



E. Q4 collector, 1 ms/cm, .5v/cm



F. Q3 collector/Q4 base, 1 ms/cm, .5v/cm

Figure 6—Typical Waveforms, Video Amplifiers, Gain Control and Output Circuits

setting of the VIDEO LEVEL potentiometer, which is a front panel control, determines the amplitude of the signal applied to the emitter of Q7. The common base configuration of Q7 provides low input impedance and the desired voltage gain. A peaking coil, L3, is used in series with the collector load, R24, to maintain the response at the high frequency end of the band. The output on the collector of Q7 is direct coupled to the base of Q6, an emitter follower. From the emitter of Q6 the signal is fed through R10 to the base of Q5, another emitter follower. The two cascaded emitter followers isolate Q7 from the succeeding series output amplifier, Q3, Q4.

The configuration of the series output amplifier is such that Q4 assumes the characteristics of both an emitter follower and a common emitter amplifier, while Q3 exhibits those of a common emitter amplifier. The input signal is applied to the base of Q4 and the inverted output is taken off the collector and coupled through C6 to the base of Q3. The output on the collector of Q3, having been inverted also, is in phase with the signal on the emitter of Q4. Since the output signal is taken at the emitter-collecor junction of these two transistors, it contains the components of both of these signals which, in effect, is the same as push-pull output. Such a configuration combines low output impedance with unity gain of the signal. The Zener diode, CR1, which is connected between the collector of Q4 and the base of Q3, maintains a constant 12-volt difference between these two elements.

The output of Q3, Q4 is fed simultaneously to the input of the sync separator circuit and to two sending-end terminated lines. The signal on one line is coupled through R4 and C4 to feed the Modulator (module A2). The signal on the other line is coupled through R5 and C5 to feed the monitor switches.

—20 Volt Regulator

The dc operating voltage for the video distribution amplifier section of this module is furnished by a —20 volt regulator consisting of Q1 and Q2, both emitter followers (see figure 7). The base of Q1 is biased to —20 volts across R1. The potential on the emitter of Q1 is virtually the same as that on the base, and since the emitter of Q1 is direct coupled to the base of Q2, the base of the latter is also biased at approximately —20 volts. Since the base of Q2 is —20 volts, the output voltage available at the emitter is the same potential. Because Q2 exhibits the low output impedance characteristic of an emitter follower, the output voltage remains constant despite variations in the load.

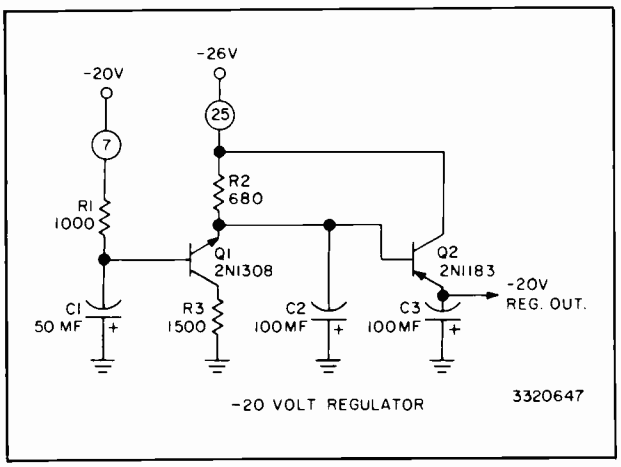


Figure 7 — —20 Volt Regulator Circuit

Sync Separator

1. Video Amplifiers

Video from Q3, Q4 is coupled through C41 to the base of Q35, an emitter follower, (figure 8) which isolates the video input line from the loading effects of the succeeding stages. From the emitter of Q35, the signal is fed across R104 through a low pass filter consisting of C39, C40, C59, and L2 to the base of Q34, a video amplifier. The filter removes high frequency video and noise but passes all frequencies below 1.2 mc.

The gain of Q34 is determined by the ratio of the collector resistor R101 over the resistance presented by R100 and R102 in parallel in the emitter circuit. The output of the collector of Q34 is direct coupled to the base of Q33. This stage has a gain of approximately 3.1, and the output signal on the collector, which is fed to the bases of the complementary symmetry emitter follower Q31, Q32, in approximately 10 volts peak-to-peak.

Both transistors of the C.S.E.F. are biased on continuously to prevent a crossover region where neither transistor conducts. A dc blocking capacitor, C36, provides isolation between the two emitters, thus preventing small differences in dc potential from upsetting the quiescent bias conditions on each transistor. The output is taken off the emitter of Q31 and fed to two branches.

The signal following one branch is coupled through C35 and applied simultaneously to diode quad Z1 (figure 10) and to the base of Q24 in the half-level clipper circuit (figure 16). The video in the second branch is direct coupled to two emitter followers, Q30 and Q29 (figure 10).

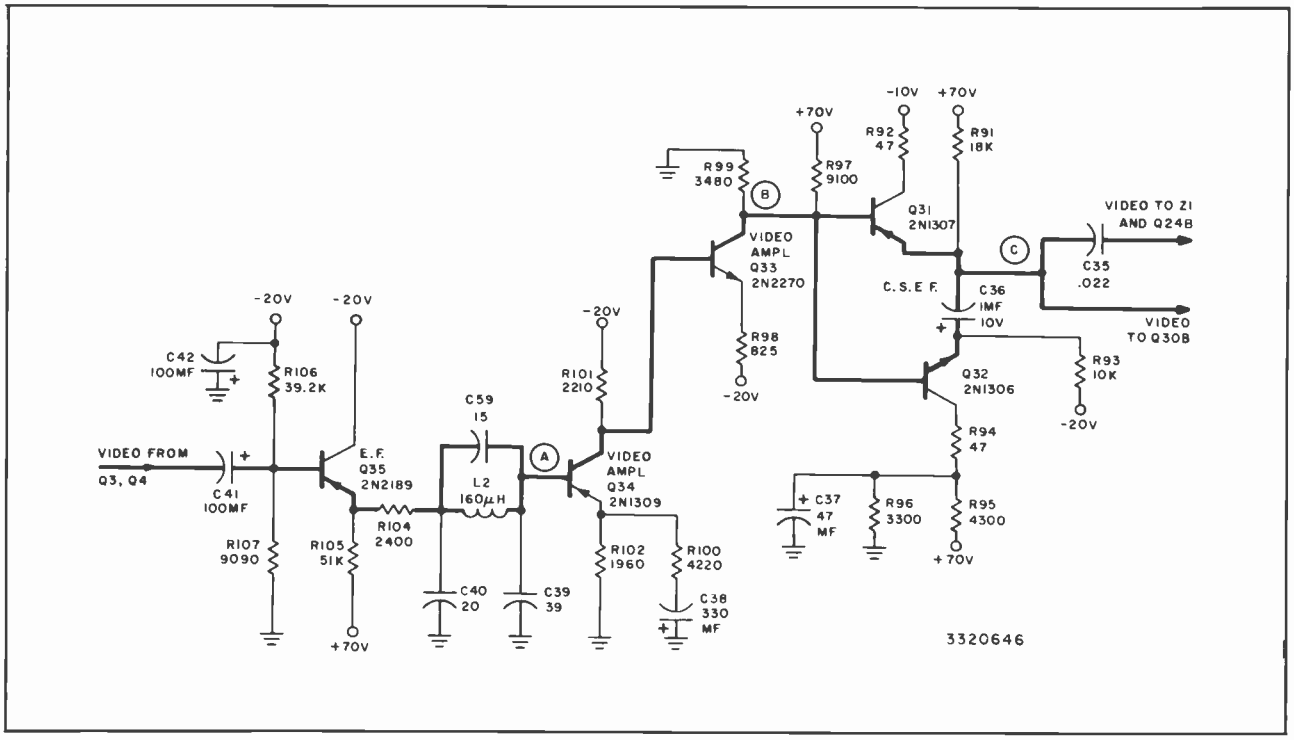
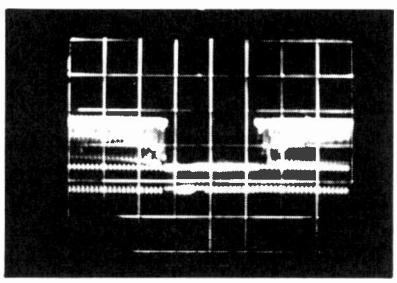
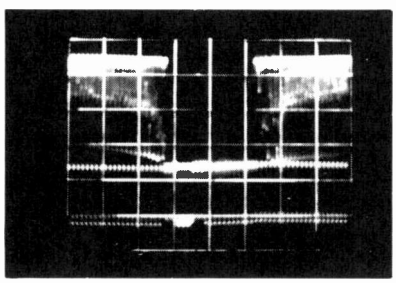


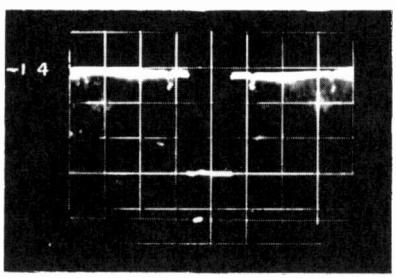
Figure 8—Video Amplifiers and Complementary Symmetry Emitter Follower Circuits



A. Q34 base, 0.5 ms/cm, 1v/cm,



B. Q33 collector, 0.5 ms/cm, 2v/cm



C. Q31 emitter, 1 ms/cm, 2v/cm

Figure 9—Typical Waveforms, Video Amplifiers and Complementary Symmetry Emitter Follower Circuits

2. Sync Tip Clipper

Transistors Q30 and Q29 produce the proper drive and isolate the C.S.E.F. from the effects of the dc setting diode, CR21. From the emitter of Q29 the signal is coupled through C55 to the base of Q47. Transistors Q47 and Q46 are connected in a differential clipper configuration to form the sync tip clipper. (The operation of this type of circuit is covered later in the description of the *Back Porch Clamp and the Half-Level Clipper.*) The base of Q47 is connected to the cathode of the dc setter diode, CR21, which is biased on by R149. Diode CR21 clamps the sync tip of the incoming video signal to approximately −1 volt. Since the amplitude of the applied signal is 10 volts, the signal on the base of Q47 (A, figure 11) goes from −1 volt of sync tip to +9 volts at peak white.

The base of Q46 is connected to a voltage divider in the collector of phase splitter Q27. The divider consists of R83, potentiometer R84, the tip separation clipping level (TIP SEP CLIP LEVEL) control, and R85 which is returned to +70 volts. The dc voltage supplied to the base by this divider depends on both the video level measured by the half-level sensor (to be described later) and the setting of the TIP SEP CLIP LEVEL control, R84. This voltage establishes the clipping level of this stage.

Transistors Q46 and Q47 are joined together at their emitters, therefore, under the bias conditions

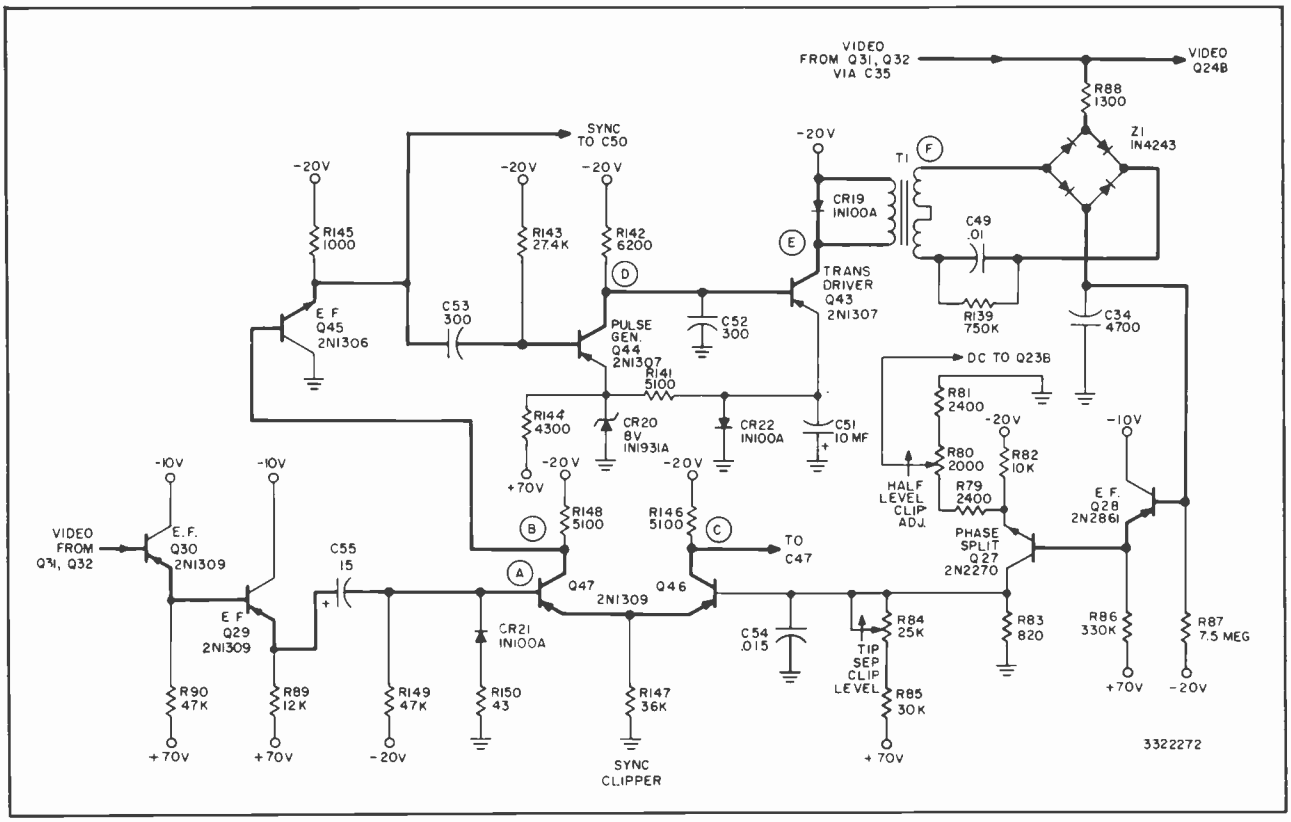
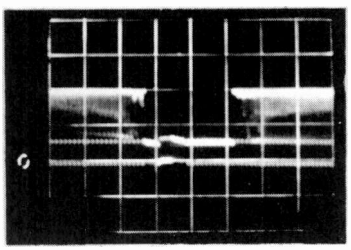
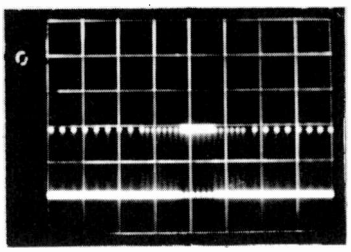


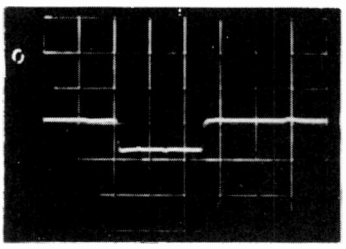
Figure 10—Video Input, Sync Clipper, Pulse Generator, Clamp Quad and Phase Splitter Circuits



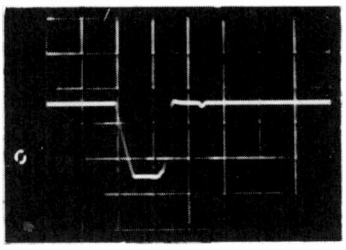
A. Q47 base, 0.5 ms/cm, 5v/cm.



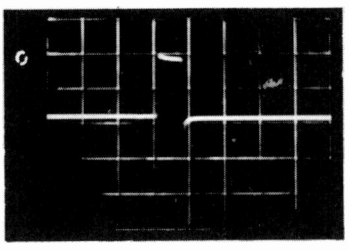
B. Q47 collector, 0.2 ms/cm, 5v/cm.



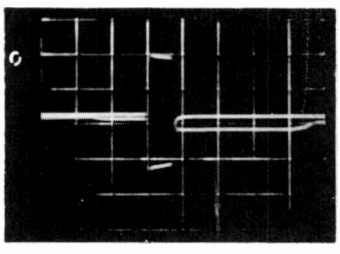
C. Q46 collector, 2 μs/cm, 5v/cm.



D. Q44 collector, 2 μs/cm, 5v/cm.



E. Q43 collector, 2 μs/cm, 10v/cm.



F. Top: T1-3, 10v/cm, Bottom: T1-5, 10v/cm, 2 μs/cm.

Figure 11—Typical Waveforms, Video Input, Sync Clipper, Pulse Generator, Clamp Quad and Phase Splitter Circuits

that have been established, Q46 conducts and Q47 is cut off when the video signal is more positive than the bias on the base of Q46. When the video signal is more negative than the bias on Q46, the latter is cut off and Q47 conducts. The resulting alternating outputs on the collectors of the sync clipper consist of a negative going sync-pulse from −10 to −20 volts on the collector of Q46 (C, figure 11) and a positive going sync pulse from −20 to −10 volts on the collector of Q47 (B, figure 11).

The positive going pulse on the collector of Q47 is direct coupled to emitter follower Q45. Two outputs are taken off the emitter of this transistor; one is coupled through C53 to the base of Q44, the pulse generator, which is part of the half-level sensor circuit. The other output is coupled through C50 to the base of Q42 in the switching pulse suppressor circuit. The negative going pulse on the collector of Q46 is coupled through C47 to the base of Q40, which is also part of the switching pulse suppressor circuit.

3. Half-Level Sensor

To return to the pulse generator, Q44 (figure 10). This transistor is a boxcar* or pulse narrowing circuit, the purpose of which is to produce keying pulses for the diode quad, Z1, that are more narrow than equalizing pulses.

In the interval between pulses when no signal is applied to its base, Q44 conducts. The base is connected to −20 volts through R143, and the emitter is at +8 volts established by Zener diode CR20 and R144, therefore the potential on the base is approximately the same as that on the emitter. When a 10 volt pulse from Q45 is applied through C53 to the base of Q44, the positive going transition causes the base to go 10 volts positive with respect to the +8 volts already present and Q44 is cut off. Capacitor C53 then begins to discharge from +18 volts toward −20 volts through R143, but when the voltage on the base reaches +8 volts, Q44 again conducts. The RC time constant of C53 and R143 is such that the duration of the keying pulse (D, figure 11) appearing on the collector of Q44 is shorter than the duration of an equalizing pulse. From the collector of Q44, the keying pulses are direct coupled to the base of Q43, the transformer driver.

In the steady state condition, the average current through transformer driver Q43 establishes a dc charge on C51 of approximately −2 volts. Since the RC time constant of C51 and R141 returned to +8 volts is long compared to the H interval — the rate at which Q43 is driven — C51 does not have time to discharge between pulses and the bias on Q43 is essentially dc. During the interval between pulses, there is no average current flowing through Q43 since it is normally off. Therefore the charge on C51 is held from going to +8 volts by diode CR22. This circuit action prevents collector to emitter breakdown at Q43 and a reverse polarity condition on C51 when there is no input signal present.

Since the collector of Q44 (D, figure 11) is normally at +8 volts, and the emitter of Q43 is normally at −2 volts, Q43 is biased off. When a negative going narrow pulse occurs on the collector of Q44, it is direct coupled to the base of Q43. The transition from +8 volts to −2 volts (the level at which Q43 conducts and clamps the signal) is slowed by the time constant of C52 and R142 returned to −20 volts. Transistor Q43 is driven into saturation, producing a narrow 18-volt pulse on the collector (E, figure 11) which is delayed with respect to the leading edge of sync. The delay introduced in the path of the half-level sensor keying pulse by the action of C52 and R142 insures that amplitude sensing occurs only during the actual sync tip interval, and not on the leading edge of sync. The output on the collector of Q43 is connected across the primary of T1 which feeds the keying pulses to the diode quad, Z1. Diode CR19, across the primary of T1, prevents inductive ringing.

The secondary of T1 is connected across two opposite sides of diode quad Z1. Video from C.S.E.F. Q31, Q32 is fed across R88 to the top of Z1 (and also directly to the base of Q24 in the half-level clipper circuit). The bottom of Z1 is connected to a memory capacitor, C34.

When a pulse from Q43 is applied to the primary of T1, two high amplitude narrow pulses of opposite polarity appear at opposite end of the secondary (F, figure 11). These pulses key all four diodes in the quad simultaneously, and the video signal is fed through to the memory capacitor, C34, which charges to the level of the sync tip. The amplitude of the voltage equivalent to sync tip on C34 is with respect to ground because the back porch is clamped to ground by Q25. During the pulse period, the parallel RC network of R139, C49, which is connected from one end of the secondary to one side of the quad, develops a bias voltage that keeps the quad cut off between pulses. When the quad is cut off, the memory capacitor, C34, essentially has no discharge path except through the 7.5 megohoms of R87 to −20 volts. Thus the charge remains on the capacitor until the next keying pulse arrives.

* *See Basic Circuit Descriptions on page 128.*

The voltage on C34 is fed through a very high input impedance emitter follower, Q28, to the base of phase splitter Q27. The emitter of Q27 is returned to ground through a voltage divider consisting of R79, R80, the HALF LEVEL CLIP ADJUST potentiometer and R81. The voltage on the arm of R80 is fed to the base of Q23 in the half-level clipper circuit. Potentiometer R80 is adjusted so that the voltage is equal to half the amplitude of the sync in the video signal that is fed to the base of Q24.

A voltage of opposite phase is taken from the voltage divider in the collector of Q27 and fed to the base of Q46. It will be recalled that this voltage determines the clipping level of Q46, Q47.

Instructions for setting R80 and R84 are given under *Adjustments,* immediately following the description.

4. Switching Pulse Suppressor

The switching pulse suppressor consists of multivibrator Q41, Q42, transistor switch Q40, and a delay clipper, Q39 (figure 12). This stage eliminates switching transients from the negative going sync which is obtained from Q46 in the sync tip clipper, by producing a modified sync signal that is wider than horizontal sync and equalizing pulses.

The collector of the Q41 section of the multivibrator and the collector of Q40, the transistor switch, are connected together to form a common input to

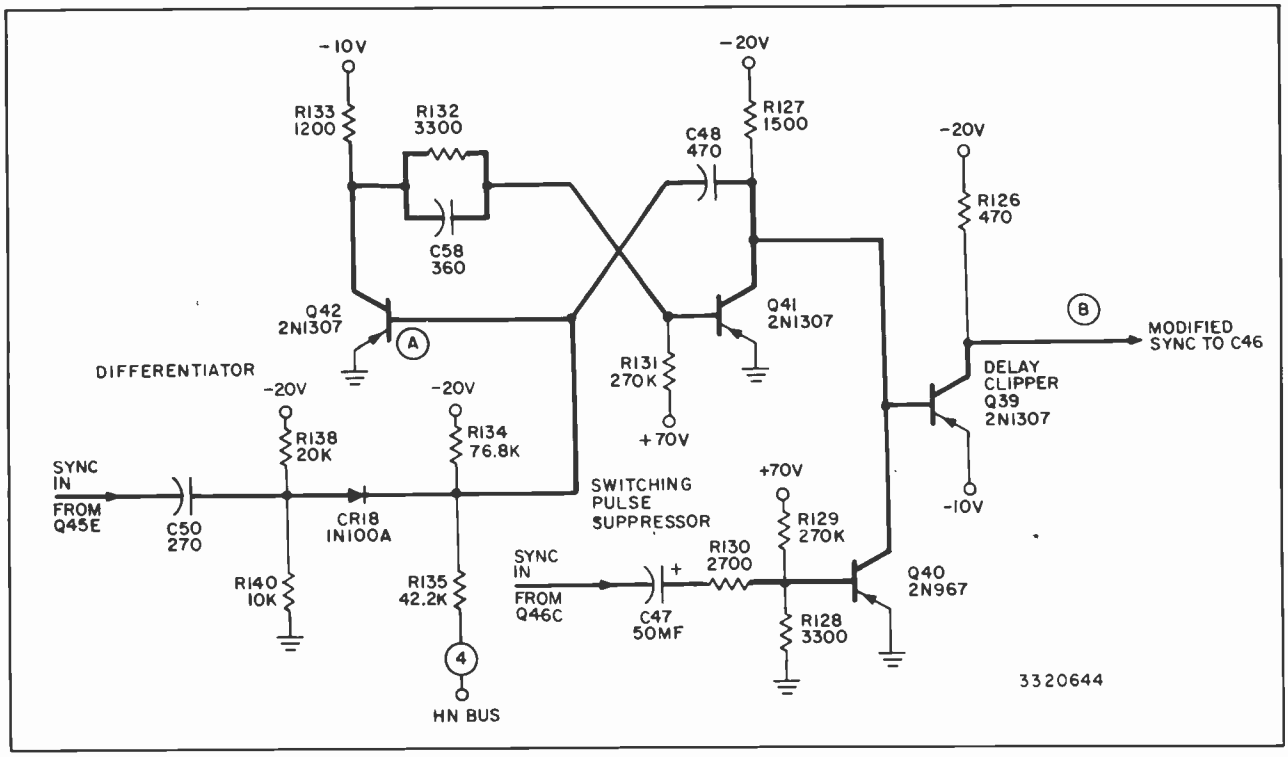
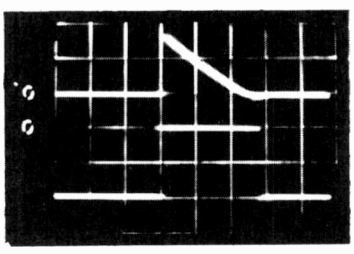
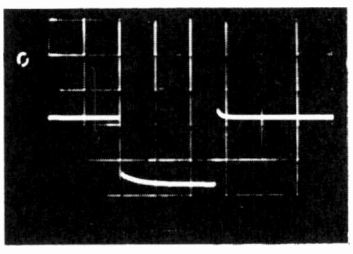


Figure 12—Switching Pulse Suppressor and Delay Clipper Circuits



A. Top: Q42 base, 5v/cm, Bottom: Q40 collector, 5v/cm, (Sweep rates 2 μs/cm)



B. Q39 collector, 2 μs/cm, 5v/cm

Figure 13—Typical Waveforms, Switching Pulse Suppressor and Delay Clipper Circuits

the base of Q39, the delay clipper. In the absence of sync, the other section of the multivibrator, Q42, is normally saturated and Q40 and Q41 are normally cut off since the emitters of the latter two are at ground and their collectors returned to −20 volts. Under these conditions, Q39 is saturated and the collector is at the same potential as the emitter, −10 volts. Transistors Q40 and Q41 form an *OR* gate which controls Q39 for (as will be shown later) when both or either conducts, the base of Q39 goes to ground and the collector to −20 volts.

Negative going sync pulses from Q46 are coupled through C47 and R130 to the base of Q40 and positive going sync pulses from Q45 are passed through a differentiator (C50, R138, R140). The negative peaks of the differentiated pulse are clipped by diode CR18 and the positive going leading edge is applied to the base of Q42. The leading edge of the negative going pulse on the base of Q40 drives this transistor into saturation and grounds the base of Q39. Simultaneously, the leading edge of the positive going pulse on the base of Q42 cuts this transistor off, causing Q41 to conduct. Thus, in effect, the base of Q39 is grounded through two switches (Q40, Q41) in parallel and Q39 is cut off. Transistor Q40 remains saturated as long as its base is negative which normally is the width of the applied sync pulse. Transistor Q41 remains saturated for the duration of the one shot period of the multivibrator. However, this period, which is established by the multivibrator timing capacitor, C48, is slightly longer than the duration of the sync pulse (A, B, figure 13).

If the sync input to Q40 contains a switching pulse, the base goes positive and Q40 becomes cut off. However, the switching pulse always occurs during the one shot period of the multivibrator, and, since this is longer than the duration of the sync pulse, the base of Q39 continues to be grounded through Q41. As a result, the pulse from the multivibrator "pushes out" the switching pulse, and the base of Q39 remains grounded through Q41.

At the end of the one shot period, Q41 becomes cut off. Transistor Q39 then conducts, and the collector (B, figure 13) goes from −20 to −10 volts. Thus, in effect, the original sync pulse has been replaced by a 10-volt pulse whose width is equal to that of the multivibrator push out pulse.

When an equalizing pulse appears in the input to Q40 and Q42 the action is similar to that previously described for a horizontal sync pulse, since the one-shot period is greater than the width of the equalizing pulse. Therefore, in the output of Q39, an equalizing pulse is replaced by a pushout pulse.

During the vertical sync interval, the action of the circuit is somewhat different. Serrated vertical sync consists of six wide pulses separated by narrow serrations. For purposes of this discussion each wide section will be referred to as a "vertical sync pulse." At the leading edge of each vertical sync pulse, both Q40 and Q41 conduct and Q39 becomes cut off. Q41 conducts only for the width of the pushout pulse. However, since the vertical sync pulse fed to Q40 is wider than the pushout pulse, Q40 continues to conduct, after Q41 becomes cut off, until the trailing edge of the vertical sync pulse. As a result, the output of Q39 reproduces normal serrated vertical sync.

The width of the pushout pulse (A, bottom, figure 13), which is equal to the one shot period of the multivibrator (A, top, figure 13), depends on the negative voltage to which timing capacitor C48 discharges during the period. This voltage is determined by the potential on the HN bus. The base of Q42 is connected to a voltage divider consisting of R134, R135 which goes from the HN bus to −20 volts. When the TR-4 is operating on 525 or 625-line standards the HN bus is at −20 volts, and therefore C48 discharges toward −20 volts. Under these conditions the one shot period is about 5.2 microseconds. On 405-line standards, the HN bus is grounded, and the capacitor discharges towards a voltage of approximately −7 volts. This increases the one-shot period to correspond with the greater width of horizontal sync. In either set of standards, the pulse is slightly wider than horizontal sync.

5. Noise Immunity Multivibrator

The noise immunity multivibrator (figure 14), removes noise (blanks during active scan) from the sync output of delay clipper Q39 and provides a sharp negative going edge to the clamp pulse generator, Q26, at the trailing edge of the modified sync. In addition, the multivibrator divides by two during the 9H vertical interval.

The noise immunity multivibrator consisting of Q36, Q38 is the one shot type whose unstable or one shot period is a very high percentage of the time between trigger pulses. Since the circuit can be triggered only during the relatively short stable period, the output remains constant during the unstable period regardless of the presence of noise in the input signal.

To make the transition period between the unstable and stable states as short as possible, the circuit includes an auxiliary transistor switch, Q37, that reduces the time constant in the capacitor charging circuit by a factor of 10 to 1.

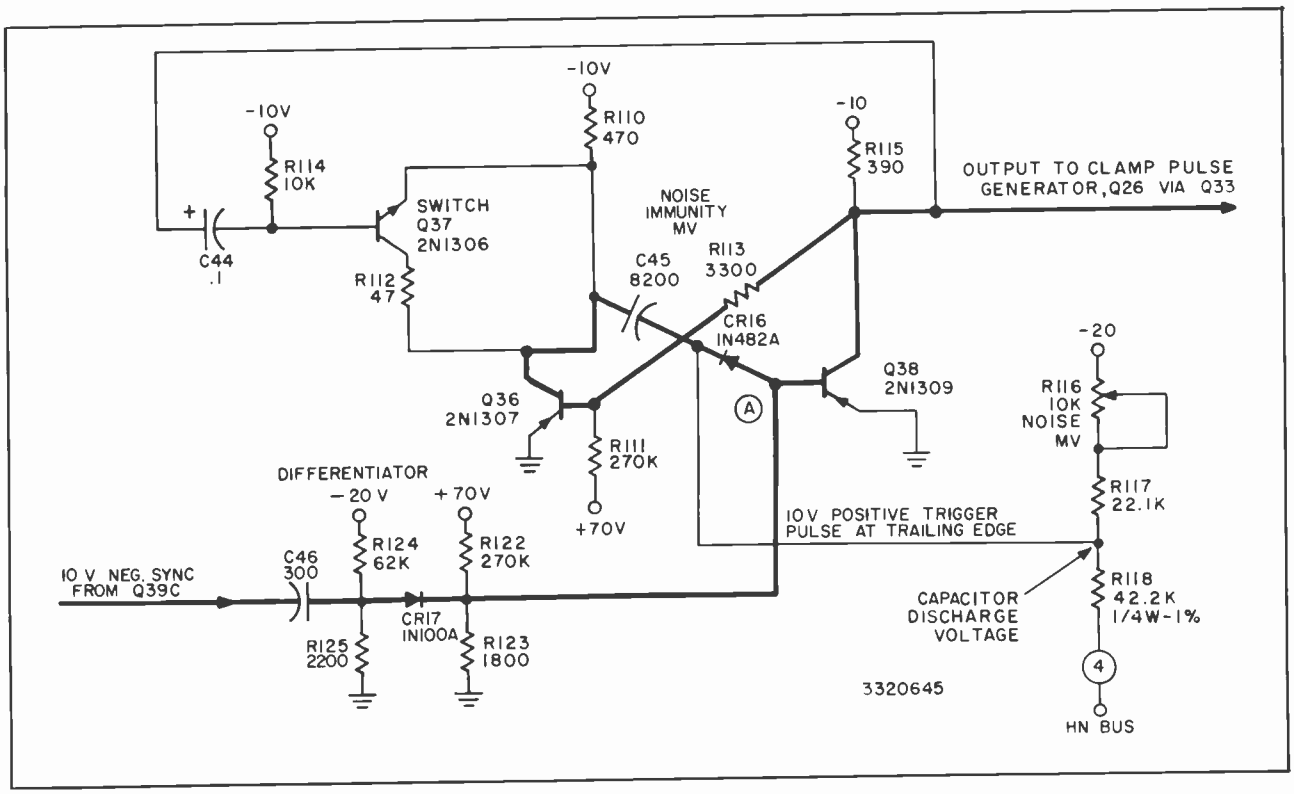
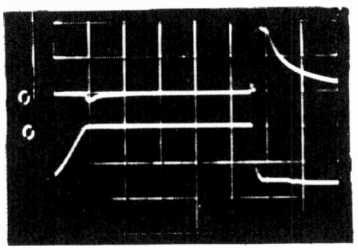


Figure 14—Noise Immunity Multivibrator Circuit



A. Top: Q38 base,
Bottom: Q38 collector,
(2 μs/cm, 5v/cm)

Figure 15—Typical Waveform, Noise Immunity Multivibrator Circuit

In the stable state Q36 is cut off and Q38 is conducting. This occurs because Q38 is biased on by the current withdrawn from its base through diode CR16 to voltage divider R118, R116 which runs from the HN bus to −20 volts. Under these conditions the collector, base, and emitter of Q38 are essentially at ground, the base of Q36 is about 0.9 volts, and the collector of Q36 is at −10 volts. This means that capacitor C45, between the collector of Q36 and the cathode of CR16, must be charged to −10 volts with respect to the Q38 base.

Triggering of the multivibrator is accomplished by applying the negative 10 volt modified sync from the collector of delay clipper Q39, through the differentiating network consisting of C46, R124, R125 to the base of Q38. Diode CR17 allows only the positive going portion of the differentiated sync pulse to reach the base of Q38 (A, figure 15). This pulse starts the one-shot period by cutting off Q38 and allowing Q36 to conduct. A 10 volt negative going edge coincident with the trailing edge of modified sync then appears at the collector of Q38, and triggers the clamp pulse generator, Q26. Because the one shot period is greater than half of a TV line, the multivibrator divides by two during the 9H interval of vertical blanking.

At the start of the unstable period, the collector and base of Q36 go essentially to ground. Since the charge on C45 cannot change instantly, +10 volts is applied to the cathode of diode CR16. At the end of the trigger pulse, the anode of CR16 goes to about +0.5 volts with respect to ground because it is returned to voltage divider R123, R122 connected between ground and +70 volts. Thus, since the cathode is at +10 volts the diode becomes cut off and disconnects the base of Q38 from C45. Therefore the leakage current of Q38 is prevented from affecting the time period of the one shot multivibrator.

During the unstable interval the 10 volt charge on C45 discharges to a voltage determined by voltage

divider R118, R116, which is connected between the HN bus and −20 volts. The rate of discharge, which determines the length of the unstable period, depends on the voltage at this point. This voltage depends on the adjustment of NOISE MV potentiometer, R116, and the potential of the HN bus.

When the TR-4 is on 525 or 625 line standards, the HN bus is at −20 volts, and R116 is adjusted so that the interval between the leading and trailing edges of the multivibrator pulse is approximately 55 microseconds. On 405 line standards the HN bus is grounded. This increases the width of the pulse to approximately 87 microseconds.

As soon as the charge on C45 reaches about 0.5 volts, diode CR16 conducts and connects the base of Q38 to the capacitor. When the voltage goes slightly below ground, Q38 starts to conduct and its collector rises from −10 volts to ground. The collector of Q38 is connected to the base of normally cut off transistor switch, Q37, through capacitor C44. When the collector of Q38 makes the transition from −10 to ground, a positive pulse passes through C44, which causes Q37 to saturate. Transistor Q37 then connects a 47 ohm resistor, R112, across R110, the 470 ohm collector resistor of Q36. This reduces the time constant of the charging path of timing capacitor C45 to about one-tenth of its normal value and allows C45 to charge to −10 volts very rapidly. Since the charging of C45 through the base of Q38 determines the minimum time allowed before the multivibrator can again be triggered, the very rapidly charging of C45 or the usually referred to "recovery time" is short, and the duty cycle can be made very high for improving noise immunity.

From the preceding analysis it can be seen that the output voltage on the collector of Q38 goes to −10 volts at the leading edge of the trigger pulse, which occurs slightly after the trailing edge of modified sync. The voltage remains at −10 volts, regardless of noise in the input sync, for the duration of the unstable interval (55 or 87 microseconds). At the end of the unstable period the voltage rises sharply to ground, and stays there until the arrival of the next trigger pulse (A, figure 15). The positive going edge of the output waveform has no effect on clamp generator Q26, since it is a normally conducting NPN transistor (figure 16). The negative going edge at the trailing edge of sync, however, cuts off Q26 and causes it to produce the clamp pulse.

6. Back Porch Clamp and Half-Level Clipper

The clamp pulse generator, Q26 (figure 16) is normally conducting since it is an NPN transistor with its emitter connected to −20 volts and its base returned

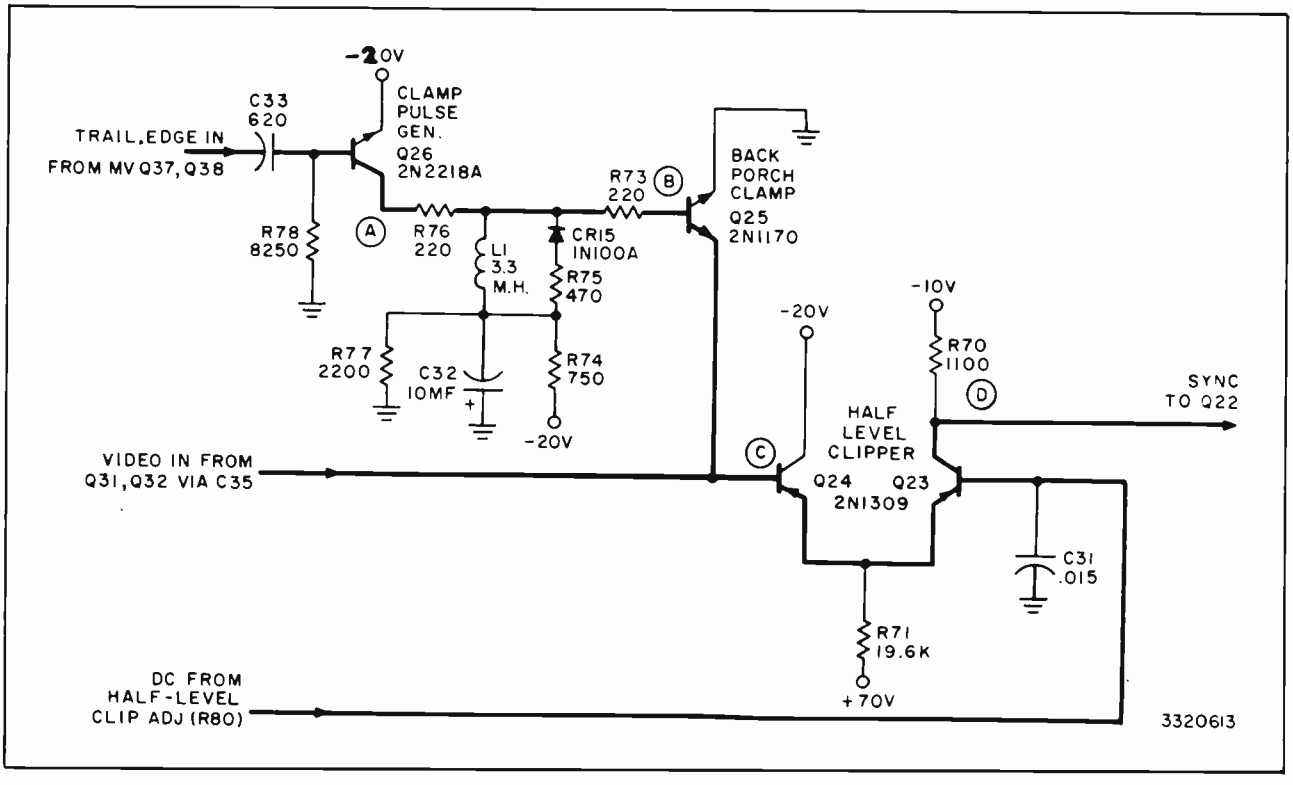
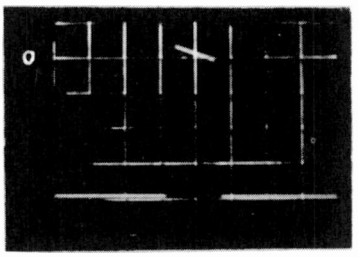
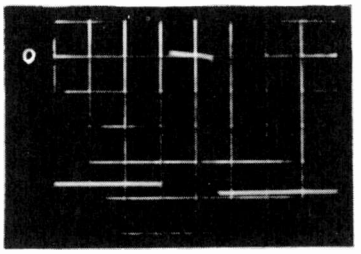


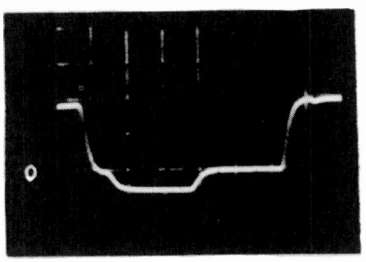
Figure 16—Clamp Pulse Generator, Back Porch Clamp and Half Level Clipper Circuits



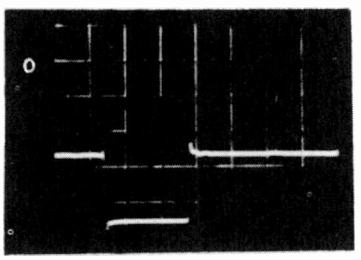
A. Q26 collector, 1 μs/cm, 5v/cm.



B. Q25 base, 1 μs/cm, 5v/cm.



C. Q24 base, 2 μs/cm, 5v/cm.



D. Q23 collector, 2 μs/cm, 2v/cm.

Figure 17—Typical Waveforms, Clamp Pulse Generator, Back Porch Clamp and Half Level Clipper Circuits

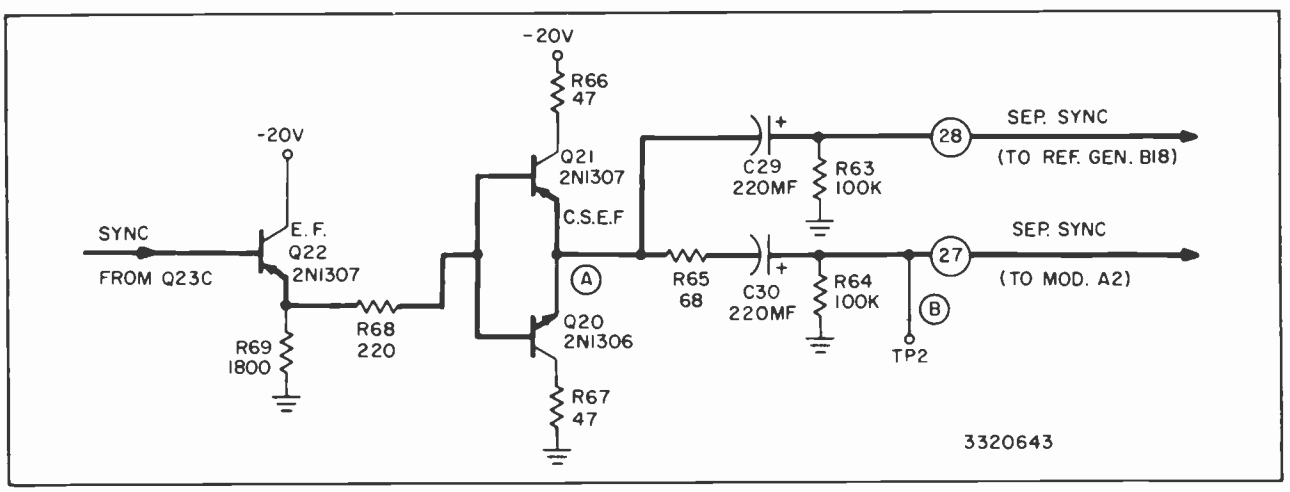
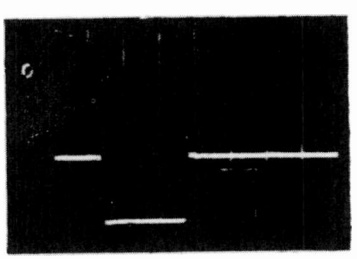
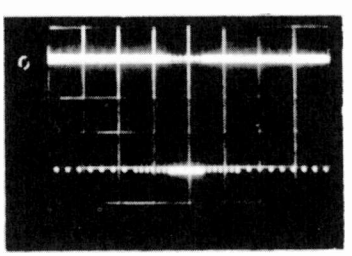


Figure 18—Sync Output Amplifier Circuit



A. Q20, Q21 emitter, 2 μs/cm, 2v/cm



B. TP2, 2 ms/cm, 1v/cm

Figure 19—Typical Waveforms, Sync Output Amplifier Circuit

to ground through R78. As previously mentioned, when the trailing edge of modified sync is applied to the noise immunity multivibrator, Q36, Q38, a sharp negative going 10 volt pulse is produced at the collector of Q38. This pulse is fed through C33 to the base of Q26, cutting off this transistor. The sudden transition from the conducting to the non-conducting state shock excites coil L1 in the collector circuit of Q26 and causes it to ring. However, a damping circuit consisting of diode CR15 and resistor R75 allows it to ring for only one positive going half cycle. This alternation produces a sharp, positive going pulse approximately 1.5 microseconds wide that constitutes the clamp pulse (A, figure 17).

The clamp pulse from Q26 is applied to the base of Q25 an NPN directional switch which serves as the back porch clamp (B, figure 17). One collector/emitter element of Q25 goes to ground, and the other goes to the base of Q24 in the half-level clipper circuit.

Transistor Q25 is normally cut off, since its base is returned to −20 volts through R73, CR15, R75 and R74. However, when the clamp pulse occurs, Q25 saturates and clamps the video signal at the base of Q24 to ground (C, figure 17). Transistors Q24 and Q23 form the half-level clipper, which is a differential clipper or "long-tailed pair." The emitters of these two transistors are tied together and connected through a large resistor (R71, 19.6K) to +70 volts.

A dc voltage equal to exactly one-half of the voltage between ground and the tip of the sync pulse is applied from the HALF LEVEL CLIP ADJ potentiometer, R80, (figure 10) in the half-level sensor to the base of Q23. Since Q23 is a PNP it can conduct only when its emitter is more positive than this voltage. Similarly, Q24, which is also a PNP, can conduct only when the voltage on its emitter is more positive than the video signal applied to its base. Because of the connection between the emitters of the two transistors, Q24 conducts when the video signal applied to its base is more negative than the dc voltage on the base of Q23, and Q23 is cut off during this period.

When the video level is more positive than the dc voltage, the action reverses and Q24 is cut off, while Q23 conducts. The resulting output of Q23 is a negative going sync pulse having exactly half the amplitude of the sync in the video signal, and a constant width, regardless of the video level (D, figure 17).

7. Sync Amplifier

The sync amplifier circuit (figure 18) is a complementary symmetry emitter follower consisting of Q20, Q21, which is driven by an emitter follower, Q22.

The clipped sync output from the collector of Q23 is direct coupled to the base of Q22. From the emitter of Q22, the signal is fed across R220 to the bases of Q20, Q21. The output of the C.S.E.F. (A, figure 19) drives two parallel output lines. The output on one line is fed through a sending-end termination, R65, and coupled through C30 to the Modulator (module A2). The other output is coupled through C29 and drives the line to the Reference Generator (module B18). The output of the former (B, figure 19) can be observed at test point TP2.

Adjustments

The sync separator adjustments involving R84 (SYNC TIP CLIP ADJ), R80 (HALF LEVEL CLIP ADJ) and R116 (NOISE MV) are critical and have been carefully made at the factory. Readjustment will be required only if the settings on these controls have been disturbed or if components affecting the adjustments have been replaced.

The adjustment procedure is in two sections. The first section is the *Performance Check* and this includes the adjustment of R84. The second section covers the adjustment of R80 and R116. When troubleshooting the sync separator stages, always go through the *Performance Check* procedure first; then proceed with the *Adjustment of R80 and R116,* if required.

Recommended Test Equipment

Dual Trace Oscilloscope, such as Tektronix 535A with CA plug-in amplifier.

Video attenuator box.

Source of composite monoscope signal.

3 volt negative bias source (battery or regulated dc source with adjustable output voltage).

.022 μf capacitor.

Performance Check

1. Remove the Video Input (module A1) from the TR-4. Disconnect the minus (input) side of capacitor C41 from the terminal. Using coaxial cable with alligator clips, connect an attenuator between this terminal and the minus side of C41.

2. Place the Video Input module in an extender and insert it in the TR-4.

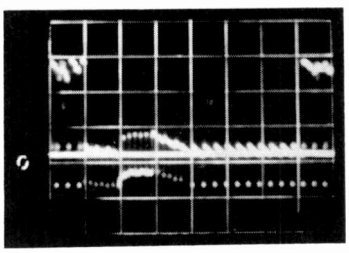
3. Place the TR-4 in STOP mode and on 525-line standards.

4. Apply a monoscope signal to the video input of the TR-4. Set the attenuator for zero attenuation. Press the DEMOD OUT button of the CRO and adjust the VIDEO LEVEL control on the Video Input

(module A1) for 1 volt peak-to-peak on the CRO. (With the video adjusted to this level, the amplitude of the video input at C41 should be approximately 2 volts.)

5. Adjust the attenuator to obtain .8 volt at C41.

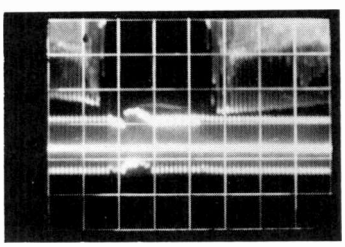
6. Set the oscilloscope for dc measurement and match both probes. Connect one probe to the base of Q47 and the other probe to the base of Q46. Observe the vertical interval on the base of Q47 at a vertical rate. Switch the oscilloscope to alternate. The dc line on the base of Q46 should be just below the black level of the lowest set of sync pulses, as shown in A,



A. Q47 base (Vert. Interval).

B. Q46 base (DC Line), (2 ms/cm, 1v/cm)

Figure 20—Sync Tip Clipper Check (Low Video Level)



A. Q47 base (Vert. Interval).

B. Q46 base (DC Line), (0.5 ms/cm, 2v/cm)

Figure 21—Sync Tip Clipper Check (Normal Video Level)

figure 20. If necessary adjust R84 (SYNC TIP CLIP ADJ) to obtain this result.

7. Restore the video level at C41 to 2 volts. The dc line on the base of Q46 should pass through approximately in the center of the sync pulses (figure 21).

8. Connect one oscilloscope probe to the base of Q24 and the other probe to the base of Q25. Adjust the sweep rate until two complete patterns are displayed, and then check the timing as shown in figure 22. Absence of the clamp pulse from the back porch of one of the two sync pulses indicates that the noise immunity multivibrator (Q36, Q37, Q38) is dividing by two. If this occurs check the adjustment of R116 (NOISE MV) as instructed in steps 6 and 7 under *Adjustment of R80, R116.*

a. If required switch to 405-line standards and adjust the oscilloscope until two complete patterns are displayed. The timing of the clamp pulse should meet the limits shown in figure 23. If the clamp pulse is absent, proceed as just instructed for the same condition on 525-line standards.

9. Switch to 525-line standards; switch the oscilloscope inputs to dc. Connect both probes to the junction of R88 and C35 and match the probes. Then connect one probe to the junction of C34 and Z1. The dc level at C34, Z1 should be the same as that of the sync tip at C35 and the back porch should be at ground.

10. Observe the output of the sync separator at TP2 at the horizontal rate and then at the vertical rate. The sync amplitude should be 3.2 to 3.4 volts. All equalizing pulses, vertical pulses and horizontal pulses must be present at normal amplitude.

Adjustment of R80, R116

1. Disconnect C35 from the junction of Q31 emitter and Q30 base. Also disconnect the lead from the junction of R72 and the base of Q24. Bypass the base of Q24 with the .022 μf capacitor. Connect the bias source to the junction of R88 and Z1 and adjust the bias to −3 volts.

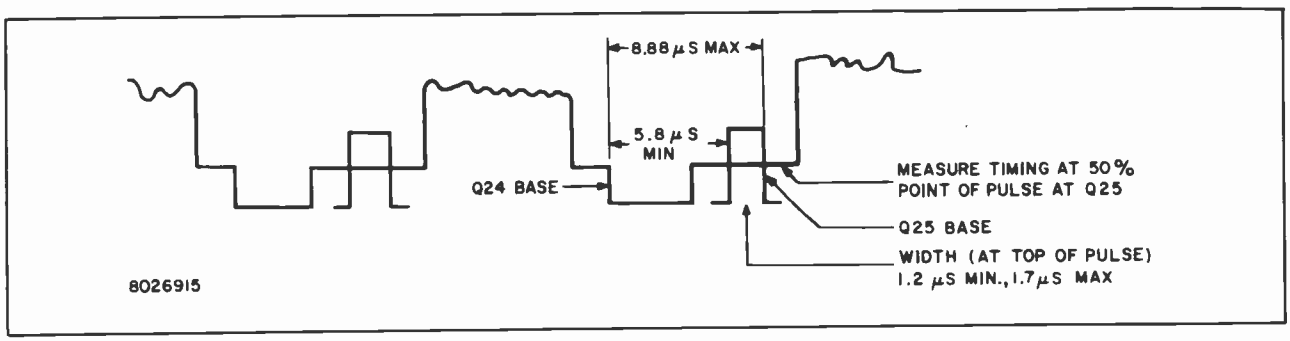


Figure 22—Timing of Clamp Pulse on Back Porch (525 Line Standards)

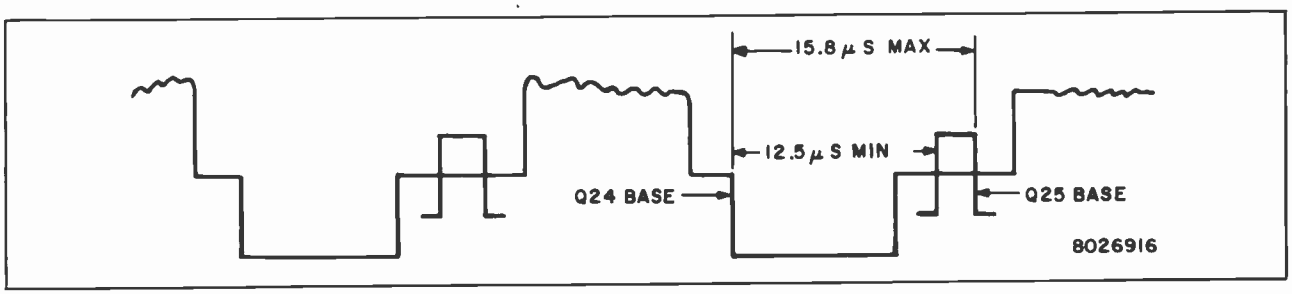
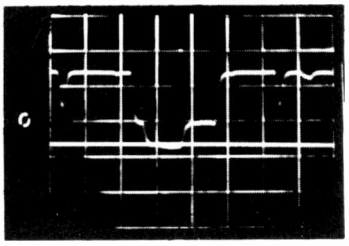


Figure 23—Timing of Clamp Pulse on Back Porch (405 Line Standards)

2. Adjust the video level at C41 to 2 volts.

3. Switch the oscilloscope inputs to dc and connect both probes to the junction of C35 and R88. Calibrate both probes to read the same with respect to ground. Connect one probe to the junction of C34 and Z1. The voltage at this point should be the same as the bias applied to C35 (see figure 24).



Top: Junction C34, Z1, 5v/cm,
Bottom: Junction R88, C35, 5v/cm.
(Sweep rates 5 μs/cm)

Figure 24—Sync Tip DC Level Check

4. Remove the probe from the junction of C35 and R88 and connect it to the arm of R80, the HALF LEVEL CLIP ADJ. Adjust R80 until the voltage is equal to half of the voltage at C34. (Measure both voltages with respect to ground.)

5. Remove the −3 volt bias supply. Remove the .022 μf capacitor and reconnect the lead to the junction of R72 and the base of Q24. Reconnect C35 to the junction of Q31 emitter and Q30 base.

6. Connect one probe to the collector of Q38 and the other to the base of Q47. Adjust R116 (NOISE MV) for a pulse width of 55 microseconds, as shown in figure 25.

7. If required switch to 405-line standards. The width of the pulse at the collector of Q38 should be 87 microseconds, as shown in figure 26. Compare the pulse with the horizontal sync at the base of Q47 to make certain the latter is not dividing by two. If division occurs readjust R116 slightly and recheck the pulse width on 525-line standards as instructed in step 6.

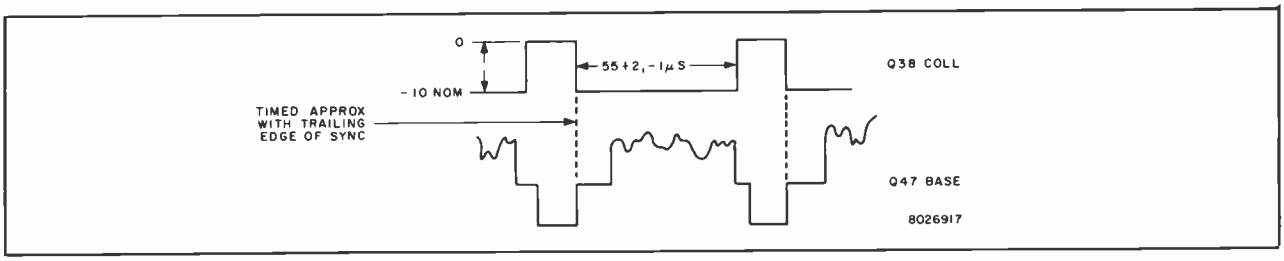


Figure 25—Noise Immunity Multivibrator Timing, R116 Adjusted for 525 Line Standards

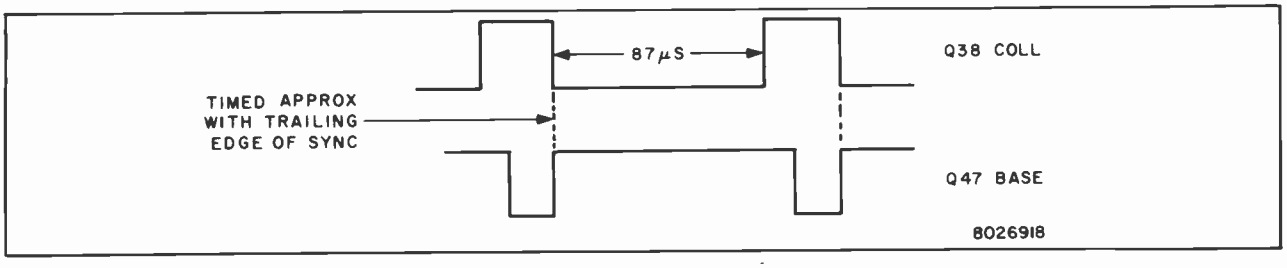


Figure 26—Noise Immunity Multivibrator Timing, R116 Adjusted for 405 Line Standards

Modulator (Module A2)

General

The Modulator generates a constant amplitude or frequency modulated signal whose deviation is a function of the amplitude variations of the video components in the composite signal. In this module the recording standard, monochrome or color, is selected. R-F Copy switching facilities are provided, enabling the output of another player/recorder to be fed through the appropriate circuits of the Modulator for re-recording.

As shown in block diagram, figure 27, video from the Video Input (module A1) is applied to an equalizer driver which is the input stage of the pre-emphasis circuit. Simultaneously with the selection of the desired standard, the appropriate pre-emphasis network is inserted in the circuit, the proper deviation and carrier frequency are established, and the appropriate sync tip metering components are chosen. The pre-emphasized signal is coupled through an emitter follower to a feedback amplifier and then through another emitter follower to the input amplifier stage of the modulator section.

The amplified video is clamped at sync tip by an adjustable dc reference voltage. The clamped video is fed through three emitter followers in cascade to two pairs of variable capacitance diodes. These diodes, when reverse biased, appear as capacitors, the amount of capacity being an inverse function of the bias. One pair of diodes is used in the tuned circuit of a high frequency oscillator to produce an output of 60 mc. The other pair is used in a relatively lower frequency oscillator to provide an output of 55.72 mc. Video and diode polarities are such that a white-going video transition causes a decrease in capacity of the pair of diodes associated with the high frequency oscillator (HFO), while increasing the capacity of the pair that tune the low frequency oscillator (LFO). Therefore, an increase in video brightness level increases the HFO frequency a corresponding amount, and simultaneously decreases the LFO frequency by the same amount. In effect, the two oscillators are driven in push-pull by the video components of the signal.

The oscillator outputs are heterodyned in a doubly balanced diode mixer that cancels the original HFO and LFO frequencies. At the output of the mixer appears only the modulation products or sum and difference frequencies. The output of the mixer is amplified and then fed to a low pass filter which eliminates all of the modulation products except the oscillator

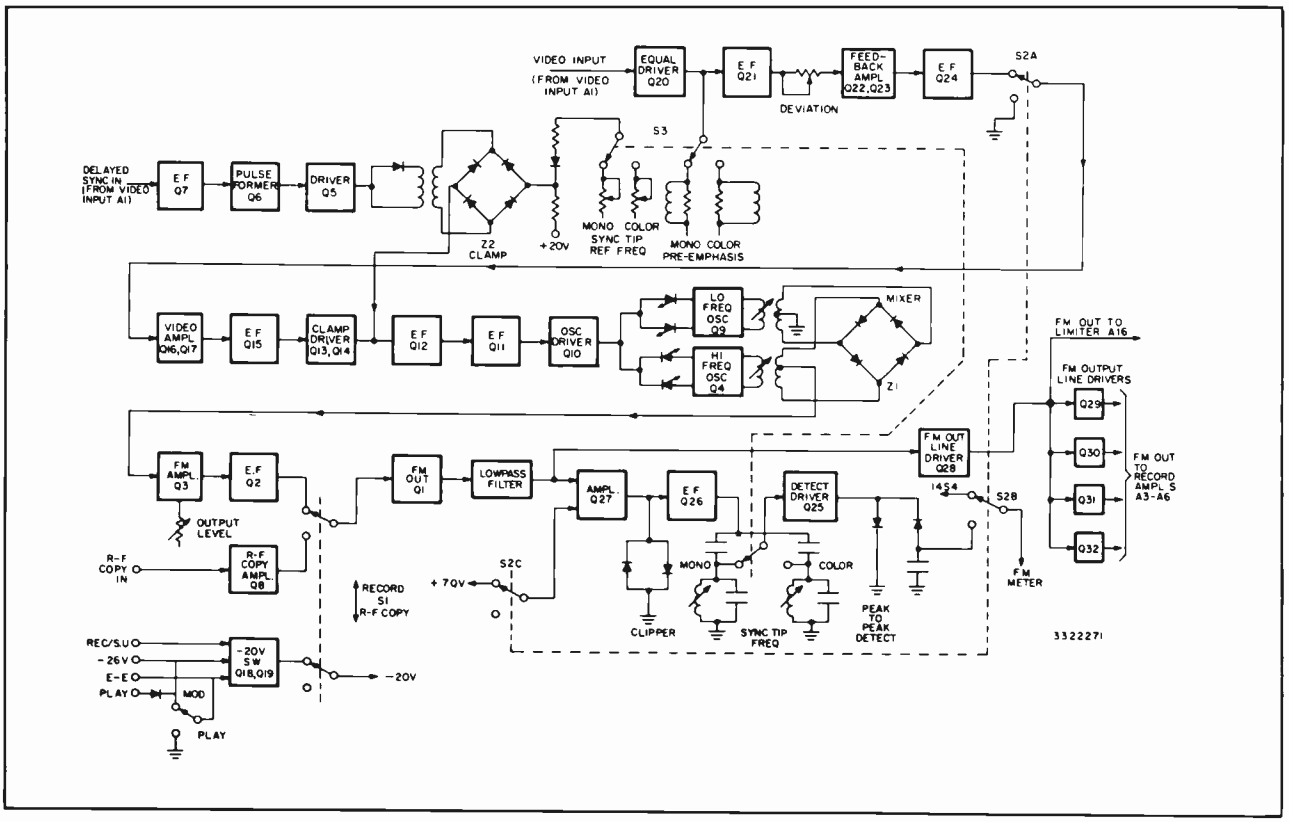


Figure 27—Block Diagram, Modulator Module

difference frequency and FM sidebands. The signal finally obtained has a frequency directly related to the instantaneous amplitude of the video input signal.

The reference for the FM signal is the sync tip frequency. This is determined by a dc potential to which sync is clamped, and this is adjusted primarily by a variable resistor appropriate to the standard chosen. The peak deviation from sync tip reference depends on peak video amplitude, and is adjusted by the DEVIATION control on the front panel of the Modulator module.

Clamp keying pulses are generated from the leading edges of separated sync from the Video Input (module A1).

An electronic switch is used to disable the frequency conversion circuits when the TR-4 is in the PLAY mode.

An R-F COPY facility is provided to enable making a dub of another recording without the necessity of demodulating the playback FM.

In STANDBY, WIND, and STOP modes, an internal switch can be used to disable the Modulator while allowing the noise originating in the heads to feeds through the playback circuits, providing a cursory check of these circuits.

A portion of the FM output is fed to a sync tip metering circuit. The meter signal is amplified then clipped and coupled through an emitter follower to either one of two tank circuits. The tank to which the signal is fed is determined by the standards selector switch. Each tank is tuned to a frequency that represents the tip of sync for the standard in use. The signal is then fed through a driver to a peak-to-peak detector to the SYNC TIP FREQ SET switch. When the switch is operated, the output of the peak-to-peak detector is fed to the FM LEVEL meter.

Circuit

For purposes of discussion, the circuitry of the Modulator is divided into the three sections listed below, each broadly classified according to function.

1. Pre-emphasis or equalization, including standards selection.

2. Modulation or frequency conversion, including R-F copy switching.

3. Sync tip frequency metering.

Pre-emphasis Section

Video from the Video Input (module A1) at a one volt level is coupled through C64 to the base of the equalizer driver, Q20, an emitter follower (figure 28). The output on the emitter is fed through the pre-emphasis equalizer appropriate to the standards selected, to the base of Q21 an emitter follower.

The desired FM standard is chosen by means of switch S3, a two-position rotary switch controlled from the front panel and designated MONO/COLOR. Separate components are used on each standard for the pre-emphasis networks, the sync tip frequency determining potentiometer and the sync tip frequency metering network. An additional feature of the group of components associated with color standards selection is that they are designed to accommodate the different line rates used on international standards. When a standard is chosen, switch S3 simultaneously inserts the appropriate pre-emphasis network, adjusts for proper deviation and carrier frequency, and selects the appropriate sync tip frequency metering network.

An inductor is used as a reactive shunt element in the equalizer network to boost the high frequency end of the pass band. Since the reactance of an inductor is directly proportional to frequency, the reactance decreases at low frequencies, and the shunting effect of the inductor results in a relatively high loss through the equalizer network. At higher frequencies the reactance of the inductor increases, therefore transmission through the equalizer will be greater. In addition to providing frequency-selective attenuation, each equalizer network introduces flat attenuation, the amount of which depends upon the deviation of the standard used.

The pre-emphasized output on the emitter of Q21 is coupled through the DEVIATION potentiometer, R95, and C66 to the base of Q22. This transistor together with Q23 forms a feedback amplifier where the signal level lost in the equalizer is restored by an amount sufficient to drive the next stage, Q24, an emitter follower. The DEVIATION control (a screwdriver adjustment on the front panel) is used to set the level of video which is subsequently fed to the modulator circuits. The amplitude of this signal determines the deviation or carrier swing of the frequency modulated signal generated in the modulator section.

Direct coupling between the collector of Q23 and the base of Q24 maintains the frequency response at the low end and stabilizes the dc conditions. Emitter follower Q24 minimizes loading on the collector of Q23.

From the emitter of Q24 the signal is coupled through C68 and R130 and fed via the closed contacts of the *A* section of switch S2 to Q17, the input of the modulator section. (The function of this switch is covered later in the discussion of the *Sync Tip Frequency Metering Circuit.)*

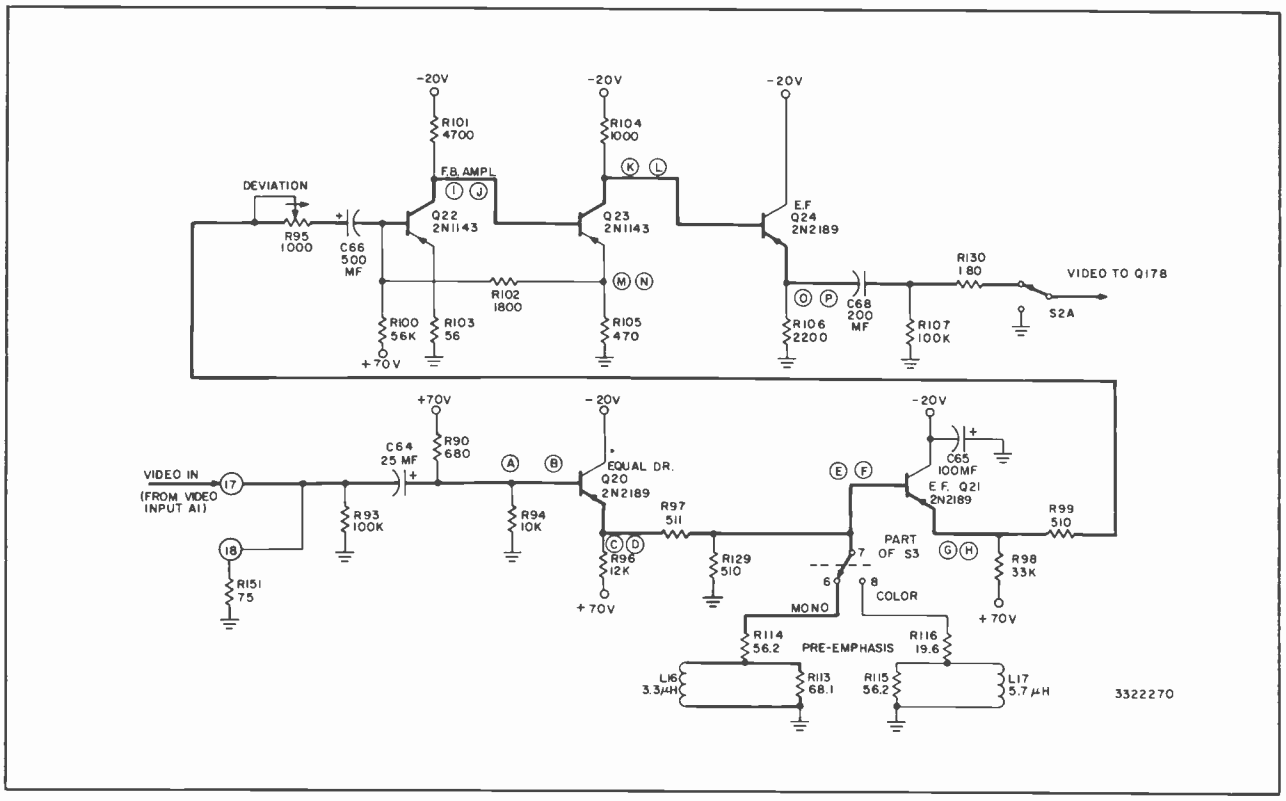
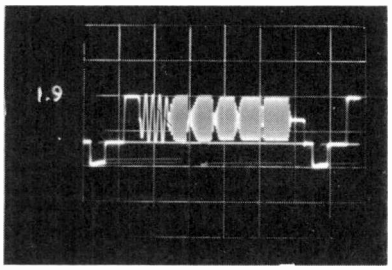
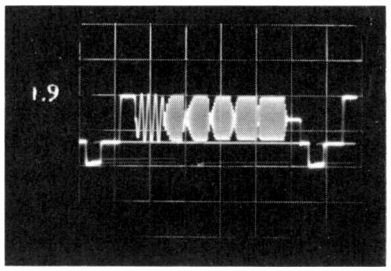


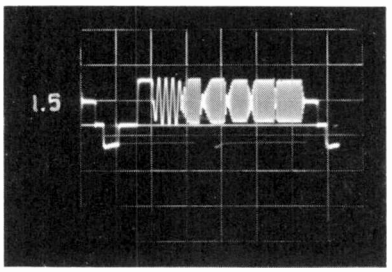
Figure 28—Equalization, Feedback Amplifier and Emitter Follower Circuits (Pre-Emphasis Section)



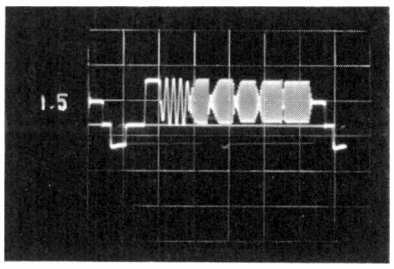
A. Q20 base, 10 μs/cm, .5v/cm, mono



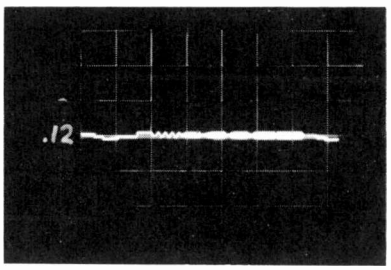
B. Q20 base, 10 μs/cm, .5v/cm, color



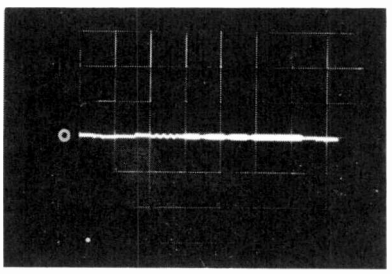
C. Q20 emitter, 10 μs/cm, .5v/cm, mono



D. Q20 emitter, 10 μs/cm, .5v/cm, color



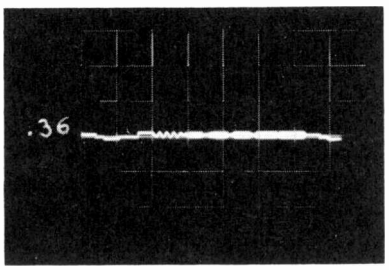
E. Q21 base, 10 μs/cm, .5v/cm, mono



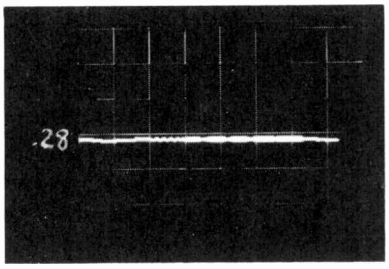
F. Q21 base, 10 μs/cm, .5v/cm, color

NOTE: The frequency increments of the multiburst signal spectrum are 0.5 mc, 1.5 mc, 2.5 mc, 3.6 mc, 4.0 mc, and 5.0 mc.

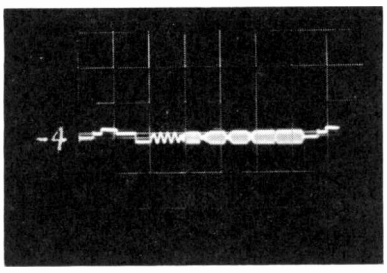
Figure 29—Typical Waveforms, Equalization, Feedback Amplifier and Emitter Follower Circuits (Pre-Emphasis Section)



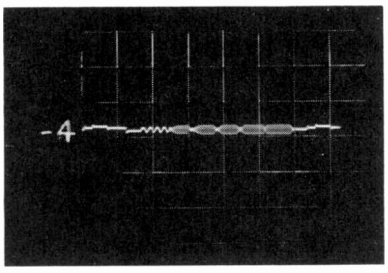
G. Q21 emitter, 10 μs/cm, .5v/cm, mono



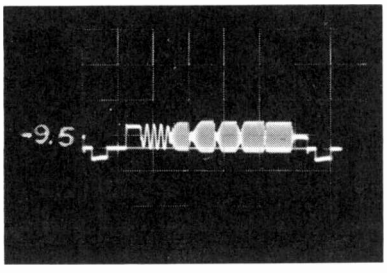
H. Q21 emitter, 10 μs/cm, .5v/cm, color



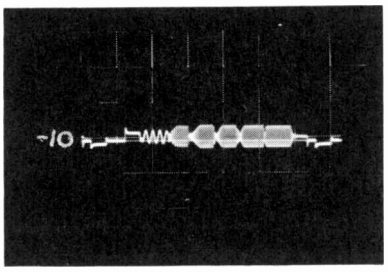
I. Q22 collector, 10 μs/cm, .5v/cm, mono



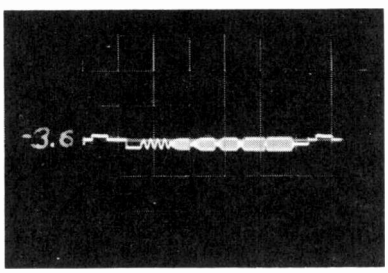
J. Q22 collector, 10 μs/cm, .5v/cm, color



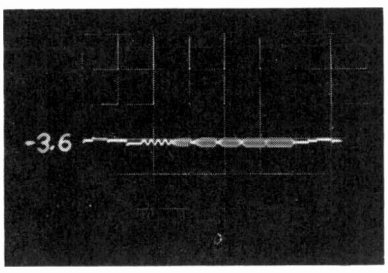
K. Q23 collector, 10 μs/cm, .5v/cm, mono



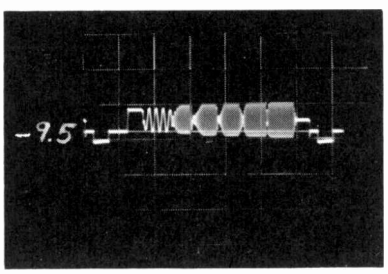
L. Q23 collector, 10 μs/cm, .5v/cm, color



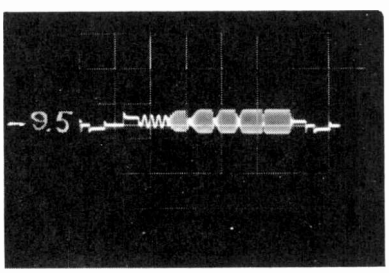
M. Q23 emitter, 10 μs/cm, .5v/cm, mono



N. Q23 emitter, 10 μs/cm, .5v/cm, color



O. Q24 emitter, 10 μs/cm, .5v/cm, mono



P. Q24 emitter, 10 μs/cm, .5v/cm, color

Figure 29—(Continued)

Modulator Section

1. Video Amplifiers, Clamp Drivers and HI and LO Frequency Oscillator Driver

As shown in figure 30, pre-emphasized video is fed to the base of Q17, an emitter follower. The level of the signal at this point is approximately .2 volt per megacycle of FM deviation. Thus the video amplitude at the base of Q17 will be about .5 volt when a standard monochrome signal is recorded with 2.5 mc deviation. From the emitter of Q17 the signal is coupled through C53 and R72 to the emitter of Q16, a common base amplifier. Together, these two transistors form an emitter coupled video amplifier stage. With this type of circuit the amplitude of the input signal is increased without polarity inversion.

The gain of this stage is due primarily to ratio of R71 over R72. The output of Q17 causes current flow

in coupling resistor R72 in accordance with the applied video. Because of the low input impedance of the common base amplifier, nearly all of the signal current in R72 passes through the emitter of Q16 and into the collector circuit. This causes a voltage drop across R71, the load resistor in the collector of Q16. Although the current flow in R71 and R72 is virtually the same, the resistance of R71 is greater than that of R72, therefore, the output signal voltage developed across the collector load, R71, will be much higher than the input signal voltage. Maximum voltage gain of this circuit would be 15, the ratio of R71 over R72, but normal losses reduce the gain to approximately 10.

D-C bias conditions in Q16 and Q17 are established by R70 and R75, respectively, which in conjunction with the −20 volts and grounded base returns result in 5 ma of collector current. Dissipation in Q17 is limited by R74 and C52, with the latter also serving as the collector decoupling capacitor.

Shunt peaking is the method used for high frequency compensation in the video amplifier. This is furnished by L12, a variable peaking coil in series with the collector load of Q16. The video amplifier is adjusted for flat response at the factory, therefore L12 should not be adjusted in the course of routine maintenance.

To minimize loading on the collector of Q16, the output is coupled by an emitter follower, Q15, to the succeeding stage, Q13, Q14, the clamp video drivers.

The clamp video drivers, Q13, Q14, are emitter followers connected to form a complementary-symmetry amplifier, the output of which drives the clamp coupling capacitor, C48. A dc reference voltage which clamps the tip of sync is added to the video signal at the output side of C48. The dc reference voltage is interposed in the signal by means of the clamp quad Z2, which is switched on for a short period during the horizontal sync interval.

The complementary-symmetry arrangement enables the clamp coupling capacitor, C48, to quickly follow sudden changes in potential caused by errors in black level during the horizontal sync interval. Errors typically result from sudden brightness changes in pic-

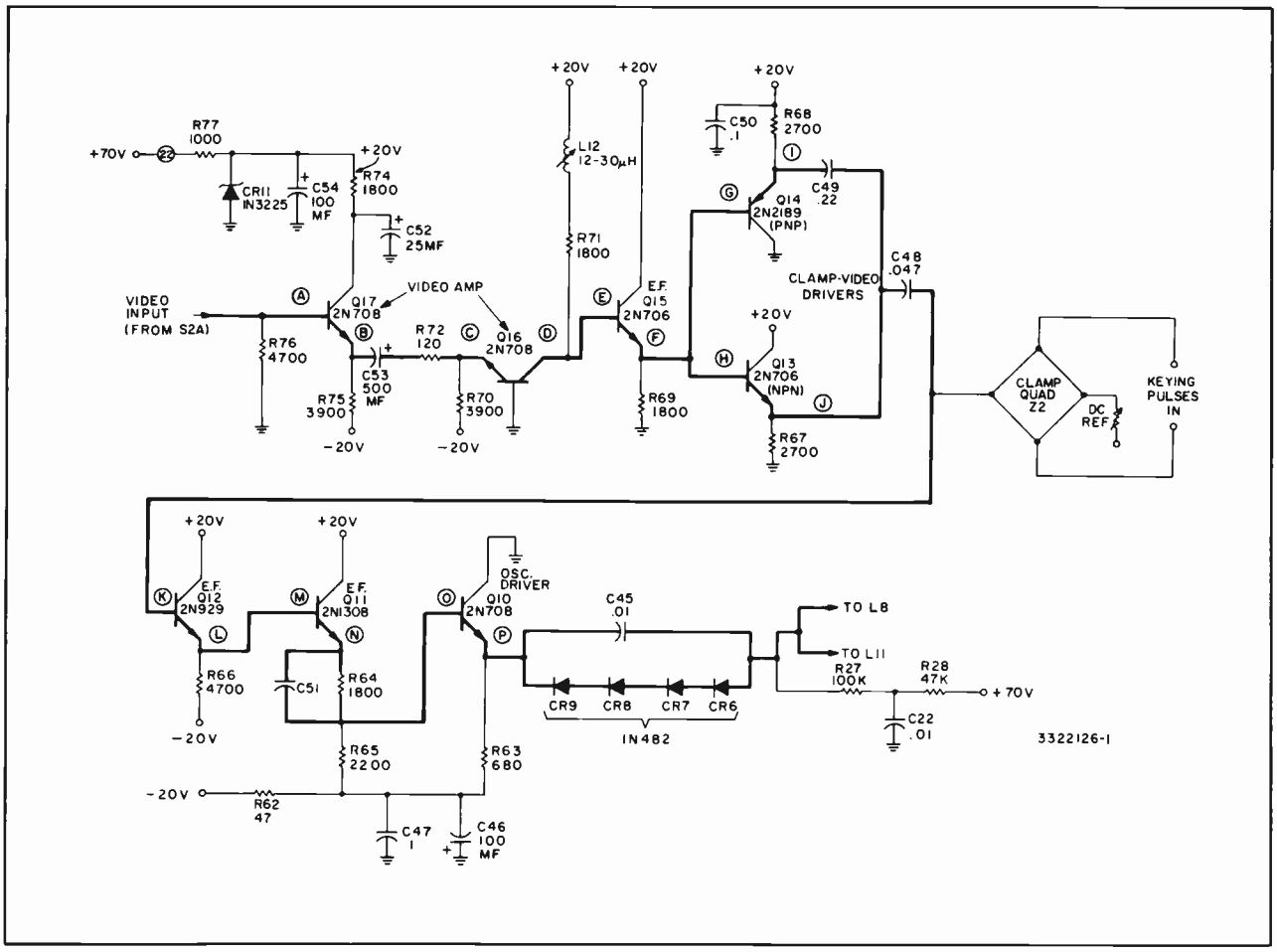
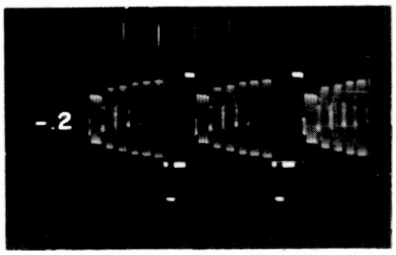
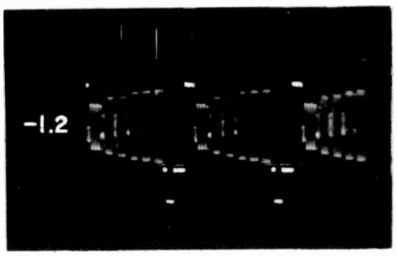


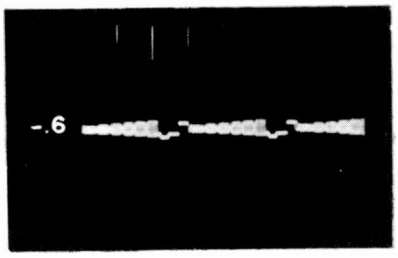
Figure 30—Video Amplifiers, Clamp Video Drivers and Oscillator Driver Circuits



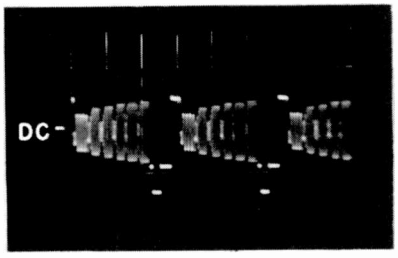
A. Q17 base, 20 μs/cm, .1v/cm.



B. Q17 emitter, 20 μs/cm, .1v/cm.



C. Q16 emitter, 20 μs/cm, .05v/cm.



20 μs/cm, .2v/cm.

This waveform is typical of points listed in chart.

KEY	LOCATION	AC AXIS
D	Q16C	+10.2v
E	Q15B	+10.2v
F	Q15E	+ 9.6v
G	Q14B	+ 9.6v
H	Q13B	+ 9.6v
I	Q14E	+ 9.9v
J	Q13E	+ 9.0v
K	Q12B	+ 0.02v
L	Q12E	− 0.58v
M	Q11B	− 0.58v
N	Q11E	− 0.66v
O	Q10B	− 8.4v
P	Q10E	− 9.1v

Figure 31—Typical Waveforms, Video Amplifiers, Clamp Video Drivers and Oscillator Driver Circuits

ture content, switching disturbances, or spurious low frequency interference. Since one transistor is an NPN and the other a PNP, a spurious surge will have an equal but opposite effect on each transistor. One will be driven into saturation while the other goes to cut-off as C48 charges or discharges, as required, through the clamp diodes in order to maintain the sync tip at the dc reference level.

Under normal signal conditions, Q13 and Q14, in effect, operate in parallel with the output on their emitters following in phase the positive and negative signal excursions. By virtue of the direct coupling existing between the collector of Q16 and the bases of Q13 and Q14, a +10 volt bias is supplied to the bases by the voltage divider formed by R69 and R71.

A quiescent current of approximately 3 ma flows through Q13 and Q14. This is obtained in Q13 by returning the emitter to ground through R67. And similarly in Q14 by placing R68 in series with the emitter to the +20 volt supply. This idling current eliminates crossover distortion that is otherwise characteristic of a complementary-symmetry emitter follower circuit. Coupling capacitor C49 provides isolation between the two emitters, thus preventing small differences in dc potential from upsetting the quiescent bias conditions.

After being clamped, the video is fed to the base of Q12, an emitter follower. The level of the video at this point is higher than that subsequently required for proper deviation, in order to lessen the effects of unbalance in the clamp quad diodes. Transistor Q12 along with the following two emitter followers, Q11 and Q10, form a direct coupled cascade amplifier. The purpose of the three cascaded emitter followers is to reduce loading on the clamp coupling capacitor, C48, and to provide a low impedance drive source for the variable capacitance diodes. (The latter are in the tank circuits of the high and low frequency oscillators, Q4 and Q9, respectively.) An attenuator consisting of R64 and R65 in the emitter of Q11 reduces the video to the level necessary for proper deviation. Capacitor C51 in parallel with R64 boosts the high frequency response about 1 db at 4 mc. The amplitude of the video output at the emitter of Q10 is approximately 1.2 volts per megacycle of deviation, or 3 volts for a standard monochrome signal of 2.5 mc.

The positive dc operating voltage (+20 volts) is developed across Zener diode CR11, which in conjunction with R77 forms a voltage divider across the +70 volt bus. Diode CR11 serves as a shunt-connected regulator.

2. High and Low Frequency Oscillators

From the emitter of Q10, the signal is coupled through C45 and CR6-CR9 to two pairs of variable capacitance diodes, CR1, CR2 in the tank circuit of the high frequency oscillator, Q4, and CR4, CR5 in the tank circuit of the high frequency oscillator, Q9 (figure 32). The operation of both oscillators is the same except that the reactance of each pair of variable capacitance diodes varies in opposite directions to the applied video signal.

The low frequency oscillator, Q9 is connected in a Colpitts configuration. A resonant circuit consisting of L10 in parallel with CR4, CR5 is ac coupled from the collector to the base. The feedback voltage is developed across the voltage divider formed by C40 and C41, the amount of feedback being determined by C41. DC bias is established by emitter resistor R55, and base bias by R53 and R54. The dc operating voltage is supplied to this stage from the −20 volt switched bus through rf choke L9 to the emitter return. Blocking capacitors C42 and C43 isolate the fixed bias on the variable capacitance diodes from ground.

Bias for CR4 and CR5 is supplied from two sources, one fixed, the other variable. The fixed source is the voltage divider consisting of R58 and R59 which is returned to +20 volts. The bias developed across this divider is a constant positive dc potential which is fed to the cathodes of CR4 and CR5 through isolation resistors R56 and R57. The variable bias source is the video drive which is coupled from Q10 through CR6-CR9 and fed through r-f choke L11 to the anodes of CR4 and CR5. This bias is comprised of two components, one being the video itself and the other a negative dc potential that is derived from the adjustable reference potential to which sync is clamped.

Diodes CR4 and CR5 remain reverse biased at all times. In conjunction with L10, they tune the low frequency oscillator, Q9, by exhibiting a varying reactance that is determined by the instantaneous value of the applied video signal. The reactance characteristic of the diodes is such that an increase in reverse bias causes a decrease in capacity, thus raising the output frequency of the ocillator. Since sync is the most negative part of the video signal, the oscillator frequency

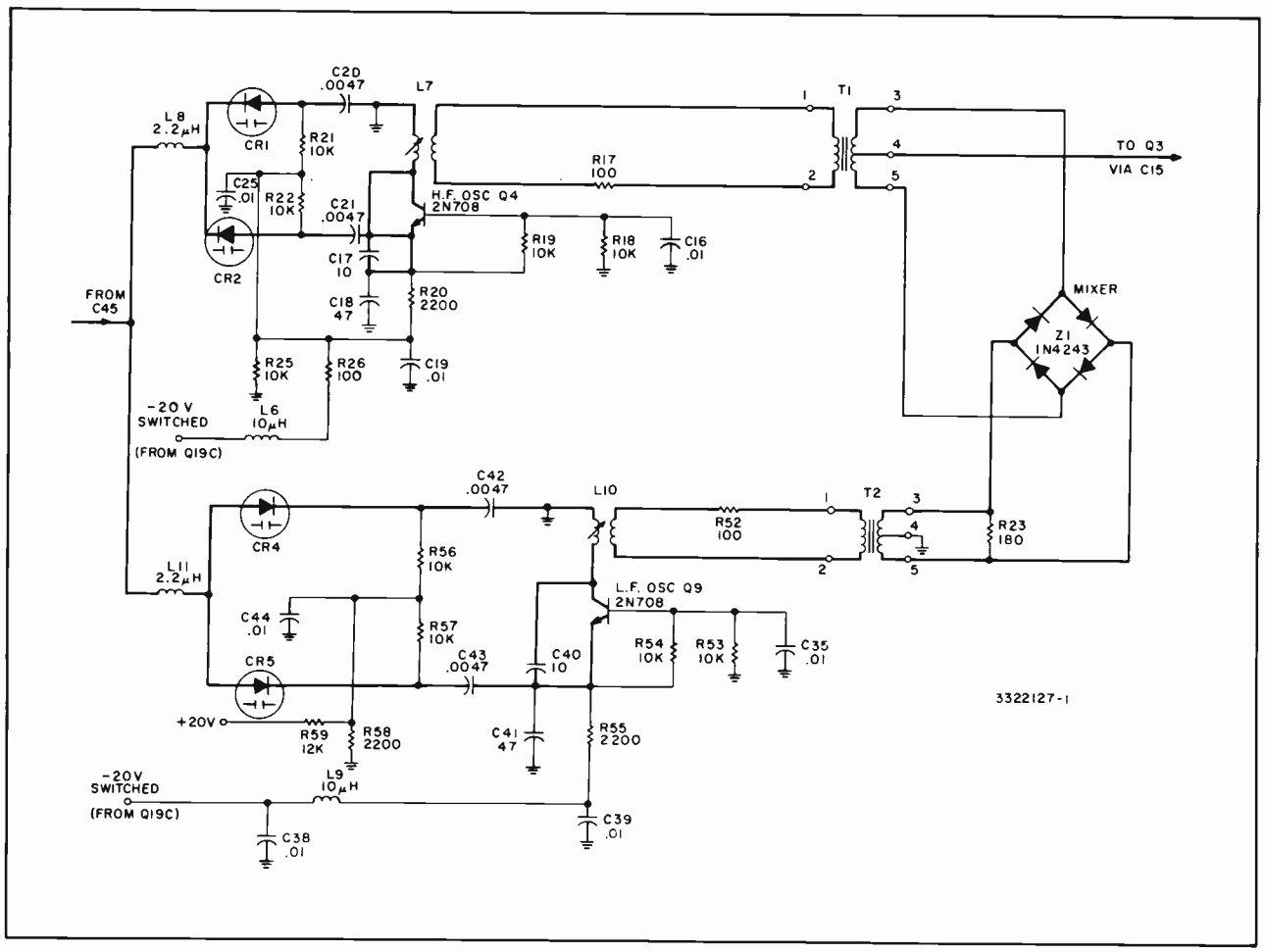


Figure 32—High and Low Frequency Oscillators and Quad Mixer Circuits

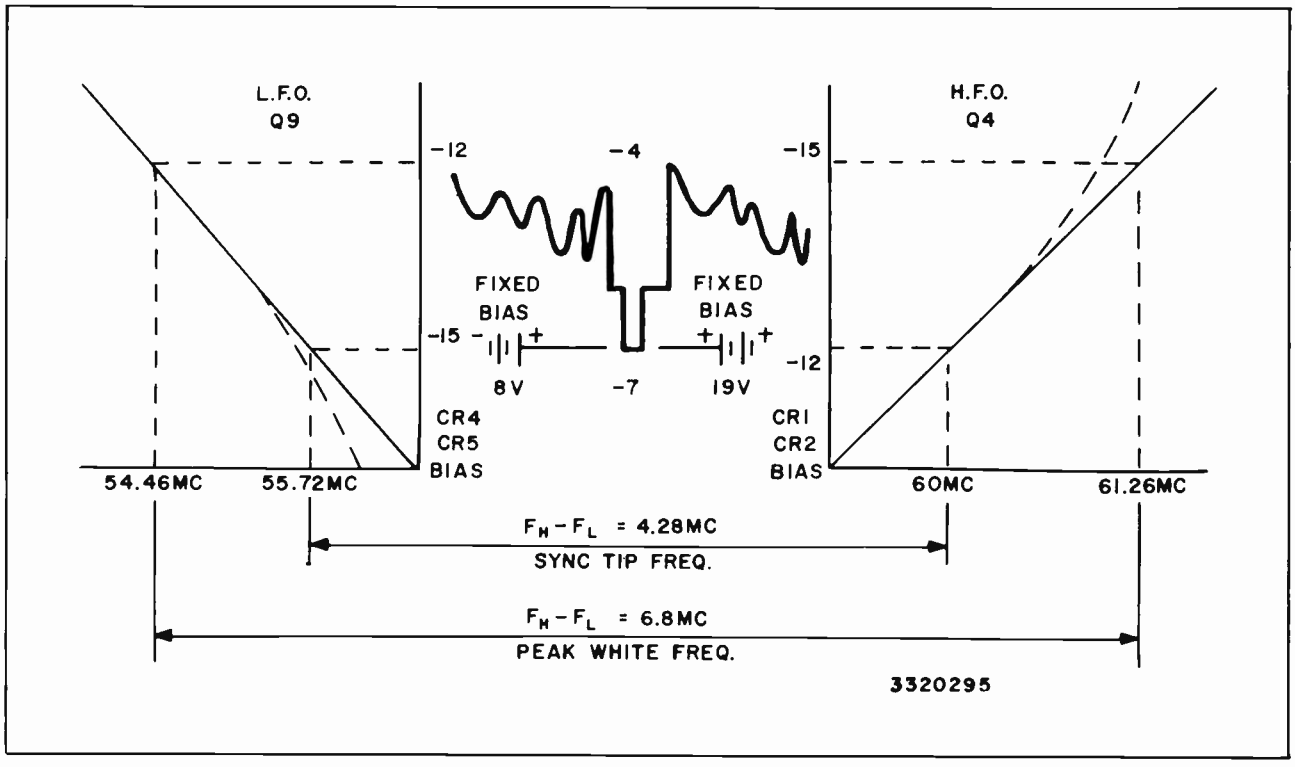


Figure 33—Modulation Transfer Characteristic

will be highest during this portion of the picture, becoming lower as the signal swings toward the more positive, white region.

The same video signal is simultaneously applied through r-f choke L8 to the variable capacitance diodes, CR1 and CR2, of the high frequency oscillator Q4. However, in constrast to the low frequency oscillator, the signal is fed to the cathodes of CR1 and CR2, and a fixed high negative bias is fed to the anodes through isolation resistors R21 and R22. The fixed bias is developed across the voltage divider formed by R25 and R26, which is returned to the −20 volts switched bus.

The output of the high frequency oscillator, as opposed to that of the low frequency oscillator, is lower in frequency during the sync interval, becoming higher as the video signal swings towards the more positive white (higher negative bias) region. As shown in figure 33, the video signal in its excursion from peak white to sync tip modulates the two oscillators in opposite directions, i.e., as the frequency of one oscillator increases, the frequency of the other decreases. The output frequencies diverge during white-going video transitions and converge during black-going transitions. The difference between the two oscillators is extracted by the mixer (as described later), resulting in the FM signal that is ultimately recorded.

The diode bias and oscillator frequencies typical of standard monochrome operation, which are depicted graphically in figure 33, are not exactly representative of the modulator, in that they do not show the curvature characteristic of the actual circuit. This is of no practical significance, however, because the push-pull modulation of the oscillator tends to cancel nonlinearity over the entire range of operation.

As noted earlier, the variable bias applied to the variable capacitance diodes, in the tank circuit of the oscillators, consists of a video component and a negative dc component. The source of the video component is, of course, the video input signal. Not so obvious is the origin of the dc component; therefore, the next part of this discussion will cover the manner in which the dc potential is obtained and its effect on the output frequency of the oscillators.

3. Variable DC Bias

The dc potential depends upon the sync tip reference, and is available as the CLAMP BIAS (TP-2) which is passed by the clamp quad, Z2 (figure 34). The clamp bias, or reference voltage, is determined by a voltage divider between −20 volts and +20 volts. The divider is comprised of R29, Zener diode CR10, R31 and potentiometer R91 or potentiometer R92. The two potentiometers are part of the standards selector switch (S3) circuit. Both are front panel screw-

driver adjustments; R91 is designated MONO FREQ SYNC TIP ADJ and R92 is designated COLOR FREQ SYNC TIP ADJ. These two controls are used to set the dc level that ultimately determines the frequency of the sync tip on monochrome or color standards.

Adjusting either R91 or R92 causes a shift in the respective clamp reference voltage that is transferred to the variable capacitance diodes. The resulting change in dc bias causes a change in the reactance of the diodes. This, in turn, produces a corresponding frequency change in that portion of the modulator output frequency that represents the sync tip region (figure 36). Since all other frequency components of the video waveform occupy various levels that bear a fixed relation to sync, the frequencies represented by these levels will also be displaced to the same degree as sync.

A similar change in output frequency can be produced by tuning coils L7 and L10 in the collector circuits of the high and low frequency oscillators, respectively. These coils, however, are not intended as operational controls, and they should not be adjusted during set-up or routine maintenance.

Thus, in the modulation process as described here, deviation depends on the amplitude of the video signal fed into the Modulator, and carrier frequency is determined by a dc potential established by means of the monochrome and color frequency sync tip adjustment potentiometers.

4. Sync Tip Clamping

The purpose of the clamp pulse former and sync tip clamp circuits (figure 34) is to provide a suitable keying pulse to turn on diode quad Z2, thus allowing the reference clamp bias to be inserted in the sync pulse.

Separated sync at 4 volts peak-to-peak from the Video Input (module A1) is coupled through C32 to the base of Q7, an emitter follower. Transistor Q7 is biased with base bias resistors R41, R43 and emitter resistor R42. A reproduction of sync, but from a low impedance source, appears at the emitter of Q7. The pulse former, Q6, is normally saturated because of the high positive base current resulting from the −20 volts emitter potential and the grounded base return resistor, R40. Under these conditions the collector potential of Q6 is also approximately −20 volts.

When a sync or an equalizing pulse occurs at the emitter of Q7, the negative-going leading edge is coupled through C31 to the base of Q6, cutting off Q6 and permitting the collector potential to move towards ground. Immediately following the negative-going excursion of the pulse, the base of Q6 begins to return to ground, as C31 charges through R40. The time constant of C31, R40 is such that the base of Q6 approaches ground in about 1.4 microseconds. When the potential on the base becomes sufficiently close to ground Q6 saturates and the collector goes to approximately −20 volts.

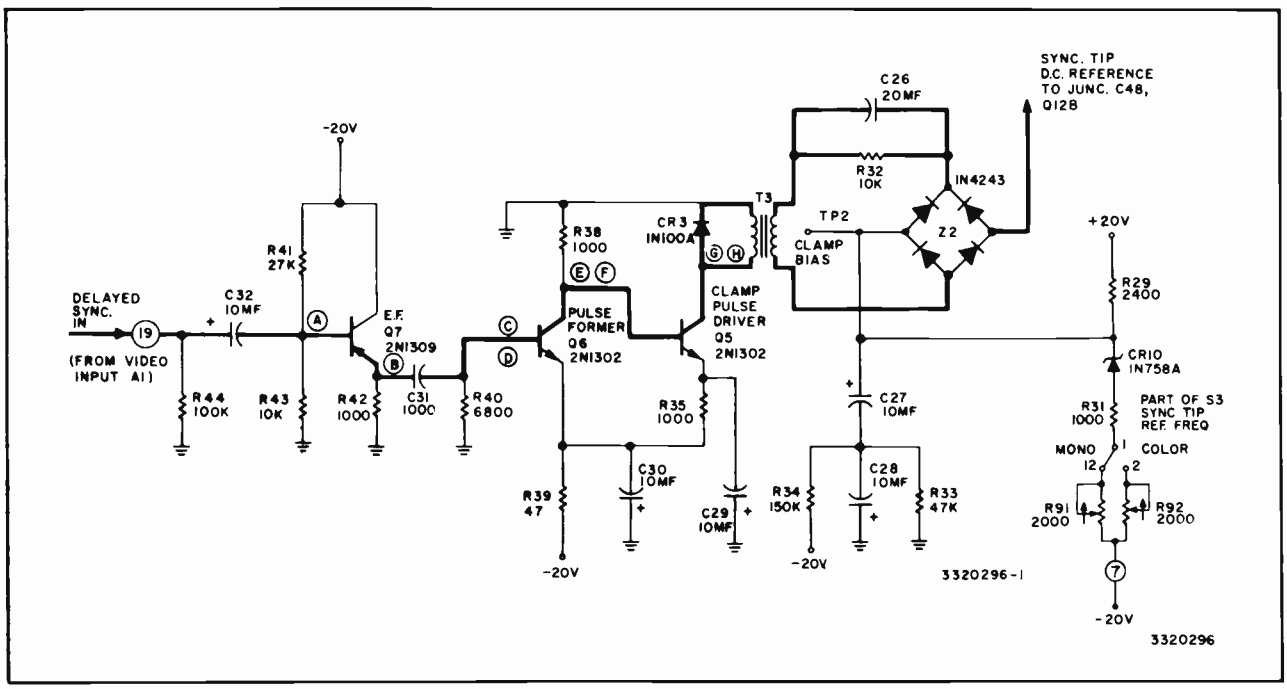
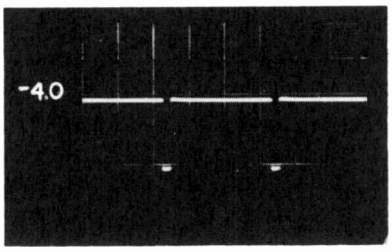
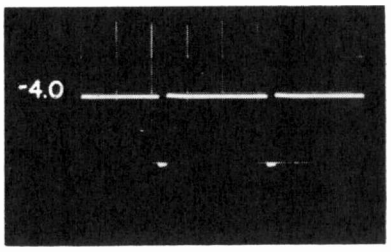


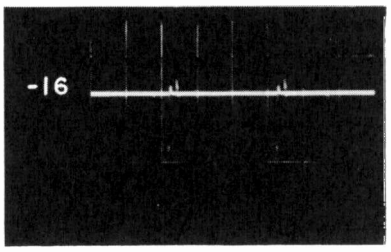
Figure 34—Pulse Former and Sync Tip Clamp Circuits



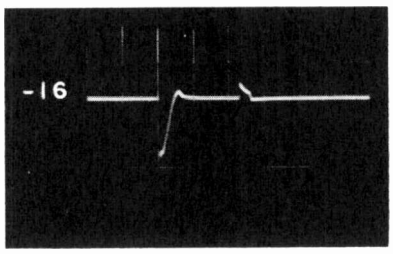
A. Q7 base, 20 μs/cm, 2v/cm.



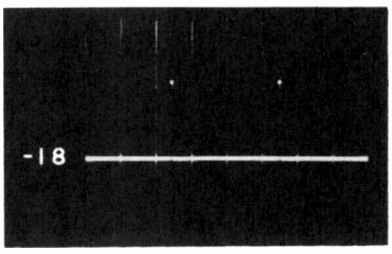
B. Q7 emitter, 20 μs/cm, 2v/cm.



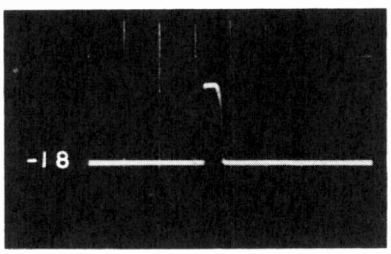
C. Q6 base, 20 μs/cm, 1v/cm.



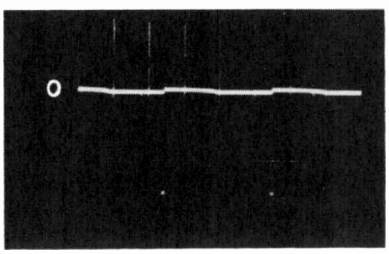
D. Q6 base, 2 μs/cm, 1v/cm.



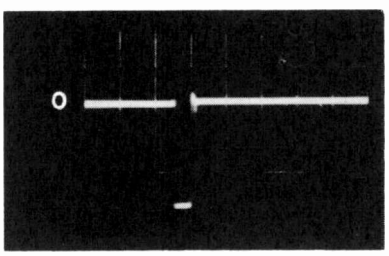
E. Q6 collector/Q5 base, 20 μs/cm, 2v/cm.



F. Q6 collector/Q5 base, 2 μs/cm, 2v/cm.



G. Q5 collector, 20 μs/cm, 5v/cm.



H. Q5 collector, 2 μs/cm, 5v/cm.

Figure 35—Typical Waveforms, Pulse Former and Sync Tip Clamp Circuits

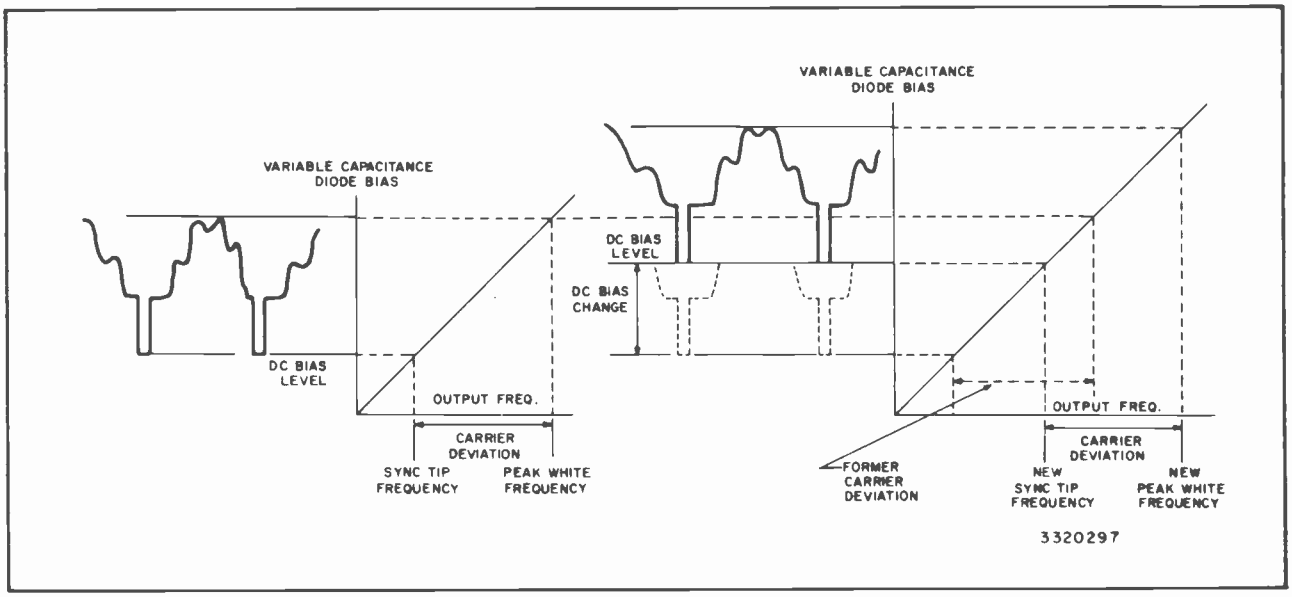


Figure 36—Effect of DC Bias on Carrier Frequency

The base of Q5 is direct coupled to the collector of Q6. Resistor R38 serves as the collector load for Q6 and as the base bias resistor for Q5.

Transistor Q5 is cut off during the picture interval, which is the period that Q6 is saturated with its collector at −20 volts. With Q5 cut off, no current flows in the primary of T3.

During the 1.4 microsecond interval following the negative going transition of the leading edge of sync (when Q6 is cut off), the base of Q5 is returned to ground through R38 and Q5 is driven into saturation. When this occurs a heavy current flows in the secondary of T3.

Each time Q5 is saturated, a pulse of emitter current flows through R35, resulting in a series of voltage drops across this resistor that are averaged by the storage capabilities of C29. The average voltage drop is only about 3 volts, which is not enough to appreciably reduce the peak current through T3, but it is sufficient to insure complete cut off of Q5 when required. In addition, R35 limits dissipation in Q5. Diode CR5 suppresses the positive inductive spike that occurs at the collector of Q5 when the latter is cut off.

Under steady state conditions, the primary of T3 is switched across 16.5 volts for 1.4 microseconds every time a horizontal timing pulse occurs. The polarity of T3 is such that during the current pulse the junction of the anodes of diode quad Z2 are driven positive and the junction of the cathodes are driven negative. Therefore all of the diodes in the quad conduct very heavily for 1.4 microseconds during every horizontal sync and equalizing pulse. During the 1.4 microsecond interval, the clamp coupling capacitor, C48, (figure 30) is connected through the low impedance of the conducting quad to the source of the reference clamp bias (TP2).

If there is any error in the potential on the coupling capacitor, C48, due to low frequency distortion such as hum, tilt or a sudden brightness change, C48 will be immediately charged or discharged through the clamp quad to the clamp bias potential. At the end of the 1.4 microsecond interval, the quad is disconnected and C48 passes the next line of video that follows at the conclusion of the sync pulse. As the line of video ends and the next sync pulse occurs, the cycle is repeated and the sync tip level will be once again compared with the reference bias.

The clamp quad is held in cutoff condition by the charge stored in C26 which results in a reverse bias that is almost equal in amplitude to that of the clamp pulse (about 15 volts). Discharge resistor R32 determines the peak on the pulse current when the clamp is operating on a signal that has no error.

The clamp bias is derived from a voltage divider, as described earlier. The bias is bypassed by C27 in series, but in opposite polarity, with C28. This arrangement is necessary because the polarity of the clamp bias may be either positive or negative. The back-to-back connection of the capacitors in conjunction with the negative bias developed across voltage divider R33, R34 insures proper polarizing potential, regardless of the polarity of the clamp bias.

5. Bias Stabilization

To return to diodes CR6-CR9 (figure 30). The chief function of these diodes is to compensate for an increase in ambient temperature which causes the carrier frequency to have a tendency to drift. Due to the physical properties of semi-conductors, temperature variations produce changes in the internal voltage drops across the junctions of the variable capacitance diodes. These internal voltage changes appear as spurious bias variations. In this case, an increase in temperature will cause the dc bias on the variable capacitance diodes to become more positive, tending to produce an increase in frequency. The parameters of the temperature stabilization diodes are such that the dc bias fed to the variable capacitance diodes is modified by the amount that counteracts drift. Negligible impedance to the video signal is offered by the diodes, since they conduct constantly and are by-passed by coupling capacitor C45. Forward bias is applied to the diodes by the current flow through the voltage divider former by R27 and R28 from the +70 volt bus.

6. Mixer

The output from the high frequency oscillator, Q4, and the low frequency oscillator, Q9, is link-coupled through transformers T1 and T2, respectively to the diode mixer, Z1 (figure 32). The secondaries of T1 and T2 are balanced, with each supplying push-pull drive to the ring-connected diodes of Z1.

The mixer output is taken off the center tapped secondaries of T1 and T2, where, due to the balanced nature of the transformers, there is no voltage developed at the original input frequencies. Between the center tap and the top and bottom of each secondary, however, a voltage is developed that is the product of modulation resulting from non-linear operation on the input signals by the mixer diodes. These modulation products are the sidebands or sum and difference frequencies of the oscillator inputs.

The upper sidebands, which represent the sum frequencies, are relatively low in amplitude since they

are in the region of 100 mc. However, these signals can be disregarded, since it is the lower sidebands or difference frequencies, which are in the 1 to 5 mc range, that are desired. The peak-to-peak amplitude of the lower sidebands is .5 volt and this signal is coupled through C15 to the base of Q3, the FM amplifier.

7. FM Amplifier, R-F Copy Amplifier, FM Output and Low Pass Filter

The FM amplifier, Q3, (figure 37) has a maximum gain of about 4 and this is determined by R14 in the emitter circuit. The gain of this stage can be controlled by varying the amount of degeneration in the emitter with R15, the OUTPUT LEVEL potentiometer, in conjunction with C14. The dc operating conditions are set by base bias resistors R13, R16 and the total emitter resistance consisting of R9, R14, and R15 in series with the −20 volts.

The amplified FM output at the collector of Q3 is coupled through C13 to the base of Q2, an emitter follower, which isolates the collector of Q3 from capacitive loading by the following stages. Peaking coil L5, in series with R10, the collector load of Q3, provides compensation for the stray capacitance shunting the collector circuit. The output from the emitter

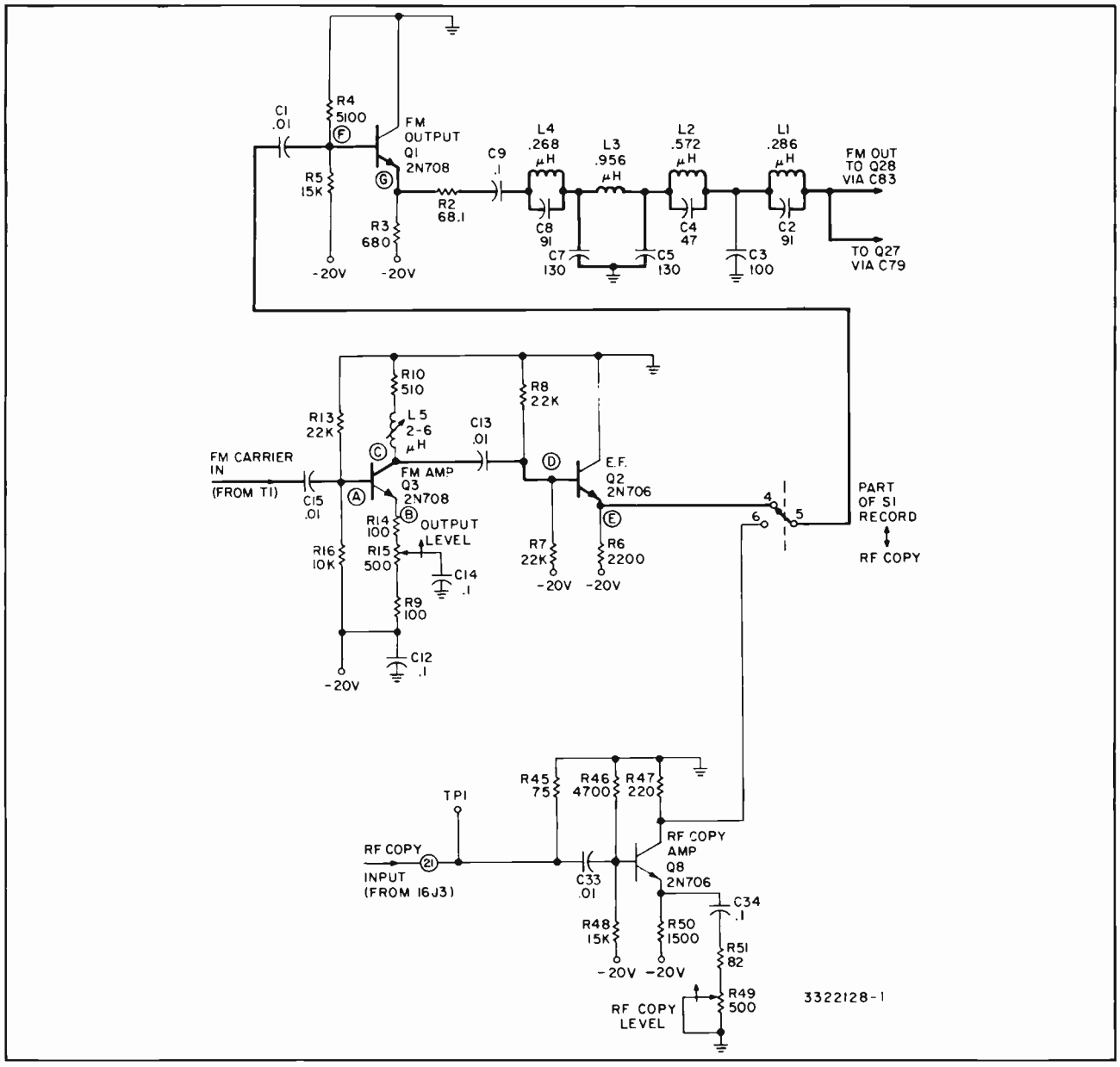
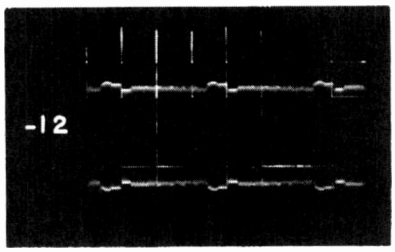
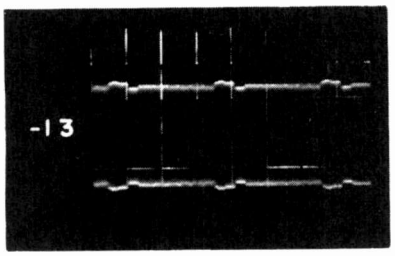


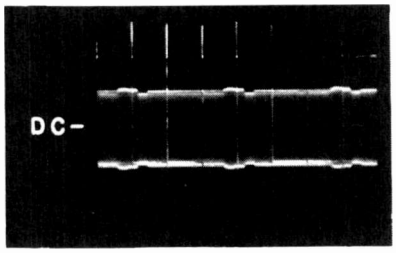
Figure 37—FM Amplifier, R-F Copy Amplifier, FM Output and Low Pass Filter Circuits



A. Q3 base, 20 μs/cm, .1v/cm.



B. Q3 emitter, 20 μs/cm, .1v/cm.



20 μs/cm, .05v/cm.

This waveform is typical of points listed in chart.

KEY	LOCATION	AC AXIS
C	Q3C	— 1.5v
D	Q2B	— 9.8v
E	Q2E	—10.5v
F	Q1B	— 5.0v
G	Q1E	— 5.7v

Figure 38—Typical Waveforms, FM Amplifier, R-F Copy Amplifier, FM Output and Low Pass Filter Circuits

of Q2 drives pole 4 of S1, the RECORD/R-F COPY switch. The output of Q8, the R-F Copy amplifier, drives pole 6 of S1.

The R-F Copy amplifier, Q8, amplifies the FM signal from another recorder. This stage permits a tape to be copied without first having to demodulate the FM signal to video then convert it to FM again in the recording process. The operation of Q8 is similar to that of the Q3, the FM amplifier, except that the output of the former is FM originating in another recorder, while the output of the latter is FM generated within the Modulator itself.

The signal from either Q3 or Q8 is selected by S1 and coupled through C1 to the base of the FM output stage, Q1, an emitter follower. In addition to selecting the FM signal for recording, when S1 is in the R-F Copy position, the other pole section of the switch (figure 40) disables the high (Q4) and the low (Q9) frequency oscillator stages by removing the —20 volts switched from these two stages.

In the RECORD mode, FM output level is adjusted by means of R15, the OUTPUT LEVEL potentiometer. In the R-F COPY mode, the output level is adjusted by means of R49, the R-F COPY LEVEL potentiometer. Both are internal controls.

The FM output from the emitter of Q1 is coupled through a source terminating resistor, R2, and capacitor C9 to drive a low pass filter. The cut-off frequency of the filter is 25 mc, which is sufficiently low to eliminate any oscillator frequency components not cancelled in the balanced mixer, as well as the upper sideband frequency components produced by the mixer. However, the bandwidth of the filter is broad enough to permit transmission of all sidebands necessary for wideband recording.

At the output of the low-pass filter, the signal is split into two branches. One branch goes to the input stage of the FM output line drivers and the other goes to the sync tip frequency metering circuit.

The signal in the first mentioned branch (figure 39) is terminated in 75 ohms by R132 and coupled through C83 to the base of Q28. This transistor is one of five emitter follower line drivers. The output on the emitter of Q28 in addition to driving the line to the Limiter (module A16) is fed simultaneously to the paralleled inputs of the remaining four line drivers, Q29-Q32. Driving a single transistor stage with the filter reduces loading that would otherwise result if all five line drivers were connected across the output of the filter. The output of Q28 driving the line to the Limiter is sending-end terminated by R138. The remaining four amplifiers, Q29-Q32 drive individual lines to the Record Amplifiers, modules A6 through A3, respectively. These lines are not terminated at the sending end, therefore furnish a signal that is twice the level of that going to the Limiter. Capacitor coupling is used in all five output lines.

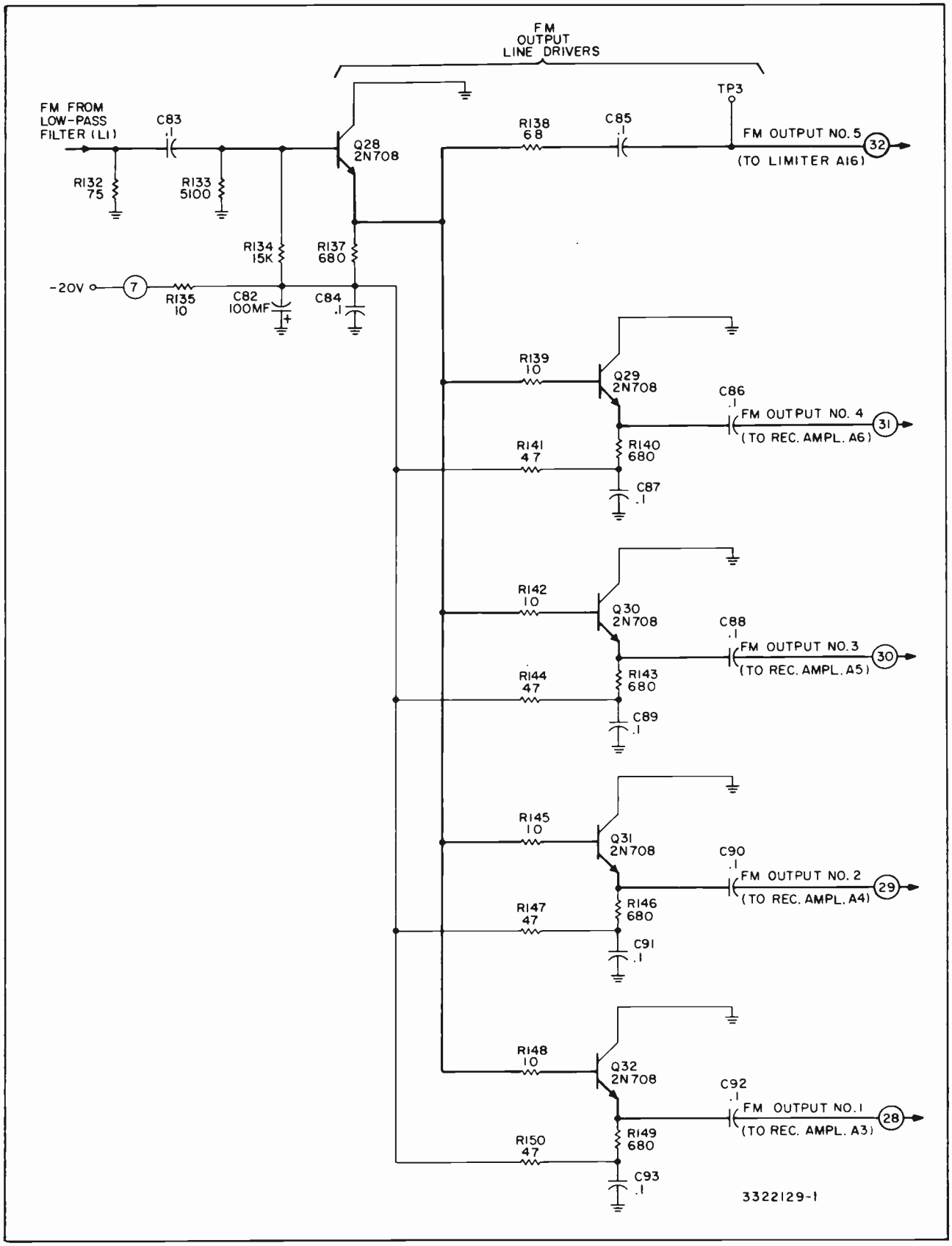


Figure 39—FM Output Line Drivers

8. —20 Volts Electronic Switch

The purpose of the —20 volts switch circuit is to electronically enable or disable the high (Q4) and the low (Q9) frequency oscillators, according to the mode in which the TR-4 is being operated, or to the function selected by means of S1, the RECORD/R-F COPY switch.

As shown in figure 40, the —20 volts switch consists of two transistors, Q18, a PNP, and Q19, an NPN. When the TR-4 is in the STANDBY, WIND or STOP mode, and the MOD-PLAY switch (S4) is in PLAY, a positive voltage is applied via the E-to-E control bus to the base of Q18, the PNP. This cuts off Q18 and the collector goes to —26 volts, to which it is connected by a voltage divider comprised of R80 and R81. The base of Q19, the NPN, is connected to the junction of these two resistors, therefore, it too is cut off since the base voltage (—26 volts) is now more negative than that on the emitter (—20 volts). With Q19 cut off, the —20 volts supply to the high and the low frequency oscillator circuits is opened.

When the MOD-PLAY switch is in MOD, a negative voltage is fed via the E-E control bus to the base of Q18 and Q18 saturates. With Q18 saturated, R80 is grounded and the voltage developed across R80 is applied to the base of Q19. Since this voltage is positive with respect to the —20 volts on the emitter of Q19, the latter is driven into saturation, closing the —20 volts supply circuit to the high and the low frequency oscillator stages.

When the RECORD or SETUP mode is selected, the E-to-E control bus is bypassed and Q18 has no part in the operation of the —20 volt switch. In this mode, the RECORD/SETUP control bus is grounded through 3J7-F by the state of the record group transfer bus in the Record Control (module 3A7), and current flows through the voltage divider consisting of R79 and R81. The voltage developed across R79 appears on the base of Q19, and since this voltage is positive with respect to the —20 volts on the emitter, Q19 is driven into saturation. When this occurs, the —20 volts appearing on the collector of Q19 is applied to the high and the low frequency oscillator circuits.

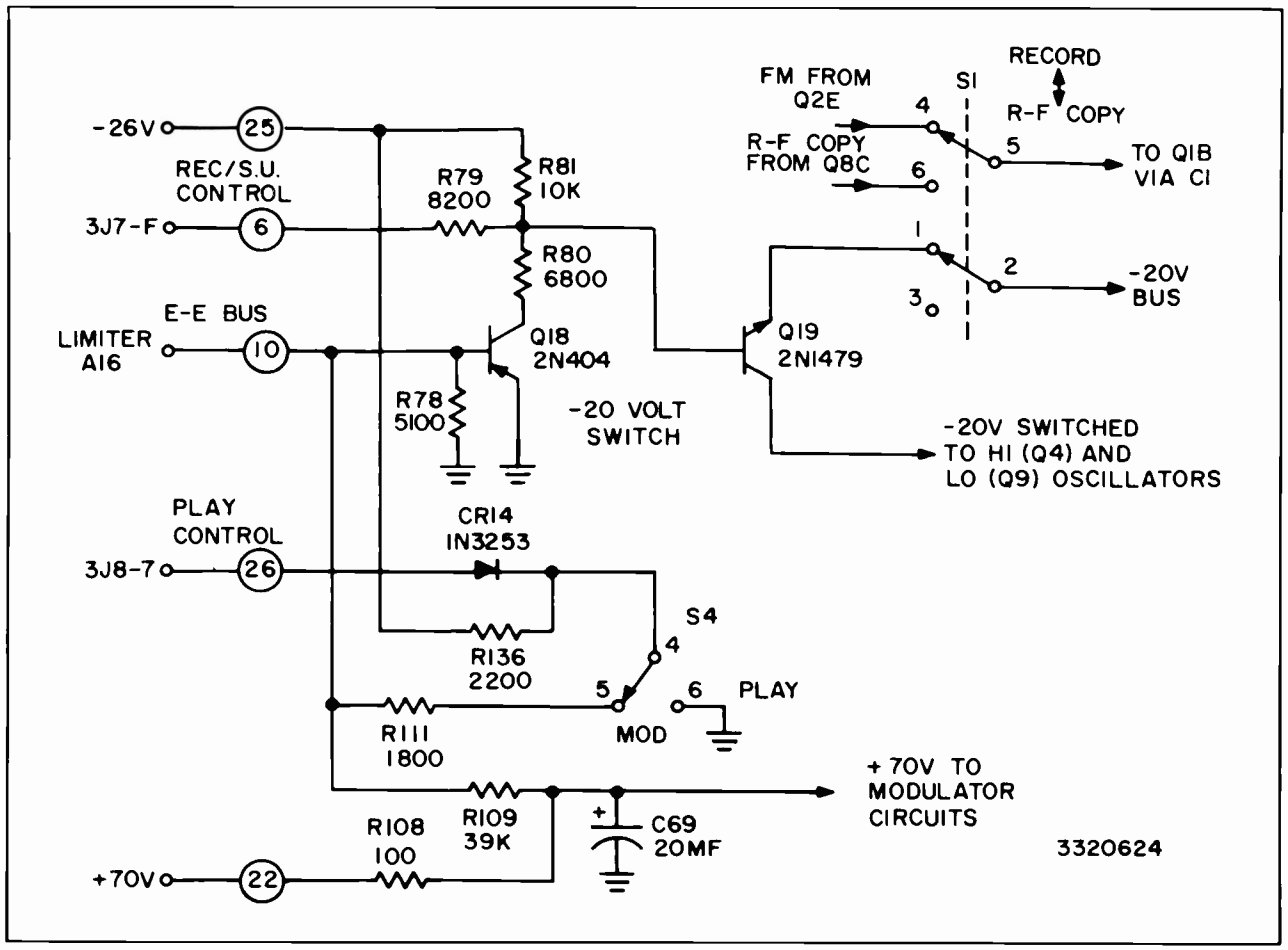


Figure 40 — —20 Volt Electronic Switch; MOD/PLAY and RECORD/R-F COPY Switches

9. MOD-PLAY Switch

The MOD-PLAY switch (figure 40) is an internal control on the Modulator that enables the TR-4 to be put in a back-to-back condition. If the TR-4 is in STANDBY or STOP modes of operation and the MOD-PLAY switch is in the PLAY position, the Modulator circuits are disabled but the playback circuits are energized. This makes it possible to use the noise originating in the heads for making a cursory check of the playback circuits. If this switch is in the MOD position, video being applied to the TR-4 enters the Modulator and is converted to FM. The FM output is then fed to the playback circuits where it is demodulated and restored to its original amplitude modulated format.

When the TR-4 is in the PLAY mode, the Modulator is disabled regardless of the function selected by the MOD-PLAY switch. When the TR-4 is in the RECORD or SET-UP modes, the MOD-PLAY switch is not effective.

10. Sync Tip Frequency Metering Circuit

The purpose of the sync tip metering circuit is to furnish a rectified signal to the FM meter that represents the sync tip region contained in the frequency modulated carrier.

As mentioned earlier, a portion of the FM output of the low-pass filter, L1, is fed to the sync tip frequency metering circuit (figure 41). The signal is coupled through C79 to the base of Q27, the input amplifier. With the SYNC TIP FREQ SET switch, S2, in the position shown, transistor Q27 is in a non-conducting state and the input signal is not passed. The cut off condition of Q27 is due to the reverse bias being applied to the base of Q27 across R131 from the +70 volt bus. This voltage is sufficiently positive to overcome the forward bias on the base, which is developed across the voltage divider consisting of R126, R127 returned to −20 volts. Until the SYNC TIP FREQ SET switch, S2, is operated, the metering circuit remains in a quiescent state; the video modulated FM output of L1 continues to feed only through the FM output line drivers, and the output line to the FM meter remains open.

When S2 is pressed (this is a pushbutton control on the front panel), the operating conditions of the circuit are changed and the following events take place.

Section S2A opens the circuit between the video output (Q24E) of the pre-emphasis section and the video input (Q17B) to the modulator section. Hence video drive to the high and the low frequency oscillators is interrupted and the signal appearing at the output of L1 is unmodulated FM.

Section S2B closes the circuit to the FM Meter on the Play Control Panel, enabling the detected output of the metering circuit to be read on the meter.

Section S2C removes the +70 volts from the base of Q27, therefore this transistor is able to conduct, amplifying the unmodulated FM signal being applied to its base.

Under the conditions just outlined, the output on the collector of Q27 is fed through a clipper (CR17, CR18) where a portion of the positive and negative peaks are clipped. The output of the clipper is coupled by an emitter follower, Q26, at approximately .5 volt peak-to-peak to either the monochrome or color sync tip frequency tank circuit.

The monochrome sync tip tank is tuned to 4.28 mc and the color sync tip tank is tuned to 5.5 mc. The latter is also designed to accommodate the sync tip frequency of the different line rates used on international standards. The frequency of each tank is set at the factory and neither L18 nor L19 should be readjusted unless they become de-tuned due possibly to component replacement or some other reason. Should it become necessary to re-tune either tank, see the appropriate procedure under *Adjustments,* which follows at the conclusion of this description. The appropriate tank is automatically inserted in the circuit when the desired recording standard is chosen by means of the MONO COLOR selector switch, S3. Both tanks are high Q circuits and the output at approximately 1.8 volts peak-to-peak is fed to the base of the detector driver, Q25.

Transistor Q25 is connected as an emitter follower to isolate the tank circuits from the loading effects of the succeeding peak-to-peak detector. The output on the emitter of Q25 is coupled through C77 to the peak-to-peak detector, which consists of CR15, CR16, and C76. When the SYNC TIP FREQ SET button is pressed, a dc level representing the tip of sync on either monochrome or color standards is fed across R121 to the FM meter (4M2) on the Play Control Panel.

During the *Initial Set Up* procedure described in the *TR-4 Operation Manual, IB-31810,* the sync tip frequency is set by adjusting the carrier frequency potentiometers, R91 and R92, for monochrome and color, respectively, to obtain a maximum reading on the FM Meter. However, the sync tip frequency should still be checked at regular intervals on the meter to make certain it is within the tolerance allowed.

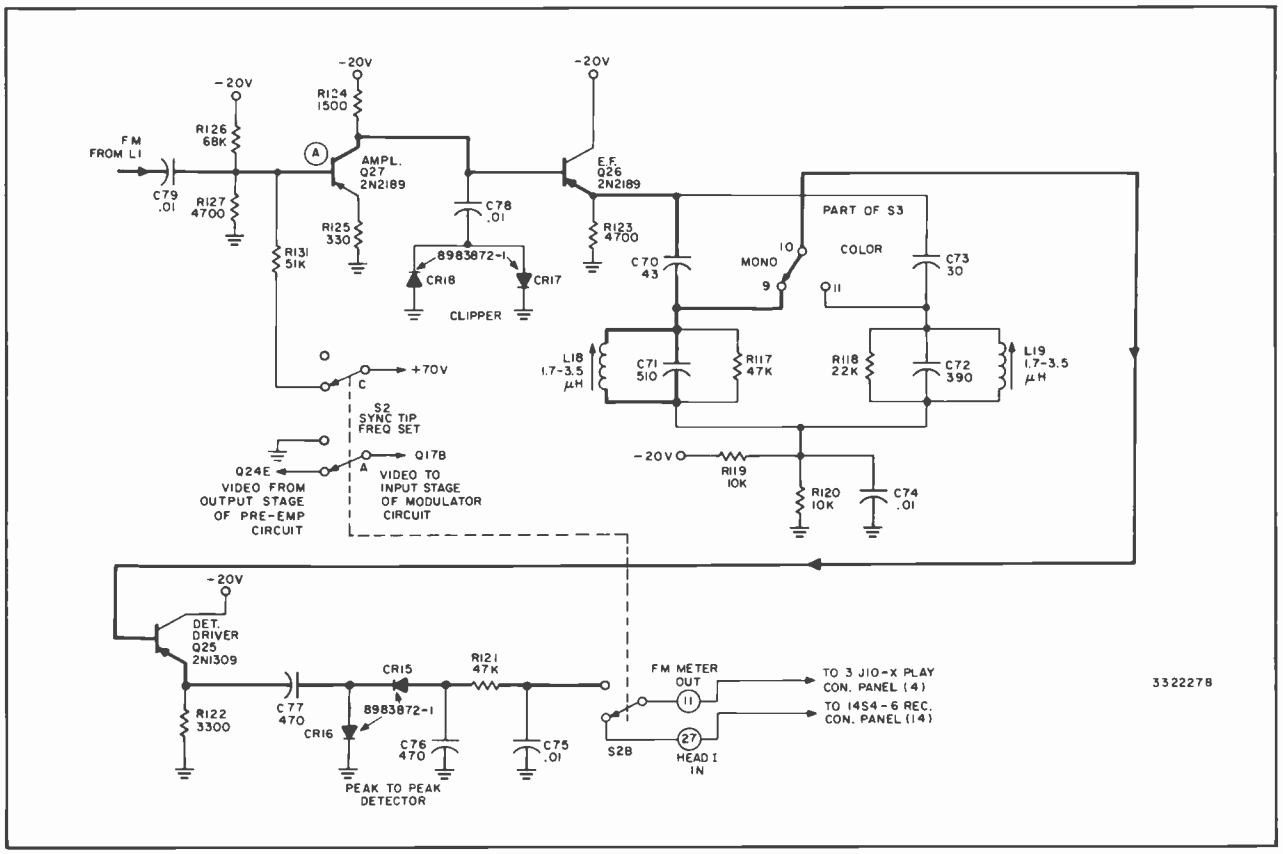
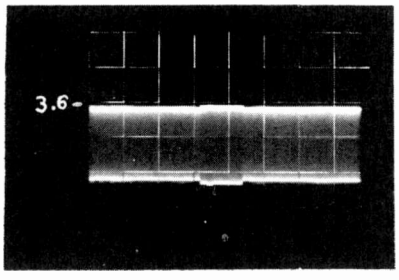


Figure 41—Sync Tip Frequency Metering Circuit



A. Q27 base, 1 ms/cm, .5v/cm

Figure 42—Typical Waveform, Sync Tip Frequency Metering Circuit

a. Sync Tip Check

To check the sync tip frequency, proceed as follows:

1. Place the TR-4 in STOP mode.

2. Remove the Modulator module and place the MOD-PLAY switch, S4, in MOD position, then replace the Modulator.

3. Place the MONO/COLOR selector switch on MONO.

4. Press the SYNC TIP FREQ SET button and observe the FM Meter. If the reading on the meter is 25% or more below the previous maximum reading, readjust R91 for maximum indication.

5. Place the MONO/COLOR selector switch on COLOR and repeat 4, readjusting R92 if required.

6. Remove the Modulator and restore the MOD-PLAY switch, S4, to PLAY position; replace the Modulator.

Adjustments

The adjustments in the procedures below are not part of routine maintenance. They should be per-

formed only if a component affecting the response of the circuits concerned in these procedures is replaced; or if for some other reason, realignment of such circuits becomes necessary. When such is the case, refer to the procedure appropriate to the circuit requiring realignment.

Video Amplifier Alignment

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) including dual trace plug-in unit and low capacity probes.

Sweep generator with good response to 10 mc

Module extender

4700 ohm resistor

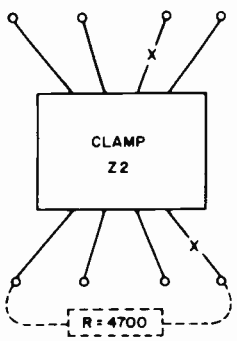
75 ohm resistor

1. Place the Equipment Power circuit breaker, 1CB1, in the OFF position.

2. (a) Remove the Modulator (module A2) from the TR-4.

(b) Disconnect C51, a 22pF capacitor between the base of Q10 and the emitter of Q11.

(c) Refer to the sketch and disable clamp Z2 by disconnecting the leads marked "X"; then connect the 4700 ohm resistor across the terminals shown in the sketch.



(d) Mount the Modulator in an extender and insert it in the TR-4.

3. Disconnect the video coaxial lead from terminals 17-1 on connector A2J1 on the rear of the TR-4; then connect the 75 ohm resistor across these two terminals.

4. Turn the Equipment Power circuit breaker, 1CB1, ON; place the TR-4 in the E-E mode of operation; switch the MONO/COLOR selector to MONO, and switch the RECORD/R-F COPY selector to RECORD.

5. Connect the output of the sweep generator to terminals 17-1 on connector A2J1. Set the sweep rate for 0 to 10 mc and adjust the gain of the generator to obtain an output not in excess of .4 volt peak-to-peak.

6. Connect one oscilloscope probe to Q17 base and the other to Q10 emitter. While observing the signal at these two points, adjust the core of L12 to obtain optimum response. Some discontinuity will appear in the sweep envelope near 6.8 mc, but up to this point, the response should be flat $\pm 5\%$. At 4 mc the response will exhibit a 1 db rise when C51 is reconnected.

7. Disconnect the 4700 and 75 ohm resistors and restore all connections for normal operation.

FM Amplifier Alignment

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) including dual trace plug-in unit and low capacity probes.

Sweep generator with good response to 20 mc

Module extender

75 ohm resistor

1. Place the Equipment Power circuit breaker, 1CB1, in the OFF position.

2. (a) Remove the Modulator (module A2) from the TR-4.

(b) Disconnect C15 from T1-4: connect the 75 ohm termination resistor between the free end of C15 and ground.

(c) Mount the Modulator in an extender and insert it in the TR-4.

3. Turn the Equipment Power circuit breaker, 1CB1, ON; place the TR-4 in the E-E mode of operation; switch the MONO/COLOR selector to MONO, and switch the RECORD/R-F COPY selector to RECORD.

4. Connect the output of the sweep generator across the 75 ohm termination on C15. Set the sweep rate for 0 to 20 mc and adjust the gain of the generator to obtain an output of 1 volt peak-to-peak.

5. Connect one oscilloscope probe to the input side of C15 and the other to Q1 emitter. While observing the signal at these two points, adjust the core of L5 for a response that is flat within $\pm 5\%$ up to 15 mc.

6. Disconnect the 75 ohm resistor and restore all connections for normal operation.

High and Low Frequency Oscillator Alignment

Recommended Test Equipment and Accessories

VTVM

Grid dip meter or sensitive absorption wavemeter

Module extender

1. Apply a composite video signal to the input of the TR-4.

2. Place the Equipment Power circuit breaker, 1CB1, in the OFF position.

3. Carefully remove the video coaxial lead from terminals 17-1 of connector A2J1 on the rear of the TR-4.

4. (a) Connect the VTVM to CLAMP BIAS (TP2) on the front of the Modulator.

(b) Place the Equipment Power circuit breaker, 1CB1, in the ON position.

(c) Observe the VTVM and adjust the MONO sync tip frequency potentiometer, R91, (on the front panel) for zero volts.

(d) Disconnect the VTVM and place the equipment power circuit breaker in the OFF position.

5. (a) Mount the Modulator in an extender and insert it in the TR-4.

(b) Place the Equipment Power circuit breaker in the ON position.

(c) Set the grid dip meter or absorption wavemeter to 60 mc and couple it loosely to the high frequency oscillator coil, L7.

(d) Adjust the core of L7 until the oscillator is tuned to 60 mc.

(e) Set the meter to 55.72 mc and couple it loosely to the low frequency oscillator coil, L10. Adjust the core of L10 until the oscillator is tuned to *approximately* 55.72 mc. Final tuning will be accomplished in step 7.

6. (a) Place the Equipment Power circuit breaker in the OFF position.

(b) Re-connect the video coaxial lead to terminals 17-1 of connector A2J1.

(c) Place the Equipment Power circuit breaker in the ON position.

7. Press and hold the SYNC TIP FREQ SET pushbutton on the front panel. Observe the FM LEVEL meter, 4M2, and adjust the core of L10 to obtain a maximum reading on the FM LEVEL meter.

8. Remove the extender and replace the Modulator in the TR-4.

9. A slight readjustment of the MONO sync tip frequency potentiometer, R91, may be necessary to compensate for detuning of the oscillator when the Modulator is plugged into its shielded compartment.

Adjustment of Sync Tip Frequency Determining Coils L18 and L19

NOTE: These coils have been adjusted at the factory and the adjustment should not be disturbed in the course of routine maintenance. The procedure below should only be performed in the event of coil replacement.

Recommended Test Equipment and Accessories

Signal generator capable of providing an accurate output signal in the range of 4–6 mc at 1 volt peak-to-peak.

Module extender

Coil L18 Adjustment

1. (a) Place the Equipment Power circuit breaker, 1CB1, in the OFF position.

(b) Remove the Modulator from the TR-4 and place the RECORD/R-F COPY switch, S1, in the R-F COPY position.

(c) Mount the Modulator in an extender and insert it in the TR-4.

(d) Turn the MONO/COLOR selector switch, S3, to MONO standards.

(e) Place the Equipment Power circuit breaker in the ON position.

2. (a) Connect the output of the signal generator to the R-F COPY IN connector, 16J3.

(b) Set the frequency of the generator to 4.28 mc, and adjust the gain for an output of 1 volt peak-to-peak.

3. (a) Press and hold the SYNC TIP FREQ SET pushbutton, S2.

(b) Observe the FM LEVEL meter, 4M2, and adjust L18 to obtain a maximum reading on the FM LEVEL meter.

4. (a) Place the Equipment Power circuit breaker in the OFF position.

(b) Remove the extender from the TR-4; restore the RECORD/R-F COPY switch, S1, to RECORD, and replace the Modulator in the TR-4.

Coil L19 Adjustment

To adjust L19, repeat the foregoing procedure but observe the following changes.

In step 1 (d) turn the MONO/COLOR selector switch, S3, to COLOR standards.

In step 2 (b) set the frequency of the signal generator to 5.5 mc.

In step 3 (b) adjust L19.

Record Amplifiers (Modules A3, A4, A5, A6)

General

There are four identical Record Amplifiers, one for each record channel. The purpose of the Record Amplifiers is to provide the correct amount of delay to offset any irregularities in head quadrature and to amplify the FM signals driving the magnetic heads.

From a functional standpoint, the circuitry of the Record Amplifiers can be divided into two sections. One section contains the delay circuits and the other contains the amplifier circuits. Accordingly, each section will be considered separately in the following description, and since all four modules are identical, only one will be discussed.

Delay Section

To obtain optimum results when recording, the effective spacing between the four magnetic heads on the headwheel theoretically should be exactly ninety degrees. The effective spacing can be adjusted either mechanically or electrically, and both of these methods are employed on the TR-4. During the manufacturing process, the heads are mechanically spaced on the headwheel to within a few seconds of the correct ninety degrees position. Then in the TR-4 final adjustments are made electrically by means of the adjustable delays to compensate for the remaining error in head quadrature.

To illustrate the function of the delay line, a headwheel with the no. 2 head incorrectly positioned by an angle equal to "x" seconds is shown in figure 43.

A recording made with this headwheel and then played back by another with the heads perfectly aligned will produce a picture with horizontal displacement as shown in figure 44. Because the angular displacement of head no. 2 is in the direction of counter rotation to its proper position, the information will be recorded late in time. However, if the signal feeding the late head is advanced in time by an amount equal to the mechanical displacement, the recorded information will appear in the proper position on the tape. This is accomplished electrically by means of the tapped delay line.

When information is being recorded the FM signal from the appropriate FM output line driver on the Modulator (module A2) is fed to the input of the delay section (see figure 45). The incoming signal is coupled through C100 to the base of Q100, an emitter follower. The input is terminated in 75 ohms by R100. From the emitter of Q100, the signal is fed

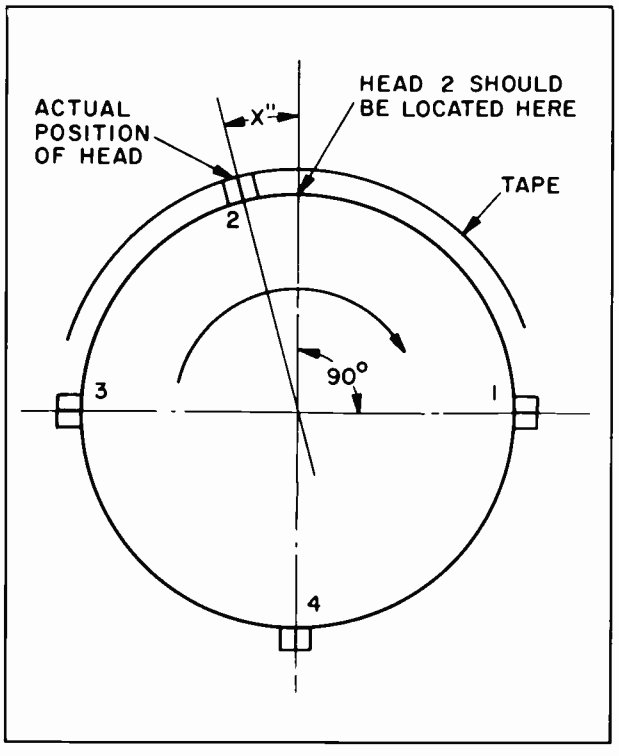


Figure 43—Video Head Placement Showing Head No. 2 Out of Quadrature

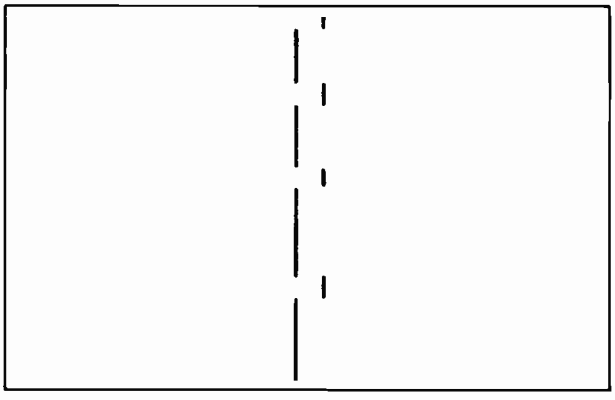


Figure 44—Vertical Line on TV Raster Showing Horizontal Displacement of Head No. 2

through R119, a parasitic suppressor, to the base of Q101, the delay line driver. The output on the collector of Q101 is fed via the delay switch, S2, to the delay line, L100.

The delay network consists of ten sections with each section connected to a tap switch. Each section of the line provides a delay of approximately .015 microseconds, which is equivalent to approximately 5 seconds of arc on the headwheel. Selection of the desired delay increment is by means of S2 which is controlled from the front panel of the module. The

delay selector dial is calibrated so that zero switch position represents the mid-point of the delay line. At this setting, 50% of the delay available is in the circuit. To the right of zero, the dial has the numerals from 1 to 5, over which is a plus sign to indicate that turning the switch in this direction increases the amount of delay. Similarly, to the left of zero are the numerals from 1 to 5, over which is a minus sign to show a decrease in the amount of delay. Such an arrangement makes it possible to delay or, in effect, advance the signal ultimately driving the heads. Each end of the delay line is terminated in 46.4 ohms; at the input by R105 and at the output by the 38.3 ohms of R108 in combination with the emitter impedance of Q102.

The output of the delay line is coupled through C114 and R108 to the emitter of Q102, a common base amplifier. This stage has a gain of slightly more than 3 and provides virtually all of the signal amplification. Nominal value of the signal initially applied to the base of the input transistor, Q100, is .6 volt peak-to-peak. Thus the output signal on the collector of Q102 is approximately 2 volts peak-to-peak. From the collector of Q102, the signal is dc coupled to the base of Q103. This transistor together with Q104, another emitter follower, are connected to form a direct coupled cascade amplifier. This configuration isolates Q102 from the succeeding input circuit of the amplifier section. The gain of the cascade amplifier is

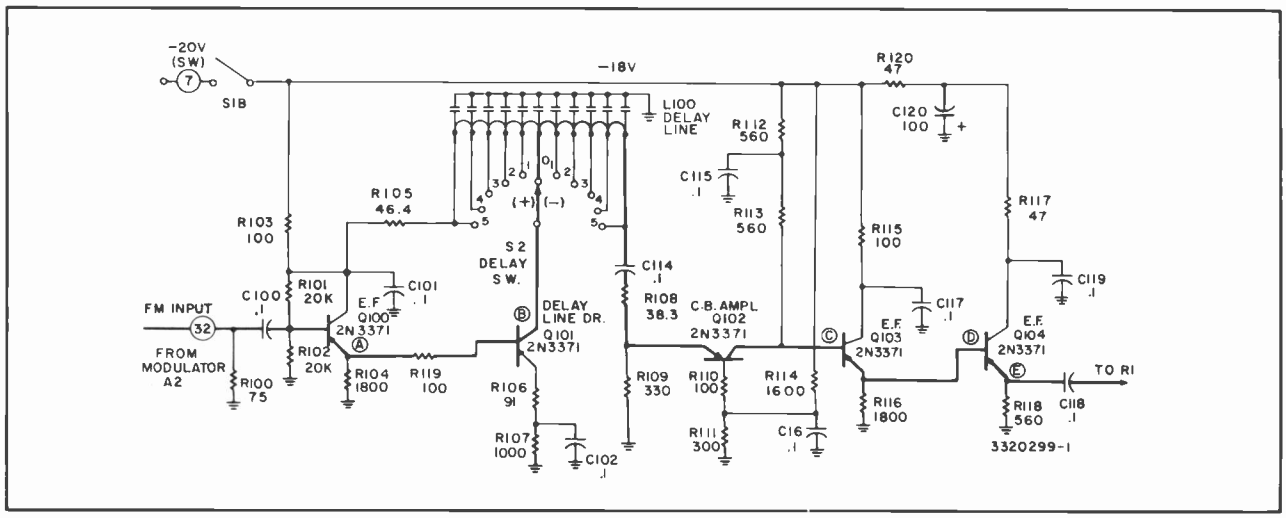
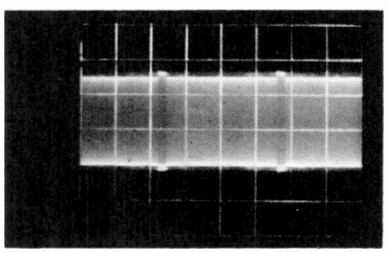
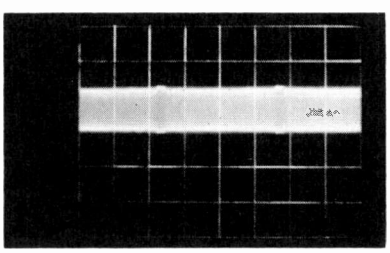


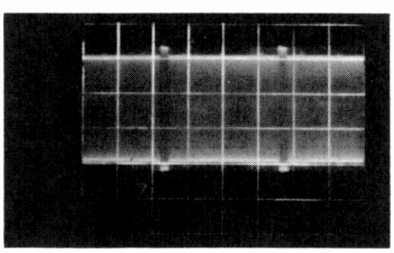
Figure 45—Delay Circuits, Record Amplifier



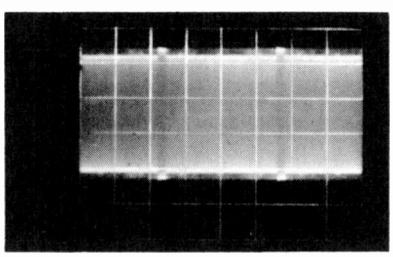
A. Q100 emitter, 5 ms/cm, .2v/cm.



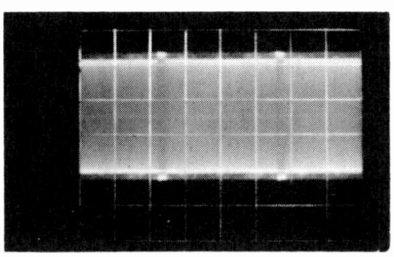
B. Q101 collector, 5 ms/cm, .1v/cm.



C. Q103 base, 5 ms/cm, .5v/cm.



D. Q104 base, 5 ms/cm, .5v/cm.



E. Q104 emitter, 5 ms/cm, .5v/cm.

Figure 46—Typical Waveforms, Delay Circuits, Record Amplifier

unity; therefore the signal available on the emitter of Q104 is of the order of 2 volts peak-to-peak. From the emitter of Q104, the signal is fed through C118 to the input stage of the amplifier section.

Amplifier Section

The output of the delay section is coupled through C118, potentiometer R1, and C1 to the base of Q1, an emitter follower (see figure 47). Potentiometer R1

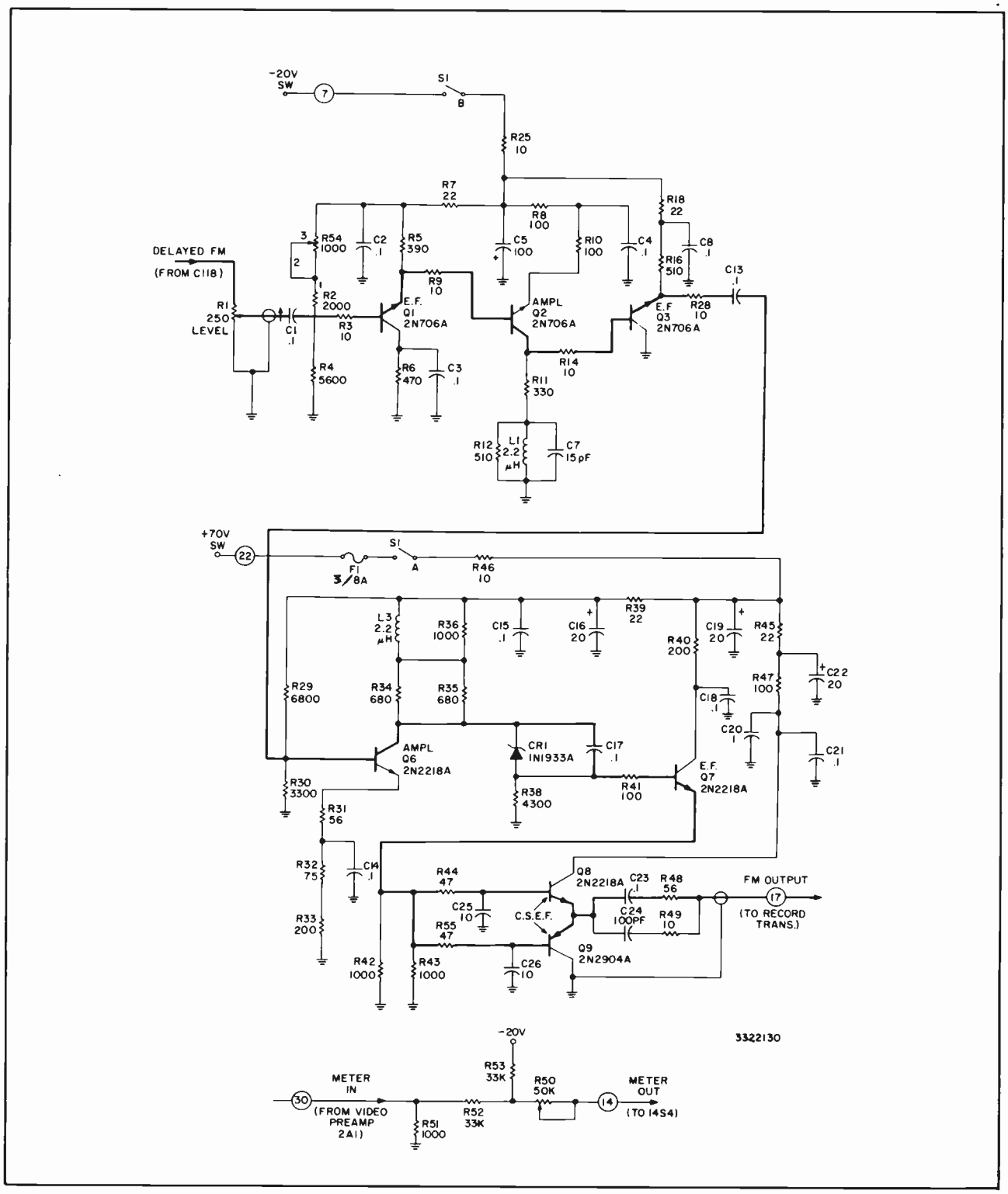


Figure 47—Amplifier Circuits, Record Amplifier

is a LEVEL control on the front panel, which permits the amplitude of the record current to be adjusted to the optimum value required for driving the heads. From the emitter of Q1, the signal is fed to the base Q2, an amplifier with a gain of about 3. A shunt peaking coil, L1, in series with the collector load provides high frequency compensation for this stage. The output on the collector of Q2 is approximately 5.5 volts and this is fed to the base of Q3, an emitter follower with unity gain. From the emitter of Q3, the signal is coupled through C13 to the base of Q6.

The gain of Q6 is almost 4, thus the signal on the collector is approximately 20 volts peak-to-peak. This stage also employs shunt peaking for high frequency compensation. Coil L3 in series with the collector load serves this purpose. The output on the collector of Q7 is fed through C17 to the base of Q7, an emitter follower. Zener diode CR1 maintains the bias on the base of Q7 at a potential that is 12 volts positive with respect to the dc voltage on the collector Q6. From the emitter of Q7, the signal is fed to the complementary symmetry amplifier, Q8, Q9.

The complementary symmetry stage is operated as a class B amplifier, with Q8 conducting on the positive half cycles and Q9 conducting on the negative half cycles. The output of this stage is coupled through C23 and R48 to the primary of the appropriate record transformer on the Video Preamplifier (module 2A1). Capacitor C24 and R49, in parallel with the output coupling components form a frequency compensation network to compensate for the response of the record transformer and the head.

The four 10 ohm resistors R3, R9, R14, and R28; the one 100-ohm resistor, R41; and the two R-C networks, R44, C25 and R55, C26, are used in the coupling circuits between stages to eliminate parasitic oscillations.

Potentiometer R50 is an internal control used to calibrate the head current metering circuit on the Video Preamplifier (module 2A1) so that the reading on the FM LEVEL meter, 4M2, will be correct.

Potentiometer R54 in the base of Q1 adjusts the bias of Q1 for optimum intermodulation distortion. This adjustment is made in the factory, and R54 should not be readjusted during routine maintenance.

The dc operating voltages, +70v switched and −20v switched, are applied to the Record Amplifier when the ON-OFF toggle switch, S1, on the front panel is in the ON position. Between the +70v contact on the input side of S1 and the incoming 70v line, there is a ⅜ ampere fuse (F1). The ON-OFF switch permits the head currents to be turned off when making tests or adjustments. For example, if adjustments are being made to the Headwheel Servo System and the headwheel is not rotating with the TR-4 in the Record or Setup modes, the ON-OFF switch on all four Record Amplifiers should be switched to the OFF position. Applying record currents with the headwheel stationary could possibly cause damage to the headwheel slip rings.

The +70v and the −20v are supplied from the Regulator (module C20). These voltages are present only when the TR-4 is in Record of Setup modes of operation; in other modes these voltages are switched off. The Regulator is interlocked with modules B15 Tonewheel Processor, B16 Tonewheel Servo, B17 Headwheel Modulator, B20 Tape Sync Processor, C19 Capstan Oscillator, and C21-C23 Headwheel/Capstan Power Amplifiers. If any of these modules are removed from the TR-4, the +70v and −20v circuits are opened. (For a detailed description of the module interlock circuitry, see *INTERLOCK SYSTEMS* in the *CONTROL AND POWER SUPPLY SYSTEMS* instruction book, *IB-31817*.)

Video Preamplifier (Module 2A1)

General

The primary purpose of the Video Preamplifier is to provide a small measure of current amplification to the signal from the heads during playback and to furnish the proper impedance match between the heads and the Playback Amplifiers.

There are four preamplifier circuits, one for each playback channel and also a head current metering circuit for each of the four record channels. In addition to these circuits, the record transformers (T1-T4), that couple the record current output of the individual Record Amplifiers to the magnetic heads, are mounted on this module.

The four preamplifiers and the four current sampling circuits are wired on two boards, with channels 1 and 3 on one board and channels 2 and 4 on the other board. The boards are assembled back-to-back to form the module. The module is enclosed in a metal shield, and it is mounted in a recess directly behind the headwheel panel on the tape transport.

Each preamplifier circuit consists of a cascode input and an emitter follower output and each metering circuit employs a single transistor. Components in number series 100 (i.e., Q101, R101) refer to channel 1. Components in number series 200 refer to channel 2 and so forth. Where a component has a numerical prefix, such as 1R1, or 1C1, it is common to channels 1 and 3. Similar components in channels 2 and 4 have prefix 2.

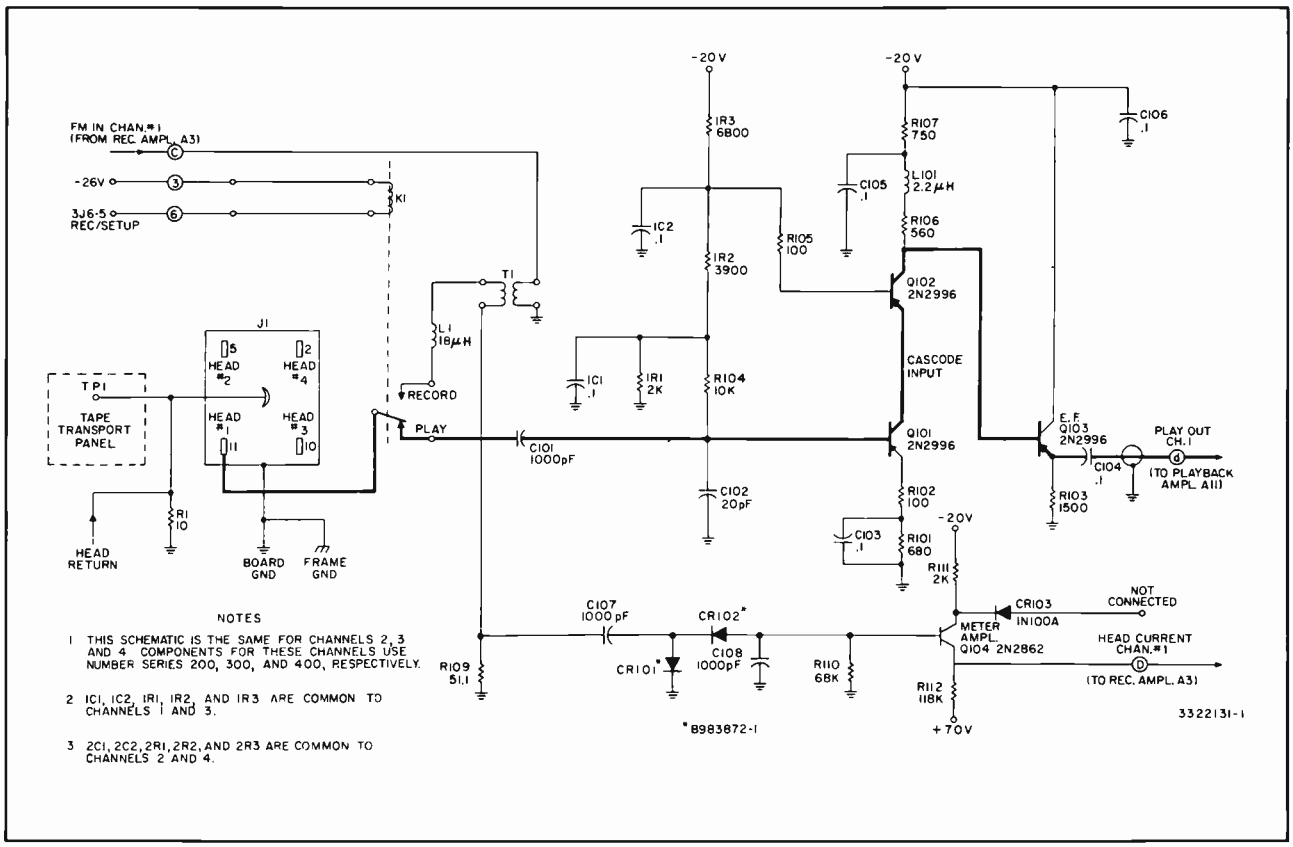


Figure 48—Video Preamplifier Circuit

Preamplifier Circuit

Since the circuits for all four channels are electrically identical only one is described here. (Refer to the simplified schematic, figure 48).

In the playback mode, low level signals from the appropriate head are fed through K1 and C101 to the base of Q101. Transistors Q101 and Q102 are connected as a cascode input amplifier. The advantage of this type of circuit in dealing with low level signals is that most of the noise is eliminated even though the signal is amplified. Virtually all of the amplification is provided by Q102. Most of the noise inherent in the circuit is confined to Q101; and since this transistor furnishes very little amplification, the amount of noise in the signal subsequently amplified by Q102 is very slight.

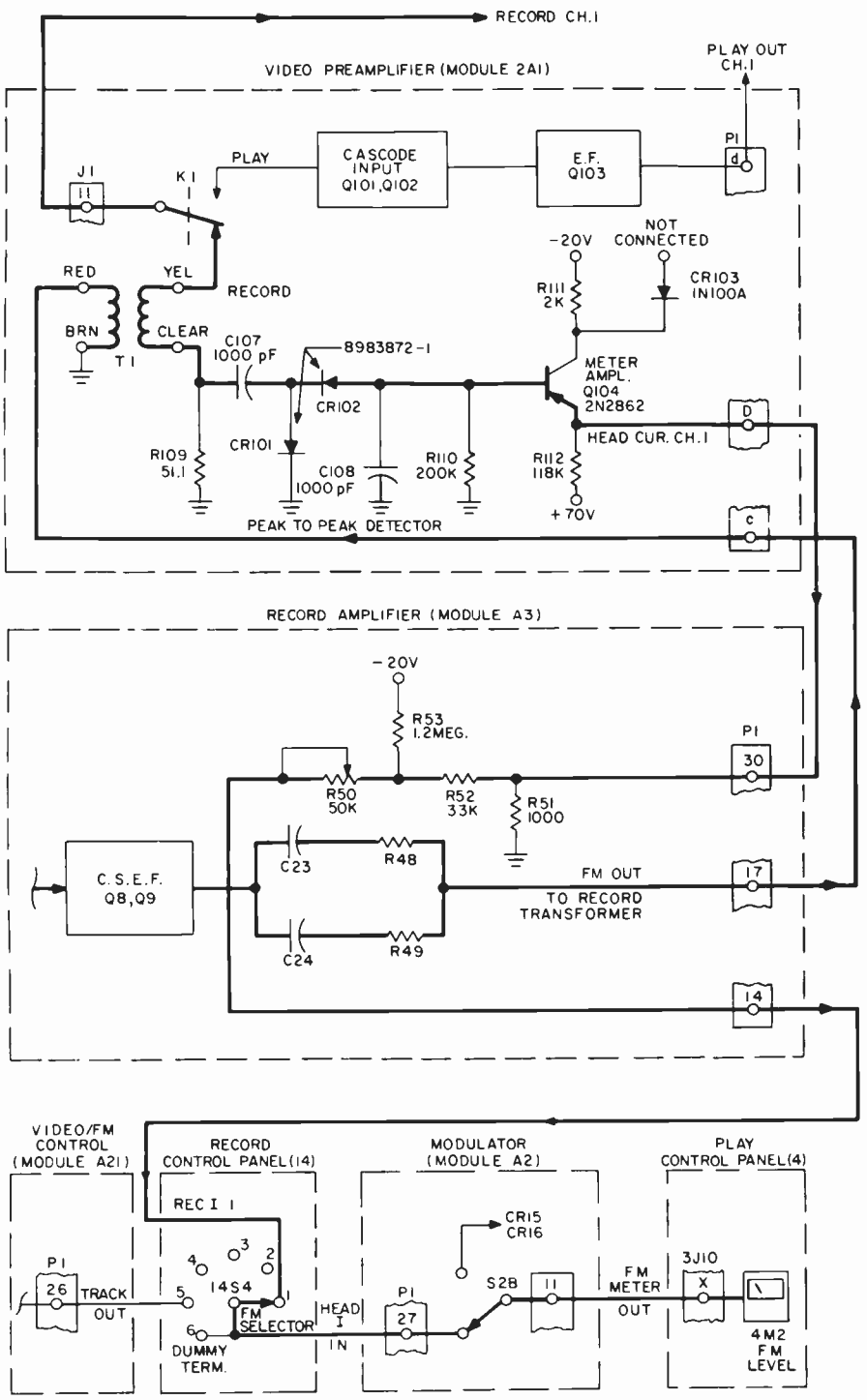
Transistor Q102 serves as the load in the collector circuit of Q101, with the output of the latter feeding directly into the emitter of Q102. The impedance presented by Q102 to the flow of signal current in the collector of Q101 is negligible, therefore the voltage available at the emitter of Q102 is very slight. However, the output of the cascode amplifier is taken across the collector load (R106) of Q102. The impedance of the load is such that the amplitude of the output signal is suitable for ultimately driving the output line. A shunt peaking coil, L101, in the collector of Q102 provides high frequency compensation. Bias voltage on the bases of Q101 and Q102 is developed across the voltage divider consisting of 1R1, 1R2, and 1R3 connected across −20 volts. Capacitor C102 is the head resonating capacitor.

The signal on the collector of Q102 is direct coupled to Q103, an emitter follower. The output on the emitter of Q103 is coupled through C104 to the input of Playback Amplifier (module A11). Emitter follower coupling prevents loading of the cascode amplifier by the input stage of the Playback Amplifier.

Meter Current Sampling

The metering current circuits of all four channels are similar, therefore only the circuit pertaining to the head current for channel number one will be described (see figure 49).

In the record mode, the amplified FM record current from Record Amplifier module A3 is fed to head number one through transformer T1. The FM signal is sampled from the secondary of T1 and fed through a peak-to-peak detector, CR101, CR102, to the base of Q104, the meter amplifier. The signal is rectified



NOTES:

1. RECORD METERING CIRCUIT IS SIMILAR FOR CHANNELS 2,3,AND 4.
2. RECORD CURRENT IS SAMPLED FOR METER 4M2 IN RECORD MODE ONLY

3322269

Figure 49—Record Current Metering Circuit

in Q104 and the rectified output appearing on the emitter is returned to Record Amplifier module A3.

The meter current is fed through two resistors on this module, R52 and potentiometer R50. The latter is an internal control that is used to calibrate the metering circuit so that the reading on the FM LEVEL meter, 4M2, will be correct. From R50 the current goes through the appropriate contacts on the record current selector switch, 14S4, which, in this case, is the REC I-1 position.

Switch 14S4 is a five-position rotary switch on the Record Control Panel, with the first four positions reserved for selecting the record current of each channel. Position five selects the control tracking signal from the Video/FM Control (module A21). From 14S4-1, the signal is fed to the B section of switch S2 on the Modulator (module A2).

This switch, which is the pushbutton type on the front panel of the Modulator, is designated SYNC TIP FREQ SET. Switch S2 is normally in the position shown, and the record current flows through the closed contacts out of the Modulator to the FM LEVEL meter, 4M2, on the Play Control Panel. When the button on S2 is pressed, the REC I-1 circuit is opened and the output from the sync tip metering circuit on the Modulator (module A2) is fed through S2B and out to the FM LEVEL meter. At this point it is sufficient to say that the latter signal represents the sync tip region of the FM signal, either monochrome or color depending on the standard selected. (The origin of this signal is discussed in description of the Modulator [module A2]).

Playback Amplifiers (Modules A11, A12, A13, A14)

General

A Playback Amplifier is used in each of the four playback channels to amplify the output of the four video preamplifiers and to enable the correct amount of delay to be inserted to compensate for errors in head quadrature. Quadrature errors are due to the magnetic heads not being exactly ninety degrees apart around the periphery of the headwheel, or to tapes that were recorded with improper headwheel quadrature. Equalization is also provided so that the response of the FM playback system can be adjusted to compensate for slight differences in the frequency response of the individual heads.

Like the Record Amplifiers (modules A3-A6), the Playback Amplifiers consist of two sections, the amplifier circuits proper (figure 50), and the delay circuits (figure 51). However, in the case of the Playback Amplifier, the delay section follows the amplifier sec-

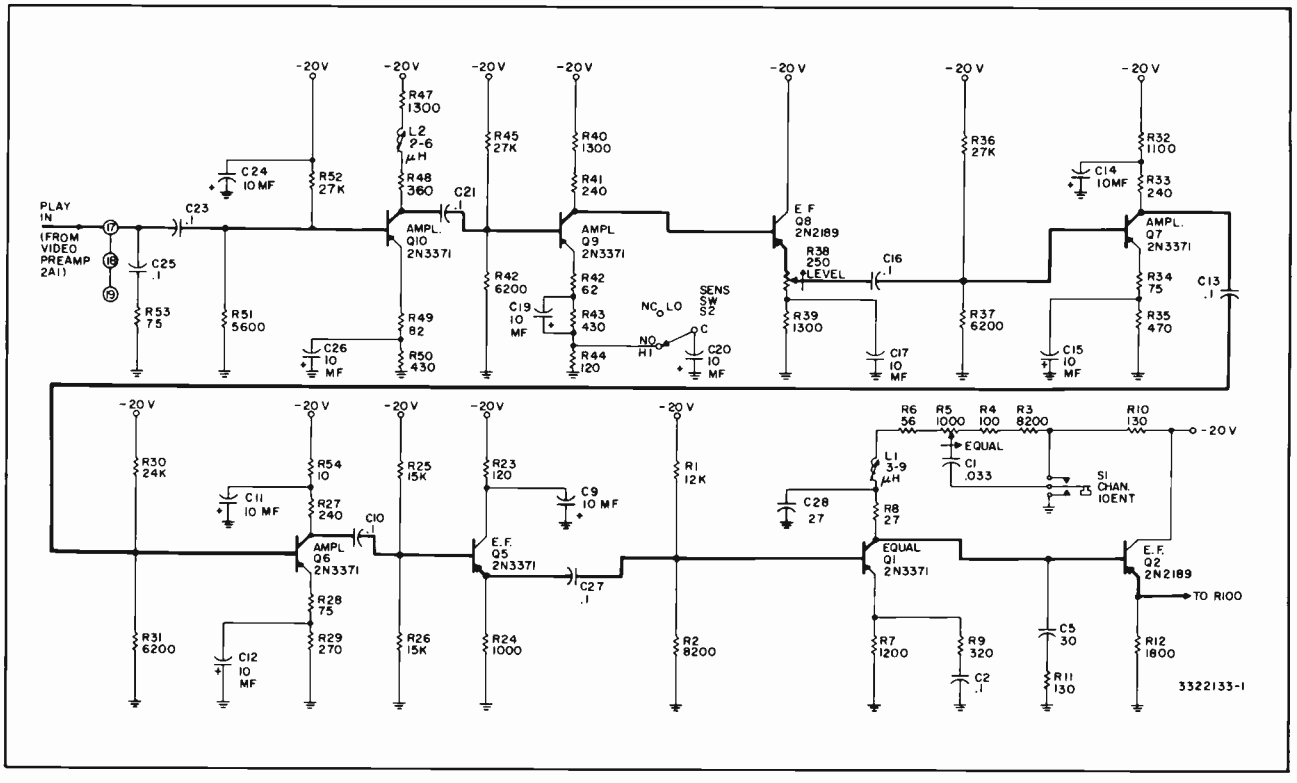


Figure 50—Amplifier Circuits, Playback Amplifier

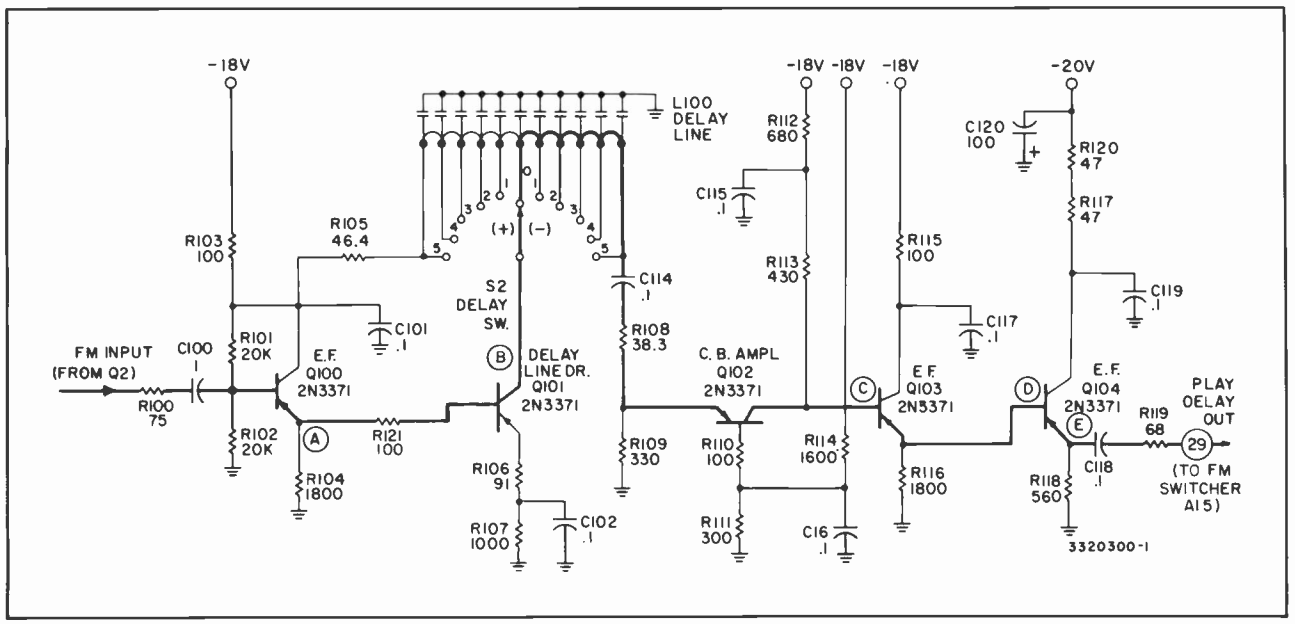
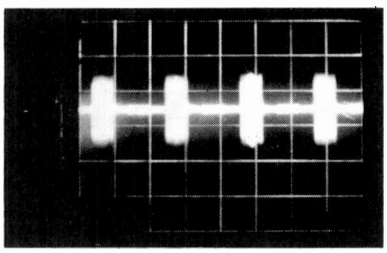
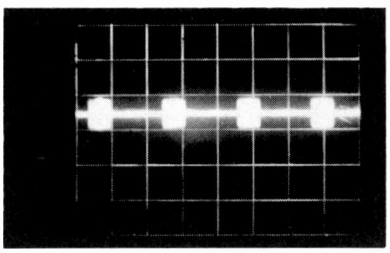


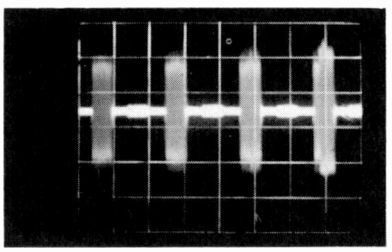
Figure 51—Delay Circuits, Playback Amplifier



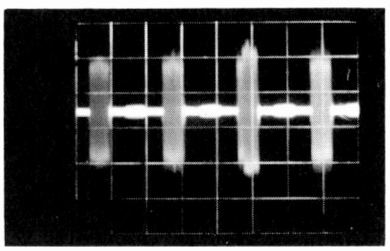
A. Q100 emitter, 2 ms/cm, .1v/cm.



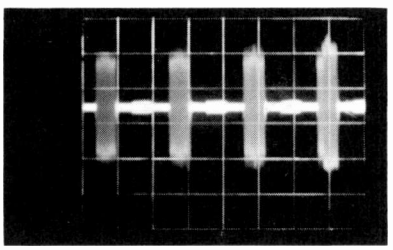
B. Q101 collector, 2 ms/cm, .05v/cm.



C. Q103 base, 2 ms/cm, .1v/cm.



D. Q104 base, 2 ms/cm, .1v/cm.



E. Q104 emitter, 2 ms/cm, .1v/cm.

Figure 52—Typical Waveforms, Delay Circuits, Playback Amplifier

tion. Since the operation and configuration of the delay circuits in the Playback Amplifiers are similar to their counterparts in the Record Amplifiers, they will not be covered as part of the Playback Amplifier description. For a discussion of the purpose and operation of the delay circuits, refer to the *Delay Section* under the *Record Amplifiers (modules A3-A6)* description, elsewhere in this book.

Since all four Playback Amplifier modules are identical, only one will be discussed.

Amplifier Circuit

In the PLAY mode the signal from the appropriate preamplifier channel on the Preamplifier (module 2A1) is coupled through C23 to the base of amplifier Q10. (See figure 50). The signal is terminated in 75 ohms at the input by R53. Variable peaking coil L2 in series with the collector load, R48, provides high frequency shunt compensation. The response of Q10 is adjusted at the factory, therefore the setting of L2 should not be disturbed unless a component affecting

the response of this stage is replaced. The output on the collector of Q10 is coupled through C21 to the base of amplifier Q9.

Amplifier Q9 contains a variable gain circuit which is controlled by the sensitivity switch (SENS SW), S2 in the emitter circuit. The SENS SW switch is an internal control which permits the gain of this stage to be changed by a fixed amount to accommodate the playback current requirements of the headwheel panel in use. With S2 in high (NO) position, as shown in figure 50, C20 is switched into the emitter circuit bypassing R44 so that maximum gain is obtained. When S2 is in the low (NC) position C20 is disconnected from the emitter and the degeneration introduced into the emitter by R44 reduces the gain of this stage 8 db.

The output on the collector of Q9 is direct coupled to the base of Q8, an emitter follower, which isolates Q9 from the succeeding amplifiers. The variable resistor, R38, in the emitter enables the FM level of each Playback Amplifier to be set individually so that the output of all four can be adjusted for equal amplitude. This control is a front panel screwdriver adjustment designated LEVEL. From the emitter of Q8, the signal is coupled through C16 to the base of amplifier Q7.

The output on the collector of Q7 is coupled through C13 to the base of Q6, another amplifier. These two transistors form a cascade amplifier. This configuration increases the amplitude of the signal to the desired level without sacrificing bandwidth. From the collector of Q6 the signal is coupled through C10 to the base of Q5, an emitter follower. Transistor Q5 isolates Q6 from the loading effects of the next stage, Q1. The output on the emitter of Q5 is coupled through C27 to the base of Q1, the equalizer.

The equalizer, Q1, is a high frequency amplifier employing shunt compensation, which is provided by variable peaking coil L1 in the collector circuit. Unless a component affecting the response of this stage is replaced, the setting of L1 should not be disturbed. The EQUAL potentiometer, R5, in the collector circuit is used to compensate for the difference in the frequency response of the individual heads. Turning R5 counterclockwise increases the response of the high frequency end of the FM band, which represents an increase in the response of the low end of the video band. The opposite occurs when R5 is turned clockwise. The response of the low end of the FM band is increased, representing an increase in the high frequency end of the video band. Optimum response is usually found with the pointer of the EQUAL control between 2 and 3 on the dial. These three conditions are illustrated in figure 53, which is a composite photograph of the response waveforms obtained with a sweep signal fed into the Video Preamplifier and observed at the output (TP1) of the Playback Amplifier. Equalization adjustments are made by means of a front panel control.

A pushbutton switch, S1, is located in the collector circuit of Q1 so that the individual playback channels can be identified. This switch is a front panel control designated CH ID. When the switch is pressed, the circuit parameters are changed. This will be evident when observed on a monitor, appearing as a change in the frequency response of a particular head. The CH ID switch should not be operated while the TR-4 is on the air, since bands will appear in the picture.

The compensated output from the collector of Q1 is dc coupled to the base of Q2, an emitter follower. From the emitter of Q2, the signal is fed through R100, C100 to the base of Q100, the input stage of the delay section. After passing through the circuits of the delay section, the signal is fed to the FM switcher (module A15).

Adjustments

To check the frequency response and the output level of the Playback Amplifiers, follow the procedure outlined below.

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) with a high gain amplifier and a low capacity probe.

Video sweep generator capable of sweeping 0 to 15 mc.

Calibrated rf attenuator network if sweep generator is not equipped with attenuator.

Module Extender.

Test Connector, RCA Stock No. 205330 or Amphenol No. 26-151.

1. Remove the power from the TR-4 by placing the equipment power circuit breaker, 1CB1, in the OFF position.

2. (a) Remove the Playback Amplifier to be swept (see chart, below) from the TR-4.

(b) Disconnect the coaxial input signal lead from pin P1-17.

(c) Check the position of the HI-LO sensitivity switch, S2. This is an internal control and for the first part of the response check, it should be in LO.

(d) Mount the Playback Amplifier in an extender and insert it in the TR-4.

3. (a) Connect the output of the sweep generator, using RG-59U coaxial cable, to the attenuator. Using the same type of cable, connect the output of the attenuator to the junction of C23, C25.

(b) Connect the low capacity probe from the oscilloscope to the junction of C27, R24.

4. Place the equipment power circuit, 1CB1, breaker in the ON position.

5. Set the sweep rate on the generator for 0 to 12 mc. Adjust the output of the sweep generator in combination with the attenuator to obtain a 50 mv signal at the junction of C23, C25.

6. Observe the oscilloscope and adjust coil L2 to obtain the flattest response.

7. Place circuit breaker, 1CB1, in the OFF position.

8. (a) Disconnect the attenuator lead from the junction of C23, C25, and the oscilloscope probe from the junction of C27, R24.

(b) Restore the HI-LO switch, S2, to its original position.

9. (a) Remove the extender from the TR-4.

(b) Remove the Playback Amplifier from the extender and reconnect the input signal lead to pin P1-17.

(c) Replace the Playback Amplifier in the TR-4.

10. Remove the Headwheel Panel from the Tape Transport Panel and plug the test connector into J1 on the Video Preamplifier. Disconnect the Limiter (module A16) from the recorder system by sliding it partly out of its slot.

11. Connect the output of the attenuator to the pin on the test connector corresponding to the channel driving the Playback Amplifier (see chart, below).

NOTE: Keep the ground lead formed by the braid on the signal cable as short as possible and make certain it is connected firmly to the frame of the TR-4 in close proximity to the test plug. Failure to exercise these precautions may cause the waveform display to appear distorted, resulting in an inaccurate representation of the response characteristics.

Channel No.	*Test Connector Pin No.*	*Playback Amplifier Module No.*
1	11	A11
2	5	A12
3	10	A13
4	2	A14

12. Terminate the appropriate input pin on the test connector in 75 ohms. Set the sweep rate on the generator for 0 to 12 mc. Adjust the output of the generator in combination with the attenuator to provide a 5 mv input signal to the Video Preamplifier. (If the generator is capable of an output of 2.5 volts peak-to-peak, 54 db of attenuation will furnish a 5 mv signal.)

13. Place circuit breaker, 1CB1, in the ON position.

14. Connect the low capacity probe from the oscilloscope to the test point on the Playback Amplifier associated with the channel being swept.

15. Adjust the EQUAL control, R5, to obtain a flat response. This is usually obtained with pointer of the control knob between 2 and 3 on the dial. Adjust the LEVEL control, R38, to obtain a .5 volt peak-to-peak output. The response curve should be $\pm$.5 db at 10 mc with respect to 5 mc.

16. Turn the EQUAL control, R5, fully ccw. The response should be the same as that shown in figure 53, with the peak occurring at 7.5 mc. This illustration is a composite photograph showing the appearance of the envelope with the EQUAL control turned to each extreme and then adjusted for a flat response. If the peak does not occur at 7.5 mc, remove the Playback Amplifier and adjust coil L1. Turning coil L1 ccw will shift the peak towards the high end of the band; turning it cw will shift the peak to the low end.

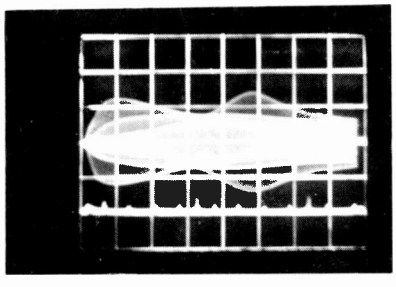


Fig. 53 Composite Waveform Showing Response of Playback Amplifier

NOTE: EQUAL control turned to each extreme then set between 2 and 3 on dial. 1 mc markers from 0 to 12 mc.

Figure 53—Composite Waveform Showing Response of Playback Amplifier

17. Repeat the foregoing procedure for the remaining Playback Amplifiers.

FM Switcher (Module A15)

General

The FM Switcher (refer to figure 54) combines the four separate FM channel outputs from the four Playback Amplifiers (modules A11-A14) into one continuous FM signal, which is then fed to the FM equalizer circuit in the Video/FM Control (module A21).

In the non-critical first switching stages, the four inputs are combined to form two outputs. Here the signals are fed in pairs, i.e., channels 1 and 3 and channels 2 and 4, from opposite sides of the headwheel into two diode gates. The gates are opened at the appropriate time by keying pulses. These pulses are generated in the two tonewheel rate (240/250 cps) multivibrators, Q13, Q14 and Q10, Q11, the latter being driven with delayed trigger.

The timing reference for the first or undelayed TW rate multivibrator, Q13, Q14, is established by a pulse (A, figure 55) derived from the Tonewheel Processor (module B15). This pulse occurs near the middle of head no. 1 due to the mechanical arrangement of the pulse-generating notch on the tonewheel in relation to the four heads.

Two pulse outputs are taken from the first TW rate multivibrator, Q13, Q14. The first output (B, figure 55) is used to key diode gate no. 2 which combines the FM input of channels 2 and 4 into a single channel (C, figure 55). The second pulse output is passed through a delay amplifier, Q12, which delays the pulse approximately 1000 microseconds (D, figure 55).

The delayed pulse is used to drive the second or delayed TW rate multivibrator, Q10, Q11. The output of this multivibrator (E, figure 55) keys diode gate no. 1 where the FM inputs of channels 1 and 3 are combined into a single output (F, figure 55). The output of each gate is fed to a separate emitter follower, each of which is followed by a diode quad. From gate 1 the output is fed to Q9 which drives quad Z2. Similarly, the output of gate 2 goes to Q1 and the latter, in turn, drives Z1. The quads, Z1 and Z2, are driven push-pull in phase opposition by 2 x TW rate (480/500 cps) pulses, to combine the two FM inputs into a single FM output. The gating input to the quads is generated in Q7, Q8, the ÷ 2 multivibrator or binary divider. The output from Q7, Q8 (K, figure 55) is passed through a three-stage feedback amplifier, Q3, Q4, and Q5, and then applied to the quads. Correct phasing of the pulse is obtained by triggering one side of the ÷ 2 multivibrator, Q7, Q8, with the tonewheel pulse, insuring that head no. 1 is keyed in when the tonewheel pulse occurs.

Switching between the quads takes place at the time the first sync pulse interval occurs during the period when two heads overlap in reading information from the tape. To confine the switching to the overlap region, a delayed 4 x Tonewheel (960/1000 cps) pulse is developed in the Tonewheel Processor (module B15). The delay of this pulse is controlled by the 4 x TW delay potentiometer on the Tonewheel Processor and the potentiometer is adjusted so that the pulse edge occurs during the overlap period.

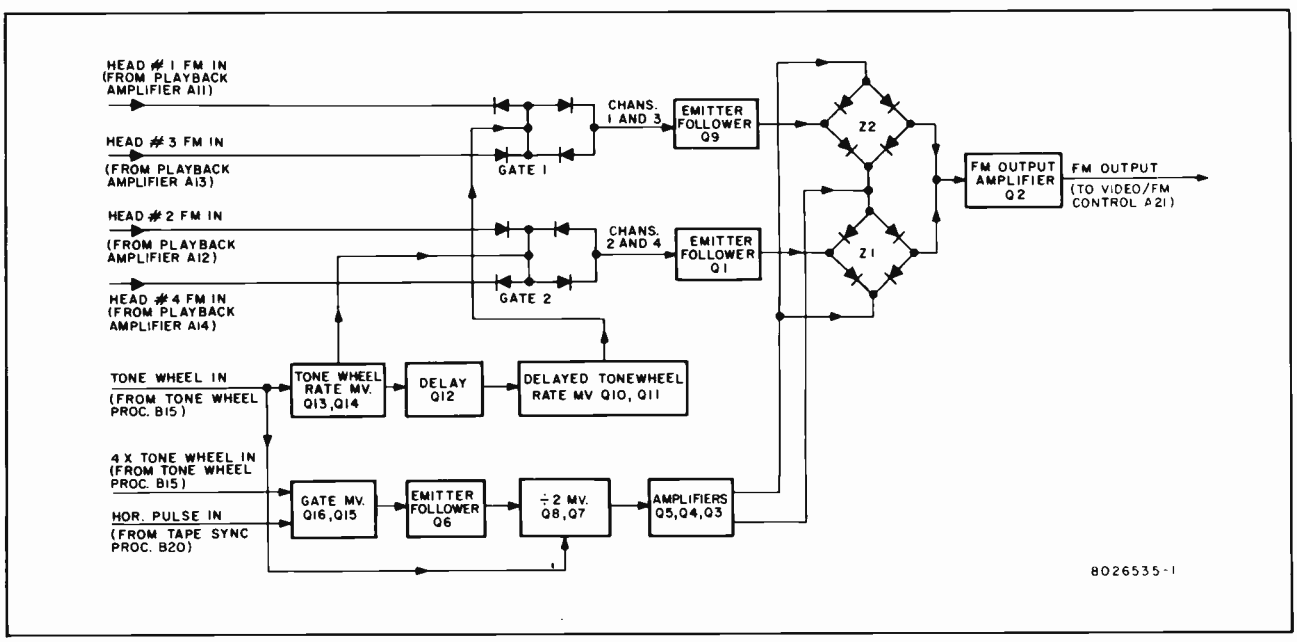


Figure 54—Block Diagram, FM Switcher Module

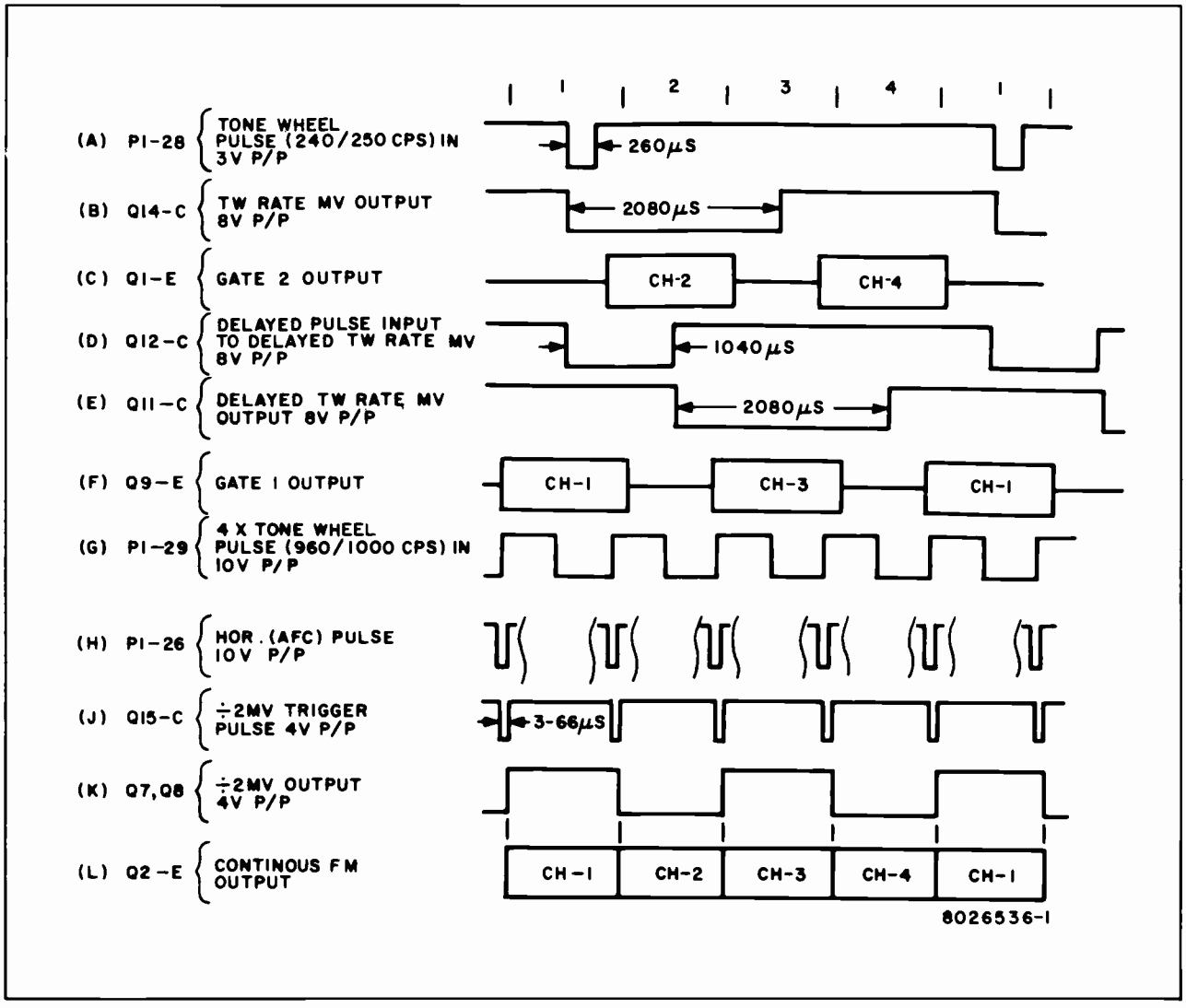


Figure 55—Idealized Waveforms, FM Switcher

The 4 x TW pulse (G, figure 55) is fed to the bistable gate multivibrator, Q15, Q16, causing it to change state. The gate (Q15, Q16) is then flipped to the opposite state by the first afc horizontal pulse (H, figure 55) arriving after the 4 x TW pulse. (The afc horizontal pulse is formed in the Tape Sync Processor (module B20). Once the gate has been flipped by this horizontal pulse, the continuing train of horizontal pulses will have no further effect on the gate, until another 4 x TW pulse arrives and causes the gate to again change state.

The output pulse from the gate (J, figure 55) is coupled through an emitter follower, Q6, to the ÷ 2 multivibrator, Q7, Q8. It is the positive-going trailing edge of this pulse, which is determined by the first horizontal pulse following the 4 x TW pulse, that triggers the ÷ 2 multivibrator.

The output of the ÷ 2 multivibrator, after passing through a three-stage amplifier, Q3, Q4, Q5, drives the two quads to combine their separate FM input signals into a single FM output signal. The single continuous FM output signal from the quads (L, figure 55) is fed to an emitter follower output stage, Q2, which couples the signal to the Video/FM Control (module A21).

Generating Diode Gate Keying Pulses

Figure 56 shows the circuits that form the keying pulses that drive the two diode gates. The tonewheel rate multivibrator, Q13, Q14, is a monostable multivibrator, with Q13 off and Q14 on in the stable state. A pulse from the Tonewheel Processor (module B15) is coupled through steering diode CR20 to Q13, turning it on. The on period of Q13 is determined by the length of time C29 takes to charge through R67, which

is approximately 2000 microseconds. From the collector of Q14, the output pulse, slightly integrated by C18 and R42, is fed to diode gate no. 2, where channels 2 and 4 are combined. The output pulse from the collector of Q13, the other half of the multivibrator, is fed to Q12, the delay stage, cutting it off. (The delay stage is a standard boxcar* circuit.) The delay interval, which is approximately 1000 microseconds or one head wide, is determined by C28 discharging through R63. The positive-going edge of the pulse appearing on the collector of Q12 is used to trigger the delayed tonewheel rate multivibrator, Q10, Q11. This is a monostable multivibrator, identical to Q13, Q14. The input trigger is fed to the base of Q11, turning off this normally on transistor. The output pulse for keying diode gate no. 1, where channels 1 and 3 are combined, is taken off the collector of Q11 and coupled through an integrator consisting of C39 and R43 to the gate.

* *See Basic Circuit Descriptions on page 128.*

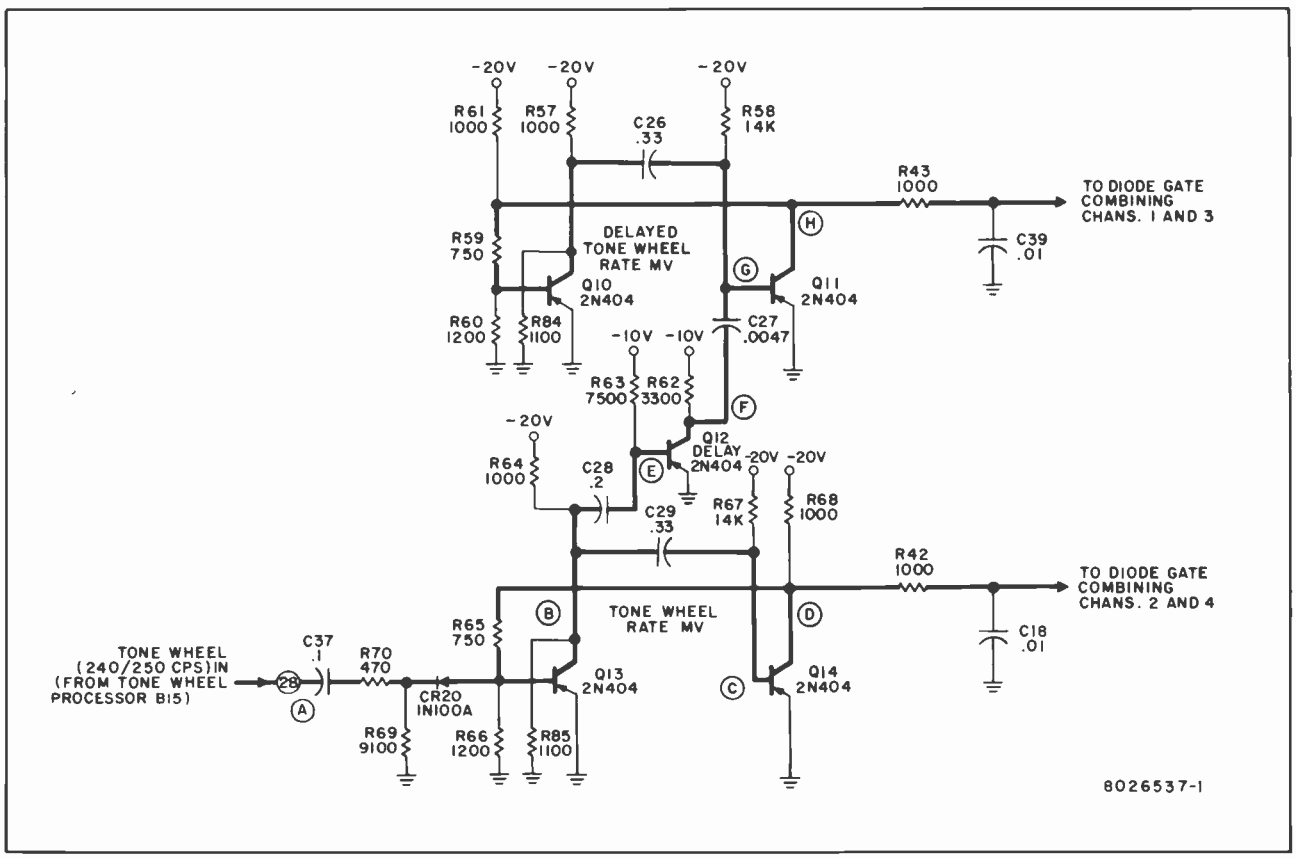
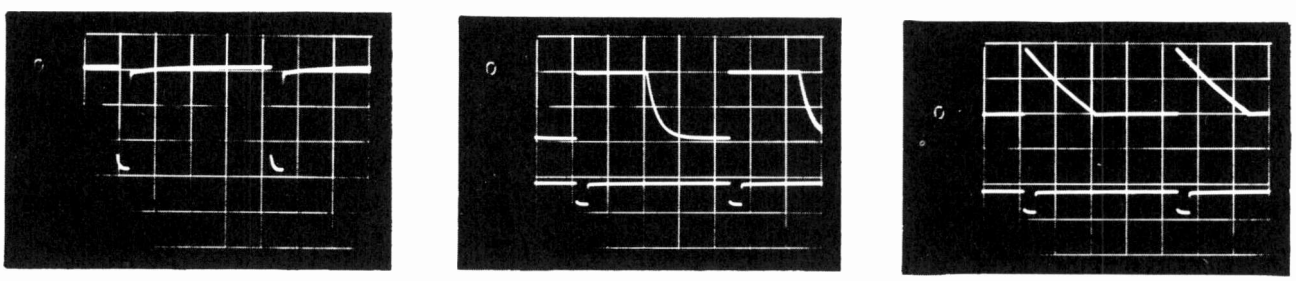


Figure 56—Tonewheel Rate Multivibrators and Delay Circuits

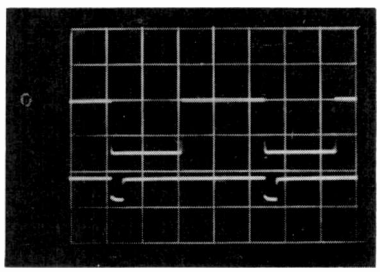


A. P1-28, tone wheel pulse, 1 ms/cm, 1v/cm.

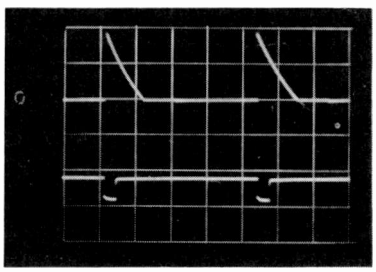
B. Top: Q13 collector, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.

C. Top: Q14 base, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.

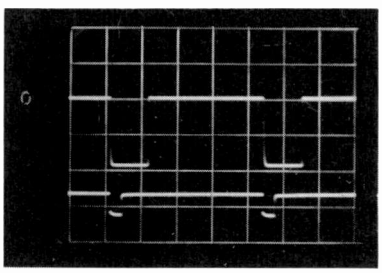
Figure 57—Typical Waveforms, Tonewheel Rate Multivibrators and Delay Circuits



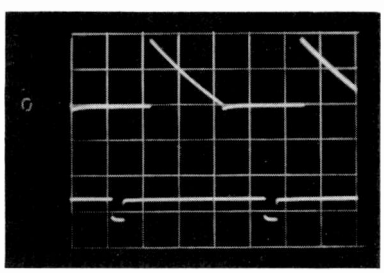
D. Top: Q14 collector, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.



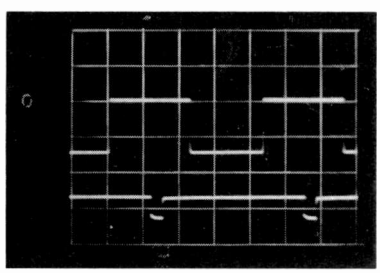
E. Top: Q12 base, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.



F. Top: Q12 collector, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.



G. Top: Q11 base, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.



H. Top: Q11 collector, 1 ms/cm, 5v/cm. Bottom: Tone wheel reference.

Figure 57—(Continued)

Diode Gates

The two diode gates are shown in figure 58. The output pulses from the tonewheel rate multivibrator, Q13, Q14, are applied to gate no. 2 at the junction of R5 and R6. During the negative half of the cycle, CR2, CR4 conduct, and CR1, CR3 are cut off, thus allowing FM input from channel 2 to pass. On the positive half of the cycle, diodes CR1, CR3 conduct while CR2, CR4 are cut off, and the FM input from channel 4 is passed. As a result of each pair of diodes switching on and off, one combined signal appears at the output. The output of the gate is coupled through

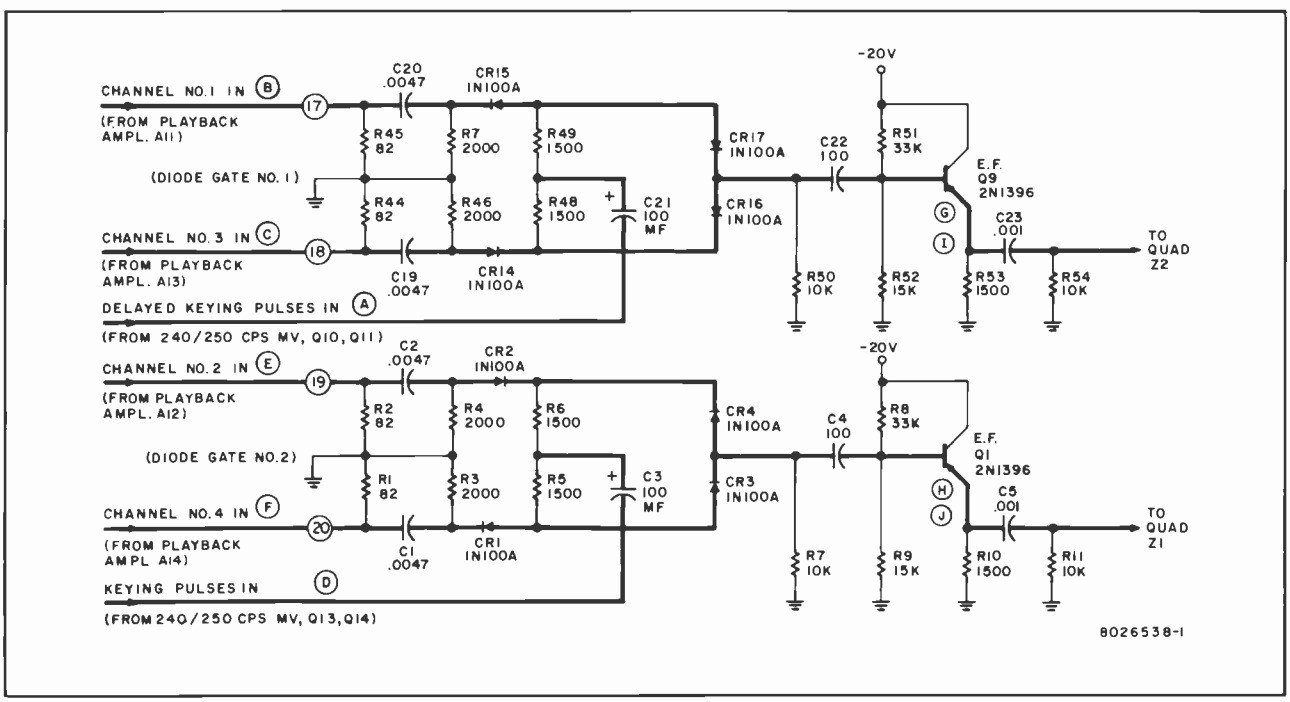
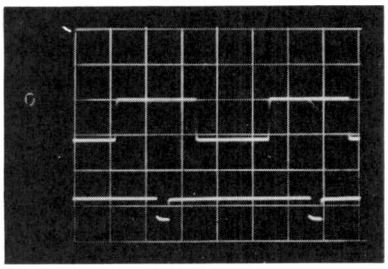
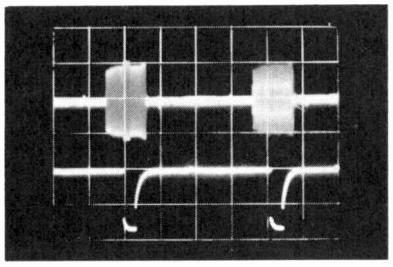


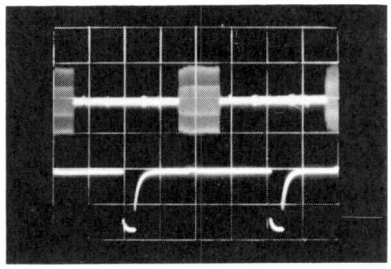
Figure 58—First Gating Stage, 4 x 2 Channel Switching and Emitter Follower Circuits



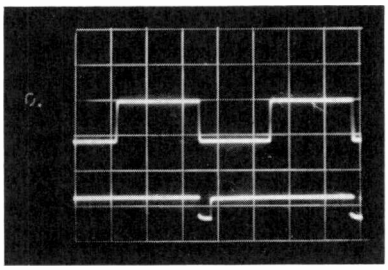
A. Top: Junc. C21, C39, R43, delayed keying pulses, 1 ms/cm, 5v/cm.
Bottom: P1-28, tone wheel reference.



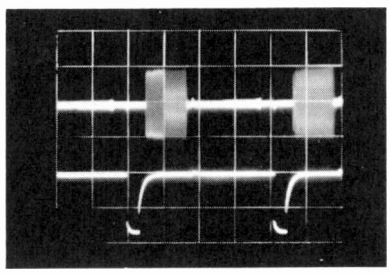
B. Top: P1-17, head #1FM, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



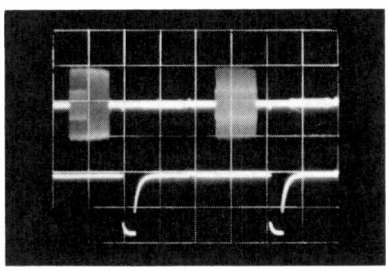
C. Top: P1-18, Head #3 FM, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



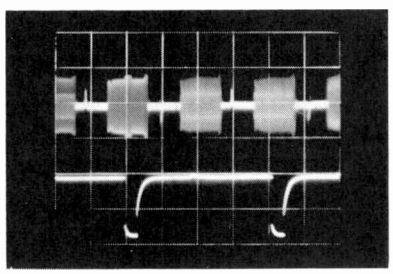
D. Top: Junc. C3, C18, R42, keying pulses, 1 ms/cm, 5v/cm.
Bottom: Tone wheel reference.



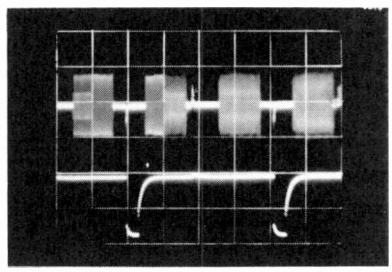
E. Top: P1-19, head #2 FM, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



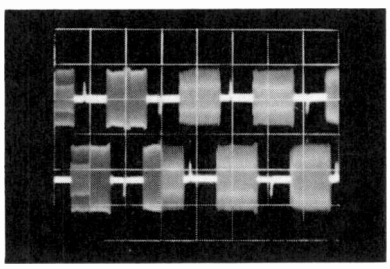
F. Top: P1-20, Head #4 FM, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



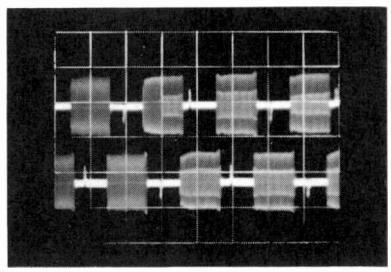
G. Top: Q9 emitter, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



H. Top: Q1 emitter, 1 ms/cm, .2v/cm.
Bottom: Tone wheel reference.



I. Top: Q9 emitter, 1 ms/cm, .2v/cm.
Bottom: Q1 emitter, 1 ms/cm, .2v/cm.



J. Top: Q1 emitter, 1 ms/cm, .2v/cm.
Bottom: Q9 emitter, 1 ms/cm, .2v/cm.

Figure 59—Typical Waveforms, First Gating Stage, 4 x 2 Channel Switching and Emitter Follower Circuits

C4 to an emitter follower, Q1. The output from the emitter of Q1 is coupled through C5 to one side of quad Z1.

Diode gate no. 1, which combines the input of channels 1 and 3, is identical to gate no. 2, except that the keying pulses originate in the delayed tonewheel rate multivibrator Q10, Q11. These pulses are delayed approximately 1000 microseconds or one head period so that they will occur during the time interval of heads 2 and 4. Similarly, the output of gate no. 1 is fed to an emitter follower, Q9, the output of which is coupled through C23 to quad Z2.

Timing of Quad Keying Pulses

The timing of the pulses used to key the quads is critical. Switching must take place during the first horizontal sync interval that occurs in the overlap region when two video heads are in contact with the tape. Switching at this time prevents any transients that might occur from being seen, and enables the redundant information read by two heads overlapping to be eliminated. The bistable gate (960/1000 cps) multivibrator, Q15, Q16, (figure 60) acts as a gate to ascertain the time this coincidence takes place. One input to Q15 is the 4 x TW (960/1000 cps) pulse, which originates in the Tonewheel Processor (module B15). This pulse is timed by adjusting the 4 x TW DELAY control on the Tonewheel Processor to coincide with the overlap period. If this control is not properly adjusted, gaps or overlaps will occur in the switching. The effect of this will be to cause noise to appear on the picture monitor every sixteen lines.

The pulse is differentiated by C30 and R73 and the positive spike is coupled through CR21 to turn off Q15 and turn on Q16. The multivibrator remains in this state until Q16 is triggered off by the trailing edge of a horizontal sync pulse, which is generated in the afc horizontal multivibrator in the Tape Sync Processor (module B20). The afc circuit advances the pulse so that switching coincides with the horizontal sync interval of the video signal. It is necessary to advance the

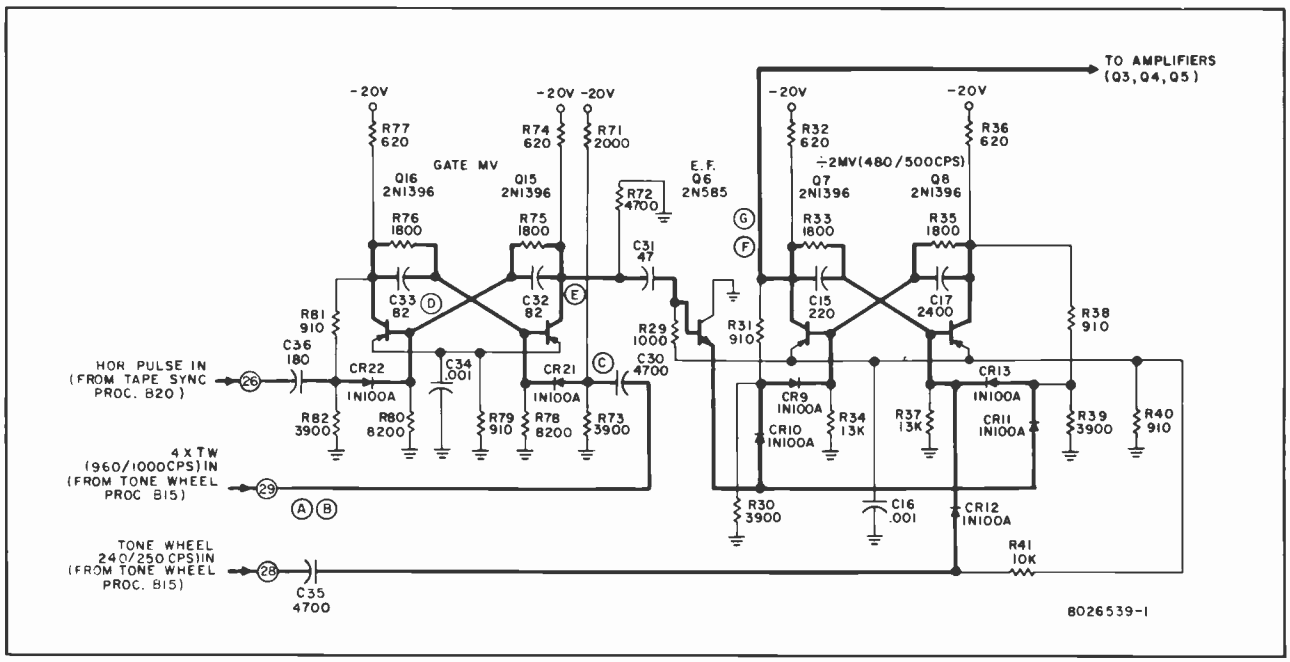
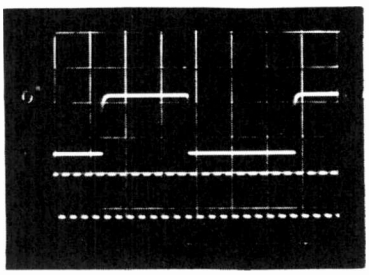
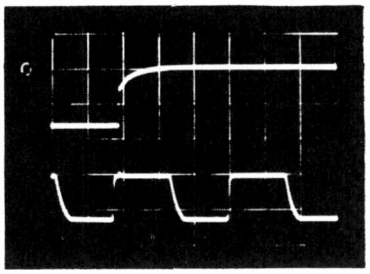


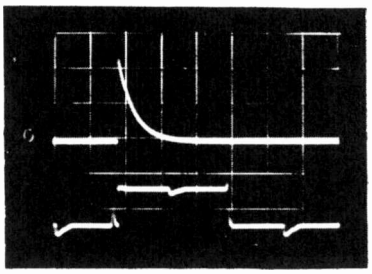
Figure 60—Gate Multivibrator and ÷ 2 Multivibrator Circuits



A. Top: P1-29, 4 x TW, .2 ms/cm, 5v/cm. Bottom: P1-26, horizontal pulse, .2 ms/cm, 10v/cm.

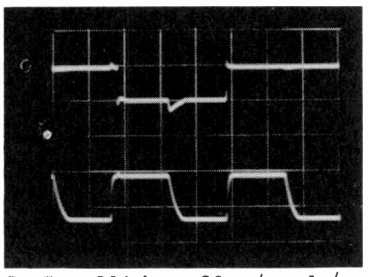


B. Top: P1-29, 4 x TW, 20 μs/cm, 5v/cm. Bottom: P1-26, hor. pulse, 20 μs/cm, 10v/cm.

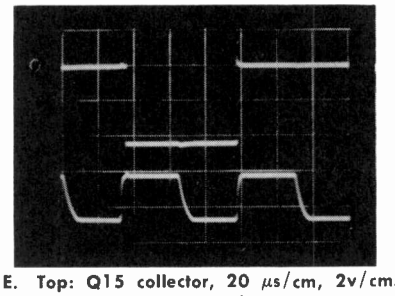


C. Top: Junction C30, R71, R73, 20 μs/cm, 2v/cm. Bottom: Junction C36, R81, R82, 20 μs/cm, 2v/cm.

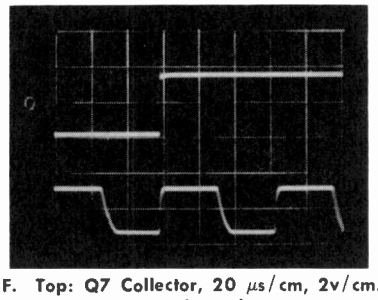
Figure 61—Typical Waveforms, Gate Multivibrator and ÷ 2 Multivibrator Circuits



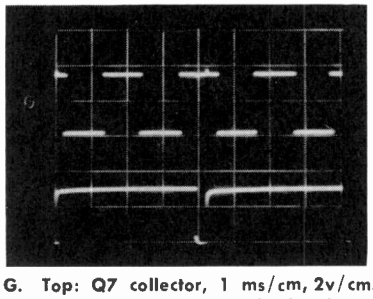
D. Top: Q16 base, 20 μs/cm, 1v/cm. Bottom: Hor. pulse reference.



E. Top: Q15 collector, 20 μs/cm, 2v/cm. Bottom: Hor. pulse reference.



F. Top: Q7 Collector, 20 μs/cm, 2v/cm. Bottom: Hor. pulse reference.



G. Top: Q7 collector, 1 ms/cm, 2v/cm. Bottom: P1-28, tone wheel pulse reference.

Figure 61—(Continued)

pulse to compensate for the delays encountered in the FM demodulation process used in recovering the video component and then separating sync from the video. The degree of pulse advance is variable and is set by adjusting the TAPE HOR FREQ SET control on the Tape Sync Processor, so that switching takes place immediately following the leading edge of sync.

The horizontal sync pulse input to Q16 is differentiated by C36 and R82 and coupled through CR22 to the base of Q16. The initial positive spike turns off Q16 and turns on Q15. The subsequent pulses have no effect on Q16 and the multivibrator remains in this state until another 4 x TW pulse arrives to trigger Q15 and then the cycle is repeated. The output pulse, at a 4 x TW rate, is taken off the collector of Q15. This pulse is of variable width, depending on when a horizontal pulse arrives after the 4 x TW pulse. The output pulse is differentiated by R72 and C31 and applied to emitter follower Q6.

The positive spike from the emitter of Q6 is fed through steering diodes to both sides of the binary divider, Q7, Q8 (see figure 60) which supplies the keying pulses to the quads. Each positive trigger causes the multivibrator to change state, resulting in a ÷ 2 action taking place. Diodes CR9 and CR13 serve as gates that conduct alternately so that the input trigger is applied first to one side cutting it off and then to the other side. To prevent phase ambiguity and to maintain the correct phase relationship so that the gate for channel 1 causes quad Z2 to conduct, the differentiated positive spike of the tonewheel pulse (240/250 cps) is fed to one side (Q8) of the multivibrator to insure it is turned off during head no. 1 interval. Phasing is established at the beginning of the cycle so the multivibrator remains correctly phased thereafter. The output of the ÷ 2 multivibrator is a 2 x TW rate pulse (480/500 cps) which is taken off the collector of Q7 and applied through Z3 to the input of the amplifier stages (see figure 62). Z3, a pair of back-to-back diodes, clips the pulse before it enters the amplifier.

The amplifier stage consists of Q5, Q4, and Q3 which forms a feedback amplifier to provide drive for the two quads, Z1 and Z2. Two pulse outputs are taken from Q3, one from the emitter, the other from the collector. Each pulse output is fed to both quads (see figure 64), driving them in phase opposition so that when one quad is conducting the other is nonconducting. This back-and-forth switching action between the quads results in the two separate FM inputs being combined into a single continuous output. The

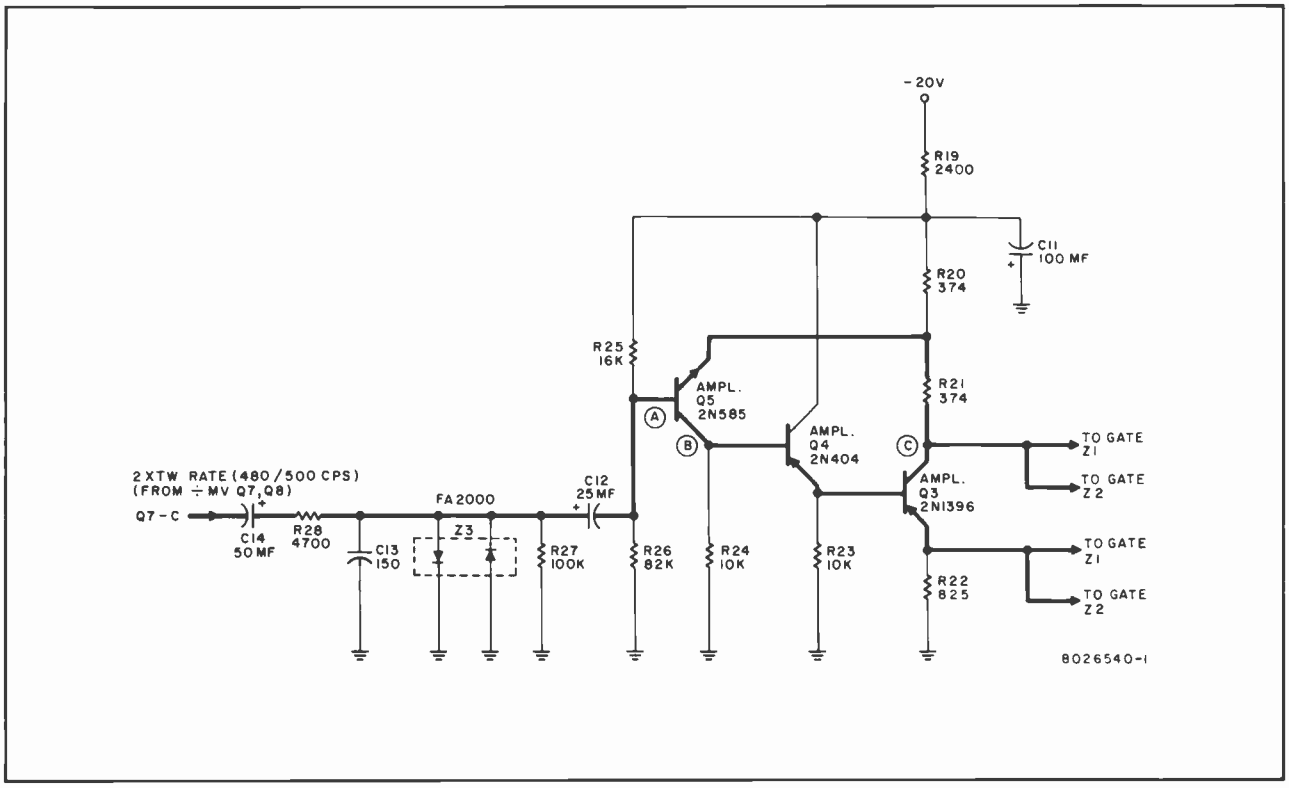
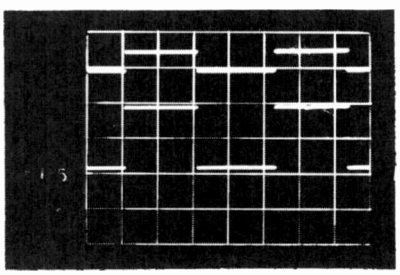
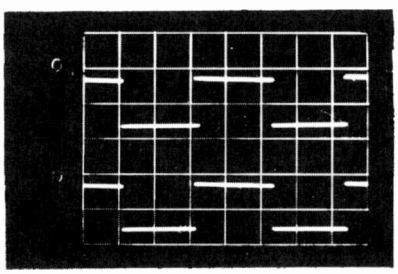


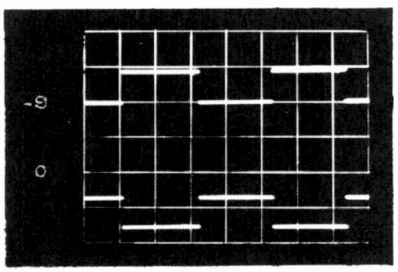
Figure 62—2 x TW Rate Amplifier Circuits



A. Top: Q5 base, .5 ms/cm, 2v/cm
Bottom: Q7 collector reference



B. Top: Q5 collector, .5 ms/cm, 2v/cm
Bottom: Q4 emitter, .5 ms/cm, 2v/cm



C. Top: Q3 collector, .5 ms/cm, 2v/cm
Bottom: Q3 emitter, .5 ms/cm, 2v/cm

Figure 63—Typical Waveforms, 2 x TW Rate Amplifier Circuits

output is fed to Q2, an emitter follower, which drives the line to the FM equalizer circuit in the Video/FM Control (module A21).

When the TR-4 is in the Record or Setup modes of operation, the FM output of the quads is turned off. The circuit that controls the on-off functioning of the quads is composed of CR23, C40, R86, and R87 (see figure 64). In the Record or Setup modes, +70 volts is switched on in the Regulator (module C20) and this develops a positive bias across R87. This positive potential is sufficient to offset the reverse bias applied to CR23 by the negative potential developed across R86 from the −20 volts. With the reverse bias overcome, CR23 conducts and any output from the quads will pass to ac ground through the path provided by C40.

When the TR-4 is in the Play mode, the +70 volts is switched off and CR23 will be cut off due to the reverse bias applied to it from the −20 volts across R86. Thus, in this mode, the signal appearing at the output of the quads will follow the path going to Q2, the FM Output amplifier.

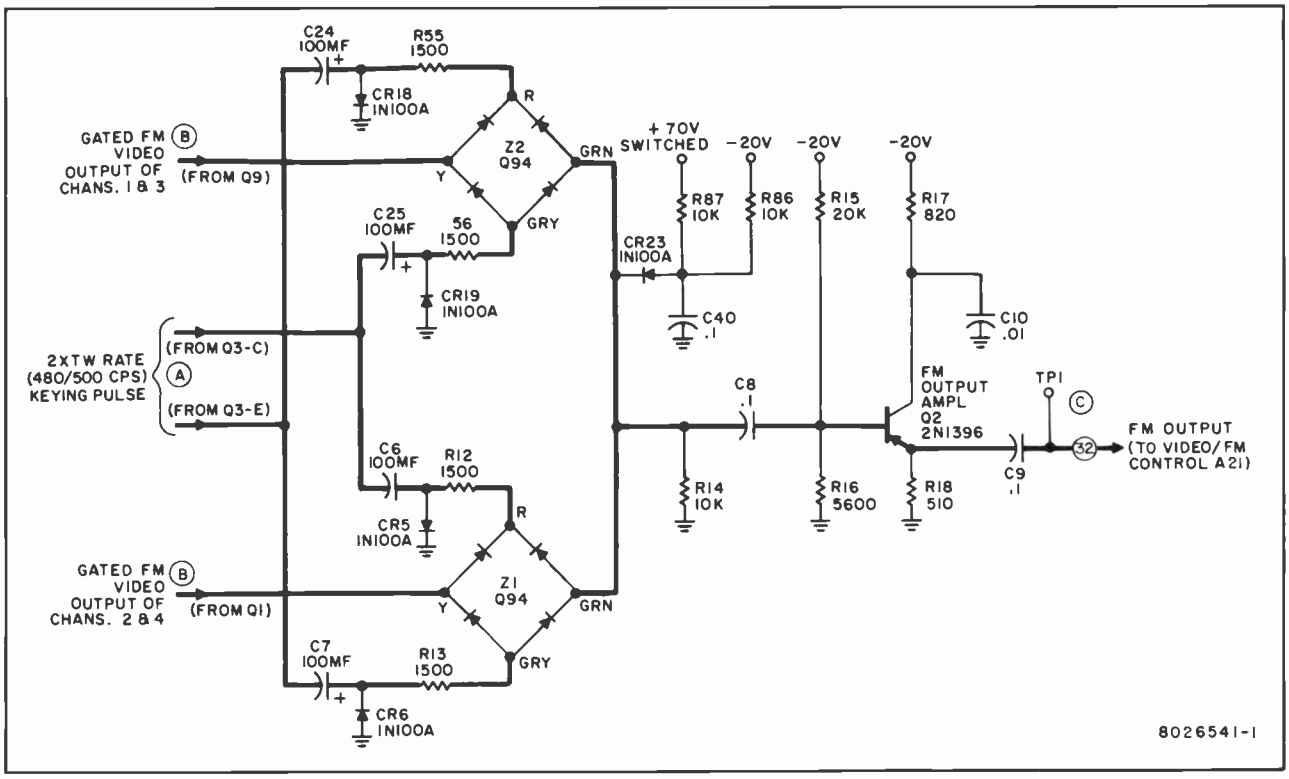
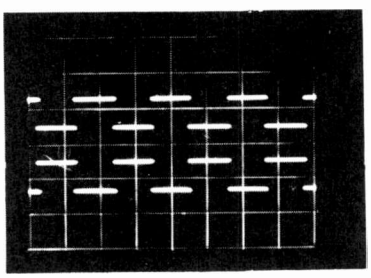
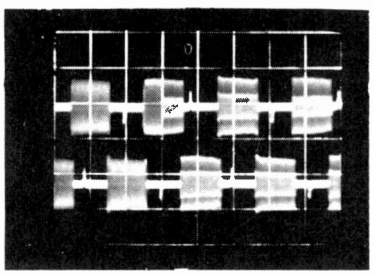


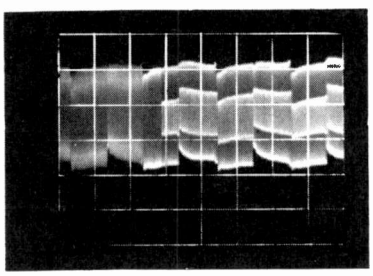
Figure 64—Second Gating Stage, 2 x 1 Switching and FM Output Circuits



A. Top: Q3 collector, 1 ms/cm, 2v/cm.
Bottom: Q3 emitter, 1 ms/cm, 2v/cm



B. Top: Q1 emitter, 1 ms/cm, .2v/cm
Bottom: Q9 emitter, 1 ms/cm, .2v/cm



C. P1-32, FM output, 1 ms/cm, .2v/cm

Figure 65—Typical Waveforms, Second Gating Stage, 2 x 1 Switching and FM Output Circuits

Video/FM Control (Module A21)

Note: The Video/FM Control module consists of two separate circuit sections, each functionally independent of the other. One is the FM equalization circuit and the other is the video control circuit. The circuit descriptions of the video system modules are arranged in the same sequence that the signal takes in passing from module to module. (See *Simplified Video Functional,* figure 1). In keeping with this arrangement, the description of the video control circuit is covered later, along with the other modules in the Signal Processing Group.

FM Equalizer Section

The FM equalizer circuit supplements the action of the individual channel equalizers in each of the Playback Amplifiers (modules A11-A14). This circuit enables the overall response of the FM signal to be adjusted to compensate for the loss of low frequency components encountered in the head to tape transfer.

The FM equalizer (figure 66) consists of an input amplifier, Q12, a shunt peaked equalizer, Q13, followed by two FM line drivers, Q15 and Q16, in cascade, and an FM detector, Q17. Each of the line drivers

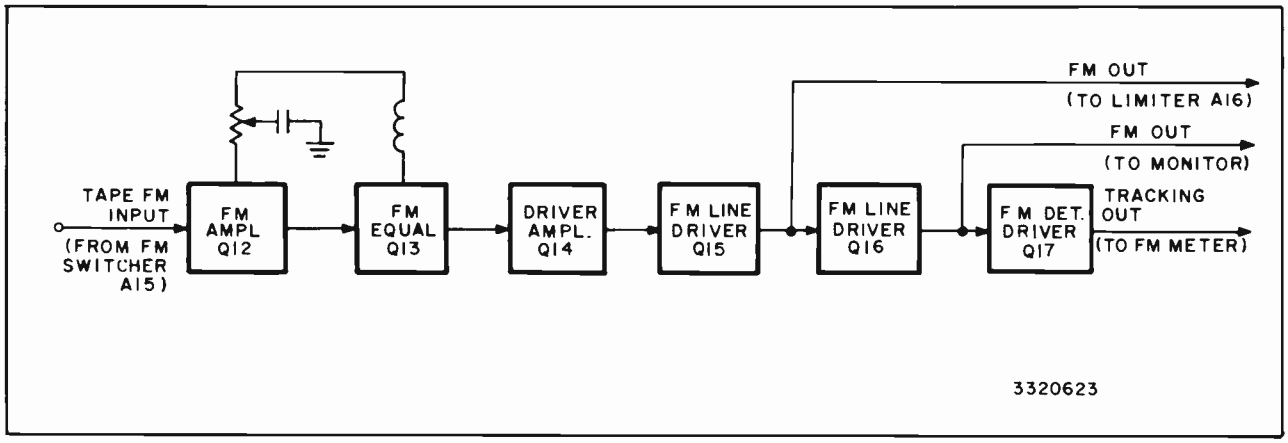


Figure 66—Block Diagram, FM Equalizer Section of Video/FM Control Module

feed a separate FM output line, and the output of the detector is fed to a peak-to-peak detector that furnishes a control signal used in tracking the phase of the heads during playback.

As shown in figure 67, tape FM from the FM Switcher (module A15) is coupled through C25 to the base of amplifier Q12, an emitter follower. The input signal is terminated in 75 ohms by R50. The output on the emitter of Q12 is coupled through R53 and C28 to the emitter of the equalizer, Q13, a common base amplifier. The high frequency compensation coil, L2, in the collector circuit of Q13 is adjusted to produce a peak at 8 mc. The frequency response of this circuit can be varied by rotating potentiometer R52 back and forth, as shown in figure 68. Potentiometer R52 is a front panel control designated FM EQUAL. When the FM EQUAL control is in the extreme ccw position, the response at the high end of the FM band is increased, which represents a boost in the low end of the video band. When the FM EQUAL control is turned fully cw, the circuit produces a relatively flat response over the range of the FM band.

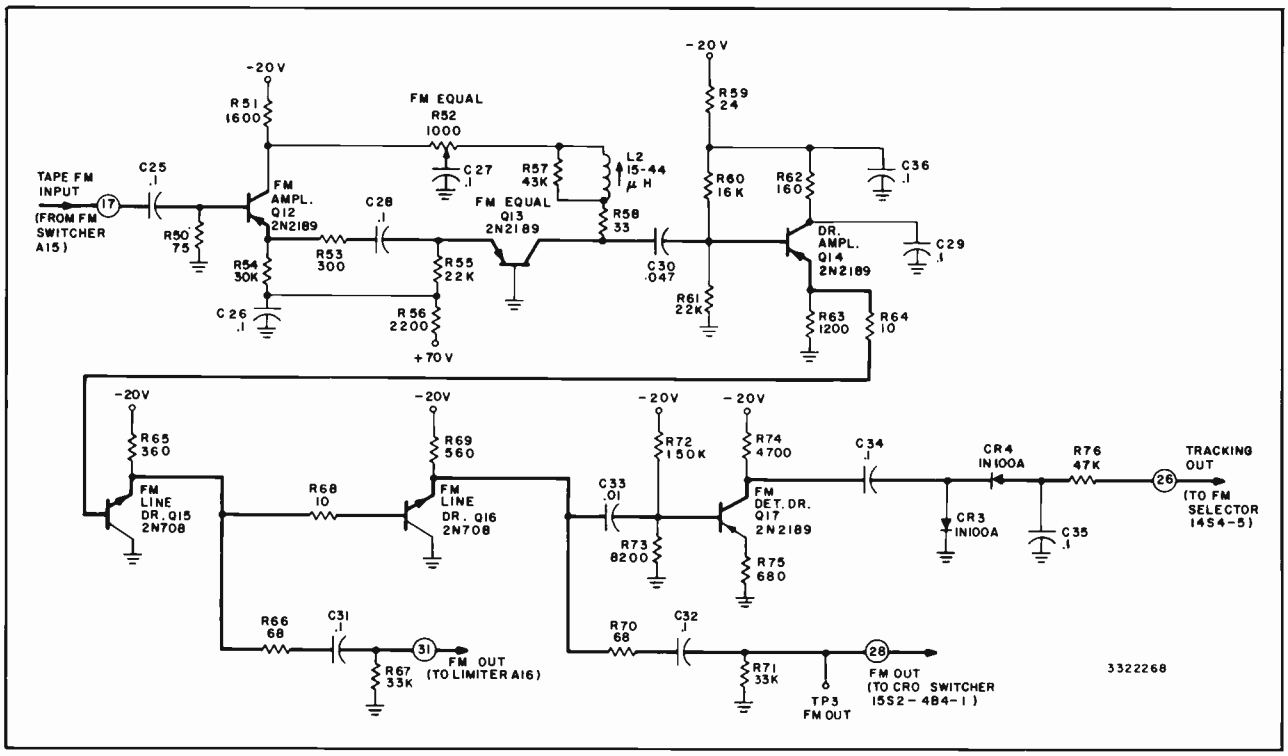


Figure 67—FM Equalizer, FM Line Drivers and FM Detector Circuits (Video/FM Control Module)

The signal on the collector of Q13 is coupled through C30 to the base of the driver amplifier, Q14, an emitter follower. From the emitter of Q14, the amplified signal is dc coupled across R64 to the base of the first FM line driver, Q15, an emitter follower. Two outputs are taken off the emitter of Q15. One is sending-end terminated in 68 ohms by R66 and coupled through C31 to the FM output line that feeds the Limiter (module A16). The other output is dc coupled by R68 to the base of the other line driver, Q16, an emitter follower.

Two outputs are also taken off the emitter of Q16. One is sending-end terminated in 68 ohms by R70 and coupled through C32 to drive the FM output line which goes to the SW OUT contact (15S2-4B4-1) on the CRO switcher. The other output is coupled through C33 to the base of Q17, the FM detector driver. The amplified output on the collector of Q17 is fed to a peak-to-peak detector consisting of CR3, CR4, and C35.

This circuit provides a rectified sample of the FM playback signal, which is used as a tracking signal in conjunction with the CT PHASE control (4R2) on the PLAY control panel to obtain the proper phase relationship between the heads and the individual playback channels. The tracking signal is fed through contact 5 of the FM SELECTOR switch (14S4) on the RECORD control panel to the FM LEVEL meter (4M2) on the PLAY control panel.

By observing the FM LEVEL meter when the TR-4 is in PLAY mode, the CT PHASE control can be adjusted to shift the longitudinal position of the tape while it is in motion with respect to the heads. Since the TRACKING signal being fed to the meter represents the magnitude of the FM playback signal, when the meter reading is maximum the tape and heads are properly phased.

Adjustments

As a matter of convenience, two methods of checking the frequency response of the FM equalizer circuit are given below. The first method permits the Video/FM Control module to remain in the TR-4 by taking the response measurements at the appropriate terminals on the Video/FM Control module connector block at the rear of the TR-4. With the second method, the response measurements can be made from the front of the TR-4 by mounting this module in an extender. It is possible, however, that the wiring in the extender may cause additional capacitance to be introduced into the module circuitry which may slightly affect the adjustment covered in the second method.

Recommended Test Equipment

Tektronix Type 535 oscilloscope (or equivalent) with low capacity probe.

Video sweep generator capable of sweeping 0 to 15 mc.

Calibrated rf attenuator network if sweep generator is not equipped with attenuator.

One 75-ohm terminating resistor.

First Method

1. Remove the power from the TR-4 by placing the equipment power circuit breaker, 1CB1, in the OFF position.

2. Remove pins 17 and 31 from their respective rectangular terminals in connector A21 on the rear of the TR-4. Use two pairs of long nose pliers for this purpose, one to hold the terminal in place in the connector block and the other to remove the pin from the terminal. Pull the pin out carefully while simultaneously applying sufficient pressure to the terminal to support it against the force of the withdrawing pin.

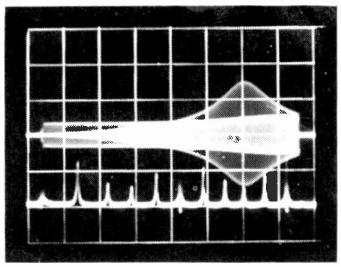
3. Connect the output of the sweep generator to the attenuator. Connect the output of the attenuator using RG-59U coaxial cable to terminal 17. Connect the ground braid on the input end of the coaxial cable to pin 1 on the connector.

4. Set the sweep rate of the generator for 0 to 10 mc, and adjust the output to obtain a .2 volt peak-to-peak signal at terminal 17, as measured on the oscilloscope.

5. Terminate the output of the FM equalizer circuit by connecting the 75-ohm resistor across terminals 31 and 15. Connect a low capacity probe from the oscilloscope input to terminal 31; fasten the ground lead to terminal 15, keeping it as short as possible.

6. Place the equipment power circuit breaker, 1CB1, in the ON position.

7. Turn the FM EQUAL control, R52, fully ccw. The response should be the same as that shown in figure 68, with the peak occurring at 8 mc. (This illustration is a composite showing the response waveforms when R52 is turned to either extreme.) If the peak appears below or above 8 mc, coil L2 will have to be adjusted until the response peaks at 8 mc. The latter adjustment will have to be on a trial and error basis, since coil L2 is an internal control. The module will have to be removed, coil L2 adjusted, the module then replaced and the waveform observed on the oscilloscope to determine the effectiveness of the adjustment. Turning L2 ccw will shift the peak towards the high end of the band; turning L2 cw will shift the peak



NOTE: FM EQ control turned to each extreme. 1 mc marker from 0 to 10 mc.

Figure 68—Composite Waveform Showing Response of FM Equalizer Circuit (Video/FM Control Module)

towards the low end of the band. Repeat adjustment if necessary.

8. Turn the FM EQUAL control, R52, fully cw. A response similar to that shown in figure 68 should be obtained.

9. Replace pin 31 in its terminal and remove pin 28. Use the same technique described in step 2 for removing the pin. Terminate the output by connecting the 75-ohm resistor across terminals 28 and 12. Connect a low capacity probe from the oscilloscope input to terminal 28; fasten the ground lead to terminal 12, keeping it as short as possible.

10. Check the response and output level at this point, with R52 first fully cw and then fully ccw. The level of the output signal at terminal 28 may be of the order of 10% lower than the output at terminal 31.

11. Replace pins 17 and 28.

Second Method

1. Place the module in an extender, and disconnect the coaxial cable on the input side of C25 within the module. Connect the output of the sweep generator to the attenuator; then connect the output of the attenuator using RG/59U coaxial cable to the input side of C25 and ground.

2. Set the sweep rate of the generator for 0 to 10 mc, and adjust the output to obtain a .2 volt peak-to-peak signal at C25, as measured on the oscilloscope.

3. Terminate the output by connecting the 75-ohm resistor from the junction of C31 and R67 to ground; then connect a low capacity probe from the oscilloscope to the junction of C31 and R67.

4. Disconnect the Limiter (module A16) from the TR-4 by sliding it partly out of its slot. This is necessary in order to prevent double termination.

5. Turn the FM EQUAL control, R52, fully cw then fully ccw. The response should be the same as that shown in figure 68, with the peak occurring at 8 mc. (This illustration is a composite showing the response waveforms when R52 is turned to either extreme.) If the peak appears below or above 8 mc, adjust coil L2 until the response is peaked at 8 mc.

6. Disconnect the terminating resistor from the junction of C31 and R67, and replace the Limiter module in the TR-4.

7. Disconnect the coaxial cable from the junction of C32 and R71 and terminate this junction in 75-ohms.

8. Connect the probe to the junction of C32 and R71. The response at this point with R52 fully ccw then fully cw should be the same as that obtained in step 5; however, the output level may be of the order of 10% lower than the output at the junction of C31 and R67.

9. Restore the coaxial lead connections at C25 and at the junction of C32 and R71.

Limiter (Module A16)

General

The Limiter module amplifies the input from either of two sources, the Record FM signal from the Modulator (module A2) or the Tape FM signal from the FM equalizer circuit in the Video/FM Control (module A21).

As shown in the block diagram, figure 69, the Limiter consists of an input selection relay (K1) with relay driver, an interlocking relay (K2), three push-pull limiter stages, a phase combiner and two output stages comprising a demodulator driver and an R-F Copy output.

The three limiter stages are similar. Each stage is a differential amplifier, with each half of the amplifier coupled by an emitter follower to the succeeding stage. The gain is approximately 26 db per stage, with overall limiting of at least 55 db for 1 volt input. To insure symmetrical clipping, a balance control is employed in the first limiter stage. The push-pull output from the final limiter is fed to a phase combiner. The output of the phase combiner is a single phase signal that goes to the two emitter follower output stages. One drives the line to the Demodulator (module A17) and the other feeds the R-F Copy line.

Circuit

Input Signal Selection

The function of K1 (figure 70) is to select either the record FM signal or the tape FM signal from the play-

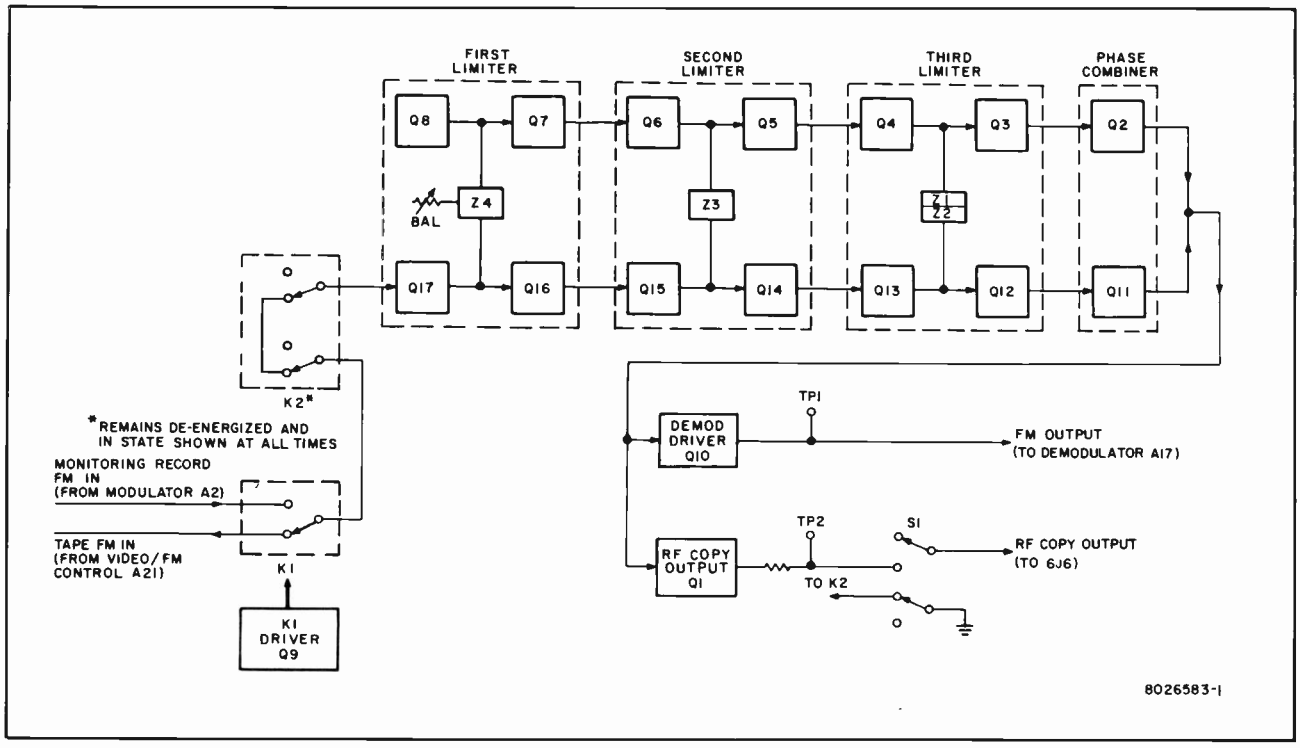


Figure 69—Block Diagram, Limiter Module

back circuits. When the TR-4 is in the RECORD or SETUP mode of operation, K1 selects record FM; in the PLAY mode, K1 selects tape FM. If the TR-4 is in STANDBY, WIND, or STOP modes, K1 will select either record FM or the zero signal output of the video heads. The choice between these two signals is determined by the position of the MOD-PLAY switch, which is an internal control on the Modulator (module A2). For a detailed discussion on the operation of this switch, see sections entitled *—20 Volts Electronic Switch* and *MOD-PLAY Switch* under *Modulator (module A2)* description.

Relay K2 is not connected to any source of power, therefore remains de-energized at all times. Relay K2 serves merely to feed the signal selected by K1 to the first stage of limiting.

With the input selection relay, K1, and relay K2, de-energized, as shown in figure 70, K1 would accept the Tape FM signal from the Video/FM Control module that appears on pin 18 of the Limiter connector. The signal would go through K1 to K2. The signal would follow the path through the jumpered contacts on K2 to the base of Q17, the input of the first limiter.

When K1 is energized, the Record FM signal from the Modulator module is applied to K1 through pin 19 on the Limiter connector. From K1 the signal goes through the still-closed loop provided by K2 to the base of Q17 via C29.

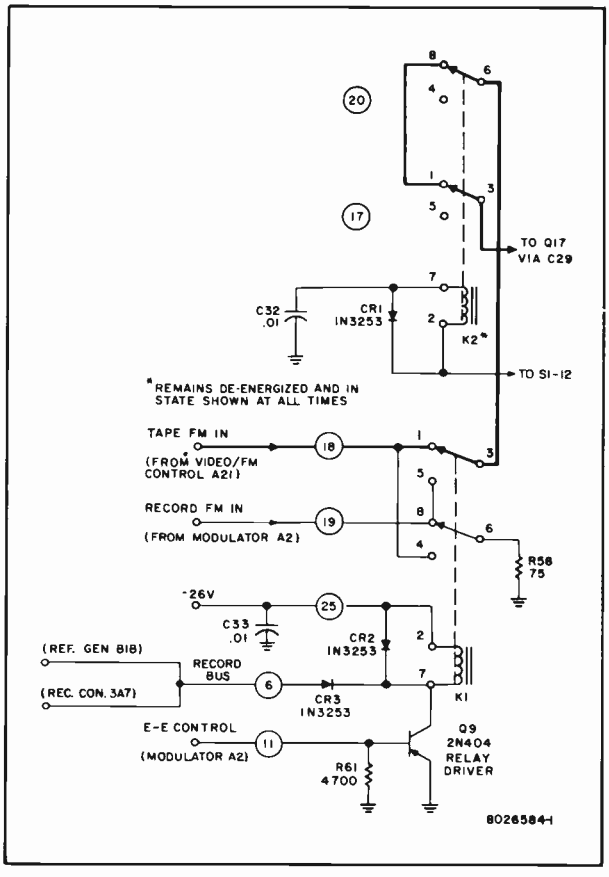


Figure 70—Input Signal Selection Circuit

Regardless of the state of K1, the coaxial input lines are properly terminated at all times by R58 (figure 70) and by R55 (figure 71). The former terminates the unused signal input line to K1 and the latter provides input termination of the signal being applied to the base of Q17, the input of the first limiter.

The input selection relay, K1, is controlled by the relay driver, Q9, or the RECORD/SETUP bus. In the STANDBY, WIND or STOP modes with the MOD-PLAY switch in the MOD position, negative voltage from the E-to-E bus saturates Q9, driving the collector to ground. This energizes K1 and it switches to the Record FM input. In the RECORD or SETUP modes, the RECORD/SETUP bus is grounded and this supplies the ground return to the coil of K1 through CR3. Again K1 is energized and switches to the Record FM input signal.

Limiters, Phase Combiner, and Output

Since the three limiter stages are similar, with the exception of the balance control circuit in the first limiter stage, only the latter will be covered in the following discussion (see figure 71).

Transistors Q8 and Q17 form the two halves of a push-pull stage generally known as a differential or emitter coupled amplifier. As mentioned earlier, the incoming signal, Tape FM or Record FM, is coupled through C29 to the base of Q17. The input signal is distributed across both halves of the amplifier by coupling the signal on the emitter of Q17 through C26 and R47 to the emitter of Q8.

The push-pull signals on the collector of Q8 and Q17 are clipped close to their ac axes by the pair of back-to-back diodes in Z4 (see figure 73). Each diode

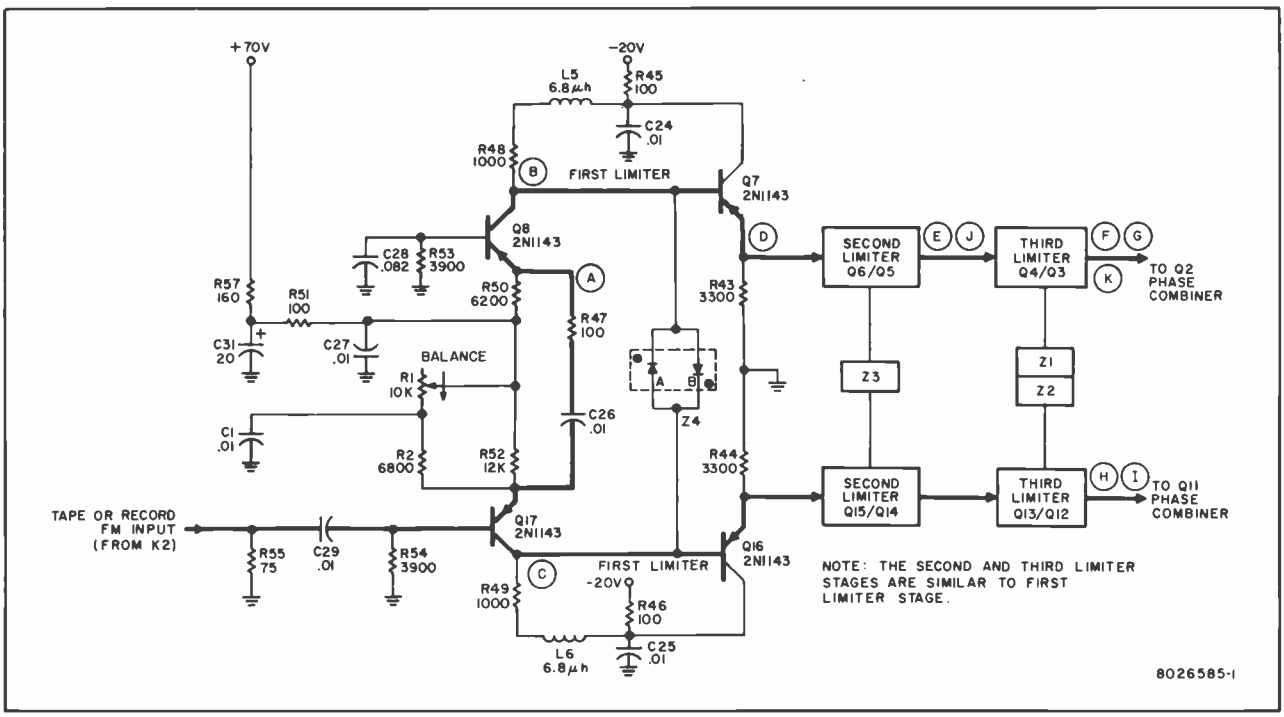
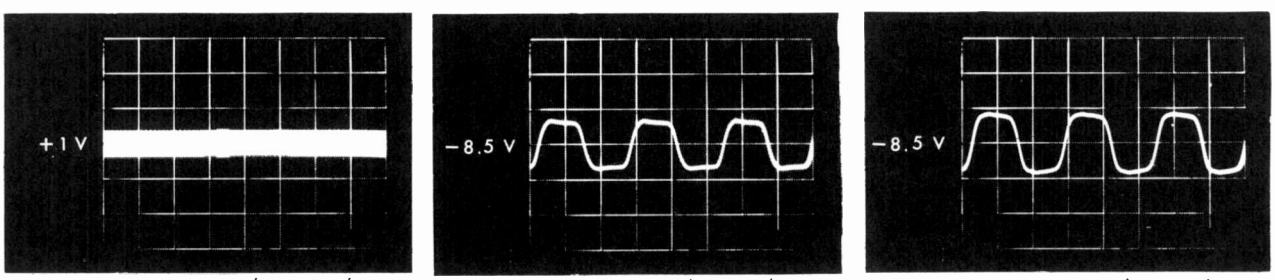


Figure 71—Amplifier and Clipper Circuits

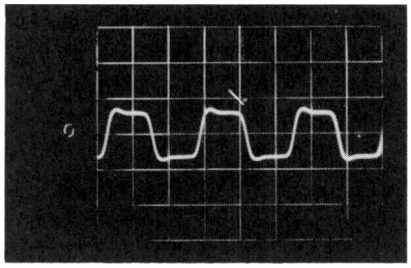


A. Q8 emitter, .5 ms/cm, .05v/cm

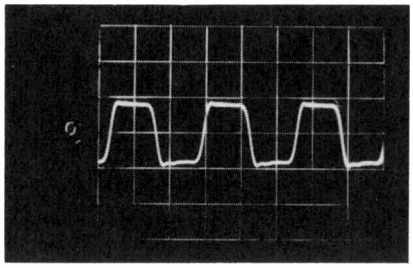
B. Q8 collector, .1 μs/cm, .5v/cm

C. Q17 collector, .1 μs/cm, .5v/cm

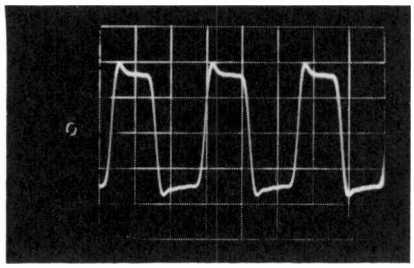
Figure 72—Typical Waveforms, Amplifier and Clipper Circuits



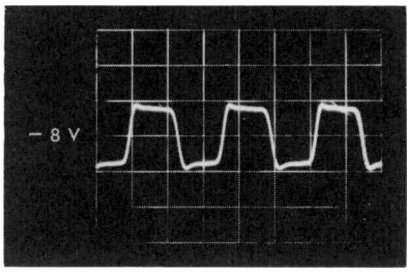
D. Q7 emitter (Q16 emitter inverted), .1 μs/cm, .5v/cm



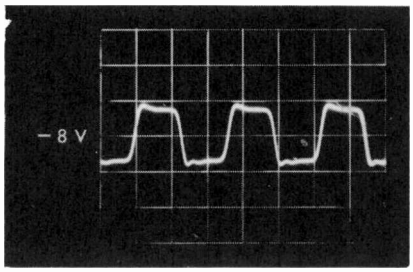
E. Q5 emitter (Q14 emitter inverted), .1 μs/cm, .5v/cm



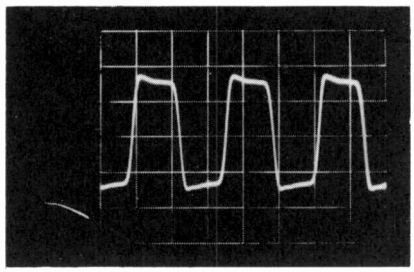
F. Q3 emitter (Q12 emitter inverted), .1 μs/cm, .5v/cm



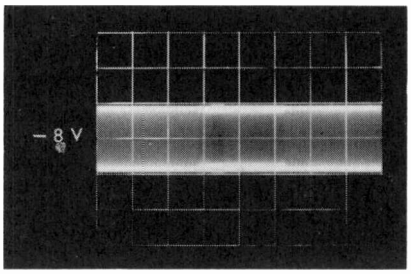
G. Q3 emitter, .1 μs/cm, 1v/cm



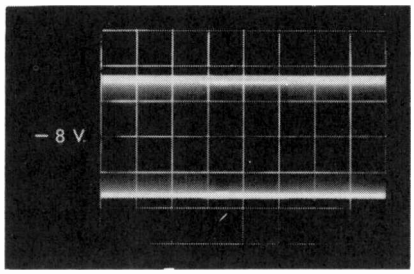
H. Q12 emitter, .1 μs/cm, 1v/cm



I. Q12 emitter/Q3 emitter, .1 μs/cm, 1v/cm



J. Q5 emitter, .5 ms/cm, .5v/cm



K. Q3 emitter, .5 ms/cm, .5v/cm

Figure 72—(Continued)

conducts alternately on the half cycles when the amplified input signal causes the collector-to-collector potential to exceed the forward conduction voltage of the diodes, which is approximately 1 volt. When the diodes conduct, the signal swing on each collector is limited and the positive and negative peaks are clipped at approximately 0.5 volt. The clipped output from each half of the first limiter is coupled to the succeeding stage through emitter followers, with Q8 driving Q7 and Q17 driving Q16. In the remaining two limiter stages, the signal is further amplified and clipped. In second limiter, clipping again takes place at the 0.5 volt level, but in the final limiter, two pairs of diodes are used in series so the clipped output is twice this level.

The BALANCE control, potentiometer R1, is a front panel screwdriver adjustment. This control is used to set the bias between both halves of the amplifier, in order to establish symmetrical clipping of the

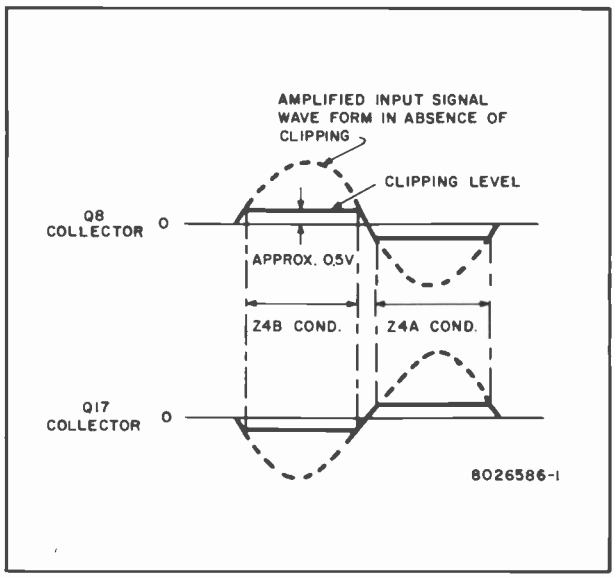


Figure 73—Waveforms Showing Conduction Cycle of First Limiter Diodes

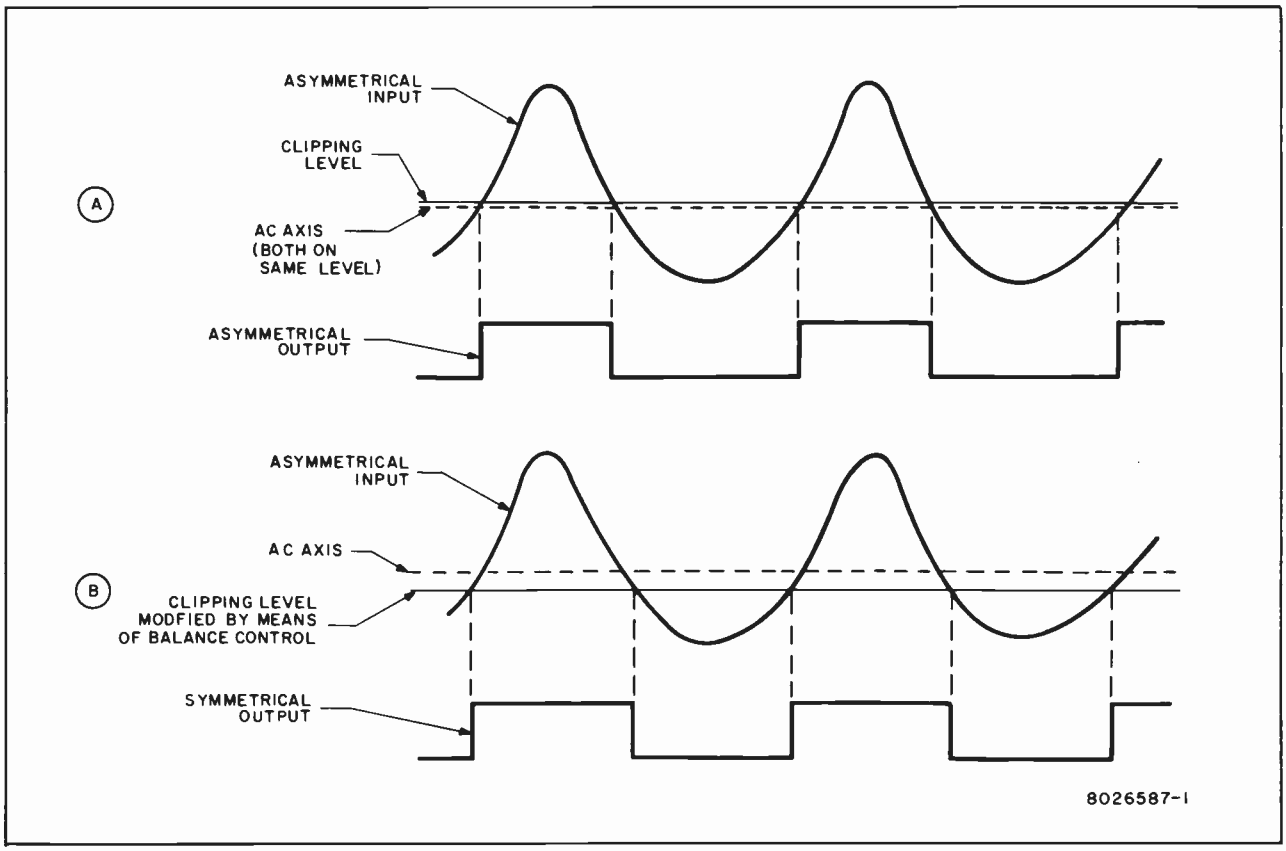


Figure 74—Balance Control Operation

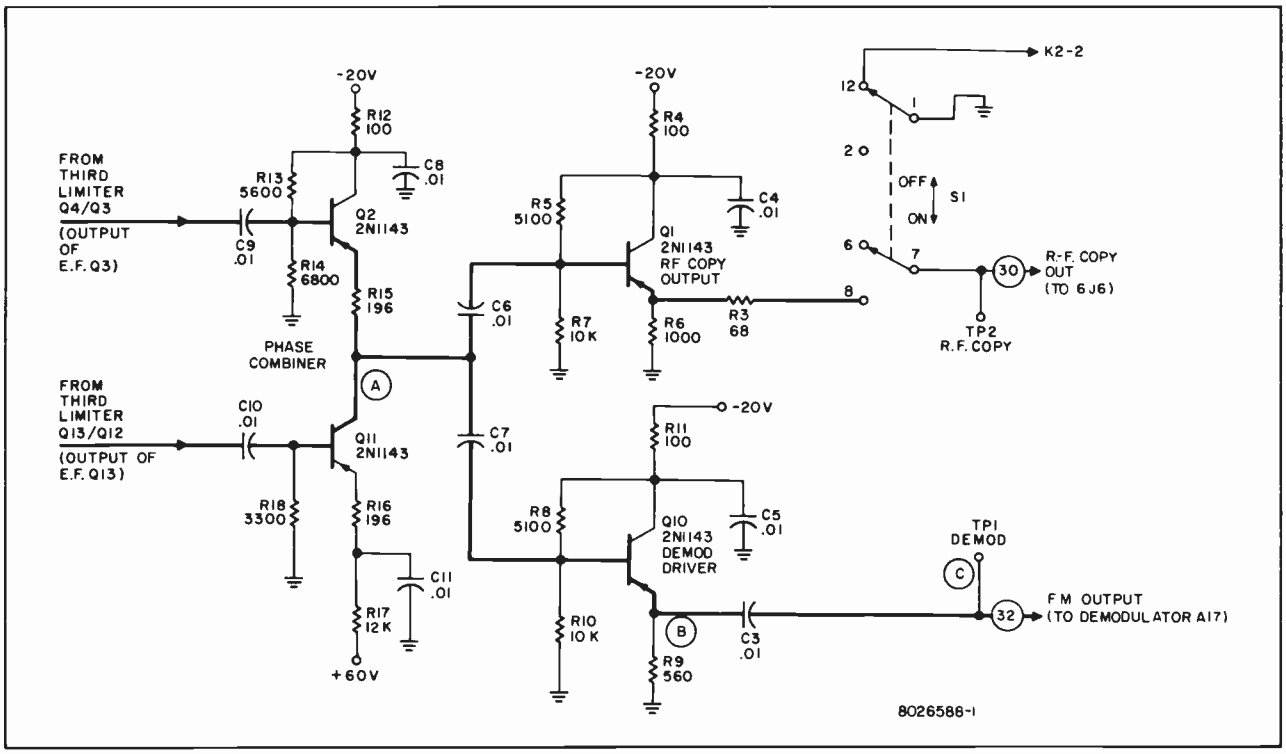
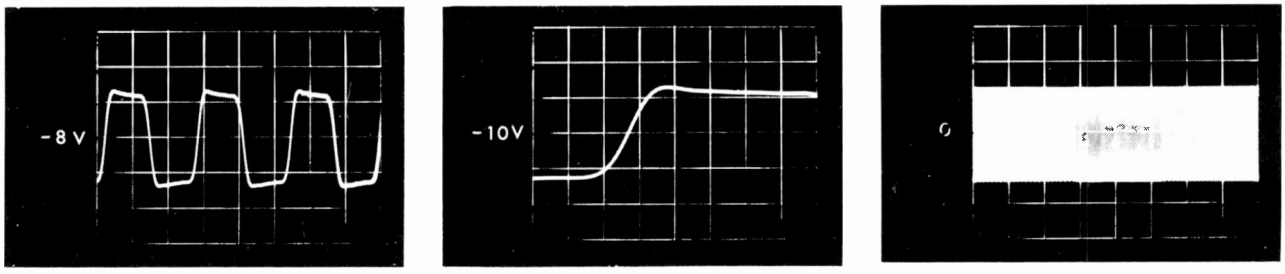


Figure 75—Phase Combiner, R-F Copy and Demodulator Driver Circuits



A. Q11 collector, .1 μs/cm, 1v/cm B. Q10 emitter, .02 μs/cm, 1v/cm C. TP1, .5 ms/cm, 1v/cm

Figure 76—Typical Waveforms, Phase Combiner, R-F Copy and Demodulator Driver Circuits

amplifier output signal. When the input signal is symmetrical, the setting of the BALANCE control is such that the combined resistance of R1, R2, and R52 in the emitter of Q17 is approximately equal to that of R50 in the emitter of Q8. Should the input signal be asymmetrical (A, figure 74), the BALANCE control can be adjusted to vary the bias on Q17, so as to shift the relation between the ac axes of the signal with respect to the clipping level to achieve a symmetrical output, as shown in B, figure 74. Symmetrical output is necessary for proper operation of the Demodulator (module A17).

The push-pull output of the third limiter is coupled to the bases of the phase combiner transistors Q2 and Q11 (see figure 75). Although at any instant the signal on the base of Q2 is opposite in phase to that on Q11, phase reversal between the input and output to each half of the phase combiner takes place only in Q11. Therefore at the output junction between the two halves of the phase combiner, the signals are added to form a single phase output. This signal then goes to the two emitter follower output stages Q1, the RF Copy output, and Q10, the demodulator driver.

The output impedance of Q1 and the 68-ohm series resistance of R3 provide a source impedance of 75 ohms for the RF Copy output, which is available at 6J6. The RF Copy output level is nominally 1 volt when the TR-4 is driving a 75-ohm load. The demodulator drive signal is fed at a 2-volt level to the Demodulator (module A17) where video information is subsequently recovered from the FM signal.

Demodulator (Module A17)

General

The Demodulator detects the video information contained in the FM output of the Limiter (module A16). As shown in the block diagram, figure 77, the incoming FM signal is coupled through an emitter follower and then split into two branches, one delayed, the other undelayed. The signal in both branches is fed to similar pairs of phase splitters. Except for the phase shift encountered by the delayed signal, both signals are identical when applied to their respective phase splitters. The output signal from each of the four phase splitters is coupled through an individual discriminator driver to form the gating input to the diode discriminator.

The configuration of the discriminator is such that each diode will conduct, in turn, during the time a delayed and an undelayed signal are both positive. Since two positive signals, one delayed, the other undelayed, are required for a diode to conduct, the output of the discriminator will be a series of constant-width positive pulses at twice the frequency of the input signals. However, the interval between the output pulses is inversely proportional to the frequency of the gating signals. Thus as the frequency of the gating signals increases, the interval between the output pulses becomes smaller, causing the average energy content to become increasingly positive. Conversely, as the frequency of the gating signals decreases, the interval between the pulses becomes greater and their average contents becomes less positive. The pulse output of the discriminator is fed through a buffer stage to either of two emitter followers, which serve as drivers for two separate filters.

Only one filter channel is used at a time. The channel in use is determined by the standards on which the TR-4 is being operated. The filter in channel one meets the frequency requirements for domestic standards. The filter in channel two is used for operation on international standards, and is designed to pass frequencies of a slightly higher order than those encountered on domestic standards. Filtering removes unwanted residual high frequency components, supplying a signal at the output that is a varying dc average of the pulse input. Since the dc variations in the filtered signal are proportional to the frequency of the input pulses, the output signal is a replica of the original video modulating signal.

The output of the appropriate filter is fed to its respective video amplifier. The amplified output is then coupled by an emitter follower to the video line driver, which feeds the line to the Demodulator Output (module A18).

Circuit

Phase Splitters

The incoming FM signal (figure 78) from the Limiter (module A16) is terminated in 75 ohms by R1 and coupled through C1 to the base of Q1, an emitter follower. Two outputs are taken off the emitter of Q1. One is coupled through C5 to the base of Q3, which together with Q4 forms a phase splitter pair. The other output signal is first passed through delay circuitry before being applied to a similar pair of phase splitters, Q12, Q13. The delay is needed in order to obtain properly phased gating signals with which to drive the diode discriminator. (This will be demonstrated later.)

The signal entering the delay branch from the emitter of Q1 is fed across R15 to the base of Q2, the delay line driver, an emitter follower. From the emitter of Q2, the signal is coupled through C4 to P1-20, where it enters the delay cable. The latter is of such length as to provide a delay of approximately .03 microseconds. The output of the delay cable is applied via P1-27 to the emitter of Q10, a common base amplifier.

Both ends of the delay line are terminated in 75 ohms. At the receiving end, 75 ohms is obtained by the 68 ohms of R8 in combination with the emitter impedance of Q2. And, similarly, at the receiving end, the 68 ohms of R36 together with the emitter impedance of Q10, appears as 75 ohms to the signal.

The loss in level incurred by the signal due to the terminations at the input and the output of the delay cable is recovered in Q10. The output signal on the collector of Q10, now restored to the same level as that appearing on the base of Q1, is coupled through C23 to the base of Q11, an emitter follower. From the emitter of Q11, the signal is coupled through C25 to the base of Q12, which, in combination with Q13, forms the other phase splitter pair. Other than the phase shift caused by the .03 microseconds delay, the signal appearing on the base of Q12 is the same as the undelayed signal appearing on the base of Q3.

Since the phase splitter circuits in each branch are identical, only one, Q3 and Q4, will be discussed. The operation of Q3, Q4 is similar to that of a differential amplifier. Transistor Q3 is a common emitter amplifier and Q4 is a common base amplifier. The emitters of these two transistors are ac coupled through R10 and C17. With this arrangement, the bias conditions between the two transistors are such that one conducts when the signal is positive and the other conducts when the signal is negative. A positive going signal on

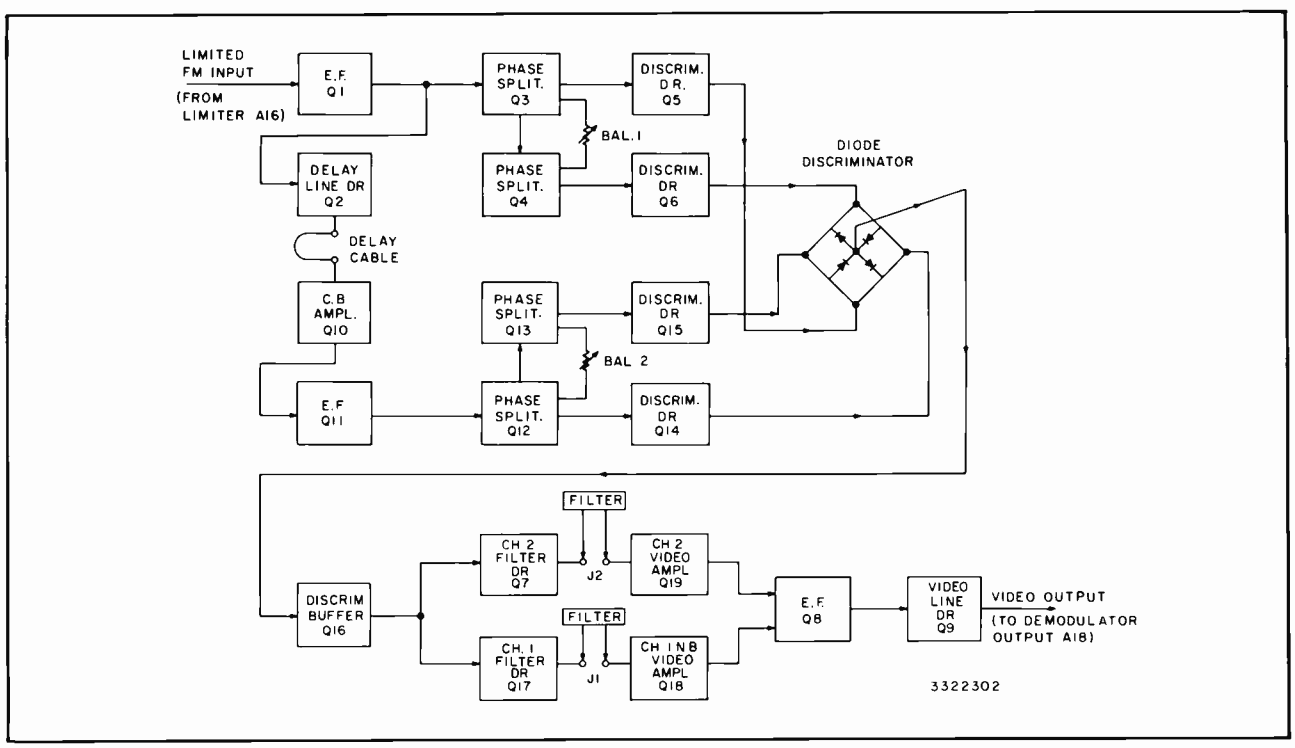


Figure 77—Block Diagram, Demodulator Module

the base of Q3 forward biases this transistor causing it to conduct. At this time a replica of the same signal appears on the emitter of Q3, and hence is also present on the emitter of Q4 by virtue of the ac coupling between these two elements. However, since this is a positive going signal, it reverse biases Q4, cutting off the latter. When the signal on the base of Q3 goes negative the opposite occurs. Transistor Q3 becomes reverse biased and is cut off. Therefore the signal representing reverse bias on the emitter of Q4 is no longer present and this transistor conducts. The resultant output available at the collectors of Q3 and Q4 is two signals 180° out of phase.

Connected in series between load resistors R11 and R13 in the collectors of Q3 and Q4, respectively, is a potentiometer, R12, designated BAL-1. Likewise in the collector circuits of Q12 and Q13 is a similar potentiometer, R53, designated BAL-2.

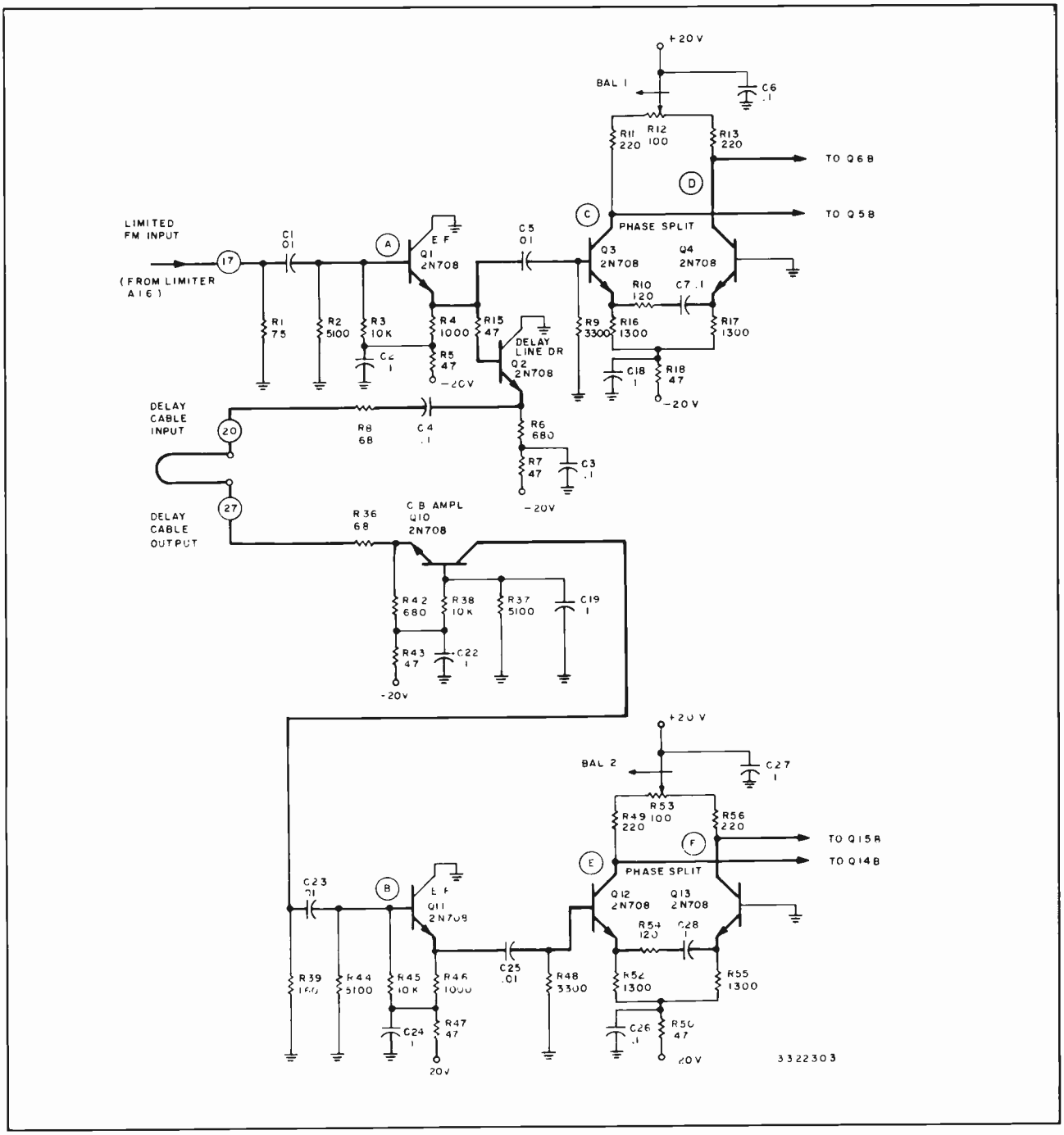
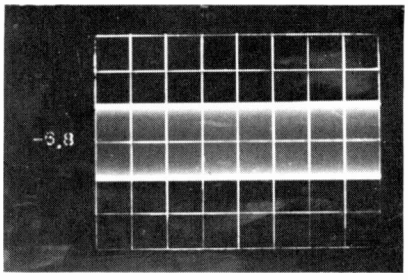
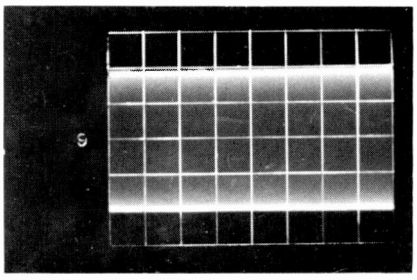


Figure 78—FM Input, Delay and Phase Splitter Circuits



1 ms/cm, 1v/cm

KEY	LOCATION
A.	Q1 base
B.	Q11 base



1 ms/cm, 1v/cm

KEY	LOCATION
C.	Q3 collector
D.	Q4 collector
E.	Q12 collector
F.	Q13 collector

Figure 79—Typical Waveforms, FM Input, Delay and Phase Splitter Circuits

The purpose of these potentiometers is to change the relative load impedance on the collectors of the phase splitters to compensate for differences in the characteristics of the discriminator diodes. Access holes, appropriately labeled, are provided on the front panel of the module to enable either of these potentiometers to be adjusted by inserting a slender screwdriver to turn the trimmer control. However, the trimmers on the balance potentiometers are not operational controls, therefore they should not be readjusted in the course of normal operation or routine maintenance.

Diode Discriminator

The complementary outputs of the phase splitters in both branches are fed to individual emitter followers which drive the diode discriminator (see figure 80).

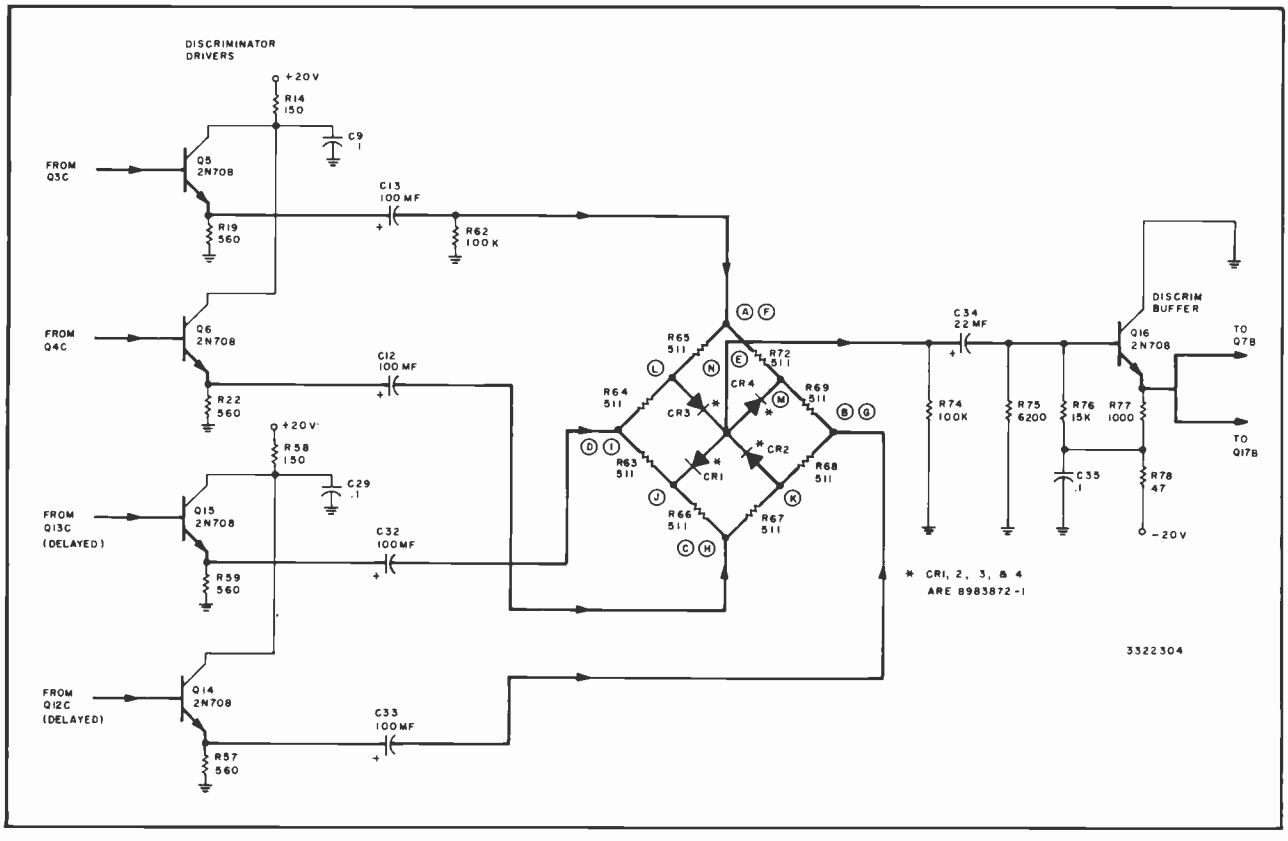
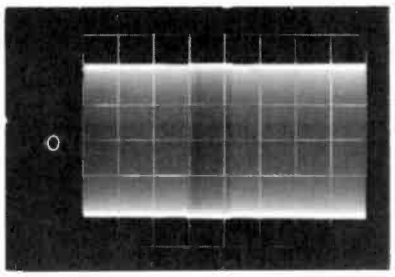
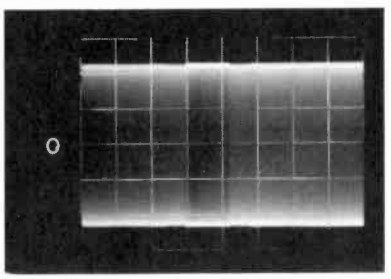


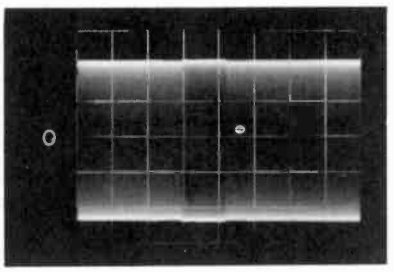
Figure 80—Discriminator Drivers, Diode Discriminator and Buffer Circuits



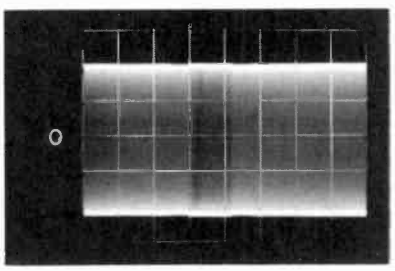
A. Junc. R65, R72, 1 ms/cm, 1v/cm



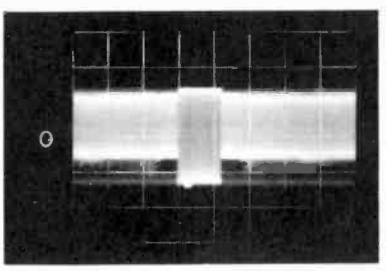
B. Junc. R69, R68, 1 ms/cm, 1v/cm



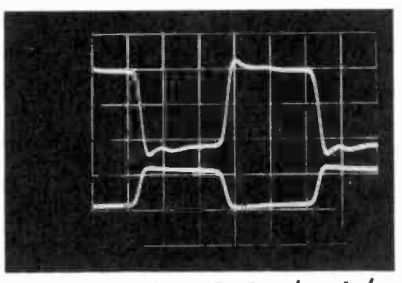
C. Junc. R66, R67, 1 ms/cm, 1v/cm



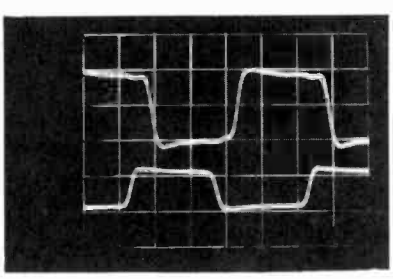
D. Junc. R64, R63, 1 ms/cm, 1v/cm



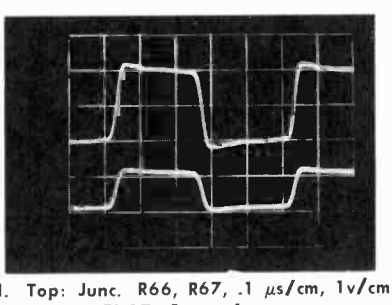
E. Junc. CR1, CR2, CR3, CR4, 1 ms/cm, .5v/cm



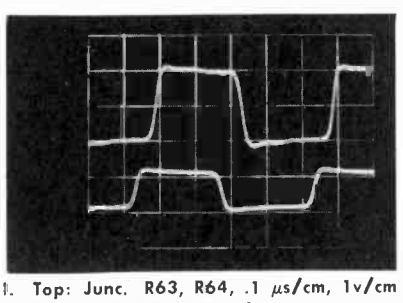
F. Top: June. R65, R72, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



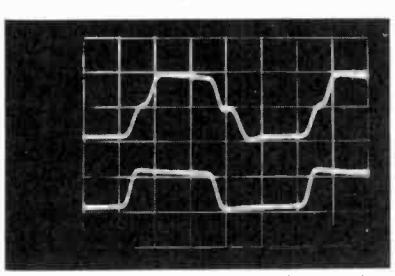
G. Top: June. R68, R69, 1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



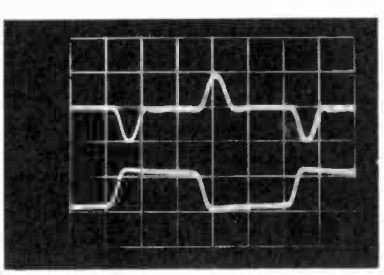
H. Top: Junc. R66, R67, .1 μs/cm, 1v/cm
Botton: PI-17, 2mc reference



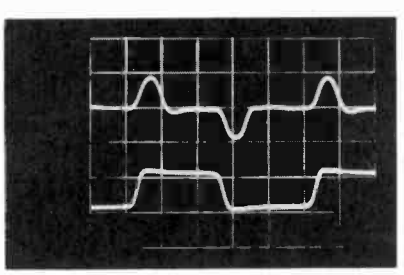
I. Top: Junc. R63, R64, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



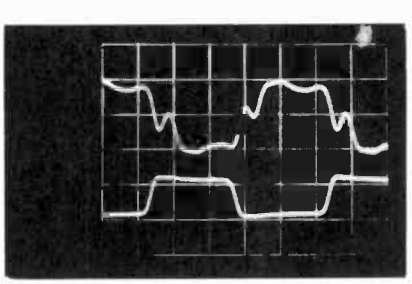
J. Top: CR1 cathode, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



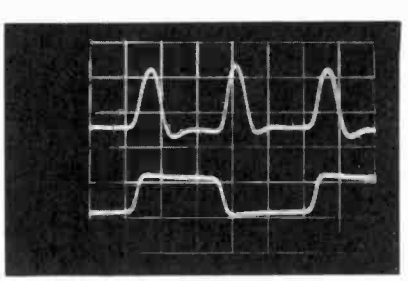
K. Top: CR2 anode, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



L. Top: CR3 anode, .1μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



M. Top: CR4 cathode, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference



N. Top: Junc. CR1, CR2, CR3, CR4, .1 μs/cm, 1v/cm
Bottom: PI-17, 2mc reference

Figure 81—Typical Waveforms, Discriminator Drivers, Diode Discriminator and Buffer Circuits

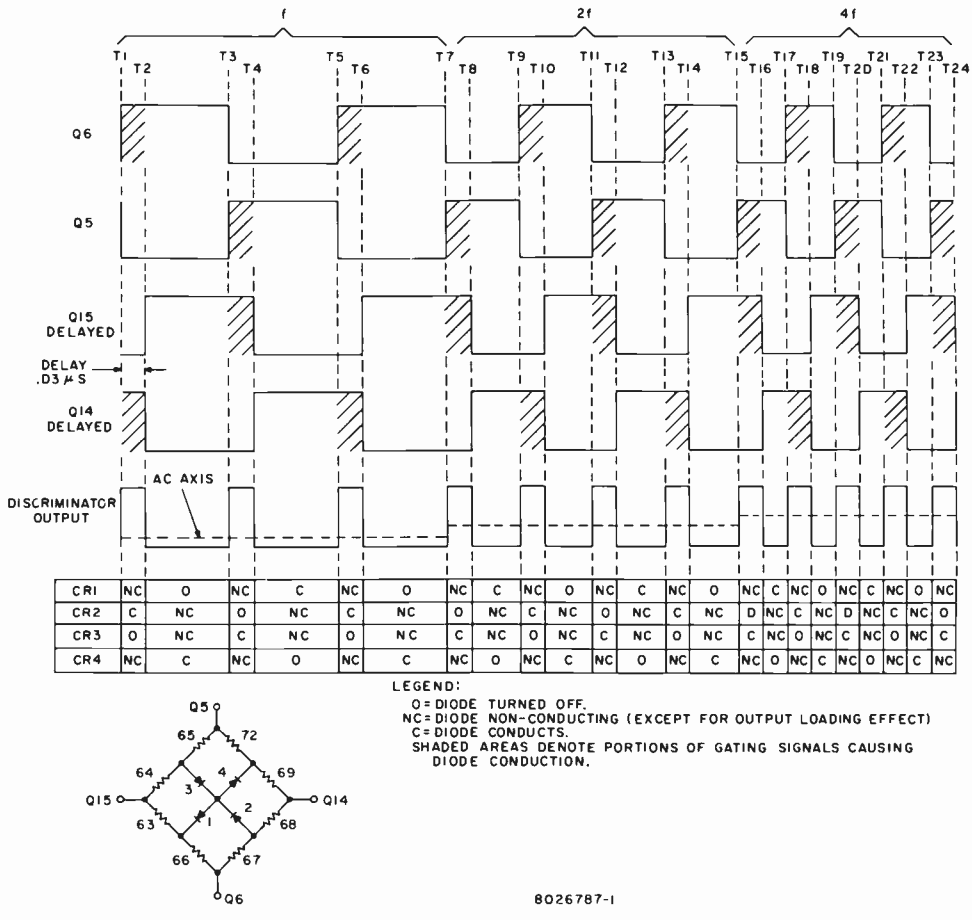


Figure 82—Diode Discriminator Conduction Cycle

The output signals on the collectors of Q3 and Q4 are fed to the bases of Q5 and Q6, respectively. The delayed output signals on the collectors of Q12 and Q13 are fed to the bases of Q14 and Q15, respectively.

The outputs from the emitter followers are connected to the discriminator network in such a manner that a delayed and an undelayed signal are combined in pairs to form a gating signal at the junction of the two resistors at the input to each diode. The output of the discriminator is a series of fixed-width positive pulses, the frequency of which is twice that of the gating signals.

A graphical analysis of the operation of the diode discriminator network is shown in figure 82. This illustration shows the phase and polarity of the gating signals applied to the diodes, over several cycles of carrier during deviation typical of a frequency modulated signal. The fixed-width positive output pulses are shown below the input pulses. The chart beneath the discriminator output waveform shows the order in which the diodes conduct.

Assuming the frequency of the discriminator input signals to be as shown in figure 82, and considering time interval t_1 to t_2 with all four signals applied across the discriminator, the diodes will conduct in the following manner.

The positive signal from Q6 and the delayed negative signal from Q15 combine at the junction of R63, R66 as the gating signal to CR1. Because these two signals are of opposite polarity, the resultant potential at CR1 is zero, tending to prevent conduction. At the same time, the positive signal from Q6 is also joined with the delayed positive signal from Q14 to form the gating input to CR2 at the junction of R67, R68. Since the polarity of the resultant gating signal is positive, CR2 conducts and a positive pulse appears at the output of the discriminator during interval t_1–t_2. The gating input to CR3 is formed at the junction of R64,

R65 by the negative signal from Q5 and the delayed negative signal from Q15. Since the resultant of these combined signals is also negative, the effect is to turn off CR3. The negative signal from Q5 and delayed positive signal from Q14 combine at the junction of R69, R72 as the gating input to CR4. However, the resultant of these two signals is zero, thus preventing CR4 from conducting.

While CR1 and CR4 do not pass their gate signals since the resultant is zero or ground potential at the junction of the input resistors and the cathodes of these diodes, they are in a quiescent state. This is due to the positive output voltage, which is present at the junction of all four diodes. Therefore this loads the output with the resistors to which the cathodes of CR1 and CR4 are connected.

From time t_2 to t_3 a similar gating action takes place, with the polarity of the undelayed signals from Q5 and Q6 remaining the same, but with the polarity of the delayed signals from Q14 and Q15 now reversed. During this interval CR1 is cut off; CR2 and CR3 tend to be cut off; but CR4 conducts, transferring its negative gate signal to the output.

The discriminator diodes continue to conduct in this fashion throughout the remaining intervals as the gating signal to each diode assumes the proper polarity.

As can be seen from the lightly shaded areas on the input pulses, positive gating signals occur twice during one alternation of each input cycle, thus the frequency of the discriminator output pulses is twice that of the input wave. Note, also, that as the frequency of the output pulses increases, the interval between becomes shorter. However, because the pulse width remains constant, due to the previously established .03 microsecond delay between the input signals, the average output level becomes more positive (greater number of positive pulses per unit of time) as frequency increases.

The pulse output of the discriminator is coupled through C34 to the base of Q16, an emitter follower which serves as a buffer between the discriminator and the following filter circuits. From the emitter of Q16, the signal is fed to the base of either of two filter drivers, Q7 or Q17.

Filtering and Video Recovery

The discriminator output signal contains both unwanted high frequency components of the carrier and the desired video information, as related to the average duty cycle. In order to recover the frequency component representing the original video, this signal must be filtered (see figure 83). Furthermore, two separate filter circuits are necessary to accommodate the bandwidth requirements of the different line rates on domestic and international standards. Only one filter circuit is active, and this is determined by the line rate on which the TR-4 is being operated. If the TR-4 is intended solely for domestic 525-line operation, the Demodulator module is equipped with a 4.2 mc filter plugged into J1 in the channel no. 1 filter circuit. When the TR-4 is for use on international standards, the Demodulator is supplied with a filter in each channel. The filter in J2 in the channel no. 2 filter circuit is 5.0 mc and is employed for 625-line operation. The bandwidth of the 4.2 mc filter is also suitable for 405-line standards; therefore it is retained as the channel no. 1 filter for 405/525-line operation. Selection of the appropriate filter for either 405/525 or 625-line rates is done by means of the VI SP and the VN SP busses. (Just how this is accomplished will be described later.)

The output from the emitter of either filter driver (Q7 or Q17) is applied to the appropriate filter, which is terminated at both ends in 91 ohms. The filter is designed to eliminate all frequencies above the video band, and deliver at the output a varying average dc whose amplitude changes are a function of the video frequency modulated input. The result of this is an output signal that is a replica of the video signal initially applied to the recorder. As mentioned earlier, the discriminator output frequency is twice that of the input. The purpose of frequency doubling is to facilitate the separation of the video and the carrier components in the filter, since with some standards the spectra of the two signals overlap. In other words, the carrier frequency, which represents the sync and blanking region, may extend down into the filter bandpass, overlapping the video component. By using the technique of frequency doubling prior to filtering, such a condition is prevented. Asymmetry, whether present in the FM signal from the Limiter (module A16) or caused by unbalance in the discriminator diodes, will introduce an unwanted component of the carrier fundamental frequency into the filter. In addition to the desired double carrier frequency, this unwanted component may be within the bandpass range of the filter and, therefore, fail to be eliminated from the video output of the filter.

The filtered signal is fed to the emitter of one of two common base video amplifiers (Q18 or Q19) where the signal is amplified to a level suitable for driving the succeeding video output stage. Shunt high frequency compensation is provided by coil L1 and variable capacitor C39 in the collector circuit of the

output common base amplifier. Use of a variable capacitor in the high frequency compensation network enables the pass band at the high end to be adjusted for a flat response.

International Standards Filter Selection

As mentioned previously, switching between the two filter circuits for operation on international standards is controlled by the VI SP and the VN SP busses. The desired line rate is selected by means of the TV STANDARDS switch, which is located on the front panel of the international Vertical Advance (module B22).

When the 625-line rate is chosen, the 5.0 mc filter (channel 2) circuit is placed in operation. The −20 volts on the VI SP bus biases Q7, the channel no. 2 filter driver, so that it will conduct, while simultaneously cutting off Q18, the channel no. 1 video amplifier. The VN SP bus, which is at ground potential, cuts off Q17, the channel no. 1 filter driver, but allows Q19, the channel no. 2 video amplifier, to conduct. Therefore the output of the diode discriminator will pass through the channel no. 2 filter circuit.

When either the 405- or 525-line rate is selected, the VI SP and VN SP potentials are reversed and the channel no. 1 filter network is in operation. In this

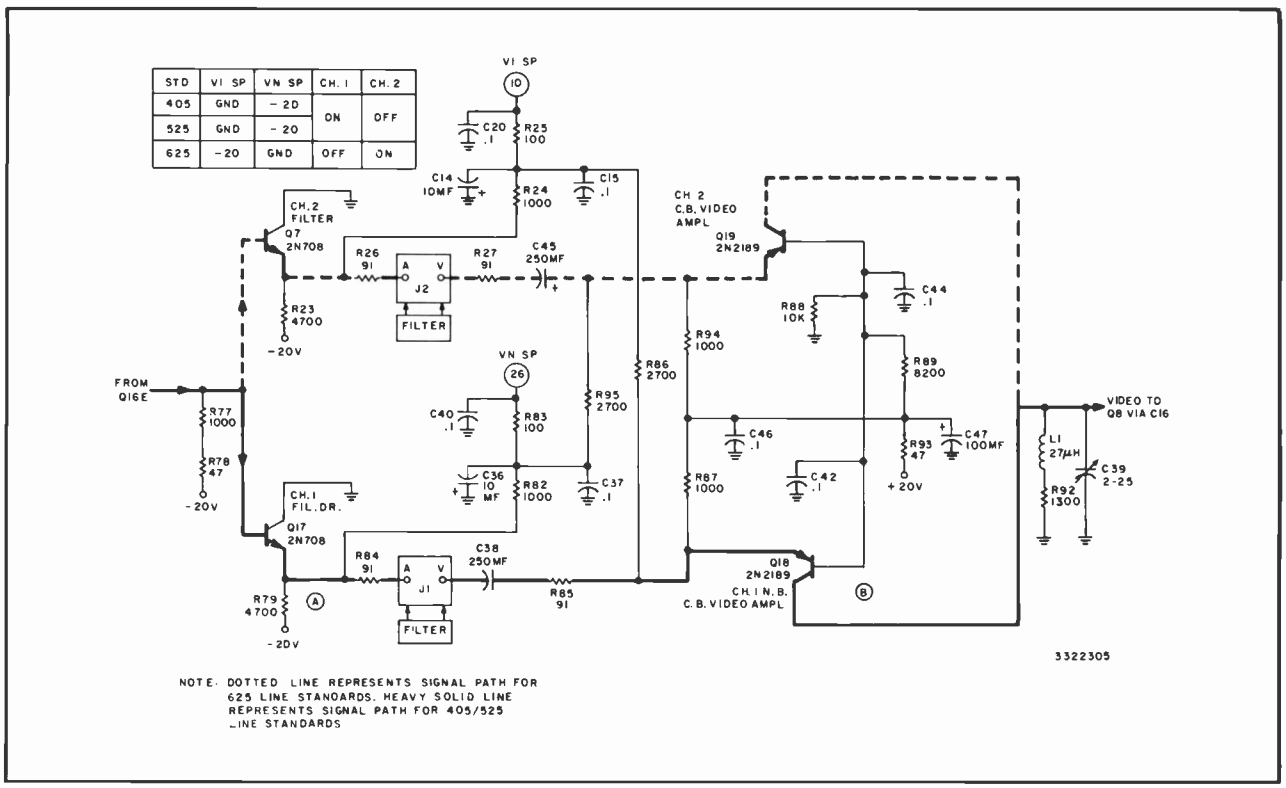
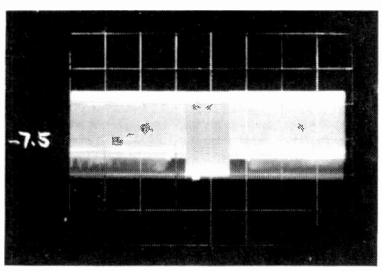
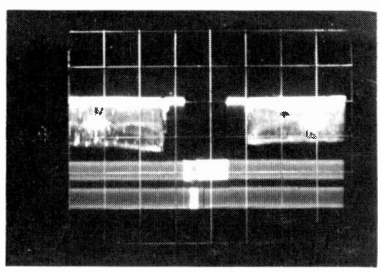


Figure 83—Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits



A. Q17 emitter, 1 ms/cm, .5v/cm



B. Q18 collector, 1 ms/cm, .5v/cm

Figure 84—Typical Waveforms, Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits

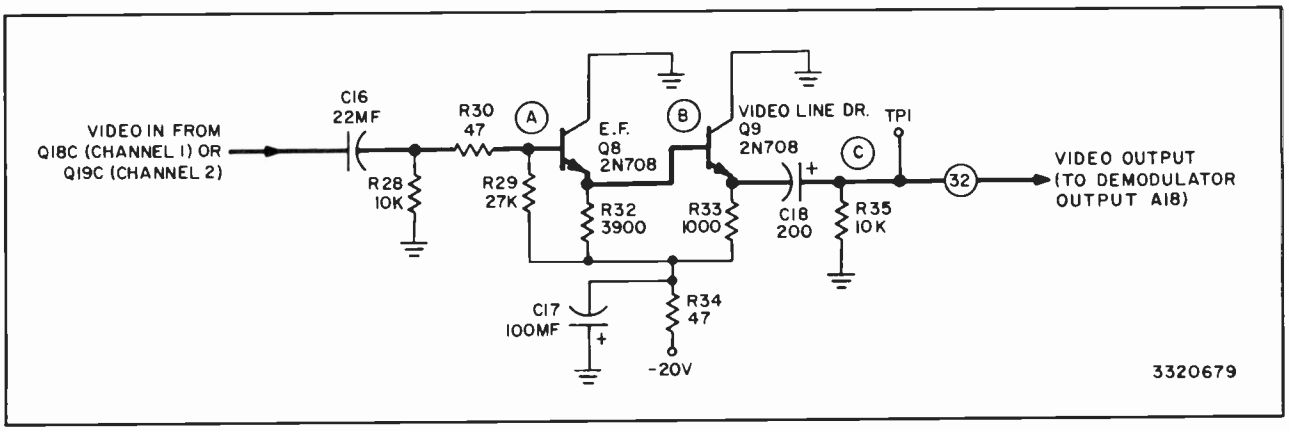
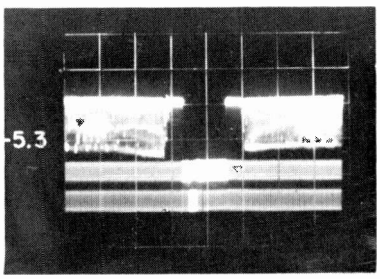
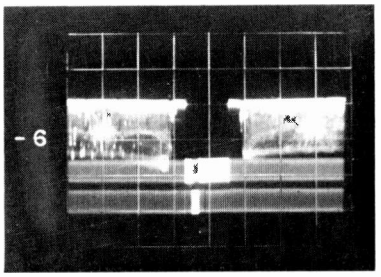


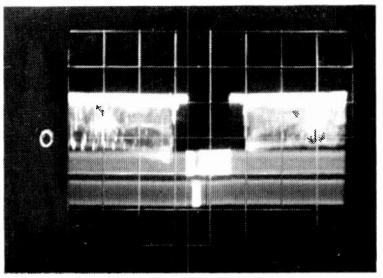
Figure 85—Emitter Follower and Video Line Driver Circuits



A. Q8 base, 1 ms/cm, .5v/cm



B. Q9 base, 1 ms/cm, .5v/cm



C. TP1, 1 ms/cm, .5v/cm

Figure 86—Typical Waveforms, Emitter Follower and Video Line Driver Circuits

case the VN bus is at −20 volts, allowing Q17 to conduct, while cutting off Q19. The VI SP bus is at ground potential and this permits Q18 to conduct, while preventing Q7 from conducting. Under these conditions, the output of the diode discriminator flows through the channel no. 1 filter circuit.

Video Output

The video output on the collector of either Q18 or Q19 is coupled through C16 to the base of Q8 (see figure 85). Transistors Q8 and Q9 form a dc coupled cascade emitter follower amplifier, which isolates the preceding stages from the video output line. From the emitter of Q9, the signal is coupled through C18 to drive the line to the Demodulator Output (module A18).

Adjustments

Balance Procedure

The demodulator discriminator circuit is balanced at the factory and the two balance potentiometers, R12 and R53 are ordinarily not disturbed during the life of the equipment. However, in the event that the balance should be upset due to the replacement of discriminator diodes or for some other reason, balance can be re-established by following the procedure outlined below.

In performing certain steps of the balance procedure, it will be necessary to attenuate the Limiter (module A16) input signal by 20 db. This may be done by interposing a video attenuator in the coaxial line connecting the FM output of the Modulator (module A2) to the Limiter (module A16). In lieu of a commercial attenuator, a network such as the one shown schematically in figure 87 can be used to provide the necessary attenuation. In assembling the latter, use 75-ohm miniature coaxial cable for the signal leads. To install the attenuator, first remove the coaxial lead from terminals 32-16 of connector A2 on the rear of the TR-4. Connect the attenuator (see figure 87) between terminals 32-16 and the free end of the coaxial lead previously removed.

1. Apply a composite video signal to the input of the TR-4; select MONO STD and place the TR-4 in the E-E mode of operation.

2. Check the sync tip frequency and deviation; adjust if necessary. (Instructions covering these adjustments are given in the TR-4 Operation Manual, IB-31810, under *Initial Setup*.)

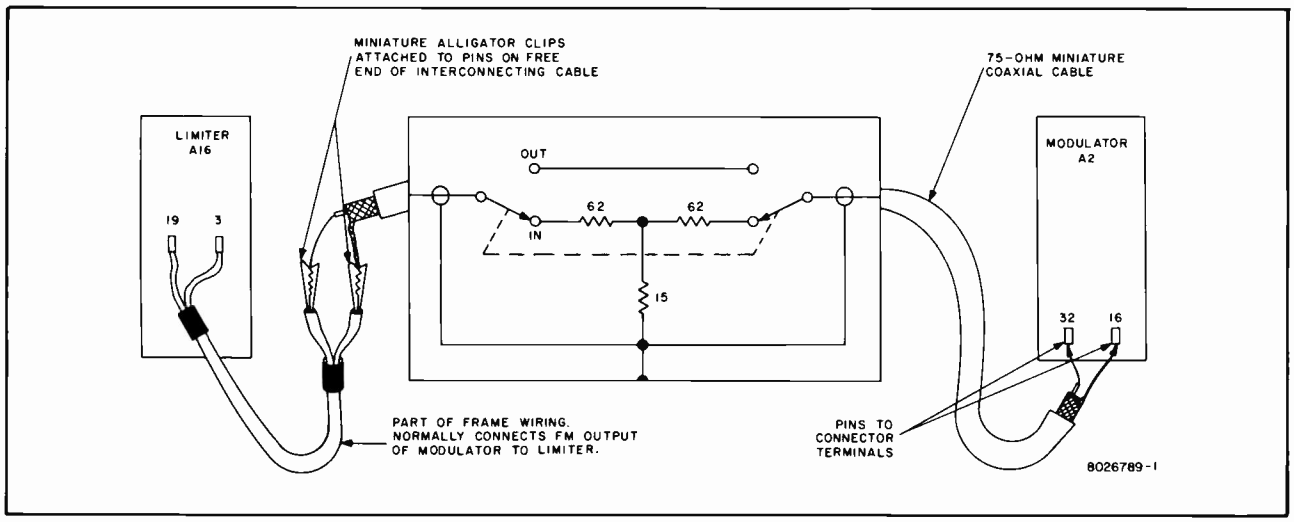


Figure 87—Schematic of Video Attenuator Showing Connection Details

3. Switch the CRO to DEMOD OUT and select the vertical interval for display.

4. Switch the attenuator into the circuit.

5. Set the Demodulator balance controls, BAL-1 and BAL-2, to approximately mid-range.

6. Observe the CRO and adjust the BALANCE control on the front panel of the Limiter (module A16) for minimum RF at blanking level.

7. Switch the attenuator out.

8. Alternately adjust the Demodulator balance controls to minimize the RF on the sync tip and blanking level.

9. Switch the attenuator in.

10. Repeat steps 6 through 9 until balance is achieved.

11. Remove the attenuator and restore the free end of the coaxial lead to its original connections.

Video Response Procedure

1. Mount the Demodulator in an extender and replace it in the TR-4.

2. Connect a multiburst signal to the video input of TR-4; select MONO STD and place the TR-4 in the E-E mode of operation.

3. Switch the CRO to DEMOD OUT and select the HOR interval for display.

4. Observe the CRO and adjust C39 for flattest response of the high end of the band.

5. Remove the extender and replace the Demodulator in the TR-4; disconnect the multiburst signal from the video input.

Demodulator Output (Module A18)

General

The Demodulator Output module distributes the post-emphasized video signal to four output lines and separated sync to two output lines.

The circuitry of the Demodulator Output module can be separated into three parts and each classified according to the function it performs:

(1) A switchable fixed and variable post-emphasis circuit, which includes the necessary equalization.

(2) A video distribution amplifier which is comprised of two branches. One branch supplies a fixed level video signal to two terminated output lines and to one unterminated line. The other branch supplies a variable level video signal to two terminated output lines.

(3) A sync separator circuit which furnishes precisely timed separated sync to two outputs.

As shown in the block diagram, figure 88, the detected video output of the Demodulator (module A17) is applied to the post-emphasis stage. Here the appropriate post-emphasis is inserted in the signal and then it is fed to the input of the video distribution amplifier circuit and split into two branches. The signal in one branch is fed through a variable gain control circuit, which in conjunction with the video level control on the Video Output (module A22), enables the level of the video signal to be varied. The signal is then fed to a series output amplifier which drives two sending-end terminated lines; one line goes to the Video/FM Control (module A21) and the other furnishes video for the optional ATC system.

The gain of the signal in the other branch remains fixed, with the signal going directly to the series output amplifier. The fixed level output of this amplifier, in addition to driving two sending-end terminated lines, one to the monitor, the other a spare, also supplies video via an unterminated line to the sync separator circuit.

The sync separator circuit is designed to extract sync from the video signal without introducing any timing errors. This is accomplished by insuring that clipping occurs at one-half the level of the sync pulse regardless of the video input level, switching spikes, dropouts, or noise. The separated sync output is fed to the Horizontal AFC (module A20) and is also available for the optional Linelock (module B19).

Circuit

Post-Emphasis

(Refer to figure 89.)

Video from the Demodulator (module A17) is fed across the DEMOD LEVEL control, R3, to the base of the equalizer driver, Q1, an emitter follower. The output from the emitter of Q1 is fed across R5, through the NORM/VAR POST-EMP switch, S2, and the MONO/COLOR standards switch, S1, to the appropriate fixed post- emphasis equalizer network, when S2 is in the OUT position shown in figure 89.

In the post-emphasis networks, a capacitor is used in shunt as the reactive element to increase attenuation at the high frequency end of the pass band. This causes a roll-off of the high frequencies, which, in effect, complements the high frequency boost obtained in the pre-emphasis circuit. Each post-emphasis network also has flat attenuation that compensates for variations in the demodulated video level which are caused by the different deviation ranges employed. Thus the post-emphasis networks restore the pass band and level so that they correspond to the original characteristics. The post-emphasis curves for monochrome and color standards are shown in figures 91 and 92, respectively.

The purpose of the variable post-emphasis equalizer network is to permit the response of a monochrome signal to be varied, in order to accommodate nonstandard tapes. The frequency response of the variable post-emphasis circuit can be changed by adjusting potentiometer R36.

Selection of the appropriate post-emphasis network is made by means of their respective controls which are on the front panel of the module. The MONO/COLOR switch, S1, is a two-section rotary switch. The A section selects either the MONO or COLOR standard fixed post-emphasis networks. The B section is wired for use with the optional color ATC system and provides a ground for the color no. 1 control. The

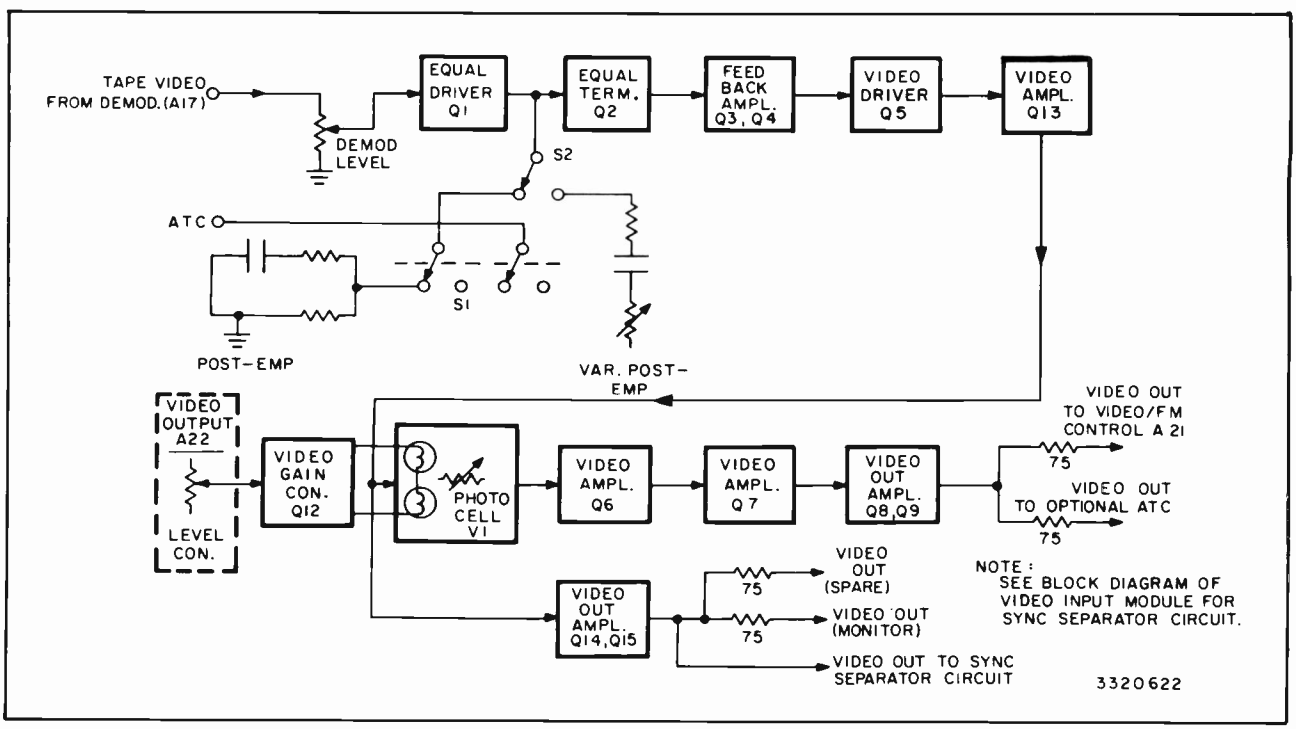


Figure 88—Partial Block Diagram, Demodulator Output Module (Post-Emphasis, Video Gain and Video Distribution Stages)

VARIABLE POST-EMPHASIS switch, S2, is the toggle type and adjacent to this is the adjustment screw for its associated circuit element R36.

The post-emphasized signal is applied to the base of the equalizer termination, Q2, an emitter follower. From the emitter of Q2 the signal is coupled through C3, C4 and R7 to the base of Q3, which together with Q4 forms the feedback amplifier. The output on the collector of Q4 is direct coupled to the base of the video driver amplifier, Q5, an emitter follower. From the emitter of Q5 the signal is coupled through C6 and R16 to the base of video amplifier Q13.

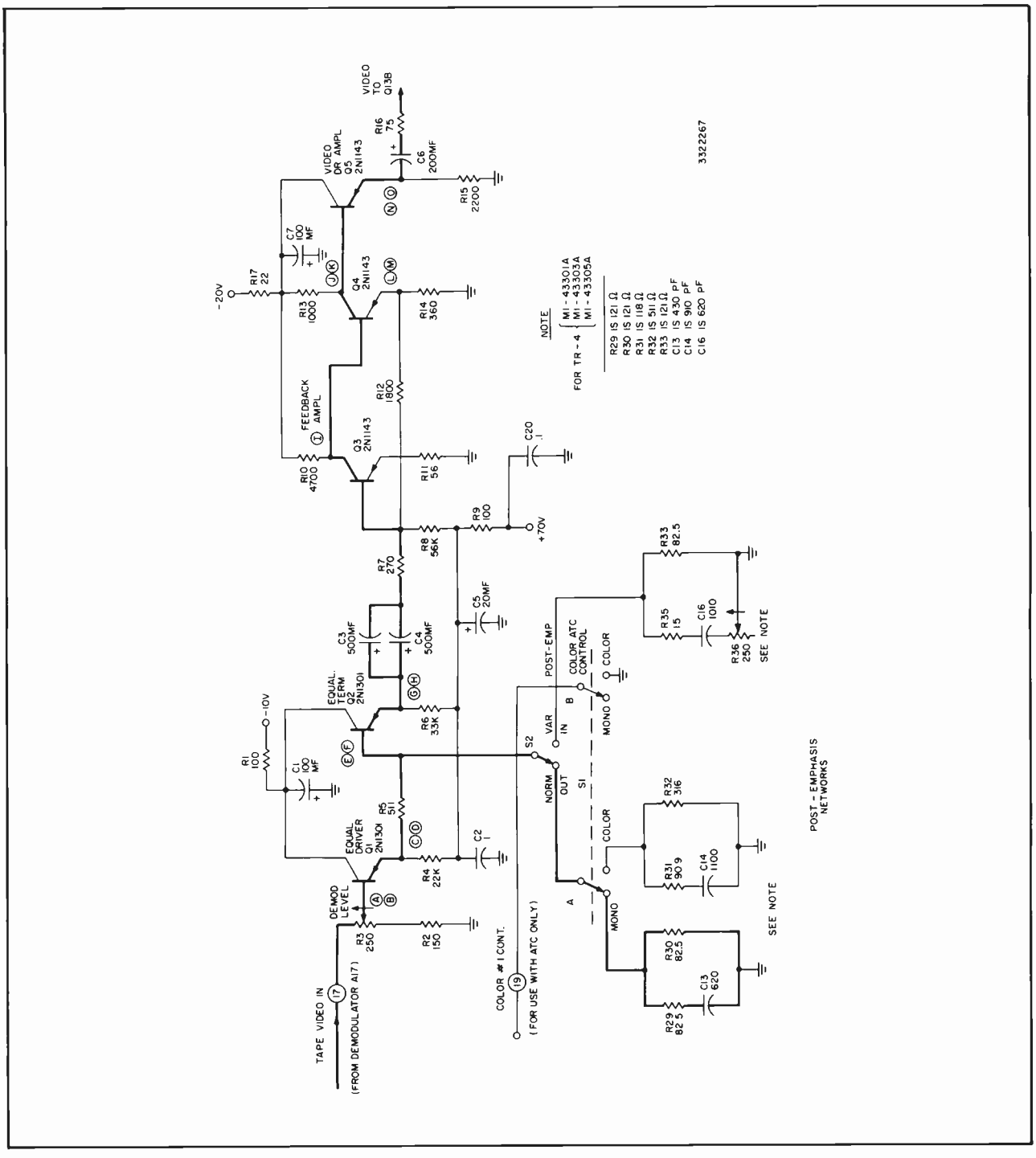
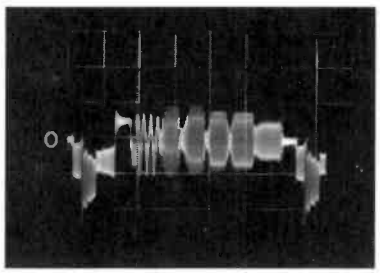
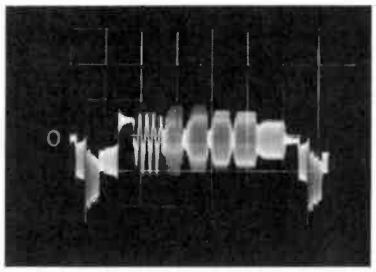


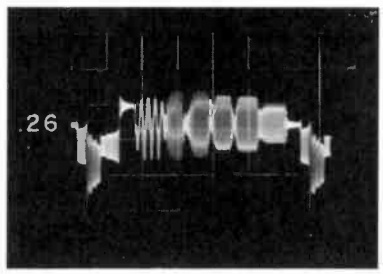
Figure 89—Equalization, Feedback Amplifier and Video Driver Amplifier Circuits (Post-Emphasis Section)



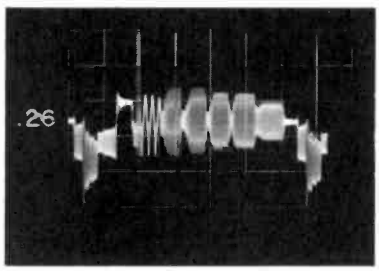
A. Q1 base, 10 μs/cm, .5v/cm, mono



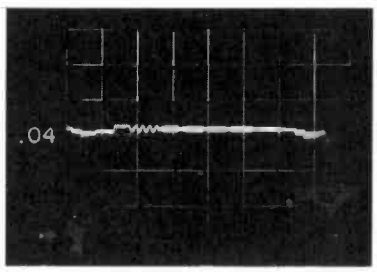
B. Q1 base, 10 μs/cm, .5v/cm, color



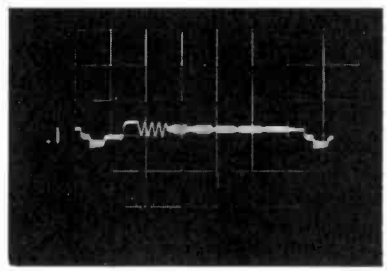
C. Q1 emitter, 10 μs/cm, .5v/cm, mono



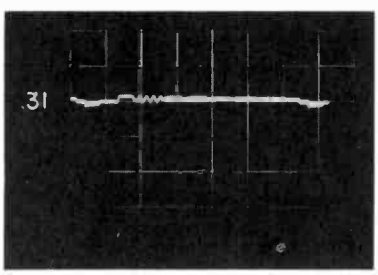
D. Q1 emitter, 10 μs/cm, .5v/cm, color



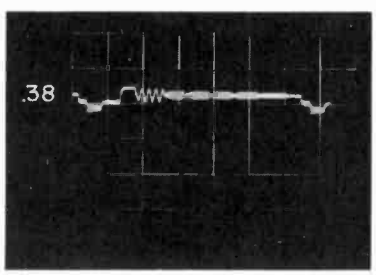
E. Q2 base, 10 μs/cm, .5v/cm, mono



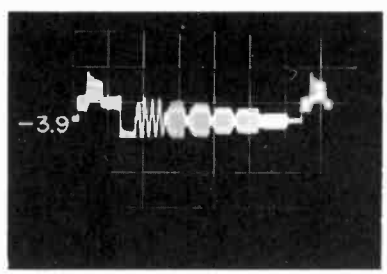
F. Q2 base, 10 μs/cm, .5v/cm, color



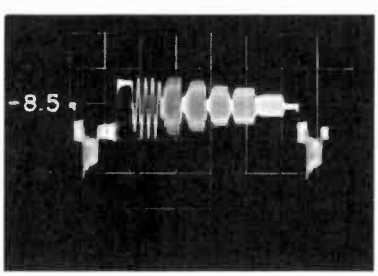
G. Q2 emitter, 10 μs/cm, .5v/cm, mono



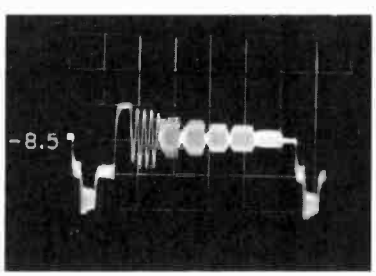
H. Q2 emitter, 10 μs/cm, .5v/cm, color



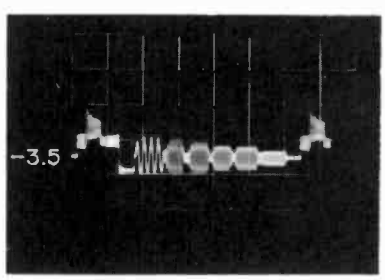
I. Q3 collector, 10 μs/mc, .5v/cm, mono



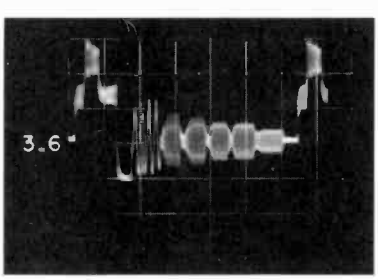
J. Q4 collector, 10 μs/cm, 1v/cm, mono



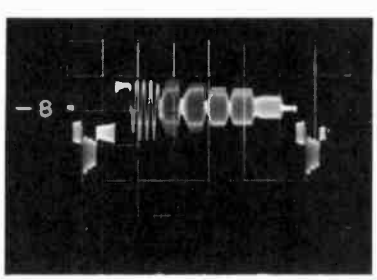
K. Q4 collector, 10 μs/cm, 2v/cm, color



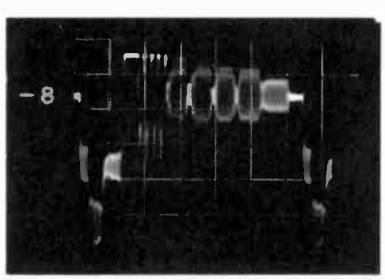
L. Q4 emitter, 10 μs/cm, .5v/cm, mono



M. Q4 emitter, 10 μs/cm, .5v/cm, color



N. Q5 emitter, 10 μs/cm, 1v/cm, mono



O. Q5 emitter, 10 μs/cm, 1v/cm, color

NOTE: The frequency increments of the multiburst signal spectrum are 0.5 mc, 1.5 mc, 2.5 mc, 3.6 mc, 4.0 mc, and 5.0 mc.

Figure 90—Typical Waveforms, Equalization, Feedback Amplifier and Video Driver Amplifier Circuits (Post-Emphasis Section)

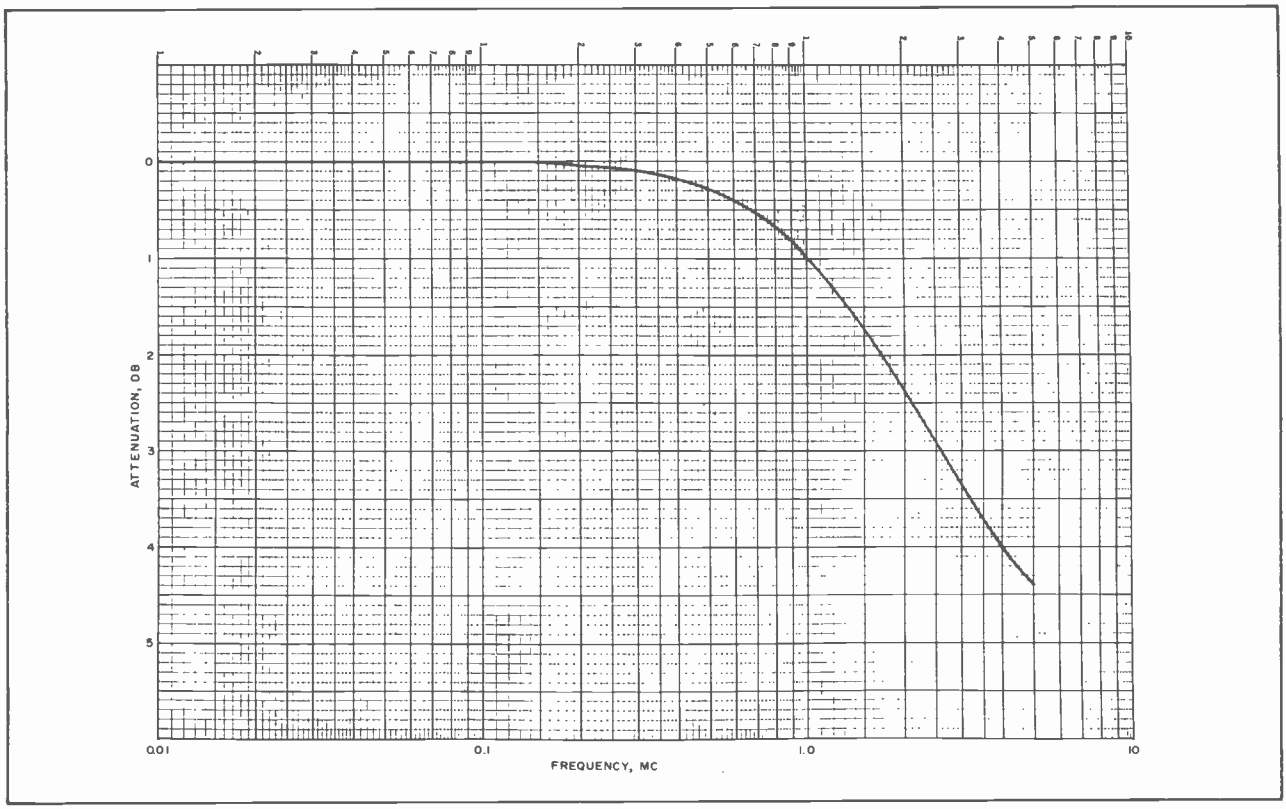


Figure 91—Post-Emphasis Curve for Monochrome Standards

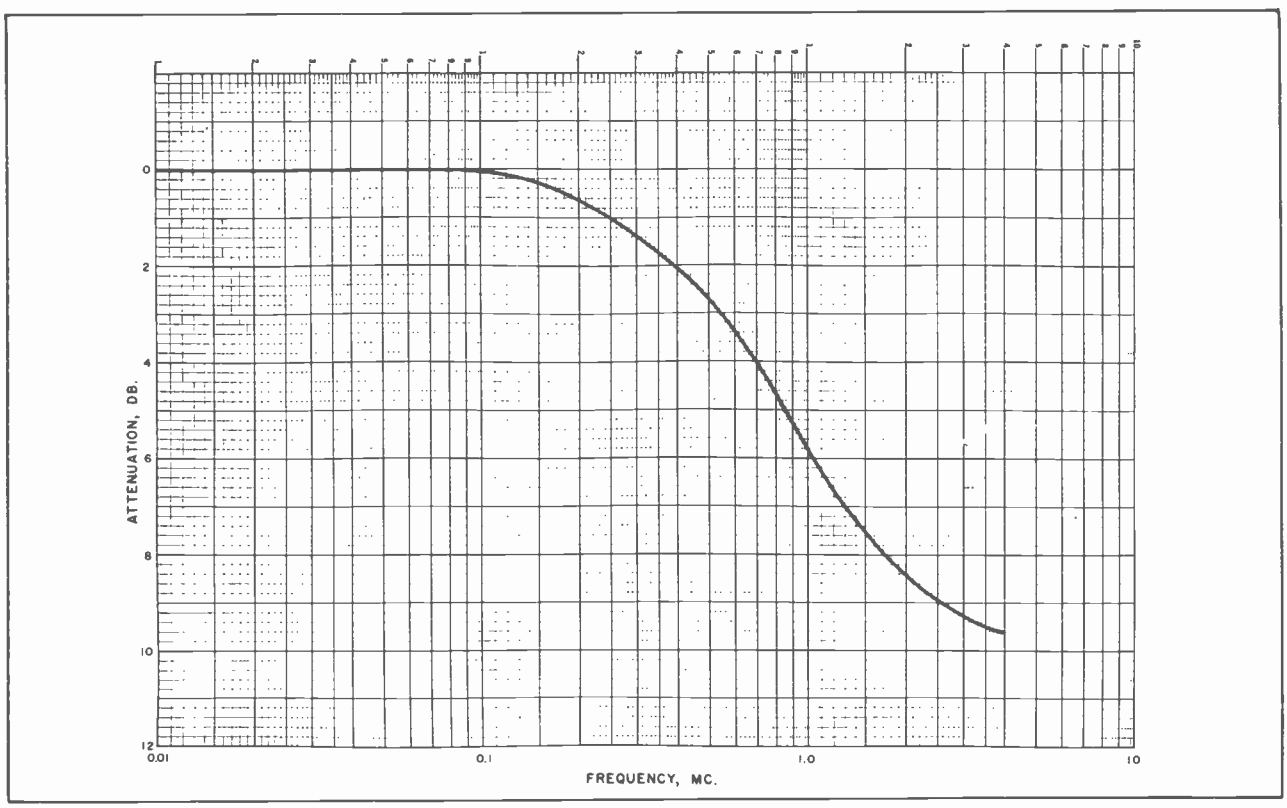


Figure 92—Post-Emphasis Curve for Color Standards

Video Distribution

Transistor Q13, an emitter follower, is the input stage to the video distribution section (see figure 93). The signal coming off the emitter of Q13 branches off into two paths, with one going to the variable gain control circuit and the other going to the fixed level circuit.

The fixed level signal is coupled through R44 to the base of Q15, which together with Q14 forms a series output amplifier. The signal on the collector of Q15 is coupled through C23 to the base of Q14. Zener diode CR2 maintains a constant difference in potential of 12 volts between the collector of Q15 and the base of Q14. Resistor R51 in the base of Q14 is used for isolation. The output on the emitter-collector junction of these two transistors is fed simultaneously to two sending-end terminated lines and to one unterminated line.

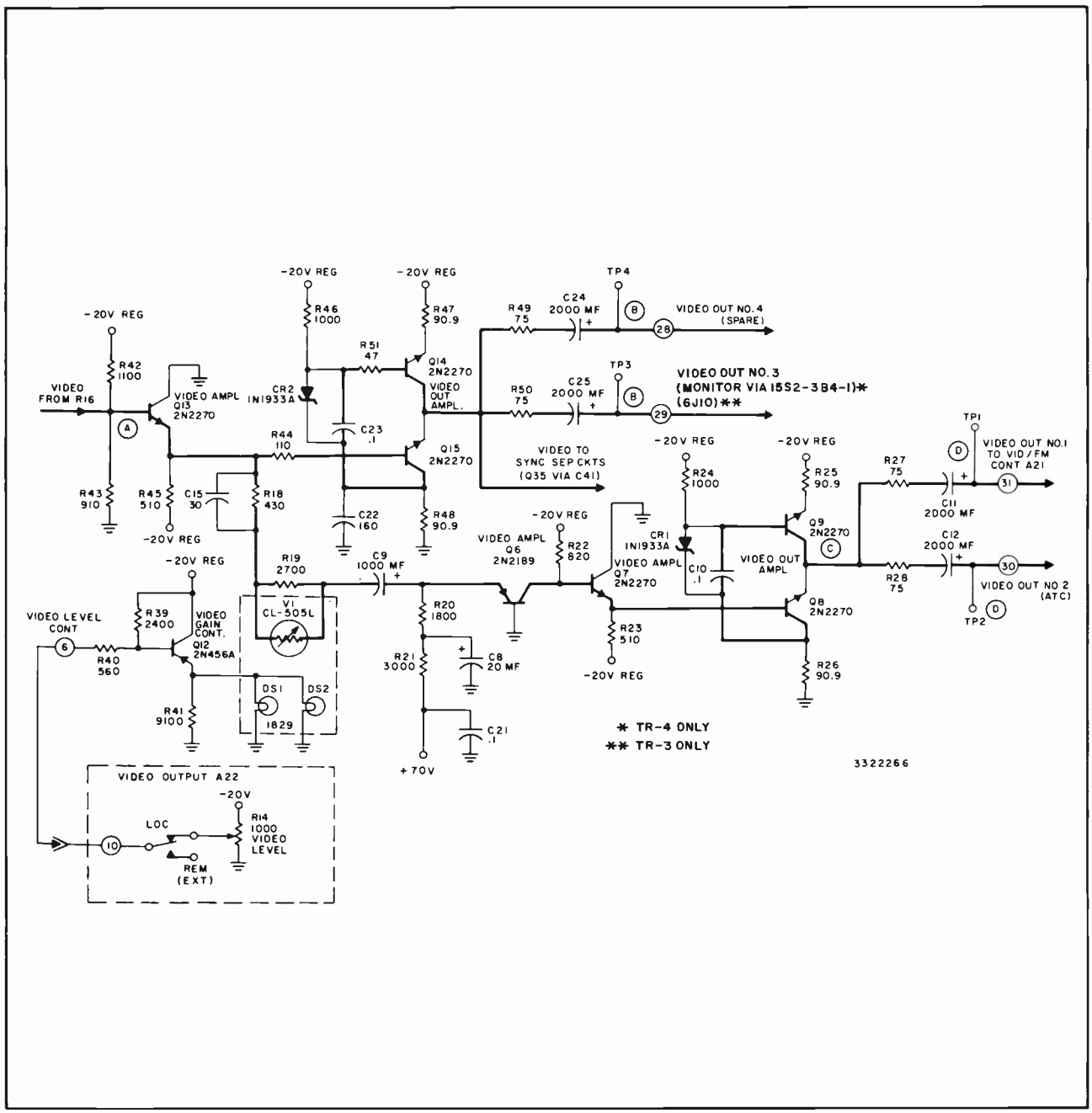
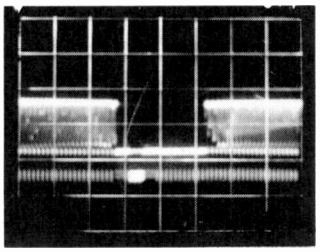
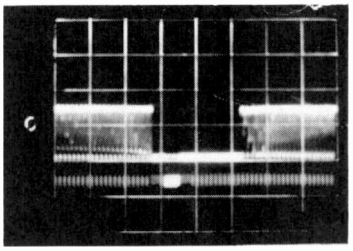


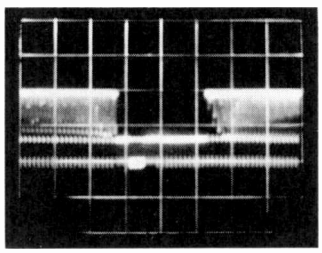
Figure 93—Video Gain Control, Video Amplifiers and Video Output Circuits (Video Distribution Section)



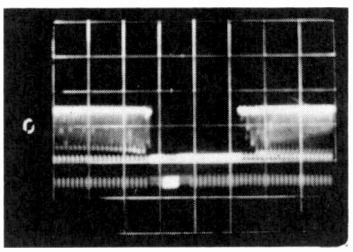
A. Q13 base,
0.5 ms/cm, 1v/cm



B. TP3, TP4,
0.5 ms/cm, 0.5v/cm



C. Q8 collector/Q9 emitter,
0.5 ms/cm, 1v/cm



D. TP1, TP2, 0.5 ms/cm

Figure 94—Typical Waveforms, Video Gain Control, Video Amplifiers and Video Output Circuits (Video Distribution Section)

One terminated line is a spare, the output being coupled through R49 and C24. The output on the other terminated line is coupled through R50 and C25 to feed the monitor. The unterminated output line goes to the sync separator circuit via C41.

The output from the emitter of Q13 going to the variable gain circuit is fed across a voltage divider formed by R18 in series with the parallel resistance of R19 and photocell V1 and coupled through C9 to the emitter of Q6, a common base amplifier. The divider is part of the variable gain control circuit which consists of the gain control transistor, Q12, an emitter follower; two lamps, DS1, DS2; and the VIDEO LEVEL potentiometer, R14. The latter is a front panel control on the Video Output (module A22).

Photocell V1 acts as variable resistance in the path of the signal. The resistance of V1 is controlled by the amount of light received from the two lamps, DS1, DS2, which is transmitted through a plexiglass prism. Transistor Q12 is the current source for the two lamps; and the current output of Q12 is determined by the dc bias applied to the base. The bias, in turn, is determined by the setting of the VIDEO LEVEL control, R14, which is on the Video Output (module A22). Varying R14 changes the light intensity and consequently the resistance offered by V1 to the signal, thus enabling control of the video level.

The common base configuration of video amplifier Q6 furnishes the low impedance required by V1 and also provides voltage amplification. The output on the collector of Q6 is direct coupled to the base of video amplifier Q7, an emitter follower. This stage prevents Q6 from the loading effects of the series output amplifier, Q8, Q9.

From the emitter of Q7, the signal is direct coupled to the base of Q8, the input section of the series output amplifier. The output on the emitter-collector junction of Q8, Q9 is fed to two output lines, Video Out no. 1 and Video Out no. 2, each terminated in 75 ohms by R27 and R28, respectively. Video Out no. 1 is coupled through C11 to feed the Video/FM Control (module A21) and Video Out no. 2 is available for use with the optional ATC system.

Sync Separator

The sync separator circuit in this module is identical to the one in the Video Input (module A1), except for the destination of the two output signals. These are shown in figure 95, which is a simplified schematic of the output stage of the sync separator used in the Demodulator Output module. One output is coupled through C29 and is available as a source of sync for the optional Linelock (module B19). The other output signal is fed across a sending-end termination, R65, and coupled through C30 to drive the line to the Horizontal AFC (module A20).

See *Sync Separator Circuit* in the description of the *Video Input (module A1)* for a discussion on the operation of this circuit.

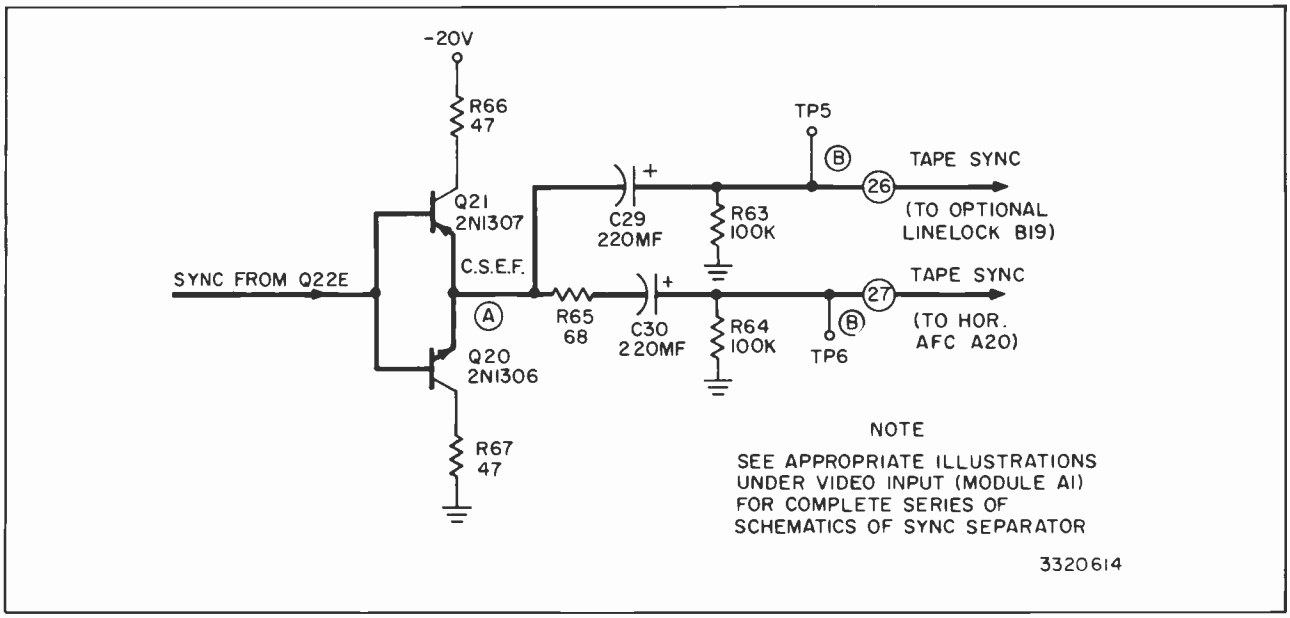
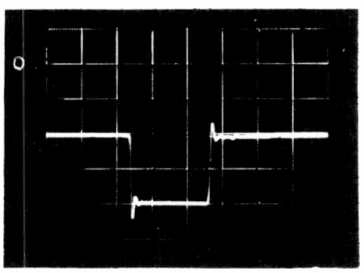
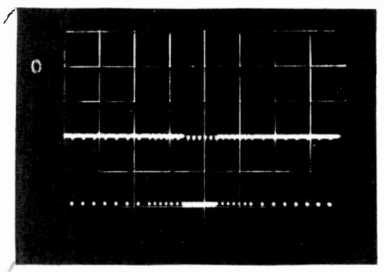


Figure 95—Complementary Symmetry Emitter Follower Sync Output Amplifier



A. Q20, Q21 emitters, 2 μs/cm, 2v/cm



B. TP6, 200 μs/cm, 2v/cm

Figure 96—Typical Waveforms, Complementary Symmetry Emitter Follower Sync Output Amplifier

Horizontal AFC (Module A20)

General

Of the three pulse-forming modules, the Horizontal AFC is the most straight-forward (see figure 97). It produces a 31.5 kc pulse, a 15.75 kc horizontal square wave and a horizontal sync pulse. The 31.5 kc pulse is provided for the Vertical Advance module and the 15.75 kc horizontal square wave and the horizontal sync for the Sync Logic module. In contrast to the Horizontal AFC module, the Vertical Advance module and the Sync Logic module are closely tied together in that they trigger each other to achieve a continuous flow of correctly timed pulses.

Horizontal Pulse Advance Technique

The sync signal can easily be recovered from the incoming composite video signal; however, the blanking signal, which cannot be removed reliably, must be regenerated from sync. The desired blanking pulse must precede by 1.7 microsecond (nominal front porch width) the sync signal from which it is regenerated. Since sync and blanking are both recurrent pulses, the position of the next sync pulse from the position of the preceding one may be predicted. Although a simple delay multivibrator with a nominal pulse width of 62.2 microseconds might seem useful to this purpose, its accuracy in pulse width and frequency is inherently inadequate for the application. Even if the tolerance of better than $\pm 0.1\%$ required in the multivibrator to hold the front porch width to within 3% were met, changes in horizontal frequency of only $+1\%$ would reduce the front porch from its nominal 1.7 microseconds to 0.43 microseconds, which is less than half the allowable minimum.

Horizontal pulse advance is obtained through the 2H master oscillator multivibrator, Q1, Q2, for which the frequency and phase is controlled by an automatic

phase control circuit referenced to the incoming tape sync. The block diagram, figure 98, illustrates this technique. The feedback loop which controls the phase of the multivibrator contains a 1.7 microsecond delay. The APC (automatic phase control) loop aligns the two pulses appearing at the phase comparator. However, the multivibrator pulse is delayed by 1.7 microseconds before reaching the comparator through Q14 and Q15. The delayed pulse is lined up with the pulses generated from reference sync. Thus, the undelayed multivibrator pulse precedes sync by 1.7 microseconds and is properly timed to regenerate horizontal blanking. In this system, the feedback loop tracks any changes in horizontal frequency, eliminating variations in front porch width due to frequency changes; also, a one percent change in delay causes only one percent change in front porch width.

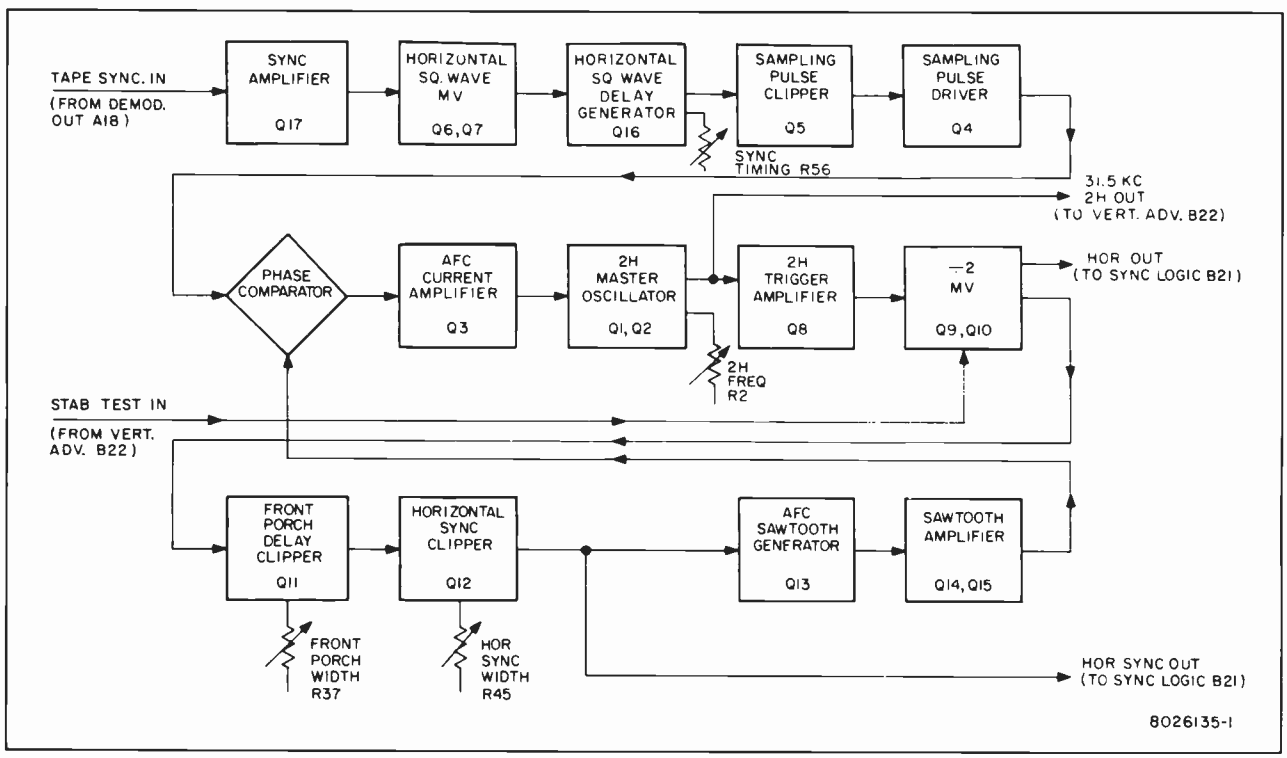


Figure 97—Block Diagram, Horizontal AFC Module

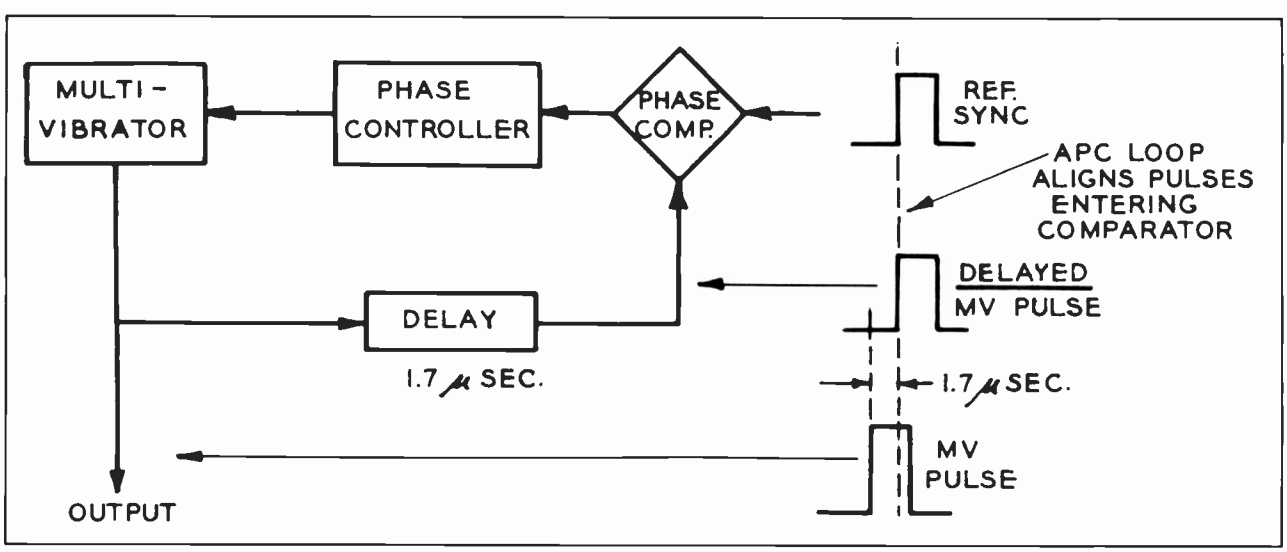


Figure 98—Block Diagram, Pulse Advance Circuit

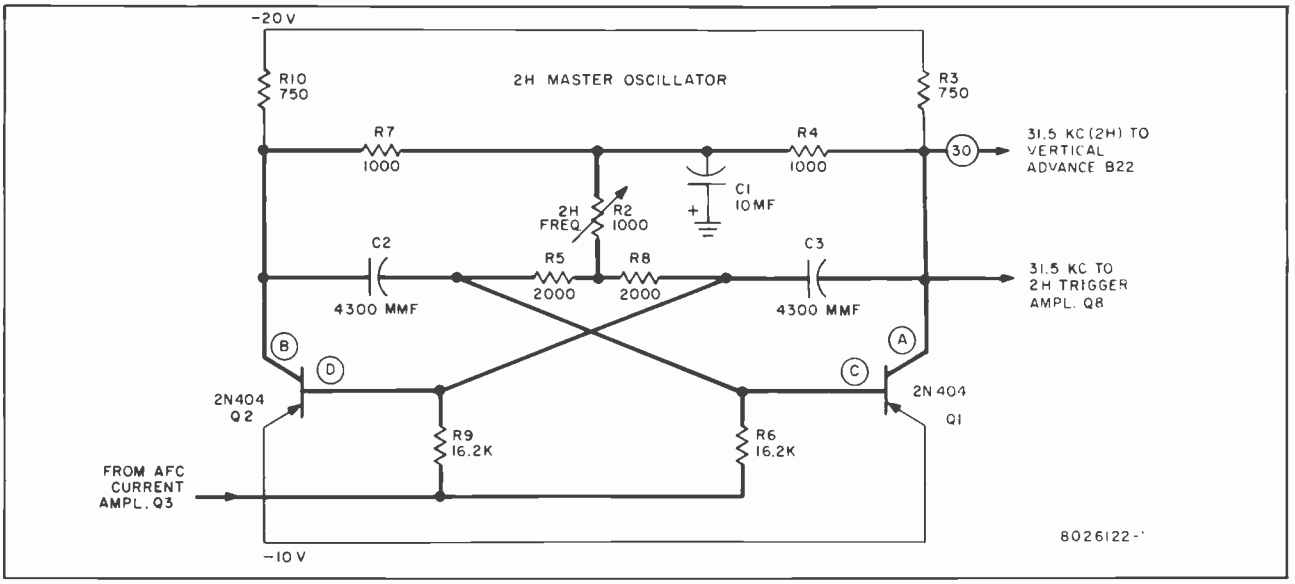
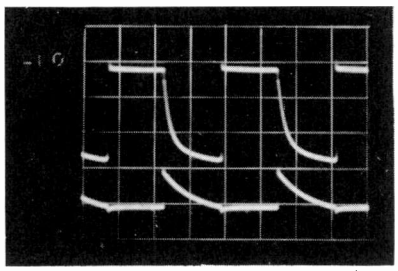
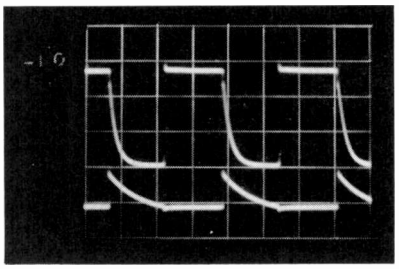


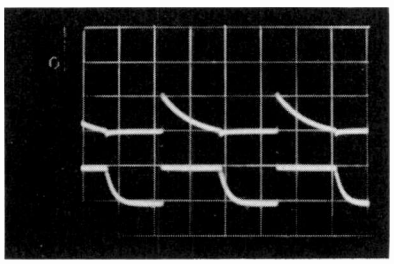
Figure 99—2H Master Oscillator Circuit



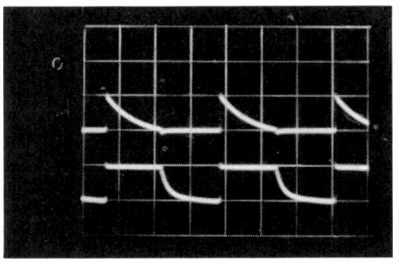
A. Top: Q1 collector, 10 μs/cm, 2v/cm
Bottom: Q1 base, 10 μs/cm, 5v/cm



B. Top: Q2 collector, 10 μs/cm, 2v/cm
Bottom: Q2 base, 10 μs/cm, 5v/cm



C. Top: Q1 base, 10 μs/cm, 5v/cm
Bottom: Q2 collector, 10 μs/cm, 5v/cm



D. Top: Q2 base, 10 μs/cm, 5v/cm
Bottom: Q1 collector, 10 μs/cm, 5v/cm

Figure 100—Typical Waveforms, 2H Master Oscillator Circuit

Circuit

The master oscillator (see figure 99) is an astable multivibrator* used to produce a square wave. The free running frequency of the master oscillator is determined by the charging time of capacitors C2 and C3 through resistors R5, R8 and R2. An afc current from the afc current amplifier, Q3, added to the charging current, corrects the frequency and phase of the master oscillator with respect to incoming sync. The frequency is set to approximately 31.5 kc by the 2H FREQ control, R2, and the AFC OFF switch, S1, which furnishes a fixed value of afc current. The fixed afc current is obtained when the AFC OFF switch (which is designated as SET-RUN on the schematic, figure 107) is closed or in the SET position. Both controls are on the front panel. The 2H FREQ is a screwdriver adjustment and the AFC OFF is a pushbutton. From the collector of Q1, the 31.5 kc

* *See Basic Circuit Descriptions on page 128.*

square wave goes to the Vertical Advance module and also to the 2H trigger amplifier, Q8, where it is coupled to the base by capacitor C14.

To provide a 15.75 kc square wave (half the 31.5 kc pulse) which is properly timed for the generation of horizontal blanking and horizontal drive in the Sync Logic module, the divide-by-two monostable multivibrator, Q9, Q10, is triggered from the 2H trigger amplifier, Q8. (Refer to figure 101.) Both transistors of the ÷ 2 multivibrator* are saturated in the stable state and driven to cutoff by a positive trigger pulse. The time constant of C16 and R36 determines the duration of the cutoff period which is slightly greater than the period of the 31.5 kc trigger pulse. Both transistors then revert to the saturated state until the next trigger pulse comes along.

A gating action is accomplished by dc connecting the emitter of Q8 through R38 to the collector of Q10. (Refer to figure 101.) When Q10 is in the saturated or stable state, the Q10 collector and Q8 emitter are at −10 v. Since the collector of Q8 is at zero potential, the transistor is capable of passing a trigger pulse applied to its base. The output from the emitter of Q8 is a positive going trigger pulse that is applied through C16 to the base of Q9. This pulse cuts off

* *See Basic Circuit Descriptions on page 128.*

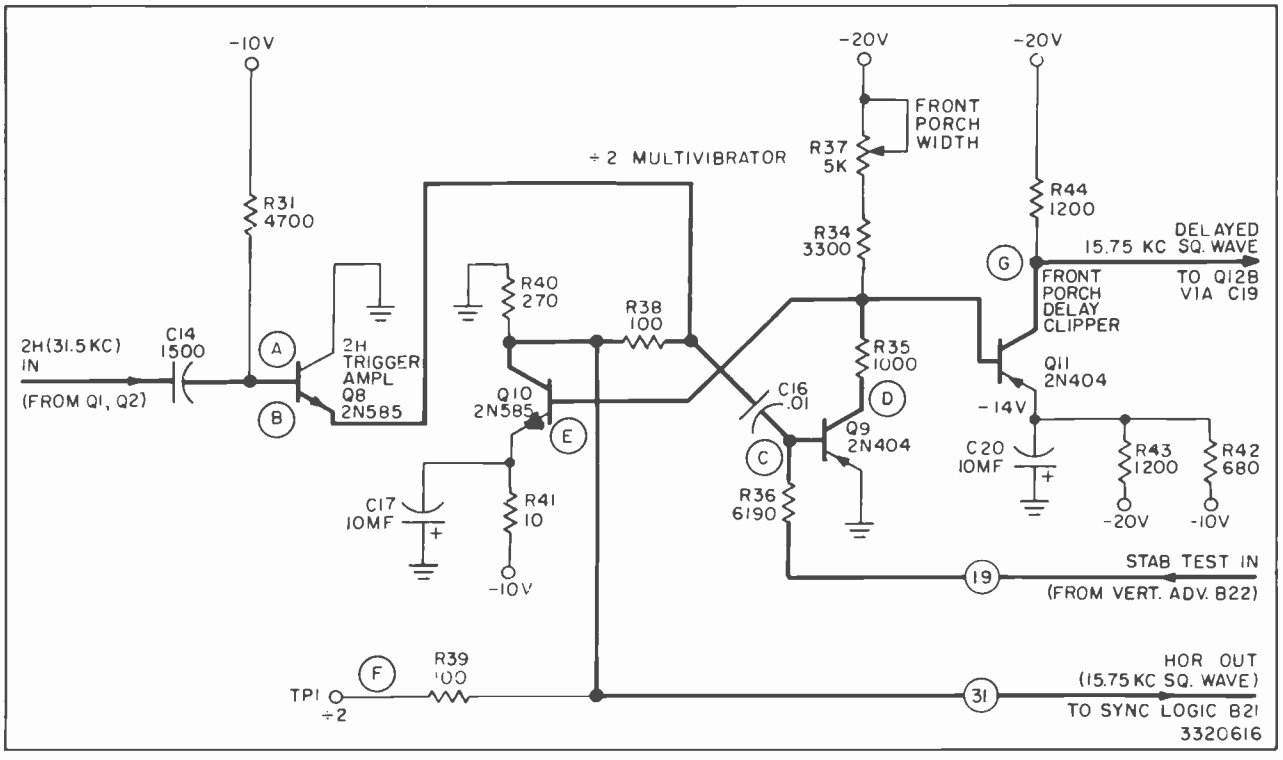
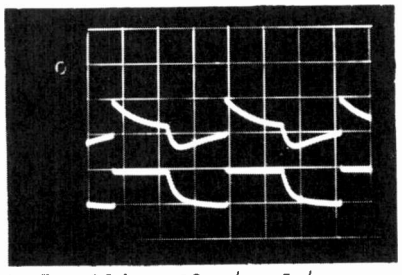
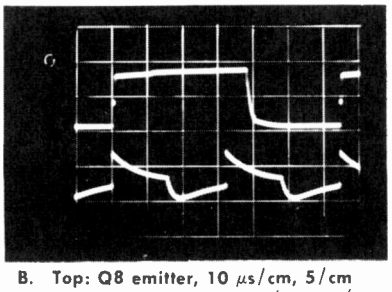


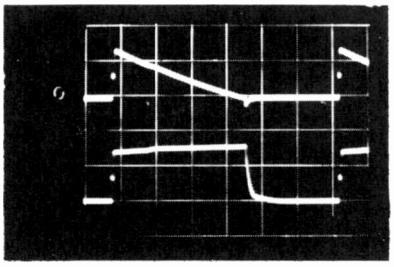
Figure 101—2H Trigger Amplifier, ÷ 2 Multivibrator and Front Porch Delay Clipper Circuits



A. Top: Q8 base, 10 μs/cm, 5v/cm
Bottom: Q1 collector, 10 μs/cm, 5v/cm

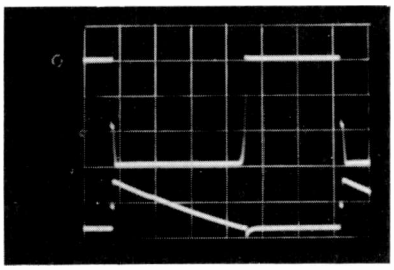


B. Top: Q8 emitter, 10 μs/cm, 5/cm
Bottom: Q8 base, 10 μs/cm, 5v/cm

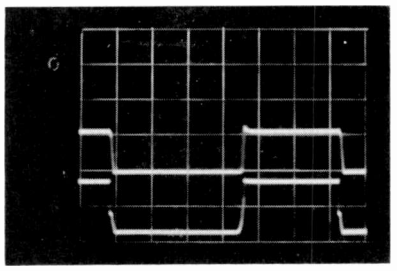


C. Top: Q9 base, 10 μs/cm, 5v/cm
Bottom: Q8 emitter, 10 μs/cm, 5v/cm

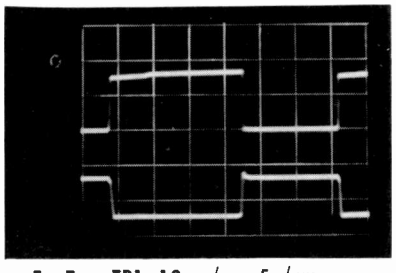
Figure 102—Typical Waveforms, 2H Trigger Amplifier, ÷ 2 Multivibrator and Front Porch Delay Clipper Circuits



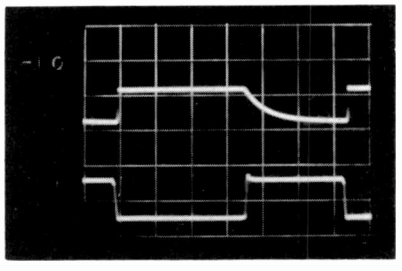
D. Top: Q9 collector, 10 μs/cm, 5v/cm
Bottom: Q9 base, 10 μs/cm, 5v/cm



E. Top: Q10 base, 10 μs/cm, 5v/cm
Bottom: Q9 collector, 10 μs/cm, 10v/cm



F. Top: TP1, 10 μs/cm, 5v/cm
Bottom: Q10 base, 10 μs/cm, 5v/cm



G. Top: Q11 collector, 10 μs/cm, 5v/cm
Bottom: Q11 base, 10 μs/cm, 5v/cm

Figure 102—(Continued)

Q9 which simultaneously cuts off Q10. When Q10 is cut off, the potential on the collector of Q10 and the emitter of Q8 is zero making it impossible for Q8 to pass trigger pulses, since the trigger pulses on the base of Q8 do not exceed zero volts in the positive direction. Amplifier Q8 is biased so that it does not pass the negative going pulses applied to the base.

A 15.75 kc square wave from the collector of Q9 is fed to the base of the front porch delay clipper, Q11. The shunt capacitor, C18, at the base of Q11 slows down the rise time of the square wave. Transistor Q11 does not conduct until the potential in the base falls to approximately the fixed emitter potential (−14 v) formed by voltage divider R42, R43. The time taken to reach this potential is the delay time. In conduction, the Q11 circuit produces, at the collector, a fast-rise-time square wave whose leading edge is delayed from that of the input square wave. The delay in the conduction of Q11 is determined by the rise time of the input square wave, which is controlled by the setting of the FRONT PORCH WIDTH potentiometer, R37.

As shown in figure 103, this delayed 15.75 kc square wave output is coupled to the base of Q12, the horizontal sync clipper, which is a pulse narrowing circuit (boxcar*). The width of the pulse is determined by the time constant of C19, R46, and R45, the last being the HOR SYNC WIDTH potentiometer. The regenerated horizontal sync appearing on the collector of Q12 is fed simultaneously to the AFC sawtooth generator, Q13, and to the Sync Logic module.

The horizontal sync pulse being fed to the base of Q13 is passed through an integrating network consisting of C22, R48. The integrator slows the rise time of the sync pulse so that there is a slight delay before Q13 can conduct. This delay contributes to the total advance in timing of the 31.5 kc square wave relative to tape sync; however, it does not affect the front porch width since that width is determined only by the delay between the 15.75 kc square wave (used to generate horizontal blanking) and the leading edge of regenerated horizontal sync. The SYNC TIMING control, R56, (figure 105) allows adjustment of the total delay of horizontal sync over a small range so that the leading edge of regenerated horizontal sync may be made coincident with the leading edge of incoming tape sync. Therefore, when regenerated horizontal sync is combined with the vertical interval of tape sync in the Sync Logic module, the equalizing pulses and the vertical sync pulses are correctly timed with respect to the horizontal sync pulses.

The afc sawtooth generator, Q13, conducts when the integrated sync pulse on its base drops to approximately the voltage (−4 v) on the emitter, which is fixed by voltage divider R49, R50 and R51. When Q13 conducts, it provides a low impedance discharge path for capacitor C25. Then, when Q13 is cut off by the decay of the input sync pulse, C25 charges slowly

* *See Basic Circuit Descriptions on page 128.*

through R52 and R53, generating a sawtooth voltage. The sawtooth voltage at the collector is direct-coupled to the bases of the sawtooth or complementary symmetry (bootstrap) amplifier, Q14 and Q15. This bootstrap circuit increases the linearity of the sawtooth waveform; the complementary symmetry arrangement provides sufficient current gain and a very low impedance to drive the phase comparator (figure 107). The output is taken from the emitters of Q14 and Q15.

During the vertical interval, equalizing pulses and vertical sync serations occur at twice the rate (31.5 kc) of the horizontal sync pulses. If this "double frequency" (half-line) information is permitted to trigger the sampling pulse clipper, Q5, (figure 107) the phase comparator would be keyed on during the wrong part of the sawtooth voltage cycle and thus provide wrong afc information to the 2H master oscillator, Q1, Q2.

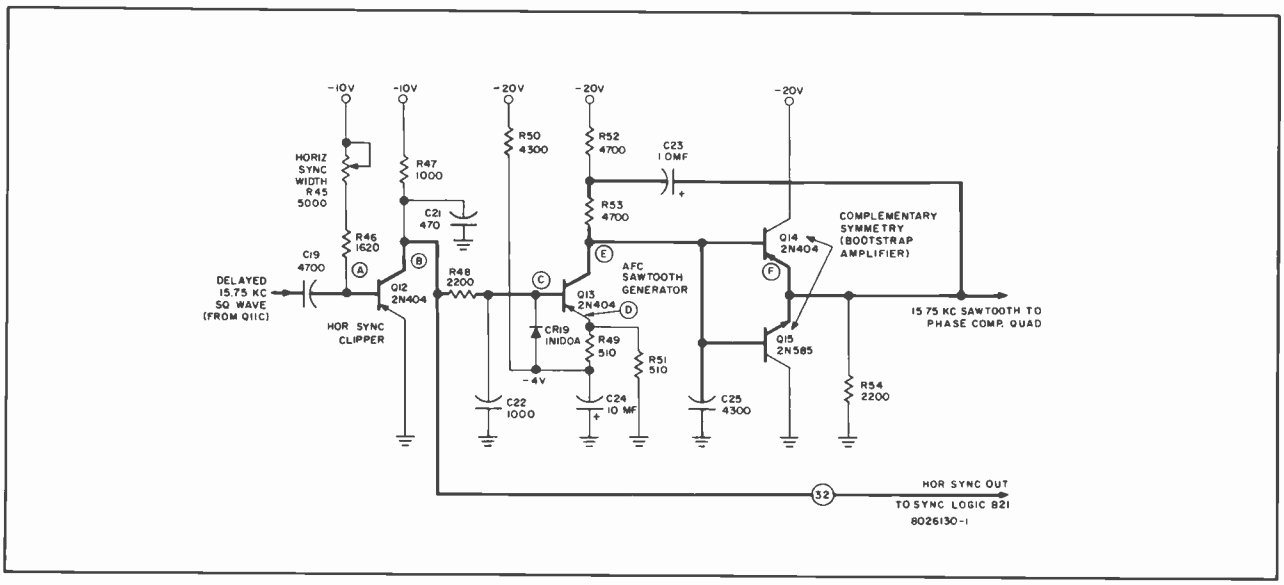
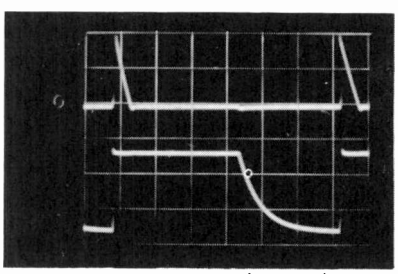
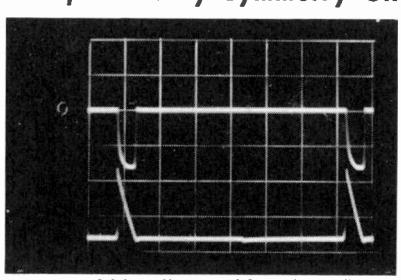


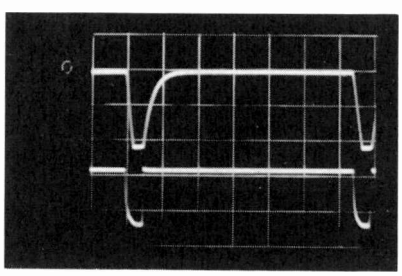
Figure 103—Horizontal Sync Clipper, AFC Sawtooth Generator and Complementary Symmetry Circuits



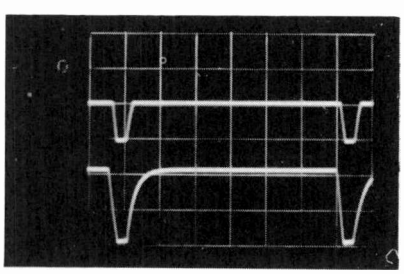
A. Top: Q12 base, 10 μs/cm, 2v/cm
Bottom: Q11 collector, 10 μs/cm, 2v/cm



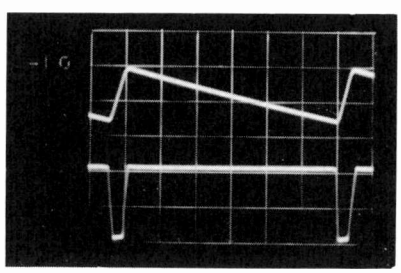
B. Top: Q12 collector, 10 μs/cm, 5v/cm
Bottom: Q12 base, 10 μs/cm, 2v/cm



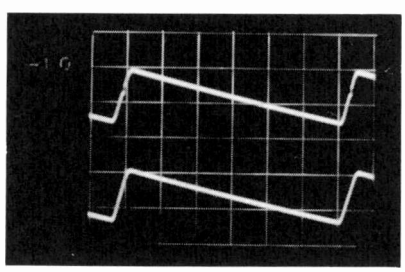
C. Top: Q13 base, 10 μs/cm, 2v/cm
Bottom: Q12 collector, 10 μs/cm, 5v/cm



D. Top: Q13 emitter, 10 μs/cm, 2v/cm
Bottom: Q13 base, 10 μs/cm, 2v/cm



E. Top: Q13 collector, 10 μs/cm, 5v/cm
Bottom: Q13 emitter, 10 μs/cm, 1v/cm



F. Top: Q14 emitter, 10 μs/cm, 5v/cm
Bottom: Q14 base, 10 μs/cm, 5v/cm

Figure 104—Typical Waveforms, Horizontal Sync Clipper, AFC Sawtooth Generator and Complementary Symmetry Circuits

The circuitry as shown in figure 105 provides only 15.75 kc pulses for the sampling pulse clipper, Q5.

Tape sync from the sync separator circuit in the Demodulator Output (module A18) is coupled by R60 and C31 to the emitter of Q17, the sync amplifier. Transistor Q17, in conjunction with R60 and C31 differentiates the negative sync input signal. The negative going leading edge of the differentiated pulse on the collector of Q17 is fed across R29 to trigger the horizontal square wave multivibrator, Q6, Q7.

The latter is a monostable multivibrator* whose time constant is such that the triggering is effective only at the horizontal frequency rate of composite sync.

With no signal, Q7 is normally in its stable or cutoff state, and Q6 is in its stable or saturation state. The collector of Q7 is nominally at −10 volts and the collector of Q6 is zero volts. The negative sync pulse from the collector of Q17 forward biases Q7. This drives Q7 into saturation thereby generating a positive pulse on the collector. This positive pulse is applied to the base of Q6 through R25 and C11. With the positive pulse on its base, Q6 is cutoff. C11 is charged to −10 volts through R27 and R25 and the base-emitter junction of Q6 during the quiescent state of Q7. C11 discharges through R24, R25 and the saturation resistance of Q7. The voltage on the base of Q6 becomes less positive and Q6 begins to conduct. As Q6 goes toward saturation, the voltage on the collector decreases negatively, and is coupled through R26 to the base of Q7, driving it into cutoff.

* *See Basic Circuit Descriptions on page 128.*

By applying a succession of negative pulses to the base of Q7, the multivibrator generates a train of positive sync pulses or horizontal square waves at the collector of Q7. The width or frequency of the horizontal square waves is determined by the time constant of R25, C11, and R24. Through the use of the horizontal square wave multivibrator, any half line (31.5 kc) information during vertical blanking is eliminated.

The positive-going square wave from the collector of Q7 is direct-coupled to the base of Q16, the horizontal square wave delay generator. Capacitor C26 in the base of Q16 delays the square wave. The amount of delay can be varied by the SYNC TIMING control, R56. This control is adjusted so that the leading edge of regenerated sync on the composite video output signal is halfway between the leading edge of sync in the video input signal and the leading edge of incoming tape sync.

> NOTE: The composite video output signal can be observed by connecting an oscilloscope to any one of the three test points on the Video Output module. In the same manner, the sync on the video input signal can be observed at test point one on the Video/FM Control module.

The emitter of Q16 is fixed at approximately −2 volts, the level at which the input signal is clipped. In the inverted output on the collector of Q16, the positive-going excursion is limited at zero volts, therefore the output appearing on the collector is a 2-volt square wave. This signal at a 15.75 kc rate is fed to the sampling pulse clipper, Q5.

As shown in figure 107, the 15.75 kc signal from the horizontal square wave delay generator is coupled through the differentiating network consisting of C10,

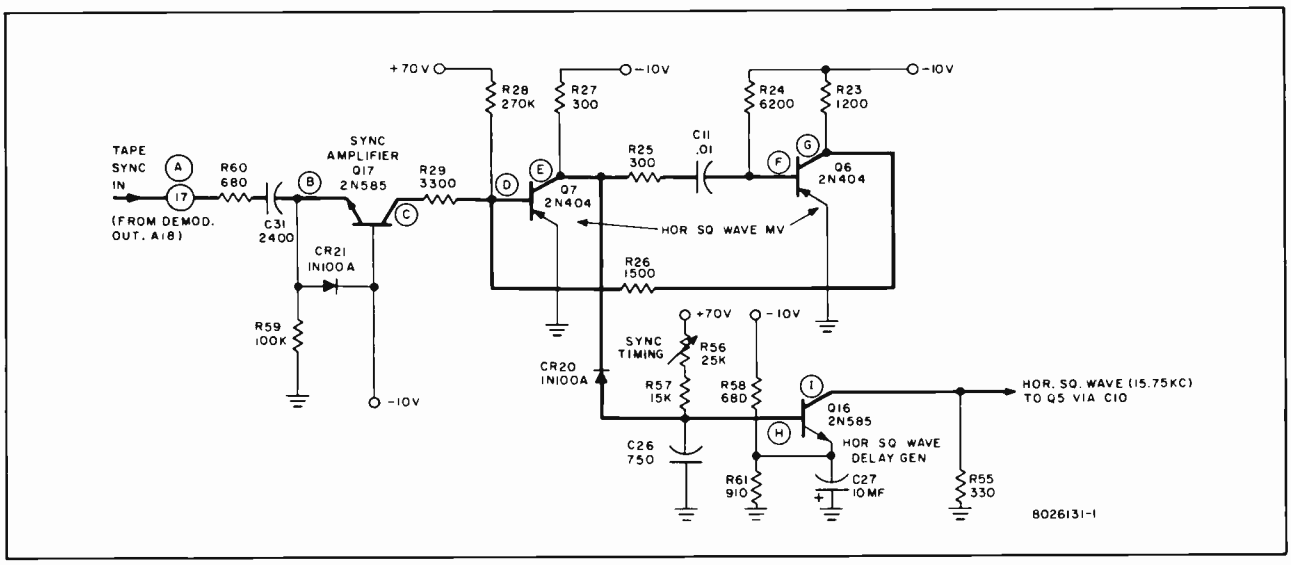
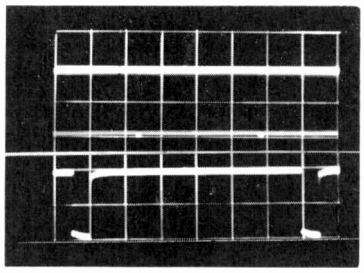
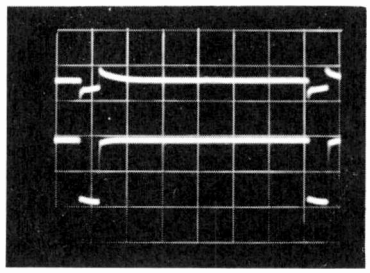


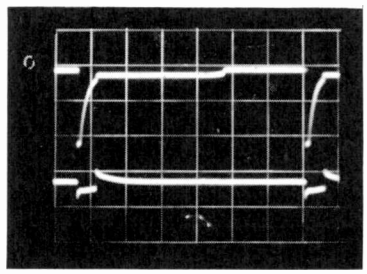
Figure 105—Sync Amplifier, Horizontal Square Wave Multivibrator and Horizontal Square Wave Delay Generator Circuits



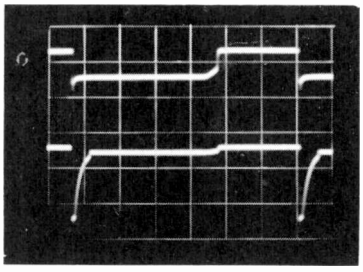
A. Top: R60 input, 5 ms/cm, 2v/cm, vert. rate
Bottom: R60 input, 10 μs/cm, 2v/cm, hor. rate



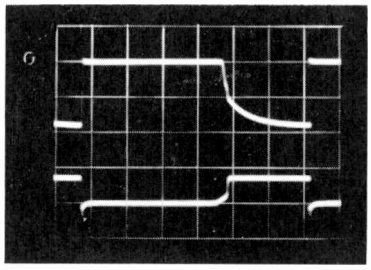
B. Top: Q17 emitter, 10 μs/cm, 1v/cm
Bottom: R60 input, 10 μs/cm, 2v/cm



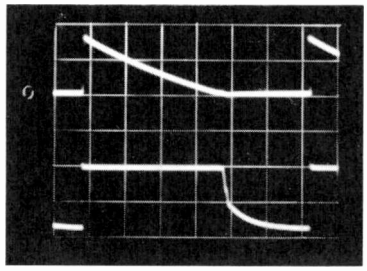
C. Top: Q17 collector, 10 μs/cm, 5v/cm
Bottom: Q17 emitter, 10 μs/cm, 1v/cm



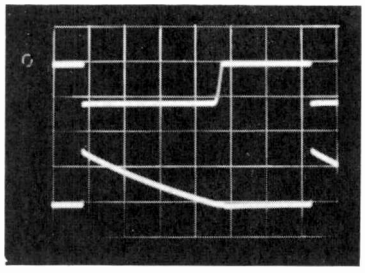
D. Top: Q7 base, 10 μs/cm, 1v/cm
Bottom: Q17 collector, 10 μs/cm, 5v/cm



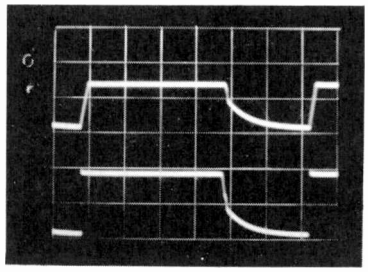
E. Top: Q7 collector, 10 μs/cm, 5v/cm
Bottom: Q7 base, 10 μs/cm, 1v/cm



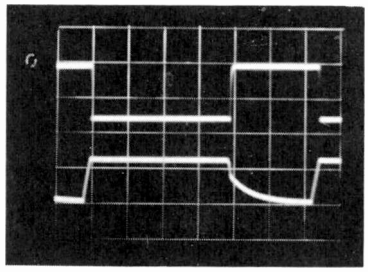
F. Top: Q6 base, 10 μs/cm, 5v/cm
Bottom: Q7 collector, 10 μs/cm, 5v/cm



G. Top: Q6 collector, 10 μs/cm, 5v/cm
Bottom: Q6 base, 10 μs/cm, 5v/cm



H. Top: Q16 base, 10 μs/cm, 5v/cm
Bottom: Q7 collector, 10 μs/cm, 5v/cm



I. Top: Q16 collector, 10 μs/cm, 2v/cm
Bottom: Q16 base, 10 μs/cm, 5v/cm

Figure 106—Typical Waveforms, Sync Amplifier, Horizontal Square Wave Multivibrator and Horizontal Square Wave Delay Generator Circuits

R21 to the base of Q5, the sampling pulse clipper. This is a boxcar* circuit which generates a narrow pulse, the leading edge of which corresponds, in time, to the leading edge of sync. The positive-going portion of the differentiated signal on the base is clipped by the diode action of the base-to-emitter junction of Q5. The remaining negative portion of this signal triggers the boxcar action of Q5. The positive output pulse at the collector of Q5 is direct-coupled to the base of the sampling pulse driver, Q4.

In the sampling pulse driver circuit, a negative pulse from the collector and a positive pulse from the emitter of Q4 apply forward bias to all four diodes simultaneously. At the tips of the pulses, the diodes conduct momentarily connecting the sawtooth voltage to capacitor C7 which acts as a memory device, storing the instantaneous voltage of the sawtooth at the moment of connection. During the remainder of the horizontal period, the diodes are reverse biased and C7 remains at the clamped voltage which sets the operating point for the afc current amplifier, Q3, which supplies the afc bias to the 2H master oscillator, Q1, Q2.

If the incoming tape sync signal changes frequency or phase slightly, the sampling pulse derived from it occurs at a slightly different time relative to the sawtooth voltage applied to the phase comparator. Therefore, there is a change in the instantaneous voltage to which C7 charges. This change causes the afc current to change the frequency and phase of the master oscillator to correspond to that of the incoming signal. When the afc loop is operating properly, sampling of the sawtooth voltage takes place on the fast positive-going portion of the sawtooth.

* *See Basic Circuit Descriptions on page 128.*

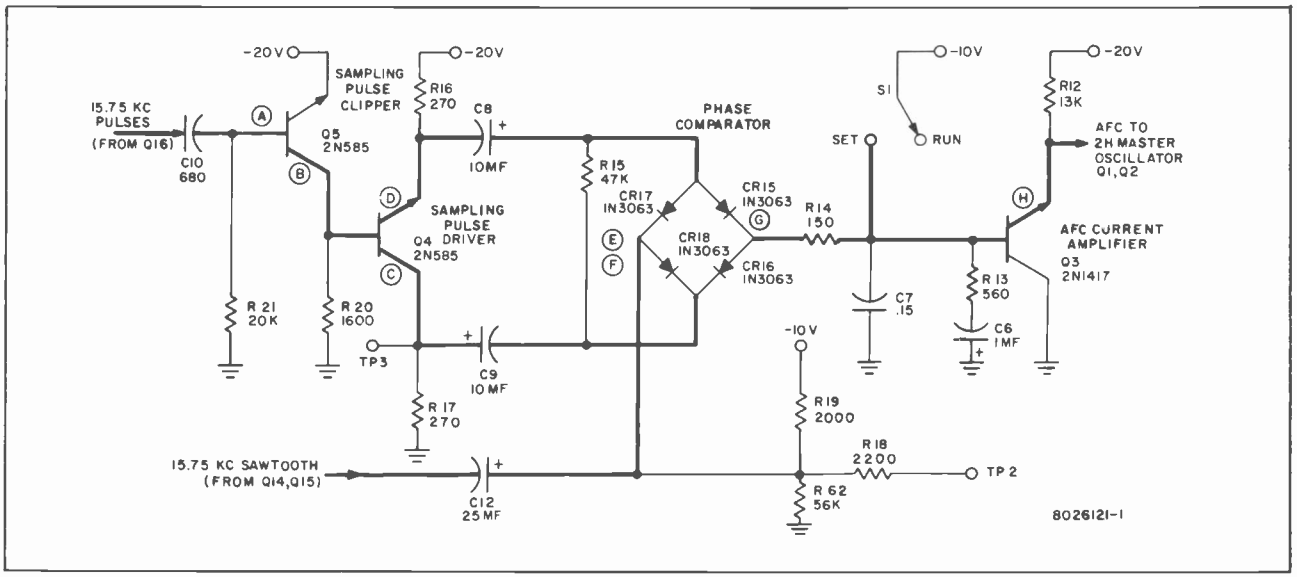
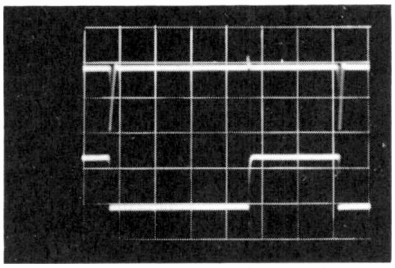
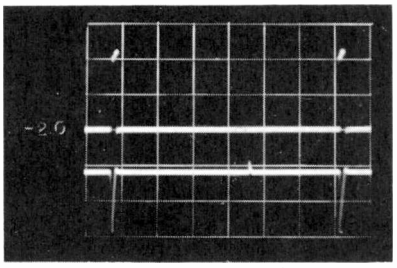


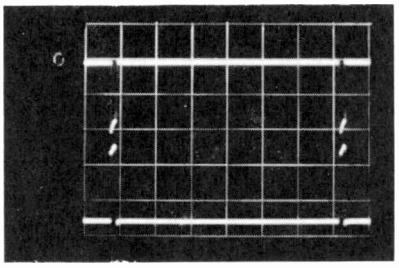
Figure 107—Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier



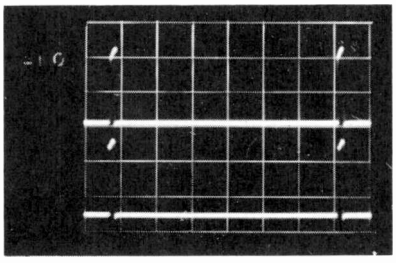
A. Top: Q5 base, 10 μs/cm, 1v/cm
Bottom: Q16 collector, 10 μs/cm, 2v/cm



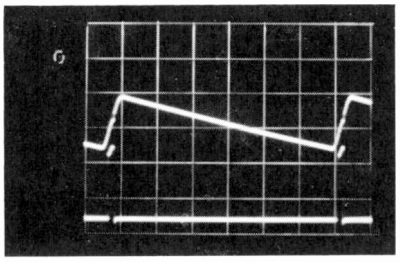
B. Top: Q5 collector, 10 μs/cm, 5v/cm
Bottom: Q5 base, 10 μs/cm, 1v/cm



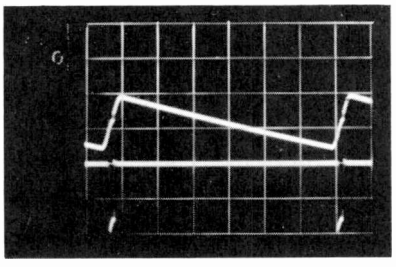
C. Top: Q4 collector, 10 μs/cm, 5v/cm
Bottom: Q4 base, 10 μs/cm, 5v/cm



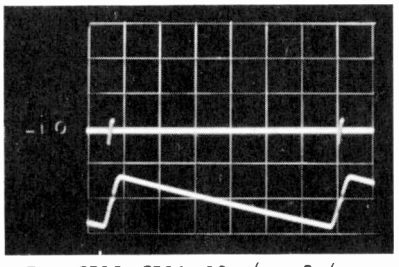
D. Top: Q4 emitter, 10 μs/cm, 5v/cm
Bottom: Q4 base, 10 μs/cm, 5v/cm



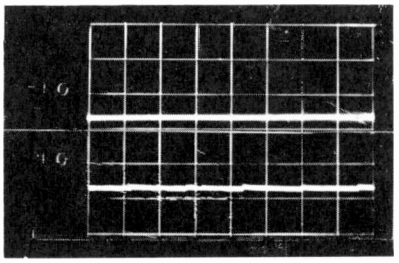
E. Top: CR17, CR18, 10 μs/cm, 5v/cm
Bottom: CR17, CR15, 10 μs/cm, 5v/cm



F. Top: CR17, CR18, 10μs/cm, 5v/cm
Bottom: CR18, CR16, 10 μs/cm, 5v/cm



G. Top: CR15, CR16, 10μs/cm, 2v/cm
Bottom: CR17, CR18, 10 μs/cm, 5v/cm



H. Top: Q3 emitter, 5 ms/cm, 1v/cm, vert. rate
Bottom: Q3 emitter, 10 μs/cm, 1v/cm, hor. rate

Figure 108—Typical Waveforms, Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier

Adjustments

2H Master Oscillator

An oscilloscope or a monitor triggered with external sync, such as the system picture monitor, can be used to adjust the center frequency of the master oscillator.

Using Oscilloscope

1. Observe the video output on the CRO by pressing VID OUT on the CRO switcher.

2. Set the CRO to the HOR sweep rate with EXT sync.

3. Press and hold the AFC OFF pushbutton (switch S1) on the front of the Horizontal AFC module. Adjust the 2H FREQ control, R2, until the pattern on the CRO is as nearly stationary as possible. Release the pushbutton.

Using Picture Monitor

1. Observe the video output on the picture monitor by pressing VID OUT on the monitor switcher.

2. Repeat step 3 above.

NOTE: To make the remaining internal adjustments, the Horizontal AFC module should be mounted in an extender. In addition, the last adjustment in this series, Sync Timing, requires the use of a dual trace oscilloscope.

Front Porch Width

1. Connect the oscilloscope to one of the three VID test jacks (TP1, TP2, TP3) on the front of the Video Output module.

2. Adjust the oscilloscope to display a horizontal blanking interval.

3. Adjust the FRONT PORCH WIDTH control, R37, to obtain a width of 1.7 microseconds.

Horizontal Sync Width

1. Connect the oscilloscope to one of the three VID test jacks (TP1, TP2, TP3) on the front of the Video Output module.

2. Adjust the oscilloscope to display a horizontal blanking interval.

3. Adjust the HOR SYNC WIDTH control, R45, to obtain a horizontal sync pulse 4.76 microseconds wide.

Sync Timing

1. Connect input 1 of a dual trace oscilloscope to the incoming tape sync (input side of R60) and connect input 2 to one of the three VID test jacks (TP1, TP2, TP3) on the Video Output module.

2. Lock the oscilloscope externally at a horizontal rate and use tape sync (input side of R60) for the trigger input.

3. Adjust the SYNC TIMING control, R56, so that the leading edge of the sync on the output signal is halfway between the leading edge of the sync on the incoming video, i.e., at TP1 on the Video/FM Control module and the leading edge of tape sync.

International Version

(Refer to the International Horizontal AFC schematic in the TR-4 Diagram Manual, IB-31807.)

In adapting the Horizontal AFC module to international standards, new time constant components and switching systems for the HN and HI busses were added, along with a two-transistor starting circuit for the 2H master oscillator.

The starting circuit, Q18 and Q19, insures that the 2H master oscillator keeps running at all times. This circuit prevents a situation from arising that could lead to both transistors of the 2H master oscillator being saturated at the same time. Were such a condition to occur, even for an instant, the collectors of both Q1 and Q2 would assume the same potential as that of their emitters, approximately −10 volts, and the 2H master oscillator would remain at rest, generating no output.

The start circuit transistors are turned on and off alternately by means of the biasing arrangement employed. The voltage at the junction of R4 and R7 cannot be more negative than −10 volts. Therefore, the voltage developed across the divider network consisting of R63, R81 and the parallel combination of R4 and R7 provides a bias on the base of Q18 that is more positive than the −10 volts on the emitter and thus cuts off this transistor. The bias voltage on the base of Q19 is developed across the voltage divider consisting of R67, R66, and R82. This voltage is more negative than that on the emitter of Q19, therefore this transistor is driven into saturation and virtually the full potential on the emitter (−10 volts) appears on the collector. The voltage on the collector of Q19 is applied across R32 and R33 to the bases of Q1 and Q2, respectively. Since there is −10 volts on the emitters of Q1 and Q2 already, the −10 volts on the bases of Q1 and Q2 causes them to become reverse biased. In this state, assuming perfect equilibrium between Q1 and Q2, no current will flow in the emitter-base circuit of either transistor, therefore both will be cut off. However, since there is inherently some unbalance between the components of each half of the multivibrator, one side of the 2H master oscillator will

begin to conduct before the other. Thus one transistor is driven into saturation and the other is cut off.

At the same time, the states of Q18 and Q19 are reversed. Now Q19 is cut off, and current from the HI or HN bus is allowed to flow into the base of the saturated transistor. Transistor Q18 is turned on by the bias on the base, which is now more negative than the voltage on the emitter. The bias is obtained from the −20 volt supply and is developed across the divider network formed by R63, R81, and the 1000 and the 750 ohm resistors in the collector circuit of the transistor that is cut off.

The time constant components are the same for both 525- and 625-line standards. For 405- or 819-line standards, different time constant components are switched into the circuits by means of the HN and HI busses. The TV STANDARDS switch used to select the desired line standard is located on the front panel of the International Vertical Advance (module B22). On 525- and 625-line standards, the HN bus is at −20 volts and the isolation diodes in the related time constant circuits are forward biased. Conversely, the HI bus is at ground potential and the isolation diodes associated with time constant components connected to this bus are reverse biased or cut off.

New time constants are switched into the circuits of the following stages on 405- or 819-line standards for the reasons stated.

1. Horizontal Square Wave Multivibrator (Q6, Q7) for setting the horizontal frequency to the proper duty cycle.

2. ÷ 2 Multivibrator (Q9, Q10) for proper timing of the front porch interval.

3. Horizontal Sync Clipper (Q12) for setting the width of regenerated sync.

4. Horizontal Square Wave Delay Generator (Q16) for correct timing of regenerated sync with respect to reference sync.

Vertical Advance (Module B22)

General

The Vertical Advance module (see figure 109) is required to produce the timing edge which determines the leading edge of vertical blanking and the 9H gating pulse. The method of vertical pulse advance used must regenerate the vertical blanking edge, which precedes the vertical sync signal by 3H. The technique used to obtain vertical advance is that of counting horizontal pulses between adjacent vertical intervals. The counters are designed to follow any change in basic sync frequency and automatically readjust the position of vertical blanking. Moreover, they recover quickly from transient disturbances in the recording system.

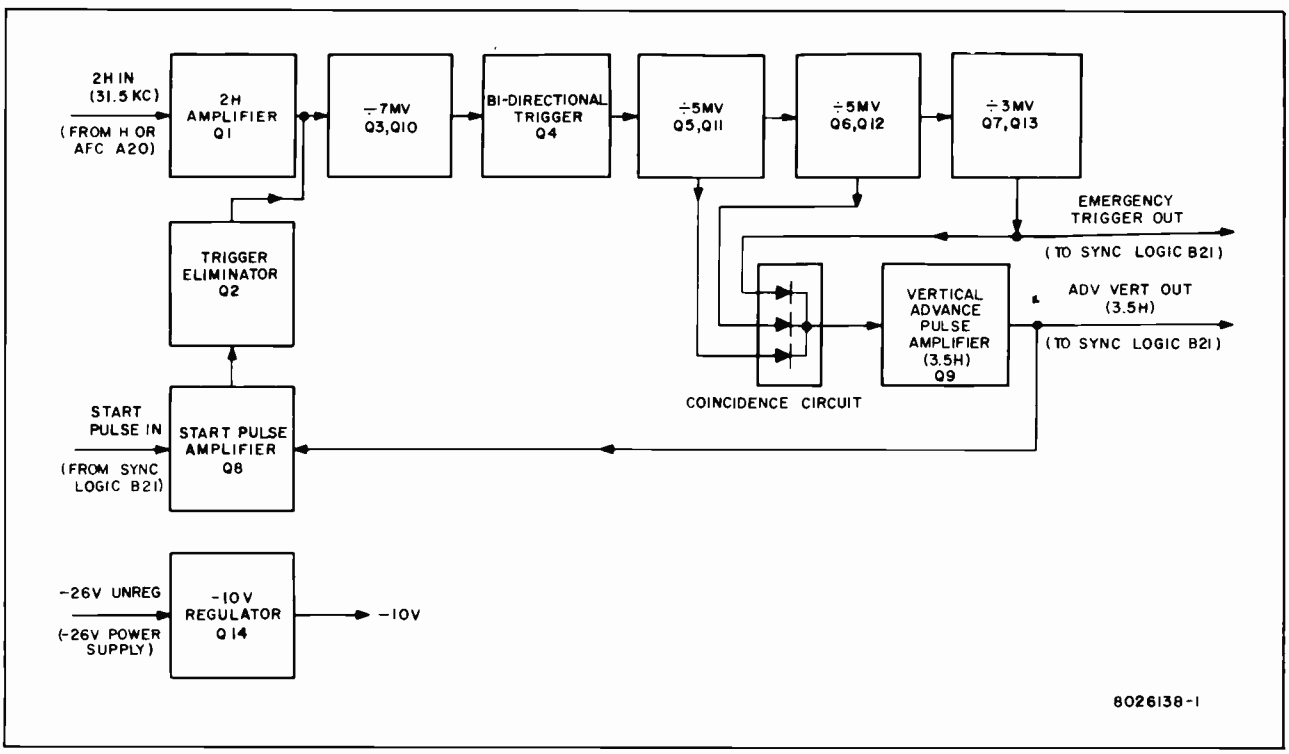


Figure 109—Block Diagram, Vertical Advance Module

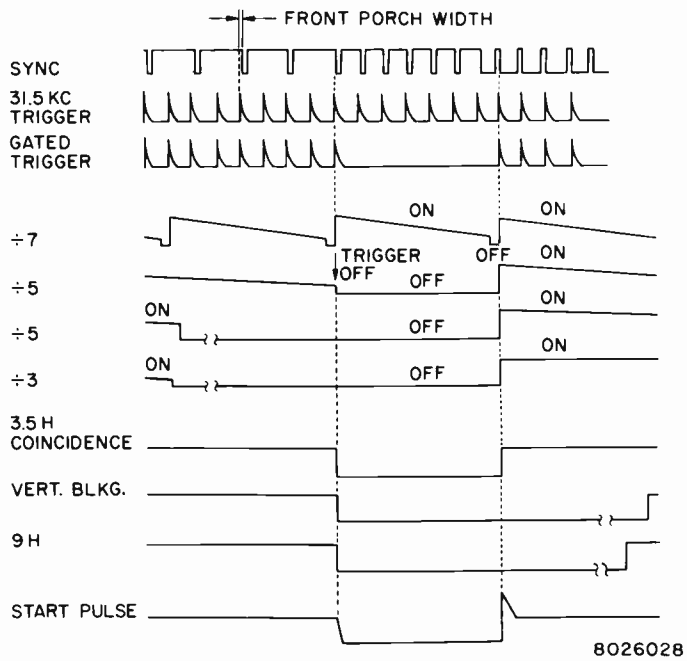


Figure 110—Pulse Timing Chart

Timing Chart

In the timing chart, figure 110, the relative positions of the vertical blanking edge, equalizing pulses and vertical sync interval are shown. The leading edge of the second vertical sync pulse is the earliest possible time for detecting accurately the position in vertical sync. Although the timing difference between the beginning of vertical blanking and vertical sync is 3H, observe on the timing chart that the difference between the two edges (vertical blanking and the second vertical sync pulse position) is actually 3.5H. This timing distance of 3.5H must be maintained to produce vertical blanking from vertical sync. The timing distance of 3.5H is exactly the period of a ÷ 7 MV counter running from a 31.5 kc master oscillator. The vertical advance circuits must, therefore, select that one period of the ÷ 7 MV (one out of the 75 periods which occur in each field) which is so phased that the beginning of the period falls on the leading edge of vertical blanking and the end of the period falls 3.5H later in vertical sync. As shown in figure 109, the 31.5 kc pulses supplied through the 2H amplifier, Q1, and the trigger eliminator, Q2, activates a string of counters. The count is initiated by the start pulse which is generated from the vertical sync in the Sync Logic module. The counters count for 259 lines then shut off due to the coincidence of the last three counters (÷ 5, ÷ 5, ÷ 3) and normally remain shut off for a period of 3.5H. This period of 3.5H added to 259H equal 262.5 lines or one field. The next cycle is started by the generation of another START pulse in the Sync Logic module. Under unusual operating conditions due to a non-synchronous switch or a bad splice in the tape, the vertical sync period of the tape sync signal may arrive at a much later time. In this event, the counters remain off until a new start pulse is generated when vertical sync does arrive.

Gating Circuits

As shown in the simplified schematic, figure 111, the 31.5 kc input pulses from the Horizontal AFC module are applied to the base of Q1 through the differentiating network C1 and R1. The 2H amplifier, Q1, is an emitter follower which clips the negative spike from the differentiated pulse. The trigger pulses from the emitter of Q1 are coupled to the counter chain through the isolation diode, CR2.

The 31.5 kc pulses are gated by Q2, the trigger eliminator, which is driven to saturation during the 3.5H interval, shorting out the pulses. At all other times, Q2 is biased off, allowing the pulses to pass to the counter chain. The 3.5H pulse driving Q2 is coupled to its base from the collector of Q8, the start pulse amplifier. Transistor Q8 is also normally biased

off because its base is held to approximately zero volts, the potential on the anode of CR6. During the 3.5H pulse interval, the anode voltage of CR6 drops to −10 volts, allowing the base of Q8 to fall to the potential determined by the bias network of R31, R32, and R34. In this state, Q8 conducts and drives Q2 to saturation.

Transistors Q8 and Q2 remain conducting until a positive start pulse drives Q8 off which, in turn, drives Q2 off. This allows a 31.5 kc trigger pulse to pass, starting the counters and thereby terminating the 3.5H pulse. The base of Q8 is again held to zero volts and does not conduct.

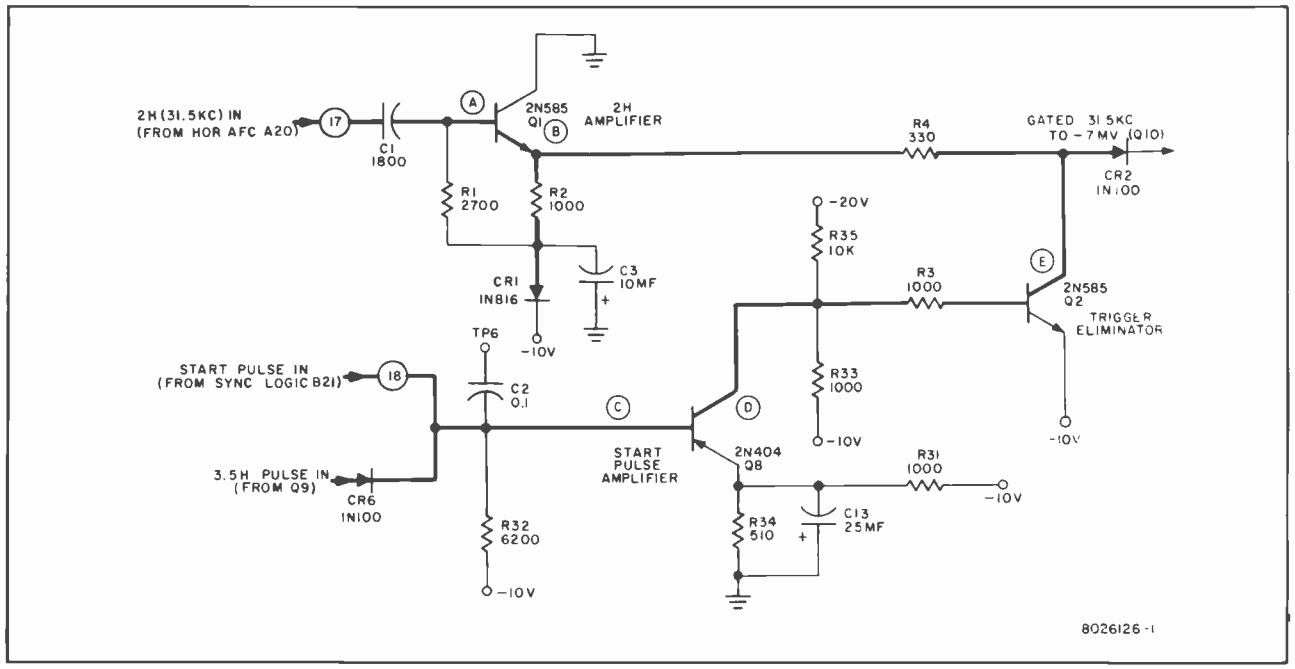
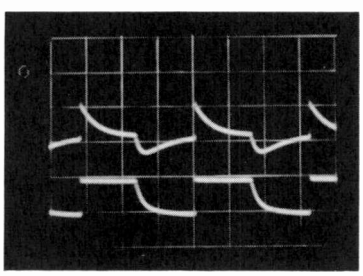
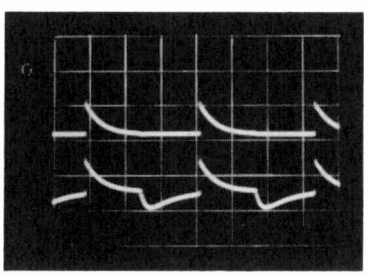


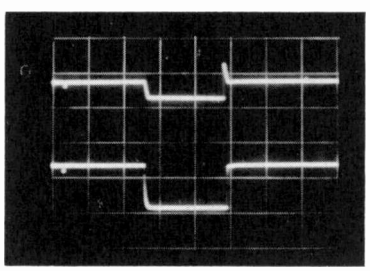
Figure 111—2H Amplifier, Start Pulse Amplifier and Trigger Eliminator Circuits



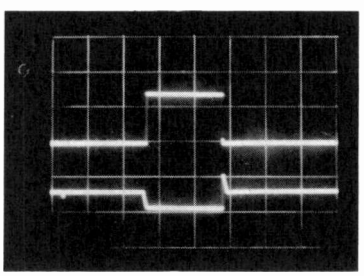
A. Top: Q1 base, 10 μs/cm, 5v/cm
Bottom: C1 input, 10 μs/cm, 5v/cm



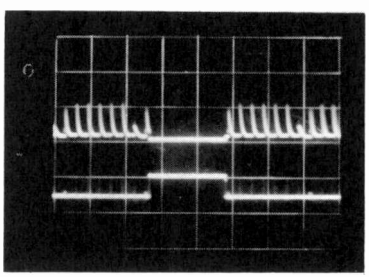
B Top: Q1 emitter, 10 μs/cm, 5v/cm
Bottom: Q1 base, 10 μs/cm, 5v/cm



C. Top: Q8 base, 100 μs/cm, 5v/cm
Bottom: CR6 input, 100 μs/cm, 5v/cm



D. Top: Q8 collector, 100 μs/cm, 5v/cm
Bottom: Q8 base, 100 μs/cm, 5v/cm



E. Top: Q2 collector, 100 μs/cm, 5v/cm
Bottom: Q2 base, 100 μs/cm, 2v/cm

Figure 112—Typical Waveforms, 2H Amplifier, Start Pulse Amplifier and Trigger Eliminator Circuits

Counters

As shown in figure 113, the first counter, the ÷ 7 MV, is a monostable multivibrator consisting of Q3 and Q10. It is similar in design to the ÷ 2 MV in the Horizontal AFC module. Both transistors, Q3 and Q10, conduct in the stable state. When the base is driven positive by the first pulse, Q3 is driven to cutoff (also cutting off Q10). Time constant C4, R6, and R7 determine the length of time the multivibrator is cut off. The transistor must return to the stable conducting state just after the seventh pulse.

The operation of the first ÷ 5 multivibrator (Q5, Q11) is similar to that of the ÷ 7 multivibrator. However, the conducting time of the transistors is not entirely dependent on the time constant of C9, R19, and R20. Variations in component values and transistor characteristics cause slight variations in timing. Since one of the conduction times of the multivibrator is the 3.5H pulse, precise timing is essential for both on and off transitions. This is accomplished by using the trigger not only to start but also to stop the timing cycle.

The positive and negative trigger pulses required to start and stop the ÷ 5 counter are generated by the bidirectional trigger, Q4, in conjunction with diodes CR3 and CR4. As shown in figure 113, the collector of Q4 is dc connected through CR4 and R17 to the junction of R44 and R45 in the collector circuit of Q11. In the stable state of the multivibrator, when Q11 is conducting, the voltage at the junction of R44 and R45 is almost −10 volts, and Q4 does not conduct since the emitter and collector of Q4 are at the same potential. However, a positive spike resulting from the differentiation of the ÷ 7 pulse is passed by CR3 through C9 to the base of Q5. The positive spike cuts off Q5 and Q11, and the voltage at the junction of R44 and R45 rises to zero volts. In this condition, CR3 is reverse-biased and does not pass the positive spikes. Now, however, the collector-to-emitter voltage of Q4 is sufficient to provide amplification of the positive spikes fed to its base. The resulting negative trigger pulses at the collector of Q4 are passed through CR4 and C9 to the base of Q5. On the fifth count, Q5 and Q11 are driven into conduction, and the cycle repeats.

As shown in figure 115, the final two counters, the ÷ 5 MV (Q6, Q12) and the ÷ 3 MV (Q7, Q13) are identical in operation to the ÷ 7 MV (Q3, Q10). Each multivibrator conducts in the stable state; each is cut off by the positive spike resulting from the differentiation of the trailing edge of the preceding pulse output. The trailing edge of the ÷ 3 counter pulse is used as an emergency trigger for the vertical blanking generator multivibrator in the Sync Logic module.

Coincidence Gate

The coincidence gate (figure 115) consists of three diodes, CR7, CR9, CR10. The cathode of each diode is connected to −10 v through resistor R36. The anode of each diode is connected to the collector of the output

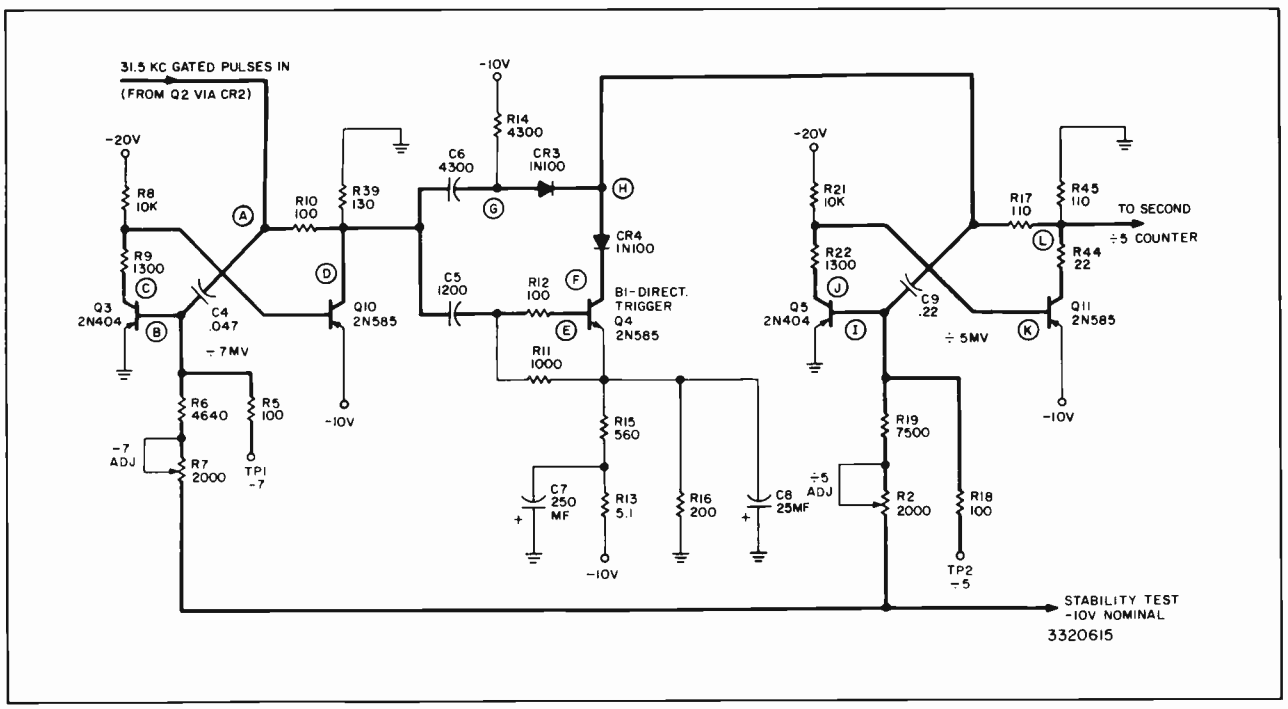
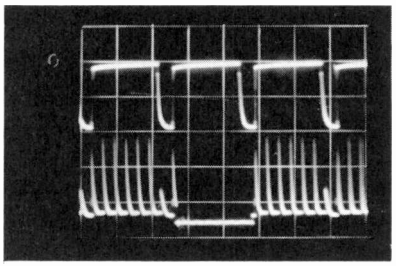
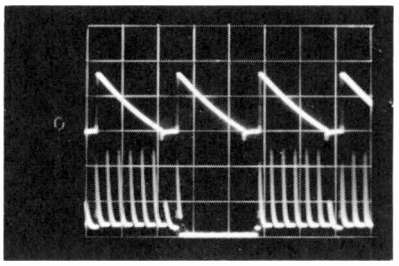


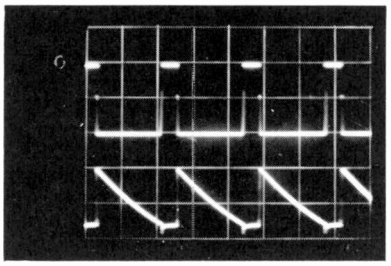
Figure 113— ÷ 7 Counter, Bi-Directional Trigger and First ÷ 5 Counter Circuits



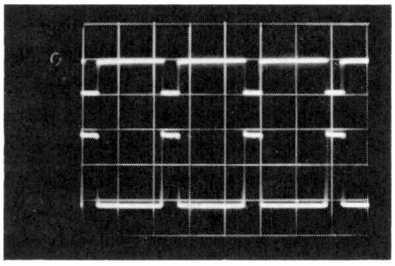
A. Top: C4, R10, CR2, 100 μs/cm, 5v/cm
Bottom: gated 31.5 kc (Q2 collector, 100 μs/cm, 2v/cm)



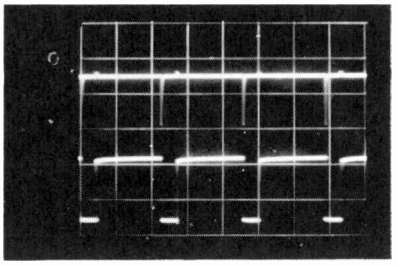
B. Top: Q3 base, 100 μs/cm, 5v/cm
Bottom: gated 31.5 kc (Q2 collector, 100 μs/cm, 2v/cm)



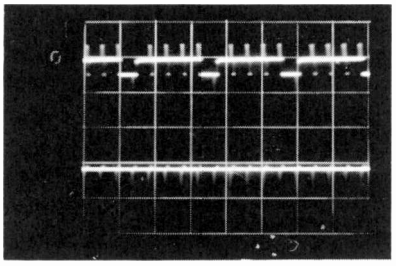
C. Top: Q3 collector, 100 μs/cm, 10v/cm
Bottom: Q3 base, 100 μs/cm, 5v/cm



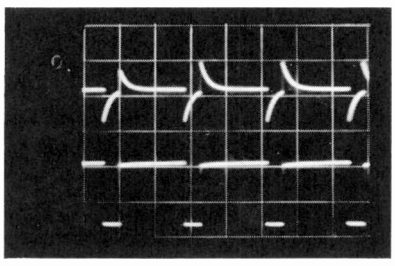
D. Top: Q10 collector, 100 μs/cm, 10v/cm
Bottom: Q10 base, 100 μs/cm, 5v/cm



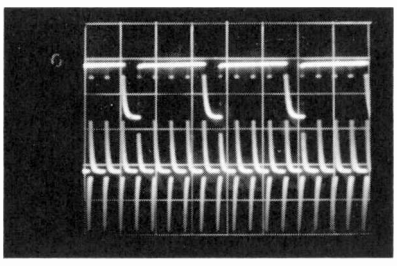
E. Top: Q4 base, 100 μs/cm, 5v/cm
Bottom: Q10 collector, 100 μs/cm, 5v/cm



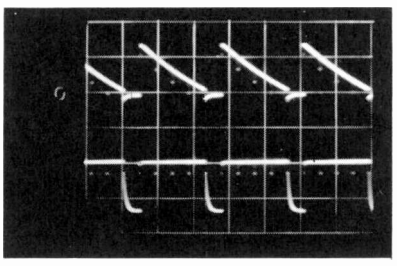
F. Top: Q4 collector, 500 μs/cm, 5v/cm
Bottom: Q4 base, 500 μs/cm, 5v/cm



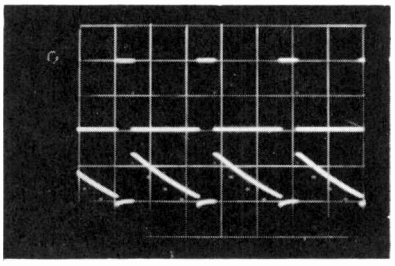
G. Top: C6, CR3, R14, 100 μs/cm, 10v/cm
Bottom: Q10 collector, 100 μs/cm, 5v/cm



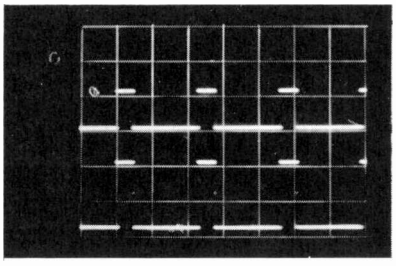
H. Top: CR3, CR4, 500 μs/cm, 5v/cm
Bottom: C6, CR3, R14, 500 μs/cm, 5v/cm



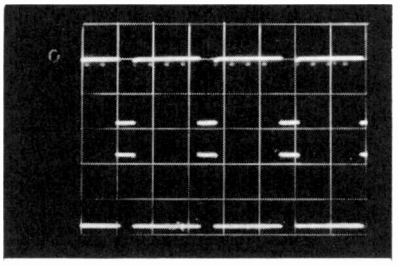
I. Top: Q5 base, 500 μs/cm, 5v/cm
Bottom: C9, R17, 500 μs/cm, 5v/cm



J. Top: Q5 collector, 500 μs/cm, 10v/cm
Bottom: Q5 base, 500 μs/cm, 5v/cm



K. Top: Q11 base, 500 μs/cm, 10v/cm
Bottom: Q5 collector, 500 μs/cm, 10v/cm



L. Top: Q11 collector, 500 μs/cm, 5v/cm
Bottom: Q11 base, 500 μs/cm, 5v/cm

Figure 114—Typical Waveforms, ÷ 7 Counter, Bi-Directional Trigger and First ÷ 5 Counter Circuits

transistor of each of the last three counter multivibrators, ÷ 5 MV, ÷ 5 MV, and ÷ 3 MV. When any one of these multivibrators is in the non-conducting (counting) state, its collector is at zero volts, and the corresponding diode connected to its collector conducts, holding the base of the vertical advance pulse (3.5H) amplifier, Q9, close to zero volts, causing the amplifier to conduct. However, if none of these multivibrators are counting, a condition which occurs 259H from the start of the counter cycle, none of the diodes conduct. The base of Q9 then drops to −10 volts and the transistor is cut off. The emitter of Q9 is normally at zero volts when the transistor is conducting, providing the holding voltage for the anode of CR6 of the trigger gating circuits. During the 3.5H period of coincidence, this voltage drops to −10 volts.

Stability Test

The stability test circuit (figure 115) provides a temporary variation in the power supply voltage to ensure that the counters have been set approximately in the middle of the range in which they provide the proper count. If one or more of the counters has been set too near the edge of its range, it will miscount when the STABILITY TEST button is pressed and the STABILITY RANGE potentiometer, R41, is varied. (The procedure for adjusting the counters is given at the end of this description, under Adjustments.)

Included on this module is a −10 volt regulator, Q14. (See the overall schematic in the TR-4 Diagram Manual, IB-31807.) The regulator isolates the large current surges on the −10 v bus in the Vertical Advance module from the remainder of the tape recorder. Transistor Q14 also provides a low-impedance power source for the Vertical Advance module.

Adjustments

Stability Test of Counter Multivibrators

The STABILITY RANGE control, potentiometer R41, and the STABILITY TEST control, pushbutton switch S1, are mounted on the front of the Vertical Advance module. When the STABILITY TEST pushbutton is pressed, a variable voltage can be applied to the counter circuits by rotating the STABILITY RANGE knob. When this voltage is varied (±.5 volt) the stability of the counters is determined. This voltage variation simulates a frequency error in the multivibrators. If each is operating correctly, no change takes place in the multivibrator operation. However, if a multivibrator is bordering on improper operation, rotating the STABILITY RANGE potentiometer

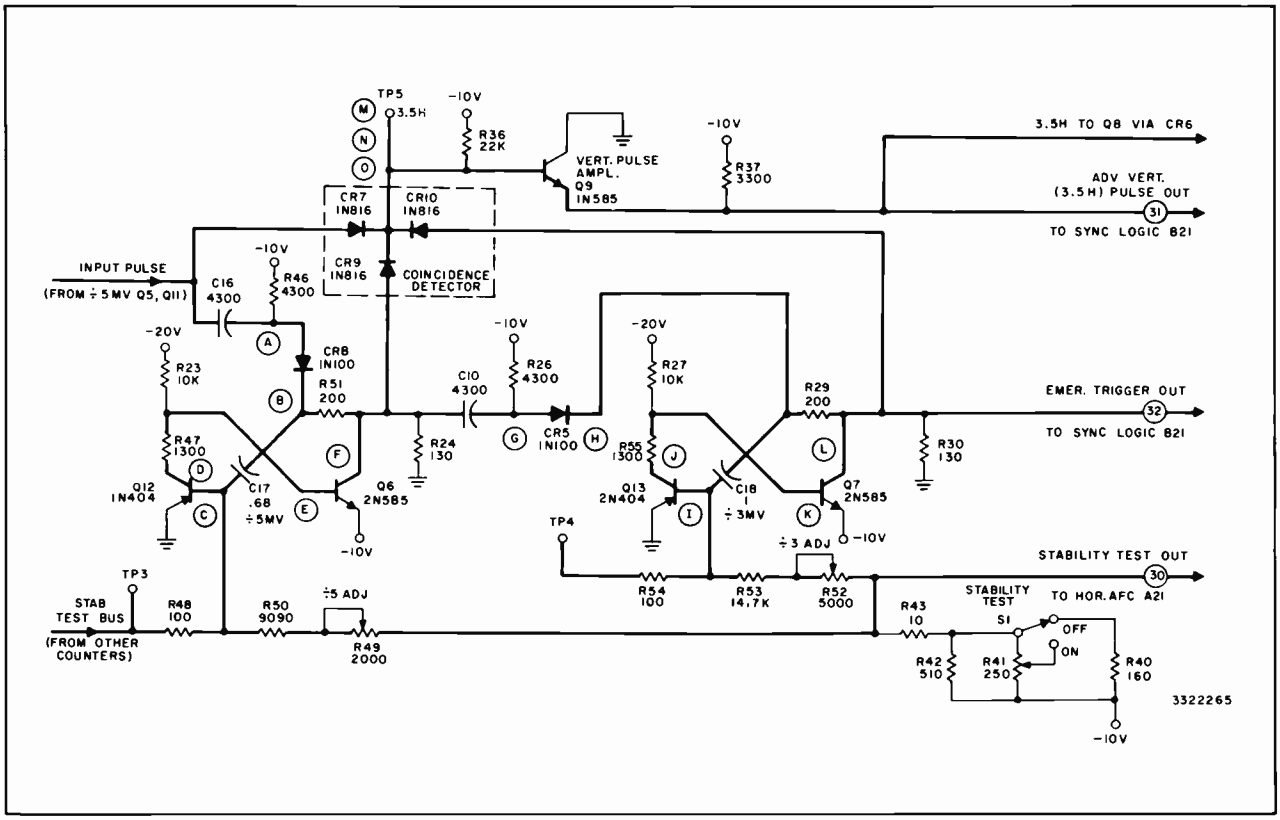
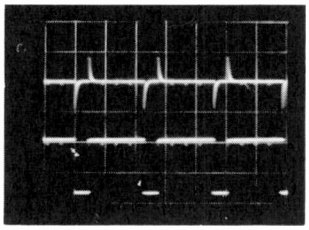
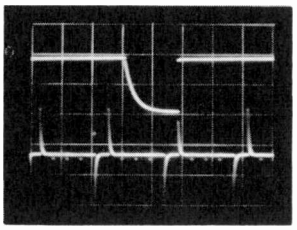


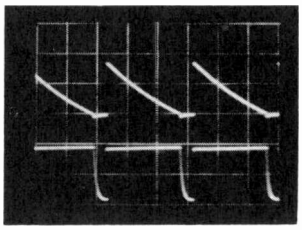
Figure 115—Second ÷ 5 Counter, ÷ 3 Counter, Coincidence Detector and Vertical Pulse Amplifier Circuits



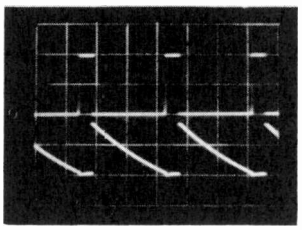
A. Top: C16, CR8, R46, 500 μs/cm, 10v/cm
Bottom: Q11 collector, 500 μs/cm, 5v/cm



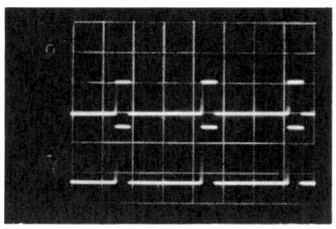
B. Top: C17, CR8, R51, 500 μs/cm, 5v/cm
Bottom: C16, CR8, R46, 500 μs/cm, 5v/cm



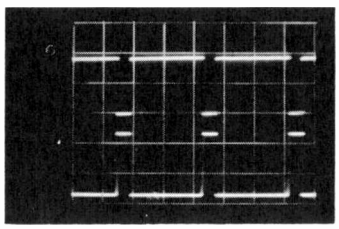
C. Top: Q12 base, 2 ms/cm, 5v/cm
Bottom: C17, CR8, R51, 2 ms/cm, 5v/cm



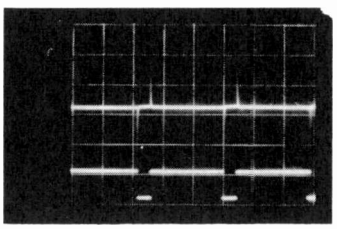
D. Top: Q12 collector, 2 ms/cm, 10v/cm
Bottom: Q12 base, 2 ms/cm, 5v/cm



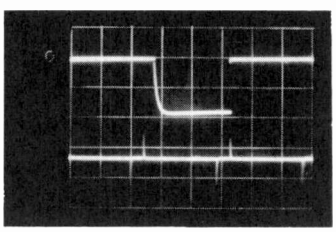
E. Top: Q6 base, 2 ms/cm, 10v/cm
Bottom: Q12 collector, 2 ms/cm, 10v/cm



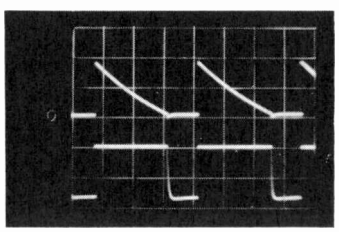
F. Top: Q6 collector, 2 ms/cm, 5v/cm
Bottom: Q6 base, 2 ms/cm, 5v/cm



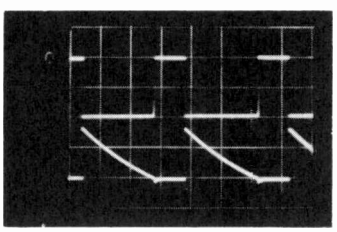
G. Top: C10, CR5, R26, 2 ms/cm, 5v/cm
Bottom: Q6 collector, 2 ms/cm, 10v/cm



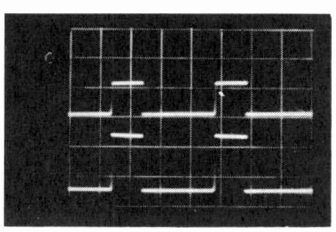
H. Top: C18, CR5, R29, 2 ms/cm, 5v/cm
Bottom: C10, CR5, R26, 2 ms/cm, 10v/cm



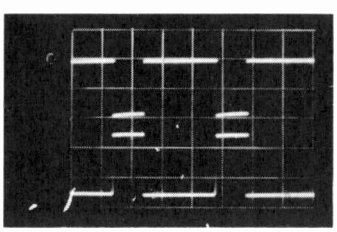
I. Top: Q13 base, 5 ms/cm, 5v/cm
Bottom: C18, CR5, R29, 5 ms/cm, 5v/cm



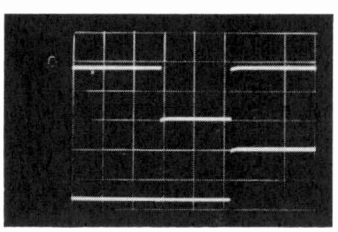
J. Top: Q13 collector, 5 ms/cm, 10v/cm
Bottom: Q13 base, 5 ms/cm, 5v/cm



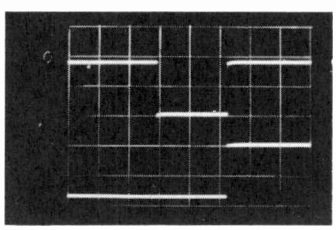
K. Top: Q7 base, 5 ms/cm, 10v/cm
Bottom: Q13 collector, 5 ms/cm, 10v/cm



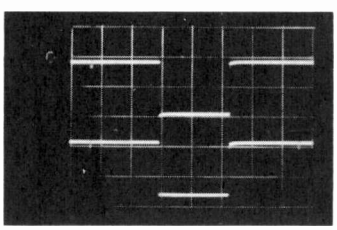
L. Top: Q7 collector, 5 ms/cm, 5v/cm
Bottom: Q7 base, 5 ms/cm, 5v/cm



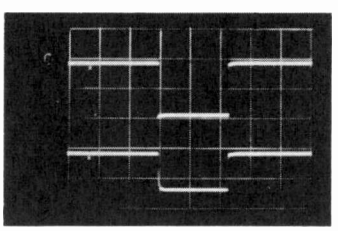
M. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q7 collector, 100 μs/cm, 5v/cm



N. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q6 collector, 100 μs/cm, 5v/cm



O. Top: TP5, 100 μs/cm, 5v/cm
Bottom: Q11 collector, 100 μs/cm, 5v/cm



P. Top: Q9 emitter, 100 μs/cm, 5v/cm
Bottom: TP5, 100 μs/cm, 5v/cm

Figure 116—Typical Waveforms, Second ÷ 5 Counter, ÷ 3 Counter, Coincidence Detector and Vertical Pulse Amplifier Circuits

knob will cause it to go into improper operation. The stability test circuit also checks the operation of the ÷ 2 multivibrator in the Horizontal AFC module. This, however, is an extremely stable circuit because of the low order of division and does not require adjustment.

The 3.5H pulse (see figure 116, waveform M, N, or O) is used to detect any improper operation of the Vertical Advance Counters. The procedure for checking the counters is given below.

1. Place the TR-4 in STANDBY or in STOP mode. Remove the Modulator (module A2); place the MOD-PLAY switch (S4) in MOD position then replace the Modulator.

2. Connect an oscilloscope to the 3.5H test point (TP5) on the front of the module.

3. Set the oscilloscope sweep time to vertical rate and expand the trace to observe the 3.5H pulse.

4. Press and hold the STABILITY TEST pushbutton; then rotate the STABILITY RANGE control through its entire range. The pulse width and amplitude should not change in any respect. Minor disturbances appearing on the base line do not indicate improper operation. If the pulse width or amplitude change while the control is being rotated, the counters must be readjusted.

Adjustment of Counters

The counters, the 3.5H pulse, and the start pulse in the Vertical Advance module form a continuous loop which makes it difficult, when a marginal counter is indicated, to determine which counter is at fault. The following procedure provides a method for identifying and correcting a marginal or defective counter.

Use of a single trace oscilloscope is assumed in the following procedure, therefore it is necessary to change the sweep of the oscilloscope as indicated in the following in order to maintain the various counter signals within the 10 cm display of the CRO. However, with a dual trace oscilloscope inspection of the signals is somewhat simplified, since the output of each counter may be compared directly to the output of the preceding stage. This makes it unnecessary to set the sweep at an arbitrary 10 cm.

The adjustments described in step 1 (below) is a precautionary measure. This step may be omitted provided it is ascertained that the Horizontal AFC module is functioning properly.

To perform the following adjustments, the module under test must be mounted in an extender.

Horizontal AFC Module

1. Set the oscilloscope on internal trigger. Place the probe on the emitter of Q8. (This is the source of 31.5 kc pulses from the master oscillator, Q1, to the ÷ 2 multivibrator, Q9, Q10.) Adjust the oscilloscope sweep so that two 31.5 kc pulses cover 10 cm on the oscilloscope. Then move the probe to the ÷ 2 test point, TP1. One cycle of the ÷ 2 MV should be 10 cm wide; if not, a failure in the Horizontal AFC module is indicated. This must be corrected before adjusting the counters in the Vertical Advance module. If the width of the ÷ 2 counter cycle is correct, press and hold the STABILITY TEST pushbutton (on the front of the Vertical Advance module) and, at the same time, rotate the STABILITY RANGE control through its entire range. The width of the ÷ 2 waveform should not change at any position of the knob. The ÷ 2 counter must pass this test before the counters in the Vertical Advance module can be adjusted.

Vertical Advance Module

2. Disconnect the collector lead of Q2 from the terminal at the junction of CR2 and R4; leave the jumper and CR2 connected to the terminal. (This opens the loop and allows the counters to run freely.)

3. Set the oscilloscope on internal trigger. Locate C1 which is connected to the base of Q1 and place the probe on the input side of C1. The CRO display will show the 31.5 kc input signal.

4. Adjust the sweep so that seven 31.5 kc pulses cover 10 cm on the oscilloscope. Then move the probe to the ÷ 7 test point, TP1. One cycle of the ÷ 7 MV should be 10 cm (seven 31.5 kc pulses) wide. If it is not, adjust R7, the ÷ 7 MV "trim-pot", until the cycle measures 10 cm.

5. Press and hold the STABILITY TEST pushbutton, and rotate the STABILITY RANGE control through its range. The width of the ÷ 7 cycle should not change.

6. Set the oscilloscope sweep so that five ÷ 7 pulses cover 10 cm on the oscilloscope. Place the probe on the first ÷ 5 test point, TP2. One cycle of the first ÷ 5 MV (Q5, Q11) should be 10 cm (five ÷ 7 pulses) wide. To obtain this it may be necessary to adjust the ÷ 5 "trim-pot", R20. If so, repeat step 5, this time observing the width of the ÷ 5 cycle, which should not vary.

7. Change the oscilloscope sweep so that five ÷ 5 pulses cover 10 cm on the oscilloscope. Place the probe on the second ÷ 5 test point, TP3. One cycle of the second ÷ 5 MV (Q6, Q12) should be 10 cm wide (the width of five of the first ÷ 5 pulses). If it is not,

adjust the second ÷ 5 "trim-pot", R49, then repeat step 5 in order to determine the stability of the second ÷ 5 counter.

8. Change the oscilloscope sweep so that three of the second ÷ 5 pulses cover 10 cm on the oscilloscope. Place the probe on the ÷ 3 test point, TP4. One cycle of the ÷ 3 MV (Q7, Q13) should be 10 cm wide (the width of three of the second ÷ 5 pulses). If not, adjust the ÷ 3 "trim-pot", R52, and again perform step 5 to determine the stability of the ÷ 3 counter.

9. Reconnect the collector of Q2 to the terminal, and replace the module in the tape recorder.

10. Refer to the first section of this procedure, *Stability Test of Counter Multivibrators,* and re-check the stability of the counters according to the instructions in steps 1 through 4.

NOTES

1. Proper counter operation is necessary but not sufficient to insure proper vertical advance. In some cases proper counting may be obtained with the collector of Q2 disconnected; however, when the loop is closed again by reconnecting Q2, improper advance is obtained. This condition results from improper off-time width of one of the counters, usually the second ÷ 5 MV (Q6, Q12). To detect the offending counter, locate the leading edge of the 3.5H pulse (which will be much wider than normal). The leading edge lines up with the turnoff edge of the offending counter. When the counter has been located, readjust its timing so as to lengthen its period. A point will be found where the counting chain jumps suddenly into proper operation. Continue to lengthen its period until the counter-chain holds to proper count throughout the entire range of the STABILITY RANGE control.

2. A condition may occur in the Vertical Advance module in which a blanking bar is generated only on alternate fields instead of on every field. This results from having the ÷ 3 MV adjusted for an excessively long time constant. The multivibrator cannot recover in time to be retriggered by the start pulse; therefore, it waits for one entire field before being retriggered. To eliminate this condition, simply readjust the ÷ 3 counter "trimpot", R52, to shorten the time constant, then check the final setting to be certain that the counter passes the STABILITY TEST.

3. Sometimes a condition occurs in which the Horizontal AFC module produces regenerated sync at 31.5 kc instead of 15.75 kc. A common cause of this fault is a shorted regulator transistor (Q14) in the Vertical Advance module. A quick check for this fault can be made by measuring the −10 volt bus in the Vertical Advance module. If transistor Q14 is shorted, the bus is at a more negative potential than −10 volts.

International Version

(Refer to the International Vertical Advance schematic in the TR-4 Diagram Manual, IB-31807.)

The Vertical Advance module designed to operate on international standards differs from the 525-line module in the following respects.

Separate time constant components are used for all standards in the first two counter stages, Q3, Q10, and Q5, Q11, respectively. In the third and fourth counters, Q6, Q12 and Q7, Q13, respectively, the time constants for the 405- and the 625-line standards are combined and the 525-time constants are separate. All time constants are selected by means of rotary switch S2, which is located in this module. This switch also supplies the international switching busses (HI, HN; VI, VN and VI SP, VN SP) with the proper dc operating levels. The switch control, designated TV STANDARDS, is mounted on the front panel of the module. In addition to new time constant components, the timing of the vertical advance pulse (3.5H) was changed to accommodate the 405- and the 625-line standards.

3H Vertical Advance for 625 Lines

Since there are five equalizing pulses in the 625-line system, the vertical advance must be 3H wide; however, the width of the first ÷ 5 count cycle is only 2.5H wide. Therefore, in order to produce a 3H pulse from the 2.5H count, a miscount pulse amplifier, Q15, and associated circuitry has been incorporated (see figure 117). The operation of this circuit is as follows:

The output of the fourth counter (Q7, Q13) is a 50-cycle signal, the leading or positive-going edge of which is used to trigger the miscount amplifier, Q15. The latter is a pulse narrowing* or "boxcar" circuit. The output of Q15 is a negative pulse, approximately 50 microseconds wide, that begins with the leading edge of the second vertical sync pulse. This pulse is applied to the first counter, Q3, Q10, through the timing network of C4 and R70.

During the duration of the miscount pulse, C4 discharges at a faster rate than when the pulse is absent so that it is discharged before the fifth trigger arrives, and then the counter can return to its resting state. This allows the fifth trigger to start the counter for the next count, thereby shortening the time cycle of the previous count (see figure 119). Additional energy is supplied from the miscount amplifier, Q15, to the second counter, Q5, Q11, through R73 during the miscount period. At the end of the miscount pulse period, the counter reverts to its normal counting

* *See Basic Circuit Descriptions on page 128.*

(÷ 5) rate. It continues to count at this rate until the next to the last count before the next field period.

The last count starts in the usual manner, and C4 discharges before the sixth trigger. However, at this time all of the counters are in the off or non-counting state, and the train of triggers from the 2H amplifier, Q1, are gated out by the trigger eliminator, Q2. During this time, there is no trigger to start the first counter before the sixth count is enclosed. After the

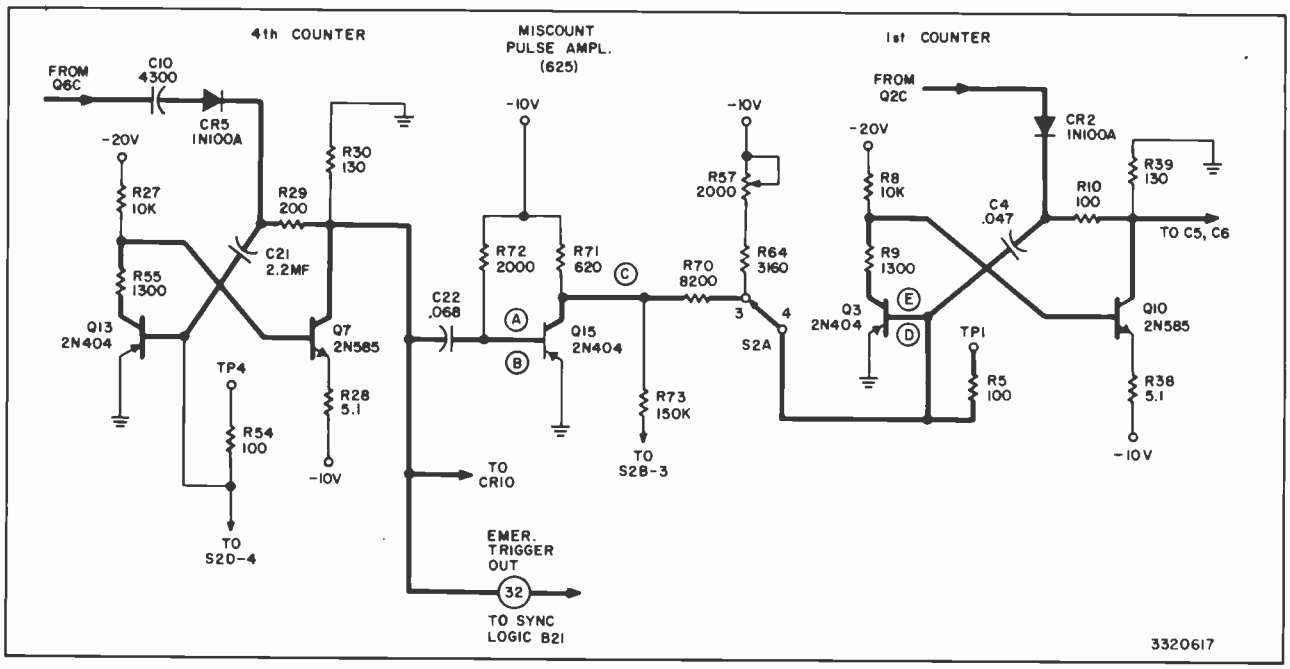
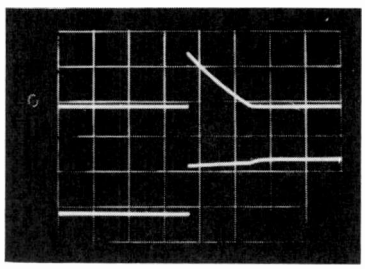
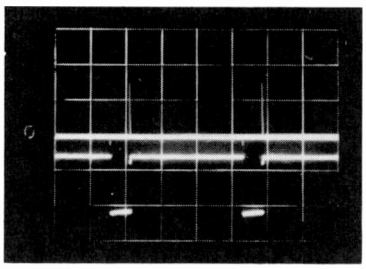


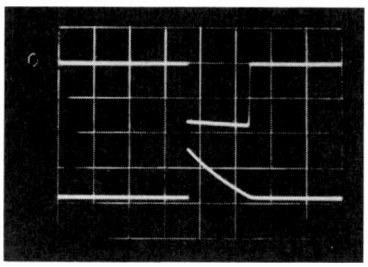
Figure 117—(International) Fourth Counter, Miscount Pulse Amplifier and First Counter Circuits



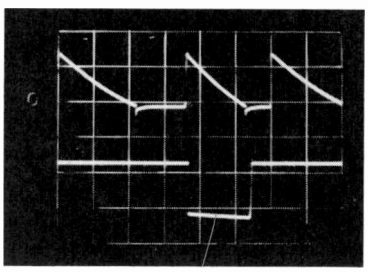
A. Top: Q15 base, 50 μs/cm, 5v/cm
Bottom: Q7 collector, 50 μs/cm, 5v/cm



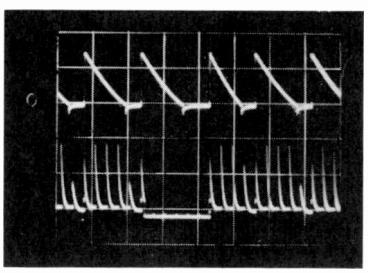
B. Top: Q15 base, 5000 μs/cm, 5v/cm
Bottom: Q7 collector, 5000 μs/cm, 5v/cm



C. Top: Q15 collector, 50 μs/cm, 5v/cm
Bottom: Q15 base, 50 μs/cm, 5v/cm



D. Top: Q3 base, 50 μs/cm, 5v/cm
Bottom: Q15 collector, 50 μs/cm, 5v/cm



E. Top: Q3 base, 100 μs/cm, 2v/cm
Bottom: Q2 collector, 100 μs/cm, 2v/cm

Figure 118—Typical Waveforms, (International) Fourth Counter, Miscount Pulse Amplifier and First Counter Circuits

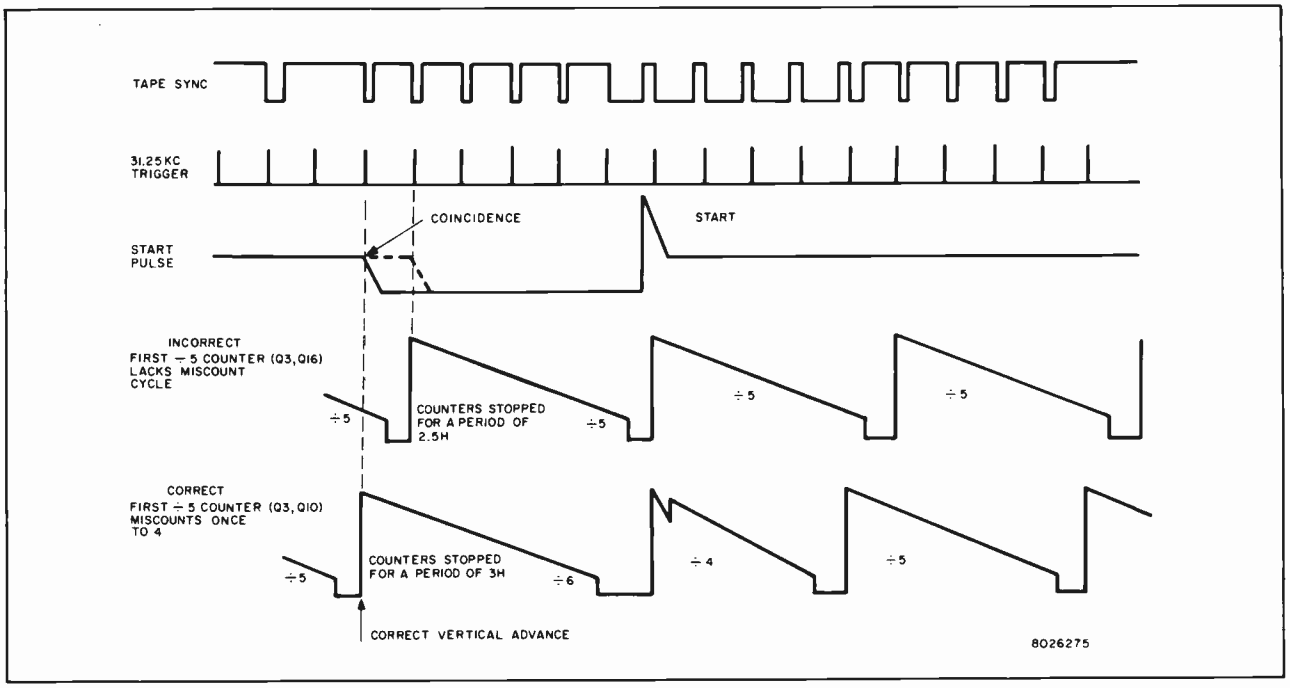


Figure 119—(International) 3H Vertical Advance for 625 Line Standards

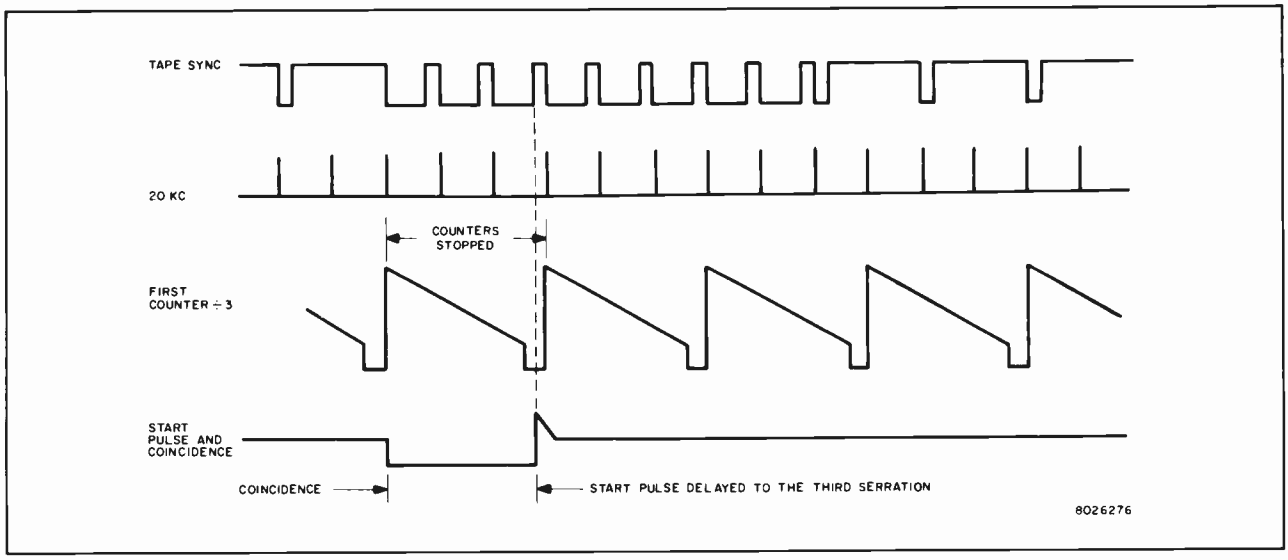


Figure 120—(International) 1.5H Vertical Advance for 405 Line Standards

sixth count, the start pulse arrives, gating on the trigger eliminator which, in turn, allows the 2H pulses to pass and trigger the first counter. The first trigger appears simultaneously with the start pulse and thus the counting cycle starts over again.

1.5H Vertical Advance for 405 Lines

In the 405-line system there are no equalizing pulses, and the vertical interval begins with the leading edge of the first vertical sync pulse. The start pulse is timed to occur with the leading edge of the third vertical sync pulse (see figure 120), therefore the vertical advance pulse is 1.5H wide. Since the first counter is a ÷ 3 multivibrator, the output is a 1.5H signal, and this is exactly the width of the vertical advance pulse. Therefore the count during one field comes out evenly and the last count is 1.5H wide. The next 2H trigger arrives simultaneously with the start pulse to begin a new counting cycle.

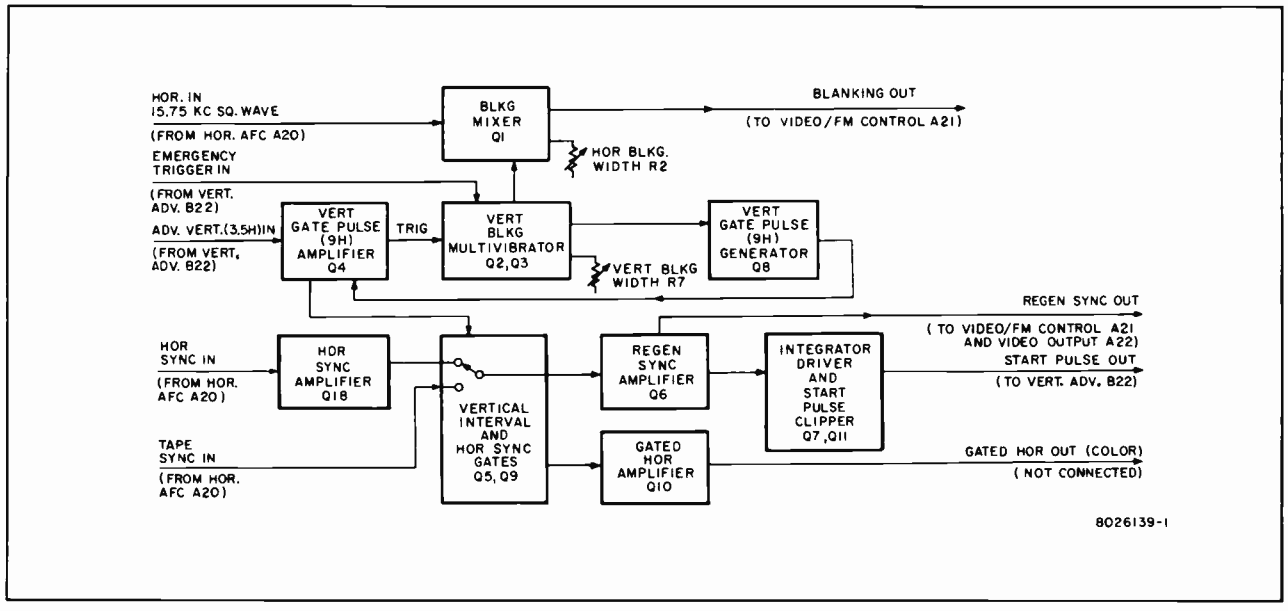


Figure 121—Block Diagram, Sync Logic Module

Sync Logic (Module B21)

General

The Sync Logic module (see figure 121) provides signals for the operation of the Vertical Advance module as well as signals for the Video/FM Control, Video Output and Color modules. When triggered by the leading edge of the 3.5H pulse, which is generated in the Vertical Advance module, the Sync Logic module regenerates the vertical blanking and reinserts the vertical sync interval. The signals supplied by this module include the start pulse for the Vertical Advance module; regenerated sync for the Video Output and the Video/FM Control modules, and also for the latter, regenerated horizontal and vertical blanking.

Vertical Blanking Generator

As shown in figure 122, the vertical blanking multivibrator, Q2, Q3, is a monostable multivibrator with Q2 on, Q3 off in the stable state. The multivibrator changes state by applying a positive trigger pulse to the base of Q2 through the isolation diode, CR3. The normal trigger for the vertical blanking multivibrator is the leading edge of the 3.5H pulse, which is obtained from the collector of Q4, the vertical gate pulse amplifier. Transistor Q2 remains off and Q3 on for the length of time determined by the charging time of capacitor C3 through resistors R7 and R8. The vertical blanking pulse width at the collector of Q3 is set to 21H by adjustment of R7, the VERT BLKG WIDTH control. This control is a screwdriver adjustment on the front panel.

The output of Q3 is coupled to the blanking mixer, Q1 (described later), through the isolation diode, CR2, and to the vertical gate pulse (9H) generator, Q8, through R34 and C16. The 9H generator is a pulse-narrowing* circuit. The 9H pulse output from the collector of Q8 is coupled through the isolation diode, CR9, and combined with the 3.5H pulse input signal. The combined pulses are then passed through R37 and C17 to the horizontal sync gate, Q9, and through R17 and C6 to the base of the vertical gate pulse (9H) amplifier, Q4. An output to the vertical interval gate, Q5, is taken from the emitter of Q4.

Emergency Trigger

As previously mentioned, the positive-going edge of the 3.5H pulse on the collector of Q4 is normally used to trigger Q2, Q3. The emergency trigger pulse is a positive-going signal taken from the ÷ 3 multivibrator in the Vertical Advance module and appears simultaneously with the negative-going (trailing edge) of the 3.5H pulse at the base of Q2. During normal conditions of operation, this pulse has no effect on the vertical blanking multivibrator (Q2, Q3) which has already been triggered by the leading edge of the 3.5H pulse and remains in that state for 21H. However, under unusual operating conditions due to a non-synchronous switch or a bad splice in the tape, the vertical sync period of the tape sync signal may arrive at a much later time. As explained in the description of the Vertical Advance module, the leading edge of the 3.5H pulse is generated exactly 259H after the previous pulse, even

* *See Basic Circuit Descriptions on page 128.*

though the vertical sync has been delayed. The trailing edge of the 3.5H pulse is coincident with the second vertical sync pulse, but since the second vertical sync pulse is delayed, the trailing edge of 3.5H will be delayed. Therefore, the 3.5H pulse will be much longer than 3.5H. This lengthened 3.5H pulse holds the vertical interval gate, Q5, open, (figure 124) allowing tape sync to pass. When the vertical sync does arrive, a start pulse is generated at the leading edge of the second vertical sync pulse, resulting in the termination of the lengthened 3.5H pulse. This trailing edge of the lengthened pulse is negative-going and does not trigger the vertical blanking multivibrator (Q2, Q3) which has returned to its stable state 21H after the leading edge of the 3.5H pulse.

If there were no emergency trigger, the vertical interval gate, Q5, would close, cutting off the remainder of the vertical interval. However, the positive-going emergency trigger coincident with the trailing edge of the lengthened 3.5H pulse does trigger the vertical blanking multivibrator, Q2, Q3 (figure 122) which in turn triggers the vertical gate pulse (9H) generator, Q8. The 9H pulse holds the vertical interval gate open for the remainder of the vertical interval, minimizing the "roll" in the picture.

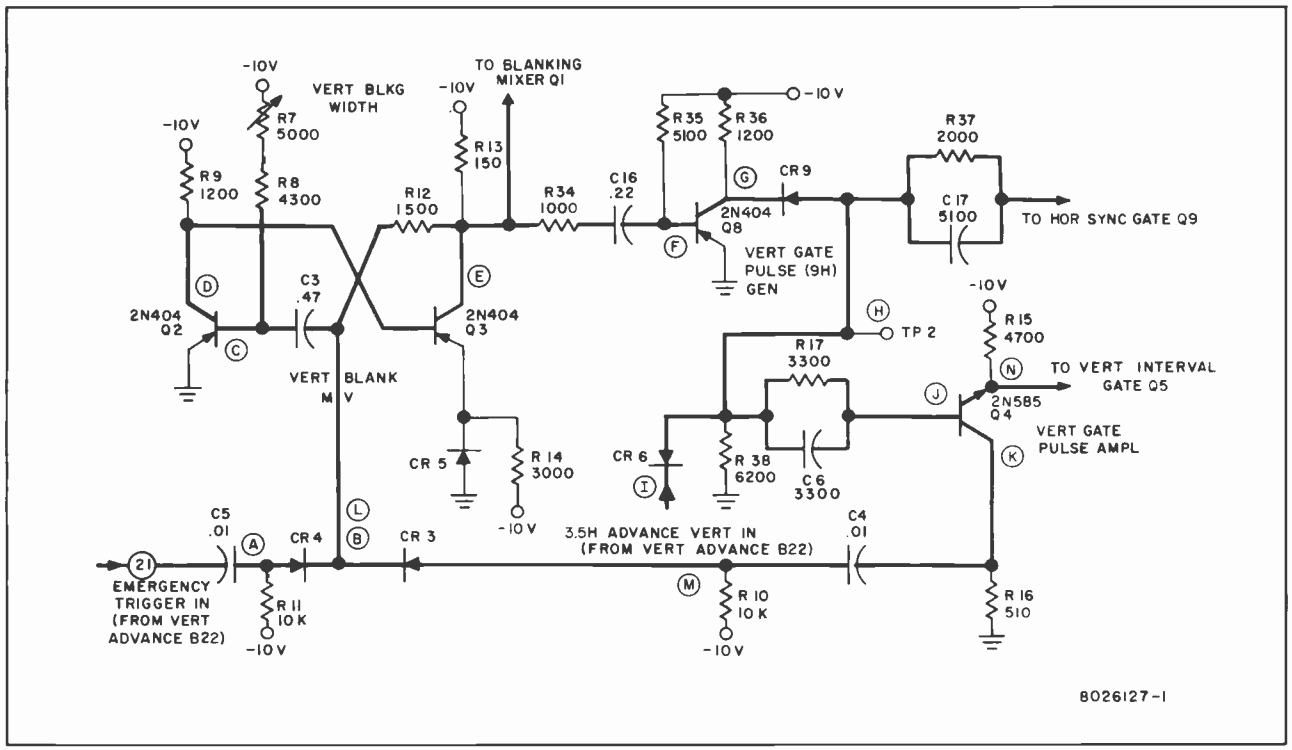
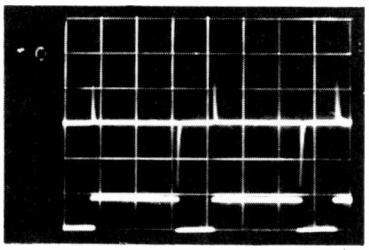
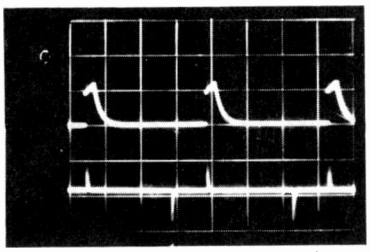


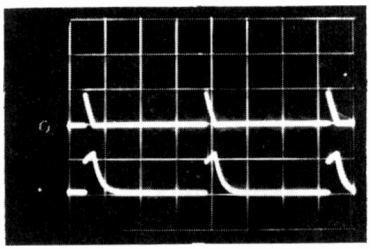
Figure 122—Vertical Blanking Multivibrator, Vertical Gate Pulse Generator and Vertical Gate Pulse Amplifier Circuits



A. Top: R11, C5, CR4, 5 ms/cm, 5v/cm
Bottom: C5 input, 5 ms/cm, 10v/cm

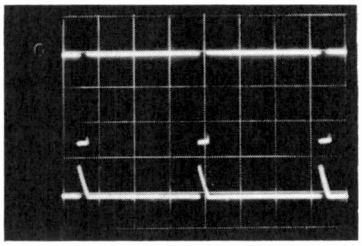


B. Top: CR4, CR3, C3, R12, 5 ms/cm, 5v/cm
Bottom: R11, C5, CR4, 5 ms/cm, 10v/cm

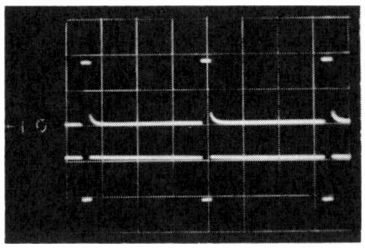


C. Top: Q2 base, 5 ms/cm, 5v/cm
Bottom: CR4, CR3, C3, R12, 5 ms/cm, 5v/cm

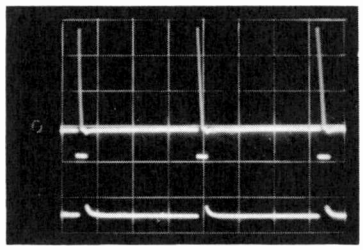
Figure 123—Typical Waveforms, Vertical Blanking Multivibrator, Vertical Gate Pulse Generator and Vertical Gate Pulse Amplifier Circuits



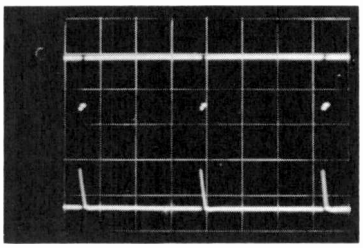
D. Top: Q2 collector, 5 ms/cm, 5v/cm
Bottom: Q2 base, 5 ms/cm, 5v/cm



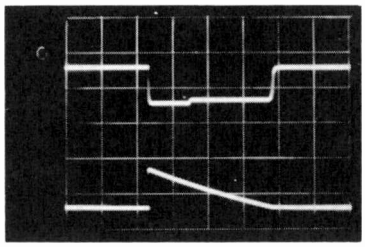
E. Top: Q3 collector, 5 ms/cm, 5v/cm
Bottom: Q3 base, 5 ms/cm, 1v/cm



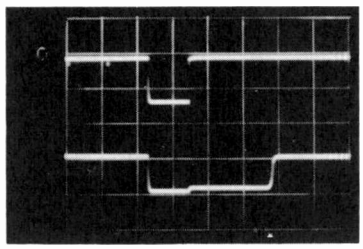
F. Top: Q8 base, 5 ms/cm, 2v/cm
Bottom: Q3 collector, 5 ms/cm, 5v/cm



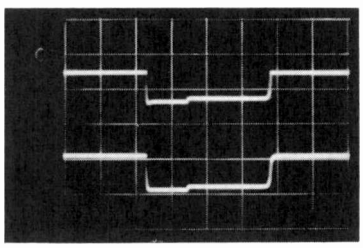
G. Top: Q8 collector, 5 ms/cm, 5v/cm
Bottom: Q8 base, 5 ms/cm, 5v/cm



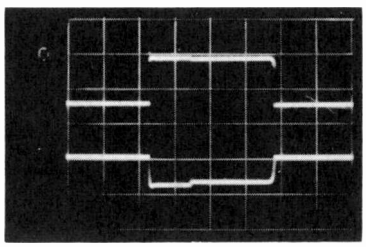
H. Top: TP2, 200 μs/cm, 5v/cm
Bottom: Q8 base, 200 μs/cm, 5v/cm



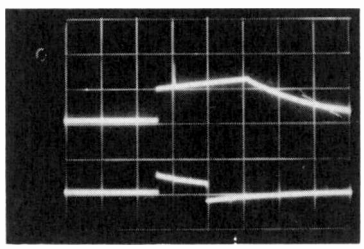
I. Top: CR6 input, 200 μs/cm, 5v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



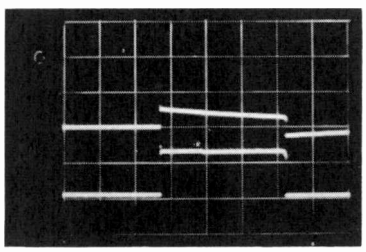
J. Top: Q4 base, 200 μs/cm, 5v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



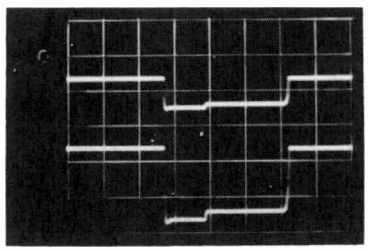
K. Top: Q4 collector, 200 μs/cm, 2v/cm
Bottom: Q4 base, 200 μs/cm, 5v/cm



L. Top: CR3, CR4, C3, R12, 500 μs/cm, 5v/cm
Bottom: CR3, C4, R10, 500 μs/cm, 5v/cm



M. Top: CR3, C4, R10, 200 μs/cm, 5v/cm
Bottom: Q4 collector, 200 μs/cm, 5v/cm



N. Top: Q4 emitter, 200 μs/cm, 5v/cm
Bottom: Q4 base, 200 μs/cm, 5v/cm

Figure 123—(Continued)

Sync Reassembly

In the reassembly of sync, the 3.5H pulse is added to the 9H pulse at both the output of the vertical gate pulse generator, Q8, and at the input to the vertical gate pulse amplifier, Q4 (see figure 122). Since these two signals are in coincidence when they are added or combined, the resultant pulse is still 9H wide under normal operating conditions.

The 3.5H and 9H combined signal appearing at the junction of CR9, C17, and R37 is fed to the horizontal sync gate, Q9, and the similarly combined signal from the emitter of Q4 is fed to Q5, the vertical interval gate (see figure 124).

Regenerated horizontal sync pulses, which originate in the Horizontal AFC (module A20), are fed to the base of Q18, the horizontal sync amplifier, an emitter

follower. The output pulses on the emitter of Q18 are coupled through C9, C10, and R20 to the collector of Q9. Incoming tape sync, which is derived in the sync separator circuit in the Demodulator Output (module A18), is fed via a common terminal on the connector on the Horizontal AFC (module A20) through the input coupling network consisting of C8, C7, and R19 to the collector of Q5.

Normally, transistor Q5 is biased to saturation, shorting out the tape sync pulses which appear at its collector, and transistor Q9 is biased to cut off. In this state, the regenerated horizontal sync pulses appearing at the collector of Q9 are applied to the base of the gated horizontal amplifier, Q10, and to the base of the regenerated sync amplifier, Q6, through isolation diode CR10. The amplified gated horizontal output pulses available at the collector of Q10 are used only when the TR-4 is equipped with the optional color ATC system. During the vertical interval, the 9H pulse applied to the base of Q5 drives it to cut-off, which permits the tape sync pulses to pass through the isolation diode, CR7, to the base of Q6. The 9H pulse applied to the base of Q9 drives it to saturation and

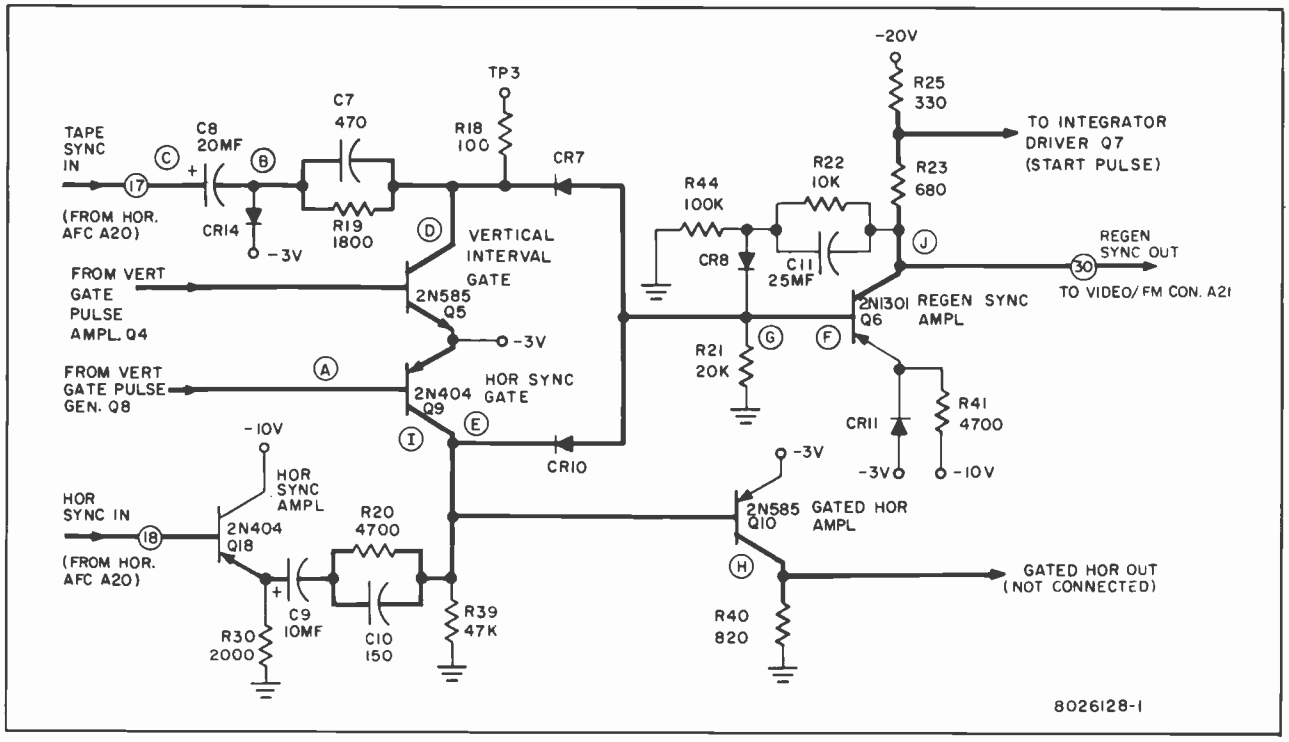
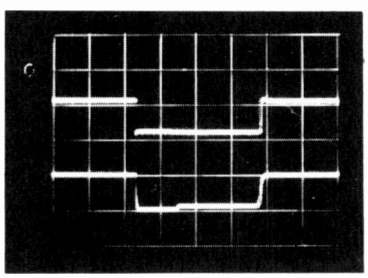
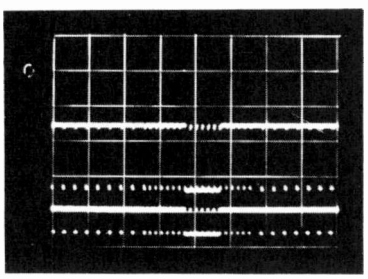


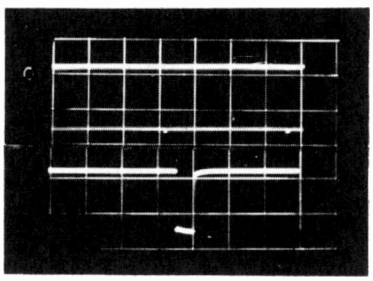
Figure 124—Vertical Interval Gate, Horizontal Sync Gate, Horizontal Sync Amplifier, Regenerated Sync Amplifier and Gated Horizontal Amplifier Circuits



A. Top: Q9 base, 200 μs/cm, 2v/cm
Bottom: TP2, 200 μs/cm, 5v/cm

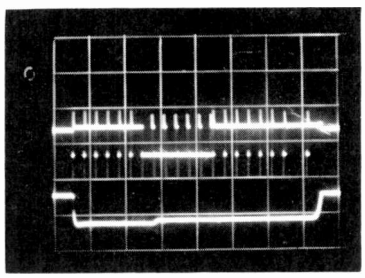


B. Top: C8, CR14, C7, R19, 200 μs/cm, 2v/cm
Bottom: C8 input, 200 μs/cm, 5v/cm

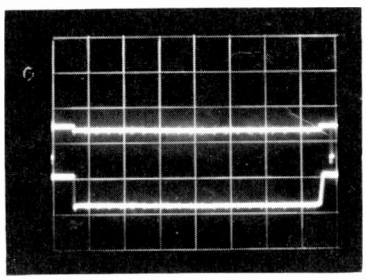


C. Top: C8 input, 5 ms/cm, 2v/cm, V rate
Bottom: C8 input, 10 μs/cm, 2v/cm, H rate

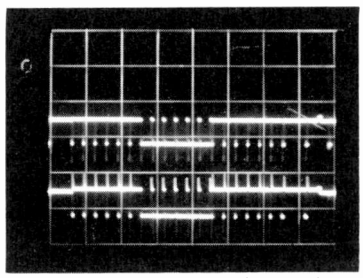
Figure 125—Typical Waveforms, Vertical Interval Gate, Horizontal Sync Gate, Horizontal Sync Amplifier, Regenerated Sync Amplifier and Gated Horizontal Amplifier Circuits



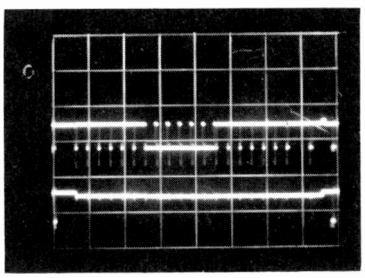
D. Top: Q5 collector, 100 μs/cm, 2v/cm
Bottom: Q5 base, 100 μs/cm, 5v/cm



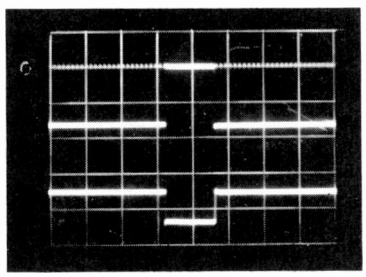
E. Top: Q9 collector, 100 μs/cm, 2v/cm
Bottom: Q9 base, 100 μs/cm, 2v/cm



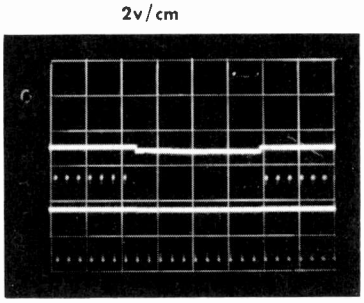
F. Top: Q6 base, 100 μs/cm, 2v/cm
Bottom: Q5 collector, 100 μs/cm, 2v/cm



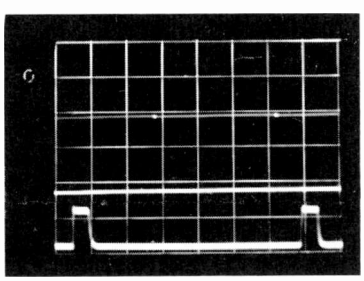
G. Top: Q6 base, 100 μs/cm, 2v/cm
Bottom: Q9 collector, 100 μs/cm, 2v/cm



H. Top: Q10 collector, 500 μs/cm, 2v/cm
Bottom: Q9 base, 500 μs/cm, 2v/cm



I. Top: Q9 collector, 200 μs/cm, 2v/cm
Bottom: C9, C10, R20, 200 μs/cm, 5v/cm



J. Top: Q6 collector, 5 ms/cm, 5v/cm, V rate
Bottom: Q6 collector, 10 μs/cm, 5v/cm, H rate

Figure 125—(Continued)

shorts out the regenerated horizontal pulses. During the vertical sync interval, the pulses at the base of Q6 are tape sync and during the rest of the period, regenerated horizontal sync pulses. These pulses are amplified by transistor Q6 to provide regenerated sync for the Video Output module and for the integrator driver, Q7. Diode CR8 together with R22, R44, and C11 prevents transistor Q6 from being driven into saturation. Diode CR11 provides a bias which insures that Q6 will be cut off in the absence of a pulse input.

Start Pulse

The regenerated sync fed to the base of the integrator driver, Q7, (figure 126) is amplified and passed through the integrating network, R24 and C12. The time constant of this network is such that the output comes mainly from the wide vertical sync pulses. The residual spikes from the horizontal and equalizing pulses are removed by diodes CR12 and CR13. As shown in figure 126, the start pulse clipper, Q11, amplifies the vertical pulse and clips it at a low level. A differentiating network consisting of capacitor C19 and the load in the Vertical Advance module (Q8 and R32) provides a start pulse of short duration which begins to rise after the leading edge of the first sync pulse and returns to zero before the leading edge of the third vertical sync pulse. This pulse selects the one 31.5 kc pulse coincident with the leading edge of the second vertical sync pulse to trigger the counters.

One additional output is provided by this module, and that is blanking. As shown in figure 128, the 15.75 kc square wave input from the Horizontal AFC module is coupled through the isolation diode, CR1, to the blanking mixer, Q1. This circuit is the pulse narrowing* type.

* *See Basic Circuit Descriptions on page 128.*

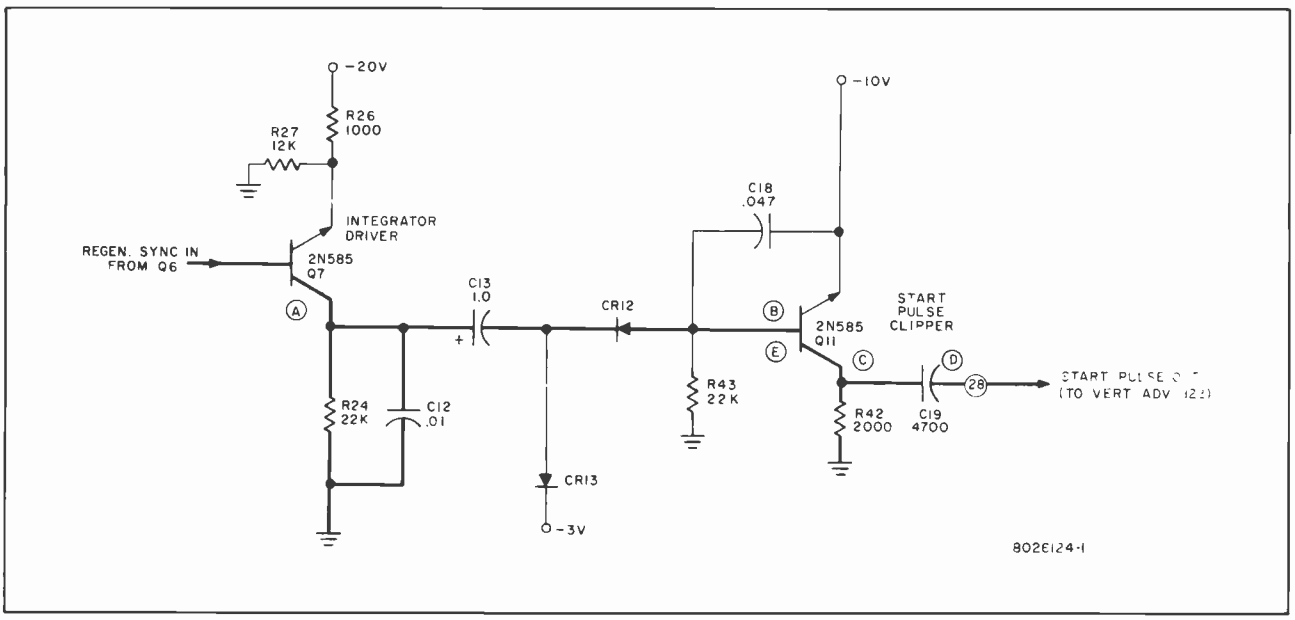
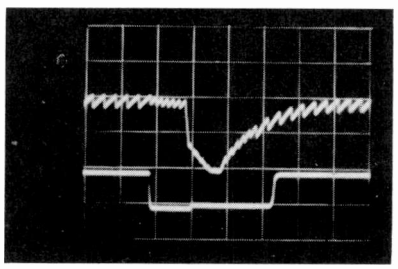
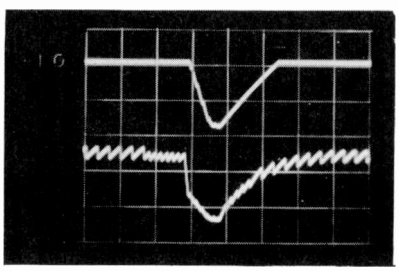


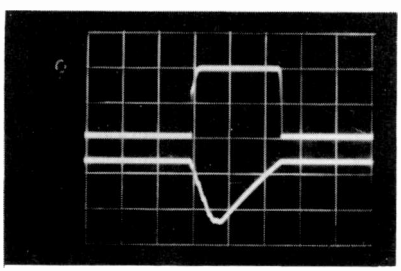
Figure 126—Integrator Driver and Pulse Clipper Circuits



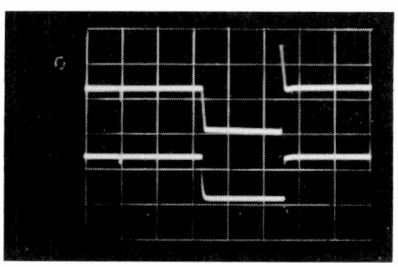
A. Top: Q7 collector, 200 μs/cm, 5v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



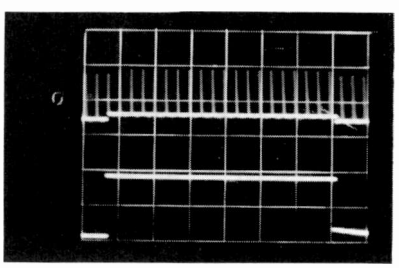
B. Top: Q11 base, 200 μs/cm, 2v/cm
Bottom: Q7 collector, 200 μs/cm, 5v/cm



C. Top: Q11 collector, 200 μs/cm, 5v/cm
Bottom: Q11 base, 200 μs/cm, 2v/cm



D. Top: C19 output, 100 μs/cm, 2v/cm
Bottom: CR6 input, 100 μs/cm, 5v/cm



E. Top: Q11 base, 200 μs/cm, 5v/cm
Bottom: CR2 anode, 200 μs/cm, 5v/cm

Figure 127—Typical Waveforms, Integrator Driver and Start Pulse Clipper Circuits

The time constant of this circuit is determined by C1, R3, and R2, the HOR BLKG WIDTH potentiometer in the base of Q1. The HOR BLKG WIDTH potentiometer, a front panel screwdriver adjustment, is set to provide horizontal blanking pulses of approximately ten microseconds duration. The vertical blanking pulse from the multivibrator, Q2, Q3, is coupled directly to the base of Q1 through the isolation diode, CR2. During the 21H vertical blanking period, Q1 is cut off, thereby generating the vertical blanking pulse and preventing the generation of horizontal blanking pulses. The output at the collector of Q1 is a composite horizontal and vertical blanking signal.

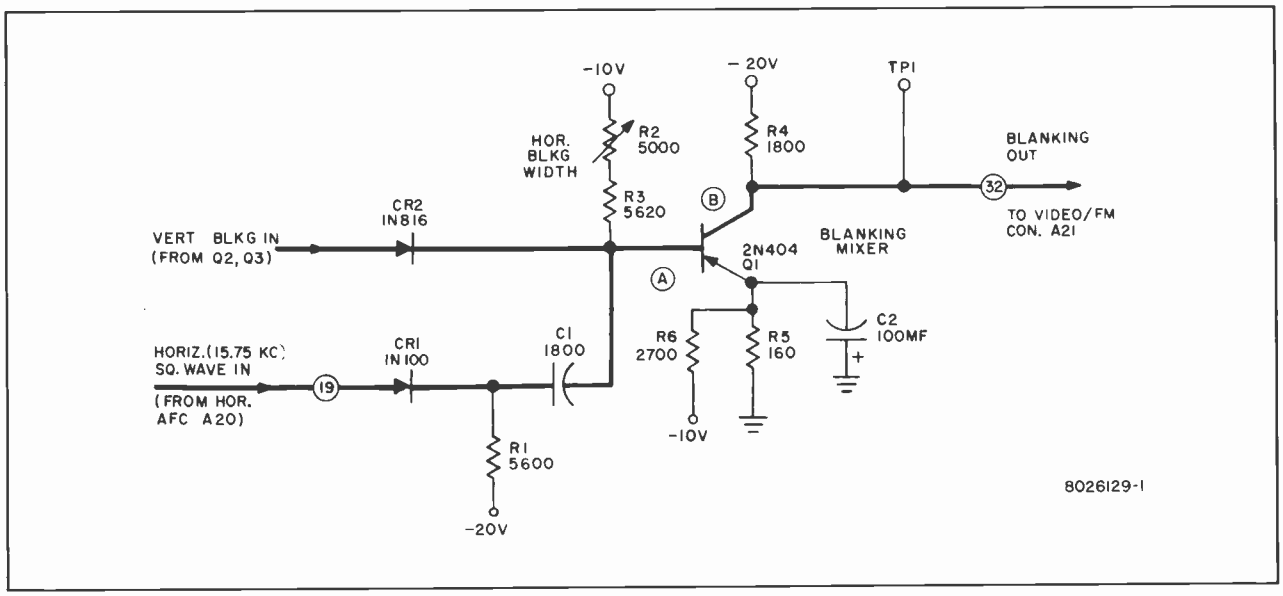
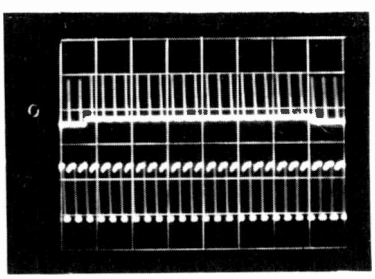
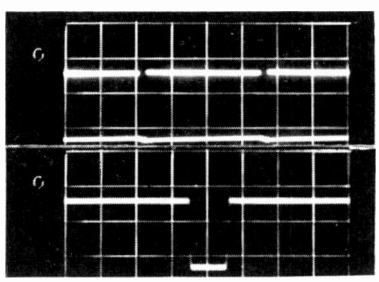


Figure 128—Blanking Mixer Circuit



A. Top: Q1 base, 200 μs/cm, 5v/cm
Bottom: C1, CR1, R1, 200 μs/cm, 5v/cm



B. Top: Q1 collector, 500 μs/cm, 5v/cm, vert. rate
Bottom: Q1 collector, 10 μs/cm, 5v/cm, hor. rate

Figure 129—Typical Waveforms, Blanking Mixer Circuit

Adjustments

To obtain the proper horizontal and vertical blanking width, connect an oscilloscope to one of the three VID test jacks (TP1, TP2, TP3) on the front of the Video Output module and make the following adjustments.

Horizontal Blanking Width

1. Adjust the oscilloscope to display a single horizontal blanking interval.

2. Adjust the HOR BLKG WIDTH control (R2) on the front of the Sync Logic module for a horizontal blanking width of 10.2 microseconds.

Vertical Blanking Width

1. Using delayed sweep and external sync (or 3.5H) as a trigger, adjust the oscilloscope to display the vertical blanking interval.

2. Adjust the VERT BLKG WIDTH control (R7) on the front of the Sync Logic module for a vertical blanking width of 21H (1333.5 microseconds).

International Version

(Refer to the International Sync Logic schematic in the TR-4 Diagram Manual, IB-31807.)

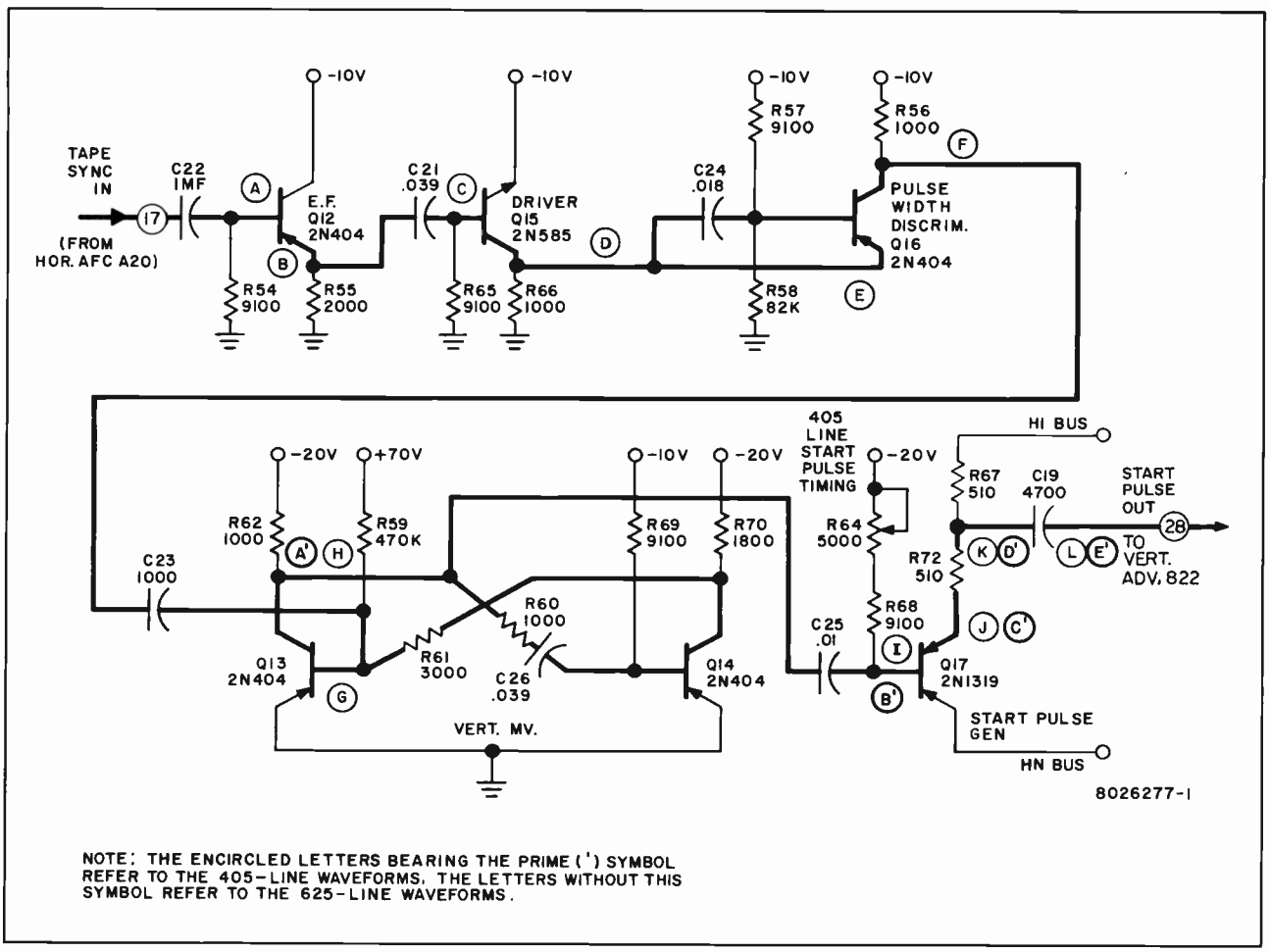
There are two areas in which the Sync Logic module has been modified to conform to international standards. One is the horizontal blanking circuit and the other is the start pulse circuit.

In the horizontal blanking circuit the time constants were made switchable. The 525- and 625-line standards use the same time constants, but separate components were added to accommodate the 405-line standard,

since it requires a different RC time constant. The time constants are electronically switched into the circuit through the HN and HI busses. The desired standard is selected by means of the TV STANDARDS switch, which is located on the International Vertical Advance (module B22). In the start pulse circuit, a major departure from the domestic module was made. This circuit (see the simplified schematic, figure 130) has been completely redesigned for international use and now contains six transistors.

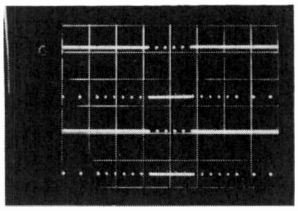
Incoming tape sync from the international Horizontal AFC module is used to generate the start pulse. The input is a 4-volt peak-to-peak negative signal which is applied to the base of Q12, an emitter follower. The latter is used as a unity gain amplifier for isolation purposes. The output appearing on the emitter of Q12 is the same polarity as the input, therefore the signal fed to the base of Q15, the driver, is negative also.

Transistor Q12 is normally cut off and Q15 is normally saturated so that C21 returns to −10 volts through the emitter-base junction of Q15. When there is no signal present on the emitter of Q12, the capacitor is charged to −10 volts through R55. The time constant of C21 and R55 is such that C21 will discharge completely when there is a negative pulse on the emitter of Q12. During the horizontal sync and the equalizing pulse intervals there is ample time between successive pulses for C21 to return to its fully charged state. However, during vertical sync, the time between successive pulses is very short and C21 is not able to recover from its discharged state before the next negative pulse arrives. After the second negative pulse, C21 recharges to a lower level than after the first negative pulse. The recharging of C21 after successive negative pulses continues to become progressively less so that the recovery pulses (serrations) become progressively smaller. This signal appears on the base of Q15, where the dc level now is shifted to −10 volts; otherwise the signal is not altered. The negative pulses arriving on the base of Q15 cuts off this transistor, while simultaneously generating positive pulses on the collector.

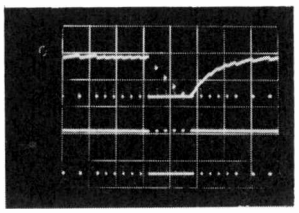


NOTE: THE ENCIRCLED LETTERS BEARING THE PRIME (') SYMBOL REFER TO THE 405-LINE WAVEFORMS. THE LETTERS WITHOUT THIS SYMBOL REFER TO THE 625-LINE WAVEFORMS.

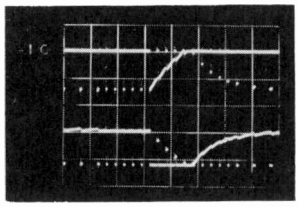
Figure 130—(International) 405 and 625 Line Standards Start Pulse Generator Circuits



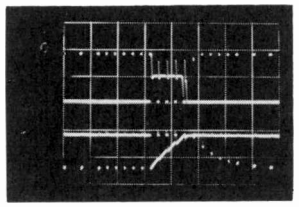
A. Top: Q12 base, 100 μs/cm, 2v/cm
Bottom: tape sync in, 100 μs/cm, 2v/cm



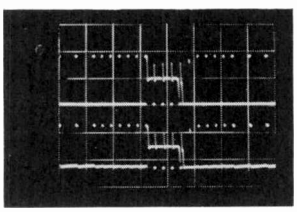
B. Top: Q12 emitter, 100 μs/cm, 2v/cm
Bottom: Q12 base, 100 μs/cm, 2v/cm



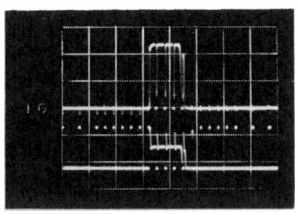
C. Top: Q15 base, 100 μs/cm, 2v/cm
Bottom: Q12 emitter, 100 μs/cm, 2v/cm



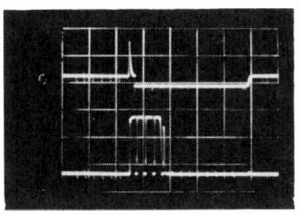
D. Top: Q15 collector/Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q15 base, 100 μs/cm, 2v/cm



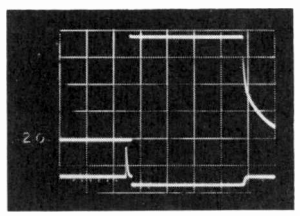
E. Top: Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q16 base, 100 μs/cm, 5v/cm



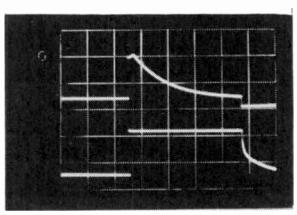
F. Top: Q16 collector, 100 μs/cm, 2v/cm
Bottom: Q16 emitter, 100 μs/cm, 5v/cm



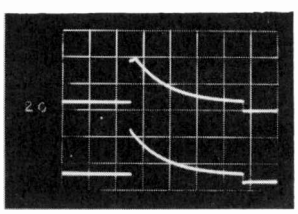
G. Top: Q13 base, 100 μs/cm, 2v/cm
Bottom: Q16 collector, 100 μs/cm, 2v/cm



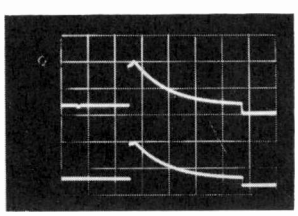
H. Top: Q13 collector, 100 μs/cm, 5v/cm
Bottom: Q13 base, 100 μs/cm, 2v/cm



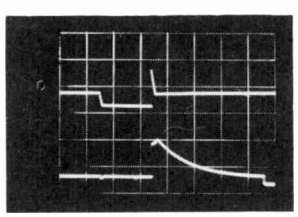
I. Top: Q17 base, 100 μs/cm, 10v/cm
Bottom: Q13 collector, 100 μs/cm, 10v/cm



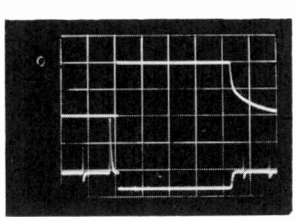
J. Top: Q17 emitter, 100 μs/cm, 10v/cm
Bottom: Q17 base, 100μs/cm, 10v/cm



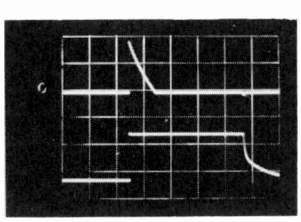
K. Top: R67, R72, 100 μs/cm, 5v/cm
Bottom: Q17 emitter, 100 μs/cm, 10v/cm



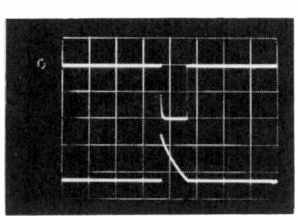
L. Top: Start pulse out, 100 μs/cm, 5v/cm
Bottom: R67, R72, 100 μs/cm, 5v/cm



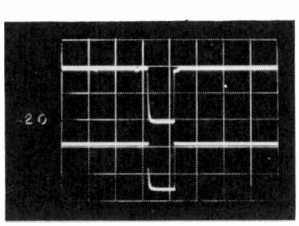
A.' Top: Q13 collector, 100 μs/cm, 10v/cm
Bottom: Q13 base, 100 μs/cm, 1v/cm



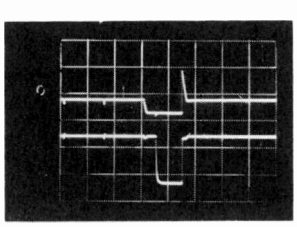
B.' Top: Q17 base, 100 μs/cm, 10v/cm
Bottom: Q13 collector, 100 μs/cm, 10v/cm



C.' Top: Q17 emitter, 100 μs/cm, 10v/cm
Bottom: Q17 Base, 100 μs/cm, 10v/cm



D.' Top: R67, R72, 100 μs/cm, 5v/cm
Bottom: Q17 emitter, 100 μs/cm, 10v/cm



E.' Top: Start pulse out, 100 μs/cm, 5v/cm
Bottom: R67, R72, 100 μs/cm, 5v/cm

Figure 131—Typical Waveforms, (International 405 and 625 Line Standards Start Pulse Generator Circuits

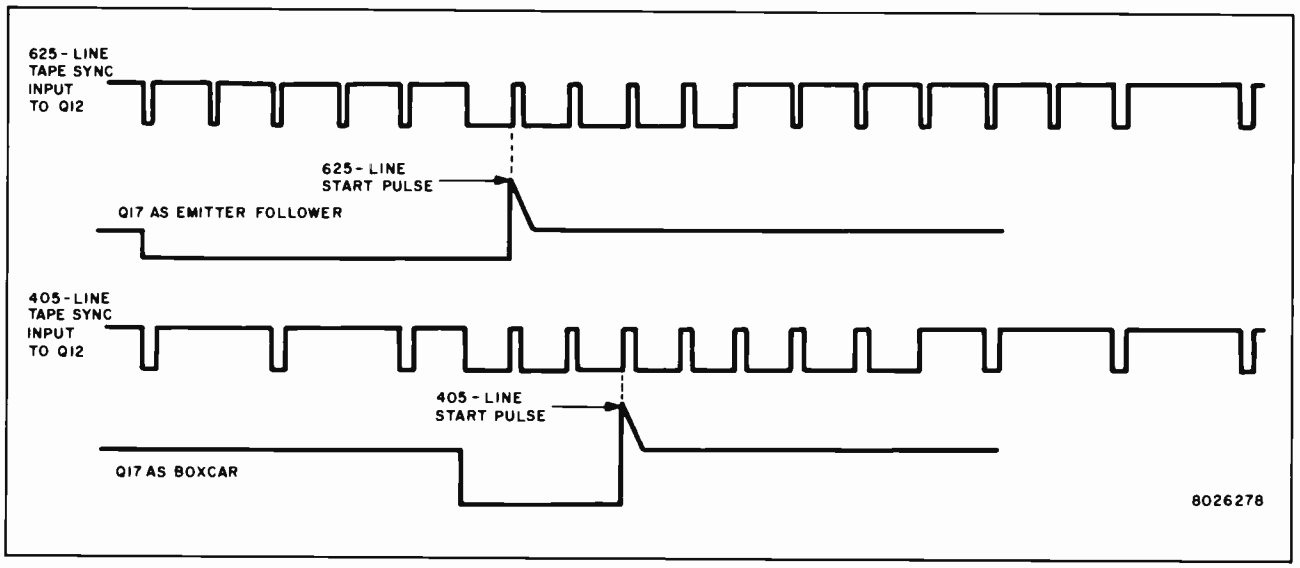


Figure 132—(International) Timing of 405 and 625 Line Start Pulses

The positive sync output from the collector of Q15 goes simultaneously to the emitter and the base of Q16, the pulse width discriminator. The input to the emitter is direct coupled; the input to the base is passed through the differentiating network consisting of C24 and R57.

The RC time constant of the differentiator in the base of Q16 is such that the duration of the capacitor discharge is longer during the horizontal and the equalizing pulse intervals than the duration of these pulses on the emitter. Therefore the pulses on the base keep Q16 cut off. Compared to the duration of the vertical sync pulses, however, the time constant of the differentiator is short. Therefore, when vertical sync arrives, the capacitor discharges before the end of the pulse, but the emitter still sees the trailing edge of the positive pulse. Thus the emitter is more positive than the base during the remainder of the pulse and the transistor conducts. Simultaneously on the collector of Q16 several positive pulses are generated to correspond to the first few vertical sync pulses.

This positive vertical output signal is passed through a differentiator, consisting of C23, R61, and R70 and then applied to the base of Q13. Transistor Q13 in conjunction with Q14 forms the vertical multivibrator which is the monostable type. The RC time constant of the differentiator permits only the differentiated trailing (negative) edge of the first pulse to trigger the vertical multivibrator. The vertical multivibrator generates a positive output pulse which is fed through a differentiator comprised of C25, R68 and variable resistor R64 and then applied to the base of Q17, the start pulse generator.

A bilateral transistor, which serves as either a pulse narrowing* amplifier (boxcar) or an emitter follower, is used for the start pulse generator. The configuration it assumes depends upon the potential applied to the HI and HN busses and this, in turn, is determined by the standards selector switch. On 525- and 625-line standards, the HN bus is at −20 volts and the HI bus is at ground potential and Q17 is an emitter follower. On 405-line standards, the potentials on the HI and HN busses are reversed and Q17 is a pulse narrowing* amplifier or boxcar.

Variable resistor R64 in the differentiator in the base of Q17 is used to fix the timing of the trailing edge of the 405-line start pulse. Since there are no equalizing pulses in the 405-line signal, this resistor is adjusted to set the RC time constant so that the positive going trailing edge of the 405-line start pulse occurs during the third vertical serration interval. Resistor R64 has no influence on the RC time constant in producing the 525/625 line start pulse, since on this line standard it is the positive-going leading edge that is used as the trigger. The timing of the start pulses is illustrated in figure 132.

The output of the start pulse generator is differentiated, and the resulting positive pulse is fed to the base of Q8, the start pulse amplifier in the international Vertical Advance (module B22). Here, on the base of Q8, the start pulse generated in Q17 and the output of the vertical advance pulse amplifier, Q9, (on the Vertical Advance module) are combined as the input to start pulse amplifier.

* *See Basic Circuit Descriptions on page 128.*

Video/FM Control (Module A21)

General

NOTE: The FM Equalizer circuitry was covered previously. This part of the discussion will be confined to the video, blanking adder, and clamp circuits.

The video control section (figure 133) provides a stabilized video signal which is then amplified to a level sufficient to insure stable clamping. The existing blanking along with sync and any transients are eliminated, and new blanking is added to the clamped video output. A pedestal control is provided that enables local or remote ajustment of the pedestal level in the outgoing video.

Circuit

Video Amplifiers

As shown in figure 134, video at 1 volt peak-to-peak from the Demodulator Output (module A18) is fed across an attenuator network consisting of R1, R2, and R3 through coupling capacitor C1 to the base of Q1, the video input amplifier.

Both high and low frequency compensation are employed in this stage. Variable peaking coil L1, in shunt with the collector circuit of Q1, preserves the high frequency response, and C2 and C3 maintain the response at the low end of the band.

The gain of this stage is determined by the setting of potentiometer R17 in the emitter of Q1. This is an internal control designated LEVEL which, when adjusted, increases or decreases the amount of degeneration introduced into the emitter of Q1. The LEVEL control is set at the factory for optimum gain, therefore it should not be readjusted in the course of normal operation or routine maintenance.

The amplified output on the collector of Q1 is direct coupled to the base of video amplifier Q2, an emitter follower. From the emitter of Q2, the signal is fed across R11 and through the coupling network consisting of C5, C6, and C37 to the base of Q3. The latter in conjunction with Q4 forms a feedback amplifier stage.

This stage is an arrangement of a common emitter amplifier (Q3) which inverts and amplifies the input signal, and an emitter follower which presents a low impedance to the output of the clamp circuit (to be discussed later). Bias for the base of Q3 is developed across a voltage divider consisting of R12, R15, R16, and Q4 returned to −20 volts. The output signal on the emitter of Q4 is approximately 5 volts peak-to-peak, and this is coupled through C9 to the base video amplifier, Q5, an emitter follower, where a dc reference is added to the signal which clamps the back porch at −12 volts.

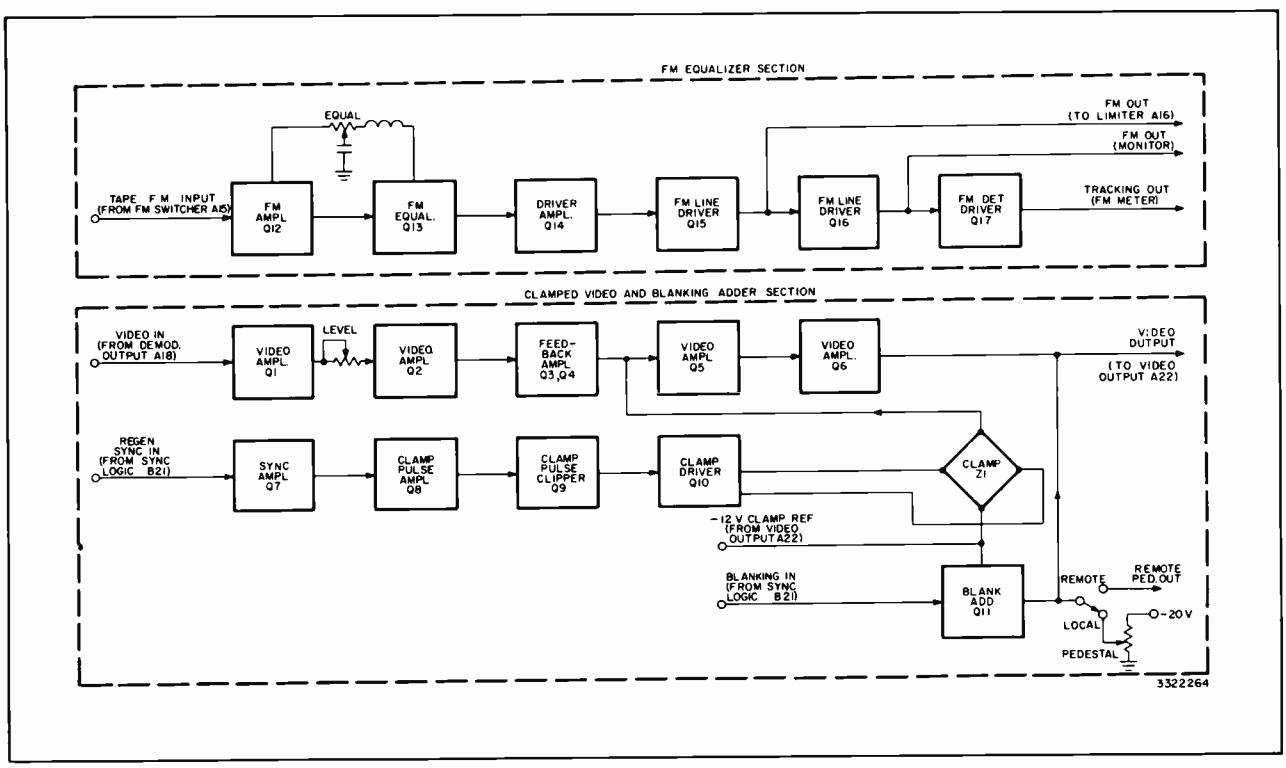


Figure 133—Block Diagram, Video/FM Control Module

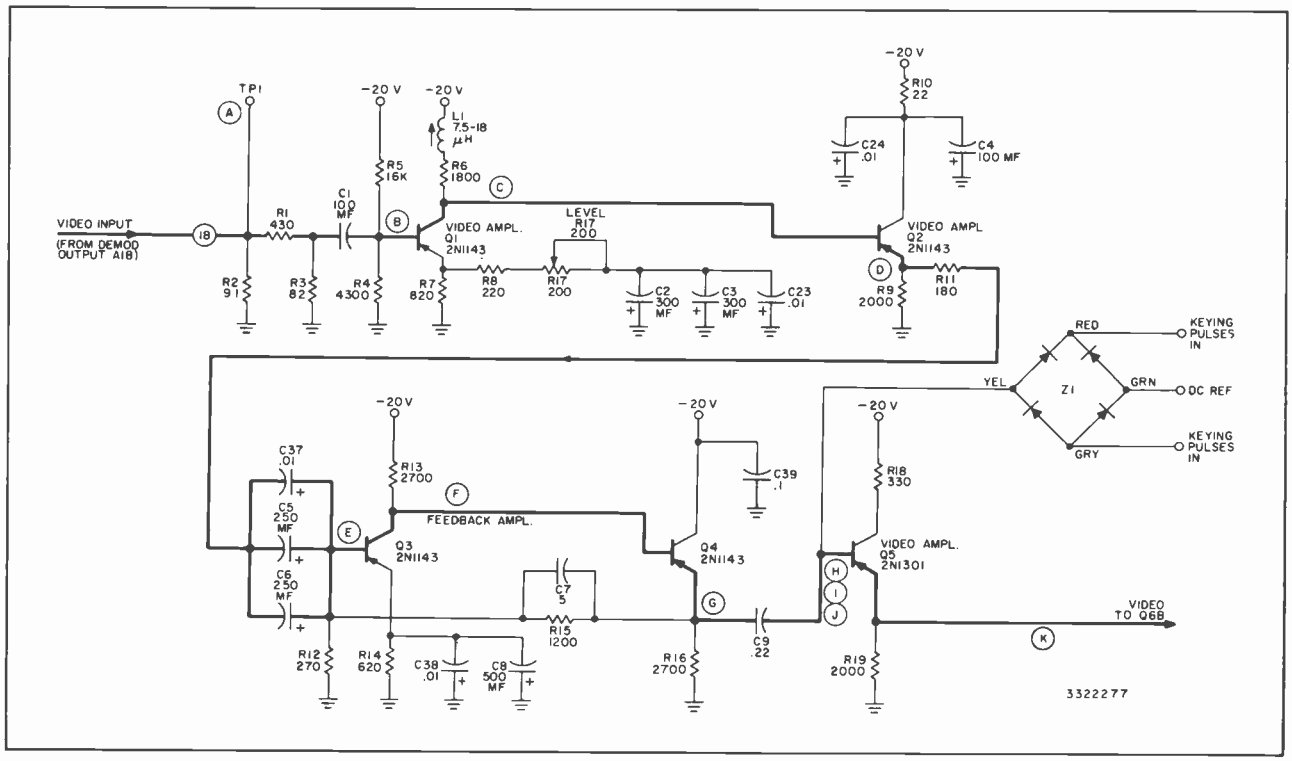
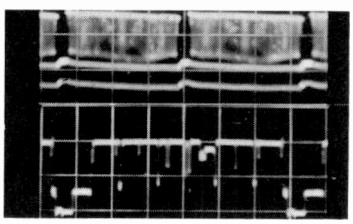
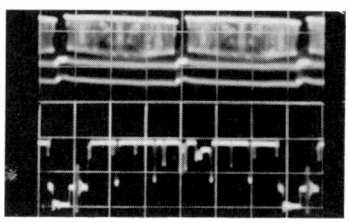


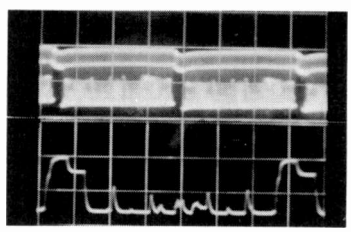
Figure 134—Video Amplifiers, Level Control, Feedback Amplifier and Clamped Video Circuits



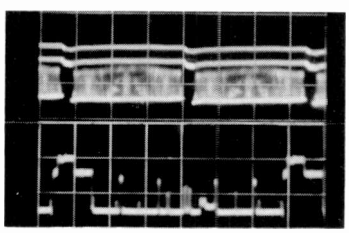
A. TP1
Top: 5 ms/cm, .5v/cm
Bottom: 10 µs/cm, .5v/cm



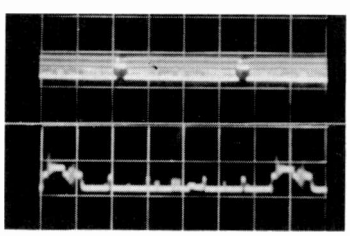
B. Q1 base
Top: 5 ms/cm, .1v/cm
Bottom: 10 µs/cm, .1v/cm



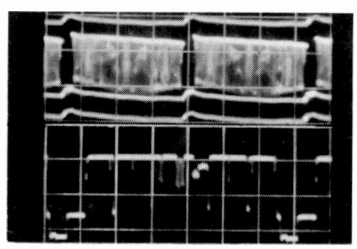
C. Q1 collector
Top: 5 ms/cm, .5v/cm
Bottom: 10 µs/cm, .5v/cm



D. Q2 emitter
Top: 5 ms/cm, .5v/cm
Bottom: 10 µs/cm, .5v/cm

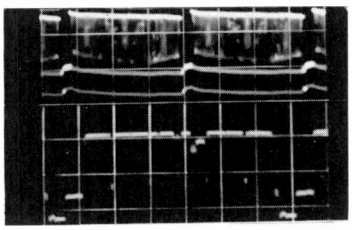


E. Q3 base
Top: 5 ms/cm, .05v/cm
Bottom: 10 µs/cm, .05v/cm

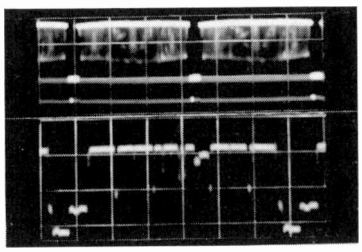


F. Q3 collector
Top: 5 ms/cm, 2v/cm
Bottom: 10 µs/cm, 2v/cm

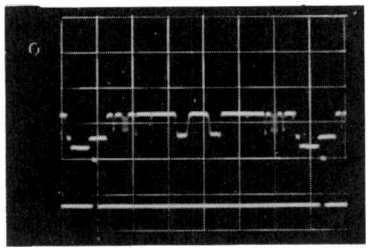
Figure 135—Typical Waveforms, Video Amplifiers, Level Control, Feedback Amplifier and Clamped Video Circuits



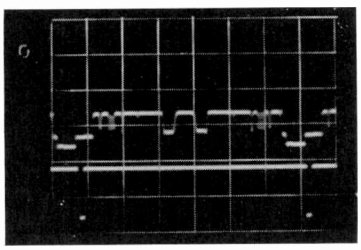
G. Q4 emitter
Top: 5 ms/cm, 2v/cm
Bottom: 10 μs/cm, 2v/cm



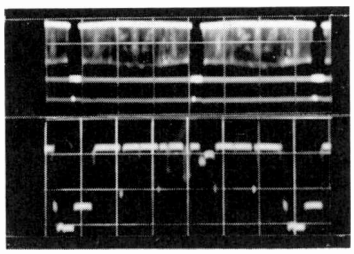
H. Q5 base
Top: 5 ms/cm, 2v/cm
Bottom: 10 μs/cm, 2v cm



I. Top: Q5 base, 10 μs/cm, 5v/cm
Bottom: Z1 gray, 10 μs/cm, 5v/cm



J. Top: Q5 base, 10 μs/cm, 5v/cm
Bottom: Z1 red, 10 μs/cm, 5v/cm



K. Q5 emitter
Top: 5 ms/cm, 2v/cm
Bottom: 10 μs/cm, 2v/cm

Figure 135—(Continued)

Clamp Quad

The clamp pulses are interposed in the signal by means of the clamp quad, Z1, (figure 136) which is keyed on during the back porch interval. Keying pulses for the clamp quad, Z1 are derived from regenerated sync that originates in the Sync Logic (module B21).

The incoming sync pulses are applied to the base of the sync amplifier, Q7, an emitter follower. The high input impedance provided by the emitter follower configuration isolates the clamp circuitry following Q7 from the preceding sync amplifier (Q6) in the Sync Logic module. The output on the emitter of Q7 is fed through a differentiator consisting of C12 and R26 to the base of Q8, the clamp pulse amplifier. Transistor Q8 is a pulse narrowing or "boxcar"* circuit, which is driven to cutoff by the negative-going trailing edge of each pulse. This transistor remains cut off for approximately 10 microseconds, this period being determined by the RC time constant of R26 and C12. The positive-going output pulses on the collector of Q8 are direct coupled to the base of Q9, the clamp pulse clipper.

The clipped and inverted output on the collector of Q9 is dc coupled across R31 to the base of Q10, the clamp pulse driver. The two out-of-phase pulses on the collector and emitter of Q10 are coupled through C16 and C17, respectively across the clamp quad, Z1. The signal applied to the junction of the anodes of the diodes is positive and the signal applied to the junction of the cathodes is negative, therefore the quad conducts. Since these pulses are timed to key the quad on during the back porch interval, the −12 volts reference potential being applied to the bottom of the quad is fed through the quad to the base of Q5 during this period. The clamp keying pulses are cancelled in Z1 during the clamping interval. The output on the emitter of Q5 is direct coupled to the base of the final video amplifier, Q6, an emitter follower (figure 138). The video output of this stage, to which regenerated blanking has been added, is fed to the Video Output (module A22).

Blanking And Video Output

As shown in figure 138, the output on the emitter of Q6 passes through the output coupling network consisting of R22, R23, and C11. On the output side of this network new blanking, which originates in the Sync Logic (module B21), is interposed in the output video. The blanking input is coupled through C21 and R39 to the base of the blanking adder, Q11, an emitter follower.

The blanking adder circuit operates in conjunction with the black clipper, Q10, in the Video Output (module A22). This is the video input stage of the latter to which the video output of this module is fed. The pedestal potentiometer, R43, in the emitter circuit

* *See Basic Circuit Descriptions on page 128.*

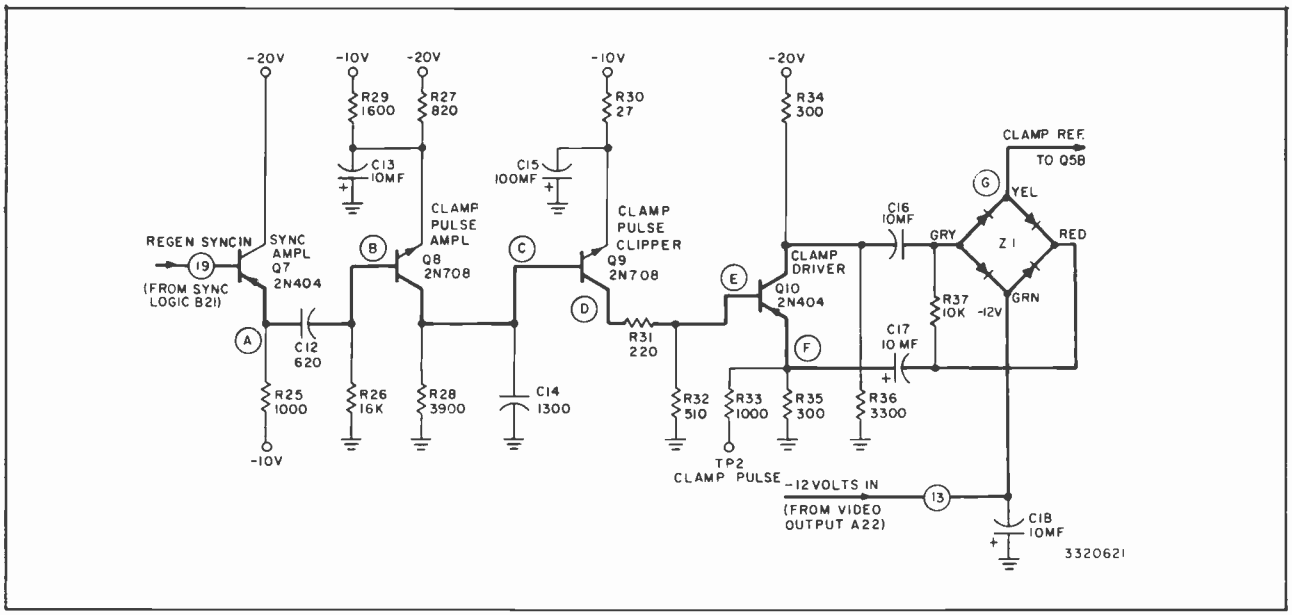
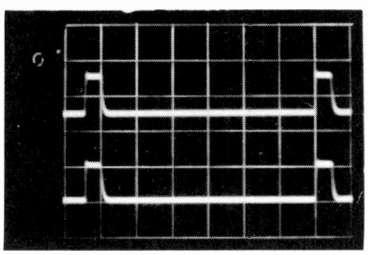
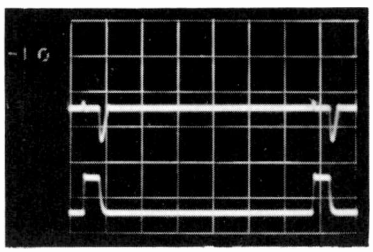


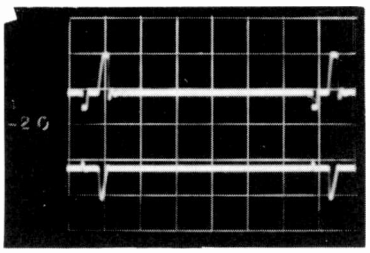
Figure 136—Sync and Clamp Pulse Amplifiers, Clamp Pulse Clipper, Clamp Driver and Clamp Quad Circuits



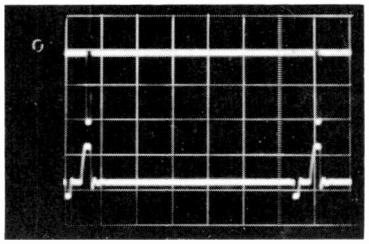
A. Top: Q7 emitter, 10 μs/cm, 10v/cm
Bottom: Q7 base, 10 μs/cm, 10v/cm



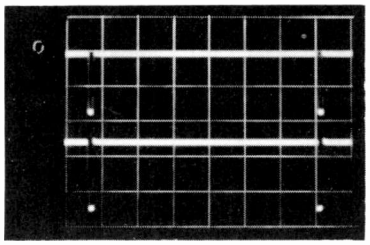
B. Top: Q8 base, 10 μs/cm, 5v/cm
Bottom: Q7 emitter, 10 μs/cm, 10v/cm



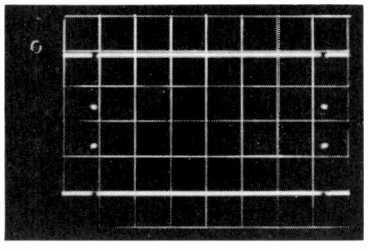
C. Top: Q8 collector, 10 μs/cm, 5v/cm
Bottom: Q8 base, 10 μs/cm, 5v/cm



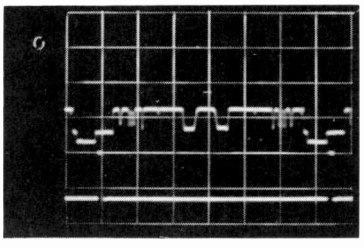
D. Top: Q9 collector, 10 μs/cm, 5v/cm
Bottom: Q9 base, 10 μs/cm, 5v/cm



E. Top: Q10 base, 10 μs/cm, 5v/cm
Bottom: Q9 collector, 10 μs/cm, 5v/cm



F. Top: Q10 emitter, 10 μs/cm, 5v/cm
Bottom: Q10 collector, 10 μs/cm, 5v/cm



G. Top: Z1 yellow, 10 μs/cm, 5v/cm
Bottom: Z1 gray, 10 μs/cm, 5v/cm

Figure 137—Typical Waveforms, Sync and Clamp Pulse Amplifiers, Clamp Pulse Clipper, Clamp Driver and Clamp Quad Circuits

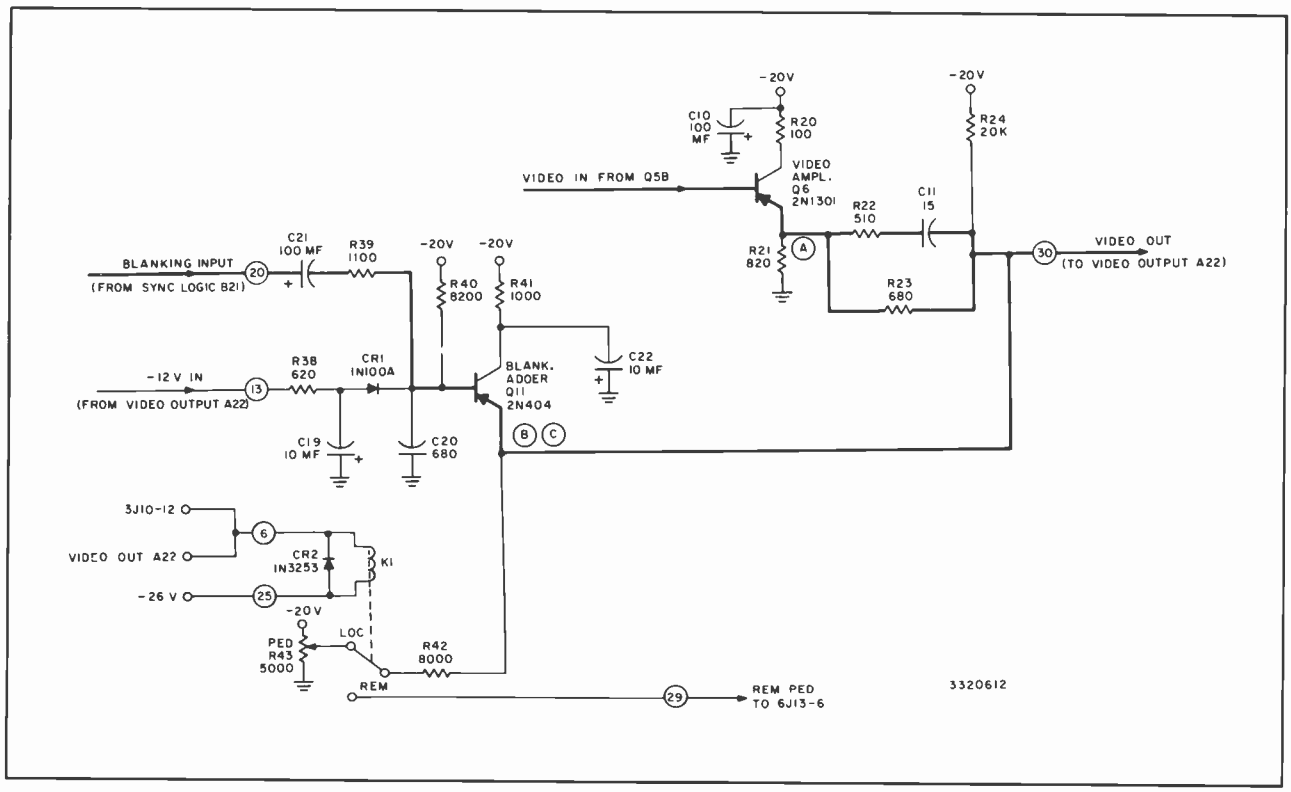
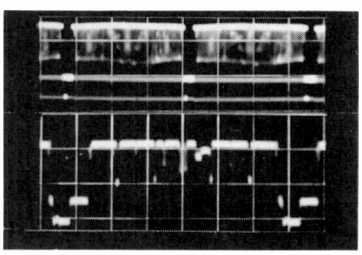
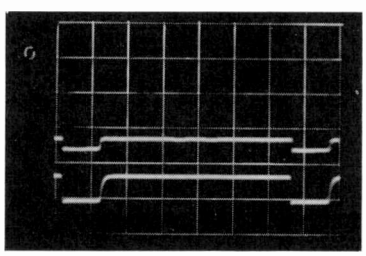


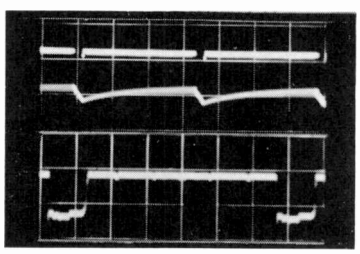
Figure 138—Video Output Amplifier, Blanking Adder and Local/Remote Pedestal Circuits



A. Q6 emitter
Top: 5 ms/cm, 2v/cm
Bottom: 10 μs/cm, 2v/cm



B. Top: Q11 emitter, 10 μs/cm, 5v/cm
Bottom: Q11 base, 10 μs/cm, 5v/cm



C. Q11 emitter
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, 1/vcm

Figure 139—Typical Waveforms, Video Output Amplifier, Blanking Adder and Local/Remote Pedestal Circuits

of Q11 establishes the dc level at which the sync is clipped by the black clipper, Q10. Adjusting R43 makes the signal go either more positive or more negative with respect to the −12 volt clamping reference. The pedestal level is set by means of the PED control on the front panel. When blanking arrives, Q11 conducts allowing clipped sync and blanking to flow through and be eliminated. At the same time, the black clipper, Q10, is cut off; therefore, no signal passes through it. However, when the actual video signal (positive with respect to the clamping reference) arrives after blanking, the states of Q11 and Q10 are reversed. Transistor Q11 is cut off, acting as an open circuit, while Q10 conducts and allows the signal to flow through it. No usable signal appears on the emitters of Q11 and Q10 because Q10 is a common base amplifier whose signal input impedance is so low as to be almost a short circuit. Diode CR1 in the base of Q11 sets the negative peak of the blanking signal at −12 volts. The −12 volt clamping reference is obtained across a voltage divider consisting of R36, R37 in the base of Q10.

Adjustments

To check the frequency response of the video section, follow the procedure outlined below:

Recommended Test Equipment and Accessories

Tektronix Type 535 oscilloscope (or equivalent) with low capacity probe.

Video sweep generator with flat response 0 to 10 mc.

Module extender

10 k resistor

1. Remove power from the TR-4 by placing the equipment power circuit breaker, 1CB1, in the OFF position.

2. Remove the Video/FM Control module from the TR-4. Disable the clamp, Z1, by disconnecting the wire at the yellow dot on Z1 from the terminal on the board. Connect a 10K resistor between this terminal and the terminal with the green dot connection from Z1. Mount the module in an extender and insert it in the TR-4.

3. Withdraw the Video Output (module A22) from the TR-4 and place the SYNC switch, S1, in the OFF position; then replace the module.

4. Place the equipment power circuit breaker, 1CB1, in the ON position.

5. Connect the sweep output of the video sweep generator, with the sweep rate set at 0 to 8 mc, to the junction of R1 and R2. Connect the oscilloscope probe to this junction and adjust the output of the generator to obtain a .5v peak-to-peak signal on the CRO.

6. Turn the PED (pedestal) control, R43, fully cw. Connect the oscilloscope probe to the VID 3 test point on the Video Output module. Terminate the oscilloscope in 75 ohms. Adjust coil L1 for flat response to 8 mc, i.e., the video input and output should be matched.

7. Place 1CB1 in the OFF position. Remove the 10K resistor and reconnect quad Z1, and replace the module in the tape recorder. Return the SYNC switch in the Video Output module to the ON position.

Video Output (Module A22)

General

The Video Output module (figure 140) combines the video and the regenerated sync to form the composite video output of the TR-4. The output signal is fed to three external lines and to one internal line, all of which are sending-end terminated. The internal line furnishes video to the CRO monitor and to the video detector circuit. The rectified output of the video detector which represents the level of the outgoing

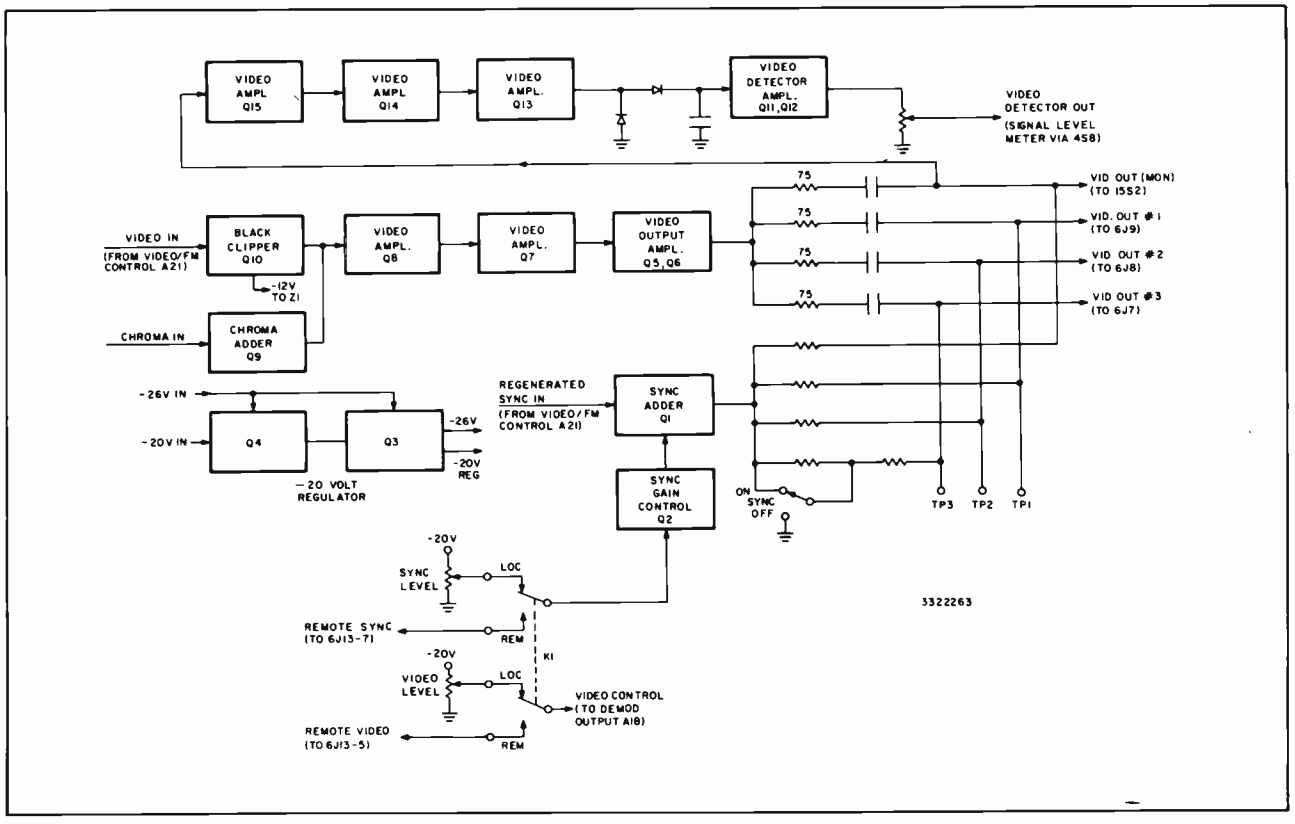


Figure 140—Block Diagram, Video Output Module

composite video, is available for evaluation on the signal level meter (4M1). A switching circuit that enables either local or remote control of both the video and sync levels is included on this module.

Circuit

Video Amplifiers

As shown in figure 141, the processed monochrome video signal from the Video/FM Control (module A21) is fed to the emitter of the black clipper, Q10, a common base amplifier. The black clipper conducts when the emitter voltage is more positive than the −12 volts applied to the base. The −12 volts on the base is developed across the voltage divider consisting of R36, R37 returned to −20 volts. This same −12 volts is also supplied to the clamp quad, Z1, and to the blanking adder, Q11, both of which are in the Video/FM Control Module Transistor Q10 in conjunction with Q11 clips and eliminates all signals more negative than the clamping reference level. Thus sync and any unwanted signals are removed during the blanking interval. The output on the collector of Q10 is dc coupled through a 5.6 volt Zener diode, CR4 to the base of Q8, the first of two cascaded emitter follower video amplifiers. Use of a Zener diode for dc coupling between these two stages eliminates the possibility of adding more tilt to the video output signal.

In a color system, Q9 is the burst and chroma adder. The output of this stage is also fed to Q8 by virtue of the direct coupling between the collector of Q9 and the base of the latter. In addition, Q9 forms part of the biasing network for Q8. The feedback loop between the emitter of Q8 and the base of Q9 serves as a dc stabilizer for the former.

From the emitter of Q8, the signal is dc coupled across R29 to the base of Q7, the second emitter follower video amplifier. The output on the emitter of Q7 is dc coupled across R27 to the base of Q6.

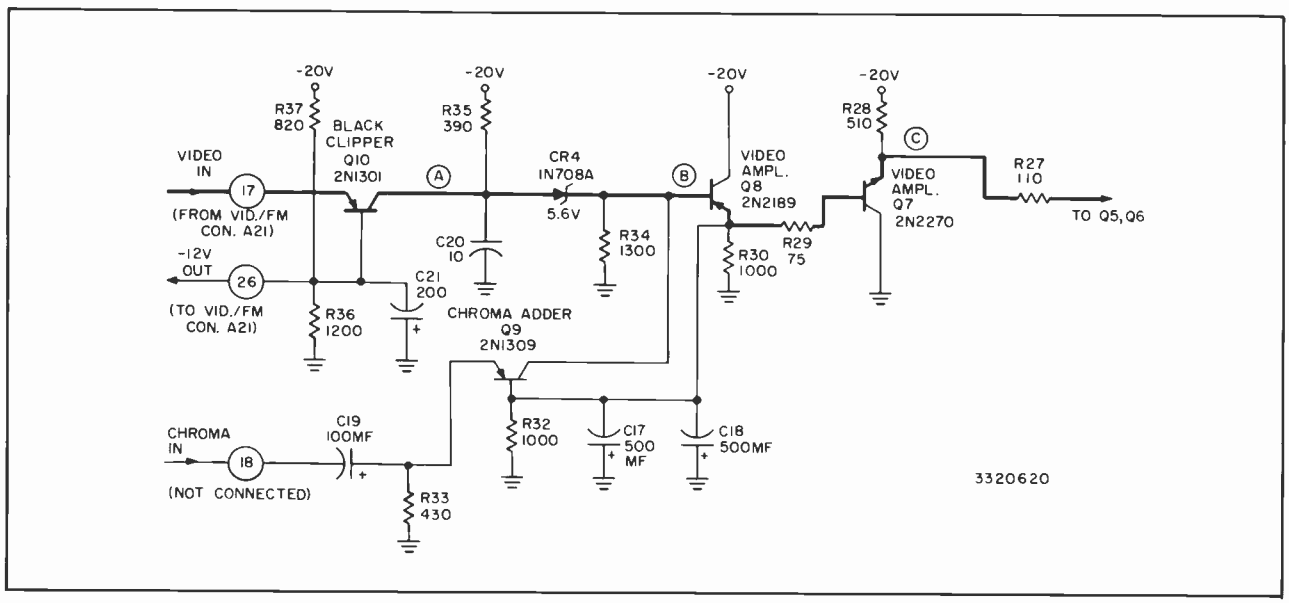
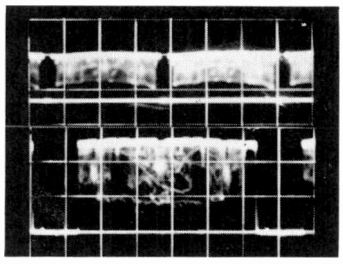
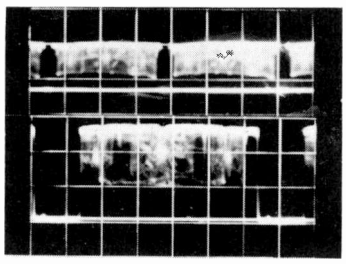


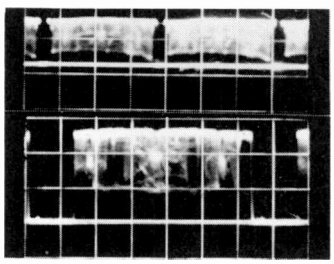
Figure 141—Black Clipper, Video Amplifiers and Chroma Adder Circuits



A. Q10 collector
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, .5v/cm



B. Q8 base
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, .5v/cm



C. Q7 emitter
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, .5v/cm

Figure 142—Typical Waveforms, Black Clipper, Video Amplifiers and Chroma Adder Circuits

Video Output

Transistor Q6 and Q5 (figure 143) are connected in a series amplifier configuration. The signal on the collector of Q6 is coupled through C15 to the base of Q5. Both ac and dc stabilization, in the form of C16 and Zener diode CR3, are employed to preserve constant levels. The series arrangement of Q5, Q6 provides signal polarities and amplitudes such that the voltage gain of the pair is unity and the output impedance low. The output signal of this stage is taken from the junction of the collector of Q5 and the emitter of Q6 and is fed to four sending-end terminated lines.

The first three outputs are fed through their associated terminating resistors and coupling capacitors; i.e., Video No. 1 via R20, C12; Video No. 2 via R21, C13; and Video No. 3 via R22, C14 to their respective coaxial connectors, 6J9, 6J8, and 6J7. The remaining output signal is fed through R19, C11 to two destinations. One is the VID OUT contact (15S2-2B4-1) on the waveform monitor switcher, and the other is the input stage (Q15) of the video detector circuit. Regenerated sync is added to each of the outgoing video signals at the output side of their respective coupling capacitors.

Sync Adder and Gain Controls

The regenerated sync signal originates in the Sync Logic (module B21). The sync signal is applied to the sync input terminal of the Video/FM Control module connector, which is connected in parallel with sync input terminal of the Video Output module connector.

The incoming sync is fed through a pulse shaping network consisting of C2, R6 to the base of Q1, the sync adder. The base of this transistor is clamped at −10 volts by CR1, and since the emitter is also at −10 volts, this transistor remains cut off until a positive-going sync pulse arrives. When this occurs, the transistor conducts and the amplified and inverted output appears on the collector.

The sync output on the collector is coupled through C1 and distributed via four isolation resistors (R1 — R4) in parallel, to each of the corresponding video output lines. The three external composite video output signals can be evaluated at their respective test points (TP1, TP2, TP3) on the front panel. The SYNC ON/OFF switch, S1, is an internal control which can be used to remove sync from the Video Out No. 3. line.

The gain of the sync adder, Q1, is determined by

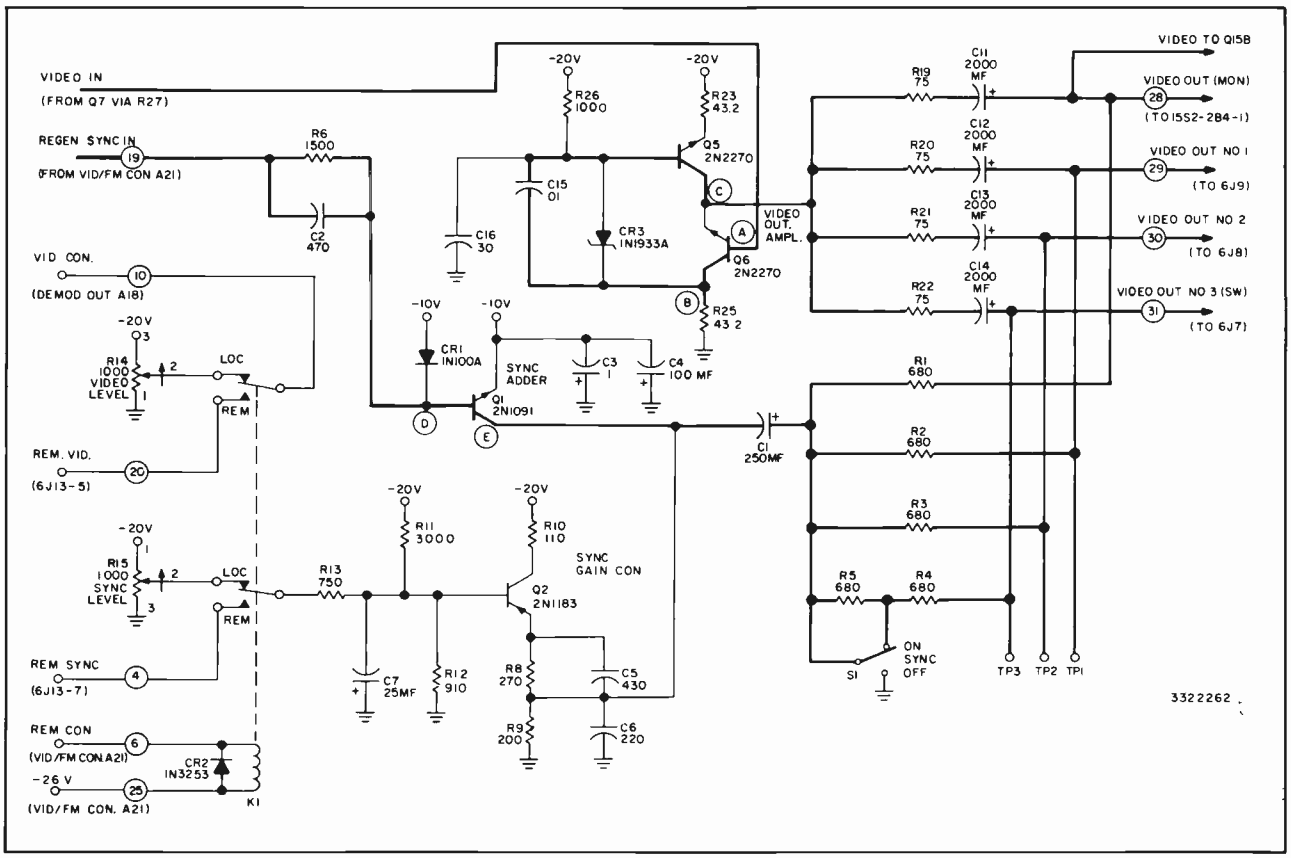
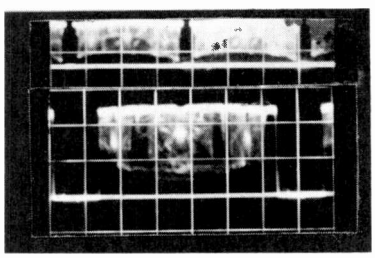
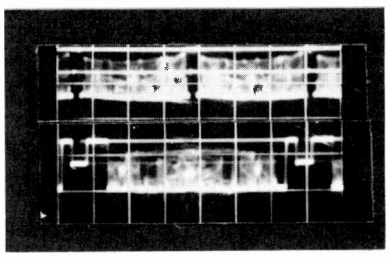


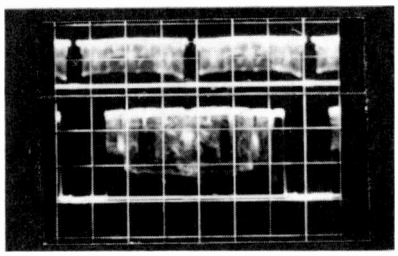
Figure 143—Sync Gain, Sync Adder and Video Output Amplifier Circuits



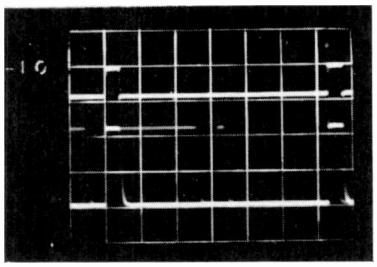
A. Q6 base
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, .5v/cm



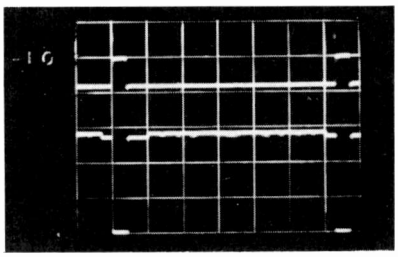
B. Q6 collector
Top: 5 ms/cm, .5v/cm
Bottom: 10 μs/cm, .5v/cm



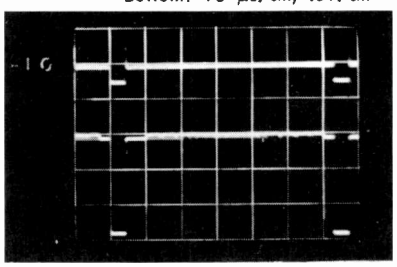
C. Q5 collector/Q6 base
Top: 5 ms/cm, 1v/cm
Bottom: 10 μs/cm, .5v/cm



D. Top: Q1 base, 10 μs/cm, 1v/cm
Bottom: C2 input, 10 μs/cm, 5v/cm



E. Top: Q1 base, 10 μs/cm, 1v/cm
Bottom: Q1 collector, 10 μs/cm, 2v/cm



F. Top: Q2 emitter, 10 μs/cm, 1v/cm
Bottom: Q1 collector, 10 μs/cm, 2v/cm

Figure 144—Typical Waveforms, Sync Gain, Sync Adder and Video Output Amplifier Circuits

the sync gain control stage, Q2. This transistor is, in effect, a dynamic load in the collector circuit of Q1. When the SYNC LEVEL potentiometer, R15, in the base of Q2 is adjusted, the circuit parameters of this stage are changed. This, in turn, causes a change in the load impedance presented by Q2 to Q1, and hence the amplitude of the sync output on the collector of Q1 is also changed.

Remote control of both video and sync levels is provided by the local/remote selector relay, K1. This relay operates in conjunction with the LOCAL/REMOTE switch, 4S6, on the PLAY control panel. The VIDEO LEVEL (R14) and the SYNC LEVEL (R15) potentiometers, (both of which are front panel controls) are connected to the local control contacts of K1. When remote control of these two functions is selected by means of switch 4S6, relay K1 disconnects R14 and R15 from their respective gain control stages.

Metering Circuit

The purpose of the video detector circuit (figure 145) is to furnish a rectified sample of the video output to the Signal Level Meter, 4M1, on the PLAY control panel, so that the level of the outgoing video can be monitored.

A portion of the video output being fed to the CRO switcher is applied through coupling capacitor C26 to the base of Q15, the first of a two-stage cascade video amplifier. The amplified output on the collector of Q15 is coupled through C25 to the base of the second video amplifier, Q14. From the collector of Q14, the signal is direct coupled to the base of Q13, an emitter follower. The output on the emitter of Q13 is coupled through C24 across the input of the peak-to-peak detector which consists of CR5, CR6, and C22. Use of the emitter follower to drive the peak-to-peak detector isolates the video amplifier from the loading effects of the former.

The rectified output of the detector is fed to a two stage video amplifier, Q11, Q12, both of which are emitter followers. The rectified signal is applied to the base of Q11 and the output on the emitter is direct coupled to the base of Q12. The meter signal is taken across potentiometer R39 in the emitter of Q12. The setting of potentiometer R39 (an internal control) determines the magnitude of the signal output current. The signal is fed via contact 3 on the B section of the AUDIO/VIDEO/CUE switch, 4S8, on the PLAY control panel, to the Signal Level Meter.

The video output level can be observed on the Signal Level Meter during playback by selecting the VIDEO position with the AUDIO/VIDEO/CUE switch. Assuming the video levels have been properly established throughout the system, the meter indicator will read zero VU for a standard 1 volt composite video output signal.

Instructions for calibrating the video level circuit of the meter are given under Adjustments.

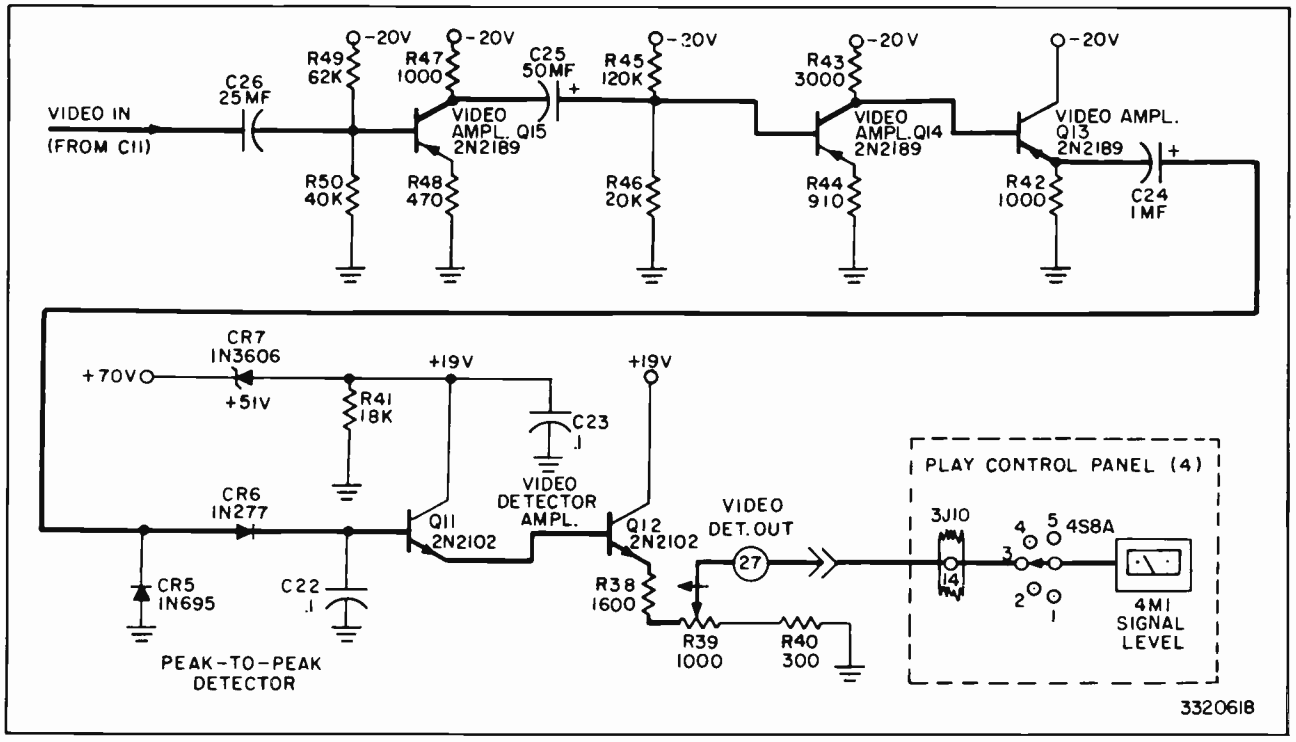


Figure 145—Video Output Level Metering Circuit

—20 Volt Regulator

A —20 volt regulator (figure 146) consisting of two emitter followers, Q3 and Q4, is used to furnish —20 volts to the video stages of this module.

The base of Q4 is biased at —20 volts therefore the potential appearing on the emitter is practically the same. The —20 volts on the emitter of Q4 is direct coupled to the base of Q3, consequently, the output available at the emitter of the latter is also —20 volts. The low output impedance associated with an emitter follower configuration insures that the output voltage will remain constant regardless of load variations. Ample filtering is provided by the three capacitors, C8, C9, and C10.

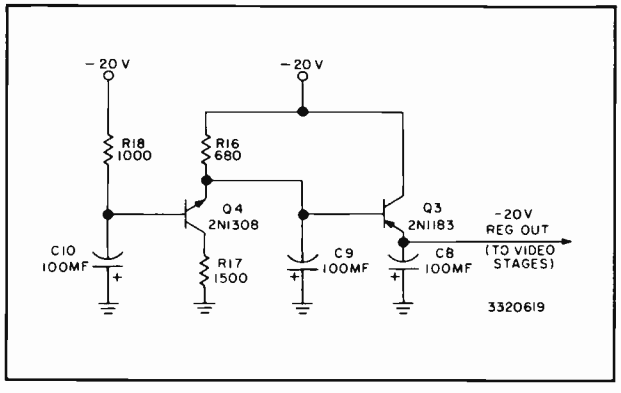


Figure 146 — —20 Regulator Circuit

Adjustments

The setting of the metering circuit signal level potentiometer, R39, should not be disturbed in the course of routine maintenance. If component replacement in the video detector circuit affects the output level, or if for some other reason the meter reading is not valid, the calibration of the circuit can be checked by following the procedure below.

1. Place the equipment power circuit breaker, 1CB1, in the OFF position.

2. Mount the Video Output module in an extender and insert in the TR-4.

3. Load the TR-4 with a tape recording of a standard signal.

4. Place the equipment power circuit breaker, 1CB1, in the ON position.

5. Place the TR-4 in PLAY mode and make the required playback operation checks. (Refer to the *TR-4 Operation Manual, IB-31810.*)

6. Turn the AUDIO/VIDEO/CUE switch on the PLAY control panel to VIDEO and observe the Signal Level Meter. The indicator should read zero VU. If not adjust R39 to obtain a reading of zero VU.

7. Place the power circuit breaker in the OFF position. Remove the extender and replace the module in the TR-4.

APPENDIX

Basic Circuit Descriptions

The three basic types of transistor configurations, common emitter, common base and common collector (emitter follower) are used in all the modules. These circuits are in many cases analogues to vacuum tube circuitry. However, some circuits, depending on the fact that both PNP and NPN transistors are available, have no direct analogy to vacuum tube circuits. In an effort to clarify both these special circuits and to show the relationship between vacuum tube circuits and transistor circuits, several basic circuit descriptions are given in the following paragraphs:

Multivibrators

An Astable Multivibrator is a two-stage oscillator in which one stage conducts while the other is cut off until a point is reached at which the stages reverse their conditions; that is, the stage which has been conducting cuts off, and the stage that has been cut-off, conducts. This type of oscillator is normally used to produce a square wave. The emitter-coupled transistor multivibrator is analogous to the cathode-coupled electron tube multivibrator circuit; or a collector-coupled transistor multivibrator is analogous to the plate coupled tube type. The time constants of the capacitors and resistors in the circuit determine the frequency. This type of multivibrator is used for the 2H master oscillator, Q1, Q2, in the Horizontal AFC Module.

A Monostable Multivibrator, basically, is a multivibrator having one stable and one unstable condition. A trigger drives the unit into the unstable state where it remains for a period of time determined by a time constant. The operating point then moves back to the original stable region. As in a vacuum tube circuit, one transistor may be conducting while the other is cutoff.

Another combination is also employed. Using an NPN and a PNP (complementary-symmetry), both transistors may be OFF in the relaxed or stabled state or both may be ON. The trigger then drives both transistors to the ON state, or OFF state, whichever case may be, and they return to the relaxed or stable state at the end of the timing cycle. This is the type of multivibrator used for the counting multivibrators in the Vertical Advance and Horizontal AFC Modules.

Pulse Narrowing Circuits

(Refer to figure 147.)

At several points in the processing amplifier circuits, the generator used narrows the input pulse to obtain the desired output pulse. These circuits are used to produce horizontal sync, horizontal blanking and the 9H pulse. The transistor circuit used for this purpose is analogous to the more familiar vacuum tube circuit which is sometimes called a "boxcar".

In the vacuum tube version, the grid of the tube is connected through a resistance R1 to the plate supply and the cathode is grounded. With no signal at the grid coupling capacitor C, the grid-cathode diode draws current through R1, reducing the grid to approximately zero potential. The plate of the saturated tube draws current through R2, reducing the potential at the plate to some low voltage. Application of a negative pulse at C cuts the tube off and stops the flow of grid current through R1. The grid-resistor current then flows into the capacitor, recharging it to its original potential with no signal. Therefore, the waveform at the grid is an R/C exponential one, charging toward +100 volts. As soon as this charging exceeds zero volts, the grid becomes positive and again draws current, thereby stopping the waveform at zero. At the plate, a pulse of opposite polarity is produced that is narrower than the input pulse. The actual width of the pulse in the output circuit depends on the value of R and C in the input circuit.

As shown in the diagram, the action of the NPN transistor circuit is similar, except that the output pulse amplitude is equal to the power supply voltage, due to the excellent saturating characteristics of the transistor, and the trailing edge of the pulse is sharper. A transistor type PNP may be used as successfully as the NPN type shown, but with opposite input and output pulse polarities.

Module Interchangeability

Listed in Table 1 are the video system modules used in the present series of RCA television tape recorders/players, i.e., TR-3, TR-4, TR-5, and TR-22. This table gives the name of the module, the unit number of that module in a particular type of recorder/player, the MI number of the module, and the type and the MI number of the recorder/player in which the module is used. Modules can be interchanged among the various recorders/players as long as the MI number of the substitute module is exactly the same as the MI number of the module being replaced. The primary purpose of the unit number is to denote the specific location of a module in a particular type of recorder/player. The unit numbers of some of the TR-22 modules have a letter right after the last digit. This alphabetical suffix, such as an A or B, signifies that the module was modified and is now different from any of its counterparts without a like suffix.

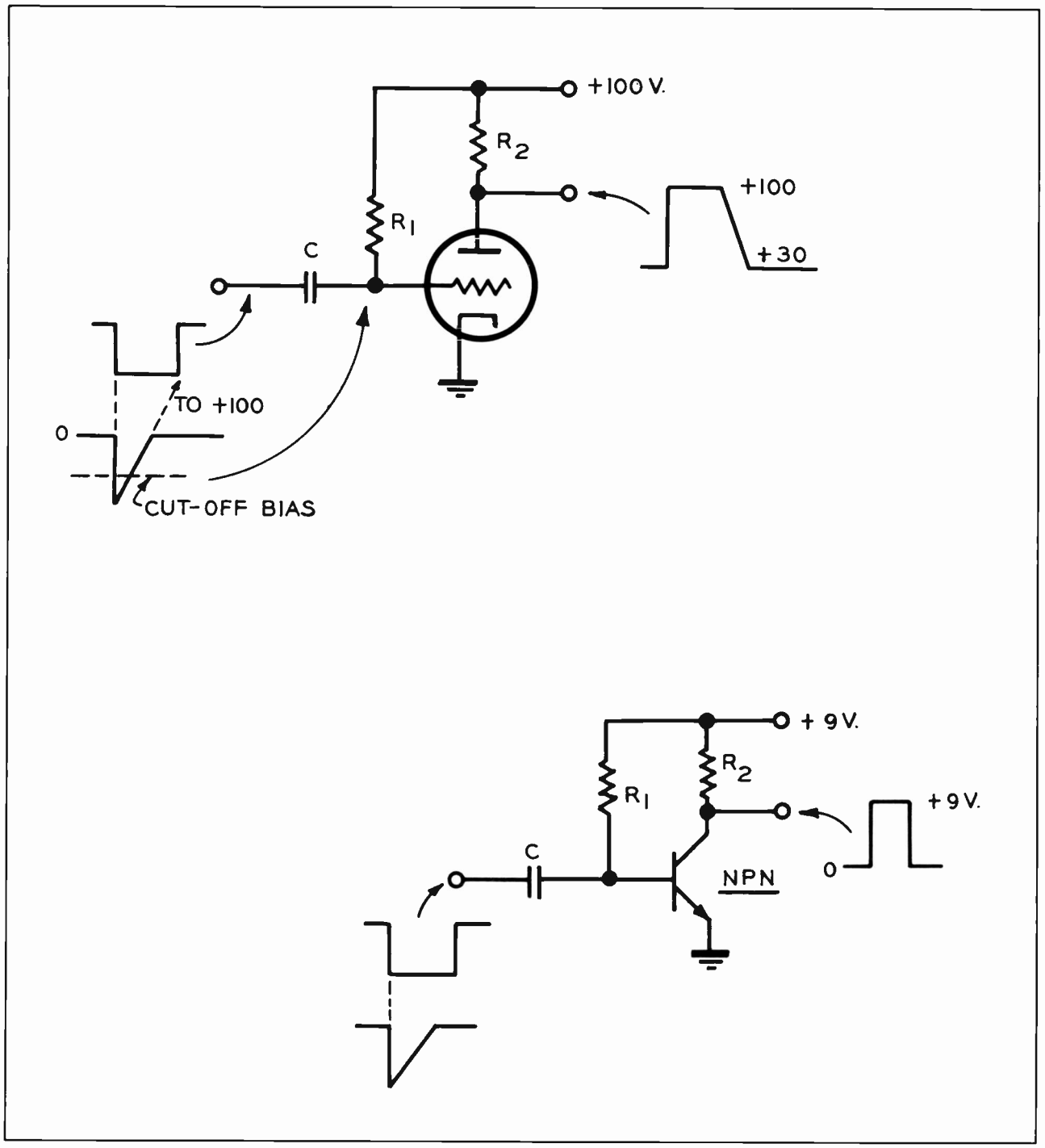


Figure 147—Vacuum Tube and NPN Transistor Pulse Narrowing Circuits

As an example in determining module interchangeability, consider the Video Preamplifier, the second module shown in Table 1.

Under unit number 116, MI-40603, this module can be used in TR-22's bearing MI numbers MI-40740, MI-40750, MI-40740A, MI-40750A, MI-40740B, and MI-40750B.

TR-22's bearing MI-40740C and MI-40750C require a Video Preamplifier designated MI-40603A, which is unit 116A. This same module, MI-40603A, appears under unit 2A1 in the TR-3 and TR-4 machines and under unit 2D1 in the TR-5's. Thus the MI-40603A module can be used in the "C" MI series of the TR-22, in the primary and "A" MI version of the TR-3 and TR-4 and in the primary MI of the TR-5.

TABLE 1. VIDEO SYSTEM MODULE INTERCHANGEABILITY CHART FOR TELEVISION TAPE RECORDERS/PLAYERS TYPES TR-3, TR-4, TR-5, TR-22

Module Name	*Module Unit No.*	*Module MI No.*	*Used In*	
			Type	*MI No.*
Video Input	103	40602	TR-22	40740 40750
	103	40602	TR-22	40740A 40750A
	103	40602	TR-22	40740B 40750B
	103	40602	TR-22	40740C 40750C
	A1	43370	TR-4	43301 43303 43305
	A1	43370	TR-4	43301A 43303A 43305A
Video Preamplifier	116	40603	TR-22	40740 40750
	116	40603	TR-22	40740A 40750A
	116	40603	TR-22	40740B 40750B
	116A	40603A	TR-22	40740C 40750C
	2A1	40603A	TR-4	43301 43303 43305
	2A1	40603A	TR-4	43301A 43303A 43305A
	2A1	40603A	TR-3	43300 43302 43304
	2A1	40603A	TR-3	43300A 43302A 43304A
	2D1	40603A	TR-5	43325
Video Control	131	40606	TR-22	40740 40750
	131	40606	TR-22	40740A 40750A
	131	40606	TR-22	40740B 40750B
	131A	40606A	TR-22	40740C 40750C

Module Name	*Module Unit No.*	*Module MI No.*	*Used In*	
			Type	*MI No.*
FM Equalizer	132	40607	TR-22	40740 40750
	132	40607	TR-22	40740A 40750A
	132	40607	TR-22	40740B 40750B
	132	40607	TR-22	40740C 40750C
Limiter	203	40608	TR-22	40740 40750
	203	40608	TR-22	40740A 40750A
	203	40608	TR-22	40740B 40750B
	203	40608	TR-22	40740C 40750C
	A16	40608	TR-4	43301 43303 43305
	A16	40608	TR-3	43300 43302 43304
	D12	43328	TR-5	43325
Demodulator	204	40609	TR-22	40740
	204	40640	TR-22	40750
	204	40609	TR-22	40740A
	204	40640	TR-22	40750A
	204	40609	TR-22	40740B
	204	40640	TR-22	40750B
	204	40640	TR-22	40740C 40750C
	A17	40640A	TR-4	43301 43303 43305
	A17	40640B	TR-4	43301A 43303A 43305A
	A17	40640A	TR-3	43300 43302 43304
	A17	40640B	TR-3	43300A 43302A 43304A
	D13	43329	TR-5	43325

TABLE 1. (Continued)

Module Name	Module Unit No.	Module MI No.	Used In	
			Type	MI No.
FM Standards	205	40610	TR-22	40740
	205	40641	TR-22	40750
	205	40610	TR-22	40740A
	205	40641	TR-22	40750A
	205	40610	TR-22	40740B
	205	40641	TR-22	40750B
	205	40641	TR-22	40740C 40750C
Modulator	207	40611	TR-22	40740 40750
	207	40611	TR-22	40740A 40750A
	207A	40611A	TR-22	40740B 40750B
	207B	40611B	TR-22	40740C 40750C
	A2	43371	TR-4	43301 43303 43305
	A2	43371	TR-4	43301A 43303A 43305A
	D5	43371	TR-5	43325
Record Delay Amplifier	209, 210	40612	TR-22	40740 40750
	209, 210	40612	TR-22	40740A 40750A
	209, 210	40612	TR-22	40740B 40750B
Record Amplifier	211-214	40613	TR-22	40740 40750
	211-214	40613	TR-22	40740A 40750A
	211-214	40613	TR-22	40740B 40750B
	211A-214A	40613A	TR-22	40740C 40750C
	A3-A6	40613A	TR-4	43301 43303 43305
	A3-A6	40613A	TR-4	43301A 43303A 43305A
	D1-D4	40613A	TR-5	43325

Module Name	Module Unit No.	Module MI No.	Used In	
			Type	MI No.
Playback Amplifier	215-218	40614	TR-22	40740 40750
	215-218	40614	TR-22	40740A 40750A
	215-218	40614	TR-22	40740B 40750B
	215A-218A	40614A	TR-22	40740C 40750C
	A11-A14	40614A	TR-4	43301 43303 43305
	A11-A14	40614A	TR-4	43301A 43303A 43305A
	A11-A14	40614A	TR-3	43300 43302 43304
	A11-A14	40614A	TR-3	43300A 43302A 43304A
Playback Delay Amplifier	219, 220	40612	TR-22	40740 40750
	219, 220	40612	TR-22	40740A 40750A
	219, 220	40612	TR-22	40740B 40750B
Horizontal AFC	227	40616	TR-22	40740
	227	40642	TR-22	40750
	227	40616	TR-22	40740A
	227	40642	TR-22	40750A
	227	40616	TR-22	40740B
	227	40642	TR-22	40750B
	227	40642	TR-22	40740C 40750C
	A20	40616	TR-4	43301
	A20	40642	TR-4	43303 43305
	A20	40642A	TR-4	43301A 43303A 43305A
	A20	40616	TR-3	43300
	A20	40642	TR-3	43302 43304
	A20	40642A	TR-3	43300A 43302A 43304A

TABLE 1. (Continued)

Module Name	Module Unit No.	Module MI No.	Used In Type	Used In MI No.
Vertical Advance	228	40617	TR-22	40740
	228	40643	TR-22	40750
	228	40617	TR-22	40740A
	228	40643	TR-22	40750A
	228	40617	TR-22	40740B
	228	40643	TR-22	40750B
	228	40617	TR-22	40740C
	228	40643	TR-22	40750C
	B22	40617	TR-4	43301
	B22	40643	TR-4	43303 43305
	B22	40617A	TR-4	43301A
	B22	40643A	TR-4	43303A 43305A
	B22	40617	TR-3	43300
	B22	40643	TR-3	43302 43304
	B22	40617A	TR-3	43300A
	B22	40643A	TR-3	43302A 43304A
Sync Logic	230	40618	TR-22	40740
	230	40644	TR-22	40750
	230	40618	TR-22	40740A
	230	40644	TR-22	40750A
	230	40618	TR-22	40740B
	230	40644	TR-22	40750B
	230	40644	TR-22	40740C 40750C
	B21	40618	TR-4	43301
	B21	40644	TR-4	43303 43305
	B21	40644A	TR-4	43301A 43303A 43305A
	B21	40618	TR-3	43300
	B21	40618	TR-3	43302 43304
	B21	40644A	TR-3	43300A 43302A 43304A
Video Output	233	40619	TR-22	40740 40750
	233	40619	TR-22	40740A 40750A
Video Output (Continued)	233	40619	TR-22	40740B 40750B
	233A	40619A	TR-22	40740C 40750C
	A22	43378	TR-4	43301 43303 43305
	A22	43378	TR-4	43301A 43303A 43305A
	A22	43378	TR-3	43300 43302 43304
	A22	43378	TR-3	43300A 43302A 43304A
FM Reference	302	40621	TR-22	40740 40750
	302	40621	TR-22	40740A 40750A
	302	40621	TR-22	40740B 40750B
	302	40621	TR-22	40740C 40750C
Demodulator Output	303	40622	TR-22	40740 40750
	303	40622	TR-22	40740A 40750A
	303	40622	TR-22	40740B 40750B
	303A*	40622A	TR-22	40740C 40750C
	A18	43376	TR-4	43301 43303 43305
	A18	43376	TR-4	43301A 43303A 43305A
	A18	43376	TR-3	43300 43302 43304
	A18	43376	TR-3	43300A 43302A 43304A
FM Switcher	318	40631	TR-22	40740 40750
	318	40631	TR-22	40740A 40750A

* Also supplied with ES-43579 ATC Kit to replace MI-40622.

TABLE 1. (Continued)

Module Name	*Module Unit No.*	*Module MI No.*	*Used In*	
			Type	*MI No.*
FM Switcher (Continued)	318	40631	TR-22	40740B 40750B
	318	40631	TR-22	40740C 40750C
	A15	40631	TR-4	43301 43303 43305
	A15	40631A	TR-4	43301A 43303A 43305A
	A15	40631	TR-3	43300 43302 43304
	A15	40631A	TR-3	43300A 43302A 43304A
	D10	43326	TR-5	43325
Video/FM Control	A21	43377	TR-4	43301 43303 43305
	A21	43377	TR-4	43301A 43303A 43305A
	A21	43377	TR-3	43300 43302 43304
	A21	43377	TR-3	43300A 43302A 43304A

TR-4 INSTRUCTION BOOKS

Because there are a number of instruction books associated with the TR-4, the following list is offered as a source of quick reference. Some of these books are not yet available. Those that are in print are supplied with the TR-4 or the applicable accessory equipment.

Title	*MI-43301* *MI-43303* *MI-43305*	*MI-43301A* *MI-43303A* *MI-43305A*
	IB Number	
Diagrams	IB-31807	IB-31807-1
Parts List	IB-31808	IB-31889
Description and Installation	IB-31809	IB-31809-A
Operation Manual	IB-31810	
TO-2A Waveform Monitor	IB-31811	
Picture Monitor	IB-31812	
Tape Transport	IB-31813	IB-31813-A
Servo System	IB-31814	
Audio System	IB-31816	IB-31816-A
Control and Power Supply Systems	IB-31817	
Video System	IB-31818	IB-31818-A
Monochrome Automatic Timing Corrector	IB-31819	
Electronic Splicer	IB-31869	
Cue Record/Playback Accessories	IB-31874	
Air Bearing Kit	IB-31886	

NOTES

RADIO CORPORATION OF AMERICA
BROADCAST AND COMMUNICATIONS PRODUCTS
CAMDEN, N. J.

Addenda

TR-4 Television Tape Recorder

VIDEO SYSTEM MAINTENANCE

IB-31818-B

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

INTRODUCTION

All modules in the TR-4 Recorder except the Playback Amplifiers, All-A14, Video Output Amplifier A22 and Demodulator Output A18 have been varied in design from the original TR-4 Recorder to enable the system to perform with greater stability and versatility in its capacity to accept accessories such as the monochrome ATC, color ATC, or the electronic splicer systems. Also, as in the horizontal AFC and sync logic modules, provisions are made for switching circuits to adapt to either domestic or international TV line standards. This Addenda must be used in conjunction with the instruction book IB-31818 supplied. The limiter circuits are combined with the demodulator circuits and therefore will be covered as a completely new module A17. Where the additions have affected the overall details of the circuitry, the information for that module has been supplied in full. Where the changes have been minor, the additions have been discussed and illustrated in relation to the already existing material in the basic TR-4 system as described in IB-31818. The modules involved, listed in the sequence of the TR-4 Tape Recorder instruction book, IB-31818, are as follows:

Symbol No.	*Title*	*MI-Number*	*Extent of Change*
A1	Video Input Module	MI-43370S	minor
A2	Modulator Module	MI-43371S	minor
A3-A6	Record Amplifier Modules	MI-40613A	minor
2A1	Video Preamplifier Module	MI-40603A	minor
A15	FM Switcher Module	MI-40631B	major
A17	Demodulator Module	MI-40640B	major
A20	Horizontal AFC Module	MI-40642B	major
B21	Sync Logic Module	MI-40644B	major
A21	Video FM Control Module	MI-43377A	minor

In the TR-4 Tape Recorder two types of vertical advance modules, B22, are used. In machines designed to operate on domestic standards only (525-lines) MI-40617A is used. In machines designed to operate on international switchable standards, 405/525/625 lines, MI-40643A is used. The international vertical advance module has a TV standards switch located on the front panel by which the desired line rate may be selected. International

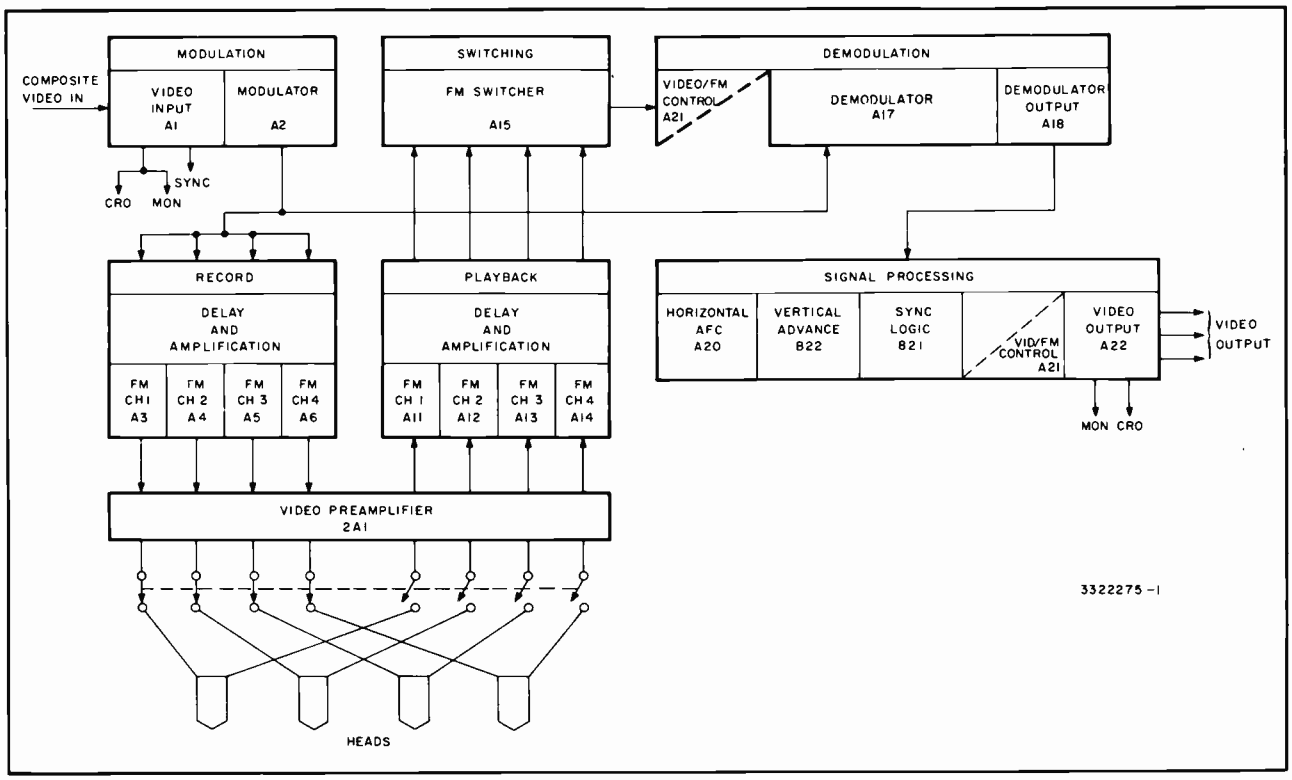


Figure 1—Simplified Video Functional Block Diagram

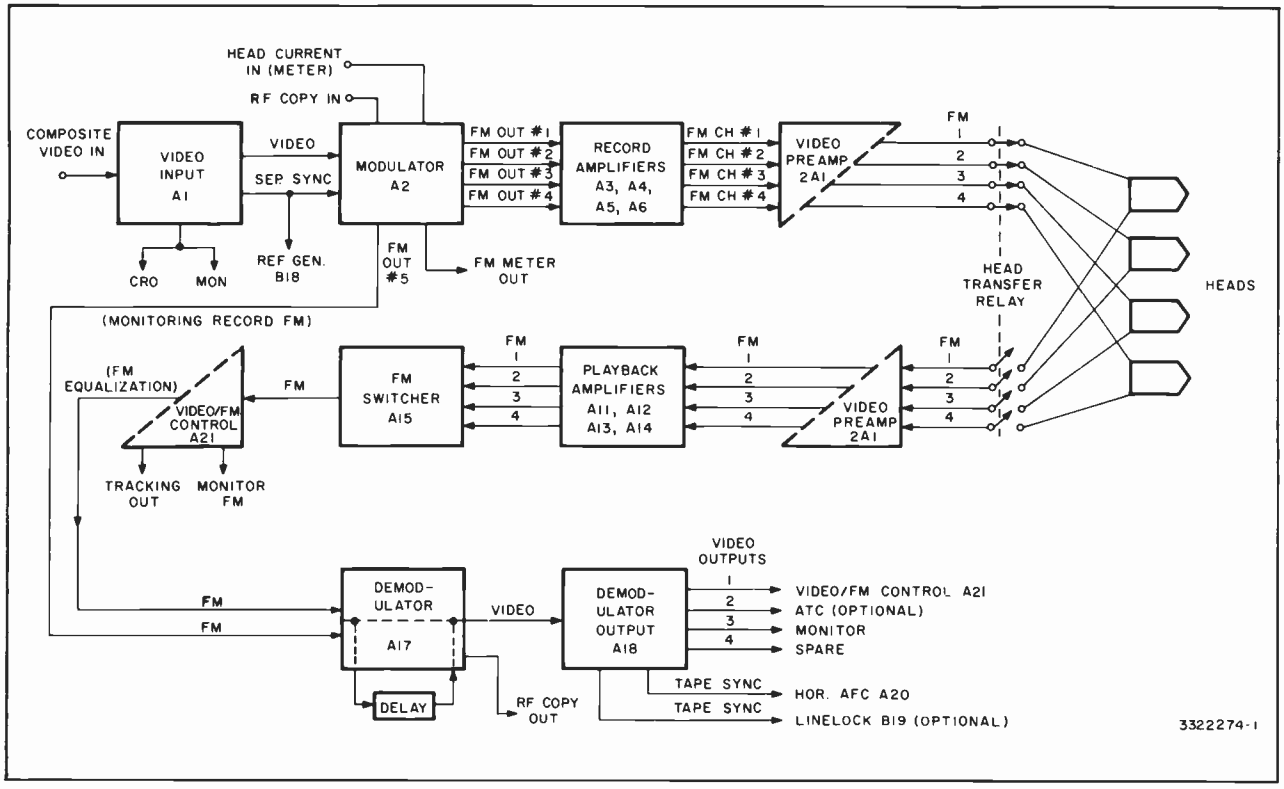


Figure 2—Block Diagram for Video/FM Subsystem

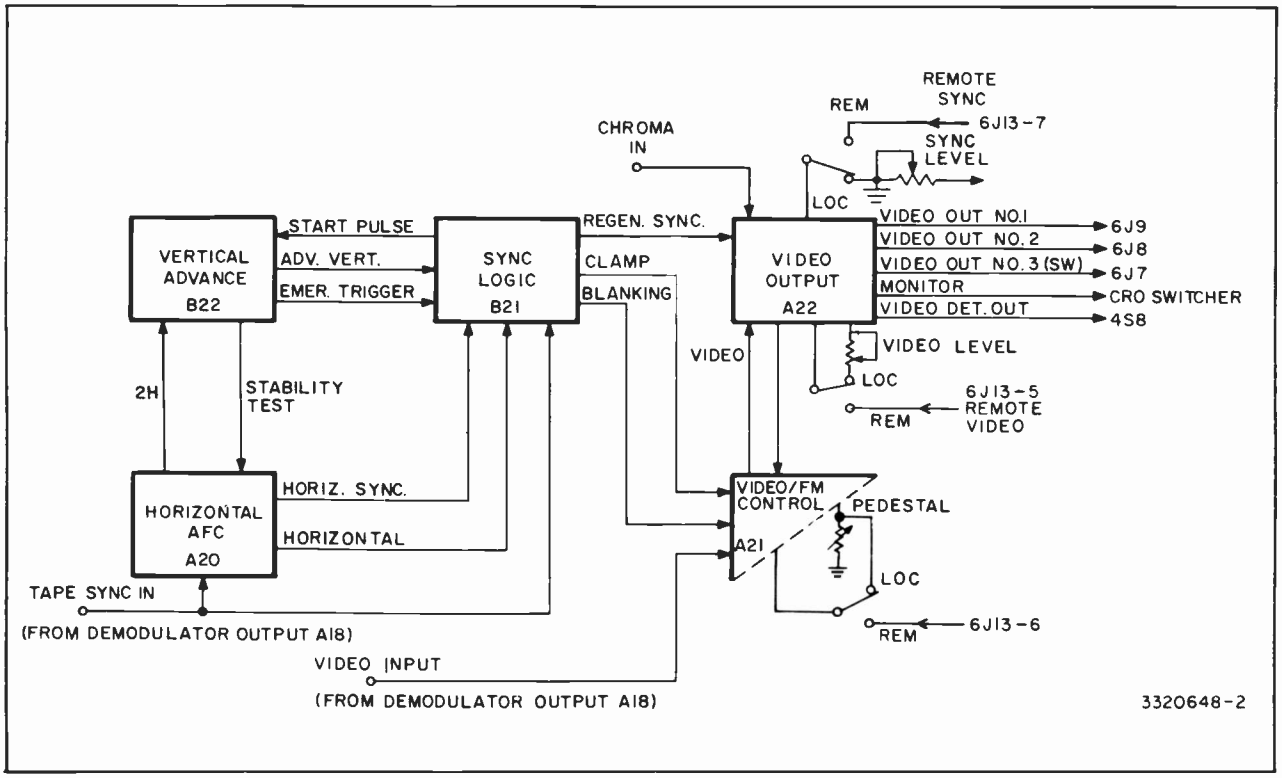


Figure 3—Block Diagram for Signal Processing Subsystem

machines as shipped from the factory are connected for operation on 405/525/625 standards unless previously requested otherwise. By changing jumper connections in the following modules: Horizontal AFC A20, Sync Logic B21, Vertical Advance B22, Tape Sync Processor B20, as shown in the schematic diagrams in IB-31807-2, the machine will operate on 525/625/819 standards.

In the Video System instruction book IB-31818, the overall systems description information is generally the same. Note that all references to the Limiter as a module are functionally true but the limiter stages and circuitry have been incorporated as part of the Demodulator module A17. The block diagrams, figures 1, 2 and 3, have been corrected and up-dated to include the latest information.

The following tabulation of instruction books for the TR-4 TV Tape Recorder will be currently available:

Title	*IB-Number*
Diagrams	IB-31807-2
Parts List	IB-31808-1
Description and Installation	IB-31809-B
Operation Manual	IB-31810-1
Servo Systems	IB-31814-1
Control and Power Supply Systems	IB-31817-1
Electronic Splicer	IB-31869

MODULE DESCRIPTIONS

Video Input Module A1

The addition of the light driver stage Q10 does not effect in any way the video input module functions. Transistor Q10 drives the switchlock indicator and is triggered through P1-3 from the splicer logic module B6. The circuit and plug connections are shown in figure 4.

Modulator Module A2

Several stages have been added to the modulator to accommodate the use of the electronic splicer system. The splice video record switch, mounted on the modulator module, ties into the modulator switch REC/RF COPY, S1, through the −20 volt switch Q18 and Q19 from the base of Q63. Refer to the block diagram, figure 5. The function of the modulator is unchanged except that the control should be adjusted so that the input of the record emitter followers is 0.7 volts peak-to-peak. Note that TP-3 should no longer be used while making this adjustment. This test point, which is marked RF OUT, is actually at the circuit's FM output as before. Refer to figure 6 for the schematic diagram of the switcher stages and connections to P1.

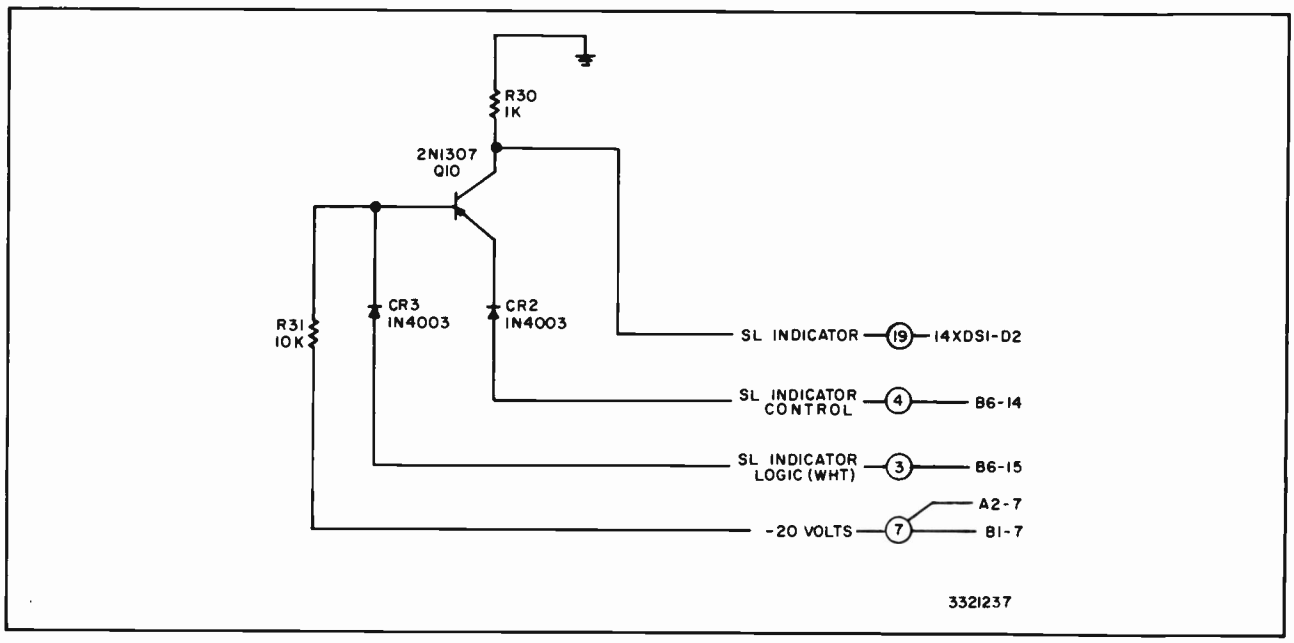


Figure 4—Switchlock Indicator Driver Stage

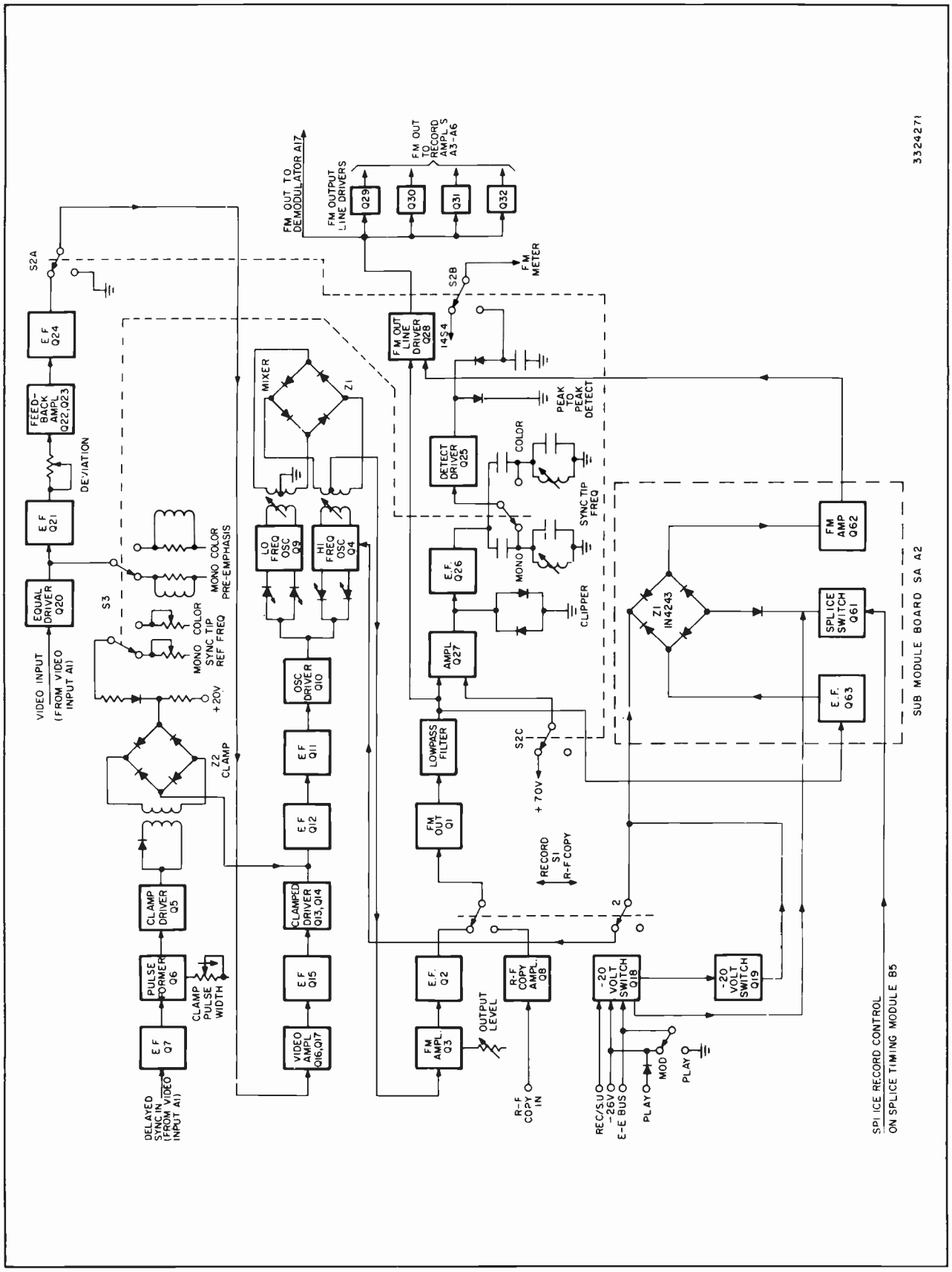


Figure 5—Block Diagram for Modulator Module A2

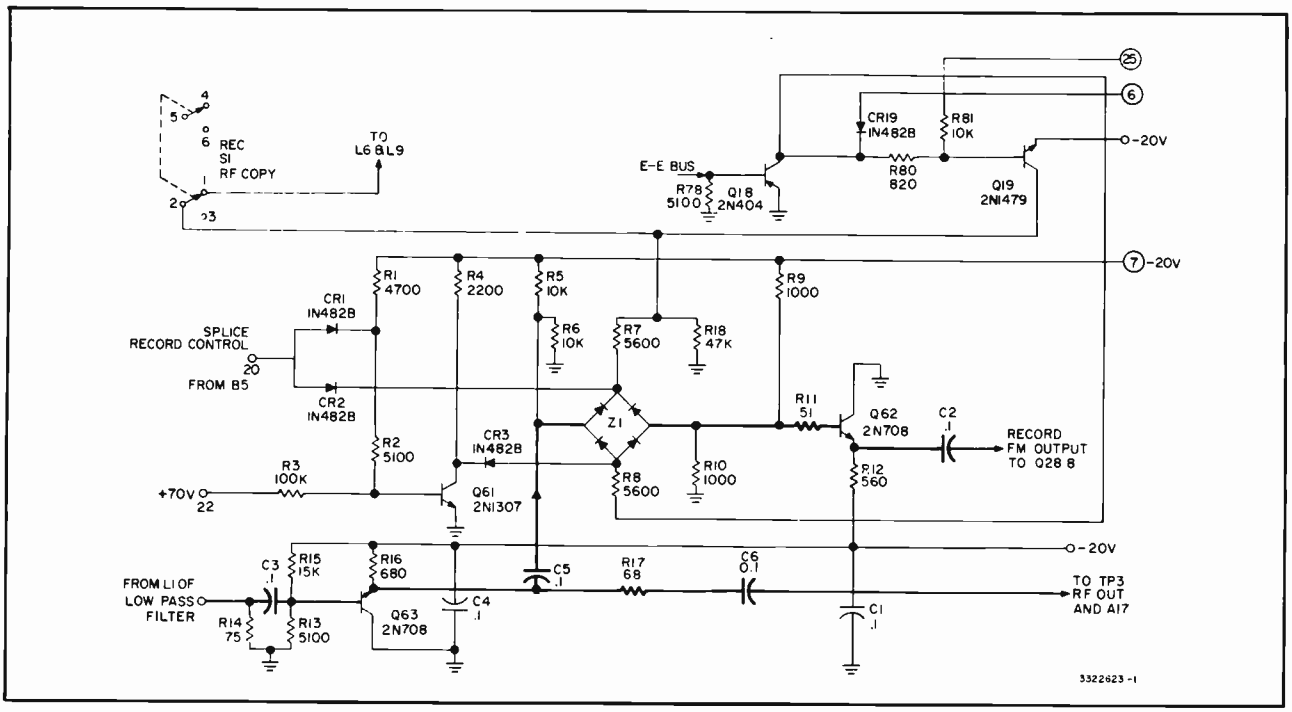


Figure 6—Switcher Stages for Electronic Splicer Modules

In IB-31818, on page 34, *Sync Tip Clamping*, the information is correct except that a clamp pulse width adjustment has been added to the pulse former circuit Q6. Refer to figure 7 in this addenda, IB-31818-B. In paragraph 3, the circuit should now be described as follows:

When a synchronizing or an equalizing pulse occurs at the emitter of Q7, the negative-going lead is coupled through C31 to the base of Q6 cutting off Q6 and permitting the collector potential to move towards ground. Immediately following the negative going excursion of the pulse, the base of Q6 begins to return to ground as C31 charges through R40. The pulse width is adjusted by potentiometer R37 to approximately 0.8 to 1.0 microsecond. Thus the base of Q6 approaches ground on a time constant deter-

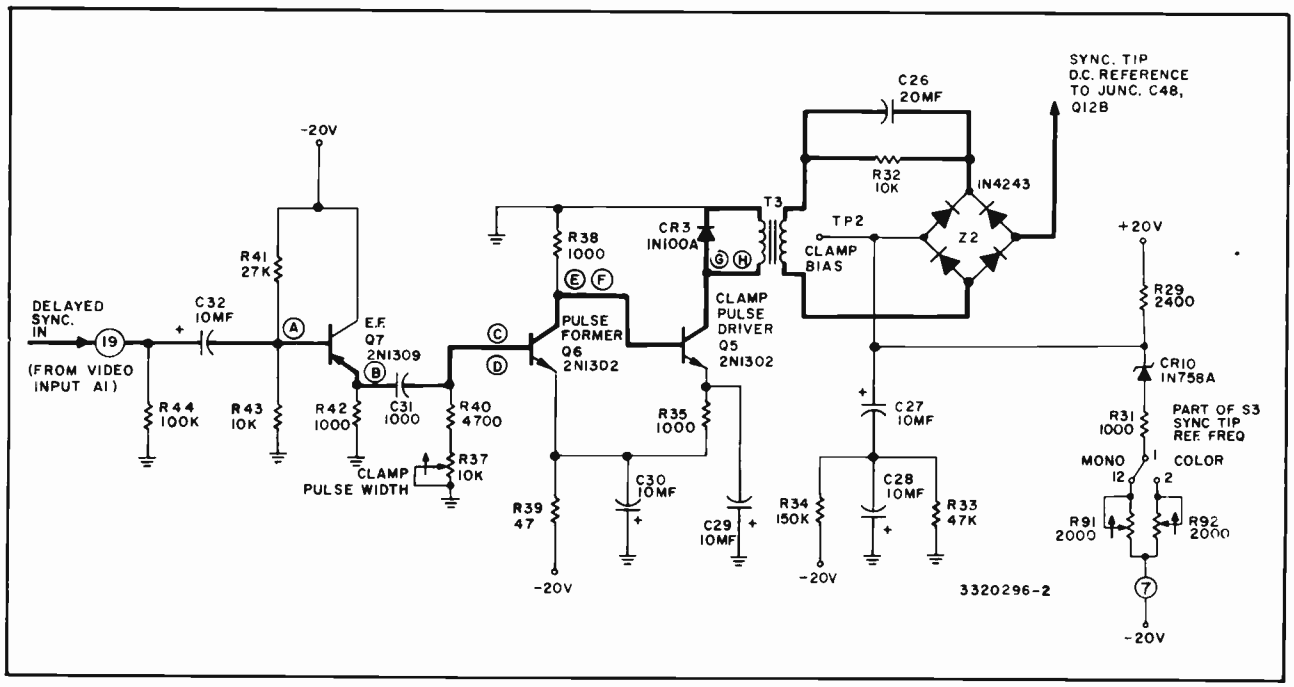


Figure 7—Pulse Former and Sync Tip Clamp Circuit

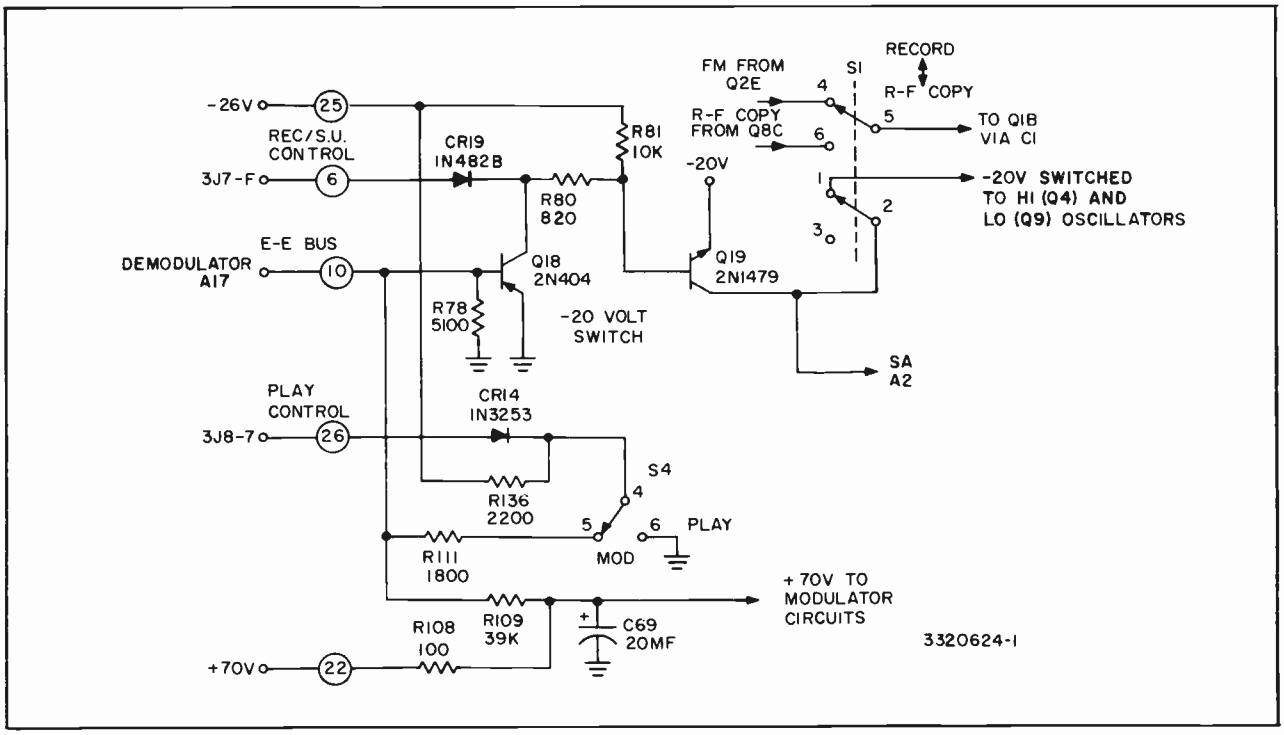


Figure 8— −20 Volt Electronic Switch, MOD/PLAY and Record RF COPY Switches

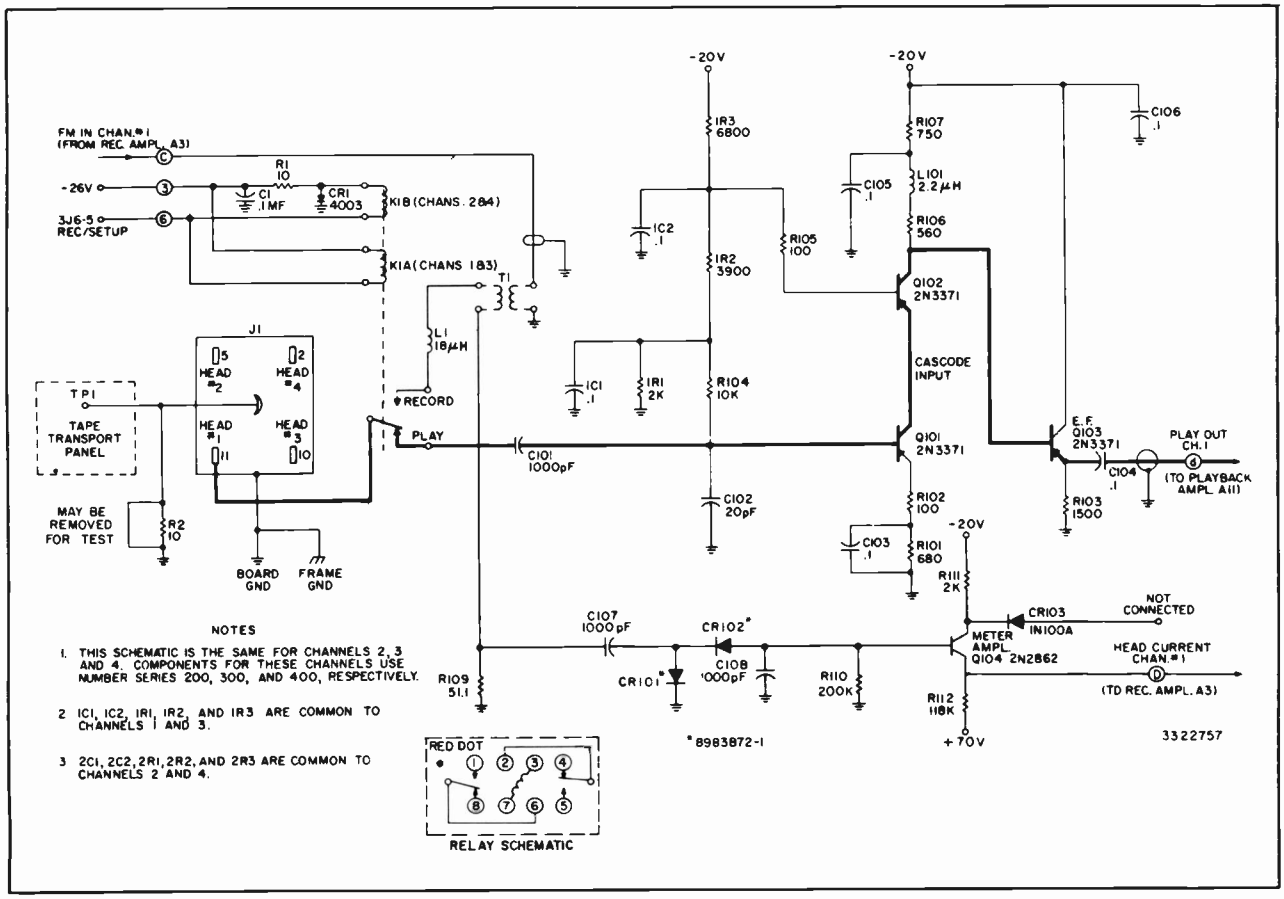


Figure 9—Video Preamplifier Circuit

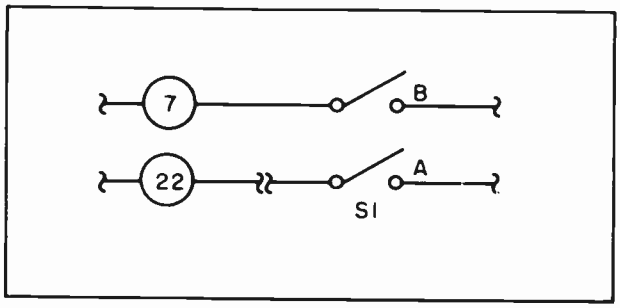
mined by capacitor C31 and the setting of potentiometer R37. When the potential on the base becomes sufficiently close to ground, Q6 saturates and the collector goes to approximately −20 volts.

On page 36 of IB-31818, change all reference to 1.4 microseconds to read 0.8 to 1.0 microseconds.

Any reference to the limiter is actually to the limiter circuits on the demodulator module, A17. On page 40, figure 40, has been corrected and inserted here as figure 8.

IB-31818, Page 47

In figure 47, for the Record Amplifiers, change the ON-OFF switch, S1, to agree with the configuration shown in the sketch.



IB-31818, Page 49, Figure 48

Relay K1 in the Video Preamplifier has been replaced with two relays, K1A and K1B. Disregard the schematic figure 48. In its place, use the one supplied with this addenda, figure 9.

IB-31818, Page 55

Under *FM Switcher Module A15,* delete all text pertaining to this module including schematics and associated waveforms. In place of the deleted material, use the following:

FM SWITCHER Module A15

General

The FM Switcher combines the four separate FM channel outputs from the four Playback Amplifiers (modules A11-A14) into one continuous FM signal, which is then fed to the FM equalizer circuit in the Video/FM Control module A21. Switching pulse suppressor circuits are provided for the Demodulator Output module A18. Refer to the block diagram figure 10.

In the non-critical first switching stages, the four inputs are combined to form two outputs. Here the

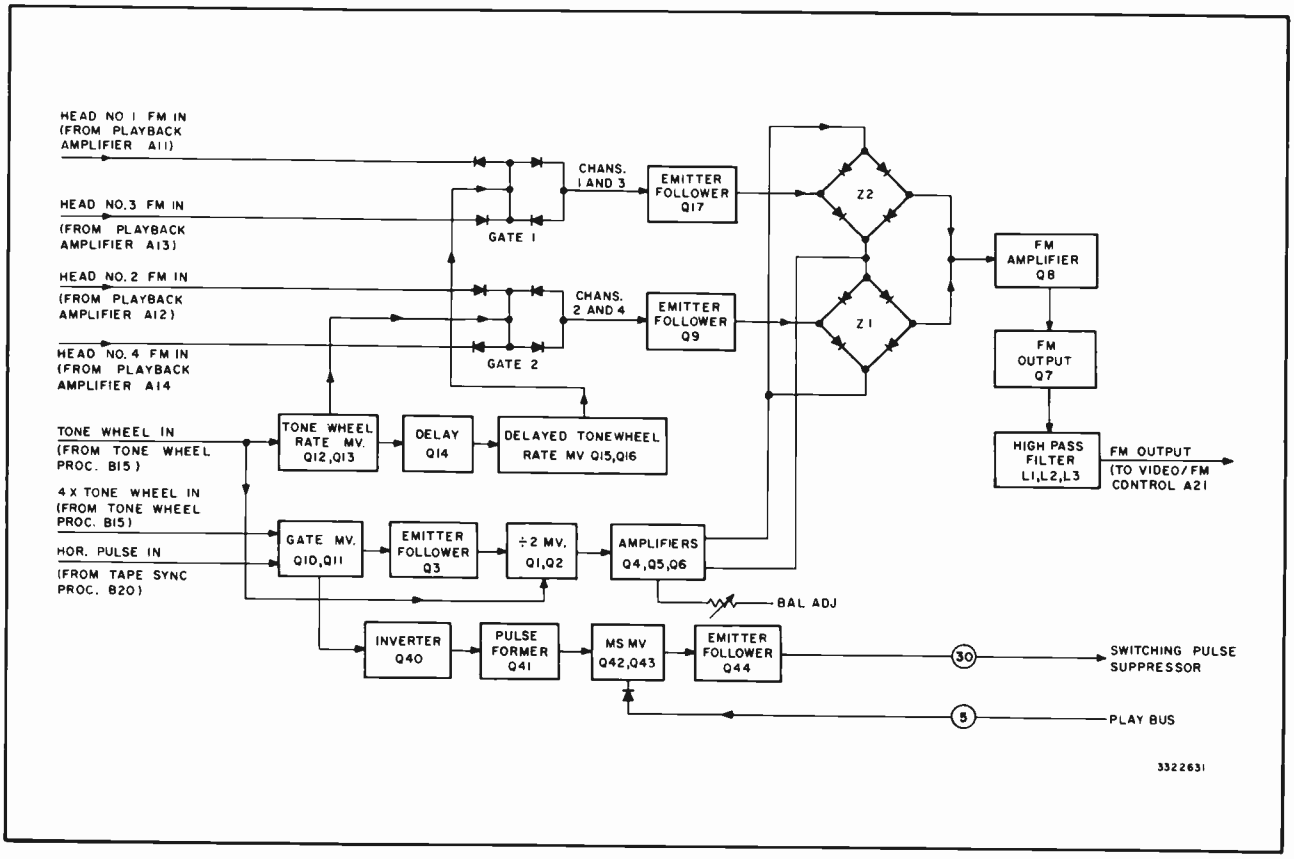


Figure 10—Block Diagram for FM Switcher A15

signals are fed in pairs, i.e., channels 1 and 3 and channels 2 and 4, from opposite sides of the headwheel into two diode gates. The gates are opened at the appropriate time by keying pulses. These pulses are generated in the two tonewheel rate (240/250 cps) multivibrators, Q12, Q13, and Q15, Q16, the latter being driven with a delay trigger.

The timing reference for the first or undelayed TW rate multivibrator, Q12, Q13, is established by a pulse (A, figure 11) derived from the Tonewheel Processor (module B15). This pulse occurs near the middle of head no. 1 due to the mechanical arrangement of the pulse-generating notch on the tonewheel in relation to the four heads.

Two pulse outputs are taken from the first TW rate multivibrator, Q12, Q13. The first output (B, figure 11) is used to key diode gate no. 2 which combines the FM input of channels 2 and 4 into a single channel (C, figure 11).

The second pulse output is passed through a delay amplifier, Q14, which delays the pulse approximately 1000 microseconds (D, figure 11). The delayed pulse is used to drive the second or delayed TW rate multivibrator, Q15, Q16. The output of this multivibrator (E, figure 11) keys diode gate no. 1 where the FM inputs of channels 1 and 3 are combined into a single output (F, figure 11). The output of each gate is fed to a separate emitter follower, each of which is followed by a diode quad. From gate 1 the output is fed to Q17 which drives quad Z2. Similarly, the output of gate 2 goes to Q9 and the latter, in turn, drives Z1. The quads, Z1 and Z2, are driven in push-pull phase opposition by a 2 x TW rate (480/500 cps) pulses, to combine the two FM inputs into a single FM output. The gating input to the quads is generated in Q1, Q2, the ÷2 multivibrator

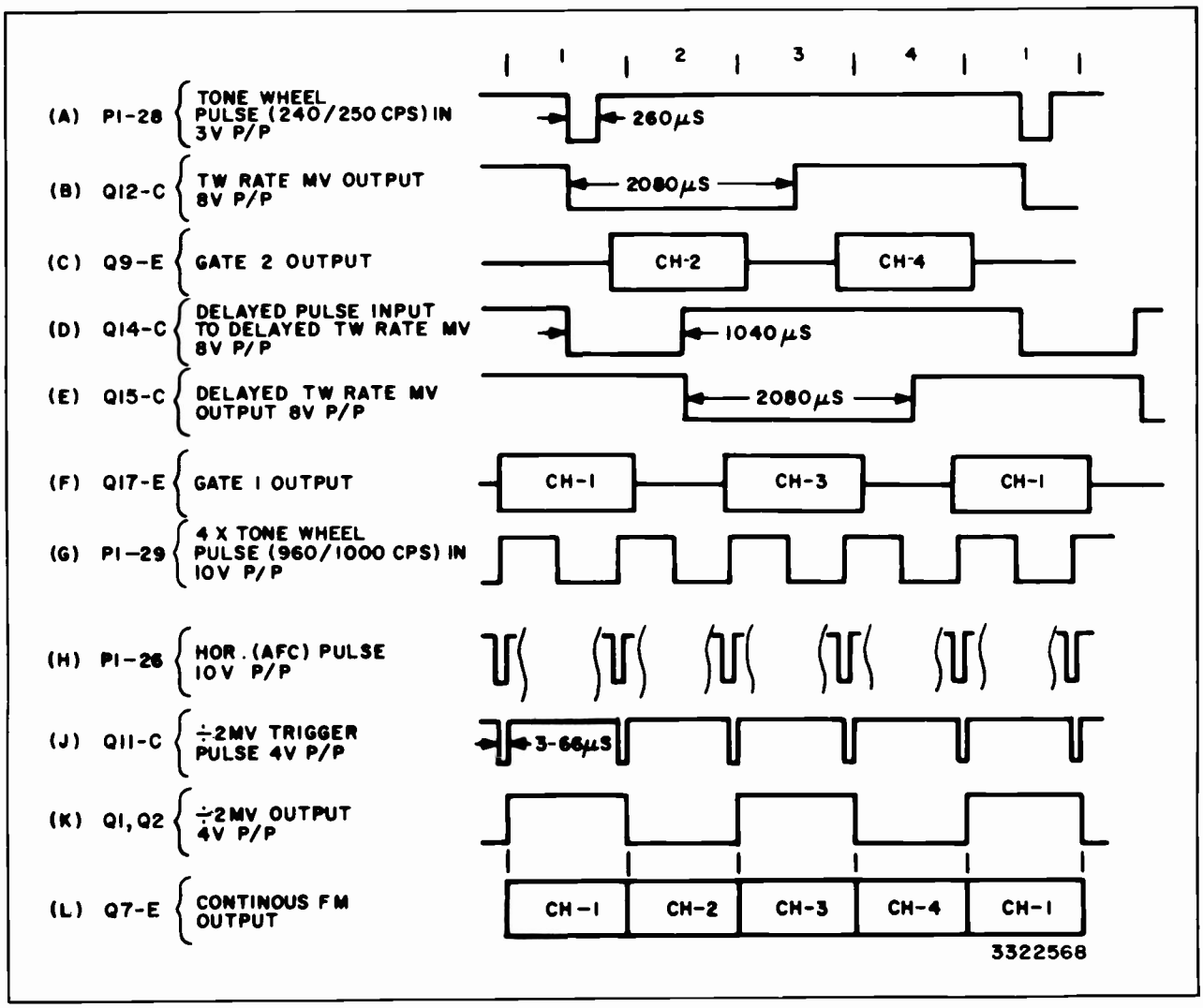


Figure 11—Idealized Waveform

or binary divider. The output from Q1, Q2 (K, figure 11) is passed through a three-stage feedback amplifier, Q4, Q5, and Q6, and then applied to the quads. Correct phasing of the pulse is obtained by triggering one side of the ÷2 multivibrator Q1, Q2, with the tonewheel pulse, insuring that head no. 1 is keyed in when the tonewheel pulse occurs.

Switching between the quads takes place at the time the first sync pulse interval occurs during the period when two heads overlap in reading information from the tape. To confine the switching to the overlap region, a delayed 4 x Tonewheel (960/1000 cps) pulse is developed in the Tonewheel Processor (module B15). The delay of this pulse is controlled by the 4 x TW delay potentiometer on the Tonewheel Processor, and the potentiometer is adjusted so that the pulse edge occurs during the overlap period.

The 4 x TW pulse (G, figure 11) is fed to the bistable gate multivibrator, Q10, Q11, causing it to change state. The gate (Q10, Q11) is then flipped to the opposite state by the first afc horizontal pulse (H, figure 11) arriving after the 4 x TW pulse. (The afc horizontal pulse is formed in the Tape Sync Processor (module B20). Once the gate has been flipped by this horizontal pulse, the continuing train of horizontal pulses will have no further effect on the gate, until another 4 x TW pulse arrives and causes the gate to again change state.

The output pulse from the gate (J, figure 11) is coupled through an emitter follower, Q3, to the ÷2 multivibrator, Q1, Q2. It is the positive-going trailing edge of this pulse, which is determined by the first horizontal pulse following the 4 x TW pulse, that triggers the ÷2 multivibrator.

The output of the ÷2 multivibrator, after passing through a three-stage amplifier, Q4, Q5, Q6, drives the two quads to combine their separate FM input signals into a single FM output signal. The single continuous FM output signal from the quads (L, figure 11) is fed to an amplifier Q8. The amplified output of Q8 is coupled by an emitter follower, Q7, to drive the line to the FM equalizer circuit on the Video/FM Control (module A21).

Generating Diode Gate Keying Pulses

Figure 12 shows the circuits that form the keying pulses which drive the two diode gates. The tonewheel rate multivibrator, Q12, Q13 is a monostable multivibrator, with Q13 off and Q12 on in the stable state. A pulse from the Tonewheel Processor (module B15) is coupled through steering diode CR20 to Q13, turning it on. The on period of Q13 is deter-

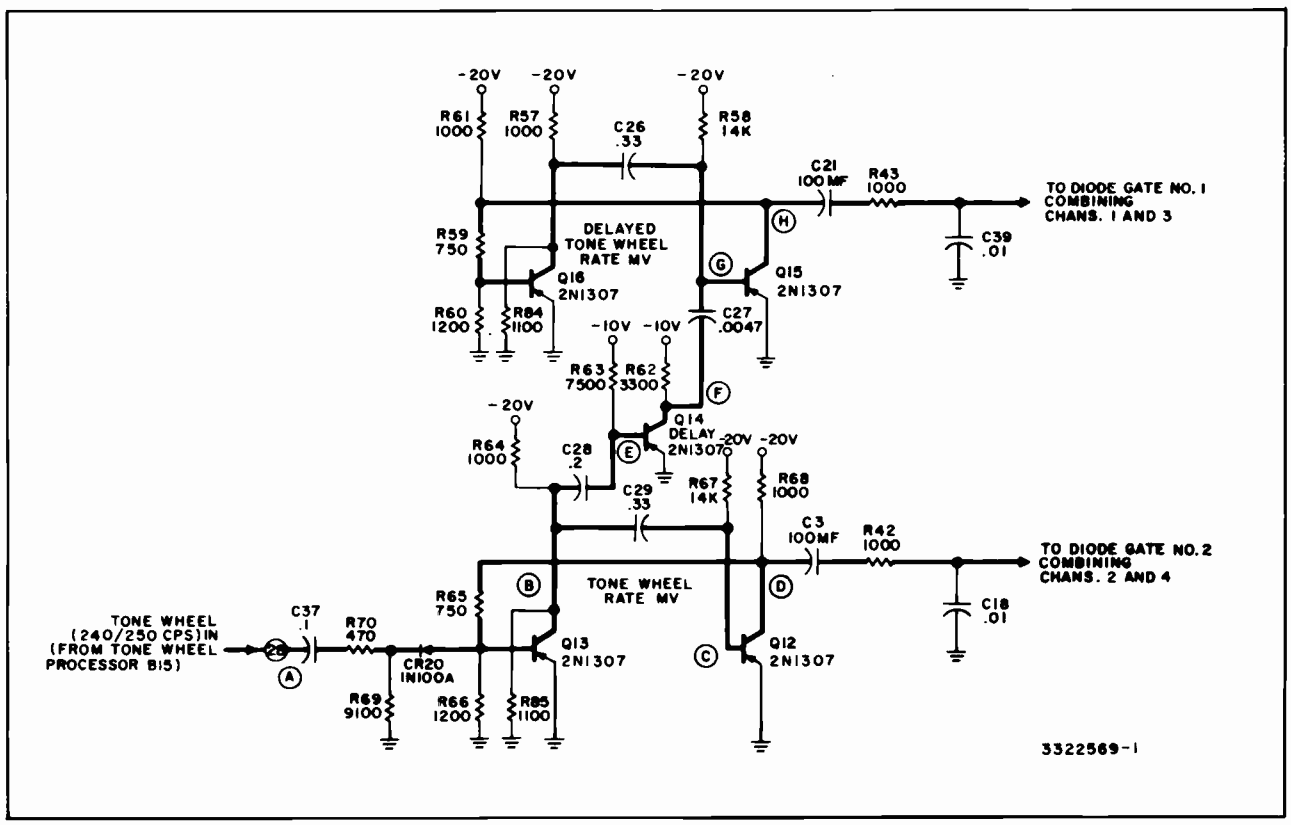


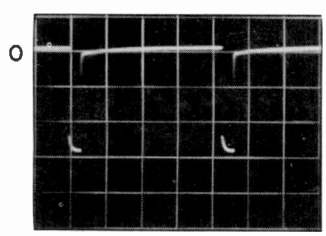
Figure 12—Tonewheel Rate MV and Delay Circuits

mined by the length of time C29 takes to charge through R67, which is approximately 2000 microseconds. From the collector of Q12, the output pulse, slightly integrated by C18 and R42, is fed to diode gate no. 2, where channels 2 and 4 are combined. The output pulse from the collector of Q13, the other half of the multivibrator, is fed to Q14, the delay stage, cutting it off. (The delay stage is a standard boxcar circuit.) The delay interval, which is approximately 1000 microseconds or one head wide, is determined by C28 discharging through R63. The positive-going edge of the pulse appearing on the collector of Q14 is used to trigger the delayed tonewheel rate mutlivibrator, Q15, Q16. This is a monostable multivibrator, identical to Q12, Q13. The input trigger is fed to the base of Q15, turning off this normally on transistor. The output pulse for keying diode gate no. 1, where channels 1 and 3 are combined, is taken off the collector of Q15 and coupled through an integrator consisting of C39 and R43 to the gate.

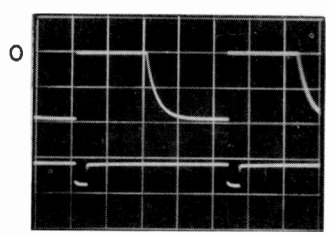
Diode Gates

The diode gate no. 2 is shown in figure 14. The output pulses from the tonewheel rate multivibrator, Q12, Q13, are applied to gate no. 2 at the junction of R5 and R6. During the negative half of the cycle, CR2, CR4 conduct, and CR1, CR3 are cut off, thus allowing FM input from channel 2 to pass. On the positive half of the cycle, diodes CR1, CR3 conduct while CR2, CR4 are cut off, and the FM input from channel 4 is passed. As a result of each pair of diodes switching on and off, one combined signal appears at the output. The output of the gate is coupled through C4 to an emitter follower, Q9. The output from the emitter of Q9 is coupled through C5 to one side of quad Z1.

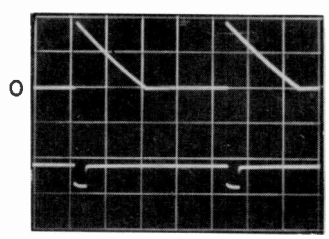
Diode gate no. 1, which combines the input of channels 1 and 3, is identical to gate no. 2, except that the keying pulses originate in the delayed tonewheel rate multivibrator Q15, Q16. These pulses are delayed approximately 1000 microseconds or one



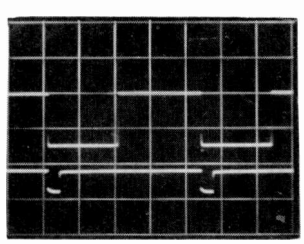
A. P1-28, tone wheel pulse, 1 ms/cm, 1 v/cm



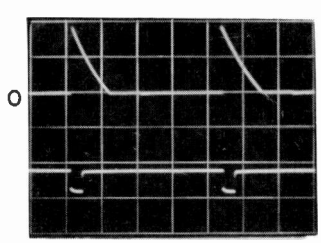
B. Top: Q13 collector, 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



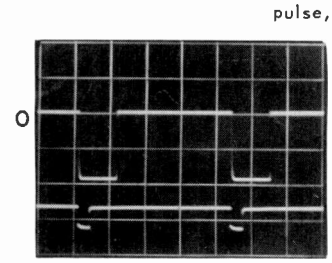
C. Top: Q12 base, 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



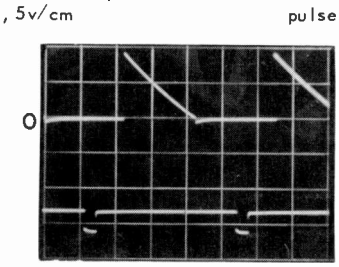
D. Top: Q12 collector, 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel, pulse, 1 ms/cm, 5v/cm



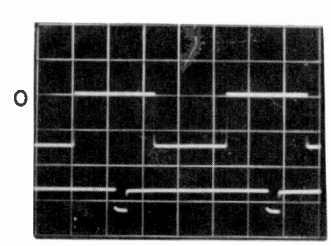
E. Top: Q14 base, 1 ms/cm, 5v/cm.
Bottom: P1-28 , tone wheel pulse, 1 ms/cm, 5v/cm



F. Top: Q14, collector, 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



G. Top: Q15 base, 1 ms/cm, 5v/cm.
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



H. Top: Q15 collector, 1 ms/cm, 5v/cm.
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm

Figure 13—Typical Waveforms, Tonewheel Rate MV and Delay Circuits

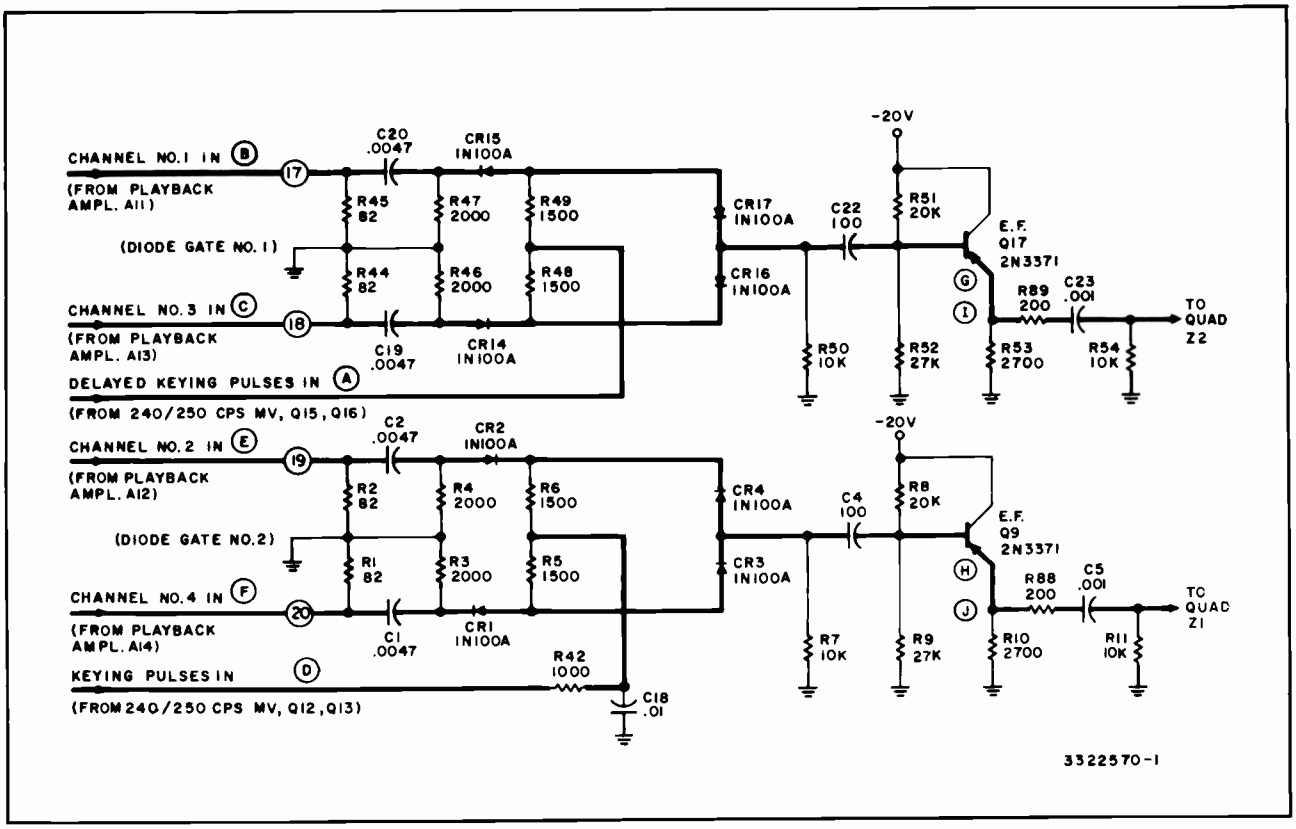


Figure 14—First Gating Stage, 4X2 Channel Switching and Emitter Follower Circuits

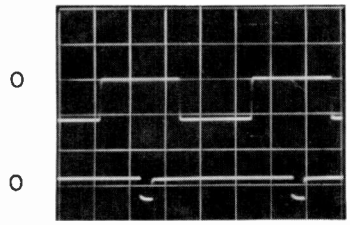
head period so that they will occur during the time interval of heads 2 and 4. Similarly, the output of gate no. 1 is fed to an emitter follower, Q17, the output of which is coupled through C23 to quad Z2.

Timing of Quad Keying Pulses

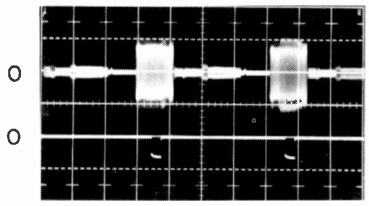
The timing of the pulses used to key the quads is critical. Switching must take place during the first horizontal sync interval that occurs in the overlap region when two video heads are in contact with the tape. Switching at this time prevents any transients that might occur from being seen, and enables the redundant information read by two heads overlapping to be eliminated. The bistable gate (960/1000 cps) multivibrator, Q10, Q11, (see figure 16) acts as a gate to ascertain the time this coincidence takes place. One input to Q11 is the 4 x TW (960/1000 cps) pulse, which originates in the Tonewheel Processor (module B15). This pulse is timed by adjusting the 4 x TW DELAY control on the Tonewheel Processor to coincide with the overlap period. If this control is not properly adjusted, gaps or overlaps will occur in the switching. The effect of this will be to cause noise to appear on the picture monitor every sixteen lines.

The pulse is differentiated by C30 and R73 and the positive spike is coupled through CR21 to turn off Q11 and turn on Q10. The multivibrator remains in this state until Q10 is triggered off by the trailing edge of a horizontal sync pulse, which is generated in the afc horizontal multivibrator in the Tape Sync Processor module B20. The afc circuit advances the pulse so that switching coincides with the horizontal sync interval of the video signal. It is necessary to advance the pulse to compensate for the delays encountered in the FM demodulation process used in recovering the video component and then in separating sync from the video. The degree of pulse advance is variable and is set by adjusting the TAPE HOR FREQ SET control on the Tape Sync Processor, so that switching takes place immediately following the leading edge of sync.

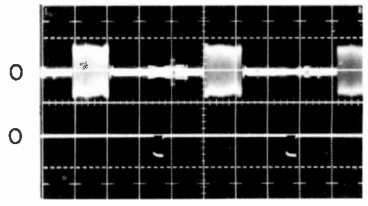
The horizontal sync pulse input to Q10 is differentiated by C36 and R82 and coupled through CR22 to the base of Q10. The initial positive spike turns off Q10 and turns on Q11. The subsequent pulses have no effect on Q10, and the multivibrator remains in this state until another 4 x TW pulse arrives to trigger Q11 and then the cycle is repeated. The output pulse, at a 4 x TW rate, is taken off the collector of Q11. This pulse is of variable width, depending on when a horizontal pulse arrives after the 4 x TW pulse. The output pulse is differentiated by R72 and C31 and applied to emitter follower Q3.



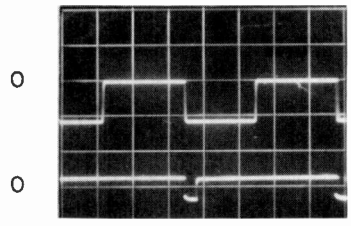
A. Top: Junc. R48, R49, C39, R43, delayed keying pulses, 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



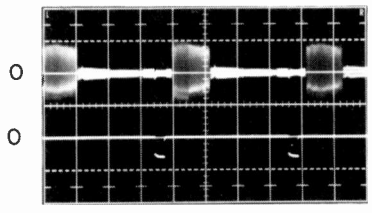
B. Top: P1-17, head #1 FM, 1 ms/cm, .2v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



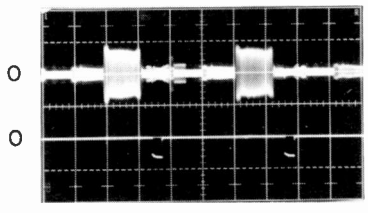
C. Top: P1-18, head #3 FM, 1 ms/cm, .2v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



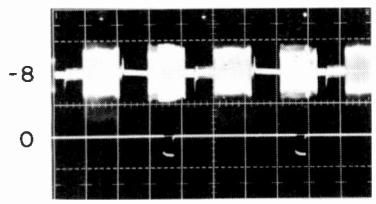
D. Top: Junc. R5, R6, C18, R42, Keying pulses 1 ms/cm, 5v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



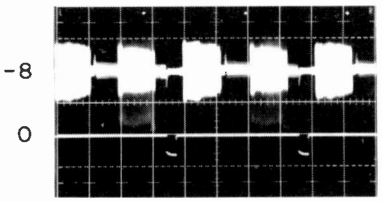
E. Top: P1-19, head #2 FM, 1 ms/cm, .2v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



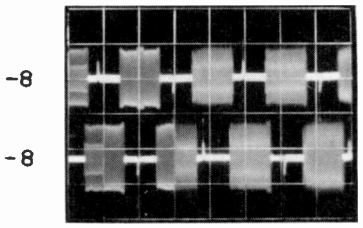
F. Top: P1-20, head #4 FM, 1 ms/cm, .2v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm



G. Top: Q17 emitter, 1 ms/cm, .2v/cm
Bottom: P1-28 tone wheel pulse, 1 ms/cm, 5v/cm



H. Top: Q9 emitter, 1 ms/cm, .2v/cm
Bottom: P1-28 tone wheel pulse, 1 ms/cm, 5v/cm



I. Top: Q17 emitter, 1 ms/cm, .2v/cm
Bottom: Q9 emitter, 1 ms/cm, .2v/cm

Figure 15—Typical Waveforms, First Gating Stage, 4X2 Channel Switching and Emitter Follower Circuits

The positive spike from the emitter of Q3 is fed through steering diodes to both sides of the binary divider, Q1, Q2 (see figure 16) which supplies the keying pulses to the quads. Each positive trigger causes the multivibrator to change state, resulting in a ÷2 action taking place. Diodes CR9 and CR13 serve as gates that conduct alternately so that the input trigger is applied first to one side cutting it off and then to the other side. To prevent phase ambiguity and to maintain the correct phase relationship so that the gate for channel 1 causes quad Z2 to conduct, the differentiated positive spike of the tonewheel pulse (240/250 cps) is fed to one side (Q1) of the multivibrator to insure it is turned off during head no. 1 interval. Phasing is established at the beginning of the cycle so the multivibrator remains correctly phased thereafter. The output of the ÷2 multivibrator is a 2 x TW rate pulse (480/500 cps) which is taken off the collector of Q2 and applied through Z3 to the input of the amplifier stages (see figure 18). A pair of back-to-back diodes, Z3 clips the pulse before it enters the amplifier.

Switching Pulse Suppressor

The switching pulse suppressor circuit shown in figure 20 is used to produce a 3.2 microseconds clamp pulse which operates at the 4XTW rate to suppress the switching pulses that occur every sixteen lines. This signal is timed to occur on the tip of sync and is fed to the sync separator in the demodulator output module A18.

The tonewheel rate square wave signal derived from multivibrator Q10, Q11 is connected to the inverter amplifier Q40. This in turn drives a pulse narrowing circuit composed of C61, R124 differentiator which is coupled to the base of Q41. The tran-

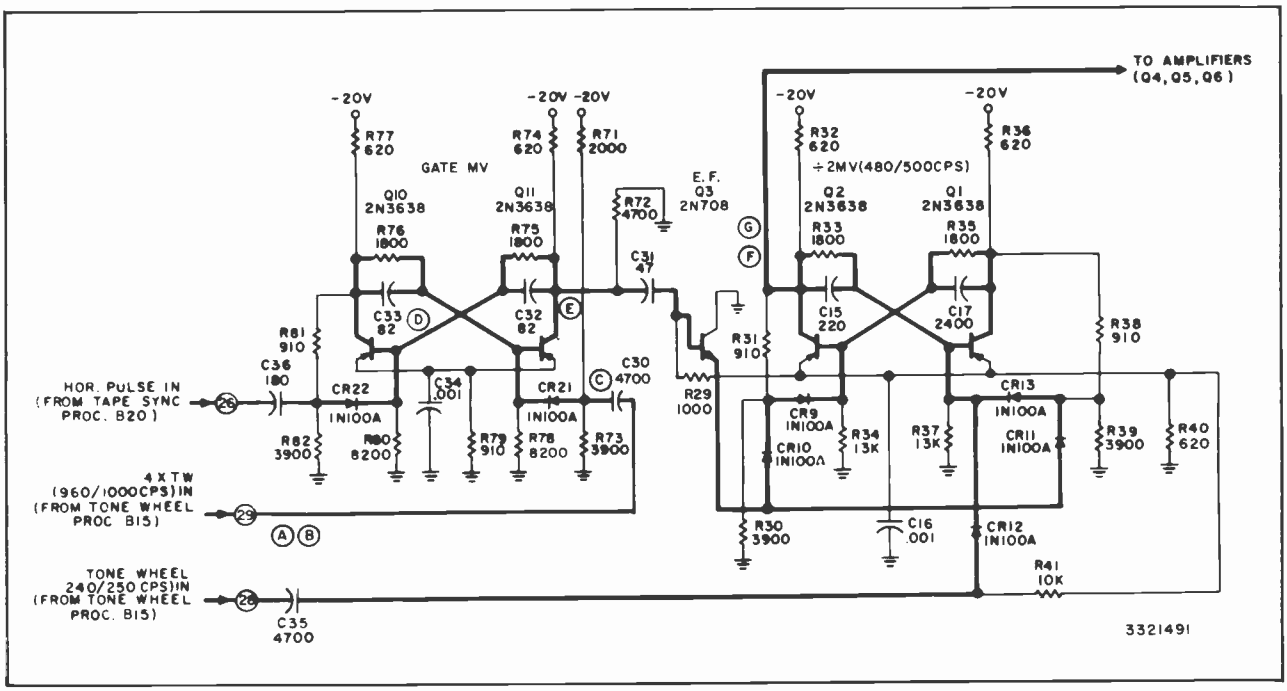
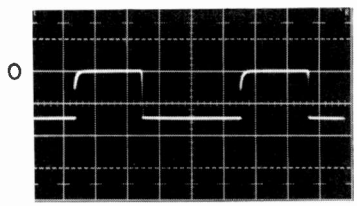
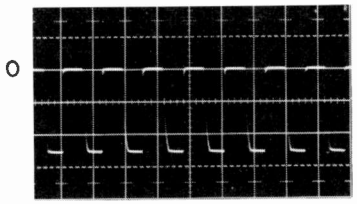


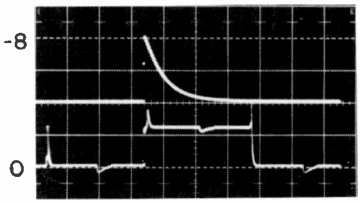
Figure 16—Gate Multivibrator and ÷2 MV Circuits



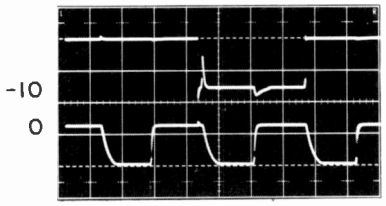
A. P1-29, 4XTW, 200 μs/cm, 5v/cm



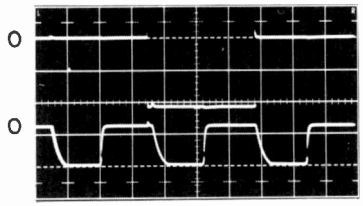
B. P1-26, hor. pulse, 50 μs/cm, 5v/cm



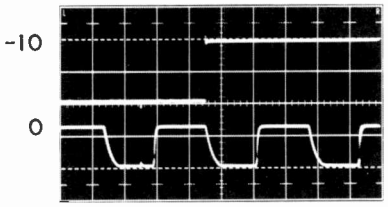
C. Top: CR21 anode, 20 μs/cm, .2v/cm
Bottom: CR22 anode, 20 μs/cm, .2v/cm



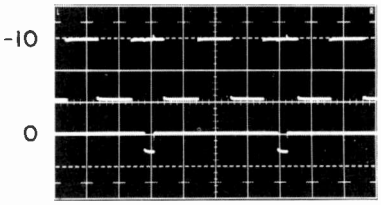
D. Top: Q10 base, 20 μs/cm, 1v/cm
Bottom: P1-26, hor. pulse, 20 μs/cm, 10v/cm



E. Top: Q11 collector, 20 μs/cm, 2v/cm
Bottom: P1-26, hor. pulse, 20 μs/cm, 10v/cm



F. Top: Q2 collector, 20 μs/cm, 2v/cm
Bottom: P1-26, hor. pulse, 20 μs/cm, 10v/cm



G. Top: Q2 collector, 1 ms/cm, 2v/cm
Bottom: P1-28, tone wheel pulse, 1 ms/cm, 5v/cm

Figure 17—Typical Waveforms, Gate Multivibrator and ÷2 MV Circuits

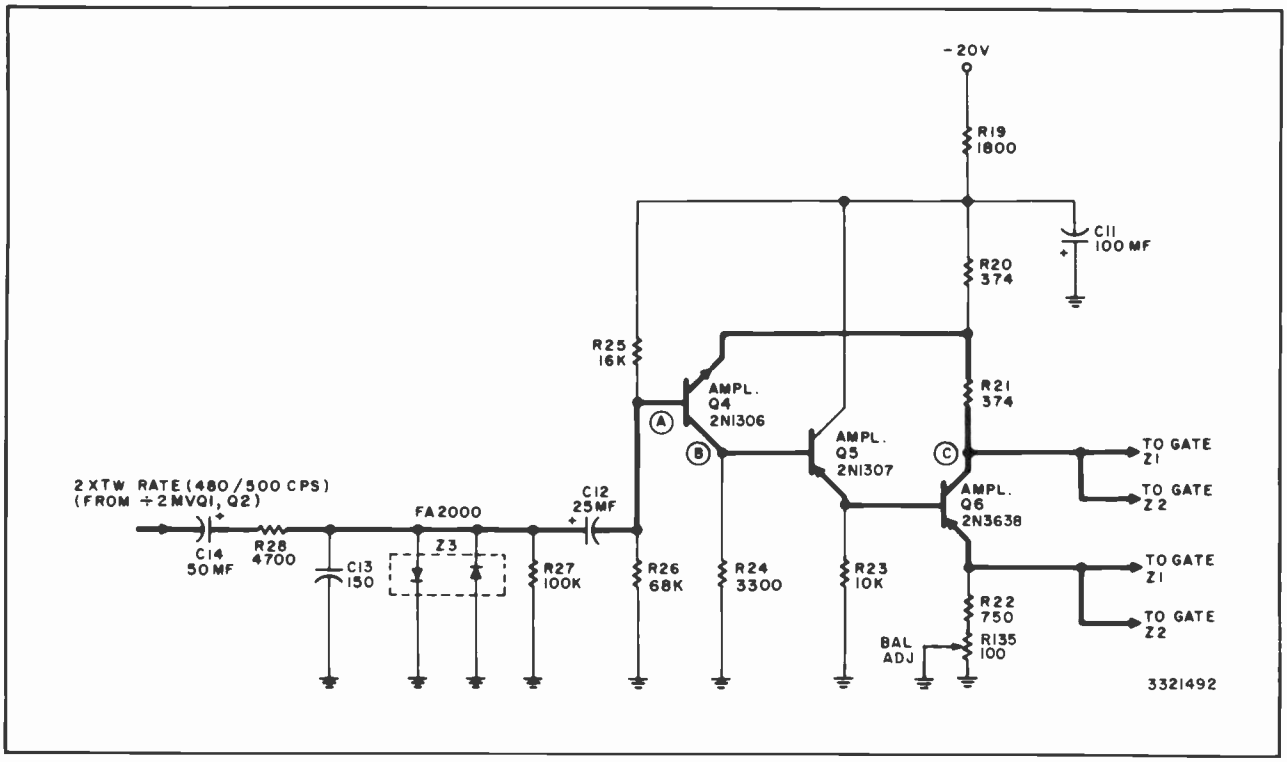
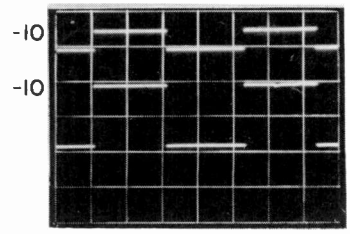
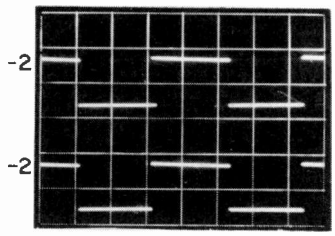


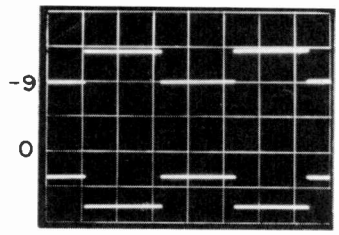
Figure 18—2XTW Rate Amplifier Circuits



A. Top: Q4 base, .5 ms/cm, 2v/cm
Bottom: Q2 collector reference



B. Top: Q4 collector, .5 ms/cm, 2v/cm
Bottom: Q5 emitter, .5 ms/cm, 2v/cm



C. Top: Q6 collector, .5 ms/cm, 2v/cm
Bottom: Q6 emitter, .5 ms/cm, 2v/cm

Figure 19—Typical Waveforms, 2XTW Rate Amplifier Circuits

sistor Q41 (boxcar) narrows the pulse to 0.5 microsecond at its collector, and is timed with the leading edge of tape sync. The positive going pulse at the base of Q42 triggers the monostable (4XTW) rate multivibrator which produces a 3.2 microsecond pulse which is fed to Q44, an emitter follower used to isolate the multivibrator from the load. This emitter follower provides a positive going clamp pulse with its leading edge timed to coincide with the leading edge of sync which appears at the base of Q23 in the sync separator of demodulator output module A18. This has the effect of "pushing out" the switching pulses that occur at the 16 line rate in the demodulator output.

The need for this switching pulse suppression arises in the use of monochrome automatic timing correction (MATC) to prevent switching pulses causing improper timing information.

Quad Keying, 2 x 1 Switching and FM Output

The amplifier stage consists of Q4, Q5, and Q6 which forms a feedback amplifier to provide drive for the two quads, Z1 and Z2. Two pulse outputs are taken from Q6, one from the emitter, the other from the collector. Each pulse output is fed to both quads (see figure 24), driving them in phase opposition so that when one quad is conducting the other is non-conducting. This back-and-forth switching action between the quads results in the two separate inputs being combined into a single continuous FM output. This signal is coupled through C8 to the base of Q8, an FM amplifier. The amplified output on the

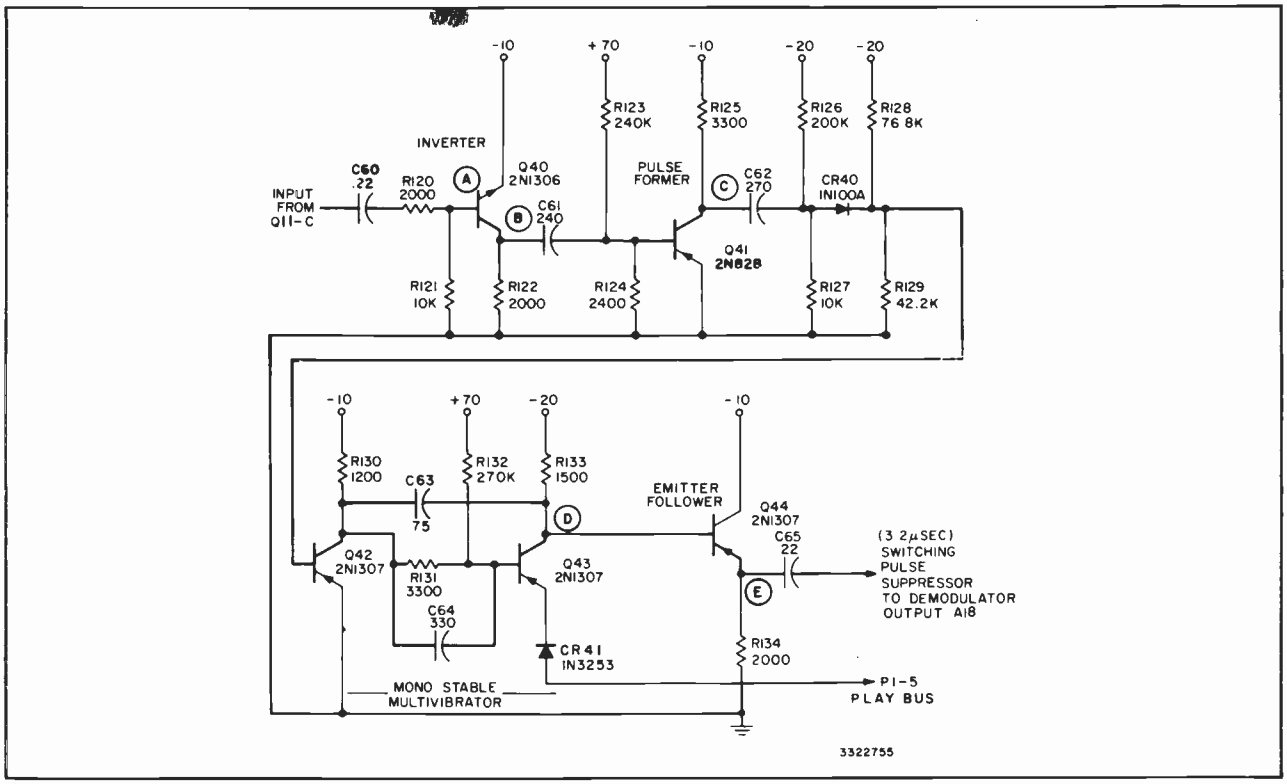
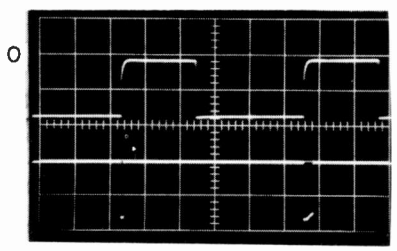
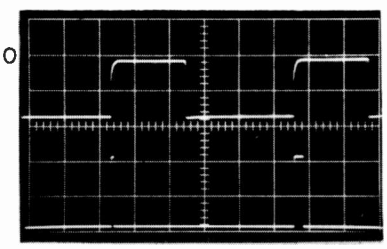


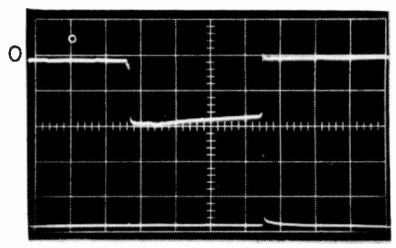
Figure 20—Sync Tip Switching Suppressor Circuits



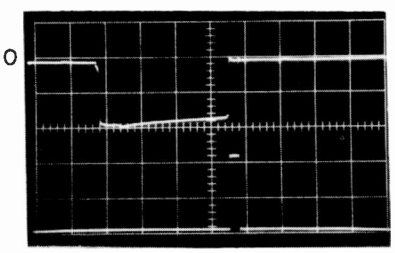
A. Top: Pin 29 of P1, 200 μs/cm, 5v/cm. Bottom: Q40 base, 200 μs/cm, 1v/cm



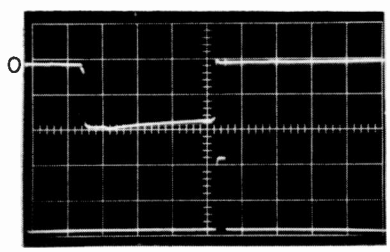
B. Top: Pin 29 of P1, 200 μs/cm, 5v/cm. Bottom: Q40 collector, 200 μs/cm, 5v/cm



C. Top: Q40 base, 10 μs/cm, 1v/cm. Bottom: Q41 collector, 10 μs/cm, 5v/cm



D. Top: Q40 base, 10 μs/cm, 5v/cm. Bottom: Q43 collector, 10 μs/cm, 5v/cm



E. Top: Q40 base, 10 μs/cm, 5v/cm. Bottom: Q44 emitter, 10 μs/cm, 2v/cm

Figure 21—Typical Waveforms, Switching Suppressor Circuits

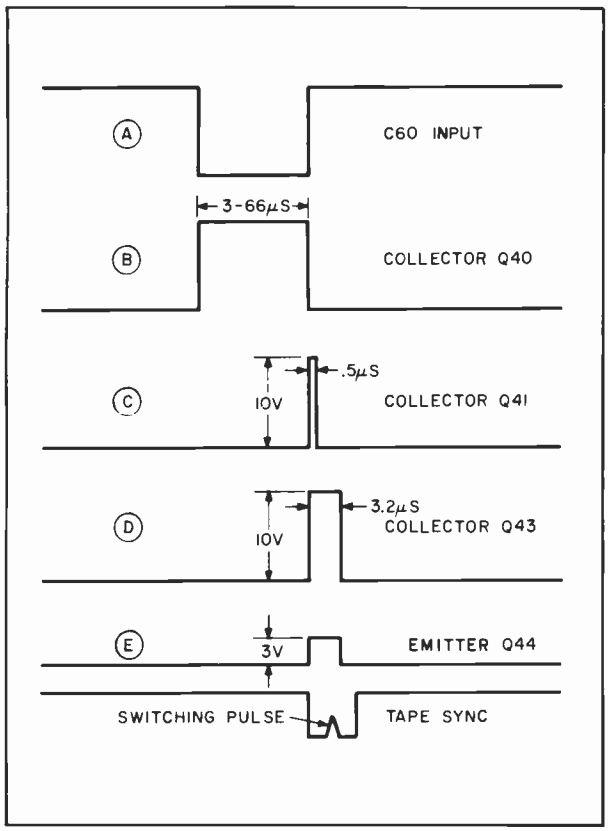


Figure 22—Timing Diagram for Sync Tip Switching Pulse Suppressor

collector of Q8 is direct coupled to the base of Q7, an emitter follower which serves as the FM output stage. The output on the emitter of Q7 is sending-end terminated by R91 and coupled through C9 to the high pass filter composed of L1, L2, L3 and C66 through C71. This filter cleans up switching transients in the output of the switcher which feeds into the input stage of the FM equalizer circuit on the Video/FM Control module A21.

When the TR-4 is in the Record or Setup modes of operation, the FM output of the quads is turned off. The circuit that controls the on-off state of the quad output is comprised of C40, CR7, and R87 in conjunction with R86. In the Record or Setup modes, +70 volts is switched on in the Regulator (module C20) and this positive voltage is applied across R87 as forward bias to CR7. This potential is sufficiently positive to offset the reverse bias applied to CR7 by the negative voltage appearing across R86 which is returned to −20 volts. Under these conditions, CR7 conducts and any output from the quads passes to ac ground through the path provided by C40.

When the TR-4 is in the Play mode, the +70 volts is switched off and CR7 will be cut off due to the reverse bias being applied to it across R86. Thus in this mode, the playback FM output of the quads will be coupled through C8 to the FM amplifier, Q8.

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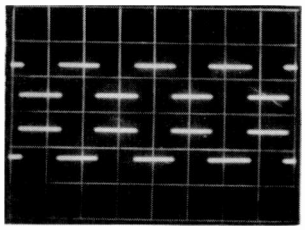
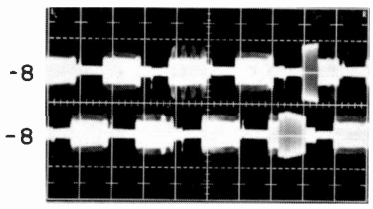
Under *Limiter Module A16,* delete all text, schematics, and waveforms pertaining to this module. This circuitry is covered by the new Demodulator module A17 description covered in this book.

IB-31818, Page 71

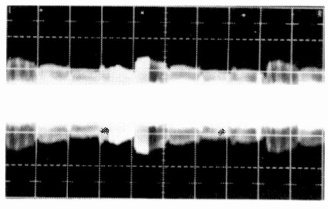
Under *Demodulator Module A17,* delete all text, schematics, and waveforms. In place of the deleted material, use the following:



A. Top: Q6 collector, 1 ms/cm, 2v/cm,
Bottom: Q6 emitter, 1 ms/cm, 2v/cm



B. Top: Q9 emitter, 1 ms/cm, .5v/cm
Bottom: Q17 emitter, 1 ms/cm, .5v/cm



C. TP1, FM output, 1 ms/cm, .2v/cm

Figure 23—Typical Waveforms, Second Gating Stage, 2X1 Switching and FM Output Circuits

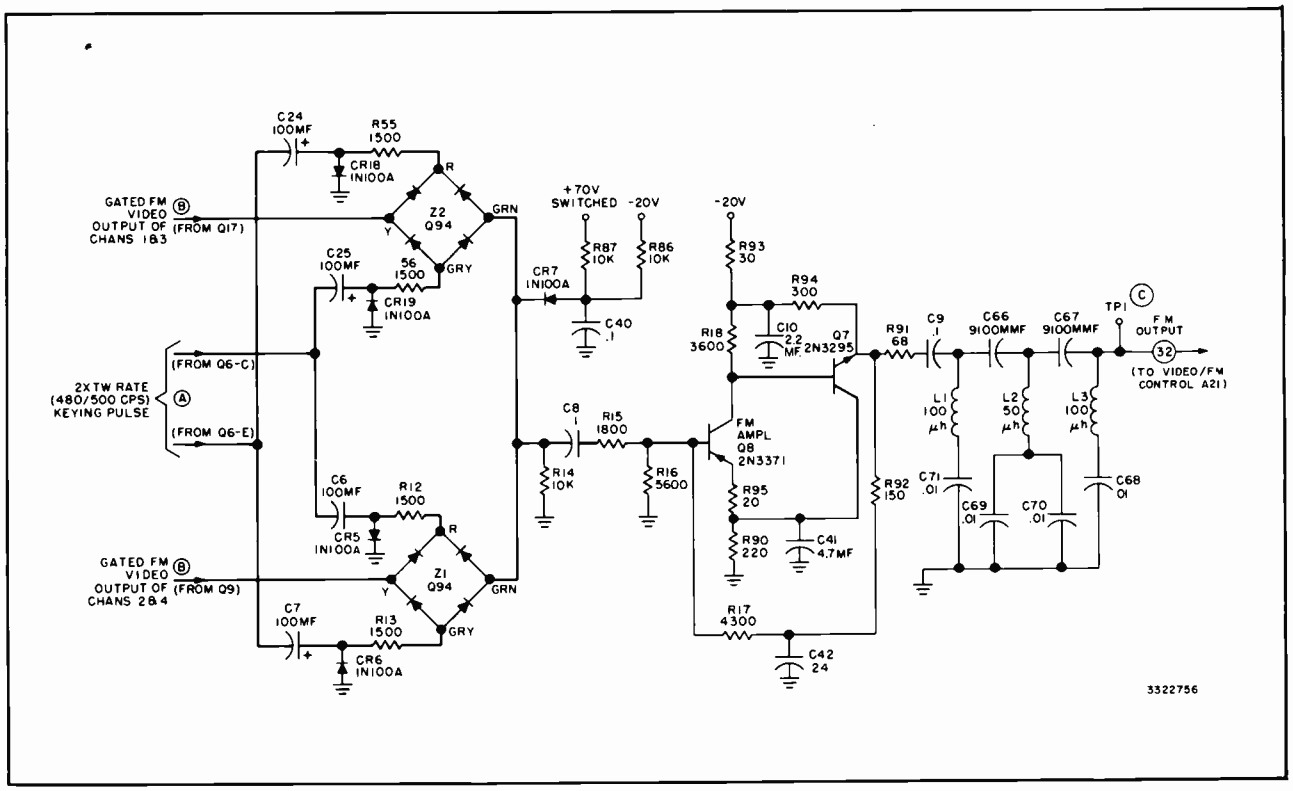


Figure 24—Second Gating Stage, 2X1 Switching and FM Output Circuits

DEMODULATOR Model A17

General

The Demodulator module A17 amplifies and limits the FM input signal, then detects the video information contained in the limited FM. In the TR-4, the input is either the record FM signal from the Modulator module A2 or the tape FM (playback) signal from the FM equalizer circuit in the Video/FM Control module A21.

As shown in the block diagram, figure 25, the incoming FM signal passes through the input signal selection circuit consisting of relays K1 and K2. Relay K2 remains as shown, but relay K1 changes states to accept the appropriate signal according to the mode of operation.

The signal is then fed to the first of four identical limiters. Each limiter is a differential amplifier, with each half of the amplifier coupled by an emitter follower to the succeeding stage. The gain is approximately 15 db per stage, with overall limiting of at least 55 db for a 1 volt intput. To ensure symmetrical clipping, a balance potentiometer is connected across the output of each of the first three differential amplifiers.

The push-pull output of the fourth and final limiter is fed to a phase combiner. The output of the phase combiner is a single phase signal which is fed to an emitter follower. The output of the latter is split into two paths.

In one the signal is coupled through an emitter follower to the R-F Copy line driver. When the R-F Copy switch is in the ON position, the output of this stage becomes available at the R-F Copy Out connector, 6J6 for re-recording. The signal in the second path is fed to the demodulator driver. The limited FM output of this stage is coupled through an emitter follower to the demodulator circuits.

The output from the emitter follower is split into two branches. The signal in both branches is fed to similar pairs of phase splitters. Except for the phase shift encountered by the delayed signal, both signals are identical when applied to their respective phase splitters. The output signal from each of the four phase splitters is coupled through an individual discriminator driver to form the gating input to the diode discriminator.

The configuration of the discriminator is such that each diode will conduct, in turn, during the time a delayed and an undelayed signal are both positive. Since two positive signals, one delayed, the other undelayed, are required for a diode to conduct, the output of the discriminator will be a series of constant-width positive pulse at twice the frequency of the

input signals. However, the interval between the output pulses is inversely proportional to the frequency of the gating signals. Thus as the frequency of the gating signals increases, the interval between the output pulses becomes smaller, causing the average energy content to become increasingly positive. Conversely, as the frequency of the gating signals decreases, the interval between the pulses becomes greater and their average contents becomes less positive. The pulse output of the discriminator is fed through a buffer stage to either of two emitter followers, which serve as drivers for two separate filters.

Only one filter channel is used at a time. The channel in use is determined by the TV line standards on which the TR-4 is being operated. The filter in channel one meets the frequency requirements for domestic standards. The filter in channel two is used for operation on international standards, and is designed to pass frequencies of a slightly higher order than those encountered on domestic standards. Fil-

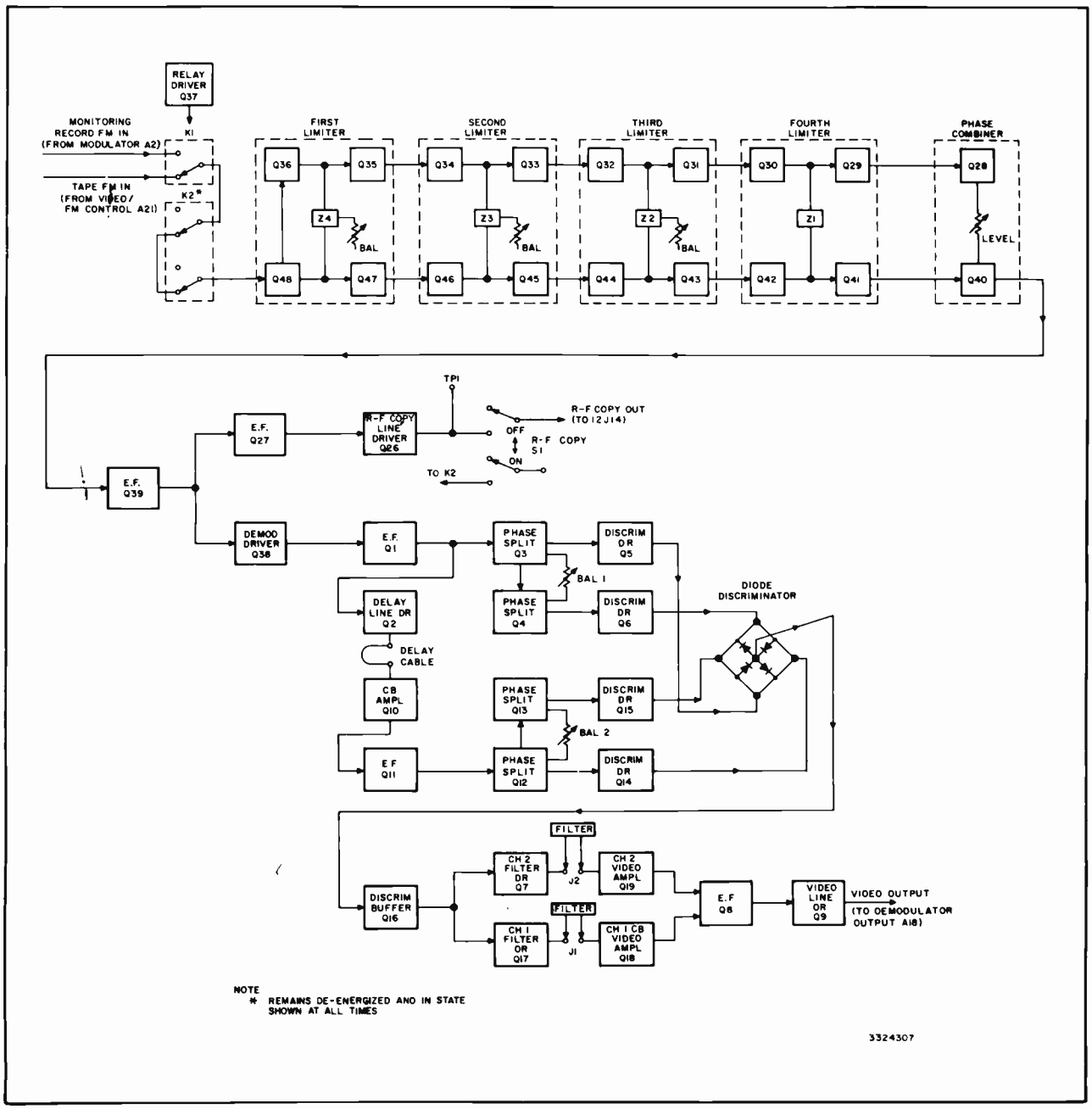


Figure 25—Block Diagram, Demodulator Module

tering removes unwanted residual high frequency components, supplying a signal at the output that is a varying dc average of the pulse input. Since the dc variations in the filtered signal are proportional to the frequency of the input pulses, the output signal is a replica of the original video modulating signal.

The output of the appropriate filter is fed to its respective video amplifier. The amplified output is then coupled by an emitter follower to the video line driver, which feeds the line to the Demodulator Output module A18.

NOTE: The two main functions performed by the Demodulator module, limiting and detection, are virtually independent of each other. Therefore each of these circuit areas will be considered separately in the following discussion.

NOTE: The typical waveforms of the Demodulator circuit, shown in figures 28, 32, 34, 36, 39, and 41, were taken on a TR-4 in the E-E or back-to-back mode of operation. The series of waveforms in figures 28, 32, 34, and 36 are of the unmodulated FM carrier. They were obtained with the Video Input (module A1) removed from the recorder system. For the last two illustrations, figures 39 and 41, the Video Input module A1 was replaced in the recorder system to show modulation. The modulated carrier appears in figure 39A and the subsequently detected video is shown in figures 39B and 41.

Circuit—Limiter Section

Input Signal Selection

The function of K1 (figure 26) is to select either the record FM signal or the tape FM signal from the playback circuits. When the TR-4 is in the RECORD or SETUP mode of operation, K1 selects record FM; in the PLAY mode, K1 selects tape FM. If the TR-4 is in STANDBY, WIND, or SETUP modes, K1 will select either record FM or the zero signal output of the video heads. The choice between these two signals is determined by the position of the MOD-PLAY switch, which is an internal control on the Modulator module A2. For a detailed discussion on the operation of this switch, see sections entitled *−20 Volts Electronic Switch* and *MOD-PLAY Switch* under *Modulator (module A2)* description in *IB-31818*.

Relay K2 is not connected to any source of power, therefore remains de-energized at all times. Relay K2 serves merely to feed the signal selected by K1 to the first stage of limiting.

With the input selection relay, K1 and relay K2, de-energized, as shown in figure 26, K1 would accept the Tape FM signal from the Video/FM Control module that appears on pin 18 of the Demodulator connector P1. The signal would go through K1 to

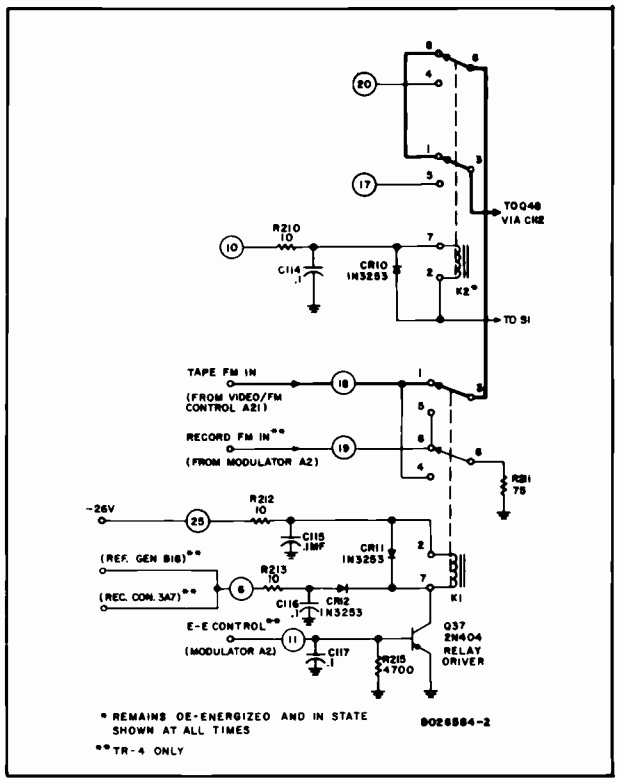


Figure 26—Input Signal Selection

K2 and would follow the path through the jumpered contacts on K2 to the base of Q48, the input of the first limiter.

When K1 is energized, the Record FM signal from the Modulator module is applied to K1 through pin 19 on the Demodulator connector P1. From K1 the signal goes through the still-closed loop provided by K2 to the base of Q48.

Regardless of the state of K1, the coaxial input lines are properly terminated at all times by R211 (figure 26) and by R203 (figure 27). The former terminates the unused signal input line to K1 and the latter provides input termination of the signal being applied to the base of Q48, the input of the first limiter.

The input selection relay, K1, is controlled by the relay driver, Q37, or the RECORD/SETUP bus. In the STANDBY, WIND or STOP modes with the MOD-PLAY switch (located in Module A2) in the MOD position, negative voltage from the E-to-E bus saturates Q37, driving the collector to ground. This energizes K1 which switches to the Record FM input. In the RECORD or SETUP modes, the RECORD/SETUP bus is grounded and this supplies the ground return to the coil of K1 through CR12. Again K1 is energized and switches to the Record FM input signal.

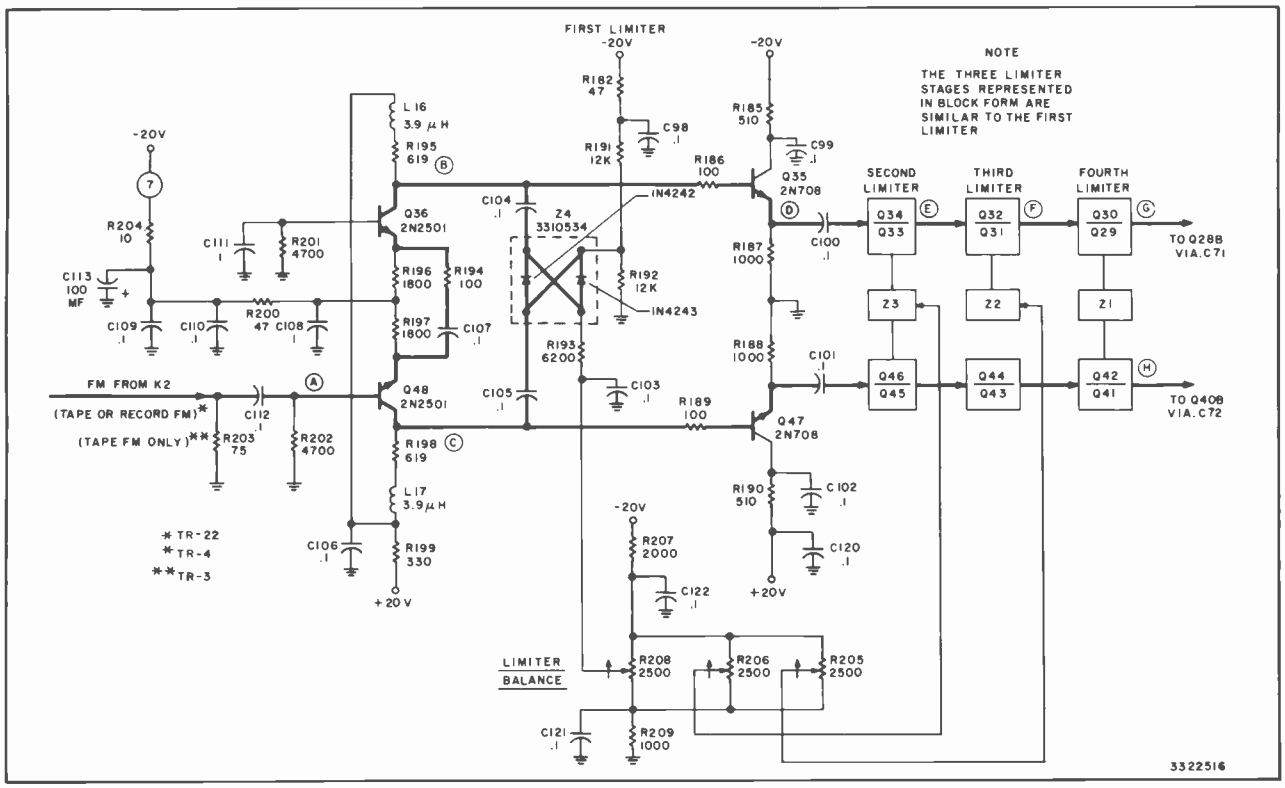
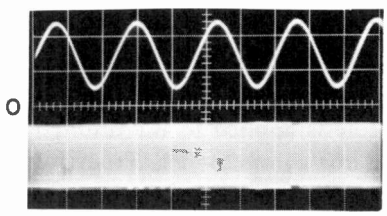
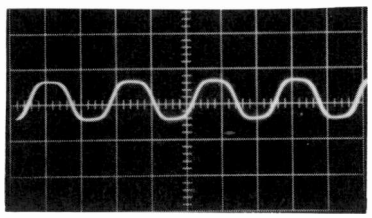


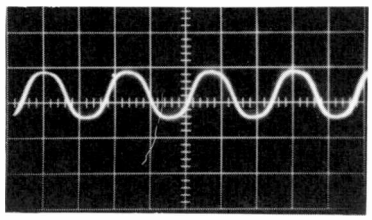
Figure 27—Amplifier and Clipper Circuits



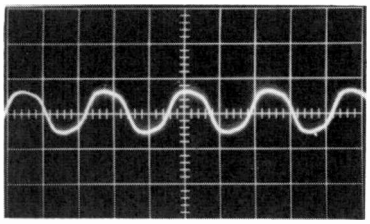
A. Top: Q48 base, .1 μs/cm, .2v/cm



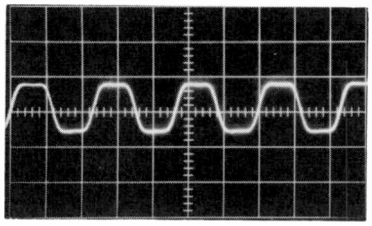
B. Q36 collector, .1 μs/cm, .5v/cm



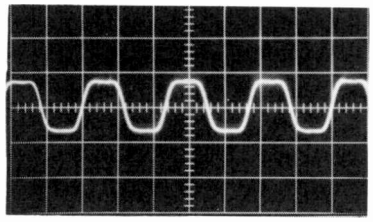
C. Q48 collector, .1 μs/cm, .5v/cm



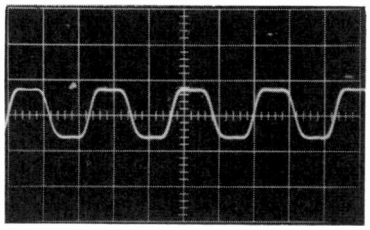
D. Q35 emitter (Q47 emitter inverted) .1 μs/cm .5v/cm



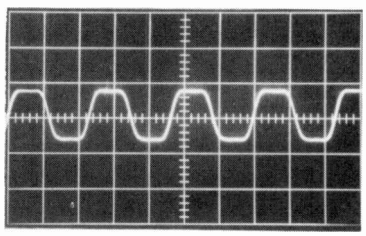
E. Q33 emitter (Q45 emitter inverted) .1 μs/cm, .5v/cm



F. Q31 emitter(Q43 emitter inverted) .1 μs/cm, .5v/cm



G. Q29 emitter, .1 μs/cm, .5v/cm



H. Q41 emitter, .1 μs/cm, .5v/cm

Figure 28—Typical Waveforms, Amplifier and Clipper Circuits

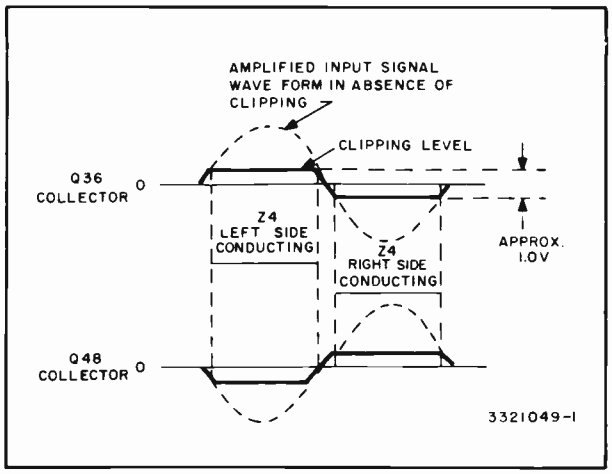


Figure 29—Waveforms Showing Conduction Cycle of First Limiter Diodes

Limiters

Since the four limiter stages are similar, with the exception of the balance potentiometer in the collectors of the first three limiters, only the first will be covered in the following discussion (see figure 27).

Transistors Q36 and Q48 form the two halves of a push-pull stage generally known as a differential or emitter coupled amplifier. As mentioned earlier, the incoming FM signal is coupled through C112 to the base of Q48. The input signal is distributed across both halves of the amplifier by coupling the signal on the emitter of Q48 through C107 and R194 to the emitter of Q36.

The push-pull signals on the collectors of Q36 and Q48 are coupled by C104 and C105 to a pair of back-to-back diodes in Z4, which clips the signals close to their ac axes (see figure 29). Each diode conducts alternately on the half cycles when the amplified input signal causes the collector-to-collector potential to exceed the forward conduction voltage of the diodes, which is approximately 1 volt. When the diodes conduct, the signal swing on each collector is limited and the positive and negative peaks are clipped at approximately 0.5 volt. The clipped output from each half of the first limiter is coupled to the succeeding limiter stage through emitter followers, with Q36 driving Q35 and Q48 driving Q47. In the remaining three limiter stages, the signal is further amplified and clipped, with clipping again taking place at the 0.5 volt level.

There is a BALANCE potentiometer connected through a series resistor to each of the limiter diodes in the first three limiter circuits (figure 27). The first potentiometer, R208, is a front panel screwdriver adjustment. The other two potentiometers, R206 and R205, are internal controls. These controls are used to set the bias between both halves of their respective amplifiers to establish symmetrical clipping of the amplifier output signal. Considering the first limter as typical, when the input signal is symmetrical, the setting of BALANCE control R208 is such that the dc bias at the junction of R193 and the anodes of Z4 is equal to the dc bias at the junction of R191 and the cathodes of Z4. Should the input signal be asymmetrical (A, figure 30), the BAL-

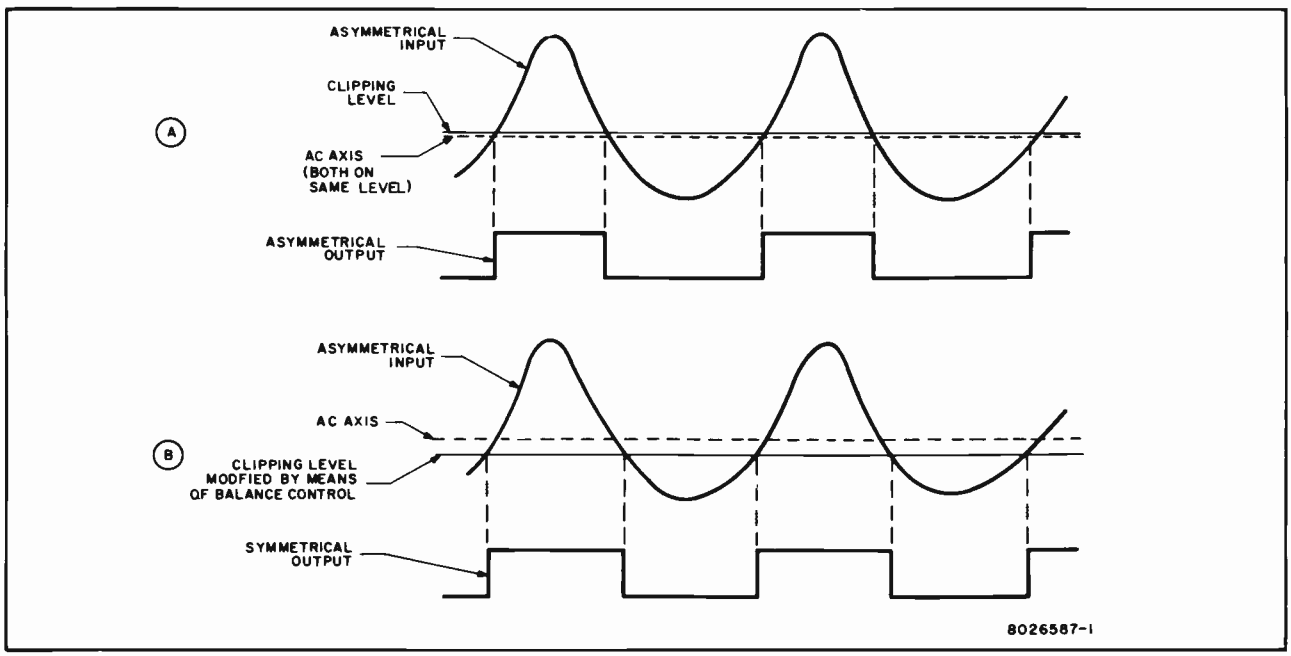


Figure 30—Balance Control Operation

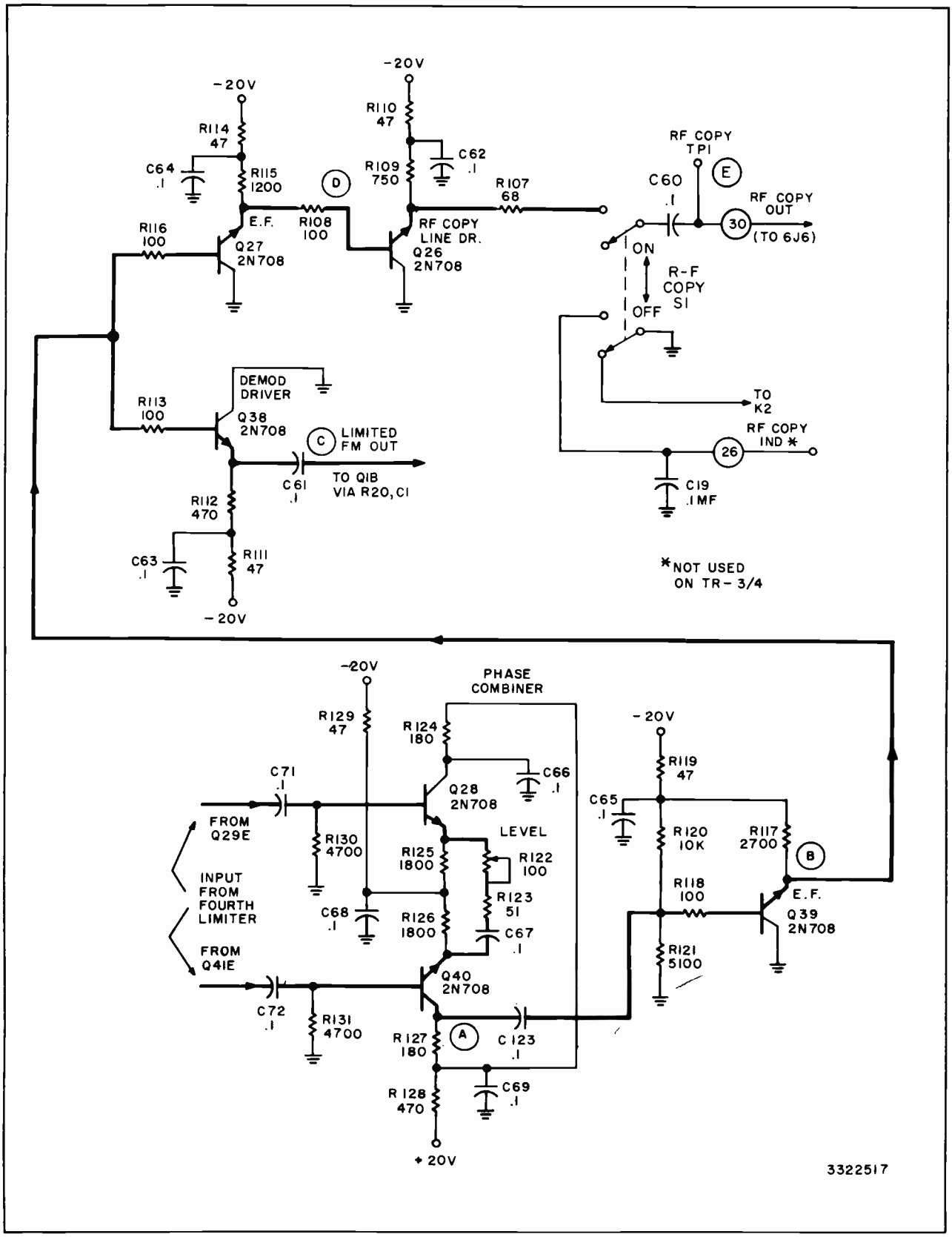


Figure 31—Phase Combiner, RF Copy, and Demodulator Driver Circuits

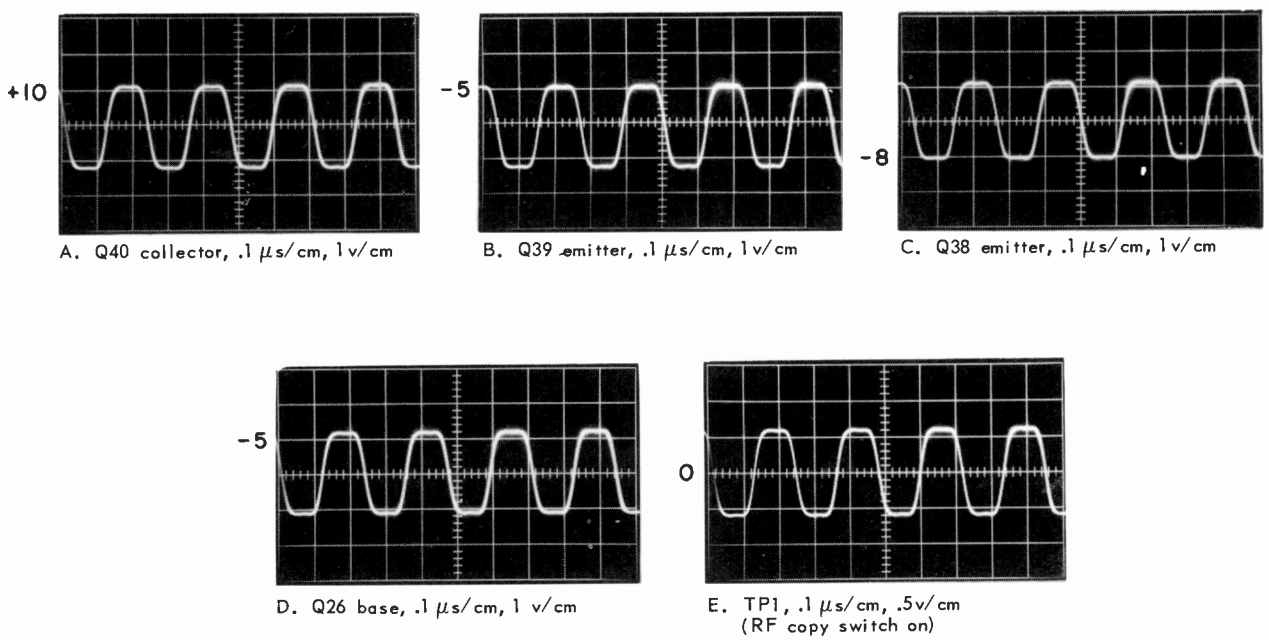
ANCE control can be adjusted to change the bias on Z4. This will effect a shift in the relation between the ac axes of the signal with respect to the clipping level, thus provide a symmetrical output as shown in B, figure 30. Symmetrical output is necessary in order to detect the video properly, later on during the demodulation process. The procedure for setting the BALANCE controls is given under *Adjustments*. The push-pull output of the fourth limiter is fed to the phase combiner, Q28, Q40.

Phase Combiner, Demodulator and R-F Copy Line Drivers

The input signal to the phase combiner, Q28, Q40 (figure 31) is applied to the base of each of these transistors. The signal on the base of Q28 is coupled through C71 from the emitter of Q29 and the signal on the base of Q40 is coupled through C72 from the emitter of Q41. Although at any instant the signal on the base of Q28 is opposite in phase to that on the base of Q40, phase reversal between the input and output to each half of the phase combiner takes place only in Q40. The emitters of these two transistors are coupled together by the LEVEL control, R122, R123, and C67, and the output is taken off the collector of Q40. With this configuration, the signal on the emitter of Q28 is effectively added to the signal on the collector of Q40 to produce a combined single phase output. The LEVEL potentiometer, an internal control, is set to provide a 2-volt peak-to-peak signal at the input to the demodulator circuit. This control is normally not disturbed and may only require adjustment if the limiter balance has to be re-established.

The output on the collector of Q40 is coupled through C123 to the base of Q39, an emitter follower. The output of Q39 is fed simultaneously to two other emitter followers, Q27 and Q38. The input is dc coupled to both transistors through R116 to the base of Q27 and through R113 to the base of Q38. The latter is the demodulator driver, the output of which is coupled through C61 to the input stage of the demodulator circuit.

The output on the emitter of Q27 is dc coupled through R108 to the base of Q26, the R-F copy line driver, also an emitter follower. These two emitter followers form a two stage cascade amplifier to isolate the R-F copy line from the preceding circuits. When S1 is in the R-F COPY position the output impedance of Q26 and 68 ohms series resistance of R107 provide a source impedance of 75 ohms for the output signal. The R-F copy output is available at 6J6, and the signal is nominally 1 volt when the TR-4 is driving a 75-ohm load.



A. Q40 collector, .1 μs/cm, 1 v/cm
B. Q39 emitter, .1 μs/cm, 1 v/cm
C. Q38 emitter, .1 μs/cm, 1 v/cm
D. Q26 base, .1 μs/cm, 1 v/cm
E. TP1, .1 μs/cm, .5 v/cm (RF copy switch on)

Figure 32—Typical Waveforms, Phase Combiner, RF Copy, and Demodulator Driver Circuits

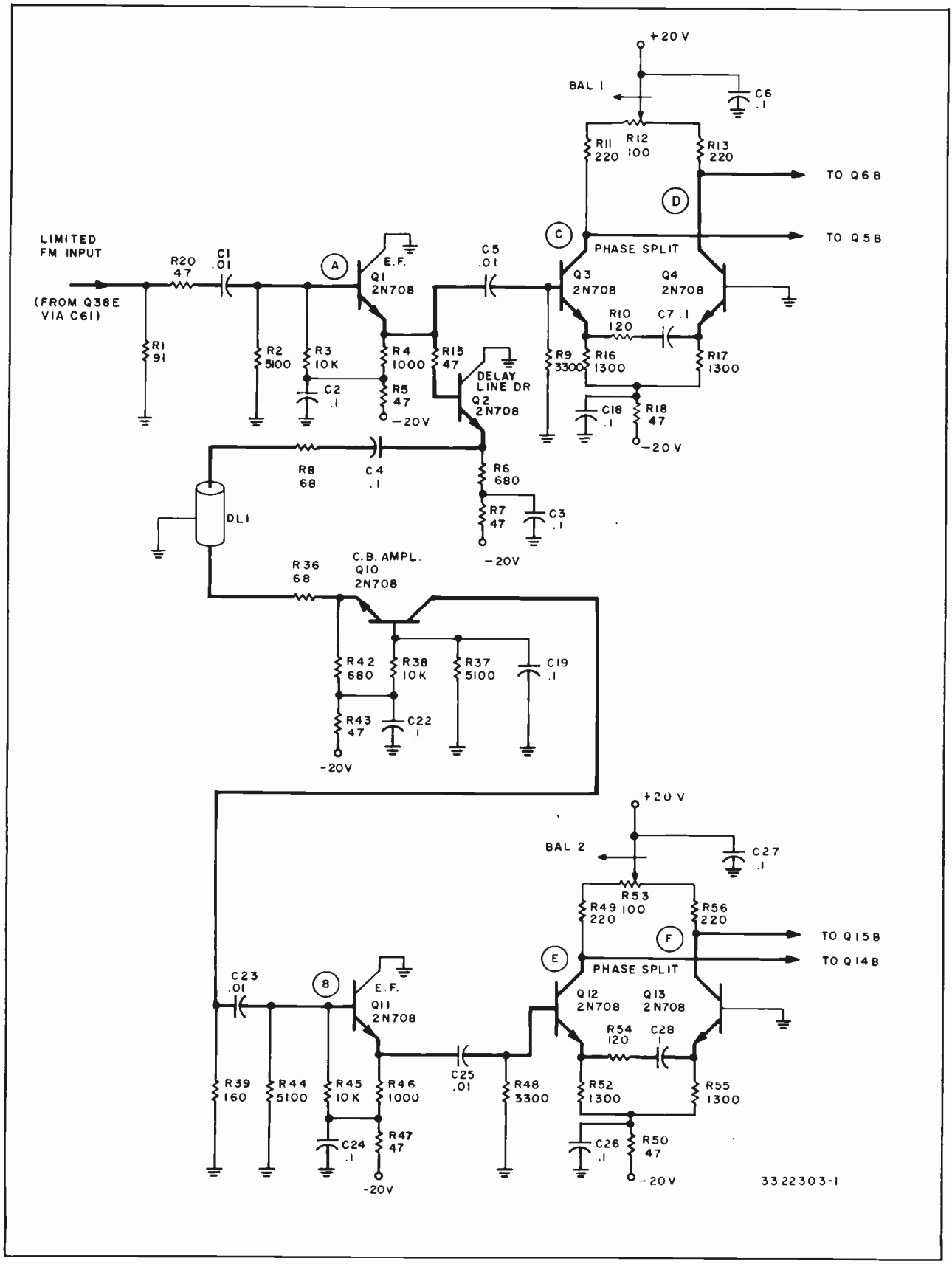


Figure 33—FM Input, Delay, and Phase Splitter Circuits

Circuit—Demodulator Section

Phase Splitters

The incoming FM signal (figure 33) from the limiter circuit is coupled through C1 to the base of Q1, an emitter follower. Two outputs are taken off the emitter of Q1. One is coupled through C5 to the base of Q3, which together with Q4 forms a phase splitter pair. The other output signal is first passed through delay line before being applied to a similar pair of phase splitters, Q12, Q13. The delay is needed in order to obtain properly phased gating signals with which to drive the diode discriminator. (This will be described later.)

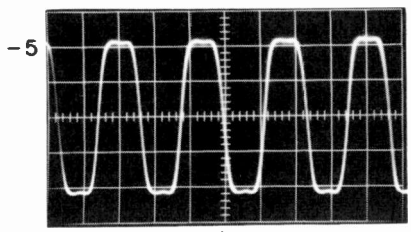
The signal entering the delayed branch from the emitter of Q1 is fed across R15 to the base of Q2, the delay line driver, an emitter follower. From the emitter of Q2, the signal is coupled through C4 and R8, where it enters the delay cable. The latter is of such length as to provide a delay of approximately .03 microseconds. The output of the delay is fed across R36 to the emitter of Q10, a common base amplifier.

Both ends of the delay line are terminated in 75 ohms. At this ending end, 75 ohms is obtained by the 68-ohm resistor R8 in combination with the emitter impedance of Q2. And, similarly, at the receiving end, 75 ohms is obtained by the 68-ohm resistor R36 together with the emitter impedance of Q10.

The loss in level incurred by the signal due to the terminations at the input and the output of the delay cable is recovered by a common base amplifier. The output signal of the collector of Q10, now restored to the same level as that appearing on the base of Q1, is coupled through C23 to the base of Q11, an emitter follower. From the emitter of Q11, the signal is coupled through C25 to the base of Q12, which, in combination with Q13, forms the other phase splitter pair. Other than the phase shift caused by the .03 microseconds delay, the signal appearing on the base of Q12 is the same as the undelayed signal appearing on the base of Q3.

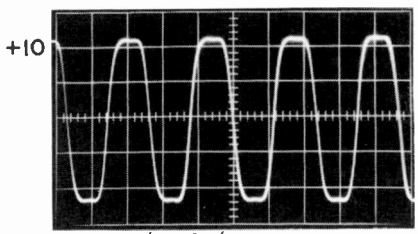
Since the phase splitter circuits in each branch are identical, only one Q3 and Q4, will be discussed. The operation of Q3 and Q4 is similar to that of a differential amplifier. Transistor Q3 is a common emitter amplifier and Q4 is a common base amplifier. The emitters of these two transistors are ac coupled through R10 and C7. With this arrangement, the bias conditions between the two transistors are such that one conducts when the signal is positive and the other conducts when the signal is negative. A positive going signal on the base of Q3 forward biases this transistor causing it to conduct. At this time a replica of the same signal appears on the emitter of Q3, and hence is also present on the emitter of Q4 by virtue of the ac coupling between these two elements. However, since this is a positive going signal, it reverse biases Q4, cutting off the latter. When the signal on the base of Q3 goes negative, the opposite occurs. Transistor Q3 becomes reverse biased and is cut off. Therefore the signal representing reverse bias on the emitter of Q4 is no longer present and this transistor conducts. The resultant outputs, available at the collectors of Q3 and Q4, are two signals 180° out of phase.

Connected in series between load resistors R11 and R13 in the collectors of Q3 and Q4, respectively, is a potentiometer, R12, designated BAL-1. Likewise in the collector circuits of Q12 and Q13 is a similar potentiometer, R53, designated BAL-2.



A. .1 μs/cm, .5v/cm

KEY	LOCATION
A	Q1 base
B	Q11 base



B. .1 μs/cm, 1 v/cm

KEY	LOCATION
C	Q3 collector
D	Q4 collector
E	Q12 collector
F	Q13 collector

Figure 34—Typical Waveforms, FM Input, Delay, and Phase Splitter Circuits

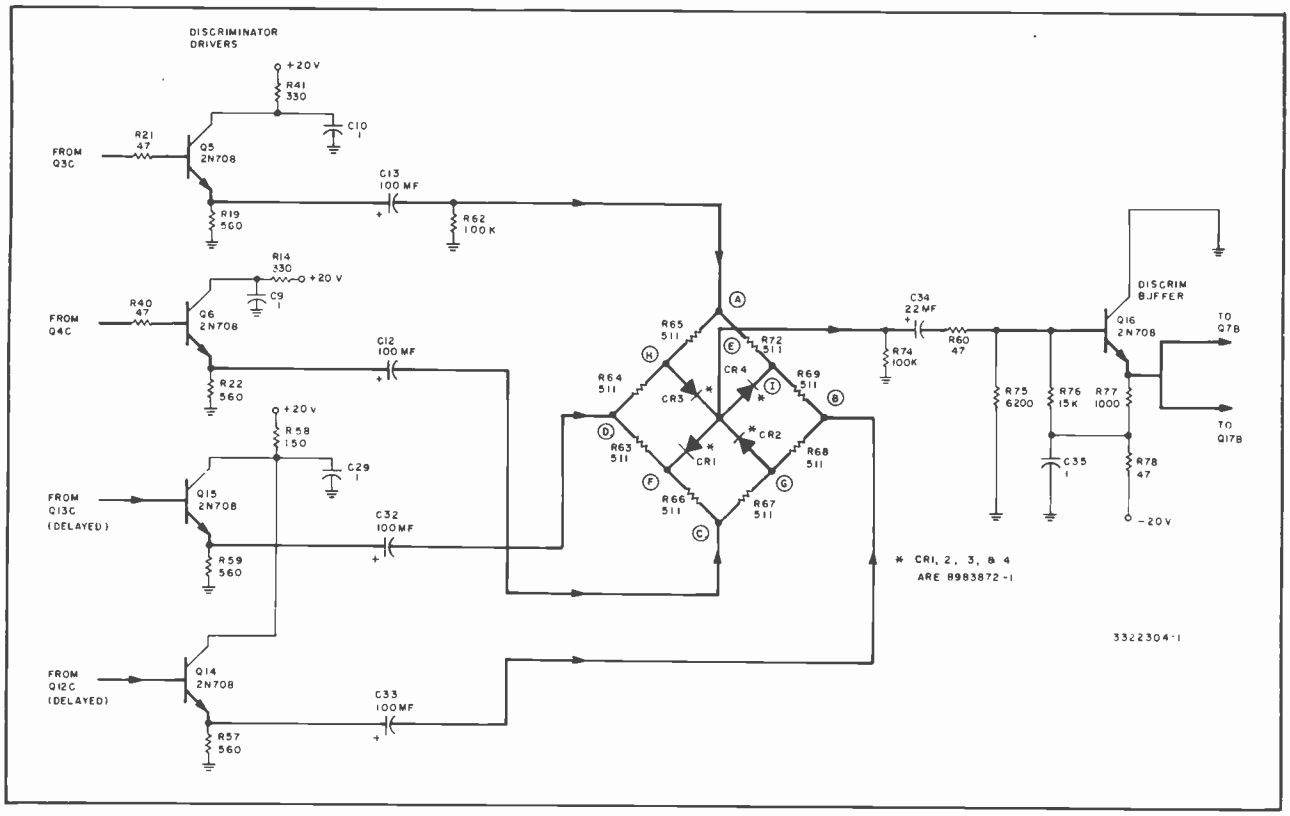
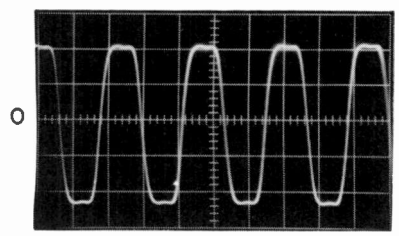
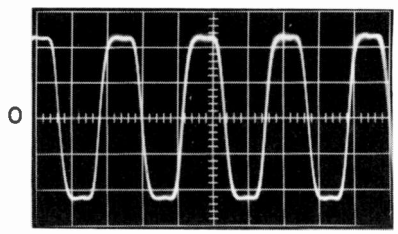


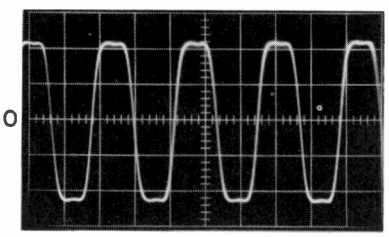
Figure 35—Discriminator Drivers, Diode Discriminator, and Buffer Circuits



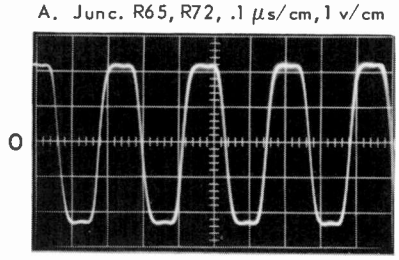
A. Junc. R65, R72, .1 μs/cm, 1 v/cm



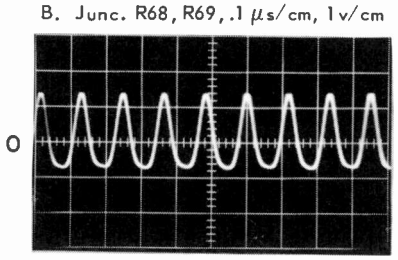
B. Junc. R68, R69, .1 μs/cm, 1 v/cm



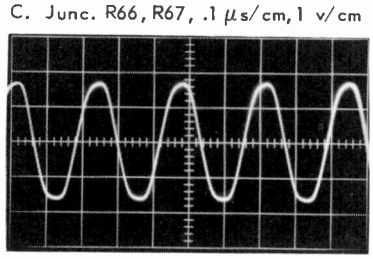
C. Junc. R66, R67, .1 μs/cm, 1 v/cm



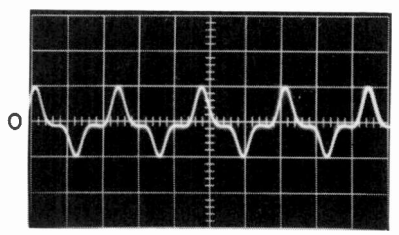
D. Junc. R63, R64, .1 μs/cm, 1 v/cm



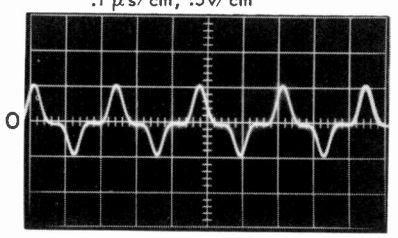
E. Junc. CR1, CR2, CR3, CR4, .1 μs/cm, .5v/cm



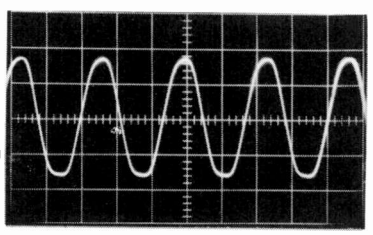
F. CR1 cathode, .1 μs/cm, 1 v/cm



G. CR2 anode, .1 μs/cm, 1 v/cm



H. CR3 anode, .1 μs/cm, 1 v/cm



I. CR4 cathode, .1 μs/cm, 1 v/cm

Figure 36—Typical Waveforms, Discriminator Drivers, Diode Discriminator, and Buffer Circuits

The purpose of these potentiometers is to change the relative load impedance on the collectors of the phase splitters to compensate for differences in the characteristics of the discriminator diodes. Access holes, appropriately labeled, are provided on the front panel of the module to enable either of these potentiometers to be adjusted by inserting a slender screwdriver to turn the preset control. However, these balance potentiometers are not operational controls, therefore they should not be adjusted in the course of normal operation or routine maintenance.

Diode Discriminator

The complementary outputs of the phase splitters in both branches are fed to individual emitter followers which drive the diode discriminator (see figure 35). The output signals on the collectors of Q3 and Q4 are fed through R21 and R40 to the bases of Q5 and Q6, respectively. The purpose of the two resistors is to suppress parasitic oscillations. The delayed output signals on the collectors of Q12 and Q13 are direct coupled to the bases of Q14 and Q15, respectively.

The outputs from the emitter followers are connected to the discriminator network in such a manner that a delayed and an undelayed signal are combined in pairs to form a gating signal at the junction of the two resistors at the input to each diode. The output of the discriminator is a series of fixed-width positive pulses, the frequency of which is twice that of the gating signals.

A graphical analysis of the operation of the diode discriminator network is shown in figure 37. This illustration shows the phase and polarity of the gating signals applied to the diodes, over several cycles of carrier during deviation typical of a frequency modulate signal. The fixed-width positive output pulses are shown below the input pulses. The chart beneath the discriminator output waveform shows the order in which the diodes conduct.

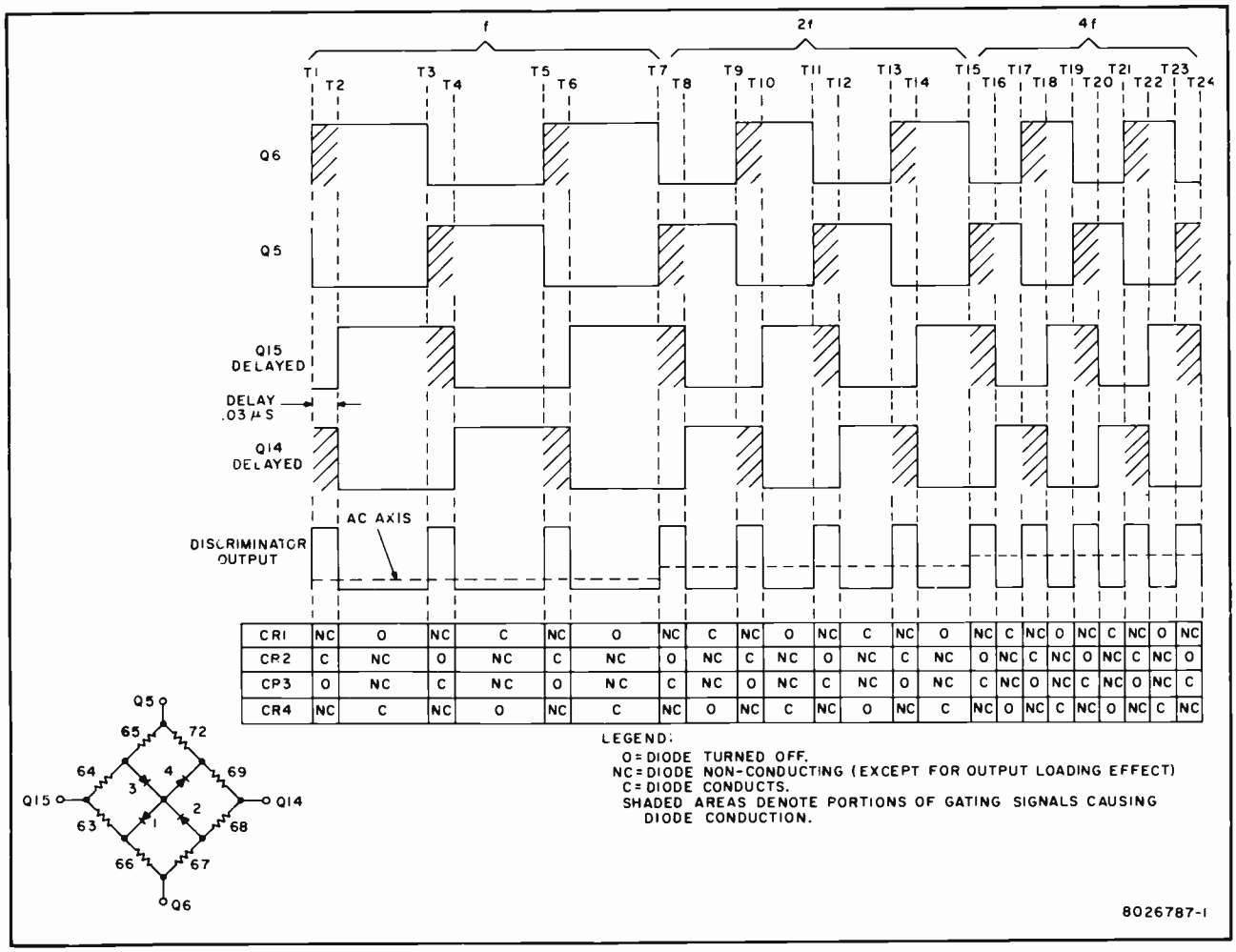


Figure 37—Diode Discriminator Conduction Cycle

Assuming the frequency of the discriminator input signals to be as shown in figure 37 and considering time interval T1 to T2 with all four signals applied across the discriminator, the diodes will conduct in the following manner.

The positive signal from Q6 and the delayed negative signal from Q15 combine at the junction of R63, R66 as the gating signal to CR1. Because these two signals are of opposite polarity, the resultant potential of CR1 is zero, tending to prevent conduction. At the same time, the positive signal from Q6 is also joined with the delayed positive signal from Q14 to form the gating input to CR2 at the junction of R67, R68. Since the polarity of the resultant gating signal is positive, CR2 conducts and a positive pulse appears at the output of the discriminator during interval T1-T2. The gating input to CR3 is formed at the junction of R64, R65 by the negative signal from Q5 and the delayed negative signal from Q15. Since the resultant of these combined signals is also negative, the effect is to turn off CR3. The negative signal from Q5 and delayed positive signal from Q14 combine at the junction of R69, R72 as the gating input to CR4. However, the resultant of these two signals is zero, thus preventing CR4 from conducting.

While CR1 and CR4 do not pass their gate signals since the resultant is zero or ground potential at the junction of the input resistors and the cathodes of these diodes, these are in a quiescent state. This is due to the positive output voltage, which is present at the junction of all four diodes. Therefore this loads the output with the resistors to which the cathodes of CR1 and CR4 are connected.

From time T2 to T3 a similar gating action takes place, with the polarity of the undelayed signals from Q5 and Q6 remaining the same, but with the polarity of the delayed signals from Q14 and Q15 now reversed. During this interval CR1 is cut off; CR2 and CR3 tend to be cut off; but CR4 conducts, transferring its negative gate signal to the output.

The discriminator diodes continue to conduct in this fashion throughout the remaining intervals as the gating signal to each diode assumes the proper polarity.

As can be seen from the lightly shaded areas on the input pulses, positive gating signals occur twice during one alternation of each input cycle, thus the frequency of the discriminator output pulses is twice that of the input wave. Note, also, that as the fre-

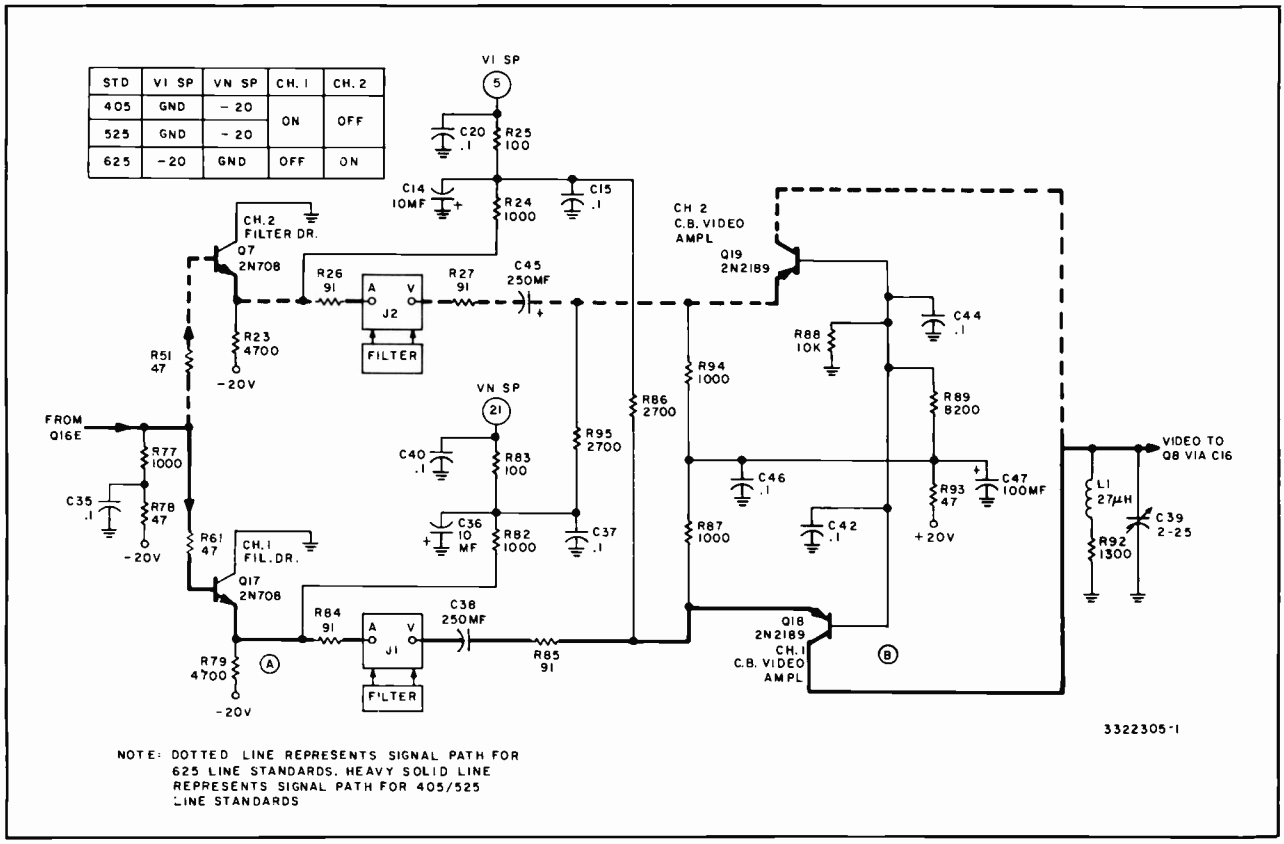


Figure 38—Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits

quency of the output pulses increases, the interval between becomes shorter. However, because the pulse width remains constant, due to the previously established .03 microsecond delay between the input signals, the average output level becomes more positive (greater number of positive pulses per unit of time) as frequency increases.

The pulse output of the discriminator is coupled through C34 and R60 to the base of Q16, an emitter follower (figure 35), which serves as a buffer between the discriminator and the following filter circuits. From the emitter of Q16, the signal is fed to the bases of two filter drivers, Q7 and Q17.

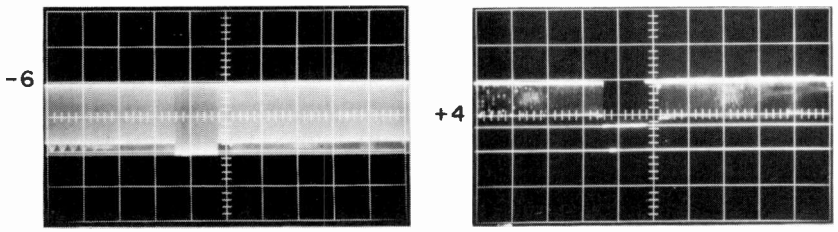
Filtering and Video Recovery

The discriminator output signal contains both unwanted high frequency components of the carrier and the desired video information, as related to the average duty cycle. In order to recover the frequency component representing the original video, this signal must be filtered (see figure 38). Furthermore, two separate filter circuits are necessary to accommodate the bandwidth requirements of the different line rates on domestic and international standards. Only one filter circuit is active, and this is determined by the line rate on which the TR-4 is being operated. If the TR-4 is intended solely for domestic 525-line operation, the Demodulator module is equipped with a 4.2 mc filter plugged on J1 in the channel no. 1 filter circuit. When the TR-4 is for use on international standards, the Demodulator is supplied with a filter in each channel. The filter in J2 in the channel no. 2 filter circuit is 5.0 mc and is employed for 625-line operation. The bandwidth of the 4.2 mc filter is also suitable for 405-line standards; therefore it is retained as the channel no. 1 filter for 405/525-line operation. Selection of the appropriate filter for either 405/525 or 625-line rates is done by means of the VI SP and the VN SP busses. (Just how this is accomplished will be described later.)

The output from the emitter of either filter driver (Q7 or Q17) is applied to the appropriate filter, which is terminated at both ends in 91 ohms. The filter is designed to eliminate all frequencies above the video band, and deliver at the output a varying average dc whose amplitude changes are a function of the video frequency modulated input. The result of this is an output signal that is a replica of the video signal from which the recording was originally made.

As mentioned earlier, the discriminator output frequency is twice that of the input. The purpose of frequency doubling is to facilitate the separation of the video and the carrier components in the filter, since with some standards the spectra of the two signals overlap. In other words, the carrier frequency, which represents the sync and blanking region, may extend down into the filter bandpass, overlapping the video component. By using the technique of frequency doubling prior to filtering, such a condition is prevented. Asymmetry if present in the FM signal, whether its due to unbalance in the limiter circuits or unbalance in the discriminator diodes, will introduce an unwanted component of the carrier fundamental frequency into the filter. In addition to the desired double carrier frequency, this unwanted component may be within the bandpass range of the filter and, therefore, fail to be eliminated from the video output of the filter.

The filtered signal is fed to the emitter of one of two common base video amplifiers (Q18 or Q19) where the signal is amplified to a level suitable for driving the succeeding video output stage. Shunt high frequency compensation is provided by coil L1 and variable capacitor C39 in the collector circuit of the output common base amplifier (Q18 or Q19). Use of a variable capacitor in the high frequency compensation network enables the pass band at the high end to be adjusted for a flat response.



A. Q17 emitter, 1 ms/cm, .5 v/cm

B. Q18 collector, 1 ms/cm, .5 v/cm

Figure 39—Typical Waveforms, Channel 1 and Channel 2 Filter Drivers and Video Amplifier Circuits

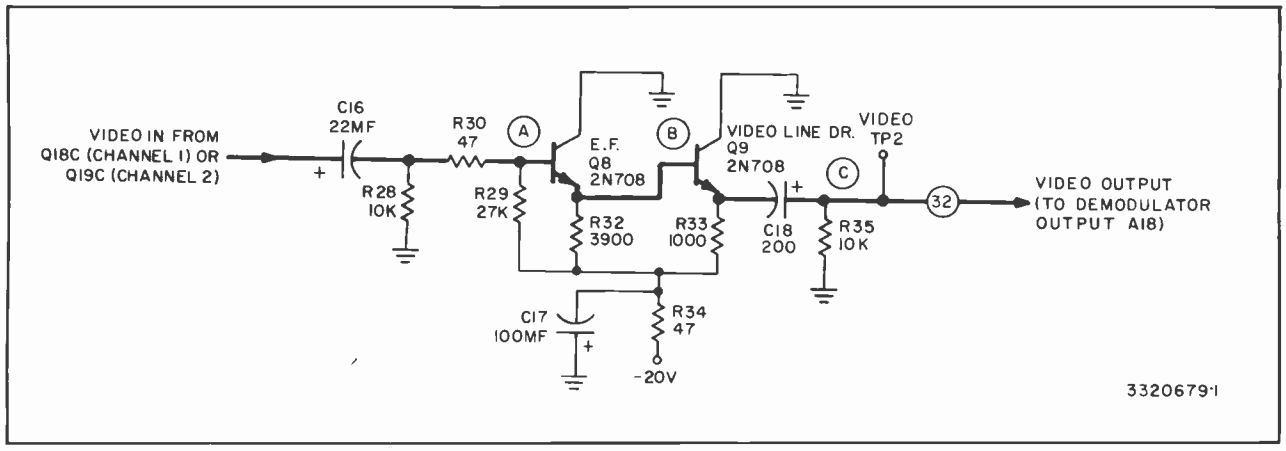
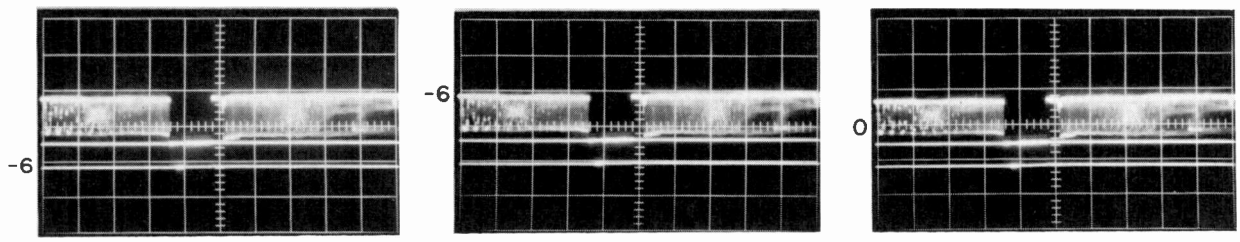


Figure 40—Emitter Follower and Video Line Driver Circuits



A. Q8 base, 1 ms/cm, .5v/cm

B. Q9 base, 1 ms/cm, .5v/cm

C. TP2, 1 ms/cm, .5v/cm

Figure 41—Typical Waveforms, Emitter Follower and Video Line Driver Circuits

International Standards Filter Selection

As mentioned previously, switching between the two filter circuits for operation on international standards is controlled by the VI SP and the VN SP busses. The desired line rate is selected by means of the TV STANDARDS switch, which is located on the front panel of the international Vertical Advance module B22.

When the 625-line rate is chosen, the 5.0 mc filter (channel 2) circuit is placed in operation. The −20 volts on the VI SP bus biases Q7, the channel no. 2 filter driver, so that it will conduct, while simultaneously cutting off Q18, the channel no. 1 video amplifier. The VN SP bus, which is at ground potential, cuts off Q17, the channel no. 1 filter driver, but allows Q19, the channel no. 2 video amplifier, to conduct. Therefore the output of the diode discriminator will pass through the channel no. 2 filter circuit.

When either the 405- or 525-line rate is selected, the VI SP and VN SP potentials are reversed and the channel no. 1 filter network is in operation. In this case the VN bus is at −20 volts, allowing Q17 to conduct while cutting off Q19. The VI SP bus is at ground potential and this permits Q18 to conduct, while preventing Q7 from conducting. Under these conditions, the output of the diode discriminator flows through the channel no. 1 filter circuit.

Video Output

The video output on the collector of the appropriate amplifier (Q18 or Q19) is coupled through C16 to the base of Q8 (see figure 40). Transistors Q8 and Q9 form a dc coupled cascade emitter follower amplifier, which isolates the preceding stages from the video output line. From the emitter of Q9, the signal is coupled through C18 to drive the line to the Demodulator Output module A18.

Adjustments

The following adjustments consist of two separate procedures. The first one covers balance of the limiters and the diode discriminator. This involves the adjustment of the three balance potentiometers (R208, R206, R205) in the clipper circuits and the two balance potentiometers (R12, R53) in the phase splitter circuits. The second procedure deals with the response of the detected video. This can be varied by adjusting C39 in the video amplifier circuits. All of these controls have been set at the factory, and they

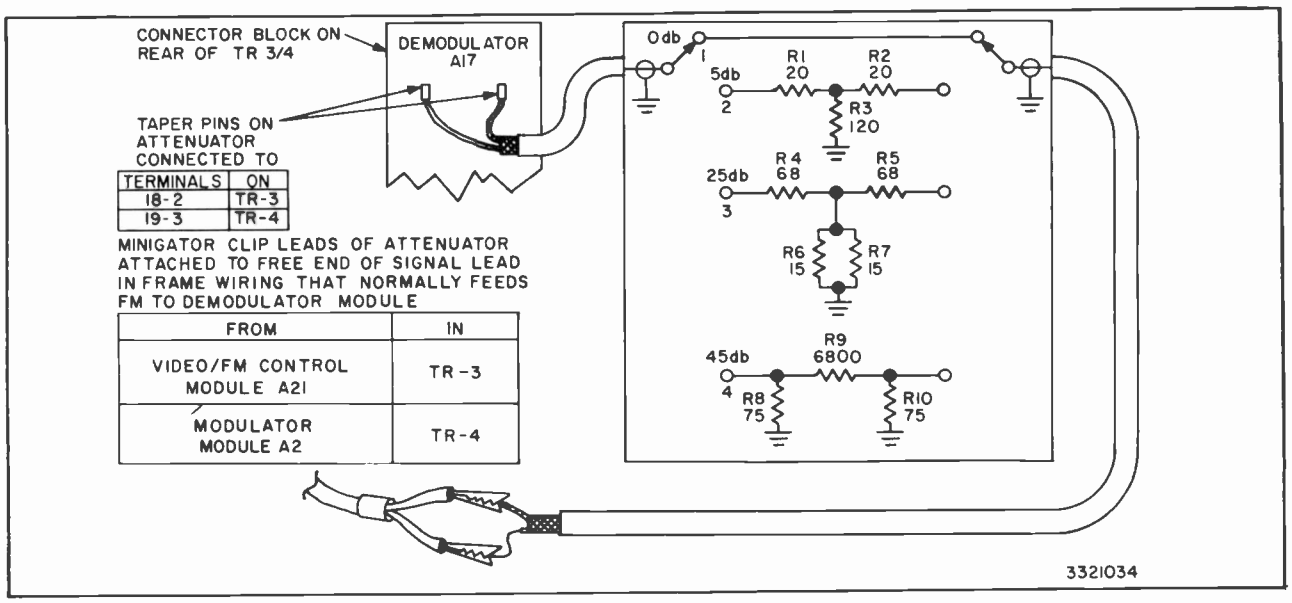


Figure 42—Schematic of Video Attenuator Showing Connection Details

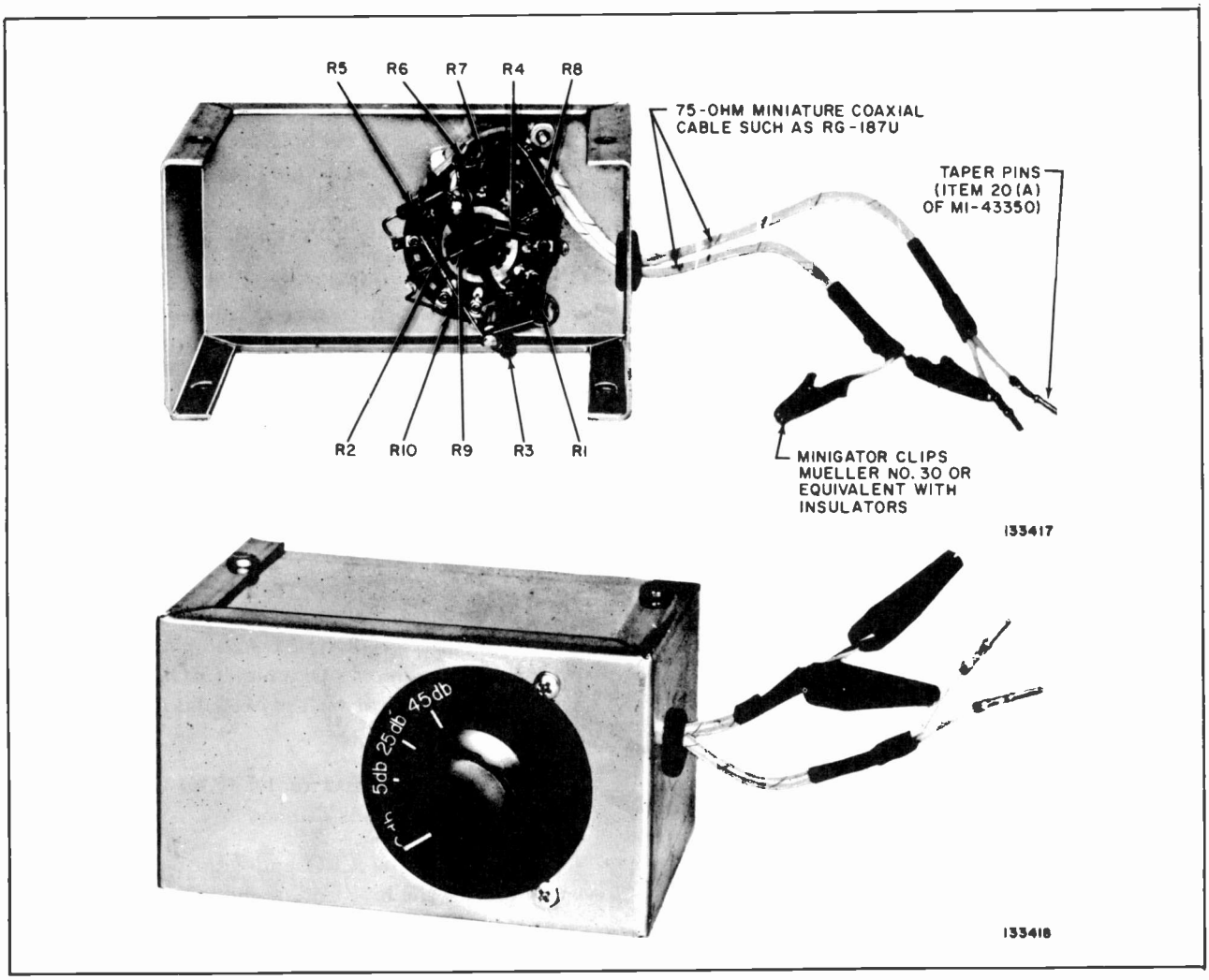


Figure 43—Typical Video Attenuator Assembly

should not be disturbed in the course of routine maintenance. However if the balance should be upset due to the replacement of diodes in the limiters or the discriminator or for some other reason, balance can be re-established by following the instructions outlined in the *Balance Procedure.* Similarly, if component replacement in the video stages adversely affects the response, the response can be restored by adjusting C39, as described in the *Video Response Procedure.*

In making the balance adjustments, it will be necessary to attenuate the input signal to the Demodulator by 5db, 25db, and 45db. This may be done by interposing a video attenuator in the coaxial line in the frame wiring that feeds the FM signal to the Demodulator. In lieu of a commercial attenuator, a network such as the one shown schematically in figure 42 can be used. This diagram also includes the interconnection details for inserting the attenuator in the coaxial line. A typical assembly of such an attenuator, with components and mechanical features illustrated, is shown in figure 43.

Balance Procedure

Recommended Test Equipment
Tektronix Type 535 oscilloscope (or equivalent) with low capacity probe.

1. Place the POWER circuit breaker in the OFF position.

2. To install the attenuator, remove the coaxial lead from terminals 19 and 3 of connector A17 on the rear of the TR-4. Connect the clip leads of the attenuator to the free end of the coaxial lead just removed. Insert the attenuator lead with the taper pins into terminals 19 and 3 of connector A17. Turn the attenuator switch to zero.

3. Mount the Demodulator in an extender and insert it in the unit. Place the TR-4 in the E-E mode; i.e., MOD-PLAY switch, an internal control on the Modulator (module A2), in the MOD position. Apply a composite video signal to the input of the recorder.

4. Place the POWER circuit breaker in the ON position. Place the TR-4 in STANDBY mode and select MONO STDS.

5. Check the sync tip frequency and deviation; adjust if necessary. (Instructions covering these adjustments are given in the *TR-4 Operation Manual,* IB-31810-1, under *Initial Setup.*)

6. Switch the CRO to DEMOD OUT and select the horizontal interval for display.

7. Switch the attenuator to 5db. Observe the CRO, and adjust the first limiter balance control (R208 on the front panel) for minimum rf at blanking and sync tip levels.

8. Switch the attenuator to 25db. Again observe the CRO, and adjust the second limiter balance control (R205, top internal trimpot) for minimum rf at blanking and sync tip levels.

9. Switch the attenuator to 45db. Repeat the same procedure, this time adjusting the third limiter balance control (R205, bottom internal trimpot).

10. Switch the attenuator back to zero db.

11. Connect a low capacity probe from the oscilloscope to the base of Q1 and measure the amplitude of the signal. The signal should be 2 volts peak-to-peak at this point. If necessary, adjust the LEVEL control, R122, to obtain this level.

12. The diode discriminator balance controls, R12 and R53, are adjusted by inserting a slender screwdriver into the access hole provided for each on the front panel of the Demodulator. Observe the CRO, and adjust each of these controls for minimum rf at blanking and sync tip levels.

13. Place the POWER circuit breaker in the OFF position. Disconnect the attenuator and restore the free end of the signal lead to its original terminals in connector A17. Return the MOD-PLAY switch to its original position; remove the extender and replace the Demodulator in the TR-4.

Video Response Procedure

1. Mount the Demodulator in an extender and insert it in the TR-4.

2. Connect a multiburst signal to the video input of TR-4; select MONO STD and place the Recorder in the E-E mode of operation. (MOD-PLAY switch, an internal control on the Modulator (module A2), in MOD position.)

3. Switch the CRO to DEMOD OUT and select the HOR interval for display.

4. Observe the CRO and adjust C39 for flattest response of the high end of the band.

5. Remove the extender and replace the Demodulator in the recorder; disconnect the multiburst signal from the video input.

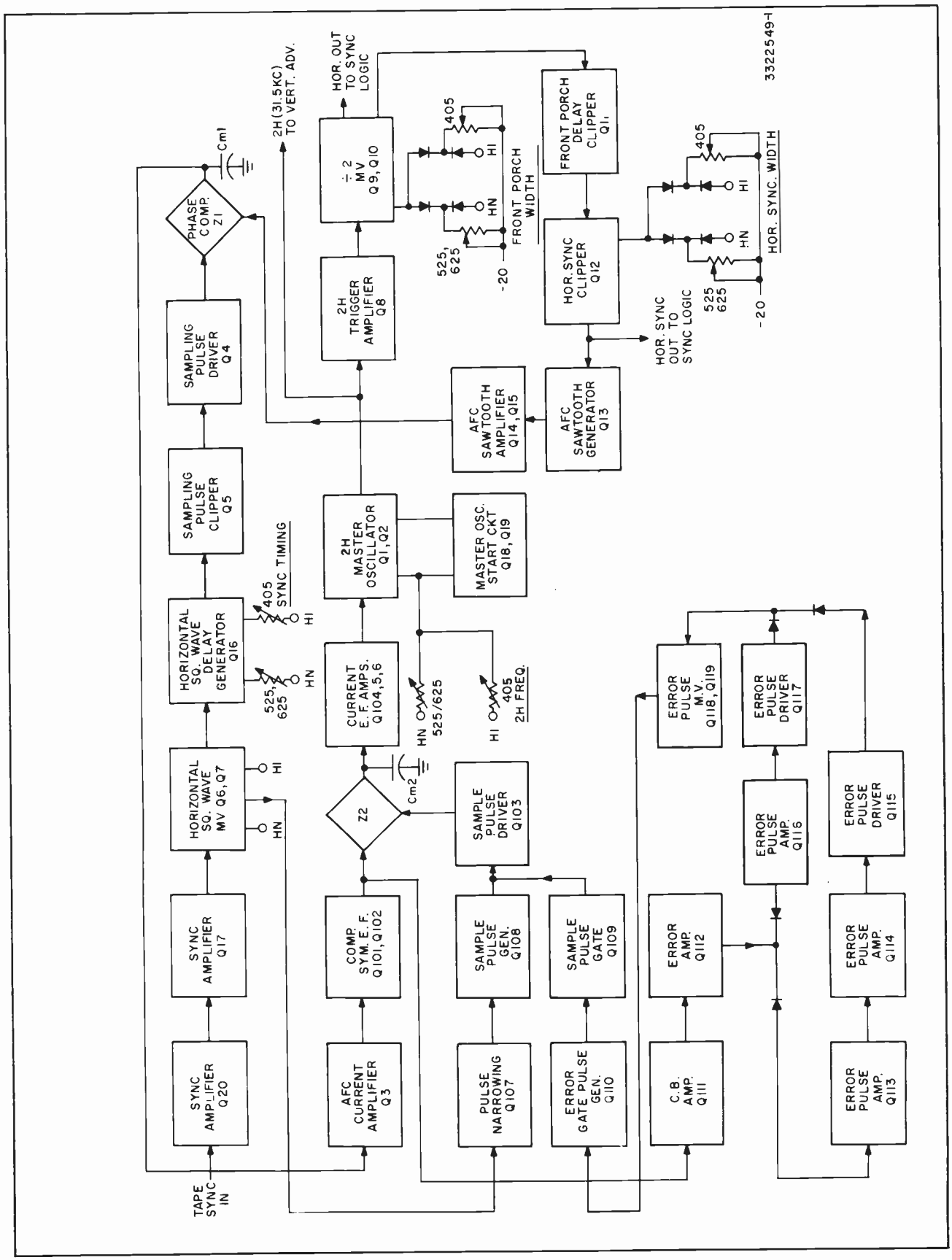


Figure 44—Block Diagram, Horizontal AFC Modules

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Under *Horizontal AFC Module A20,* delete all text, schematics and waveforms. In place of the deleted material, use the following:

Horizontal AFC Module A20

General

The Horizontal AFC module, shown in figure 44, produces a 31.5 kc (2H) pulse, a 15.75 kc horizontal square wave, and a horizontal sync pulse for 525-line standards. The 31.5 kc pulse is provided for the Vertical Advance (module B22) and the 15.75 kc square wave and the horizontal sync for the Sync Logic (module B21). For international standards operation, the counterpart of these pulses, characteristic of 405- and 625-line standards, are produced by this module. In contrast to the Horizontal AFC module, the Vertical Advance module and the Sync Logic module are closely tied together in that they trigger each other to achieve a continuous flow of correctly timed pulses. The Horizontal AFC module can be modified for 819-line standards operation in lieu of 405-line standards, by making minor wiring changes to the existing circuitry.

Standards Switching

In order to accommodate differences in the characteristics of the horizontal rate and horizontal sync pulses required for the various line standards, switchable time constant components are used in the pulse forming and pulse timing circuits. The time constant components are the same for 525- and 625-line standards; for 405-line standards, separate time constant components are used. The appropriate time constant components are switched into the circuit by means of the HN and HI busses, one of which is at −20 volts while the other is at ground. The potential that either bus is at depends upon the line standard in use.

The desired line standard is selected by means of the TV STANDARDS switch, which is located on the front panel of the international Vertical Advance (module B22). When 525- or 625-line operation is chosen, −20 volts is applied to the HN bus and the HI bus goes to ground. Hence, the time constant components related to 525/625-line standards are activated, while those associated with 405-line standards remain inactive. On 405-line standards the opposite is true. The HN bus is at ground and the HI bus is at −20 volts. Thus the 405-line time constant components are switched into the circuit, while those for 525/625-line standards are switched out. Diodes are connected in series with the HN and HI busses to isolate the time constant components in the active circuit from those in the inactive circuit.

> NOTE: For purposes of discussion, the following description is slanted towards 525-line standards operation. In most cases, when values referring to circuit parameters are mentioned they apply to 525-line standards, unless otherwise noted. However, from a functional standpoint, the description is equally valid for the other line standards.

Horizontal Pulse Advance Technique

The sync signal can easily be recovered from the incoming composite video signal; however, the blanking signal, which cannot be removed reliably, must be regenerated from sync. The desired blanking pulse must precede by 1.7 microseconds (nominal front porch width) the sync signal from which it is regenerated. Since sync and blanking are both recurrent pulses, the position of the next sync pulse from the position of the preceding one may be predicted. Al-

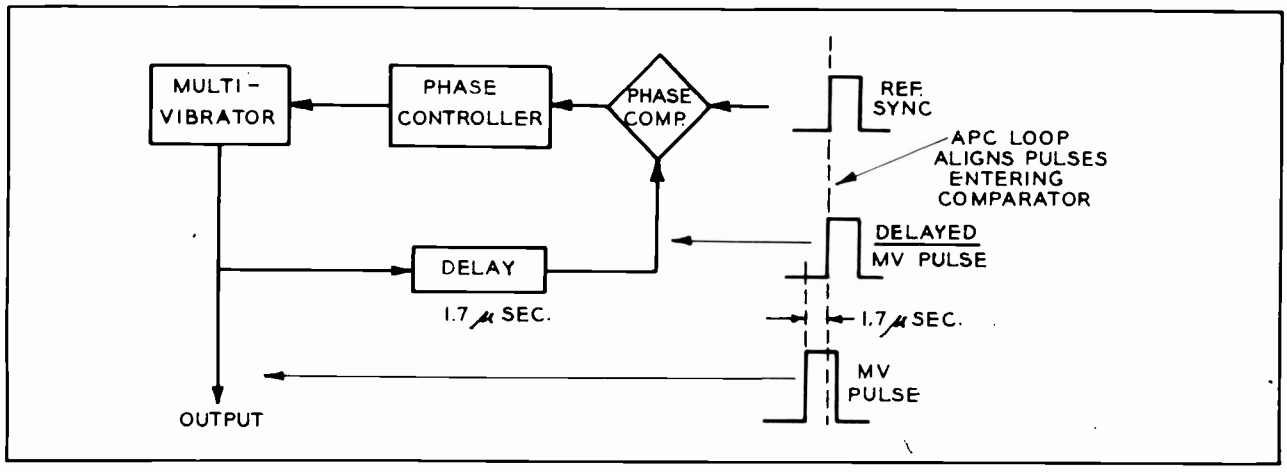


Figure 45—Block Diagram, Pulse Advance Circuit

though a simply delay multivibrator with a nominal pulse width of 62.2 microseconds might seem useful to this purpose, its accuracy in pulse width and frequency is inherently inadequate for the application. Even if the tolerance of better than $\pm 0.1\%$ required in the multivibrator to hold the front porch width to within 3% were met, changes in horizontal frequency of only $+1\%$ would reduce the front porch from its nominal 1.7 microseconds to 0.43 microseconds, which is less than half the allowable minimum.

Horizontal pulse advance is obtained through the 2H master oscillator multivibrator, Q1, Q2, for which the frequency and phase is controlled by an automatic phase control circuit referenced to the incoming tape sync. The block diagram, figure 45 illustrates this technique. The feedback loop which controls the phase of the multivibrator contains a 1.7 microsecond delay. The automatic phase control loop aligns the two pulses appearing at the phase comparator. However, the multivibrator pulse is delayed by 1.7 microseconds before reaching the comparator through Q14 and Q15. The delayed pulse is lined up with the pulses generated from referenced sync. Thus, the undelayed multivibrator pulse precedes sync by 1.7 microseconds and is properly timed to regenerate horizontal blanking. In this system, the feedback loop tracks any changes in horizontal frequency, eliminating variations in front porch width due to frequency changes; also, a one percent change in delay causes only one percent change in front porch width.

2H Master Oscillator

The 2H master oscillator, Q1, Q2, (figure 46) forms an astable multivibrator. On 525/625-line standards, the HN bus is at -20 volts and the HI bus is at zero on ground. The free running frequency of the multivibrator is determined by the charging time of capacitors C28 and C29 through resistors R32, R33, R65, and R2, the 2H FREQ potentiometer used for 525/625-line standards. An afc current from the afc current amplifier, Q3, (described later) is added to the charging current, correcting the frequency and phase of the 2H oscillator with respect to incoming sync. The frequency is set to approximately 31.5 kc on 525-line standards by the 2H FREQ control, R2, and the AFC OFF switch, S1, which furnishes a fixed value of afc current. The fixed afc current is obtained when the AFC OFF switch (designated SET-RUN on the schematic, figure 58) is closed or in the SET position. Both 2H FREQ potentiometrs are screwdriver adjustments and the AFC OFF is a pushbutton switch. All are mounted on the front panel. The 2H output on the collector of Q1 is fed simultaneously to the base of the 2H trigger amplifier, Q8, and to the line going to the Vertical Advance (module B22).

Switching Transient Suppression

In conjunction with the 2H master oscillator circuitry just discussed another loop of circuits is involved. These are best described as protection or disabling circuits. The reason these come into action is that in the playback of certain types of tapes known as "RF dubs" switching pulses are actually recorded on the tape. In the situation where these pulses occur just prior to every 16th horizontal sync pulse, difficulty in the form of line-pulling for three or four lines could develop.

The sync separating circuits cannot distinguish between these transients and the normal horizontal sync. As a result of this, improper correction signals would be fed to the AFC system. In addition, once disturbed in this fashion the disturbance would continue for several lines while the AFC feedback loop goes through its recovery cycle.

To prevent improper control a second sampling system is used. (Refer to block diagram figure 44.) The voltage stored on memory capacitor CM1 is not passed immediately to control the oscillator but is forced to await a second sampling "inspection." In normal sampling, each sample produces nearly the same voltage on CM1 as did the previous sample. This voltage is continuously monitored by a differentiator, and amplifier Q111. This amplifier and subsequent error amplifiers respond only to changes in voltage. If the voltage at CM1 stays constant, within predetermined limits; a second sampler, S2, transfers the voltage on CM1 to CM2, where it is applied to the controlled oscillator Q1, Q2. However, if the differentiator detects a large change from the preceding sample, it sends an inhibit signal by the ten line monostable multivibrator Q118, Q119 and on to the sample pulse gate, Q109; through which the sample pulse passes to actuate S2. With this gate inhibited, no sample pulse passes to S2; hence, the voltage on CM1 is not transferred to CM2, and the oscillator is not disturbed by the bad sample.

The previous voltage on CM2 holds the oscillator on the right frequency and phase until a proper sample is passed by S1. This sampled voltage is then passed on to CM2, and the normal functioning of the circuit resumes.

During the lockup cycle, each sample differs considerably from the preceding one. This system, applied in its simplest form, would inhibit every sample, and would prevent lockup from ever taking place. The ten line mutlivibrator Q118, Q119 allows inhibiting action only on every tenth sample; the 9 intermediate samples are passed without regard to the differentiator's evaluation of them. This assures lockup.

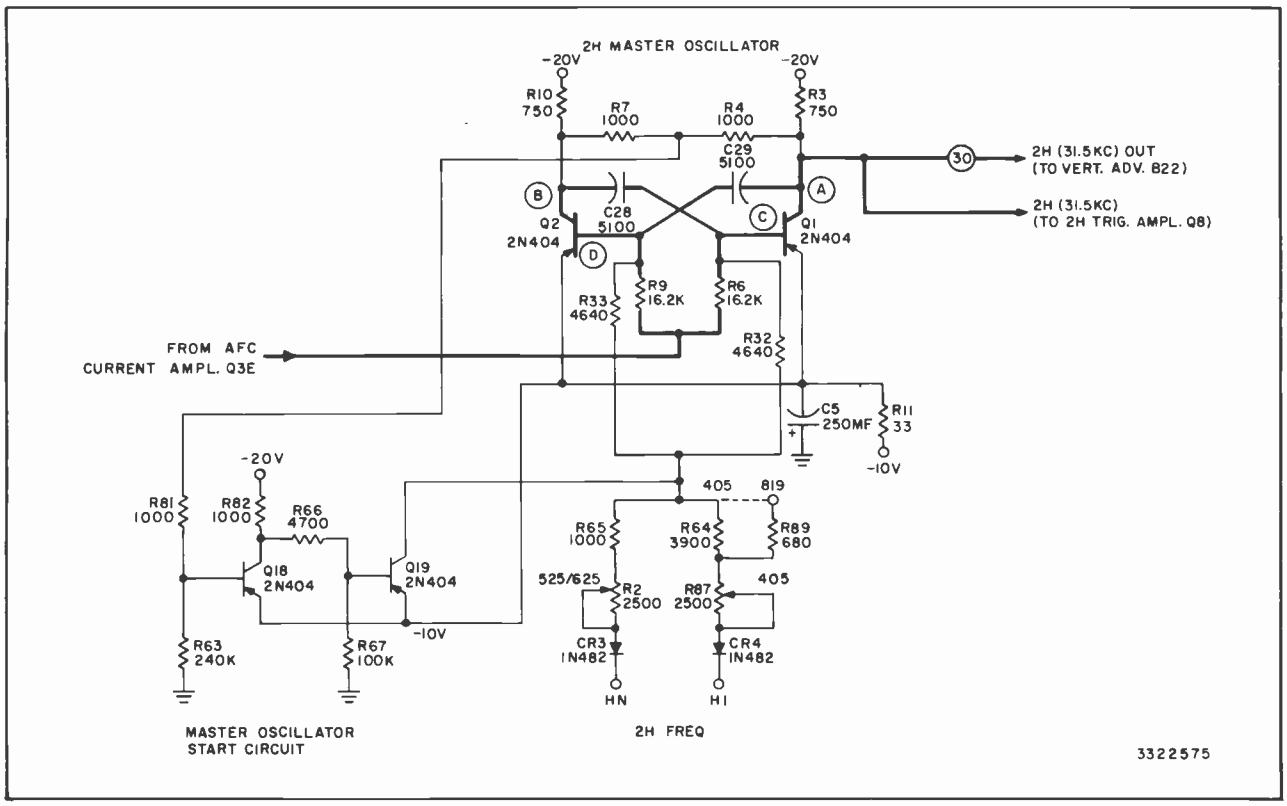
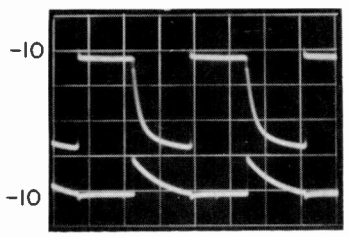
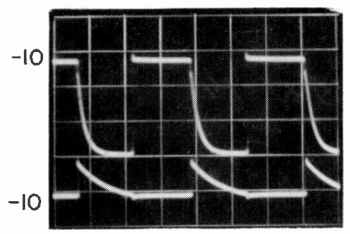


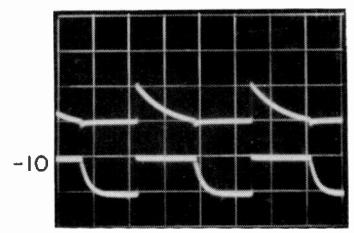
Figure 46—2H Master Oscillator Circuit



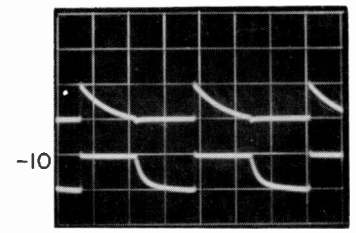
A. Top: Q1 collector, 10 μs/cm, 2v/cm
Bottom: Q1 base, 10 μs/cm, 5v/cm



B. Top: Q2 collector, 10 μs/cm, 2v/cm
Bottom: Q2 base, 10 μs/cm, 5v/cm



C. Top: Q1 base, 10 μs/cm, 5v/cm
Bottom: Q2 collector, 10 μs/cm, 5v/cm



D. Top: Q2 base, 10 μs/cm, 5v/cm
Bottom: Q1 collector, 10 μs/cm, 5v/cm

Figure 47—Typical Waveforms, 2H Master Oscillator Circuit

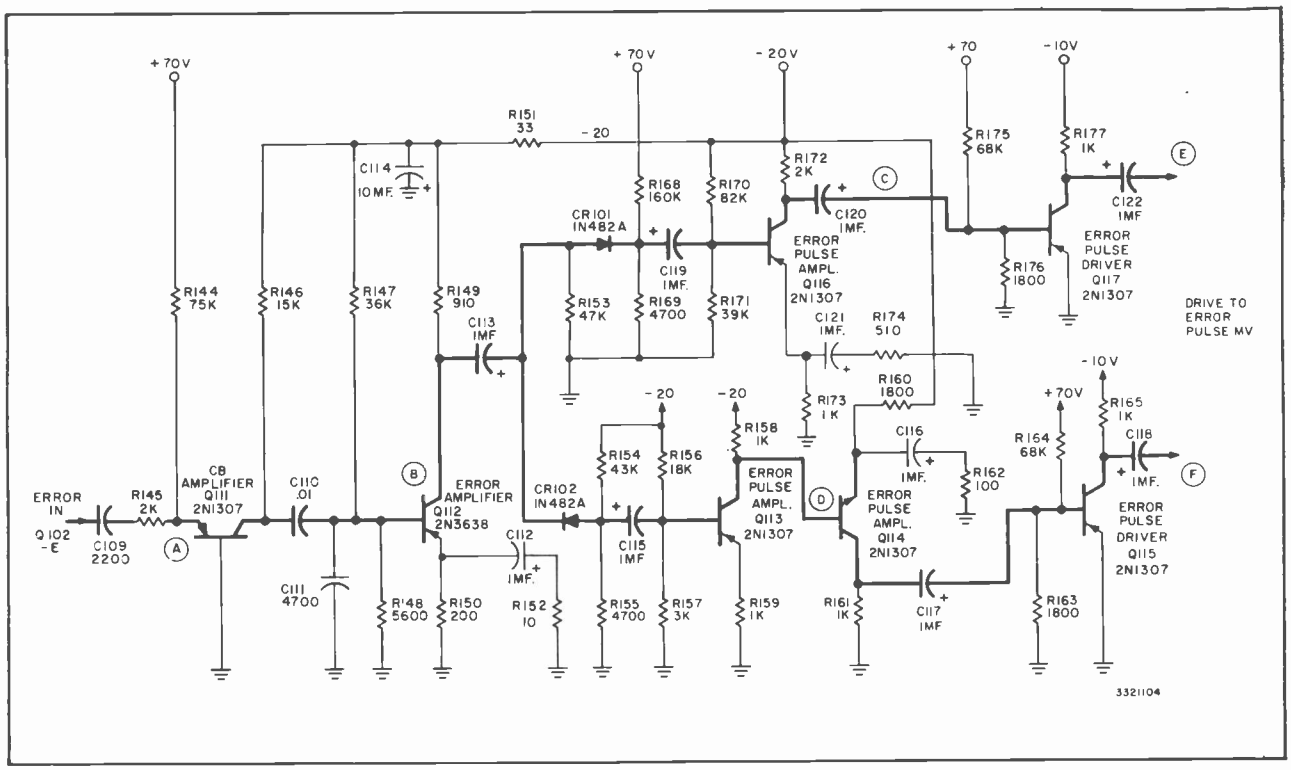
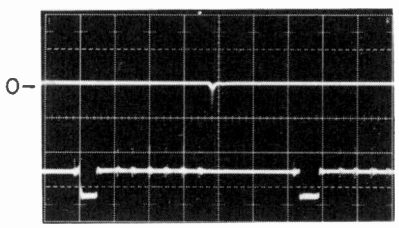
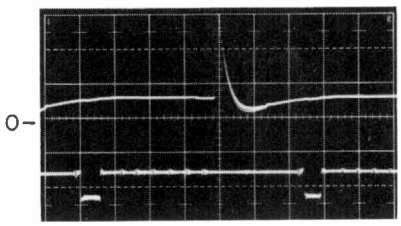


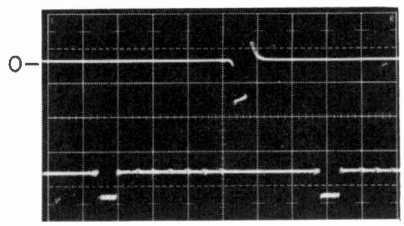
Figure 48—Error Pulse Amplifiers



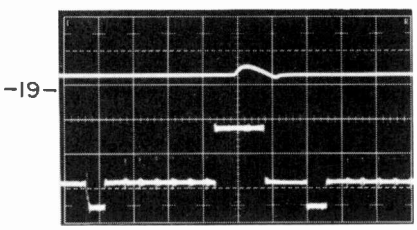
A. Top: Q111E, 10 μs/cm, 2v/cm
Bottom: TP3 DEMOD OUT, 10 μs/cm, .5v/cm



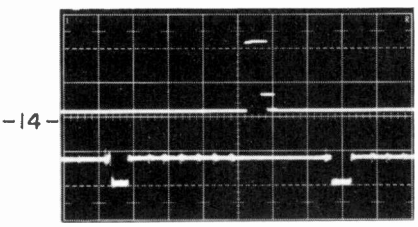
B. Top: JUNCTION CR101 & CR102, 10 μs/cm, 2v/cm
Bottom: TP3 DEMOD OUT, 10 μs/cm, .5v/cm



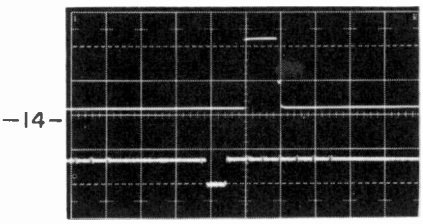
C. Top: Q117B, 10 μs/cm, 2v/cm
Bottom: TR3 DEMOD OUT, 10 μs/cm, .5v/cm



D. Top: Q114B, 10 μs/cm, 2v/cm
Bottom: TP3 DEMOD OUT, 10 μs/cm, .5v/cm



E. Top: C122 NEG, 10 μs/cm, 5v/cm
Bottom: TP3 DEMOD OUT, 10 μs/cm, .5v/cm



F. Top: C118 NEG, 10 μs/cm, 5v/cm
Bottom: TP3 DEMOD OUT, 10 μs/cm, .5v/cm

Figure 49—Typical Waveforms, Error Pulse Amplifiers

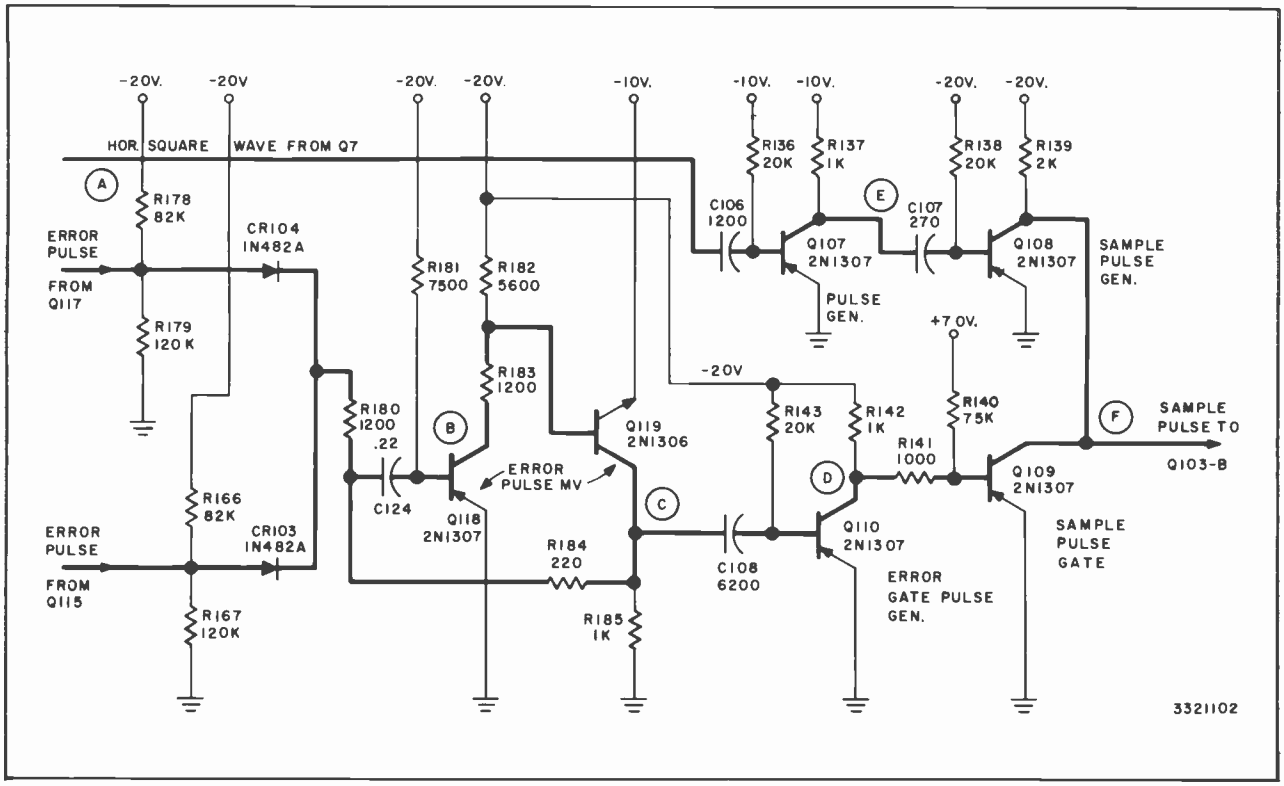
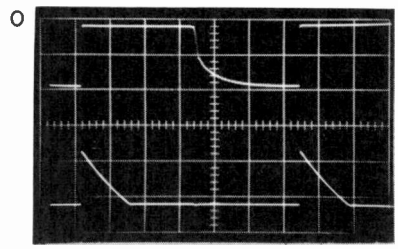
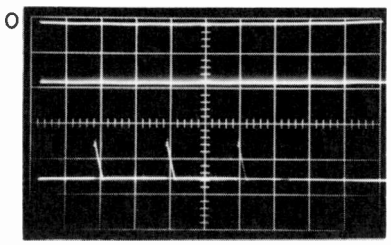


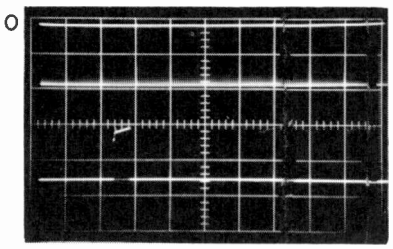
Figure 50—Error Pulse MV and Sample Pulse Generator



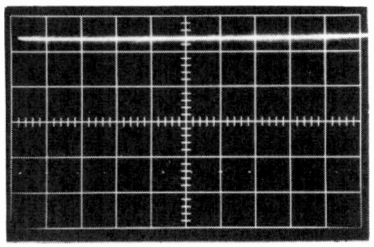
A. Top: Q7 collector, 10 μs/cm, 5v/cm Bottom: Q107 base, 10 μs/cm, 2v/cm



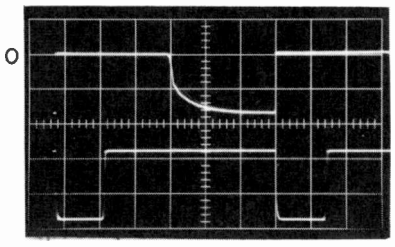
B. Top: Q7 collector, 2 ms/cm, 5v/cm Bottom: Q118 base, 2 ms/cm, 2v/cm



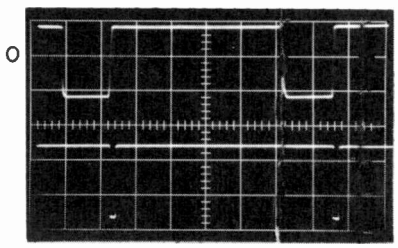
C. Top: Q7 collector, 2 ms/cm, 5v/cm. Bottom: Q119 collector (Adj. switching pulse to leading edge of sync) 2 ms/cm, 5v/cm



D. Q110 collector, 5 ms/cm, 2v/cm



E. Top: Q7 collector, 2 μs/cm, 5v/cm Bottom: Q107 collector, 10 μs/cm, 5v/cm



F. Top: Q107 collector, 10 μs/cm, 5v/cm Bottom: Q109 collector, 10 μs/cm, 5v/cm

Figure 51—Typical Waveforms, Error Pulse MV and Sample Pulse Generator

Since transients can be either negative or positive in direction two error pulse paths are provided; one via Q116, Q117; the other via Q113, Q114, Q115. The extra stage in the latter path inverts the signal so that the output pulses at Q117 and Q115 are always of positive polarity for triggering the error pulse multivibrator. See figures 48, 49, 50, 51.

Start Circuit

The starting circuit, Q18 and Q19, ensures that the 2H master oscillator keeps running at all times. This circuit prevents a situation from arising that could lead to both transistors of the 2H master oscillator being saturated at the same time. Were such a condition to occur, even for an instant, the collectors of both Q1 and Q2 would assume the same potential as that of their emitters, approximately −10 volts, and the 2H master oscillator would remain at rest, generating no output.

The start circuit transistors are turned on and off alternately by means of the biasing arrangement employed. The voltage at the junction of R4 and R7 cannot be more negative than −10 volts. Therefore, the voltage developed across the divider network consisting of R63, R81 and the parallel combination of R4 and R7 provides a bias on the base of Q18 that is more positive than the −10 volts on the emitter and thus cuts off this transistor. The bias voltage on the base of Q19 is developed across the voltage divider consisting of R67, R66, and R82. This voltage is more negative than that on the emitter of Q19, therefore this transistor is driven into saturation and virtually the full potential on the emitter (−10 volts) appears on the collector. The voltage on the collector of Q19 is applied across R32 and R33 to the bases of Q1 and Q2, respectively. Since there is −10 volts on the emitters of Q1 and Q2 already, the −10 volts on the bases Q1 and Q2 causes them to become reverse biased. In this state, assuming perfect equilibrium between Q1 and Q2, no current will flow in the emitter-base circuit of either transistor therefore both will be cut off. However, since there is inherently some unbalance between the components of each half of the multivibrator, one side of the 2H master oscillator will begin to conduct before the other. Thus one transistor is driven into saturation and the other is cut off.

At the same time, the states of Q18 and Q19 are reversed. Now Q19 is cut off, and current from the HI or HN bus is allowed to flow into the base of the saturated transistor. Transistor Q18 is turned on by the bias on the base, which is now more negative than the voltage on the emitter. The bias is obtained

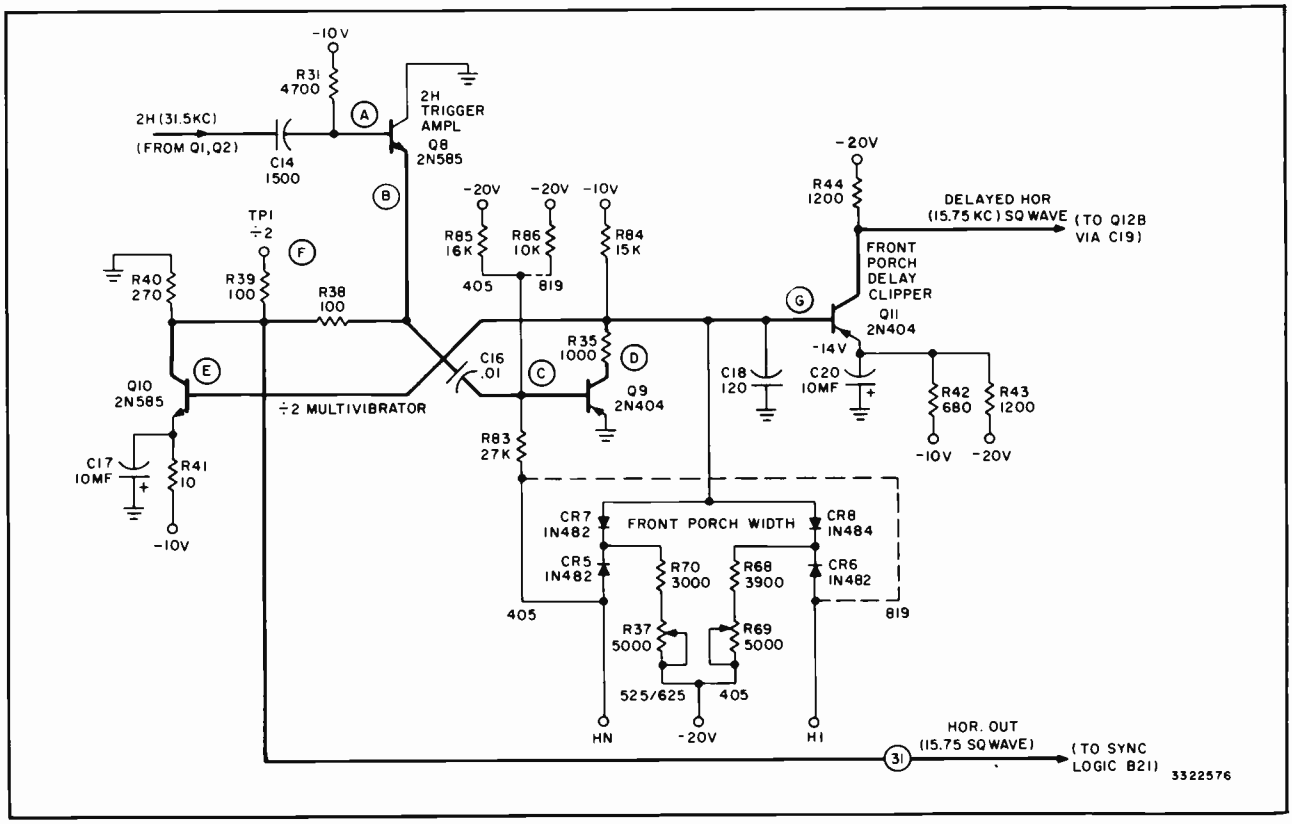


Figure 52—2H Trigger Amplifier, ÷2 MV and Front Porch Delay Clipper Circuits

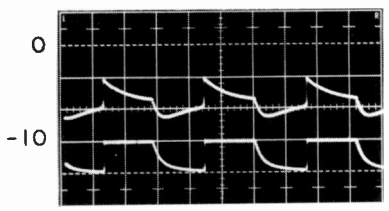
from the −20 volt supply and is developed across the divider network formed by R63, R81, and the 1000 and the 750 ohm resistors in the collector circuit of the transistor that is cut off.

15.75 kc Generator and Front Porch Delay Clipper

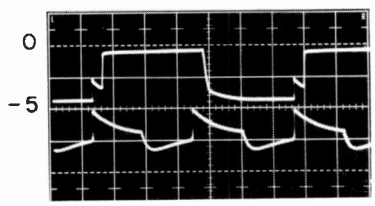
To provide a square wave that is half the 2H pulse (15.75 kc on 525-line standards) which is properly timed for the generation of horizontal blanking and horizontal drive in the Sync Logic (module B21), the divide by two monostable multivibrator, Q9, Q10, is triggered from the 2H amplifier, Q8 (figure 52). Both transistors of the ÷2 multivibrator are saturated in the stable state and are driven to cutoff by a positive going trigger pulse. The leading edge of the 2H pulse (31.5 kc) appearing on the emitter of the 2H amplifier, Q8, serves as the trigger. The time constant of C16, R83, and R85 determines the duration of the cutoff period, which is longer than the period of the 2H pulse (31.5 kc). Both transistors of the ÷2 multivibrator then revert to the saturated state until the next trigger pulse comes along.

A gating action is accomplished by dc connecting the emitter of Q8 through R38 to the collector of Q10. When the ÷2 multivibrator is in the saturated or stable state, the collector of Q10 and the emitter of Q8 are at −10 volts, and the collector of Q8 is at zero. Under these conditions, the 2H pulse on the base of Q8 causes the latter to conduct.

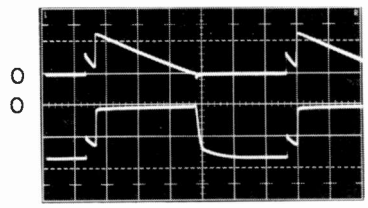
The output pulse on the emitter of Q8 is coupled through C16 to the base of Q9. The positive going leading edge of this pulse serves as a trigger to cut off Q9, which simultaneously cuts off Q10. When



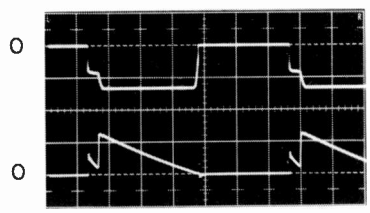
A. Top: Q8 base, 10 μs/cm, 5v/cm
Bottom: Q1 collector, 10 μs/cm, 5v/cm



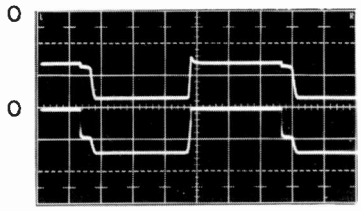
B. Top: Q8 emitter, 10 μs/cm, 5v/cm
Bottom: Q8 base, 10 μs/cm, 5v/cm



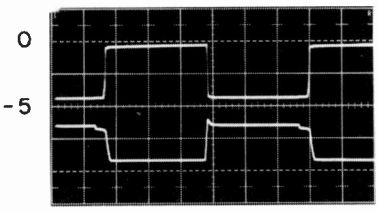
C. Top: Q9 base, 10 μs/cm, 5v/cm
Bottom: Q8 emitter, 10 μs/cm, 5v/cm



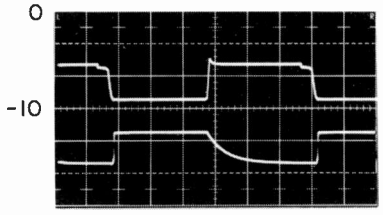
D. Top: Q9 collector, 10 μs/cm, 10v/cm
Bottom: Q9 base, 10 μs/cm, 5v/cm



E. Top: Q10 base, 10 μs/cm, 5v/cm
Bottom: Q9 collector, 10 μs/cm, 10v/cm



F. Top: TP1, 10 μs/cm, 5v/cm
Bottom: Q10 base, 10 μs/cm, 5v/cm



G. Top: Q11 base, 10 μs/cm, 5v/cm
Bottom: Q11 collector, 10 μs/cm, 5v/cm

Figure 53—Typical Waveforms, 2H Trigger Amplifier, ÷2 MU and Front Porch Delay Clipper Circuits

Q10 is cut off, the potential on the collector of Q10 and the emitter of Q8 is zero. This makes it impossible for Q8 to pass the trigger pulses, since the pulses appearing on the base of Q8 do not exceed zero volts in the positive direction. Transistor Q8 is biased so that it does not pass the negative pulses applied to the base.

The output on the collector of Q9 is a square wave whose frequency is 15.75 kc or half the frequency of the 2H pulse on 525-line standards. This signal is direct coupled to the base of Q11, the front porch delay clipper. The shunt capacitor, C18, in the base of Q11 slows the rise time of the square wave. Transistor Q11 does not conduct until the potential on the base falls to approximately the emitter potential of −14 volts, which is developed across the voltage divider formed by R42, R43. The time Q11 takes to reach this potential is the delay time. When Q11 conducts, the output on the collector is a fast rise time square wave whose leading edge is delayed with respect to the input square wave. The delay time of Q11 is determined by the rise time of the square wave applied to the base. The rise time of this signal is controlled by the appropriate internal FRONT PORCH WINDOW potentiometer (R37 on 525/625-line standards or R69 on 405-line standards).

Regenerated Sync

As shown in figure 52, the delayed 15.75 kc output pulse on the collector of Q11 is coupled through C19 to the base of Q12, the horizontal sync clipper, which is a pulse narrowing or boxcar circuit. The output pulses produced by this circuit are regenerated sync. The width of the pulse is determined by the time constant of C19, R74, R75, and on 525/625-line standards, R72 and HOR SYNC WIDTH potentiometer R45, an internal control. The regenerated horizontal sync appearing on the collector of Q12 is fed simultaneously to the AFC sawtooth generator, Q13, and to the Sync Logic (module B21).

The horizontal sync is applied to the base of Q13 after passing through an integrator consisting of R48 and C15. The purpose of the integrator is to slow the rise time of the sync pulse so there will be a slight delay before Q13 conducts. This delay contributes to the total advance in the timing of the 31.5 kc (2H) square wave relative to tape sync. However, the delay does not affect the front porch width, since that is determined only by the delay between the 15.75 kc square wave (used to generate horizontal blanking) and the leading edge of regenerated horizontal sync. A sync timing control circuit (described later) in the base of the horizontal square wave delay generator, Q16, enables the timing of the regenerated horizontal sync to be adjusted so that it is in phase with the incoming tape sync.

AFC Sawtooth

Transistor Q13 conducts when the voltage of the integrated sync pulse on the base drops to the same potential on the emitter (approximately −4 volts.) See figure 54. The voltage on the emitter is established by the voltage divider consisting of R91, R49 and R50 returned to −20 volts. When Q13 conducts, it provides a low impedance discharge path for the sawtooth capacitor, C25. Then, when Q13 is cut off by the decay of the input sync pulse, C25 charges slowly through R53 and R52, generating a sawtooth voltage. The sawtooth voltage on the collector of Q13 is direct coupled to the bases of the sawtooth amplifier, Q14, Q15.

Transistors Q14 and Q15 are connected to form a complementary symmetry emitter follower bootstrap amplifier. The bootstrap configuration increases the linearity of the sawtooth waveform; the complementary symmetry arrangement provides sufficient current gain and a very low impedance to drive the phase comparator. The sawtooth output on the emitter of Q14, Q15 is coupled through an isolation capacitor, C12, as the input to one side of the phase comparator (figure 58 which will be described later).

Delayed Horizontal Square Wave

Tape sync from the sync separator circuit in the Demodulator Output (module A18) is coupled through C37 to the base of sync amplifier Q20, an emitter follower (figure 56). Transistor Q20 presents a low output impedance to the succeeding sync amplifier, Q17, a common base amplifier, and also isolates the latter from the output stage in the sync separator circuit. The output on the emitter of Q20 is coupled across R60 and C31 to the emitter of Q17. Transistor Q17 in conjunction with R60 and C31 differentiates the negative input sync. The negative going leading edge of the output pulse on the collector of Q17 is fed across R29 to trigger the horizontal square wave multivibrator Q6, Q7.

The latter is a monostable multivibrator whose time constant is such that triggering is effective only at the horizontal frequency rate of composite sync. Otherwise, during the vertical blanking interval, the equalizing pulses and vertical sync serrations, which occur at twice the rate of the horizontal sync pulses, would trigger Q6, Q7. If this "double frequency" (31.5 kc on 525-line standards) or half line informa-

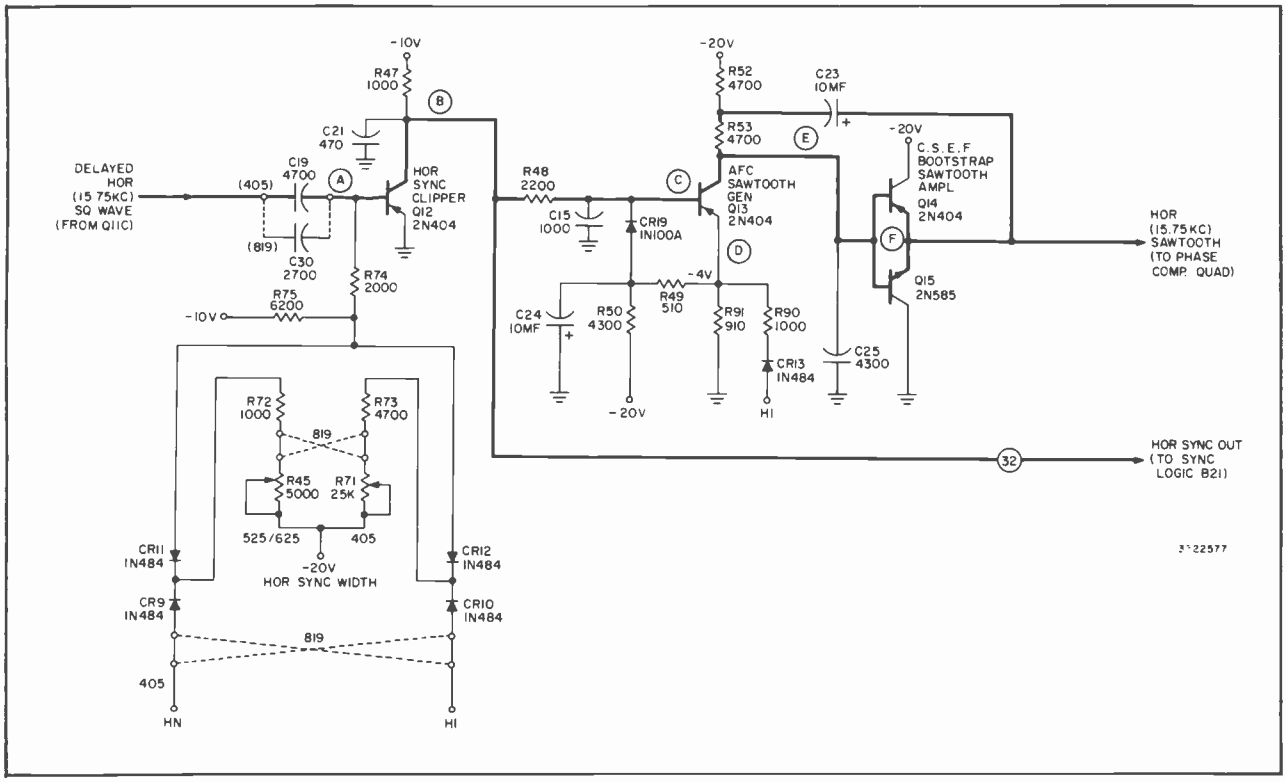
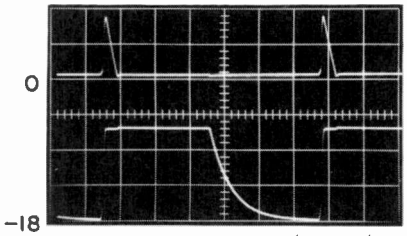
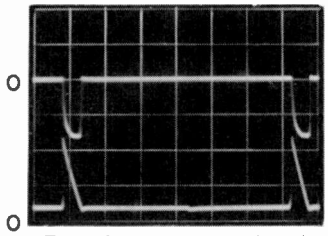


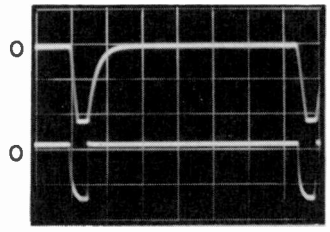
Figure 54—Horizontal Sync Clipper AFC Sawtooth Clipper and Complementary Symmetry Circuits



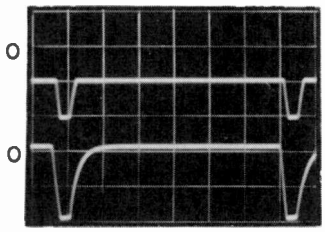
A. Top: Q12 base, 10 μs/cm, 2v/cm
Bottom: Q11 collector, 10 μs/cm, 2v/cm



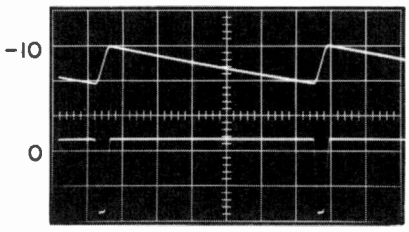
B. Top: Q12 collector, 10 μs/cm, 5v/cm
Bottom: Q12 base, 10 μs/cm, 2v/cm



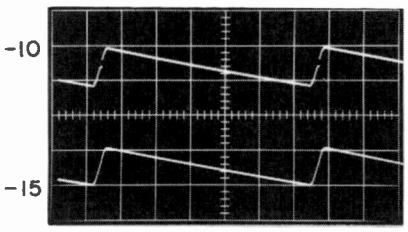
C. Top: Q13 base, 10 μs/cm, 2v/cm
Bottom: Q12 collector, 10 μs/cm, 5v/cm



D. Top: Q13 emitter, 10 μs/cm, 2v/cm
Bottom: Q13 base, 10 μs/cm, 2v/cm



E. Top: Q13 collector, 10 μs/cm, 5v/cm
Bottom: Q13 emitter, 10 μs/cm, 1v/cm



F. Top: Q14 emitter, 10 μs/cm, 5v/cm
Bottom: Q14 base, 10 μs/cm, 5v/cm

Figure 55—Typical Waveforms, Horizontal Sync Clipper AFC Sawtooth Clipper and Complementary Symmetry Circuits

tion were permitted to pass, it would trigger the sampling pulse clipper, Q5, (described later) ultimately keying on the phase comparator during the wrong part of the sawtooth voltage cycle. Were this to happen, the 2H master oscillator, Q1, Q2, would receive the wrong afc information. Therefore, to prevent such an occurance, the horizontal square wave multivibrator, Q6, Q7, is designed to produce keying pulses only at a horizontal rate (15.75 kc on 525-line standards) for the sampling pulse clipper, Q5.

In the quiescent state with no signal applied, Q7 is cut off and Q6 is saturated. The collector of Q7 is approximately −10 volts and the collector of Q6 is at zero volts or ground potential, and C11 is charged to 10 volts through R27, R25, and the base-emitter junction of Q6. When a negative pulse from the collector of Q17 is applied to the base of Q7, it forward biases this transistor, driving it into saturation. As Q7 becomes saturated, it generates a positive pulse on the collector which is coupled through C11 to the base of Q6. With a positive pulse applied to its base, Q6 becomes reverse biased and goes to cut off. Capacitor C11 then begins to discharge through the saturation resistance of Q7, R25, and R78, R80 in parallel, and the multivibrator starts to return to its original state. As C11 discharges, the voltage on the base of Q6 becomes less positive and Q6 begins to conduct, causing the voltage on the collector of Q6 to become less negative. Since the collector of Q6 is coupled to the base of Q7 through R26, this decreasing negative (or relatively more positive) voltage begins to reverse bias the base of Q7. As Q6 reaches saturation, the voltage on the base of Q7 is sufficiently positive to cut off this transistor. With Q6 saturated and Q7 cut off, the multivibrator is in its original quiescent state, in which it remains until the next trigger pulse arrives.

By applying a succession of negative trigger pulses to the base of Q7, the multivibrator generates a train of positive sync pulses or horizontal square waves at the collector of Q7. On 525/625-line standards, the width or frequency of these pulses is determined by the time constant of R25, C11, and the parallel resistance of R78 and R80. On 405-line standards, the pulse width or frequency is determined by R25, C11, and R78. Through the use of a horizontal square wave multivibrator, any half line information during vertical blanking is eliminated. i.e., 2H or, on 525-line standards, 31.5 kc.

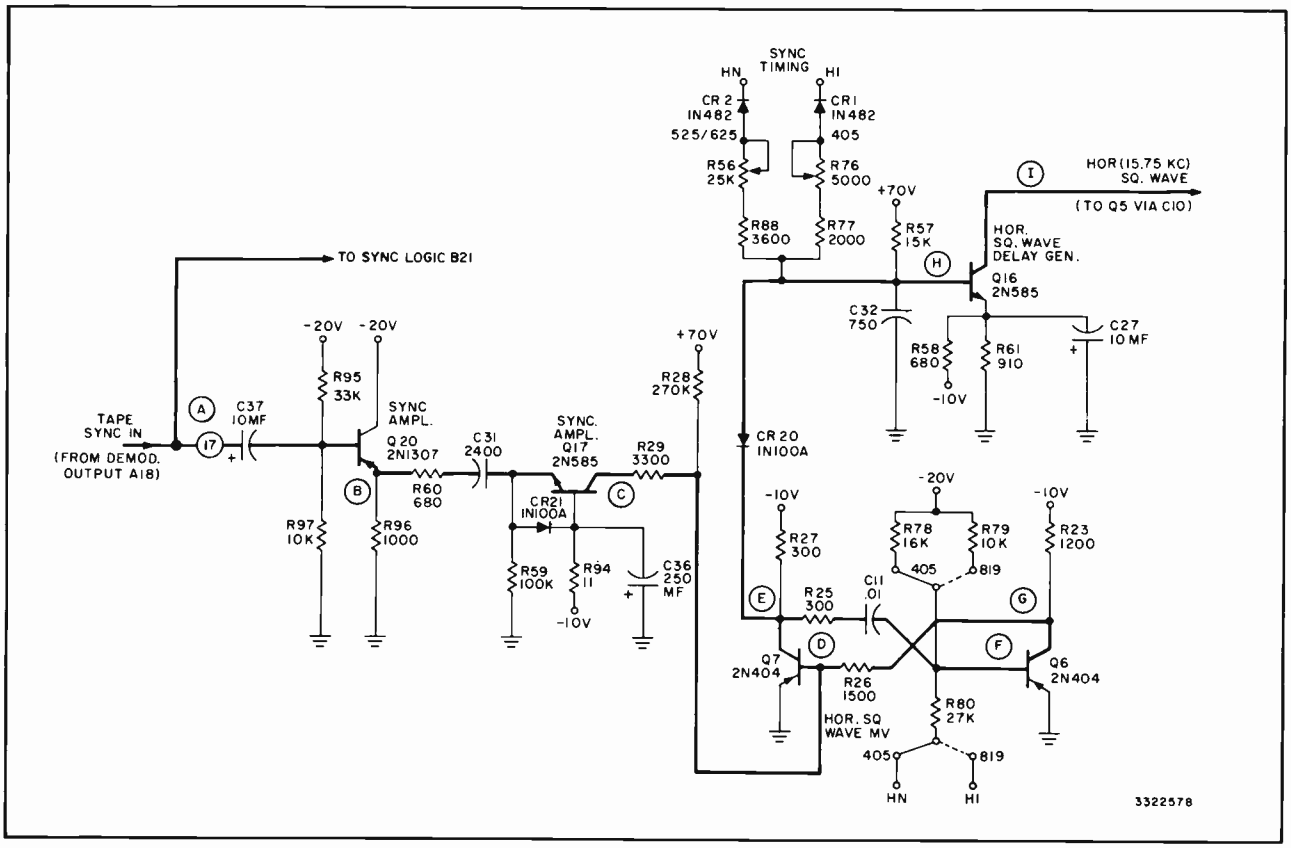
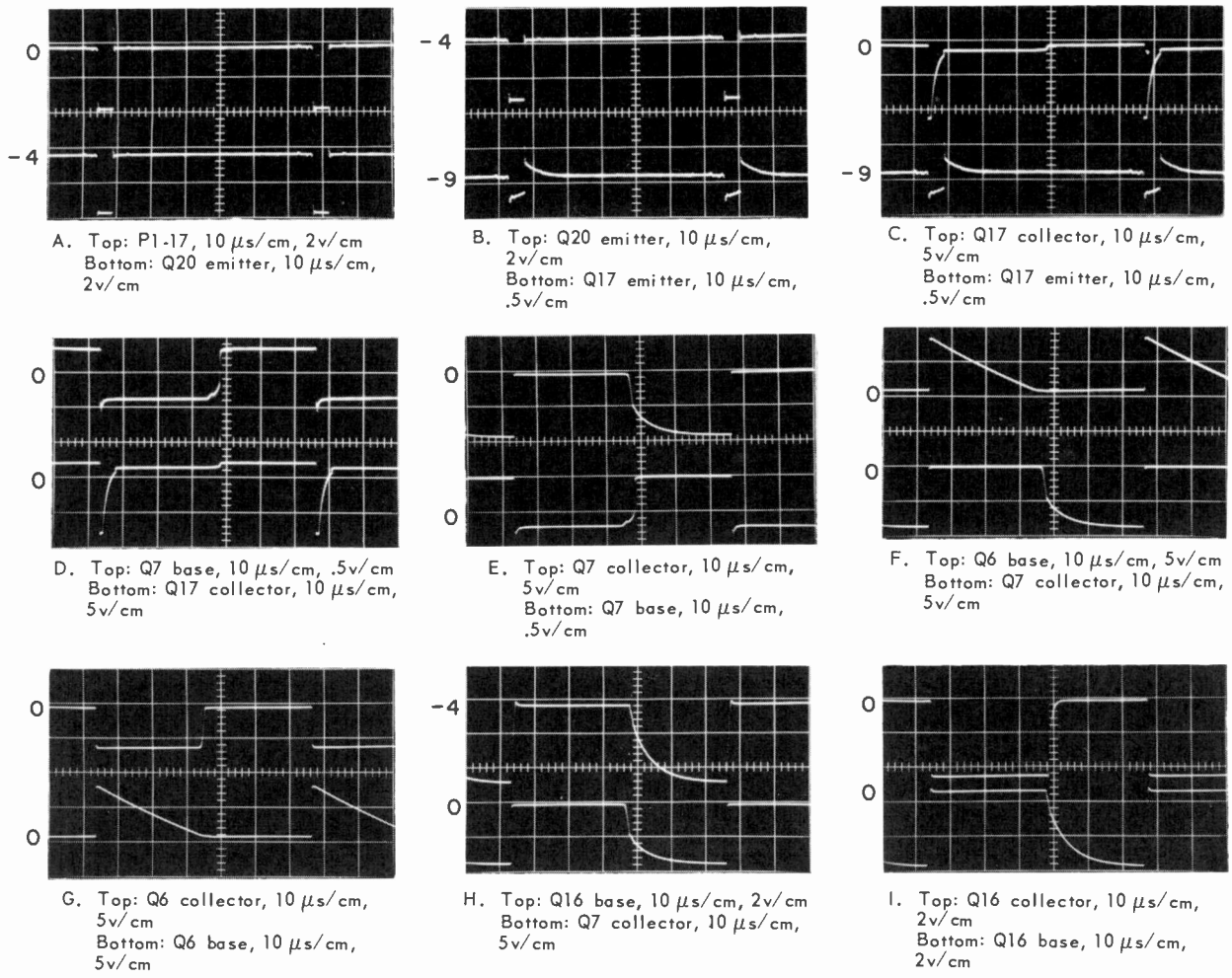


Figure 56—Sync Amplifier, Hor. Square Wave MV and Hor. Square Wave Delay Generator Circuits



A. Top: P1-17, 10 μs/cm, 2v/cm
Bottom: Q20 emitter, 10 μs/cm, 2v/cm

B. Top: Q20 emitter, 10 μs/cm, 2v/cm
Bottom: Q17 emitter, 10 μs/cm, .5v/cm

C. Top: Q17 collector, 10 μs/cm, 5v/cm
Bottom: Q17 emitter, 10 μs/cm, .5v/cm

D. Top: Q7 base, 10 μs/cm, .5v/cm
Bottom: Q17 collector, 10 μs/cm, 5v/cm

E. Top: Q7 collector, 10 μs/cm, 5v/cm
Bottom: Q7 base, 10 μs/cm, .5v/cm

F. Top: Q6 base, 10 μs/cm, 5v/cm
Bottom: Q7 collector, 10 μs/cm, 5v/cm

G. Top: Q6 collector, 10 μs/cm, 5v/cm
Bottom: Q6 base, 10 μs/cm, 5v/cm

H. Top: Q16 base, 10 μs/cm, 2v/cm
Bottom: Q7 collector, 10 μs/cm, 5v/cm

I. Top: Q16 collector, 10 μs/cm, 2v/cm
Bottom: Q16 base, 10 μs/cm, 2v/cm

Figure 57—Typical Waveforms, Sync Amplifier, Hor. Square Wave MV and Hor. Square Wave Delay Generator Circuits

The positive going square wave output on the collector of Q7 is coupled through a steering diode, CR20, to the base of Q16, the horizontal square wave delay generator. The appropriate SYNC TIMING potentiometer (R56 for 525/625-line standards or R76 for 405-line standards) and associated series resistor (R88 or R77) form in conjunction with C32, in the base of Q16, an integrator which delays the square wave. The SYNC TIMING control allows adjustment of the total delay of horizontal sync over a small range so that the leading edge of regenerated horizontal sync can be made to coincide with the leading edge of incoming tape sync. Therefore in the Sync Logic (module B21) when regenerated horizontal sync is combined with the vertical interval of tape sync on 525/625-line standards, the equalizing pulses and the vertical sync pulses will be correctly timed with respect to the horizontal sync pulses. Similarly on 405-line standards, when the regenerated horizontal sync is combined with the vertical sync pulse group interval, the vertical sync pulses will be correctly timed with respect to the horizontal sync pulses.

The emitter of Q16 is fixed at approximately −3 volts, the level at which the input signal is clipped. In the inverted output on the collector of Q16, the positive going excursion is limited at zero volts. Therefore the output signal on the collector of Q16 is a square wave approximately −3 volts. This signal is fed to the sampling pulse clipper, Q5, at a horizontal rate (H) or 15.75 kc on 525-line standards.

Phase Comparator and AFC Current Amplifier

As shown in figure 58, the H rate square wave is coupled through a differentiating network consisting of C10 and R22 to the base of Q5, the sampling

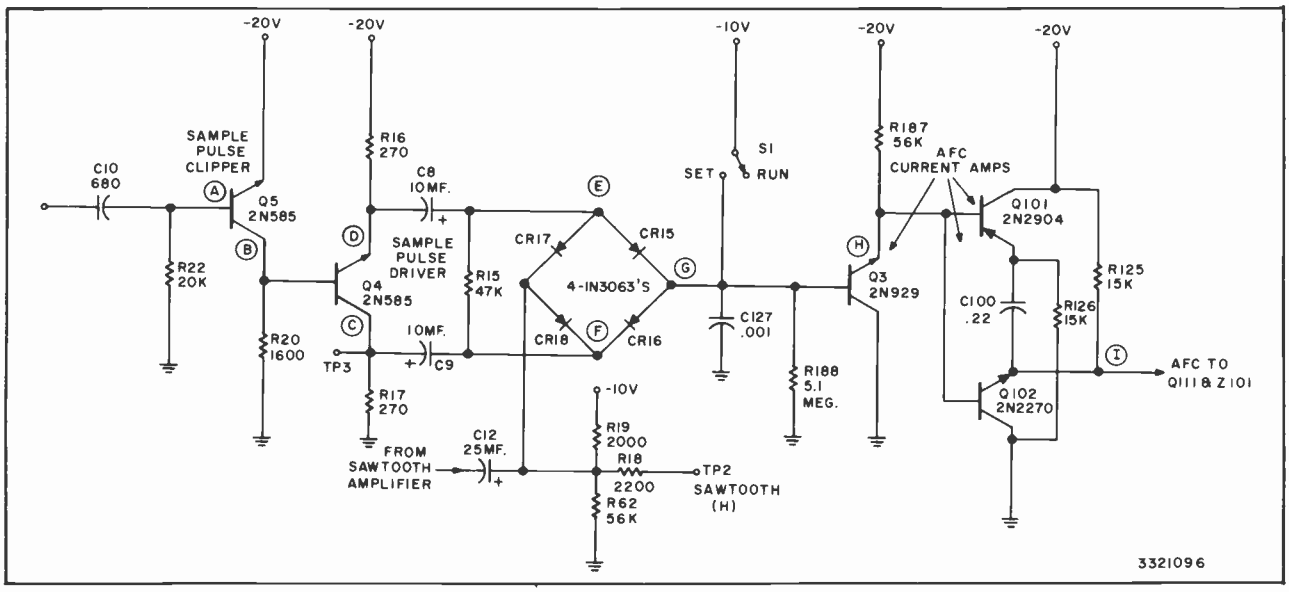
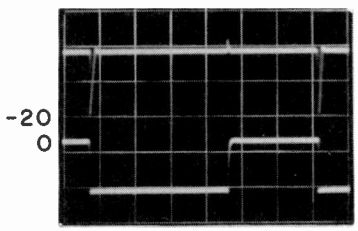
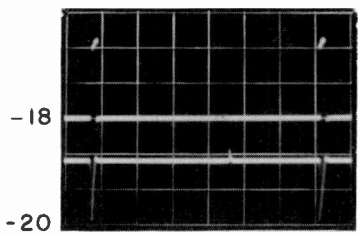


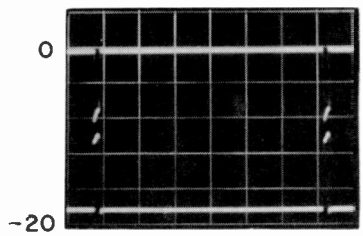
Figure 58—Sampling Pulse Clipper and Driver, Phase Comparator and AFC Current Amplifier



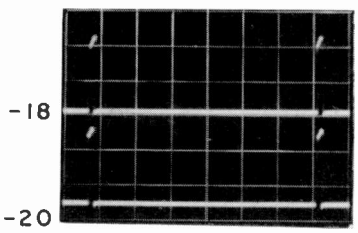
A. Top: Q5 base, 10 μs/cm, 1v/cm
Bottom: Q16 collector, 10 μs/cm, 2v/cm



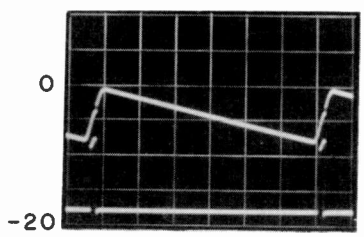
B. Top: Q5 collector, 10 μs/cm, 5v/cm
Bottom: Q5 base, 10 μs/cm, 1v/cm



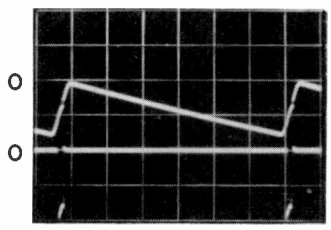
C. Top: Q4 collector, 10 μs/cm, 5v/cm
Bottom: Q4 base, 10 μs/cm, 5v/cm



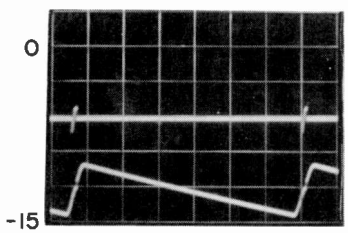
D. Top: Q4 emitter, 10 μs/cm, 5v/cm
Bottom: Q4 base, 10 μs/cm, 5v/cm



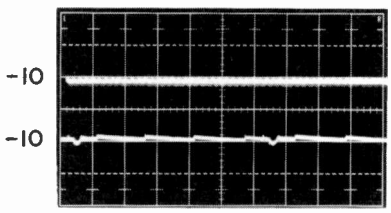
E. Top: CR17, CR18, 10 μs/cm, 5v/cm
Bottom: CR17, CR15, 10 μs/cm, 5v/cm



F. Top: CR17, CR18, 10 μs/cm, 5v/cm
Bottom: CR18, CR16, 10 μs/cm, 5v/cm



G. Top: CR15, CR16, 10 μs/cm, 2v/cm
Bottom: CR17, CR18, 10 μs/cm, 5v/cm



H. Top: Q3 emitter, 5 ms/cm, .2v/cm
Bottom: Q3 emitter, 10 μs/cm, .2v/cm

Figure 59—Typical Waveforms, Sampling Pulse Clipper and Driver Phase Comparator and AFC Current Amplifier

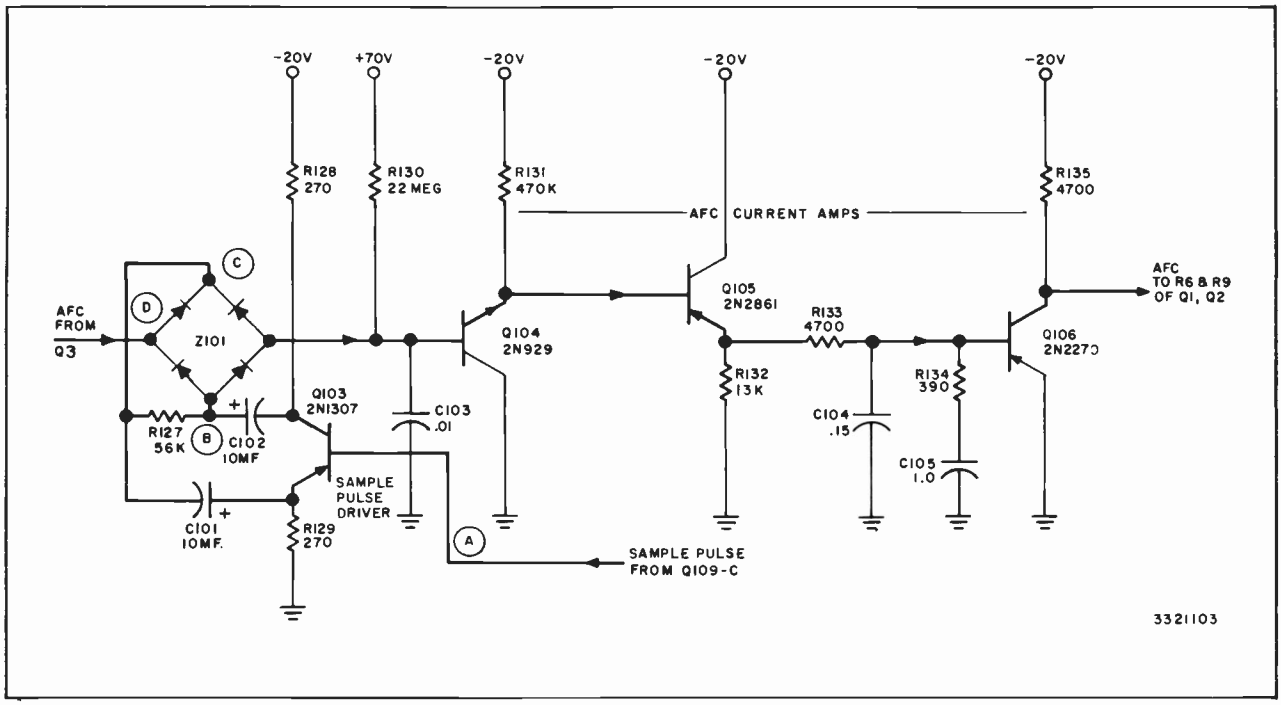
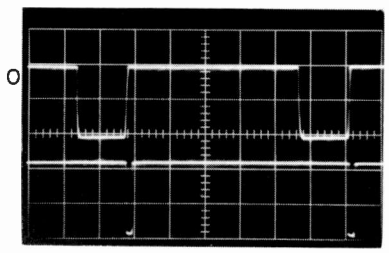
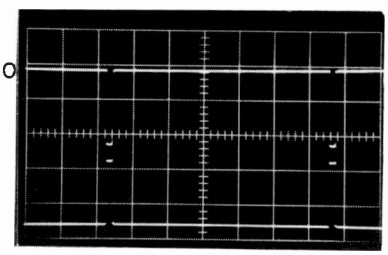


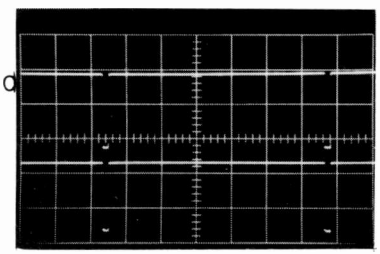
Figure 60—AFC Current Amplifiers



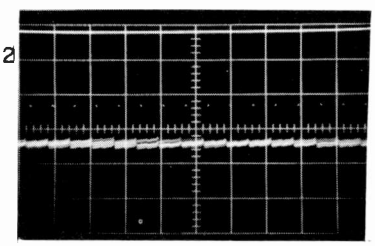
A. Top: Q107 collector, 10 μs/cm, 5v/cm Bottom: Q103 base, 10 μs/cm, 5v/cm



B. Top: Q103 base, 10 μs/cm, 5v/cm Bottom: R127, C102, 10 μs/cm, 5v/cm



C. Top: Q103 base, 10 μs/cm, 5v/cm Bottom: R129, C101, 10 μs/cm, 5v/cm



D. Top: Q103 base, 10 μs/cm, 5v/cm Bottom: Q102 emitter, 100 μs/cm, 1v/cm

Figure 61—Typical Waveforms, AFC Current Amplifiers

pulse clipper. This is a boxcar or pulse narrowing circuit which generates a narrow pulse. The leading edge of this pulse corresponds in time to the leading edge of sync. The positive going portion of the differentiated signal on the base of Q5 is clipped by the diode action of the base-to-emitter junction. The negative portion of this signal triggers the boxcar action of Q5. The positive output pulse on the collector of Q5 is direct-coupled to the base of Q4, the sampling pulse driver.

The sampling pulse driver, Q4, serves as a phase splitter, providing the two out-of-phase signals which are fed to opposite sides of the phase comparator to key the diodes on. The output on the emitter of Q4 is a positive going pulse which is coupled through C8 to the junction of the anodes of CR15, CR17. The output on the collector is a negative going pulse which is coupled through C12 to the junction of the cathodes of CR16, CR18. The horizontal (15.75 kc) sawtooth used in comparing the phase and frequency of the incoming tape sync is coupled through C12 to the junction of the cathode of CR17 and the anode of CR18. The output is taken from the opposite side of the phase comparator, at the junction of the cathode of CR15 and the anode of CR16.

When the driver pulses are applied to the phase comparator, all four diodes become forward biased simultaneously. At the tips of the pulses the diodes conduct, momentarily connecting the input sawtooth voltage across R14 to C7. Capacitor C7 acts as a memory device, storing the instantaneous sawtooth voltage that was passed when the diodes conducted. During the remainder of the horizontal period, the diodes are reverse biased and C7 remains at the clamped voltage. The voltage on C7 sets the operating point for the afc current amplifier, Q3, which supplies the afc bias to the 2H master oscillator, Q1, Q2. The output is taken off the emitter of Q3 and fed to the bases of Q1, Q2.

If the incoming tape sync signal changes frequency or phase slightly, the sampling pulse derived from this signal occurs at a slightly different time relative to the sawtooth voltage applied to phase comparator. Therefore the value of the instantaneous voltage to which C7 charges changes, causing a change in the output current of Q3. As a result, the frequency and phase of the 2H master oscillator, Q1, Q2, is shifted to correspond to that of the incoming tape sync. When the afc loop is operating properly, sampling of the sawtooth voltage takes place on the fast positive going portion of the sawtooth.

Adjustments

The 2H master oscillator, the front porch width, the horizontal sync width and the sync timing control have been set at the factory and they should not be disturbed in the course of normal operation or routine maintenance. However, if component replacement or some other condition makes it necessary to readjust any of these controls, follow the procedure given below.

Recommended Test Equipment and Accessories
Tektronix Type 535 oscilloscope (or equivalent) and low capacity probe Module extender

2H Master Oscillator Adjustment

The oscilloscope or the picture monitor triggered with external sync, can be used to adjust the center frequency of the master oscillator.

Using Oscilloscope

1. Observe the video output on the CRO by pressing VID OUT on the CRO switcher.

2. Press the CRO HOR button and EXT SYNC, on the CRO switcher.

3. With the switch on the PLAY panel in MOD-DEMOD position, and an incoming video signal of the desired line standards, observe the outgoing video on CRO.

4. Press and hold the AFC OFF pushbutton (switch S1) on the front of the horizontal AFC module. Adjust the appropriate 2H FREQ control, until the pattern on the CRO is as nearly stationary as possible. The upper control on the module is for 525/625 and the lower control 405 or 819 lines. Release the pushbutton.

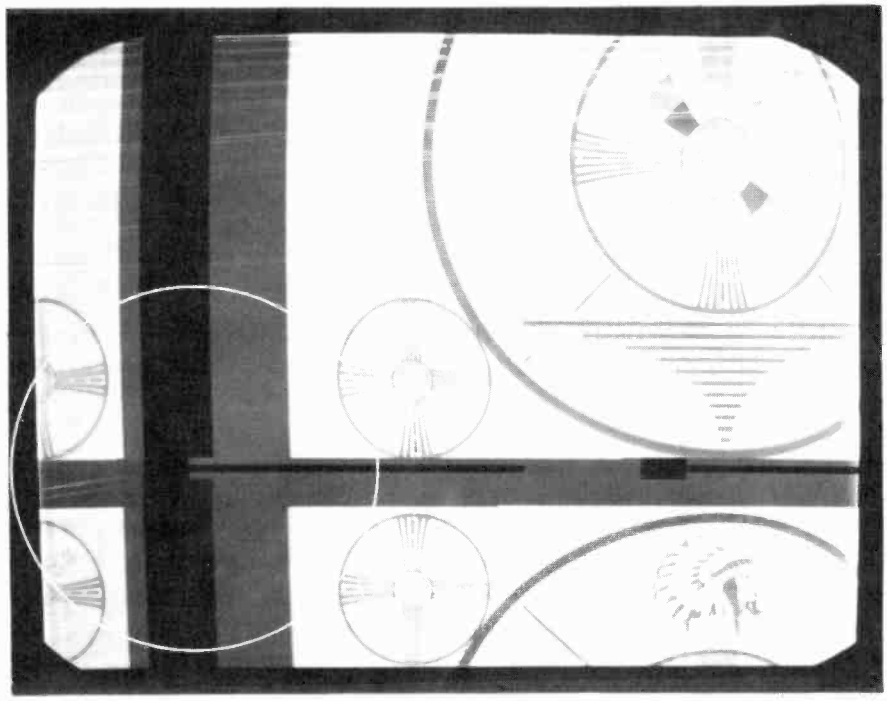
Using Picture Monitor

1. Observe the video output on the picture monitor by pressing VID OUT on the monitor switcher.

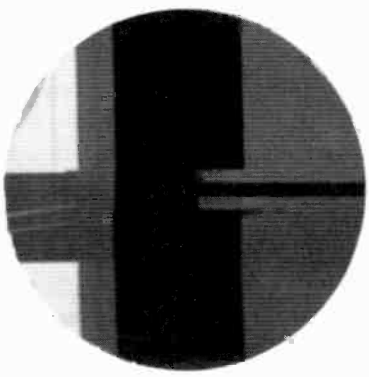
2. Repeat step 4 above but observe the picture monitor while making the adjustment.

NOTE: To make the remaining internal adjustments, the Horizontal AFC module should be mounted in the extender. In addition, the adjustments require the use of an external oscilloscope such as the Tektronix 535A. Dual trace is at times desirable. Refer to the chart below for various pulse widths for different standards. Individual minor changes due to local requirements may be made.

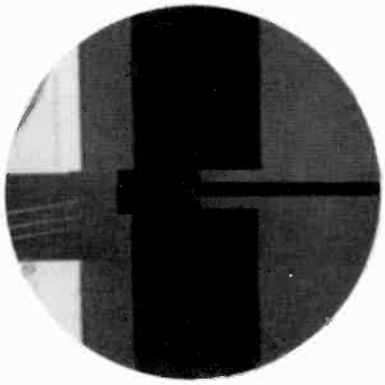
PULSE CROSS PRESENTATION



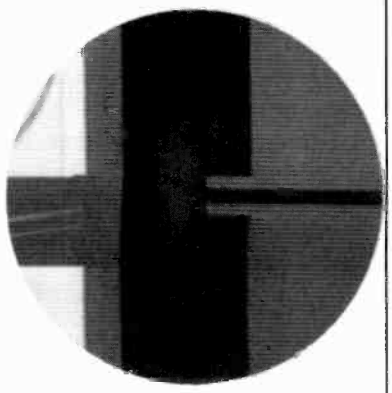
a. Normal Test Pattern (Picture Monitor)



b. Misadjusted Sync Gate Width Control, R-32 (Sync Logic Module 230B)



c. Misadjusted Sync Timing Adjustment Control, R-56 (Horizontal AFC Module 227B)



d. Normal Sync Timing

Figure 62—Adjustment of Sync Forming Circuits (Picture Monitor)

Pulses	*Line Standard*		
	405	*525*	*625*
Hor. Sync	9.25	4.75	4.9
Hor. Blanking	18.0	11.0	11.85
Front Porch	1.56	1.5	1.4
Vert. Blanking	1425	1250	1290
(Times are in microseconds)			

Front Porch Width

1. Mount the Horizontal AFC module in an extender and insert it in the TR-4. Connect the oscilloscope probe to one of the three video output test points (VID 1, VID 2, VID 3) on the front panel of the Video Output (module A22). Adjust the oscilloscope to display a horizontal blanking interval, appropriate to the line standard in use.

2. Adjust the appropriate FRONT PORCH WIDTH control (R37 or R69) to obtain the proper front porch width as described below:

(a) For 525 lines, adjust R37 so that the front porch is 1.5 microseconds wide.

(b) For 625 lines, adjust R37 so that the front porch is 1.4 microseconds wide.

(c) For 405 lines, adjust R69 so that the front porch is 1.56 microseconds wide.

Horizontal Sync Width

1. Mount the Horizontal AFC module in an extender and insert it in the TR-4. Connect the oscilloscope probe to one of the three video output test points (VID 1, VID 2, VID 3) on the front panel of the Video Output (module A22). Adjust the oscilloscope to display a horizontal blanking interval, appropriate to the line standard in use.

2. Adjust the appropriate HOR SYNC WIDTH control (R45 or R71) to obtain the proper horizontal sync width as described below:

(a) For 525 lines, adjust R45 so that the sync pulse is 4.75 microseconds wide.

(b) For 625 lines, adjust R45 so that the sync pulse is 4.9 microseconds wide.

(c) For 405 lines, adjust R71 so that the sync pulse is 9.25 microseconds wide.

Sync Timing

Mount the Horizontal AFC module in an extender and insert it in the TR-4. Select the pulse cross for display on the picture monitor, as shown in A figure 62. Observe the pulse cross area on the monitor; an indentation in the leading edge of the signal (B, figure 62) indicates tape sync and output sync are not in coincidence. If this condition exists, adjust the appropriate SYNC TIMING control (R56 for 525/625 lines or R76 for 405 lines) until the indentation is eliminated (C, figure 62) indicating that tape sync and output sync are in phase.

Vertical Advance Module B22
IB-31818, Pages 102, 104, 105

Under *Adjustments,* delete the existing text; in its place use the following:

Recommended Test Equipment and Accessories
Tektronix Type 535 oscilloscope (or equivalent) and low capacity probe.
Module extender.

Adjustments

Stability Test of Counter Multivibrators

The STABILITY RANGE control, potentiometer R41, and the STABILITY TEST control, pushbutton switch S1, are mounted on the front of the Vertical Advance module. When the STABILITY TEST pushbutton is pressed, a variable voltage can be applied to the counter circuits by rotating the STABILITY RANGE knob. When this voltage is varied (±.5 volt) the stability of the counters is determined. This voltage variation simulates a frequency error in the multivibrators. If each is operating correctly, no change takes place in the multivibrator operation. However, if a multivibrator is bordering on improper operation, rotating the STABILITY RANGE potentiometer knob will cause it to go into improper operation.

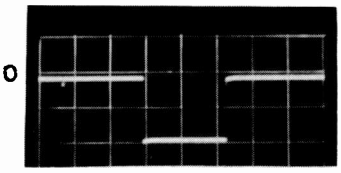
The 3.5H pulse (see waveform below) is used to detect any improper operation of the Vertical Advance counters. The procedure for checking the counters is given below.

1. Place the TR-4 in STANDBY or in STOP mode. Remove the Modulator (module A2); place the MOD-PLAY (S4) in MOD position then replace the Modulator.

2. Connect an oscilloscope to the 3.5H test point (TP5) on the front of the module.

3. Set the oscilloscope sweep time to vertical rate and expand the trace to observe the 3.5H pulse. (See waveform below.)

4. Press and hold the STABILITY TEST pushbutton; then rotate the STABILITY RANGE control



through its entire range. The pulse width and amplitude should not change in any respect. Minor disturbances appearing on the base line do not indicate improper operation. If the pulse width or amplitude change while the control is being rotated, the counters must be readjusted.

Adjustment of Counters

The counters, the 3.5H pulse, and the start pulse in the Vertical Advance module form a continuous loop which makes it difficult, when a marginal counter is indicated, to determine which counter is at fault. The following procedure provides a method for identifying and correcting a marginal or defective counter.

Since the use of a single trace oscilloscope is assumed in the following procedure, it will be necessary to change the sweep of the oscilloscope as the adjustments progress in order to maintain the various counter signals within the 10 cm display of the CRO. However, with a dual trace oscilloscope inspection of the signals is somewhat simplified, since the output of each counter may be compared directly to the output of the preceding stage. This makes it unnecessary to set the sweep at an arbitrary 10 cm.

To perform the following adjustments, the module under test must be mounted in an extender.

NOTE: The adjustments described in step 1 (below) is a precautionary measure. This step may be omitted provided it is ascertained that the Horizontal AFC module is functioning properly.

1. In the *Horizontal AFC module* set the oscilloscope on internal trigger. Place the probe on the emitter of Q8. (This is the source of 31.5 kc pulses from the 2H master oscillator, Q1, Q2, to the ÷2 multivibrator, Q9, Q10.) Adjust the oscilloscope sweep so that two 31.5 kc pulses cover 10 cm on the oscilloscope. Then move the probe to the ÷2 test point, TP1. One cycle of the ÷2 MV should be 10 cm wide; if not, a failure in the Horizontal AFC module is indicated. This must be corrected before adjusting the counters in the Vertical Advance module. See *2H Master Oscillator* under *Adjustments* at end of *Horizontal AFC module* description.

2. In the *Vertical Advance module,* disconnect the collector lead of Q2 from the terminal at the junction of CR2 and R4; leave the jumper and CR2 connected to the terminal. (This opens the loop and allows the counters to run freely.)

3. Set the oscilloscope on internal trigger. Locate C1 which is connected to the base of Q1 and place the probe on the input side of C1. The CRO display will show the 31.5 kc input signal.

4. Adjust the sweep so that seven 31.5 kc pulses cover 10 cm on the oscilloscope. Then move the probe to the ÷7 test point, TP1. One cycle of the ÷7 MV (Q3, Q10) should be 10 cm (seven 31.5 kc pulses) wide. If it is not, adjust R7, the ÷7 MV "trim-pot", until the cycle measures 10 cm.

5. Press and hold the STABILITY TEST pushbutton, and rotate the STABILITY RANGE control through its range. The width of the ÷7 cycle should not change.

6. Set the oscilloscope sweep so that five ÷7 pulses cover 10 cm on the oscilloscope. Place the probe on the first ÷5 test point, TP2. One cycle of the first ÷5 MV (Q5, Q11) should be 10 cm (five ÷7 pulses) wide. To obtain this it may be necessary to adjust the ÷5 "trim-pot", R20. If so, repeat step 5, this time observing the width of the ÷5 cycle, which should not vary.

7. Change the oscilloscope sweep so that five ÷5 pulses cover 10 cm on the oscilloscope. Place the probe on the second ÷5 test point, TP3. One cycle of the second ÷5 MV (Q6, Q12) should be 10 cm wide (the width of five of the first ÷5 pulses). If it is not, adjust the second ÷5 "trim-pot", R49, then repeat step 5 in order to determine the stability of the second ÷5 counter.

8. Change the oscilloscope sweep so that three of the second ÷5 pulses cover 10 cm on the oscilloscope. Place the probe on the ÷3 test point, TP4. One cycle of the ÷3 MV (Q7, Q13) should be 10 cm wide (the width of three of the second ÷5 pulses). If not, adjust the ÷3 "trim-pot", R52, and again perform step 5 to determine the stability of the ÷3 counter.

9. Reconnect the collector of Q2 to the terminal, and replace the module in the tape recorder/player.

10. Refer to the first section of this procedure, *Stability Test of Counter Multivibrators,* and recheck the stability of the counters according to the instructions in steps 1 through 4.

NOTES

1. Proper counter operation is necessary but not sufficient to insure proper vertical advance. In some cases proper counting may be obtained with the collector of Q2 disconnected; however, when the loop is closed again by reconnecting Q2, improper advance is obtained. This condition results from improper off-time width of one of the counters, usually the second ÷5 MV (Q6, Q12). To detect the offending counter, locate the leading edge of the 3.5H pulse (which will be much wider than normal). The leading edge lines up with the turnoff edge of the offending counter. When the counter has been located, readjust its timing so as to lengthen its period. A point will be found where the counting chain jumps suddenly into proper operation. Continue to lengthen its period until the counter-chain holds to proper count throughout the entire range of the STABILITY RANGE control.

2. A condition may occur in the Vertical Advance module in which a blanking bar is generated only on alternate fields instead of on every field. This results from having ÷3 MV adjusted for an excessively long time constant. The multivibrator cannot recover in time to be retriggered by the start pulse; therefore, it waits for one entire field before being retriggered. To eliminate this condition, simply readjust the ÷3 circuit "trimpot", R52, to shorten the time constant, then check the final setting to be certain that the counter passes the STABILITY TEST.

3. Sometimes a condition occurs in which the Horizontal AFC module produces regenerated sync at 31.5 kc instead of 15.75 kc. A common cause of this fault is a shorted regulator transistor (Q14) in the Vertical Advance module. A quick check for this fault can be made by measuring the −10 volt bus in the Vertical Advance module. If transistor Q14 is shorted, the bus is at a more negative potential than −10 volts.

IB-31818, Page 108

Under *Sync Logic (Module B21),* delete all text, schematics, and waveforms. In place of the deleted material, use the following:

Sync Logic Module B21

General

In the following discussion the 525 line system will be discussed with appropriate notes or comments added to cover the 405, 625, and 819 line system as required. The numbers in parentheses, in the 525 line discussion, indicate that these values will probably change for other line standards. A few examples are given in the following table:

	525	*405*	*625*
Vert. Advance	3.5H	1.5H	3.0H
Vert. Gate	9.0H	4.0H	7.5H
Vert. Blanking	21.0H	15.0H	25.0H
2H	31.5 Kc/s	20.25 Kc/s	31.25 Kc/s

The Sync Logic module (figure 63) provides signals for the operation of the Vertical Advance module as well as signals for the Video/FM Control, Video Output, and color modules. When triggered by the leading edge of the vertical advance (3.5H) pulse, which is generated in the Vertical Advance module, the Sync Logic module regenerates vertical blanking and reinserts the vertical sync interval. The signals supplied by this module include the start pulse for the Vertical Advance module, regenerated sync for the Video Output and the Video/FM Control modules, and also for the latter, regenerated horizontal and vertical blanking. For international standards, the Sync Logic module produces counterparts of the start pulse and the regenerated horizontal and vetrical blanking signals, characteristic of 405- and 625-line operation. Similarly, the timing of the vertical advance trigger pulse is also changed to accommodate the different TV line rates. For 625-line standards this pulse is 3H wide, and for 405-line standards the width is 1.5H. The Sync Logic module is also capable of operation on 819-line standards in lieu of 405-lines, by making a slight modification to the existing circuitry.

Standards Switching (International Machines Only)

Since the width of the regenerated horizontal and vertical blanking pulses and the timing of the start pulse is a function of the time constant components in the blanking mixer and start pulse generator circuits, respectively, switchable time constant components are used in these stages. The time constant components used for 525- and 625-line standards are the same, but those for 405-line standards are different. The time constant components, appropriate to the TV line standard in use, are electronically switched into their respective circuits by means of the HN and HI busses. These busses furnish a dc control voltage and when one is at −20 volts the other is at ground. The potential that either bus is at depends upon the TV line standard selected.

The desired TV line standard is selected by means of TV STANDARDS switch, which is located on the

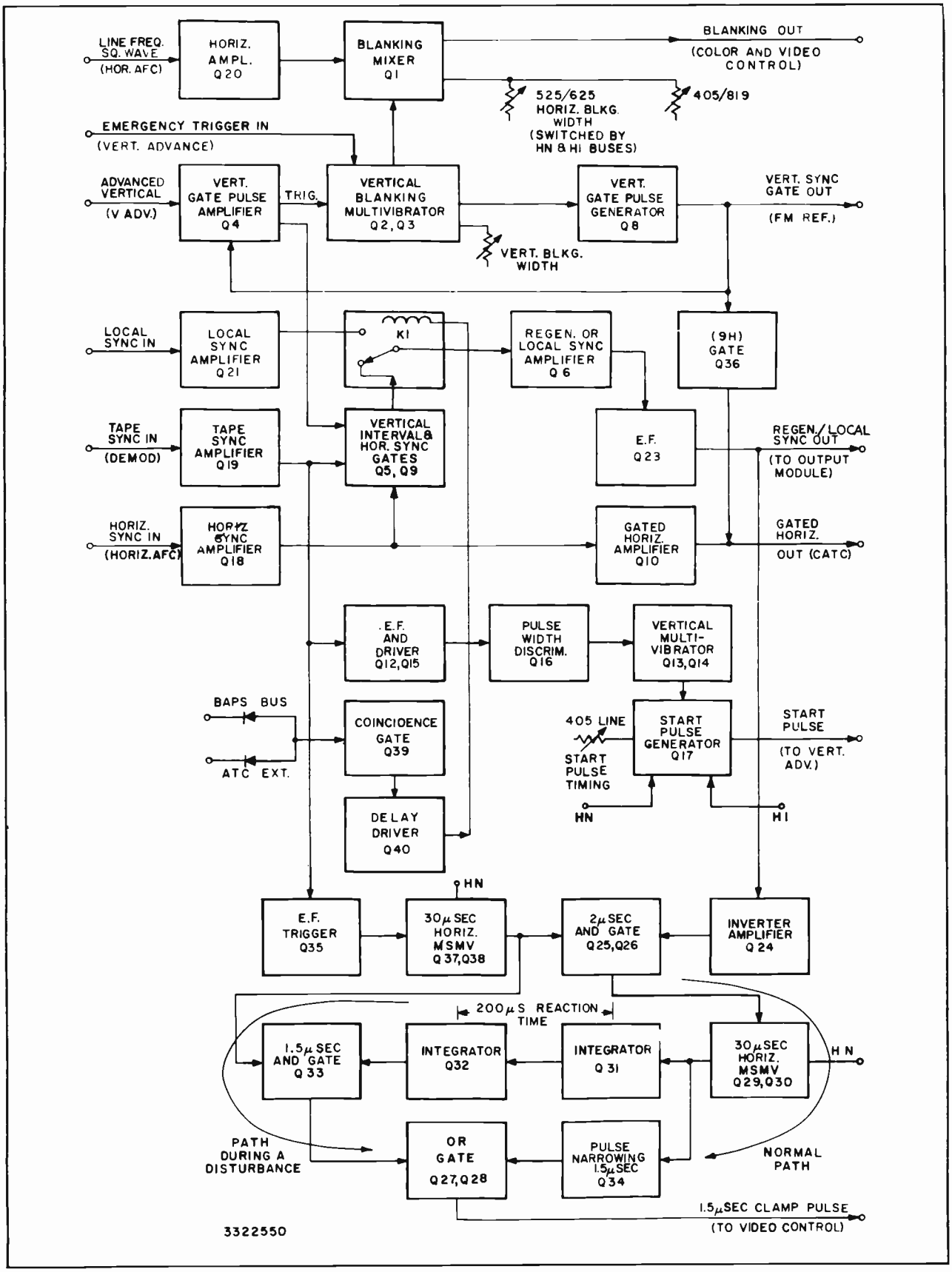


Figure 63—Block Diagram for Sync Logic Module B21

front panel of the international Vertical Advance (module B22). When 525- or 625-line operation is selected, −20 volts is applied to the HN bus and the HI bus goes to zero or ground. This switches the 525/625-line time constant components into the circuit, while simultaneously disabling the 405-line time constant components. When 405-line operation is selected, the opposite is true. The HN bus goes to ground and the HI bus is at −20 volts. Thus the 405-line time constant components are activated and those used for 525/625-line standards are disabled. Isolation diodes are connected in series with the HN and HI busses to prevent the −20 volts on the active bus from feeding back to the inactive bus.

Circuits

Vertical Blanking Generator

The vertical blanking multivibrator, transistors Q, Q3, (figure 64) form a monostable multivibrator with Q2 on and Q3 off in the stable state. The multivibrator changes state when a positive going trigger pulse is applied to the base of Q2 through C4, isolation diode CR3, and C3. The normal trigger for the vertical blanking multivibrator is the leading edge of the 3.5H pulse, which is obtained from the collector of Q4, the vertical pulse amplifier. On 625-line standards this pulse is 3H, and on 405-line standards, 1.5H. Transistor Q2 remains off and Q3 on for the length of time determined by the charging time of C3 through potentiometer R7, the VERT BLKG WIDTH control, and R52. The VERT BLKG WIDTH potentiometer, a screwdriver adjustment on the front panel, is adjusted so that the width of the vertical blanking output pulse on the collector of Q3 is approximately 21H. For 625- and 405-line standards, this control is set for a pulse width approximately 25H and 15H, respectively. The output on the collector of Q3 is fed through isolation diode CR2 to the blanking mixer, Q1, (described later) and to the base of Q8, the vertical gate pulse (9H) generator.

The 9H generator, Q8, is a pulse narrowing circuit or boxcar which derives a 9H output pulse from the 21H input pulse. The input pulse is applied to the base of Q8 across R34 and a differentiator consisting of C42, R31, and R32, the VERT GATE WIDTH potentiometer. The latter, an internal control, is adjusted so that the trailing edge of the 9H pulse falls half-way between the last equalizing pulse and the first horizontal pulse on an even field. The 9H pulse output on the collector of Q8 is coupled through isolation diode CR9 and is then combined with the 3.5H pulse from the Vertical Advance module. The combined pulse is fed through C17, R37 to Q9, the horizontal sync gate, (described later) and through C6, R17 to the base of Q4, the vertical gate pulse

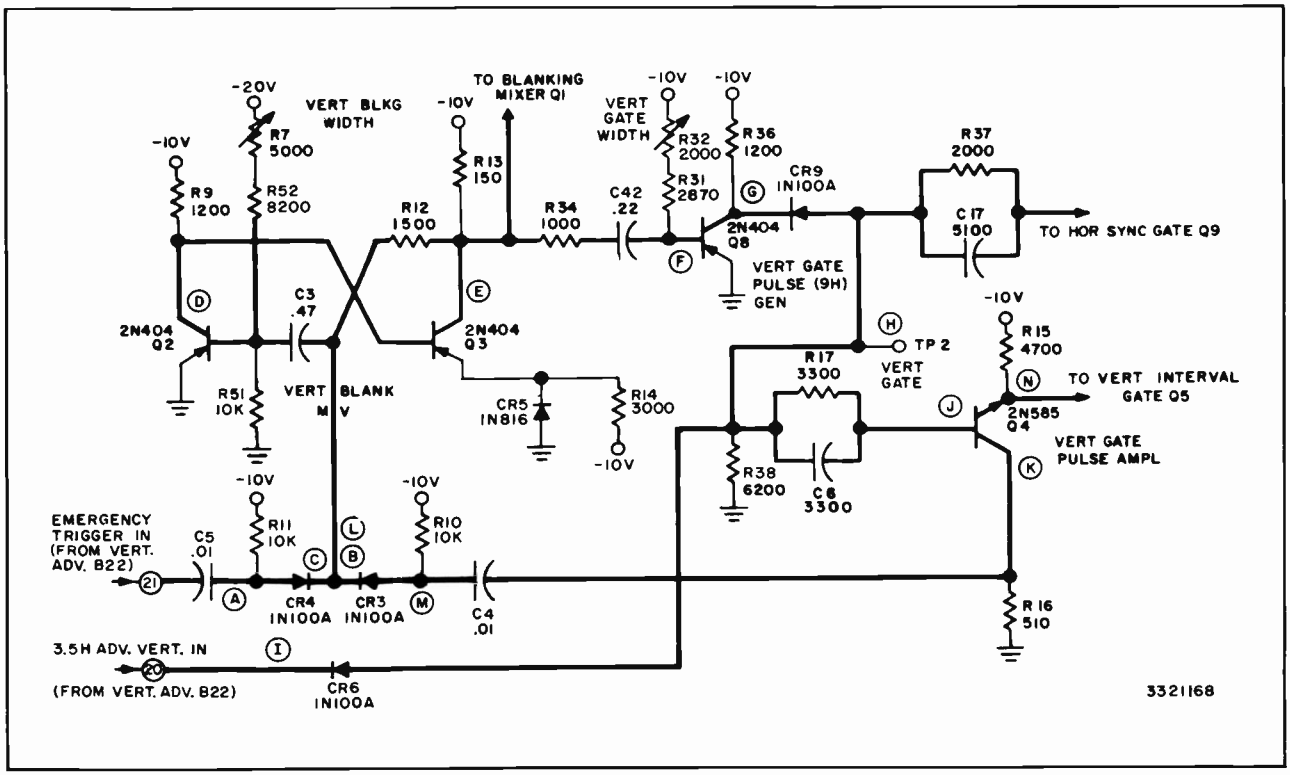
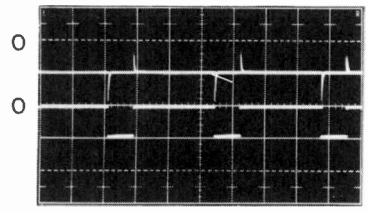
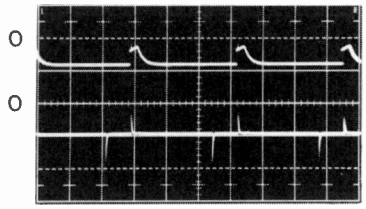


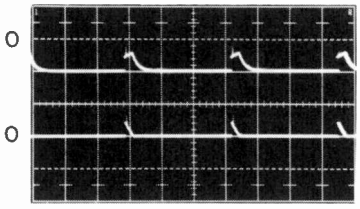
Figure 64—Vertical Blanking MV, Vertical Gate Pulse Generator and Amplifier Circuits



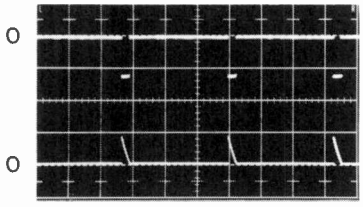
A. Top: CR4 anode, 5 ms/cm, 10v/cm
Bottom: P1-21, 5 ms/cm, 10v/cm



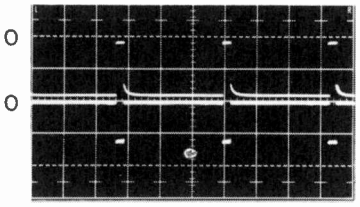
B. Top: CR4, CR3 cathode, 5 ms/cm, 10v/cm
Bottom: CR4 anode, 5 ms/cm, 10v/cm



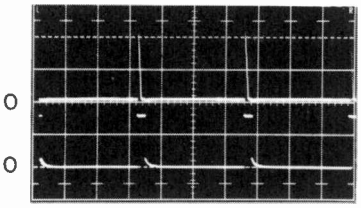
C. Top: CR4, CR3 cathode, 5 ms/cm, 10v/cm
Bottom: Q2 base, 5 ms/cm, 10v/cm



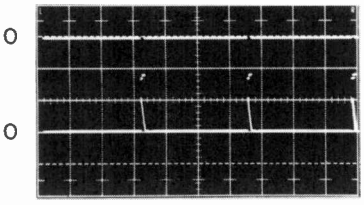
D. Top: Q2 collector, 5 ms/cm, 1v/cm
Bottom: Q2 base, 5 ms/cm, 5v/cm



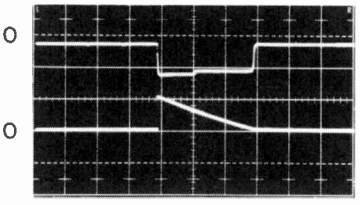
E. Top: Q3 collector, 5 ms/cm, 5v/cm
Bottom: Q3 base, 5 ms/cm, 1v/cm



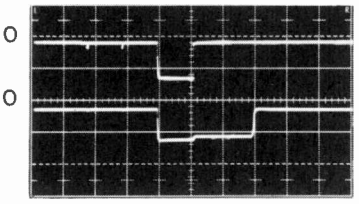
F. Top: Q8 base, 5 ms/cm, 2v/cm
Bottom: Q3 collector, 5 ms/cm, 5v/cm



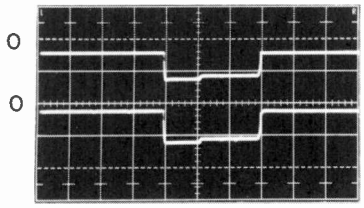
G. Top: Q8 collector, 5 ms/cm, 5 v/cm
Bottom: Q8 base, 5 ms/cm, 5v/cm



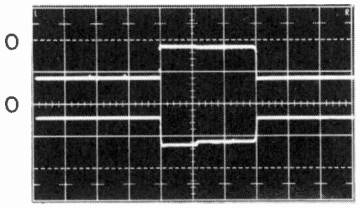
H. Top: TP2, 200 μs/cm, 5v/cm
Bottom: Q8 base, 200 μs/cm, 5v/cm



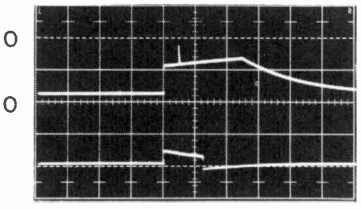
I. Top: CR6 cathode, 200 μs/cm, 5v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



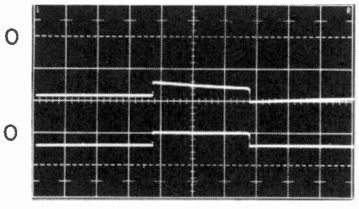
J. Top: Q4 base, 200 μs/cm, 5v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



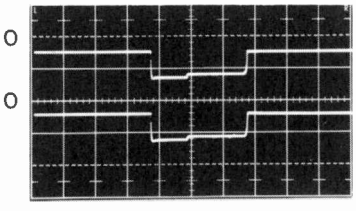
K. Top: Q4 collector, 200 μs/cm, 2v/cm
Bottom: Q4 base, 200 μs/cm, 5v/cm



L. Top: CR3, CR4 cathode, 500 μs/cm, 5v/cm
Bottom: CR3 anode, 500 μs/cm, 5v/cm



M. Top: CR3 anode, 200 μs/cm, 5v/cm
Bottom: Q4 collector, 200 μs/cm, 5v/cm



N. Top: Q4 emitter, 200 μs/cm, 5v/cm
Bottom: Q4 base, 200 μs/cm, 5v/cm

Figure 65—Typical Waveforms, Vertical Blanking MV, Vertical Gate Pulse Generator and Amplifier

amplifier. It should be noted that the leading edges of both pulses are in coincidence, therefore the resultant pulse is still 9H wide.

This same generator (Q8) produces a 7.5H pulse from the 25H input pulse for 625-line standards, and a 4H pulse from a 15H input pulse for 405-line standards. For 625-line standards, the same relative timing applies to the VERT GATE WIDTH adjustment of the 7.5H pulse, as that of the 9H pulse on 525-line standards. On 405-line standards, however, there are no equalizing pulses; therefore the VERT GATE width control is adjusted so that the trailing edge of the 4H pulse occurs 4 microseconds after the trailing edge of the last broad pulse in the vertical sync pulse group interval. In the case of 625-line standards, the pulses being combined would be 7.5H and 3H, and those for 405-line standards would be 4H and 1.5H.

Two outputs are taken from Q4, the vertical gate pulse amplifier, one off the emitter and the other off the collector. The signal on the emitter is direct coupled to the base of Q5, the vertical interval gate (described later). The output on the collector is coupled through C4, isolation diode CR3, and C3 to the base of Q2, one half of the vertical blanking multivibrator.

> NOTE: The difference in pulse widths with respect to the various line rates was established in the preceding part of this discussion. In the discussion of the Emergency Trigger and the Sync Reassembly circuits which follow, no mention will be made of the timing of these pulse on international standards. The circuit analysis, however, is valid for all standards.

Emergency Trigger

As previously mentioned, the positive-going edge of the 3.5H pulse on the collector of Q4 is normally used to trigger the vertical blanking multivibrator, Q2, Q3 (figure 64). The emergency trigger pulse is a positive-going signal from the ÷3 multivibrator in the Vertical Advance module and appears simultaneously with the negative-going (trailing edge) of the 3.5H pulse at the base of Q2. During normal conditions of operation, this pulse has no effect on Q2, Q3 which has already been triggered by the leading edge of the 3.5H pulse and remains in that state for 21H. However, under unusual operating conditions due to a non-synchronous switch or a bad splice in the tape, the vertical sync period the tape sync signal may arrive at a much later time. As explained in the description of the Vertical Advance module, the leading edge of the 3.5H pulse is coincident with the second vertical sync pulse, but since the second vertical sync pulse is delayed, the trailing edge of 3.5H will be delayed. Therefore, the 3.5H pulse will be much longer than 3.5H. This lengthened 3.5H pulse holds the vertical interval gate, Q5, open allowing tape sync to pass. When the vertical sync does arrive, a start pulse is generated at the leading edge of the second vertical sync pulse, resulting in the termination of the lengthened 3.5H pulse. This trailing edge of the lengthened pulse is negative-going and does not trigger Q2, Q3 which has returned to its stable state, 21H after the leading edge of the 3.5 pulse.

If there were no emergency trigger, the vertical interval gate, Q5, would close, cutting off the remainder of the vertical interval. However, the positive-going emergency trigger coincident with the trailing edge of the lengthened 3.5H pulse does trigger Q2, Q3, which in turn triggers the vertical gate pulse (9H) generator, Q8. The 9H pulse holds the vertical interval gate open for the remainder of the vertical interval, minimizing the "roll" in the picture.

Sync Reassembly

In the reassembly of sync, the 3.5H and 9H combined signal appearing at the junction of CR9, C17, and R37 is fed to the base of the horizontal sync gate, Q9, and the similarly combined signal from the emitter of Q4 is fed to the base of the vertical interval gate, Q5 (figure 66). Since the leading edges of the 3.5H pulse and the 9H pulse are in coincidence when they are added or combined, the resultant pulse is still 9H wide under normal operating conditions.

Regenerated horizontal sync pulses, which originate in the Horizontal AFC (module A20), are fed to the base of the horizontal sync amplifier, Q18, an emitter follower. The output pulses on the emitter of Q18 are coupled through a network consisting of C9, C38, and R87 and fed simultaneously to the collector of Q9 and to the base of the gated horizontal amplifier, Q10.

Incoming tape synce, which is derived in the sync separator circuit in the Demodulator Output (module A18), is coupled through C30 to the base of the tape sync amplifier, Q19, an emitter follower. The tape sync is applied via a terminal on the Horizontal AFC module that is common to the sync input for the latter and the Sync Logic module. The emitter follower configuration of Q19 provides isolation and a low source impedance for the succeeding stages. The tape sync output on the emitter of Q19 is split into two branches. In one, the signal is coupled through C43 to the base of Q12, an emitter follower which serves as the input to the start pulse generator circuit. (This circuit will be discussed later.) The signal in the other branch is coupled through a net-

work comprised of C8, R89, C37, and R86 to the collector of Q5, the vertical interval gate.

The vertical interval gate, Q5, and the horizontal sync gate, Q9, are normally biased so that Q5 is saturated and Q9 is cut off. With the two gates in this state, the tape sync pulses being applied to the collector of Q5 are shorted out, and the regenerated horizontal sync pulses being applied to the collector of Q9 are fed through isolation diode CR10 to the emitter of a common base amplifier, Q22. The regenerated horizontal sync appearing on the collector of Q9 is also present on the base of the gated horizontal amplifier, Q10. The amplified output on the collector of Q10 is not utilized, however, unless the TR-4 is equipped with the optional color ATC system.

During the vertical interval, the state of Q5 and Q9 is reversed. The 9H pulse on the base of Q5 cuts off this transistor, and the tape sync pulses on the collector pass through isolation diode CR7 through relay K1 contact Q6 to the base of the regenerated sync amplifier. At the same time, the 9H pulse on the base of Q9 drives this transistor into saturation, and the regenerated horizontal sync being applied to the base of Q9 and the base of Q10 is shorted out.

As a result of the on-off switching action between Q5 and Q9, tape sync is passed, and regenerated sync shorted out, during the 9H pulse interim. This is the period in the vertical blanking interval when equalizing, vertical sync, and equalizing pulses are present. During the remainder of the vertical blanking interval, regenerated horizontal sync pulses are passed.

Capacitor C11, R22, R94, and CR8 in the collector-base circuit of Q6 prevent this transistor from being driven into saturation. Diode CR11 in the emitter circuit provides a bias which insures that Q6 will be cut off during the absence of a pulse input. The amplified sync output on the collector of Q6 is fed through R96 to the base of Q23, an emitter follower. Transistor Q23 is used for isolation purposes and the sync output on the emitter is fed to the Video/FM Control (module A21) and the Video Output (module A22). There is also a second output to Q24.

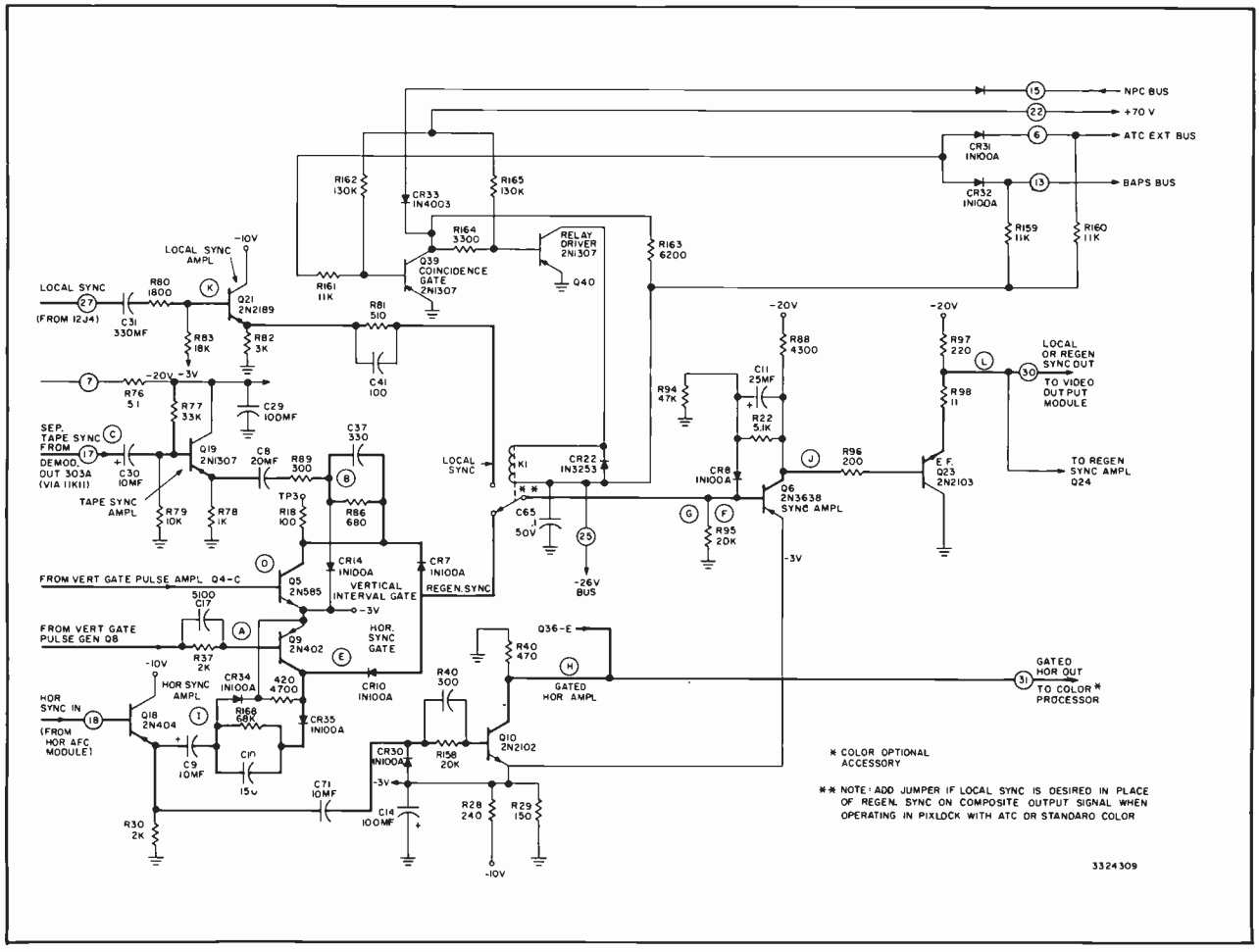
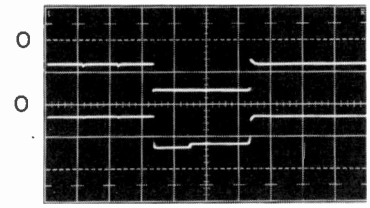
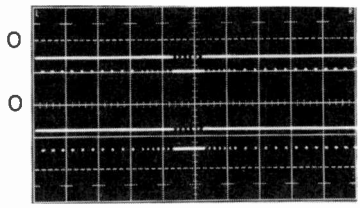


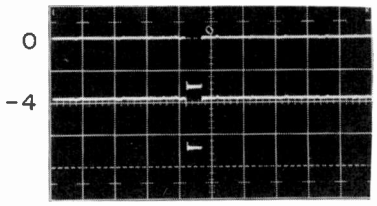
Figure 66—Vertical Interval, Horizontal Sync Gate and Amplifier, Regen. Sync Adder and Gated Hor. Amplifier



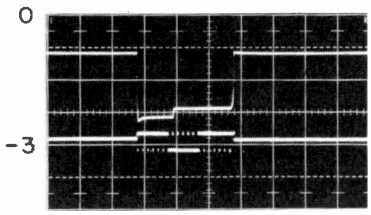
A. Top: Q9 base, 200 μs/cm, 2v/cm
Bottom: TP2, 200 μs/cm, 5v/cm



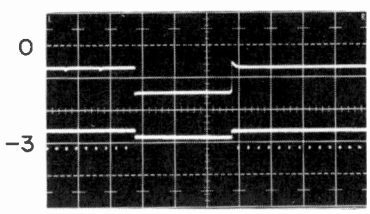
B. Top: CR14 anode, 200 μs/cm, 5v/cm
Bottom: Q19 emitter, 200 μs/cm, 5v/cm



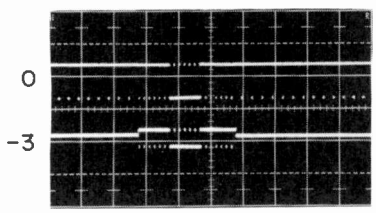
C. Top: P1-17, 10 μs/cm, 2 v/cm
Bottom: Q19 emitter, 10 μs/cm, 2v/cm



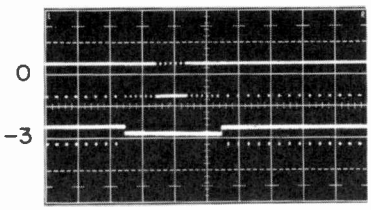
D. Top: Q5 base, 200 μs/cm, 2v/cm
Bottom: Q5 collector, 200 μs/cm, 1v/cm



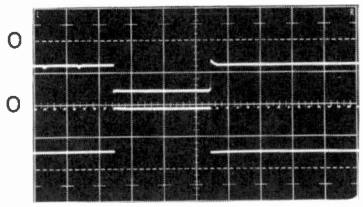
E. Top: Q9 base, 200 μs/cm, 2v/cm
Bottom: Q9 collector, 200 μs/cm, 1v/cm



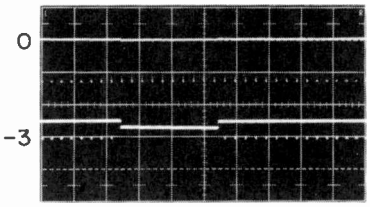
F. Top: Q6 base, 200 μs/cm, 2v/cm
Bottom: Q5 collector, 200 μs/cm, 1v/cm



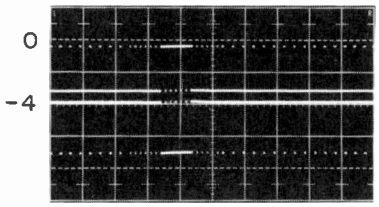
G. Top: Q6 base, 200 μs/cm, 2v/cm
Bottom: Q9 collector, 200 μs/cm, 1v/cm



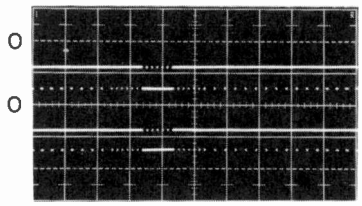
H. Top: Q9 base, 200 μs/cm, 2v/cm
Bottom: Q10 collector, 200 μs/cm, 2v/cm



I. Top: Q18 emitter, 200 μs/cm, 5v/cm
Bottom: Q9 collector, 200 μs/cm 1v/cm



J. Top: Q6 collector, 200 μs/cm 10v/cm
Bottom: Q19 base, 200 μs/cm, 2v/cm



K. Top: Q21 base, 200 μs/cm, 5v/cm
Bottom: Q19 base, 200 μs/cm, 5v/cm

Figure 67—Typical Waveforms, Vertical Interval, Hor. Sync Gate and Amplifier, Regenerated Sync Adder and Gated Hor. Amplifier

The diodes CR14, CR34 returned to −3 volts serve as dc setters and clamp the positive going excursion of sync at −3 volts.

The local sync input circuit, comprised of an emitter follower, Q21, the local sync amplifier, relay K1, and associated components, is utilized only when the TR-4 is equipped with the optional monochrome ATC system.

This circuit permits local sync to be added to the video instead of regenerated sync to form the composite output. Under certain circumstances, such as making multiple dubs or other in applications where

only a minimum amount of jitter can be tolerated, use of local sync may be more desirable.

For the local sync circuit to be effective, the TR-4 must be in pixlock mode and the selector switch on the front panel of the ATC Delay/Output (module B11) must be in either the COLOR OFF or the COLOR ATC position. Under these conditions, ground is applied to one side of the relay coil energizing the relay. When K1 is energized, the vertical interval gate, Q5, and the horizontal sync gate, Q9, are disabled and local sync feeds through to the sync output emitter follower, Q23.

Coincidence Gate and Relay Driver

Diodes CR31 and CR32 form an AND gate, with both CR31 and CR32 conducting under normal conditions. Under these conditions Q39 is forward biased which in turn ensures that Q40 is cut off and relay K1 is thus deenergized, that is, in the regenerated sync position. When Bus Asking for Pixlock Servo (BAPS) and Automatic Timing Corrector (ATC) External BUs are called for simultaneously, CR31 and CR32 are cut off by a ground potential applied to their cathodes. This in turn causes a positive potential to be applied to the base of transistor Q39, cutting it off. This in turn causes transistor Q40 to conduct which energizes relay K1 that is, selecting local sync.

An overriding Non Phased Color (NPC) Bus is fed through diode CR33 which ensures the use of regenerated sync when operating in the NPC mode. This is effected by forwarded biasing diode CR33 and grounding the collector of Q30. This in turn cuts Q40 off, thus deenergizing relay K1.

Start Pulse

The start pulse is generated from tape sync which is fed from the emitter of Q19. The sync input is a 4 volt peak-to-peak negative signal that is coupled through C43 to the base of Q12, an emitter follower (figure 68). The latter is used as a unity gain amplifier for isolation purposes. The output on the emitter of Q12 is coupled through C21 to the base of Q15, which serves as the driver for the succeeding stage, Q16, the pulse width discriminator.

With no signal present, Q12 is normally cut off and Q15 is normally saturated. Under these conditions there is no pulse on the emitter of Q12 and C21 is charged to −10 volts through the base-emitter junction of Q15 and R55. When a negative pulse is applied to the base of Q12, a replica of this pulse appears on the emitter of this transistor. The RC time constant of C21 and R55 is such that when the pulse is present on the emitter of Q12, C21 will discharge completely. During the horizontal sync and equalizing pulse intervals there is ample time between successive pulses for C21 to return to its fully charged state. During the vertical sync pulse interval, however, the time between successive pulses is relatively short, and C21 is unable to recover from its discharged state before the next negative vertical sync pulse arrives. After the second vertical pulse arrives, C21 charges to a level lower than it had following the first vertical sync pulse. As the vertical sync pulse interval continues, the charge on C21 becomes progressively less; therefore, the recovery pulses (serrations) become progressively smaller. This signal is applied to the base of Q15, where the dc level is shifted to −10 volts; otherwise the signal is not altered. Each time one of these negative pulses arrives on the base of Q15 the latter goes to cut off, the effect of which is to produce a positive pulse on the collector of Q15.

The positive pulse output on the collector of Q15 is fed simultaneously to the emitter and the base of Q16, the pulse width discriminator. The input to the emitter is direct coupled; the input to the base is passed through a differentiator comprised of C24 and R57.

The RC time constant of the differentiator is such that the duration of the capacitor discharge is longer during the horizontal and the equalizing pulse intervals than is the duration of these pulse on the emitter. Therefore the pulses on the base keep Q16 cut off. Compared to the duration of the vertical sync pulses, however, the time constant of the differentiator is short. Therefore, when vertical sync arrives, the capacitor discharges before the end of the pulse, but the emitter still sees the trailing edge of the positive pulse. Thus the emitter is more positive than the base during the remainder of the pulse and the transistor conducts. Simultaneously on the collector of Q16 several positive pulses are generated to correspond to the first few vertical sync pulses.

This positive vertical output signal is passed through a differentiator, consisting of C23, R61, and R70 and applied to the base of Q13. Transistor Q13 in conjunction with Q14 forms the vertical multivibrator which is the monostable type. The RC time constant of the differentiator permits only the differentiated trailing (negative) edge of the first pulse to trigger the vertical multivibrator. The vertical multivibrator generates a positive output pulse which is fed through a differentiator comprised of C25, R33 and variable resistor R100 and applied to the base of Q17, the start pulse generator.

A bilateral transistor, which serves as either a pulse narrowing circuit (boxcar) or an emitter follower, is used for the start pulse generator, Q17. The configuration it assumes depends upon the potential applied to the HI and HN busses. This, in turn, is determined by the TV STANDARDS switch on the international Vertical Advance module. On 525- and 625-line standards, the HN bus is at −20 volts and the HI bus is at ground potential and Q17 is an emitter follower. On 405-line standards, the potentials on the HI and HN busses are reversed and Q17 is a pulse narrowing circuit or boxcar.

Variable resistor R100 (405 Start Pulse Timing) in the base of Q17 is used to fix the timing of the trailing edge (or width) of the output pulse from which the 405-line start pulse is derived (figure 70). Since there are no equalizing pulses in the 405-line signal, R100 is adjusted to establish the RC time constant of the boxcar so that the positive going trailing edge of the output pulse occurs during the third vertical serration interval (figure 70). The RC time constant established by R100 has no influence on the start pulse produced for 525- or 625-line standards. On either of these standards, it is the positive going leading edge of the output pulse that is used in deriving the start pulse (figure 70).

The start pulse for all standards is formed by passing the output pulse of Q17 through a differentiator comprised of C19 and, in the Vertical Advance module, R32. The resultant positive start pulse is applied to the base of Q8, the start pulse amplifier in the Vertical Advance module. The start pulse and the vertical advance pulse (3.5H, 3H, or 1.5H according to the line standards, 525, 625, or 405, respectively) are combined on the base of Q8 as the input to this stage.

Blanking Mixer

The blanking mixer circuit provides new composite horizontal and vertical blanking. The new blank-

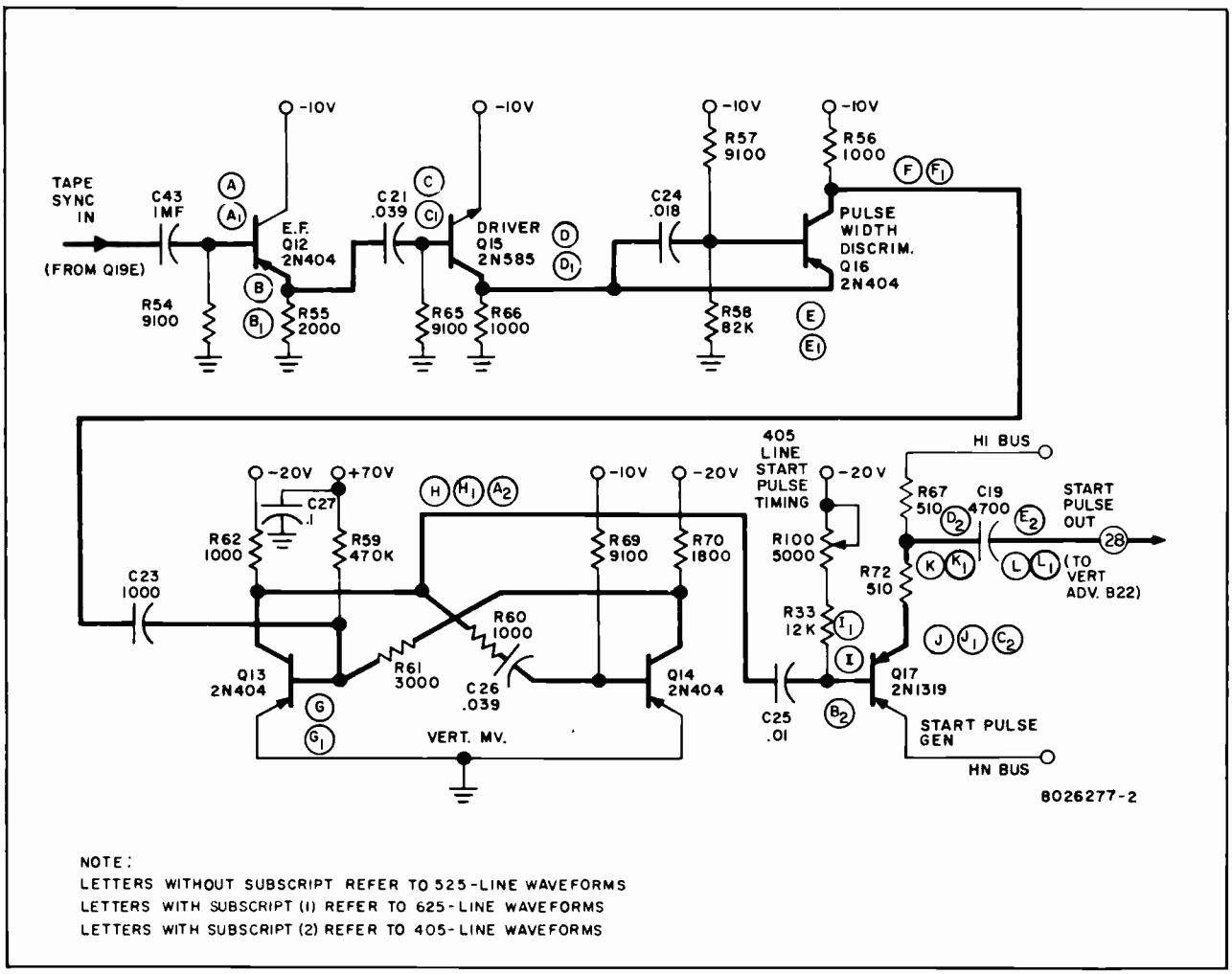
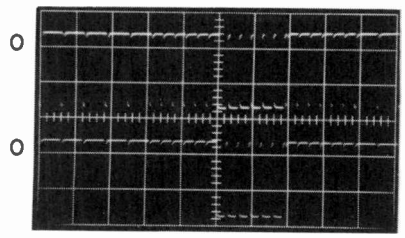
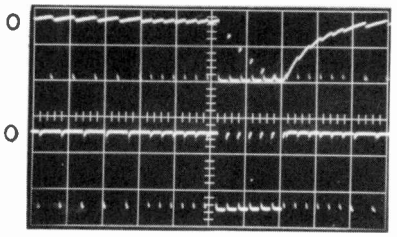


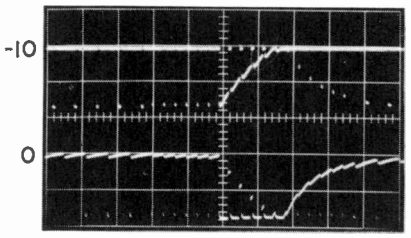
Figure 68—Start Pulse Generator Circuits



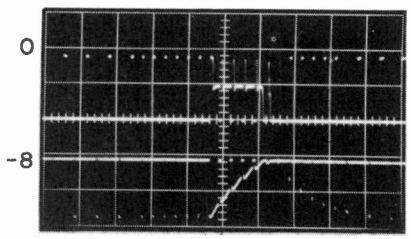
A. Top: Q12 base, 100 μs/cm, 2v/cm
Bottom: P1-17, 100 μs/cm, 2v/cm



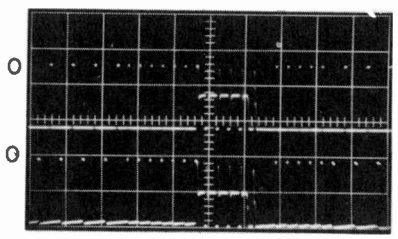
B. Top: Q12 emitter, 100 μs/cm, 2v/cm
Bottom: Q12 base, 100 μs/cm, 2v/cm



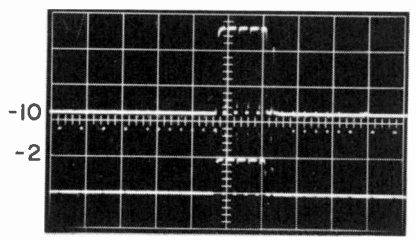
C. Top: Q15 base, 100 μs/cm, 2v/cm
Bottom: Q12 emitter, 100 μs/cm, 2v/cm



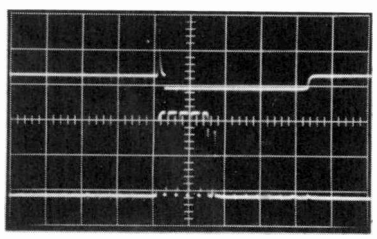
D. Top: Q15 collector/Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q15 base, 100 μs/cm, 2v/cm



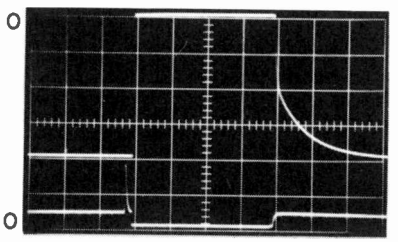
E. Top: Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q16 base, 100 μs/cm, 5v/cm



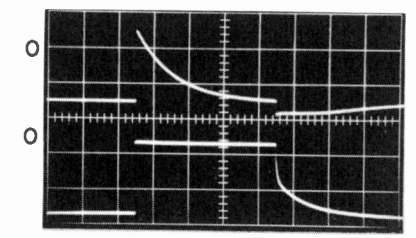
F. Top: Q16 collector, 100 μs/cm, 2v/cm
Bottom: Q16 emitter, 100 μs/cm, 2v/cm



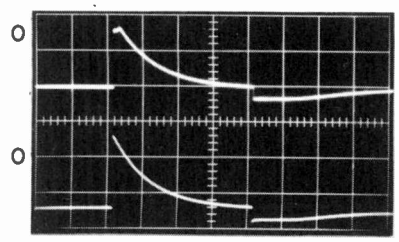
G. Top: Q13 base, 100 μs/cm, 2v/cm
Bottom: Q16 collector, 100 μs/cm, 2v/cm



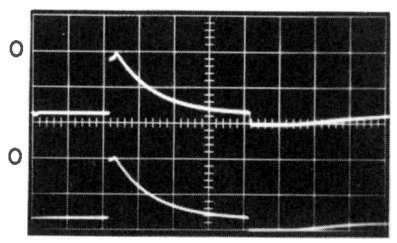
H. Top: Q13 collector, 100 μs/cm, 5v/cm
Bottom: Q13 base, 100 μs/cm, 2v/cm



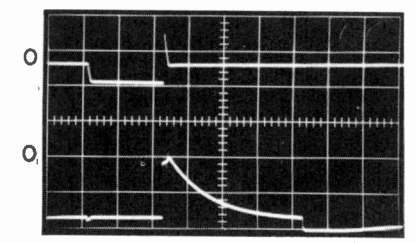
I. Top: Q17 base, 100 μs/cm, 10v/cm
Bottom: Q13 collector, 100 μs/cm, 10v/cm



J. Top: Q17 emitter, 100 μs/cm, 10v/cm
Bottom: Q17 base, 100 μs/cm, 10v/cm



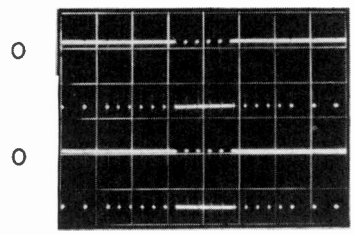
K. Top: R67, R72, 100 μs/cm, 5v/cm
Bottom: Q17 emitter, 100 μs/cm, 10v/cm



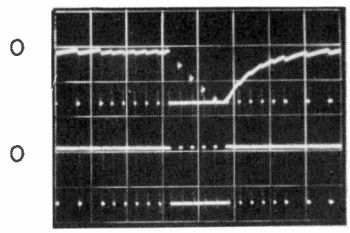
L. Top: P1-28, 100 μs/cm, 5v/cm
Bottom: R67, R72, 100 μs/cm, 5v/cm

NOTE: Letters without subscript refer to 525-line waveforms.
Letters with subscript $_1$ refer to 625-line waveforms.
Letters with subscript $_2$ refer to 405-line waveforms.

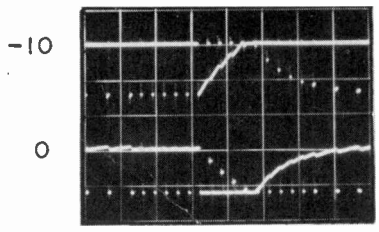
Figure 69—Typical Waveforms, Start Pulse Generator Circuits



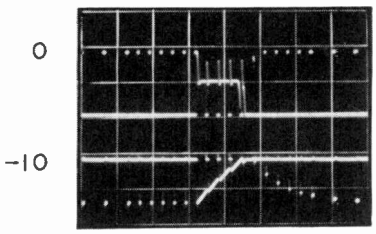
A 1 Top: Q12 base, 100 μs/cm, 2v/cm
Bottom: P1-17, 100 μs/cm, 2v/cm



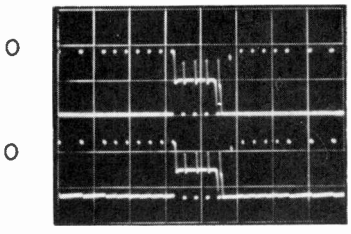
B 1 Top: Q12 emitter, 100 μs/cm, 2v/cm
Bottom: Q12 base, 100 μs/cm, 2v/cm



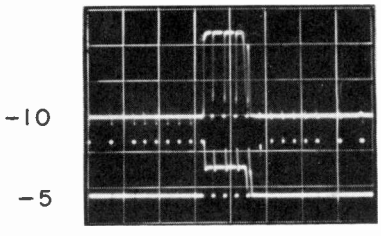
C 1 Top: Q15 base, 100 μs/cm, 2v/cm
Bottom: Q12 emitter, 100 μs/cm, 2v/cm



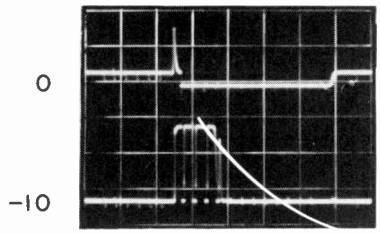
D 1 Top: Q15 collector/Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q15 base, 100 μs/cm, 2v/cm



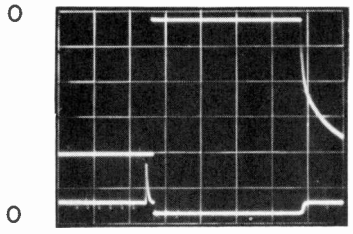
E 1 Top: Q16 emitter, 100 μs/cm, 5v/cm
Bottom: Q16 base, 100 μs/cm, 5v/cm



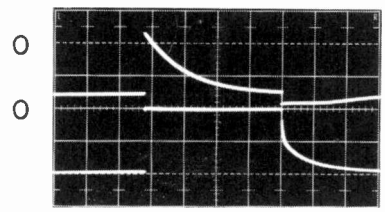
F 1 Top: Q16 collector, 100 μs/cm, 2v/cm
Bottom: Q16 emitter, 100 μs/cm, 5v/cm



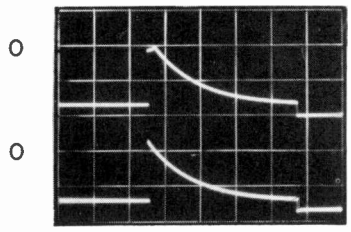
G 1 Top: Q13 base, 100 μs/cm, 2v/cm
Bottom: Q16 collector, 100 μs/cm, 2v/cm



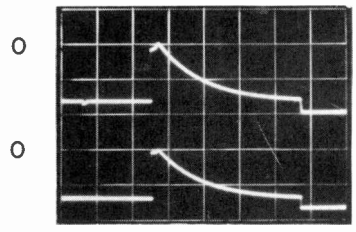
H 1 Top: Q13 collector, 100 μs/cm, 5v/cm
Bottom: Q13 base, 100 μs/cm, 2v/cm



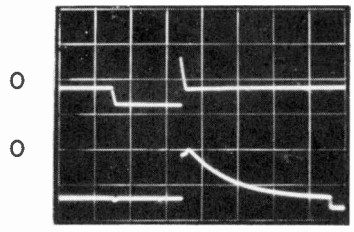
I 1 Top: Q17 base, 100 μs/cm, 10v/cm
Bottom: Q13 collector, 100 μs/cm, 10v/cm



J 1 Top: Q17 emitter, 100 μs/cm, 10v/cm
Bottom: Q17 base, 100 μs/cm, 10v/cm



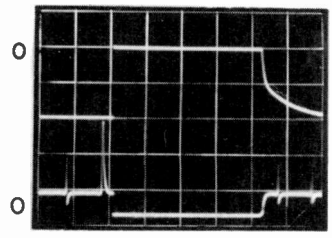
K 1 Top: R67, R72, 100 μs/cm, 5v/cm
Bottom: Q17 emitter, 100 μs/cm, 10v/cm



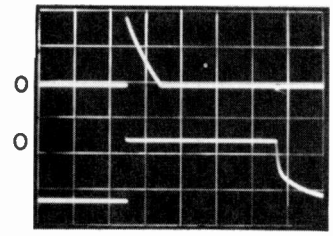
L 1 Top: P1-28, 100 μs/cm, 5v/cm
Bottom: R67, R72, 100 μs/cm, 5v/cm

NOTE: Letters without subscript refer to 525-line waveforms.
Letters with subscript 1 refer to 625-line waveforms.
Letters with subscript 2 refer to 405-line waveforms.

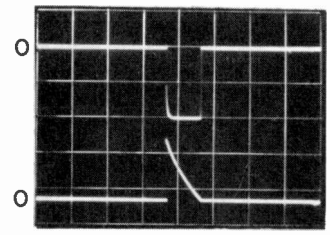
Figure 69—Typical Waveforms, Start Pulse Generator Circuits (Cont'd)



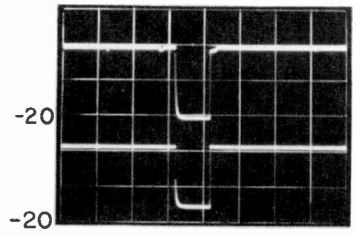
A_2 Top: Q13 collector, 100 μs/cm, 10 v/cm
Bottom: Q13 base, 100 μs/cm, 1 v/cm



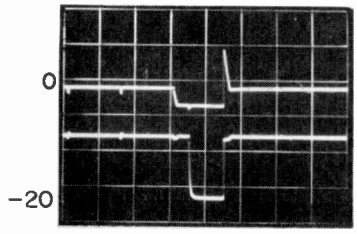
B_2 Top: Q17 base, 100 μs/cm, 10 v/cm
Bottom: Q13 collector, 100 μs/cm, 10 v/cm



C_2 Top: Q17 emitter, 100 μs/cm, 10 v/cm
Bottom: Q17 base, 100 μs/cm, 10 v/cm



D_2 Top: R67, R72, 100 μs/cm, 5 v/cm
Bottom: Q17 emitter, 100 μs/cm, 10 v/cm



E_2 Top: P1-28, 100 μs/cm, 5 v/cm
Bottom: R67, R72, 100 μs/cm, 5 v/cm

NOTE: Letters without subscript refer to 525-line waveforms.
Letters with subscript 1 refer to 625-line waveforms.
Letters with subscript 2 refer to 405-line waveforms.

Figure 69—Typical Waveforms, Start Pulse Generator Circuits (Cont'd)

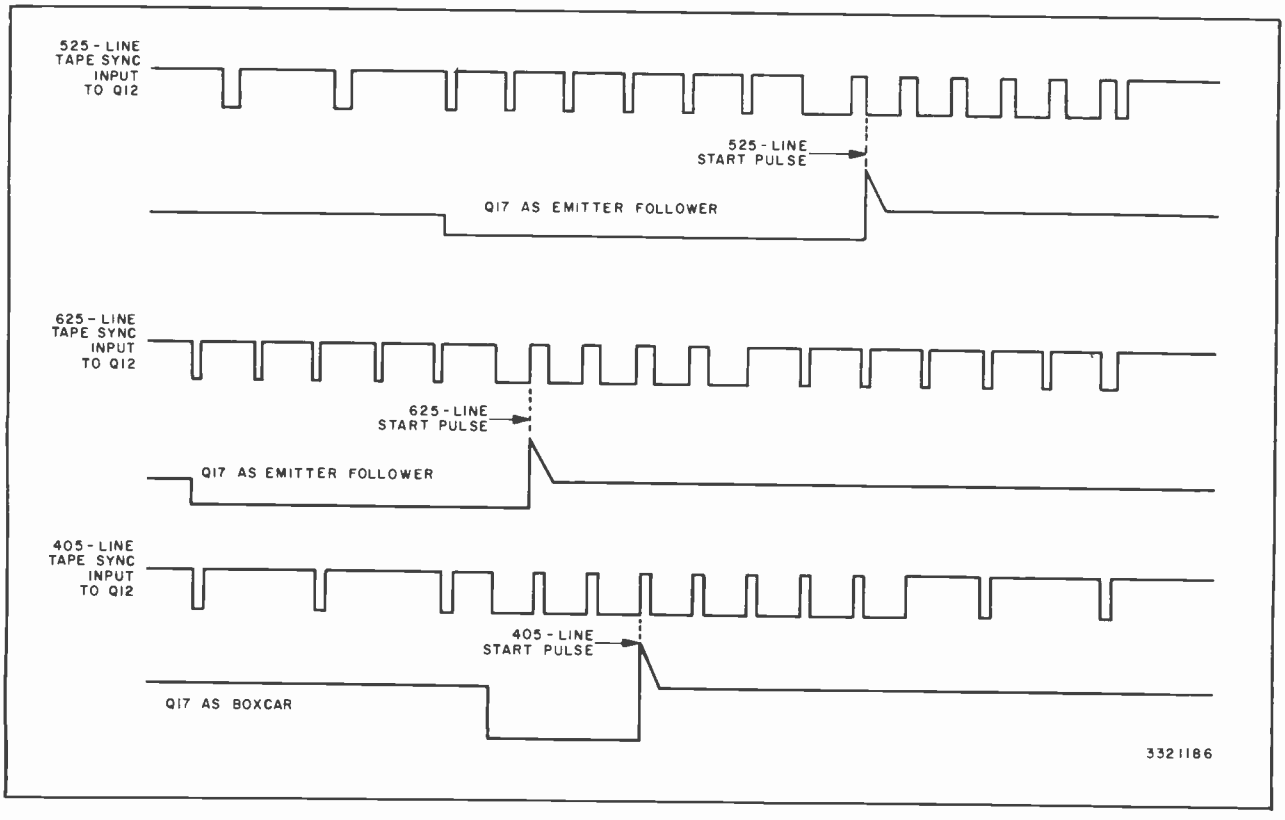


Figure 70—Timing Chart for 525, 625 and 405 Line Standard Pulses

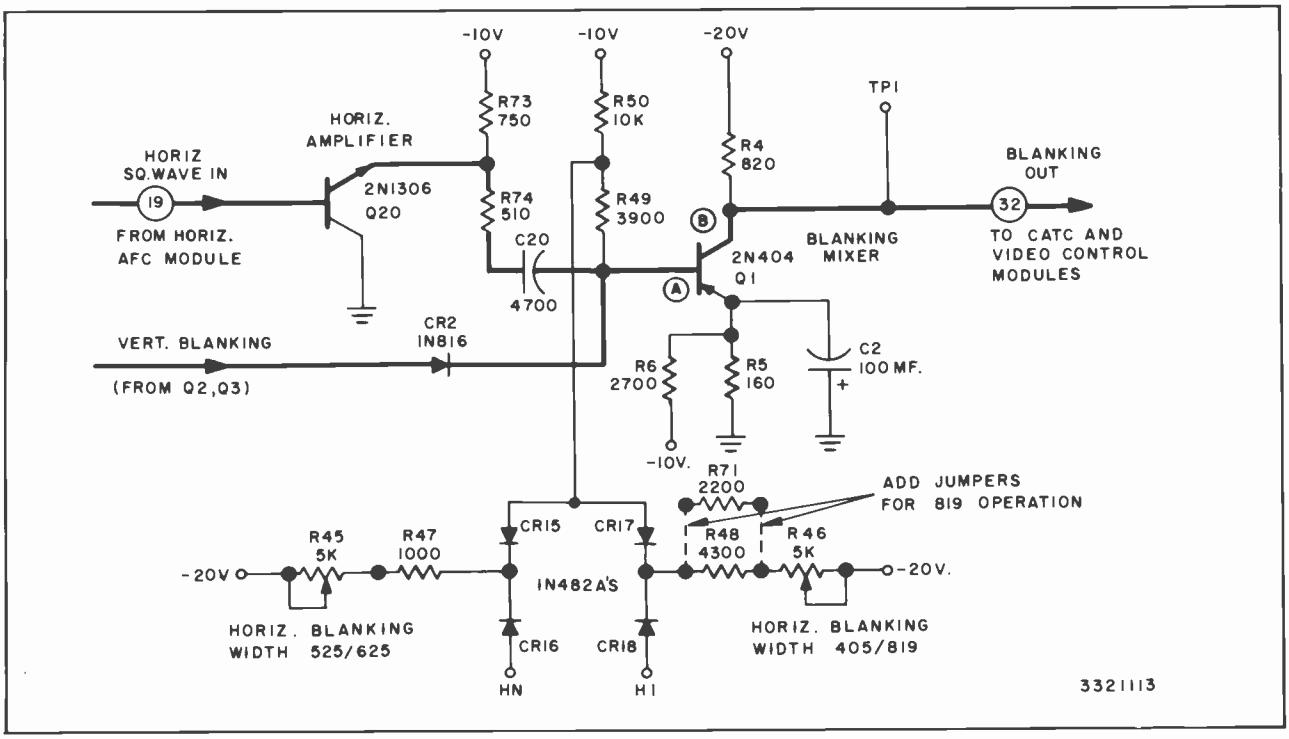
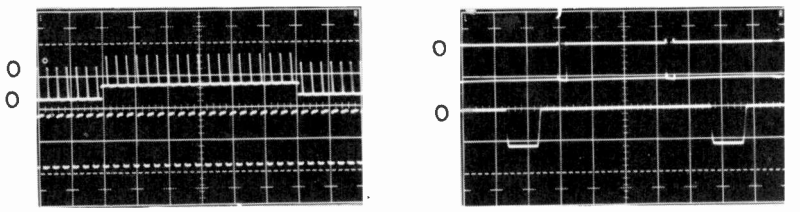


Figure 71—Blanking Mixer Circuits



A. Top: Q1 base, 200 μs/cm, 5v/cm
Bottom: Q20 base, 200 μs/cm, 5v/cm

B. Top: Q1 collector, 5 ms/cm, 10v/cm
Bottom: Q1 collector, 10 μs/cm, 10v/cm

Figure 72—Typical Waveforms, Blanking Mixer Circuits

ing signal is fed to the Video/FM Control (module A21), where it is added to the video component.

As shown in figure 71, the appropriate horizontal square wave (15.75 kc or 15.625 kc on 525- or 625-line standards; or 10.125 kc on 405-line standards) is fed to the base of Q20, the horizontal amplifier. The latter, an emitter follower, serves as a unity gain amplifier in providing the required isolation. The output on the emitter of Q20 is coupled by R74 and C20 to the base of Q1, the blanking mixer. This is a pulse narrowing circuit or boxcar.

To conform to the different horizontal blanking widths required for operation on international standards, some of the resistive components used in the RC time constant circuit of Q1 are switchable. On 525- and 625-line standards the time constant of Q1 is determined by C20, R49, R47, and potentiometer R45. On 405- or 819-line standards, the time constant of Q1 is determined by C20, R49, R48, and potentiometer R48. As discussed earlier, the time constants are electronically switched into the circuit by means of the dc control potential on the HN and HI busses. The potential on the HN and HI busses is a function of the line standard chosen for operation with the TV STANDARDS switch on the international Vertical Advance (module B22). The HN bus is at −20 volts on 525- and 625-line standards and the HI bus is at zero. Conversely, on 405- or 819-line standards, the HN bus is at zero and the HI bus is at −20 volts. Diodes CR15, CR16 and CR17, CR18 in the HN and HI busses, respectively, are used to iso-

late the time constant components in the active branch from those in the inactive branch.

The HOR BLKG WIDTH potentiometers are front panel screwdriver adjustments. Each is labeled according to the line standards to which it applies. The appropriate HOR BLKG WIDTH control is adjusted to set the width of the horizontal blanking pulse in accordance with the line standard in use. The approximate pulse widths for 525- and 625-line standards are 11 microseconds. For 405-line standards, the width is 18 microseconds. (See *Adjustments* for exact settings.)

Each time a horizontal pulse is applied to the base of Q1, a narrow horizontal blanking pulse is produced at the collector. During the 21H interval, (25H on 625-line standards or 15H on 405-line standards) the vertical blanking pulse output of the vertical blanking pulse output of the vertical blanking multivibrator, Q2, Q3, is fed through isolation diode CR2 to the base of Q1. For this period (21H, 25H, or 15H as the case may be) Q1 is cut off, thereby generating the vertical blanking pulse on the collector. Since Q1 is cut off during this period, horizontal blanking is also eliminated at this time. As a result, the output appearing on the collector is a composite horizontal and vertical blanking signal. The composite blanking is fed to the Video/FM Control (module A21).

Clamp Pulse Generating Circuits

The purpose of the clamp pulse generating circuit, is to generate a video clamp pulse. This is derived from one of two sources; from the regenerated sync pulse (originating in the Horizontal AFC module A20) during normal machine operation; or from tape sync during the time of signal disturbance. The circuit is designed to revert back to the regenerated sync pulse when the disturbance ends. Since any signal disturbances present will also be present on the tape sync signal, any change in clamping level will be eliminated.

Under normal operation the regenerated sync signal is applied to the base of inverter amplifier Q24 (figures 73 and 76). The output signal of Q24 is applied to the base of Q25 which forms part of a 2-microsecond coincidence AND gate. The tape sync signal from the Horizontal MSMV Q37 and Q38 is applied to the base of Q26, also part of the 2-microseconds AND gate. When both signals are time coincident (within 2 microseconds) AND gate Q25 and Q26 is thus actuated triggering MSMV Q29 and Q30. The output per pulse from the MSMV Q29 and Q30 is divided into two paths; one path is to integrator Q31 and the other is to the pulse narrowing circuit composed of Q34, C65, R148 and fed through C59 and R129 to the base of Q27. Transistors Q27 and Q28 form an OR gate which couples the regenerated sync to the Video/FM Control module A21.

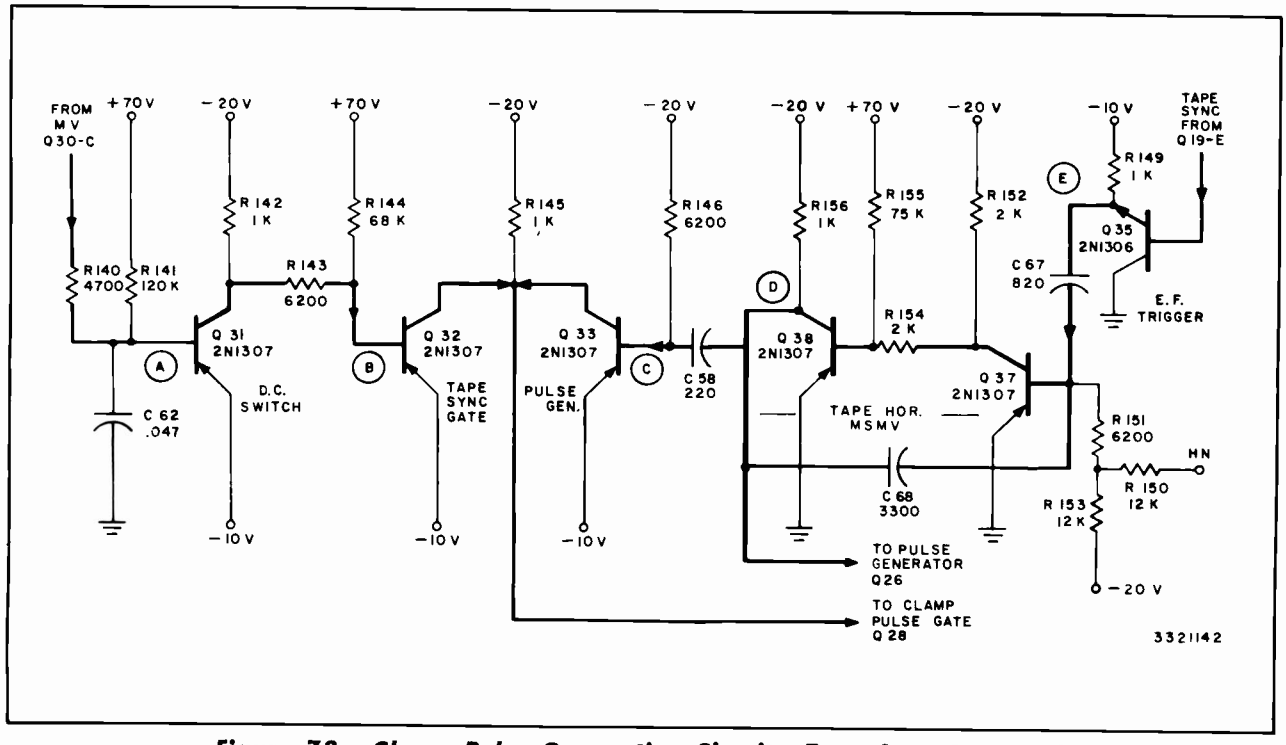
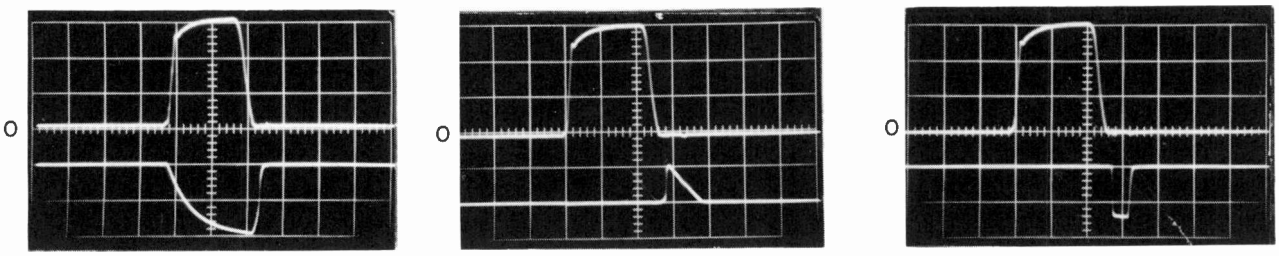


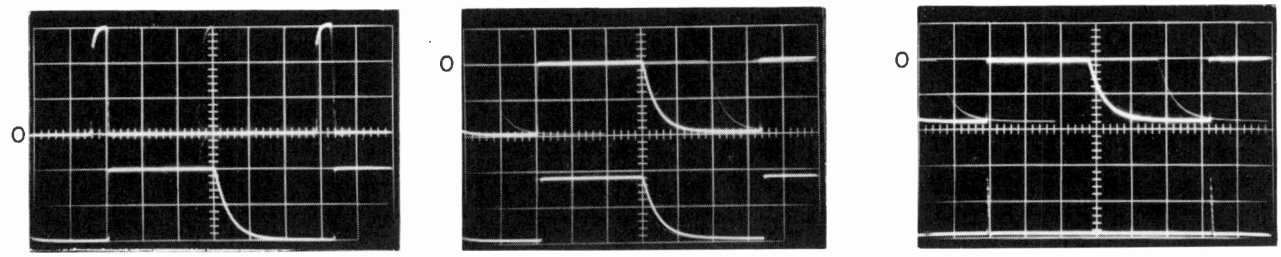
Figure 73—Clamp Pulse Generating Circuits, Tape Sync Gate and Horizontal MV



A. Top: Q24 base, 2 μs/cm, 2v/cm
Bottom: Q24 collector, 2 μs/cm, 5v/cm

B. Top: Q24 base, 2 μs/cm, 2v/cm
Bottom: Q25 base, 2 μs/cm, 5v/cm

C. Top: Q24 base, 2 μs/cm, 2v/cm
Bottom: Q25 collector, 2 μs/cm, 10v/cm



D. Top: Q24 base, 10 μs/cm, 2v/cm
Bottom: Q38 collector, 10 μs/cm, 10v/cm

E. Top: Q38 collector, 10 μs/cm, 10v/cm
Bottom: Q30 collector, 10 μs/cm, 10v/cm

F. Top: Q30 collector, 10 μs/cm, 10v/cm
Bottom: Q34 base, 10 μs/cm, 5v/cm

Figure 74—Typical Waveforms, Clamp Pulse Generating Circuits, Tape Sync Gate and Horizontal MV

When a signal disturbance occurs at AND gate Q25 and Q26, MSMV Q28 and Q29 is not triggered. Tape sync is now used to generate the clamp pulse. Refer to figures 73 and 76. Since MSMV Q28 and Q29 is is not triggered, this allows C62 in the integrator network to discharge after 200 microseconds and cause Q31 (a DC switch) to conduct (refer to figure 75, waveform B). This enables the 1.5 microsecond AND gate Q32 and Q33. The output pulse from the AND gate Q32 and Q33 is fed to the OR gate Q27 and Q28. The output pulse of the OR gate Q27 and Q28 is fed to the Video/FM Control module A21.

When the disturbance is not present, AND gate Q32 and Q33 is not actuated and regenerated sync again generates the clamp pulses sent to the Video/FM Control module A21.

Adjustments

To obtain the proper horizontal blanking, vertical blanking and vertical gate widths, follow the procedure outlined below. A single trace oscilloscope can be used to make the first two adjustments, but the last mentioned requires a dual trace oscilloscope such as a Tektronix Type 535A.

1. Connect the oscilloscope probe to one of the three video test jacks (VID 1, VID 2, VID 3) on the front panel of the Video Output (module A22). Adjust the oscilloscope sweep to display a single horizontal blanking interval.

2. Adjust the appropriate HOR BLKG WIDTH control (R45 or R48) on the front panel as described below:

a. For 525 lines, adjust R45 so that the horizontal pulse is 11 microseconds wide.

b. For 625 lines, adjust R45 so that the horizontal pulse is 11.85 microseconds wide.

c. For 405 lines, adjust R48 so that the horizontal pulse is 18 microseconds wide.

Vertical Blanking Width

1. Connect the oscilloscope probe to one of the three video test jacks (VID 1, VID 2, VID 3) on the front panel of the Video Output (module A22). Using delayed sweep and external sync for a trigger, adjust the oscilloscope to display the vertical blanking interval. (The advanced vertical pulse available at the 3.5H test pack (TP5) on the front panel of the Vertical Advance (module B22) can be used in lieu of external sync for a trigger.)

2. Adjust the VERT BLKG WIDTH control (R7) on the front panel as described below:

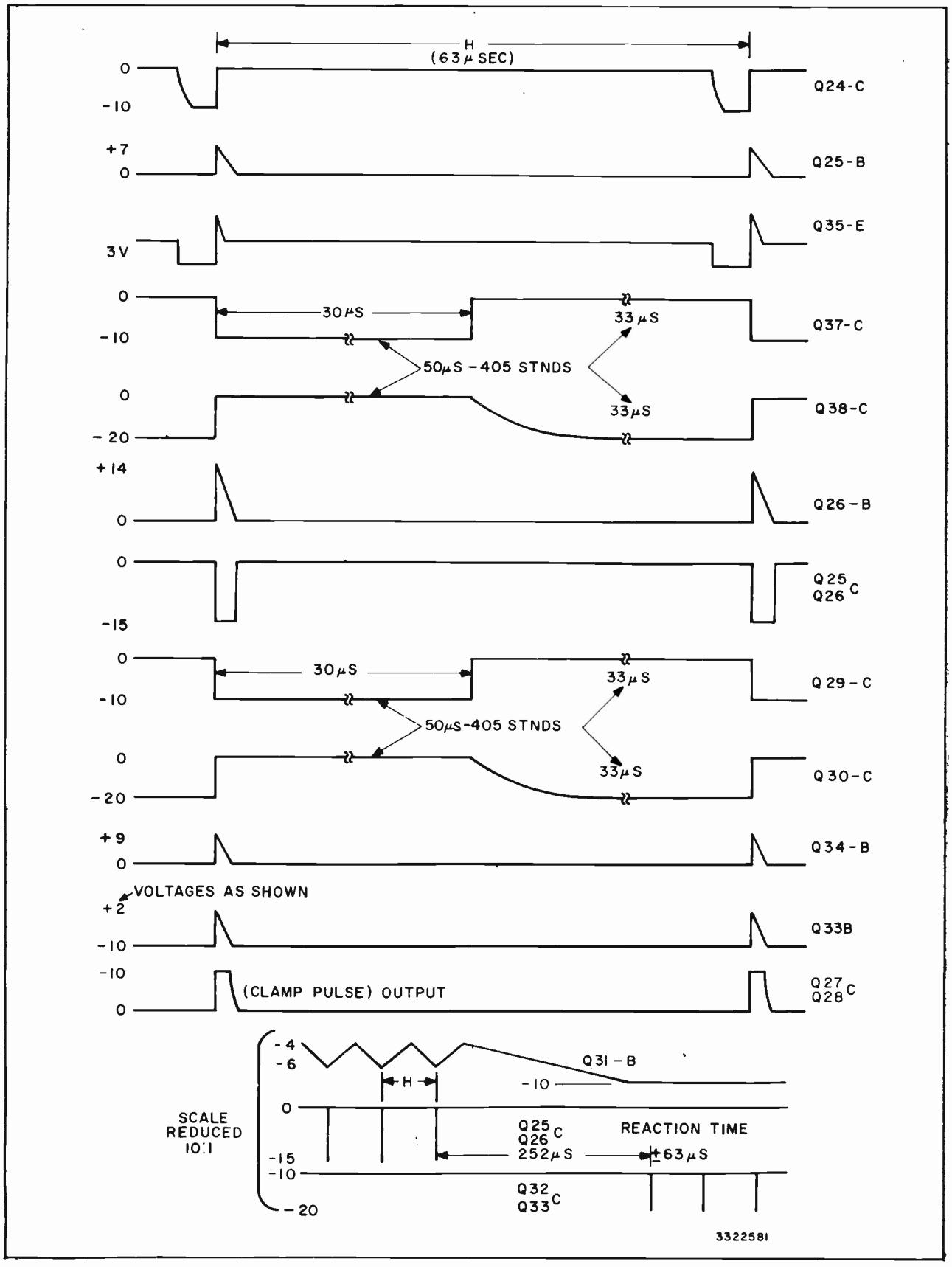


Figure 75—Waveform and Timing Chart for 525 Line Standard Clamp Pulses

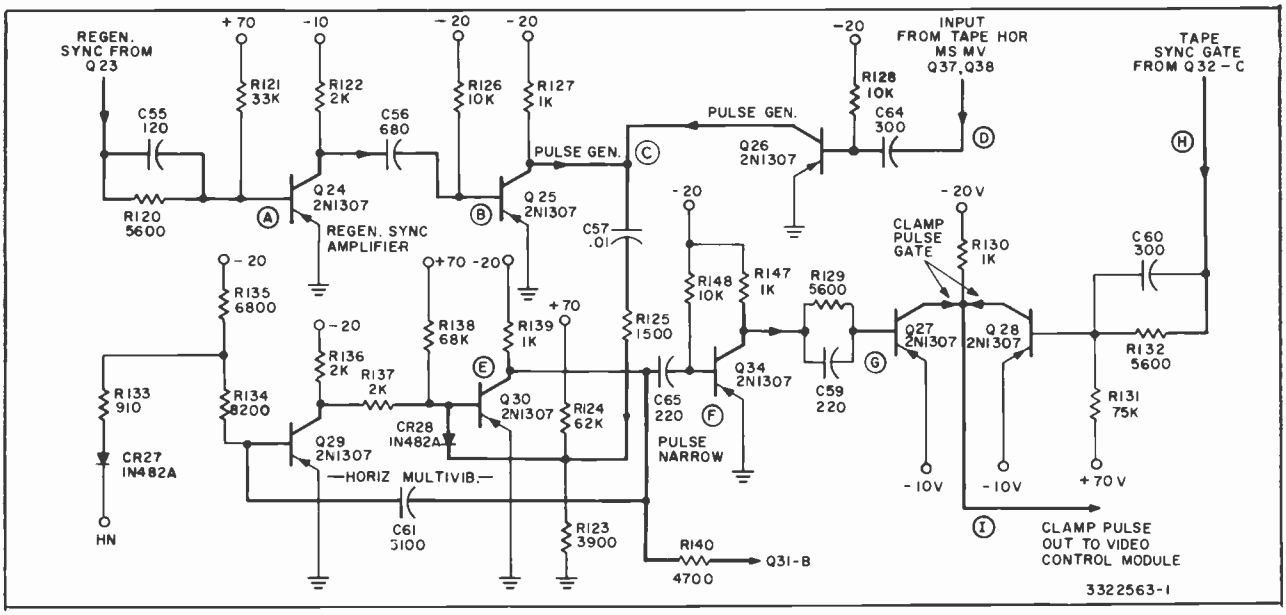
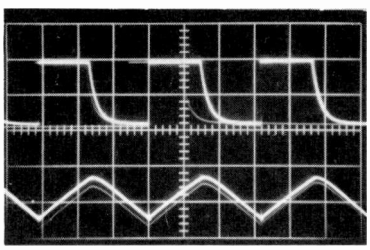
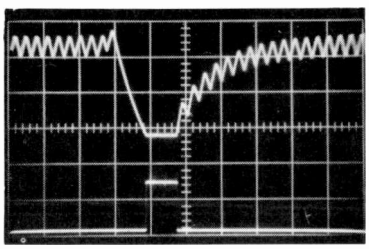


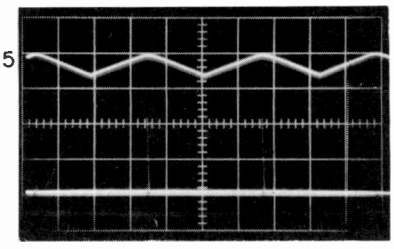
Figure 76—Clamp Pulse Circuits, Regenerated Sync, Clamp Pulse Generator and Hor. MV



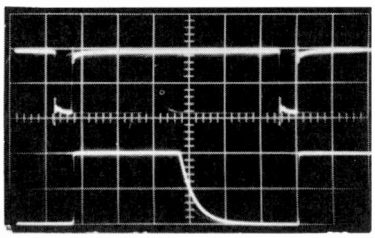
A. Top: Q30 collector, 10 μs/cm, 10v/cm
Bottom: Q31 base, 10 μs/cm, 1v/cm



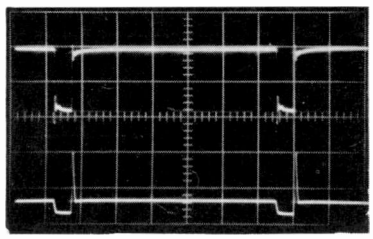
B. Top: Q31 base, 200 μs/cm, 2v/cm
Bottom: Q23 base, 200 μs/cm, 5v/cm



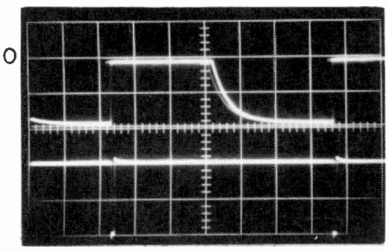
C. Top: Q31 base, 20 μs/cm, ½ v/cm
Bottom: Q33 base, 20 μs/cm, 10v/cm



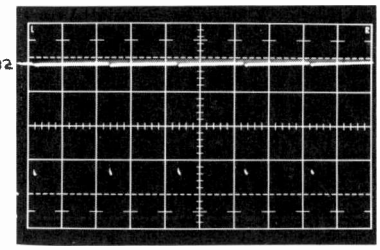
D. Top: Q38 collector, 10 μs/cm, 2v/cm
Bottom: Q35 base, 10 μs/cm, 2v/cm



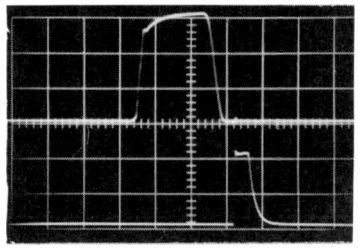
E. Top: Q35 base, 10 μs/cm, 2v/cm
Bottom: Q35 collector, 10 μs/cm, 2v/cm



G. Top: Q30 collector, 10 μs/cm, 10v/cm
Bottom: Q27 base, 10 μs/cm, 2v/cm



H. Q32 collector, 20 μs/cm, 2v/cm during machine start-up



I. Top: Q24 base, 2 μs/cm, 2v/cm
Bottom: Q27 collector, 2 μs/cm, 5v/cm

Figure 77—Typical Waveforms, Clamp Pulse Circuits, Regenerated Sync Clamp Pulse Generator and Horizontal MV

a. For 525 lines, adjust R7 so that the vertical blanking interval is 1250 microseconds wide.

b. For 625 lines, adjust R7 so that the vertical blanking interval is 1290 microseconds wide.

c. For 405 lines, adjust R7 so that the vertical blanking interval is 1425 microseconds wide.

Vertical Gate Width

1. Mount the Sync Logic module on an extender and insert it in the TR-4. Connect the channel A input probe of the dual trace oscilloscope to the VERT GATE test jack (TP2) on the front of the module. Connect the channel B input probe to one of the three video test jacks (VID 1, VID 2, VID 3) on the front panel of the Video Output (module A22). Trigger each channel with external sync; or, in lieu of this, use the advanced vertical pulse available at the 3.5H test jack (TP5) on the front panel of the Vertical Advance (module B22). Using delayed sweep, adjust the sweep of channel B to display the vertical blanking interval (525/625 lines) or the vertical sync pulse group interval (405 lines). Using delayed sweep, adjust the sweep of channel A to display the vertical gain width pulse.

2. Adjust the VERT GATE WIDTH control (R32) as described below:

a. For 525/625 lines, adjust R32 so that the trailing edge of the 9H/7.5H pulse is halfway between the last equalizing pulse and the first horizontal pulse. See figure 64.

b. For 405 lines, adjust R32 so that the trailing edge of the 4H pulse occurs 4 microseconds after the trailing edge of the last broad pulse in the vertical sync pulse group interval. Refer to figure 78.

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As shown in the block diagram figure 79, two stages Q8 and Q9 have been deleted from the circuitry of the Video/FM Control module A21. Transistor Q7 now becomes a clamp pulse amplifier.

On page 120, in IB-31818, delete under *Clamp Quad,* paragraphs 2 and 3 in the left-hand column. Delete also figures 136 and 137.

The incoming pulses, from the regenerated sync in the Sync Logic module B21, are already clipped and inverted for properly keying the quad Z1. These pulses are amplified in the clamp pulse amplifier Q7, then direct-coupled from the collector of Q7 to the base of Q10, the clamp pulse driver. The two out-of-phase pulses on the collector and emitter of Q10 are coupled through C16 and C17 respectively across the clamp quad Z1. Refer to figure 80.

The video output amplifier and blanking adder circuits remain the same as described in IB-31818.

IB-31818, Page 119

In figure 134, change the value of C9 from .22 to .82.

IB-31818, Page 121

In figure 136, change the value of C12 from 620 to 390, and C14 from 1300 to 820.

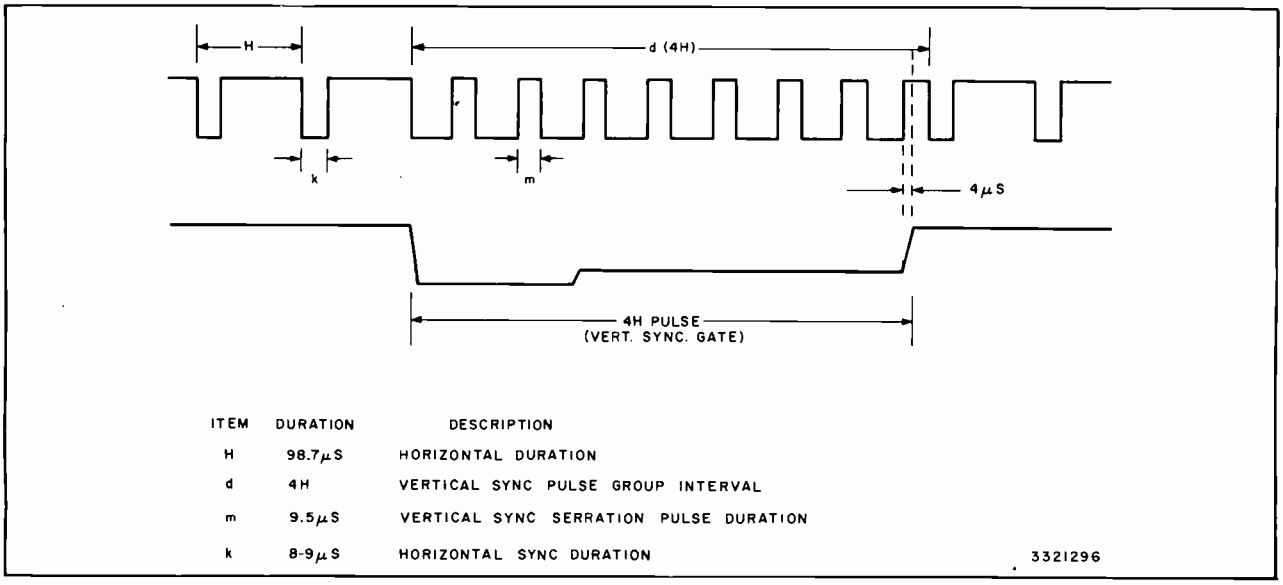


Figure 78—Vertical Gate Width Adjustment for 405 Lines

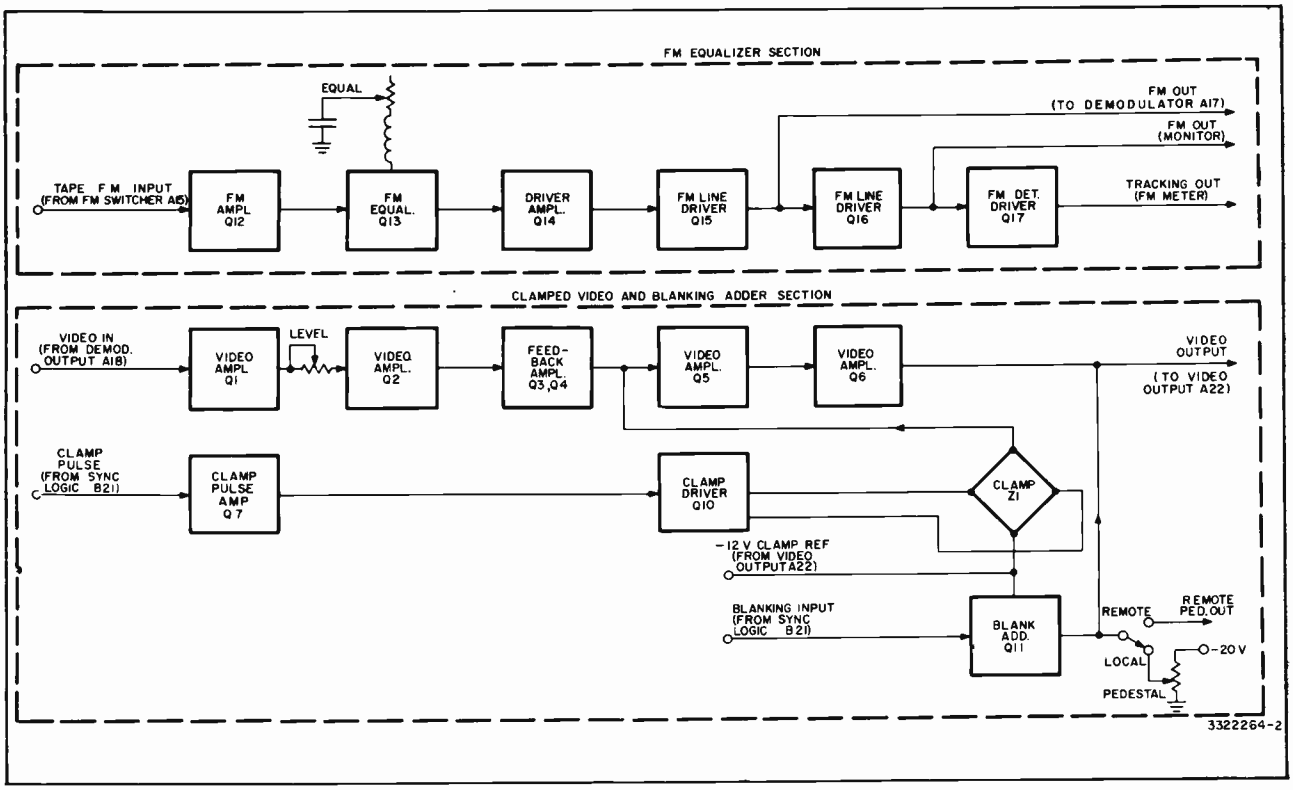


Figure 79—Block Diagram for Video/FM Control Module

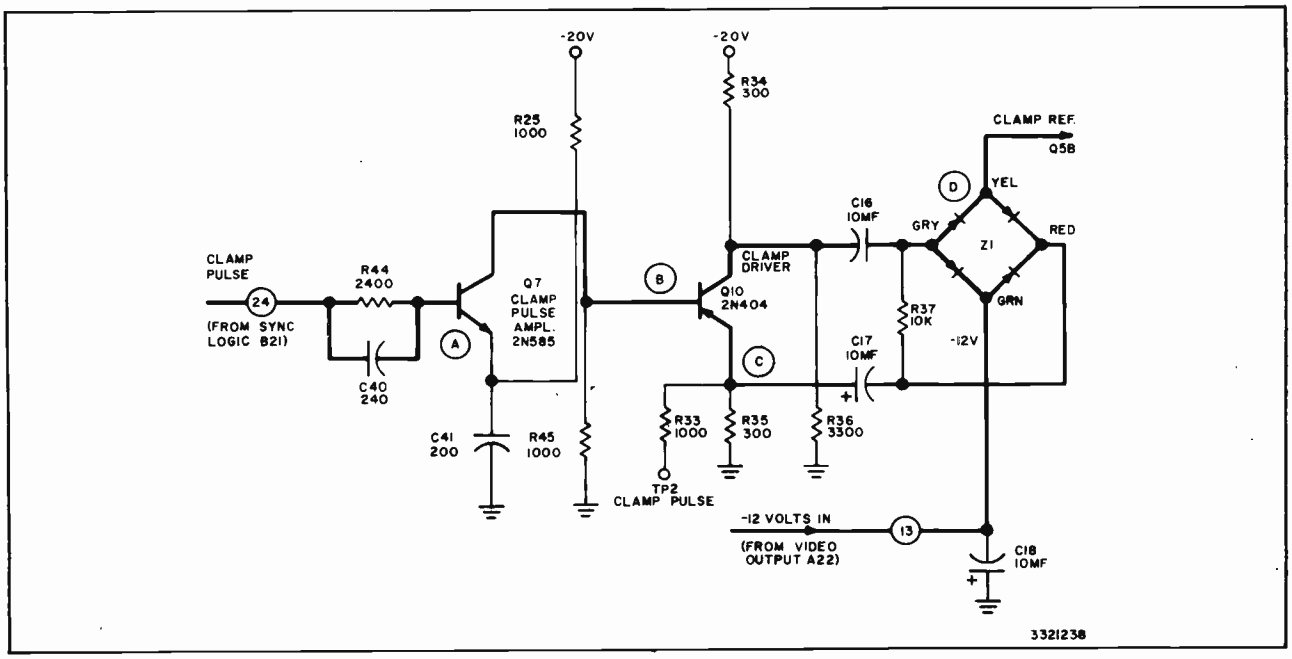
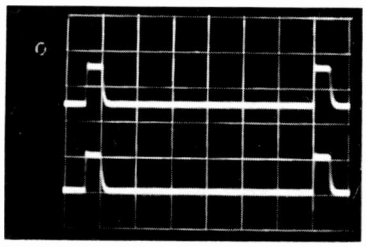
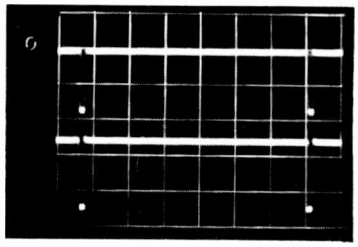


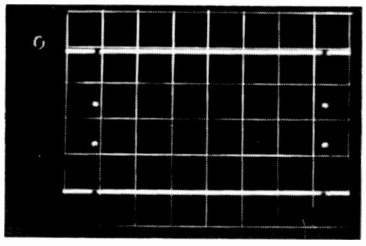
Figure 80—Clamp Pulse Amplifier, Clamp Driver and Quad Circuits



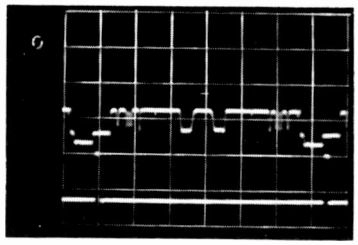
A. Top: Q7 emitter, 10 μs/cm, 10v/cm
Bottom: Q7 base, 10 μs/cm, 10v/cm



B. Top: Q10 base, 10 μs/cm, 5v/cm



C. Top: Q10 emitter, 10 μs/cm, 5v/cm
Bottom: Q10 collector, 10 μs/cm, 5v/cm



D. Top: Z1 yellow, 10 μs/cm, 5v/cm
Bottom: Z1 gray, 10 μs/cm, 5v/cm

Figure 81—Typical Waveforms, Clamp Pulse Amplifier, Clamp Driver and Quad Circuits

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