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MOS FET Biasing Techniques

by S. Reich

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A wide variety of applications exist for field-effect transistors today including rf amplifiers and mixers, i-f and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits.

Several different FET structures have also evolved. The dual-gate metal-oxide-semiconductor FET, for example, appears particularly advantageous in rf stages because of low feedback capacitance, high transconductance and superior cross modulation with automatic-gain-control capability.

The rules for biasing FETs vary slightly depending upon the type of FET being applied. But we'll attempt to cover most of the possibilities by looking at several typical examples.

As you know, all FETs including junction devices, can be classified as depletion or enhancement types, depending upon the conductivity state of the channel at zero gate-to-source voltage or bias. In a depletion type, charge carriers are present and the channel is conductive when no bias is applied to the gate. Reverse bias depletes this charge and reduces channel conductivity; forward bias draws more charge carriers into the channel and increases conductivity. In an enhancement type, no useful channel conductivity exists at either zero or reverse gate bias; the gate must be forward-biased to produce active carriers and permit conduction through the channel.

Test circuits which can be used to measure the zero-bias drain current I_{DSS} of junction-gate and insulated-gate field-effect transistors are shown in Fig. 1. The junction-gate device, shown in Fig. 1(a), is always a depletion type and thus exhibits a reading for I_{DSS}. Insulated-gate or MOS devices may be either depletion or enhancement types; depletion types exhibit reasonable I_{DSS} readings in the circuit of Fig. 1(b), while enhancement types are cut off. The transistor

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symbol shown in Fig. 1(b) uses a solid channel line to indicate the "normally ON" channel of a depletion type. An enhancement type is represented by an interrupted channel line, that indicates the "normally OFF" channel.

Although enhancement types are always operated (activated) in the enhancement mode (because application of reverse bias would simply cut the device off), depletion types can operate in either mode. Junction-gate devices can operate in the enhancement mode only within a very limited range because gate voltages exceeding 0.3 V also forward-bias the gate-to-source input diode and load the signal source. However, MOS depletion devices can operate in either the enhancement or the depletion mode without the constraints associated with input-diode loading.

The field-effect transistors shown in Fig. 1 are single-channel, single-gate, or triode-type devices. Although it is possible that the substrate of either the junction-gate or insulated-gate transistor may be used as a separate control element, in most circuits it is adequate as a control element and is extrinsically connected to the source or operated at a fixed potential.

When two separate control elements are required in a circuit, a dual-gate MOS transistor such as that shown in Fig. 2 is usually used. In this type of device, two independent gate electrodes that control individual channels are serially interconnected. In newer dual-gate MOS transistors, gate protection is provided by intrinsic back-to-back diodes, as shown in Fig. 2(b). The substrate in this type of device is internally connected to the source.

Biasing a single-gate MOS transistor

The bias circuit for a single-gate MOS transistor may take three forms, as shown in Fig. 3: (a) self-bias, (b) an external supply, or (c) a combination of the two. The design of a self-bias circuit is fairly straightforward. For example, if it is desired to operate a 3N128 MOS transistor (an n-channel, depletion device) with a drain-to-source V_{DS} voltage of 15 V and a small-signal transconductance g_{fs} of 7.4 mmhos, the drain current I_D required for the desired transconductance is first obtained from published transfer-characteristics curves such as those shown in Fig. 4(a). A published curve such as the one shown in Fig. 4(b) is then used to determine the gate-to-source voltage V_{GS} required for the desired value of I_D. The circuit parameters can then be calculated using $V_{DS} =$ 15 V, $I_D = 5$ mA, $V_{GS} = -1.1$ V and $V_G = 0$.

$$V_S = V_G - V_{GS} = 1.1 \text{ V} \quad (1)$$

$$R_S = V_S/I_D = 1.1/5 = 220\ \Omega \quad (2)$$

$$V_{DD} = V_{DS} + V_S = 15 + 1.1 = 16.1 \text{ V} \quad (3)$$

In a circuit designed for applied bias only, the problem becomes more complicated. For example, the voltage divider consisting of R_1 and R_2 in Fig. 3(b) may be required to apply a V_{GS} of -1.1 V. In addition to the fact that a negative supply is required, a more serious problem exists. The bias-voltage computations shown above were based on the solid-line curve shown in Fig. 4(b) for a typical device.

However, the drain currents for individual devices may cover a wide range of values, as indicated by the dashed curves H and L representing high- and low-limit devices, respectively. With a fixed-bias supply of -1.1 V, therefore, drain current could range from cutoff to 18.5 mA. Some form of dc feedback is obviously desirable to maintain the drain current constant over the normal range of product variation.

The combination bias method shown in Fig. 3(c) makes use of a larger value of R_S to narrow the range of drain current to plus or minus a few milliamperes. Figure 5 shows curves of I_{DSS} as a function of I_D for various values of R_S. The normal range of I_{DSS} for the 3N128 is from 5 to 25 mA, or a spread of 20 mA. The use of the 220-Ω source resistor R_S calculated in the previous example reduces this spread to about 5 mA, for a 4-to-1 improvement. Higher values of R_S achieve tighter control of the spread of drain-current values.

As an example, the circuit of Fig. 3(c) may

be required to maintain drain current constant within ±1 mA for the same conditions given in the previous example. Figure 5 shows that a value of R_S equal to or greater than 1000 Ω will satisfy the required drain-current tolerance. However, a quiescent current of 5 mA through a source resistor of 1000 Ω produces a V_{GS} value of −5 V, which is incompatible with a drain current of 5 mA. Therefore, an applied bias must be used in conjunction with the self-bias. The circuit parameters for Fig. 3(c) are then calculated using $V_{DS} = 15$ V, $I_D = 5$ mA, $V_{GS} = -1.1$ V, and $R_S = 1000$ Ω.

$$V_S = I_D R_S = (0.005)\ (1000) = 5 \text{ V} \quad (4)$$

$$V_G = V_{GS} + V_S = -1.1 + 5 = 3.9 \text{ V} \quad (5)$$

$$V_{DD} = V_{DS} + V_S = 15 + 5 = 20 \text{ V} \quad (6)$$

$$\frac{V_{DD}}{V_G} = \frac{R_1 + R_2}{R_2} = \frac{20}{3.9} = 5.12 \quad (7)$$

The lower limits of R_1 and R_2 are established by determining the maximum permissible loading of the input circuit and setting this value equal to the parallel combination of the two resistors. For example, if the total shunting of the input circuit is to be no less than 50,000 Ω, R_1 and R_2 are calculated as follows:

$$\frac{R_1 R_2}{R_1 + R_2} = 50{,}000 \quad (8)$$

$$\frac{R_1 + R_2}{R_2} = 5.12 \quad (9)$$

$R_1 = 256{,}000$ Ω, and $R_2 = 62{,}000$ Ω.

In practice, the effects of input-circuit loading can frequently be eliminated by the use of the circuit arrangement shown in Fig. 5.

The upper limits of R_1 and R_2 are usually determined by practical consideration of the resistor component values because the absolute values of gate-leakage current I_{GSS} are extremely small. In unique applications where I_{GSS} is a significant factor, a maximum value for the parallel combination of R_1 and R_2 can be determined by dividing the total permissible change in voltage V_G across the combination by the maximum allowable value of I_{GSS} at the expected operating temperature, as determined from the published data for the transistor used.

Because I_{GSS} consists of leakage currents from both drain and source, and these currents are usually measured with a maximum-rated voltage stress on the gate with respect to all other elements, the published value of I_{GSS} is generally much higher than that which could be expected under typical circuit conditions. As a result, the values of R_1 and R_2 determined in this manner are conservative.

Substrate biasing

As mentioned previously, many single-gate FETs incorporate provisions for separate connection to the substrate because it is sometimes desirable to apply a separate bias to the substrate and use it as an additional control element. A simple arrangement for achieving this bias is shown in Fig. 7(a). In this circuit, the substrate bias V_{US} is equal to $I_D\ (R_1 + R_2)$ and the gate bias V_{GS} is equal to $I_D R_1$.

One application in which substrate bias is mandatory is the attenuator circuit shown in Fig. 7(b). An MOS transistor is extremely useful as an attenuation device because it acts as a fairly linear resistance whose intrinsic conductivity can be drastically changed by means of a dc voltage applied to the gate. In the circuit of Fig. 7(b), for example, a signal applied to the drain can be attenuated by application of a positive voltage to the MOS transistor gate. The attenuation A_V obtained is given by

$$A_V = \frac{R_D}{R_D + R_s} \quad (10)$$

where R_D, the device channel resistance, is a function of bias voltage and can be varied from approximately 100 Ω to 10^5 MΩ. Because of the construction of the MOS transistor, however, the drain must always be positive with respect to the substrate so that the drain-to-source diode (diffusion) will not be biased into conduction. Therefore, the substrate must be back-biased to at least the peak value of the negative-going signal that might be applied to the drain. Figure 7(b) shows how this back-bias is obtained.

Biasing a junction-gate transistor

The biasing techniques that have been described for single-gate MOS transistors are directly applicable to junction-gate devices with one exception. Because the input gate of a junction-gate field-effect transistor consists of a back-biased diode, the device must always be biased so that the input-gate diode is not in conduction. Effectively, therefore, a junction-gate device will almost always be operated in the depletion mode.

Although the biasing considerations covered thus far are applicable to all types of single-gate transistors, it should be remembered that enhancement-type devices must be turned on before they can be used as amplifiers. Therefore, applied bias such as shown in Fig. 3(b) and 3(c) must always be used with these devices. In addition, it is desirable to narrow the range of drain current by means of a source resistor, such as that shown in Fig. 3(c), that produces self-bias after the transistor is turned on.

As an example of this type of biasing, it may be assumed that a 2N4065 p-channel enchance-

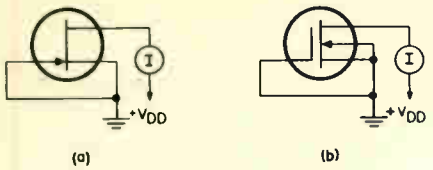


Fig. 1. I_{DSS} test circuits for (a) junction-gate and (b) insulated-gate field-effect transistors.

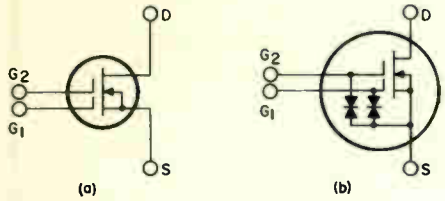


Fig. 2. Dual-gate MOS transistors. (a) conventional symbol, (b) modified symbol to show gate-protected device.

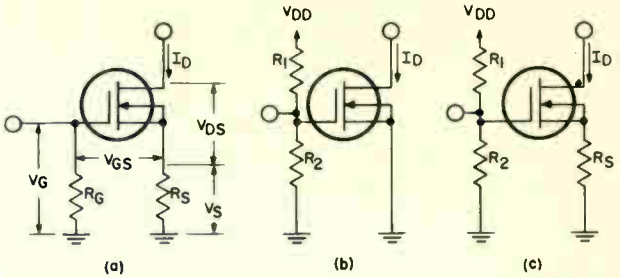


Fig. 3. Biasing circuits for single-gate transitors: (a) self-biasing; (b) external biasing; (c) a combination of self-biasing and external biasing.

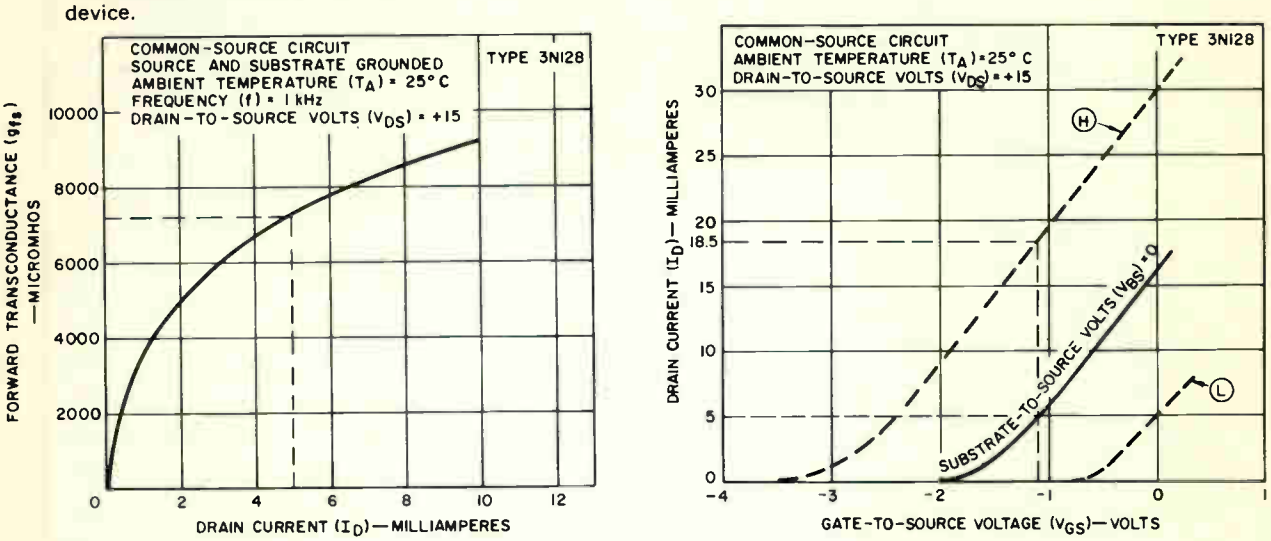


Fig. 4. (a) Transfer and (b) operating characteristics of the 3N128 single-gate MOS transistor.

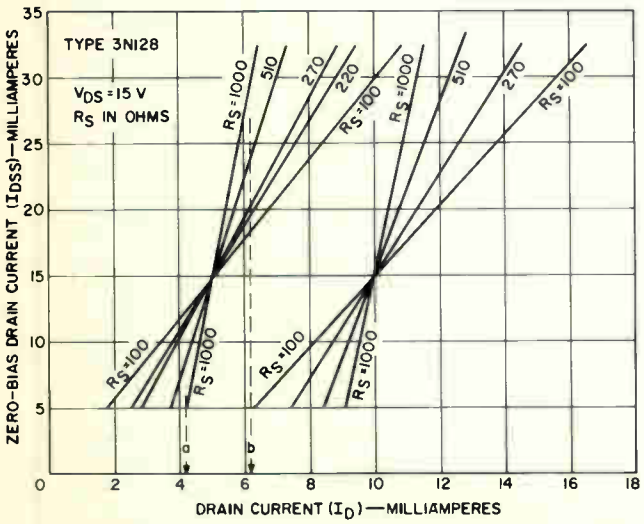


Fig. 5. Zero-bias drain current I_{DSS} as a function of drain current I_D for various values of source resistance R_S in a 3N128 single-gate MOS transistor.

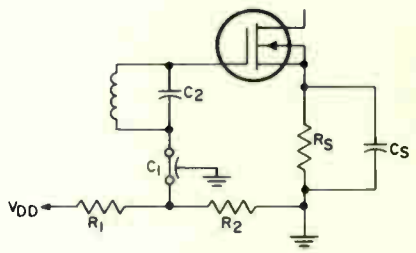


Fig. 6. Circuit used to eliminate input-circuit loading.

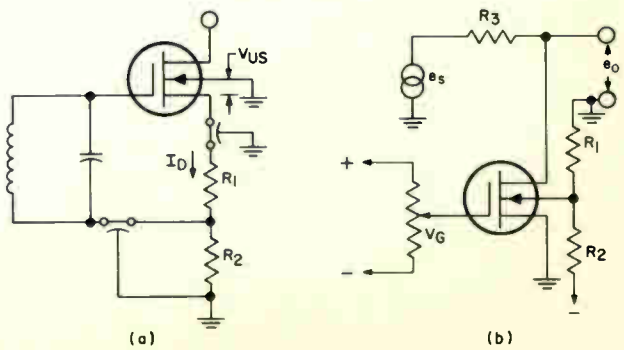


Fig. 7. Substrate biasing circuits.

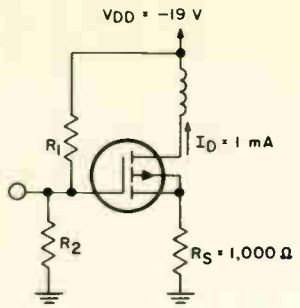


Fig. 8. Biasing circuit for an enhancement-type MOS transistor.

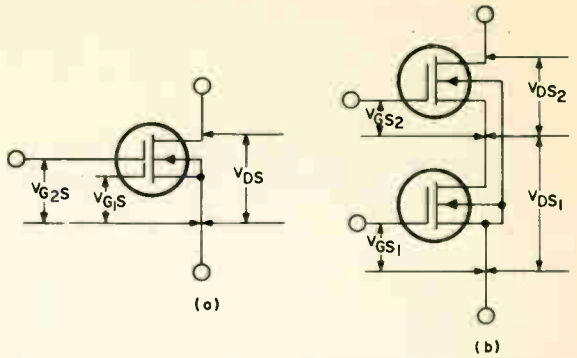


Fig. 9. Circuits showing element voltage associated with MOS dual-gate transistors.

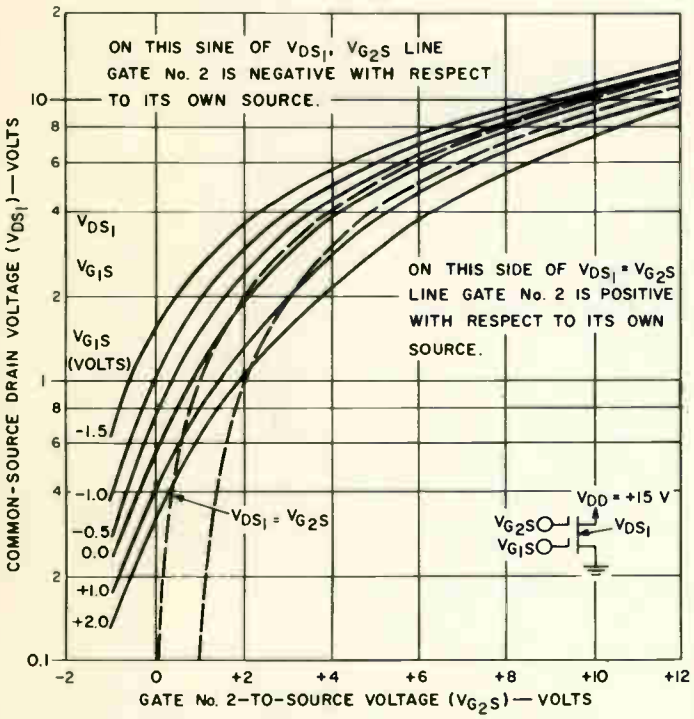


Fig. 10. Voltage distributions for the 3N140 dual-gate MOS transistor.

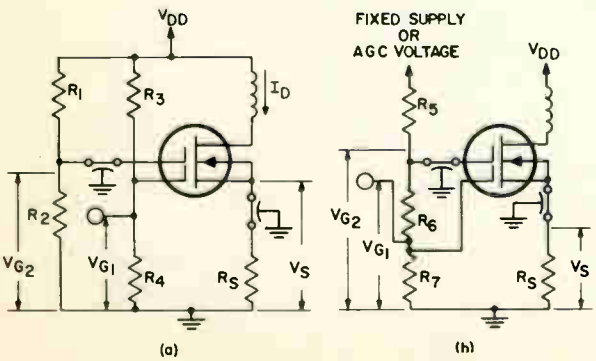
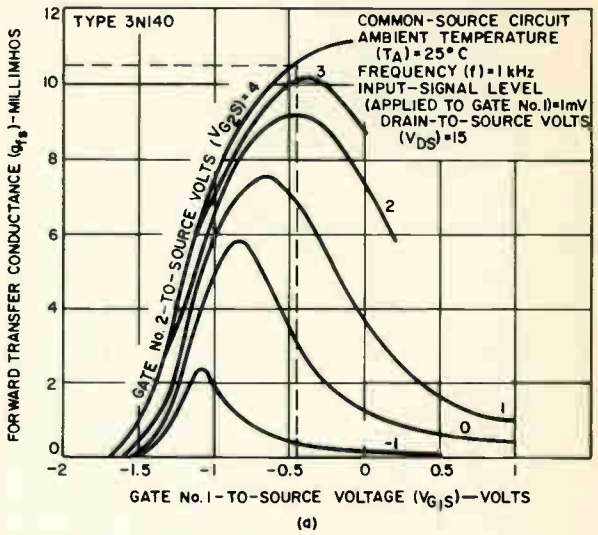


Fig. 12. Typical biasing circuits for the 3N140.



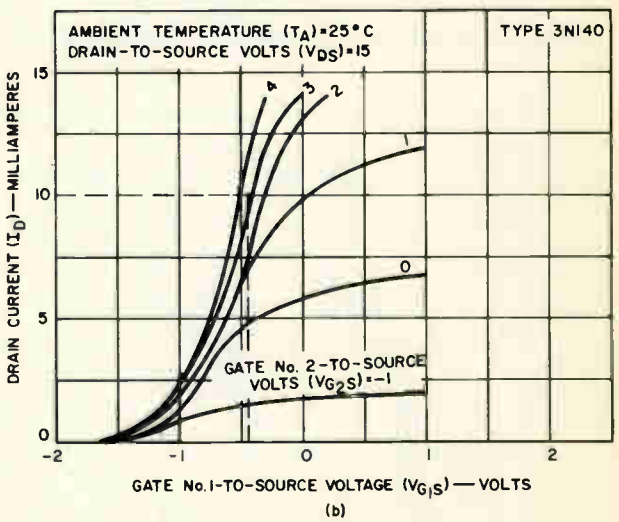


Fig. 11. Characteristics curves for the 3N140.

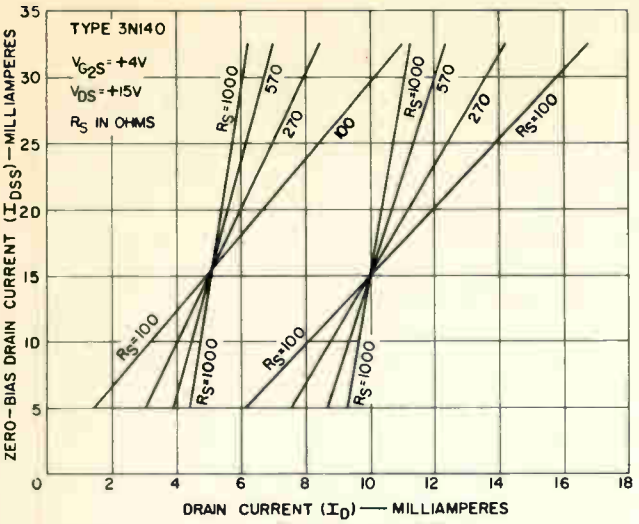


Fig. 13. Drain-current curves for various values of R_S for the 3N140.

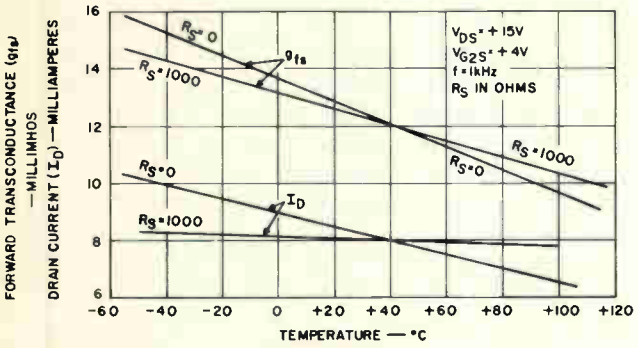


Fig. 14. Drain current and transconductance as a function of temperature for the 3N140.

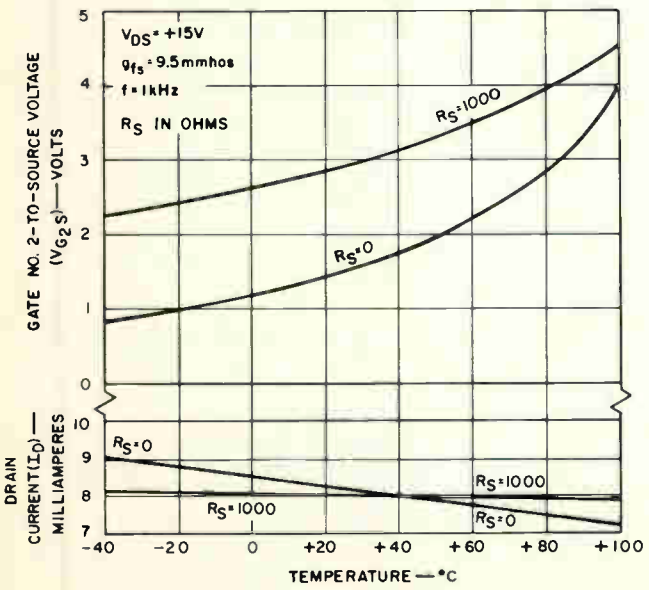


Fig. 15. Drain current and gate-No. 2-to-source voltage for constant I_D as a function of temperature for the circuit of Fig. 14 (b).

ment-type MOS transistor is to be operated at room temperature with a supply voltage of 19 V, a source resistance of 1000 Ω, and a drain current of 1 mA, as shown in Fig. 8. To complete the bias circuit, it is necessary to determine the values of R_1 and R_2 to satisfy a total input-loading requirement of 10,000 Ω.

The 2N4065 transistor has a typical threshold voltage of −5.3 V and requires a gate voltage of approximately −9.2 V for a drain current of 1 mA. (The threshold voltage V_{TH} for an enhancement-type device is comparable to the cut-off voltage V_{GS} (OFF) for a depletion-type device, and is the value of gate voltage required to initiate drain current. It is usually specified for a drain-current value between 10 and 100 mA). Circuit parameters for the network of Fig. 8 are then calculated as follows:

$$V_S = I_S R_S = (-0.001)(1000) = -1 \text{ V} \quad (11)$$

$$V_{DS} = V_{DD} - V_S = -19 + 1 = -18 \text{ V} \quad (12)$$

$$V_G = V_{GS} + V_S = -9.2 - 1 = -10.2 \text{ V} \quad (13)$$

$$\frac{R_1 + R_2}{R_2} = \frac{V_{DD}}{V_G} = \frac{19}{10.2} = 1.86 \quad (14)$$

$$\frac{R_1 R_2}{R_1 + R_2} = 10{,}000\ \Omega \quad (15)$$

$$R_1 = 18{,}600\ \Omega \quad (16)$$

$$R_2 = 21{,}500\ \Omega \quad (17)$$

Biasing the dual-gate MOS transistor

A dual-gate MOS transistor such as that shown in Fig. 9(a) is actually a combination of two single-gate MOS transistors arranged in a cascode configuration, as depicted in Fig. 9 (b). The element voltages associated with each of the individual transistors can be analyzed as follows:

$$V_{DS} = V_{DS1} + V_{DS2} \quad (18)$$

$$V_{G2S} = V_{DS1} + V_{GS2} \quad (19)$$

$$V_{G1S} = V_{GS1} \quad (20)$$

Curves of the voltage distributions for the 3N140 dual-gate MOS transistor are shown in Fig. 10. It can be seen for an applied gate-No. 1-to-source voltage V_{G1S} of zero, a supply voltage V_{DD} of +15 V and a gate-No. 2-to-source voltage V_{G2S} of + 3 V ,the actual drain voltage across the grounded-source unit is approximately +2.75 V and gate No. 2 is 0.25 V positive with respect to its own source. These curves explain the logic behind the apparently high positive gate-No. 2 voltages (in the order of +4 V) recommended for typical operation of dual-gate MOS transistors.

Operating curves for the 3N140 are shown in Fig. 11. These curves can be used to establish a quiescent operating condition for the transistor. For example, a typical application may require the 3N140 to be operated at a drain-to-source voltage V_{DS} of 15 V and a transconductance g_{fs} of 10.5 mmhos. As shown in Fig. 11(a),

the desired value of g_{fs} can be obtained with a gate-No. 2-to-source voltage V_{G2S} of +4 V and a gate-No. 1-to-source voltage V_{G1S} of −0.45 V. From Fig. 11(b), the drain current compatible with these gate voltages is 10 mA.

Two biasing arrangements which can be used to provide these operating conditions for the 3N140 are shown in Fig. 12. For the application mentioned above, it may be assumed that shunt resistance for gate No. 1 should be 25,000 Ω and the dc potential on gate No. 2 should be fixed and at rf ground. The remaining parameters for the biasing circuits can then be obtained from the curves showing I_D as a function of R_S in Fig. 13, with $R_S = 270\ \Omega$:

$$V_S = I_D R_S = +2.7\ \text{V} \quad (21)$$
$$V_{G1} = V_{G1S} + V_S = +2.25\ \text{V} \quad (22)$$
$$V_{G2} = V_{G2S} + V_S = +6.7\ \text{V} \quad (23)$$
$$V_{DD} = V_{DS} + V_S = +17.7\ \text{V} \quad (24)$$

The values of the resistance voltage dividers required to provide the appropriate gate voltages are determined in the same manner as shown previously for single-gate transistors. For the circuit of Fig. 12(a), R_3 is 197,000 Ω, R_4 is 28,600 Ω, and $R_1\ R_2 = 11/6.7$.

The circuit of Fig. 12(a) is normally used in rf-mixer applications and in rf-amplifier circuits which do not use agc. The circuit of Fig. 12(b) is recommended for the application of agc voltage to rf-amplifier stages. In this circuit, the rf signal is applied to gate No. 1, and the agc voltage to gate No. 2.

The dual-gate MOS transistor is useful in agc-supplied rf amplifiers because almost no agc power is required by the device as a result of the high dc input resistance indigenous to the MOS transistor. Another advantage provided by the MOS transistor is revealed by the ease with which it obtains delayed agc action and good cross-modulation characteristics as a function of agc. The application of agc bias to gate No. 2 while the bias on gate No, 1 is changed improves the cross-modulation characteristics of the transistor as a function of agc applied.

Biasing to compensate for temperature variations

Unlike bipolar transistors, MOS transistors exhibit a negative temperature coefficient for typical values of drain current. That is, drain current and dissipation decrease as temperature increases, and there is no possibility of I_D runaway with elevated temperature. Unfortunately, transconductance and rf power gain also decrease as temperature increases. Figure 14 shows curves of drain current and transconductance as a function of temperature. These curves also show the compensating effects produced by the use of source resistance R_S; variations in drain current are reduced significantly by use of an R_S value of 1000 Ω.

Variations in transconductance can be virtually eliminated by application of a gain-control voltage from a temperature-dependent voltage-divider network to gate No. 2. For example, the values of the resistance voltage dividers in the circuit of Fig. 12(a) were determined to provide a transconductance of 9.5 mmhos at ambient temperature, and the device temperature was then varied through the range of −45 to +100°C. The values of gate-No. 2-to-source voltage V_{G2S} required to maintain a constant transconductance over the entire temperature range, for R_S values of zero and 1000 Ω are shown in Fig. 15.

In a practical circuit, the required voltages can be applied to gate No. 2 if R_1, or the combination of R_1 and R_2, is a temperature-sensitive resistor that is thermally linked to the MOS transistor package. This thermistor network can be designed to provide a desired voltage characteristic at gate No. 2 either to keep the transconductance constant or to permit some variation with temperature to compensate for changes in other stages. The effects of temperature given in percentages on these other stages may be summarized as follows: R_{in}—one percent; C_{in}—one percent; $C_{feedback}$—one percent; R_{out}—plus 45 percent; C_{out}—one percent.

The data was measured on a 3N140 MOS transistor in the circuit of Fig. 12(a). Drain current was 8 mA, frequency was 200 MHz, and the temperature varied from 0 to 100°C.

Summary

All field-effect transistors may be biased similarly. Uniform quiescent operating points can be easily achieved in MOS field-effect transistors by employing circuit designs that incorporate a source resistance. For a given I_{DSS} range, the value of the source resistance inversely affects the in-circuit I_D spread. An increase in the value of the source resistance minimizes variations in I_D as a function of temperature. The dual-gate MOS field-effect transistor is ideally suited for use in gain-controlled stages; dual-gate transistor biasing can provide various types of agc action including temperature compensation to assure constant output. **EEE**

Acknowledgements

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