ONE DOLLAR

TRANSISTOR MANUAL

THIRD EDITION

- CIRCUITS
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- SPECIFICATIONS

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BASIC SEMICONDUCTOR THEORY

Transistors and junction rectifiers are the natural outgrowth of our rapidly advancing technology and the need for electronic devices with small size and high efficiency and reliability. They are made from materials known as semiconductors – materials that will pass more current than an insulator, but not as much as a metal. The two materials now being utilized in the manufacture of semiconductor products are Germanium and Silicon.

It is possible to change the electrical characteristics of semiconductor materials by adding closely controlled amounts of certain impurities. Impurities such as arsenic and antimony cause a surplus of electrons, or free negative charges, while others such as gallium and indium cause a deficiency of electrons, which may be considered as holes in the crystalline structure, and act as mobile positive charges.

A crystal with a surplus of holes, or positive active electric "particles" is known as p-type while a crystal with a surplus of electrons, or negative active electric particles is known as n-type. As might be expected, when a positive charge and a negative charge meet in the crystal, they combine and cease to exist as mobile charge carriers – the excess mobile electron meets a mobile electron deficiency or hole and fills the hole, becoming a fixed part of the crystalline structure.

Therefore, in a semiconductor material such as silicon or germanium, we have a material which is a very poor conductor of electricity unless we add mobile charge carriers, and we can add either positive or negative charge carriers. The significance of this will become apparent when we consider what happens when we join a crystal of p-type and a crystal of n-type material together forming a distinct boundary, or junction, between the two types, as in Figure 1.

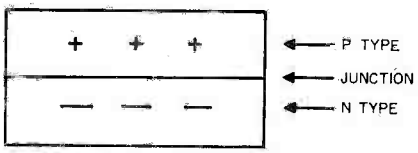


FIGURE 1

This crystal is now capable of passing current readily in one direction while blocking current in the opposite direction and we have a useful electronic device, a rectifier.

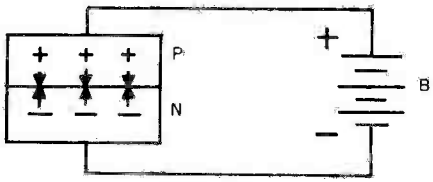


FIGURE 2

When a battery is attached as shown in Figure 2 the electrons will be pushed towards the junction by the negative voltage of the battery and combine with holes attracted towards the junction by the battery's negative voltage. Electrons constantly enter the crystal at the n-terminal to replenish the electrons that have combined with holes, and electrons leave the p-terminal to replenish the hole supply of the p-type portion of the crystal, and current flows.

If we reverse the polarity of the battery as in Figure 3 we have the following situation:

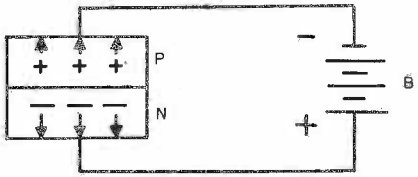


FIGURE 3

Now the positive and negative particles are drawn away from the junction by the battery's voltage, leaving the section of the crystal near the junction practically void of charge carriers and crystal effectively blocks current. A few random charge carriers do remain in the junction area allowing a minute current to pass. This current is known as "leakage current" and is usually in the order of a few microamperes.

We have seen how semiconductors are capable of rectifying current by the use of a single junction within a crystal. By adding a second junction and making a P-N-P or N-P-N sandwich of N and P types we have a device capable of amplification known as a transistor.

The transistor may be compared to a triode tube in some ways, so let's quickly review the triode tube. The tube represented in Figure 4 has three distinct elements:

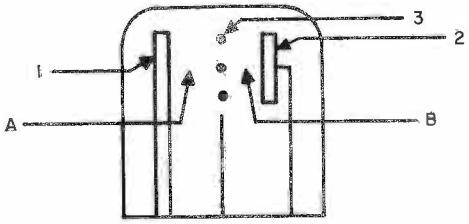


FIGURE 4

1. The cathode, which emits electrons; 2. The plate which collects the emitted electrons, and 3. The control grid, which controls the charge concentration of the spaces A and B separating the elements by altering the charge of these spaces. When a large fixed voltage is applied between the cathode and plate and a small varying voltage is applied to the control grid, the plate current varies as much as it would if we made large changes in the plate voltage, giving us a device capable of amplifying voltage.

Now consider the transistor. Again we have three elements, separated by junctions as shown in Figure 5.

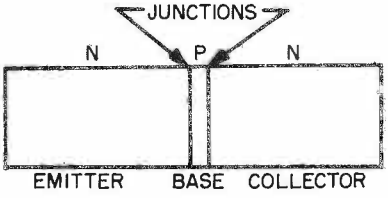


FIGURE 5

Here the emitter emits electrons, the collector collects electrons and the base controls the flow of electrons by controlling the charge concentration in the base region, so in the broadest sense, the function of the three elements in the triode tube and the transistor are similar. However, in the transistor we are amplifying current, not voltage, and its operation is not really as analogous to the tube's operation as this comparison shows.

Let's look a little closer at how a transistor works. First of all we will put the transistor in a circuit as in Figure 6.

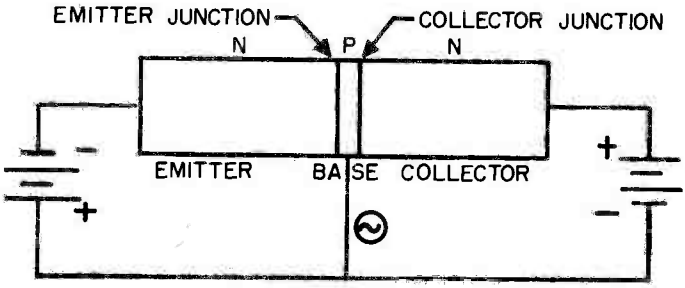


FIGURE 6

Here we see that the emitter junction will pass current easily, because it has a forward bias. The collector junction however, will not pass current from the collector to base, because this junction is back biased. These bias conditions are necessary for transistor operation. It is found that the majority of the current flows between the emitter and the collector because of the large number of electrons from the emitter which diffuse through the very thin base region and into the collector without combining with the holes in the base. As the base is made more positive, more electrons are pulled out of the emitter and are made available for diffusion into the collector.

If the base is made less positive, less electrons are pulled from the emitter, so less reach the collector. The electrons that enter the base, but do not reach the collector, combine with holes in the base and contribute to the base current, reducing the gain of the transistor. To reduce the base current, the base is kept as thin as possible (usually less than a thousandths of an inch thick) and the hole content kept to a minimum by using high-purity material, or in other words, the base material is only slightly "p" type material.

The ratio of the collector current to the base current is called beta, usually shown on specification sheets as h_{FE}, and the ratio of the collector current to the emitter current is called alpha, usually shown as h_{FB}. Of course it is desirable to have the alpha of a transistor as high as possible and alphas of 0.95 to 0.99 are common in commercial transistors.

No current (except a small leakage current) will flow in the collector circuit unless current is introduced into the emitter. Since very little voltage (.1 to .5 volts) is needed to cause appreciable current flow into the emitter, the input power is very low. Almost all the emitter current (emitter current times alpha) will flow in the collector circuit where the voltage can be as high as 45 volts. Therefore, a relatively large amount of power can be controlled in an external load and the power gain (G_e) of a transistor (power out/power in) can be up to 40,000 in some applications.

TRANSISTOR CONSTRUCTION TECHNIQUES

The most common type of junction transistor is the PNP diffused alloyed type. This transistor is made by taking a wafer of "N" type germanium, mounting it on a holder and pressing indium dots into each side. The assembly is then heated in a furnace until the indium melts and alloys with the germanium forming a "P" layer within the "N" type germanium. The complete assembly is shown by Figure 7.

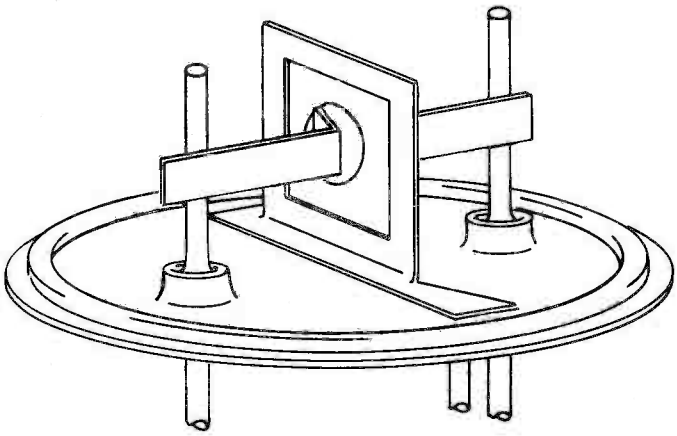


FIGURE 7

By changing the size of the indium dots and the depth to which the indium is alloyed into the base material, it is possible to obtain a transistor optimized either for audio amplifiers or high speed switching. In addition, by starting with P type germanium, it is possible to make a NPN transistor. With the alloy type of structure, it is possible to pass currents of up to ½ an ampere through the transistor. This structure is not generally suitable for high frequency linear amplifiers since the indium dots produce a high capacitance between collector and base making the unit inherently unstable at high frequencies.

The rate grown transistor is produced by an entirely different technique. A bar of germanium is grown from a bath of molten germanium so doped that the material will change from "P" type to "N" type depending on the temperature and rate of pulling. By suitable growing techniques, 10 to 15 thin "P" type layers are formed in a bar about the size of a cigar. This bar is then sawed up into pieces about 10 mils by 10 mils by 100 mils with the thin "P" layer in the center and long "N" regions on each side. About 7 to 10 thousand transistor bars can be cut from each ingot of germanium. The internal appearance of one of these transistors is shown in Figure 8. This transistor has a low collector capacitance and has excellent gain up to several megacycles. It is stable at high frequencies and is ideally suited for the radio frequency section of broadcast receivers. A rate grown transistor also makes an excellent unit for high speed gates and counting circuits.

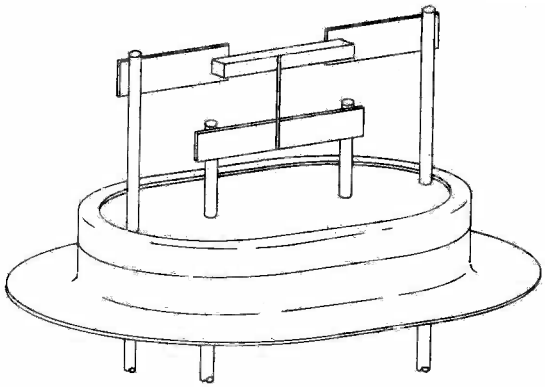


FIGURE 8

The meltback method of transistor construction starts off with a bar of germanium about 10 x 10 x 100 mils. The end of the bar is melted and allowed to refreeze very quickly. By suitable doping of the original material, the junction between the melted portion and the unmelted portion becomes a thin layer of "P" type material and the melted and unmelted portion of "N" type material remains "N" type material. This transistor is essentially a rate grown transistor, but the rate growing is done on an individual small bar rather than on the large germanium ingot. By the addition of an extra base connection to a triode, a tetrode is formed. If a current is passed through the base region from one base lead to the other, the active portion of the base region is electrically narrowed and high gain is possible up to 200 mc.

Another method of making semiconductor devices is by gaseous diffusion of impurities. In this type of construction, the base material and the impurity are sealed together in a quartz tube and the complete assembly heated to about 1200°C. At this high temperature, the impurities form a gas which diffuses into the surface of the base material forming P or N type layers. With this technique, it is possible to form very large flat junctions of precisely controlled thickness. An example of a transistor built using this technique is the 2N451 silicon 85 watt power transistor shown in Figure 9.

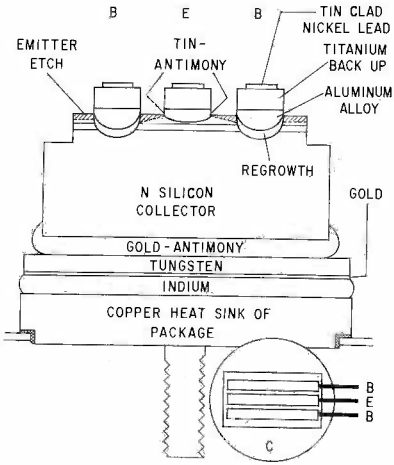


FIGURE 9

By using two impurities diffused simultaneously, it is possible to form a P type layer .2 mil thick and an N type emitter layer .3 mil thick. By making contacts to the base and emitter regions, a transistor is produced capable of carrying up to 10 amperes. Since the diffused layers are very thin, the frequency response of this power transistor is good up to 5 to 10 mc.

Another recently developed device using diffusion techniques is the Controlled Rectifier. A Controlled Rectifier is a four layer PNPN structure as shown in Figure 10.

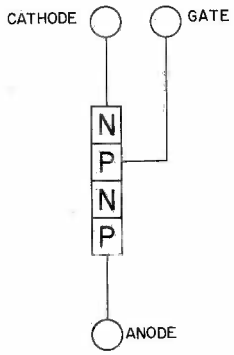


FIGURE 10

By making connections to three of the layers, a regenerative switch is obtained which acts in a manner very similar to a vacuum tube thyratron. This device will switch on in less than 1 μsec and with the large areas made possible by diffusion, it will carry 15 amperes continuously and 150 amperes on a surge basis.

G-E silicon signal transistors are grown junction devices with a diffused base and utilize an entirely new type of pellet mounting to obtain maximum mechanical strength and reliability. This construction, used with both the silicon triode and the silicon unijunction transistors is called the ceramic disk construction or fixed-bed mounting, and is shown in Figure 11. A wafer of ceramic which has the same coefficient as the pellet forms the basic mechanical structure. Gold is deposited on the disk in three areas to form the electrical contacts. The silicon bar is mounted across a narrow slit in the disk and between two of the gold contacts. The third connection is made between the silicon bar and the third gold contact by means of a small aluminum wire. The aluminum wire forms the base contact of the silicon triode, and the emitter contact of the unijunction transistor. After the transistor is assembled on the ceramic disk, the entire disk assembly is mounted on a standard header by soldering the gold to the transistor leads.

The use of this fixed-bed construction results in a number of important advantages:

1. The mechanical strength of the structure is increased greatly since the basic transistor structure is not subjected to stress during shock and vibration.
2. The transfer of heat between the transistor bar and the case is improved permitting higher power ratings.
3. The possibility of failure from extreme temperature cycling is greatly reduced because of the matched temperature coefficients of the structure.
4. The electrical characteristics are more stable and reproducible from unit to unit because of the improved uniformity of the mechanical structure.

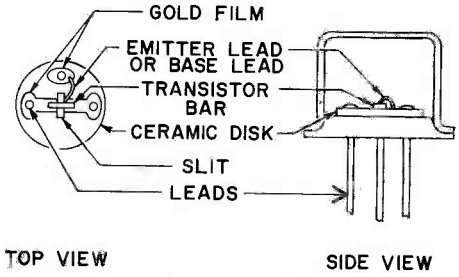


FIGURE 11

MAJOR PARAMETERS

There are many properties of a transistor which can be specified, but this section will only deal with the more important specifications. A fundamental limitation to the use of transistors in circuits is BV_{CER}, the breakdown voltage in the grounded emitter connection. The grounded emitter breakdown voltage is a function of the resistance from the base to the emitter and it is necessary to specify this resistance shown as R in Figure 12.

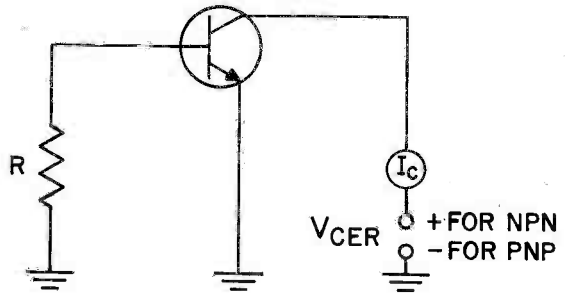


FIGURE 12

Since the breakdown voltage is not sharp, it is also necessary to specify a value of collector current at which breakdown will be considered to have taken place. For example, in PNP audio transistors the collector current is specified to be less than 600 μa with 25 volts applied and the resistance R equal to 10,000 ohms. With NPN transistors, the collector current should be less than 300 μa with 15 volts applied, and the base open-circuited.

The small signal parameters of transistors are usually specified in terms of the "h" or hybrid parameters. These parameters are defined for any network by the following equations:

$$e_{in} = h_i\, i_{in} + h_r\, e_{out}$$
$$i_{out} = h_f\, i_{in} + h_o\, e_{out}$$

where h_i = input impedance (ohms)
h_r = feedback voltage ratio (dimensionless)
h_f = forward current transfer ratio (dimensionless)
h_o = output conductance (mhos)

For transistors, a second subscript is added to designate which terminal of the transistor is grounded. For example, h_{fe} is the grounded emitter forward current transfer ratio.

The current transfer ratio is equal to the ratio of an a-c variation in collector current to an a-c variation in base current. This current gain can be specified either

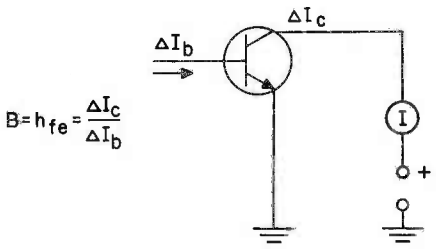


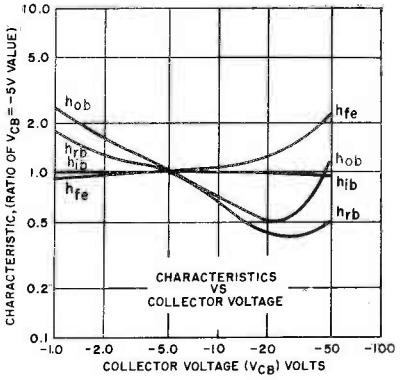
FIGURE 13

for small a-c values of base current or for large values of base current in which case it would be known as h_{FE}, the d-c current gain. The current gain is the most important property of a transistor in determining the gain of audio amplifiers.

The small signal "h" parameters of a transistor are a function of frequency and bias conditions. For a P-N-P alloy audio transistor, typical h parameters at 270 cps, and bias conditions of 5 volts (collector to emitter) and 1 ma collector current are:

	Grounded Base		*Grounded Emitter*
h_{ib}	30 ohms	h_{ie}	1500 ohms
h_{rb}	4×10^{-4}	h_{re}	11×10^{-4}
h_{fb}	−0.98	h_{fe}	50
h_{ob}	1×10^{-6} mhos	h_{oe}	50×10^{-6}

The h parameters at other bias conditions are shown by Figure 14.



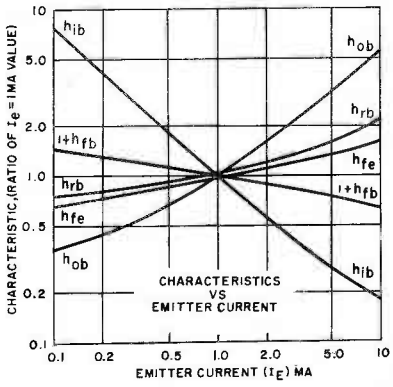


FIGURE 14

With transistors used as radio frequency amplifiers, it is necessary to specify a transformer coupled power gain as indicated in Figure 15. The power gain is the ratio of output power to input power under conditions where the input and output impedances are matched by means of the transformers. The input and output impedances must also be specified to select the proper transformer.

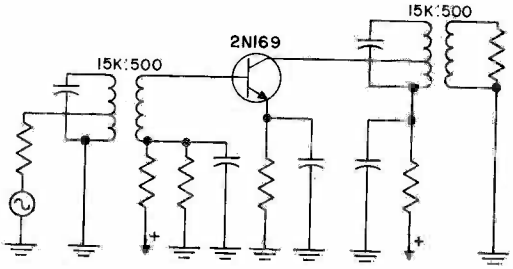


FIGURE 15

Another common transistor specification is the alpha cut-off frequency. This is the frequency at which the grounded base current gain has decreased to 0.7 of its low frequency value. For audio transistors, the alpha cut-off frequency is in the region of 1 mc. For transistors used in the rf section of radios, the alpha cut-off frequency should be 3 to 15 mcs. Other examples of transistor specifications are shown on the specification sheets starting on page 110.

RECTIFIER CONSTRUCTION

Germanium and Silicon rectifiers are two-element semiconductor devices constructed around the single P-N junction described earlier in Figures 1, 2 and 3. Because of their inherently low forward resistance and high reverse resistance, these devices are widely used for converting alternating current to direct current, to block reverse currents in control circuits, and to increase the power gain of magnetic amplifiers through the effects of self-saturation.

Rectifiers are generally designed to handle power rather than small signals, and sizeable currents in addition to high voltages. These capabilities are attained through use of large cross-sectional area junctions and efficient means for dissipating heat losses, such as fins, heat sinks, etc.

A section through a typical low power germanium rectifier is shown in Figure 16. The germanium pellet, which is soldered to the base disc, is approximately 1/16 inch square. Yet the junction of this germanium pellet with the indium alloy can rectify

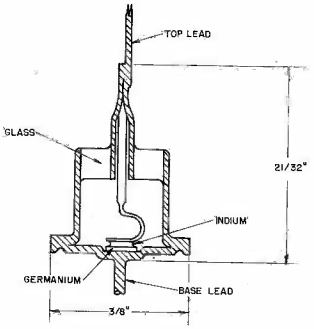


FIGURE 16

over 1/4 ampere at room temperature and block voltages in the reverse direction up to 300 volts peak. This latter rating is called the "Peak Inverse Voltage" of the cell. When this same cell is mounted on a 1-1/2 inch square fin as shown in Figure 17, its current carrying capabilities are increased to over 3/4 ampere at room temperature.

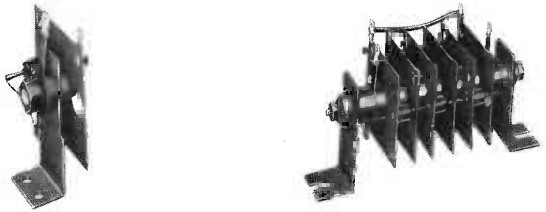


FIGURE 17

Germanium rectifiers of this type offer outstanding advantages over other types of rectifiers:

1. Low forward drop, unexcelled by any other type of rectifier with the same inverse voltage rating.
2. Reverse resistance so high as to be negligible for most applications.
3. No aging, and therefore indefinitely long life. Also, no filament to burn out.
4. No junction forming required . . . it is always ready to function after prolonged idleness.
5. Withstands corrosive atmospheres and fluids . . . the junction is protected by a welded hermetic seal.
6. Wide temperature range, from —65°C to as high as +85°C.
7. Ability to withstand shock and vibration . . . no moving parts, flimsy supports, or sensitive filament.

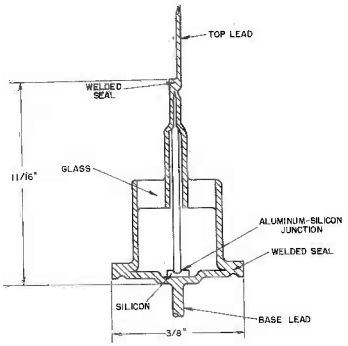


FIGURE 18

When ambient temperatures exceed 85°C, or when extremely low reverse currents are required, the silicon rectifier shown in cross-section in Figure 18 can be used. In outward appearance, the silicon rectifier looks identical to the germanium rectifier. However, instead of a germanium-indium junction inside, this cell employs the junction of a piece of aluminum wire alloyed into a wafer of the metal silicon. This device can operate in ambients up to 165°C and can handle currents up to 3/4 ampere at room temperature. Whereas its forward resistance is approximately 40% higher than a germanium device of the same rating, its reverse leakage current may be several hundred times less than a comparable germanium cell. It too can be mounted on a fin for higher current rating.

BIASING

A major problem with transistor amplifiers is establishing and maintaining the proper collector to emitter voltage and collector current (called biasing conditions) in the circuit. These biasing conditions must be maintained despite variations in ambient temperature and variations of gain and leakage current between transistors of the same classification.

If the current gain (h_{FE}) of a transistor was constant with temperature and the leakage current was negligible, it would be possible to set up the bias conditions by feeding a base current of the proper magnitude into the transistor as indicated by Figure 19.

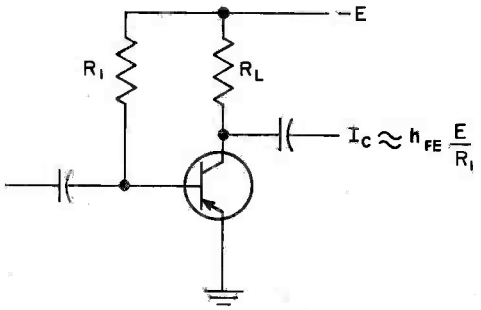


FIGURE 19

The collector current that flows is equal to $h_{FE}\frac{E}{R_1}$. This type of biasing is extremely dependent upon the h_{FE} of the transistor and is not recommended except in cases where the biasing resistance can be individually adjusted for optimum results.

In general, it is necessary to use some type of feedback circuit so that the bias conditions of the transistor tend to be relatively independent of the transistor parameters. The use of an emitter resistor will provide feedback to stabilize the operating point. This type of biasing is shown by Figure 20.

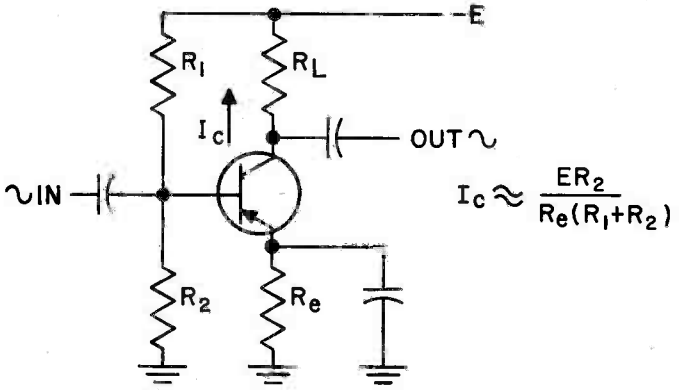


FIGURE 20

A voltage divider consisting of resistors R_1 and R_2 is connected to the base and the resistance R_e is placed in the emitter. Since the emitter junction is forward biased, the current that flows in the emitter circuit is essentially equal to the voltage at the base divided by R_e. To prevent degeneration of the a-c signal to be amplified, the emitter resistance is by-passed with a large capacitance. Good design practice is to make R_2 no larger than 5 to 10 times R_e. A typical value of R_e is 500-1000 ohms. The method outlined above does not consider the variations of base to emitter voltage drop or the variations of leakage current with temperature. A more general approach to the biasing problem is to consider the circuit of Figure 21.

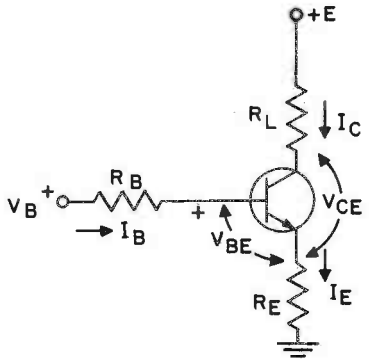


FIGURE 21

From this general circuit, the following equations can be derived:

$$V_B = [(1 - \alpha)\, R_B + R_E]\, I_E + V_{BE} - I_{CO} R_B$$

V_{BE} is the base to emitter voltage drop at the specified biasing point. At 25°C this is 0.2 volts for germanium and 0.7 volts for silicon. At higher temperatures, V_{BE} is −0.1 for germanium and 0.5 for silicon. If the minimum acceptable emitter current, minimum alpha, maximum emitter current and maximum alpha and maximum leakage current are known, the following equation can be derived for the value of R_B:

$$R_B = \frac{(I_E{}^{max} - I_E{}^{min})\, R_E + V_{BE}{}^{min} - V_{BE}{}^{max}}{I_{CO}{}^{max} - (1 - \alpha^{max})\, I_E{}^{max} + (1 - \alpha^{min})\, I_E{}^{min}}$$

As an example, consider the 2N525 transistor with the following characteristics used in a typical circuit:

$E = 20$ volts
$R_L = 8.2$ K ohms
$I_{CO}{}^{max} = 100\ \mu$amp 55°C
$h_{FE}{}^{max} = 66,\ \alpha^{max} = \frac{66}{67}$
$h_{FE}{}^{min} = 30,\ \alpha^{min} = \frac{30}{31}$
$V_{BE}{}^{max} = 0.2,\ V_{BE}{}^{min} = -0.1$
Desired $I_E{}^{max} = 1.24$ ma
Desired $I_E{}^{min} = 0.81$

Substituting these values into the equation and assuming various R_E's gives the following results for R_B:

for $R_E =$ 1k, $R_B = 1.2$k
$R_E = 2.2$k, $R_B = 5.8$k
$R_E = 3.3$k, $R_B =$ 10k

By substituting the value of R_B into the original equation, a value of V_B can be obtained. For example, using a 3.3K emitter resistance and a 10K value of R_B, the value of V_B equals 3.1 volts. Transforming from V_B and R_B to a more practical voltage divider type biasing is done with the equations in Figure 22.

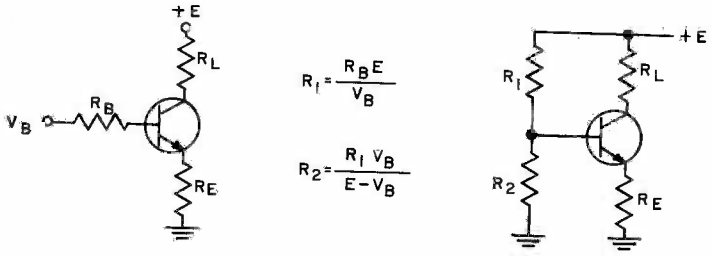


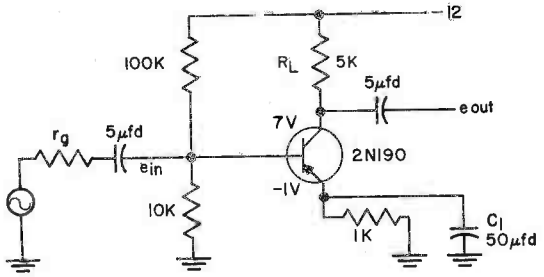
FIGURE 22

By use of the above approach, it is possible to design a bias circuit which will accommodate all the variations of the transistor and maintain the bias points within the value desired.

BASIC AMPLIFIERS

SINGLE STAGE AUDIO AMPLIFIER

Figure 23 shows a typical single stage audio amplifier using a 2N190 PNP transistor.



SINGLE STAGE AUDIO AMPLIFIER
FIGURE 23

With the resistance values shown, the bias conditions on the transistor are 1 ma of collector current and six volts from collector to emitter. At frequencies at which C_1 provides good by-passing, the input resistance is given by the formula: $R_{in} = (1 + h_{fe})\, h_{ib}$. At 1 ma for a design center 2N190, the input resistance would be 37×30 or about 1100 ohms.

The a-c voltage gain $\frac{e_{out}}{e_{in}}$ is approximately equal to $\frac{R_L}{h_{ib}}$. For the circuit shown this would be $\frac{5000}{30}$ or approximately 167.

The frequency at which the voltage gain is down 3 db from the 1 Kc value depends on r_g. This frequency is given approximately by the formula:

$$\text{low } f_{3db} \approx \frac{1+h_{fe}}{6.28(r_g C_1)}$$

TWO STAGE R-C COUPLED AMPLIFIER

The circuit of a two stage R-C coupled amplifier is shown by Figure 24. The input impedance is the same as the single stage amplifier and would be approximately 1100 ohms.

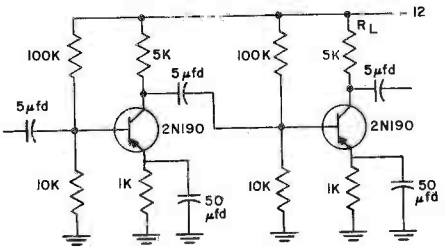


FIGURE 24

The load resistance for the first stage is now the input impedance of the second stage. The voltage gain is given approximately by the formula:

$$A_v \approx h_{fe} \frac{R_L}{h_{ib}}$$

More exact formulas for the performance of audio amplifiers may be found in the Reading List at the end of this manual.

CLASS B PUSH-PULL OUTPUT STAGES

In the majority of applications, the output power is specified so a design will usually begin at this point. The circuit of a typical push-pull Class B output stage is shown in Figure 25.

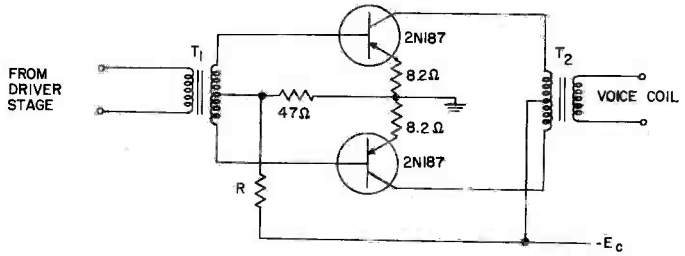


FIGURE 25

The voltage divider consisting of resistor, R and the 47 ohm resistor gives a slight forward bias on the transistors to prevent cross-over distortion. Usually about 1/10 of a volt is sufficient to prevent cross-over distortion and under these conditions, the no-signal total collector current is about 1.5 ma. The 8.2 ohm resistors in the emitter leads stabilize the transistors so they will not go into thermal runaway when the junction temperature rises to 60°C. Typical collector characteristics with a load line are shown below:

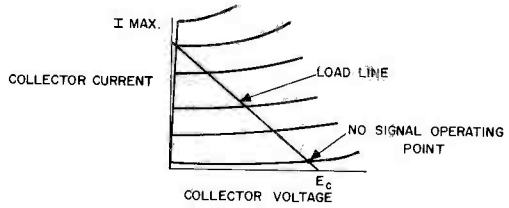


FIGURE 26

It can be shown that the maximum a-c output power without clipping using a push-pull stage is given by the formula:

$$P_{out} = \frac{I_{max} \quad E_c}{2}$$

Since the load resistance is equal to

$$R_L = \frac{E_c}{I_{max}}$$

and the collector to collector impedance is four times the load resistance per collector, the output power is given by the formula:

$$P_o = \frac{2 \quad E_c^2}{R_{c-c}} \tag{1}$$

Thus, for a specified output power and supply voltage the collector to collector load resistance can be determined. For output powers in the order of 50 mw to 750 mw, the load impedance is so low that it is essentially a short circuit compared to the output impedance of the transistors. Thus, unlike small signal amplifiers, no attempt is made to match the output impedance of transistors in power output stages.

The power gain is given by the formula:

$$\text{Power Gain} = \frac{P_{out}}{P_{in}} = \frac{I_o^2 \quad R_L}{I_{in}^2 \quad R_{in}}$$

Since $\frac{I_o}{I_{in}}$ is equal to the current gain, Beta, for small load resistance, the power gain formula can be written as:

$$P.G. = \beta^2 \frac{R_{c-c}}{R_{b-b}} \tag{2}$$

where R_{c-c} = collector to collector load resistance.

R_{b-b} = base to base input resistance.

β = grounded emitter current gain.

Since the load resistance is determined by the required maximum undistorted output power, the power gain can be written in terms of the maximum output power by combining equations (1) and (2) to give:

$$P.G. = \frac{2\beta^2 E^2 c}{R_{b-b} P_{out}} \tag{3}$$

CLASS A OUTPUT STAGES

A Class A output stage is biased as shown on the collector characteristics below:

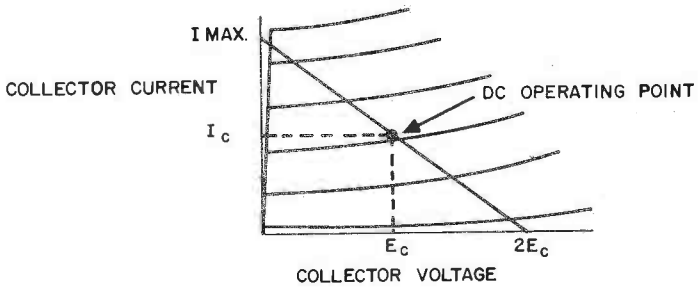


FIGURE 27

The operating point is chosen so that the output signal can swing equally in the positive and negative direction. The maximum output power without clipping is equal to:

$$P_{out} = \frac{E_c \quad I_c}{2}$$

The load resistance is then given by the formula:

$$R_L = \frac{E_c}{I_c}$$

Combining these two equations, the load resistance can be expressed in terms of the supply voltage and power output by the formula below:

$$R_L = \frac{E_c^2}{2 P_o} \tag{4}$$

For output powers of 10 mw and above, the load resistance is very small compared to the transistor output impedance and the current gain of the transistor is essentially the short circuit current gain Beta. Thus for a Class A output stage the power gain is given by the formula:

$$P.G. = \frac{\beta^2 R_L}{R_{in}} = \frac{\beta^2 E_c^2}{2 R_{in} P_o} \tag{5}$$

CLASS A DRIVER STAGES

For a required output power of 250 mw, the typical gain for a push-pull output stage would be in the order of 23 db. Thus the input power to the output stage would be about 1 to 2 mw. The load resistance of a Class A driver stage is then determined by the power that must be furnished to the output stage and this load resistance is given by equation (4). For output powers in the order of a few milliwatts, the load resistance is not negligible in comparison to the output impedance of the transistors, therefore, more exact equations must be used to determine the power gain of a Class A driver stage. From four terminal network theory, after making appropriate approximations, it can be shown that the voltage gain is given by the formula:

$$A_V = \frac{R_L}{h_{ib}} \tag{6}$$

where h_{ib} = grounded base input impedance.

The current gain is given by the formula:

$$A_I = \frac{\alpha}{1 - \alpha + R_L h_{ob}} \tag{7}$$

where h_{ob} = grounded base output conductance.

The power gain is the product of the current gain and the voltage gain, thus unlike the formula for high power output stages, there is no simple relationship between required output power and power gain for a Class A driver amplifier.

DESIGN CHARTS

Figures 28 through 36 are design charts for determination of transformer impedances and typical power gains for Class A driver stages, Class A output stages, and Class B push-pull stages. Their use can be best understood by working through a typical example. It will be assumed that it is desired to design a driver and push-pull amplifier capable of delivering a 250 mw with a 9 volt supply. Using Figure 28, for 250 mw of undistorted output power, the required collector to collector load resistance is 450 ohms. From Figure 30 using a typical 2N187, the power gain is 22.5 db. In numerical terms, a power gain of 22.5 db is 178. Therefore, the required input power to the driver stage would be:

$$P_{in} = \frac{250}{178}$$

or 1.4 mw. Assuming about 70% efficiency in the transformers, the required output power of the driver stage will be 2 mw. From Figure 32, for 2 mw of undistorted output power, the load resistance is slightly over 10,000 ohms so a 10,000 ohm transformer could be used. From Figure 35 assuming a 2N191 driver transistor, the power gain is 41 db. The typical power gain of the two stages using a 2N191 driver and

2N187's in the output would be 63.5 db. The secondary impedance of the driving transformer should be 2,000 ohms center tapped as shown on the specification sheet for the 2N186, 2N187 and 2N188. The secondary impedance of the output transformer should be selected to match the impedance of the load.

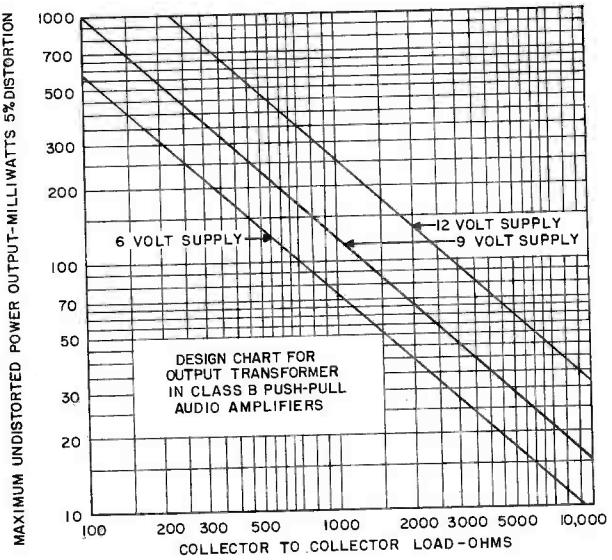


FIGURE 28

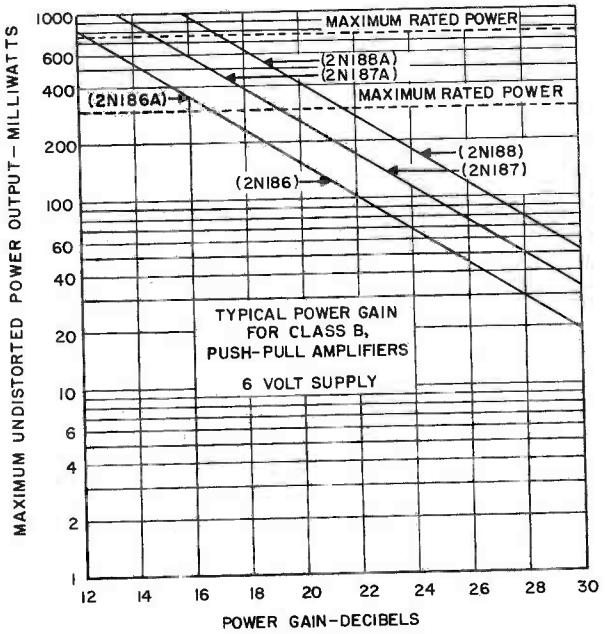


FIGURE 29

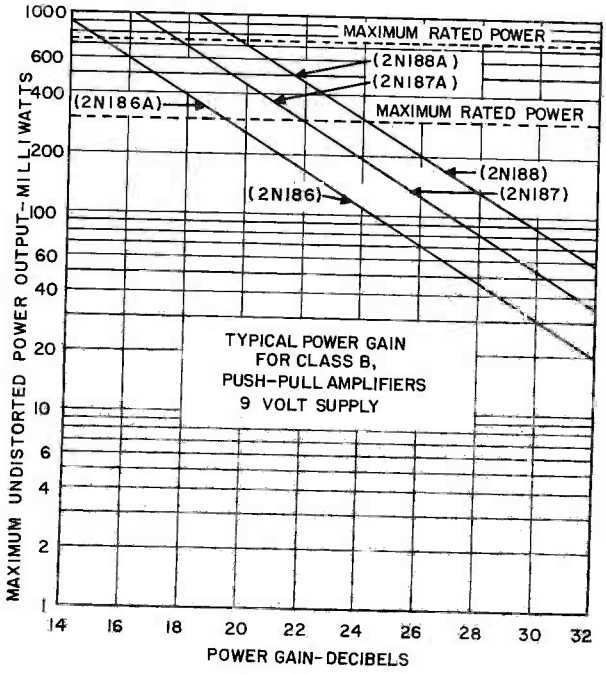


FIGURE 30

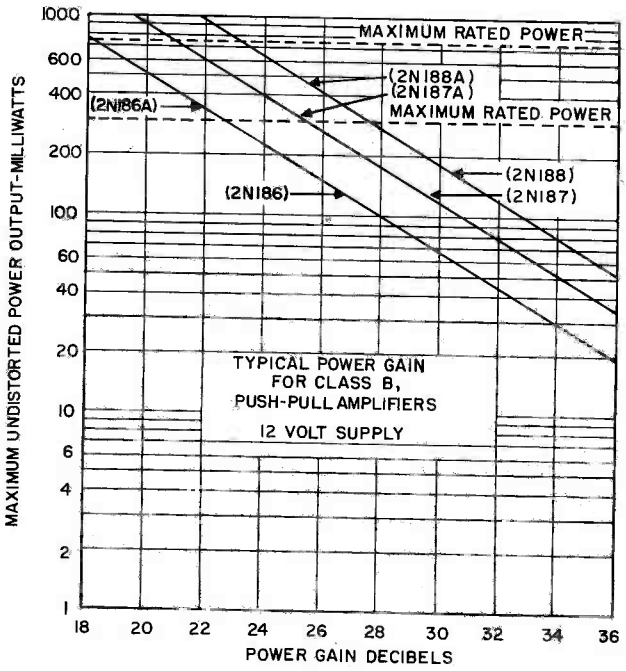


FIGURE 31

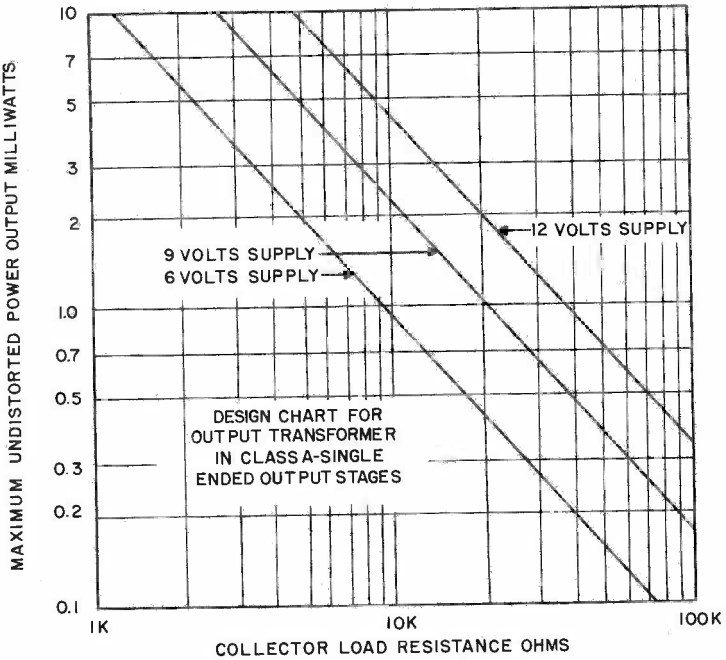


FIGURE 32

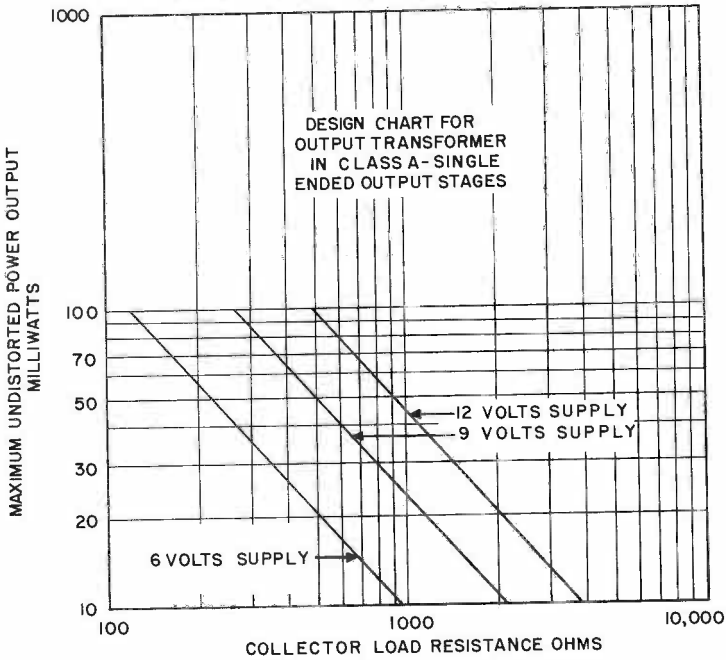


FIGURE 33

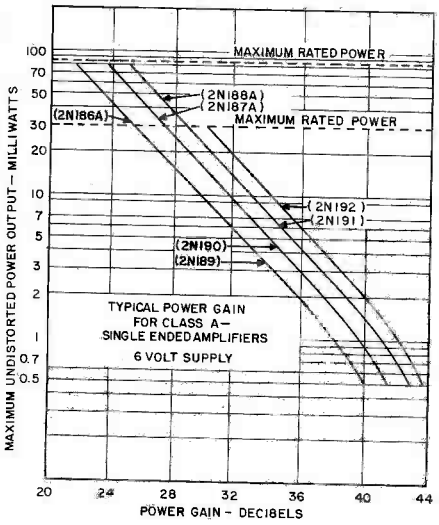


FIGURE 34

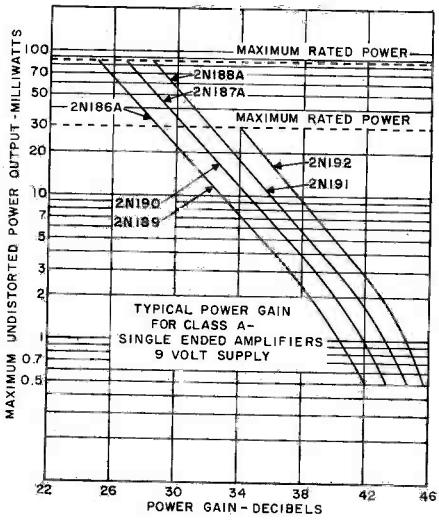


FIGURE 35

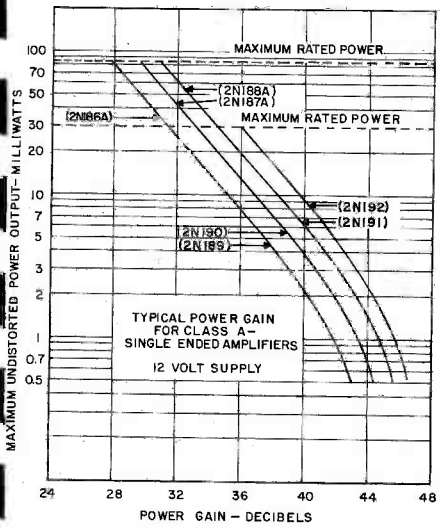
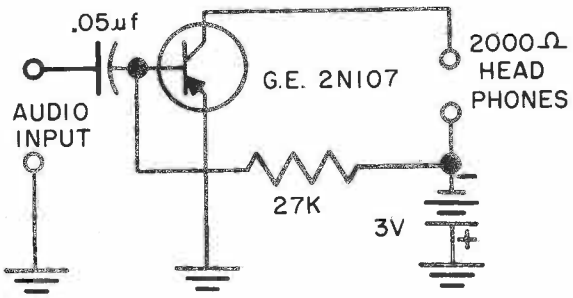
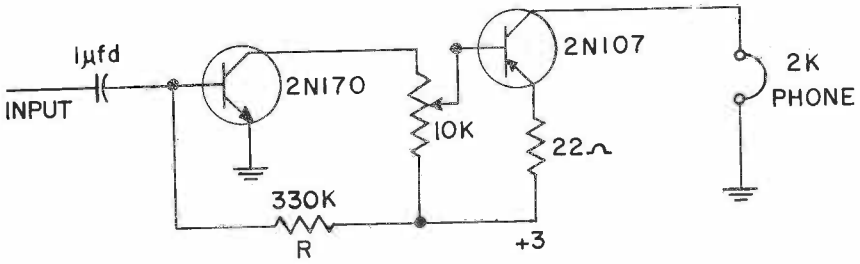


FIGURE 36

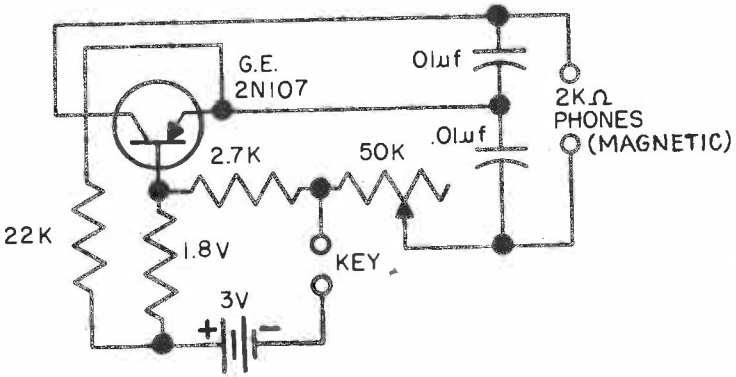


SIMPLE AUDIO AMPLIFIER
FIGURE 37

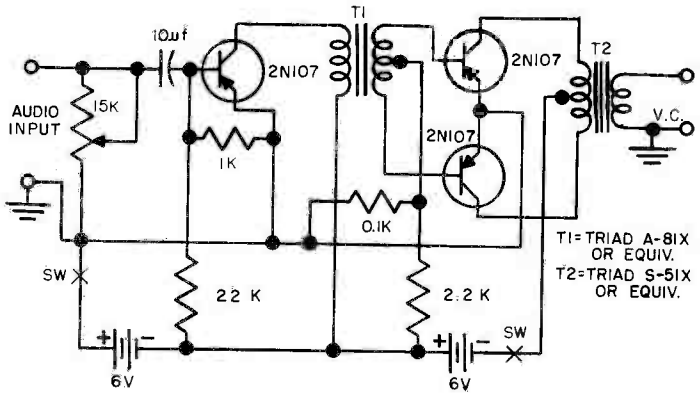


R SHOULD BE ADJUSTED FOR OPTIMUM RESULTS

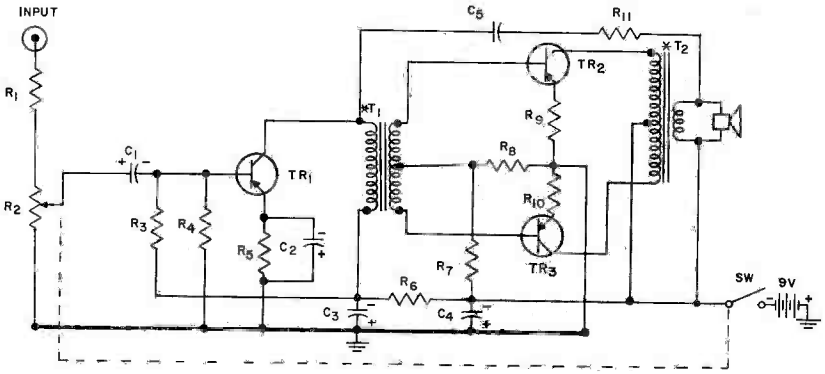
DIRECT COUPLED "BATTERY SAVER" AMPLIFIER
FIGURE 38



CODE PRACTICE OSCILLATOR
FIGURE 39



LOUDSPEAKER AUDIO AMPLIFIER
FIGURE 40



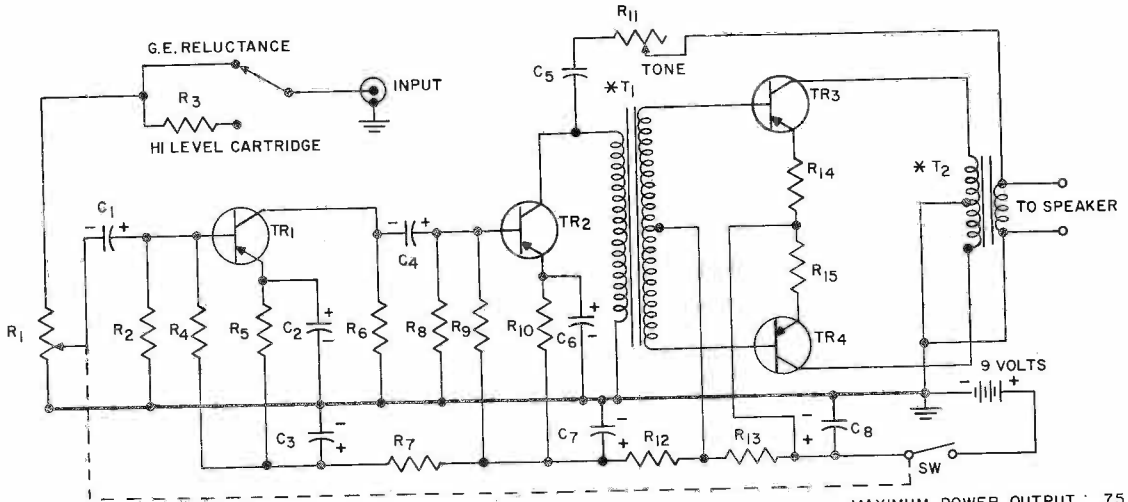
R_1 —— 220,000 OHM
R_2 —— VOLUME CONTROL 10,000 OHM 1/2 W AUDIO TAPER
R_3 —— 68,000 OHM
R_4 —— 10,000 OHM
R_5 —— 470 OHM
R_6 —— 220 OHM
R_7 —— 1800 OHM
R_8 —— 33 OHM
R_9, R_{10} —— 8.2 OHM
R_{11} —— 4.7K OHM

C_1 —— 6μfd, 12V
C_2 —— 100μfd, 3V
C_3, C_4 —— 50μfd, 12V
C_5 —— .02μfd
TR_1 —— GE. 2N192 OR 2N265
TR_2, TR_3 —— G.E. 2N241A
* T_1 —— 6KΩ/5KΩCT
* T_2 —— 500Ω CT/ V.C.

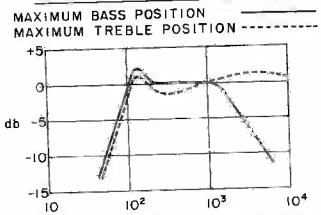
MAXIMUM POWER OUTPUT : .35 WATTS
MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION : .25 WATTS
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT : .2 VOLTS
FOR USE WITH MAGNETIC CARTRIDGE OMIT R1, IN THIS CONDITION SENSITIVITY : 5 MILLIVOLTS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

THREE TRANSISTOR PHONO AMPLIFIER
FIGURE 41



FREQUENCY RESPONSE
OF FOUR TRANSISTOR AMPLIFIER



AMPLIFIER LOADED WITH 3.2 Ω VOICE COIL SPEAKER RESONANCE @ 130 CPS

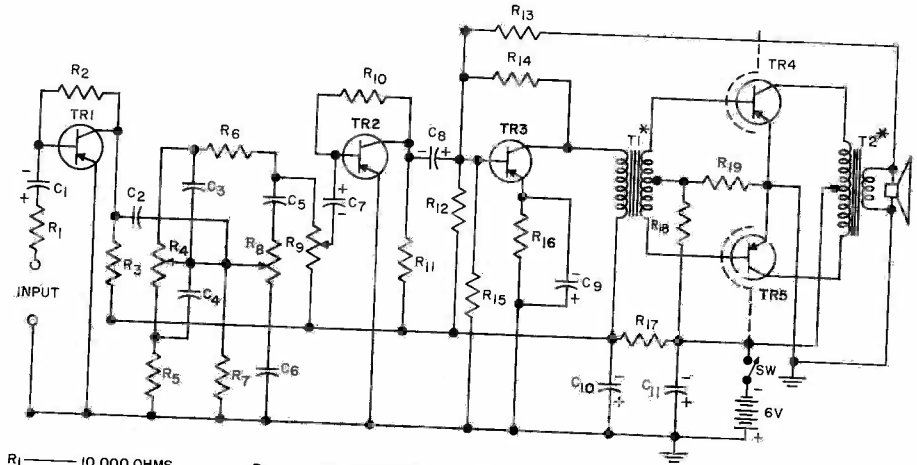
R1,—5000 OHM VOLUME CONTROL 1/2 W AUDIO TAPER
R2,——150,000 OHM
R3,——470,000 OHM
R4,——10,000 OHM
R6, R9,—4700 OHM
R7,——1000 OHM
R8,——33,000 OHM
R11,——25,000 OHM LINEAR
R12,——220 OHM
R5, R10,—470 OHM
R13,——47 OHM
R14, R15,——8.2 OHM
C1, C3, C7, C8,—50μfd
C2, C6,——50μfd
C4,——15μfd
C5,——.02μfd
TR1, TR2,—G.E. 2N191 OR 2N323
TR3, TR4,—G.E. 2N188A OR 2N320
*T1,——4K/2.6K CT.
*T2,——200Ω C.T./VC.

MAXIMUM POWER OUTPUT : .75 WATTS
MAXIMUM POWER OUT AT 10% HARMONIC DISTORTION : .45 WATTS
DISTORTION AT 100 MILLIWATTS
AT 100 C/S : 5%
AT 1000 C/S : 2%
AT 5000 C/S : 5%
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT : CRYSTAL CARTRIDGE : 150 M.V.
MAGNETIC PICK UP : 2 M.V.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

FOUR TRANSISTOR PHONO AMPLIFIER

FIGURE 42



R_1	10,000 OHMS	R_{11}	2200 OHMS	C_1	8 mfd
R_2	150,000 OHMS	R_{12}	4700 OHMS	C_2	.50
R_3	6800 OHMS	R_{13}	33,000 OHMS	C_3	.02
R_4	50,000 OHMS BASS LINEAR	R_{14}	47,000 OHMS	C_4	.20
R_5	1000 OHMS	R_{15}	1500 OHMS	C_5	.005
R_6	10,000 OHMS	R_{16}	330 OHMS	C_6	.10
R_7	100,000 OHMS	R_{17}	220 OHMS	C_7	10 mfd
R_8	50,000 OHMS TREBLE LINEAR	R_{18}	1200 OHMS	C_8	10 mfd
R_9	10,000 OHMS TAPER AUDIO V.C.	R_{19}	33 OHMS	C_9	50 mfd
R_{10}	220,000 OHMS			C_{10}	50 mfd
TR_1, TR_2, TR_3	GE 2N323			C_{11}	50 mfd
TR_4, TR_5	GE 2N321 (WITH CLIP-ON HEATSINK)			*T_1	1K/1K C.T.
				*T_2	100 Ω C.T./V.C.

PERFORMANCE DATA:

MAXIMUM POWER OUTPUT	1.00 WATTS
MAXIMUM POWER OUTPUT @ 10% DISTORTION	.75 WATTS
DISTORTION AT 100 MILLIWATTS:	
60 c/s	3.0 %
1000 c/s	1.5 %
5000 c/s	3.0 %
SENSITIVITY FOR 50 MILLIWATTS REFERENCE POWER OUTPUT (CRYSTAL CARTRIDGE)	3.8 mv

* FOR FURTHER INFORMATION SEE PAGE 167

FIVE TRANSISTOR AUDIO AMPLIFIER

FIGURE 43

"HI-FI" CIRCUITS

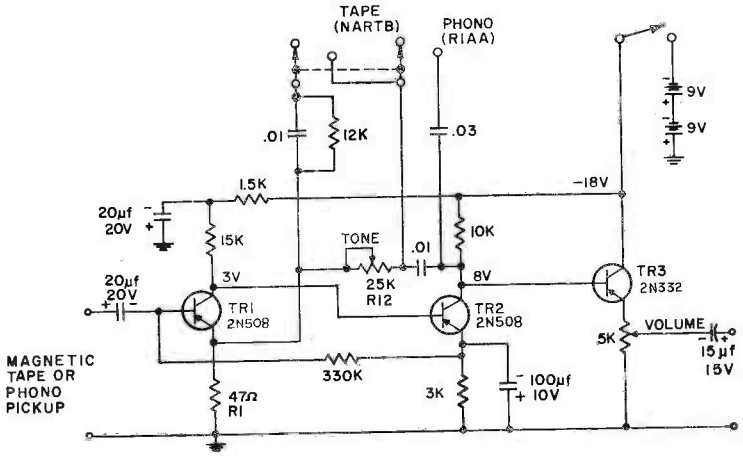
Transistors are ideally suited for Hi-Fi amplifiers since there is no problem with microphonics or hum pick-up from filaments as there is with tubes. Transistors are inherently low impedance devices and thus offer better matching to magnetic pick-ups and loudspeakers for more efficient power transfer.

Transistor circuits with negative feedback can give the wide frequency response and low distortion needed in hi-fi equipment.

PREAMPLIFIERS

Preamplifiers have two major functions (1) increasing the signal level from a pick-up device to 1 or 2 volts rms, and (2) providing compensation if required to equalize the input signal for a constant output with frequency.

The circuit of Figure 44 meets these requirements when the pick-up device is a variable reluctance phono cartridge such as the General Electric VRII, or a tape head.



PHONO-TAPE PREAMPLIFIER

FIGURE 44

This preamp will accommodate most magnetic pick-up impedances. The input impedance to the preamp increases with frequency because of the frequency selective negative feedback to the emitter of TR1. The impedance of the magnetic pick-ups will also increase with frequency but are below that of the preamp.

The first two stages of this circuit have a feedback bias arrangement for current stabilization of both stages. The 330K from the emitter of TR2 provides this DC current feedback to the base of TR1. The output stage is well stabilized with a 5K emitter resistance.

The AC negative feedback from the collector of TR2 to the emitter of TR1 is frequency selective to compensate for the standard NARTB recording characteristic for tape or the standard RIAA for phonograph records. The flat response from a standard NARTB pre-recorded tape occurs with the tone control (R12) at mid-position or 12K ohms. (See Figure 45.) There is 7 to 8 db of treble boost with the control at 25K maximum position, and approximately 20 db of treble cut with R12=0. Mid-position of the tone control also gives flat response from a standard RIAA recording.

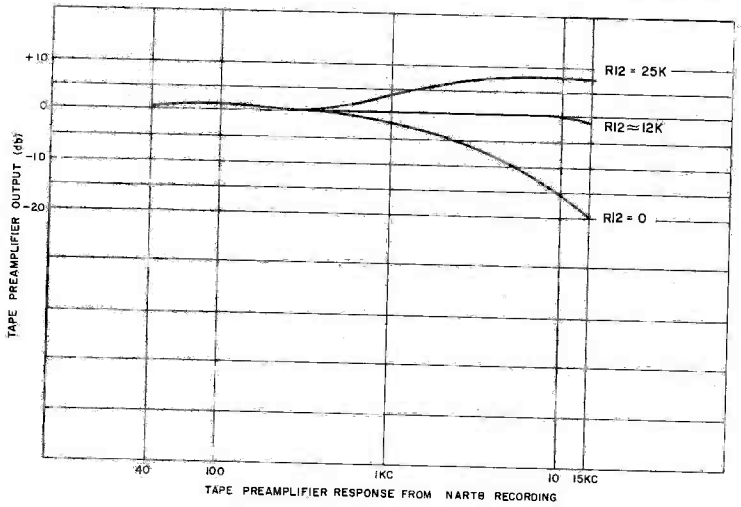


FIGURE 45

The voltage feedback from the collector of TR2 decreases at low frequencies because of the increasing reactance of the feedback capacitor in series with the tone control. Each of the two feedback networks give the desired increase in gain at the lower frequencies to accomplish the correct compensation. If this feedback capacitor were shunted by an electrolytic capacitor, the preamplifier would give constant gain at all frequencies (in the "Tape" switch position). This gain is determined by R12/R1.

The RIAA feedback network (with tone control at mid-position) has a net feedback resistance of 6K to decrease the gain because of the higher level input. This resistance has a .01 μf capacitor in parallel for decreasing the amplifier gain at the higher frequencies in accordance with RIAA requirements. This eliminates the need to load a reluctance pick-up with the proper resistance for high frequency compensation. If it is desirable to build the preamplifier for phonograph use only, the compensating feedback network would consist only of a .04 μf feedback capacitor in series with a 6K resistor (or a 10K Tone control) which has a .01 μf capacitor in parallel.

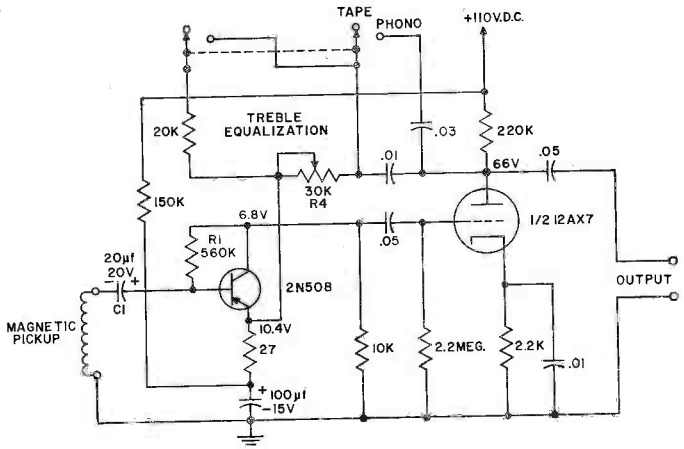
The emitter-follower output stage of the preamp gives a low impedance output for a cable run to a power amplifier, and acts as a buffer so that any preamp loading will not affect the equalization characteristic.

The Tone control should have a linear taper and the Volume control an audio taper. Two 9 volt batteries will give good life in this application since the total supply drain is approximately 3.5 ma DC. This 18 volts may also be obtained by suitable decoupling from a higher voltage supply that is available.

HYBRID PREAMPLIFIER

The hybrid preamplifier circuit of Figure 46 uses a similar feedback equalization technique to that of Figure 44. There is a small amount of treble boost above 10 KC due to the .01 μf capacitor from the 12AX7 cathode to ground. The Treble Control is set at the same position (R4 = 20K) for a compensated output from a standard RIAA recording or an NARTB recorded tape.

The 2N508 transistor is biased at approximately .7 ma from a constant current source for good current stability with temperature and transistor interchangeability. R1 biases the base for the desired V_{CE}, and since this bias is taken from the collector, the



HYBRID PHONO-TAPE PREAMPLIFIER
FIGURE 46

d-c feedback helps to keep V_{CE} in the range of 1 to 5 volts. This voltage varies with leakage current of C1 and with h_{FE} for different transistors. This range of V_{CE} bias has little effect on the operation of the preamplifier.

The standard reference level for S/N (signal-to-noise) measurements in tape recording is the maximum level at which a 400 cycle signal can be recorded at 2% harmonic distortion. The hybrid preamplifier of Figure 46 is capable of a S/N in excess of 60 db. The signal output from this reference level is approximately 1.5 volts. The variation of treble equalization for tape is shown in Figure 47.

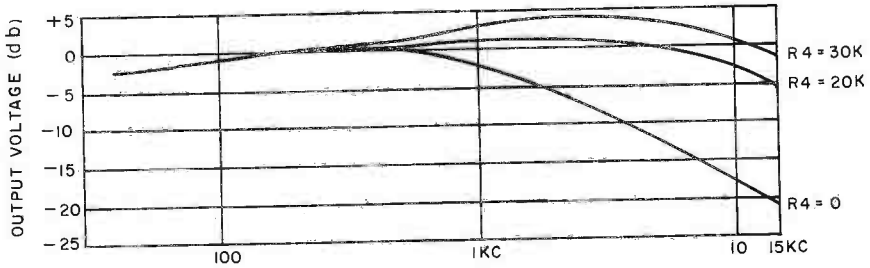


FIGURE 47

A dual preamp for a stereophonic disc or tape system could be built with two identical preamps as in Figure 46, using only one tube (12AX7) and two transistors (2N508).

TONE CONTROLS

Tone control circuits for transistor amplifiers are somewhat different than conventional vacuum tube tone controls since the impedance levels in transistor circuits are lower. A satisfactory bass and treble tone control for use between transistor stages is shown by Figure 48. *

* "Transistor Electronics," Lo, Endres et al (Prentice-Hall).

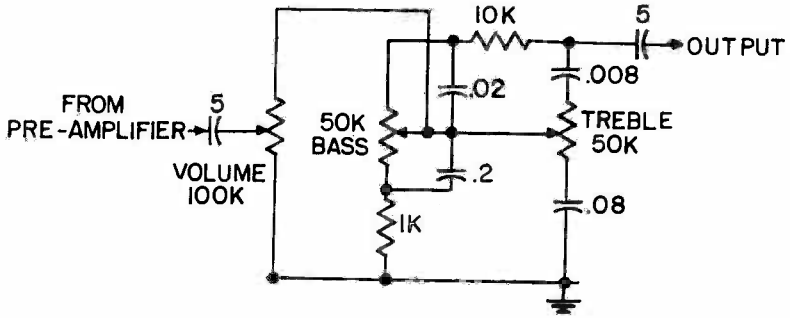
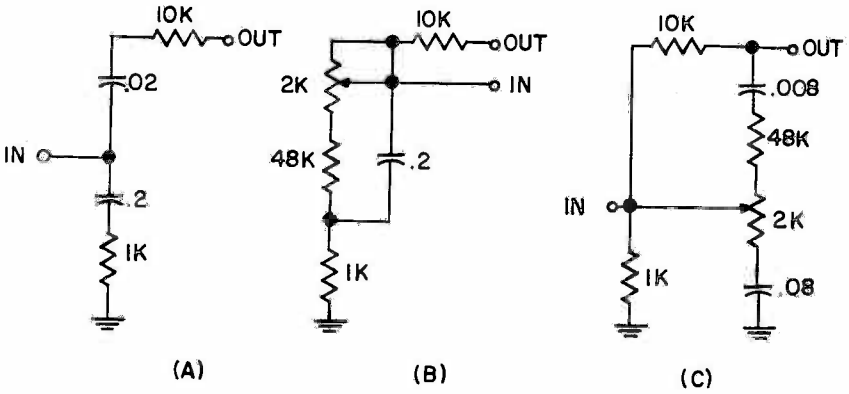


FIGURE 48

The action of the tone controls is easily understood if they are considered as current transfer networks rather than voltage transfer networks as in vacuum tube amplifiers. The output current from the preceding stage goes to the volume control where part of it is shunted to ground and the rest goes to the junction of the 0.02 μfd and 0.2 μfd capacitors and the center arms of the potentiometers. At 1000 cycles, the equivalent circuit of the tone controls is very simple, as shown in Figure 49(A). At this frequency, the current is divided so that 10/11ths of the current is shunted to ground and 1/11th goes on to the next transistor. The low-frequency equivalent circuit for the "bass boost" condition is shown in Figure 49(B). With the movable arm of the potentiometer near the top, the 0.02 μfd capacitor is bypassed and more of the current is shunted into the 10,000 ohm resistor as the impedance of the 0.2 μfd capacitor rises at low frequencies.

The high-frequency equivalent circuit of the tone control is shown in Figure 49(C) for the "treble cut" condition. Depending on the potentiometer setting, most of the higher frequencies will be shunted to ground as compared to a 1000 cycle signal. With the potentiometer arm at the top, the higher frequency current would bypass the 10,000 ohm resistor and a treble boost would be achieved.

The performance of the tone control is shown by Figure 50.



(A) A 1 KC EQUIVALENT CIRCUIT. (B) LOW-FREQUENCY EQUIVALENT CIRCUIT, AND (C) THE EQUIVALENT CIRCUIT AT HIGH FREQUENCIES.

FIGURE 49

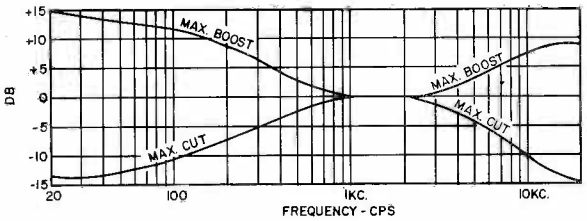
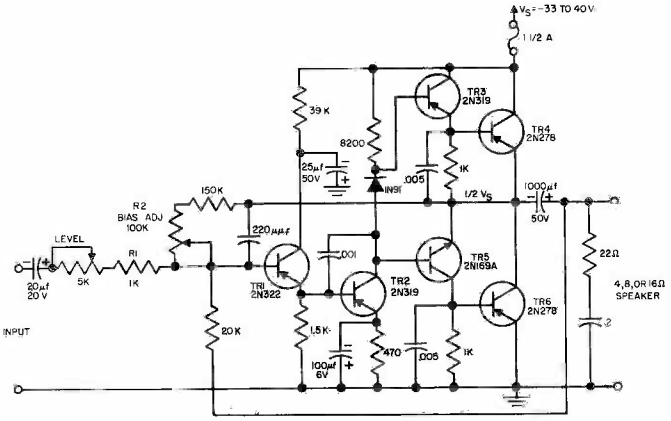


FIGURE 50

POWER AMPLIFIERS

A great deal of effort has gone into developing transformerless push-pull amplifiers using vacuum tubes. Practical circuits, however, use many power tubes in parallel to provide the high currents necessary for direct driving of low impedance loudspeakers.

The advent of power transistors has given new impetus to the development of transformerless circuits since the transistors are basically low voltage, high current devices. The emitter follower stage, in particular, offers the most interesting possibilities since it has low inherent distortion and low output impedance.



SIX WATT POWER AMPLIFIER
FIGURE 51

Figure 51 is a direct coupled power amplifier with excellent low frequency response, and also has the advantage of a feedback arrangement for current stabilization of all stages. The feedback system also stabilizes the voltage division across the power output transistors TR4 and TR6 which operate in a Class B push-pull arrangement. TR3 and TR5 also operate Class B in the Darlington connection to increase the current gain. Using an NPN for TR5 gives the required phase inversion for driving TR6 and also has the advantage of push-pull emitter follower operation. TR4 and TR6 have a small forward bias to minimize crossover distortion. This bias is set by the voltage drop across the 1K resistors that shunt the input to TR4 and TR6. TR3 and TR5 are biased for the same reason with the voltage drop across the 1N91. A 68 ohm resistor would serve the same function as the 1N91 except there would be no temperature compensation. Thermistors have also been used to compensate for the temperature variation of the emitter-base resistance, but they do not track this variation as well as a germanium junction diode which has temperature characteristics similar to the transistor.

TR2 is a Class A driver requiring a very low impedance drive which is accomplished by an emitter follower TR1. TR1 needs a current source for low distortion thus R1 and the Level Control supply the desired drive impedance. The Level Control should be set for a value of approximately 1K ohms when this amplifier is driven by the preamplifier of Figure 44. This will permit the amplifier to be driven to full output. TR1 has an emitter current of .8 to 1 ma, and TR2 has a 2.5 to 3 ma bias.

The bias adjuster R2 is set for one-half the supply voltage across TR6. TR4 and TR6 have a beta cut-off at approximately 7Kc. The phase shift and drop in beta gives rise to a decline in transistor efficiency which causes an elevation of junction temperature. To help stabilize this runaway condition, the higher frequency drive has been decreased by the .005 μf capacitors in parallel with the 1K ohm drive resistors. This reduces the drive by 3 db at 30 Kc. The .001 μf feedback from collector to base of TR2 also aids in this stabilization by reducing the high frequency gain of this stage. The 220 $\mu\mu$f capacitor shunting the bias network further aids the stabilization of the amplifier with high frequency negative feedback from output to input. This circuit has approximately 17 db of overall voltage feedback with the 20K resistor from load to input. The output to speaker is shunted by 22 ohms in series with .2 μf to prevent the continued rise of speaker impedance and its accompanying phase shift beyond the audio spectrum.

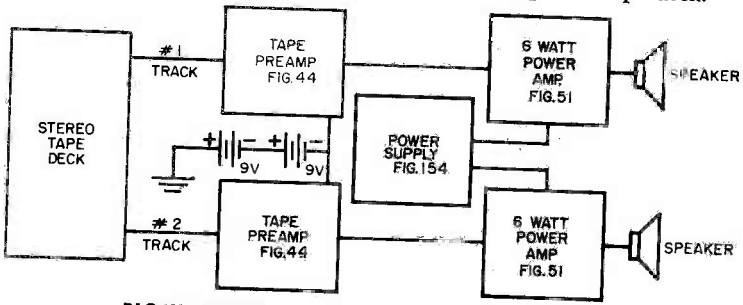
The overall result, from using direct coupling, no transformers, and ample degeneration, is an amplifier with output impedance less than one ohm for good speaker damping, and very low total harmonic distortion. The frequency response at 100 milliwatts is flat over the audio spectrum. When checking for maximum power out at the higher frequencies, a sinewave can be applied only for a short duration before sufficient heating for runaway results as indicated above. To protect the power transistors, a current meter should be used in series with the voltage supply for quick, visual indication of runaway while checking power output above approximately 2Kc. There is not sufficient sustained high frequency power in regular program material to precipitate this instability. Thus the actual performance of the amplifier does not suffer since the power level in music and speech declines as the frequency increases beyond about 1Kc.

This amplifier is capable of a 5 watt output with less than 1% harmonic distortion into a 4, 8 or 16 ohm speaker when used with the power supply of Figure 153, page 108.

The power transistors TR4 and TR6 should be mounted on an adequate heat radiator such as used for transistor output in an automobile radio, or mounted on a 3" x 4" x ⅛" aluminum plate.

STEREOPHONIC TAPE SYSTEM

A complete semiconductor, stereophonic tape playback system may be assembled by using the following circuits in conjunction with a stereophonic tape deck.

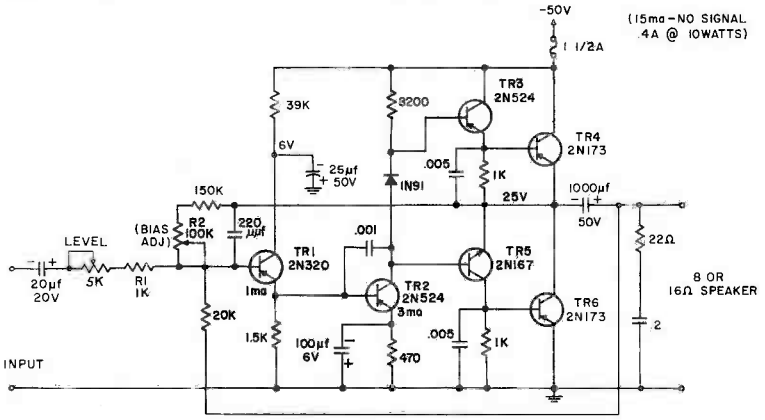


BLOCK DIAGRAM OF STEREOPHONIC TAPE SYSTEM
FIGURE 52

Two identical tape preamplifier circuits can use a common 18 volt battery supply. The circuitry of Figure 44 may be used with the switch and RIAA network eliminated if the preamps are to be used for tape only.

The output of each preamp is fed to a power amplifier as indicated in Figure 52. Two identical power amplifiers with circuitry as in Figure 51 can use a common power supply as shown in Figure 154, page 108. The output coupling capacitor of the preamps may be eliminated when fed to an amplifier with an input coupling capacitor as in Figure 51. The output of each amplifier fed to its respective speaker completes the stereo system as shown in Figure 52.

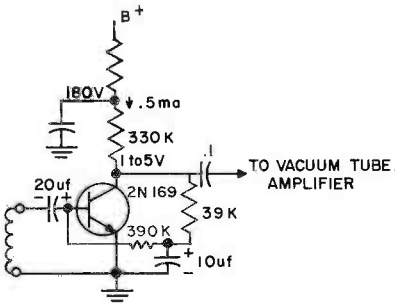
A dual 10 watt stereo system consists of two identical amplifiers with circuitry of Figure 53 using the common power supply of Figure 155, page 109. This power supply has separate decoupled outputs for each amplifier. The 1N1115 rectifiers should be mounted on a metal chassis with the electrically insulating mounting kit provided with each unit. The stereo system uses the same tape preamplifiers as that of Figure 52.



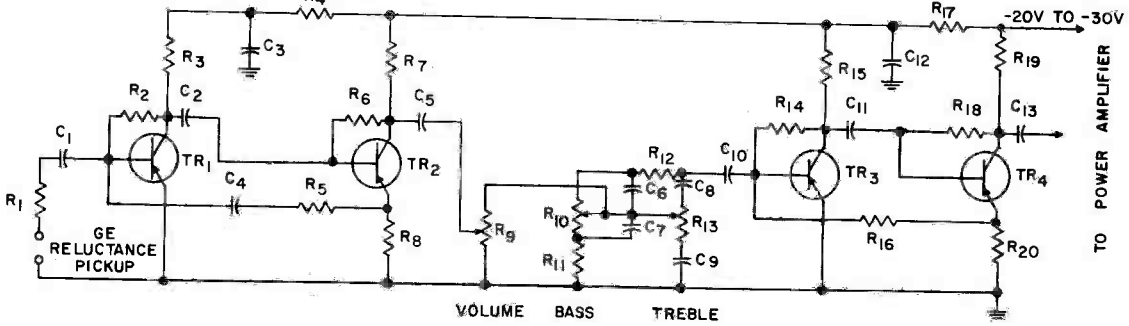
TEN WATT POWER AMPLIFIER
FIGURE 53

The power amplifier of Figure 53 is the same circuit as Figure 51 except for the transistors which have a higher voltage rating. This amplifier with the power supply of Figure 155, page 109, is capable of a 10 watt output with very low distortion into an 8 or 16 ohm speaker.

HI-FI CIRCUIT DIAGRAMS



NPN PREAMPLIFIER FOR MAGNETIC PICKUPS
FIGURE 54



R_1 —— 2700 OHM

R_2, R_6, R_{14}, R_{18} — 180,000 OHM (SEE NOTE)

R_3, R_{15} —— 15,000 OHM

R_4 —— 2200 OHM

R_5 —— 22,000 OHM

R_7 —— 8200 OHM

R_8 —— 220 OHM

R_9 —— VOLUME CONTROL
100,000 OHM 1/2 W AUDIO TAPER

R_{10}, R_{13} —— 50,000 OHM, LINEAR TAPER POT

R_{11} —— 1000 OHM

R_{12}, R_{19} —— 10,000 OHM

R_{16} —— 6800 OHM

R_{17} —— 1800 OHM

R_{20} —— 100 OHM

C_1, C_2, C_5, C_{10}, C_{11}, C_{13} — 5 μfd

C_3, C_{12} —— 50 μfd

C_4 —— .015 μfd

C_6 —— .02 μfd

C_7 —— .2 μfd

C_8 —— .01 μfd

C_9 —— .1 μfd

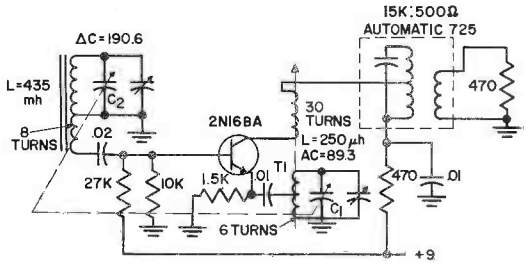
TR_1, TR_2, TR_3, TR_4 —— GE 2N190

NOTE:
HIGHER OR LOWER VALUES MAY BE NECESSARY DEPENDING ON TRANSISTORS AND SUPPLY VOLTAGE. SELECT RESISTORS SO THAT COLLECTOR TO EMITTER D-C VOLTAGE IS 4 TO 8 VOLTS.

PREAMPLIFIER AND DRIVER
FIGURE 55

AUTODYNE CONVERTER CIRCUITS

The converter stage of a transistor radio is a combination of a local oscillator, a mixer and an IF amplifier. A typical circuit for this stage is shown in Figure 56.



FOR ADDITIONAL INFORMATION SEE PAGE 167

AUTODYNE CONVERTER
FIGURE 56

Redrawing the circuit to illustrate the oscillator and mixer sections separately, we obtain Figures 57A and 57B.

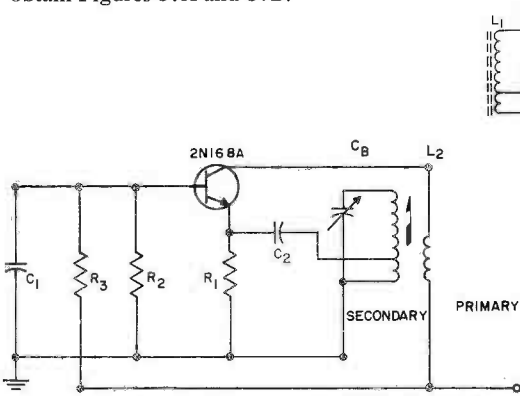


FIGURE 57A

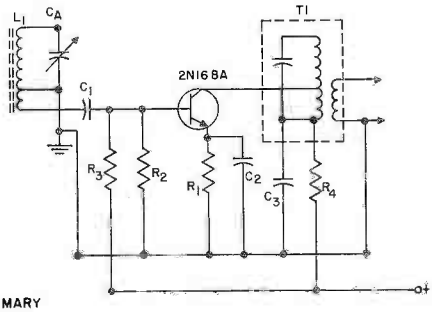


FIGURE 57B

The operation of the oscillator section (57A) is as follows:

Random noise produces a slight variation in base current which is subsequently amplified to a larger variation of collector current. This A.C. signal in the primary of L_2 induces an A.C. current into the secondary of L_2 tuned by C_B to the desired oscillator frequency. C_2 then couples the resonant frequency signal back into the emitter circuit. If the feedback (tickler) winding of L_2 is properly phased the feedback will be positive (regenerative) and of proper magnitude to cause sustained oscillations. The secondary of L_2 is an auto-transformer to achieve proper impedance match between the high impedance tank circuit of L_2 and the relatively low impedance of the emitter circuit.

C_1 effectively bypasses the biasing resistors R_2 and R_3 to ground, thus the base is A.C. grounded. In other words, the oscillator section operates essentially in the grounded base configuration.

The operation of the mixer section (57B) is as follows:

The ferrite rod antenna L_1 exposed to the radiation field of the entire frequency spectrum is tuned by C_A to the desired frequency (broadcast station).

The transistor is being biased in a relatively low current region, thus exhibiting quite non-linear characteristics. This enables the incoming signal to mix with the oscillator signal present, creating signals of the following four frequencies:

1. *The local oscillator signal.*
2. *The received incoming signal.*
3. *The sum of the above two.*
4. *The difference between the above two.*

The IF load impedance T_1 is tuned here to the difference between the oscillator and incoming signal frequencies. This frequency is called the intermediate frequency (I.F.) and is conventially 455 KC/S. This frequency will be maintained fixed since C_A and C_B are mechanically geared (ganged) together. R_4 and C_3 make up a filter to prevent undesirable currents to flow through the collector circuit. C_2 essentially bypasses the biasing and stabilizing resistor R_1 to ground. Since the emitter is grounded and the incoming signal injected into the base, the mixer section operates in the "grounded emitter" configuration.

IF AMPLIFIERS

A typical circuit for a transistor IF amplifier is shown by Figure 58.

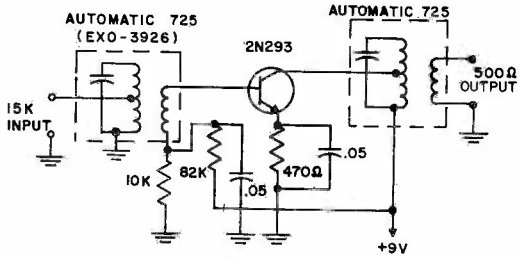


FIGURE 58

The collector current is determined by a voltage divider on the base and a large resistance in the emitter. The input and output are coupled by means of tuned IF transformers. The .05 capacitors are used to prevent degeneration by the resistance in the emitter. The collector of the transistor is connected to a tap on the output transformer to provide proper matching for the transistor and also to make the performance of the stage relatively independent of variations between transistors of the same type. With a rate-grown NPN transistor such as the 2N293, it is unnecessary to use neutralization to obtain a stable IF amplifier. With PNP alloy transistors, it is necessary to use neutralization to obtain a stable amplifier and the neutralization capacitor depends on the collector capacitance of the transistor. The gain of a transistor IF amplifier will decrease if the emitter current is decreased. This property of the transistor can be used to control the gain of the IF amplifier so that weak stations and strong stations will produce the same audio output from a radio. Typical circuits for changing the gain of an IF amplifier in accordance with the strength of the received signal are explained in the A.V.C. section of this chapter.

AUTOMATIC VOLUME CONTROLS

A.V.C. is a system which automatically varies the total amplification of the signal in a radio receiver with changing strength of the received signal carrier wave.

From the definition given, it would be correctly inferred that a more exact term to describe the system would be automatic gain control (A.G.C.).

Since broadcast stations are at different distances from a receiver and there is a great deal of variation in transmitted power from station-to-station, the field strength around a receiver can vary by several orders of magnitude. Thus, without some sort of automatic control circuit, the output power of the receiver would vary considerably when tuning through the frequency band. It is the purpose of the A.V.C. or A.G.C. circuit to maintain the output power of the receiver constant for large variations of signal strengths.

Another important purpose of this circuit is its so-called "anti-fading" properties. The received signal strength from a distant station depends on the phase and amplitude relationship of the ground wave and the sky wave. With atmospheric changes this relationship can change, yielding a net variation in signal strength. Since these changes may be of periodic and/or temporary nature, the A.V.C. system will maintain the average output power constant without constantly adjusting the volume control.

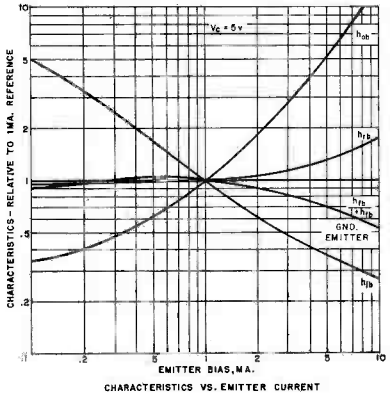
The A.V.C. system consists of taking, at the detector, a voltage proportional to the incoming carrier amplitude and applying it as a negative bias to the controlled amplifier thereby reducing its gain.

In tube circuits the control voltage is a negative going DC grid voltage creating a loss in transconductance (Gm).

In transistor circuits various types of A.V.C. schemes can be used:

EMITTER CURRENT CONTROL

As the emitter current of a transistor is reduced (from 1.0 ma to ,1 ma for instance) various parameters change considerably (see Figure 59).



CHARACTERISTICS VS. EMITTER CURRENT

FIGURE 59

The effect of these changes will be twofold:

1. *A change in maximum available gain and*
2. *A change in impedance matching since it can be seen that both h_{ob} and h_{ib} vary radically.*

Therefore, a considerable change in power gain can be obtained as shown by Figure 60.

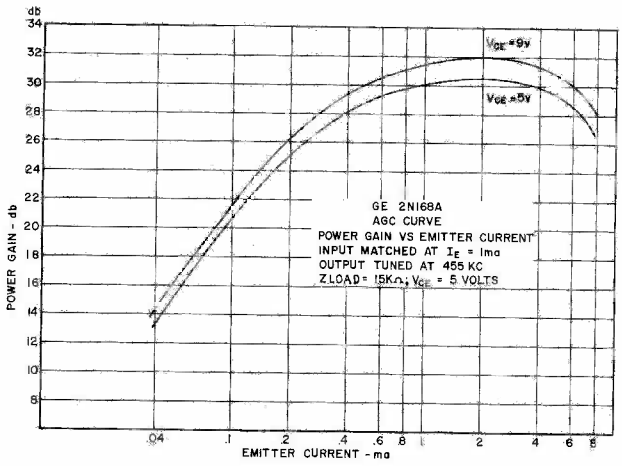


FIGURE 60

On the other hand, as a result of I_{CO} (collector leakage current) some current always flows, thus a transistor can be controlled only up to a point and cannot be "cut-off" completely. This system yields generally fair control and is, therefore, used more than others. For performance data see Figure 61.

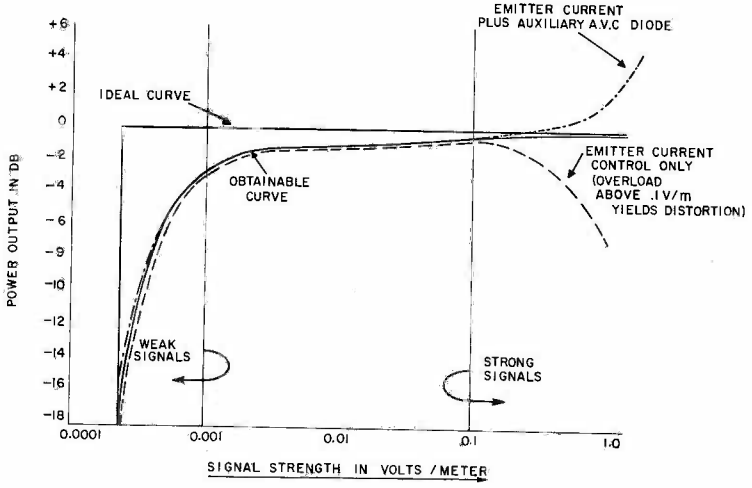


FIGURE 61

AUXILIARY A.V.C. SYSTEMS

Since most A.V.C. systems are somewhat limited in performance, to obtain improved control, auxiliary diode A.V.C. is sometimes used. The technique used is to shunt some of the signal to ground when operating at high signal levels, as shown by Figure 62.

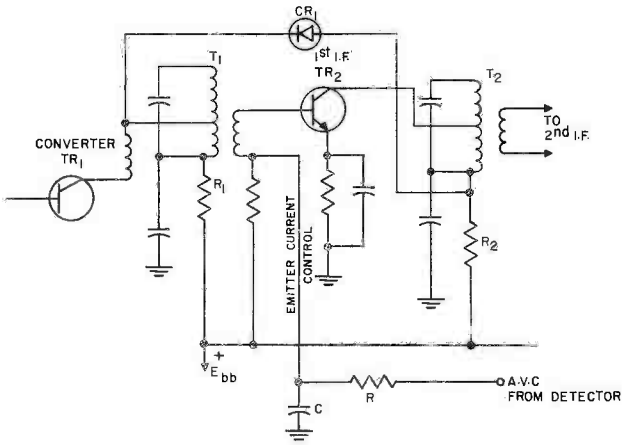


FIGURE 62

In the circuit of Figure 62 diode CR_1 is back-biased by the voltage drops across R_1 and R_2 and represents a high impedance across T_1 at low signal levels. As the signal strength increases, the conventional emitter current control A.V.C. system creates a bias change reducing the emitter current of the controlled stage. This current reduction coupled with the ensuing impedance mismatch creates a power gain loss in the stage. As the current is further reduced, the voltage drop across R_2 becomes smaller thus changing the bias across CR_1. At a predetermined level CR_1 becomes forward biased, constituting a low impedance shunt across T_1 and creating a great deal of additional A.V.C. action. This system will generally handle high signal strengths as can be seen from Figure 61. Hence, almost all radio circuit diagrams in the circuit section of this manual use this system in addition to the conventional emitter current control.

"TETRODE" OR BASE #2 CONTROL

In tetrode transistor amplifiers the high frequency gain of the transistor depends on the base-to-base bias voltage, varying the latter will give good gain control. For circuit see Figure 63.

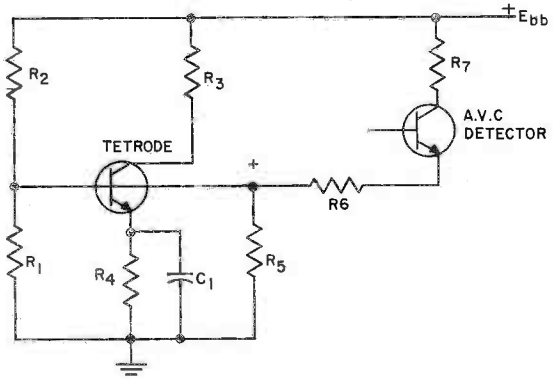


FIGURE 63

REFLEX CIRCUITS

"A reflex amplifier is one which is used to amplify at two frequencies – usually intermediate and audio frequencies."*

The system consists of using an I.F. amplifier stage and after detection to return the audio portion to the same stage where it is then amplified again. Since in Figure 64,

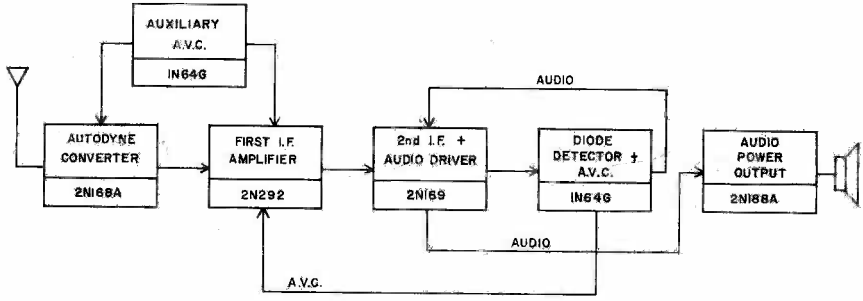


FIGURE 64

two signals of widely different frequencies are amplified, this does not constitute a *"regenerative effect"* and the input and output loads of these stages can be split audio – I.F. loads. In Figure 65, the I.F. signal (455 Kc/s) is fed through T2 to the detector circuit CR1, C3 and R5. The detected audio appears across the volume control R5 and is returned through C4 to the cold side of the secondary of T1.

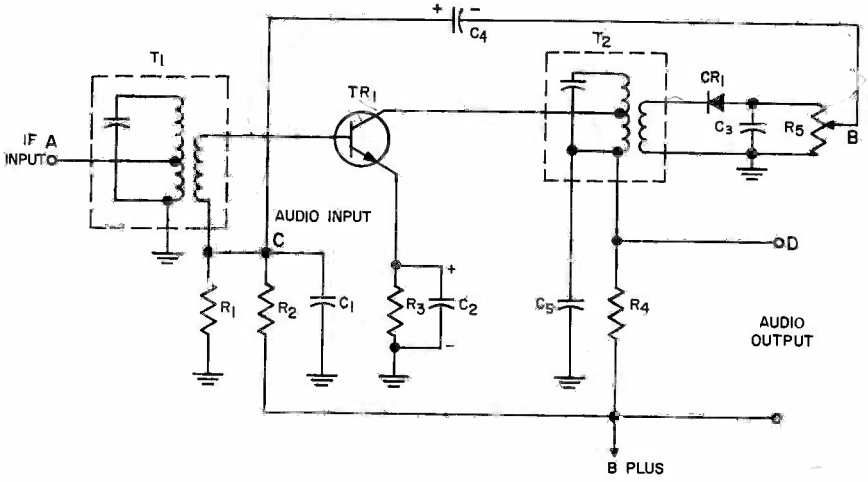


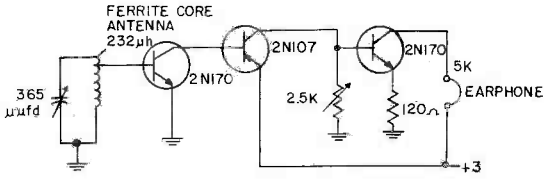
FIGURE 65

* F. Langford-Smith, Radiotron Designers Handbook, Australia, 1953, p. 1140

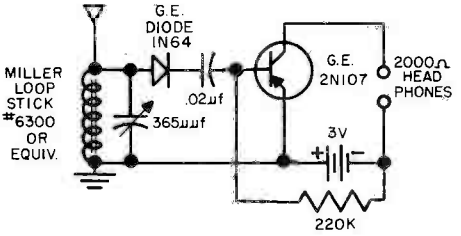
Since the secondary only consists of a few turns of wire, it is essentially a short circuit at audio frequencies. C1 bypasses the I.F. signal otherwise appearing across the parallel combination of R1 and R2. The emitter resistor R3 is bypassed for both audio and I.F. by the electrolytic condenser C2. After amplification, the audio signal appears across R4 from where it is then fed to the audio output stage. C5 bypasses R4 for I.F. frequencies and the primary of T2 is essentially a short circuit for the audio signal.

The advantage of "reflex" circuits is that one stage produces gain otherwise requiring two stages with the resulting savings in cost, space, and battery drain. The disadvantages of such circuits are that the design is considerably more difficult, although once a satisfactory receiver has been designed, no outstanding production difficulties should be encountered. Other disadvantages are a somewhat higher amount of playthrough (i.e. signal output with volume control at zero setting), and a minimum volume effect. The latter is the occurrence of minimum volume at a volume control setting slightly higher than zero. At this point, the signal is distorted due to the balancing out of the fundamentals from the normal signal and the out-of-phase playthrough component. Schematics of complete radios are on pages 44 through 55.

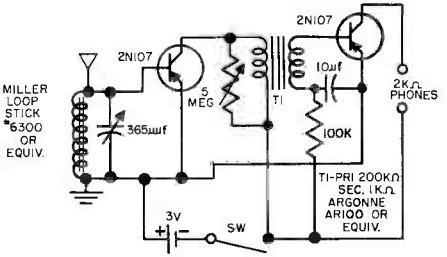
COMPLETE RADIO CIRCUIT DIAGRAMS



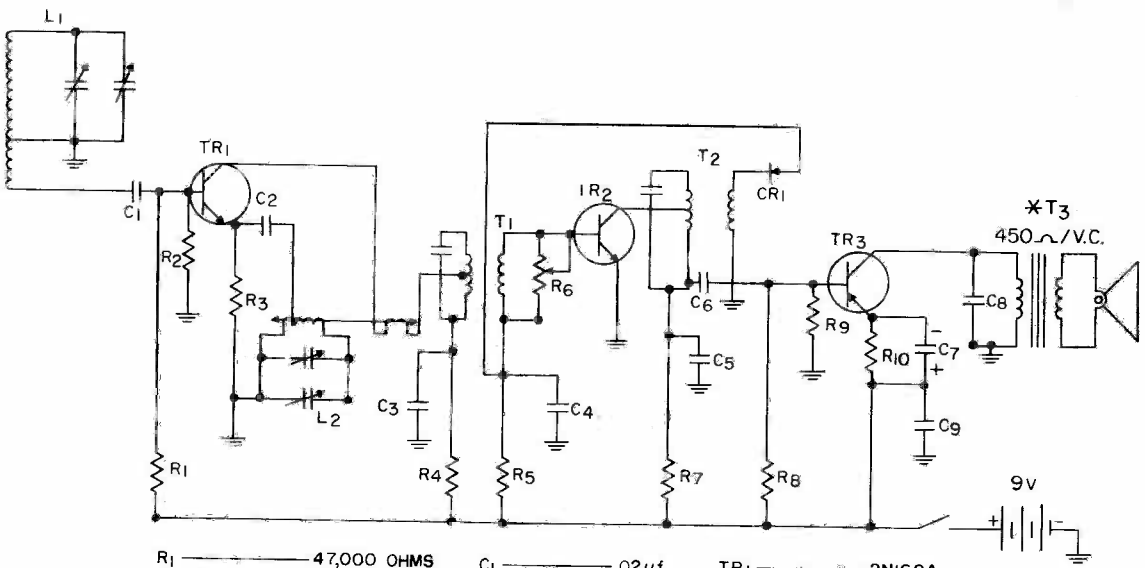
DIRECT COUPLED VEST POCKET RADIO
FIGURE 66



SIMPLE RADIO RECEIVER
FIGURE 67



TWO TRANSISTOR RADIO RECEIVER
FIGURE 68

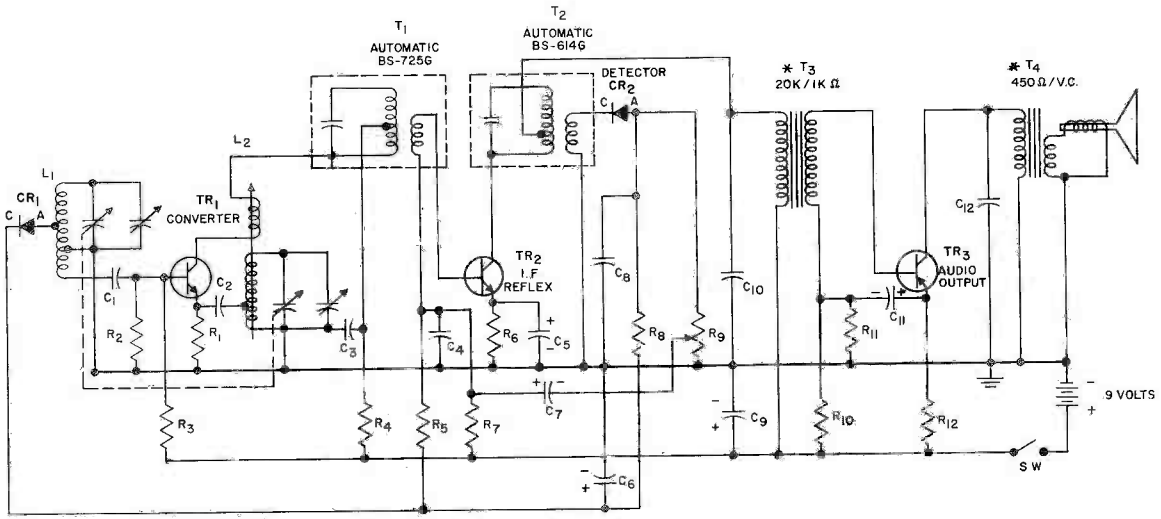


R_1	47,000 OHMS	C_1	.02μf	TR_1	2N168A
R_2	10,000 OHMS	C_2	.01 μf	TR_2	2N169 OR 2N168A CR_1 IN64G OR EQUIV.
R_3, R_7	1500 OHMS	C_3	.01 μf	TR_3	2N241A
R_4	270 OHMS	C_4	.01 μf	T_1	AUTOMATIC BS725G
R_5	33,000 OHMS	C_5	.002 μf	T_2	AUTOMATIC BS614G
R_6	2,000 OHMS VOLUME CONTROL	C_6	5μf	NOMINAL SENSITIVITY: 2.0 MILLIVOLTS/METER (MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)	
R_8	1000 OHMS	C_7	50μf	MAXIMUM POWER OUTPUT: 75 MILLIWATTS	
R_9	4700 OHMS	C_8	.05μF	SELECTIVITY AT -6db: 10 KC/S	
R_{10}	100 OHMS	C_9	50μfd-12V	SELECTIVITY AT -60db: 120 KC/S	
				TOTAL BATTERY DRAIN: 19 MILLIAMPS	

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

THREE TRANSISTOR REFLEX RECEIVER

FIGURE 69



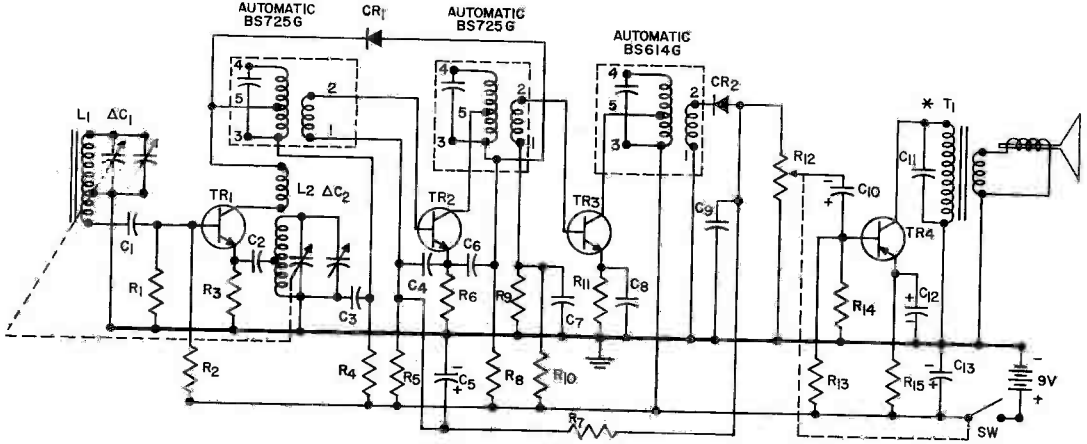
R_1	1500 OHM	C_1, C_4, C_8	.02 μfd	L_1	435 μh ± 10%
R_2, R_5, R_8	10,000 OHM	C_2, C_3	.01 μfd	L_2	250 μh ± 10%
R_3	47,000 OHM	C_5, C_{11}	50 μfd, 3V	CR_1, CR_2	IN64G OR EQUIV.
R_4	270 OHM	C_6	15 μfd, 12V	ΔC_1 — 190.6	R/C MODEL 242
R_6	330 OHM	C_7	6 μfd, 6V	ΔC_2 — 89.3	
R_7	330,000 OHM	C_9	50 μfd, 12V		
R_9	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER	C_{10}	.002 μfd,		
R_{10}	1000 OHM	C_{12}	0.1 μfd		
R_{11}	4700 OHM	TR_1	G.E. 2N168A CONVERTER		
R_{12}	100 OHM	TR_2	G.E. 2N168A OR 2N169 REFLEX		
		TR_3	G.E. 2N241A AUDIO		

NOMINAL SENSITIVITY: 600 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 10 KC/S
SELECTIVITY AT -60db : 120 KC/S
TOTAL BATTERY DRAIN : 17.5 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

THREE TRANSISTOR REFLEX RECEIVER

FIGURE 70



R_1, R_7, R_9 — 10,000 OHM
R_{12} — VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_2 — 27,000 OHM
R_3 — 1500 OHM
R_4, R_{11} — 470 OHM
R_5 — 39,000 OHM
R_6 — 330 OHM
R_8 — 1800 OHM
R_{10} — 68,000 OHM
R_{13} — 1000 OHM
R_{14} — 5600 OHM
R_{15} — 68 OHM
* T_1 — 500Ω/V.C.
* ΔC_1 — 190.6
* ΔC_2 — 89.3
} R/C MODEL 242

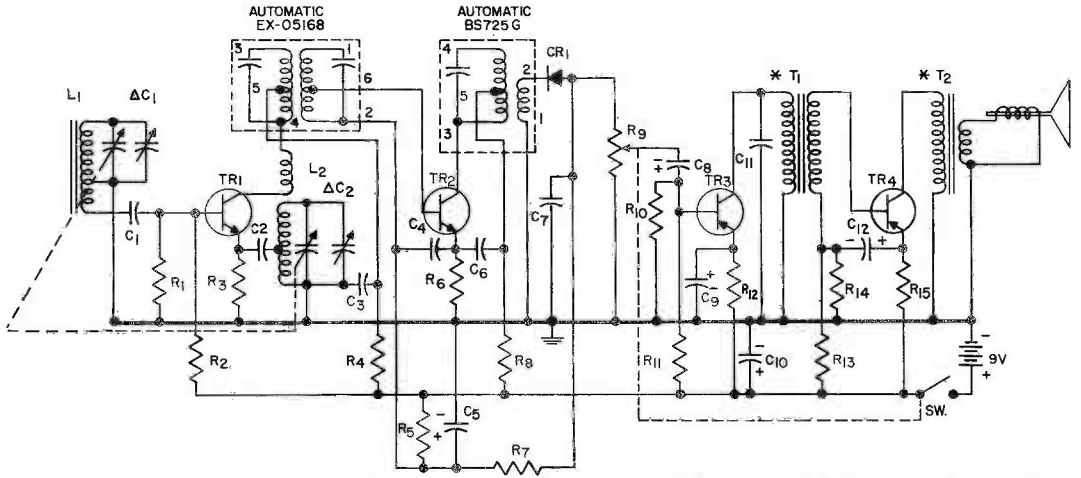
C_1 — .02μfd
C_2, C_3 — .01μfd
C_4, C_6, C_7, C_8, C_9 — .05μfd
C_5 — 15μfd, 12V
C_{10} — 6μfd, 12V
C_{11} — .1μfd
C_{12} — 100μfd, 12V
C_{13} — 50μfd, 12V
TR_1 — G.E. 2N168A CONVERTER
TR_2, TR_3 — G.E. 2N293 IST & 2ND I.F.
TR_4 — G.E. 2N241A OR 2N321 AUDIO
* L_1 — 435μh, ±10%
* L_2 — 250μh, ±10%
CR_1, CR_2 — DR117, IN64G, OR CK706A OR EQUIV.

NOMINAL SENSITIVITY : 500 MICROVOLTS / METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 75 MILLIWATTS
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 65.0 KC/S
TOTAL BATTERY DRAIN : 20.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

FOUR TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 71



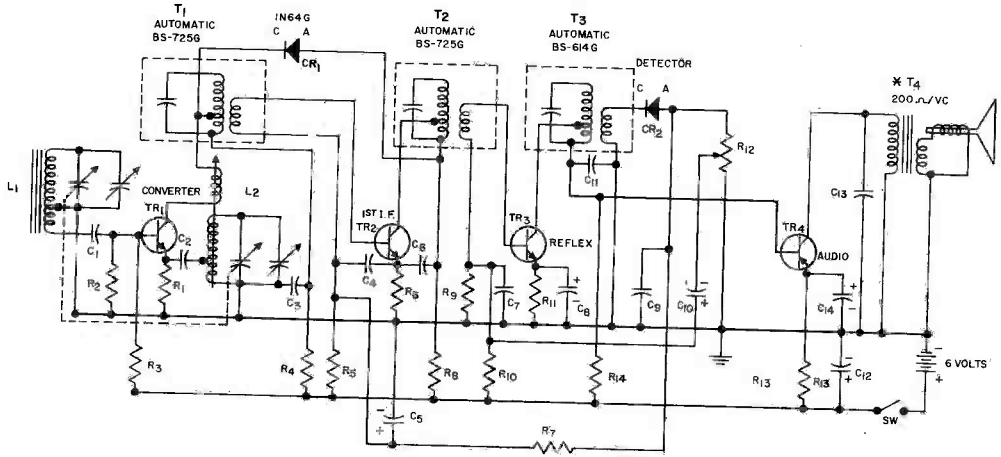
R_1,	6800 OHM	C_1, C_4, C_6,	.05μfd
R_2,	27,000 OHM	C_2, C_3,	.01μfd
R_3,	1500 OHM	C_5,	15μfd, 12V
R_4, R_8,	470 OHM	C_7, C_{11},	.02μfd,
R_5,	120,000 OHM	C_8,	6μfd, 12V
R_6,	330 OHM	C_9, C_{10}, C_{12},	50μfd, 12V
R_7,	12,000 OHM	CR_1,	DRII7, IN64G, OR CK706A OR EQUIV
R_{10},	47,000 OHM	TR_1	G.E. 2N168A CONVERTER
R_{11}	10,000 OHM	TR_2	G.E. 2N293 I.F.
R_{12}, R_{13},	1000 OHM	TR_3	G.E. 2N192 OR 2N324 DRIVER
R_{14},	5600 OHM	TR_4	G.E. 2N241A OR 2N321 AUDIO
R_{15},	68 OHM	* T_1	20KΩ/600Ω
R_9,	VOLUME CONTROL 10,000Ω 1/2W AUDIO TAPER	* T_2	500 Ω/V.C.
* L_1,	435 μh ±10%	* ΔC_1,	190.6 R/C MODEL 242
* L_2,	250 μh ±10%	* ΔC_2,	89.3 R/C MODEL 242

NOMINAL SENSITIVITY : 300 MICROVOLTS / METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 75 MILLIWATTS
SELECTIVITY AT -6 db : 8.0 KC/S
SELECTIVITY AT -60db : 65.0 KC/S
TOTAL BATTERY DRAIN : 18.0 MILLIAMPS

*FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

FOUR TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 72



R_1	1500 OHM
R_2, R_9	10,000 OHM
R_3	15,000 OHM
R_4	270 OHM
R_5	56,000 OHM
R_6	330 OHM
R_7	3300 OHM
R_8	1800 OHM
R_{10}	68,000 OHM
R_{11}	470 OHM
R_{12}	VOLUME CONTROL 10,000 OHM ½ W AUDIO TAPER
R_{13}	39 OHM
R_{14}	1000 OHM

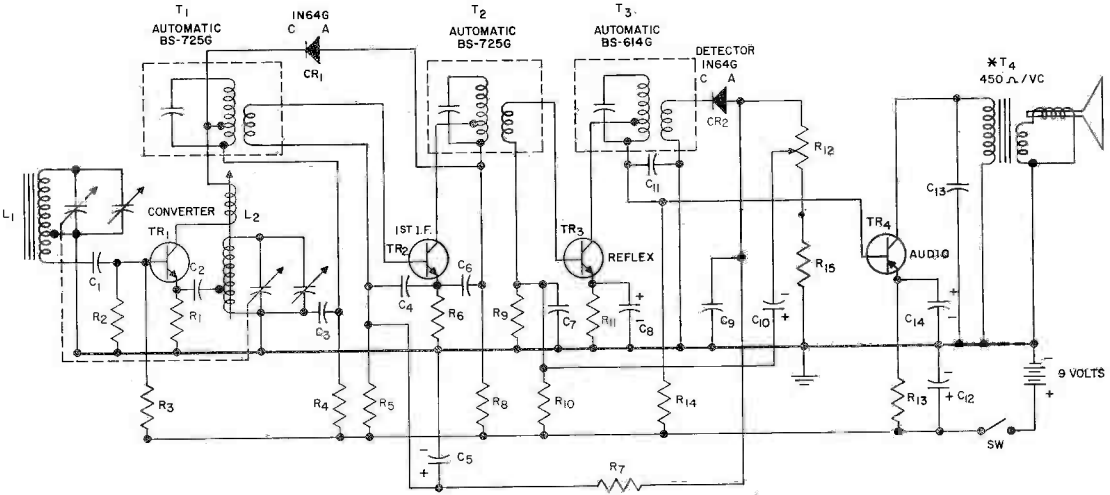
C_1, C_{11}	.02 μfd
C_2, C_3, C_7	.01 μfd
C_4, C_6, C_9	.05 μfd
C_5	15 μfd, 12 V
C_8	50 μfd, 3 V
C_{10}	6 μfd, 12 V
C_{12}	50 μfd, 12 V
C_{13}	0.1 μfd
C_{14}	100 μfd, 12 V
TR_1	2N168A CONVERTER
TR_2	2N292 1ST I.F.
TR_3	2N169 REFLEX
TR_4	2N241A OR 2N321 AUDIO

L_1	435 μh ±10%
L_2	250 μh ±10%
CR_1, CR_2	IN64G OR EQUIV.
ΔC — 190.6	R/C MODEL 242
ΔC — 89.3	

NOMINAL SENSITIVITY: 150 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 65.0 KC/S
TOTAL BATTERY DRAIN : 25.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

SIX VOLT FOUR TRANSISTOR REFLEX RECEIVER
FIGURE 73



R_1, R_{14}	1500 OHM
R_2	6800 OHM
R_3	27,000 OHM
R_4, R_{11}	470 OHM
R_5	82,000 OHM
R_6	330 OHM
R_7, R_8	3300 OHM
R_9	10,000 OHM
R_{10}	91,000 OHM
R_{12}	VOLUME CONTROL 10,000 OHM AUDIO TAPER
R_{13}	100 OHM
R_{15}	120 OHM

C_1, C_{11}	.02μfd
C_2, C_3, C_7	.01μfd
C_4, C_6, C_9, C_{13}	.05μfd
C_5	15μfd, 12V
C_8	50μfd, 3V
C_{10}	6μfd, 12V
C_{12}	50μfd, 12V
C_{14}	100μfd, 12V
TR_1	2N168A CONVERTER
TR_2	2N292 IST I.F.
TR_3	2N169 REFLEX
TR_4	2N188A OR 2N320 AUDIO

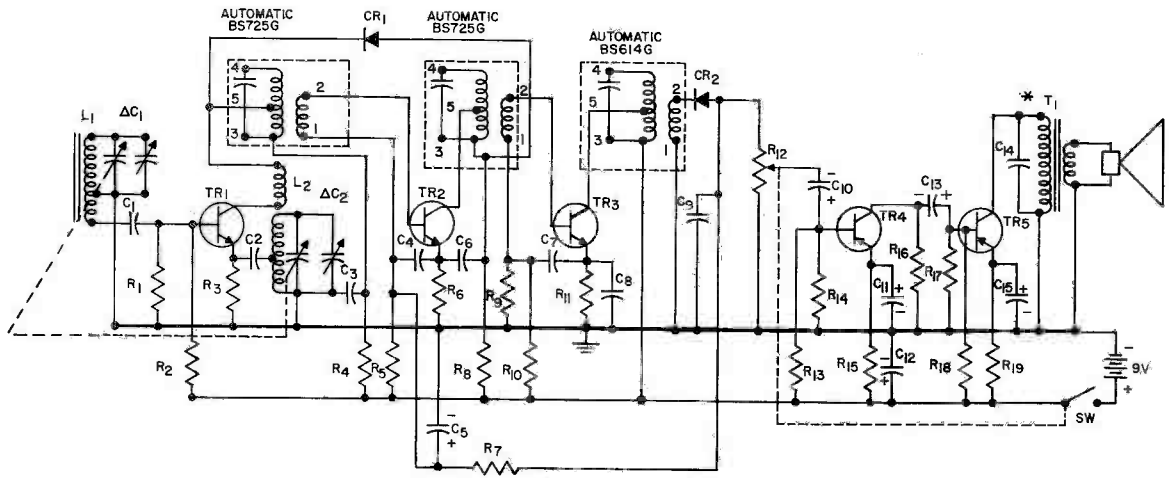
L_1	435μh±10%
L_2	250μh±10%
CR_1, CR_2	IN64G OR EQUIV.
ΔC_1 — 190.6 ΔC_2 — 89.3	R/C MODEL 242

NOMINAL SENSITIVITY: 200 MICROVOLTS/METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT: 75 MILLIWATTS
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 60.0 KC/S
TOTAL BATTERY DRAIN : 17.0 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

NINE VOLT FOUR TRANSISTOR REFLEX RECEIVER

FIGURE 74



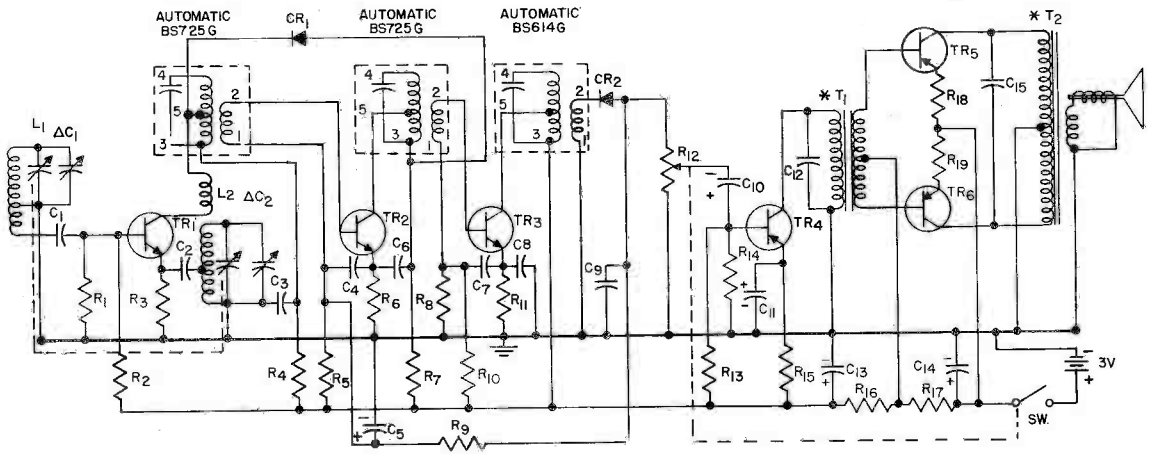
R_1,	6800 OHM	C_1,	.02 μfd	ΔC_1, — 190.6 ΔC_2, — 89.3 }	R/C MODEL 242
R_2,	27,000 OHM	C_2, C_3,	.01 μfd		
R_3,	1500 OHM	$C_4, C_6, C_7, C_8, C_9, C_{14}$,	.05 μfd		
R_4, R_{11}, R_{15},	470 OHM	C_5,	15 μfd, 12V		
R_5,	68,000 OHM	C_{10}, C_{13},	6 μfd, 12V		
R_6,	330 OHM	C_{11}, C_{15},	100 μfd, 12V		
R_7,	2700 OHM	C_{12},	50 μfd, 12V		
R_8, R_{16},	3300 OHM	TR_1,	G.E. 2N168A CONVERTER		
R_9	10,000 OHM	TR_2,	G.E. 2N293 IST I.F.		
R_{10},	82,000 OHM	TR_3,	G.E. 2N169 2ND I.F.		
R_{12},	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER	TR_4,	G.E. 2N265 DRIVER		
		TR_5,	G.E. 2N188A OR 2N320 OUTPUT		
R_{13},	4700 OHM	* T_1,	500 Ω/VC		
R_{14},	56,000 OHM	L_1,	435 μh ± 10%		
R_{17},	5600 OHM	L_2,	250 μh ± 10%		
R_{18},	1000 OHM	CR_1, CR_2,	DR117, IN64G OR CK706A		
R_{19},	68 OHM				

NOMINAL SENSITIVITY : 150 MICROVOLTS/ METER
(MEASURED WITH 5 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 75 MILLIWATTS.
SELECTIVITY AT −6db : 8.0 KC/S.
SELECTIVITY AT −60db: 65.0KC/ S.
TOTAL BATTERY DRAIN: 18.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

FIVE TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 75



R_1, R_8 — 10,000 OHM
R_2 — 33,000 OHM
R_3, R_{11} — 470 OHM
R_4 — 270 OHM
R_5 — 12,000 OHM
R_6 — 330 OHM
R_7 — 1500 OHM
R_9 — 2700 OHM
R_{10} — 18,000 OHM
R_{13} — 4700 OHM
R_{14} — 15,000 OHM
R_{15} — 390 OHM
R_{16} — 100 OHM
R_{17} — 39 OHM
R_{18}, R_{19} — 5.0 OHM
R_{12} — VOLUME CONTROL 10,000 OHM 1/2 W AUDIO TAPER

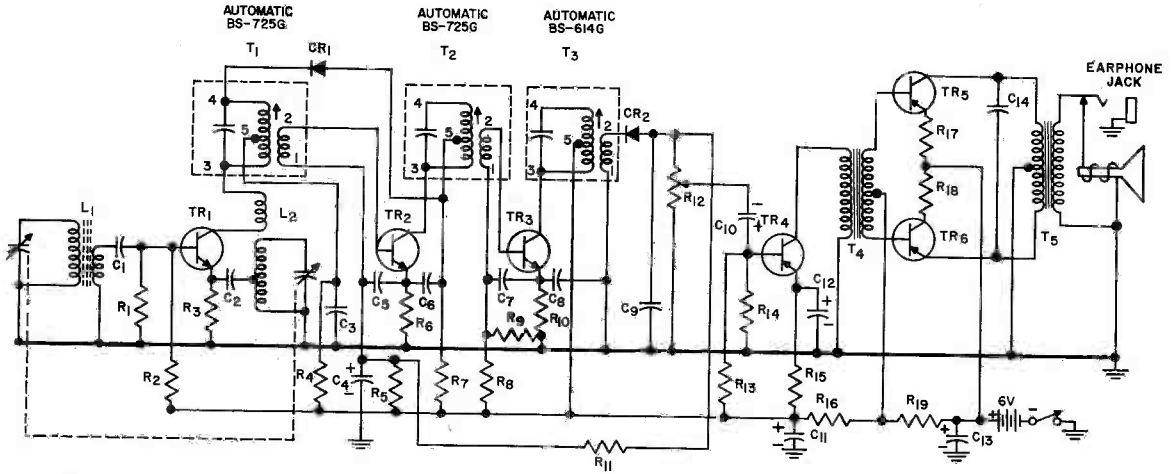
C_1 — .02μfd C_{12} — .003μfd
C_2, C_3 — .01μfd
C_4, C_6, C_7, C_8, C_9 — .05μfd
C_5, C_{10} — 6μfd, 6V
C_{11}, C_{13}, C_{14} — 50μfd, 6V
C_{15} — 0.1μfd
TR_1 — G.E. 2N168A CONVERTER
TR_2 — G.E. 2N293 IST I.F.
TR_3 — G.E. 2N169 2ND I.F.
TR_4 — G.E. 2N192 OR 2N324 DRIVER
TR_5, TR_6 — G.E. 2N188 AUDIO
* T_1 — 2600/2600Ω CT.
* T_2 — 300Ω CT/VC.
* L_1 — 435μh ±10%
* L_2 — 250μh ±10%
CR_1, CR_2 — DR117, IN646, OR CK706A OR EQUIV.
* ΔC_1 — 190.6 } R/C MODEL 242
* ΔC_2 — 89.3 }

NOMINAL SENSITIVITY: 250 MICROVOLTS / METER
(MEASURED WITH 5 MW REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 100 MILLIWATTS.
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 65.0 KC/S
ZERO SIGNAL BATTERY DRAIN : 7.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

THREE VOLT BROADCAST RECEIVER
CAN BE POWERED BY SUN OR FLASHLIGHT BATTERIES

FIGURE 76



R_1, R_8	10,000 OHM
R_2	15,000 OHM
R_3	1500 OHM
R_4	270 OHM
R_5	47,000 OHM
R_6	220 OHM
R_7, R_9	2200 OHM
R_{10}	1000 OHM
R_{11}, R_{14}	4700 OHM
R_{12}	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_{13}	68,000 OHM
R_{15}	470 OHM
R_{16}	100 OHM
R_{17}, R_{18}	8.2 OHM
R_{19}	33 OHM

C_1	.02 μfd.
$C_2, C_3, C_5, C_6, C_7, C_8$	.01μfd.
C_4, C_{10}	6μfd.
C_9	.05μfd.
C_{11}, C_{12}, C_{13}	50μfd.
C_{14}	.2μfd
CR1, CR2	IN64G OR EQUIV
TR_1	G.E. 2N168A
TR_2	G.E. 2N293
TR_3	G.E. 2N169
TR_4	G.E. 2N192
TR_5, TR_6	G.E. 2N188

* T_4 = 3600Ω/2000Ω CT

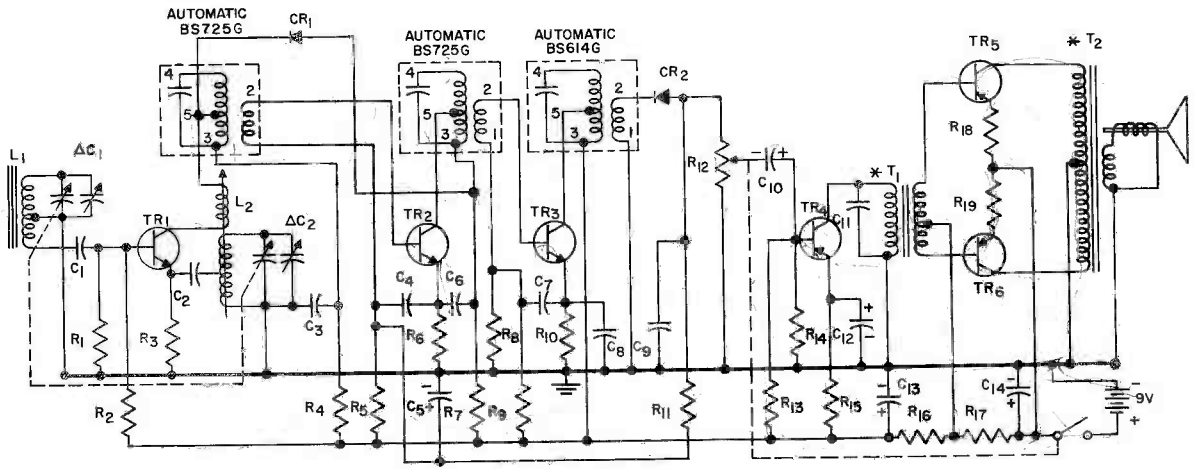
* T_5 = 360Ω CT/VC

NOMINAL SENSITIVITY: 200 MICRO VOLTS/METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER)
MAXIMUM POWER OUTPUT: 200 MW
SELECTIVITY AT -6 db: 8.0 Kc/S
SELECTIVITY AT -60 db: 60.0 Kc/S
ZERO SIGNAL BATTERY DRAIN: 8 MILLIAMPS

* FOR FURTHUR INFORMATION SEE PAGE 167

SIX VOLT SIX TRANSISTOR BROADCAST RECEIVER

FIGURE 77



R_1,	6800 OHM
R_2,	27,000 OHM
R_3,	1500 OHM
R_4, R_{10}, R_{15},	470 OHM
R_5,	68,000 OHM
R_6,	330 OHM
R_7,	3300 OHM
R_8,	10,000 OHM
R_9,	82,000 OHM
R_{11},	2700 OHM
R_{12},	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER
R_{13},	4700 OHM
R_{14},	56,000 OHM
R_{16},	220 OHM
R_{17},	33 OHM

R_{18}, R_{19},	8.2 OHM
C_1,	.02 μfd
C_2, C_3,	.01 μfd
C_4, C_6, C_7, C_8,	.05 μfd
C_5, C_{10},	6 μfd, 12V
C_9,	.05 μfd
C_{11},	.003 μfd
C_{12}, C_{13}, C_{14},	50 μfd, 12V
TR_1,	G.E. 2N168A CONVERTER
TR_2,	G.E. 2N293 IST I.F.
TR_3,	G.E. 2N169 2ND I.F.
TR_4,	G.E. 2N192 OR 2N324 DRIVER
TR_5, TR_6,	G.E. 2N188A OR 2N320 AUDIO
* T_1,	5,000 / 2600Ω CT
* T_2,	250Ω CT/V.C.

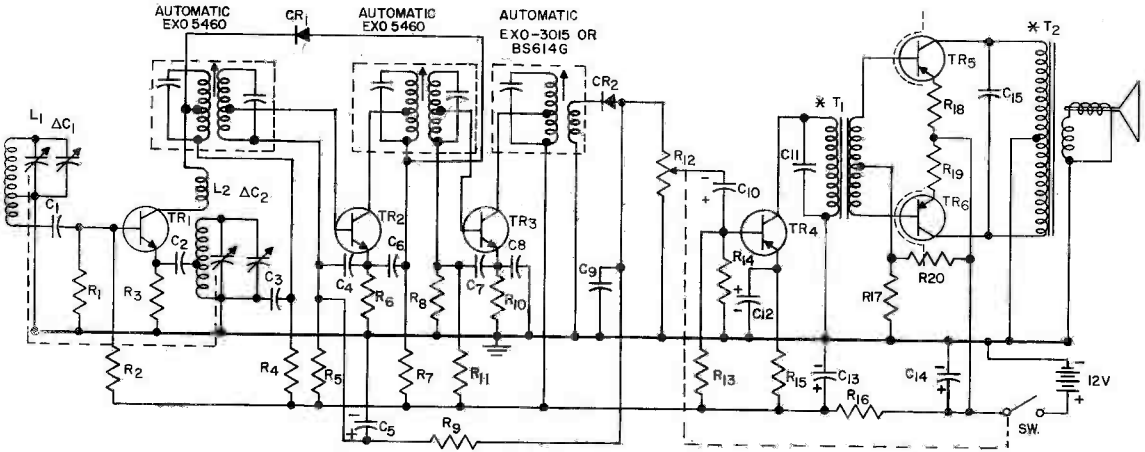
* L_1	435 μh ±10%
* L_2	250 μh ±10%
CR_1, CR_2,	DR117, IN64G, OR CK706A OR EQUIV.
* ΔC1,	190.6 } R/C MODEL 242
* ΔC2	89.3 }

NOMINAL SENSITIVITY = 200 MICROVOLTS / METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT .6 WATTS.
SELECTIVITY AT −6db : 8.0 KC/S
SELECTIVITY AT −60db : 60.0 KC/S
ZERO SIGNAL BATTERY DRAIN 7.0 MILLIAMPS.

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

SIX TRANSISTOR SUPERHETERODYNE BROADCAST RECEIVER

FIGURE 78



R_1, R_{11}	6800 OHM	C_1	.02 μfd
R_2	33,000 OHM	C_2, C_3	.01 μfd
R_3	1500 OHM	C_4, C_6, C_7, C_8	.1 μfd
R_4, R_{10}, R_{15}	470 OHM	C_5	6 μfd, 12V
R_5	100,000 OHM	C_9	.05 μfd
R_6	330 OHM	C_{10}	6 μfd, 6V
R_7, R_{13}	4700 OHM	C_{11}	.003 μfd
R_8	2200 OHM	C_{12}, C_{13}, C_{14}	50 μfd, 12V
R_9	27 00 OHM	C_{15}	.2 μfd
R_{12}	VOLUME CONTROL 10,000 OHM 1/2W AUDIO TAPER	TR_1	G.E. 2N168A CONVERTER
R_{14}	15,000 OHM	TR_2	G.E. 2N293 IST. I.F.
R_{16}	220 OHM	TR_3	G.E. 2N169 OR 2ND. I.F.
R_{17}	2700 OHM	TR_4	G.E. 2N92 OR 2N324 DRIVE
R_{18}, R_{19}	10 OHM	TR_5, TR_6	G.E. 2N188A OR 2N320 AUDIO 1&2 WITH CLIP-ON HEAT SINK
R_{20}	33 OHM		

* T_1	2000/2600 CT.	
* T_2	200Ω CT/VC	
L_1	435 μh ± 10%	
L_2	250 μh ± 10%	
ΔC_1 — 190.6 ΔC_2 — 89.3	R/C MODEL	
CR_1, CR_2	IN64 OR IN295 OR EQUIV.	

NOMINAL SENSITIVITY : 150 MICROVOLTS/METER
(MEASURED WITH 50 MILLIWATTS REFERENCE POWER OUTPUT)
MAXIMUM POWER OUTPUT : 1 WATT
SELECTIVITY AT -6db : 8.0 KC/S
SELECTIVITY AT -60db : 38.0 KC/S
ZERO SIGNAL BATTERY DRAIN : 10 MILLIAMPS

* FOR FURTHER COMPONENT INFORMATION SEE PAGE 167

SIX TRANSISTOR, 1 WATT RECEIVER

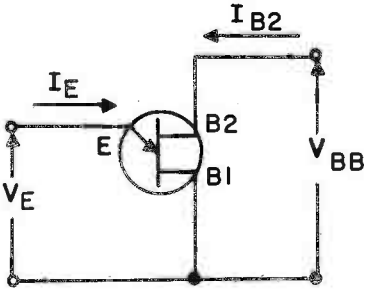
FIGURE 79

UNIJUNCTION TRANSISTOR CIRCUITS

The unijunction transistor is a three-terminal semiconductor device which has electrical characteristics that are quite different from those of conventional two-junction transistors. Its most important feature is its highly stable negative resistance characteristic which permits its application in oscillator circuits, timing circuits and bistable circuits. Circuits such as sawtooth generators, pulse generators, delay circuits, multivibrators, one-shots, trigger circuits and pulse rate modulators can be greatly simplified by the use of the unijunction transistor.

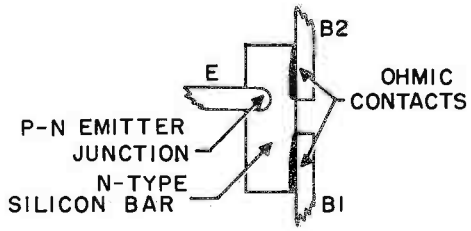
THEORY OF OPERATION

The construction of the unijunction transistor is shown in Figure 81. Two ohmic contacts, called base-one (B1) and base-two (B2) are made at opposite ends of a small bar of n-type silicon. A single rectifying contact, called the emitter (E), is made on the opposite side of the bar close to base-two. An interbase resistance, R_{BB}, of between 5K and 10K exists between base-one and base-two. In normal circuit operation, base-one is grounded and a positive bias voltage, V_{BB}, is applied at base-two. With no emitter current flowing, the silicon bar acts like a simple voltage divider (Figure 82) and a certain fraction, η, of V_{BB} will appear at the emitter. If the emitter voltage, V_E, is less than ηV_{BB}, the emitter will be reverse-biased and only a small emitter leakage current will flow. If V_E becomes greater than ηV_{BB}, the emitter will be forward biased and emitter current will flow. This emitter current consists primarily of holes injected into the silicon bar. These holes move down the bar from the emitter to base-one and result in an equal increase in the number of electrons in the emitter to base-one region. The net result is a decrease in the resistance between emitter and base-one so that as the emitter current increases, the emitter voltage decreases and a negative resistance characteristic is obtained (Figure 84).



Symbol for unijunction transistor with indentification of principle voltages and currents

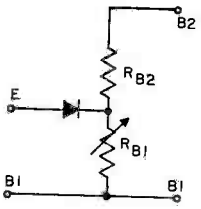
FIGURE 80



Construction of unijunction transistor—cross sectional view

FIGURE 81

The operation of the unijunction transistor may be best understood by the representative circuit of Figure 82. The diode represents the emitter diode, R_{B1} represents the resistance of the region in the silicon bar between the emitter and base-one and R_{B2} represents the resistance between the emitter and base-two. The resistance R_{B1} varies with the emitter current as indicatd in Figure 83.



Unijunction transistor representative circuit

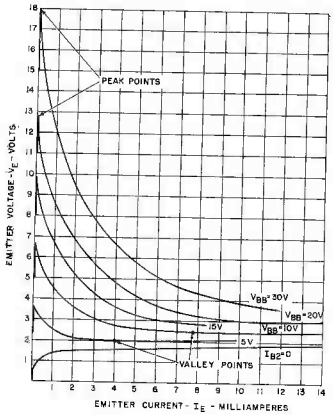
FIGURE 82

I_E (MA)	R_{B1} (OHMS)
0	4600
1	2000
2	900
5	240
10	150
20	90
50	40

Variation of R_{B1} with I_E in representative circuit (typical 2N492)

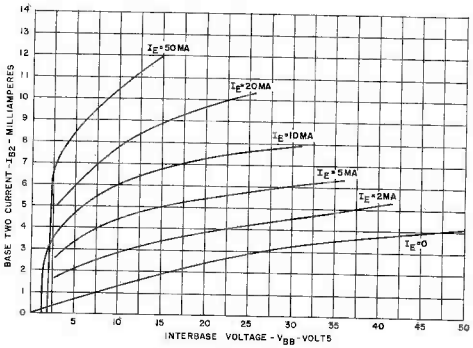
FIGURE 83

The large signal properties of the unijunction transistor are usually given in the form of characteristic curves. Figure 84 gives typical emitter characteristic curves as plots of emitter voltage vs. emitter current for fixed values of interbase voltage. Figure 85 gives typical interbase characteristic curves as plots of interbase voltage vs. base-two current for fixed values of emitter current. On each of the emitter characteristic curves there are two points of interest, the peak point and the valley point. On each of the emitter characteristic curves the region to the left of the peak point is called the cut-off region; here the emitter is reverse biased and only a small leakage current flows. The region between the peak point and the valley point is the negative resistance region. The region to the right of the valley point is the saturation region; here the dynamic resistance is positive and lies in the range of 5 to 20Ω.



Typical emitter characteristics (type 2N492)

FIGURE 84



Typical interbase characteristics (type 2N492)

FIGURE 85

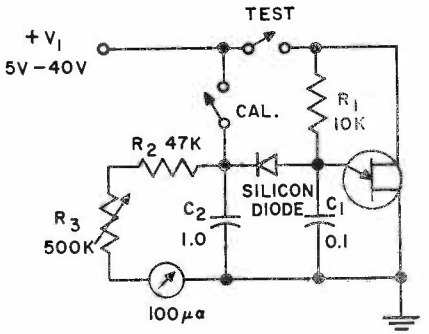
PARAMETERS—DEFINITION AND MEASUREMENT

1. R_{BB} – Interbase Resistance. The interbase resistance is the resistance measured between base-one and base-two with the emitter open circuited. It may be measured with any conventional ohmmeter or resistance bridge if the applied voltage is five volts or less. The interbase resistance increases with temperature at about 0.8%/°C. This temperature variation of R_{BB} may be utilized for either temperature compensation or in the design of temperature sensitive circuits.

2. η – Intrinsic Stand-off Ratio. This parameter is defined in terms of the peak point voltage, V_P, by means of the equation: $V_P = \eta V_{BB} + V_D$ . . . where V_D is about 0.70 volt at 25°C and decreases with temperature at about 3 millivolts/°C. It is

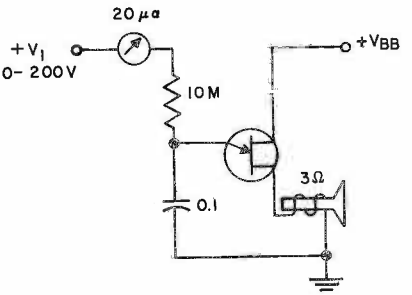
found that η is constant over wide ranges of temperature and interbase voltage. A circuit which may be used to measure η is shown in Figure 86. In this circuit R_1, C_1, and the unijunction transistor form a relaxation oscillator and the remainder of the circuit serves as a peak voltage detector with the diode automatically subtracting the voltage V_D. To use the circuit, the voltage V_1 is set to the value desired, the "cal." button is pushed and R_3 adjusted to make the meter read full scale. The "test" button is then pushed and the value of η is read directly from the meter (1.0 full scale). If the voltage V_1 is changed, the meter must be recalibrated.

3. I_P – Peak Point Current. The peak point current corresponds to the emitter current at the peak point. It represents the minimum current which is required to fire the unijunction transistor or required for oscillation in the relaxation oscillator circuit. I_P is inversely proportional to the interbase voltage. I_P may be measured in the circuit of Figure 87. In this circuit, the voltage V_1 is increased until the unijunction transistor fires as evidenced by noise from the loudspeaker. V_1 is then reduced slowly until the unijunction ceases to fire and the current through the meter is read as I_P.



TEST CIRCUIT FOR INTRINSIC STANDOFF RATIO (η)

FIGURE 86



TEST CIRCUIT FOR PEAK POINT EMITTER CURRENT (IP)

FIGURE 87

4. V_P – Peak Point Emitter Voltage. This voltage depends on the interbase voltage as indicated in (2). V_P decreases with increasing temperature because of the change in V_D and may be stabilized by a small resistor in series with base-two.

5. V_E (sat) – Emitter Saturation Voltage. This parameter indicates the forward drop of the unijunction transistor from emitter to base-one when it is conducting the maximum rated emitter current. It is measured at an emitter current of 50 ma and an interbase voltage of 10 volts.

6. I_{B2} (mod) – Interbase Modulated Current. This parameter indicates the effective current gain between emitter and base-two. It is measured as the base-two current under the same condition used to measure V_E (sat).

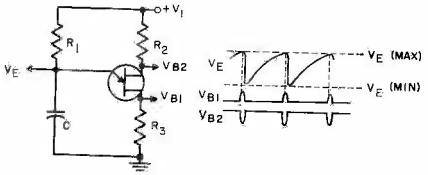
7. I_{EO} – Emitter Reverse Current. The emitter reverse current is measured with 60 volts between base-two and emitter with base-one open circuit. This current varies with temperature in the same way as the I_{CO} of a conventional transistor.

8. V_V – Valley Voltage. The valley voltage is the emitter voltage at the valley point. The valley voltage increases as the interbase voltage increases, it decreases with resistance in series with base-two and increases with resistance in series with base-one.

9. I_V – Valley Current. The valley current is the emitter current at the valley point. The valley current increases as the interbase voltage increases and decreases with resistance in series with base-one or base-two.

RELAXATION OSCILLATOR

The relaxation oscillator circuit shown in Figure 88 is a basic circuit for many applications. It is chiefly useful as a timing circuit, a pulse generator, a trigger circuit or a sawtooth wave generator.



BASIC RELAXATION OSCILLATOR WITH TYPICAL WAVEFORMS
FIGURE 88

Conditions for Oscillation.

$$\frac{V_1 - V_P}{R_1} > I_p, \quad \frac{V_1 - V_V}{R_1} < I_V$$

It is found that these conditions are very broad permitting a 1000 to 1 range of R_1 from about 2K to 2M. R_2 is used for temperature compensation, its value may be calculated from the equation:

$$R_2 \cong \frac{0.65\ R_{BB}}{\eta V_1}$$

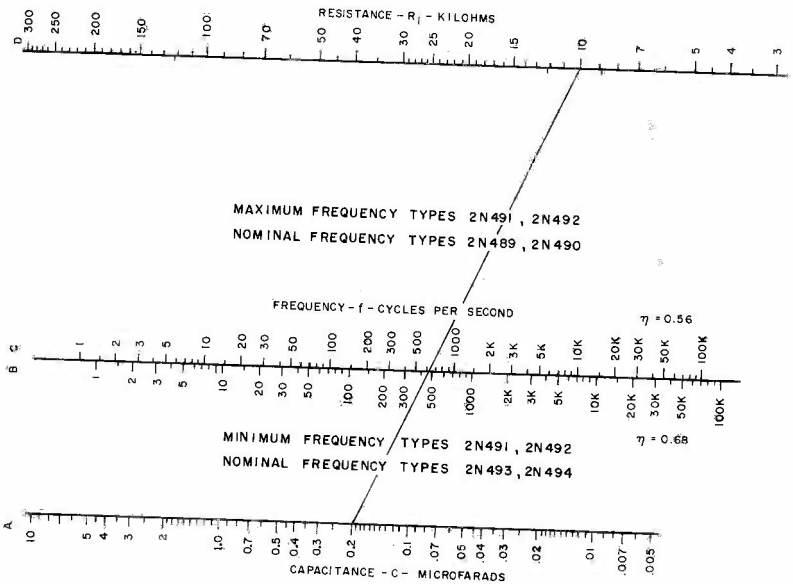
The maximum and minimum voltages of the emitter voltage waveform may be calculated from:

$$V_E\ (\text{max.}) = V_p = \eta V_{BB} + 0.7$$
$$V_E\ (\text{min.}) \cong 1/2\ V_E\ (\text{sat})$$

The frequency of oscillation is given by the equation:

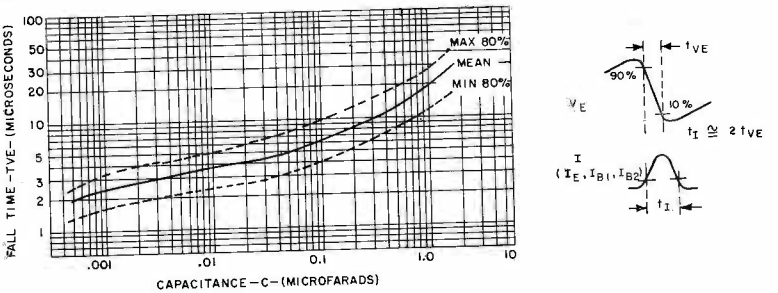
$$f \cong \frac{1}{R_1 C \ln\left(\frac{1}{1-\eta}\right)}$$

and may be obtained conveniently from the nomogram of Figure 89.



Nomogram for calculating frequency of relaxation oscillation
FIGURE 89

The emitter voltage recovery time, t_{VE}, is defined as the time between the 90% and 10% points on the emitter voltage waveform. The value of t_{VE} is determined primarily by the size of the capacitor C in Figure 88 and may be obtained from Figure 90.



Recovery time of unijunction transistor relaxation oscillator vs. capacity

FIGURE 90

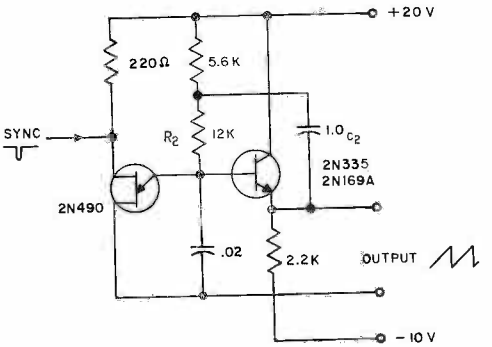
The pulse amplitude at base-one or base-two may be determined from the equations:

$$I_{E(peak)} \cong \frac{[V_p - 1/2\ V_E(sat)]C}{t_{VE}}$$

$$I_{B_2(peak)} \cong \frac{I_{B2}(mod)}{7}\sqrt{I_{E(peak)}}$$

SAWTOOTH WAVE GENERATOR

The circuit of Figure 91 may be used as a linear sawtooth wave generator. The NPN transistor serves as an output buffer amplifier with the capacitor C_2 and resistor R_2 serving in a bootstrap circuit to improve the linearity of the sawtooth. The output of the circuit shown has an amplitude of about 12 volts peak to peak and a frequency of about 2 Kc. Note that a negative synchronizing pulse may be used at base-two.



LINEAR SAWTOOTH GENERATOR

FIGURE 91

MULTIVIBRATOR

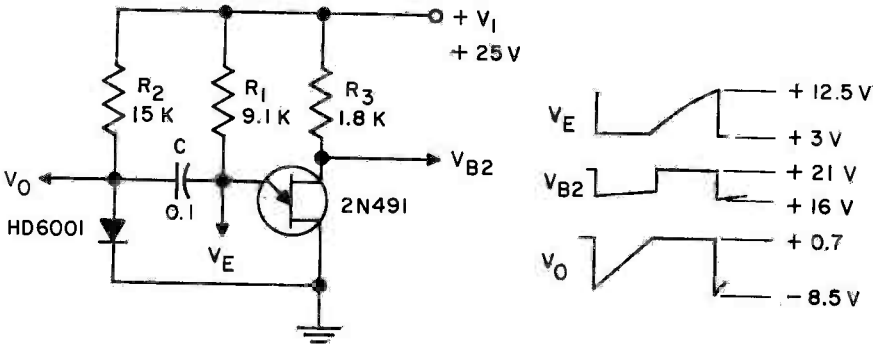
Figure 92 shows a unijunction transistor multivibrator circuit which has a frequency of about 1 Kc. The conditions for oscillation of this circuit are the same as for the relaxation oscillator. The length of time during which the unijunction transistor is off (no emitter current flowing) is determined primarily by R_1. The length of time during

which the unijunction transistor is on is determined primarily by R_2. The periods may be calculated from the equations:

$$t_1 = R_1 C \ln\left[\frac{V_1 - V_E}{V_1 - V_p}\right]$$

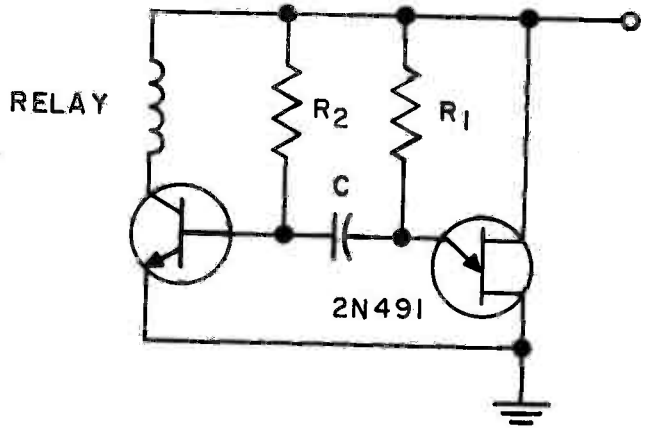
$$t_2 = R_2 C \ln\left[\frac{V_1 + V_p - V_E}{V_1}\right]$$

Where V_E is measured at an emitter current of $I_E = \frac{V_1 (R_1 + R_2)}{R_1 R_2}$ and may be obtained from the emitter characteristic curves.



UNIJUNCTION TRANSISTOR MULTIVIBRATOR WITH TYPICAL WAVE FORMS
FIGURE 92

An NPN transistor may be direct coupled to the multivibrator circuit by replacing the diode as shown in Figure 93. This circuit has the advantage that the load does not have any effect on the timing of the circuit.

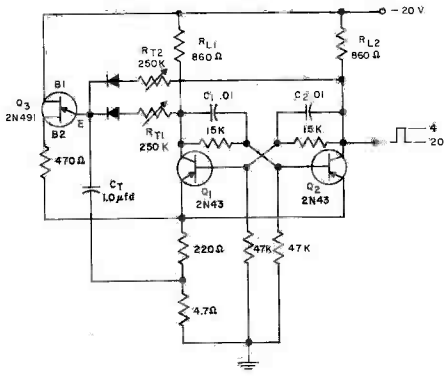


Unijunction transistor multivibrator used to drive NPN transistor
FIGURE 93

HYBRID MULTIVIBRATOR

The circuit of Figure 94 illustrates how the unijunction transistor may be used in conjunction with conventional transistors to obtain the maximum advantages of each. The two PNP transistors form a conventional flip-flop with the unijunction serving the timing and triggering function. The timing capacitor C_T is charged alternately through R_{T1} and R_{T2}. The advantages obtained by a circuit of this type are:

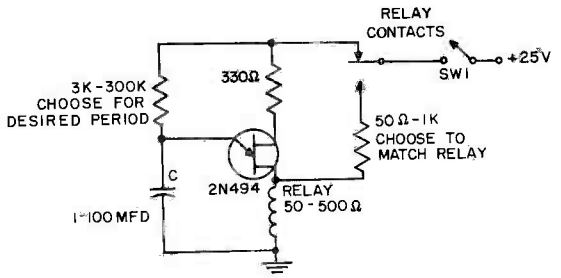
(1) The two periods may be adjusted independently over a range of as much as 1000 to 1. (2) The output at the collector of each of the transistors is very nearly an ideal rectangular waveform. (3) The circuit will tolerate large changes in I_{CO} or beta of the transistors. It is not prone to "lock-up" or non-oscillation. (4) The timing stability is very good. (5) A small timing capacitor C_T may be used, avoiding the use of electrolytic capacitors in many applications.



HYBRID MULTIVIBRATOR
FEATURING WIDE RANGE OPERATION
FIGURE 94

RELAY DELAY

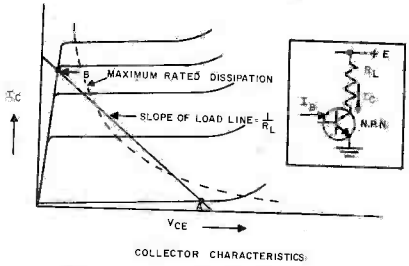
Figure 95 shows the use of the unijunction transistor to obtain a precise delay in the operation of a relay. When the switch SW1 is closed, the capacitor C is charged to the peak point voltage at which time the unijunction transistor fires and the capacitor discharges through the relay thus causing it to close. One set of relay contacts hold the relay closed. For supply voltages of 30 volts or above, about one second of delay can be obtained per microfarad of capacitance.



TIME DELAY CIRCUIT WITH RELAY
FIGURE 95

TRANSISTOR SWITCHES

A switch is characterized by a high resistance when it is open and a low resistance when it is closed. Transistors can be used as switches. They offer the advantages of no moving or wearing parts and are easily actuated from various electrical inputs. Transistor collector characteristics as applied to a switching application is shown in Figure 96. The operating point A at which $I_C = I_{CO}/1-\alpha$ indicates the transistor's high resistance



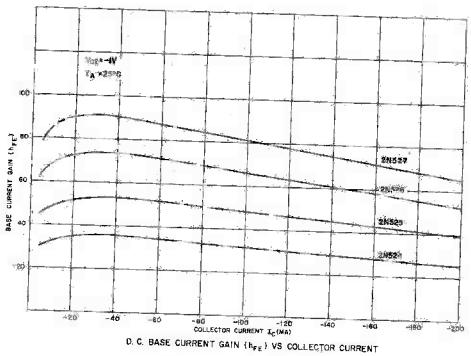
COLLECTOR CHARACTERISTICS

FIGURE 96

when $I_B = O$. Since $1-\alpha$ is a small number, I_C may be many times greater than I_{CO}. Shorting the base to the emitter results in a smaller I_C. If the base to emitter junction is reversed biased by more than .2v, I_C will approach I_{CO}. Reverse biasing achieves the highest resistance across an open transistor switch.

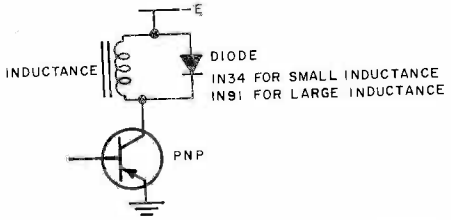
When the transistor switch is turned on, the voltage across it should be a minimum. At operating point B of Figure 96, the transistor is a low resistance. Alloy transistors such as the 2N525 have about one ohm resistance when switched on. Grown junction transistors, such as the 2N167 have approximately 80 ohms resistance which makes them less suitable for high power switching although they are well suited for high speed computer applications. In order that a low resistance be achieved, it is necessary that point B lie beyond the knee of the characteristic curves. The region beyond the knee is referred to as the saturation region. Enough base current must be supplied to ensure that this point is reached. It is also important that both the on and off operating points lie in the region below the maximum rated dissipation to avoid transistor destruction. It is permissible, however, to pass through the high dissipation region very rapidly since peak dissipations of about one watt can be tolerated for a few microseconds with a transistor rated at 150 mw. In calculating the I_B necessary to reach point B, it is necessary to know how h_{FE} varies with I_C. Curves such as Figure 97 are provided for switching transistors. Knowing h_{FE} from the curve gives

FIGURE 97



D. C. BASE CURRENT GAIN (h_{FE}) VS COLLECTOR CURRENT

$I_{B\,min}$ since $I_{B\,min} = \frac{I_C}{h_{FE}}$. Generally I_B is made two or three times greater than $I_{B\,min}$ to allow for variations in h_{FE} with temperature or aging. The maximum rated collector voltage should never be exceeded since destructive heating may occur once a transistor breaks down. Inductive loads can generate injurious voltage transients. These can be avoided by connecting a diode across the inductance to absorb the transient as shown in Figure 98.

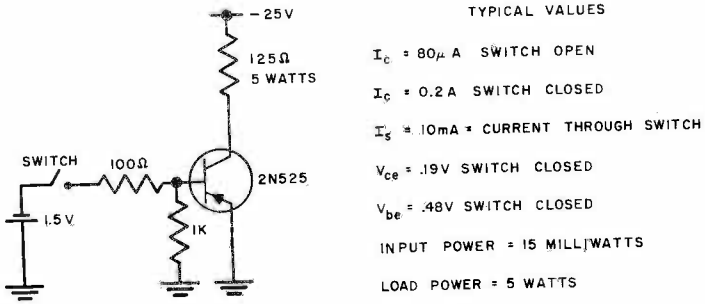


DIODE USED TO PROTECT TRANSISTOR FROM INDUCTIVE VOLTAGE TRANSIENTS.

FIGURE 98

Lighted incandescent lamps have about 10 times their off resistance. Consequently, I_B must be increased appreciably to avoid overheating the switching transistor when lighting a lamp.

A typical switching circuit is shown in Figure 99. The requirement is to switch a



Typical transistor switch application

FIGURE 99

200 ma current in a 25 volt circuit, delivering 5 watts to the load resistor. The mechanical switch contacts are to carry a low current and be operated at a low voltage to minimize arcing. The circuit shown uses a 2N525. The 1K resistor from the base to ground reduces the leakage current when the switch is open. Typical values are indicated in Figure 99.

TEMPERATURE EFFECTS ON SWITCHING CIRCUITS

At high junction temperatures, I_{CO} can become a problem. In the off condition, both the emitter and collector junctions are generally reverse-biased. As a rule, the bias source has an appreciable resistance permitting a voltage to be developed across the resistance by I_{CO}. The voltage can reduce the reverse bias to a point where the base becomes forward biased and conduction occurs. Conduction can be avoided by reducing the bias source resistance, by increasing the reverse bias voltage or by reducing I_{CO} through a heat sink or a lower dissipation circuit design.

The I_{CO} of a transistor is generated in three ways. One component originates in the semiconductor material in the base region of the transistor. At any temperature, there are a number of interatomic energy bonds which will spontaneously break into a hole-electron pair. If a voltage is applied, the hole and electron drift in opposite directions and can be seen as the I_{CO} current. If no voltage is present, the hole and electron eventually recombine. The number of bonds that will break can be predicted theoretically to double about every 10°C in germanium transistors and every 6°C in silicon. Theory also indicates that the number of bonds broken will not depend on voltage over a considerable voltage range. At low voltages, I_{CO} appears to decrease because the drift field is too small to extract all hole-electron pairs before they recombine. At very high voltages, breakdown occurs.

A second component of I_{CO} is generated at the surface of the transistor by surface energy states. The energy levels established at the center of a semiconductor junction cannot end abruptly at the surface. The laws of physics demand that the energy levels adjust to compensate for the presence of the surface. By storing charges on the surface, compensation is accomplished. These charges can generate an I_{CO} component; in fact, in the processes designed to give the most stable I_{CO}, the surface energy levels contribute much I_{CO} current. This current behaves much like the base region component with respect to voltage and temperature changes. It is described as the surface thermal component in Figure 100.

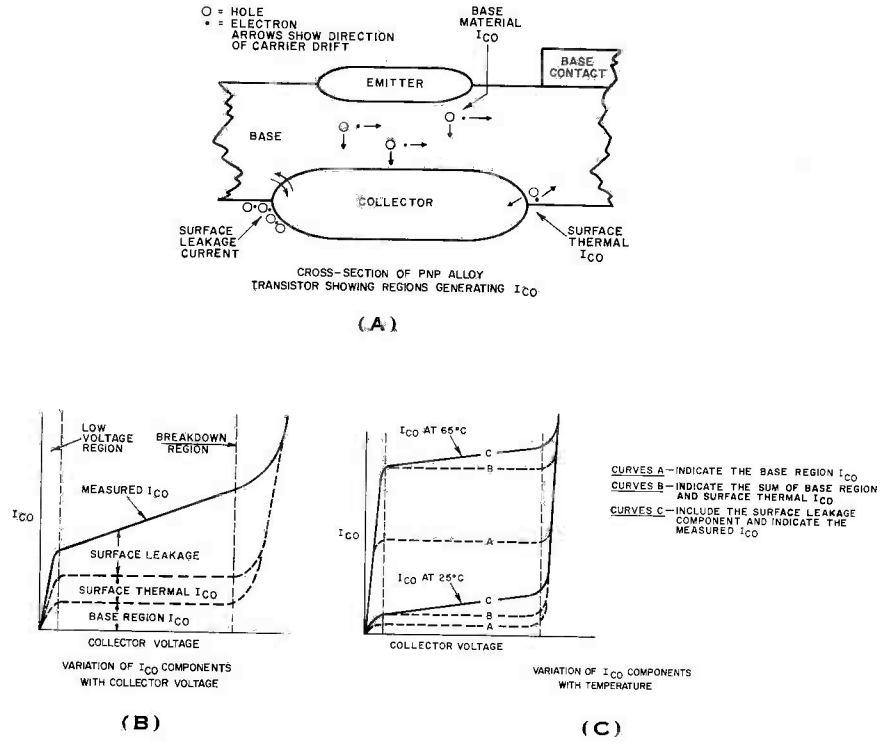
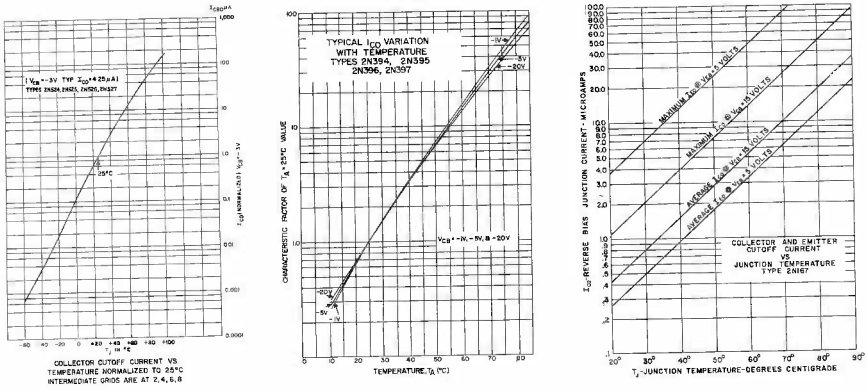


FIGURE 100

A third component of I_{CO} is generated at the surface of the transistor by leakage across the junction. This component can be the result of impurities, moisture or surface imperfections. It behaves like a resistor in that it is relatively independent of temperature but varies markedly with voltage. Figure 100(a) shows the regions which contribute to the three components. Figure 100(b) illustrates how the components vary with voltage. It is seen that while there is no way to measure the base region and surface energy state components separately, a low voltage I_{CO} consists almost entirely of these two components. Thus, the surface leakage contribution to a high voltage I_{CO} can be readily determined by subtracting out the low voltage value of I_{CO}.

Figure 100(c) shows the variation of I_{CO} with temperature. Note that while the surface thermal and base I_{CO} components have increased markedly, the leakage component is unchanged. For this reason, as temperature is changed the high voltage I_{CO} will change by a smaller percentage than the low voltage I_{CO}.



(A) (B) (C)

FIGURE 101

Figure 101 shows the variation of I_{CO} with temperature and voltage for a number of transistor types. Note that the three curves for the 2N396 agree with the principles above and show a leakage current less than one microampere.

The variation of current gain at high temperatures is also significant. Since h_{FE} is defined as I_C/I_B, h_{FE} depends on I_{CO} since $I_C \approx h_{fe}(I_B + I_{CO})$. If $I_B = 0$ i.e., if the base is open circuited, a collector current still flows, $I_C = h_{fe}I_{CO}$. Thus h_{FE} is infinite when $I_B = 0$. As base current is applied, the ratio I_C/I_B becomes more meaningful. If h_{FE} is measured for a sufficiently low I_C, then at a high temperature $h_{fe}I_{CO}$ will become equal to I_C. At this temperature h_{FE} becomes infinite since no I_B is required to maintain I_C. The AC current gain h_{fe}, however, is relatively independent of I_{CO} and generally increases about 2:1 from $-55°C$ to $+85°C$.

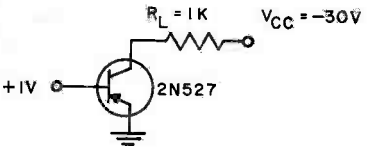
The different electrical properties of the base, emitter and collector regions tend to disappear at high temperatures with the result that transistor action ceases. This temperature usually exceeds 85°C and 150°C in germanium and silicon transistors respectively.

At high junction temperatures, it is possible for the transistor to heat itself regeneratively until it destroys itself. The factors which enter into this problem are I_{CO}, V_{CB}, and collector load resistance and the thermal impedance of the transistor. If the load

resistance is large enough, it can limit the transistor dissipation to a safe value; otherwise, the transistor is heated by $I_{CO} \times V_{CB}$. As the temperature rises, this heating can become appreciable.

The following procedure, illustrated in Figure 102 gives a conservative estimate of the run-away temperature for a transistor with both junctions reverse biased. Thermal run-away will occur at the temperature where the rate at which I_{CO} increases heating, exceeds the thermal derating factor. To calculate this temperature, let us assume a 1°C rise in junction temperature. The increased heating due to the rise will be, 0.08 I_{CO} ($V_{CC} - 2R_L I_{CO}$), since I_{CO} increases about 8% per 1°C. If this power will in fact raise the junction temperature by 1°C according to the derating factor, run-away occurs.

CIRCUIT



CALCULATE

$0.08\ I_{COM}\ (V_{CC} - 2R_L\ I_{COM}) = 1/K$ where I_{CO} at run-away temperature = I_{COM}. Use:

Data from specifications
$K = .27°C/mw$

Data from circuit
$R_L = 1K$
$V_{CC} = 30$ volts. The solution by substitution is
$I_{COM} = 1.75$ ma or 13.2 ma.

The smaller value is always the correct one.

Using $I_{CO} = 10\ \mu a$ max at $T_J = 25°C$, from Figure 101A, $T_J = 100°C$ when $I_{CO} = 1.75$ ma.

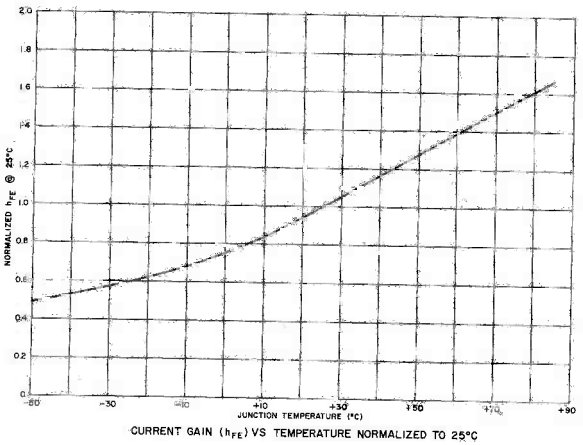
Heating due to I_{COM} is
$P = I_{COM}\ (V_{CC} - R_L\ I_{COM}) = 49.5$ mw.

Rise in junction temperature above ambient temperature is
$KP = (.27)\ (49.5) = 13.4°C = T_J - T_A$
$T_A = 86.6°C$ = thermal run-away temperature.

Since worst condition values were used throughout, the circuit can safely be used to 86°C.

Calculation of Thermal Run-away Temperature
FIGURE 102

The major problem encountered in low temperature operation is the reduction of h_{FE}. Figure 103 shows the variation of h_{FE} for the 2N525 indicating that h_{FE} drops about 50% from its 25°C value when $T_J = -55°C$. Most transistors show approximately this variation in h_{FE}.



CURRENT GAIN (h_{FE}) VS TEMPERATURE NORMALIZED TO 25°C

FIGURE 103

POWER DISSIPATION

As with most electrical components, the transistor's range of operating conditions is limited by the transistor power dissipation.

Because the transistor is capable of a very low V_{CE} when it is in saturation it is possible to use load lines which exceed the maximum rated dissipation during the switching transient, but do not exceed it in the steady state. Such load lines can be used safely if the junction temperature does not rise to the runaway temperature during the switching transient. If the transient is faster than the thermal time constant of the junction, the transistor case may be considered to be an infinite heatsink. The junction temperature rise can then be calculated on the basis of the infinite heatsink derating factor. Since the thermal mass of the junctions is not considered, the calculation is conservative.

In some applications there may be a transient over-voltage applied to transistors when power is turned on or when circuit failure occurs. If the transistor is manufactured to high reliability standards, the maximum voltages may be exceeded provided the dissipation is kept within specifications. While quality alloy transistors and grown junction transistors can tolerate operation in the breakdown region, low quality alloy transistors with irregular junctions should not be used above the maximum voltage ratings.

Quality transistors can withstand much abuse. In experimental work, a 2N43 was operated at a peak power of 15 watts and a peak current of 0.5 amperes with no change in characteristics. 2N396 Transistors in an avalanche mode oscillator were operated at peak currents of one ampere. 3N37 Tetrodes rated at 50 milliwatts and 25 milliamperes maximum were operated at a peak power of one watt and a peak current of 200 milliamperes without change in characteristics. Standard production units however should be operated within ratings to ensure consistent circuit performance and long life.

It is generally desirable to heatsink a transistor to lower its junction temperature since life expectancy as well as performance decreases at high temperatures. Heat sinks also minimize thermal fatigue problems, if any exist.

SATURATION

A transistor is said to be in saturation when both junctions are forward biased. Looking at the common emitter collector characteristics shown in Figure 104(a) the saturation region is approximately the region below the knee of the curves, since h_{FE}

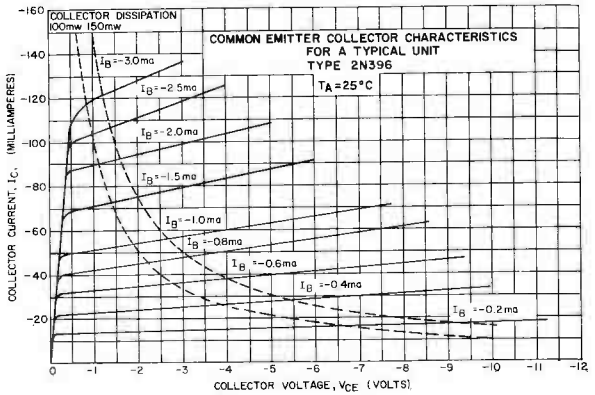


FIGURE 104(A)

usually falls rapidly when the collector is forward biased. Since all the characteristic curves tend to become superimposed in the saturation region, the slope of the curves is called the saturation resistance. If the transistor is unsymmetrical electrically — and most transistors are unsymmetrical — then the characteristics will not be directed towards the zero coordinates but will be displaced a few millivolts from zero. For ease of measurement, generally the characteristics are assumed to converge on zero so that the saturation resistance is $r_s = \frac{V_{CE}(sat)}{I_C}$.

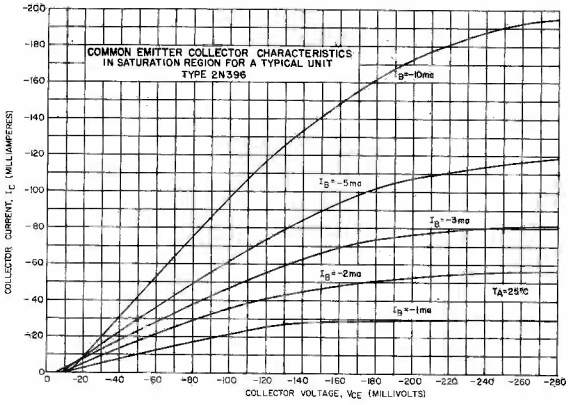
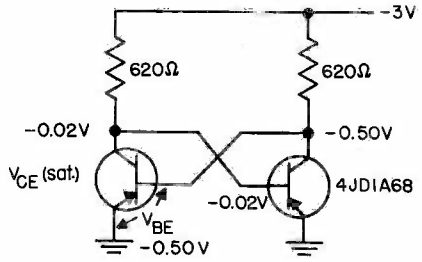


FIGURE 104(B)

While the characteristic curves appear superimposed, an expanded scale shows that $V_{CE}(sat)$ depends on I_B for any given I_C. The greater I_B is made, the lower $V_{CE}(sat)$ becomes until I_B is so large that it develops an appreciable voltage across the ohmic emitter resistance and in this way increases $V_{CE}(sat)$. In most cases the saturation voltage, $V_{CE}(sat)$, is specified rather than the saturation resistance. Figure 104(b) showing the collector characteristics in the saturation region, illustrates the small voltage off-set due to asymmetry and the dependence of r_s on I_B. Note also that r_s is a low resistance to both AC and DC.



DIRECT COUPLED TRANSISTOR LOGIC (DCTL) FLIP-FLOP
FIGURE 105

Some circuits have been designed making specific use of saturation. The direct coupled transistor logic (DCTL) flip-flop shown in Figure 105 utilizes saturation. In saturation $V_{CE}(sat)$ can be so low that if this voltage is applied between the base and emitter of another transistor, as in this flip-flop, there is insufficient forward bias to cause this transistor to conduct appreciably. The extreme simplicity of the circuit

is self evident and is responsible for its popularity. However, special requirements are placed on the transistors. The following are among the circuit characteristics:

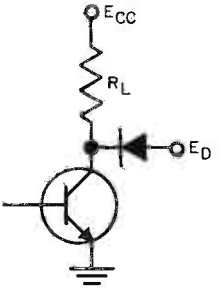
First, the emitter junction is never reverse biased permitting excessive current to flow in the off transistor at temperatures above 40°C in germanium. In silicon, however, operation to 150°C has proved feasible.

Second, saturation is responsible for a storage time delay, slowing up circuit speed. In the section on transient response we see the importance of drawing current out of the base region to increase speed. In DCTL, this current results from the difference between $V_{CE}(sat)$ and V_{BE} of a conducting transistor. To increase the current, $V_{CE}(sat)$ should be small and r'_b should be small. However, if one collector is to drive more than one base, r'_b should be relatively large to permit uniform current sharing between bases since large base current unbalance will cause large variations in transient response resulting in circuit design complexity.

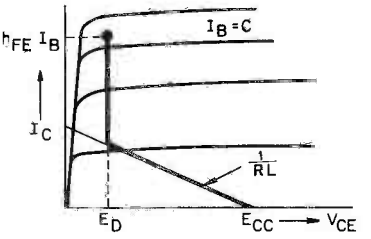
Third, since $V_{CE}(sat)$ and V_{BE} differ by less than .3 volt, in germanium, stray voltage signals of this amplitude can cause faulty performance. While stray signals can be minimized by careful circuit layout, this leads to equipment design complexity. Silicon transistors with a .7 volt difference between $V_{CE}(sat)$ and V_{BE} are less prone to being turned on by stray voltages but are still susceptible to turn off signals. This is somewhat compensated for in transistors with long storage time delay since they will remain on by virtue of the stored charge during short turn-off stray signals. This leads to conflicting transistor requirements — long storage time for freedom from noise; short storage time for circuit speed.

Another application of saturation is saturated flip-flops of conventional configuration. Since $V_{CE}(sat)$ is generally very much less than other circuit voltages, saturating the transistors permits the assumption that all three electrodes are nearly at the same potential making circuit voltages independent of transistor characteristics. This yields good temperature stability, and good interchangeability. The stable voltage levels are useful in generating precise pulse widths with monostable flip-flops. The section on flip-flop design indicates the ease with which saturated circuits can be designed.

In general, the advantages of saturated switch design are: (a) simplicity of circuit design, (b) well defined voltage levels, (c) fewer parts required than in non-saturating circuits, (d) low transistor dissipation when conducting, and (e) immunity to short stray voltage signals. Against this must be weighed the reduction in circuit speed. Speed is affected in a number of ways: (a) much higher trigger power is required to turn off a saturated transistor than an unsaturated one, (b) since $V_{CE}(sat)$, h_{FE} and V_{BE} all vary markedly with temperature, circuit speed also depends on temperature.



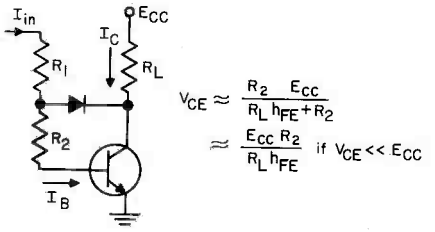
DIODE COLLECTOR CLAMPING CIRCUIT TO AVOID SATURATION



COLLECT CHARACTERISTICS SHOWING LOAD LINE AND OPERATING POINT PATH

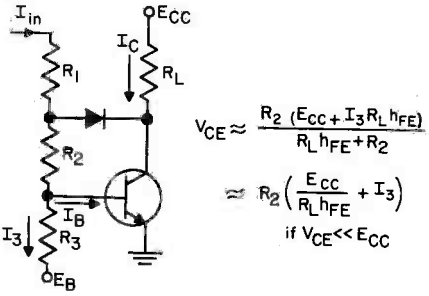
Collector voltage clamp
FIGURE 106

A number of techniques are used to avoid saturation. The simplest is shown in Figure 106. The diode clamps the collector voltage so that it cannot fall below the base voltage to forward bias the collector junction. Response time is not improved appreciably over the saturated case since I_C is not clamped but rises to $h_{FE}I_B$. With typical variations of I_B and h_{FE} with temperature and life for a standard transistor, I_C may vary by as much as 10:1. Care should be taken to ensure that the diode prevents saturation with the highest I_C. When the transistor is turned off, I_C must fall below the value given by $(E_{CC}-E_D)/R_L$ before any change in collector voltage is observed. The time required can be determined from the fall time equations in the section on transient response. The diode can also have a long recovery time from the high currents it has to handle. This can further increase the delay in turning off.



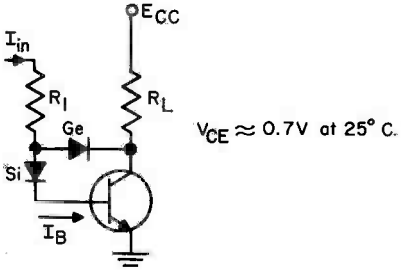
Collector current clamp without bias supply

FIGURE 107 (A)



Collector current using bias supply

FIGURE 107 (B)



Collector current clamp using silicon and germanium diodes

FIGURE 107 (C)

A much better way of avoiding saturation is to control I_B in such a way that I_C is just short of the saturation level. This can be achieved with the circuit of Figure 107(a). The diode is connected between a tap on the base drive resistor and the collector. When the collector falls below the voltage at the tap, the diode conducts diverting base current into the collector, preventing any further increase in I_C. The voltage drop across R_2 is approximately I_CR_2/h_{FE} since the current in R_2 is I_B. Since the voltage drop across the diode is approximately the same as the input voltage to the transistor, V_{CE} is approximately I_CR_2/h_{FE}. It is seen that if the load decreases (I_C is reduced) or h_{FE} becomes very high, V_{CE} decreases towards saturation. Where the change in h_{FE} is known and the load is relatively fixed, this circuit prevents saturation.

To avoid the dependence of V_{CE} on I_C and h_{FE}, R_3 may be added as in Figure 107(b). By returning R_3 to a bias voltage, an additional current is drawn through R_2. Now V_{CE} is approximately $(\frac{I_C}{h_{FE}} + I_3)\, R_2$. I_3 can be chosen to give a suitable minimum V_{CE}.

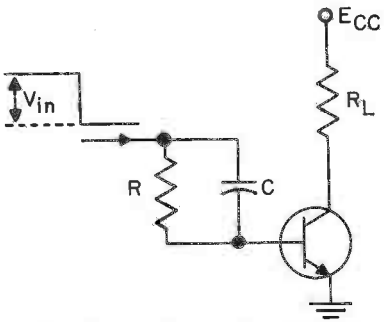
The power consumed by R_3 can be avoided by using the circuit of Figure 107(c). The silicon diode replaces R_2. Since the silicon diode has a forward voltage drop of approximately .7 volts over a considerable range of current, it acts as a constant voltage source making V_{CE} approximately .7 volts. If considerable base drive is used, it may be necessary to use a high conductance germanium diode to avoid momentary saturation as the voltage drop across the diode increases to handle the large base drive current.

In applying the same technique to silicon transistors with low saturation resistance, it is possible to use a single germanium diode between the collector and base. While this permits V_{CE} to fall below V_{BE}, the collector diode remains essentially non-conducting since the .7 volt forward voltage necessary for conduction cannot be reached with the germanium diode in the circuit.

The diode requirements are not stringent. The silicon diode need never be back biased, consequently, any diode will be satisfactory. The germanium diode will have to withstand the maximum circuit V_{CE}, conduct the maximum base drive with a low forward voltage and switch rapidly under the conditions imposed by the circuit, but these requirements are generally easily met.

Care should be taken to include the diode leakage currents in designing these circuits for high temperatures. All the circuits of Figure 107 permit large base drive currents to enhance switching speed, yet they limit both I_B and I_C just before saturation is reached. In this way, the transistor dissipation is made low and uniform among transistors of differing characteristics.

It is quite possible to design flip-flops which will be non-saturating without the use of clamping diodes by proper choice of components. The resulting flip-flop is simpler than that using diodes but it does not permit as large a load variation before malfunction occurs. The design procedure for an unclamped non-saturating flip-flop can be found in *Transistor Circuit Engineering* by R. F. Shea, et al (Wiley).

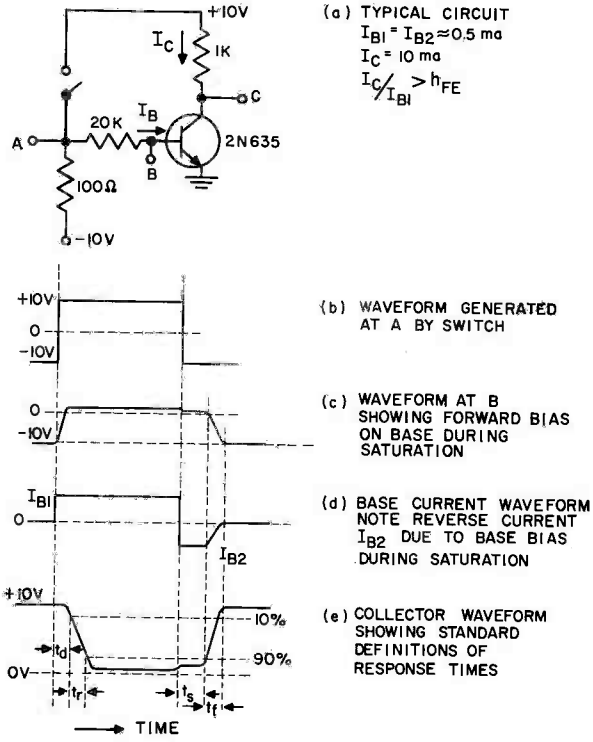


Stored neutralization by capacitor
FIGURE 108

Another circuit which is successful in minimizing storage time is shown in Figure 108. If the input is driven from a voltage source, it is seen that if the input voltage and capacitor are appropriately chosen, the capacitor charge can be used to neutralize the stored charge, in this way avoiding the storage time delay. In practical circuits, the RC time constant in the base necessary for this action limits the maximum pulse repetition rate.

TRANSIENT RESPONSE TIME

The speed with which a transistor switch responds to an input signal depends on the load impedance, the gain expected from the transistor, the operating conditions just prior to the input signal, as well as on the transistor's inherent speed. The following discussion will assume that the collector load resistance is sufficiently small that $2\pi R_L C_c f_\alpha << 1$ where C_c is the collector capacitance. If this is not the case, all the response time equations must be multiplied by the correction factor $(1 + 2\pi R_L C_c f_\alpha)$.



Transient response

FIGURE 109

Let us consider the simple circuit of Figure 109(a). If we close and open the switch to generate a pulse as shown in 109(b), we will obtain the other waveforms shown in the figure. When the switch closes, current flows through the 20K resistor to turn on the transistor. However there is a delay before collector current can begin to flow since the 20K must discharge the emitter capacitance which was charged to −10 volts prior to closing the switch. Time must also be allowed for the emitter current to diffuse across the base region. A third factor adding to the delay time is the fact that at low emitter current densities current gain and frequency response decrease. The total delay from all causes is called the "delay time" and is measured conventionally from the beginning of the input pulse to the 10% point on the collector waveform as shown in Figure 109(e). Delay time can be decreased by reducing the bias voltage across the emitter capacitance, and by reducing the base drive resistor in order to reduce the charging time constant. At high emitter current densities, delay time becomes negligible. Figure 110 shows typical delay times for the 2N396 transistor.

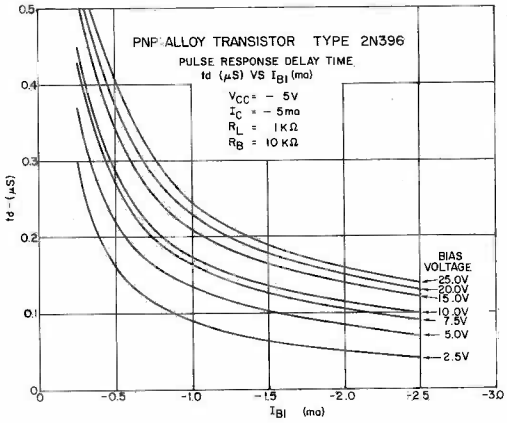
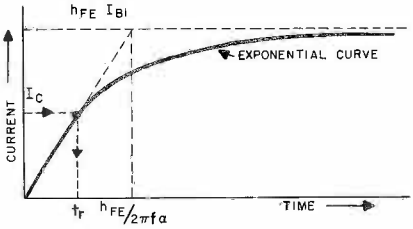


FIGURE 110

The rise time refers to the turn-on of collector current. By basing the definition of rise time on current rather than voltage it becomes the same for NPN and PNP transistors. The collector voltage change may be of either polarity depending on the transistor type. However, since the voltage across the collector load resistor is a measure of collector current, it is customary to discuss the response time in terms of the collector voltage. The theoretical analysis of rise time suggests that a single exponential curve as defined in Figure 111 fits the experimental results.



GRAPHICAL ANALYSIS OF RISE TIME
SYMBOLS DEFINED IN FIGURE 109
THE INTERCEPT OF I_C AND THE CURVE GIVES t_r.

FIGURE 111

If the load resistor R_L in Figure 109(a) is small enough that a current, $h_{FE}I_{B1}$, through it will not drive the transistor into saturation, the collector current will rise exponentially to $h_{FE}B_{B1}$ with a time constant, $h_{FE}/2\pi f_\alpha$. However, if R_L limits the current to less than $h_{FE}I_{B1}$, the same exponential response will apply except that the curve will be terminated at $I_C = \frac{V_{CC}}{R_L}$. Figure 111 illustrates the case for $I_C \approx h_{FE}I_{B1}/2$. Note that the waveform will no longer appear exponential but rather almost linear. This curve can be used to demonstrate the roles of the circuit and the transistor in determining rise time. For a given h_{FE} and f_α, it is seen that increasing $h_{FE}I_{B1}/I_C$ will decrease rise time by having I_C intersect the curve closer to the origin. On the other hand, for a given I_{B1} and I_C, speed will be proportional to f_α but nearly independent of h_{FE} since its effect on the time constant is balanced by its effect on the curve amplitude. A useful expression for rise time is $t_r = I_C/I_{B1}\ 2\pi f_\alpha$. It is valid for $I_C/I_B < h_{FE}/5$. Since this

analysis assumes that h_{FE} and f_α are the same for all operating points the calculated results will not fit experimental data where these assumptions are invalid. Figure 112 shows that the rise time halves as the drive current doubles, just as the expression for t_r suggests. However the calculated value for t_r is in error by more than 50%. This shows that even though the calculations may be in error, if the response time is specified for a circuit, it is possible to judge fairly accurately how it will change with circuit modifications using the above equations.

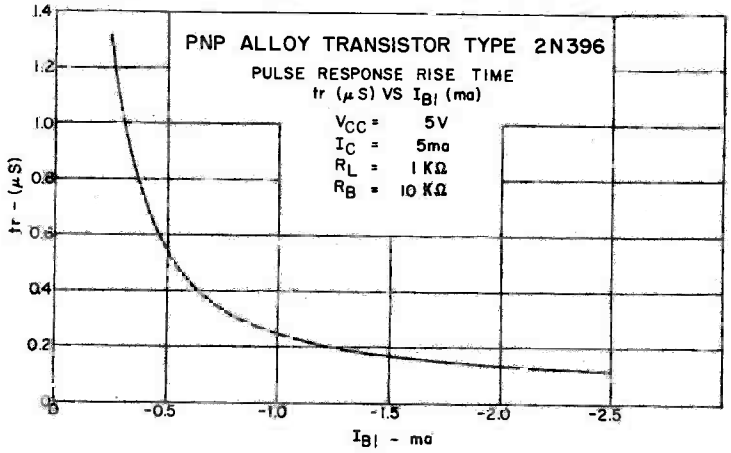
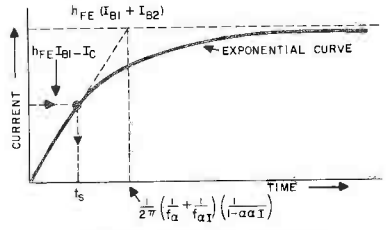


FIGURE 112

Storage time is the delay a transistor exhibits before its collector current starts to turn off. In Figure 109, R_B and R_L are chosen so that R_L rather than h_{FE} will limit the collector current. The front edge of the collector waveform, Figure 109(e), shows the delay time followed by the nearly linear risetime. When the collector voltage falls below the base voltage, the base to collector diode becomes forward biased with the result that the collector begins emitting. By definition, the transistor is said to be in saturation when this occurs. This condition results in a stored charge of carriers in the base region. Since the flow of current is controlled by the carrier distribution in the base, it is impossible to decrease the collector current until the stored carriers are removed. When the switch is opened in Figure 109, the voltage at A drops immediately to —10 volts. The base voltage at B however cannot go negative since the transistor is kept on by the stored carriers. The resulting voltage across R_B causes the carriers to flow out of the base to produce a current I_{B2}. This is illustrated in Figure 109(c) and 109(d). As soon as the stored carriers are swept out, the transistor starts to turn off; the base voltage dropping to —10 volts and the base current decreasing to zero. The higher I_{B1} is, the greater the stored charge; the higher I_{B2} is, the faster they are swept out. Since both junctions are forward biased during storage time, the inverse characteristics of the transistor are involved. The inverse characteristics are obtained by interchanging the collector and emitter connections in any test circuit. They are identified by the subscript I following the parameter, e.g., h_{FEI} is the inverse DC beta. Figure 113 shows a curve which is useful for calculating storage time graphically. The maximum value is $h_{FE}(I_{B1}+I_{B2})$ where I_{B2} is given the same sign as I_{B1}, ignoring the fact it flows in the opposite direction. The time constant of the curve involves the forward and inverse current gain and frequency cut-off. The storage time corresponds to the time required to reach the current $h_{FE}I_{B1}-I_C$. It can be seen that for a given frequency response, high h_{FE} gives long storage time. The storage time also decreases as I_{B2} is increased or I_{B1} is decreased.



GRAPHICAL ANALYSIS OF STORAGE TIME.
THE INTERCEPT OF $(h_{FE}\,I_{B1}-I_C)$ AND THE CURVE GIVES t_s

FIGURE 113

The time constant for a very unsymmetrical transistor is approximately $\frac{h_{FEI}+1}{2\pi f_{\alpha I}}$. It is seen that the generally specified normal h_{FE} and f_α are of little use in determining storage time. For a symmetrical transistor, the time constant is approximately $\frac{h_{FE}+1}{2\pi f_\alpha}$. It is possible for a symmetrical transistor to have a longer storage time than

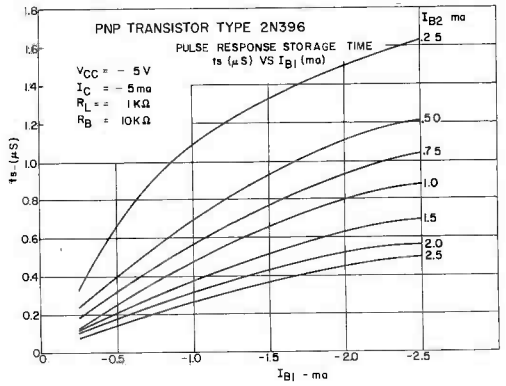
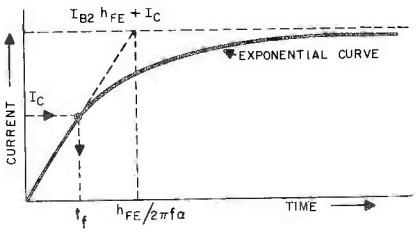


FIGURE 114

an unsymmetrical transistor with the same h_{FE} and f_α. Figure 114 shows the dependence of storage time on I_{B1} and I_{B2} for the 2N396 transistor.



GRAPHICAL ANALYSIS OF FALL TIME
THE INTERCEPT OF I_C AND THE CURVE GIVES t_f.

FIGURE 115

The collector current fall time can be analyzed in much the same manner. Figure 115 indicates the exponential curve of amplitude $I_C + h_{FE}I_{B2}$, and a time constant,

$h_{FE}/2\pi f_\alpha$. The fall time is given by the time it takes the exponential to reach I_C. If $h_{FE}I_{B2} >> I_C$, fall time is given by the expression,

$$t_F = \frac{1}{2\pi f_\alpha} \frac{h_{FE}\, I_C/I_{B2}}{h_{FE} + I_C/I_{B2}}$$

As h_{FE} becomes large, this expression reduces to,

$$t_F = \frac{1}{2\pi f_\alpha} \frac{I_C}{I_{B2}}$$

which is identical to the expression for t_r except that I_{B2} replaces I_{B1}. Figure 116 shows typical fall time measurements for a 2N396.

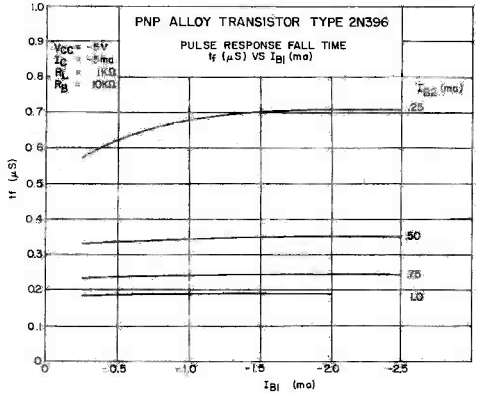


FIGURE 116

FLIP-FLOP DESIGN PROCEDURES

The bistable Eccles-Jordan circuit or flip-flop is a building block for counters, shift registers, data storage and control machinery. At the outset, the designer has the choice of using saturating or non-saturating circuits. If he chooses saturating circuits, the design becomes very straightforward.

SATURATING FLIP-FLOPS

The simplest flip-flop possible is shown in Figure 105, however, for standard transistor types the circuit in Figure 117(a) is preferable at moderate temperatures. We shall refer to the conducting and non-conducting transistors as the on and off

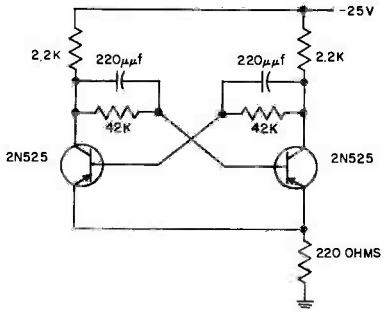


FIGURE 117(A)

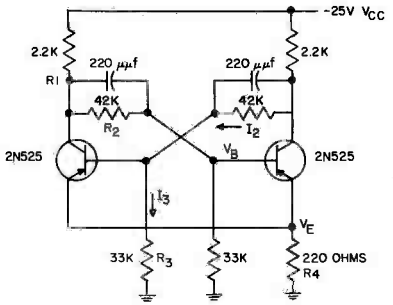
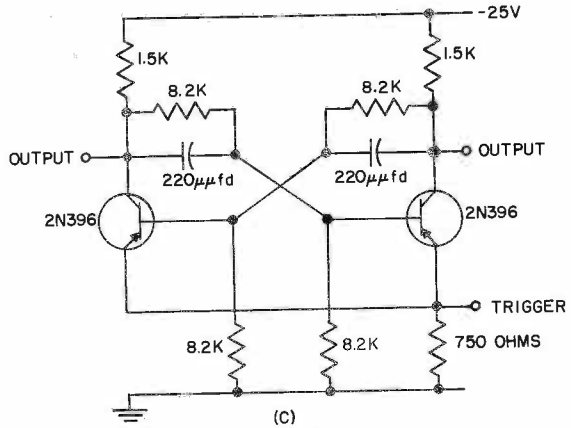


FIGURE 117(B)

SATURATED FLIP-FLOPS

transistors respectively. For stability, the circuit depends on the low collector to emitter voltage of the saturated on transistor to reduce the base current of the off transistor to a point where the circuit gain is too low for regeneration. The 220Ω emitter resistor could be removed if emitter triggering is not used. By adding resistors from base to ground as in Figure 117(b), the off transistor has both junctions reverse biased for greater stability. While the 33K resistors divert some of the formerly available base current, operation no longer depends on a very low saturation voltage consequently less base current may be used. Adding the two resistors permits stable operation beyond 50°C ambient temperature.



SATURATED FLIP-FLOP
FIGURE 117 (C)

The circuit in Figure 117(c) is stabilized to 100°C. The price that is paid for the stability is (1) smaller voltage change at the collector, (2) more battery power consumed, (3) more trigger power required, (4) a low I_{co} transistor must be used. The capacitor values depend on the trigger characteristics and the maximum trigger repetition rate as well as on the flip-flop design.

By far, the fastest way to design saturating flip-flops is to define the collector and emitter resistors by the current and voltage levels generally specified as load requirements. Then assume a tentative cross-coupling network. With all components specified, it is easy to calculate the on base current and the off base voltage. For example, the circuit in Figure 117(b) can be analyzed as follows. Assume $V_{BE} = .3$ volt and $V_{CE} = .2$ volt when the transistor is on. Also assume that $V_{EB} = .2$ volts will maintain the off transistor reliably cut-off. Transistor specifications are used to validate the assumptions.

I. Check for the maximum temperature of stability.

$$V_E = \frac{R_4 V_{CC}}{R_1 + R_4} = \frac{220}{2200 + 220}(25) = 2.3 \text{ volts}$$

$$V_{C\,on} = V_E + V_{CE\,on} = 2.3 + .2 = 2.5 \text{ volts}$$

Assuming no I_{co}, the base of the off transistor can be considered connected to a potential,

$$V'_B = V_{C\,on}\frac{R_3}{R_2 + R_3} \text{ through a resistor } R'_B = \frac{R_2 R_3}{R_2 + R_3}$$

$$V'_B = \frac{(2.5)\,(33K)}{(42K + 33K)} = 1.1 \text{ volts}$$

$$R'_B = \frac{(33K)\,(42K)}{75K} = 18.5K$$

The I_{CO} of the off transistor will flow through R'_B reducing the base to emitter potential. If the I_{CO} is high enough, it can forward bias the emitter to base junction causing the off transistor to conduct. In our example, $V_E = 2.3$ volts and $V_{EB} = .2$ volts will maintain off conditions. Therefore, the base potential can rise from 1.1 volts to 2.1 volts (2.3 — .2) without circuit malfunction. This potential is developed across R'_B by $I_{CO} = \frac{2.1 - 1.1}{18.5K} = 54\ \mu a$. A germanium transistor with $I_{CO} = 10\ \mu a$ at 25°C will not exceed 54 μa at 50°C. If a higher operating temperature is required, R_2 and R_3 may be decreased and/or R_4 may be increased.

II. Check for sufficient base current to saturate the on transistor.

$$V_{B\,on} = V_E + V_{BE\,on} = 2.3 + .3 = 2.6 \text{ volts}$$

The current through $R_3 = I_3 = \frac{2.6v}{33K} = .079$ ma

The current through R_1 and R_2 in series is $I_2 = \frac{V_{CC} - V_{B\,on}}{R_1 + R_2} = \frac{25 - 2.6}{42K + 2.2K} = .506$ ma

The available base current is $I_B = I_2 - I_3 = .43$ ma

The collector current is $I_C = \frac{V_{CC} - V_{C\,on}}{R_1} = \frac{25 - 2.5}{2.2K} = 10.25$ ma

The transistor will be in saturation if h_{FE} at 10 ma is greater than

$$\frac{I_C}{I_B} = \frac{10.25}{.43} = 24$$

If this circuit were required to operate to −55°C, allowance must be made for the reduction of h_{FE} at low temperatures. The minimum allowable room temperature h_{FE} should be doubled, or h_{FE} min = 48.

Generally it is not necessary to include the effect of I_{CO} flowing through R_1 when calculating I_2 since at temperatures where I_{CO} subtracts from the base drive it simultaneously increases h_{FE}. If more base drive is required, R_2 and R_3 may be decreased. If their ratio is kept constant, the off condition will not deteriorate, and so need not be rechecked.

III. Check transistor dissipation to determine the maximum junction temperature.

The dissipation in the on transistor is

$$V_{BE\,on} I_B + V_{CE\,on} I_C = \frac{(.3)(.43)}{1000} + \frac{(.2)(10.25)}{1000} = 2.18 \text{ mw}$$

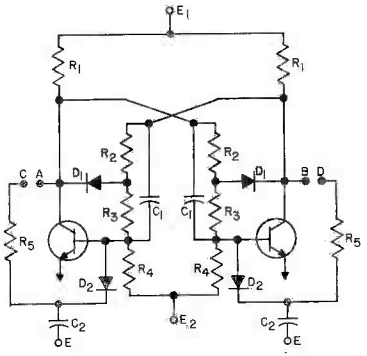
The dissipation in the off transistor resulting from the maximum I_{CO} is

$$V_{CB} I_{CO} \approx \frac{(25)(55)}{10^6} = 1.4 \text{ mw}$$

Generally the dissipation during the switching transient can be ignored at speeds justifying saturated circuitry. In both transistors the junction temperature is within 1°C of the ambient temperature if transistors in the 2N394-97 or 2N524-27 series are used.

NON-SATURATED FLIP-FLOP DESIGN

The abundance of techniques to prevent saturation makes a general design procedure impractical if not impossible. While it is a simple matter to design a flip-flop as shown above, it becomes quite tedious to check all the worst possible combinations of component change to ensure manufacturability and long term reliability. Often the job is assigned to a computer which calculates the optimum component values and tolerances. While a number of flip-flop design procedures have been published, they generally make simplifying assumptions concerning leakage currents and the voltages developed across the conducting transistors.



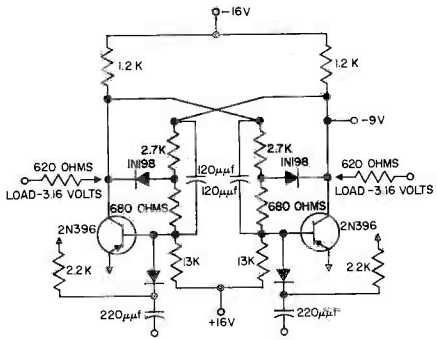
CIRCUIT CONFIGURATION FOR NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

Characteristics:

- Trigger input at points E
- Trigger steering by D_2 and R_5
- Collector clamping by D_1 and R_3
- Connect points A, B, C, D, E as shown in Figure 119 to get counter or shift register operation
- C1 and C2 chosen on basis of speed requirements

FIGURE 118(A)

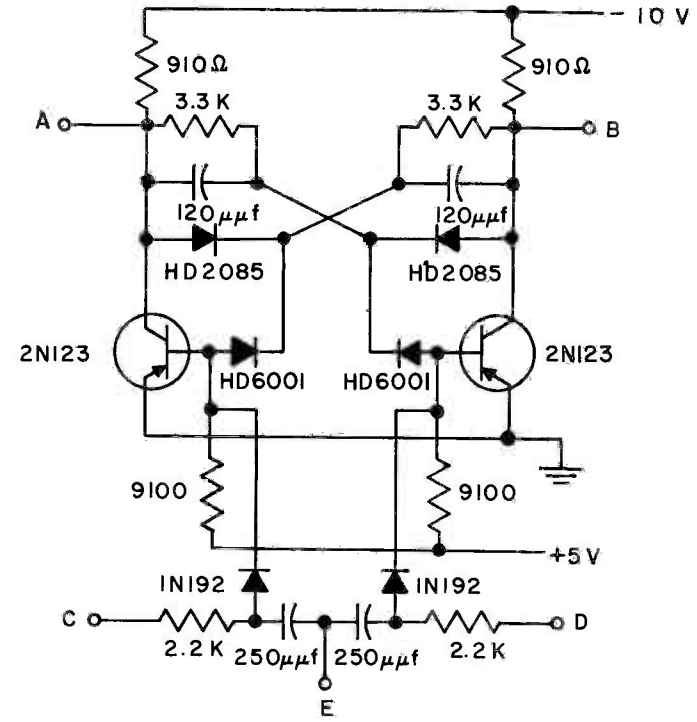
The design procedure described here is for the configuration in Figure 118(a). No simplifying assumptions are made but all the leakage currents and all the potentials are considered. The design makes full allowance for component tolerances, voltage fluctuations, and collector output loading. The anti-saturation scheme using one resistor (R3) and one diode (D1) was chosen because of its effectiveness, low cost and simplicity. The trigger gating resistors (R5) may be returned to different collectors to get different circuit functions as shown in Figure 119. This method of triggering offers the trigger sensitivity of base triggering and the wide range of trigger amplitude permissible in collector triggering. The derivation of the design procedure would require much space, therefore for conciseness, the procedure is shown without any substantiation. The procedure involves defining the circuit requirements explicitly then determining the transistor and diode characteristics at the anticipated operating points. A few astute guesses of key parameters yield a fast solution. However, since the procedure deals with only one section of the circuit at a time, a solution is readily reached by cut and try methods without recourse to good fortune. A checking procedure permits verification of the calculations. The symbols used refer to Figure 118(a) or in some cases are used only to simplify calculations. A bar over a symbol denotes its maximum value; a bar under it, its minimum. The example is based on polarities associated with NPN transistors for clarity. The result is that only E_2 is negative. While the procedure is lengthly, its straightforward steps lend themselves to computation by technically unskilled personnel and the freedom from restricting assumptions guarantees a working circuit when a solution is reached. The circuit designed by this procedure is shown in Figure 118(b).



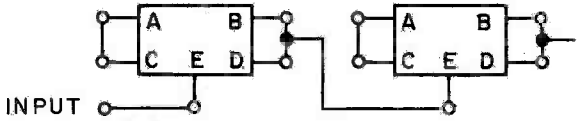
NON-SATURATED FLIP-FLOP

FIGURE 118(B)

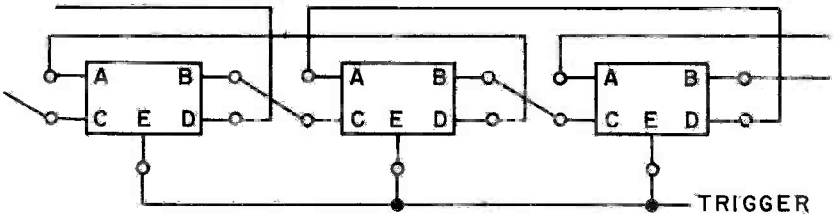
The same procedure can be used to analyze existing flip-flops of this configuration by using the design check steps.



(a) FLIP—FLOP



(b) INTER CONNECTION AS COUNTER



(c) INTERCONNECTION AS SHIFT REGISTER

500 KC COUNTER-SHIFT REGISTER FLIP-FLOP
FIGURE 119

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
	(A) Circuit Requirements and Device Characteristics		
1	Assume maximum voltage design tolerance	Δe	Let $\Delta e = \pm 5\%$
2	Assume maximum resistor design tolerance	Δr	Let $\Delta r = \pm 7\%$ (assuming $\pm 5\%$ resistors)
3	Assume maximum ambient temperature	T_A	Let $T_A = 40°C$
4	Assume maximum load current out of the off side	I_0	Let $I_0 = 1$ ma
5	Assume maximum load current into the on side	I_1	Let $I_1 = 0.2$ ma
6	Estimate the maximum required collector current in the on transistor	I_1	Let $I_1 \leq 17.5$ ma
7	Assume maximum design I_{CO} at 25°C		From spec sheet $I_{CO} < 6$ μa
8	Estimate the maximum junction temperature	T_J	Let $T_J = 60°C$
9	Calculate I_{CO} at T_J assuming I_{CO} doubles every 10°C or $I_{CO_{T_J}} = I_{CO_{25}} e^{.07(T_J-25)}$	I_2	$I_2 = 6e^{.07T_J} = 71$ μa; Let $I_2 = 100$ μa
10	Assume the maximum base leakage current is equal to the maximum I_{CO}	I_3	Let $I_3 = 100$ μa
11	Calculate the allowable transistor dissipation		2N396 is derated at 2.5 mw/°C. The junction temperature rise is estimated as 20°C therefore 50 mw can be allowed. Let $P_C = 50$ mw
12	Estimate h_{FE} minimum taking into account low temperature degradation and specific assumed operating point	β_{min}	Let $\alpha_{min} = 0.94$ or $\beta_{min} = 15.67$
13	Estimate the maximum design base to emitter voltage of the "on" transistor	V_1	Let $V_1 = 0.35$ volts
14	Assume voltage logic levels for the outputs		Let the level separation be ≥ 7 volts

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
15	Choose the maximum collector voltage permissible for the "on" transistor	V_2	Let $V_2 \leq 2.0$ volts
16	Choose suitable diode types		Let all diodes be 1N198
17	Estimate the maximum leakage current of any diode	I_4	Maximum leakage estimated as ≤ 25 μa. Let $I_4 = 40$ μa at end of life
18	Calculate $I_5 = I_3 + I_4$	I_5	$40 + 100 = 140$ μa
19a	Choose the minimum collector voltage for the "off" transistor keeping in mind 14 and 15 above	V_3	Let $V_3 \geq 9.0$ volts
19b	Choose the maximum collector voltage for the "off" transistor	V_4	Let $V_4 \leq 13.0$ volts
20	Choose the minimum design base to emitter reverse bias to assure off conditions	V_5	Let $V_5 = 0.5$ volt
21a	Estimate the maximum forward voltage across the diodes	V_6	Let $V_6 = 0.8$ volt
21b	Estimate the minimum forward voltage	V_7	Let $V_7 = 0.2$ volt
22	Estimate the worst saturation conditions that can be tolerated.		
22a	Estimate the minimum collector voltage that can be tolerated	V_8	Let $V_8 = 0.1$ volt
22b	Estimate the maximum base to collector forward bias voltage that can be tolerated	V_9	Let $V_9 = 0.1$ volt
23a	Calculate $V_9 + V_7$	V_{10}	$2 + 0.2 = 2.2$ volts
23b	Calculate $V_2 + V_6$	V_{11}	$2 + 0.8 = 2.8$ volts
24a	Calculate $V_8 + V_7$	V_{12}	$0.1 + 0.2 = 0.3$ volt
24b	Calculate $V_3 + V_6$	V_{13}	$0.1 + 0.8 = 0.9$ volt
25	Calculate $V_8 + V_9$	V_{14}	$0.1 + 0.1 = 0.2$ volt

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
(B) Cut and Try Circuit Design			
1	Assume E_2	E_2	Let $E_2 = -16$ volts $\pm$ 5%; $\overline{E_2} = -15.2$ v; $\underline{E_2} = -16.8$ v
2a	Calculate $\frac{(1 + \Delta r)}{(1 - \Delta r)}$	K_1	$\frac{1.07}{0.93} = 1.15$
2b	Calculate $\frac{(1 + \Delta e)}{(1 - \Delta e)}$	K_2	$\frac{1.05}{0.95} = 1.105$
2c	Calculate $\frac{I_1}{\beta_{min}}$	K_3	$\frac{17.5}{15.67} = 1.117$ ma
2d	Calculate $I_2 + I_0 + 2I_4$	K_4	$0.1 + 1.0 + 0.08 = 1.18$ ma
2e	Calculate $\frac{V_6 - V_9}{V_8 + V_9 - \overline{E_2}}$	K_5	$\frac{0.8 - 0.1}{0.1 + 0.1 + 15.2} = 0.0454$
3	Calculate $\overline{R_4} \leq \frac{1}{K_3}\left[\frac{V_{10} - V_1}{K_1 K_5} - K_1 (V_1 - \underline{E_2})\right]$		$\frac{1}{1.117}\left[\frac{2.2 - 0.35}{(1.15)(0.0454)} - 1.15 (0.35 + 16.8)\right] = 14.03$ K
4	Choose R_4	R_4	Let $R_4 = 13$K $\pm$ 7%; $\overline{R_4} = 13.91$ K; $\underline{R_4} = 12.09$ K
5	Calculate $\underline{R_3} \geq K_5 \overline{R_4}$		$(0.0454)(13.91\text{K}) = 0.632$ K
6	Choose R_3	R_3	Let $R_3 = 0.68$ K $\pm$ 7%; $\overline{R_3} = 0.7276$ K; $\underline{R_3} = 0.6324$ K
7	Check R_3 by calculating $\overline{R_3} \leq \frac{\underline{R_4}(V_{10} - V_1)}{V_1 - \underline{E_2} + K_3 \underline{R_4}}$		$\frac{(12.09\text{ K})(2.2 - 0.35)}{0.35 + 16.8 + (1.117)(12.09)} = 0.730$ K; choice of R_3 satisfactory
8	Calculate $\frac{\overline{R_4}}{-V_5 - \overline{E_2} - I_5 \overline{R_4}}$	K_6	$\frac{13.91\text{ K}}{-0.5 + 15.2 - (0.14)(13.91)} = 1.091$ K/V

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
9	Calculate $\underline{R_2} \geq \dfrac{K_6 (V_2 + V_5) - \underline{R_3}}{1 - K_6 I_4}$		$\dfrac{(1.091)\ (2.0 + 0.5)\ \text{K} - 0.632\ \text{K}}{1 - (1.091)\ (0.04)} = 2.19\ \text{K}$
10	Choose R_2 — *If there are difficulties at this point, assume a different E_2.*	R_2	Let $R_2 = 2.7\ \text{K} \pm 7\%$; $\overline{R_2} = 2.889\ \text{K}$; $\underline{R_2} = 2.511\ \text{K}$
11	Calculate $\dfrac{K_1^2\ [V_3 - V_{12} + K_4\ \underline{R_2}]}{V_4 - V_{11}}$	K_7	$\dfrac{(1.15)^2[9.0 - 0.3 + (1.18)\ (2.511)]}{13.0 - 2.8} = 1.51$
12	Calculate $\overline{E_1} \leq \dfrac{K_7 V_4 - V_3}{K_7 - 1/K_2}$		$\dfrac{(1.51)\ (13.0) - 9.0}{1.51 - 1/1.105} = 17.63$ volts
13	Choose E_1	E_1	Let $E_1 = 16$ volts $\pm 5\%$; $\overline{E_1} = 16.8$ volts; $\underline{E_1} = 15.2$ volts
14	Calculate $\overline{R_1} \leq \dfrac{(\underline{E_1} - V_3)\ \underline{R_2}}{V_3 - V_{12} + K_4\ \underline{R_2}}$		$\dfrac{(15.2 - 9.0)\ (2.511)}{9.0 - 0.3 + (1.18)\ (2.511)} = 1.335\ \text{K}$
15	Calculate $\underline{R_1} \geq \dfrac{(\overline{E_1} - V_4)\ (\underline{R_2})}{V_4 - V_{11}}$		$\dfrac{(16.8 - 13.0)\ (2.889)}{13.0 - 2.8} = 1.077\ \text{K}$
16	Choose R_1	R_1	Let $R_1 = 1.2\ \text{K} \pm 7\%$; $\overline{R_1} = 1.284\ \text{K}$; $\underline{R_1} = 1.116\ \text{K}$
(C)	*Design Checks*		
1	Check "off" stability. Reverse bias voltage is given by: $V_{EB} \leq \overline{E_2} + \dfrac{\overline{R_4}}{\overline{R_4} + \underline{R_3} + \underline{R_2}}[V_2 - \overline{E_2} + I_4\ \underline{R_2} + I_5\ (\underline{R_2} + \underline{R_3})]$ Circuit stable if $V_{EB} \leq -V_5$	V_{EB}	$-15.2 + \dfrac{13.91}{17.05}$ $[2 + 15.2 + (0.04)\ (2.511) + (0.14)\ (3.14)] = -0.7$ volts The design value of V_5 was 0.5 volts. Therefore, the "off" condition is stable.
2	Check for non-saturation under the worst conditions. $V_{BE} \leq \overline{E_2} + \dfrac{\overline{R_4}\ (V_{13} - \overline{E_2})}{\overline{R_4} + \underline{R_2}}$ Circuit non-saturated if $V_{BE} \leq V_{14}$	V_{BE}	$-15.2 + \dfrac{13.91\ (0.9 + 15.2)}{14.54} = 0.19$ volts The design maximum of V_{14} was 0.2 volts.

NON-SATURATING FLIP-FLOP DESIGN PROCEDURE (CONTINUED)

STEP	DEFINITION OF OPERATION	SYMBOL	SAMPLE DESIGN FOR 2N396 TRANSISTOR
3	Check for stability. Calculate:		
3a	$R_A = \overline{R_1} + \overline{R_2}$	R_A	$1.284 + 2.889 = 4.173$ K
3b	$R_B = \overline{R_1} + \overline{R_2} + \overline{R_3} + \underline{R_4}$	R_B	$1.284 + 2.889 + .728 + 12.09 = 16.99$ K
3c	$R_C = \overline{R_3} + \underline{R_4}$	R_C	$.728 + 12.09 = 12.82$ K
3d	$E'_1 = \underline{E_1} - K_4 \overline{R_1}$	E'_1	$15.2 - (1.18)(1.284) = 13.68$ volts
3e	$R_D = \underline{R_1} + \overline{R_2} + \overline{R_3} + \overline{R_4}$	R_D	$1.116 + 2.889 + .728 + 13.91 = 18.643$ K
3f	$I_6 = \dfrac{R_D(\overline{E_1} - V_2) - \underline{R_1}[\overline{E_1} - \underline{E_2} - I_5\overline{R_4} - I_4(\overline{R_3} + \overline{R_4})]}{\underline{R_1}(R_D - \underline{R_1})}$	I_6	$\dfrac{18.64(16.8 - 2) - 1.116[16.8 + 16.8 - (0.14)(13.91)}{1.116(18.64 - 1.116)}$ $\dfrac{- (.04)(.728 + 13.91)]}{} = 12.34$ ma
3g	$I_7 = \dfrac{R_B}{R_A R_C}(E'_1 - V_{10}) - \dfrac{1}{R_C}(E'_1 - \underline{E_2})$	I_7	$\dfrac{16.99}{(4.173)(12.82)}(13.68 - 2.2) - \dfrac{(13.68 + 16.8)}{12.82} = 1.266$ ma
3h	$I_8 = \dfrac{I_1 + I_6 + I_7}{\beta_{min} + \underline{R_4}/R_C}$	I_8	$\dfrac{0.2 + 12.34 + 1.266}{15.67 + 12.09/12.82} = 0.831$ ma
3i	$V'_{BE} = \underline{E_2} + \dfrac{\underline{R_4}}{R_B}\left(1 + \dfrac{R_A}{R_C}\right)(E'_1 - \underline{E_2})$ $- \dfrac{\underline{R_4}}{R_C}(E'_1 - V_{10}) - I_8\dfrac{\underline{R_4}}{R_B}\left(\dfrac{R_A\underline{R_4}}{R_C} - R_A - \overline{R_3}\right)$	V'_{BB}	$-16.8 + \dfrac{12.09}{16.99}\left(1 + \dfrac{4.173}{12.818}\right)(13.683 + 16.8)$ $- \dfrac{12.09}{12.818}(13.683 - 2.2) - 0.831\dfrac{12.09}{16.99}$ $\left(\dfrac{(4.173)(12.09)}{12.818} - 4.173 - 0.7276\right) = .55$V .55V is greater than $V_1 = .35$V, therefore the design is satisfactory.

TRIGGERING

Flip-flops are the basic building blocks for many computer and switching circuit applications. In all cases it is necessary to be able to trigger one side or the other into conduction. For counter applications, it is necessary to have pulses at a single input make the two sides of the flip-flop conduct alternately. Outputs from the flip-flop must have characteristics suitable for triggering other similar flip-flops. When the counting period is finished, it is generally necessary to reset the counter by a trigger pulse to one side of all flip-flops simultaneously. Shift registers, and ring counters have similar triggering requirements.

In applying a trigger to one side of a flip-flop, it is preferable to have the trigger turn a transistor off rather than on. The off transistor usually has a reverse-biased emitter junction. This bias potential must be overcome by the trigger before switching can start. Furthermore, some transistors have slow turn on characteristics resulting in a delay between the application of the trigger pulse and the actual switching. On the other hand, since no bias has to be overcome, there is less delay in turning off a transistor. As turn-off begins, the flip-flop itself turns the other side on.

A lower limit on trigger power requirements can be determined by calculating the base charge required to maintain the collector current in the on transistor. The trigger source must be capable of neutralizing this charge in order to turn off the transistor. It has been determined that the base charge for a non-saturated transistor is approximately $Q_B = 1.22\ I_C/2\pi f_a$. The turn-off time constant is approximately $h_{FE}/2\pi f_a$. This indicates that circuits utilizing high speed transistors at low collector currents will require the least trigger power. Consequently, it may be advantageous to use high speed transistors in slow circuitry if trigger power is critical. If the on transistor was in saturation, the trigger power must also include the stored charge. The stored charge is given by

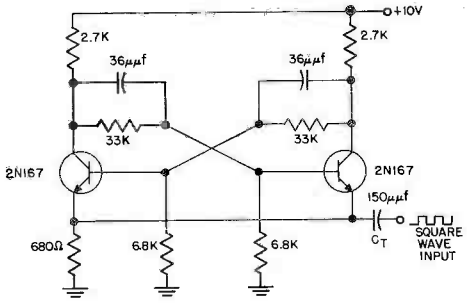
$$Q_S = \frac{1}{2\pi}\left(\frac{1}{f_a} + \frac{1}{f_{aI}}\right)\left(\frac{1}{1 - \alpha_N\alpha_I}\right)\left(I_{B1} - \frac{I_C}{h_{FE}}\right)$$

where the symbols are defined in the section on transient response time.

Generally, the trigger pulse is capacitively coupled. Small capacitors permit more frequent triggering but a lower limit of capacitance is imposed by base charge considerations. When a trigger voltage is applied, the resulting trigger current causes the charge on the capacitor to change. When the change is equal to the base charge just calculated, the transistor is turned off. If the trigger voltage or the capacitor are too small, the capacitor charge may be less than the base charge resulting in incomplete turn-off. In the limiting case $C = \frac{Q_B}{V_T}$. The speed with which the trigger turns off a transistor depends on the speed in which Q_B is delivered to the base. This is determined by the trigger source impedance and r'_b.

In designing counters, shift registers or ring counters, it is necessary to make alternate sides of a flip-flop conduct on alternate trigger pulses. There are so-called steering circuits which accomplish this. At low speeds, the trigger may be applied at the emitters as shown in Figure 120. It is important that the trigger pulse be shorter than the cross coupling time constant for reliable operation. The circuit features few parts and a low trigger voltage requirement. Its limitations lie in the high trigger current required.

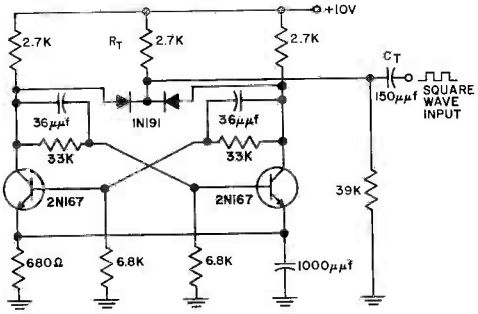
At this point, the effect of trigger pulse repetition rate can be analyzed. In order that each trigger pulse produce reliable triggering, it must find the circuit in exactly the same state as the previous pulse found it. This means that all the capacitors in the circuit must stop charging before a trigger pulse is applied. If they do not, the result



EMITTER TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 500 KCS WITH TRIGGER AMPLITUDE FROM 2V TO 12V

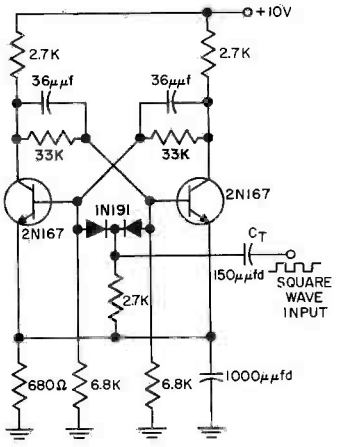
FIGURE 120

is equivalent to reducing the trigger pulse amplitude. The transistor being turned off presents a low impedance permitting the trigger capacitor to charge rapidly. The capacitor must then recover its initial charge through another impedance which is generally much higher. The recovery time constant can limit the maximum pulse rate.



COLLECTOR TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 1MC WITH TRIGGER AMPLITUDE FROM 4V TO 12V.

FIGURE 121

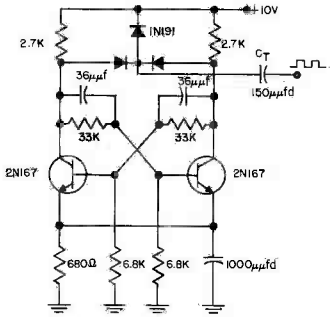


BASE TRIGGERING
MAXIMUM TRIGGER RATE EXCEEDS 1 MC WITH TRIGGER AMPLITUDE FROM 0.75 TO 3 VOLTS.

FIGURE 122

Steering circuits using diodes are shown in Figures 121 and 122. The collectors are triggered in 121 by applying a negative pulse. As a diode conducts during triggering, the trigger pulse is loaded by the collector load resistance. When triggering is accomplished, the capacitor recovers through the biasing resistor R_T. To minimize trigger loading, R_T should be large; to aid recovery, it should be small. To avoid the recovery problem mentioned above, R_T can be replaced by a diode as shown in 123. The diode's low forward impedance ensures fast recovery while its high back impedance avoids shunting the trigger pulse during the triggering period.

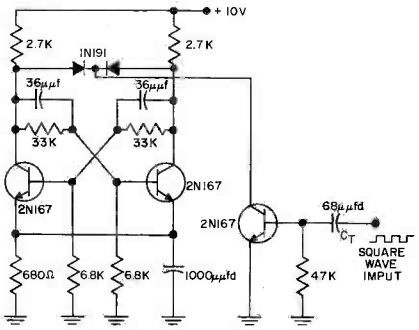
Collector triggering requires a relatively large amplitude low impedance pulse but has the advantage that the trigger pulse adds to the switching collector waveform to enhance the speed. Large variations in trigger pulse amplitude are also permitted.



COLLECTOR TRIGGERING

DIODE TO SUPPLY VOLTAGE REDUCES TRIGGER POWER AND EXTENDS MAXIMUM TRIGGER RATE.

FIGURE 123



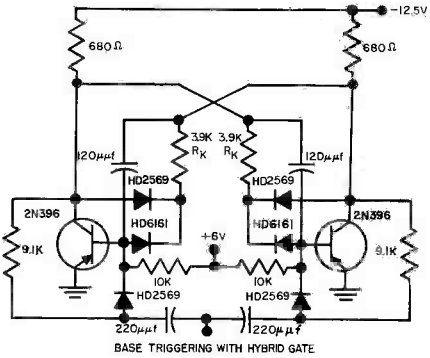
COLLECTOR TRIGGERING WITH TRIGGER AMPLIFIER

FOR IMC TRIGGER RATE LESS THAN 1 VOLT TRIGGER AMPLITUDE REQUIRED.

FIGURE 124

In designing a counter, it may be advantageous to design all stages identically the same to permit the economies of automatic assembly. Should it prove necessary to increase the speed of the early stages, this can be done by adding a trigger amplifier as shown in Figure 124, without any change to the basic stage.

Base triggering shown in Figure 122 produces steering in the same manner as collector triggering. The differences are quantitative with base triggering requiring less trigger energy but a more accurately controlled trigger amplitude. A diode can replace the bias resistor to shorten the recovery time.



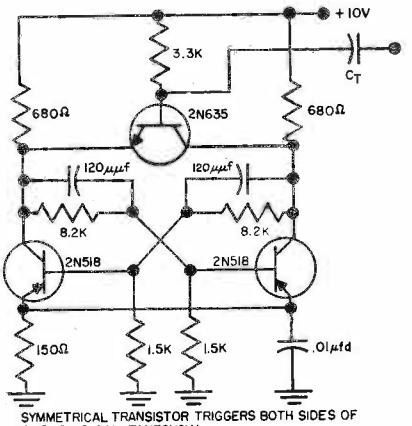
BASE TRIGGERING WITH HYBRID GATE

FIGURE 125

Hybrid triggering illustrated in Figure 125 combines the sensitivity of base triggering and the trigger amplitude variation of collector triggering. In all the other steering circuits, the bias potential was fixed, in this one the bias potential varies in order to more effectively direct the trigger pulse. By returning the bias resistor to the collector, the bias voltage is V_{CB}. For the conducting transistor, V_{CB} is much less than for the off transistor, consequently, the trigger pulse is directed to the conducting transistor. This steering scheme is particularly attractive if V_{CB} for the conducting transistor is very small as it is in certain non-saturating circuits such as shown in Figure 107.

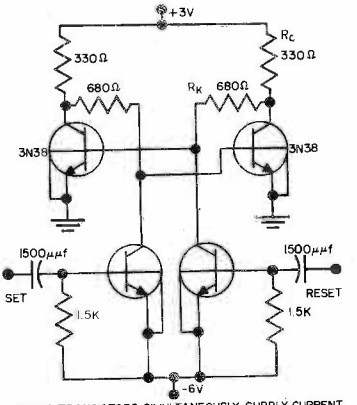
Care should be taken that the time constant C_TR_T does not limit the maximum counting rate. Generally R_T can be made approximately equal to R_K the cross-coupling resistor.

To design a shift register or a ring counter, it is only necessary to return R_T to the appropriate collector to achieve the desired switching pattern. The connections for the shift register are shown in Figure 119(a) and (b). A ring counter connection results from connecting the shift register output back to its input as shown in Figure 119(c).



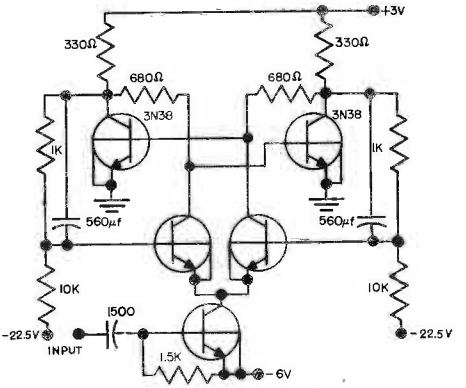
SYMMETRICAL TRANSISTOR TRIGGERS BOTH SIDES OF FLIP-FLOP SIMULTANEOUSLY.

FIGURE 126(A)



TRIGGER TRANSISTORS SIMULTANEOUSLY SUPPLY CURRENT TO TURN OFF ONE SIDE OF FLIP-FLOP AND TO DEVELOP A VOLTAGE ACROSS THE COLLECTOR LOAD ON THE OTHER SIDE.

FIGURE 126(B)



CIRCUIT OF FIGURE 126(b) WITH TRIGGER STEERING ADDED FOR COUNTER APPLICATION

TRIGGER CIRCUITS
USING TRIGGER POWER TO INCREASE SWITCHING SPEED
FIGURE 126(C)

By using transistors as trigger amplifiers, some circuits superpose the trigger on the output of the flip-flop so that an output appears even if the flip-flop is still in the transient condition. Figure 126(a) shows a symmetrical transistor used for steering. The transistor makes the trigger appear in opposite phase at the flip-flop collectors speeding up the transition. The circuit in Figure 126(b) can have R_C and R_K so chosen so that a trigger pulse will bring the collector of the transistor being turned on to ground even though the transistor may not have started conducting. The circuit in 126(b) may be converted to a steering circuit by the method shown in 126(c).

LOGIC

Large scale scientific computers, smaller machine control computers and electronic animals all have in common the facility to take action without any outside help when the situation warrants it. For example, the scientific computer recognizes when it has completed an addition, and tells itself to go on to the next part of the problem. A machine control computer recognizes when the process is finished and another part should be fed in. Electronic animals can be made to sense obstructions and change their course to avoid collisions. Mathematicians have determined that such logical operations can be described using the conjunctives AND, OR, AND NOT, OR NOT. Boolean algebra is the study of these conjunctives, the language of logic. Transistors can be used to accomplish logic operations. To illustrate this an example from automobile operation will be used.

Let us consider the interactions between the ignition switch, the operation of the motor and the oil pressure warning light. If the ignition is off, the motor and light will both be off. If the ignition is turned on, but the starter is not energized the warning lamp should light because the motor has not generated oil pressure. Once the motor is running, the ignition is on and the lamp should be off. These three combinations of ignition, motor and lamp conditions are the only possible combinations signifying proper operation. Note that the three items discussed have only two possible states each, they are on or off. This leads to the use of the binary arithmetic system, which has only two symbols corresponding to the two possible states. Binary numbers will be discussed later in the chapter.

	I	M	L	Result
1	0	0	0	✓
2	0	0	1	X
3	0	1	0	X
4	0	1	1	X
5	1	0	0	X
6	1	0	1	✓
7	1	1	0	✓
8	1	1	1	X

I = IGNITION
M = MOTOR
L = LAMP
R = RESULT
1 = ON
0 = OFF
✓ = ACCEPTABLE
X = UNACCEPTABLE
N = 3 = NO. OF VARIABLES
$2^N = 8$

Table of all possible combinations of ignition, motor and lamp conditions
FIGURE 127

To write the expressions necessary to derive a circuit, first assign letters to the variables, e.g., I for ignition, M for motor and L for lamp. Next assign the number one to the variable if it is on; assign zero if it is off. Now we can make a table of all possible combinations of the variables as shown in Figure 127. The table is formed by writing ones and zeros alternately down the first column, writing ones and zeros in series of two down the second; in fours down the third, etc. For each additional variable, double the number of ones or zeros written in each group. Only 2^N rows are written, where N is the number of variables, since the combinations will repeat if more rows are added. Indicate with a check mark in the result column if the combination represented in the row is acceptable. For example, combination 4 reads, the ignition is off and the motor is running and the warning light is on. This obviously is an unsatisfactory

situation. Combination 7 reads, the ignition is on and the motor is running and the warning light is off. This obviously is the normal situation while driving. If we indicate that the variable is a one by its symbol, and that it is a zero by the same symbol with a bar over it, and if we use the symbol plus (+) to mean "OR" and multiplication to mean "AND" we can write the Boolean equation $\overline{I}M\overline{L} + I\overline{M}L + IM\overline{L} = R$ where R means an acceptable result. The three terms on the left hand side are combinations 1, 6, and 7 of the table since these are the only ones to give a check mark in the result column. The plus signs indicate that any of the three combinations individually is acceptable. While there are many rules for simplifying such equations, they are beyond the scope of this book.

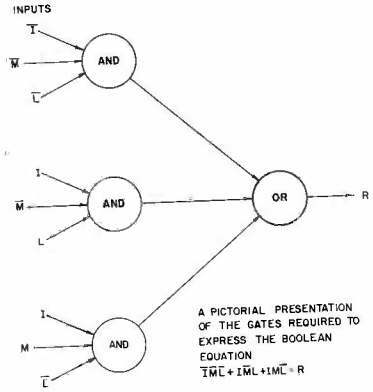


FIGURE 128

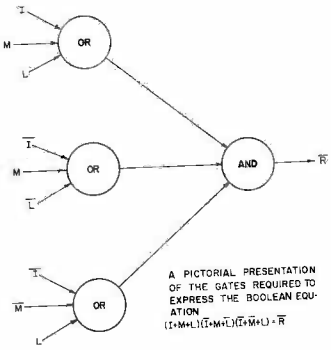


FIGURE 129

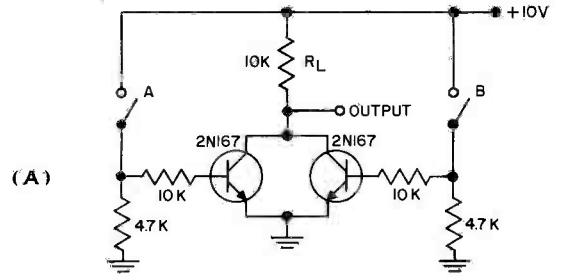
To express this equation in circuitry, two basic circuits are required. They are named gates because they control the signal passing through. An "AND" gate generates an output only if all the inputs representing the variables are simultaneously applied and an "OR" gate generates an output whenever it receives any input. Our equation translated into gates would be as shown in Figure 128. Only if all three inputs shown for an "AND" gate are simultaneously present will an output be generated. The output will pass through the "OR" gate to indicate a result. Note that any equation derived from the table can be written as a series of "AND" gates followed by one "OR" gate.

It is possible to rearrange the equation to give a series of "OR" gates followed by one "AND" gate. To achieve this, interchange all plus and multiplication signs, and remove bars where they exist and add them where there are none. This operation gives us,

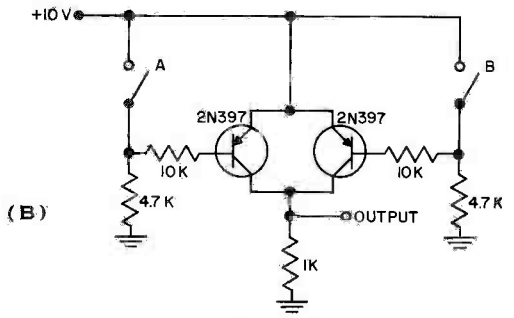
$$(I + M + L)\,(\overline{I} + M + \overline{L})\,(\overline{I} + \overline{M} + L) = \overline{R}$$

In ordinary language this means if any of the ignition or motor or lamp is on, and simultaneously either the ignition is off or the motor is on or the lamp is off, and simultaneously either the ignition is off or the motor is off or the lamp is on, then the result is unacceptable. Let us apply combination 4 to this equation to see if it is acceptable. The ignition is off therefore the second and third brackets are satisfied. The first bracket is not satisfied by the ignition because it requires that the ignition be on. However, the motor is on in combination 4, satisfying the conditions of the first bracket. Since the requirements of all brackets are met, an output results. Applying combination 7 to the equation we find that the third bracket cannot be satisfied since its conditions are the opposite of those in combination 7. Consequently, no output appears. Note that for this equation, an output indicates an unacceptable situation, rather than an acceptable one, as in the first equation. In gate form, this equation is shown in Figure 129.

Consider the circuits in Figure 130. The base of each transistor can be connected through a resistor either to ground or a positive voltage by operating a switch. In Figure 130(a) if both switches are open, both transistors will be non-conducting except for a small leakage current. If either switch A *or* switch B is closed, current will flow through R_L. If we define *closing* a switch as being synonymous with applying an input then we have an "OR" gate. When either switch is closed, the base of the transistor sees a positive voltage, therefore, in an "OR" gate the output should be a positive voltage also. In this circuit it is negative, or "NOT OR". The circuit is an "OR" gate with phase inversion. It has been named a "NOR" circuit. Note that if we define *opening* a switch as being synonymous with applying an input, then we have an "AND" circuit with phase inversion since both switch A *and* switch B must be open before the current through R_L ceases. We see that the same circuit can be an "AND" or an "OR" gate depending on the polarity of the input.



GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT, THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT, THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT



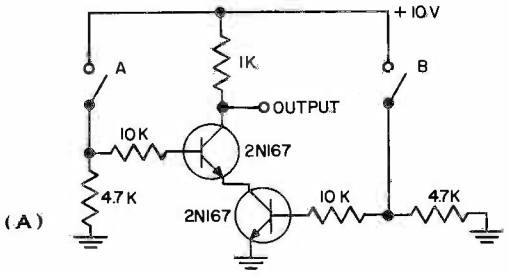
GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

BASIC LOGIC CIRCUITS USING PARALLEL TRANSISTORS
FIGURE 130

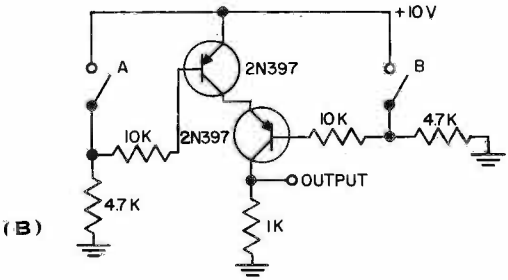
The circuit in Figure 130(b) has identically the same input and output levels but uses PNP rather than NPN transistors. If we define closing a switch as being an input,

we find that both switches must be closed before the current through R_L ceases. Therefore, the inputs which made the NPN circuit an "OR" gate make the PNP circuit an "AND" gate. Because of this, the phase inversion inherent in transistor gates does not complicate the overall circuitry excessively.

Figure 131(a) and (b) are very similar to Figure 130(a) and (b) except that the transistors are in series rather than in parallel. This change converts "OR" gates into "AND" gates and vice versa.



GATE USING NPN TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
NOTE: PHASE INVERSION OF INPUT

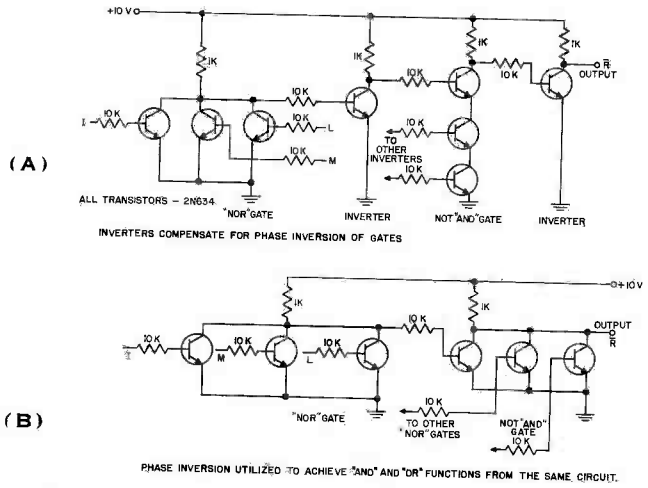


GATE USING PNP TRANSISTORS
IF CLOSING A SWITCH IS AN INPUT THIS IS AN "OR" GATE
IF OPENING A SWITCH IS AN INPUT THIS IS AN "AND" GATE
NOTE: PHASE INVERSION OF INPUT

BASIC LOGIC CIRCUITS
USING SERIES TRANSISTORS
FIGURE 131

Looking at the logic of Figure 129, let us define an input as a positive voltage; a lack of an input as zero voltage. By using the circuit of Figure 130(a) with three transistors in parallel, we can perform the "OR" operation but we also get phase inversion. We can apply the output to an inverter stage which is connected to an "AND" gate of three series transistors of the configuration shown in Figure 131(b). An output inverter stage would also be required. This is shown in Figure 132(a).

By recognizing that the circuit in Figure 130(a) becomes an "AND" gate if the input signal is inverted, the inverters can be eliminated as shown in Figure 132(b).



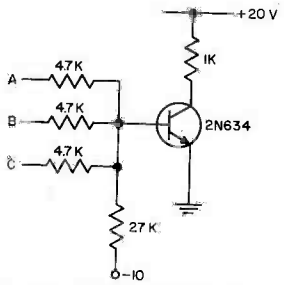
Circuits representing $(I + M + L)(\overline{I} + M + \overline{L})(\overline{I} + \overline{M} + L) = \overline{R}$

FIGURE 132

If the transistors are made by processes yielding low saturation voltages and high base resistance, the series base resistors may be eliminated. Without these resistors the logic would be called direct-coupled transistor logic DCTL. While DCTL offers extreme circuit simplicity, it places severe requirements on transistor parameters and does not offer the economy, speed or stability offered by other logical circuitry.

The base resistors of Figure 132 relax the saturation voltage and base input voltage requirements. Adding another resistor from each base to a negative bias potential would enhance temperature stability.

Note that the inputs include both "on" and "off" values of all variables e.g., both I and $\overline{I}$ appear. In order that the gates function properly, I and $\overline{I}$ cannot both be positive simultaneously but they must be identical and oppositely phased, i.e. when I is positive $\overline{I}$ must be zero and vice versa. This can be accomplished by using a phase inverter to generate $\overline{I}$ from I. Another approach, more commonly used, is to take I and $\overline{I}$ from opposite sides of a symmetrical flip-flop.

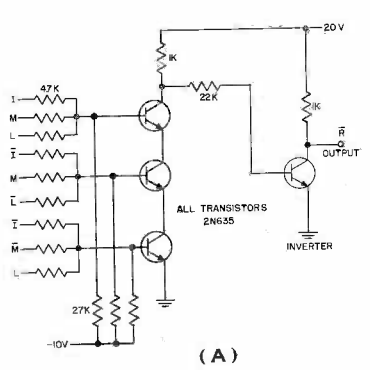


BASIC NOR CIRCUIT

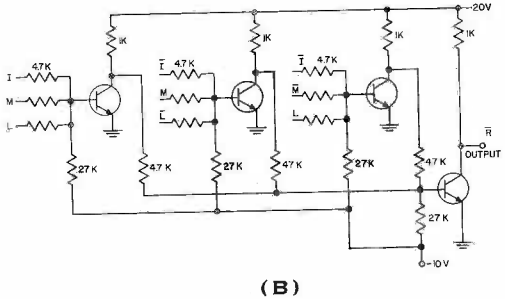
FIGURE 133

"NOR" logic is a natural extension of the use of resistors in the base circuit. In the circuit of Figure 133, if any of the inputs is made positive, sufficient base current

results to cause the transistor to conduct heavily. The "OR" gating is performed by the resistors; the transistor amplifying and inverting the signal. The logic of Figure 129 can now be accomplished by combining the "NOR" circuit of Figure 133 with the "AND" circuit of Figure 131(a). The result is shown in Figure 134. In comparing the circuits in Figure 132(a) and 134, we see that the "NOR" circuit uses one-fourth as many transistors and one-half as many resistors as the brute force approach. In fact if we recall that the equation we are dealing with gives $\overline{R}$ rather than R, we see that we can get R by removing the output phase inverter and making use of the inherent inversion in the "NOR" circuit.



(A)



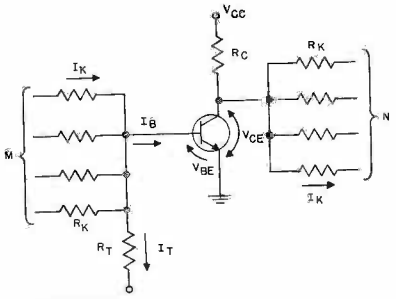
(B)

"NOR" logic using inversion for "AND" gate

"NOR" logic using series transistors for "AND" gate

FIGURE 134

Because of the fact that a generalized Boolean equation can be written as a series of "OR" gates followed by an "AND" gate as was shown, it follows that such equations can be written as a series of "NOR" gates followed by a "NOR" gate. The low cost of the resistors used to perform the logic and the few transistors required make "NOR" logic attractive.



DEFINITIONS

I_K = MINIMUM CURRENT THROUGH R_K FOR TURNING TRANSISTOR ON

I_B = MINIMUM BASE CURRENT FOR TURNING TRANSISTOR ON

I_T = BIAS CURRENT TO KEEP TRANSISTOR OFF AT HIGH TEMPERATURES

M = MAX. NUMBER OF INPUTS PERMITTED

N = MAX. NUMBER OF OUTPUTS PERMITTED

V_{BE} = MAX. BASE TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

V_{CE} = MAX. COLLECTOR TO EMITTER VOLTAGE WHEN THE TRANSISTOR IS ON.

Circuit used for design of "NOR" circuitry

FIGURE 135

A detailed "NOR" building block is shown in Figure 135. The figure defines the basic quantities. The circuit can readily be designed with the aid of three basic equations. The first derives the current I_K under the worst loading conditions at the collector of a stage.

$$I_K = \frac{V_{CC} - V_{BE} - I_{COM}R_C}{R_K + NR_C} \quad \text{where } I_{COM} \tag{A}$$

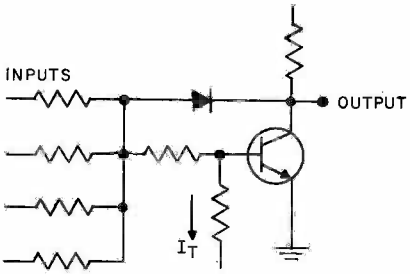
is the maximum I_{CO} that is expected at the maximum junction temperature. The second equation indicates the manner in which I_K is split up at the base of the transistor.

$$I_K = I_B + \frac{M\,(V_{CEM} - V_{CEN} + V_{BE} - V_{EB}) - (V_{BE} - V_{CEN})}{R_K} + I_{COM} \tag{B}$$

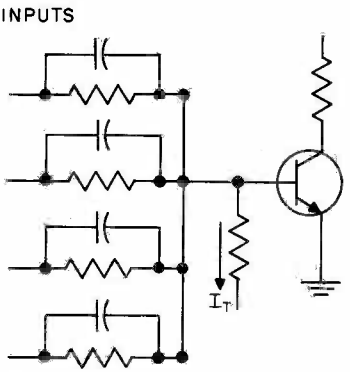
where V_{CEN} is the minimum expected saturation voltage, V_{CEM} is the maximum expected saturation voltage and V_{EB} is the reverse bias required to reduce the collector current to I_{CO}. V_{EB} is a negative voltage. The third equation ensures that V_{EB} will be reached to turn off the transistor.

$$I_{COM} + \frac{(V_{CEM} - V_{EB})M}{R_K} = I_T \tag{C}$$

Knowing I_T and choosing a convenient bias potential permits calculation of R_T. In using these equations, first select a transistor type. Assume the maximum possible supply voltage and collector current consistent with the rating of the transistor and the maximum anticipated ambient temperature. This will ensure optimization of N and M. From the transistor specifications values of I_{COM}, V_{BE}, V_{CEN}, and I_B (min) can be calculated. I_B (min) is the minimum base current required to cause saturation. R_C is calculated from the assumed collector current. In equation (A) solve for I_K using the desired value of N and an arbitrary value for R_K. Substitute the value for I_K in equation (B) along with a chosen value for M and solve for I_B. While superficially I_B need only be large enough to bring the transistor into saturation, increasing I_B will improve the rise time.



(a) CLAMPING DIODE REDUCES STORAGE TIME TO INCREASE SPEED



(b) CAPACITORS REDUCE STORAGE TIME TO INCREASE SPEED

FIGURE 136

Circuit speed can also be enhanced by using a diode as shown in Figure 136(a) to prevent severe saturation or by shunting R_K by a capacitor as in 136(b). The capacitors may cause malfunction unless the stored charge during saturation is carefully

controlled; they also aggravate crosstalk between collectors. For this reason it is preferable to use higher frequency transistors without capacitors when additional speed is required.

BINARY ARITHMETIC

Because bistable circuits can be readily designed using a variety of components from switches to transistors, it is natural for counters to be designed to use binary numbers, i.e. numbers to the base 2. In the conventional decimal system, a number written as 2904 is really a contraction for $2 \times 10^3 + 9 \times 10^2 + 0 \times 10^1 + 4 \times 1$. We see that each place refers to a different power of 10 in ascending order from the right. In the binary system, only two symbols are permitted, 0 and 1. All numbers are constructed on the basis of ascending powers of 2. For example, 11011 means $1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 1$. This is 27 in the decimal system. Using this construction, we can compare the form of binary and decimal numbers.

Binary	*Decimal*
0	0
1	1
10	2
11	3
100	4
101	5
110	6
111	7

We see that the table in Figure 127 is actually a list of the first 8 binary numbers. The count in a binary counter can be determined by noting whether each stage is in the 1 or 0 condition, and then assigning the appropriate power of 2 to the stage to construct the number as in our examples.

To multiply a number by 10 we add a zero to the right hand side in the decimal system. In the binary system, we add a zero when multiplying by two. This is equivalent to shifting the number one place to the left. This operation is done by a shift register.

If it is required to count to a base other than 2, a binary counter can be modified to counter to another base.

The rules for accomplishing the modification will be illustrated by constructing a counter to the base 10.

Rule	Example
1) Determine the number of binary stages (N) required to count to the desired new base (M)	$M = 10$ $2^3 < 10 < 2^4$ $N = 4$
2) Subtract M from 2^N	$2^4 - 10 = 6$
3) Write the remainder in binary form	$6 = 110$
4) When the count reaches 2^{N-1}, feed back a one to each stage having a one in the remainder	$2^{N-1} = 2^3 = 1000$ Feedback added gives 1 110

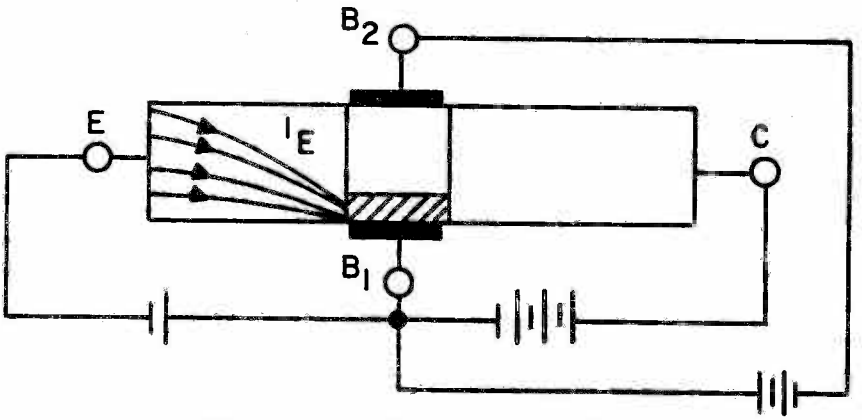
As additional pulses are added they will count through to M and then recycle to zero. This method is based on advancing the count at the point 2^{N-1} to the extent that the indicated count is 2^N when M input pulses are applied. The feedback is applied when the most significent place becomes a one but it is imperative that feedback be delayed until the counter settles down in order to avoid interference with the normal counter action.

TETRODE TRANSISTORS

Transistor types 3N36 and 3N37 are grown germanium NPN tetrodes manufactured by the meltback process. The 3N36 is generally used between 30 MC and 90 MC while the 3N37 is used from 90 MC to 200 MC. Primarily intended for high frequency use as RF amplifiers, IF amplifiers, mixers and oscillators, these transistors are also excellent for wide band video amplifiers. The use of base-two for AGC control is also attractive in that very little detuning of the collector circuit results.

Formerly designated by the development number ZJ-22, these types are now in quantity production. The case dimensions of these transistors conform to the JETEC TO-12 package. They are electrically isolated from the case, which may be grounded by the indexing tab, if required for shielding purposes. The design is suitable for automatic insertion into printed circuit boards.

It has long been recognized that smaller bar size will improve high frequency transistor performance. In particular, small cross section base regions will reduce the base spreading resistance, r'_b, (or high frequency base resistance). High r'_b is the most degradating high frequency parameter and is almost always the performance-limiting factor. One approach to reducing r'_b is to use physically minute bars. While this solves the electrical problem and is technically possible, the cost of manufacture is high and mechanical reliability is low. To overcome these problems, G.E. uses a reasonable size bar and obtains the high frequency performance by electrical means. With the addition of a second base lead and the application of a suitable cross-base bias, an electric field is established which "compresses" the active base region and thereby brings about a significant reduction in the high frequency base resistance. See Figure 137.

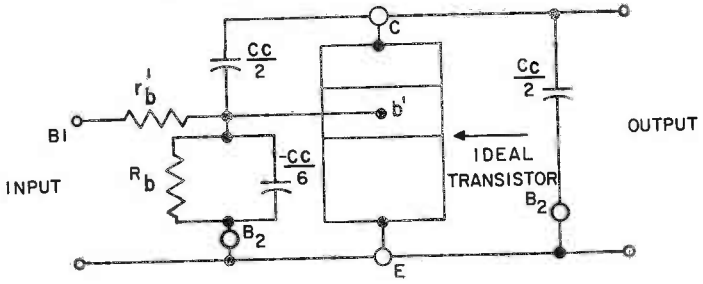


Effect of base-two bias on current distribution
FIGURE 137

Improvements in base resistance of the order of 10 to 1 are achieved by the tetrode over the triode. Since the collector-base junction is normally biased in the inverse direction, the addition of base-two bias has relatively little effect on the collector junction. It merely increases the average bias by $V_{B_1B_2}/2$ which at any collector bias over a few volts has practically no effect.

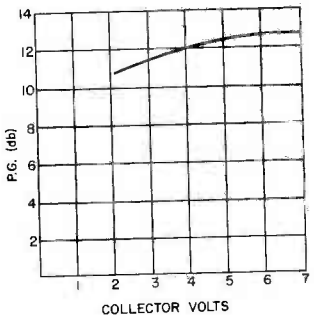
Operation in the common emitter configuration is generally recommended for several reasons. Operation is more stable and is less likely to be regenerative. Power gain is higher except at the upper frequency limits. The effect of collector capacity on

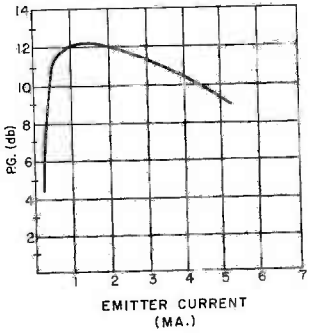
internal feedback is approximately halved when base-two is connected to a-c ground. See Figure 138 for a simplified equivalent circuit.

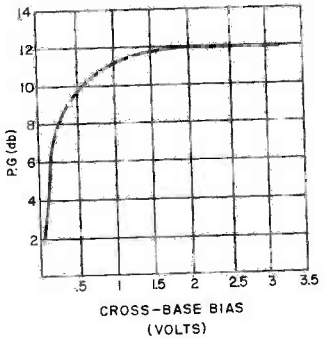


Approximate equivalent circuit of tetrode
FIGURE 138

As can be seen, half the collector capacity is across the load and can be tuned out. Thus, it does not contribute to the internal feedback. Output impedance is increased by a factor of 2, with a corresponding improvement in high frequency available power gain. Figure 139 shows the typical power gain variations of a 3N36 at 60 MC with collector voltage, emitter current and base-two bias. Curves for the 3N37 at 150 MC have the same general shape.



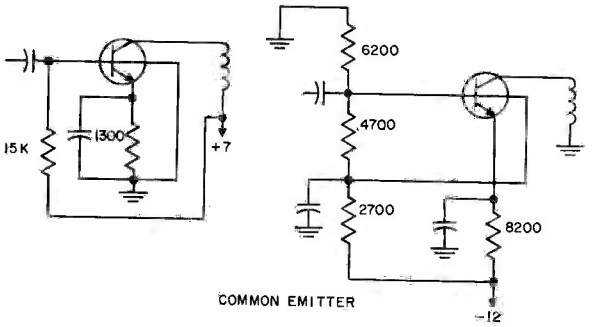




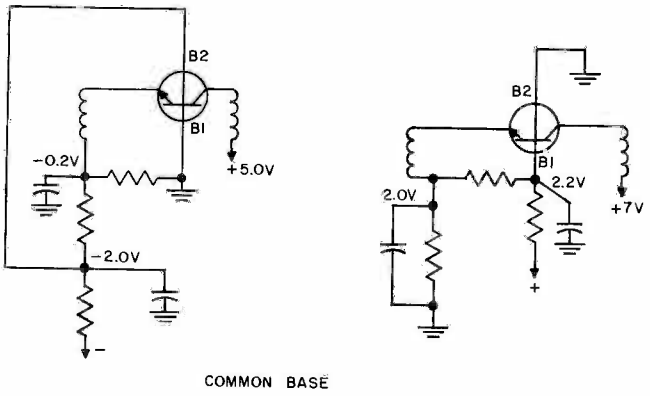
Power gain variations with bias
FIGURE 139

Typical d-c biasing methods are shown in Figures 140 and 141. Recommended conditions are:

Collector to emitter voltage, $V_{CE} = 5$ volts; base-one to base-two voltage, $V_{B_1B_2} = 2$ volts; base-one to base-two current, $I_{B_1B_2} = .5$ ma; emitter current, $I_E = 1.5$ ma.



Typical biasing methods
FIGURE 140



Typical biasing methods
FIGURE 141

Typical circuit configurations utilizing tetrode transistors are shown in Figures 142, 143, and 144.

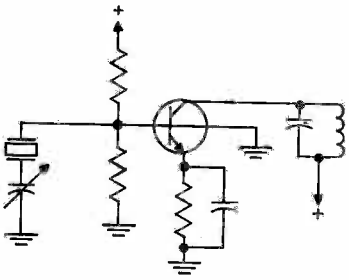
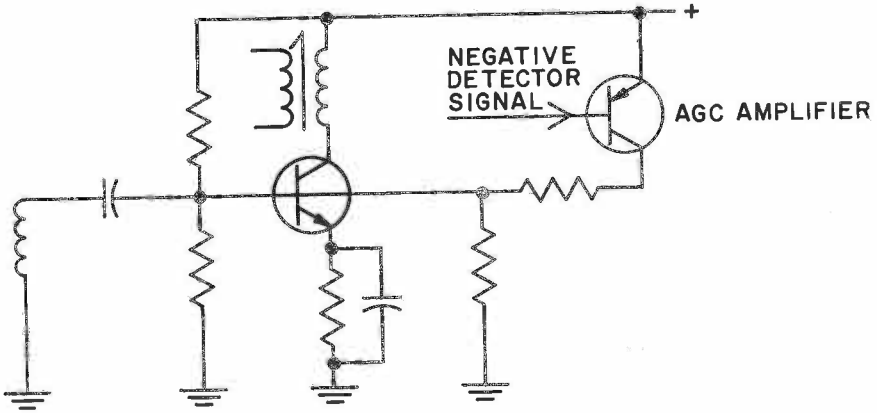
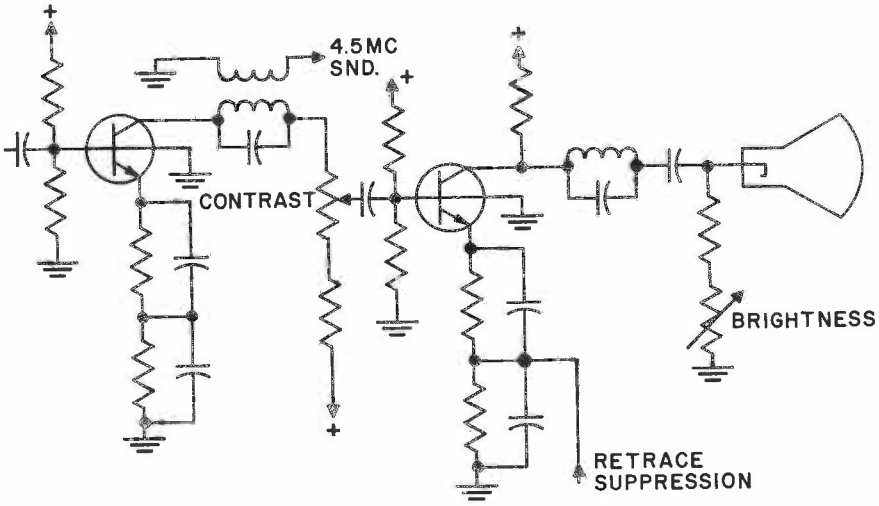


FIGURE 142



BASE 2 AGC FOR RF AND IF AMPLIFIERS

FIGURE 143



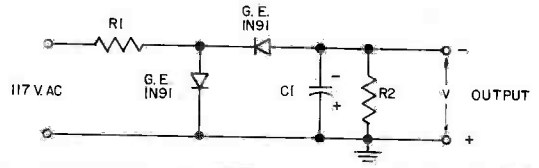
TV VIDEO AMPLIFIER (FOR HIGH Gm PICTURE TUBES)

FIGURE 144

Pages 103 &104 missing

POWER SUPPLIES

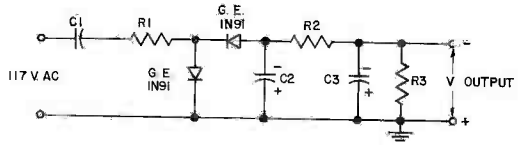
Both silicon and germanium cells can be used in the types of power supplies illustrated in Figures 149, 150, 151, and 152. All four of these power supplies are designed for low ripple output and high reliability at minimum expense. However, they are limited to Class A types of load in which the average load current does not vary with the amplitude of the impressed signal. Class B loads require a stiffer voltage source than



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	C1	R2*	APPROX. RIPPLE
12 VOLTS	1 MA.	43K, 1/2W	250 μf 15 VOLT ELECTROLYTIC	180K 1/2W	0.1%
12 VOLTS	2 MA.	22K, 1/2W	250 μf 15 VOLT ELECTROLYTIC	100K 1/2W	0.1%
25 VOLTS	2 MA.	18K, 1/2W	250 μf 30 VOLT ELECTROLYTIC	180K 1/2W	0.1%

*TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R2.

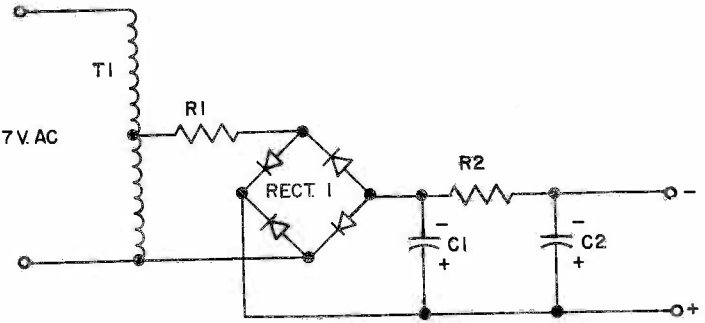
PRE-AMP POWER SUPPLY
FIGURE 149



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	R3*	C1 METALLIZED PAPER	C2	C3	APPROX RIPPLE
12 VOLTS	100MA.	2Ω 1 WATT	100Ω 2W	2200Ω 1W	THREE 2-μf IN PARALLEL 200 V	250 μf 15 VOLT ELECTROLYTIC	250 μf 15 VOLT ELECTROLYTIC	0.5%
12 VOLTS	150MA	2Ω 1 WATT	100Ω 10 W	2200Ω 1W	FOUR 2-μf IN PARALLEL 200V	250μf 15 VOLT ELECTROLYTIC	250μf 15 VOLT ELECTROLYTIC	0.5%
25 VOLTS	50MA	2Ω 1 WATT	250Ω 2W	10,000Ω 1W	TWO 2-μf IN PARALLEL 200V	100μf 50 VOLT ELECTROLYTIC	250μf 30 VOLT ELECTROLYTIC	0.5%

* TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R3.

GENERAL PURPOSE TRANSISTOR POWER SUPPLY
FIGURE 150



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	C1	C2	RECT. 1	APPROX. RIPPLE
40 VOLTS	1 AMP	3Ω 10 WATTS	20Ω 20 WATTS	300μf 150 VOLT ELECTROLYTIC	1000μf 50 VOLT ELECTROLYTIC	FOUR G.E. 1N537	1%

T1 - U.T.C. R-43 AUTOTRANSFORMER OR EQUAL
2:1 WINDING RATIO

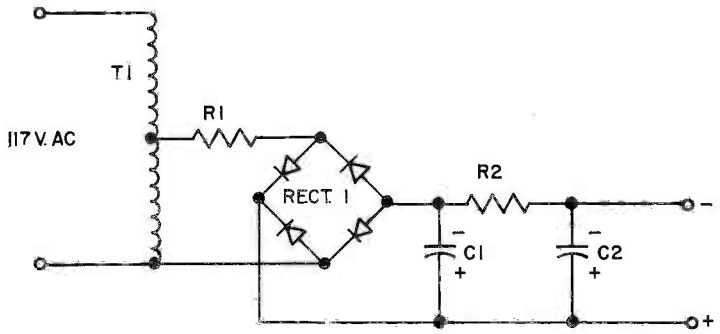
POWER SUPPLY FOR HIGH POWER CLASS A TRANSISTOR AMPLIFIER
FIGURE 151

the resistance-capacity combinations of the illustrated power supplies can provide. For Class B and other loads that require good voltage regulation, it is recommended that the line voltage be reduced through transformers rather than series resistance or capacitance, and that chokes be substituted for the series resistance in the filter elements. Alternately, a regulated power supply such as shown on page 108 can be used.

This circuit uses a step-down transformer and full-wave rectifier as a source of unregulated DC. A power transistor acts as a series regulator and mercury batteries are used for the voltage reference. The battery drain is very small so their life is essentially equal to the shelf life.

When a semiconductor rectifier feeds a capacity-input filter such as in Figures 149 through 152, it is necessary to limit the high charging current that flows into the input capacitor when the circuit is energized. Otherwise this surge of current may destroy the rectifier. Resistor R1 is used in Figures 149 through 152 to limit this charging current to safe values.

As shown, the four power supplies do not isolate the load circuit from the 117 volt AC line. In Figures 149 and 150, the load circuit may be grounded provided a polarized



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	C1	C2	RECT. 1	APPROX. RIPPLE
40 VOLTS	1 AMP.	3Ω 10 WATTS	20Ω 20 WATTS	300μf 150 VOLT ELECTROLYTIC	1000μf 50 VOLT ELECTROLYTIC	FOUR G.E. 1N537	1%

T1 - U.T.C. R-43 AUTOTRANSFORMER OR EQUAL
2:1 WINDING RATIO

POWER SUPPLY FOR HIGH POWER CLASS A TRANSISTOR AMPLIFIER
FIGURE 151

the resistance-capacity combinations of the illustrated power supplies can provide. For Class B and other loads that require good voltage regulation, it is recommended that the line voltage be reduced through transformers rather than series resistance or capacitance, and that chokes be substituted for the series resistance in the filter elements. Alternately, a regulated power supply such as shown on page 108 can be used.

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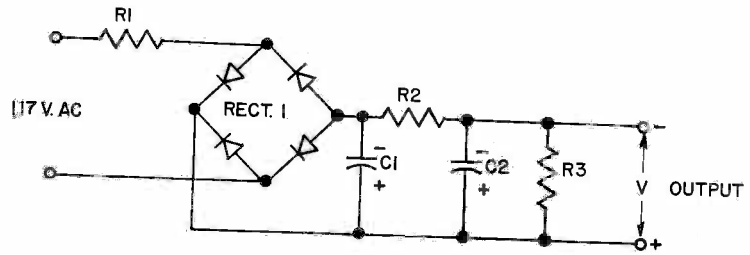
As shown, the four power supplies do not isolate the load circuit from the 117 volt AC line. In Figures 149 and 150, the load circuit may be grounded provided a polarized



OUTPUT VOLTAGE V	OUTPUT CURRENT	R1	R2	C1	C2	R3*	RECT. 1	APPROX. RIPPLE
40 VOLTS	1 AMP	5Ω 20W	75Ω 100W	100μf 150 VOLTS ELECTROLYTIC	300μf 50 VOLTS ELECTROLYTIC	1000Ω 2 W	FOUR G.E. IN538	1%

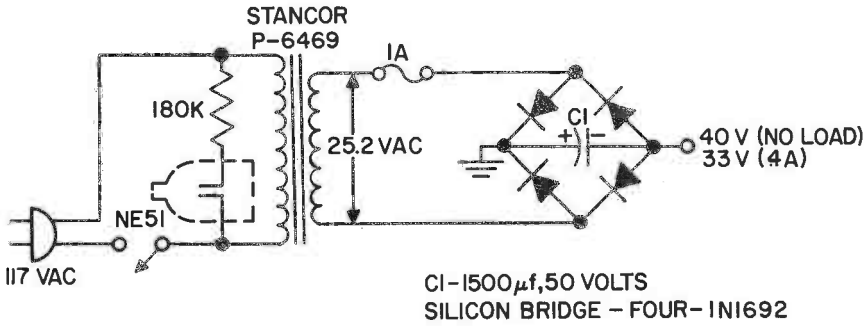
* TO ADJUST VOLTAGE OUTPUT FOR OTHER OUTPUT CURRENTS, ADJUST R3.

POWER SUPPLY FOR HIGH POWER CLASS A TRANSISTOR AMPLIFIER
FIGURE 152

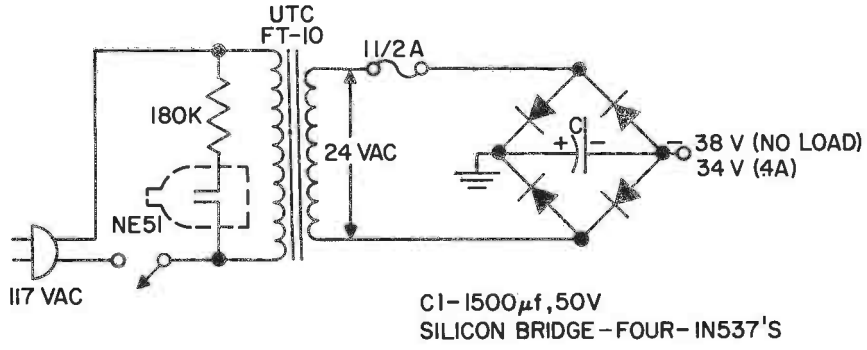
plug is used on the AC line cord to ensure that the grounded side of the AC line is always connected to the grounded side of the load. Figures 151 and 152 utilize what is called a single phase bridge rectifier circuit to achieve full wave rectification, and hence, lower ripple. Since ground cannot be carried through on a common line to the load in this type of circuit, it is necessary to insulate the load "ground" from accidental contact with true ground, or to insert an isolation transformer ahead of the power supply to isolate the two systems. Careful attention to these factors is of particular importance when supplying DC to high gain amplifiers to eliminate hum.

As illustrated, Figures 149 and 150 develop a negative output voltage with respect to ground as required when supplying P-N-P transistors with grounded emitters. To develop a positive voltage with respect to ground, it is only necessary to reverse the rectifiers and electrolytic capacitors in the circuit.

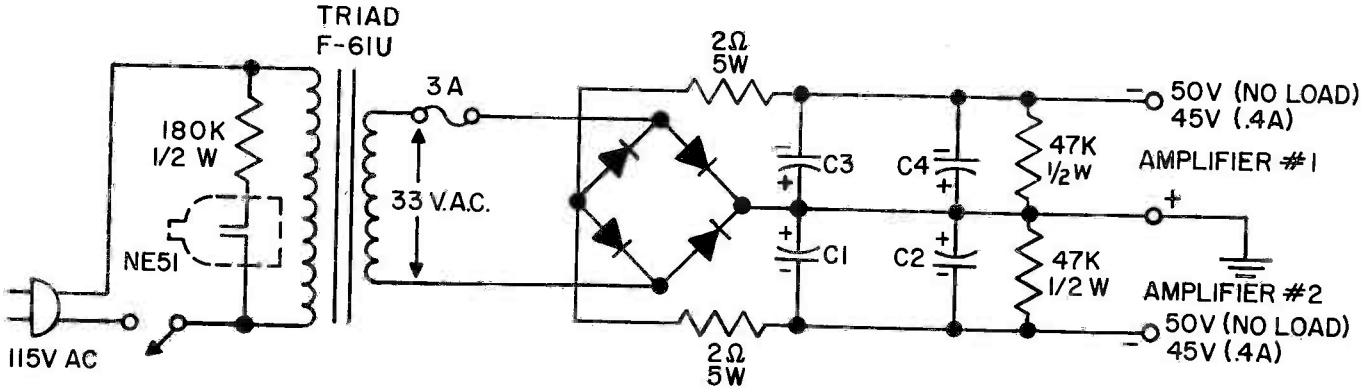
The power supply of Figure 151 uses an autotransformer to reduce the line voltage to one-half normal value before applying to the rectifiers. Provided the additional heat dissipation is not objectionable, Figure 152 provides a cheaper means of achieving the same objective by using resistor R2 to reduce the voltage to the desired value.



POWER SUPPLY FOR FIVE-WATT AMPLIFIER
FIGURE 153



POWER SUPPLY FOR DUAL SIX-WATT AMPLIFIER
FIGURE 154



C1 – 1500 μf, 50 VOLTS
C2 – 1500 μf, 50 VOLTS
C3 – 1500 μf, 50 VOLTS
C4 – 1500 μf, 50 VOLTS
SILICON BRIDGE – FOUR – IN1115

POWER SUPPLY FOR DUAL TEN-WATT AMPLIFIERS
FIGURE 155

TRANSISTOR SPECIFICATIONS

HOW TO READ A SPECIFICATION SHEET

Semiconductors are available in a large variety of different types, each with its own unique characteristics. At the present time there are over 2200 different types of diodes and rectifiers and over 750 different types of transistors being manufactured.

The Characteristics of each of these devices are usually presented in specification sheets similar to the ones represented on the next two pages. These specifications, particularly the transistor specification on the next page, contain many terms and ratings that are probably new to you, so we have selected several of the more important ones and explained what they mean.

NOTES ON TRANSISTOR SPECIFICATION SHEET

(1) The lead paragraph is a general description of the device and usually contains three specific pieces of information – The kind of transistor, in this case a silicon NPN triode, – A few major application areas, amplifier and switch, – General sales features, electrical stability and a standard size hermetically sealed package.

(2) The **Absolute Maximum Ratings** are those ratings which should not be exceeded under any circumstances. Exceeding them may cause device failure.

(3) The **Power Dissipation** of a transistor is limited by its junction temperature. Therefore, the higher the temperature of the air surrounding the transistor (ambient temperature), the less power the device can dissipate. A factor telling how much the transistor must be derated for each degree of increase in ambient temperature in degrees centigrade is usually given. Notice that this device can dissipate 150mw at 25°C. By applying the given derating factor of 1mw for each degree increase in ambient temperature, we find that the power dissipation has dropped to 0mw at 175°C, which is the maximum operating temperature of this device.

(4) All of the remaining ratings define what the device is capable of under specified test conditions. These characteristics are needed by the design engineer to design matching networks and to calculate exact circuit performance.

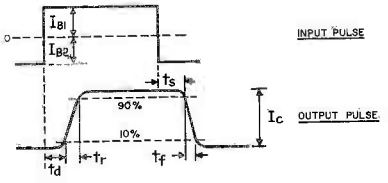
(5) **Current Transfer Ratio** is another name for beta. In this case we are talking about an a-c characteristic, so the symbol is h_{fe}. Many specification sheets also list the d-c beta using the symbol h_{FE}. Beta is partially dependent on frequency, so some specifications list beta for more than one frequency.

(6) The **Noise Figure** is a measurement derived to evaluate the amount of electrical noise produced by the transistor in a circuit.

(7) The **Frequency Cutoff** f_{ab} of a transistor is defined as that frequency at which the grounded base current gain drops to .707 of the 1kc value. It gives a rough indication of the useful frequency range of the device.

(8) The **Collector Cutoff Current** is the leakage current from collector to base when no emitter current is being applied. This leakage current varies with temperature changes and must be taken into account whenever any semiconductor device is designed into equipment used over a wide range of ambient temperature.

(9) The **Switching Characteristics** given show how the device responds to an input pulse under the specified driving conditions. These response times are very dependent on the circuit used. The terms used are explained in the curves at right.



2N332

Outline Drawing No. 4

The General Electric Type 2N332 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt
Collector Current	I_C	25 ma
Power*		
Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (125°C)	P_C	50 mw
Temperature Range		
Storage	T_{STG}	−65°C to 200°C
Operating	T_A	−55°C to 175°C

*Derate 1mw/°C increase in ambient temperature.

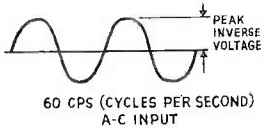
ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; $f = 1kc$)

		MIN.	NOM.	MAX.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	9	15	20	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.25	1.0	5.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.25	1.2	μmhos
Power Gain ($V_{CB} = 20v$; $I_E = -2ma$; $f = 1kc$; $R_G = 1K$ ohms; $R_L = 20K$ ohms)	G_e		35		db
Noise Figure	NF		28		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1ma$)	f_{ab}		15		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1ma$; $f = 1mc$)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2ma$; $f = 5mc$)	G_e		17		db
D-C Characteristics					
Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1ma$; $I_C = 5ma$)	R_{SC}		80	200	ohms
Switching Characteristics					
($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)					
Delay Time	t_d		.75		μsec
Rise Time	t_r		.5		μsec
Storage Time	t_s		.05		μsec
Fall Time	t_f		.15		μsec

NOTES ON RECTIFIER SPECIFICATION SHEET

The performance of a rectifier is judged primarily on four key measurements, or parameters. They are always given for specific ambient conditions, such as still air and 55°C, and are based on a 60 cycles per second (A-C) input with the rectifier feeding a resistive or inductive load (see Ⓐ below). A capacitive load will increase the Peak Inverse Voltage and necessitate a different set of ratings than shown here. These key parameters are:



① **Maximum Peak Inverse Voltage** (usually referred to as PIV), the peak a-c voltage which the unit will withstand in the reverse direction; ② **Maximum Allowable D-C Output Current,** which varies with ambient temperature; ③ **Maximum Allowable One-cycle Surge Current,** representing the maximum instantaneous current which the rectifier can withstand, usually encountered when the equipment is turned on; ④ **Maximum Full-load Forward Voltage Drop,** measured with maximum d-c output flowing and maximum PIV applied. This is a measure of the rectifier's efficiency.

1N1692, 1N1693
1N1694, 1N1695

These alloy junction silicon rectifiers are designed for general purpose applications requiring maximum economy. These rectifiers are hermetically sealed and will perform reliably within the operating specifications.

RATINGS AND SPECIFICATIONS

Ⓐ (60 CPS, Resistive or Inductive)

	1N1692	1N1693	1N1694	1N1695	
① Max. Allowable Peak Inverse Voltage	100	200	300	400	volts
Max. Allowable RMS Voltage	70	140	210	280	volts
Max. Allowable Continuous Reverse DC Voltage	100	200	300	400	volts
② Max. Allowable DC Output 100°C Ambient	250	250	250	250	ma
② Max. Allowable DC Output 50°C Ambient	600	600	600	600	ma
③ Max. Allowable One Cycle Surge Current	20	20	20	20	amps
④ Max. Full Load Forward Voltage Drop (Full cycle average at 100°C)	.60	.60	.60	.60	volts
Max. Leakage Current at Rated PIV (Full cycle average at 100°C)	0.5	0.5	0.5	0.5	ma
Peak Recurrent Forward Current	2.0	2.0	2.0	2.0	amps
Max. Operating Temperature	←	+ 115°C		→	

The other ratings or specifications are additional yardsticks of performance which are more or less critical depending on the operating conditions to be experienced. For instance, the IN536 Series for which specifications are shown, being silicon rectifiers, are able to show a higher range of *Ambient Operating Temperatures* with higher output than a germanium unit would, and are preferred on this basis for many applications. *Maximum Leakage Current* refers to the reverse current which will flow when voltage is applied, and here, too, can be a critical measure of performance for specific applications such as magnetic amplifiers.

Sometimes there is confusion as to whether a unit is a *Diode* or a *Rectifier*. Actually the word *Diode* means "two" and both rectifiers and diodes have two elements. However, rectifiers are capable of handling much larger currents than diodes. The term diode is used to describe units used in high frequency, low current, signal applications such as in high frequency circuits of television receivers.

EXPLANATION OF PARAMETER SYMBOLS

SMALL SIGNAL & HIGH FREQUENCY PARAMETERS (at specified bias)

Symbols	Abbreviated Definitions
h_{ob}	Com. base – output admittance, input AC open-circuited
h_{ib}	Com. base – input impedance, output AC short-circuited
h_{rb}	Com. base – reverse voltage transfer ratio, input AC open-circuited
h_{fb}	Com. base — forward current transfer ratio, output AC short-circuited
h_{fe}	Com. emitter — forward current transfer ratio, output AC short-circuited
h_{fc}	Com. collector — forward current transfer ratio, output AC short-circuited
h_{oe}, h_{ie}	Examples of other corresponding com. emitter symbols
$f_{\alpha b}$	Com. base — the frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 of its low frequency value.
$f_{\alpha e}$	Com. emitter — the frequency at which the magnitude of the small-signal short-circuit forward current transfer ratio is 0.707 of its low frequency value.
f_{MAX}	Maximum frequency of oscillation
C_{ob}	Collector to base — Capacitance measured across the output terminals with the input AC open-circuited
C_{oe}	Collector to emitter — Capacitance measured across the output terminals with the input AC open-circuited
r'_b	Base spreading resistance
G_e	Com. emitter Power Gain (use G_b for com. base)
CG_e	Conversion gain
NF	Noise Figure

SWITCHING CHARACTERISTICS (at specified bias)

t_d	Ohmic delay time — These depend on both transistor and circuit parameters
t_r	Rise time — These depend on both transistor and circuit parameters
t_s	Storage time — These depend on both transistor and circuit parameters
t_f	Fall time — These depend on both transistor and circuit parameters
V_{CE} (SAT.)	Saturation voltage at specified I_C and I_B. This is defined only with the collector saturation region.
h_{FE}	Com. emitter – static value of short-circuit forward current transfer ratio, $h_{FE} = \frac{I_C}{I_B}$
h_{FE} (INV)	Inverted h_{FE} (emitter and collector leads switched)

UNIJUNCTION TRANSISTOR MEASUREMENTS

I_{B2} (MOD)	Modulated interbase current
I_P	Peak point emitter current
I_V	Valley current
R_{BBO}	Interbase resistance
V_{BB}	Interbase voltage
V_V	Valley voltage
η	Intrinsic stand-off ratio. Defined by $V_P = \eta V_{BB} + \frac{200}{T_J}$ (in ° Kelvin)

DC MEASUREMENTS

I_C, I_E, I_B	DC currents into collector, emitter, or base terminal
V_{CB}, V_{EB}	Voltage collector to base, or emitter to base
V_{CE}	Voltage collector to emitter
V_{BE}	Voltage base to emitter
BV_{CBO}	Breakdown voltage, collector to base junction reverse biased, emitter open-circuited (value of Ic should be specified)
V_{CEO}	Voltage collector to emitter, at zero base current, with the collector junction reverse biased. Specify Ic.
BV_{CEO}	Breakdown voltage, collector to emitter, with base open-circuited. This may be a function of both "m" (the charge carrier multiplication factor) and the h_{FB} of the transistor. Specify Ic.
V_{CER}	Similar to V_{CEO} except a resistor of value "R" between base and emitter.
V_{CES}	Similar to V_{CEO} but base shorted to emitter.
V_{PT}	Punch-through voltage, collector to base voltage at which the collector space charge layer has widened until it contacts the emitter junction. At voltages above punch-through, $V_{PT} = V_{CB} - V_{EB}$
V_{CCB} V_{CCE} V_{BBE}	Supply voltage collector to base Supply voltage collector to emitter Supply voltage base to emitter NOTE – third subscript may be omitted if no confusion results.
I_{CO}, I_{CBO}	Collector current when collector junction is reverse biased and emitter is DC open-circuited.
I_{EO}, I_{EBO}	Emitter current when emitter junction is reverse biased and collector is DC open-circuited.
I_{CEO}	Collector current with collector junction reverse biased and base open-circuited.
I_{CES}	Collector current with collector junction reverse biased and base shorted to emitter.
I_{ECS}	Emitter current with emitter junction reverse biased and base shorted to collector.
R_{SC}	Collector saturation resistance

OTHER SYMBOLS USED

P_{CM}	Peak collector power dissipation for a specified time limit
P_{CAV}	Average maximum collector power dissipation
P_o	Power output
Z_i	Input impedance
Z_o	Output impedance
T_A	Operating Temperature
T_J	Junction Temperature
T_{STG}	Storage Temperature

NOTE: In devices with several electrodes of the same type, indicate electrode by number. Example: I_{B2}. In multiple unit devices, indicate device by number preceding electrode subscript. Example: I_{2C}. Where ambiguity might arise, separate complete electrode designations by hyphens or commas. Example: $V_{1C1-2C1}$ (Voltage between collector #1 of device #1 and collector #1 of device #2.)

NOTE: Reverse biased junction means biased for current flow in the high resistance direction.

TRANSISTOR SUMMARY

The table below shows all current General Electric Signal Transistor types along with the maximum dimension of the package base and general application area.

			PNP INLINE LEAD .460 MAX	PNP TRIANGULAR LEAD .370 MAX	NPN INLINE LEAD .530 MAX	NPN TRIANGULAR LEAD .370 MAX
INDUSTRIAL • COMPUTER • MILITARY	SILICON	AMPLIFIER & COMPUTER				2N332 2N333 2N335
		UNIJUNCTION				2N489* 2N490* 2N491* 2N492* 2N493* 2N494* *A PN Device
	GERMANIUM	AUDIO PNP	2N43 2N43A 2N44 2N44A	2N524 2N525 2N526 2N527		
		COMPUTER PNP	2N123 2N450 2N518	2N394 2N395 2N396 2N397		
		COMPUTER NPN			2N78 2N167	2N634 2N635 2N636
		TETRODE NPN				3N36 3N37
ENTERTAINMENT	GERMANIUM	IF NPN			2N168A 2N169 2N169A 2N292 2N293	
		AUDIO PNP	2N186 2N186A 2N187 2N187A 2N188 2N188A 2N189 2N190 2N191 2N192 2N241 2N241A 2N265	2N319 2N320 2N321 2N322 2N323 2N324 2N508		

GENERAL ELECTRIC TRANSISTOR SPECIFICATIONS

2N43

Outline Drawing No. 1

The General Electric Type 2N43 Germanium Alloy Junction Transistor Triode is a PNP unit particularly recommended for high gain, low power applications. A hermetic enclosure is provided by use of glass-to-metal seals and welded seams.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	−45 volts
Collector to Emitter	V_{CE}	−30 volts
Emitter to Base	V_{EB}	−5 volts
Collector Current	I_C	−300 ma
Power		
Total Transistor Dissipation	P_M	240 mw
Temperature		
Storage	T_{STG}	Max. +100 °C Min. −65 °C
Operating Junction	T_J	Max. + 85 °C

ELECTRICAL CHARACTERISTICS: (25°C)

		MIN.	MAX.	DESIGN CENTER	
Small Signal Characteristics (V_{CB} or $V_{CE} = -5$ volts, $I_E = 1$ ma; f = 270 cps unless otherwise specified)					
Common base output admittance (input A-C open circuited)	h_{ob}	.1	1.5	.8	μmhos
Forward current transfer ratio (output A-C short circuited)	h_{fe}	30	66	42	
Common base input impedance (output A-C short circuited)	h_{ib}	25	35	29	ohms
Common base reverse voltage transfer ratio (input A-C open circuited)	h_{rb}	1	15	5	$\times 10^{-4}$
Common base output capacity (input A-C open circuited; f = 1 mc)	C_{ob}	20	60	40	μμf
Noise Figure (f = 1 Kc; BW = 1 cycle)	NF		20	6	db
Frequency cutoff (Common Base)	f_{ab}	.5	3.5	1.3	mc
D-C Characteristics					
Collector cutoff current ($V_{CBO} = -45$v)	I_{CO}		−16	−8	μamps
Emitter cutoff current ($V_{EBO} = -5$v)	I_{EO}		−10	−4	μamps
Base input voltage, common emitter ($V_{CE} = -1$ volt; $I_C = -20$ ma)	V_{BE}			−.23	volts
Common emitter static forward current transfer ratio ($V_{CE} = -1$ volt; $I_C = -20$ ma)	h_{FE}	34	65	53	
Common emitter static forward current transfer ratio ($V_{CE} = -1$ volt; $I_C = -100$ ma)	h_{FE}	30		48	
Collector to emitter voltage (10 K ohms resistor base to emitter; $I_C = -0.6$ ma)	V_{CER}	−30			volts
Punch-through voltage	V_{PT}	−30			volts
Thermal Characteristics					
Junction temperature rise/unit collector or emitter dissipation (in free air)			0.25		°C/mw
Junction temperature rise/unit collector or emitter dissipation (infinite heat sink)			0.11		°C/mw

The 2N43A is a commercial version of the military type 2N43A per MIL-T-19500, and is tested to the same electrical, mechanical and degradation tests.

2N43A

Outline Drawing No. 1

The General Electric Type 2N44 Germanium Alloy Junction Transistor Triode is a PNP unit particularly recommended for medium gain, low power applications. A hermetic enclosure is provided by use of glass-to-metal seals and welded seams.

2N44

Outline Drawing No. 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	−45 volts
Collector to Emitter	V_{CE}	−30 volts
Emitter to Base	V_{EB}	−5 volts
Collector Current	I_C	−300 ma
Power		
Total Transistor Dissipation	P_M	240 mw
Temperature		
Storage	T_{STG}	Max. +100 °C Min. −65 °C
Operating Junction	T_J	Max. + 85 °C

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics (V_{CB} or V_{CE} = −5 volts, I_E = 1 ma; f = 270 cps unless otherwise specified)		MIN.	MAX.	DESIGN CENTER	
Common base output admittance (input A-C open circuited)	h_{ob}	.1	1.5	.9	μmhos
Forward current transfer ratio (output A-C short circuited)	h_{fe}			25	
Common base input impedance (output A-C short circuited)	h_{ib}	27	38	31	ohms
Common base reverse voltage transfer ratio (input A-C open circuited)	h_{rb}	1.0	13	4	× 10^{-4}
Common base output capacity (input A-C open circuited; f = 1 mc)	C_{ob}	20	60	40	μμf
Noise Figure (f = 1 Kc; BW = 1 cycle)	NF		15	6	db
Frequency cutoff (Common Base)	f_{ab}	.5	3.0	1.0	mc
D-C Characteristics					
Collector cutoff current (V_{CBO} = −45v)	I_{CO}		−16	−8	μamps
Emitter cutoff current (V_{EBO} = −5v)	I_{EO}		−10	−4	μamps
Base input voltage, common emitter	V_{BE}			−.25	volts
Common emitter static forward current transfer ratio (V_{CE} = −1 volt; I_C = −20 ma)	h_{FE}	18	43	31	
Common emitter static forward current transfer ratio (V_{CE} = −1 volt; I_C = −100 ma)	h_{FE}	13		25	
Collector to emitter voltage (10 K ohms resistor base to emitter; I_C = −0.6 ma)	V_{CER}	−30			volts
Punch-through voltage	V_{PT}	−30			volts
Thermal Characteristics					
Junction temperature rise/unit collector or emitter dissipation (in free air)			0.25		°C/mw
Junction temperature rise/unit collector or emitter dissipation (infinite heat sink)			0.11		°C/mw

The 2N44A is a commercial version of the military type 2N44A per MIL-T-19500, and is tested to the same electrical, mechanical and degradation tests.

2N44A

Outline Drawing No. 1

2N78

Outline Drawing No. 3

The General Electric 2N78 is a grown junction NPN high frequency transistor intended for high gain RF and IF amplifier service and general purpose applications. The G.E. rate-growing process used in the manufacture of the 2N78 provides the uniform and stable characteristics required for military and industrial service.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Collector to Emitter Voltage (base open), V_{CEO}	15 volts
Collector to Base Voltage (emitter open), V_{CBO}	15 volts
Collector Current, I_C	20 ma
Emitter Current, I_E	−20 ma
Collector Dissipation*, P_{CM}	65 mw
Storage Temperature, T_{STG}	85 °C

ELECTRICAL CHARACTERISTICS: (25°C)

	DESIGN CENTER	LIMITS MIN.	LIMITS MAX.	
Low Frequency Characteristics (Common Base)				
(V_{CB} = 5 V, I_E = −1 ma, f = 270 cps)				
Input Impedance (output short circuit), h_{ib}	55			ohms
Voltage Feedback Ratio (input short circuit), h_{rb}	2	.8	10	× 10^{-4}
Current Amplification (output short circuit), h_{fb}	−.983			
DC Base Current Gain (I_B = 20 μa; V_{CE} = 1 V) h_{FE}	70	45	135	
Output Admittance (input open circuit), h_{ob}	.2			μmhos
Noise Figure (V_{CB} = 1.5 V; I_E = −0.5 ma; f = 1 KC), NF	12			db
High Frequency Characteristics (Common Base)				
(V_{CB} = 5 V, I_E = −1 ma)				
Alpha Cutoff Frequency, f_{ab}	9	5		mc
Output Capacity (f = 2 mc), C_{ob}	3		6	μμf
Voltage Feedback Ratio (f = 1 mc), h_{rb}			12	× 10^{-3}
Power Gain in Typical IF Test Circuit, G_e		27		db
Cutoff Characteristics				
Collector Cutoff Current (V_{CB} = 15 V), Ico			5	μa
Collector Cutoff Current (V_{CB} = 5 V), Ico	.7			μa

*Derate 1.1 mw/°C increase in ambient temperature.

2N107

Outline Drawing No. 1

The General Electric type 2N107 is an alloy junction PNP transistor particularly suggested for students, experimenters, hobbyists, and hams. It is available only from franchised General Electric distributors. The 2N107 is hermetically sealed and will dissipate 50 milliwatts in 25°C free air.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Collector Voltage (referred to base), V_{CB}	−12 volts
Collector Current, I_C	−10 ma
Emitter Current, I_E	10 ma
Junction Temperature, T_J	60 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Common Base, T_J = 30°C, f = 270 cps	
V_{CB} = −5v, I_E = 1 ma)	
Collector Voltage, V_{CB}	−5.0 volts
Emitter Current, I_E	1.0 ma
Output Admittance (input open circuit), h_{ob}	1.0 μmhos
Current Amplification (output short circuit), h_{fb}	−.95
Input Impedance (output short circuit), h_{ib}	32 ohms
Voltage Feedback Ratio (input open circuit), h_{rb}	3 × 10^{-4}
Collector Cutoff Current, Ico	10 μa
Output Capacitance, C_{ob}	40 μμf
Frequency Cutoff, f_{ab}	0.6 mc
Common Emitter, (V_{CE} = −Iv, I_E = 1 ma)	
Base Current Gain, h_{fe}	20

The General Electric type 2N123 is a PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance.

2N123

Outline Drawing No. 8

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Collector to Emitter Voltage (base open), V_{CEO}	−15 volts
Collector to Base Voltage (emitter open), V_{CBO}	−20 volts
Emitter to Base Voltage (collector open), V_{EBO}	−10 volts
Collector Current, I_C	−125 ma
Peak Collector Current (10 μs max.), I_{CM}	−500 ma
Emitter Current, I_E	125 ma
Collector Dissipation*, P_{CAV}	100 mw
Peak Collector Dissipation (10 μs max.)**, P_{CM}	500 mw
Total Transistor Dissipation***, P_{AV}	150 mw
Storage Temperature, T_{STG}	−55 to 85 °C

ELECTRICAL CHARACTERISTICS: (25°C)

	DESIGN CENTER	LIMITS MIN.	LIMITS MAX.	
Switching Characteristics (Common Emitter)				
D.C. Base Current Gain (V_{CE} = −1 v; I_C = 10 ma) h_{FE}	50	30	150	
Saturation Voltage (I_B = .5 ma; I_C = 10 ma), V_{CE}	.15		0.2	volts
Pulse Response Time (I_C = 10 ma)				
Delay & Rise Time, $t_d + t_r$	.9			μsec
Storage Time, t_s	3.5			μsec
Fall Time, t_f	.5			μsec
Cutoff Characteristics				
Collector Cutoff Current (V_{CB} = −20v), I_{CO}	2		6	μa
Emitter Cutoff Current (V_{EB} = −10v), I_{EO}	2		6	μa
Collector to Emitter (Base open, I_C = −0.6 ma), V_{CE}	25	15		volts
High Frequency Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma)				
Alpha Cutoff Frequency, $f_{\alpha b}$	8	5		mc
Collector Capacitance (f = 1 mc), C_{ob}	15			μμf
Voltage Feedback Ratio (f = 1 mc), h_{rb}	8			× 10⁻³
Base Spreading Resistance, r'_b	80			ohms
Low Frequency Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)				
Input Impedance, h_{ib}	28			ohms
Voltage Feedback Ratio, h_{rb}	8			× 10⁻⁴
Current Amplification, h_{fb}	−.980	−.970		
Output Admittance, h_{ob}	.9			μmhos

Derate for increase in ambient temperature:
*1.67 mw/°C, **8 mw/°C, ***2.5 mw/°C

The General Electric types 2N135, 2N136 and 2N137 are PNP alloy junction germanium transistors intended for RF and IF service in broadcast receivers. Special control of manufacturing processes provides a narrow spread of characteristics, resulting in uniformly high power gain at radio frequencies. These types are obsolete and available for replacement only.

2N135, 2N136, 2N137

Outline Drawing No. 8

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)	2N135	2N136	2N137	
Collector Voltage:				
Common Base (emitter open), V_{CBO}	−20	−20	−10	volts
Common Emitter (R_{BE} = 100 ohms), V_{CER}	−20	−20	−10	volts
Common Emitter (R_{BE} = 1 megohm), V_{CER}	−12	−12	− 6	volts
Collector Current, I_C	−50	−50	−50	ma
Emitter Current, I_E	50	50	50	ma
Collector Dissipation, P_{CM}	100	100	100	mw
Storage Temperature, T_{STG}	85	85	85	°C
ELECTRICAL CHARACTERISTICS: Design Center Values (Common Base, 25°C, V_{CB} = 5v, I_E = 1 ma)				
Voltage Feed back Ratio (input open circuit, f = 1 mc), h_{rb}	7	7	7	× 10⁻³
Output Capacitance (f = 1 mc), C_{ob}	14	14	14	μμf

2N167

Outline Drawing No. 3

The General Electric type 2N167 is an NPN high frequency, high speed switching transistor intended for industrial and military applications where reliability is of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Collector to Emitter Voltage (base open), V_{CEO}	30 volts
Collector to Base Voltage (emitter open), V_{CBO}	30 volts
Emitter to Base Voltage (collector open), V_{EBO}	5 volts
Collector Current, I_C	75 ma
Emitter Current, I_E	−75 ma
Collector Dissipation*, P_{CM}	65 mw
Transistor Dissipation**, P_M	75 mw
Storage Temperature, T_{STG}	85 °C

ELECTRICAL CHARACTERISTICS: (25°C)	DESIGN CENTER	LIMITS MIN.	LIMITS MAX.	
Switching Characteristics (Common Emitter)				
D-C Base Current Gain (V_{CE} = 1 v; I_C = 8 ma), h_{FE}	30	17		
Saturation Voltage (I_B = .8 ma; I_C = 8 ma), V_{CE}	0.35			volts
Pulse Response Time (I_C = 8 ma)				
Delay & Rise Time, $t_d + t_r$	.5			μsec
Storage Time, t_s	.3			μsec
Fall Time, t_f	.2			μsec
Cutoff Characteristics				
Collector Cutoff Current (V_{CB} = 15 v), I_{CO}	.7		1.5	μa
Emitter Cutoff Current (V_{EB} = 5 v), I_{EO}	.6		5	μa
Collector to Emitter Voltage (Base open, I_C = 0.3 ma), V_{CE}		30		volts
High Frequency Characteristics (Common Base)				
(V_{CB} = 5v; I_E = 1 ma)				
Alpha Cutoff Frequency, f_{ab}	9.0	5.0		mc
Collector Capacity (f = 1 mc), C_{ob}	2.5		8	μμf
Voltage Feedback Ratio (f = 1 mc), h_{rb}	7.3			$\times 10^{-3}$
Low Frequency Characteristics (Common Base)				
(V_{CB} = 5v; I_E = −1 ma; f = 270 cps)				
Input Impedance, h_{ib}	55			ohms
Voltage Feedback Ratio, h_{rb}	1.5			$\times 10^{-4}$
Base Current Amplification, h_{fb}	−.985	−.952		
Output Admittance, h_{ob}	.2			μmhos

*Derate 1.1 mw/°C increase in ambient temperature.
**Derate 1.25 mw/°C increase in ambient temperature.

2N168A

Outline Drawing No. 3

The 2N168A is a rate grown NPN germanium transistor intended for mixer/oscillator and IF amplifier applications in radio receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity so that neutralization in many circuits is not required. The 2N168A has a frequency cutoff control to provide proper operation as an oscillator or autodyne mixer. For IF amplifier service the range in power gain in controlled to 3 db.

CONVERTER TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage	
Collector to Emitter (base open), V_{CEO}	15 volts
Collector to Base (emitter open), V_{CBO}	15 volts
Current	
Collector, I_C	20 ma
Power	
Collector Dissipation at 25°C*, P_{CM}	65 mw
Temperature Range	
Operating and Storage, T_A, T_{STG}	−55 to 85 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Converter Service

Maximum Ratings

Collector Supply Voltage, Vcc	12 volts

Design Center Characteristics	
Input Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC), Z_i	400 ohms
Output Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC), Z_o	12 K ohms
Voltage Feedback Ratio (I_E = 1 ma; V_{CB} = 5v; f = 1 mc), h_{rb}	5×10^{-3}
Collector to Base Capacitance (I_E = 1 ma; V_{CB} = 5v; f = 1 mc), C_{ob}	2.4 $\mu\mu$f
Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v), f_{ab}	8 mc
Min. Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v), f_{ab}	5 mc min
Base Current Gain (I_B = 20 μa; V_{CE} = 1v), h_{FE}	40
Minimum Base Current Gain, h_{FE}	23
Maximum Base Current Gain, h_{FE}	135
Conversion Gain, CG_e	25 db
IF Amplifier Performance	
Collector Supply Voltage, V_{CC}	5 volts
Collector Current, I_C	1 ma
Input Frequency, f	455 KC
Available Power Gain, G_e	39 db
Minimum Power Gain in typical IF circuit, G_e	28 db min
Power Gain Range of Variation in typical IF circuit, G_e	3 db
Cutoff Characteristics	
Collector Cutoff Current (V_{CB} = 5v), I_{CO}	.5 μa
Collector Cutoff Current (V_{CB} = 15v), I_{CO}	5 μa max

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.

2N169A, 2N169

Outline Drawing No. 3

The 2N169A and 2N169 are rate grown NPN germanium transistors intended for use as IF amplifiers in broadcast radio receivers. The collector capacity is controlled to a low value so that neutralization in most circuits is not required. The power gain at 455 KC is maintained at a 3 db spread for the 2N169A. The 2N169A is a special high voltage unit intended for second IF amplifier service where large voltage signals are encountered. The 2N169 is also intended for low gain IF amplifier and power detector applications.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)	**2N169A**	**2N169**	
Voltage			
Collector to Emitter (base open), V_{CEO}	25	15	volts
Collector to Base (emitter open), V_{CBO}	25	15	volts
Current			
Collector, I_C	20	20	ma
Power			
Collector Dissipation*, P_{CM}	65	65	mw
Temperature Range			
Operating and Storage, T_A, T_{STG}	−55 to 85	−55 to 85	°C
TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)			
IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage, V_{CC}	12	12	volts
Design Center Characteristics			
(I_E = −1 ma; V_{CE} = 5v; f = 455 KC except as noted)			
Input Impedance, Z_i	700	700	ohms
Output Impedance, Z_o	7	7	K ohms
Voltage Feedback Ratio (V_{CB} = 5v; f = 1 mc), h_{rb}	10	10	$\times 10^{-3}$
Collector to Base Capacitance (V_{CB} = 5v; f = 1 mc), C_{ob}	2.4	2.4	$\mu\mu$f
Frequency Cutoff (V_{CB} = 5v), f_{ab}	9	9	mc
Base Current Gain (I_B = 20 μa; V_{CE} = 1v), h_{FE}	72	72	
Minimum Base Current Gain, h_{FE}	36	36	
Maximum Base Current Gain, h_{FE}	220	220	
IF Amplifier Performance			
Collector Supply Voltage, V_{CC}	5	5	volts
Collector Current, I_C	1	1	ma
Input Frequency, f	455	455	KC
Available Power Gain, G_e	36	36	db
Minimum Power Gain in typical IF circuit, G_e	24	24	db min
Power Gain Range of Variation in typical IF circuit, G_e	3	3	db
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v), I_{CO}	.5	.5	μa
Collector Cutoff Current (V_{CB} = 15v), I_{CO}	5	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature.

2N170

Outline Drawing No. 3

The 2N170 is a rate grown NPN germanium transistor intended for use in high frequency circuits by amateurs, hobbyists, and experimenters. The 2N170 can be used in any of the many published circuits where a low voltage, high frequency transistor is necessary such as for regenerative receivers, high frequency oscillators, etc. If you desire to use the 2N170 NPN transistor in a circuit showing a PNP type transistor, it is only necessary to change the connections to the power supply.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage	
Collector to Emitter, V_{CE}	6 volts
Current	
Collector, I_C	20 ma
Power	
Collector Dissipation*, P_{CM}	25 mw
Temperature Range	
Operating and Storage, T_A, T_{STG}	−55 to 50 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

High Frequency Characteristics

(I_E = 1 ma; V_{CE} = 5v; f = 455 KC except as noted)

Input Impedance (Common Emitter), Z_I	800 ohms
Output Impedance (Common Emitter), Z_O	15 K ohms
Collector to Base Capacitance (f = 1 mc), C_{ob}	2.4 $\mu\mu$f
Frequency Cutoff (V_{CB} = 5V), f_{ab}	4 mc
Power Gain (Common Emitter), G_e	22 db

Low Frequency Characteristics

(I_E = 1 ma; V_{CE} = 5v; f = 270 cps)

Input Impedance, h_{ib}	55 ohms
Voltage Feedback Ratio, h_{rb}	4×10^{-4}
Current Gain, h_{fb}	.95
Output Admittance, h_{ob}	$.5 \times 10^{-6}$ μmhos
Common Emitter Base Current Gain, h_{fe}	20

Cutoff Characteristics

Collector Cutoff Current (V_{CB} = 5v), I_{CO}	5 μa max

*Derate 1 mw/°C increase in ambient temperature.

2N186, 2N187, 2N188

Outline Drawing No. 1

The 2N186, 2N187, and 2N188 are medium power PNP transistors, intended for use as audio output amplifiers in radio receivers and quality sound systems. By unique process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain provides low distortion in Class B circuits, and permits use of any two transistors from a particular type without matching.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages	
Collector to Base (emitter open), V_{CBO}	−25 volts
Collector to Emitter (R_{EB} = 10K ohm), V_{CER}	−25 volts
Emitter to Base (collector open), V_{EBO}	− 5 volts
Collector Current, I_C	−200 ma
Power	
Collector Dissipation*, P_{CM}	100 mw
Temperature	
Operating Range, T_A	−55 to 60 °C
Storage Range, T_{STG}	−55 to 85 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Class B Audio Amplifier Operation

(Values for two transistors. Note that matching is not required to hold distortion to less than 5% for any two transistors from a type)

	2N186	2N187	2N188	
Maximum Class B Ratings (Common Emitter)				
Collector Supply Voltage, V_{CC}	−12	−12	−12	volts
Power Output (Distortion less than 5%), P_o	300	300	300	mw
Design Center Characteristics				
Input Impedance large signal base to base ($\triangle I_E = 100$ ma), h_{ie}	1200	2000	2600	ohms
Base Current Gain ($V_{CE} = -1$ v; $I_C = 100$ ma), h_{FE}	24	36	54	
Collector Capacity ($V_{CB} = -5$ v; $I_E = 1$ ma; $f = 1$ mc), C_{ob}	40	40	40	$\mu\mu$f
Frequency Cutoff ($V_{CE} = -5$ v; $I_E = 1$ ma), f_{ab}	.8	1.0	1.2	mc
Class B Circuit Performance (Common Emitter)				
Collector Voltage, V_{CC}	−12	−12	−12	volts
Minimum Power Gain at 100 mw power output, G_e	28	30	32	min db
Cutoff Characteristics				
Maximum Collector Cutoff Current ($V_{CB} = -25$ v), I_{CO}	16	16	16	max μa
Maximum Emitter Cutoff Current ($V_{EB} = -5$ v), I_{EO}	10	10	10	max μa

*Derate 3 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N186A, 2N187A 2N188A

Outline Drawing No. 1

The 2N186A, 2N187A, and 2N188A are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By unique process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain provides low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages

Collector to Base (emitter open), V_{CBO}	−25 volts
Collector to Emitter ($R_{EB} = 10$K ohm), V_{CER}	−25 volts
Emitter to Base (collector open), V_{EBO}	− 5 volts
Collector Current, I_C	−200 ma
Power	
Collector Dissipation*, P_{CM}	200 mw
Temperature	
Operating Range, T_A	−55 to 75 °C
Storage Range, T_{STG}	−55 to 85 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

	2N186A	2N187A	2N188A	
Class B Audio Amplifier Operation (Values for two transistors. Note that matching is not required to hold distortion to less than 5% for any two transistors from a type)				
Maximum Class B Ratings (Common Emitter)				
Collector Supply Voltage, V_{CC}	−12	−12	−12	volts
Power Output (Distortion less than 5%), P_o	750	750	750	mw
Design Center Characteristics				
Input Impedance large signal base to base ($\triangle I_E = 100$ ma), h_{ie}	1200	2000	2600	ohms
Base Current Gain ($V_{CE} = -1$ v; $I_C = 100$ ma), h_{FE}	24	36	54	
Collector Capacity ($V_{CB} = 5$ v; $I_E = 1$ ma; $f = 1$ mc), C_{ob}	40	40	40	$\mu\mu$f
Frequency Cutoff ($V_{CB} = -5$ v; $I_E = 1$ ma), f_{ab}	.8	1.0	1.2	mc
Class B Circuit Performance (Common Emitter)				
Collector Voltage, V_{CC}	−12	−12	−12	volts
Minimum Power Gain at 100 mw power output, G_e	28	30	32	min db
Class A Audio Amplifier Operation (Common Emitter) ($V_{CC} = 12$v; $I_E = 10$ ma)				
Power Gain at 50 mw power output, G_e	30	32	34	db
Cutoff Characteristics				
Maximum Collector Cutoff Current ($V_{CB} = -25$ v), I_{CO}	16	16	16	max μa
Maximum Emitter Cutoff Current ($V_{EB} = -5$ v), I_{EO}	10	10	10	max μa

*Derate 4 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N189, 2N190, 2N191, 2N192

Outline Drawing No. 1

The 2N189, 2N190, 2N191, and 2N192 are alloy junction PNP transistors intended for driver service in transistorized audio amplifiers. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage		
Collector to Emitter (R_{EB} = 10K ohm), V_{CER}		−25 volts
Collector Current, I_C		−50 ma
Power		
Collector Dissipation (25°C)*, P_{CM}		75 mw
Temperature		
Operating Range, T_A		−55 to 60 °C
Storage Range, T_{STG}		−55 to 85 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

	2N189	2N190	2N191	2N192	
Audio Driver Class A Operation (Values for one transistor driving a transformer coupled output stage)					
Maximum Class A Ratings (Common Emitter)					
Collector Supply Voltage, V_{CC}	−12	−12	−12	−12	volts
Design Center Characteristics					
Input Impedance base to emitter (I_E = 1 ma), h_{ie}	1000	1400	1800	2200	ohms
Base Current Gain (V_{CE} = −5 v; I_E = 1 ma), h_{fe}	24	36	54	75	
Collector Capacity (V_{CB} = −5 v; I_E = 1 ma), C_{ob}	40	40	40	40	$\mu\mu$f
Frequency Cutoff (V_{CB} = −5 v; I_E = 1 ma), f_{ab}	.8	1.0	1.2	1.5	mc
Noise Figure (V_{CB} = −5 v; I_E = 1 ma; f = 1 KC; BW = 1 cycle), NF	15	15	15	15	db
Audio Circuit Performance (Common Emitter)					
Collector Supply Voltage, V_{CC}	−12	−12	−12	−12	volts
Emitter Current, I_E	1	1	1	1	ma
Minimum Power Gain at 1 mw power output, G_e	37	39	41	43	min db
Small Signal Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)					
Input Impedance, h_{ib}	29	29	29	29	ohms
Voltage Feedback Ratio, h_{rb}	4	4	4	4	$\times 10^{-4}$
Current Amplification, h_{fb}	−.96	−.973	−.98	−.987	
Output Admittance, h_{ob}	1.0	.8	.6	.5	μmhos
Cutoff Characteristics					
Maximum Collector Cutoff Current (V_{CB} = −25 v), I_{CO}	16	16	16	16	max μa

*Derate 2 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N241, 2N241A

Outline Drawing No. 1

The 2N241, and 2N241A are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By special process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain insures low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

		2N241	2N241A	
Voltages				
Collector to Base (emitter open)	V_{CBO}	−25	−25	volts
Collector to Emitter (R_{EB} = 10K ohm)	V_{CER}	−25	−25	volts
Emitter to Base (collector open)	V_{EBO}	− 5	− 5	volts
Collector Current	I_C	−200	−200	ma
Power Collector Dissipation	P_{CM}	100*	200**	mw
Temperature				
Operating Range	T_A	−55 to 60	−55 to 75	°C
Storage Range	T_{STG}	−55 to 85	−55 to 85	°C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Class B Audio Amplifier Operation

(Values for two transistors. Note that matching is not required to hold distortion to less than 5% for any two transistors from a type)

		2N241	2N241A	
Maximum Class B Ratings (Common Emitter)				
Collector Supply Voltage	V_{CC}	−12	−12	volts
Power Output (Distortion less than 5%)	P_o	300	750	mw
Design Center Characteristics				
Input Impedance large signal base to base ($\triangle I_E$ = 100 ma)	h_{ie}	400*	400*	ohms
Base Current Gain (V_{CE} = −1v; I_C = 100 ma)	h_{FE}	73	73	
Collector Capacity (V_{CB} = −5v; I_E = 1 ma; f = 1 mc)	C_{ob}	40	40	$\mu\mu$f
Frequency Cut off (V_{CE} = −5v; I_E = 1 ma)	f_{ab}	1.3	1.3	mc
Class B Circuit Performance (Common Emitter)				
Collector Voltage	V_{CC}	−12	−12	volts
Minimum Power Gain at 100 mw power output	G_e	34	34	min db
Class A Audio Amplifier Operation (Common Emitter)				
(V_{CC} = −12v; I_E = 10 ma)				
Power Gain at 50 mw power output	G_e	35	35	db
Cutoff Characteristics				
Maximum Collector Cutoff Current (V_{CB} = −25v)	I_{CO}	16	16	max μa
Maximum Emitter Cutoff Current (V_{EB} = −5v)	I_{EO}	10	10	max μa

*Derate 3 mw/°C increase in ambient temperature within range 25°C to 60°C.
**Derate 4 mw/°C increase in ambient temperature within range 25°C to 75°C.

The 2N265 is an alloy junction PNP transistor intended for driver service in transistorized audio amplifiers. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

2N265

Outline Drawing No. 1

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltage
Collector to Emitter (R_{EB} = 10K ohm), V_{CER} . . . . . −25 volts

Collector Current, I_C . . . . . −50 ma

Power
Collector Dissipation (25°C)*, P_{CM} . . . . . 75 mw

Temperature
Operating Range, T_A . . . . . −55 to 60 °C
Storage Range, T_{STG} . . . . . −55 to 85 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

Audio Driver Class A Operation

(Values for one transistor driving a transformer coupled output stage)

Maximum Class A Ratings (Common Emitter)
Collector Supply Voltage, V_{CC} . . . . . −12 volts

Design Center Characteristics
Input Impedance base to emitter (I_E = 1 ma), h_{ie} . . . . . 4000 ohms
Base Current Gain (V_{CE} = −5 v; I_E = 1 ma), h_{re} 110
Collector Capacity (V_{CB} = −5 v; I_E = 1 ma), C_{ob} . . . . . 40 $\mu\mu$f
Frequency Cutoff (V_{CB} = −5 v; I_E = 1 ma), f_{ab} . . . . . 1.5 mc
Noise Figure (V_{CB} = −5 v; I_E = I ma; f = 1 KC; BW = 1 cycle), NF . . . . . 15 db

Audio Circuit Performance (Common Emitter)
Collector Supply Voltage, V_{CC} . . . . . −12 volts
Emitter Current, I_E . . . . . 1 ma
Minimum Power Gain at 1 mw power output, G_e . . . . . 45 min db

Small Signal Characteristics (Common Base)
(V_{CB} = −5v; I_E = 1 ma; f = 270 cps)
Input Impedance, h_{ib} . . . . . 29 ohms
Voltage Feedback Ratio, h_{rb} . . . . . 4×10^{-4}
Current Amplification, h_{fb} . . . . . −.991
Output Admittance, h_{ob} . . . . . .5 μmhos

Cutoff Characteristics
Maximum Collector Cutoff Current (V_{CB} = −25 v), I_{CO} . . . . . 16 max μa

*Derate 2 mw/°C increase in ambient temperature within range 25°C to 60°C.

2N292, 2N293

Outline Drawing No. 3

Types 2N292 and 2N293 are rate grown NPN germanium transistors intended for amplifier applications in radio receivers. Special manufacturing techniques provide a low value and a narrow spread in collector capacity so that neutralization in many circuits is not required. The type 2N293 is intended for receiver circuits where high gain is needed. In IF amplifier service the range in power gain is controlled to 3 db.

IF TRANSISTOR SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)	2N292	2N293	
Voltage			
Collector to Emitter (base open), V_{CEO}	15	15	volts
Collector to Base (emitter open), V_{CBO}	15	15	volts
Current			
Collector, I_C	20	20	ma
Power			
Collector Dissipation*, P_{CM}	65	65	mw
Temperature Range			
Operating and Storage, T_A, T_{STG}	−55 to 85	−55 to 85	°C
ELECTRICAL CHARACTERISTICS: (25°C)**			
IF Amplifier Service			
Maximum Ratings			
Collector Supply Voltage, V_{CC}	12	12	volts
Design Center Characteristics			
Input Impedance (I_E = 1 ma; V_{CB} = 5v; f = 455 KC), Z_i	350	350	ohms
Output Impedance (I_E = 1 ma; V_{CE} = 5v; f = 455 KC), Z_o	16	18	K ohms
Voltage Feedback Ratio (I_E = 1 ma; V_{CB} = 5v; f = mc), h_{rb}	10	5	$\times 10^{-3}$
Collector to Base Capacitance (I_E = 1 ma; V_{CB} = 5v; f = 1 mc), C_{ob}	2.4	2.4	$\mu\mu$f
Frequency Cutoff (I_E = 1 ma; V_{CB} = 5v), f_{ab}	6	7	mc
Base Current Gain (I_B = 20 μa; V_{CE} = 1v), h_{FE}	25	25	
Min. Base Current Gain, h_{FE}	6	6	
Max. Base Current Gain, h_{FE}	44	55	
IF Amplifier Performance			
Collector Supply Voltage, V_{CC}	5	5	volts
Collector Current, I_C	1	1	ma
Input Frequency, f	455	455	KC
Available Power Gain, G_e	36	39	db
Min. Power Gain in Typical IF Test Circuit, G_e	24	28	db min
Power Gain Range of Variation in Typical IF Circuit	3	3	db
Cutoff Characteristics			
Collector Cutoff Current (V_{CB} = 5v), I_{CO}	.5	.5	μa
Collector Cutoff Current (V_{CB} = 15v), I_{CO}	5	5	μa max

*Derate 1.1 mw/°C increase in ambient temperature over 25°C.
**All values are typical unless indicated as a min or max.

2N319, 2N320, 2N321

Outline Drawing No. 2

The 2N319, 2N320, and 2N321 are miniaturized versions of the 2N186A series of G-E transistors. Like the prototype versions, the 2N319, 2N320, and 2N321 are medium power PNP transistors intended for use as audio output amplifiers in radio receivers and quality sound systems. By unique process controls the current gain is maintained at an essentially constant value for collector currents from 1 ma to 200 ma. This linearity of current gain provides low distortion in both Class A and Class B circuits, and permits the use of any two transistors from a particular type without matching in Class B Circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)		
Voltages		
Collector to Emitter	V_{CE}	−20 volts
Collector to Base	V_{CB}	−30 volts
Emitter to Base	V_{EB}	− 3 volts
Collector Current	I_C	−200 ma

Power					
Collector Dissipation	P_{CM}				200 mw
Temperature					
Operating and Storage Range	T_A-T_{STG}				−65 to 85 °C
TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)					
D.C. Characteristics		2N319	2N320	2N321	
Base Current Gain (I_C = −20 ma; V_{CE} = −1v)	h_{FE}	33	48	80	
Base Current Gain (I_C = −100 ma; V_{CE} = −1v)	h_{FE}	30	44	70	
Collector to Emitter Voltage (R_{EB} = 10K; I_C = .6 ma)	V_{CER}	−20	−20	−20	volts
Collector Cutoff Current (V_{EB2} −25v)	I_{CO}	8	8	8	μa
Maximum Collector Cutoff Current (V_{CB} = −25v)	I_{CO}	16	16	16	μa
Emitter Cutoff Current (V_{EB} = 3v)	I_{EO}	2	2	2	μa
Small Signal Characteristics (Common Base) (V_{CB} = −5v; I_E = 1 ma; f = 270 cps)					
Frequency Cutoff	f_{ab}	2.0	2.5	3.1	mc
Collector Capacity (f = 1 mc)	C_{ob}	25	25	25	μμf
Noise Figure	NF	6	6	6	db
Input Impedance	h_{IB}	30	30	30	ohms
Thermal Characteristics					
Thermal Resistance					
Without Heat Sink (Junction to Air)		.27	.27	.27	°C/mw
With Clip On Heat Sink (Junction to Case)		.2	.2	.2	°C/mw
Performance Data (Common Emitter)					
Class A Power Gain (V_{CC} = −9v)	G_e	30	31	32	db
Power Output	P_o	50	50	50	mw
Class B Power Gain (V_{CC} = −9v)	G_e	27	29	31	db
Power Output	P_o	100	100	100	mw

2N322, 2N323, 2N324

Outline Drawing No. 2

The 2N322, 2N323, 2N324 are alloy junction PNP transistors intended for driver service in audio amplifiers. They are miniaturized versions of the 2N190 series of G.E. transistors. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)					
Voltages					
Collector to Emitter	V_{CE}				−16 volts
Collector to Base	V_{CB}				−16 volts
Collector Current	I_C				−100 ma
Power					
Collector Dissipation	P_{CM}				140 mw
Temperature					
Operating and Storage Range	T_A-T_{STG}				−65 to + 65 °C
TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)					
D.C. Characteristics		2N322	2N323	2N324	
Base Current Gain (I_C = −20 ma; V_{CE} = −1v)	h_{FE}	48	80	95	
Collector to Emitter Voltage (R_{EB} = 10K; I_C = −.6 ma)	V_{CER}	16	16	16	volts
Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	10	10	10	μa
Max. Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	16	16	16	μa
Small Signal Characteristics					
Frequency Cutoff (V_{CB} = −5v; I_E = 1 ma)	f_{ab}	2.5	3.1	3.4	mc
Collector Capacity (V_{CB} = −5v; I_E = 1 ma)	C_{ob}	25	25	25	μμf
Noise Figure (V_{CB} = −5v; I_E = 1 ma)	NF	6	6	6	db
Input Impedance (V_{CE} = −5v; I_E = 1 ma)	h_{ie}	2200	2600	3300	ohms
Current Gain (V_{CE} = −5v; I_E = 1 ma)	h_{fe}	50	70	84	
Thermal Characteristics					
Thermal Resistance Junction to Air		.27	.27	.27	°C/mw
Performance Data Common Emitter					
Power Gain Driver (V_{CC} = 9v)	G_e	39	41	43	db
Power Output	P_o	1	1	1	mw

2N332

Outline Drawing No. 4

The General Electric Type 2N332 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt
Collector Current	I_C	25 ma
Power		
Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (100°C)	P_C	100 mw
Collector Dissipation (150°C)	P_C	50 mw
Temperature Range		
Storage	T_{STG}	−65 to 200 °C
Operating	T_A	−55 to 175 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; f = 1kc)

		MIN.	NOM.	MAX.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	9	15	20	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.25	1.0	5.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.25	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2$ma; f = 1kc; R_G = 1K ohms; R_L = 20K ohms)	G_e		35		db
Noise Figure	NF		28		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ma)	$f_{\alpha b}$		15		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ma; f = 1mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ma; f= 5mc)	G_e		17		db
D-C Characteristics					
Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance (I_B = 1ma; I_C = 5ma)	Rsc		80	200	ohms
Switching Characteristics					
($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)					
Delay Time	td		.75		μsec
Rise Time	tr		.5		μsec
Storage Time	ts		.05		μsec
Fall Time	tf		.15		μsec

2N333

Outline Drawing No. 4

The General Electric Type 2N333 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages

Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt

Collector Current

	I_C	25 ma

Power

Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (100°C)	P_C	100 mw
Collector Dissipation (150°C)	P_C	50 mw

Temperature Range

Storage	T_{STG}	−65 to 200 °C
Operating	T_A	−55 to 175 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; f = 1kc)

Small Signal Characteristics		MIN.	NOM.	MAX.	
Current Transfer Ratio	h_{fe}	18	30	41	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.25	2.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.2	1.2	μmhos
Power Gain ($V_{CB} = 20v$; $I_E = -2$ma; f = 1kc; R_G = 1K ohms; R_L = 20K ohms)	G_e		39		db
Noise Figure	NF		25		db

High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1$ma)	f_{ab}		17		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1$ma; f = 1mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2$ma; f= 5mc)	G_e		16		db

D-C Characteristics					
Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1$ma; $I_C = 5$ma)	Rsc		80	200	ohms

Switching Characteristics					
($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)					
Delay Time	t_d		.7		μsec
Rise Time	t_r		.4		μsec
Storage Time	t_s		.15		μsec
Fall Time	t_f		.18		μsec

2N334

Outline Drawing No. 4

The General Electric Type 2N334 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt
Collector Current	I_C	25 ma
Power		
Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (100°C)	P_C	100 mw
Collector Dissipation (150°C)	P_C	50 mw
Temperature Range		
Storage	T_{STG}	−65 to 200 °C
Operating	T_A	−55 to 175 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; f = 1kc)

		MIN.	NOM.	MAX.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	18	39	90	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.5	3.5	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.18	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2ma$; f = 1kc; R_G = 1K ohms; R_L = 20K ohms)	G_e		40		db
Noise Figure	NF		25		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1ma$)	$f_{\alpha b}$	8.0	20		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1ma$; f = 1mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2ma$; f= 5mc)	G_e		15		db
D-C Characteristics					
Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1ma$; $I_C = 5ma$)	R_{SC}		80	200	ohms
Switching Characteristics					
($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)					
Delay Time	t_d		.65		μsec
Rise Time	t_r		.4		μsec
Storage Time	t_s		.2		μsec
Fall Time	t_f		.18		μsec

2N335

Outline Drawing No. 4

The General Electric Type 2N335 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages

Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt

Collector Current

	I_C	25 ma

Power

Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (100°C)	P_C	100 mw
Collector Dissipation (150°C)	P_C	50 mw

Temperature Range

Storage	T_{STG}	−65 to 200 °C
Operating	T_A	−55 to 175 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; f = 1kc)

Small Signal Characteristics

		MIN.	NOM.	MAX.	
Current Transfer Ratio	h_{fe}	37	60	90	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	5	3.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.15	1.2	μmhos
Power Gain ($V_{CB} = 20v$; $I_E = -2ma$; f = 1kc; R_G = 1K ohms; R_L = 20K ohms)	G_e		42		db
Noise Figure	NF		20		db

High Frequency Characteristics

Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1ma$)	f_{ab}		22		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1ma$; f = 1mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2ma$; f = 5mc)	G_e		14		db

D-C Characteristics

Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1ma$; $I_C = 5ma$)	R_{SC}		80	200	ohms

Switching Characteristics

($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)

Delay Time	t_d		.65	μsec
Rise Time	t_r		.35	μsec
Storage Time	t_s		.25	μsec
Fall Time	t_f		.19	μsec

2N336

Outline Drawing No. 4

The General Electric Type 2N336 is a silicon NPN triode transistor intended for amplifier applications in the audio and radio frequency range and for general purpose switching. It is a grown junction device with a diffused base. Electrical stability is insured by means of a minimum 150 hour 200°C cycled aging operation included in the manufacturing process. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. This transistor is hermetically sealed in a welded case. The case dimensions and lead configuration conform to the JETEC TO-5 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base (Emitter Open)	V_{CBO}	45 volts
Emitter to Base (Collector Open)	V_{EBO}	1 volt
Collector Current	I_C	25 ma
Power		
Collector Dissipation (25°C)	P_C	150 mw
Collector Dissipation (100°C)	P_C	100 mw
Collector Dissipation (150°C)	P_C	50 mw
Temperature Range		
Storage	T_{STG}	−65 to 200 °C
Operating	T_A	−55 to 175 °C

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified; $V_{CB} = 5v$; $I_E = -1$ ma; f = 1kc)

		MIN.	NOM.	MAX.	
Small Signal Characteristics					
Current Transfer Ratio	h_{fe}	76	120	333	
Input Impedance	h_{ib}	30	53	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}	.5	4.0	10.0	$\times 10^{-4}$
Output Admittance	h_{ob}	0.0	.13	1.2	μmhos
Power Gain ($V_{CE} = 20v$; $I_E = -2ma$; f = 1kc; R_G = 1K ohms; R_L = 20K ohms)	G_e		43		db
Noise Figure	NF		15		db
High Frequency Characteristics					
Frequency Cutoff ($V_{CB} = 5v$; $I_E = -1ma$)	f_{ab}		23		mc
Collector to Base Capacity ($V_{CB} = 5v$; $I_E = -1ma$; f = 1mc)	C_{ob}		7		$\mu\mu$f
Power Gain (Common Emitter) ($V_{CB} = 20v$; $I_E = -2ma$; f= 5mc)	G_e		13		db
D-C Characteristics					
Collector Breakdown Voltage ($I_{CBO} = 50\mu a$; $I_E = 0$; $T_A = 25°C$)	BV_{CBO}	45			volts
Collector Cutoff Current ($V_{CB} = 30v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.02	2	μa
($V_{CB} = 5v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			50	μa
Collector Saturation Resistance ($I_B = 1ma$; $I_C = 5ma$)	R_{SC}		80	200	ohms
Switching Characteristics					
($I_{B_1} = 0.4$ ma; $I_{B_2} = -0.4$ ma; $I_C = 2.8$ ma)					
Delay Time	t_d		.65		μsec
Rise Time	t_r		.2		μsec
Storage Time	t_s		.5		μsec
Fall Time	t_f		.2		μsec

The General Electric types 2N394, 2N395 are PNP alloy junction high frequency switching transistors intended for military, industrial, and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

2N394, 2N395

Outline Drawing No. 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

		2N394	2N395	
Voltages				
Collector to Emitter	V_{CE}	−10	−15	volts
Collector to Base	V_{CB}	−10	−15	volts
Emitter to Base	V_{EB}	−10	−10	volts
Collector Current	I_C	−200	−200	ma
Power Dissipation	P_{AV}	150	150	mw
Peak Power Dissipation (50 μsec. max. 20% duty cycle)	P_M	500	500	mw
Storage Temperature	T_{STG}	−65 to 100	−65 to 100	°C

ELECTRICAL CHARACTERISTICS: (25°C)

High Frequency Characteristics (Common Base) ($V_{CB} = -5v$; $I_E = 1$ ma)		2N394 MIN.	2N394 MAX.	2N394 DESIGN CENTER	2N395 MIN.	2N395 MAX.	2N395 DESIGN CENTER	
Alpha Cutoff Frequency	$f_{\alpha b}$	4		5.5	5		7	mc
Collector Capacity (f = 1 mc)	C_{ob}		20	12		20	12	μμf
Voltage Feedback Ratio (f = 1 mc)	h_{rb}			10			9×10^{-3}	
Base Spreading Resistance	r'_b			150			130	ohms
Cutoff Characteristics								
Collector Cutoff Current ($V_{CBO} = -10v$)	I_{CO}		−6					μamps
($V_{CBO} = -15v$)	I_{CO}					−6		μamps
Emitter Cutoff Current ($V_{EBO} = -5v$)	I_{EO}		−6					μamps
($V_{EBO} = -10v$)	I_{EO}					−6		μamps
Punch-through Voltage	V_{PT}	−10			−15			volts
D-C Characteristics								
D-C Base Current Gain ($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	20	150		25	150		
($V_{CE} = -0.5v$; $I_C = -100$ ma)	h_{FE}				20			
Saturation Voltage ($I_B = -1$ ma; $I_C = -20$ ma)	V_{CE} (SAT)			−0.1			−0.1	volts
Pulse Response Time ($I_C = -5$ ma; $I_{B_1} = I_{B_2} = 0.5$ ma)								
Delay and Rise Time	$t_d + t_r$			0.9			0.9	μsec
Storage Time	t_s			0.35			0.28	μsec
Fall Time	t_f			0.35			0.28	μsec

Thermal Characteristics

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N396, 2N397

Outline Drawing No. 2

The General Electric types 2N396, 2N397 are PNP alloy junction high frequency switching transistors intended for military, industrial, and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

		2N396	2N397	
Voltages				
Collector to Emitter	V_{CE}	−20	−10	volts
Collector to Base	V_{CB}	−20	−10	volts
Emitter to Base	V_{EB}	−10	−10	volts
Collector Current	I_C	−200	−250	ma
Power Dissipation	P_{AV}	150	150	mw
Peak Power Dissipation (50 μsec. max. 20% duty cycle)	P_M	500	500	mw
Storage Temperature	T_{STG}	−65 to 100	−65 to 100	°C

ELECTRICAL CHARACTERISTICS: (25°C)

		2N396			2N397			
High Frequency Characteristics		MIN.	MAX.	DESIGN CENTER	MIN.	MAX.	DESIGN CENTER	
(Common Base) ($V_{CB} = -5v$; $I_E = 1$ ma)								
Alpha Cutoff Frequency	$f_{\alpha b}$	5.0		7	8		10	mc
Collector Capacity ($f = 1$ mc)	C_{ob}		20	12		20	12	μμf
Voltage Feedback Ratio ($f = 1$ mc)	h_{rb}			10			11 × 10⁻³	
Base Spreading Resistance	r'_b			140			160	ohms
Cutoff Characteristics								
Collector Cutoff Current ($V_{CBO} = -10v$)	I_{CO}					−6		μamps
($V_{CBO} = -20v$)	I_{CO}		−6					μamps
Emitter Cutoff Current ($V_{EBO} = -10v$)	I_{EO}		−6			−6		μamps
Punch-through Voltage	V_{PT}	−20			−10			volts
D-C Characteristics								
D-C Base Current Gain ($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	30	150		30	150		
($V_{CE} = -0.5v$; $I_C = -100$ ma)	h_{FE}	20						
($V_{CE} = -0.35v$; $I_C = -200$ ma)	h_{FE}				20			
Saturation Voltage ($I_B = -1$ ma; $I_C = -20$ ma)	V_{CE} (SAT)		−0.2	−0.09			−0.085	volts
Pulse Response Time ($I_C = -5$ ma; $I_{B_1} = I_{B_2} = 0.5$ ma)								
Delay and Rise Time	$t_d + t_r$			0.9			0.66	μsec
Storage Time	t_s			0.35			0.35	μsec
Fall Time	t_f			0.25			0.25	μsec

Thermal Characteristics

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N450

Outline Drawing No. 8

The General Electric Type 2N450 is a PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	−20 volts
Collector to Emitter	V_{CE}	−12 volts
Emitter to Base	V_{EB}	−5 volts
Collector Current	I_C	−125 ma
Temperature		
Storage	T_{STG}	−65 to 85 °C
Junction	T_J	85 °C
Power		
Total Transistor Dissipation	P_{AV}	150 mw

ELECTRICAL CHARACTERISTICS: (25°C)

High Frequency Characteristics (Common Base) ($V_{CB} = -5v$; $I_E = 1$ ma)		MIN.	MAX.	DESIGN CENTER	
Alpha Cutoff Frequency	f_{ab}	5			mc
Collector Capacity ($f = 1$ mc)	C_{ob}		16	12	$\mu\mu$f
Voltage Feedback Ratio ($f = 1$ mc)	h_{rb}		13	10	$\times 10^{-3}$
Cutoff Characteristics					
Breakdown Voltage Collector to Base to Base Emitter Open ($I_C = -100$ μamps)	BV_{CBO}	−20			volts
Breakdown Voltage Collector to Emitter Base Open ($I_C = -600$ μamps)	BV_{CEO}	−12			volts
Collector Cutoff Current ($V_{CBO} = -6v$)	I_{CBO}		−6	−2	μamps
Emitter Cutoff Current ($V_{EBO} = -5v$)	I_{EBO}		−6	−2	μamps
D-C Characteristics					
D-C Base Current Gain ($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	30			
Saturation Voltage ($I_B = -5$ ma; $I_C = -10$ ma)	V_{CE} (SAT)		−0.2		volts

2N451

Outline Drawing No. 6

The General Electric Type 2N451 is an NPN silicon power transistor intended for general application at low to medium-high frequencies where large amounts of power are required at high operating temperatures. The high collector current rating in combination with the low saturation resistance and low thermal resistance of this device make it useful in a wide variety of applications. A single Type 2N451 in a Class A circuit is capable of 25 watts output at a mounting base temperature of +30°C. A pair of Type 2N451 units in Class B will deliver 50 watts output at mounting base temperatures up to +100°C. The high cut-off frequency of the Type 2N451 makes it useful in common-emitter amplifier circuits at frequencies up to 500 kc or more. The Type 2N451 transistor is a diffused-junction device manufactured by the General Electric vapor diffusion process. It is hermetically sealed in a welded case which is designed for mounting on an external heat sink by means of a simple threaded stud. The type 2N451 transistor is designed to meet the requirements of MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS		
Temperature Range		
Storage	T_{STG}	−65 to + 150 °C
Junction (Operating)	T_J	+ 150 °C
Voltages		
Collector-Base	V_{CB}	65 volts
Emitter-Base	V_{EB}	10 volts
Collector-Emitter ($R_{BE} \leqq 50$ ohms)	V_{CE}	65 volts
Currents		
Base		0.5 amps
Collector		5 amps
Collector DC Power Dissipation		
25°C Mounting Base Temp.		85 watts
100°C Mounting Base Temp.		35 watts

ELECTRICAL CHARACTERISTICS					
D-C Characteristics (25°C Mtg. Base Temp. except where otherwise indicated)		MIN.	NOM.	MAX.	
Collector Reverse Current ($V_{CB} = +65v$)	I_{CBO}			20	ma
($V_{CE} = +30v$; $R_{BE} \leqq 50$ Ω; $T_A = +125$°C)	I_{CER}			20	ma
Collector Saturation Resistance ($I_C = 1$ amp; $I_B = 0.3$ amp.)	R_{SE}		2	4	ohms
Forward Current Transfer Ratio ($I_C = 1$ amp; $V_{CE} = 10v$)	h_{FE}	10			
Input Resistance ($I_C = 1$ amp; $V_{CE} = 10v$)	h_{IE}		25		ohms
A-C Characteristics (Common Emitter) ($V_{CE} = 30v$; $I_C = 1$ amp)					
Forward Current Transfer Ratio ($I_C = 0.5$ amp rms; $f = 1$ kc)			14		
Input Resistance ($I_C = 0.5$ amp rms; $f = 1$ kc)			20		ohms
Frequency Cutoff (3db)	f_{ae}		400		kc
Thermal Characteristics					
Thermal resistance from collector junction to mounting base				1.5	°C/watt

2N452

Outline Drawing No. 6

The General Electric Type 2N452 features very low collector saturation resistance and high current capability. These characteristics make this transistor particularly suitable for high power amplifier and switching applications. The Type 2N452 transistor is a diffused-junction device manufactured by the General Electric vapor diffusion process. It is hermetically sealed in a welded case which is designed for mounting on an external heat sink by means of a simple threaded stud. The Type 2N452 transistor is designed to meet the requirements of MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range		
Storage	T_{STG}	−65 to + 150 °C
Junction (Operating)	T_J	+ 150 °C
Voltages		
Collector-Base	V_{CB}	65 volts
Emitter-Base	V_{EB}	10 volts
Collector-Emitter ($R_{BE} \leqq 50$ ohms)	V_{CE}	65 volts
Currents		
Base		0.5 amps
Collector		5 amps
Collector DC Power Dissipation		
25°C Mounting Base Temp.		85 watts
100°C Mounting Base Temp.		35 watts

ELECTRICAL CHARACTERISTICS

D-C Characteristics (25°C Mtg. Base Temp. except where otherwise indicated)		MIN.	NOM.	MAX.	
Collector Reverse Current ($V_{CB} = +65$v)	I_{CBO}			50	ma
($V_{CE} = +65$v; $R_{BE} \leqq 50\ \Omega$; $T_A = +125$°C)	I_{CER}			50	ma
Collector Saturation Resistance ($I_C = 2$ amp; $I_B = 0.5$ amp.)	R_{SE}			2.5	ohms
Forward Current Transfer Ratio ($I_C = 2$ amp; $V_{CE} = 20$v)	h_{FE}	8			
Input Resistance ($I_C = 2$ amp; $V_{CE} = 20$v)	h_{IE}		15		ohms
Thermal Characteristics					
Thermal resistance from collector junction to mounting base				1.5	°C/watt

2N453

Outline Drawing No. 6

The General Electric Type 2N453 features a high forward current transfer ratio. This transistor is especially well suited as a series regulator element in d-c regulated power supplies and generally as a high gain, medium power amplifier at frequencies up to several hundred kc. The Type 2N453 transistor is a diffused-junction device manufactured by the General Electric vapor diffusion process. It is hermetically sealed in a welded case which is designed for mounting on an external heat sink by means of a simple threaded stud. The Type 2N453 transistor is designed to meet the requirements of MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Range		
Storage	T_{STG}	−65 to + 150 °C
Junction (Operating)	T_J	+ 150 °C
Voltages		
Collector-Base	V_{CB}	30 volts
Emitter-Base	V_{EB}	10 volts
Collector-Emitter ($R_{BE} \leqq 50$ ohms)	V_{CE}	30 volts
Currents		
Base		0.5 amps

Collector (For good performance, maximum collector current should be limited to 2 amps.)					5 amps
Collector DC Power Dissipation					
25°C Mounting Base Temp.					85 watts
100°C Mounting Base Temp.					35 watts
ELECTRICAL CHARACTERISTICS					
D-C Characteristics					
(25°C Mtg. Base Temp. except where otherwise indicated)		MIN.	NOM.	MAX.	
Collector Reverse Current ($V_{CB} = +30v$) ($V_{CE} = +30v$; $R_{BE} \leqq 50\ \Omega$; $T_A = +125°C$)	I_{CEO}			20	ma
Collector Saturation Resistance ($I_C = 1$ amp; $I_B = 0.3$ amp.)	I_{CER}			20	ma
Forward Current Transfer Ratio ($I_C = 1$ amp; $V_{CE} = 20v$)	R_{SE}			6	ohms
Input Resistance ($I_C = 1$ amp; $V_{CE} = 20v$)	h_{FE}	20			
	h_{IE}		50		ohms
Thermal Characteristics					
Thermal resistance from collector junction to mounting base				1.5	°C/watt

2N454

Outline Drawing No. 6

The General Electric Type 2N454 is an NPN silicon power transistor intended for use as a general purpose, medium power amplifier at frequencies up to several hundred kc. The Type 2N454 transistor is a diffused-junction device manufactured by the General Electric vapor diffusion process. It is hermetically sealed in a welded case which is designed for mounting on an external heat sink by means of a simple threaded stud. The Type 2N454 transistor is designed to meet the requirements of MIL-T-19500A.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS					
Temperature Range					
Storage	T_{STG}				
Junction (Operating)	T_J			−65 to + 150 °C	+ 150 °C
Voltages					
Collector-Base	V_{CB}				65 volts
Emitter-Base	V_{EB}				10 volts
Collector-Emitter ($R_{BE} \leqq 50$ ohms)	V_{CE}				65 volts
Currents					
Base					0.5 amps
Collector (For good performance, maximum collector current should be limited to 2 amps.)					5 amps
Collector DC Power Dissipation					
25°C Mounting Base Temp.					85 watts
100°C Mounting Base Temp.					35 watts
ELECTRICAL CHARACTERISTICS					
D-C Characteristics					
(25°C Mtg. Base Temp. except where otherwise indicated)		MIN.	NOM.	MAX.	
Collector Reverse Current ($V_{CB} = +65v$) ($V_{CE} = +30v$; $R_{BE} \leqq 50\ \Omega$; $T_A = +125°C$)	I_{CBO}			20	ma
Collector Saturation Resistance ($I_C = 1$ amp; $I_B = 0.3$ amp.)	I_{CER}			20	ma
Forward Current Transfer Ratio ($I_C = 1$ amp, $V_{CE} = 20v$)	R_{SE}			10	ohms
Input Resistance ($I_C = 1$ amp, $V_{CE} = 20v$)	h_{FE}	8			
	h_{IE}		25		ohms
Thermal Characteristics					
Thermal resistance from collector junction to mounting base				1.5	°C/watt

2N489–2N494

Outline Drawing No. 5

The General Electric Silicon Unijunction Transistor is a hermetically sealed three terminal device having a stable "N" type negative resistance charactistic over a wide temperature range. A high peak current rating makes this device useful in medium power switching and oscillator applications, where it can serve the purpose of two conventional silicon transistors. These transistors are hermetically sealed in a welded case. The case dimensions and lead configuration are suitable for insertion in printed boards by automatic assembly equipment. The Silicon Unijunction Transistor consists of an "N" type silicon bar mounted between two ohmic base contacts with a "P" type emitter near base-two. The device operates by conductivity modulation of the silicon between the emitter and base-one when the emitter is forward biased. In the cutoff, or standby condition, the emitter and interbase power supplies establish potentials between the base contacts, and at the emitter, such that the emitter is back biased. If the emitter potential is increased sufficiently to overcome this bias, holes (minority carriers) are injected into the silicon bar. These holes are swept towards base-one by the internal field in the bar. The increased charge concentration, due to these holes, decreases the resistance and hence decreases the internal voltage drop from the emitter to base-one. The emitter current then increases regeneratively until it is limited by the emitter power supply. The effect of this conductivity modulation is also noticed as an effective modulation of the interbase current.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

RMS Power Dissipation	250 mw*
RMS Power Dissipation – Stabilized**	350 mw*
RMS Emitter Current	50 ma
Peak Emitter Current*** ($T_J = 150°C$)	2 amps
Emitter Reverse Voltage ($T_J = 150°C$)	60 volts
Operating Temperature Range	−65 to 150 °C
Storage Temperature Range	−65 to 200 °C
Interbase Voltage (V_{BB})	See Fig. A

*Derate 2 mw/°C increase in ambient temperature.
**Total power dissipation must be limited by external circuit.
***Capacitor discharge —10 μfd or less.

Types 2N489-2N494 are specified primarily in three ranges of stand-off and two ranges of interbase resistance. Each range of stand-off ratio has limits of ±10% from the center value and each range of interbase resistance has limits of ±20% from the center value.

2N489, 2N490

MAJOR ELECTRICAL CHARACTERISTICS:		2N489 MIN.	2N489 NOM.	2N489 MAX	2N490 MIN.	2N490 NOM.	2N490 MAX.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.51	.56	.62	.51	.56	.62	
Modulated Interbase Current (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	I_{B_2} (MOD)	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (V_{B_2E} = 60v; T_J = 25°C)	I_{EO}		.07	1.0		.07	1.0	μa
(V_{B_2E} = 60v; T_J = 150°C)	I_{EO}		28	100		28	100	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	V_E (SAT)	1.5	2.2	3.5	1.5	2.4	3.6	volts
Peak Point Emitter Current (V_{BB} = 25v; T_A = 25°C)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.1	1.9	3.4	1.0	1.9	3.5	volts
Valley Current	I_V	12	19	35	11	19	31	ma
Maximum Frequency of Oscillation (I_{B_2} = 4.5 ma; Relaxation Oscillator)	f_{MAX}		0.9			0.7		mc

2N491, 2N492

MAJOR ELECTRICAL CHARACTERISTICS:		2N491 MIN.	2N491 NOM.	2N491 MAX.	2N492 MIN.	2N492 NOM.	2N492 MAX.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.56	.62	.68	.56	.62	.68	
Modulated Interbase Current (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	I_{B_2} (MOD)	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (V_{B_2E} = 60v; T_J = 25°C)	I_{EO}		.07	1.0		.07	1.0	μa
(V_{B_2E} = 60v; T_J = 150°C)	I_{EO}		28	100		28	100	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	V_E (SAT)	1.7	2.6	3.8	1.8	2.8	4.0	volts
Peak Point Emitter Current (V_{BB} = 25v; T_A = 25°C)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.2	2.2	3.9	1.2	2.2	3.9	volts
Valley Current	I_V	13	20	37	12	20	38	ma
Maximum Frequency of Oscillation (I_{B_2} = 4.5 ma; Relaxation Oscillator)	f_{MAX}		0.8			0.7		mc

2N493, 2N494

MAJOR ELECTRICAL CHARACTERISTICS:		2N493 MIN.	2N493 NOM.	2N493 MAX.	2N494 MIN.	2N494 NOM.	2N494 MAX.	
Interbase Resistance at 25°C Junction Temperature	R_{BB_O}	4.7	5.6	6.8	6.2	7.5	9.1	kilohms
Intrinsic Stand-off Ratio	η	.62	.68	.75	.62	.68	.75	
Modulated Interbase Current (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	I_{B_2} (MOD)	6.8	12	22	6.8	12	22	ma
Emitter Reverse Current (V_{B_2E} = 60v; T_J = 25°C)	I_{EO}		.07	1.0		.07	1.0	μa
(V_{B_2E} = 60v; T_J = 150°C)	I_{EO}		28	100		28	100	μa
MINOR ELECTRICAL CHARACTERISTICS: (Typical Values)								
Emitter Saturation Voltage (I_E = 50 ma; V_{BB} = 10v; T_A = 25°C)	V_E (SAT)	2.0	3.0	4.5	2.1	3.2	4.6	volts
Peak Point Emitter Current (V_{BB} = 25v; T_A = 25°C)	I_P		4	12		4	12	μa
Valley Voltage	V_V	1.4	2.5	4.4	1.4	2.5	4.3	volts
Valley Current	I_V	14	24	40	12	21	35	ma
Maximum Frequency of Oscillation (I_{B_2} = 4.5 ma; Relaxation Oscillator)	f_{MAX}		0.7			0.65		mc

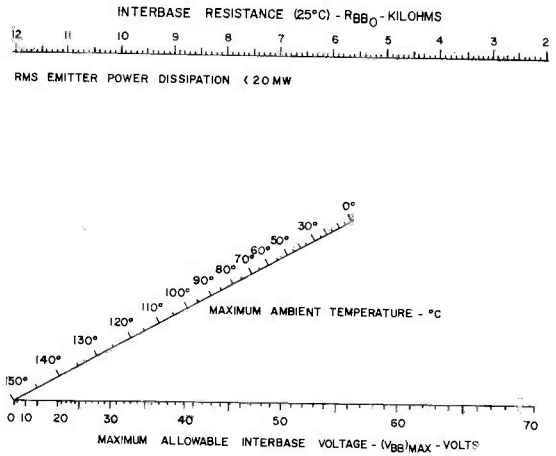


FIGURE A

2N508

Outline Drawing No. 2

The 2N508 is an alloy junction PNP transistor intended for driver service in audio amplifiers. It is a miniaturized version of the 2N265 G.E. transistor. By control of transistor characteristics during manufacture, a specific power gain is provided for each type. Special processing techniques and the use of hermetic seals provides stability of these characteristics throughout life.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Emitter	V_{CE}	−16 volts
Collector to Base	V_{CB}	−16 volts
Collector Current	I_C	−100 ma
Power		
Collector Dissipation	P_{CM}	140 mw
Temperature		
Operating and Storage Range	T_A-T_{STG}	−65 to + 65 °C

TYPICAL ELECTRICAL CHARACTERISTICS: (25°C)

D.C. Characteristics			
Base Current Gain (I_C = −20 ma; V_{CE} = −1v)	h_{FE}	125	
Collector to Emitter Voltage (R_{EB} = 10K; I_C = −.6 ma)	V_{CER}	−16	volts
Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	10	μa
Max. Collector Cutoff Current (V_{CB} = −16v)	I_{CO}	16	μa
Small Signal Characteristics			
Frequency Cutoff (V_{CB} = −5v; I_E = 1 ma)	f_{ab}	3.5	mc
Collector Capacity (V_{CB} = −5v; I_E = 1 ma)	C_{ob}	24	μμf
Noise Figure (V_{CB} = −5v; I_E = 1 ma)	NF	6	db
Input Impedance (V_{CE} = −5v; I_E = 1 ma)	h_{ie}	3	K ohms
Current Gain (V_{CE} = −5v; I_E = 1 ma)	h_{fe}	112	
Thermal Characteristics			
Thermal Resistance Junction to Air		.25	°C/mw
Performance Data Common Emitter			
Power Gain Driver (V_{CC} = 9v)	G_e	45	db
Power Output	P_o	1	mw

The General Electric Type 2N518 is a germanium PNP alloy junction high frequency switching transistor intended for military, industrial and data processing applications where high reliability at the maximum ratings is of prime importance.

2N518

Outline Drawing No. 8

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	−45 volts
Collector to Emitter	V_{CE}	−12 volts
Emitter to Base	V_{EB}	−30 volts
Collector Current	I_C	−125 ma
Temperature		
Storage	T_{STG}	−65 to 85 °C
Junction	T_J	85 °C
Power		
Total Transistor Dissipation	P_{AV}	150 mw

ELECTRICAL CHARACTERISTICS: (25°C)

		MIN.	MAX.	DESIGN CENTER	
High Frequency Characteristics (Common Base)					
($V_{CB} = -5v$; $I_E = 1$ ma)					
Alpha Cutoff Frequency	f_{ab}	10			mc
Collector Capacity ($f = 1$ mc)	C_{ob}		16	12	$\mu\mu f$
Voltage Feedback Ratio ($f = 1$ mc)	h_{rb}		13	10	$\times 10^{-3}$
Cutoff Characteristics					
Breakdown Voltage Collector to Base Emitter Open ($I_C = -100$ μamps)	BV_{CBO}	−45			volts
Breakdown Voltage Emitter to Base Collector Open ($I_E = -100$ μamps)	BV_{EBO}	−30			volts
Breakdown Voltage Collector to Emitter Base Open ($I_C = -600$ μamps)	BV_{CEO}	−12			volts
Collector Cutoff Current ($V_{CBO} = -12v$)	I_{CBO}		−6		μamps
Emitter Cutoff Current ($V_{EBO} = -12v$)	I_{EBO}		−6		μamps
D-C Characteristics					
D-C Base Current Gain ($V_{CE} = -1v$; $I_C = -10$ ma)	h_{FE}	60			
Saturation Voltage ($I_B = -.25$ ma; $I_C = -10$ ma)	V_{CE} (SAT)		−0.150		volts
Pulse Response Time ($I_C = -10$ ma; $I_{B_1} = I_{B_2} = -.5$ ma)					
Delay and Rise Time	$t_d + t_r$			0.8	μsec
Storage Time	t_s			0.9	μsec
Fall Time	t_f			0.5	μsec

Thermal Characteristics

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N524, 2N525

Outline Drawing No. 2

The General Electric types 2N524 and 2N525 are germanium PNP alloy junction transistors particularly recommended for low to medium power amplifier and switching application in the frequency range from audio to 100 KC. This series of transistors is intended for military, industrial and data processing applications where high reliability and extreme stability of characteristics are of prime importance. The 2N524 and 2N525 are equivalent to the 2N44 and 2N43 respectively and may be directly substituted in most applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CBO}	−45 volts
Collector to Emitter	V_{CER}	−30 volts
Emitter to Base	V_{EBO}	−15 volts
Collector Current	I_{CM}	−500 ma
Temperatures		
Storage	T_{STG}	−65 to 100 °C
Operating	T_J	85 °C
Power		
Total Transistor Dissipation	P_{AV}	225 mw

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics

(Unless otherwise specified $V_C = -5V$ common base; $I_E = -1$ ma; f = 270 cps)

		2N524			2N525			
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Output Admittance (Input AC Open Circuited)	h_{ob}	.10	.65	1.3	.1	.6	1.2	μmhos
Input Impedance (Output AC Short Circuited)	h_{ib}	26	31	36	26	31	35	ohms
Reverse Voltage Transfer Ratio (Input AC Open Circuited)	h_{rb}	1	4.0	10	1	5.0	11	$\times 10^{-4}$
Forward Current Transfer Ratio (Common Emitter; Output AC Short Circuited)	h_{fe}	16	30	41	30	44	64	
Frequency Cutoff	f_{ab}	.8	2.0	5.0	1	2.5	5.5	mc
Output Capacity (f = 1 mc; Input AC open circuited)	C_{ob}	18	25	40	18	25	40	μμf
Noise Figure (f = 1 kc; BW = 1 cycle)	NF	1	6	15	1	6	15	db

D-C Characteristics

Forward Current Gain (Common Emitter, I_C/I_B)								
($V_{CE} = -1v$; $I_C = -20$ ma)	h_{FE}	19	35	42	34	52	65	
($V_{CE} = -1v$; $I_C = -100$ ma)	h_{FE}	13	31		30	45		
Base Input Voltage, Common Emitter ($V_{CE} = -1v$; $I_C = -20$ ma)	V_{BE}	−.220	−.255	−.320	−.200	−.243	−.300	
Collector Cutoff Current ($V_{CBO} = -30v$)	I_{CO}		−5	−10		−5	−10	μa
Emitter Cutoff Current ($V_{EBO} = -15v$)	I_{EO}		−4	−10		−4	−10	μa
Collector to Emitter Voltage (R_{BE} = 10K ohms; $I_C = -.6$ ma)	V_{CER}	−30			−30			volts
Punch-through Voltage	V_{PT}	−30			−30			volts

Thermal Resistance (k)

Junction Temperature Rise/ Total Transistor Dissipation:								
Free Air				.27			.27	°C/mw
Infinite Heat Sink				.11			.11	°C/mw
Clip-on Heat Sink in Free Air				.20			.20	°C/mw

2N526, 2N527

The General Electric types 2N526 and 2N527 are germanium PNP alloy junction transistors particularly recommended for low to medium power amplifier and switching application in the frequency range from audio to 100 KC. This series of transistors is intended for military, industrial and data processing applications where high reliability and extreme stability of characteristics are of prime importance.

Outline Drawing No. 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CBO}	−45 volts
Collector to Emitter	V_{CER}	−30 volts
Emitter to Base	V_{EBO}	−15 volts
Collector Current	I_{CM}	−500 ma
Temperatures		
Storage	T_{STG}	−65 to 100 °C
Operating	T_J	85 °C
Power		
Total Transistor Dissipation	P_{AV}	225 mw

ELECTRICAL CHARACTERISTICS: (25°C)

Small Signal Characteristics

(Unless otherwise specified $V_C = -5V$ common base; $I_E = -1$ ma; f = 270 cps)

		2N526			2N527			
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Output Admittance (Input AC Open Circuited)	h_{ob}	.1	.42	1.0	.1	.37	.9	μmhos
Input Impedance (Output AC Short Circuited)	h_{ib}	26	30	33	26	29	31	ohms
Reverse Voltage Transfer Ratio (Input AC Open Circuited)	h_{rb}	1	6.5	12	1	8.0	14	$\times 10^{-4}$
Forward Current Transfer Ratio (Common Emitter; Output AC Short Circuited)	h_{fe}	44	64	88	60	81	120	
Frequency Cutoff	f_{ab}	1.3	3.0	6.5	1.5	3.3	7	mc
Output Capacity (f = 1 mc; Input AC open circuited)	C_{ob}	18	25	40	18	25	40	μμf
Noise Figure (f = 1 kc; BW = 1 cycle)	NF	1	6	15	1	6	15	db

D-C Characteristics

Forward Current Gain (Common Emitter, I_C/I_B)								
($V_{CE} = -1v$; $I_C = -20$ ma)	h_{FE}	53	73	90	72	91	121	
($V_{CE} = -1v$; $I_C = -100$ ma)	h_{FE}	47	66		65	86		
Base Input Voltage, Common Emitter ($V_{CE} = -1v$; $I_C = -20$ ma)	V_{BE}	−.190	−.230	−.280	−.180	−.216	−.260	
Collector Cutoff Current ($V_{CBO} = -30v$)	I_{CO}		−5	−10		−5	−10	μa
Emitter Cutoff Current ($V_{EBO} = -15v$)	I_{EO}		−4	−10		−4	−10	μa
Collector to Emitter Voltage (R_{BE} = 10K ohms; $I_C = -.6$ ma)	V_{CER}	−30			−30			volts
Punch-through Voltage	V_{PT}	−30			−30			volts

Thermal Resistance (k)

Junction Temperature Rise/ Total Transistor Dissipation:					
Free Air					
Infinite Heat Sink	.27		.27		°C/mw
Clip-on Heat Sink in Free Air	.11		.11		°C/mw
	.20		.20		°C/mw

2N634

Outline Drawing No. 2

The General Electric type 2N634 is an NPN germanium alloy triode transistor designed for high speed switching applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	20 volts
Emitter to Base	V_{EB}	15 volts
Collector to Emitter	V_{CE}	20 volts
Currents		
Collector	I_C	300 ma
Base	I_B	50 ma
Emitter	I_E	300 ma
Temperature		
Storage	T_{STG}	−65 to 85 °C
Operating Junction	T_A	85 °C
Power		
Dissipation	P_M	150 mw

ELECTRICAL CHARACTERISTICS: (25°C)

		MIN.	NOM.	MAX.	
Collector Voltage (I_C = 15 μamp; I_E = 0)	V_{CBO}	20			volts
Emitter Voltage (I_E = 10 μamp; I_C = 0)	V_{EBO}	15			volts
Collector to Emitter Voltage (I_C = 600 μamp; R = 10 K)	V_{CER}	20			volts
Collector Cutoff Current (V_{CB} = 5v; I_E = 0)	I_{CBO}			5	μamps
Punch Through Voltage	V_{PT}	20			volts
D-C Current Gain (I_C = 200 ma; V_{CE} = 0.75v)	h_{FE}	15			
Alpha Cutoff Frequency (V_{CB} = 5v; I_E = −1 ma)	f_{ab}	5	8		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

2N635

Outline Drawing No. 2

The General Electric type 2N635 is an NPN germanium alloy triode transistor designed for high speed switching applications.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	20 volts
Emitter to Base	V_{EB}	15 volts
Collector to Emitter	V_{CE}	20 volts
Currents		
Collector	I_C	300 ma
Base	I_B	50 ma
Emitter	I_E	300 ma
Temperature		
Storage	T_{STG}	−65 to 85 °C
Operating Junction	T_A	85 °C
Power		
Dissipation	P_M	150 mw

ELECTRICAL CHARACTERISTICS: (25°C)

		MIN.	NOM.	MAX.	
Collector Voltage ($I_C = 15$ μamp; $I_E = 0$)	V_{CBO}	20			volts
Emitter Voltage ($I_E = 10$ μamp; $I_C = 0$)	V_{EBO}	15			volts
Collector to Emitter Voltage ($I_C = 600$ μamp; R = 10 K)	V_{CER}	20			volts
Collector Cutoff Current ($V_{CB} = 5$v; $I_E = 0$)	I_{CBO}			5	μamps
Punch Through Voltage	V_{PT}	20			volts
D-C Current Gain ($I_C = 200$ ma; $V_{CE} = 0.75$v)	h_{FE}	25			
Alpha Cutoff Frequency ($V_{CB} = 5$v; $I_E = -1$ ma)	$f_{\alpha b}$	10	12		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

The General Electric type 2N636 is an NPN germanium alloy triode transistor designed for high speed switching applications.

2N636

Outline Drawing No. 2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base	V_{CB}	20 volts
Emitter to Base	V_{EB}	15 volts
Collector to Emitter	V_{CE}	20 volts
Currents		
Collector	I_C	300 ma
Base	I_B	50 ma
Emitter	I_E	300 ma
Temperature		
Storage	T_{STG}	−65 to 85 °C
Operating Junction	T_A	85 °C
Power		
Dissipation	P_M	150 mw

ELECTRICAL CHARACTERISTICS: (25°C)

		MIN.	NOM.	MAX.	
Collector Voltage ($I_C = 15$ μamp; $I_E = 0$)	V_{CBO}	20			volts
Emitter Voltage ($I_E = 10$ μamp; $I_C = 0$)	V_{EBO}	15			volts
Collector to Emitter Voltage ($I_C = 600$ μamp; R = 10 K)	V_{CER}	15			volts
Collector Cutoff Current ($V_{CB} = 5$v; $I_E = 0$)	I_{CBO}			5	μamps
Punch Through Voltage	V_{PT}	15			volts
D-C Current Gain ($I_C = 200$ ma; $V_{CE} = 0.75$v)	h_{FE}	35			
Alpha Cutoff Frequency ($V_{CB} = 5$v; $I_E = -1$ ma)	$f_{\alpha b}$	15	17		mc

Thermal Characteristic

Derate 2.5 mw/°C increase in ambient temperature over 25°C.

3N36

Outline Drawing No. 7

The General Electric Type 3N36 is a germanium meltback NPN transistor designed for high frequency use as an amplifier, oscillator or mixer. It is recommended for use in the frequency range from 30mc to 100mc. The 3N36 is excellent for wide band video amplifiers from low frequency to 10mc. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. These transistors are hermetically sealed in welded cases. The case dimensions conform to the JETEC TO-12 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages		
Collector to Base 1 or Base 2	V_{CB}	7 volts
Emitter to Base 1 or Base 2	V_{EB}	2 volts
Collector to Emitter	V_{CE}	6 volts
Currents		
Collector	I_C	20 ma
Emitter	I_E	−20 ma
Base 2	I_{B_2}	2 ma
Temperature		
Storage	T_{STG}	−65 to +85 °C
Operating Junction	T_J	+85 °C
Power		
Total Transistor Dissipation	P_M	30 mw

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB_1} = +5v$; $I_E = -1.5$ ma; $V_{B_2B_1} = -2v$; f = 60 mc)

		MIN.	DESIGN CENTER	MAX.	
Small Signal High Frequency Parameters					
Output Capacity	C_{ob}		2	3	$\mu\mu f$
Noise Figure (Common Base)	NF		11		db
Base Spreading Resistance	r'_b		50		ohms
Common Emitter "h" Parameters					
Input Impedance	h_{ie}		100 − j27		ohms
Reverse Voltage Transfer Ratio	h_{re}		.022 ∠ 47°		
Current Transfer Ratio	h_{fe}		2.2 ∠ −81°		
Output Admittance	h_{oe}		8 + j8.8		$\times 10^{-4}$ mhos
Common Base Cutoff Frequency	f_{ab}	50			mc
Common Emitter Power Gain	G_e	10	11.5		db
D-C Characteristics					
Voltage Collector to Emitter ($R_{BE} = 10K$; $V_{B_2E} = -2v$; $I_C = 25$ μamp)	V_{CER}	5			volts
Collector Cutoff Current ($V_{CB_1B_2} = 7v$)	I_{CO}		3	10	μamps
Cross Base Resistance	$R_{B_1B_2}$	2.4K	4K	10K	ohms

Thermal Characteristic

Derate .5mw/°C increase in ambient temperature over 25°C.

3N37

Outline Drawing No. 7

The General Electric Type 3N37 is a germanium meltback NPN transistor designed for high frequency use as an amplifier, oscillator or mixer. It is recommended for use in the frequency range of 100mc to 200mc. The 3N37 is excellent for wide band video amplifiers from low frequency to 10mc. All units are subjected to a rigorous mechanical drop test to control mechanical reliability. These transistors are hermetically sealed in welded cases. The case dimensions conform to the JETEC TO-12 package and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: (25°C)

Voltages

Collector to Base 1 or Base 2	V_{CB}	7 volts
Emitter to Base 1 or Base 2	V_{EB}	2 volts
Collector to Emitter	V_{CE}	6 volts

Currents

Collector	I_C	20 ma
Emitter	I_E	−20 ma
Base 2	I_{B_2}	2 ma

Temperature

Storage	T_{STG}	−65 to +85 °C
Operating Junction	T_J	+85 °C

Power

Total Transistor Dissipation	P_M	30 mw

ELECTRICAL CHARACTERISTICS: (25°C)

(Unless otherwise specified $V_{CB_1} = +5v$; $I_E = -1.5$ ma; $V_{B_2B_1} = -2v$; f = 150 mc)

Small Signal High Frequency Parameters		MIN.	DESIGN CENTER	MAX.	
Output Capacity	C_{ob}		1.5	3	$\mu\mu f$
Noise Figure (Common Base)	NF		11		db
Base Spreading Resistance	r'_b		50		ohms

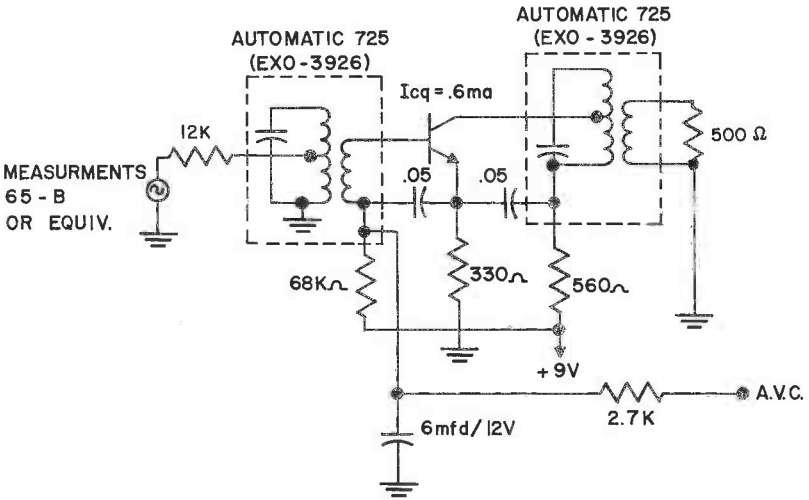
Common Emitter "h" Parameters					
Input Impedance	h_{ie}		80 − j10		ohms
Reverse Voltage Transfer Ratio	h_{re}		.018 ∠ 84°		
Current Transfer Ratio	h_{fe}		1.1 ∠ −100°		
Output Admittance	h_{oe}		5.5 + j12.514		$\times 10^{-4}$ mhos
Common Base Cutoff Frequency	$f_{\alpha b}$	90			mc
Common Emitter Power Gain	G_e	7	9		db

D-C Characteristics					
Voltage Collector to Emitter ($R_{BE} = 10K$; $V_{B_2E} = -2v$; $I_C = 25\ \mu$amp)	V_{CER}	5			volts
Collector Cutoff Current ($V_{CB_1B_2} = 7v$)	I_{CO}		3	10	μamps
Cross Base Resistance	$R_{B_1B_2}$	2.5K	4K	10K	ohms

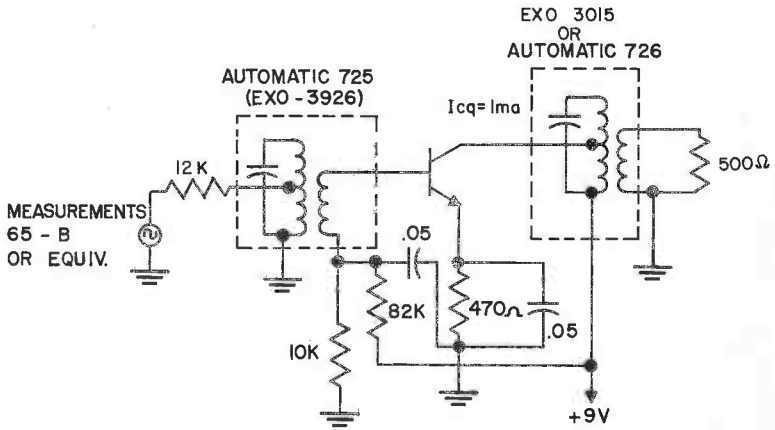
Thermal Characteristic

Derate .5mw/°C increase in ambient temperature over 25°C.

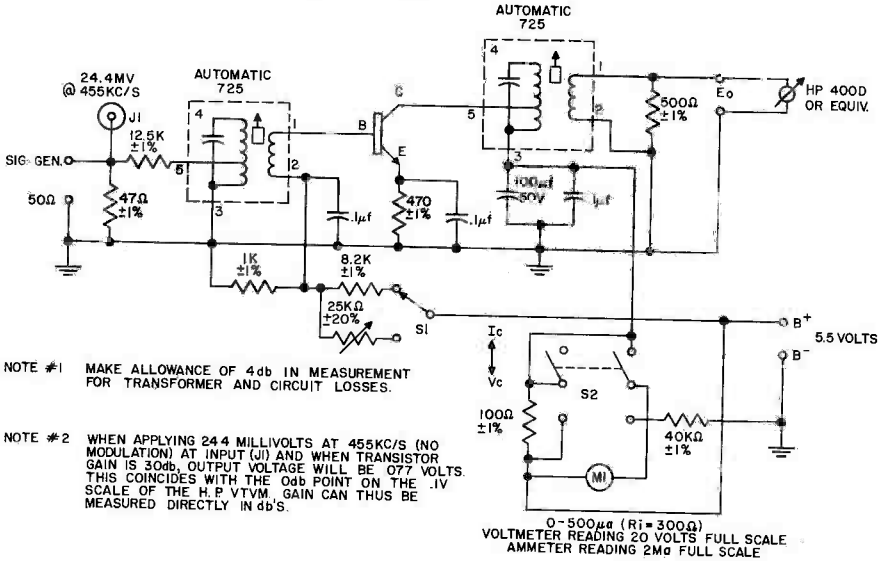
TYPICAL 1ST I. F. AMPL.



TYPICAL 2ND I. F. AMPL.



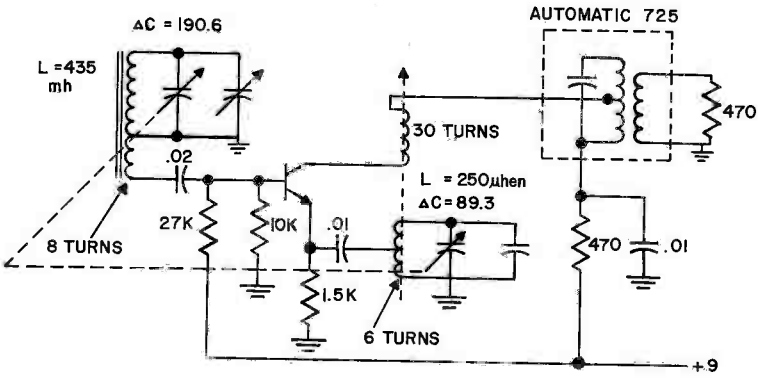
TYPICAL IF TEST CIRCUIT



NOTE #1 MAKE ALLOWANCE OF 4db IN MEASUREMENT FOR TRANSFORMER AND CIRCUIT LOSSES.

NOTE #2 WHEN APPLYING 244 MILLIVOLTS AT 455KC/S (NO MODULATION) AT INPUT (J1) AND WHEN TRANSISTOR GAIN IS 30db, OUTPUT VOLTAGE WILL BE 077 VOLTS. THIS COINCIDES WITH THE 0db POINT ON THE .1V SCALE OF THE H.P VTVM. GAIN CAN THUS BE MEASURED DIRECTLY IN db'S.

TYPICAL AUTODYNE CONVERTER



ANTENNA - DELTA COIL #1 - 105A OR EQUIVALENT
OSCILLATOR COIL - E. STANWYCK CO. #1129 (MODIFIED) OR EQUIVALENT
CAPACITOR - RADIO CONDENSER #242 OR EQUIVALENT
I.F TRANSFORMER - AUTOMATIC 725 (EXO-3926) OR EQUIVALENT

For explanation of symbols, ratings and mfg. symbols see page 160.

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVCB	fα mc	TJ°C	TYPICAL VALUES hfe	fαb mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N22	Pt	WE	Sw		120	−100	−20	55	1.9α					
2N23	Pt	WE	Sw		80	−50	−40	55	1.9α					
2N24	Pt	WE	AF		120	−30	−25	50	2.2α					
2N25	Pt	WE	AF		200	−50	−30	60	2.5α					
2N26	Pt	WE	Sw		90	−30	−40	55						
2N27	NPN	WE	AF		50	35	100	85	100	1				
2N28	NPN	WE	AF		50	30	100	85	100	.5				
2N29	NPN	WE	AF		50	35	30	85	100	1				
2N30	Pt	GE	Obsolete		100	30	7	40	2.2α	2	17			old G11
2N31	Pt	GE	Obsolete		100	30	7	40	2.2α	2				old G11A
2N32	Pt	RCA			50	−40	−8	40	2.2α	2.7	21			
2N33	Pt	RCA	Obsolete		30	−8.5	−7	40			Osc.			
2N34	PNP	RCA	AF		50	−25	−8	50	40	.6	40			2N190
2N35	NPN	RCA	IF		50	25	8	50	40	.8	40		125	2N169A
2N36	PNP	CBS	AF		50	−20	−8	50	45		40			2N191
2N37	PNP	CBS	AF		50	−20	−8	50	30		36			2N190
2N38	PNP	CBS	AF		50	−20	−8	50	15		32			2N189
2N38A	PNP	CBS	AF		50	−20	−8	50	18		32			2N189
2N41	PNP	RCA			50	−25	−15	50	40		40			2N190
2N43	PNP	GE	AF	1	240	−30	−300	100	53	1.3	40	40		2N43
2N43A	PNP	GE	AF	1	155	−25		100	53	1.3	40	40		2N43A
2N44	PNP	GE	AF	1	240	−30	−300	100	31	1.0	39	40		2N44
2N45	PNP	GE	Obsolete		155	−25		100	31	1.0	38	40		
2N46	PNP	RCA			see 2N41									2N190
2N47	PNP	Phil	AF		50	−35	−20	65	38	8	40			2N190 25V
2N48	PNP	Phil	AF		50	−35	−20	65	32	8	40			2N189 25V
2N49	PNP	Phil	AF		50	−35	−20	65	38	8	40			2N190 25V
2N50	Pt	Cle			50	−15	−1	50	2α	3	20			
2N51	Pt	Cle	Sw		100	−50	−8	50			20			
2N52	Pt	Cle	RF		120	−50	−8	50			20			
2N53	Pt	Cle	RF		100	−50	−8	50	2α	5	20			
2N54	PNP	W	AF		200	−45	−10	60	32	.5	40			2N190 25V
2N55	PNP	W	AF		200	−45	−10	60	20	.5	39			2N190 25V
2N56	PNP	W	AF		200	−45	−10	60	12	.5	38			2N189 25V
2N57	PNP	W	Pwr		20W	−60	−.8A		60		14	5W		
2N59	PNP	W	AF Out		180	−20	−200	85	90		30	30	300	2N241A or 2N321

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS				TYPICAL VALUES					Closest GE
					P_C mw @ 25°C	BV_{CB}	I_C ma	T_J°C	h_{fe}	f_{ab} mc	G_e db	P_o mw — Class A	P_o mw — Class B	
2N60	PNP	W	AF Out		180	−20	−200	85	65		28	30	300	2N188A or 2N320
2N61	PNP	W	AF Out		180	−20	−200	85	45		26	30	300	2N187A or 2N319
2N62	PNP	Phil	Obsolete		50	−35	−20		40					
2N63	PNP	Ray	AF		100	−22	−10	85	22	6	39	40		2N107
2N64	PNP	Ray	AF		100	−15	−10	85	45	8	41	40		2N191
2N65	PNP	Ray	AF		100	−12	−10	85	90	1.2	42	40		2N192
2N66	PNP	WE	Obsolete		1W	−40	.8A	80		.2				
2N68	PNP	Syl	Pwr		2W/4W	−25	−1.5A	70	40	.4	23	600	5W	
2N71	PNP	W	Pwr		1W	−50	−250	60		.25	25	400		
2N72	Pt	RCA	Obsolete		50	−40	−20	55		2.5				
2N73	PNP	W	AF Sw		200	−50					low level			
2N74	PNP	W	AF Sw		200	−50					high level			
2N75	PNP	W	AF Sw		200	−50					very low level			
2N76	PNP	GE	Obsolete		50	−20	−10	60	20	1	38			
2N77	PNP	RCA	AF		35	−25	−15	50	55	.7	44	50		2N190
2N78	NPN	GE	RF	3	65	15	20	85	70	9	28			2N191
2N79	PNP	RCA	AF		35	−30	−50		46	.7	44	50		2N78
2N80	PNP	CBS	AF		50	−25	−8	Hi	80					2N191
2N81	PNP	GE	Obsolete		50	−20	−15	100	30					2N192
2N82	PNP	CBS	AF		35	−20	−15	Hi	30					use 2N189
2N94	NPN	Syl	RF Sw		30	20	50	75	30	3	38			
2N94A	NPN	Syl	RF Sw		30	20	50	75	40	6	38			{2N169A (and 2N123 PNP)
2N95	NPN	Syl	Pwr		2.5W/4W	25	1.5A	70	40	.4	23	600	5W	
2N96	PNP	RCA	Obsolete		50	−30*	−20	55	35	.5				
2N97	NPN	GP	IF		50	30	10	75	13	1	20			2N190 or 2N322
2N97A	NPN	GP	IF		50	40	10	85	13	1	20			2N169 15V
2N98	NPN	GP	IF		50	40	10	75	38	2.5	22			2N169A 25V
2N98A	NPN	GP	IF		50	40	10	85	38	2.5	22			2N169A 25V
2N99	NPN	GP	IF		50	40	10	75	38	3.5	22			2N169A 25V
2N100	NPN	GP	IF		25	25	5	50	100	5	23			2N170 6V
2N101	PNP	Syl	Pwr		1W	−25	−1.5A	70			23	600		
2N102	NPN	Syl	Pwr		1W	25	1.5A	70			23	600	5W	
2N103	NPN	GP	Genl IF		50	35	10	75	5	.75	15			2N170 6V
2N104	PNP	RCA	AF		70	−30	−50	70	44	.7	41			2N190 25V
2N105	PNP	RCA	AF		35	−25	−15	50	55	.75	42			2N191
2N106	PNP	Ray	AF		100	−6	−10	85	45	.8	36	40		2N189
2N107	PNP	GE	AF	1	50	−6	−10	60	20	1	38			2N107
2N108	PNP	CBS	AF Out		50	−20	−15							
2N109	PNP	RCA	AF Out		50	−12	−35	50	70		33	75	35	2N188-2N192
2N110	Pt	WE	Sw		180	−50*	−50	85	32	5.0			150	
2N111	PNP	Ray	IF		150	−15	−200	85	40	3	30			
2N111A	PNP	Ray	IF		150	−15	−200	85	40	3	33			2N135
2N112	PNP	Ray	RF		150	−15	−200	85	40	5	32			2N135
														2N136-2N135

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVCE	Ic ma	TJ°C	TYPICAL VALUES hfe	fab mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N112A	PNP	Ray	IF		150	−15	−200	85	40	5	35			2N136
2N113	PNP	Ray	RF		100	−6	−5	85	45	10	33			2N137
2N114	PNP	Ray	RF Sw		100	−6	−5	85	65	20				2N137 or 2N123
2N117	NPN	TI	Si (=903)		150	45*	25	175	12	4				2N332
2N118	NPN	TI	Si (=904)		150	45*	25	175	24	5				2N333
2N119	NPN	TI	SiAF		150	45*	25	175	.98a	6				2N335
2N123	PNP	GE	RF Sw	8	100	−20	−125	85	50	8				2N123
2N124	NPN	TI	RF Sw		50	10	8	75	18	3				2N168
2N125	NPN	TI	RF Sw		50	10	8	75	32	5				2N167
2N126	NPN	TI	RF Sw		50	10	8	75	60	5				2N167
2N127	NPN	TI	RF Sw		50	10	8	75	130	5				2N167
2N128	PNP	Phil	SB Osc		30	−4.5	−5	85	35	60				
2N129	PNP	Phil	SB Osc		30	−4.5	−5	85	20	40				
2N130	PNP	Ray	AF		84	−22	−10	85	22		39			2N186 or 2N319
2N131	PNP	Ray	AF		84	−15	−10	85	45		41			2N187 or 2N319
2N132	PNP	Ray	AF		84	−12	−10	85	90		42			2N241 or 2N321
2N133	PNP	Ray	AF		84	−15	−10	85	25		36			2N186
2N135	PNP	GE	IF	8	100	−12	−50	85	20	4.5	29			2N135
2N136	PNP	GE	RF	8	100	−12	−50	85	40	6.5	31			2N136
2N137	PNP	GE	RF	8	100	−6	−50	85	60	10	33			2N137
2N138	PNP	Ray	AF Out		50	−12	−20	40	140		30		50	2N192
2N138A	PNP	Ray	AF Out		80	−45	−100	85	10		29	25	100	2N187 25V
2N139	PNP	RCA	IF		35	−16	−15	70	48	4.7	29			2N136-2N135
2N140	PNP	RCA	Osc		35	−16	−15	70	45	7	28			2N136-2N137
2N141	PNP	Syl	Pwr		1.5W/4W	−30	−.8A	65	40	.4	26	600	5W	
2N142	NPN	Syl	Pwr		1.5W/4W	30	.8A	65	40	.4	26	600	5W	
2N143	PNP	Syl	Pwr		1W/4W	−30	−.8A	65	40	.4	26	600	5W	
2N144	NPN	Syl	Pwr		1W/4W	30	.8	65	40	.4	26	600	5W	
2N145	NPN	TI	IF		65	20	5	75			33 max			2N169 or 2N292
2N146	NPN	TI	IF		65	20	5	75			36 max			2N169 or 2N292
2N147	NPN	TI	Osc		65	20	5	75			39 max			2N168A or 2N293
2N148	NPN	TI	lo IF		65	16	5	75			35 max			2N169 or 2N292
2N148A	NPN	TI	lo IF		65	32	5	75			35 max			2N169A
2N149	NPN	TI	lo IF		65	16	5	75			38 max			2N169 or 2N292
2N149A	NPN	TI	lo IF		65	32	5	75			38 max			2N169A
2N150	NPN	TI	lo IF		65	16	5	75			41 max			2N169 or 2N292
2N150A	NPN	TI	lo IF		65	32	5	75			41 max			2N169A
2N155	PNP	CBS	Pwr		8.5W	−30	−3A	85	48	.18	33	2W	9W	
2N156	PNP	CBS	Pwr		8.5W	−30	−3A	85	40	.18	36	2W	9W	
2N158	PNP	CBS	Pwr		8.5W	−60	−3A	85	40	.18	40	2W	17W	
2N158A	PNP	CBS	Pwr		8.5W	−60	−3A	85	41	.18				
2N159	Pt	Sprague	Sw		80	−50	−10			2				

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVCB	Ic ma	TJ°C	TYPICAL VALUES hfe	fab mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N160	NPN	GP	Si IF		150	40	25	150	14	4	34			2N332
2N160A	NPN	GP	Si IF		150	40	25	150	14	4	34			2N332
2N161	NPN	GP	Si RF		150	40	25	150	28	5	37			2N333
2N161A	NPN	GP	Si RF		150	40	25	150	28	5	37			2N333
2N162	NPN	GP	Si RF		150	40	25	150	38	8	38			2N335
2N162A	NPN	GP	Si RF		150	40	25	150	38	8	38			2N335
2N163	NPN	GP	Si RF		150	40	25	150	50	6	40			2N335
2N163A	NPN	GP	Si RF		150	40	25	150	50	6	40			2N335
2N164A	NPN	GE	Obsolete		65	15	20	85	40	8	39 max			2N168A
2N165	NPN	GE	Obsolete		65	15	20	85	72	5	36 max			2N169
2N166	NPN	GE	Obsolete		25	6	20	50	32	5	24			2N170
2N167	NPN	GE	Sw	3	75	30	75	85	30	9				2N167
2N168	NPN	GE	Obsolete		55	15	20	75	20	6	39 max			use 2N293
2N168A	NPN	GE	Osc	3	65	15	20	85	40	8	39 max			2N168A
2N169	NPN	GE	IF	3	65	15	20	85	72	9	35 max			2N169
2N169A	NPN	GE	IF	3	65	25	20	85	72	9	35 max			2N169A
2N170	NPN	GE	RF	3	55	6	20	50	20	4	27			2N170
2N172	NPN	TI	IF		65	16	5	75			28			2N168A
2N173	PNP	Dlc	Pwr		40W	−60	−7A	90	100	.6		8	20W	
2N174	PNP	Dlc	Pwr		40W	−80	−7A	90	45	.2		20	80W	
2N175	PNP	RCA	AF		20	−10	−2	50	65	.8	43			2N192
2N176	PNP	Motor	Pwr			−12	−600	80			25	3W		
2N178	PNP	Motor	Pwr		10W	−12	−600	80	30		29	3W		
2N179	PNP	Motor	Pwr			−20	−60	88			32	300		
2N180	PNP	CBS	AF Out		150	−30	−25	75	60	.7	37	3W	300	2N188
2N181	PNP	CBS	AF Out		250	−30	−38	75	60	.7	34	110	600	2N188A 25V
2N182	NPN	CBS	IF		100	25	10	75	25	3.5				2N167
2N183	NPN	CBS	Sw		100	25	10	75	40	7.5				2N167
2N184	NPN	CBS	Sw		100	25	10	75	60	12				2N167
2N185	PNP	TI	AF		150	−20	−150	50	55		40.5	2	250	2N188A
2N186	PNP	GE	AF Out	1	100	−25	−200	85	24	.8	28		300	2N186
2N186A	PNP	GE	AF Out	1	200	−25	−200	85	24	.8	30		750	2N186A
2N187	PNP	GE	AF Out	1	100	−25	−200	85	36	1	30		300	2N187
2N187A	PNP	GE	AF Out	1	200	−25	−200	85	36	1	30		750	2N187A
2N188	PNP	GE	AF Out	1	100	−25	−200	85	54	1.2	32		300	2N188
2N188A	PNP	GE	AF Out	1	200	−25	−200	85	54	1.2	32		750	2N188A
2N189	PNP	GE	AF	1	75	−25	−50	85	24	.8	37	1		2N189
2N190	PNP	GE	AF	1	75	−25	−50	85	36	1	39	1		2N190
2N191	PNP	GE	AF	1	75	−25	−50	85	54	1.2	41	1		2N191
2N192	PNP	GE	AF	1	75	−25	−50	85	75	1.5	43	1		2N192
2N193	NPN	Syl	Osc		50	15		75	6	3				2N167
2N194	NPN	Syl	Osc		50	15	50	75	7.5	3.5	15			2N169

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVCE	Ic ma	TJ°C	TYPICAL VALUES hfe	fab mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N206	PNP	RCA	AF		75	−30	−50	85	47	.8	46			2N191
2N207	PNP	Phil	AF		50	−12	−20	65	100	2				
2N207A	PNP	Phil	AF		50	−12	−20	65	100	2				2N241
2N207B	PNP	Phil	AF		50	−12	−20	65	100	2				2N241
2N211	NPN	Syl	Osc		50	10	50	75	30	3.5				2N293
2N212	NPN	Syl	Osc		50	10	50	75	15	6	22			2N293
2N213	NPN	Syl	AF		50	25	100	75	150		42			2N169A
2N214	NPN	Syl	AF Out		125	25	75	70	70	.8	29		200	2N188 (PNP)
2N215	PNP	RCA	AF		50	−30	−50	70	44	.7	41			2N191
2N216	NPN	Syl	IF		50	15	50	75	15	3	26			2N169
2N217	PNP	RCA	AF		50	−25	−70	50	70		33		160	2N192
2N218	PNP	RCA	IF		35	−16	−15	70	48	4.7	30			2N135
2N219	PNP	RCA	Osc		80	−16	−15	71	75	10	27			2N136
2N220	PNP	RCA	AF		50	−10	−2	71	65	.8	43			2N192
2N223	PNP	Phil	AF		100	−18	−150	65	95	.6	37	1		2N192
2N224	PNP	Phil	AF Out		150	−25	−150	75	75	.5	36		300	2N241A
2N225	PNP	Phil	AF Out		150	−25	−150	75	75	.5	36		300	2N241A
2N226	PNP	Phil	AF Out		100	−25	−150	65	55	.4	30		300	2N188A
2N227	PNP	Phil	AF Out		100	−25	−150	65	55	.4	30		300	2N188A
2N228	NPN	Syl	AF Out		50	25		75	70	.8	26		100	2N169
2N229	NPN	Syl	AF		50	12	40	75	25	1.6				2N169
2N230	PNP	Mall	Pwr		15W	−30	−2A	85	83	.014 (β)				
2N233	NPN	Syl	AF		50	10	50	75	4.5					
2N234	PNP	Bendix	Pwr		25W	−30	−3A	90			25	2		
2N234A	PNP	Bendix	Pwr		25W	−30	−3A	90			25	2		
2N235	PNP	Bendix	Pwr		25W	−40	−3A	90			33	2W		
2N235A	PNP	Bendix	Pwr		25W	−40	−3A	90			33	2W		
2N236	PNP	Bendix	Pwr		25W	−40	−3A	95			35	4		
2N236A	PNP	Bendix	Pwr		25W	−40	−3A	95			35	4		
2N237	PNP	Mar	AF		150	−45	−20	55	70	1	44			2N192 25V
2N238	PNP	TI	AF		50	−20		60			42			2N191
2N240	PNP	Phil	SB Sw		10	−6	−15		16					
2N241	PNP	GE	AF Out	1	100	−25	−200	85	73	1.3	35		300	2N241
2N241A	PNP	GE	AF Out	1	200	−25	−200	85	73	1.3	35		750	2N241A
2N242	PNP	Syl	Pwr			−45	−2A	100	40	5 Kc (β)	30	2.5W		
2N243	NPN	TI	SiAF		750	60*	60	150	.94α		30			
2N244	NPN	TI	SiAF		750	60*	60	150	.97α		30			
2N247	PNP	RCA	Drift RF		35	−35	−10	85	60	30	(37 @ 1.5Mc)			
2N248	PNP	TI	RF		30	−25	−5	85	20	50	12			
2N249	PNP	TI	AF Out		350	−25	−200	60	45		31	50	500	2N188A
2N250	PNP	TI	Pwr		12W	−30	−2A	80	50	6 Kc	34	6W		
2N251	PNP	TI	Pwr		12W	−60	−2A	80	50	6 Kc	34	6W		

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS				TYPICAL VALUES					Closest GE
					P_C mw @ 25°C	BV_{CE}	I_C ma	T_J°C	h_{fe}	f_{ab} mc	G_e db	P_o mw — Class A	P_o mw — Class B	
2N253	NPN	TI	IF		65	12	5	75			30			2N293
2N254	NPN	TI	IF		65	20	5	75			34			2N293
2N255	PNP	CBS	Pwr		1.5W/6.25W	−15	−3A	85	40	.2	23	1W	5W	
2N256	PNP	CBS	Pwr		1.5W/6.25W	−30	−3A	85	40	.2	26	2W	10W	
2N257	PNP	Cle	Pwr		2W/25W	−20		85	50	7 Kc (β)	30	1W		
2N260	PNP	Cle	Si		200	−10	−50	150	16	1.8	38			
2N260A	PNP	Cle	Si		200	−30	−50	150	16	1.8	38			
2N261	PNP	Cle	Si		200	−75	−50	150	10	1.8	36			
2N262	PNP	Cle	Si RF		200	−10	−50	150	20	6	40			
2N262A	PNP	Cle	Si RF		200	−30	−50	150	20	6	40			
2N265	PNP	GE	AF	1	75	−25	−50	85	110	1.5	45			2N265
2N267	PNP	RCA	RF Drift		Same as 2N247 except for flex. leads									
2N268	PNP	Cle	Pwr		2W/25W	−30			7	6 Kc (β)	28			
2N268A	PNP	Cle	Pwr		2W/10W	−60		90	20					
2N269	PNP	RCA	Sw		35	−20	−100	70	35	4				2N123
2N270	PNP	RCA	AF Out		150	−25	−150	50	70		32		500	2N320
2N274	PNP	RCA	RF Drift		35	−40*	−10	85	60	30	45			
2N277	PNP	Dlco	Pwr		55W	−40	−12A	95	60	.5	34	16W	30W	
2N278	PNP	Dlco	Pwr		55W	−50	−12A	95	60	.5	34	16W	30W	
2N279	PNP	Am	AF		125	−20	−10	75	30	.3				2N187
2N280	PNP	Am	AF		125	−20	−10	75	52	.3				2N188
2N281	PNP	Am	AF		167	−16	−50	75	70	.35	34	38		2N241
2N282	PNP	Am	AF (matched pr)			−16	−50	75	70	.35	23		390	2N241
2N283	PNP	Am	Sw		125	−20	−10	75	40	.5				2N188
2N284	PNP	Am	Sw		125	−32	−125	75	45	.35 min				2N188
2N284A	PNP	Am	Sw		125	−60	−125	75	45	.35 min				
2N290	PNP	Dlco	Pwr		55W	−70	−12A	95	50	.4	25	20W	85W	
2N291	PNP	TI	AF		180	−25	−200	85	45		33	50	500	2N188A
2N292	NPN	GE	IF	3	65	15	20	85	25	6	35 max			2N292
2N293	NPN	GE	RF	3	65	15	20	85	25	7	39 max			2N293
2N297	PNP	Cle	Pwr		15W	−60	−5A	85	35	6 Kc				
2N301	PNP	RCA	Pwr		12W	−40	−2A	85	70		30	2.7W		
2N301A	PNP	RCA	Pwr		12W	−60	−2A	85	70		30	2.7W		
2N302	PNP	Ray	Obsolete		150	−10	−200	85	45	7				2N186A
2N303	PNP	Ray	Obsolete		150	−30	−200	85	75	14				2N186A
2N306	NPN	Syl	AF		50	12		75	30	.75				2N292
2N307	PNP	Syl	AF Out			−35	−1A	75	25	4				
2N307A	PNP	Syl	Pwr		17W	−35	−2A	75	20	3.5 Kc	27			
2N308	PNP	TI	IF		30	−20	−5	55			41			
2N309	PNP	TI	IF		30	−20	−5	55			43			
2N310	PNP	TI	IF AF		30	−30	−5	55			37			

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVcb	Ic ma	Tj°C	TYPICAL VALUES hfe	fab mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N311	PNP	Motor	Sw		75	−15		85	50					2N123
2N312	NPN	Motor	Sw		75	15		85	50					2N167
2N313	NPN	GE	Obsolete		65	15	20	85	25	5	36 max			2N292
2N314	NPN	GE	Obsolete		65	15	20	85	25	8	39 max			2N293
2N315	PNP	GT	Sw		100	−15	−200	85	20	5				
2N316	PNP	GT	Sw		100	−10	−200	85	30	12				
2N317	PNP	GT	Sw		100	−6	−200	85	30	20				
2N318	PNP	GT	Photo		50	−12	−20		100	.75				
2N319	PNP	GE	AF Out	2	240	−20	−200	85	33	2	30		750	2N187A
2N320	PNP	GE	AF Out	2	240	−20	−200	85	48	2.5	32		750	2N188A
2N321	PNP	GE	AF Out	2	240	−20	−200	85	48	3	35		750	2N241A
2N322	PNP	GE	AF	2	140	−16	−100	85	70	2	39			2N190
2N323	PNP	GE	AF	2	140	−16	−100	85	90	2.5	41			2N191
2N324	PNP	GE	AF	2	140	−16	−100	85	80	3	43			2N192
2N325	PNP	Syl	Pwr		12W	−35	−2A	85	40	.2				
2N326	NPN	Syl	Pwr		7W	35	2A	85	40	.2				
2N327	PNP	Ray	SiAF		335	−50	−100	160	14	.2	32			
2N328	PNP	Ray	AF		335	−35	−100	160	24	.35	34			
2N329	PNP	Ray	AF		335	−30	−100	160	50	.5	36			
2N330	PNP	Ray	AF		335	−45	−50	160	30	.25	34			
2N331	PNP	RCA	AF		200	−30*	−10	85	48	.7	44.5			2N188A
2N332	NPN	TI-GE	SiAF	4	150	45*	25	200	15	30	35			2N332
2N333	NPN	TI-GE	SiAF	4	150	45*	25	200	35	33	39			2N333
2N334	NPN	TI-GE	SiAF	4	150	45*	25	175	.975 α	8 min				2N334
2N335	NPN	TI-GE	SiAF	4	150	45*	25	200	50	38	42			2N335
2N336	NPN	TI-GE	SiAF	4	150	45*	25	175	.99 α	7				2N336
2N344	PNP	Phil	RF (=SB101)		20	−5	−5	85	22	50				
2N345	PNP	Phil	RF (=SB102)		20	−5	−5	85	60	50				
2N346	PNP	Phil	RF (=SB103)		20	−5	−5	85	15	75				
2N350	PNP	Motor	Pwr		10W	−40*	−3A	90	30	5 Kc min	31		8W	
2N351	PNP	Motor	Pwr		10W	−40*	−3A	90	45	5 Kc min	33		8W	
2N352	PNP	Phil	Pwr		25W	−40	−2A	100	65	16 Kc	36	2.5W	10W	
2N353	PNP	Phil	Pwr		30W	−40	−2A	100	90	16 Kc	36	5W	10W	
2N354	PNP	Phil	Si Osc		150	−25	−50	140	18	15 f_{max}				
2N355	PNP	Phil	Si Sw		150	−10	−50	140	18	25 f_{max}				
2N356	NPN	GT	Sw		100	18	500	85	30	3				
2N357	NPN	GT	Sw		100	15	500	85	30	6				2N634
2N358	NPN	GT	Sw		100	12	500	85	30	9				2N635
2N376	PNP	Motor	Pwr		10W	−40*	−3A	90	60	5 Kc min	35		8W	
2N378	PNP	TS	Sw		15W	−20	−3A	85	35	7 Kc (β)				
2N379	PNP	TS	Sw		15W	−40	−3A	85	30	7 Kc (β)				
2N380	PNP	TS	Sw		15W	−30	−3A	85	60	7 Kc (β)				

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS				TYPICAL VALUES					Closest GE
					P_C mw @ 25°C	BV_{CE}	I_C ma	T_J°C	h_{fe}	f_{ab} mc	G_e db	P_o mw — Class A	P_o mw — Class B	
2N381	PNP	TS	AF Out		200	−25	−200	85	50	1.2	25		500	2N320
2N382	PNP	TS	AF Out		200	−25	−200	85	75	1.5	33		500	2N321
2N383	PNP	TS	AF Out		200	−25	−200	85	100	1.8	31		500	2N321
2N384	PNP	RCA	RF Drift		120	−30	−10	85	.984 α	100	34			
2N386	PNP	Phil	Pwr		12.5W	−60	−3A	100	20	7 Kc				
2N387	PNP	Phil	Pwr		12.5W	−80	−3A	100	20	6 Kc				
2N393	PNP	Phil	Sw		50	−6	−50	85	155	60 f_{max}				
2N394	PNP	GE	Sw	2	150	−10	−200	100	150	5.5				2N394
2N395	PNP	GE	Sw	2	150	−15	−200	100	150	7				2N395
2N396	PNP	GE	Sw	2	150	−10	−200	100	150	7				2N396
2N397	PNP	GE	Sw	2	150	−10	−250	100	150	10				2N397
2N398	PNP	RCA	Sw	2	50	−105	−100	85	60					
2N399	PNP	Bendix	Pwr		25W	−40	−3A	90			33			
2N401	PNP	Bendix	Pwr		25W	−40	−3A	90			30			
2N402	PNP	W	AF		180	−20	−150	85	.96 α	600 Kc	37			2N188A
2N403	PNP	W	AF Out		180	−20	−200	85	.97 α	850 Kc	32	30		2N187A
2N404	PNP	RCA	Sw		120	−24	−100	85		12				2N396
2N405	PNP	RCA	AF		150	−18	−35	85	35	650 Kc	43			2N188A
2N406	PNP	RCA	AF		150	−18	−35	85	35	650 Kc	43			2N188A
2N407	PNP	RCA	AF Out		150	−18	−70	85	65		33		160	2N241A
2N408	PNP	RCA	AF Out		150	−18	−70	85	65		33		160	2N241A
2N409	PNP	RCA	IF		80	−13	−15	85	45	6.8	38.8			2N135
2N410	PNP	RCA	IF		80	−13	−15	85	45	6.8	38.8			2N135
2N411	PNP	RCA	RF		80	−13	−15	85	75	10				2N137
2N412	PNP	RCA	RF		80	−13	−15	85	75	10				2N137
2N413	PNP	Ray	RF		150	−18	−200	85	30	2.5	10			2N135
2N413A	PNP	Ray	IF		150	−15	−200	85	30	2.5	33			2N135
2N414	PNP	Ray	RF		150	−15	−200	85	60	7	16			2N136
2N414A	PNP	Ray	IF		150	−15	−200	85	60	7	35			2N136
2N415	PNP	Ray	RF		150	−10	−200	85	80	10	30			2N137
2N415A	PNP	Ray	IF		150	−10	−200	85	80	10	30			2N137
2N416	PNP	Ray	RF		150	−12	−200	85	80	10	20			2N137
2N417	PNP	Ray	RF		150	−10	−200	85	140	20	27			
2N422	PNP	Ray	AF		150	−20	−100	85	50	.8	38			2N188A(2N320)
2N425	PNP	Ray	Sw		150	20	−400	85	15	4				2N394
2N426	PNP	Ray	Sw		150	−18	−400	85	18	6				2N395
2N427	PNP	Ray	Sw		150	−15	−400	85	20	11				2N396
2N428	PNP	Ray	Sw		150	−12	−400	85	30	17				2N397
2N438	NPN	CBS	Sw		100	30*		85	25	2.5 min				
2N439	NPN	CBS	Sw		100	30*		85	35	5 min				2N634
2N440	NPN	CBS	Sw		100	30*		85	65	10 min				2N635
2N444	NPN	GT	Sw		100	15		85	15	.5 min				

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS Pc mw @ 25°C	BVCE	Ic ma	TJ°C	TYPICAL VALUES hfe	fab mc	Ge db	Po mw — Class A	Po mw — Class B	Closest GE
2N445	NPN	GT	Sw		100	12		85	35	2 min				2N634
2N446	NPN	GT	Sw		100	10		85	60	5 min				2N635
2N447	NPN	GT	Sw		100	6		85	125	9 min				
2N450	PNP	GE	Sw	8	150	−12	−125	85	60 min	11				2N450
2N451	NPN	GE	SiPwr	6	85W	65	5A	150	16	400 Kc	4			2N451
2N452	NPN	GE	SiPwr	6	85W	65	5A	150	12	400 Kc	2.5			2N452
2N453	NPN	GE	SiPwr	6	85W	65	2A	150	30	400 Kc	6			2N453
2N454	NPN	GE	SiPwr	6	85W	65	2A	150	15	400 Kc	10			2N454
2N460	PNP	TS	AF		200	−45*	−400	100	.96α	1.2				2N319
2N461	PNP	TS	AF		200	−45*	−400	100	.98α	1.2				2N320
2N462	PNP	Phil	Sw		150	−40*	−200	75	45	.5 min				2N188A
2N464	PNP	Ray	AF		150	−40	−100	85	26	.7	40			
2N465	PNP	Ray	AF		150	−30	−100	85	45	.8	42			2N188A(2N320)
2N466	PNP	Ray	AF		150	−20	−100	85	90	1	44			2N241A(2N321)
2N467	PNP	Ray	AF		150	−15	−100	85	180	1.2	45			
2N489		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N489
2N490		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N490
2N491		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N491
2N492		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N492
2N493		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N493
2N494		GE	SiUni	5	SEE G-E TRANSISTOR SPECIFICATIONS SECTION									2N494
2N495	PNP	Phil	SiOSC		150	−25	−50	140	18	15 f_{max}				
2N496	PNP	Phil	SiOSC		150	−10	−50	140	18	25 f_{max}				
2N508	PNP	GE	AF	2	140	−16	−100	85	125	3.5	45			2N508
2N518	PNP	GE	Sw	8	150	−12	−125	85	60 min	11				2N518
2N519	PNP	GT	Sw		100	−15		85	25	.5 min				2N186
2N520	PNP	GT	Sw		100	−12		85	40	3 min				
2N521	PNP	GT	Sw		100	−10		85	70	8 min				2N397
2N522	PNP	GT	Sw		100	−8		85	120	15 min				
2N523	PNP	GT	Sw		100	−6		85	200	21 min				
2N524	PNP	GE	AF	2	225	−30	−500	100	30	2				2N524
2N525	PNP	GE	AF	2	225	−30	−500	100	44	2.5				2N525
2N526	PNP	GE	AF	2	225	−30	−500	100	64	3.0				2N526
2N527	PNP	GE	AF	2	225	−30	−500	100	81	3.3				2N527
2N529	NPN-PNP	GT	AF		100	15		85	17	2.5				
2N530	NPN-PNP	GT	AF		100	15		85	22	3.0				
2N531	NPN-PNP	GT	AF		100	15		85	27	3.5				

JETEC No.	Type	Mfr.	Use	Dwg. No.	MAX. RATINGS				TYPICAL VALUES					Closest GE
					P_C mw @ 25°C	BV_{CE}	I_C ma	T_J°C	h_{fe}	f_{ab} mc	G_e db	P_o mw — Class A	P_o mw — Class B	
2N532	NPN-PNP	GT	AF		100	15		85	32	4.0				
2N533	NPN-PNP	GT	AF		100	15		85	37	4.5				
2N538	PNP	M-H	Pwr		10W	−80*	−20	95		8 Kc				
2N538A	PNP	M-H	Pwr		10W	−80*	−20	95		8 Kc				
2N539	PNP	M-H	Pwr		10W	−80*	−20	95		7 Kc				
2N539A	PNP	M-H	Pwr		10W	−80*	−20	95		7 Kc				
2N540	PNP	M-H	Pwr		10W	−80*	−20	95		6 Kc				
2N540A	PNP	M-H	Pwr		10W	−80*	−20	95		6 Kc				
2N544	PNP	RCA	RF		80	−18*	−10	85	60	30	30.1			
2N554	PNP	Motor	Pwr		10W	−40*	−3A	90	30	8 Kc	34			
2N555	PNP	Motor	Pwr		10W	−40*	−3A	90	30	8 Kc	34			
2N574	PNP	M-H	Pwr		100W	−60*	−15A	95		6 Kc				
2N574A	PNP	M-H	Pwr		100W	−80*	−15A	95		6 Kc				
2N575	PNP	M-H	Pwr		100W	−60*	−15A	95		5 Kc				
2N575A	PNP	M-H	Pwr		100W	−80*	−15A	95		5 Kc				
2N577	PNP	Mu	Photo		25	−25	−10	55						
2N578	PNP	RCA	Sw		120	−14	−400	85	15	5				2N395
2N579	PNP	RCA	Sw		120	−14	−400	85	30	8				2N396
2N580	PNP	RCA	Sw		120	−14	−400	85	45	15				2N397
2N581	PNP	RCA	Sw		80	−15	−100	85	30	8				2N396
2N582	PNP	RCA	Sw		120	−14	−100	85	60	18				
2N583	PNP	RCA	Sw		80	−15	−100	85	30	8				
2N584	PNP	RCA	Sw		120	−14	−100	85	60	18				
2N585	NPN	RCA	Sw		120	24	200	85	40	5				
2N634	NPN	GE	Sw	2	150	20	300	85	15	8				2N634
2N635	NPN	GE	Sw	2	150	20	300	85	25	12				2N635
2N636	NPN	GE	Sw	2	150	20	300	85	35	17				2N636
3N21	Pt	Syl	Sw		100	−60		50						
3N22	NPN	WE	RF			15*		85	96α	24				
3N23	NPN	GP			50	30	5			10	12			
3N23A	NPN	GP			50	30	5			20	14			
3N23B	NPN	GP			50	30	5			35	15			
3N23C	NPN	GP			50	30	5			50	17			
3N29	NPN	GE	Obsolete		50	6	20	85	100	40	10			
3N30	NPN	GE	Obsolete		50	6	20	85	100	80	10			
3N31	NPN	GE	Obsolete		50	6	20	85	100	20	10			
3N36	NPN	GE	RF	7	30	6	20	85	2.2∠−81°	50 min	11.5			3N36
3N37	NPN	GE	RF	7	30	6	20	85	1.1∠−100°	90 min	9			3N37

NOTE: *Closest GE types* are given only as a general guide and are based on available published electrical specifications. However, General Electric Company makes no representation as to the accuracy and completeness of such information. Since manufacturing techniques are not identical, the General Electric Company makes no claim, nor does it warrant, that its transistors are exact equivalents or replacements for the types referred to.

EXPLANATION OF SYMBOLS

TYPES AND USES:

Si—Silicon High Temperature Transistors (all others germanium)
Pt—Point contact types
AF—Audio Frequency Amplifier—Driver
AF Out—High current AF Output
Pwr—Power output 1 watt or more
RF—Radio Frequency Amplifier
Osc—High gain High frequency RF oscillator
IF—Intermediate Frequency Amplifier
lo IF—Low IF (262 Kc) Amplifier
Sw—High current High frequency switch
AF Sw—Low frequency switch

RATINGS:

P_C=*Maximum collector dissipation* at 25°C (76°F) ambient room temperature. Secondary designations are ratings with connection to an appropriate heat sink.

BV_{CE}=*Minimum collector-to-emitter breakdown voltage.* GE transistors measured with Base-to-emitter resistance as follows:
10K for AF and AF Out PNP
1 Meg for RF, IF, and Osc PNP
Open circuit for NPN

*Under BV_{CB}=Minimum collector-to-base breakdown voltage (for grounded base applications).

I_C=*Maximum collector current.* (Negative for PNP, Positive for NPN.)

T_J=Maximum centigrade *junction temperature.* P_C must be derated linearily to O mw dissipation at this temperature.

h_{fe}=Small signal base to collector *current-gain,* or Beta (except where emitter to collector gain, alpha α, is given).

f_{ab}=*Alpha cut-off-frequency.* Frequency at which the emitter to collector current gain, or alpha, is down to $1\sqrt{2}$ or .707 of its low frequency audio value. For some power transistors, the Beta or base-to-collector current-gain cutoff—frequency is given as noted.

G_e=Grounded-emitter *Power Gain.*
AF, AF Out, and Pwr Gain measured at 1 Kc.
RF, IF, and Osc Gains at 455 Kc.
(Sw Gain is dependent on circuit and wave-shape.)
(All measured at typical power output level for given transistor type.)

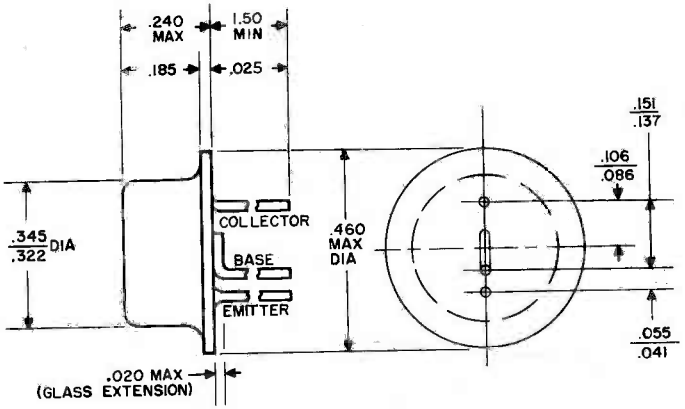
P_o=Maximum *Power Output* at 5% harmonic distortion, in mw except where noted as watts. Class A single-ended, Class B Push Pull.

MANUFACTURERS:

Am—Amperex
Bendix—Bendix Aviation Corp.
CBS—CBS-Hytron.
Cle—Clevite Transistor Products.
Dlc—Delco Radio Div., General Motors Corp.
GE—General Electric Company.
GP—Germanium Products Corp.
Mall—P. R. Mallory and Company, Inc.
Mar—Marvelco, National Aircraft Corp.
M-H—Minneapolis-Honeywell Regulator Co.
Motor—Motorola, Inc.
Mu—Mullard Ltd.
Phil—Philco.
Ray—Raytheon Manufacturing Company.
RCA—RCA.
Sprague—Sprague Electronics Company.
Syl—Sylvania Electric Products Company.
TI—Texas Instruments, Inc.
TS—Tung-Sol.
W—Westinghouse Electric Corp.
WE—Western Electric Company.

OUTLINE DRAWINGS

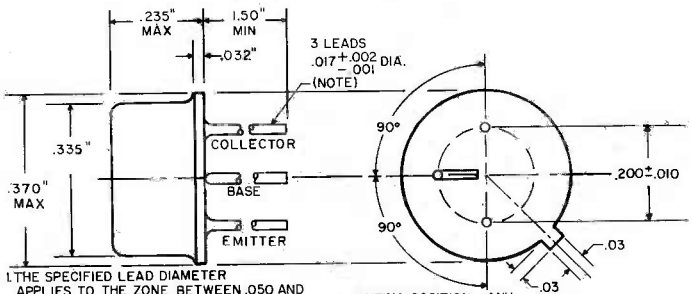
1



2

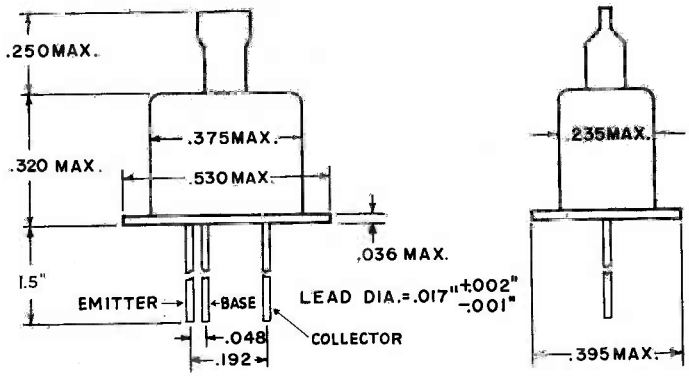
DIMENSIONS WITHIN

JETEC OUTLINE	JETEC BASE
TO-5	E3-44



1. THE SPECIFIED LEAD DIAMETER APPLIES TO THE ZONE BETWEEN .050 AND .250 FROM THE BASE SEAT. A MAXIMUM DIAMETER OF .021 IS HELD BETWEEN .250 AND 1.5. THE LEAD DIAMETER IS NOT CONTROLLED OUTSIDE OF THESE ZONES.
2. MOUNTING POSITION – ANY
3. WEIGHT .05 OZ.
4. BASE CONNECTED TO TRANSISTOR SHELL
5. DIMENSIONS IN INCHES

3

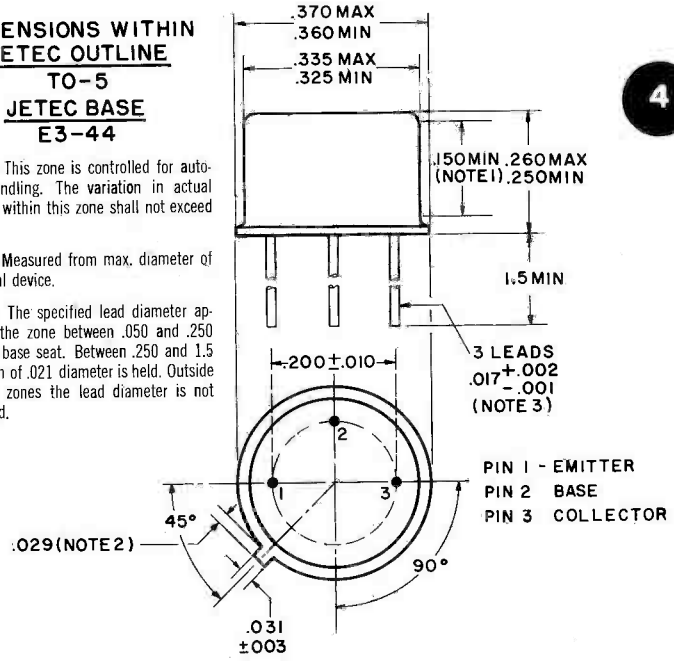


DIMENSIONS WITHIN JETEC OUTLINE TO-5 JETEC BASE E3-44

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.



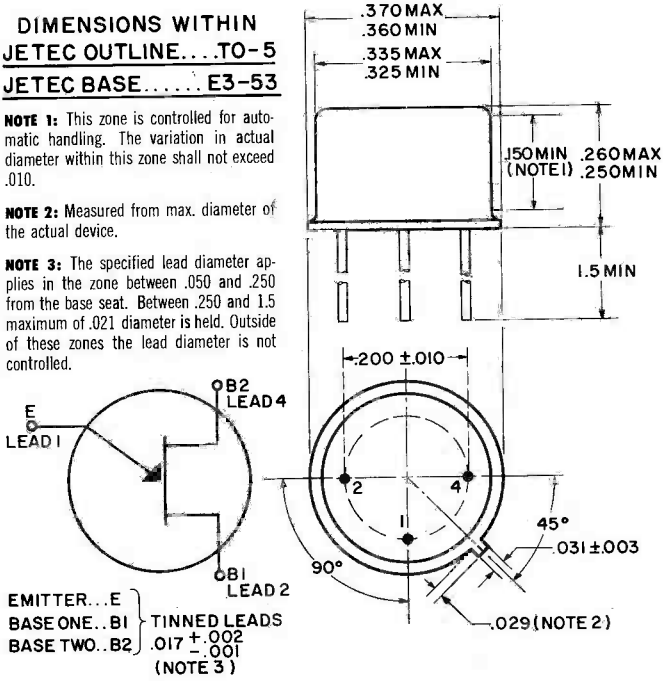
4

DIMENSIONS WITHIN JETEC OUTLINE....TO-5 JETEC BASE.....E3-53

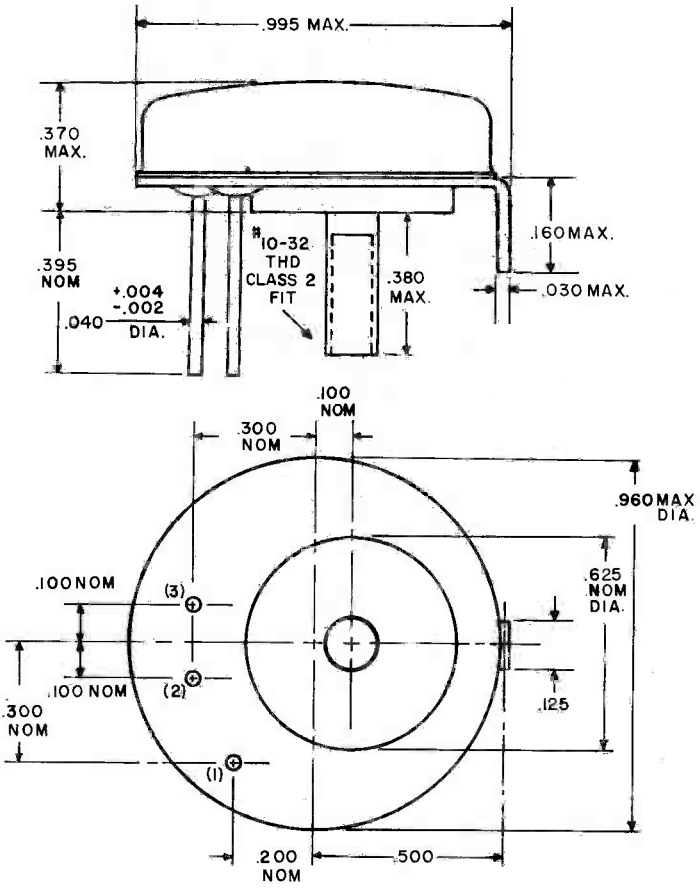
NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and 1.5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.

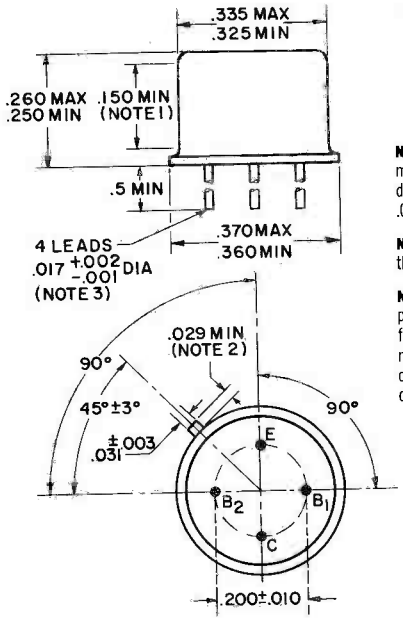


5



PIN 1 - EMITTER
PIN 2 BASE
PIN 3 COLLECTOR (INTERNALLY CONNECTED TO CASE)
WEIGHT: .40 OZ.

MAX. ALLOWABLE TORQUE ON STUD - 15 IN. LBS



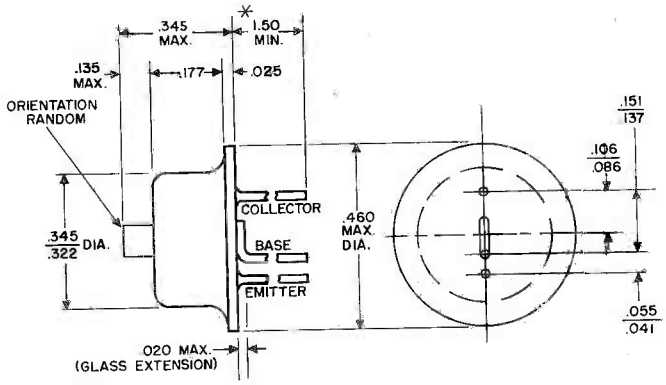
DIMENSIONS WITHIN JETEC OUTLINE TO-12 JETEC BASE E4-54

7

NOTE 1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed .010.

NOTE 2: Measured from max. diameter of the actual device.

NOTE 3: The specified lead diameter applies in the zone between .050 and .250 from the base seat. Between .250 and .5 maximum of .021 diameter is held. Outside of these zones the lead diameter is not controlled.



8

* CUT TO 0.200" FOR USE IN SOCKETS.
LEADS TINNED DIA. .018
MOUNTING POSITION - ANY
WEIGHT: .05 OZ.
BASE CONNECTED TO TRANSISTOR SHELL.
DIMENSIONS IN INCHES.

CIRCUIT DIAGRAM INDEX

Continued — following page

NOTES ON THE CIRCUIT DIAGRAMS

TRANSFORMERS

The audio transformers used in these diagrams were wound on laminations of 1⅝" by 1⅜" and a ½" stock size, and having an electrical efficiency of about 80%. Smaller or less efficient transformers will degrade the electrical fidelity of the circuits.

OSCILLATOR COIL

Ed Stanwyck Coil Company #1265
Onondaga Electronic Laboratories #A-10047 or equivalent

VARIABLE CONDENSER

Radio Condenser Company Model 242
Onondaga Electronic Laboratories #A-10053 or equivalent

FERRITE ROD ANTENNA

Onondaga Electronic Laboratories #A-10067 or equivalent

If you are unable to obtain these components from either your local or a national electronic parts distributor, we suggest you contact:

Onondaga Electronic Laboratories
112 Dewitt Street
Syracuse 3, N. Y.

READING LIST

The following list of semiconductor references gives texts of both elementary (E) and advanced (A) character. Obviously, the list is not inclusive, but it will guide the reader to other references.

Garner, L., *Transistor Circuit Handbook* (E)
(Coyne)

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(McGraw-Hill)

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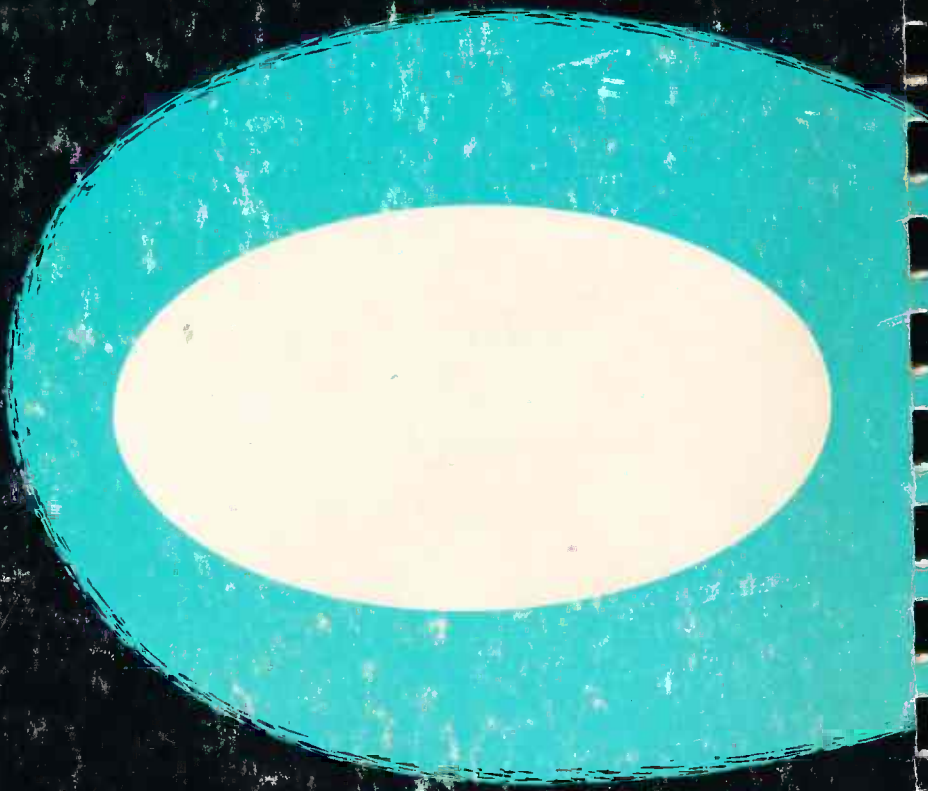

SEMICONDUCTOR PRODUCTS DEPARTMENT

GENERAL ELECTRIC

ELECTRONICS PARK • SYRACUSE 1, N. Y.

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