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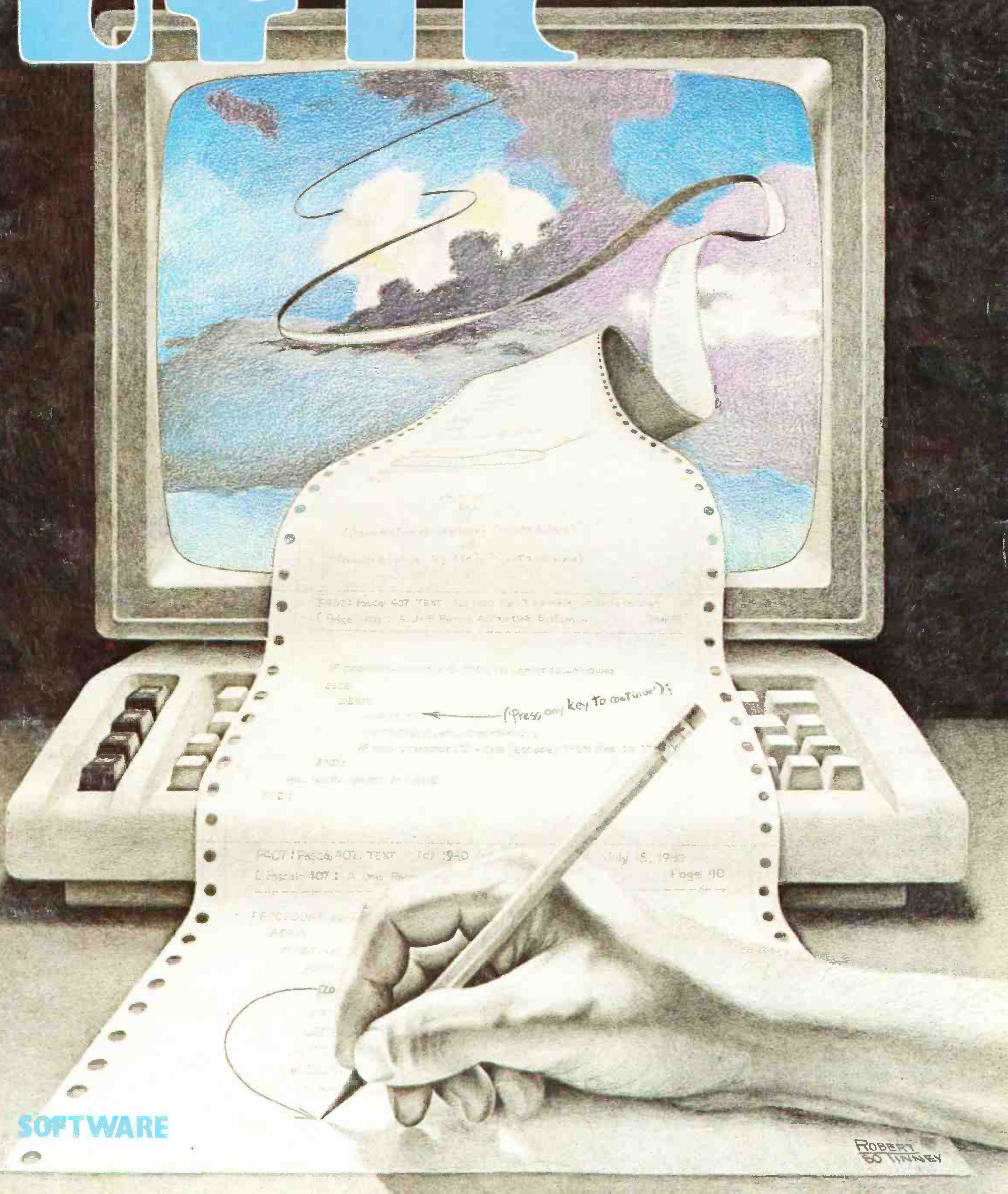
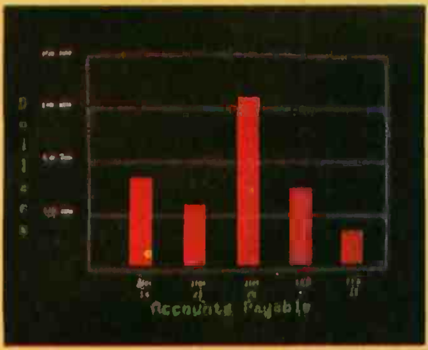
BYTE®

the small systems journal

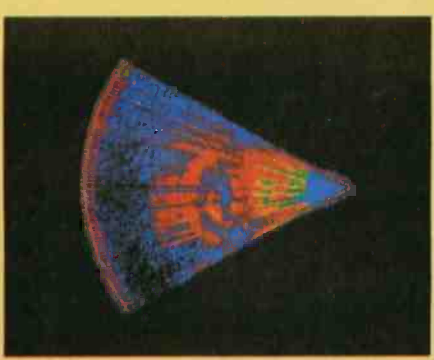
A McGRAW-HILL PUBLICATION



SOFTWARE



Management Information Display



Ultrasonic heart sector scan

High-resolution display with alphanumerics

Get the professional color display that has BASIC/FORTRAN simplicity

LOW-PRICED, TOO

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

Basically, this new Cromemco Model SDI* is a two-board interface that plugs into any Cromemco computer.

The SDI then maps computer display memory content onto a convenient color monitor to give high-quality, high-resolution displays (756 H x 482 V pixels).

When we say the SDI results in a high-quality professional display, we mean **you can't get higher resolution than this system offers in an** NTSC-conforming display.

The resolution surpasses that of a color TV picture.

BASIC/FORTRAN programming

Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

*U.S. Pat. No. 4121283

Model SDI High-Resolution Color Graphics Interface

HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

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Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

DISPLAY MEMORY

Along with the SDI we also offer an optional fast and novel **two-port** memory that gives independent high-speed access to the computer memory. The two-port memory stores one full display, permitting fast computer operation even during display.

CONTACT YOUR REP NOW

The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

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Tomorrow's computers today

Circle 1 on Inquiry card.

Here's the state of the art in low-cost hard-disk computers

11 MEGABYTES OF FAST HARD-DISK STORAGE

Yes, the Cromemco Model Z-2H is in a class by itself in the computer field.

These Z-2H features tell you why:

- **11 megabytes of hard-disk storage**
- **64 kilobytes of fast RAM**
- **Two dual-sided floppy disk drives**
- **Z-80A type processor**
- **Fast 4 MHz operation—150 nanosecond access time**
- **Fast hard-disk transfer rate of 5.6 megabits/second**
- **Low cost**

And that's not all you get. Not nearly.

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You also get Cromemco software support—the broadest software support in the microcomputer field. Software that Cromemco is known for. Like this:

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- **FORTRAN IV**
- **RATFOR (RATional FORtran)**
- **COBOL**
- **Z-80 Macro Assembler**
- **Word Processing System**
- **Data Base Management**

And more all the time.

FIELD PROVEN

The Z-2H is clearly in a class by itself. We introduced it last summer. It's field proven. It's reliable.

And it's rugged. Housed in a sturdy, all-metal cabinet.

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As always with Cromemco, you get expandability. The fast 64K RAM in this Model Z-2H can be expanded to 512 kilobytes. That amount of RAM combined with 11 megabytes of hard-disk storage gives you enormous computer power—the equal or even beyond what much larger computers sometimes offer.

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LOW COST — SEE IT NOW

The Z-2H is real. It's been in the field for many months. It's proven itself.

You should see the Z-2H now. Contact a Cromemco representative and arrange for a demo. Learn that Cromemco is a survey-winner for reliability.

And learn that the Z-2H is under $10K.

In the long run it always pays to get the best.

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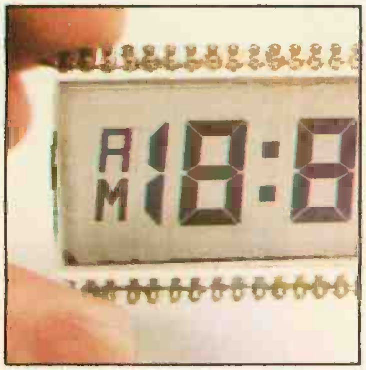
In The Queue

BYTE October 1980
Volume 5, Number 10



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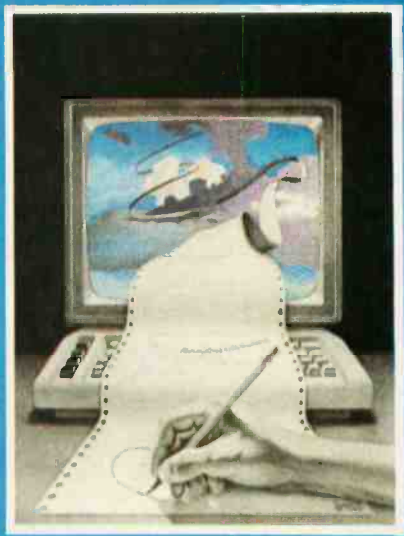
Foreground

Background

Nucleus



IN THIS ISSUE

Our main topic this month is Software — a perennial favorite among BYTE readers. This month's cover painting by Robert Tinney illustrates the colorful road that programmers often travel in search of bug-free code.

The software articles include: a tiny compiler that handles floating-point operations; machine problem-solving using cryptarithmetic; sorting with binary trees; a macro assembler for your computer; adding to the 6502's instruction set; an easy-to-use information retrieval system; and symbolic math using BASIC.

Also this month: Steve Ciarcia's explanation of how to use liquid-crystal displays; a description of some vector graphics for raster-scan displays; a follow-up on FORTH; and the second part of a three-part discussion of an 8088 processor for the S-100 bus.

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Editorial

Who Reads BYTE?

by Carl Helmers

In this month's editorial we will summarize some of the key results of a recent BYTE reader survey, performed by the McGraw-Hill Research group. A six-page questionaire was mailed to 2000 BYTE subscribers earlier this year. The subscribers were selected from our mailing list on an every-*n*th-name basis. Of the 2000 questionaires mailed, 1445 were completed and returned within the six-week deadline. The 73.5% response to this survey request was exceptional. Such a large response to a detailed six-page form by itself indicates the enthusiasm and interest of our typical reader.

A major objective of the survey was to analyze the reading habits of our readers; a second objective was to obtain hard information about the professional orientation of our readers; and a third was to determine demographic data.

Dear to our editorial convictions, our survey contained a major section on programming languages. Next, we wanted to characterize the impact of microcomputing on the reader's personal life. Some miscellaneous information about present and future computing-equipment ownership completed the survey design. The form of the survey followed that of the two previous surveys we have done. The layout of the questionaire was designed and executed by Nancy Estle and her associates in the BYTE production department. In this editorial, we can cover only some selected results from the survey. The complete computer-tabulated results take much more room than the space available in a single issue of BYTE.

We found that the typical BYTE reader is a professional who uses a computer as part of his or her job. Of the entire sample, 85% use computers in their everyday work.

One question we asked was "What is your principal occupation?" Almost 40% of the readers responded that they were engineers or scientists. Programmers or analysts (in the traditional data-processing sense of the terms) comprised 18% of the response. Some 13% classified themselves as owners or managers of a business. Table 1a shows the seven categories on the questionaire and their percentages.

As an alternative approach to the same truth, we asked respondents to list their exact job title. The survey's analysis classified responses to the question in several categories. Table 1b shows the catagories that received 1% or more in ratings.

As in the two previous surveys, the results showed a highly educated reader. In this year's survey, 10% indicated completion of a PhD (7%) or other advanced professional degree (3%), 18% have master's degrees, 19% have had some graduate school, and 21% indicated completion of a four-year college degree. This gives a total of 68% of BYTE readers who have completed a bachelor's degree or higher. If we extend the categories to "some college" (17%) and "associate's degree" (8%), we find that 93% of BYTE's readers have achieved some educational accomplishments beyond high school.

Consistent with this educational background and professional orientation, the typical BYTE reader is fairly well-paid for the work he does. In this year's survey, we found an average personal income of about $29,000 and an average household income of about $36,000. If this is the average, we should expect that a fair amount of discretionary money is available for personal computing and other trappings of the modern middle-class life. And so it is.

Essentially all (98%) of BYTE readers have high-fidelity audio equipment averaging $619.33 in cost. Having such equipment, 99% of our readers indicated that they purchase an average of 9.13 records or tapes during a year's

"For reliable data storage, you can't beat Shugart's Minifloppy."™

Raymond Schlitzer, Owner–
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"I sell systems my customers can depend on. That's why most of the personal and small business computer systems sold here feature Minifloppy disk drives. I know from experience I can rely on the Minifloppy."

Since 1976 Shugart's Minifloppy has been used by more small computer system manufacturers than any other drive. In fact, more than half-a-million Minifloppys have been installed. The Minifloppy looks small—but it stores a lot of data. 250 kilobytes on one side, or up to 500 kilobytes in the double-sided model. That's about 50 pages of printed information on a single-sided Minidiskette, and twice that on the double-sided version. You'll have plenty of storage capacity for your programs, letters, forms, or ledger entries. And you find your data fast, too, because the Minifloppy is a random access device that eliminates the need to search for your data serially as you must with a tape cassette unit.

No matter what problem you're solving with your computer system, you can rely on Shugart's Minifloppy for data storage. We're known as the Headstrong company for good reason. We're Headstrong about reliability, quality, and value. Ask your dealer. He knows us.

Rely on the Headstrong Company.

Shugart

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TM—Minifloppy is a trademark of Shugart Associates.

Occupation	Percent
Programmer/Analyst	18
Engineer/Scientist	39.5
Business Owner/Manager	13
Educator	4.5
Student	8
Professional (law, medicine, accounting, etc)	5.5
Other	11.5

Table 1a: *"What is your principal occupation? (check one)*

Title	Percent
Engineer	20
Manager or Director	17
Engineering Technician	11
Executive or Official	10
Programmer	6
Professional (Lawyers, Doctors, etc)	5.5
Teacher, Professor, or Educator	5
Systems Analyst	3.5
Student	3
Scientist	3
Consultant	2
Financial	1
All other titles	11
None or Unemployed	2

Table 1b: *Classifications of job titles. This table shows how McGraw-Hill Research classified open-ended responses to the question "What is your exact title?" as found in the 1980 BYTE Reader Survey. The table shows only those classifications which had 1% response or more. Percentages are rounded to the nearest half percent.*

time. Many BYTE readers have spent significant sums on photographic equipment; 48% of those surveyed spent between $201 and $1000 on cameras and related equipment. But only 12% of BYTE readers as of this survey indicate possession of a videotape recorder.

Fortunately for the quality of air at conventions and other meetings where BYTE readers are likely to be seen, 78% of our readers are nonsmokers. One quarter of our readers never drink wine, and 38% drink wine only occasionally (1 to 4 times per month; the average BYTE reader drinks wine 4.65 times per month). We did *not* ask a complementary question regarding personal tastes which is suggested by these low figures for smoking and drinking: "How many hours a day do you spend doing intense exercise activities (walking, bicycling, jogging, playing tennis or racquetball, swimming, calisthenics, etc)?" We suspect that the responses would be fairly high to this category of question.

Continuing with demographic data, we learned that our typical BYTE reader is 35 years of age, male, and head of a household with four members. Overall, 98% of the readers sampled were male. Some 79% of the readers indicated that they were the head of a household. In response to the "marital status" question, 62% indicated that they were married, 31% indicated they were still single, 5% indicated that they were divorced or separated. The question "How many people are there in your household?" found 3.95 as the mean response. Some 52.1% of the readers sampled indicated that there were 3 or more members of their household. One can

Cost of System	Percentage
Less Than $500	9.7
$500 to $1000	18.3
$1100 to $2000	17.9
$2100 to $3000	11.7
$3100 to $4000	9.7
$4100 to $5000	8.2
$5100 to $7500	7.7
$7510 to $15000	6.8
Over $15000	10.0

Table 2: *Distribution of approximate cost of personal-computer systems. The approximate costs of personal-computer systems owned by BYTE readers were classified into 9 bins. In each bin, we show a percentage response of the total number of those readers who stated a cost of their systems in the survey.*

thus draw the conclusion that most of BYTE's readers are family-oriented.

One of the most frequently asked questions we hear is "How many people have personal computers?" In terms of the BYTE survey's results, the percentage is 71%. The mean system price is $7415, based on the 792 respondents who gave a cost figure in response to the question "What is the approximate cost of your system?" From this mean price, ignoring any deviation in the distribution, we can extrapolate the economic effects of the approximately 160,000 BYTE readers to the ballpark figure of $842 million over the time period in which this equipment was being acquired. Seven-eighths of a billion dollars is no small amount.

	Frequent (F)	Occasional (O)	Intended (I)	1980 Literacy F+O+I	1978 Literacy F+O+I	Change
BASIC	47	25	14.5	86.5	86	+ .5
Assembly Language	33	26	13	72	76	− 4
FORTRAN	21	39	12	72	79	− 7
Machine Object Code	18.5	34	13.5	66	74	− 8
Pascal	6.5	6	28	40.5	14	+26.5
COBOL	8	16	11	35	36	− 1
PL/I	5	12	10	27	31	− 4
APL	2	9	11	22	30	− 8
ALGOL	1.5	9	9	19.5	23	− 3.5
C	3	2	7	12	NA	NA
PL/M	2	2.5	6.5	11	11	0
FORTH	1.5	1.5	7	10	4	+ 6
LISP	.5	2	1.5	4	NA	NA
RPG	1	2	1	4	NA	NA
SNOBOL	.5	2.5	.5	3.5	NA	NA

Table 3: *Ranking of language literacy. The first three columns contain raw data expressed as a percentage of the total number of returned survey forms in the 1980 survey. Defining literacy in a computer language as "knowing enough about it to use it" or "a desire to use it," we formed the fourth column as a sum of responses to frequent use, occasional use, or intended use. This gives a ranking of the various language options available for small computer users. The most significant change relative to the earlier (1978 survey) data is the movement of Pascal into fifth place in the ranking from its previous ninth-place ranking in our 1978 survey. The questions in both surveys were identical except that in the later one we added several languages to the list. Thus "NA" in the 1978 column indicates a language which was not mentioned explicitly in the earlier survey; no entry is shown in the change column for these languages.*

Rank	CATEGORY	Mean
1.	Applications to Every Day Life	6.42
2.	Computer Control of Mechanics	6.21
3.	The Art of Programming	6.20
4.	Applications to Engineering	6.05
5.	The Art of Hardware Design	5.87
6.	Household Automation	5.75
7.	Personal Data Base Design and Implementation	5.73
8.	Applications to Personal Business	5.72
9.	Text Editing and Processing	5.67
10.	Computer System Design	5.58
11.	Graphics Software Design	5.52
12.	Computer Communications Networks	5.39
13.	Logical (Thinking) Games	5.25
14.	Educational Uses	5.15
15.	Voice Recognition	5.05
16.	Experimentation with Designs	4.94
17.	Design of Information Structures	4.90
18.	Simulations	4.87
19.	Voice Synthesis	4.86
20.	Applications to Physical Sciences	4.78

Table 4: *Rankings of interest areas. A list of 38 categories was presented as part of the survey. Respondents were asked to give a personal preference ranking from 0 (no interest) to 10 (highest interest). The data from this question was tallied and the mean ratings for each computed. This list shows the top 20 categories ranked by this mean. The lowest ranking of the 38 categories shown in the question was 2.24.*

Table 2 shows the distribution of costs. Note that approximately 43% of those who specified an approximate cost of their personal systems indicated $3100 or more had been spent. The average amount spent was computed using the raw data for this question, prior to creation of this table. It is thus clear that the deviation between the average and the median is caused by a few expensive machines in the last, open-ended category of "over $15,000."

A result of the high average cost of the present-day personal-computer system is that such systems are becoming more and more elaborate. No longer do we see as much use of a bare machine, without peripherals or mass storage. The typical $7415 machine can and does support a significant amount of computing power. Nowhere is this more evident than in our continuing survey of that crucial part of computing, computer language literacy. Table 3 summarizes the respondents' use of various languages. As in previous versions of the survey, each language was associated with a mutually exclusive set of five states of language use: frequent, occasional, intended, no knowledge, and the catch-all "don't know or no answer." The interesting point to make here

The man, the wi

is the change between this year's survey and the 1978 survey.

In particular, due to the dominance of BASIC-oriented personal-computing machinery, BASIC remains unchanged at the top of the list in terms of literacy. (Literacy is defined here as the sum of the responses that indicated sufficient knowledge to use, or intend to use, the language.) But also significant was the change in the perception of Pascal on the part of readers. The ranking of this language by literacy has advanced 26.5 percentage points since the previous survey in January 1978. This is undoubtedly due to the increasing size of the typical machine and the wide availability of computer systems with the UCSD Pascal Software System (now marketed by SofTech Microsystems of San Diego, California). Software advertisements in BYTE for Pascal compilers or systems today number in the vicinity of a half a dozen, a significant indicator of interest in that language on the part of vendors.

We'll conclude by presenting one more table (table 4) which was derived from the survey responses. This table is a ranking of the top 20 areas of personal interest in the application and use of computers. Finally, to all those readers that reponded to this survey with such enthusiasm, the entire staff of BYTE thanks you.■

Articles Policy

BYTE is continually seeking quality manuscripts written by individuals who are applying personal computer systems, designing such systems, or who have knowledge which will prove useful to our readers. For a more formal description of procedures and requirements, potential authors should send a large (9 by 12 inch, 30.5 by 22.8 cm), self-addressed envelope, with 28 cents US postage affixed, to BYTE Author's Guide, 70 Main St, Peterborough NH 03458.

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Software Privateers

Personal computing today is confronted with one problem: software. Individual users can, with a few trivial commands, copy and give away any large, complex program. The result is a tremendous economic "disincentive" to the potential creators of great software. No one would spend years of his life creating an algorithmic masterpiece, only to see it stolen upon release.

The solution to this problem is not unenforceable threats to prosecute thieves; one can go to any computer-club meeting and see how seriously those threats are taken, as users swap disks with abandon.

Some manufacturers are trying another approach. They are making their machines hard to program, so that users must buy plug-in software that cannot be copied. This attempt to establish a monopoly, however, tends to fail: few people write programs for such machines, so they are unattractive to users, they do not sell well, and eventually they drop out of sight. By cutting themselves off from the vast, invisible army of user-programmers, makers of these machines cut their own throats.

I have a modest suggestion that may help solve this problem of software, economics, and theft. A producer of significant software must have the assurance that his creation, when sold to one user, cannot be given to another user to run for less than the original purchase price. There must be something unique (or at least distinctive) about the legitimate buyer's central-processing unit, so that his copy of the program can recognize its owner's computer, and work for it, but not for the thief's machine. (The program should be something like the giant's purse in "Jack and the Beanstalk," which cried out when stolen.)

I suggest that microprocessor manufacturers design into their processors a new command, IDENTIFY. When executed, the ID instruction would put some identifying number into one or several machine registers or memory locations.

After that, everything is up to the software producer. He must take the identifying number, manipulate it, move it around the programmable memory space, and otherwise so embed it in his program that any attempt to remove it will cost far more labor than the price of the program. When a user orders the program, he specifies his central-processor identifying number, and receives a personalized copy of the software. The backup copies that he makes will all run perfectly for him, as will the original program. They just won't work on a machine with a different identity.

Trustworthy, bonded distributors of the software, such as retail computer stores, can be given instructions (in the form of master programs) as to how to create personalized copies for purchasers. No radical changes in the software distribution system that currently exists would be necessary.

Even if microprocessors only give distinctive and not unique identifying numbers perhaps only 8 bits long, this system for discouraging software theft could still work well. If there is only one

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In late 1978, Intertec conceived the idea of the InterTube Video Display Terminal. Since that time, we've greatly enhanced its operation with the addition of many new exciting features. But perhaps the most significant announcement in the InterTube line of video terminals is our new InterTube III.

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InterTube III also boasts newly designed processor, video and power supply circuits. All in all, the InterTube III is what we believe to be the most powerful, reliable video terminal available today. And it costs less than its predecessor - our popular InterTube II.

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If you're an existing InterTube user, you no doubt have discovered the exceptional value the InterTube really is. And, if you're not, why not call or write us today for the name and address of your nearest InterTube III dealer. Intertec video terminals are distributed worldwide and may be available in your area now.

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chance in 256 that a bootleg copy will run, a lot less copying will occur. Producers of large programs can charge less for their software and still get a good return on their investments; lower prices for good software, in turn, will further reduce the pressure to steal it, etc.

The hardware/software combination approach to protecting programmers' property rights is simple and has many advantages. It can protect work done in high-level languages as well as machine-language products. It encourages users to develop and distribute their own programs. Most importantly, it works with economic forces instead of against them, unlike other antitheft techniques. A relatively free market in computers has led to the miracle of constantly cheaper and more powerful machines for the past few decades. If software can fit into the same market system, I foresee an explosion in the release of creative human energy in that field too.

Mark Zimmermann
9410 Woodland Dr
Silver Spring MD 20910

While attempts to eliminate software piracy are commendable, they very often fail because of the cleverness of personal-computer users; many take the anticopy measures as a challenge. The problem lies in making the protection scheme easy enough to be affordable, but complex enough to work.

*Serial number protection is easy to defeat, since all the program is looking for is a number. A program similar to an interpreter can be written that supplies numbers sequentially, when the protect code is requested. Who cares if the computer must iterate through 256 or more combinations until it finds the key?...*CPF

Saving Fingers

I was interested to read Rod Hallen's article "My TRS-80 Talks to My Cromemco Z2," June 1980 BYTE, page 88. My organization markets engineering design packages, mainly for structural engineering, which have been developed on large minicomputers and mainframes in BASIC and FORTRAN. We convert these into CP/M-compatible languages and distribute them on ALTOS, Cromemco, and similar computers.

We recently faced the grim prospect of having to hand-key 3500 lines of very complex FORTRAN IV program code for STRESS, a frame analysis program, but, on giving the matter careful thought, we organized the direct transfer of source code files from a large minicomputer into CP/M disk files using the PIP facility.

The steps we took were as follows:

1. Load ASCII (American Standard Code for Information Interchange) source file tape on a Varian V77 operating under MP3.
2. Using the ALTOS in stand-alone mode, we loaded PIP, the CP/M transfer utility program. The command CON: = <filename.FOR> was entered. In this case, if the source tape had a set parity bit then the PIP command could have been extended to strip it off.
3. The video terminal cable to the ALTOS was disconnected.
4. A video terminal cable with the RS-232 pins 2 and 3 (TX,RX) reversed was connected between the Varian terminal-controller outlet and the ALTOS terminal connection. A patch box came in very handy here to check pin status.
5. The Varian was then given a command to read a named ASCII source file from tape and display it on the terminal selected for the transfer.
6. The data was then read into the ALTOS memory, 64 K bytes in this case.
7. On completion of the data transfer, the Varian terminal cable connection at the ALTOS was replaced with its own video terminal cable.
8. Control Z was entered on the ALTOS video terminal which caused the transfer of data from the ALTOS memory to the disk file named in the PIP command.

We repeated this activity until all the programs and libraries were transferred. The whole activity took about 1 hour. This compares very favorably with our estimate of at least 120 hours and indeterminate debugging of entry errors.

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Blaise Trees

The article "Understanding ISAM," by Reginald Gates (June 1980 BYTE, page 108) was interesting and informative. Unfortunately, the article does not mention alternative ISAM organizations based upon B-trees. Such ISAM files do not suffer from disadvantages of reorganization as described in the article. An article in the *ACM Computer Surveys* (June 1979) describes the principles involved in the operation of B-tree files. One important property of these file structures is that reorganization is done as the file is created and changed.

There are several successful implementations of ISAM files using these structures. We have implemented a UCSD Pascal Unit for ISAM using a modified B-tree approach on file organization and maintenance. An index to a file is treated as another indexed file, so the system can handle any level of indexing and any size file. A primary key can be made up of several parts of the record, and secondary keys can also be defined on the record.

There are many extra features not normally available to ISAM users that increase our implementation's utility. Some of these are: an empty file does not need special handling, there is a read forward *and* a read reverse, there is an efficient block delete, there are various options on backup for the prime blocks and index blocks, and there are several utilities available for reorganization, creation, statistics, and recovery. The file scheme works equally well without an index and can be used for small tables.

The unit is being packaged and sold by ERA Computers, POB 500, Fyshwick, Canberra, 2609, Australia; further information can be obtained from them. ERA is also marketing another of our packages which enables FORMS for screen and printers to be easily created and manipulated. This also runs as a Unit in UCSD Pascal. It is a considerable advance on other known FORMS packages.

K Cox and Trevor Lawrence
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Prime Performance

As a TRS-80 owner, I read with some amazement the results of a performance evaluation submitted by Charles H Porter and highlighted in the Technical Forum, on page 216 of the July 1980 BYTE. (See "TRS-80 Performance, Evaluation by Program Timing," March 1980 BYTE, page 84 and "Some More on Performance Evaluation," by Carl Helmers, respectively.) Inspecting Mr Porter's program revealed the algorithm to be the Sieve of Eratosthenes, and as written, won't work! Line 110 should read:

```
110 IF A(X)=0 THEN 100 ELSE 90
```

One can also eliminate line 50 and change line 60 to read:

```
60 DIM A(L)
```

Also, consider the following: In the process of DIMensioning an integer array, Level II BASIC initializes the elements to 0. Why bother to reinitialize them to 1 only to later set them back to 0 to flag that the element's subscript is *not* prime? Instead, eliminate the array "initialization" in line 70 and set the *nonprime* elements to 1. The result will be that all *prime* subscripts are represented by element values of 0. (Negative logic is often more appropriate or efficient, as in this case.) Eliminating the initialization loop from the program cuts another 55 seconds off the already impressive 6 minute 12 second execution time.

I also take issue with Mr Porter's use of Level II error trapping to implement the algorithm. A simple test of the value of X*2 exceeding the array limit would have sufficed as well as made the program more readily understandable.

The following version of Mr Porter's program will thus execute faster as well as include the "missing" prime not displayed in the original. Non-DISK BASIC users should eliminate lines 20 and 70.

```
10 DEFINT A-Z
20 S$=RIGHT$(TIME$,8)
30 L=10000 : X=2
40 DIM A(L)
50 FOR I=2*X TO L STEP X : A(I)=1 :
   NEXT
60 X=X+1 : IF 2*X<=L THEN IF
   A(X)=1      THEN 60 ELSE 50
70 PRINT "START ";S$ : PRINT "STOP ";
   RIGHT$(TIME$,8)
75 INPUT "DISPLAY PRIME NUMBERS";X$
   : IF LEFT$(X$,1)<>"Y" THEN END
80 FOR I=1 TO L : IF A(I)=0 THEN
   PRINT I,
90 NEXT
99 END
```

Les Parent
35 Barnesdale Rd
Natick MA 01760

Treasure-80

Different strokes for different folks. Here is one TRS-80 customer that thinks the Tandy Corporation does just fine in the software department. The TRS-80 is not just another CP/M machine, thank goodness. For my money, TRSDOS is a slicker, easier to use, and more modern operating system. And NEWDOS, the highly touted modified version of TRSDOS, is mainly notable for its incompatibility. If it weren't for NEWDOS, users wouldn't need SUPERZAP to apply all those machine-language patches to get their software to run. I haven't seen a word-processing package that can touch SCRIPSIT. I spent good money for the Microsoft macroassembler, then went back to using EDTASM. The list goes on.

Personal-computer magazines need to look at the TRS-80 in a new light, and view it as an entity unto itself, not an aberration to be forced into the familiar CP/M mold. CP/M may be familiar to some, but TRSDOS is familiar to me,

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and the CP/M-based software I have seen thus far is clumsy and old-fashioned by comparison to the newer products. CP/M is touted as "the software bus." Let us take note of the obsolescence of the S-100 bus standard. It will soon be replaced by a new standard. Is not CP/M in the same position?

Many years ago, IBM's customer base insisted that IBM retain its old familiar operating systems. Those customers today suffer from obsolete, clumsy, inefficient, and troublesome software that is truly laughable by today's standards. There is a lesson here for the microcomputer world. Nostalgia is a luxury we cannot afford.

John R Culleton Jr
Culleton Group
2401 Haight Ave
Sykesville MD 21784

Superb Brain

For any BYTE readers who may have had problems with the Intertec Superbrain operating systems, I would like to recommend the services of Information Engineering, POB 198, 8 Bay Rd, Newmarket NH 03857, (603) 659-5891.

I am a writer who bought a Superbrain for use with Micropro's Word Star software as a word-processing system. A bug was present from the beginning. After saving a file and calling it back for editing, I was always confronted by several lines of garbled text (usually about 28 lines into the file). I had difficulty meeting deadlines because overcoming the bug, which happened in every file, proved time-consuming. I thought that the fault lay with Word Star, but Word Star proved blameless. Both my software and hardware vendors tried to help, but neither succeeded.

Intertec listened to my description of the problem and offered two suggestions. The first: that I should have my local dealer replace the EPROM (erasable programmable read-only memory) that came in my Superbrain. The Intertec representative suggested that \$125 would be a reasonable fee for this replacement. The second suggestion: that I should have a \$1500 hardware "upgrade." When I asked my local dealer, he knew nothing about the replacement EPROM. He said calls to Intertec provided no clarification. As for spending \$1500 to "upgrade" a two-month-old computer that never worked correctly, I considered that suggestion tantamount to an admission that something was wrong with the computer as originally sold.

My hardware vendor heard about Information Engineering and gave me the telephone number. I called, and Mark Klein answered. He asked me a few questions that indicated familiarity with the kind of problem I was having. He took down the serial number of my Superbrain and my phone number. Later he called and said that he could definitely fix the problem. Information Engineering made and sent me an EPROM to replace the one supplied by Intertec. Together with an operating-system patch supplied by Information Engineering on disk, the Information Engineering EPROM fixed the Superbrain at once. Not only did Word Star and CBASIC run perfectly, but the disk drives operated much more quickly and quietly.

I have written this letter because I would like other Superbrain owners to know that they can get help from Information Engineering if they experience problems like the one that I did.

Philip Lemmons
201 E 36th St
New York NY 10016

I talked with Mark Klein of Information Engineering, and learned that the problems encountered by Superbrain users were frequently due to software. In most cases, a new EPROM (erasable programmable read-only memory) and a patch to the CP/M BIOS (the input/output handler for CP/M) cures the problem. According to a flyer put out by Information Engineering, the cost of the fix is \$150, and the following advantages are gained:

- *improved disk handling;*
- *use of all available space on disk;*
- *ability to run programs larger than 30 K bytes;*
- *keyboard type-ahead;*
- *ADM-3A cursor- and screen-control codes available; and*
- *serial number keyed to machine serial number. . .* **.CPF**

A SwTPC 6800 User Needs Help

I own a Southwest Technical Products (SwTPC) 6800 development system, with which I need to program some PROMs (programmable read-only memories). I have not been able to successfully load my memory-resident PROM-programming code using my cassette interface. Can a reader of BYTE send me a listing of this PROM-programming program, so that I can compare it against the code in my system's memory? Thanks.

Bob Abbott
3333 Toledo Ave
Lubbock TX 79412

Letters continued on page 294

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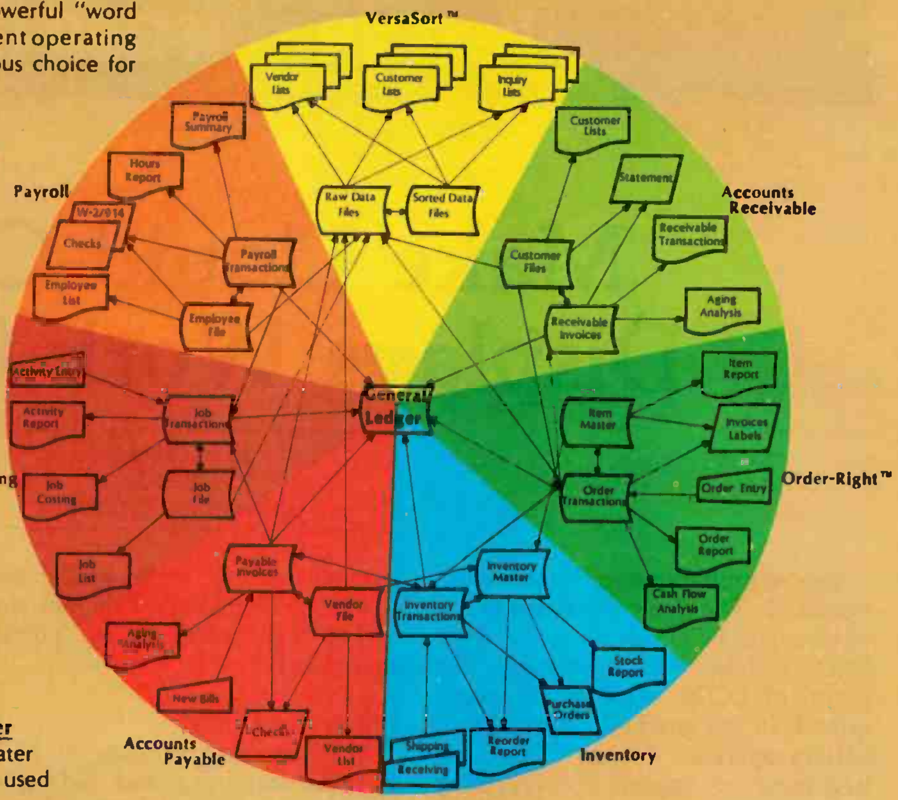

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Make Liquid-Crystal Displays Work for You

Steve Ciarcia
POB 582
Glastonbury CT 06033

You've probably seen the abbreviation LCD. The chances are that many of you own LCD calculators or wear LCD watches. Liquid-crystal displays, or LCDs, are enjoying rapid growth in key markets, especially in battery-operated devices. They are beginning to appear in everything from computer games to handheld terminals.

Rather than emitting light, as in the case of LEDs (light-emitting diodes), LCDs are light *reflectors*. They are primarily used in high-ambient-light situations and require external "backlighting" for low-ambient-light use. Since they are non-illuminating, they consume very little power and can be driven directly from CMOS (complementary metal-oxide semiconductor) circuitry. This fact alone makes them valuable for portable equipment.

What Are LCDs?

They are two families of LCDs: *dynamic-scattering* and *field-effect*. *Dynamic-scattering* devices harness the intermolecular turbulence created when a current flows through liquid-crystal material. This turbulence produces a frosty characteristic on a clear or reflective background. Dynamic-scattering LCDs were the first type of LCDs to be developed, and they have some built-in problems.

Besides having a high threshold voltage (12 V to 15 V), there is a "Catch 22" associated with their operating principle. Small impurities are added to facilitate current flow. These impurities, which are susceptible to humidity, oxygen, and the ultraviolet component of sunlight, break down. As they break down, current flow increases, causing further contamination. These early displays lasted only about a year in normal operation. They are not widely used anymore.

Second-generation LCDs utilize *field-effect* technology. In contrast to the current-operated dynamic-scattering devices, field-effect LCDs are voltage-operated.

The liquid-crystal material is an organic compound with *nematic* properties. The long axes of the molecules are parallel but are not arranged in distinct layers. Within specific temperature ranges they exhibit properties of both liquid and solid states. The long and cylindrical molecules, when brought in contact with a treated glass surface, align themselves along a specific axis to form a polarizing filter.

There are three types of LCDs: *reflective*, *transmissive*, and *transflective*. The *reflective* LCD consists of a vertical polarizer, the liquid-crystal material, a horizontal polarizer, a reflector, and indium-oxide electrodes all mounted in a glass sandwich (see figure 1). The vertical polarizer, which works like a Polaroid sunglass lens, permits light only with a particular orientation to pass through.

When the display is unenergized, this light passes through the liquid-crystal material and is twisted 90°

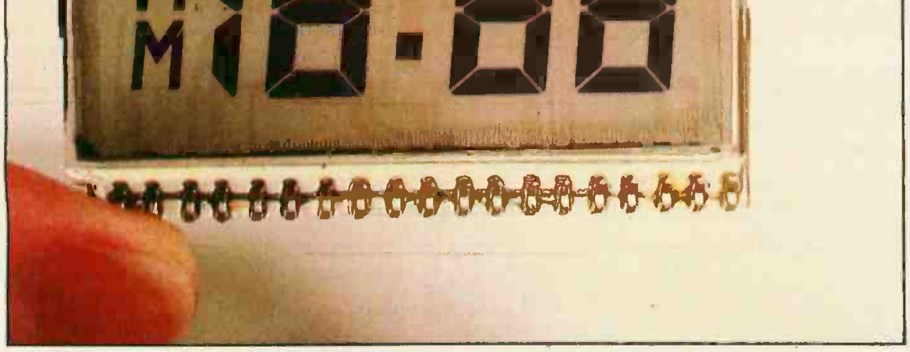

Photo 1: *Standard three-and-a-half-digit clock/multimeter display. The unit shown is* transmissive *and has no rear reflector. All segments are energized in this photo.*

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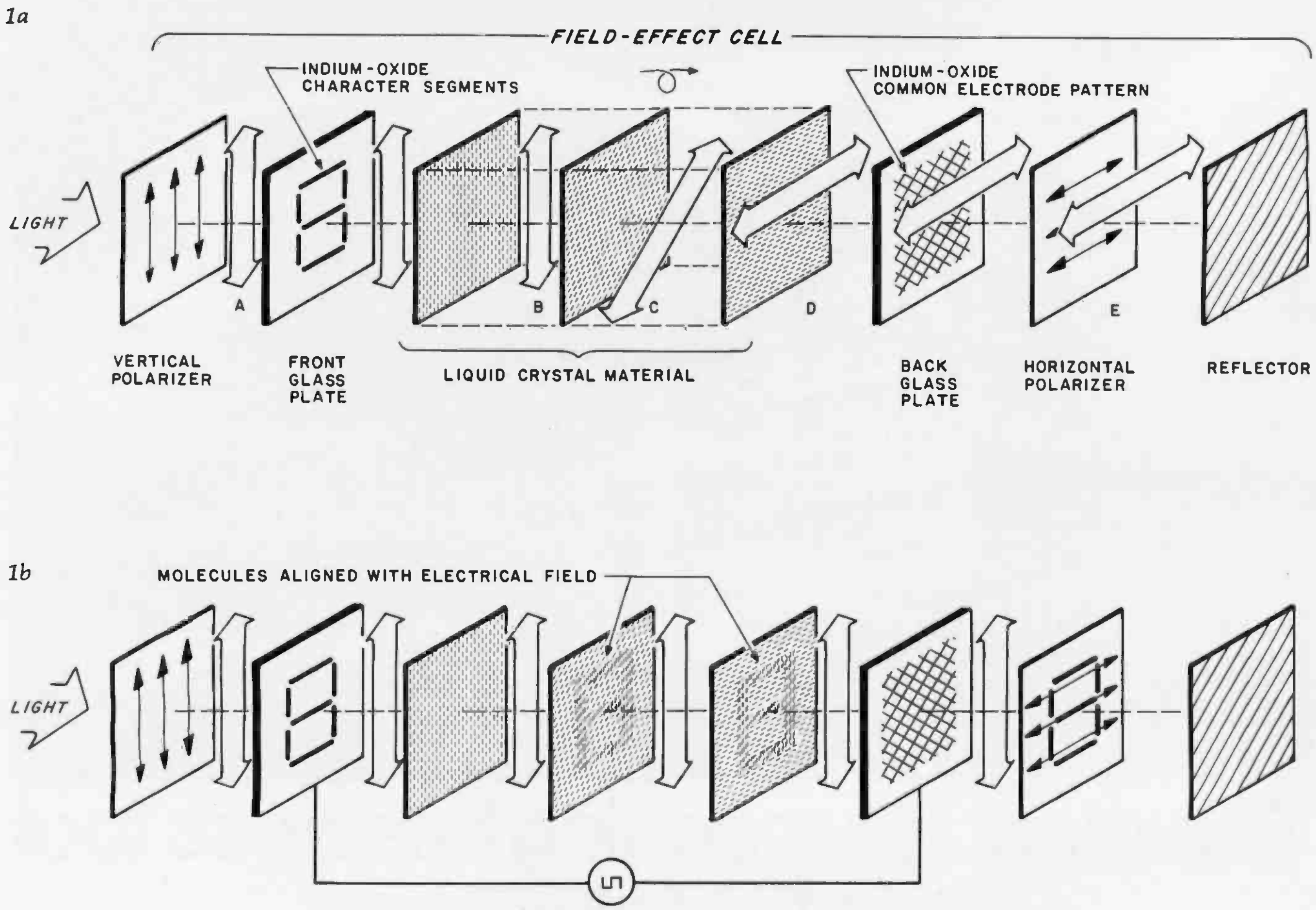

Figure 1: *Block diagram of a field-effect liquid crystal. Field-effect liquid crystals are voltage-operated.*

In the unenergized case (figure 1a), light enters a vertical polarizer at the front, and proceeds through the front glass plate containing indium-oxide electrodes, in the shape of a seven-segment display in this case. (Note: The electrodes are shown darkened in this illustration for clarity. In actual operation, they are transparent.) The light is then twisted 90° through the liquid-crystal material, proceeds through the horizontal polarizer, and is reflected back through the entire assembly. The viewer sees a blank display.

In the energized case (figure 1b), the indium-oxide electrodes are activated and the corresponding portions of the liquid crystal align themselves with the electrical field. Thus, they no longer twist the light going through them by 90°. Light passing through these segments cannot pass through the horizontal polarizer, and these portions look dark to the viewer.

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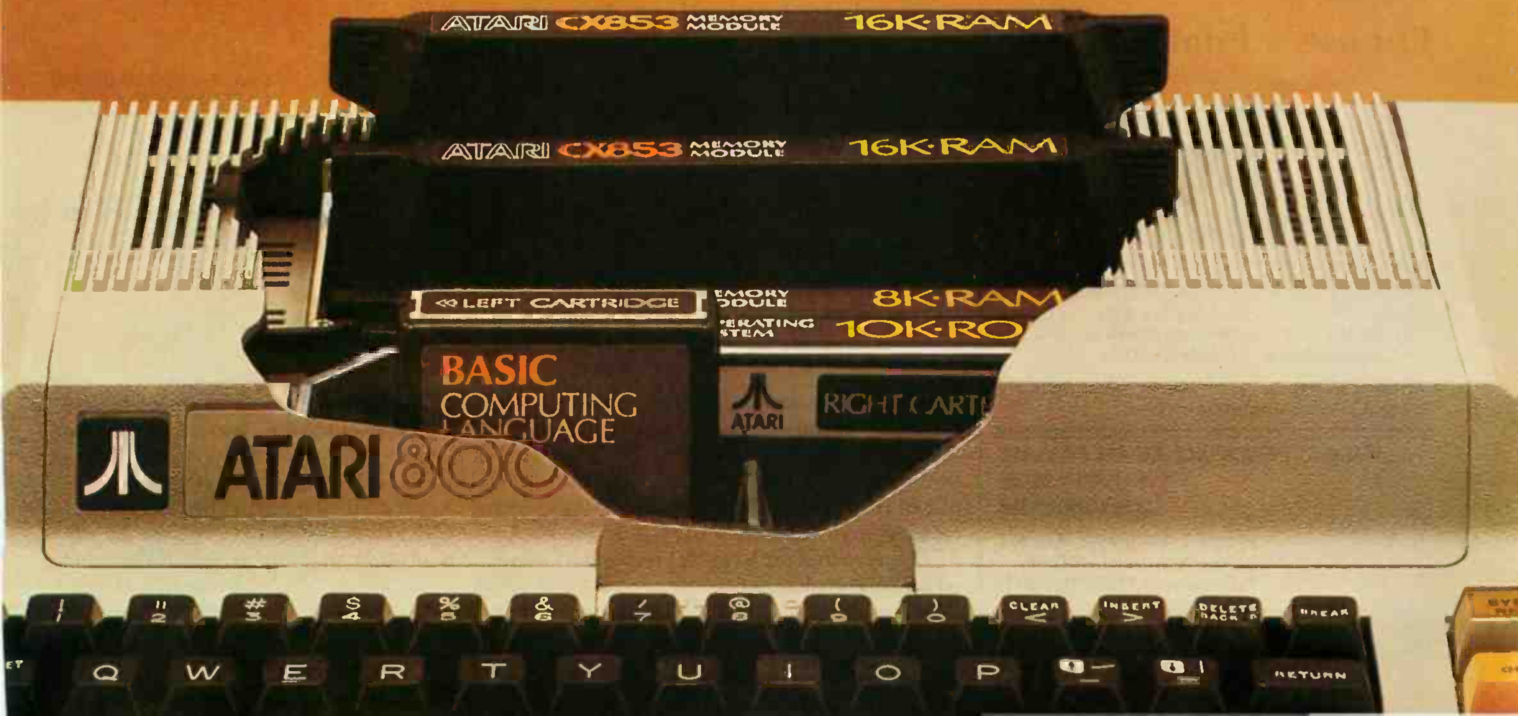


with respect to the vertical polarizer. Shifted in this way, the light passes through the horizontal polarizer, which has a similar polar orientation. The result is that light passes freely through the cell and the LCD appears transparent.

When the display is energized, the molecules in the liquid-crystal material align themselves with the electrical field, and polar rotation no longer occurs in the region of the character-pattern elements. The vertically-polarized light conforming to the image produced by these elements cannot pass through the horizontal polarizer, and is absorbed by it instead. The energized display elements therefore appear as black images against a light-colored background. The reflector is placed behind the display to take advantage of ambient light and reflect the pattern image back to the viewer.

The *transmissive* LCD has no reflector and appears as plain glass when unenergized. Both reflective and transmissive LCDs are shown in photo 2. To view the characters on this unit properly, a light source must be placed behind the display. A *transflective* LCD combines the properties of both. It has a reflector for daylight operation, but the reflector is thin enough to allow back lighting in the dark. An example is an LCD display in a wristwatch.

Using LCDs

Basically, LCDs are low-voltage AC (alternating current) devices. They typically operate within the range of 3 to 12 V RMS (root mean square). (Some circuits run on 1.5 V

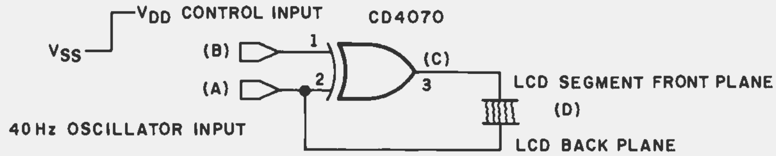


Figure 2: *Liquid-crystal driver technique. LCDs are driven using symmetrical square waves with less than 50 mV DC offset. The low-offset AC drive is obtained in all LCD drivers by the use of exclusive-OR outputs. The configuration shown will result in a low-DC-offset AC drive with 2 × V_{DD} peak value, or an RMS value of V_{DD} for the LCD.*

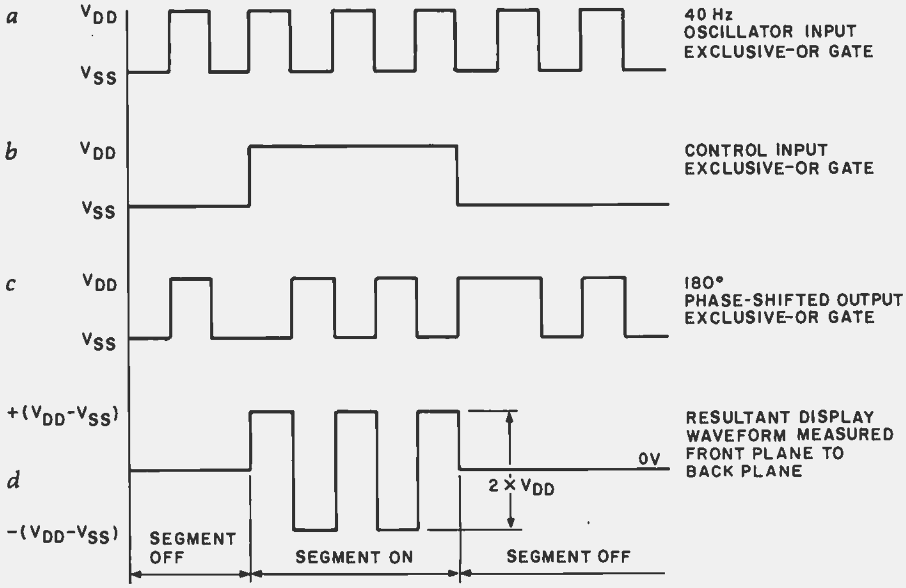
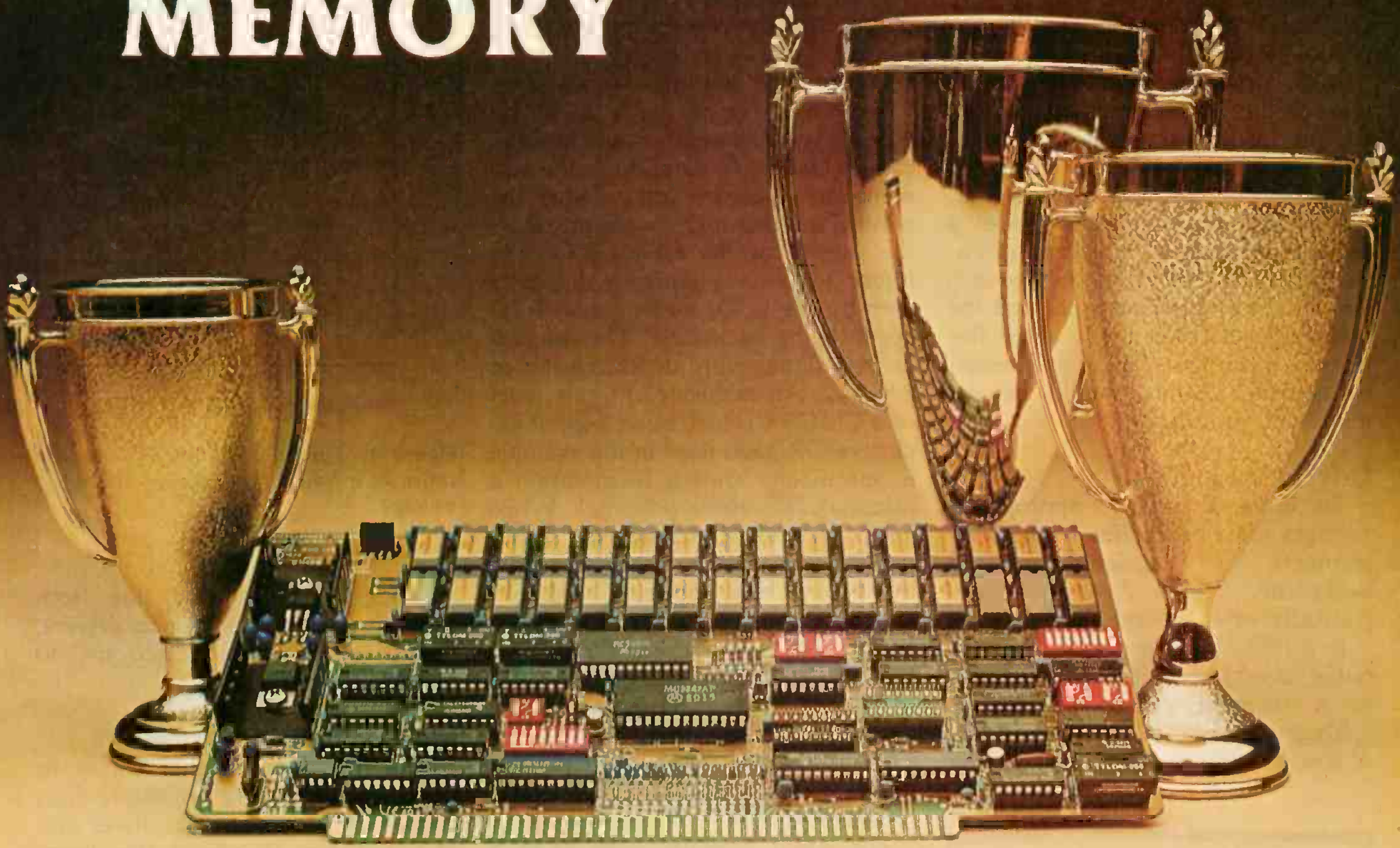


Figure 3: *Waveforms occurring during typical LCD operation. To drive an LCD, appropriate voltages must be applied to the "on" segments, the "off" segments, and the backplane. Here an exclusive-OR logic gate is used to drive one of the segment electrodes, as shown in figure 2. Waveform (a) is a 40 Hz 50%-duty-cycle square-wave input to the exclusive-OR gate. (b) is the segment on/off control input. When the control input is high, (c) is the output of the exclusive-OR; (d) is the waveform seen by the LCD, measured with respect to the backplane. It is an AC signal with a peak RMS value equal to 2 × V_{DD}.*

THE UNBEATABLE S-100 MEMORY



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but incorporate a voltage doubler or tripler for the display.) Higher peak voltages are allowed, but it is the RMS value that is important. The DC (direct current) offset potential of the drive signal must be less than 50 mV; DC tends to degrade the liquid-crystal material.

Also, since the device consists of two conductors separated by a *dielectric* (ie: insulating material), it functions electrically like a capacitor. The frequency of the AC drive signal, while not critical, does have a preferable range. A property of capacitors is that the higher the frequency, the lower the reactance, and the greater the current drain. If the frequency is too low, flicker will result. In general, 25 Hz should be the minimum frequency.

Driving the LCD

To drive a display, appropriate voltages must be applied to the "on" segments, "off" segments, and the backplane. Figure 2 shows schematically what this entails.

In a typical driver circuit, the output of an exclusive-OR logic gate goes to a segment electrode. This is analogous to one of the seven inputs of a seven-segment LED display. The

	Function	Pin Number
	a1	37
	b1	38
	c1	39
digit 1	d1	40
	e1	2
	f1	4
	g1	3
	a2	6
	b2	7
	c2	8
digit 2	d2	9
	e2	10
	f2	12
	g2	11
	a3	13
	b3	14
	c3	15
digit 3	d3	16
	e3	17
	f3	19
	g3	18
	a4	20
	b4	21
	c4	22
digit 4	d4	23
	e4	24
	f4	26
	g4	25

Table 1: *Pin functions of the Siliconix DF411 four-digit LCD driver used in figure 6.*

oscillator input, which also cycles the exclusive-OR gate, is connected to the LCD backplane terminal. This connection is roughly equivalent to the common cathode on an LED display. To turn the segment on, simply apply a logic 1 to the control input (pin 1); to turn it off, apply a logic 0.

Figure 3 illustrates the resultant waveforms. Figure 3a is a 40 Hz 50%-duty-cycle square-wave input to the exclusive-OR gate; 3b is the segment on/off control input. When the control input is high, waveform 3c is the output of the exclusive-OR. In figure 3d, the waveform is shown as seen by the LCD, measured with respect to the backplane. The result is an AC signal with an RMS peak of 2× V_{DD}. An exclusive-OR gate (part of a CMOS CD4070 quad 2-input exclusive-OR gate) used in the example is specifically chosen to maintain a minimal DC offset potential. While TTL (transistor-transistor logic) devices will work in theory, the 200 mV typical offset potential will considerably shorten the life of the LCD and should not be used. To connect LCDs to TTL, the preferred method is to use a CMOS BCD (binary-coded decimal) latch/decoder/ LCD-driver such as the MC14543. A schematic diagram of a typical circuit is shown in figure 5.

For larger displays, such as in a four-digit multimeter, we could add three more MC14543s or use a single Siliconix DF411 four-digit LCD driver. (Figure 6 demonstrates this application.) Rather than four separate BCD inputs, totaling sixteen lines, the DF411 relies on a multiplexed data input. Each digit is sequentially loaded by setting the 4-bit BCD code lines on B0 thru B3 and

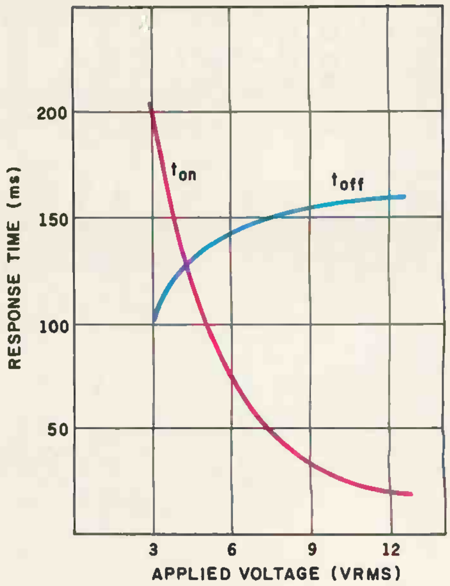

Figure 4: *Typical LCD on/off response times as a function of applied AC input voltage.*

strobing the proper digit line. Both examples utilize static display drivers. This is the least complicated method to use.

Multiplexed LCD Displays

The first thought that comes to mind when using multiple-digit displays is to use a single driver unit and multiplex it among the digits. This is the classic method used in LED displays. With LCDs, however, there are some extra considerations.

Of the two basic types of LCDs, the

Number	Type	+5 V	GND
IC1	MC14543	16	8
IC2	CD4047	14	7

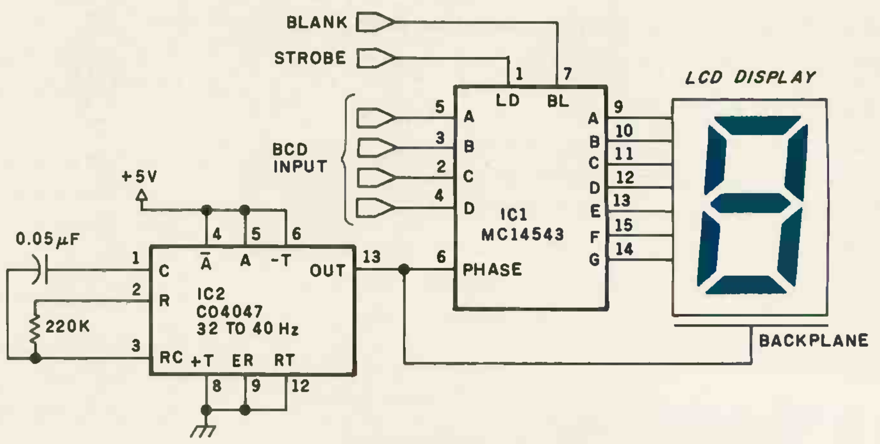

Figure 5: *A single-digit, seven-segment LCD driver circuit.*

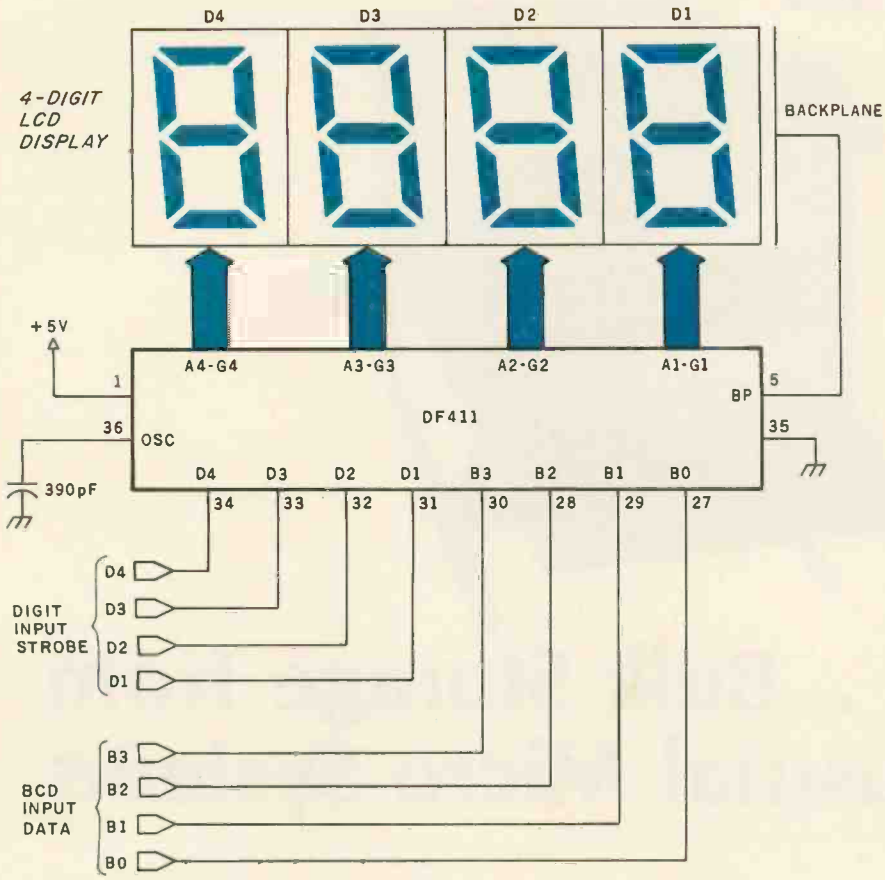

Figure 6: *A four-digit LCD driver circuit, the DF411, made by Siliconix, Inc, 2201G Laurelwood Rd, Santa Clara CA 95054.*

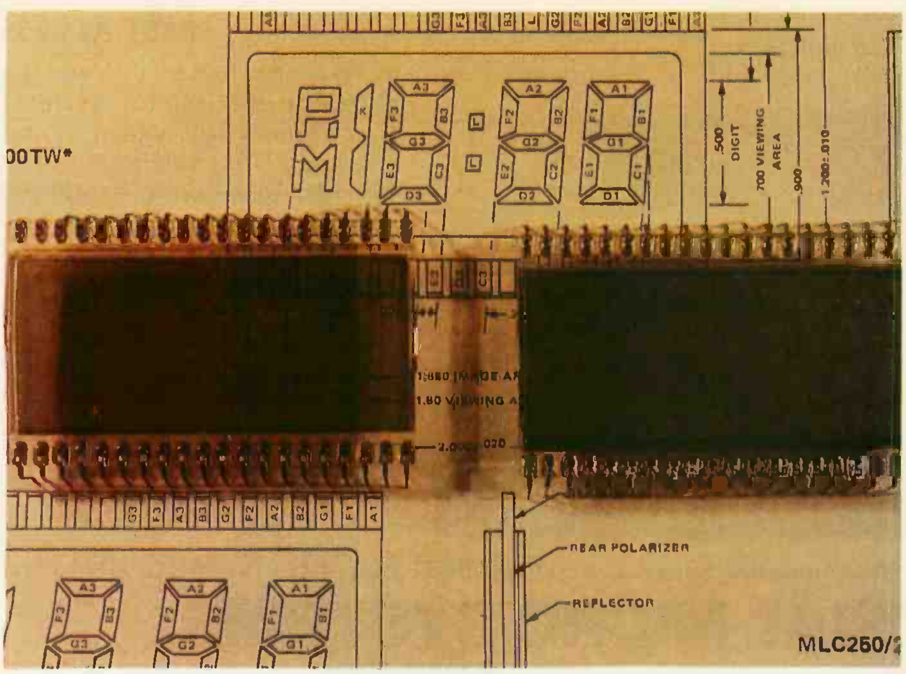

Photo 2: *Comparison of two types of LCDs. At left is a transmissive display; at right is a reflective display. Both units are unenergized in the photo.*

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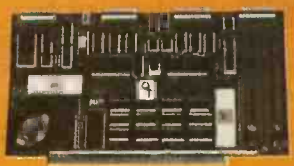

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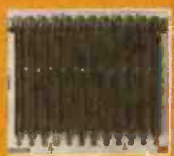

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excitation and threshold voltages of the field-effect device are lower and more suitable for multiplexing. The threshold voltage is defined as the level at which the segment switches from "off" to "on." In a multiplexed driver arrangement, the effective threshold voltage varies as a function of the duty cycle. In effect, as the number of multiplexed digits increases (while the duty cycle decreases), the power-supply voltage must increase.

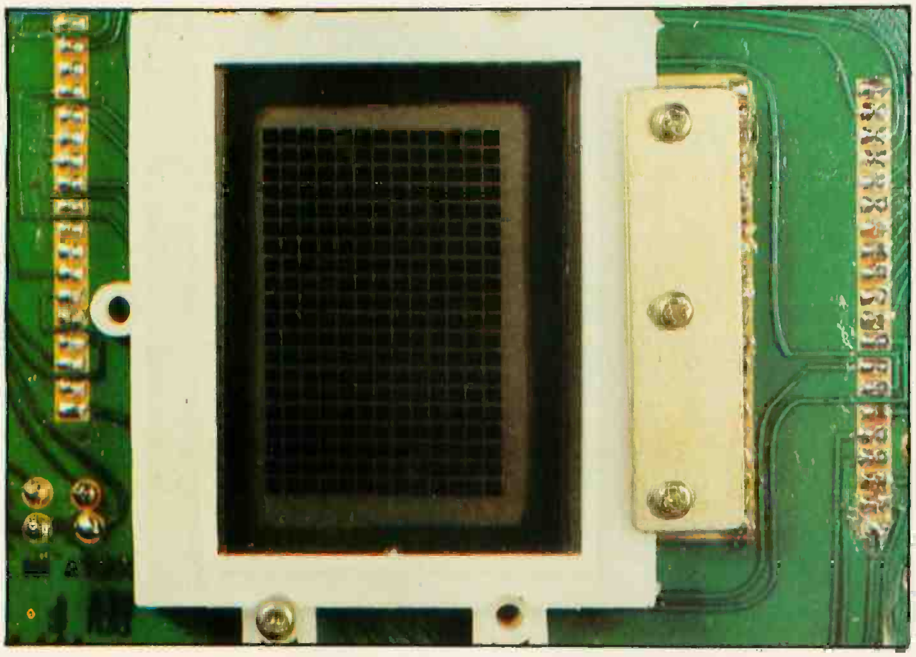

Photo 3: *A 14-by-20 LCD dot-matrix display taken from a Mego Mini-Vid space-war game. The unit is shown with all dots turned on.*

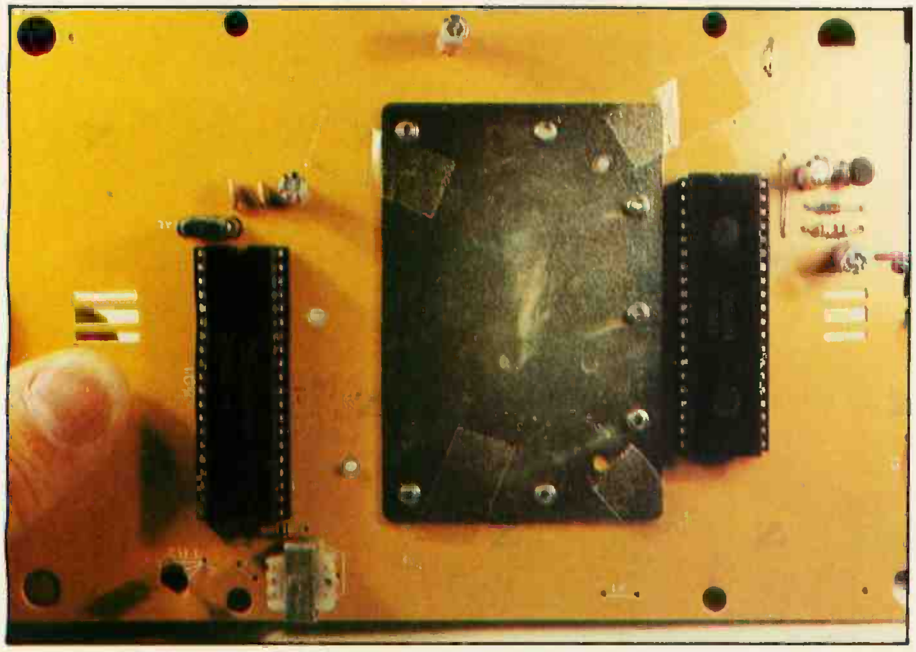

Photo 4: *Rear of the printed-circuit board used in the Mego Mini-Vid game, revealing the location of the liquid crystal display shown in photo 3. The complete electronic circuitry for the game is visible. The integrated circuit on the left is an Intel/NEC 8048 8-bit microcomputer. At the right is a custom LCD dot-matrix driver component. The three sets of discrete components (clockwise from top right) are a voltage regulator, an audio amplifier, and a 6 MHz clock circuit. I bought the game on sale for $24.95.*

To overcome this difficulty while still reducing the number of connections and drivers, several special techniques are used. The most common is called the voltage-select or "V/3" method which operates the nonselected display-pattern segments just below the threshold voltage and the selected segments just above it. Most eight-digit liquid-crystal calculator displays use this scheme.

A common misconception is that relatively slow LCD response times preclude conventional multiplexing approaches (see figure 4). This is because an LCD is essentially a capacitor that can be "charged" (turned on) by a series of pulses over a period of time (presuming constant data input during this time).

The integration of the pulses is accomplished by the long *time constant* of the LCD itself. (In reading an LED display, the eye performs the integration of the short-duty-cycle images.) It may take a half second for an LCD display to settle out the displayed image. This is not a problem with slowly changing data, such as a clock display. An arrangement like this would be unacceptable for use with data that updates ten times a second, however. Only a static driver could be effective at that rate.

The real problem is not with multidigit displays, but rather with dot-matrix LCD displays like the one shown in photo 3. This particular display is a 14-by-20 dot matrix from a "Mini Vid" space-war game by Mego. I didn't care much for the game, but the display was fun to experiment with and less expensive when salvaged from a toy rather than purchased directly from an LCD manufacturer. The popular MicroVision games from Milton-Bradley use a similar display with a 16-by-16 matrix.

With a matrix-addressed LCD, each segment plus its associated backplane is electrically equivalent to a lossy, nonlinear, voltage-dependent capacitor. In fact, the entire array may be represented schematically as rows and columns interconnected by capacitors at each intersection. A series of "select" pulses drives each row, while a series of data pulses, which are either in phase or out of phase with the select pulses, drives each column.

LCDs have electro-optical char-

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acteristics independent of the direction of the applied voltage. The fact that they have no polarity or diode action presents a fundamental constraint, because "cross talk" would exist between selected and nonselected segments in a conventional multiplexing scheme. The successful use of a dot-matrix LCD results only from a complicated tradeoff between operating voltage, threshold voltage, contrast ratio, viewing angle, and multiplex frequency.

Both Mego and Milton-Bradley use the same custom integrated circuit to drive the dot-matrix display. Already aware of the problems associated with standard drive electronics, I had hoped to adapt one of these games as a computer peripheral for this article. This was easier said than done.

The custom integrated circuit used in the game is a forty-pin CMOS LSI (large-scale integration) component. Thirty-four pins go directly to the matrix, two pins are for the power supply and ground, and four lines are used for control signals from the microprocessor. One seems to be a data strobe, two appear to be row and column incrementers, and one is data. Even though both games use the same controller, the display quality is considerably better on the Milton-Bradley device. This led me to believe that the timing of the signals is as important as knowing which line is which.

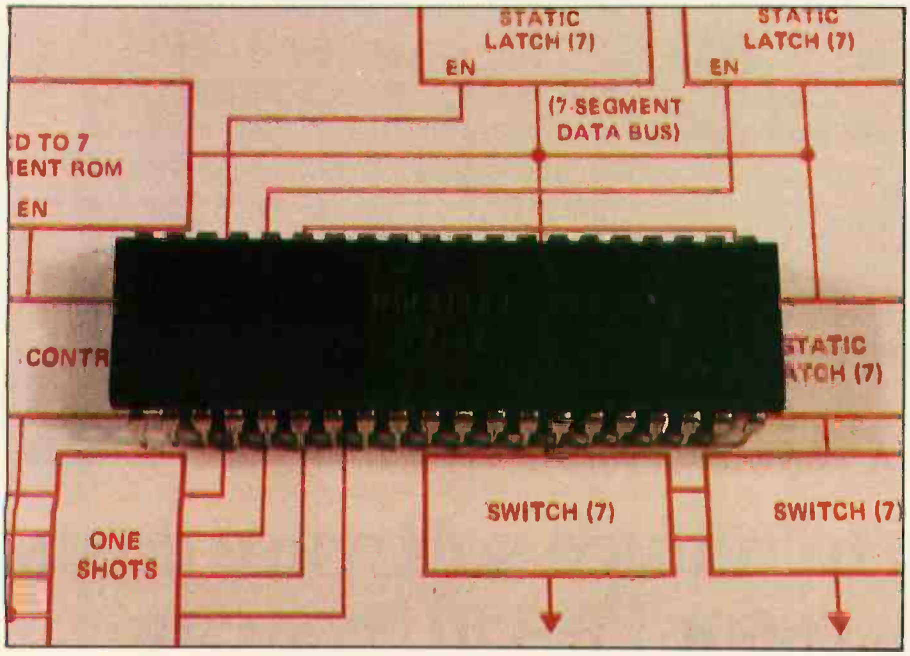

Photo 5: *The Siliconix DF411 four-digit direct-drive LCD driver integrated circuit.*

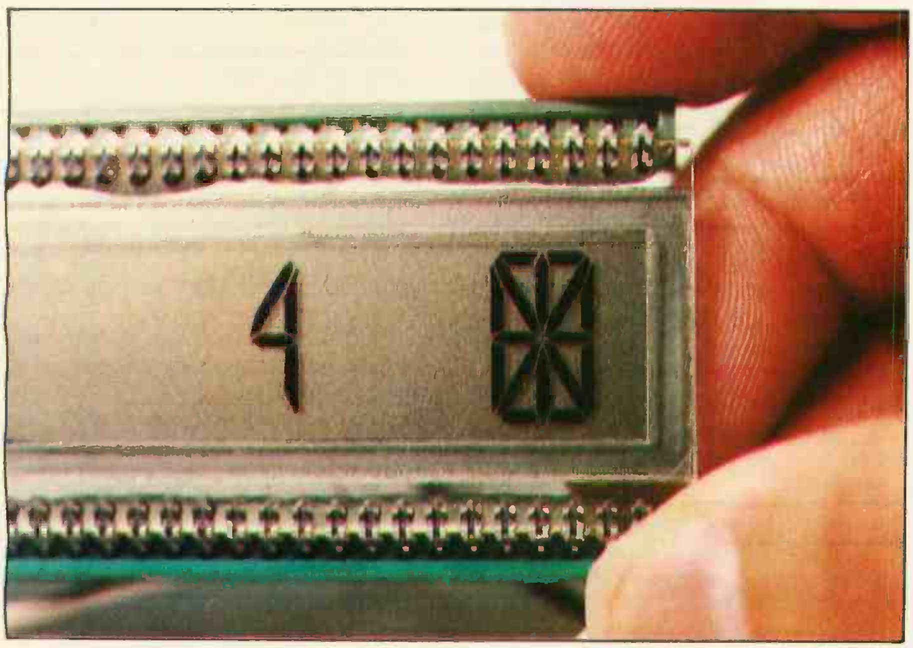

Photo 6: *An LCD designed to display both letters and numerals.*

Rather than writing something which might risk my credibility, I contacted Milton-Bradley and asked for the timing and control sequence of this device. Apparently, because the toy industry is very competitive, they were reluctant to divulge any information. This is quite the opposite from the response I usually get when I contact electronics manufacturers. The only alternative was to persuade the company that made the device to provide more information, or disassemble the game program and see what goes out on these four lines. I decided it wasn't worth it.

General Limitations

LCDs will probably never replace LEDs or gas-discharge displays. More likely they will dominate applications in which power and ambient light are the prime considerations. There are limitations, however.

Field-effect LCDs properly sealed in hermetic packages and employing stable compounds with high initial purity are inherently reliable. Early problems were due to poor sealing techniques and chemical reactions within the liquid-crystal material.

LCD response time, while not a deterrent in multiplexing, is long by normal electronic-component standards. Some users find these response times annoying. As figure 4 shows, the turn-off time can be as much as 200 ms. The effect is that the segment image appears to fade out rather than snap off. Increasing the drive voltage, making the cell thinner, and using less-viscous liquid-crystal materials are ways to increase the speed. I expect reasonable progress, but in my opinion it will be a long time before the microsecond range necessary for flat-screen television will be achieved while keeping the LCDs competitively priced.

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Also, the operating-temperature range, especially at the low end, is not broad enough to serve some key applications, such as automotive use. Present low-temperature limits are around −10° C (18° F), at which point the turn-off time can be as high as one second. Cold does not harm the display, but it does make it temporarily inoperative. This limitation is not easy to overcome because the fundamental properties of the device are involved. An optimum lower limit of −40° C (−40° F) will require major technological breakthroughs.

The Future

LCD technology is advancing at a pace consistent with the rest of the electronics industry. The dot matrix used in some computer games is essentially a first-generation device, complete with all the problems that go with using new devices. Larger matrices, say 256 by 256, will not use 512-pin custom LSI chips. Future devices will depend on a return to simulated static operation such as that used on a single-character display. To attain this sophistication, it will be necessary to etch the drive electronics directly onto the LCD. This is the only way that the thousands of transistors which combine to function as exclusive-ORs and other building blocks can be connected to large matrices. Work in this area has begun, and companies like Kylex in Mountain View, California have already produced forty-character dot-matrix LCDs which are loaded like programmable memory buffers. Perhaps I will use one in a future article.

Even though I've painted a tough picture for LCDs, their price/performance ratios continue to improve, especially in large-character displays. With their high versatility, increasingly competitive cost, low power requirements, and high readability, LCDs will continue to compete head-to-head with LEDs and gas-discharge displays for many general applications. As the drive circuitry becomes less complicated through technological advancements, they will undoubtedly add new dimensions to personal computing.■

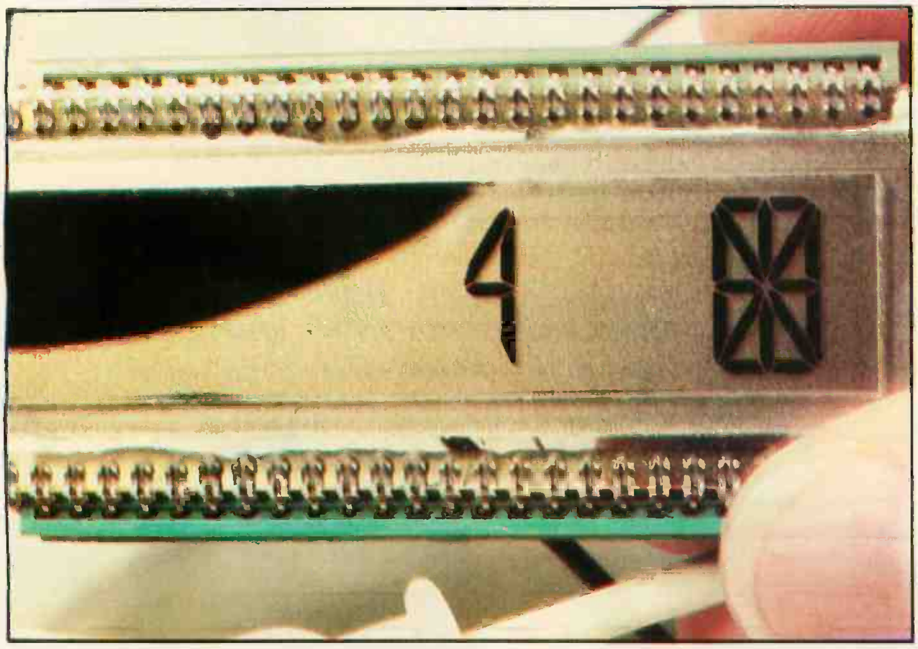

Photo 7: *LCD turning black as a result of the hot lights used to take the picture. LCDs are sensitive to heat, but recover immediately upon cooling.*

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Photo 8: *Typical eight-digit, seven-segment LCD calculator display.*


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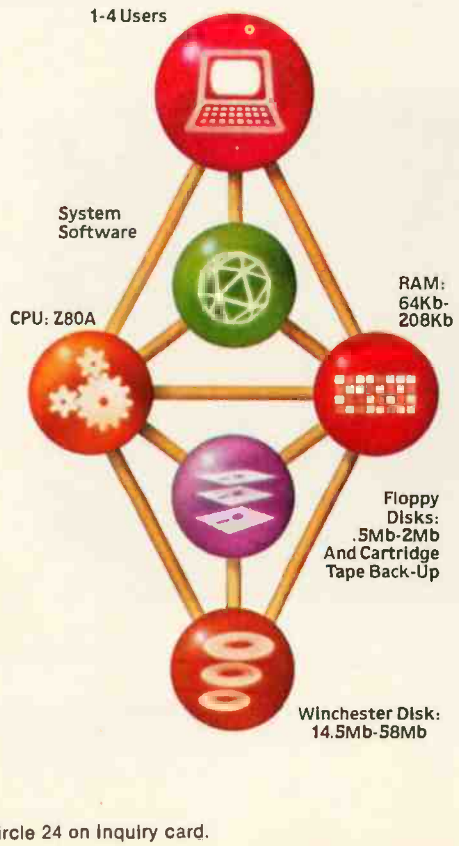

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Product Review

Synertek Systems KTM-2 Terminal-on-a-Board

Phil Nowes, 823 Whitethorne Dr, San Jose CA 95128

The KTM-2 Terminal-on-a-Board developed by Synertek Systems provides a data entry and display system for the serious computer user. Having used both the CT-1024 and CT-64 terminals offered by Southwest Technical Products (SwTPC), I was rather skeptical of the claims made by Synertek Systems for their dual microprocessor terminal, which costs just $349. After using the KTM-2, though, every word Synertek said about it is justified.

The board provides a 24-line by 40-character scrolling display of exceptional quality, and interfaces over one of its two serial input/output (I/O) ports. Not only does the board provide the 128-character ASCII (American Standard Code for Information Interchange) set and some special characters (such as Greek Σ and π), but it also generates 128 graphic characters—a feature not available on some systems that cost twice as much.

But, just what is KTM-2? It's a circuit board that measures 40.6 cm (16 inches) long and 17.1 cm (6.75 inches) wide, with a full 54-key array. It also contains all the circuitry necessary to provide a composite-video output, two serial ports (with switch-selectable data rates from 110 to 9600 bps), and relative and absolute cursor control. The board draws about 1.4 amperes and

Photo 1: *The KTM-2 board. The board contains a 54-key array, with all the circuitry necessary for composite-video output. This 40-character per-line version requires 1.4 A at 5 V. The 80-character version draws 1.6 A. Both are able to provide RS-232-compatible outputs with the addition of extra power supplies.*

operates from a single +5 V power supply.

There is another version, the KTM-2/80, which provides a 24-line by 80-character display for $424. This board draws about 1.6 A and operates at a much higher clock frequency—7.2 MHz versus 3.6 MHz for the KTM-2. Because of the higher clock frequency, a high-quality video monitor must be used with the KTM-2/80, while the KTM-2 could use an ordinary television set with an RF (radio-frequency) video modulator. For our purposes here, all comments will pertain to the KTM-2 system with the 40-character per line capability.

Removing the board from the carton and setting it up are relatively simple procedures—there is very little assembly required. It is only necessary to wire the power supply to the proper connector, connect a video monitor or RF modulator to the composite video output, and set the desired serial port data rate. Because it can operate in *self-check mode* (transmit-data output can be fed back into the receive-data input), the board can be tested immediately to ensure that it is functioning properly, before connecting it to the rest of your computer system.

To operate the board in local mode, the transmit and receive pins of serial port 1 must be connected to each other, then the Clear-to-Send pin of the port must be asserted. Since there is no computer to assert the pin in this mode, the pin must be connected to a voltage source greater than three volts and less than twenty-five volts; this can be done by connecting the pin to the Request-to-Send line, which is always at +5 V. Once these connections are made and power is applied, the terminal is ready for test in a stand-alone mode.

Basic functions of the keyboard are identical to most of the terminals made today—both uppercase and lowercase characters are available, as well as reverse video of the uppercase characters. There is no shift-lock key; however, the board does have a CAPS-lock key that provides only uppercase alphabetical characters plus the normal numbers and symbols available during lowercase operations. Switching between normal and reverse video is accomplished by hitting the escape (ESC) key and entering an uppercase R. To return to normal video from the reverse mode, just press the ESC key and then enter a lowercase r.

As mentioned earlier, graphics characters are available to the user. These are just as accessible as reverse video—just press the ESC key and then enter uppercase G to change into the graphics mode. To exit the graphics mode, just type ESC, g. Reverse video is also available in the graphics mode. Both the alpha mode and the graphics mode can be intermixed on the screen simply by typing the desired sequence of control functions. All of these modes can be computer controlled; all the computer has to do is send out the same sequence of ASCII codes on the serial port.

I mentioned earlier that the KTM-2 has two serial ports, these are labeled 1 and 2. Port 1 is the main port and is used primarily with a computer for information transfer. The other port acts as an auxiliary port, primarily for a printer, so that hard copy can easily be obtained without using one of the other computer ports.

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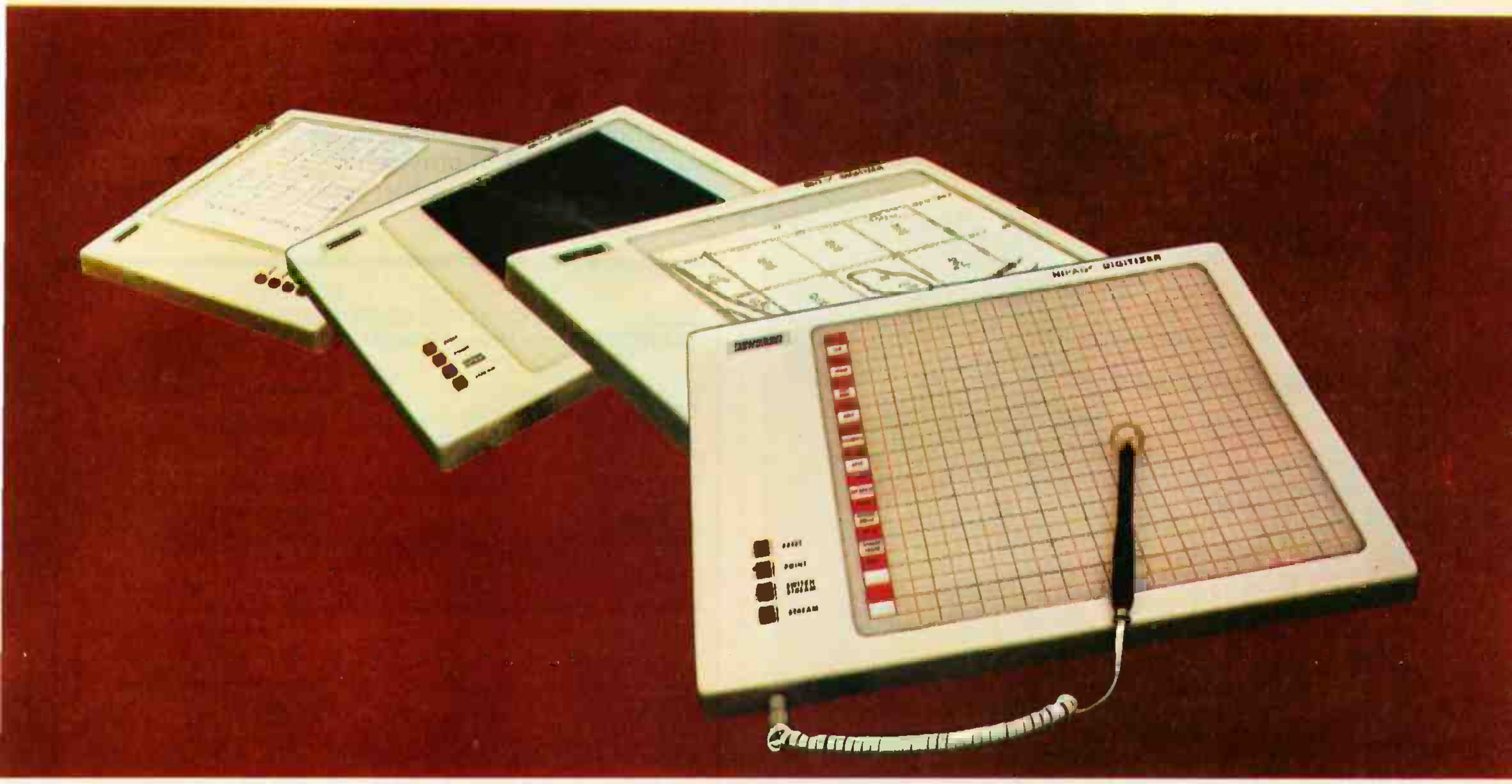

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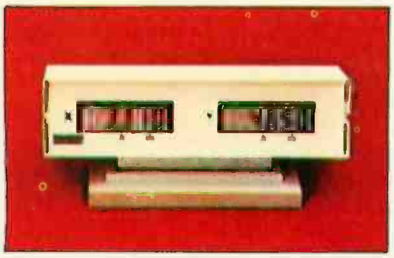

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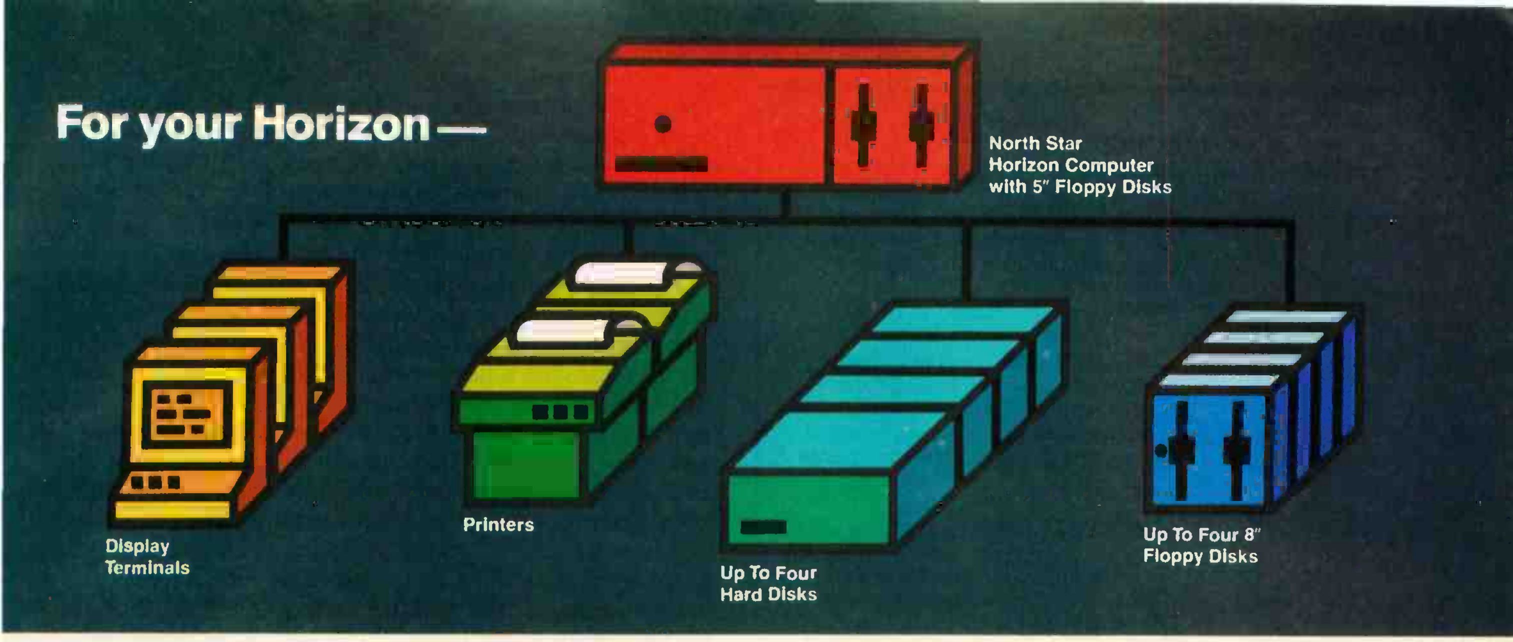
Both of these serial ports are full duplex, permitting information to be sent and received simultaneously. The serial data format consists of a start bit, seven data bits, a parity bit, and either one or two stop bits. Data can be transmitted at one of eight rates, switch selectable from 110 to 9600 bps (bits per second).

The serial ports are set up with TTL (transistor-transistor logic) interface levels, but are format-compatible with the RS-232 standard. The interface can easily be modified to provide full RS-232 compatibility, but two more power supplies must be added to provide

KEYS DEPRESSED	ASCII CONTROL CODE (Hexadecimal)	ACTION TAKEN BY KTM-2
CTRL G CTRL g CTRL '	07	Bell output
CTRL H CTRL h CTRL (	08	Cursor back one space (backspace)
CTRL I CTRL i CTRL)	09	Cursor right one space (horizontal tab)
LINE FEED CTRL J CTRL j CTRL *	0A	Cursor down one space (line feed)
CTRL K CTRL k CTRL +	0B	Cursor up one space (vertical tab)
CTRL L CTRL l (alpha) CTRL ,	0C	Clear display and move cursor home (upper left) (from feed)
RETURN CTRL M CTRL m CTRL —	0D	Cursor to beginning of the same character line (carriage return)
CTRL S CTRL s CTRL: 3	13	Set DC low
CTRL T CTRL t CTRL 4	14	Set DC high
ESC CTRL ; CTRL [	1B	Begin ESCAPE sequence (see ESCAPE SEQUENCE)
CTRL space CTRL @ CTRL shift return	—	Reset KTM-2, clear screen and read option switches
CTRL ALPHA	—	Special—no output is sent over Tx; local clear screen
All Others		Ignored

Table 1: *Many special functions are available to the user of a KTM-2 Terminal-on-a-Board, as demonstrated by this chart of control codes. Control may be asserted manually or by software.*



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SEQUENCE OF CODES RECEIVED BY KTM-2	ACTION TAKEN BY KTM-2
ESC E	FORM FEED: Display is cleared to spaces and cursor moved to first position of first line (the HOME position).
ESC H	HOME: Cursor is moved to HOME.
ESC J	CLEAR EOS (End of Screen): Every position on the screen from the current position of the cursor to the last position of the last line, inclusive, is cleared to spaces. The position of the cursor does not change.
ESC K	CLEAR EOL (End of Line): Every position from the current position of the cursor to the end of the line occupied by cursor, inclusive, is cleared to spaces. The position of the cursor does not change.
ESC R	BEGIN REVERSE: All uppercase letters and all graphics characters received subsequent to reception of the ESC R sequence will be displayed in reverse video.
ESC r	END REVERSE: All displayable characters received subsequent to reception of the ESC r sequence will be displayed in normal video.
ESC G	BEGIN GRAPHICS: Each displayable character received subsequent to reception of the ESC G sequence will cause one of the graphic characters to be displayed.
ESC g	END GRAPHICS: Return to normal display mode.
ESC L	AUX ON: Auxiliary serial port transmission is enabled on-line.
ESC l(alpha)	AUX OFF: Auxiliary serial port transmission is disabled.
ESC +	RELATIVE CURSOR ADDRESSING
ESC =	ABSOLUTE CURSOR ADDRESSING

Table 2: *Special operations, such as reverse video and graphics control, are accessed through the use of the ESCAPE key (ESC) and certain uppercase and lowercase keys.*

SEQUENCE OF CODES RECEIVED	EFFECT ON CURSOR
ESC=SP SP	Cursor to HOME
ESC+SP SP	Position unchanged
ESC+ * ,	Cursor down 10 and right 12
ESC+ 7G	Cursor down 23 and right 39 (or effectively, cursor up 1 and left 1 for a 24-x-40 character display)
ESC= , 4	Cursor to line 12, column 20

Table 3: *The cursor may be addressed in either* relative *or* absolute *mode. Vertical addresses are treated modulo 24, while horizontal addresses are interpreted modulo 40 (modulo 80 for the KTM-2/80). This means that any cursor address that would be off the screen actually wraps around.*

the ±12 V levels. The data transfer rate is selectable via three option switches, but five additional switches provide selectable options such as: even, odd, or no parity; interlaced or noninterlaced screen; line truncation or wraparound; and 60 or 50 Hz frame rate.

The system I connected to the KTM-2 was a Ball Brothers Research video monitor (9-inch diagonal), which has a composite video input that responds to a signal between 0 and 1 V (the KTM-2 can also be jumper set by removing a jumper to deliver a 0 to 2.4 V signal). The computer I used consists of an old IMSAI 8080 microcomputer with 48 K of programmable memory, and some disk drives. Communication to the computer used a dual serial I/O card, and hard copy was provided by a Texas Instruments thermal printer. The printer did not have graphics capability, so I was able to view the graphics display only on the video monitor screen.

Operation of the serial interface requires that the KTM-2 check to see if the $\overline{\text{CTS}}$ line on the main port is asserted before each character transmission. If the signal is not asserted, the KTM-2 will wait until it is—this can be seen on the video display when the cursor stops blinking. When the line is asserted, the waiting character will be transmitted and the cursor will resume blinking.

The keyboard has many control functions available, as shown in table 1. More than one control code is available for a specific operation. There are also many special operations that can be done by use of the ESC key on the KTM-2. These operations are defined in table 2.

One of the special features of the KTM-2 is its capability to perform either *relative* or *absolute* cursor addressing (positioning). Relative cursor addressing causes a vertical displacement supplied by the computer or keyboard to be added to the current cursor vertical address; likewise, a horizontal displacement is added to the current cursor horizontal address. In absolute addressing, the decimal values of two ASCII characters are used to calculate the absolute position of the cursor referenced from the home position in the upper left-hand corner of the screen.

The instruction sequences for absolute and relative cursor addressing modes are shown in table 3 along with some simple positioning examples. All cursor vertical addresses are interpreted as modulo 24, while horizontal addresses are modulo 40 for the KTM-2 and modulo 80 for the KTM-2/80. Modulo implies that the cursor "wraps around"; attempting to position the cursor beyond the end of a line causes it to wrap around to the beginning of the line, and positioning it below the bottom of the screen causes it to appear at the top of the screen.

The KTM-2 manual offered by Synertek Systems is reasonably complete, and it even includes some minor troubleshooting hints. Aside from having to provide your own monitor, power supply, and cabinet, the KTM-2 is a very complete system. There are features lacking that some people might desire for convenience, such as a screen read capability, a parallel ASCII output, or a separate numeric keypad. Aside from this, however, the KTM-2 really seems like a complete solution to the computer user's needs: a low-cost, but powerful, data entry and display system.

For further information, Synertek Systems can be contacted at POB 552 Santa Clara CA 95052, (408) 988-5689.■

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Darth Vader's Force Battle for the TI-59

Clete Jackson, 1715 Dogwood Dr, Rock Hill SC 29730

After purchasing a Texas Instruments TI-59, I realized I owned one of the most capable pocket calculators in the world. I wrote the following program, and allowed several of my friends to play it. They agreed it was the most exciting calculator game they had ever played. The program also uses capabilities of the TI-59 that Texas Instruments does not advertise.

Texas Instruments gives the TI-59 a capability of seventy-two labels. With the following keystrokes, you can add nine more labels that are accessible only through the program; the keystrokes are:

LBL, STO, STO, XX.

Now go back and delete the two STO instructions.

Any of the following can go into the XX location as the label:

62 = Pgm Ind, 63 = Exc Ind, 64 = Prd Ind,
72 = STO Ind, 73 = RCL Ind, 74 = SUM Ind,
83 = GTO Ind, 84 = OP Ind, 92 = INV SBR.

The TI-59 has a decrement and skip branching capability with memories 0 thru 9. With the following keystrokes, this ability can be given to all 100 memories except memory 40, since it implies indirect: DSZ, STO, XX, Y, STO, YY, followed by deleting the two STOs. The XX refers to any memory register except 40. The Y by itself is the hundreds digit of the address to be

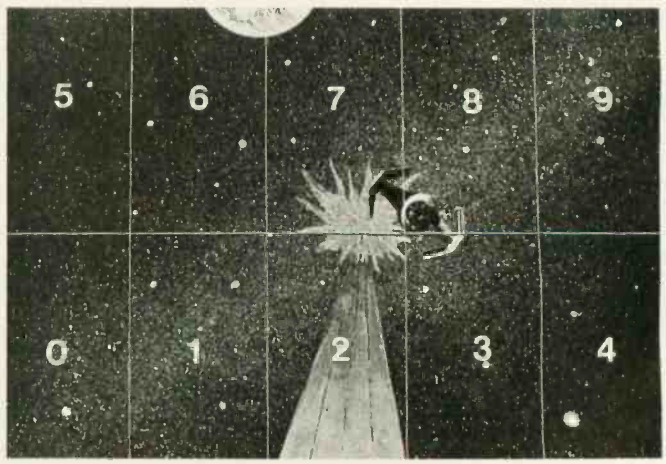

Photo 1: *Battle sector map for* Darth Vader's Force Battle. *To fire into a sector, you wait for the number to appear on the Texas Instruments TI-59 display, press R/S to lock onto it, and press A. See text for further game details.*

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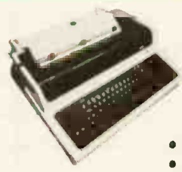

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Listing 1: Darth Vader's Force Battle *for Texas Instruments TI-59 calculator. Shaded entries indicate that two keystrokes are needed to enter the number. See text for details on how the game is played.*

Location	Keys						Commentary
000	LBI	A	x=t	1	39	STO	Firing and positioning subroutine
006	19	SUM	20	−	1	=	
012	x=t	0	26	+	2	=	
018	x=t	0	26	INV	DSZ		
023	CLR	2	B'				Memory address 217
026	RCL	5	+	π	+	RCL	Random number generator
032	20	=	X	7	y^x		
037	9	÷	1	0	y^x		
042	5	=	INV	INT	x		
047	1	0	=	INT			
051	SUM	19	STO	20	x⇄t		
056	Exc Ind	19	Pause	DSZ	19	0	Display subroutine
062	56						
063	if flg	0	1	26			
067	2	Pause	2	Pause	2	Pause	Subroutine to indicate you are losing
073	2	Pause	2	Pause	2	Pause	back position
079	2	Pause	2	Pause	2	Pause	
085	2	Pause					
087	CLR	St flg	0	5	STO	25	
093	GTO	0	26				
096	1	Pause	1	Pause	1	Pause	Subroutine to indicate you are gaining
102	1	Pause	1	Pause	1	Pause	preferred back position
108	1	Pause	1	Pause	1	Pause	
114	1	Pause					
116	CLR	5	STO	25	INV	St flg	
122	0	GTO	0	26			
126		0	0	0	0	0	Subroutine to indicate you are
132	0	0	0	0			being shot down
136	Pause	GTO	1	26			
140	if flg	0	1	26			
144	5	0	5	Pause	GTO	1	Subroutine indicating enemy hit
150	44						
151	LBI	E	STO	20	2	STO	
157	01	5	STO	02	8	STO	
163	03	4	STO	04	9	STO	
169	00	8	STO	05	3	STO	
175	06	6	STO	07	2	STO	
181	08	9	STO	09	1	STO	
187	10	7	STO	11	1	STO	
193	13	4	STO	14	7	STO	
199	15	6	STO	16	8	STO	
205	17	5	STO	18	STO	25	
211	INV	St flg	0	GTO	0	26	
217	if flg	0	0	96	GTO	0	
223	67	LBI	C	GTO	0	02	

branched to. The YY is the tens and units digits of the address to be branched to.

The Program

I wrote the *Darth Vader's Force Battle* program at least a dozen times before I obtained the speed of execution and realism that I desired.

After programming the TI-59, enter a seed number (in the range 0 thru 9999999999), then press E. The game begins.

Imagine yourself in the computer battle scene in photo 1, and that you are the pilot of an X-wing fighter. You are in combat and on the trail of the nefarious Darth Vader. Digits flashing on the display indicate that Darth Vader is making evasive moves to outwit you and sneak in behind your fighter for the kill. You lock on to his location by


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choosing one of the flashing digits and pushing R/S, which locks that digit in the display. You fire into that section by pushing A. But remember that Darth Vader has the force, and he may or may not be at that location by the time you fire. You might use your own force (otherwise known as ESP) and enter a different number by pressing any number 0 thru 9, then fire by pressing A.

If you wait too long before firing, he will outmaneuver you and come in from behind. This is indicated by a string of twos walking across the display. Once Darth Vader is behind you, the flashing digits on the display represent the areas he is firing into. Your flight computer is no match for Darth Vader's force, so you must manually pilot your ship through its maneuvers. You change your position by first pushing R/S. This will lock a digit into the display; pushing C changes your position to the entered location. Remember, your maneuvers will appear on Darth Vader's battle screen just as his did on yours. Once he is behind you, there must be little time wasted in your maneuvers or else you will become just another one of his victims.

Both contestants receive a minimum of 5 shots at each other (ie: if the proper evasive maneuvers are made). A walking display of ones indicates that you have outmanuvered Darth Vader and he is again in your gun sights. A flashing 505 (SOS) indicates that Darth Vader has been hit. A flashing 0000000000 indicates that you have been hit. To start a new game push R/S, enter a seed number, and push E.

The only way you can consistently conquer Darth Vader is if your ESP is strong (otherwise known as luck). Have fun and may the force be with you. ■

Prime Numbers on the HP-19C

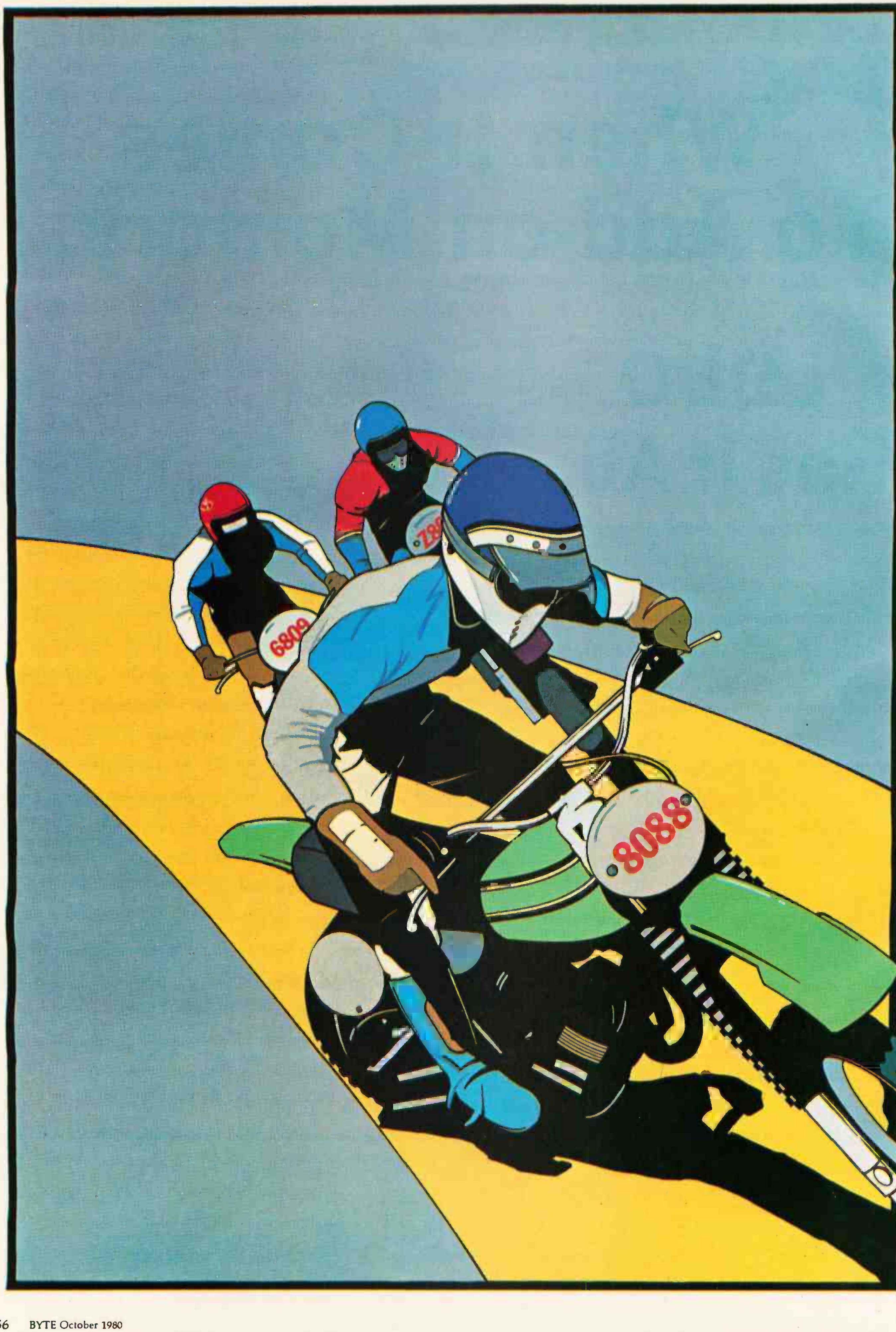
Wilfred Aslan, 26 Twin Brooks Dr, Willow Grove PA 19090

A few months back, a neighbor proudly showed me a program she had developed for her first computer science course. As James R Lewis speculated in his article "TRS-80 Performance Evaluation by Program Timing" (see March 1980 BYTE, page 84), the program concerned the determination of prime numbers. Intrigued, I spent some time on this subject working with my little Hewlett-Packard HP-19C programmable printing calculator. Assuming that Lewis has rekindled interest in the competitive programmer's desire for fast programs, I offer a more efficient means for the test of a prime number.

In the classic algorithm, the number being tested is always odd, because even numbers are divisible by 2. The number being tested is divided by a series of odd numbers, starting with three, and progressing by twos. If the remainder of each successive division includes fractions, the number must be prime. The trick, of course, is knowing when to stop dividing.

A moment's reflection will show that as the value of the divisor progresses beyond the square root of the number under test, the quotients will all be smaller than the square root. Since numbers less than the square root have already been tried, further testing is pointless.

 Circle 32 on inquiry card. Circle 33 on inquiry card. →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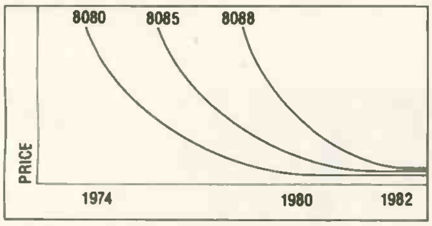

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Listing 1: *A program which calculates the prime numbers to 10,000, using the square-root test limit. This listing is for the HP-19C calculator, which finished the job in just over fifteen hours.*

```
01 *LBL0 25 14 00      24    2          02
02   1           01    25  ST+1 45 41 01
03  PRTX         65    26  RCL1     55 01
04  ST01      45 01    27  RCL3     55 03
05   2           02    28   X⇄Y        11
06  PRTX         65    29  X≤Y?     16 31
07   3           03    30  GT03     14 03
08  PRTX         65    31  RCL2     55 02
09  ST02      45 02    32  PRTX        65
10   EEX         23    33    1         01
11   2           02    34  ST01     45 01
12  ST04      45 04    35  GT01     14 01
13 *LBL1 25 14 01      36 *LBL3 25 14 03
14   2           02    37  RCL2     55 02
15  ST+2  45 41 02     38  RCL1     55 01
16  RCL2      55 02    39    ÷         61
17   √X       16 53    40   FRC     25 52
18  ST03      45 03    41  X≠0?     25 51
19  RCL4      55 04    42  GT02     14 02
20  X>Y?      16 41    43    1         01
21  GT02      14 02    44  ST01     45 01
22   R/S         64    45  GT01     14 01
23 *LBL2 25 14 02      46   R/S        64
```

Listing 2: *The beginning and end of the program when run to calculate all primes up to 10,000.*

```
 1.            97. ***     9769. ***
 2.           101. ***     9781. ***
 3.           103. ***     9787. ***
 5. ***       107. ***     9791. ***
 7. ***       109. ***     9803. ***
11. ***       113. ***     9811. ***
13. ***                    9817. ***
17. ***      9613. ***     9829. ***
19. ***      9619. ***     9833. ***
23. ***      9623. ***     9839. ***
29. ***      9629. ***     9851. ***
31. ***      9631. ***     9857. ***
37. ***      9643. ***     9859. ***
41. ***      9649. ***     9871. ***
43. ***      9661. ***     9883. ***
47. ***      9677. ***     9887. ***
53. ***      9679. ***     9901. ***
59. ***      9689. ***     9907. ***
61. ***      9697. ***     9923. ***
67. ***      9719. ***     9929. ***
71. ***      9721. ***     9931. ***
73. ***      9733. ***     9941. ***
79. ***      9739. ***     9949. ***
83. ***      9743. ***     9967. ***
89. ***      9749. ***     9973. ***
             9767. ***
```

By limiting the tests in this way, the number of loops necessary may be reduced significantly. In the "Lewis Test" of numbers to 10,000, the largest prime number is 9973, and his program uses test divisors to half that (4986.5), requiring 2491 executions of the loop. By using a divisor limit of 99 (the square root is actually 99.86), the loop need only be executed forty-eight times. On the HP-19C, this gives times of 38 m 18.1 s (for the original test) versus 46.4 s (testing only to the square root limit). For the complete computation of primes up to 10,000, the little calculator finished the assignment in 15 h 16 m 22.7 s, using the square-root limit. Listing 1 shows the program; listing 2 contains the beginning and end of my list of prime numbers. ■

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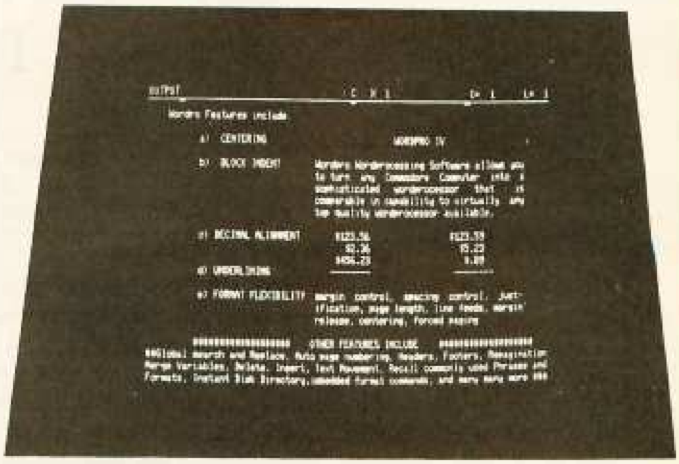

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An 8088 Processor for the S-100 Bus

Part 2

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2475 Borax Dr
Santa Clara CA 95051

Last month I talked about the Intel 8088 microprocessor (a 16-bit processor with 8-bit connections to the outside world), its associated support devices, and the general subject of doing 16-bit processing on the S-100 bus. In this portion of this three-part article, I will present the design of my 8088-based S-100 processor board. In part 3, I will describe MON88, a machine-language monitor for this processor board.

Interfacing

While the processor board presented here is compatible with the S-100 boards in *my* system, it does *not* fully conform to the proposed IEEE (Institute of Electrical and Electronics Engineers) standard. By devoting a little additional design effort, an interested reader should be able to make the board as IEEE-compatible as he wishes and can implement features I chose not to include. Refer to figure 1, the schematic diagram for the processor board on pages 66 and 67, throughout the following section.

The adaptation of the basic computer to the S-100 bus can be broken up into four necessary tasks:

- providing a buffered, demultiplexed address bus;
- providing for separate 8-bit buffered input and output data buses;
- generating a buffered command/control bus;
- producing the required status signals.

The Address Bus

It is necessary to demultiplex and buffer the address bus of the 8088 to communicate with the rest of the system. An immediate question is how to deal with twenty address bits instead of the traditional sixteen. The IEEE S-100 *standard* defines certain pins for *extended addressing*. However, some popular memory boards use bank-switching techniques, which are ill-defined between various manufacturers. My solution is to simply ignore the problem by using only the lower 16 address bits. A 64 K-byte address space is more than adequate for my current needs; and besides, none of the spare memory boards I will be using have either extended addressing or bank-select capability.

Looking at the schematic in figure 1, we see that IC6 and IC7 solve the problem. These are 8282 octal latch buffers, which are much like the familiar 8212 device (see figure 2). Two differences are that the drive capability of the 8282 is greater than that of the 8212, and it comes in a narrow twenty-pin package (versus the wider twenty-four-pin package of the 8212).

In the case of lines AD0 thru AD7, the 8282 also does the required demultiplexing of data and address information. By tying the 8282 STB (strobe) input line to the 8088 ALE (address latch enable), IC7 serves to latch the address. Since A8 thru A15 are only address information, the STB input of IC6 can simply be tied high. Also note the presence of S-100 signal ADSB* (address disable) at the OE* (output enable) pins of both IC6 and IC7. (The asterisk indicates an active-low signal.)

Each basic bus (address, data, status, and command/control) has a signal that can be used to cause the bus to go into its "disconnected" high-impedance state. This is important for DMA (direct memory access) -type functions in which different bus masters (processor, DMA controller, etc) must take control of the system. By causing the bus of the processor board to go into its high-impedance state, the whole processor board effectively "disappears" as far as the rest of the system is concerned. ADSB* performs this disappearing act for the address bus of the 8088 by pulling the 8282 OE* (output enable) pins high.

As a final note, the IEEE S-100 extended-addressing standard could be easily implemented by feeding lines A16/S3 thru A19/S6 into another 8282, demultiplexing the information with the ALE line, and bringing the appropriate outputs onto the defined S-100 lines.

Data Buses

IC8 (another 8282) buffers the data-output bus. Note that the S-100 signal DODSB* (data-out disable) serves to disconnect the output data bus for DMA, just as ADSB* did for the address bus. IC9 (an 8282) buffers the input data bus. Notice here that:

- There is no DIDSB* line. The purpose of the four bus-disable signals ADSB*, DODSB*, SDSB* and CDSB* (address-, data out-, status-, and control-disable lines) is to make the processor disappear from the bus, so that another processor can take control. Consequently, the only buses that need to disappear are ones that drive the bus (hence only output buses).
- IC9's OE* connection (B) is the output of some TTL (transistor-transistor logic) at the top of the schematic which serves to disable IC9. (Rest assured that I will explain what is going on in more detail.) Whenever we are reading from the on-board memory and I/O (input/output) ports (8185-2 and 8755A-2), this disconnects the data-input bus from the 8088, thereby eliminating a potential for bus contention.

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- The eight 1 k-ohm pull-up resistors have a number of effects. First, accessing nonexistent memory or I/O devices will always yield hexadecimal 0FF (all 1 bits). Second, it is easier and faster to pull a normally high signal low than the other way around. Most important, the S-100 bus traditionally allows boards that drive the input data bus of the processor to use either TTL three-state drivers or open-collector drivers. The S-100 standard requires the existence of 1 k-ohm pull-up resistors to +5 V somewhere on the open collector lines. Here they are.
- "IC10" is a sixteen-pin socket with the eight address/data lines wired across it. This is for connection to the diagnostic front panel.

So far, everything has been pretty straightforward. Now comes the interesting part of the design effort. The question is how hard is the design, and how much TTL "glue" will it take to emulate the required status and control signals.

The Control Bus

Another 8282 buffer (IC5) is used to drive four control output signals (pHLDA, pWR*, pDBIN and pSYNC):

- **pHLDA:** The processor hold-acknowledge line is used when a DMA controller (or other bus master) wishes to take control of the system bus. It does this by asserting the HOLD* command to the current processor (bus master). Then the processor turns off its own address, data, and status output buses using ADD ADSB*, DODSB*, and SDSB* lines. When the processor is ready to "get off" the bus, it will assert pHLDA, which informs the processor "getting on" the bus that the final transfer of bus control can take place. At this point, the new master completes the transfer by turning off the old master's control bus (via CDSB*).

The 8088 HLDA pin provides the S-100 bus pHLDA function.

- **pWR*:** The processor write line is the general-purpose write or output strobe for transmitting data to system memory or peripherals. The 8088 WR* pin provides the S-100 bus pWR* function.
- **pDBIN:** The processor data-bus-in signal is the general-purpose read or input stobe for transmitting data from system memory or peripherals.

The 8088 RD* pin, inverted by IC11, provides the S-100 bus pDBIN function.

- **pSYNC:** The processor sync signal tells the rest of the system when a new bus cycle is starting. This makes possible processor designs that are independent of the number of intrinsic bus cycles per machine cycle. Many 8-bit machines have three bus cycles for each machine cycle. The 8088 has four bus cycles per machine cycle. Any bus slave that is concerned with what cycle the bus is in can synchronize pSYNC, regardless of the processor being used.

The 8088 ALE signal correctly identifies the start of a bus cycle and can be used for the S-100 bus pSYNC signal.

The control input bus lines are scattered on the right side of the schematic and consist of the RDY, XRDY, INT* and HOLD* signals. (See figure 1.)

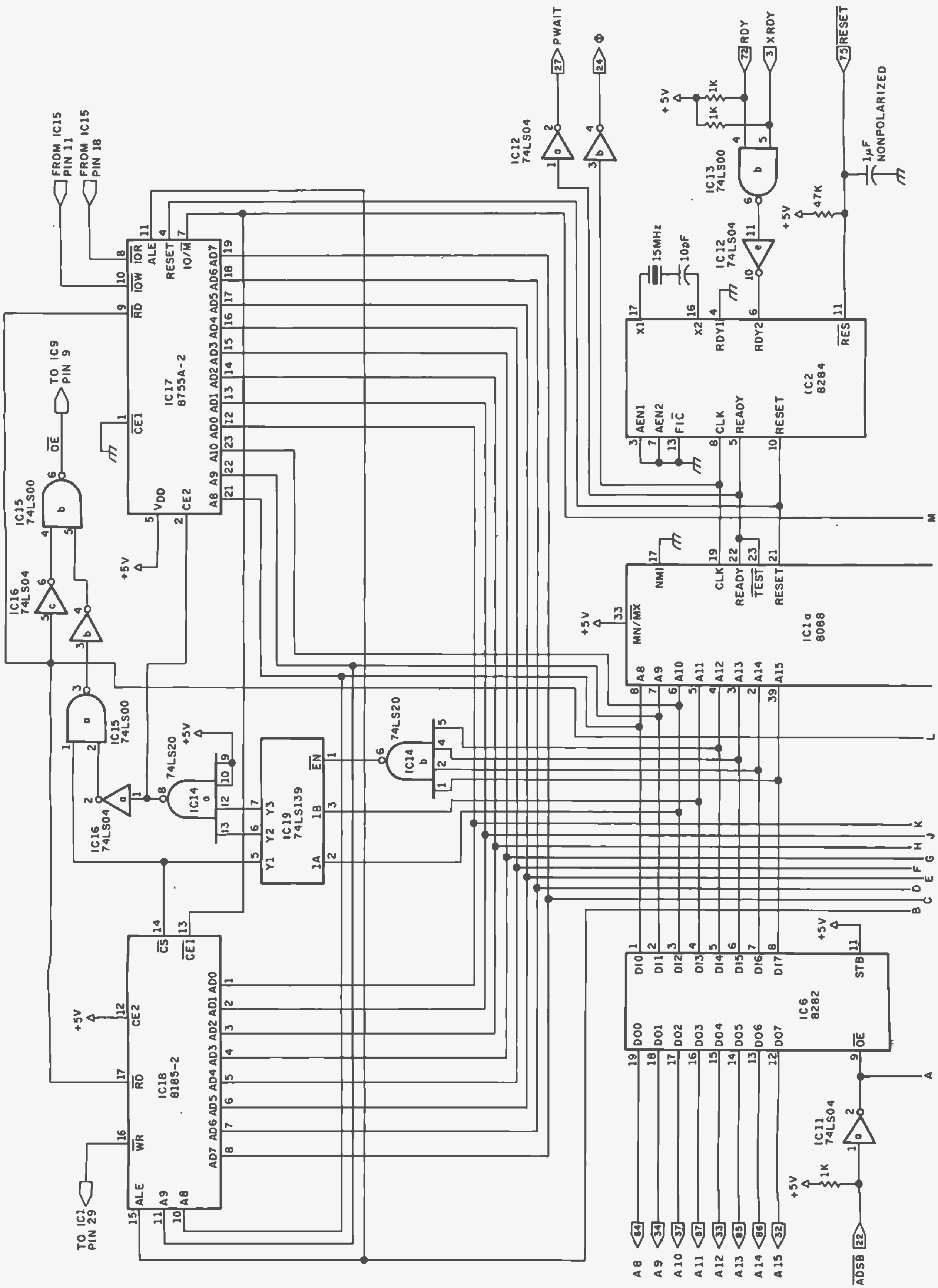
- **RDY and XRDY:** These lines serve essentially the same purpose, to force the processor to execute wait states. RDY is traditionally used by slow memory or I/O devices, while XRDY is used by front panels to implement run/stop and single-step capabilities. Both lines are pulled up by 1 k-ohm resistors, and if either goes low, IC12 and IC13 bring the 8284 line RDY2 low and the information goes through the 8284 to the 8088 (via their READY lines).
- **HOLD*:** The HOLD* line on the S-100 bus is equivalent to the HOLD line on the 8088 when it is inverted by IC12.
- **INT*:** The INT* line on the S-100 bus is equivalent to the INTR line on the 8088 when it is inverted by IC11.

The Status Bus

The question here is how closely the status outputs of the 8088 correspond to those needed by the system. This can be a real problem in interfacing processors to buses for which they were not designed. After all, it is a fundamental architectural decision about what a given processor will tell the rest of a system about its activities and when. Creating status signals with TTL devices can be quite a problem.

In this case, we are very fortunate with the 8088. Consistent Intel design philosophy is apparent here, easing our interface task. Looking back at table 2 of Part 1 last month, we recall that the states of three pins (IO/M*, DT/R*, and SSO*) fully encode the 8088 status. The timing diagram shows that status is valid at the right time, shortly after the start of the bus cycle. Using an 8205 1-of-8 decoder (IC3), the decoded status can be fed to the bus through a buffer (IC4). IC4 is not an 8282; it is an 8283, which is an 8282 with inverted outputs.

Text continued on page 68



IC17 8755A-2
IC18 8185-2
IC19 74LS139
IC2 8284
IC1a 8088
IC6 8282
IC15 74LS00
IC16 74LS04
IC14 74LS20
IC12 74LS04
IC13 74LS00
IC11 74LS04
FROM IC15 PIN 11
FROM IC15 PIN 18
TO IC9 PIN 9
TO IC1 PIN 29
PWAIT
Φ
RDY
XRDY
RESET
15MHz
10pF
1µF NONPOLARIZED
47K
1K
+5V
ADSB
A8
A9
A10
A11
A12
A13
A14
A15

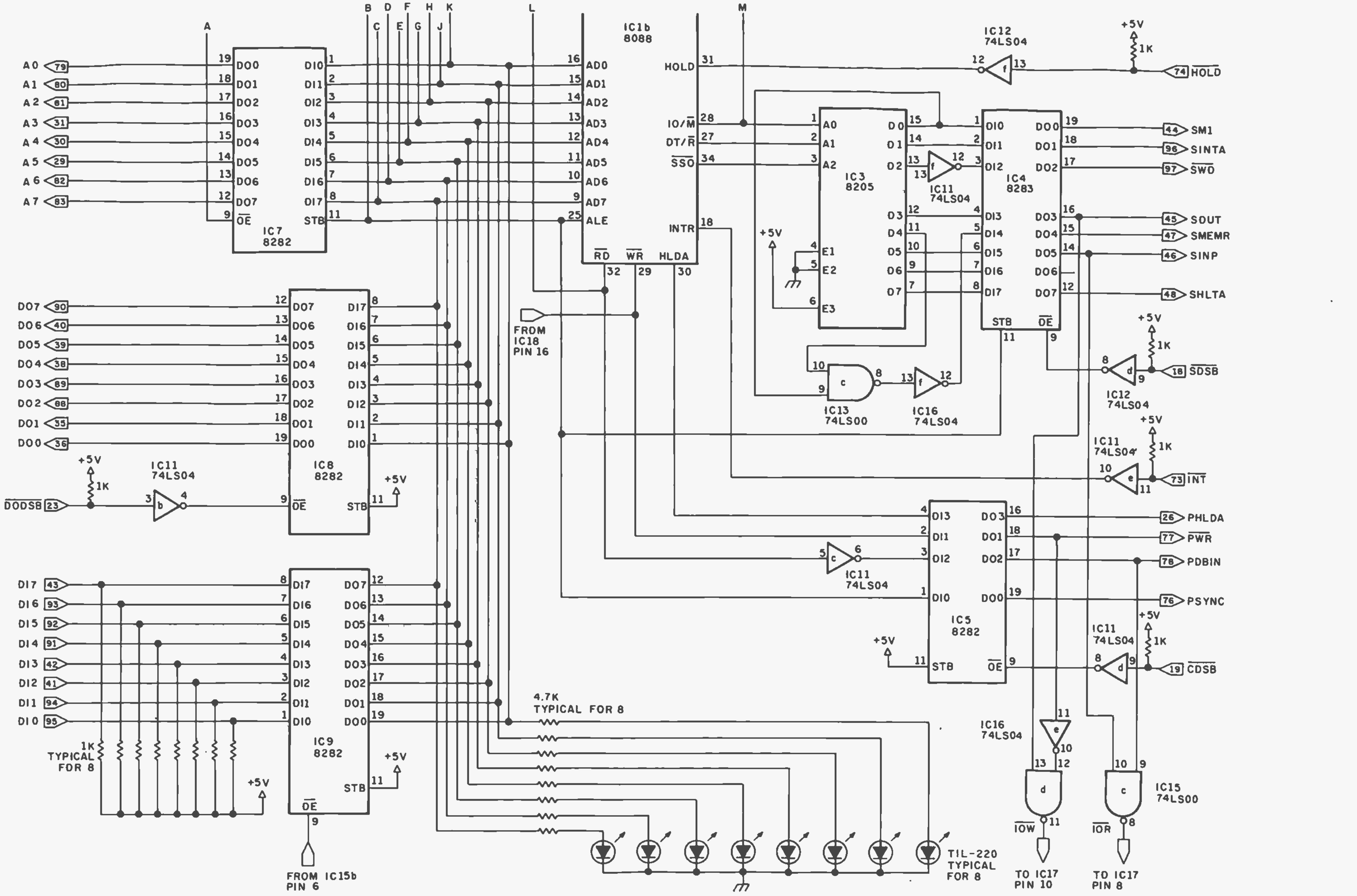


Figure 1: *Schematic diagram of the 8088 processor board for the S-100 bus. This shows the logic necessary to provide a buffered, demultiplexed address bus, and input and output buses for the S-100 standard. Logic also produces the necessary status signals and buffers the control bus. Power connections for the integrated circuits are given in table 1.*

Number	Type	+5 V	GND
IC1	8088	40	1
IC2	8284	18	9
IC3	8205	16	8
IC4	8283	20	10
IC5	8282	20	10
IC6	8282	20	10
IC7	8282	20	10
IC8	8282	20	10
IC9	8282	20	10
IC10	7474	14	7
IC11	74LS04	14	7
IC12	74LS04	14	7
IC13	74LS00	14	7
IC14	74LS20	14	7
IC15	74LS00	14	7
IC16	74LS04	14	7
IC17	8755A-2	40	20
IC18	8185-2	18	9
IC19	74LS139	16	8

Table 1: *Power connections for the integrated circuits in the schematic diagrams of figure 1 and figure 5.*

Text continued from page 64:

As usual, the OE* of IC4 is tied to the appropriate disable signal (in this case, S-100 SDSB*, or status disable).

Thus, 8088 pins IO/M*, DT/R*, and SSO* are fed as inputs to the 8205 decoder (IC3), and the status appears through the inverting 8283 (IC4):

- **sM1:** The status M1 signal indicates to the system that an op-code fetch (8080A style) is taking place. The reason I say "8080A" style is that sM1 for an 8080A is different from the status instruction fetch of the 8088.

For example, on an 8080A, you must use 3 bytes when you want to load a register (pair) with a 16-bit data item. The first is the instruction itself, while the second and third bytes are the data. The 8080A treats only the first byte-fetch as an instruction fetch; the second 2 bytes are operand fetches. The 8088, on the other hand, treats all three fetches as instruction fetch (ie: sM1).

This signal is not required by any of the boards I plan to use in the system, so the only real difference I notice is that the 8088's front-panel sM1 light seems brighter than the one on the IMSAI (due to its being on more often).

- **sINTA:** The S-100 status interrupt-acknowledge line indicates that the processor is in an interrupt-acknowledge sequence. 8088 interrupt-acknowledge status works just fine.
- **sWO*:** The S-100 status write/output signal is used to tell slave units that the processor is sending data to them. Commonly, the signal, in conjunction with address-decoding circuitry, acts as a select signal for other boards in the system. Since this signal is active low, the inverter at IC11 conditions the 8088 status.
- **sOUT:** The status output line tells the rest of the system that the processor is transferring data to an output port. The derived "write I/O" line from the 8088 is used to implement the S-100 sOUT line.
- **sMEMR:** The S-100 status memory-read line is used to select memory boards for input. On the 8080A, sMEMR is generated for all memory accesses including code, operand, and data (stack operations). On the 8088, status memory-read is generated only for data movement (eg: MOV MEMPOINTER, 0) and stack operations (eg: POP AX).

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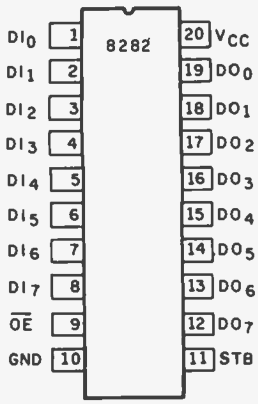

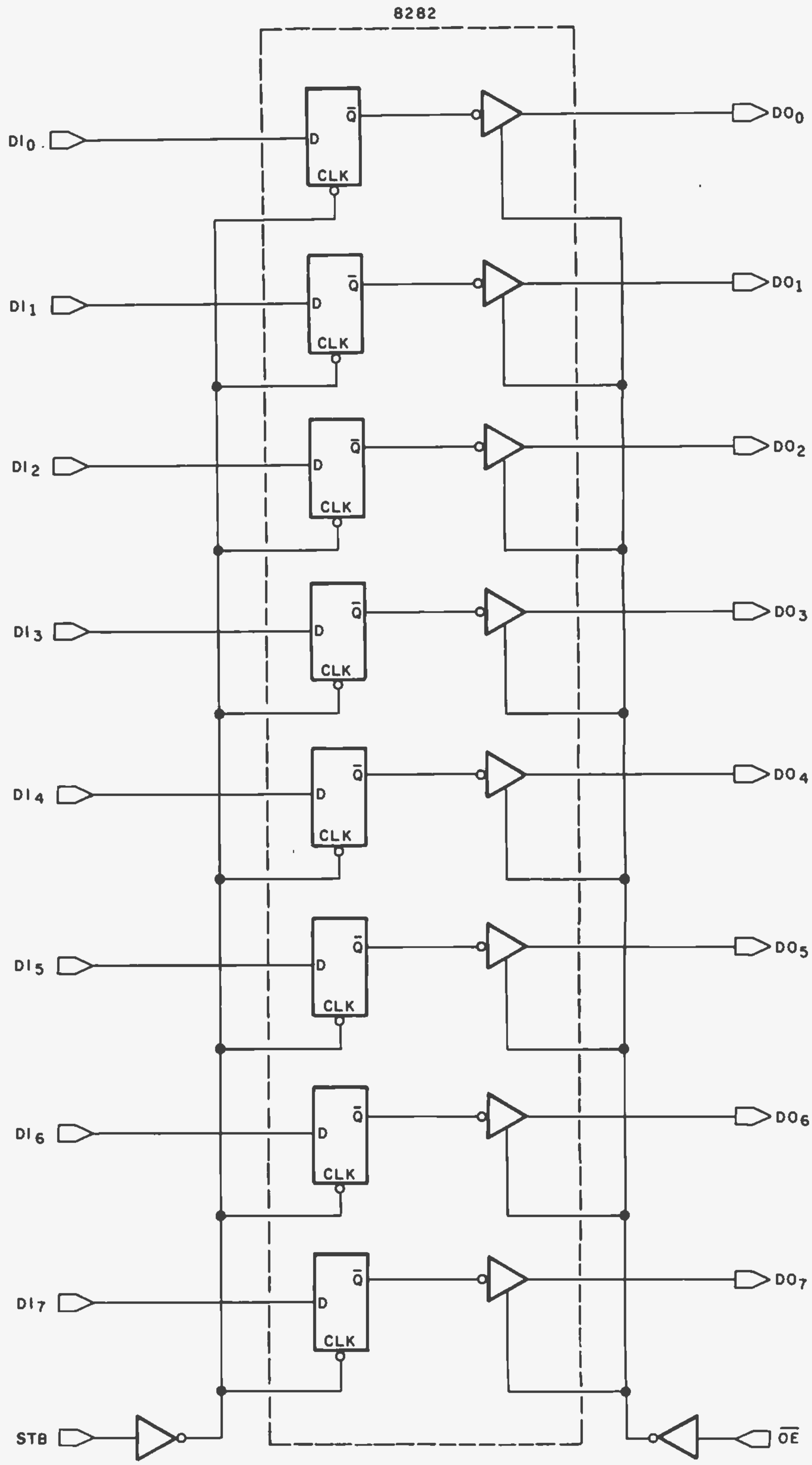

Figure 2: *The 8282 8-bit buffer/latch. Similar to the familiar 8212, the 8282 has a greater drive capacity and comes in a narrower, twenty-pin dual-in-line package.*

Examining the schematic, we see that IC3 output 0 (indicating code access) and IC3 output 4 (indicating memory-read) are gated into NAND gate IC13, and the result is fed through inverter IC16 before being brought out as sMEMR via IC4. This allows sMEMR to be generated by the 8088's read-memory status, but it also insures that sMEMR is asserted whenever the 8088 status is "code access" (ie: sM1).

- **sINP:** This status input line tells the rest of the system that the processor is requesting data from a port; this signal is easily implemented with the 8088 "read I/O" derived status signal.

● **sHLTA:** The S-100 status halt-acknowledge signal is asserted when the processor enters a halt state. The 8088 "halt" decoded status line provides this function.

Design Details

The S-100 system-clock signal (Φ, pin 24) is sent from the CLK output of the 8284 through an inverter in IC12 that serves to invert and buffer the 5 MHz signal.

Another signal, PWAIT, is the logical inversion of the READY input to the processor. This is brought out to S-100 pin 27. I use this to observe READY status on the front panel.

A front panel RESET switch (closure to ground) comes onto the board through the RC (resistor/capacitor) timing network (47 k-ohm resistor, 1 μF capacitor) and is connected to the 8284 RES* input.

The bottom-right of figure 1 contains a couple of gates and an inverter. This circuit determines if an I/O READ or I/O WRITE is taking place and properly controls the IOR* and IOW* inputs to the 8755A-2. These signals are used when the two 8-bit parallel ports it contains are accessed.

Finally, the circuit containing IC19, IC14, and various inverters (these appear in the upper-middle portion of the schematic) fully decodes (ie: with no wasted address space) the address for the 2 K bytes of EPROM (erasable programmable read-only memory) and 1 K bytes of programmable memory on the processor board (8755A-2 and 8185-2). The 2 K bytes of EPROM are addressed from hexadecimal XF800 to XFFFF, and the 1 K bytes of user memory are addressed from hexadecimal XF400 to XF7FF.

Since only sixteen address lines are used, the contents of the upper four address lines are not important, hence the X in the above hexadecimal numbers. Some I/O space is wasted though; the 8755A-2 uses the state of address lines AD0 and AD1 to determine whether to utilize port A or port B during I/O operations. With my decoding, I/O addressing is such that port A will be accessed with port addresses between hexadecimal F800 and FFFF, which map into the following address pattern:

Port A address = 1111 1XXX XXXX XX00
(ie: 0F800, 0F804, etc)

Port B uses addresses in the same range (ie: 0F800 to 0FFFF) that match the following pattern:

Port B address = 1111 1XXX XXXX XX01
(ie: 0F801, 0F805, etc)

Remember that the 8088 uses a full 16-bit I/O address (as the IEEE standard recommends) rather than echoing the 8-bit I/O address on the high and low bytes of the address bus (as the 8080A does).

Other Signals: Pins 1 to 50

I have left some signals off the board that you may want to use, so before you start building, you may want to pencil in a few of your own design additions. Some of the missing signals relate to the IEEE standard and some are old standbys that appear on many boards. The following is a general summary of my usage (or nonusage) of all S-100 lines.

● **XRDY:** Pin 3 on the S-100 bus is one of the two

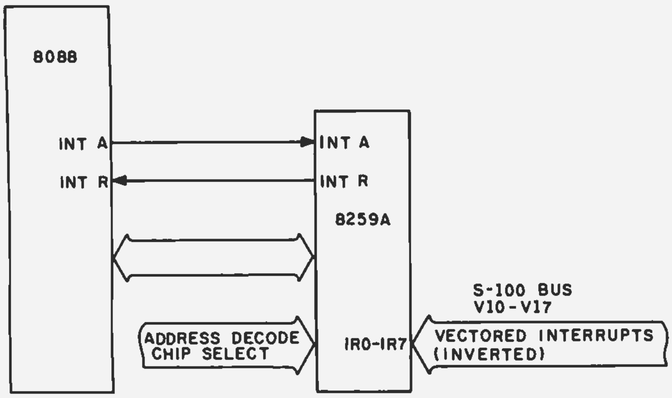

Figure 3: *An 8259A Programmable Interrupt Controller can be added to the system by following this logic diagram. The 8259A requires access to the demultiplexed bidirectional data bus of the processor in order to properly interpret vectored interrupts from the S-100 bus.*

"ready" inputs used (the other is RDY, pin 72). In particular, XRDY is meant to be used by front panels, as opposed to slow memory or I/O devices. I use this signal for just this purpose, allowing the implementation of run/stop and single-step functions.

- **VI0 thru VI7:** S-100 pins 4 thru 11 are dedicated to eight different vectored-interrupt inputs. These were originally designed around Intel's 8259A PIC (Programmable Interrupt Controller). Without going into a lot of detail, the use of a PIC allows flexible assignment of priorities for eight levels of interrupts and a programmable definition of the processor response to each. While the basic method of operation of an 8259A with the 8088 is slightly different from its operation with an 8080A or 8085A, the 8259A is still the interrupt controller to use.

I have not implemented an 8259A in my design, but it is a logical and easy addition. All that is required is that the VI0 thru VI7 inputs (inverted) be tied to IR0 thru IR7 on the interrupt side of the 8259A. Then the INT output of the 8259A is tied to the INTR input of the 8088 (see figure 3). On the programmable side of the 8259A, we need to connect the data bus of the processor (D0 thru D7, the demultiplexed data bus). In addition, address decoding and chip-select logic that meets your needs (ie: hardwired or switch-selectable) is needed to access the 8259A.

- **NMI*:** S-100 pin 12 is a nonmaskable interrupt line. As the name implies, this is an interrupt input to the processor that cannot be masked in software. All that is necessary to use this input is to run the S-100 NMI* line through an inverter and into the NMI input of the 8088. Nonmaskable interrupts are usually reserved for catastrophic occurrences that require immediate processor attention (such as impending power failure or recurring bus errors).
- **PWRFAIL*:** The IEEE standard specifies pin 13 as a power-failure signal, an input that indicates impending power failure. Noticing the physical proximity to pin 12 (NMI*) and the same inverted-logic convention, the intention is to jumper pin 12 to 13 and use PWRFAIL* to generate an NMI before a power interruption. In this case, the NMI routine of the processor could save critical system-status parameters (register contents, stack pointer and contents) in battery-powered programmable memory, then perform a software halt to prevent the processor from causing the system to crash as it "dies."
- **DMA0 thru DMA3:** The IEEE standard uses pins 55, 56, 57, and 14 for DMA-priority arbitration. This allows resolution of requests for use of the bus by up to 16 would-be bus masters. As I had no use for this feature, these lines are not used in this design. The traditional HOLD/HLDA (hold, hold acknowledge) protocol using pins 74 and 26 is implemented, however.
- **A16 thru A23:** As mentioned before, the IEEE standard does provide for an extended addressing scheme. Since I have chosen to use only sixteen address lines (A0 thru A15), none of the extended lines are used. If you have memory boards that support the IEEE standard, it is a simple matter to bring the upper four address lines of the 8088 (A16/S3 thru A19/S6) onto the S-100 bus using an additional 8282 latch. Remember to demultiplex the address and status information on these lines using the 8088 ALE connected to the strobe input of the 8082 (STB, pin 11).
- **SDSB*, CDSB*, ADSB*, and DODSB*:** The status-, control-, address-, and data-out-disable lines are used as they are intended, namely to disable the associated buses by causing them to change to their high-impedance state.
- **pSTVAL*:** The IEEE standard calls for a processor-status-valid signal used to latch the processor status. Since none of my boards require the presence of this signal, it is not implemented. If you need pSTVAL*, some massaging of the 8088's ALE signal with the system clock (Φ) will probably do the trick.

● **SS, SSW DSBL*, and RUN:** The IMSAI uses pins 21, 53, and 71 for single-step, a sense-switch-disable signal and a run indicator. These are all officially archaic according to the IEEE standard and are not used.

● **PROTECT, UNPROTECT and PROTECT STATUS:** S-100 pins 70, 20, and 69 represented a short-lived attempt by some manufacturers to implement memory protection and unprotection in software. It was soon noticed that the first thing a "crashing" program always does is to randomly produce the right code sequence to unprotect your memory. So much for these three signals. They are not implemented in my design.

● **Φ:** Another holdover from the 8080A is the two-phase clock. The other phase is almost an inversion of the Φ (main system) clock, but not quite. If you need $\phi 1$ (probably not), you will need to synthesize it using TTL devices.

●**PWAIT:** One leftover from the IMSAI that I did retain is the processor-wait-control output line (PWAIT, pin 27). I use this to light a front-panel LED (light-emitting diode) so I know if the processor is running or has stopped. It is also handy for monitoring the reaction of the processor to memory slow enough to need wait states.

The remaining signals (thru pin 50) are used as intended, and specified by the IEEE standard with an exception for the definition of sM1 and the deletion of CLOCK:

● **sM1:** Pin 44 is used for a status M1 signal, generally occurring during an op-code-fetch cycle. A potential problem occurs here in that the 8080A's op-code fetch is different from the code-access status signal of the 8088 as decoded from IO/M*, DT/R* and SSO*.

As I mentioned earlier, allowing sM1 to occur for both op-code and operand fetches causes no problems.

Looking over the schematics for some of the boards I own, I noticed that sM1 is rarely used except by some front-panel controllers. Front panels use it to insure that the STOP part of the RUN/STOP function always occurs at the first byte of an instruction. I have used the 8088's status-code access as a substitute for sM1 without problems.

● **CLOCK:** This line (pin 49) is specified as a 2 MHz clock running asynchronously with the main processor and thereby independent of its clock frequency. I/O boards may use this for data-rate generation. If I ever need to implement CLOCK, I will probably use a 2 MHz crystal oscillator circuit, since it is not obvious how to generate 2 MHz from 5 MHz. (Let's see, where's that divide by two-and-a-half circuit?) Now if the 8088 could run at 8 MHz, we could just divide PCLK (you remember the 8284 peripheral-clock output) by 2 and have our 2 MHz CLOCK signal.

Other Signals: Pins 51 to 100

Here are some more S-100 bus signals you may want to add to your design:

● **SLAVE CLR*:** S-100 pin 54 is meant to be kind of a reset for bus slave devices (primarily I/O boards) so they can reset counters or whatever. If you want to implement SLAVE CLR* use either a separate front-panel switch or the other side of the master RESET switch (as the IMSAI computer does).

● **PHANTOM*:** Pin 67 is the much maligned PHAN-

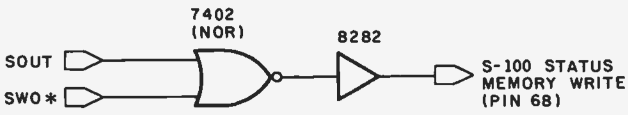

Figure 4: *The MWRT (memory write) signal required by S-100 systems can be provided by simple logic, if it is not generated elsewhere in the system.*

TOM* line. It was originally developed to resolve the conflict between the reset start address of 0 on the 8080A and the fact that most people prefer processing to begin at some higher address (to support ROM and EPROM monitors in high memory). Without going into a lot of detail, PHANTOM* is used to make a programmable memory board addressed at memory location 0 "disappear" while it is "replaced" by a read-only memory at some higher address. Consequently, when the computer starts executing at location 0, it is actually executing the first few instructions in the read-only memory. This is usually a JMP instruction to the actual address of the read-only-memory board. Since the 8088 nicely begins executing in high memory at absolute address hexadecimal 0FFFF0, which is treated as hexadecimal 0FFF0 by my machine (remember, only sixteen address lines are currently used), the problem resolves itself and PHANTOM* is not needed.

- **MWRT:** S-100 pin 68 is used for the memory-write status line. This is simply a logical combination of two existing status signals (sWO*, status write out; and sOUT, status out). MWRT can be a real problem if you are not careful. The basic problem is that MWRT is not required to be generated by the processor, but it must be present somewhere in the system. It seems that every manufacturer does you a favor by providing MWRT capability on their board. I have seen MWRT on front-panel boards, memory boards, processor boards, disk controllers, etc. Ensure that there is one and only one MWRT in your system. If it does not exist, let me recommend that you add a 7402 NOR gate and use one of the unassigned outputs of the 8282 (IC5) for buffering as shown in figure 4. In my case, MWRT is generated on the BYT-8 motherboard.
- **SSTACK and ERROR*:** Pin 98 on the IMSAI was used for the 8080A-dependent signal, status stack-access. It indicates that the stack is being accessed (ie: via PUSH or POP) and is never used for anything. In a segmented-memory machine like the 8088, however, it might be of more interest to know if the stack is being accessed. By decoding S4 and S3 (equivalent to A17/S4, A16/S3 on the 8088), this can be determined.

Realizing the nebulous virtues of SSTACK, the IEEE standard uses pin 98 as a general-purpose ERROR* indicator. When memory boards with parity capability are widely used, ERROR* could be used to indicate parity errors. ERROR* could then be tied to NMI*, and the processor's nonmaskable-interrupt routine could call for a rerun of the failing bus cycle. Since none of this grandiose scheme is currently implemented on my board, pin 98 is not used.

- **POC*:** Pin 99 is defined as power-on-clear line, which is supposed to exercise both master RESET* (pin 75) and SLAVE CLR* (pin 54) upon system power-up. Since the RC timing network I use on RESET* does the trick for resetting the 8088, and SLAVE CLR* is not used; there is no need for POC*.

Before you go overboard trying to implement a lot of the above, I want you to know that most of it is probably not needed. The current design works just fine with all of my boards, including:

- Wameco 8 K 2102 memory boards (and others of similar design)
- Godbout 16 K and 32 K 4044 (or equivalent) based memory boards
- SSM Parallel I/O board
- SSM VB1 Video Interface
- Cromemco Bytesaver 2708 board
- TDL VDB Video Interface
- Tarbell Cassette Interface
- Tarbell single-density floppy-disk controller
- Vector Graphics 2708 programmable read-only memory board

Implementation

Start by looking at the photos of the front and back of the board (see photos 1a and 1b on page 80). Regarding the back side, all I can say is "functional is beautiful." It is not really as formidable as it seems. I will proceed to give some hints that may prove useful.

Remember, patience is a virtue. I used a CCS (California Computer Systems) wire-wrap board for a number of reasons. The provision for voltage regulation (and filtering) and the ground plane around the edge of the board are nice. The board is uncommitted to any particular device size, allowing any combination of dual-in-line sockets. In addition, the feed-through holes are all plated,

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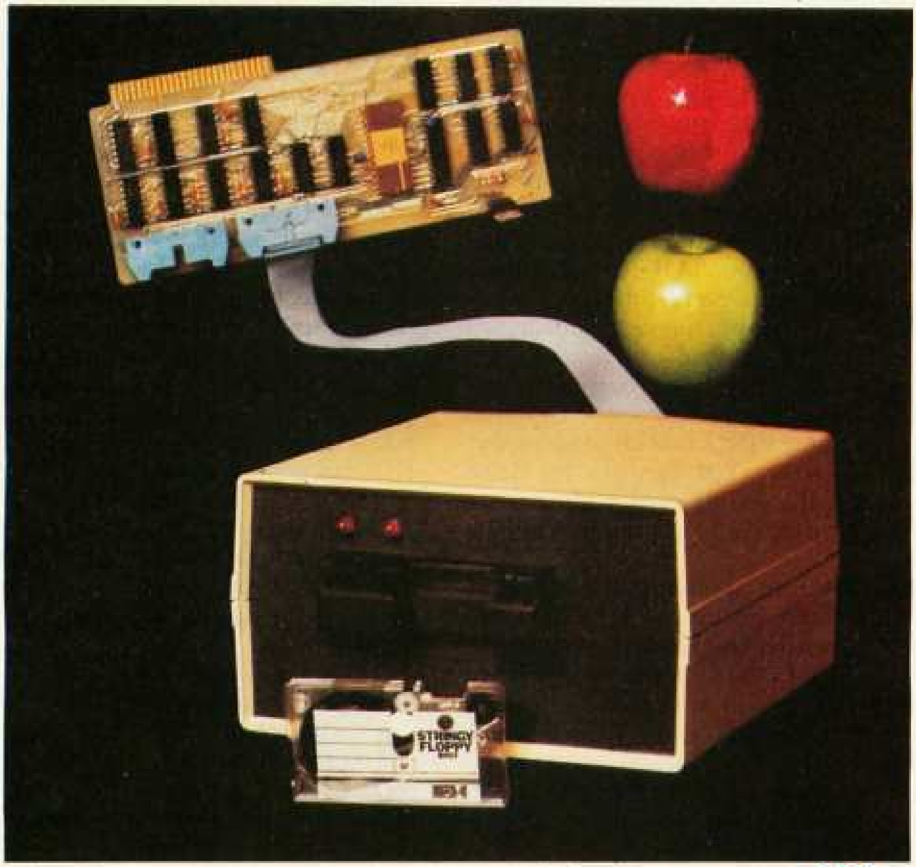

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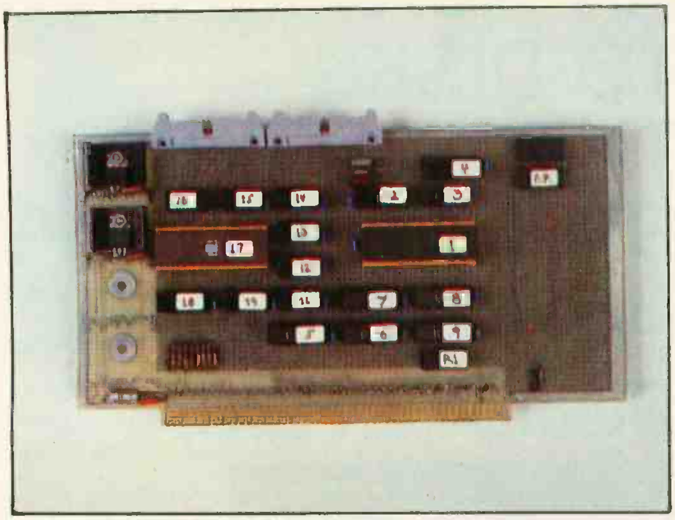
Circle 50 on inquiry card.

1a



1b

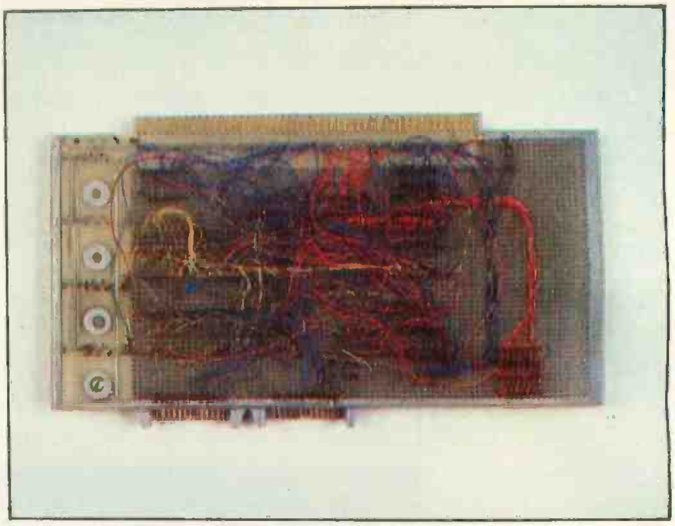


Photo 1: *The processor board from front (photo 1a) and back (photo 1b). There is a large area left for design additions. Note that upper pins on dual-in-line connectors are soldered to the ground plane for shielding. Multi-colored wiring makes debugging easier.*

facilitating soldering when necessary.

Probably the most important feature is that all the S-100 lines are labeled at the bottom of the board. Unless you enjoy doing a table-lookup every time you try to associate an S-100 signal with its pin number, get a board with the lines labeled.

Try to use a wire-wrap tool with daisy-chaining capability. This will allow you to connect common signals (like ALE, RD*, and WR*) quickly and easily, with less possibility for error. You can use the same technique for connecting the multiplexed address/data bus of the 8088 (AD0 thru AD7) to all the bus buffers (IC7, IC8, and IC9).

Be careful, though, because connect-and-wrap tools sometimes forget the connect operation. Whenever the wiring of one signal is complete, check each connection in the chain. It is easier to find a bad connection this way than by waiting until you are done. If you need more convincing, simply look at photo 1b and imagine hunting in that jungle of wires.

Important precaution: once you have wired the board, *test the power supply before you plug in any integrated circuits!* Measure the resistance between pins 1 and 51 (+8 V) and pins 50 and 100 (ground). If there is zero resistance, find the short before continuing. Make sure that the +5 V regulators are regulating, then check the power and ground pins of every socket for the correct value. Use the proper technique when handling MOS (metal-oxide semiconductor) devices. If you ruin an 8088, you will be sad.

The Board

On the left border of the board is the power-supply section. (See photo 1a.) At the bottom are a couple of capacitors (15 pF and 0.1 μF, both rated at 12 V) that filter the +8 V power supply from the system (this comes onboard via pins 1 and 51). At the top are two 7805 voltage regulators (+5 V) with heat sinks. Each uses a 0.1 μF bypass capacitor between the +5 V regulator outputs and ground (note: S-100 ground is pins 50 and 100). At the top center of the board, we see two 25-pin flat cable connectors. These are used as I/O-port connections to both parallel I/O ports (ports A and B) on the 8755A-2 EPROM-I/O circuit. Both ports could be wired to one connector, but I chose to shield each I/O line with a ground line. I did this by soldering the top row of connector pins to the ground plane, which runs around the circumference of the board.

Lower on the board, the 40-pin 8755A-2 (in the package labeled 17) is surrounded by eight dual-in-line packages. IC18 (labeled 18) is the 8185-2 static programmable memory. The other seven circuits complete the TTL circuitry required for this board. The schematic reveals that TTL devices are used for two basic functions. One is to decode the addresses for the on-board memory and I/O (ie: the 8755A-2, 8185-2 pair). The second is for the miscellaneous inversion and simple gating of signals necessary to successfully interface the processor card to the S-100 bus.

At the bottom are nine 1 k-ohm resistors used to pull up various processor input control-bus signals (the bus-disable inputs, RDY, HOLD*, etc).

To the right are IC6 thru IC9. These are all 8282s that serve to buffer the address bus, the input and output data buses, and the control bus. Immediately below IC9 is a resistor pack (labeled R1, containing eight 1 k-ohm resistors) used to pull up the input data bus of the processor. Remember that some I/O boards may have open-collector drivers (per the IEEE standard); thus, these pull-ups are necessary.

Higher on the board, IC1 is the 8088 microprocessor. Above the 8088, are IC2, IC3, IC4, a capacitor, two crystals, and a jumper. IC4 is the 8283 (inverting 8282) buffer for the status bus. IC3 is the 8205 1-of-8 decoder used to decode the processor status. IC2 is the 8284 clock generator. The capacitor (10 pF) is used between the crystal input and pin X2 of the 8284.

Why two crystals? While the 8088 is impressive at 5 MHz, faster is better, right? Ignoring manufacturer's specs is a "do at your own risk" proposition, but when I saw the 18.432 MHz crystal lying in my junk box, I could not resist. Under normal operating conditions, my 8088 has no problems running at 6.1 MHz (remember, the 8284 divides the crystal frequency by 3 to get the operating frequency of the 8088). The jumper selects between the 15 and 18.432 MHz crystals.

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Circle 51 on inquiry card.

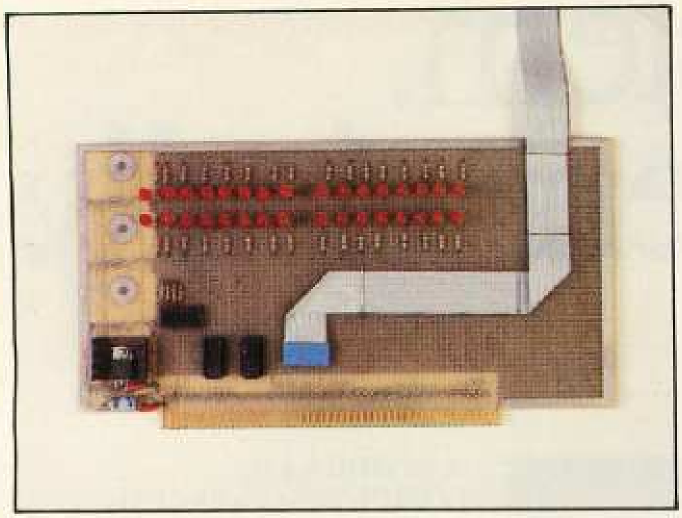

Photo 2: *Circuit board for the front panel. This board contains the LED assemblies (see figure 5) that monitor the states of selected lines on the S-100 bus.*

Photo 3: *Assembled front panel for the 8088-based computer. Two toggle switches and a push-button switch have been added to the LED assemblies shown in photo 2.*

At the bottom right is the resistor/capacitor timing network (47 k-ohm, 1 μF) connected to the RESET* input (pin 75).

Finally, at the upper right (above the package marked FP) is the dual-in-line socket for connecting the data bus of the processor to the front panel.

The Front Panel

"And now I see with eye serene
The very pulse of the machine"
William Wordsworth

As I said before, I am trying to avoid experimenting with my IMSAI. The IMSAI front panel will not work with my 8088 board, and it provides more functionality than I really need; therefore, I decided to build my own front panel (see figure 5).

The front-panel switches allow the system to be reset and allow the processor to be placed in run, stop, or single-step mode. It also allows monitoring of the address bus, the data bus, and the status bus. These few functions, in conjunction with a logic probe, are all that are needed for debugging the system.

Looking at photo 3 and figure 5 (on page 84), you can see that the front panel is really very simple. Additional controls and LEDs can be added to suit your own needs. One function I plan to add is a slow-step control, utilizing a simple timer (555-based) and the existing single-step circuitry. If you decide to use the upper four address bits, LEDs can be added to monitor them and other status and control lines.

Looking at the left-hand portion of the front-panel card in photo 2, we see the 7805 +5 V regulator and its filtering capacitors. This is used to power the 7400 and 7474, which implement the run/stop and single-step circuitry. Above this are the thirty-two LEDs that are tied to the appropriate S-100 bus lines through 4.7 k-ohm current-limiting resistors. The socket at the lower left is used to connect to the front-panel run/stop and single-step switches via a dual-in-line plug, allowing easy removal of the panel if necessary. The ribbon cable running across, then off, the board connects to the dual-in-line socket on the processor card, allowing the 8088 data bus to be monitored.

Connecting the 8088 RDY input and TEST* input on the processor card results in a simple, yet powerful, debugging feature. By placing a WAIT instruction in a program, full-speed execution of the program can be stopped. Then a specific routine can be single-stepped through, if necessary, for debugging purposes.

The TEST* input is a very powerful tool. A variation of the above strategy would be to add a switch to the front panel dedicated to controlling the TEST* input. This would allow WAIT instructions to be selectively ignored. However, the automatic stopping feature might then require some agile manipulation of the TEST* switch at the appropriate time.

Check out the front panel as thoroughly as possible. Ensure that all the LEDs work, and verify that the run/stop and single-step switches exercise the S-100 XRDY line correctly.

Debugging the Front Panel

Initially, install only the processor board and the front panel in your motherboard. This will minimize the number of variables to deal with at one time.

Place the run/stop switch in the stop position and apply power. Hit the reset switch; at this point, the lights on the front panel should reflect the following:

- The address bus should show hexadecimal 0FFF0.
- The status bus should show sM1 and sMEMR.

Note that in my case, I am using the SSTACK light to show run/stop status (stopped = LED on) so SSTACK is also lit.

The state of the data-bus LEDs depends on the program in your 8755A-2 EPROM. At this point, the 8088 is reading the hexadecimal address 0FFF0, which is in the on-board 8755A-2 EPROM. If your EPROM is erased, the data bus display will be hexadecimal 0FF, which is not very helpful. For instance, if the EPROM address/chip-select circuitry is incorrect, you may well see hexadecimal

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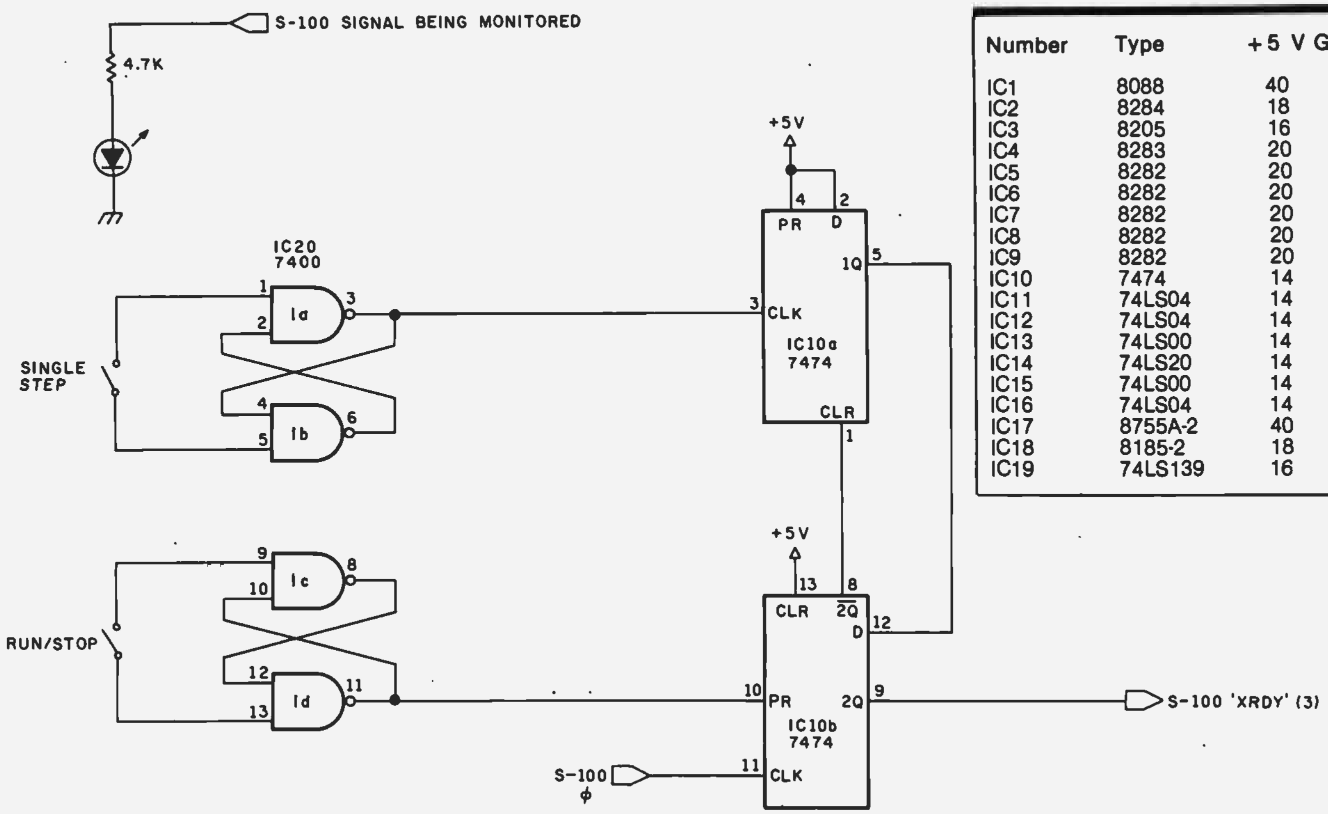

Number	Type	+5 V	GND
IC1	8088	40	1
IC2	8284	18	9
IC3	8205	16	8
IC4	8283	20	10
IC5	8282	20	10
IC6	8282	20	10
IC7	8282	20	10
IC8	8282	20	10
IC9	8282	20	10
IC10	7474	14	7
IC11	74LS04	14	7
IC12	74LS04	14	7
IC13	74LS00	14	7
IC14	74LS20	14	7
IC15	74LS00	14	7
IC16	74LS04	14	7
IC17	8755A-2	40	20
IC18	8185-2	18	9
IC19	74LS139	16	8

Figure 5: *The front panel design is simple and requires little in the way of hardware. The utilitarian controls can be augmented if necessary, but the functions shown are almost universally accepted as the only ones needed for basic debugging. The author connects one of the LED assemblies to each of the S-100 bus lines being monitored. Power connections for the integrated circuits are given in table 1.*

OFF anyway, due to the pull-up resistors on the data bus.

I suggest that for initial testing you have the 8755A-2 EPROM burned with a short diagnostic program that exercises some of the functions of the processor board. This program should allow testing of the on-board programmable memory and I/O ports. By single-stepping, each function can be tested. You may want to add instructions to test the S-100-interface portion of the design (such as moving data from and to external memory, and data transfer to and from external I/O ports).

If what your front panel displays is only slightly different from this description, there cannot be much wrong. For instance, if the address bus shows hexadecimal 0FFE8, you can suspect that address lines 3 and 4 have been swapped on the processor board or the front panel. If the display shows hexadecimal 0FFF8, look for a short between the same address lines, etc. In fact, if you have a problem at this point, a good strategy is to verify that the front panel is correctly monitoring the processor. With the processor stopped and reset, insure that the outputs of the address, data, and status bus buffers on the processor board are correctly reflected on the front panel. If they are not, the front panel still has problems. Fix these before continuing.

If the front panel is correctly interpreting the outputs of the processor board, and your LED display is still incorrect, the problem lies on the processor board itself.

Debugging the Processor Board

When a new hardware design fails to work, the problem usually lies in one of three areas:

- design errors,
- wiring errors, or
- component failure.

Note that this is closely related to the system environment in which the processor board is operating. In particular, I have given interrupt handling and DMA handshaking only cursory examination since none of the boards I use exercise these functions. The addition of your favorite Brand XYZ interrupt-driven DMA Video Board may uncover design errors I am not aware of. (I would appreciate correspondence in this matter.)

Wiring errors are the most likely culprit. Checking connections as you go can prevent a lot of these. Sometimes, the problem is a bad component. Fortunately, these problems usually produce distinct, easy-to-diagnose symptoms.

The strategy now is to start with the basic computer (8284, 8088, 8755A-2, and 8185-2) and work outwards until all problems are corrected.

Start by checking for fundamental signs of life. At the 8284, look for the presence of the 15 MHz crystal signal on the X1 and X2 inputs. Ensure that the 5 MHz clock signal is present on the CLK output of the 8284. The RESET switch should pull the 8284 RES* input low for at least 1 μs, and it should produce a high-going pulse on the RESET output of the 8284. The RDY2 input and READY output of the 8284 should correctly reflect the state of the front panel run/stop and single-step switches.

Moving to the 8088, first verify that the CLK, READY, and RESET outputs of the 8284 are getting to the CLK, READY, and RESET inputs of the 8088. If not, find the wiring error. The HOLD, INTR, and NMI inputs should all be low. The MN/MX* input should be tied high.

With the 8088 reset and running, look for activity on the ALE line of the 8088; address lines; data lines, and status and control lines should all show basic signs of life.

Once things are operating properly, stop and reset the system and probe the output buses of the 8088 with a logic probe. The sixteen address outputs should reflect the hexadecimal 0FFF0 RESET start address, and the status lines (IO/M*, DT/R* and SSO*) should correspond to op-code-fetch status. Make sure that the correct status output at the decoder (IC3) results from the three status inputs.

Next, make sure that the outputs of the 8088 are getting to the appropriate output buffers. For example, the inputs to 8282 IC6 (pins 1 thru 8) should be the same as the A8 thru A15 outputs of the 8088, and so forth for the other output buses. If not, find the wiring error. The outputs of all the buffers should reflect the inputs. If not, suspect a bad buffer or faulty STB (strobe) or OE* (output-enable) connections.

Wiring errors are the most likely culprits in a project such as this. TTL circuits are easy to debug. Swapping components and looking for resulting symptomatic changes is a useful debugging technique. You probably have extra TTL circuits available, and the five 8282s can be swapped. As a last resort, the MOS chips can be swapped. Try to borrow an 8088 and an 8284 to swap; the 8755A-2 and 8185-2 are not necessary for initial debugging. The risk is that a wiring error can damage

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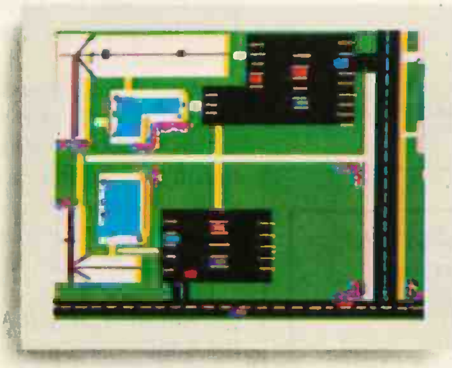

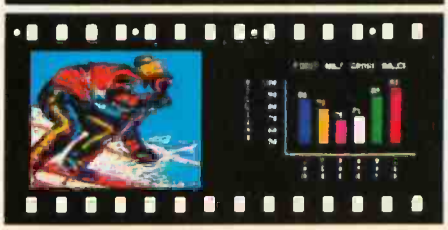

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these circuits.

Once the processor and front-panel boards are operating, you can begin integrating and testing other boards. Insert one board at a time and try to verify its operation before continuing.

Hints

Watch out for I/O boards that use the upper eight address lines to enable the board; my SSM parallel I/O board does this. The problem can be corrected by software, as an example will show:

> The 8088 has two forms of input instructions. One is much like the 8080A IN instruction (the same holds for output). Its form is
>
> IN Accumulator, 8-bit port address
>
> The second form is an indirect input instruction that allows access to the extended I/O addressing of the 8088 (ie: 64 K port addresses).
>
> MOV DX register pair, 16-bit port address
> IN Accumulator, DX (port address is in DX register pair)
>
> The first form of input instruction zeroes out the upper eight address bits. For example:
>
> IN A, 60H
>
> will place hexadecimal 0060 on the sixteen address lines.
>
> Now assume there are two I/O boards in the system. One decodes the lower eight address lines and is addressed at hexadecimal 60. The other (like the SSM parallel I/O board) decodes the upper eight address lines and is addressed at 0.
>
> The problem occurs if we try to use the short form of the input instruction to read from the I/O board addressed at hexadecimal 60 with the instruction:
>
> IN A, 60H
>
> The address bus will contain hexadecimal 0060 (ie: binary 0000 0000 0110 0000). Now the board at hexadecimal address 60 will correctly decode the lower eight address lines and select itself. Unfortunately, the other board (addressed at 0) will see the high-order part of the address and select itself. The result is that both boards will try to drive the data bus at the same time...bus contention being the result.
>
> The solution is to use the indirect form of I/O. To read from port hexadecimal 60, use:
>
> MOV DX, 6060H
> IN AL, DX

If you are sure you will never want to use an I/O board that decodes the upper eight address lines, the short form I/O instructions are valid; otherwise, use the indirect form of I/O.

Once the 8088 processor board is solidly up and talking with all the other boards via the S-100 bus, there are still a few problems to be considered. All that hardware is nothing more than a "wall socket tester" without the software to make it do something. As in the case of large mainframes, the hardware advances are progressing far more rapidly than our ability to generate useful software.

Next month, in the third and final part of this article, we will look at MON88, a machine-language monitor for the 8088-based processor board described here. ■

Editor's Note: *The author is planning to make printed circuit boards available through Microfuture, POB 5951, San Jose CA 95150. The boards will use more common 2708 read-only memory circuits in place of the 8755, and 2114 programmable memory instead of the 8185. Twenty address lines are implemented per the IEEE standard. Price is expected to be $59.95; Microfuture can be contacted at (408) 249-0560.*

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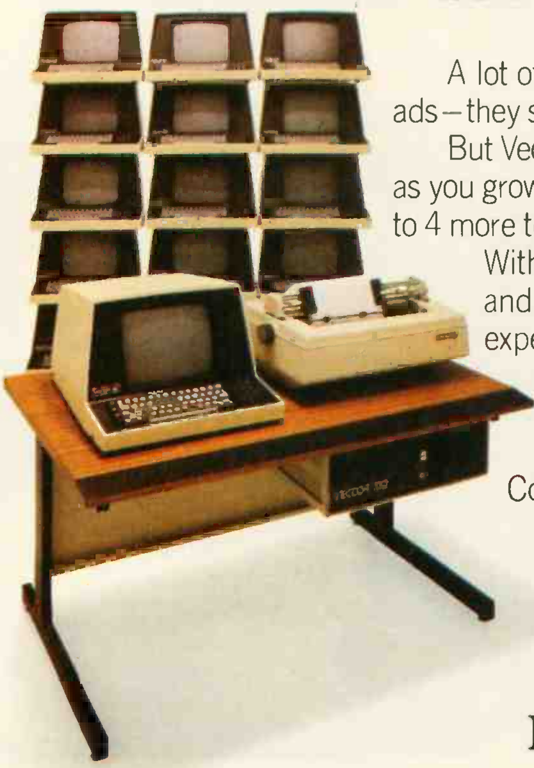

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A Multiple-Machine Loader for Classroom Computers

Richard C Hallgren, Assistant Professor, Michigan State University, Department of Biomechanics, East Lansing MI 48824

Many educators are becoming aware of the impact that personal computers can have by providing a learning experience, and the combined factors of decreasing cost and increasing capability are prompting many school systems to include the personal computer in their curriculum. Ideally, each instructional system should have its own floppy-disk drive, but the present cost of drives can inflate the cost of an individual system by 50%. The alternative is to supply every system with a low-cost cassette recorder. Unfortunately, the most frustrating phase of computer operation can be associated with reading a tape into a computer from a cassette recorder. The problem is greatly magnified when the cassette recorder being used to load the program tape is not the recorder that was used to create the program tape. The problem becomes unmanageable when twenty students are attempting to load twenty tapes from twenty cassette recorders.

Acknowledgment

This project was supported by Independent School District #196 in Rosemount, Minnesota.

A simple solution is to build an interface which will load a program into a number of peripheral computers from a single source. Figure 1 shows the basic approach. The instructor has a system with a floppy disk containing all the instructional programs to be used; all the students' computers are connected in parallel to a two-conductor shielded cable coming from the interface. The instructor first loads the desired program into his computer from the disk, and then the program is transferred over the cable to the students' computers. Three specific examples of the interface will be described, but the concept can be extended to almost any personal computer system.

Multiple-machine loading transfers the program data by connecting the cassette-output port on the instructor's computer to the cassette-input port on the students' computers, through the interface circuitry. The interface matches the respective impedances and provides the necessary signal conditioning.

Photo 1: *The multiple-machine loader in use at a school administrators' workshop, where computer-aided instruction programs were being evaluated. This network-like system can involve up to twenty-four TRS-80s, Apple IIs, or Commodore PETs.*

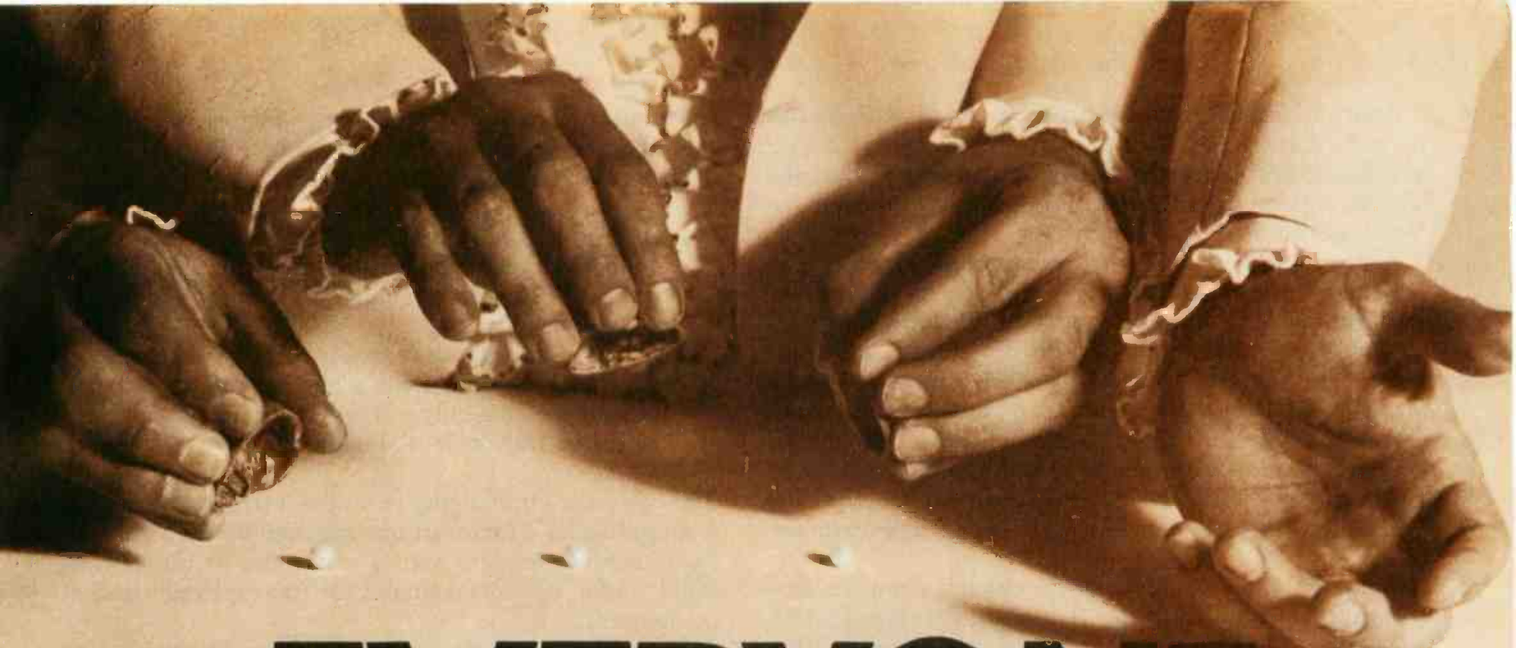

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Figure 2a shows the waveform from the cassette-output port of a Radio Shack TRS-80 after the user types CSAVE and Enter, and figure 2d shows the waveform that the TRS-80 expects to see at the cassette input port after the user types CLOAD and Enter.

Figure 3a is a diagram of the interface circuitry. The cassette-output signal from connector J3-5 on the instructor's computer is buffered and amplified by the RCA CA3140T operational amplifier to drive the power transistor. The signal from the MJE 3055 transistor is connected to J3-4 on the students' computers and provides drive capability for twenty-four units. Power for the interface is obtained from the +19.8 V output of a TRS-80 AC adapter. The LM340 regulator is set via the 1.2 k-ohm and 560-ohm resistors to supply approximately 9.5 V.

Figure 2b shows the waveform coming from the cassette-output port of an Apple II after the user types SAVE and Return, and figure 2e shows the waveform that the Apple II would like to see at the cassette-input port after typing LOAD and Return. Figure 3b shows a diagram of the interface circuitry. There are two factors which make the interface design easier for the Apple II than for the TRS-80:

- The Apple II has eight peripheral connectors on the computer's motherboard, thus allowing the interface to reside inside the computer and use the computer's 5 V power supply.
- The input impedance of the Apple II cassette circuitry is high (12 k-ohm). Even a number of computers in parallel presents only a small load; thus the need for the driver transistor is eliminated.

The cassette-output signal from the instructor's Apple II is amplified by a factor of one hundred by the CA3140T operational amplifier, and is connected to the cassette input jacks on a maximum of twenty-four student computers.

Figure 2c shows the waveform from cassette-output port number 2 of a Commodore PET computer after the user types SAVE "NAME", 2 and Return. Figure 2f shows

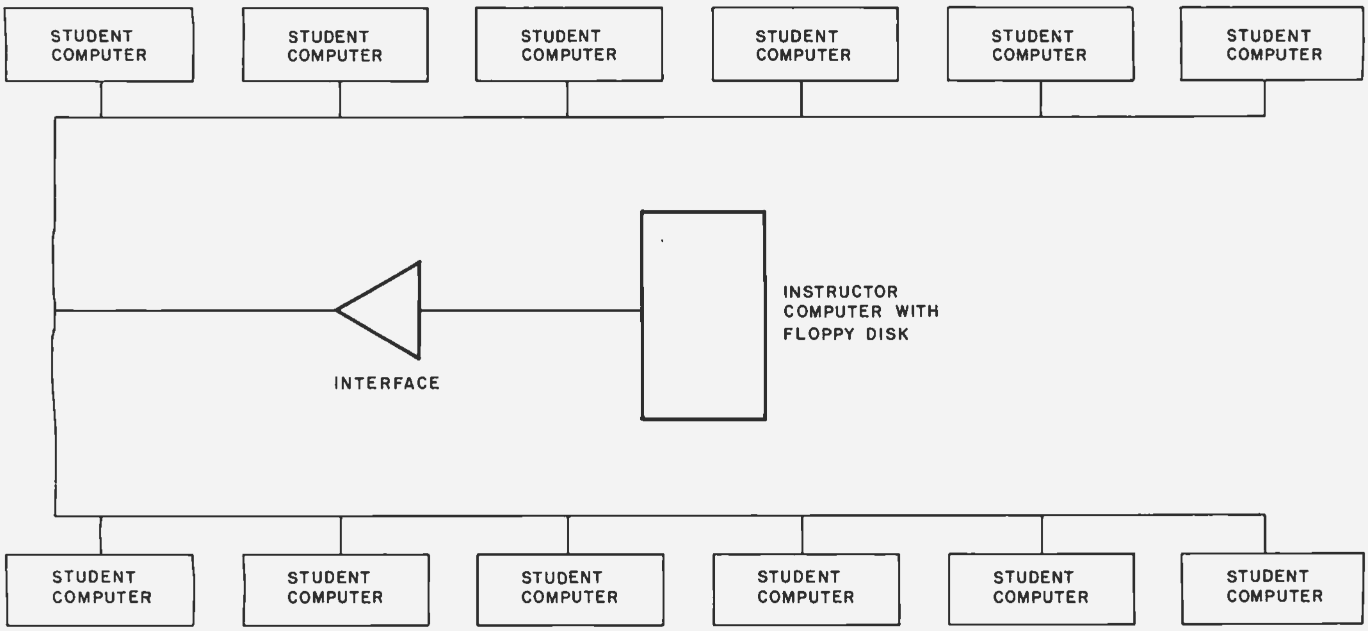

Figure 1: *Block diagram of a multiple-machine loader system. The network is composed of an instructor's computer, a cable-driver interface, and up to twenty-four student computers.*

the waveform form that the PET would like to see at cassette-input port number 2 after typing a LOAD "NAME",2 and Return. Figure 3c shows the diagram of the interface circuitry. Cassette-interface connector number 2 on the back of the PET is used to gain access to input and output lines. The single integrated circuit is mounted in the connector hood at the instructor's machine so as to make the installation as simple as is possible.

Operation of each system is quite simple:

1. The instructor loads the desired program from disk into his computer.
2. All students that are to use this particular program are instructed to type CLOAD and Enter (LOAD and Return for the Apple II; LOAD "NAME",2 and Return for the PET) as if they were loading a program from cassette tape. Their computers will now wait for a program to be loaded.
3. The instructor types CSAVE and Enter (SAVE and Return for the Apple II; SAVE "NAME",2 and Return for the PET) as if a program were being saved on cassette tape.
4. The program is automatically transferred from the instructor's computer to the students' computers.
5. After the program is transferred, control of the computer is returned to the students.

Results from using the interfaces described have been quite encouraging. Not only have the problems of loading programs from twenty different cassette recorders been eliminated, but the process of generating twenty program tapes containing material updates has also been avoided. ■

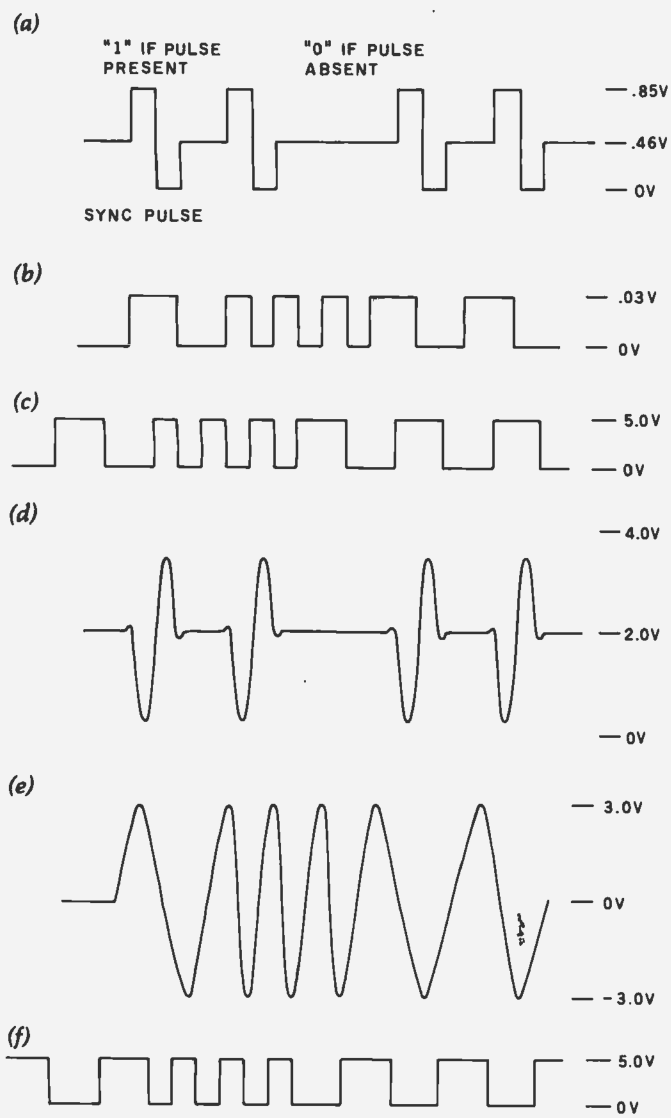

Figure 2: *Cassette-interface output of the Radio Shack TRS-80 Model I (a), Apple II (b), and Commodore PET (c). The respective cassette-interface inputs expect to receive the waveforms of d, e, and f. Different specimens of these computers may produce slightly different waveforms from those shown here.*

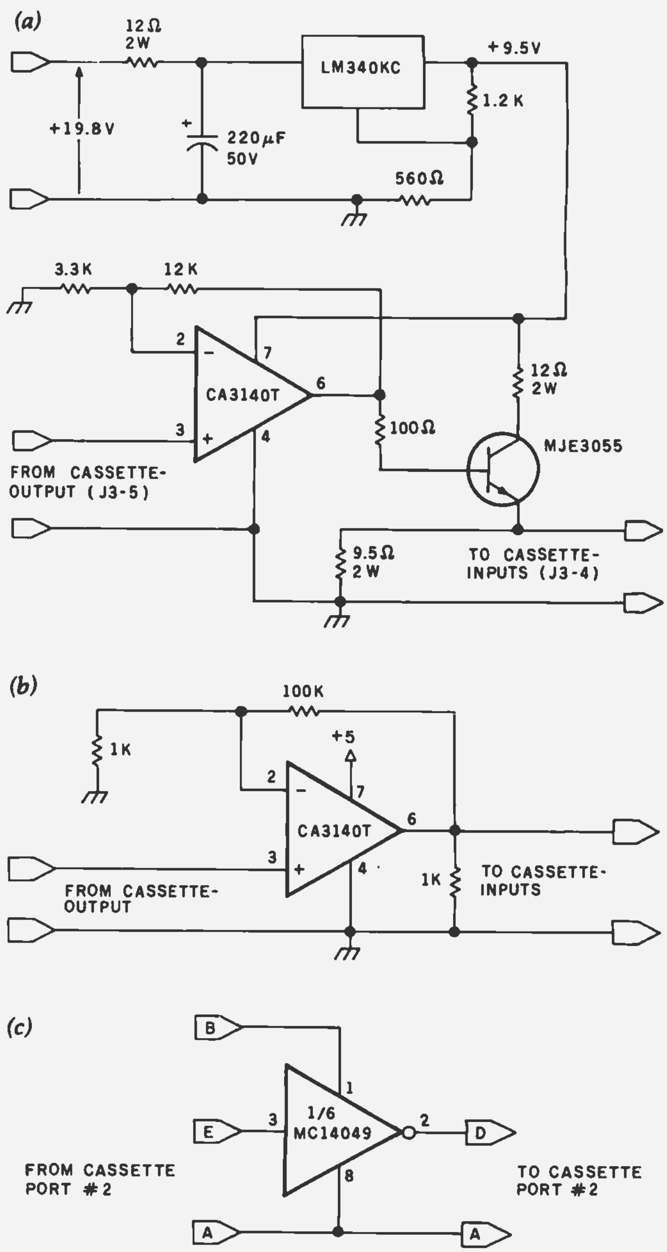

Figure 3: *The various interfacing circuits necessary are shown at a, b, and c. The low input impedance of the TRS-80 (a) presents the greatest load, and so requires a power transistor to achieve the proper drive. The interface circuit for the Apple II (b) requires much less power, and so it can use the power supply in the instructor's computer, as can the PET interface (c).*


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Sorting with Binary Trees

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University of Oklahoma
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202 W Boyd
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Of the numerous sorting techniques know to the average computer user, one that is seldom talked about is the *binary sort*. This is probably because, at first glance, it seems unnecessarily complicated when compared to, say, the common *bubble sort*. (The bubble sort is so-called because a new element reaching its proper position in a sorted list does so by being compared successively with each element already in the list, rising like a bubble from the bottom of the list.) Nonetheless, I was curious enough about the binary sort to compare it to the more common bubble sort in a practical demonstration. The results were interesting enough to warrant further study. First, let me describe the experiment.

The program of listing 1 (with line 5 deleted) was used to implement a binary sort on an 8 K Commodore PET. Timing comparisons were made, using the PET's internal real-time clock, for both this program and a bubble-sort program (not listed in this article), both of which were instructed to sort a random list of 100 integers. The binary sort took approximately half as long as the bubble sort to order the random list of numbers. However, the real payoff came when the computer was told to either add to or delete from the list, *and then* print the new sorted list. The bubble sort took the same amount of time it took to do its first sort, but the binary sort was finished before the display had time to record the fact.

It is on this seemingly amazing note that we begin a discussion of binary sorts.

Figures 1 and 2 are examples of what are called *trees*. They are extremely useful in several branches of mathematics and figure largely in the construction of a binary search. Trees are made of *nodes* (the circles in figures 1 and 2), each of which usually contains information. The single node in the top row is called the *root*. A given node can be connected to one or more nodes on the next level below it; if this is the case, the higher node is called the *parent node* (or parent), and the lower nodes directly connected to it are called its *children*.

For years, mathematicians have known many properties of tree diagrams. Most of these properties

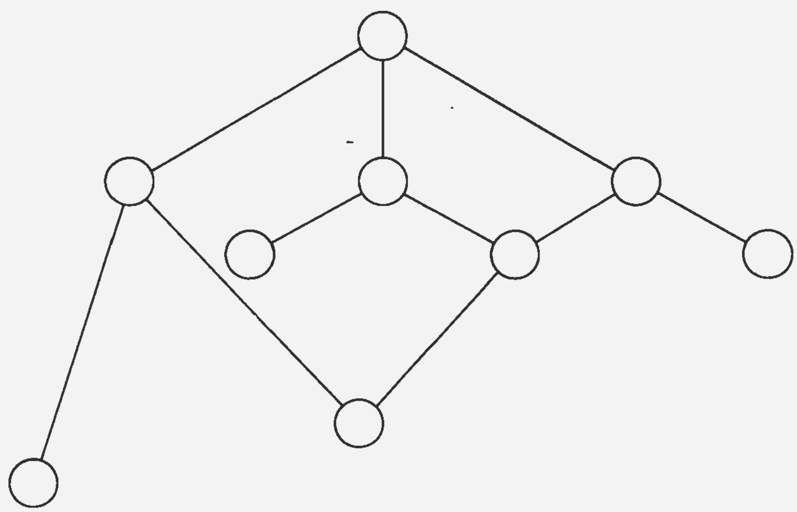

Figure 1: *A generalized tree. A tree is characterized by having only one root node (the one at the top) and by each node (represented here as a circle) having zero or more nodes connected to it by a straight line. The nodes below the given node connected directly by one line segment are called child nodes; the node itself is called the parent node.*

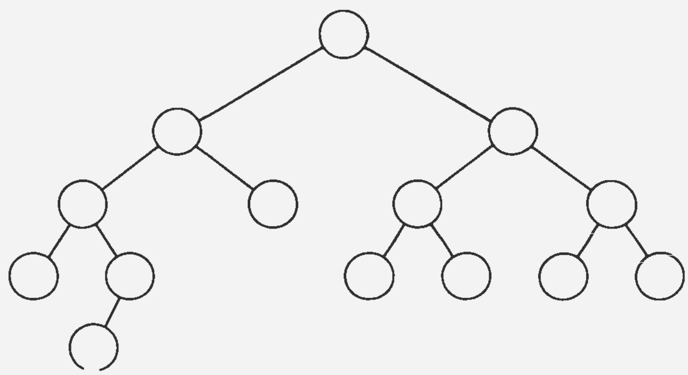

Figure 2: *A binary tree. This tree is characterized by the properties that a given parent node can have, at most, two child nodes, and that each non-root node has exactly one parent. The child nodes are called the left child node and the right child node.*

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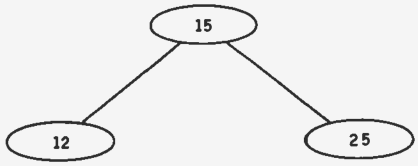


Figure 3: *A simple binary tree. Data is arranged within a binary tree so that the sequence right child, parent, left child gives the contents of the tree in sorted order. Here, the sorted order is 12, 15, 25.*

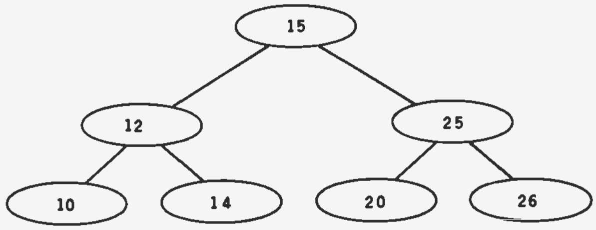


Figure 5: *Example of a binary tree. Here, more nodes have been added, giving the sequence 10, 12, 14, 15, 20, 25, 26.*

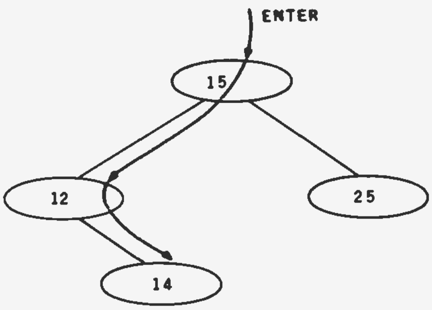
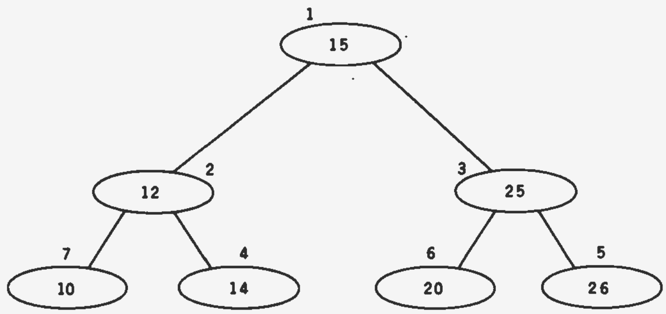


Figure 4: *Adding to a binary tree. The colored arrow shows the direction of search when placing a new node in a binary tree. Here, 14 is greater than 12, so it is placed as a right child of 12. Here, the sorted order is 12, 14, 15, 25.*

6a



6b

NODE	KEY	LEFT POINTER	RIGHT POINTER
1 (ROOT)	15	NODE 2 (12)	NODE 3 (25)
2	12	NODE 7 (10)	NODE 4 (14)
3	25	NODE 6 (20)	NODE 5 (26)
4	14	NIL	NIL
5	26	NIL	NIL
6	20	NIL	NIL
7	10	NIL	NIL

Figure 6: *Example of a binary tree. Here (6a), the binary tree of figure 5 is reproduced with numbers above each node that give the order in which the nodes were added to the tree. The table below (6b) gives the node number, key, left pointer, and right pointer of each node; both pointers refer to the node number of a node, not its key value. The word NIL indicates there is no node in the direction given by the pointer.*

are complex or so general as to be of little practical use. But if we restrict ourselves to a specific subset of trees with a given structure, these properties become readily understandable and usable. Figure 1 shows a general tree; figure 2 is an example of the type of tree that we will be studying, a *binary tree*.

A binary tree is characterized by the restriction that each parent node can have, at most, two children, and that any node (except for the root node) must have exactly one parent node. Later we will see that this kind of tree is well suited to representation in a digital computer, where the binary nature of decisions (answered with yes or no) goes hand in hand with the maximum of two child nodes allowed each parent node.

How does this structure enable us to perform searches and sorts? If we define *less than* as meaning *to the left and down* and *greater than* as meaning *to the right and down*, this gives us an ordering that can be used to store members of a sorted list as nodes of a binary tree.

Suppose we start with three numbers: 15, 12, and 25. Since 15 is the first number encountered, we will designate it as the root of our tree. Since 12 is the next number in the list, we attach it below and to the left of the root node (12 is less than 15). Since the next number, 25, is greater than the root, 15, we attach it below and to the right of the root. This gives us the binary tree in figure 3.

Now let us add a new number to the list: 14. We can add this to the existing binary tree as follows: start at the root node, 15, and move to the left because the node we want to insert, 14, is less than 15. At the node numbered 12, we compare 12 to 14 and conclude that we should go to the right. Since no node exists to the right of 12, we can place a new node there with the value of the number to be added, giving us the binary graph in figure 4. Similarly, we can add the numbers 26, 20, and 10 to our tree, giving us the tree in figure 5.

Given the tree in figure 5 as a "sorted" tree, this implies that there is some procedure that allows us to extract the sorted list of numbers from the "sorted" binary tree.

If we were presented with the diagram of figure 3 and asked to read it in proper order, we would do so by first reading the leftmost node, then the parent, then the rightmost node. We note that the far more complicated trees of figure 4 and figure 5 can be read in a similar fashion by

Text continued on page 102

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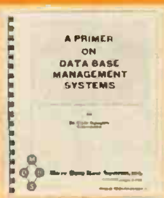
- System specific manual for bringing up our software



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Listing 1: *BASIC program for sorting a threaded binary tree. This program allows the user to create, add to, delete from, and list a binary tree. The tree is threaded in that it is possible to print the tree sorted in ascending key sequence by using the pointers associated with each node. This version is written in Microsoft BASIC and currently runs on an Apple II. With the deletion of line 5, it has also been run on the Commodore PET, the Radio Shack TRS-80, and a PDP-10. It should also run without modification on any other computer using Microsoft BASIC.*

```
  5 CALL -936
 10 DIM KEY(125),RLINK(125),LLINK(
    125)
 12 FALSE=0:TRUE=1:N=0:ROOT=1:NIL=
    0
 14 EMPTY=FALSE
 16 PRINT "THIS PROGRAM GENERATES 10
    0 RANDOM NUMBERS AND SORTS THEM
    USING"
 18 PRINT "A BINARY SEARCH TREE.  IT
     ALSO ALLOWS DELETIONS FROM, OR
    ADDITIONS"
 20 PRINT "TO THE TREE."
 22 REM  ** GENERATE DATA **
 24 FOR N=1 TO 100
 26 KEY(N)= RND (100)
 27 LLINK(N)=NIL
 28 RLINK(N)=NIL
 29 Q=N
 30 GOSUB 580
 32 NEXT N
 34 PRINT : PRINT "ELEMENTS AS THEY
    WERE GENERATED ARE :": PRINT

 36 FOR I=1 TO 100: PRINT KEY(I)
    ,: NEXT I
 38 PRINT
100 PRINT : PRINT "DO YOU WANT TO:"

110 PRINT "  1.   ADD A NODE"
120 PRINT "  2.   DELETE A NODE"

130 PRINT "  3.   LIST THE TREE"

132 PRINT "  4.   END"
140 INPUT X
150 IF X=1 THEN 160
151 IF X=2 THEN 200
152 IF X=3 THEN 300
153 IF X=4 THEN 9999
154 GOTO 100
160 N=N+1
162 IF EMPTY THEN 164
163 GOTO 170
164 FOR I=1 TO N
165 LLINK(I)=NIL
166 RLINK(I)=NIL
167 NEXT I
168 N=1
169 ROOT=1
170 INPUT "GIVE KEY ",KEY(N)
175 Q=N
180 GOSUB 580
190 GOTO 100
200 INPUT "GIVE KEY TO BE DELETED "
    ,P
205 ALPHA=P
210 GOSUB 1390
212 P=SEARCH
220 GOSUB 3000
230 GOTO 100
300 PRINT : PRINT "TREE FOLLOWS:"
    : PRINT
310 GOSUB 980
320 GOTO 100
580 REM  ** SUBROUTINE BILDER **
582 EMPTY=FALSE
600 IF N=1 THEN 830
630 P=ROOT
640 INSERT=FALSE
650 IF KEY(Q)<=KEY(P) THEN 740
660 IF RLINK(P)<=NIL THEN 690
670 P=RLINK(P)
680 GOTO 810
690 RLINK(Q)=RLINK(P)
700 RLINK(P)=Q
710 LLINK(Q)=NIL
720 INSERT=TRUE
730 GOTO 810
740 IF LLINK(P)<>NIL THEN 800
750 LLINK(P)=Q
760 LLINK(Q)=NIL
770 RLINK(Q)=-P
780 INSERT=TRUE
790 GOTO 810
800 P=LLINK(P)
810 IF INSERT=FALSE THEN 650
830 RETURN
850 REM  ** SUBROUTINE FIX **
890 I=1
900 IF I<=N THEN 920
910 GOTO 960
920 LLINK(I)=NIL
921 RLINK(I)=NIL
940 I=I+1
950 GOTO 900
960 RETURN
980 REM  ** SUBROUTINE LIST **
1000 PRINT
1020 IF EMPTY=FALSE THEN 1030
1022 PRINT "TREE EMPTY"
1023 GOTO 1220
1030 RET=FALSE
1040 R=ROOT
1050 PRINT "ELEMENTS IN ORDER"
1070 IF LLINK(R)=NIL THEN 1115
1100 R=LLINK(R)
1110 GOTO 1070
1115 B=R
1120 IF ((RLINK(B)<>NIL) AND (RET=
     FALSE)) THEN 1140
1130 GOTO 1200
1140 PRINT KEY(B),
1145 P=B
1150 GOSUB 1240
1151 B=SUC
1160 IF B<>NIL THEN 1120
1170 RET=TRUE
1180 GOTO 1120
1200 IF RET THEN 1220
1210 PRINT KEY(B)
1220 RETURN
1240 REM  ** SUBROUTINE SUCCESSOR **
1280 Q=RLINK(P)
1290 IF RLINK(P)>NIL THEN 1320
1300 Q=-Q
1310 GOTO 1360
1320 IF LLINK(Q)=NIL THEN 1360
1340 Q=LLINK(Q)
1350 GOTO 1320
1360 SUC=Q
1370 RETURN
1390 REM  ** SUBROUTINE SEARCH **
1450 P=ROOT
1460 F1=FALSE
1470 IF ((P<>NIL) AND (F1=FALSE)
     ) THEN 1490
1480 GOTO 1600
1490 IF ALPHA=KEY(P) THEN 1580
1500 IF ALPHA<KEY(P) THEN 1560
1510 IF RLINK(P)<=NIL THEN 1540
1520 P=RLINK(P)
1530 GOTO 1470
1540 P=NIL
1550 GOTO 1470
1560 P=LLINK(P)
1570 GOTO 1470
1580 F1=TRUE
1590 GOTO 1470
1600 SEARCH=P
1610 RETURN
2480 REM  ** SUBROUTINE PAR **
2530 F1=FALSE
2540 R=ROOT
2550 IF P<>ROOT THEN 2560
2555 F1=TRUE:R=NIL
2560 IF ((LLINK(R)=P) OR (RLINK(
     R)=P) OR (F1=TRUE)) THEN 2630

2570 IF KEY(R)<KEY(P) THEN 2600
```

Listing 1 continued on page 102

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Listing 1 continued:

```
2580 R=LLINK(R)
2590 GOTO 2610
2600 R=RLINK(R)
2610 IF R=NIL THEN F1=TRUE
2620 GOTO 2560
2630 PAR=R
2640 REM
2650 RETURN
3000 REM  ** SUBROUTINE DEL **
3010 IF P=ROOT THEN GOTO 7000
3020 REM  CASE II
3030 GOSUB 2480
3035 Q=PAR
3040 IF LLINK(Q)=P THEN GOTO 6000

3050 REM  CASE II GROUP B
3060 IF RLINK(P)>NIL THEN GOTO 3200

3070 IF LLINK(P)<>NIL THEN GOTO
     3110
3080 REM  SUBCASE 1
3090 RLINK(Q)=NIL
3100 GOTO 9000
3110 REM  SUBCASE 3
3120 RLINK(Q)=LLINK(P)
3130 R=LLINK(P)
3140 IF RLINK(R)=-P THEN 3150
3145 R=RLINK(R)
3147 GOTO 3140
3150 RLINK(R)=RLINK(P)
3160 GOTO 9000
3200 IF LLINK(P)<>NIL THEN GOTO
     3240
3210 REM  SUBCASE 2
3220 RLINK(Q)=RLINK(P)
3230 GOTO 9000
3240 REM  SUBCASE 4
3250 RLINK(Q)=RLINK(P)
3260 R=RLINK(P)
3270 IF LLINK(R)=NIL THEN 3280
3275 R=LLINK(R)
3277 GOTO 3270
3280 LLINK(R)=LLINK(P)
3320 R1=LLINK(P)
3330 IF RLINK(R1)=-P THEN 3340
3335 R1=RLINK(R1)
3337 GOTO 3330
3340 RLINK(R1)=-R
3350 GOTO 9000
6000 REM  CASE II GROUP A
6010 IF RLINK(P)>NIL THEN GOTO 6150

6020 IF LLINK(P)<>NIL THEN GOTO
     6060
6030 REM  SUBCASE 1
6040 LLINK(Q)=NIL
6050 GOTO 9000
6060 REM  SUBCASE 3
6070 LLINK(Q)=LLINK(P)
6080 R=LLINK(P)
6090 IF RLINK(R)=-P THEN 6100
6095 R=RLINK(R)
6097 GOTO 6090
6100 RLINK(R)=-Q
6110 GOTO 9000
6150 IF LLINK(P)<>NIL THEN GOTO
     6190
6160 REM  SUBCASE 2
6170 LLINK(Q)=RLINK(P)
6180 GOTO 9000
6190 REM  SUBCASE 4
6200 LLINK(Q)=RLINK(P)
6210 R=RLINK(P)
6220 IF LLINK(R)=NIL THEN 6230
6225 R=LLINK(R)
6227 GOTO 6220
6230 LLINK(R)=LLINK(P)
6270 R1=LLINK(P)
6280 IF RLINK(R1)=-P THEN 6290
6285 R1=RLINK(R1)
6287 GOTO 6280
6290 RLINK(R1)=-R
6300 GOTO 9000
7000 REM  CASE I
7010 IF RLINK(P)>NIL THEN 7150
7020 IF LLINK(P)>NIL THEN 7070
7030 REM  SUBCASE A
7040 EMPTY=TRUE
7050 N=0
7060 GOTO 9000
7070 REM  SUBCASE C
7080 ROOT=LLINK(P)
7090 R=LLINK(P)
7100 IF RLINK(R)=-P THEN 7130
7110 R=RLINK(R)
7120 GOTO 7100
7130 RLINK(R)=NIL
7140 GOTO 9000
7150 IF LLINK(P)>NIL THEN 7190
7160 REM  SUBCASE B
7170 ROOT=RLINK(P)
7180 GOTO 9000
7190 REM  SUBCASE D
7200 ROOT=RLINK(P)
7210 R=ROOT
7220 IF LLINK(R)=NIL THEN 7250
7230 R=LLINK(R)
7240 GOTO 7220
7250 LLINK(R)=LLINK(P)
7260 R1=LLINK(P)
7270 IF RLINK(R1)=-P THEN 7300
7280 R1=RLINK(R1)
7290 GOTO 7270
7300 RLINK(R1)=-R
9000 RETURN
9999 END
```

Text continued from page 98:
first visiting the leftmost node in each branch, then moving to the parent, then to the rightmost node, then moving to the next group and repeating the sequence.

Unfortunately, such a description, while easy for people, is tough for computers, because computers lack the ability to observe spatial placement of nodes. It becomes necessary for us to provide the computer with a series of *pointers* that indicate the relationships between nodes. Each node is provided with two pointers, one of which points to the left child of the node, while the other points to the right child of the node.

In figure 6, we have listed the nodes (in the order encountered) and the left and right pointers of each parent node. Note the presence of the word "NIL" for the four children at the bottom of the branches. These represent pointers to possible future nodes that have not yet been added to the tree.

To properly pass through the computer representation of the tree, we have to supply it with the proper information as to the relationship of the nodes to each other. This can be done economically by assigning four numbers to each node, as shown in figure 7. The four numbers are the number of the node, the value or key of the node, and the left and right pointers to the node numbers (not to their keys).

Some explanation should be given of the values that can be assumed by the left and right pointers. The left pointer always points to either a node number (greater than zero) or zero (denoting the end of one "branch" of the tree in the leftward direction).

The right pointer can assume either positive or zero values with the same meanings as above. In addition, it can be negative; this is an *upward pointer* to the node that is the next node in the ascending key sequence. (The node with the upward pointer is the rightmost node of a left subtree; the node being pointed to is the parent node of this same left subtree.) An example of this in figure 7 is the upward pointer from node 4 to node 1; the upward pointer denotes that the subtree of nodes 2, 4, and 7 has been listed already.

The upward pointers in figures 7

Text continued on page 110

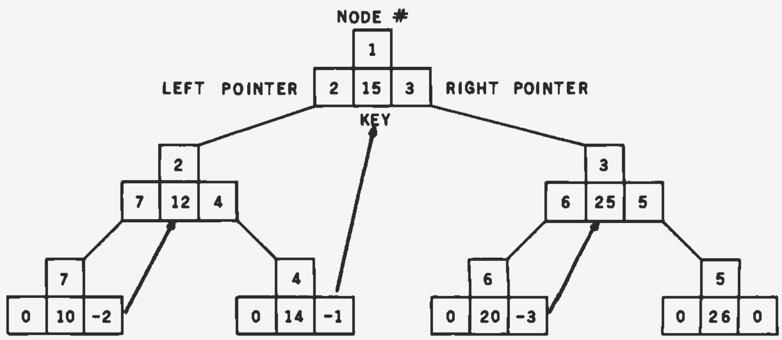

Figure 7: *Computer representation of a binary tree. In the BASIC program of listing 1, each node is represented by four numbers: the node number (given for purposes of illustration only), the key, and the right and left pointers. To "thread" the tree so that a thread of pointers runs through the nodes in their sorted-key order, a right pointer, when negative, points not to a right child node but to the ancestor node that follows the current node in the sorted sequence; these upward right pointers are drawn in color.*

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Listing 2: *Running the program of listing 1. In this listing, a hundred random numbers are generated, used to create a binary tree, and listed in sorted key sequence. The node containing key value of 8 is deleted, a node with key value of 39 is added, and the tree is listed again.*

```
>RUN
THIS PROGRAM GENERATES 100 RANDOM NUMBERS AND SORTS THEM USING
A BINARY SEARCH TREE.  IT ALSO ALLOWS DELETIONS FROM, OR ADDITIONS
TO THE TREE.
ELEMENTS AS THEY WERE GENERATED ARE
64      22      76      30      15      85      98      69      76      33
53      9       91      30      3       15      34      75      16      97
50      28      53      10      71      23      99      28      27      41
99      28      8       94      69      6       26      13      76      21
6       55      90      82      24      92      19      96      43      97
78      7       66      81      97      36      32      37      58      47
21      60      97      86      50      99      72      35      32      62
96      14      37      99      89      78      38      42      46      92
47      49      56      91      22      88      63      67      5       34
26      22      65      33      10      73      54      38      11      45
DO YOU WANT TO:
  1.   ADD A NODE
  2.   DELETE A NODE
  3.   LIST THE TREE
  4.   END
?3
TREE FOLLOWS:
ELEMENTS IN ORDER
3       5       6       6       7       8       9       10      10      11
13      14      15      15      16      19      21      21      22      22
22      23      24      26      26      27      28      28      28      30
30      32      32      33      33      34      34      35      36      37
37      38      38      41      42      43      45      46      47      47
49      50      50      53      53      54      55      56      58      60
62      63      64      65      66      67      69      69      71      72
73      75      76      76      76      78      78      81      82      85
86      88      89      90      91      91      92      92      94      96
96      97      97      97      97      98      99      99      99      99
DO YOU WANT TO:
  1.   ADD A NODE
  2.   DELETE A NODE
  3.   LIST THE TREE
  4.   END
?2
GIVE KEY TO BE DELETED ?8
DO YOU WANT TO:
  1.   ADD A NODE
  2.   DELETE A NODE
  3.   LIST THE TREE
  4.   END
?3
TREE FOLLOWS:
ELEMENTS IN ORDER
3       5       6       6       7       9       10      10      11      13
14      15      15      16      19      21      21      22      22      22
23      24      26      26      27      28      28      28      30      30
32      32      33      33      34      34      35      36      37      37
38      38      41      42      43      45      46      47      47      49
50      50      53      53      54      55      56      58      60      62
63      64      65      66      67      69      69      71      72      73
75      76      76      76      78      78      81      82      85      86
88      89      90      91      91      92      92      94      96      96
97      97      97      97      98      99      99      99      99
DO YOU WANT TO:
  1.   ADD A NODE
  2.   DELETE A NODE
  3.   LIST THE TREE
  4.   END
?1
GIVE KEY ?39
DO YOU WANT TO:
  1.   ADD A NODE
  2.   DELETE A NODE
  3.   LIST THE TREE
  4.   END
?3
TREE FOLLOWS:
ELEMENTS IN ORDER
3       5       6       6       7       9       10      10      11      13
14      15      15      16      19      21      21      22      22      22
23      24      26      26      27      28      28      28      30      30
32      32      33      33      34      34      35      36      37      37
38      38      39      41      42      43      45      46      47      47
49      50      50      53      53      54      55      56      58      60
62      63      64      65      66      67      69      69      71      72
73      75      76      76      76      78      78      81      82      85
86      88      89      90      91      91      92      92      94      96
96      97      97      97      97      98      99      99      99      99
DO YOU WANT TO:
  1.   ADD A NODE
```

I will delete the circled element.

The circled element has been added.

Listing 2 continued on page 106

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Listing 2 continued:

```
   2.   DELETE A NODE
   3.   LIST THE TREE
   4.   END
?4
```

Listing 3: *Pascal program for sorting a binary tree. Due to the nature of the program, the binary tree does not need to be threaded; this simplifies most of the procedures and functions of the program. Program details are given in the text. This program, written to run on a Digital Equipment Corporation PDP-11/70, should run in UCSD Pascal without modification.*

```
program tree (input,output);
const  nul =0;
       n=20;
        n1=10;

var top,q,parent,value,node,root,p:integer;
        full,found,fulltree,empty,quit,emptytree,insert : boolean;
        stack :array [1..n] of integer;
        lp,rp,data : array [1..n1] of integer;


procedure initstack;
  begin
        begin
                full:=false;
                empty:=true;
                top:=n;
        end;
end;


procedure push(p:integer);
        begin
                empty:=false;
                if not full then
                        begin
                                stack[top]:=p;
                                top:=top-1;
                                if top=0 then full:=true;
                        end
                else
                        begin
                                writeln ('stack overflow !!!');
                                quit:=true;
                        end;
        end;


function pop:integer;
begin
        full:=false;
        if not empty then
                begin
                        top:=top+1;
                        pop:=stack[top];
                        if top=n then empty:=true
                        else;
                end
        else;
end;


procedure moveleft;
  begin
        if not full then
                        repeat
                                begin
                                        push(p);
                                        p:=lp[p];
                                end
                        until (p=nul) or full
        else
                writeln ('overflow stack');
  end;


procedure moveright;
  begin
        repeat
                begin
                        p:=pop;
                        writeln (data[p]);
                end
        until (rp[p]<>nul) or empty;
```

Listing 3 continued on page 108

Listing 3 continued:

```
      if (rp[p]=nul) and empty then quit:=true else
              begin
                     p:=rp[p];
                     moveleft;
              end;
end;

procedure scan;
  begin
if not emptytree then begin
quit:=false;
  p:=root;
        moveleft;
        while not quit do moveright;
  end
else writeln ('tree empty');
  end;

procedure initree;
  begin
        emptytree:=true;
        root:=nul;
        fulltree:=false;
        for p:=1 to n1 do
                begin
                        lp[p]:=nul;
                        rp[p]:=nul;
                end;
  end;


procedure addnode(a:integer);
  begin
  if emptytree then
   begin
     root:=a;
     emptytree:=false;
   end
  else
  begin
    p:=root;
    insert:=false;
    while not insert do
        begin
                if data[a]<=data[p] then
                        begin
                                if lp[p]=nul then
                                        begin
                                                insert:=true;
                                                lp[p]:=a;
                                        end
                                else p:=lp[p];
                        end
                else
                        begin
                                if rp[p]=nul then
                                        begin
                                                insert:=true;
                                                rp[p]:=a;
                                        end
                                else p:=rp[p];
                        end;
        end;
end;
end;


procedure search;
  begin
        node:=0;
        found:=false;
        parent:=0;
        p:=root;
        while not found do
          begin
                if value=data[p] then
                  begin
                        found:=true;
                        node:=p;
                  end
                else
                  begin
                        if value < data[p] then
                          if lp[p]<>nul then
                                begin
                                  parent:=p;
                                  p:=lp[p];
                                end
                          else
                                begin
```

```
                                  node:=0;
                                  parent:=0;
                                  found:=true;
                                  writeln ('value not in tree');
                                end
                        else
                          if rp[p]<>nul then

                          begin
                                parent:=p;
                                p:=rp[p];
                          end
                        else
                          begin
                                node:=0;
                                parent:=0;
                                found:=true;
                                writeln (' value not in tree');
                          end;
                  end;
                end;
        end;
procedure delete;
begin
if node=root then begin
     if (lp[node]=nul) and (rp[node]=nul) then initree else;
     if (lp[node]=nul) and (rp[node]<>nul) then root:=rp[node] else;
     if (lp[node]<>nul) and (rp[node]=nul) then root:=lp[node] else;
     if (lp[node]<> nul) and (rp[node]<> nul) then
        begin
          root:=lp[node];
          p:=lp[node];
          while rp[p]<>nul do p:=rp[p];
          rp[p]:=rp[node];
        end
     else;
  end
else
  begin
        if lp[node]=0 then
          if rp[parent]=node then
                rp[parent]:=rp[node]
            else lp[parent]:=rp[node]
        else
          if rp[node]=0 then
                if rp[parent]=node then rp[parent]:=lp[node]
                else lp[parent]:=lp[node]
          else
                if lp[parent]=node then
                  begin
                        lp[parent]:=lp[node];
                        p:=lp[node];
                        while rp[p]<>nul do p:=rp[p];
                         rp[p]:=rp[node]
                  end
                else
                  begin
                        rp[parent]:=lp[node];
                        p:=lp[node];
                        while rp[p]<>nul do p:=rp[p];
                        rp[p]:=rp[node];    .
                  end
  end;
end;

 begin (*main program*);
   initree;
   initstack;
     for q:=1 to n1 do
        begin
                writeln ('give node to add');
                readln (data[q]);
                addnode(q);
                scan;
        end;

 (*deletion section*)
 while not emptytree do
        begin
                writeln ('give node to delete');
                readln (value);
                search;
                if node<>0 then delete else writeln ('value not found');
                scan;
         end;
 end.
 %
 :
  ECN 11/70 Unix
 login:
```

Text continued from page 102:
and 8 are highlighted for clarity. Note that only one node in the tree, the rightmost node (containing the largest entry in the sorted list), has a right pointer with a value of zero. This is a signal that the end of the tree has been reached.

Let us look at the process of reading the sorted numbers from the tree in figure 7. We enter the tree at the root node, which contains the integer 15. We move left down the tree until we encounter the first node with a left pointer of zero (which we

Text continued on page 250

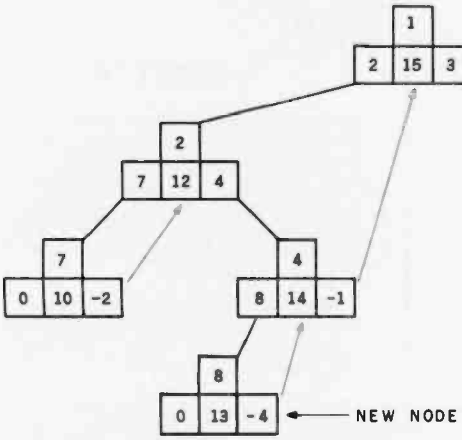

Figure 8: *Addition of a node to a binary tree. Using the notation of figure 7, this figure shows the addition of node 8, which has a key value of 13. The left pointer of node 8 is 0, denoting no left child. The right pointer of node 8 is -4, denoting two things: first, that node 8 has no right child; and second, that the node whose key follows the key of node 8 in the sorted-key sequence is node 4. The upward right pointers are shown here in color.*

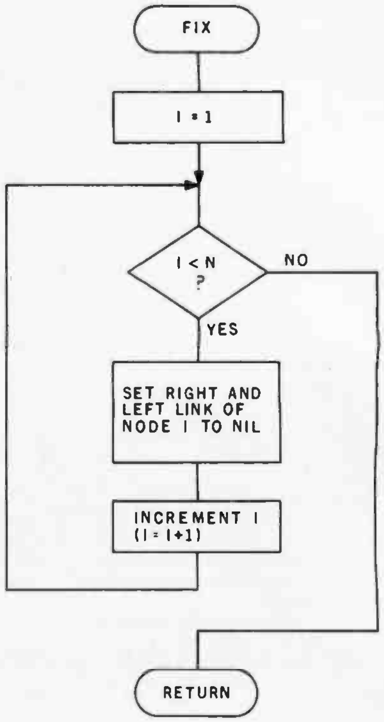

Figure 9: *Flowchart for subroutine FIX. This subroutine initializes storage space in a computer for later use as a threaded binary tree.*

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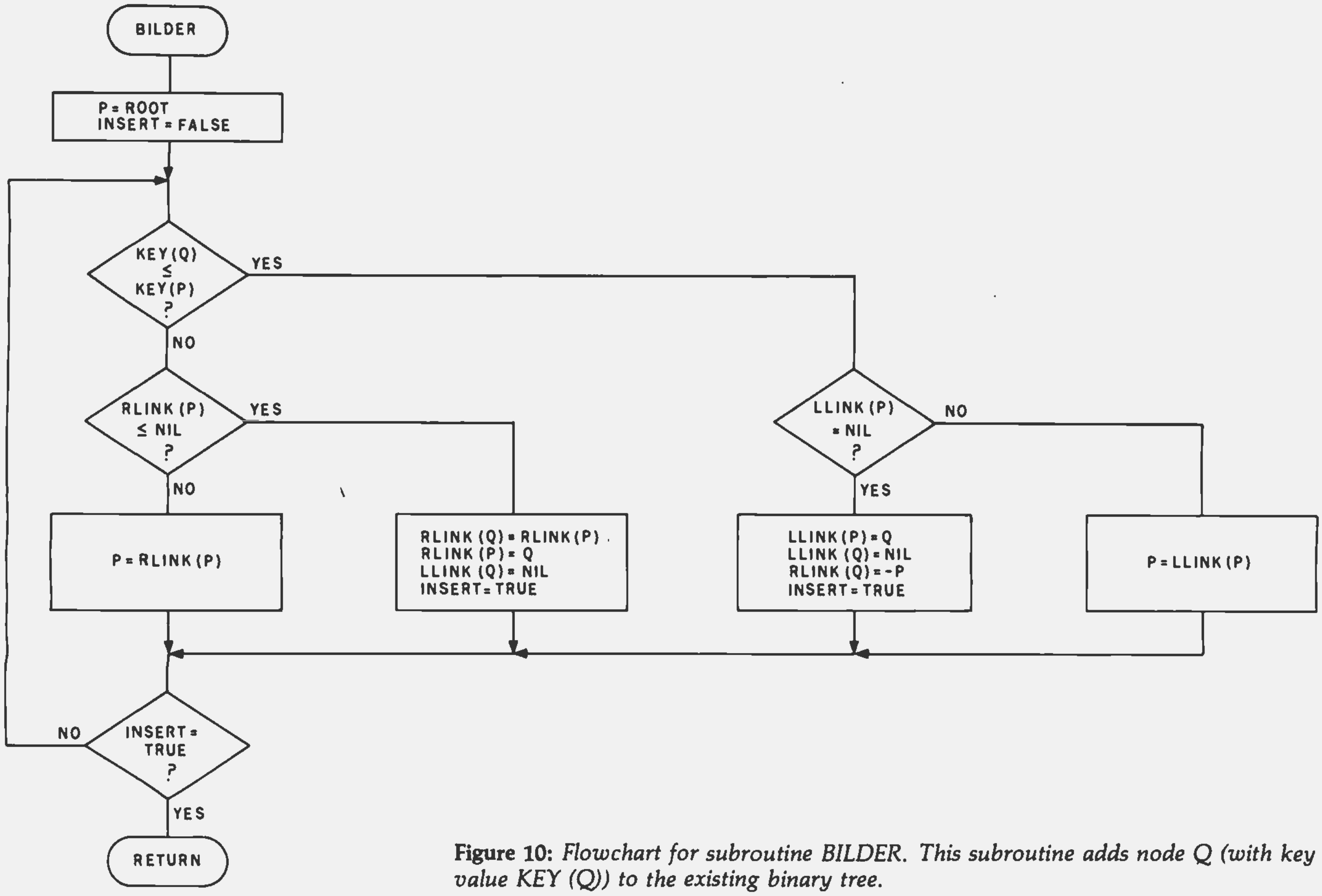

Figure 10: *Flowchart for subroutine BILDER. This subroutine adds node Q (with key value KEY (Q)) to the existing binary tree.*

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An Information-Retrieval System

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Much has been said in recent years regarding the reduction in size and increase in the capabilities of computing equipment. Manufacturers appear to be flooding the marketplace with ever more and more sophisticated small systems. One result of this expansion is that small computers of adequate capability are now within the financial reach of smaller businesses which previously could not justify the expense associated with the use of larger systems.

Unfortunately, the prospective buyer of such hardware may still be faced with a serious problem. He must, quite probably, pay someone to develop the software required by his particular application. This expense may be substantial since software development costs have taken a trend opposite to the cost of hardware.

An information-retrieval system is a fairly common software need. This usually must be tailored to a very specific application—an employee file or an inventory file, for example. Further, it is frequently the case that the user of the information-retrieval system is not a programmer, and may find that the system is confusing and therefore difficult to use.

The preceding provides the motivation for the concepts and software described in this article. In writing this article, we have kept in mind four goals:

- to present a method of organizing data such that its manipulation by the algorithms presented is, to a high degree, independent of the data itself;
- to describe a high-level query-answering language that may be used by nonprogrammers with minimal difficulty;
- to demonstrate the feasibility of implementing such an information-retrieval system on a small computer system; and
- to show that such an implementation can be relatively system-independent and therefore transportable.

Frequently, the user of the information-retrieval system is not a programmer.

An attempt has been made to make the system as easy to use as possible. This has been facilitated through the use of highly interactive programming. Although the user must give careful consideration as to how he wishes to use his data (since this will affect its organization), the program that creates and organizes files simply prompts the user for information which he should have already determined, eg: file size and record length. Data input requires little more than the data itself; the user is prompted for the values to be placed in a record. Formatting of the data for storage is accomplished through the use of information supplied when the file was created.

The query-answering language has been modeled after the PL/I structure declaration. It may be entered in free format, and its syntax has relatively few restrictions. We believe that this form is well suited for use by persons with little or no programming experience.

Implementation of the information-retrieval system described was accomplished using a Hewlett-Packard System 1000 minicomputer with the RTE-III operating system. All output examples were generated on this system, and all programs were written in Hewlett-Packard's implementation of FORTRAN IV. Since this language enjoys such widespread use, system dependencies are largely confined to calls to file-management routines, and modifications necessary to adapt the software to another system should be relatively minor.

Defining the File

The key to the manipulation of data bases in the manner described is the organization of the data itself. The structure used is that of a *flat file*, which is self-defining. A flat file may be thought of as a simple two-dimensional array of data elements. This organization is made self-defining by storing all necessary descriptive infor-

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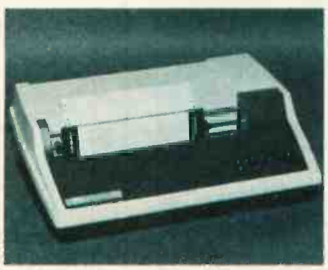

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mation about data in the file in a location within the file itself. Since this location is fixed, programs that access the file can determine the location and nature of file data by referencing this descriptive information. No input from a user regarding the physical organization of a file is needed once that file has been defined.

Figure 1a illustrates the organization of descriptive information and the data itself within a self-defining file. Region 1 contains five fields (this will be true for any file) as listed in table 1. Region 2 contains aggregates (the number of which is defined in field 4 of region 1) consisting of four pieces of information, as listed in table 2. Region 3 and those following contain the records of the file. The fields are concatenated as shown, and their order corresponds to that of the descriptive aggregates stored in region 2.

To better illustrate this file organization, an example of a specific application will be considered in detail. The application is that of a personnel data base that is used to store the job applications submitted by prospective employees. Records such as this would typically be maintained by a manual filing system, which might be large and restricted to one pattern of organization (eg: filed alphabetically by name). We will demonstrate that, with a minimal amount of preparation, an easily maintained data base can be constructed for this information. This will allow the user the capability to search for and quickly locate records satisfying a great number of different criteria.

Figure 1b illustrates one possible record description for this data base. Each record consists of twelve fields, each of which is described in the figure. The type of each field (alphanumeric or digital) and its length in characters are shown. The total record length is 130 characters. It should be emphasized that the field and record lengths are, to a certain extent, arbitrary. The record could have been defined with a different number of fields and different field and record lengths.

Listing 1a shows regions 1 and 2, as well as the file data for the personnel data base in an unformatted form (ie: just as it is stored), which was created using the information-retrieval system. Listing 1b is a partial listing of the file data formatted in a readable form. This is simply accomplished by making use of the field positions and length information stored in region 2.

Text continued on page 126

1. Date of creation: the date on which the file was created.
2. Date of last update: each time a record is added to or deleted from a file, the current date is inserted.
3. First free region: this is a pointer to the next location that may be used for inserting a new record. Since records are stored sequentially and kept compacted, this pointer will be incremented for each addition and decremented for each deletion of a record.
4. Number of tags: this defines the number of fields within a record, which is also the number of field-description aggregates contained in region 2 (see table 2).
5. Record length: the length of records (fixed) contained in the file.

Table 1: *Descriptive information for a self-defining file. The five fields listed here make up region 1 of a self-defining file. Any program that wants to reference or update information in this file must first read regions 1 and 2 in order to know the organization of the file.*

1. Tag_i: a short character identifier for the ith field in the records.
2. Type: a "flag" that indicates whether the ith field contains an alphanumeric or digital value.
3. Length: the length of the ith field within a record.
4. Starting position: the location within a record which marks the beginning of the ith field.

Table 2: *Descriptive information for field definition. The four fields here are repeated for each field in the record. Together, they make up region 2 of a self-defining file. The four fields here completely describe a field within the defined record.*

REGION 1	DATE OF CREATION	DATE OF LAST UPDATE	FIRST FREE REGION	NUMBER OF TAGS	RECORD LENGTH			
REGION 2	TAG 1	TYPE	LENGTH	STARTING POSITION	---	TAG N	TYPE	LENGTH	STARTING POSITION
REGION 3	FIELD 1	FIELD 2	---	FIELD N				

(a) GENERAL FILE ORGANIZATION

TYPE	D	A	A	A	A	D	A	A	A	A	D	D
	DATE	SURNAME	NAME	INITIAL	ADDRESS	PHONE	DEGREE	MAJOR	WORK INTEREST 1	WORK INTEREST 2	EXPERIENCE 1	EXPERIENCE 2
FIELD LENGTHS	8	10	10	2	28	8	4	16	20	20	2	2

RECORD LENGTH 130

1) DATE: DATE ON WHICH APPLICATION WAS SUBMITTED
2) SURNAME:
3) FIRST NAME: } 3 FIELDS COMPRISING THE APPLICANT'S NAME
4) INITIAL:
5) ADDRESS: ADDRESS OF APPLICANT
6) PHONE: TELEPHONE NUMBER OF APPLICANT
7) DEGREE: HIGHEST DEGREE EARNED (E.G. B.S.)
8) MAJOR: MAJOR FIELD OF STUDY (E.G. MATHEMATICS)
9) WORK INTEREST 1: PRIMARY AREA OF INTEREST (E.G. SALES)
10) WORK INTEREST 2: SECONDARY AREA OF INTEREST (E.G. PURCHASING)
11) EXPERIENCE 1: YEARS OF EXPERIENCE IN PRIMARY AREA OF INTEREST
12) EXPERIENCE 2: YEARS OF EXPERIENCE IN SECONDARY AREA OF INTEREST

(b) RECORD DESCRIPTION FOR A PERSONNEL DATA BASE

Figure 1: *Organization and example of a self-defining file. Figure 1a illustrates the data organization of a self-defining file. Figure 1b presents the layout of a file record used in examples throughout this article.*

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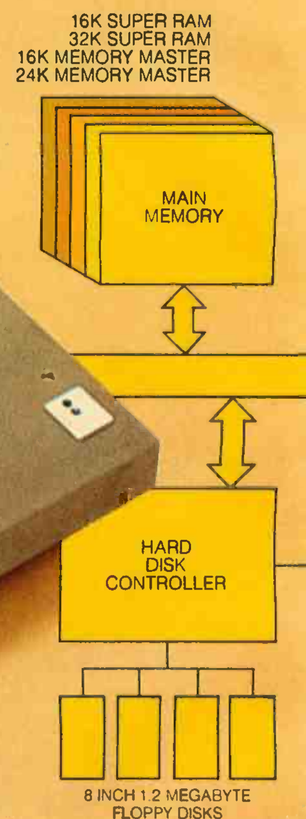

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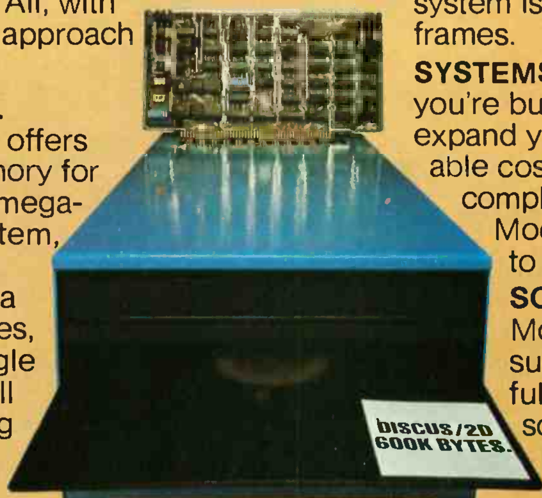

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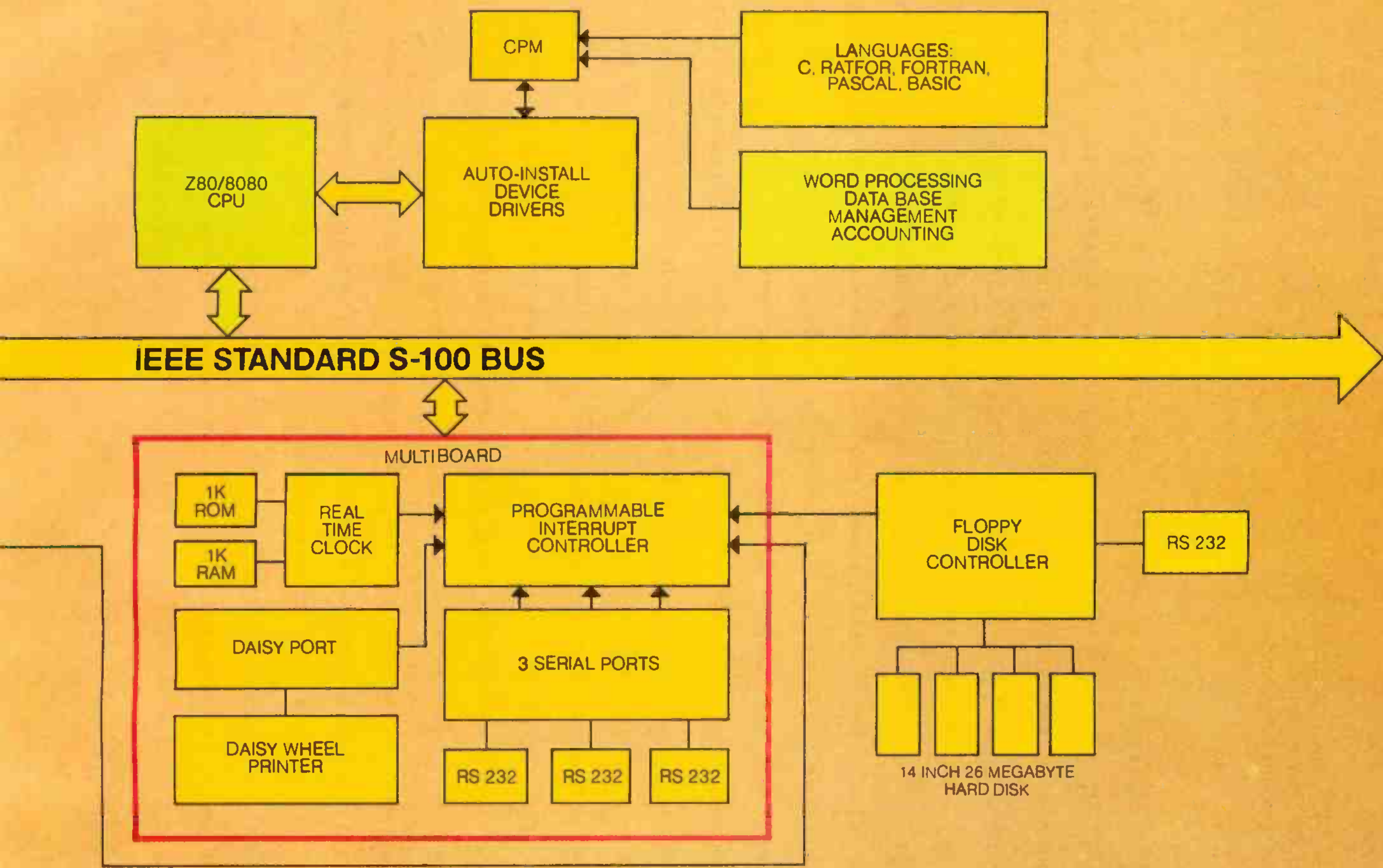

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Listing 1a: *A complete self-defining file. The first line, which begins "2-3-79", is region 1 of the file. The second and third lines, which begin with "DATED" and "10", are region 2 of the file. The rest of the file is region 3, that contains data beginning with one line per record on this listing.*

```
 2- 3-79   2- 3-79          24         12         65

DATED     4   1LNAMA     5   5FNAMA     5  10INITA     1  15ADDRA    14  16TEL#D     4  30DEG A     2  34MJR A     8  36INT1A    10  44INT2A
 10  54EXP1D    1  64EXP2D     1  65
78/11/08BLACKWELL LARRY     W 8180 PALLISTER DETROIT MI   871-9167BA  GENERAL BUSINESSSALES/MARKETING     PURCHASING            4 2

78/11/12KRAFT     PATRICK   A 26044 VILLAGE PLYMOUTH MI   445-6176MS  MATHEMATICS     PRODUCT ENGRG       MANUFACTURING ENGRG  2 0

78/11/02HACKMAN   GERALD    R 292 CARDWELL TOLEDO OH      222-57528A  GENERAL BUSINESSSALES/MARKETING     QUALITY CONTROL       7 0

78/09/28MARCHANT  HAROLD    R 9670 TREELANE DEARBORN MI   561-25538S  MECHANICAL ENGRGPRODUCT ENGRG       MANUFACTURING ENGRG  1 0

78/09/29MALST     DENNIS    R 1025 CHENE TOLEDO OH        333-4714MS  MECHANICAL ENGRGPRODUCT ENGRG       TECHNICAL RESEARCH    8 2

78/10/19DUNNING   ALLAN     G 1021 THIRD WYANDOTTE MI     868-73268S  EDUCATION       COMPUTER PROGRAMMINGQUALITY CONTROL       0 2

78/10/05REDFORD   KEVIN     D 17504 RANIER ALLEN PARK MI  277-45458A  ECONOMICS       QUALITY CONTROL     SALES/MARKETING       3 4

78/09/15STANLEY   SUSAN     A 29213 GREENLAWN DETROIT MI  555-8002HS+ GENERAL BUSINESSACCOUNTING          SALES/MARKETING       7 0

78/10/10MAYNARD   STEPHEN   L 36500 RUSHMORE FRANKLIN MI  815-4202MS  PSYCHOLOGY      INDUSTRIAL RELATIONSSALES/MARKETING       1 0

78/12/10PALINDROMEANTHONY   J 43441 DARTMOUTH NOVI MI     447-39028S  ELECTRICAL ENGRGTECHNICAL RESEARCH  PRODUCT ENGRG        15 2

78/10/04DAYTON    THOMAS    F 2125 TULANE WESTLAND MI     666-3820HS+ DRAFTING        DESIGN/DRAFTING     PRODUCT ENGRG         6 0

78/09/30HAYDEN    MARY      E 24042 PIPER TAYLOR MI       755-9550A   MATHEMATICS     ACCOUNTING          SALES/MARKETING      10 2

78/09/25VAN HORN  BERNARD   G 1741 SUNSET LIVONIA MI      227-40218A  PSYCHOLOGY      INDUSTRIAL RELATIONSPURCHASING            2 4

78/09/16TIBBY     MARTIN    W 1401 LAKELAND CHICAGO IL    656-37088S  ELECTRICAL ENGRGTECHNICAL RESEARCH  PRODUCT ENGRG         0 0

78/09/13SUNICK    PAUL      W 5419 HILL OAKPARK MI        599-3497A   DRAFTING        DESIGN/DRAFTING     PRODUCT ENGRG         3 0

78/09/15KOHN      ROBERT    C 6565 ABNER SOUTHFIELD MI    533-84528S  COMPUTER SCIENCECOMPUTER PROGRAMMINGNONE                  1 0

78/08/22HAYES     JAMES     K 1521 SHOETREE TROY MI       551-98748S  PHYSICS         TECHNICAL RESEARCH  PRODUCT ENGRG         5 1

78/11/20SMITH     HENRY     M 130 BARD DEARBORN MI        469-7412MS  MECHANICAL ENGRGPRODUCT ENGRG       NONE                  3 0

78/07/06KYSER     CYNTHIA   A 5820 MULBERRY WAYNE MI      666-92878S  COMPUTER SCIENCECOMPUTER PROGRAMMINGTECHNICAL RESEARCH    1 0

78/08/02ROSSMAN   MARVIN    T 3355 ACADEMY DETROIT MI     638-7663HS+ GENERAL BUSINESSACCOUNTING          INDUSTRIAL RELATIONS 5 2

78/09/25MARSHALL  PETER     K 7914 HADLEY BRIGHTON MI     383-2737HS+ DRAFTING        DESIGN/DRAFTING     PRODUCT ENGRG        13 6
```

Listing 1b: *File records from the self-defining file of listing 1a, printed in formatted form.*

```
REC#  3
DATE      =    78/11/08
LNAM      =    BLACKWELL
FNAM      =    LARRY
INIT      =    W
ADDR      =    8180 PALLISTER DETROIT MI
TEL#      =    871-9167
DEG       =    BA
MJR       =    GENERAL BUSINESS
INT1      =    SALES/MARKETING
INT2      =    PURCHASING
EXP1      =     4
EXP2      =     2

REC#  4
DATE      =    78/11/12
LNAM      =    KRAFT
FNAM      =    PATRICK
INIT      =    A
ADDR      =    26044 VILLAGE PLYMOUTH MI
TEL#      =    445-6176
DEG       =    MS
MJR       =    MATHEMATICS
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     2
EXP2      =     0

REC#  5
DATE      =    78/11/02
LNAM      =    HACKMAN
FNAM      =    GERALD
INIT      =    R
ADDR      =    292 CARDWELL TOLEDO OH
TEL#      =    222-5752
DEG       =    BA
MJR       =    GENERAL BUSINESS
INT1      =    SALES MARKETING
INT2      =    QUALITY CONTROL
EXP1      =     7
EXP2      =     0

REC#  6
DATE      =    78/09/28
LNAM      =    MARCHANT
FNAM      =    HAROLD
INIT      =    R
ADDR      =    9670 TREELANE DEARBORN MI
TEL#      =    581-2553
DEG       =    BS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     1
EXP2      =     0

REC#  7
DATE      =    78/09/29
LNAM      =    MALST
FNAM      =    DENNIS
INIT      =    R
ADDR      =    1025 CHENE TOLEDO OH
TEL#      =    333-4714
DEG       =    MS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    TECHNICAL RESEARCH
EXP1      =     8
EXP2      =     2

REC#  8
DATE      =    78/10/19
LNAM      =    DUNNING
FNAM      =    ALLAN
INIT      =    G
ADDR      =    1021 THIRD WYANDOTTE MI
TEL#      =    888-7326
DEG       =    BS
MJR       =    EDUCATION
INT1      =    COMPUTER PROGRAMMING
INT2      =    QUALITY CONTROL
EXP1      =     0
EXP2      =     2
```

Text continued from page 116:

The overall organization of the information-retrieval system is illustrated in the block diagram of figure 2a. The main program serves only to call segment 1 into memory from the disk, and is never returned to. More will be said of this later when the use of memory overlays in this implementation is discussed.

A Nassi-Schneiderman flowchart of segment 1 is presented in figure 2b. (Such flowcharts are given for all routines.) It is quite straightforward and serves only to parse commands entered by the user. These are:

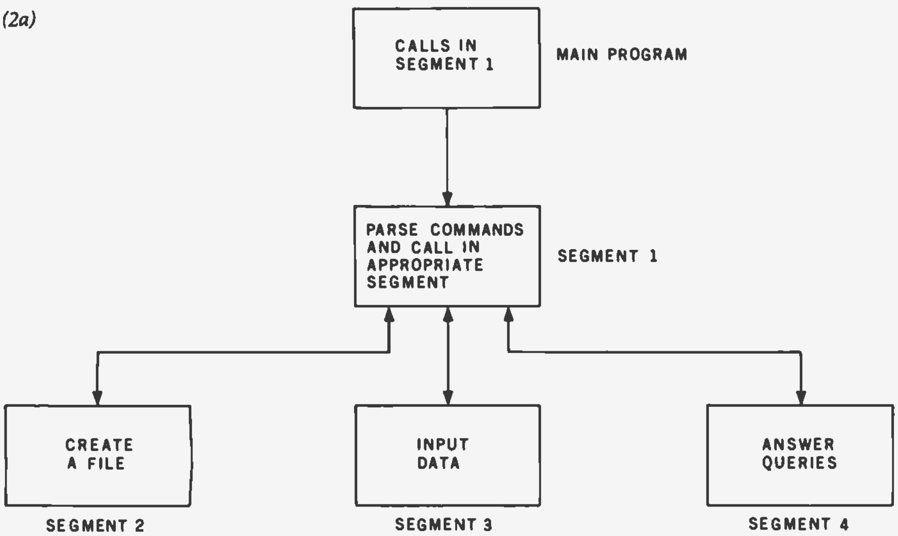
- CREATE: this command causes segment 2 to be called into memory, which will prompt the user for the information necessary to create a file.
- INPUT: this command causes segment 3 to be called in, which will prompt the user for information necessary to insert new records into a file.
- QUERY: this command causes segment 4 to be called in to prompt the user for and answer queries pertaining to a file.
- STOP: terminates program execution.

Whenever creation, input, or query operations are terminated, the respective segment (2, 3, or 4) calls in segment 1 once again to parse additional commands. This structure (segments 1 thru 4) is completely analogous to a main program and three subroutines, and will be treated as such in the discussion of the three major file operations.

As previously indicated, some planning is required prior to the creation of a file. The user must first determine the information to be stored, the number of required fields per record, appropriate tags for the fields, field lengths and types (alphanumeric or digital) and the maximum number of records required. This last requirement might not be necessary in implementations where extendable files are used. However, our implementation made use of nonextendable files with fixed record lengths.

An example of the interaction which takes place when creating the personnel file is shown in listing 2. Segment 1 prints the prompts "ENTER A COMMAND" and"#". The reply to the prompt "#" is the command "CREATE". Segment 2 then prompts for the name the user wishes to give the file, the number of records the file is to contain, the record length, and the number of tags. This dialogue corresponds to steps 1 thru 12 of the create-routine algorithm shown in figure 3. The test at step 8 determines whether or not the user's logical record will fit within 128-word (256-character), fixed-length physical records. (The Hewlett-Packard computer uses 16-bit words.) The test at step 13 is necessary because there is only enough room in one record (region 2) for eighteen field-description aggregates. Two words (four characters) are needed for the tag,

(2a)



(2b)

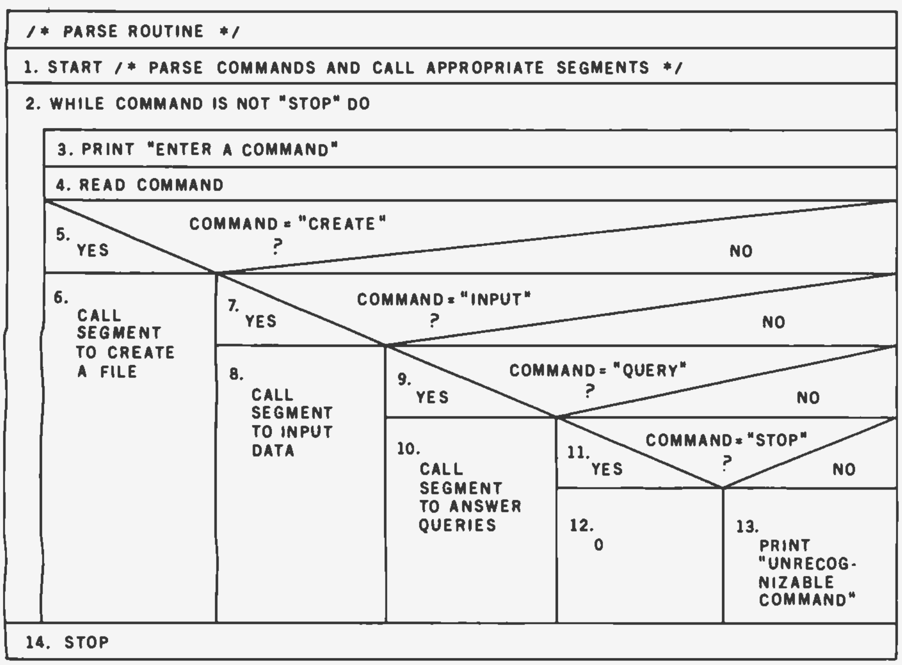


Figure 2: *Block diagram of program design and Nassi-Schneiderman chart for parsing routine. Figure 2a illustrates the overall design of the information-retrieval system program. It is designed in such a way that only one of the four program segments needs to be in computer memory at any one time. Figure 2b is a Nassi-Schneiderman chart of the routine in segment 1 that decides what segment is to be loaded into memory next. The L-shaped bracket labeled step 2 performs steps 3 thru 13 under the control of a "while" loop statement. Any step labeled 0 means to do nothing for that step. (See reference 5 for more information on this type of structured flowchart).*

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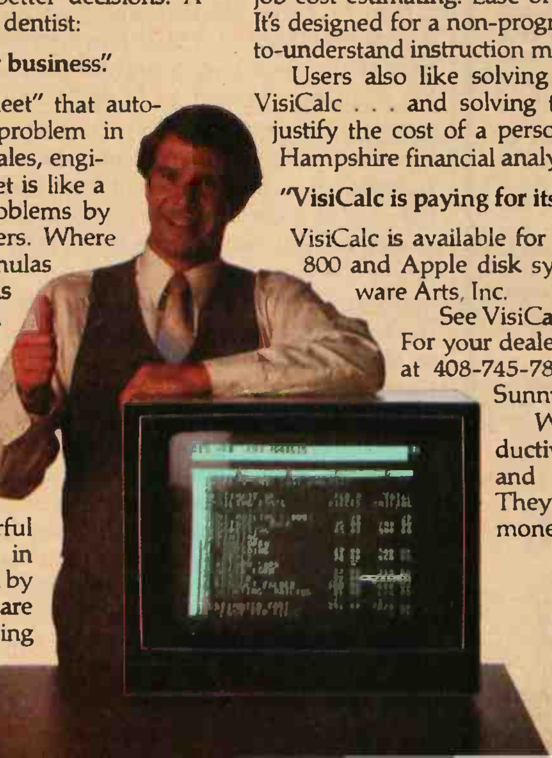

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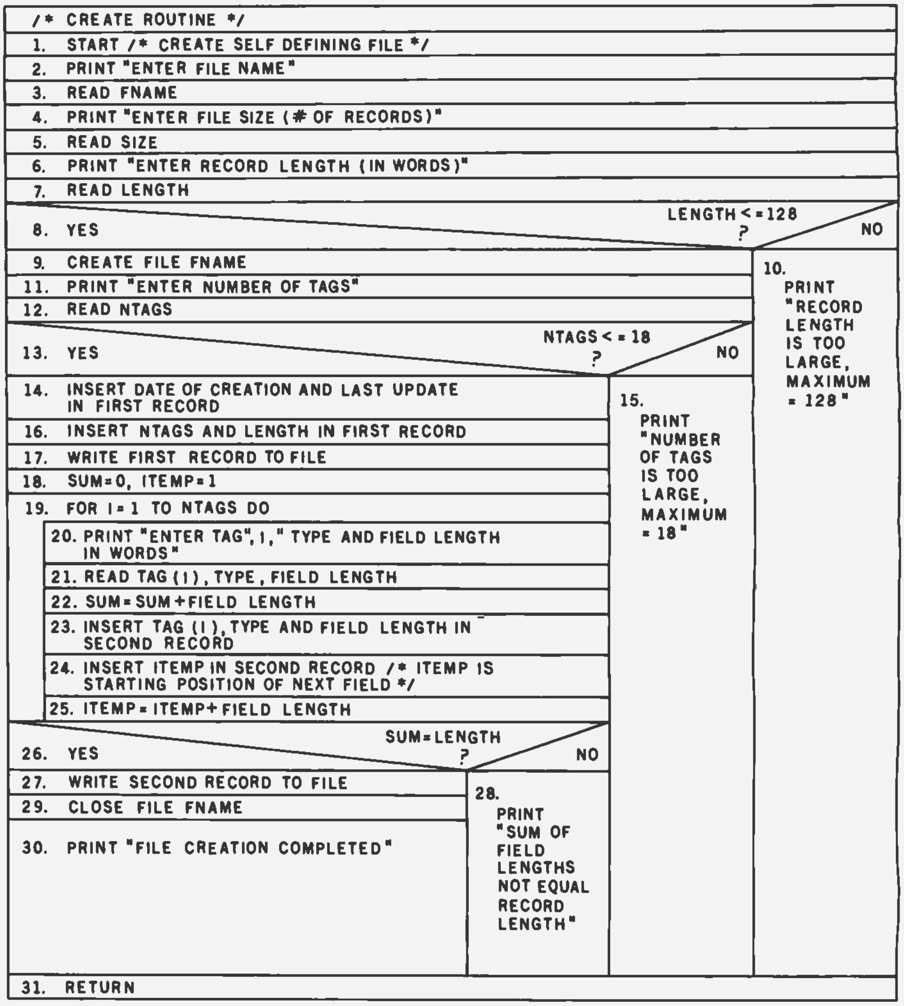

Figure 3: *Nassi-Schneiderman chart for the file-creating routine in segment 2. This routine prompts the user for the overall characteristics of the file and the characteristics of each field within the file.*

one for the field type (the letter D for digital or A for alphanumeric) and 2 words each for the ASCII representation of the field length and the starting position. At step 14, a call to an operating-system function retrieves the current time, which is inserted into region 1. The number of tags and the logical record lengths are inserted at step 16, and then the region is written to the file.

Steps 19 thru 25 prompt the user for the tags, types, and field lengths as shown in listing 2. The only syntactic restrictions on tags, other than a maximum length of four characters, is that they not begin with a digit and do not contain a colon. The reasons for these restrictions will become clear when the query routine is discussed. These values are placed in region 2 as the aggregates that were previously described. Step 26 is a check to insure that the sum of the field lengths given equals the specified record length. Region 2 is then written, the file closed, a message indicating successful file creation given to the user, and control is returned to segment 1.

Entering Data

Putting data into a file previously created is the most straightforward of all operations in this information-retrieval system. In preparation, all that is required is that the user have on hand the values to be inserted in each of the fields that make up a record in that file.

Listing 3 is a listing of the dialogue that took place during the insertion of three records in the personnel data base. Once the command "INPUT" is given, the user is prompted for the name of the file to be modified. This corresponds to steps 1 thru 3 in the Nassi-Schneiderman chart for the in-

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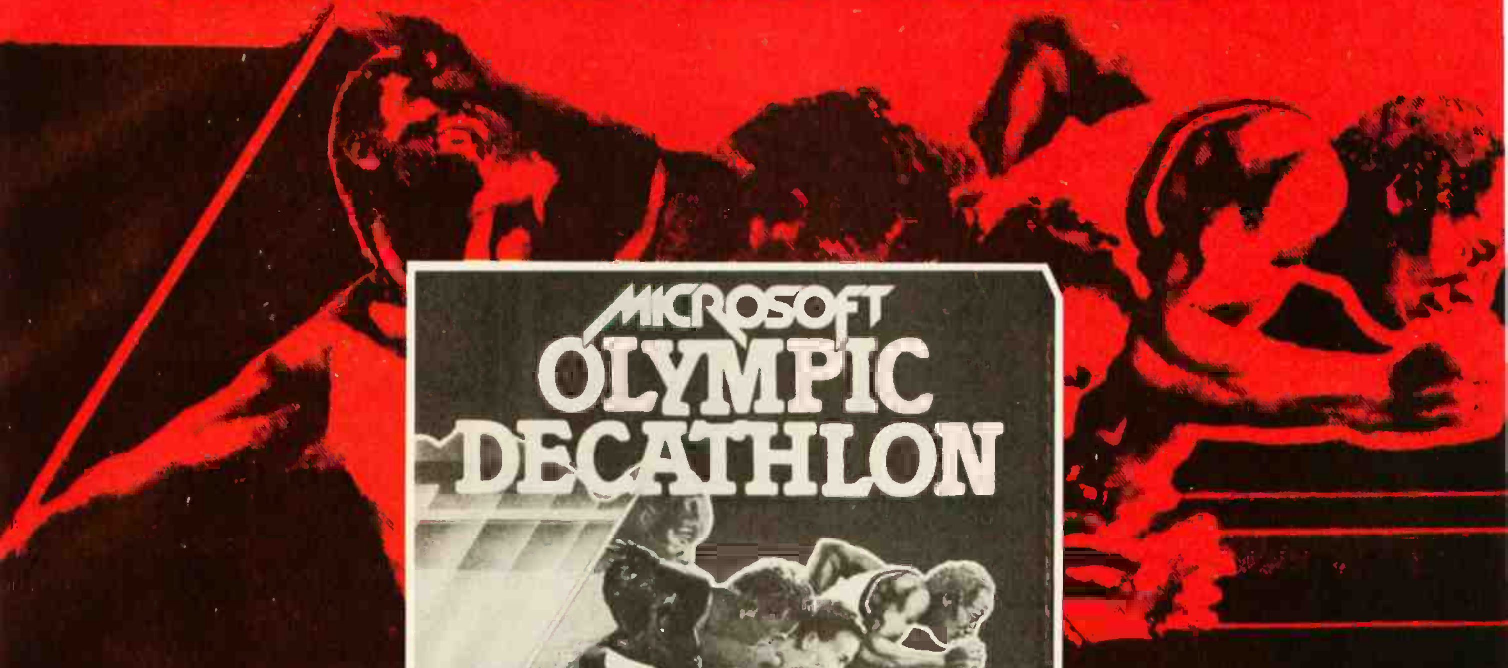

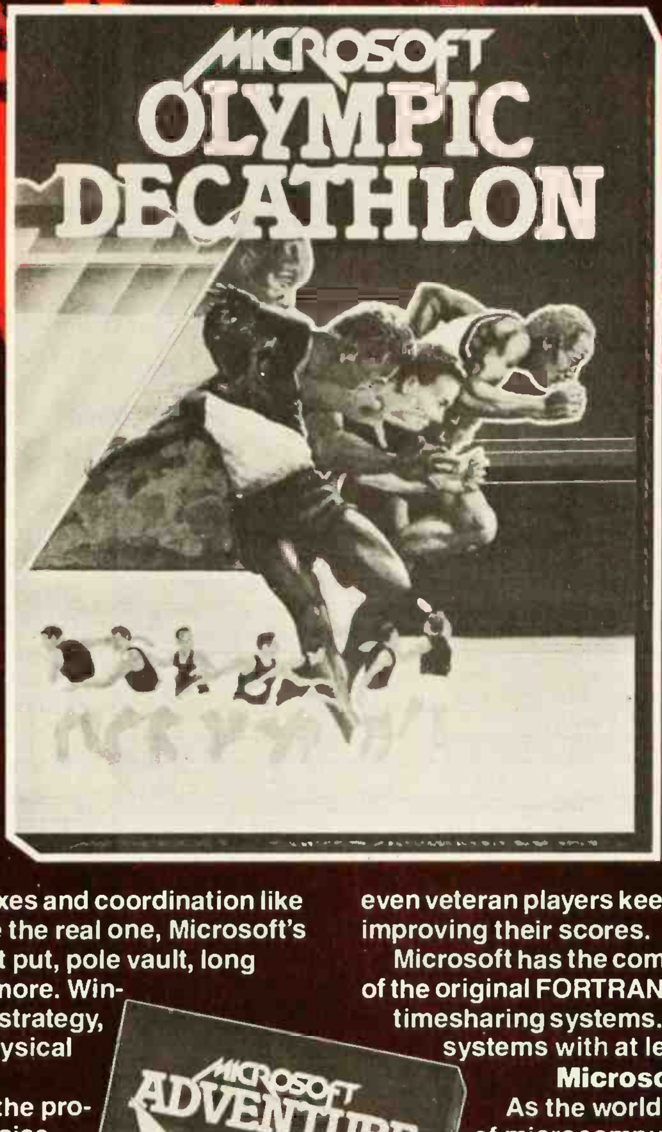

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Listing 2: *The file-creation process. This listing details the questions and answers necessary to create the employee file EMPFL1 of listing 1. It follows the structured flowchart of figure 3. This computer uses a 16-bit word length.*

```
ENTER A COMMAND
#CREATE
ENTER FILENAME
#EMPFL1
ENTER FILE SIZE (#OF RECORDS)
#30
ENTER RECORD LENGTH (IN WORDS)
# 65
ENTER NUMBER OF TAGS
#12
ENTER TAG 1, TYPE, AND FIELD LENGTH IN WORDS
#DATE
#D
# 4
ENTER TAG 2, TYPE, AND FIELD LENGTH IN WORDS
#LNAM
#A
# 5
ENTER TAG 3, TYPE, AND FIELD LENGTH IN WORDS
#FNAM
#A
# 5
ENTER TAG 4, TYPE, AND FIELD LENGTH IN WORDS
#INIT
#A
# 1
ENTER TAG 5, TYPE, AND FIELD LENGTH IN WORDS
#ADDR
#A
#14
ENTER TAG 6, TYPE, AND FIELD LENGTH IN WORDS
#TEL#
#D
# 4
ENTER TAG 7, TYPE, AND FIELD LENGTH IN WORDS
#DEG
#A
# 2
ENTER TAG 8, TYPE, AND FIELD LENGTH IN WORDS
#MJR
#A
# 8
ENTER TAG 9, TYPE, AND FIELD LENGTH IN WORDS
#INT1
#A
#10
ENTER TAG 10, TYPE, AND FIELD LENGTH IN WORDS
#INT2
#A
#10
ENTER TAG 11, TYPE, AND FIELD LENGTH IN WORDS
#EXP1
#D
# 1
ENTER TAG 12, TYPE, AND FIELD LENGTH IN WORDS
#EXP2
#D
# 1
FILE CREATION COMPLETED
```

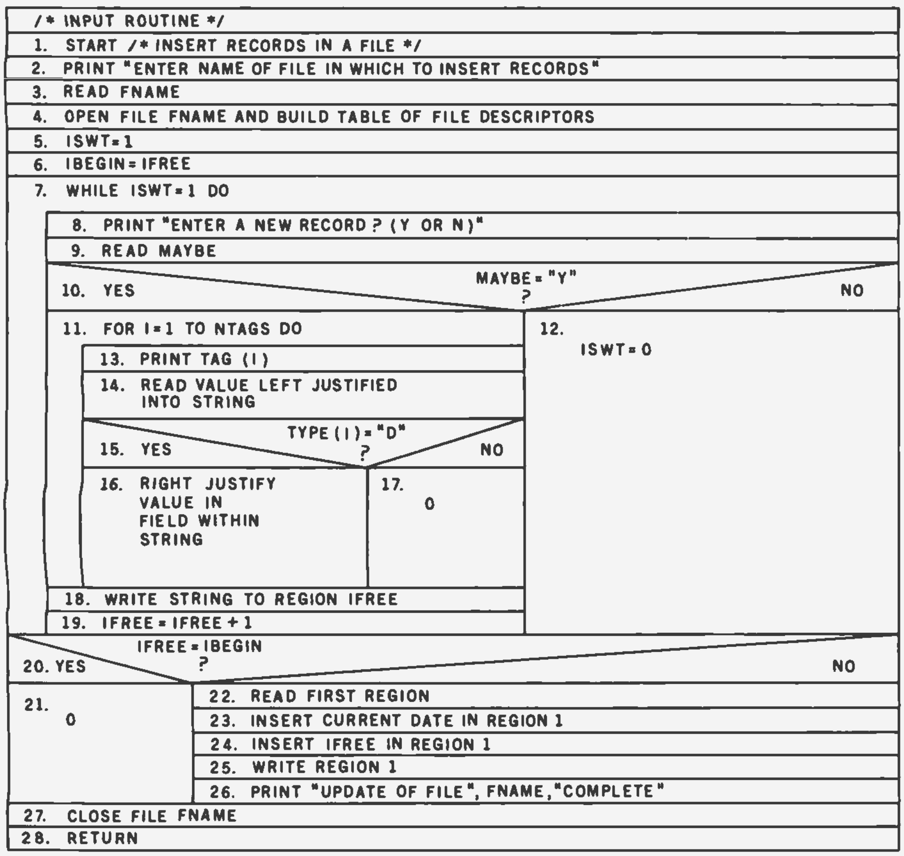

Figure 4: *Nassi-Schneiderman chart for the record-input routine in segment 3. This routine prompts the user for all the fields of a new record to be added to an existing file.*

put routine given in figure 4. Step 4 of the flowchart accesses the first two regions of the file specified and retrieves the information necessary to allow the proper formatting of new records and their insertion in the file. This information is as follows:

- first free region, number of tags, and record length
- four arrays, the dimension of which is determined by the number of tags (Remember that the maximum number is eighteen.) The information in these arrays corresponds to the values stored in region 2. That is, one array contains the tags, another the associated types, and the other two contain the field lengths and starting positions. Thus, by referencing the *i*th element of each array, all of the descriptive information regarding the *i*th field may be obtained.

Referring once again to listing 3, it may be seen that if the user responds with "YES" (or simply "Y") to the prompt "ENTER A NEW RECORD", he will be prompted for values to insert in each of the fields which define a record. The form of the

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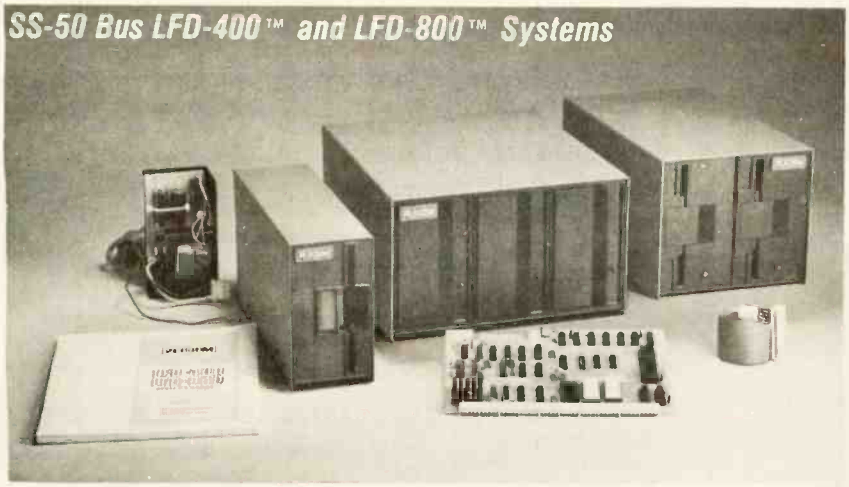

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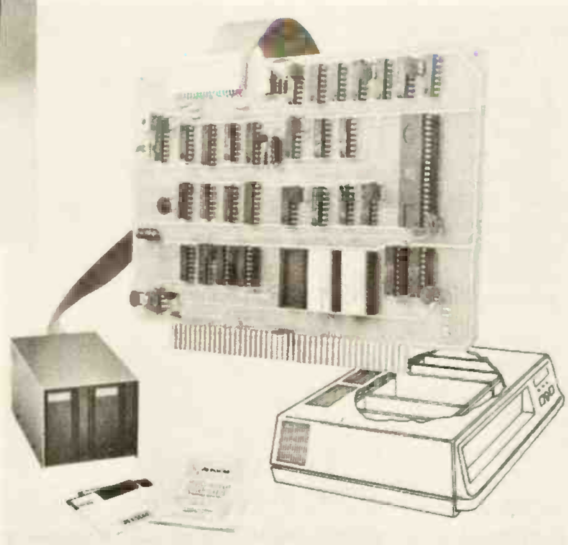

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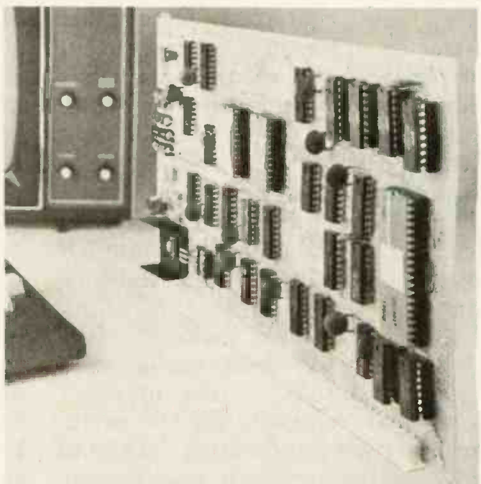

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Listing 3: *The record-input process. This listing details the questions and answers necessary to add three records to the EMPFL1 file. It follows the structured flowchart of figure 4.*

```
ENTER A COMMAND
#INPUT
ENTER NAME OF FILE IN WHICH TO INSERT RECORDS
 +EMPFL1
ENTER A NEW RECORD?(Y OR N)
 +Y
DATE=78/10/05
LNAME=REDFORD
FNAME=KEVIN
INIT=D
ADDR=17504 RANIER ALLEN PARK MI
TEL#=277-4545
DEG=BA
MJR=ECONOMICS
INT1=QUALITY CONTROL
INT2=SALES/MARKETING
EXP1=3
EXP2=4
ENTER A NEW RECORD?(Y OR N)
 +Y
DATE=78/09/15
LNAM=STANLEY
FNAM=SUSAN
INIT=A
ADDR=29213 GREENLAWN DETROIT MI
TEL#=555-8002
DEG=HS+
MJR=GENERAL BUSINESS
INT1=ACCOUNTING
INT2=SALES/MARKETING
EXP1=7
EXP2=0
ENTER A NEW RECORD?(Y OR N)
 +Y
DATE=78/10/10
LNAM=MAYNARD
FNAM=STEPHEN
INIT=L
ADDR=36500 RUSHMORE FRANKLIN MI
TEL#=895-4202
DEG=MS
MJR=PSYCHOLOGY
INT1=INDUSTRIAL RELATIONS
INT2=SALES/MARKETING
EXP1=1
EXP2=0
ENTER A NEW RECORD?(Y OR N)
 +N
UPDATE OF FILE EMPFL1 COMPLETE
```

prompt is "TAGN=". Once all of the values for a record have been obtained, the record is written to the file in the first free region, the free region *pointer* is incremented, and the prompt for entry of a new record is given once again. This sequence of operations corresponds to the iteration of steps 7 thru 19 in figure 4. Once all records have been formatted and written to the file, the current date is inserted in region 1 along with the new value for the pointer to the first free region.

Steps 14 thru 16 accomplish the formatting of values within a record. Although a field may contain any ASCII characters, if we wish to compare these characters to another character string, it is necessary that we know whether the characters represent an alphanumeric or a digital value, and that they be left or right justified accordingly within the field. For example, the string "ABC" compared to the string "AB*b*" will yield predictable results since they are *left* justified. (A lowercase, italic *b* represents a significant blank character.) However, the comparison of "ABC" to "*b*AB" will yield misleading results. Correspondingly, fields that represent digital values must be *right* justified (eg: "123" and "*b*12"). This approach also permits the comparison of fixed-point digital values (eg: "57.23" and "*b*1.12").

It may also be necessary to change the order of information within a field to obtain a meaningful comparison. For example, the date field in the personnel data base is input as year/month/day, as well as being right justified. This was necessary to maintain the values in a decreasing order of magnitude. Another approach would have been to assign separate tags to each of the three date components.

Answering Queries

Now that records have been created and inserted into the personnel data base, the answering of queries related to it may be discussed.

At the user level, the vehicle used to accomplish this is the query-answering language that was mentioned earlier. The elementary form of a query, which shall be referred to as a *simple* query, is constructed of the three components [tag_i], [relational operator], [value], where [tag_i] is one of the tags defined in region 2 of the file, [relational operator] is either less than (<), greater than (>), or equal (=), and [value] is a character string. The meaning of this construct is that the string given in [value] is to be tested against the field indicated by [tag_i], in the manner determined by [relational operator] for each record contained in the data base. Figure 5a illustrates two valid simple queries. The first is a request for all records such that the field LNAM equals "JONES". The second is a request for all records such that the DATE field is greater than "78/00/00", in other words, all records dated after the beginning of 1978.

These simple queries may be combined to form more complex queries by using the logical operators AND and OR, the general form of which is [level number] [logical operator], where [level number] is an integer from 1 to 99, and [logical operator] is either the string "AND:" or "OR:". When simple queries are combined by using logical operators, they must also be preceded by a level number which must be higher than that of the logical operator of which they are operands.

Figure 5b is an example of the logical AND of two simple queries. It is a request for all records such that the first area of interest is technical research and the experience in this area is more than 1 year.

Figure 5c is somewhat more complex and serves to point out two important features. First, a logical operation may apply to two or more operands; and second, the operands of a logical operation may actually be logical operations themselves. This query is a request for all records such that the applicant is primarily interested in computer science, has more than 1 year experience in that area, and has a Bachelor of Science degree in the field, or that the applicant is primarily interested in computer science and has more than 3 years experience in that area.

As one final point of interest, it should be noted that blanks are

generally ignored within a query. The only restriction is that at least one blank must separate a level number from a logical operator or a simple query.

Listings 4 thru 10 show the interaction that took place in answering seven queries pertaining to the personnel data base.

In all cases, just prior to the entry of the query, the user specifies what have been called *print/delete options*. These are represented by the characters P and D. Their meaning is as follows:

- P — Print the records satisfying this query.
- PD — Print the records satisfying this query and delete them from the data base.
- D — Delete the records satisfying this query from the data base but do not print them.

Although none of the examples of listings 4 thru 10 specifies the delete option, it will be discussed more fully later.

The query of listing 4 is a request for all applications dated since November 1, 1978. Five records satisfy this condition, and examination of the contents of the entire file (listing 1a) reveals that these are indeed the only records that satisfy the query.

The remaining examples are interpreted as follows:

- Listing 5 prints all records such that the applicant has either a Bachelor or Master of Arts or Science *and* his major was computer science or mathematics.
- Listing 6 prints all records satisfying two conditions. The first condition is that the applicant has either a Bachelor or Master of Science degree with a major in mechanical engineering *or* his primary area of interest is product engineering and he has more than 1 year of experience in that area. The second condition is that the application is dated September, 1978, or later.
- Listing 7 prints all records such that the application is dated during October, 1978.
- Listing 8 prints all records such that the applicant's primary area of interest is technical research and he

Text continued on page 144

```
LNAME = JONES
DATE > 78/00/00

(a)

1 AND:
  2 INT1 = TECHNICAL RESEARCH
  2 EXP2 > 1

(b)

1 OR:
  2 AND:
    3 DEG = BS
    3 MJR = COMPUTER SCIENCE
    3 INT1 = COMPUTER SCIENCE
    3 EXP1 > 1
  2 AND:
    3 INT1 = COMPUTER SCIENCE
    3 EXP1 > 3

(c)
```

Figure 5: *Examples of valid data queries. Figure 5a presents two examples of simple (one condition) queries; note the absence of numbers at the beginning of the line. Figures 5b and 5c are compound (multiple condition) queries. Refer to the text for an English interpretation of these queries.*

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Listing 4: *A simple file query. In this dialogue, the user asks the computer for all records with an application date of November 1978 or later. The five records printed satisfy this criterion.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>DATE>78/11/00

REC#  3
DATE      =    78/11/08
LNAM      =    BLACKWELL
FNAM      =    LARRY
INIT      =    W
ADDR      =    8180 PALLISTER DETROIT MI
TEL#      =    871-9167
DEG       =    BA
MJR       =    GENERAL BUSINESS
INT1      =    SALES/MARKETING
INT2      =    PURCHASING
EXP1      =     4
EXP2      =     2

REC#  4
DATE      =    78/11/12
LNAM      =    KRAFT
FNAM      =    PATRICK
INIT      =    A
ADDR      =    26044 VILLAGE PLYMOUTH MI
TEL#      =    445-6176
DEG       =    MS
MJR       =    MATHEMATICS
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     2
EXP2      =     0

REC#  5
DATE      =    78/11/02
LNAM      =    HACKMAN
FNAM      =    GERALD
INIT      =    R
ADDR      =    292 CARDWELL TOLEDO OH
TEL#      =    222-5752
DEG       =    BA
MJR       =    GENERAL BUSINESS
INT1      =    SALES/MARKETING
INT2      =    QUALITY CONTROL
EXP1      =     7
EXP2      =     0

REC#  12
DATE      =    78/12/10
LNAM      =    PALINDROME
FNAM      =    ANTHONY
INIT      =    J
ADDR      =    43441 DARTMOUTH NOVI MI
TEL#      =    447-3902
DEG       =    BS
MJR       =    ELECTRICAL ENGRG
INT1      =    TECHNICAL RESEARCH
INT2      =    PRODUCT ENGRG
EXP1      =    15
EXP2      =     2

REC#  20
DATE      =    78/11/20
LNAM      =    SMITH
FNAM      =    HENRY
INIT      =    M
ADDR      =    130 BARD DEARBORN MI
TEL#      =    469-7412
DEG       =    MS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    NONE
EXP1      =     3
EXP2      =     0

ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

Listing 5: *A compound file query. The logical operators on a given level (the line number at the beginning of a line) link all entries of the next lowest level (the next higher line number). The query is for all applicants who have any degree (BA, BS, MA, or MS) in either mathematics or computer science. Three records satisfy this query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>     2 OR:
>         3 DEG=BS
>         3 DEG=BA
>         3 DEG=MA
>         3 DEG=MS
>     2 OR:
>         3 MJR=COMPUTER SCIENCE
>         3 MJR=MATHEMATICS
>

REC#  4
DATE      =    78/11/12
LNAM      =    KRAFT
FNAM      =    PATRICK
INIT      =    A
ADDR      =    26044 VILLAGE PLYMOUTH MI
TEL#      =    445-6176
DEG       =    MS
MJR       =    MATHEMATICS
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     2
EXP2      =     0

REC#  18
DATE      =    78/09/15
LNAM      =    KOHN
FNAM      =    ROBERT
INIT      =    C
ADDR      =    6565 ABNER SOUTHFIELD MI
TEL#      =    533-8452
DEG       =    BS
MJR       =    COMPUTER SCIENCE
INT1      =    COMPUTER PROGRAMMING
INT2      =    NONE
EXP1      =     1
EXP2      =     0
```

Listing 5 continued on page 138

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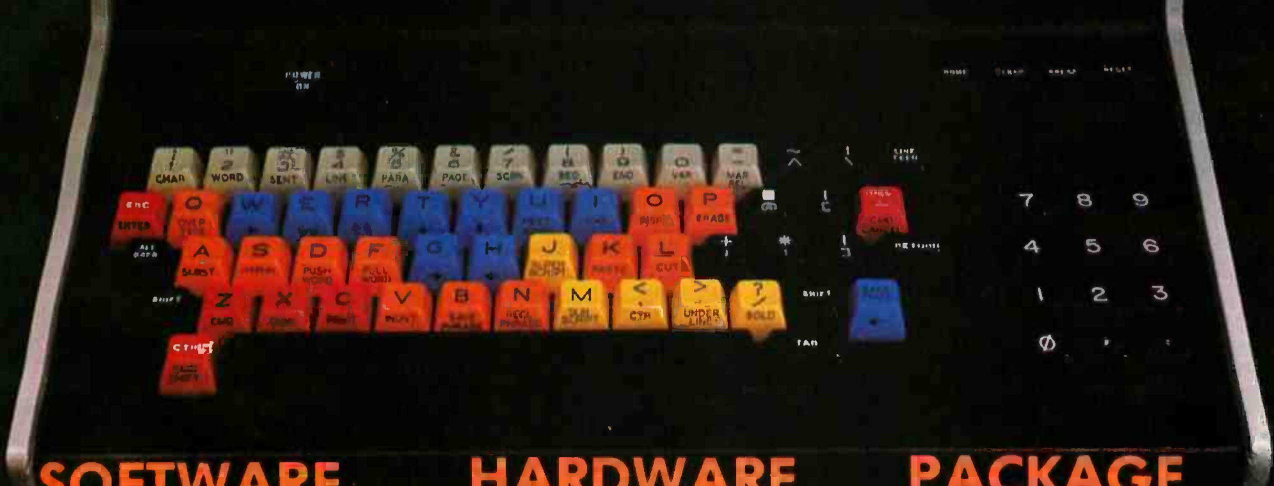

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Listing 5 continued:

```
REC#  21
DATE      =    78/07/06
LNAM      =    KYSER
FNAM      =    CYNTHIA
INIT      =    A
ADDR      =    5820 MULBERRY WAYNE MI
TEL#      =    666-9287
DEG       =    BS
MJR       =    COMPUTER SCIENCE
INT1      =    COMPUTER PROGRAMMING
INT2      =    TECHNICAL RESEARCH
EXP1      =     1
EXP2      =     0


ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

Listing 6: *A compound file query. The query being made is explained in the text. Four records satisfy this query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>     2 OR:
>          3 AND:
>               4 OR:
>                    5 DEG=BS
>                    5 DEG=MS
>               4 MJR=MECHANICAL ENGRG
>          3 AND:
>               4 INT1=PRODUCT ENGRG
>               4 EXP1>1
>          2 DATE>78/09/00
>


REC#  4
DATE      =    78/11/12
LNAM      =    KRAFT
FNAM      =    PATRICK
INIT      =    A
ADDR      =    26044 VILLAGE PLYMOUTH MI
TEL#      =    445-6176
DEG       =    MS
MJR       =    MATHEMATICS
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     2
EXP2      =     0


REC#  6
DATE      =    78/09/28
LNAM      =    MARCHANT
FNAM      =    HAROLD
INIT      =    R
ADDR      =    9670 TREELANE DEARBORN MI
TEL#      =    581-2553
DEG       =    BS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     1
EXP2      =     0


REC#  7
DATE      =    78/09/29
LNAM      =    MALST
FNAM      =    DENNIS
INIT      =    R
ADDR      =    1025 CHENE TOLEDO OH
TEL#      =    333-4714
DEG       =    MS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    TECHNICAL RESEARCH
EXP1      =     8
EXP2      =     2


REC#  20
DATE      =    78/11/20
LNAM      =    SMITH
FNAM      =    HENRY
INIT      =    M
ADDR      =    130 BARD DEARBORN MI
TEL#      =    469-7412
DEG       =    MS
MJR       =    MECHANICAL ENGRG
INT1      =    PRODUCT ENGRG
INT2      =    NONE
EXP1      =     3
EXP2      =     0


ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

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Listing 7: *A compound file query. The query is for all applications dated October, 1978. Four records satisfy this query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>      2 DATE>78/10/00
>      2 DATE <78/11/00
>


REC#  8
DATE        =     78/10/19
LNAM        =     DUNNING
FNAM        =     ALLAN
INIT        =     G
ADDR        =     1021 THIRD WYANDOTTE MI
TEL#        =     888-7326
DEG         =     BS
MJR         =     EDUCATION
INT1        =     COMPUTER PROGRAMMING
INT2        =     QUALITY CONTROL
EXP1        =       0
EXP2        =       2


REC#  9
DATE        =     78/10/05
LNAM        =     REDFORD
FNAM        =     KEVIN
INIT        =     D
ADDR        =     17504 RANIER ALLEN PARK MI
TEL#        =     277-4545
DEG         =     BA
MJR         =     ECONOMICS
INT1        =     QUALITY CONTROL
INT2        =     SALES/MARKETING
EXP1        =       3
EXP2        =       4


REC#  11
DATE        =     78/10/10
LNAM        =     MAYNARD
FNAM        =     STEPHEN
INIT        =     L
ADDR        =     36500 RUSHMORE FRANKLIN MI
TEL#        =     835-4202
DEG         =     MS
MJR         =     PSYCHOLOGY
INT1        =     INDUSTRIAL RELATIONS
INT2        =     SALES/MARKETING
EXP1        =       1
EXP2        =       0


REC#  13
DATE        =     78/10/04
LNAM        =     DAYTON
FNAM        =     THOMAS
INIT        =     F
ADDR        =     2125 TULANE WESTLAND MI
TEL#        =     666-3820
DEG         =     HS+
MJR         =     DRAFTING
INT1        =     DESIGN/DRAFTING
INT2        =     PRODUCT ENGRG
EXP1        =       6
EXP2        =       0


ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

Listing 8: *A compound file query. Here, the query is for an applicant who lists an MS in physics and a primary interest in technical research. No records satisfy this query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>     2 INT1=TECHNICAL RESEARCH
>     2 DEG=MS
>     2 MJR=PHYSICS
>
***NO RECORDS SATISFY THIS QUERY***
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

Listing 9: *A compound file query. The query is for any application put in by Anthony J Palindrome. Since this query has a unique response, one record satisfies the query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>     2 LNAM=PALINDROME
>     2 FNAM=ANTHONY
>     2 INIT=J
>

REC#  12
DATE      =    78/12/10
LNAM      =    PALINDROME
FNAM      =    ANTHONY
INIT      =    J
ADDR      =    43441 DARTMOUTH NOVI MI
TEL#      =    447-3902
DEG       =    BS
MJR       =    ELECTRICAL ENGRG
INT1      =    TECHNICAL RESEARCH
INT2      =    PRODUCT ENGRG
EXP1      =    15
EXP2      =     2

ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

Listing 10: *A compound file query. The query here is for the applications of all applicants whose last name begins with K. Three records satisfy this query.*

```
ENTER A COMMAND
#QUERY
ENTER NAME OF FILE TO QUERY
>EMPFL1
ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>P
>1 AND:
>     2 LNAM<L
>     2 LNAM>J
>

REC#  4
DATE      =    78/11/12
LNAM      =    KRAFT
FNAM      =    PATRICK
INIT      =    A
ADDR      =    26044 VILLAGE PLYMOUTH MI
TEL#      =    445-6176
DEG       =    MS
MJR       =    MATHEMATICS
INT1      =    PRODUCT ENGRG
INT2      =    MANUFACTURING ENGRG
EXP1      =     2
EXP2      =     0

REC#  18
DATE      =    78/09/15
LNAM      =    KOHN
FNAM      =    ROBERT
INIT      =    C
ADDR      =    6565 ABNER SOUTHFIELD MI
TEL#      =    533-8452
DEG       =    BS
MJR       =    COMPUTER SCIENCE
INT1      =    COMPUTER PROGRAMMING
INT2      =    NONE
EXP1      =     1
EXP2      =     0

REC#  21
DATE      =    78/07/06
LNAM      =    KYSER
FNAM      =    CYNTHIA
INIT      =    A
ADDR      =    5820 MULBERRY WAYNE MI
TEL#      =    666-9287
DEG       =    BS
MJR       =    COMPUTER SCIENCE
INT1      =    COMPUTER PROGRAMMING
INT2      =    TECHNICAL RESEARCH
EXP1      =     1
EXP2      =     0

ENTER PRINT/DELETE OPTIONS, AND QUERY (RETURN=CR)
>
ENTER A COMMAND
```

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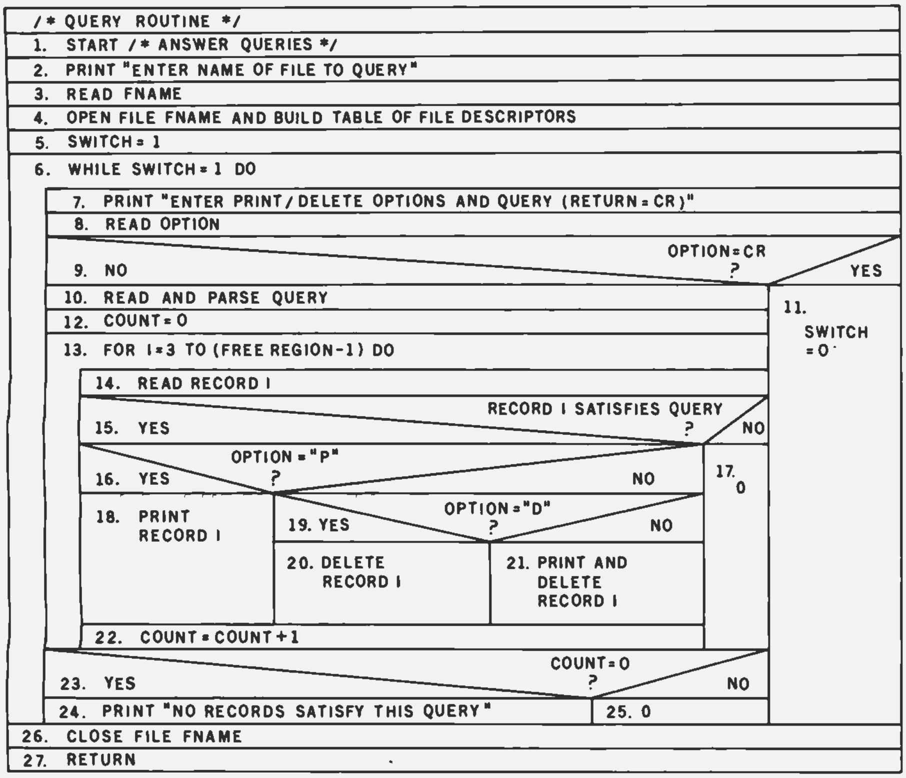

Figure 6: *Nassi-Schneiderman chart for the query-answering routine in segment 4. This routine prompts the user for the selection criteria of records to be listed and possibly deleted.*

Text continued from page 134:

has a Master of Science degree with a major in physics. (As can be seen, no records satisfy these conditions.)

- Listing 9 is a request for the record containing information about the applicant Anthony J Palindrome.
- Listing 10 is simply a request for all records such that the applicant's surname begins with a K.

Now that we have examined the query language and the operation of the query routine from the user's viewpoint, we will look at the algorithms that parse queries and determine whether or not records satisfy them.

The flowchart for the query routine is given in figure 6. It is self-explanatory with two major exceptions, steps 10 and 15. (Note that step 4 performs the same operations that were discussed with respect to the input routine.) To illustrate the parsing and answering of queries, follow an example through these operations. The query that will be parsed is that of listing 6 on page 138, and a trace of how it is answered for record number 4 will be followed.

The query is read in line by line as the user enters it. Once a line is read, it is broken down into components that are stored in one or more arrays as shown in figure 7a. After each line is read, it is left justified, and the first two characters are taken to be a level number, which is converted to integer form. Thus, the first line is found to have a level number of 1. The line is then shifted left, throwing away the level number and any succeeding blanks. Because the level number is expected first, tags may not use a number as the first character. If a level number is not found, it is assumed that the query is a simple one. The first four characters of the line are then examined to determine whether or not it is a logical operation. This is accomplished simply by checking for one of the character strings "AND:" or "OR:". The presence of a colon in the string is actually what identifies it as a logical operation, and this is the reason why tags may not use this character.

At this point, it is known that *line 1* is an AND operation. The type of operation and its level number are then put in array 1 as shown in figure 7a. No further processing of this line is

What's the difference between BASIC and Pascal?

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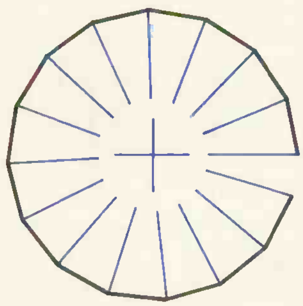
in BASIC

"This is easy . . ."

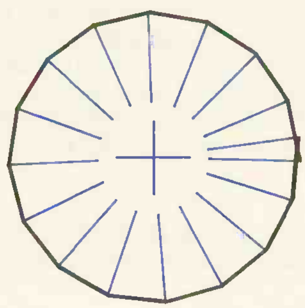
```
100 MOVE R,0
110 FOR T=0 TO 360 STEP 25
120 DRAW R*COS(T), R*SIN(T)
130 NEXT T
```



"Oops, didn't quite meet . . .

. . . but that's easy to fix."

```
100 MOVE R,0
110 FOR T=0 TO 360+25 STEP 25
120 DRAW R*COS(T), R*SIN(T)
130 NEXT T
```



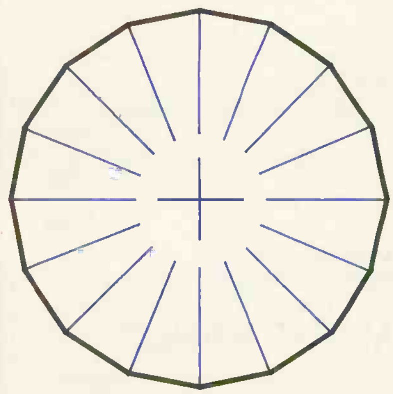
"Oh, now it closes . . .
in fact, it overlaps."

Programming by trial and error

in Pascal

"The simplest circle drawn with line segments is a regular polygon . . ."

```
procedure Circle (X, Y, Radius: real);
const Sides = 16; Pi = 3.14159265;
var    N : integer; Theta : real;
begin
   Move (X+Radius,Y);
   for N : = 1 to Sides do begin
      Theta : = 2 * Pi * (N/Sides);
      Draw (Radius * cos (Theta) + X,
               Radius * sin (Theta) + Y);
      end;
end;
```



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ARRAY 1: LEVEL AND LOGICAL OPERATOR (IF ANY)	ARRAY 2: TAG NUMBER	ARRAY 3: RELATIONAL OPERATOR	ARRAY 4: VALUE
AND,1			
OR,2			
AND,3			
OR,4			
5	7	=	BS
5	7	=	MS
4	8	=	MECHANICAL ENGRG
AND,3			
4	9	=	PRODUCT ENGRG
4	11	>	1
2	1	>	78/09/00

(a)

WORKING ARRAY

	1	2	3	4	5	6	7	8	9	10	11	12	13
5	AND,1	AND,1	1	1	1	1	1	1	1	1	1	1	1
4	OR,2	OR,2	0	0	0	0	0	0	0	0	1	-1	-1
3	AND,3	AND,3	1	1	1	1	1	1	0	-1	-1	-1	-1
2	OR,4	OR,4	0	0	0	0	1	-1	-1	-1	-1	-1	-1
	5	>	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1
	5	=	1	1	1	1	-1	-1	-1	-1	-1	-1	-1
	4	<	0	0	0	0	0	0	-1	-1	-1	-1	-1
1	AND,3	AND,3	1	1	1	1	1	1	1	1	-1	-1	-1
	4	=	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
	4	>	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1
	2	>	1	1	1	1	1	1	1	1	1	1	-1
	ANSWER SIMPLE QUERIES AND SET ANDS TO 1 - ORS TO 0			1		2		3		4		5	

(b)

Figure 7: *Classification of records according to the query criteria. Figure 7a demonstrates the breakdown of a set of query criteria (the query shown in listing 6) as the first step in determining whether or not a given record matches the query criteria. Figure 7b presents the process by which a record (record number 4) is compared against the query criteria. The algorithm for this process is given in table 3. The circled areas in steps 4 thru 13 show the amount of the array that has been or is being processed to evaluate the compound query line (one using a logical operation) with the number at the left-hand and bottom sides of figure 7b. The result of the comparison is in the upper right-hand number in the circled area.*

done. Lines 2 thru 4 are treated in a similar fashion and are also entered in array 1.

Line 5 is found to have a level number of 5. However, the check for a logical operator fails, and it must be parsed further. First, the line is scanned to find the relational operator. This having been found, the characters preceding it are isolated and compared to the table of tags until a match is made. In this case, it is tag number 7. A "7" is entered in array 2. The previously found relational operator is entered in array 3. The first nonblank character following the relational operator is then found and the remainder of the line is taken to be the value. This value is justified within a field according to the type associated with the tag found and is stored in array 4. The remainder of the lines in the query are further examples of the two cases that have just been detailed, and will result in the arrays shown in figure 7a.

Now that the query has been parsed, a trace will be followed (figure 7b) of how it is determined whether or not a record satisfies the query.

Since this process involves modifying array 1, a copy of it is made (we will refer to this copy as the *working array*). Obviously, this is necessary because the answering algorithm will

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be repeated for every record in the data base.

The first step is to answer all of the simple queries. In this case, there are six of them. They may be identified within array 1 by an entry consisting only of a level number. Thus, as array 1 is scanned from beginning to end, the first simple query encountered corresponds to line 5 ("DEC=BS"). The value to be used in the comparison is in the corresponding element of array 4, and the tag number, which will allow us to find the field in record 4 to compare this value to, is in the first element of array 2. Making the comparison, we find that the value in record 4 ("MS") is greater than the value in array 4 ("BS"). The results of this comparison replace the level number in the working array. The results of the tests indicated by the other five simple queries are entered in the working array in a completely analogous fashion. The results of this step are shown in column 2 of figure 7b.

Next, the results of the comparisons just made are compared with the corresponding relation stored in array 3. If they are the same, the entry in the working array is replaced by a 1 (true), otherwise with a 0 (false). For example, the first simple query (line 5) is false (the degree field does not equal "BS"). This is indicated by a 0 in the working array. Finally, ANDs are replaced by 1s and ORs by 0s. This completes the transformation from column 2 to column 3.

At this point, we are ready to perform the logical operations indicated. The algorithm which does this is given in table 3. Applying this algorithm to array 1 and the working array will yield the final result in the first element of the working array. In this case, that element is a 1 and, therefore, record 4 satisfies the query. The transformations that the working array goes through are shown in columns 4 thru 13 of figure 7b.

One last point should be made with respect to the flowchart of figure 6. This concerns steps 20 and 21 where records are deleted from the data base. A count n is kept of the number of records that satisfy a query, and when a record is encountered that does not, it is written to a new position within the file n records prior to its present position.

For example, if the file consists of six records, where record 3 satisfies the criteria for deletion, the process proceeds as follows. Record 1 is scanned; the value of n remains 0. Record 2 is then scanned; n remains 0. Because n is zero, no records are rewritten. Record 3 is next scanned and is found to be suitable for deletion. The value of n is increased to 1. Record 4 is scanned in turn and is found to be not suitable for deletion. The value of n stays at 1, but now record 4 is rewritten into position $4-n$ (ie: 3) within the file, thereby destroying record 3. When records 5 and 6 are examined, the value of n remains at 1, and record 5 is written into position 4 (ie: $5-n$) in the file, while record 6 goes into position 5 (ie: $6-n$). Once all records in the file have been checked, the file will be properly compacted and the pointer

```
1)  I = INDEX OF LAST ELEMENT OF ARRAY 1
2)  IF ARRAY 1 (I) ≠ LOGICAL OPERATION, GO TO 11
3)  LEVEL = LEVEL NUMBER IN ARRAY 1 (I)
4)  J = I
5)  IF LEVEL NUMBER IN ARRAY 1 (J + 1)< = LEVEL, GO TO 11
6)  IF WORKING ARRAY (J + 1) = - 1, GO TO 9
7)  IF ARRAY 1 (I) = 'AND', THEN WORKING ARRAY (I) = LOGICAL AND OF WORKING
      ARRAY (I) WITH WORKING ARRAY (J + 1)
    ELSE WORKING ARRAY (I) = LOGICAL OR OF WORKING ARRAY (I) WITH WORKING
      ARRAY (J + 1)
8)  WORKING ARRAY (J + 1= - 1
9)  J = J + 1
10) IF J< INDEX OF LAST ELEMENT OF ARRAY 1, GO TO 5
11) I = I - 1
12) IF I> = 1, GO TO 2
    ELSE STOP
```

Table 3: Algorithm for determining record status in relation to a compound query. This algorithm requires the record to be tested and the given query to be in the form of columns 1 thru 3 of figure 7b. It scans the table from bottom to top for the line with the highest-value level and a logical operator. It then calculates the result of that operation with all values below it having a higher-value level; then these lines just operated on are flagged as such with a −1. This operation is repeated until the entire query has been evaluated, giving a 1 if the record matches and a 0 otherwise.

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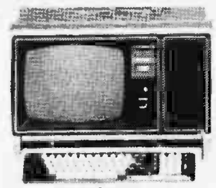

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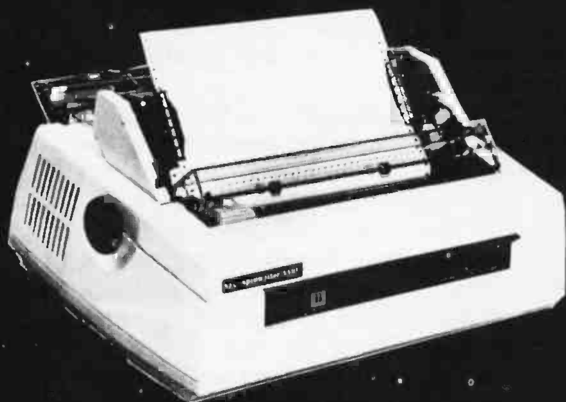

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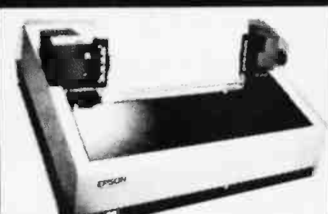

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to the first free region is updated by subtracting from it the number of records satisfying the query (ie: *n*).

General Observations

The information-retrieval system that has been described is quite flexible in several respects. It allows the user to define and organize his data in ways which are meaningful to him and to interrogate that data in a manner that imposes few restrictions. Further, it should be possible to implement this system on virtually any disk-based machine that supports FORTRAN IV. The problems encountered should be fairly minor.

The greatest difficulty encountered with the Hewlett-Packard System 1000 was the fact that the configuration of the operating system did not allow for memory partition sizes sufficient to contain all of the information retrieval system in a single object-code module. Because of this, it was necessary to use overlays. Fortunately, the code was easily segmented since the processes of file creation, data entry, and query answering are mutually exclusive.

Other difficulties were encountered because of the use of FORTRAN IV. Since the language does not allow character-string variables, and Hewlett-Packard's version does not include a byte-length data type of any description, the necessary character manipulation became a bit troublesome.

A previous implementation used PL/I (on an IBM System/360) and employed an alternate query language. The syntax of a simple query was the same (ie: [tag$_i$] [relational operator] [value]), with the exception of the use of enclosing parentheses. For example, the simple query of listing 4 becomes (DATE >78/11/00). These simple queries were combined using logical operators "&" (AND) and "|" (OR), and enclosing parentheses. Using this notation, the example of listing 7 becomes ((DATE>78/10/00) & (DATE<78/11/00)), and the example in listing 6 becomes (((((DEG=BS) | (DEG=MS)) & (MJR=MECHANICAL ENGRG)) | ((INT1=PRODUCT ENGRG) & (EXP1 > 1))) & (DATE >78/09/00)). This parenthesized form is obviously somewhat cumbersome when more complex queries are formed; the meaning is obscured by the notation. This provided the major motivation for the development of the query language present.

Having demonstrated the power of this system, it is also appropriate to mention some of its shortcomings and possible extensions to it. Although it is designed to handle most types of ASCII data, the representation of signed numbers poses a problem. For example, comparing the ASCII representation of the integers +123 and −123 will show that +123 is the smaller of the two, since "+" precedes "−" in the collating sequence.

Another limitation is that relations are not allowed between records. For example, if the personnel data base was to be extended to include a field for the name of the applicant's spouse, there would be no way to specify a query for a list of all applicants whose spouse had also filed an application. The only way to extract this information would be to manually check each application.

A final problem that should be mentioned concerns response time. For small data bases (perhaps a few hundred records or so) the response time should be quite tolerable. However, if the data base consists of several thousand records or more, the user could wait many minutes (or hours) for his reply. In this case, we prefer to be somewhat pragmatic by suggesting that this long response time is still better than searching all records manually.

If faster response times are necessary, the addition of secondary indices to the system should make a dramatic improvement. These indices would consist of small files (one for each field in a record) and would contain all unique values for a field along with pointers to the records containing the value. Thus, a query could be answered by examining a set of smaller files that normally would not need to be searched from beginning to end.

Another extension that would enhance the capabilities of the system is the inclusion of the logical operator NOT. This, along with AND and OR, would allow the synthesis of all Boolean operators (eg: NAND, NOR, XOR).

A final point concerns checking the syntax of queries. Although queries are checked for proper syntax on a line by line basis, there is no provision for checking the syntax of the entire query (eg: making sure that a logical operator is followed by at least two operands). In the present system, this responsibility is left to the user and it should be understood that errors will yield results that may be misleading.

In closing, it is important to emphasize that what has been presented is not intended to be a cookbook for the implementation of an information-retrieval system. However, we do feel that we have satisfied the goals stated at the outset and that the material presented is sufficiently comprehensive to allow other interested persons to implement similar systems and, perhaps, to expand upon ours. ■

The authors have developed a functionally-equivalent data-base package for the Radio Shack TRS-80 Model I microcomputer; the TRS-80 package uses the same query language and file structure as the FORTRAN system. Some additional features have been included, as well.

The TRS-80 package is coded partially in Disk BASIC and partially in Z80 assembly language, and it runs under version 2.2 of the TRSDOS operating system. For efficiency, the sort routine is coded entirely in assembly language.

The package is supplied on a single 5-inch floppy disk with a user's manual containing over one hundred pages. It may be obtained for $99.95 from:

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iCOM 3712	1.4	170/25 *
iCOM 3812	1.4	170/25 *
Mits 3202/Altair 8800	1.4	145/25
Heath H8 + H17	1.4	145/25
Heath H89	1.4	145/25
Heath H89 by Magnolia	1.4	250/25 ◇
Heath H89 by Magnolia	2.x	300/25 ◇
Onyx C8001	2.x	300/25 ◇
Ohio Scientific C3	2.x	200/25
TRS-80 Model I	1.4	145/25
TRS-80 Model II	2.x	170/25
TRS-80 Model II + Corvus	2.x	250/25
Processor Technology Helios II	1.4	145/25
Cromemco System 3	1.4	145/25
Intel MDS Single Density	1.4	145/25
Intel MDS Single Density	2.x	170/25
Micropolis Mod I	1.4	145/25
Micropolis Mod II	1.4	145/25

The following configurations are scheduled for release soon:

System	Version	Price
North Star Double/Quad + Corvus	2.x	250/25
North Star Horizon HD-1	2.x	250/25
Ohio Scientific C3-C	2.x	250/25
Micropolis Mod II	2.x	200/25
Mostek MDX STD Bus System	2.x	350/25 **
iCOM 3812	2.x	225/25 *
iCOM 4511/Pertec D3000	2.x	375/25 *+

*Software consists of the operating system, text editor, assembler, debugger and other utilities for file management and system maintenance. Complete set of Digital Research's documentation and additional implementation notes included. Systems marked * and ** include firmware on 2708 and 2716. Systems marked + include 5440 media charge. Systems marked Ⓜ require the special Ⓜ versions of software in this catalog. Systems marked Ⓥ have minor variants available to suit console interface of system. Call or write for full list of options. ◇ includes hardware addition to allow our standard versions of software to run under it.*

☐ **Z80 DEVELOPMENT PACKAGE**—Consists of: (1) disk file line editor, with global inter and intra-line facilities; (2) Z80 relocating assembler, Zilog/Mostek mnemonics, conditional assembly and cross reference table capabilities; (3) linking loader producing absolute Intel hex disk file .... $95/$20

☐ **ZDT**—Z80 Monitor Debugger to break and examine registers with standard Zilog/Mostek mnemonic disassembly displays. $35 when ordered with Z80 Development Package .... $50/$10

AVOCET SYSTEMS

☐ **XASM-68**—Non-macro cross-assembler with nested conditionals and full range of pseudo operations. Assembles from standard Motorola MC6800 mnemonics to Intel hex .... $200/$25

☐ **XASM-65**—As XASM-68 for MOS Technology MCS-6500 series mnemonics .... $200/$25

☐ **XASM-48**—As XASM-68 for Intel MCS-48 and UPI-41 families .... $200/$25

☐ **XASM-18**—As XASM-68 for RCA 1802 .... $200/$25

☐ **DISTEL**—Disk based disassembler to Intel 8080 or TDL/Xitan Z80 source code, listing and cross reference files. Intel or TDL/Xitan pseudo ops optional. Runs on 8080 .... $65/$10

☐ **DISILOG**—As DISTEL to Zilog/Mostek mnemonic files .... $65/$10

Software with Manual / Manual Alone

☐ **SMAL/80** Structured Macro Assembler Language—Package of powerful general purpose text macro processor and SMAL structured language compiler. SMAL is an assembler language with IF-THEN-ELSE, LOOP-REPEAT-WHILE, DO-END, BEGIN-END constructs .... $75/$15

PHOENIX SOFTWARE ASSOCIATES

☐ *New* **PASM***—Z80 macro assembler. Intel/TDL mnemonics. Generates Intel hex format or relocatable code in either TDL Object Module format or PSA Relocatable Binary Module format. Supports text insertion, conditional branching within macros, recursive macro calls and parameter passing .... $129/$25

☐ *New* **EDIT**—Character oriented text file editor. Includes macro definition capabilities. Handles insertion, deletion, searching, block move, etc. for files of any length. Does not require a CRT .... $129/$25

☐ *New* **PLINK***—Two pass disk-to-disk linkage editor/loader which can produce re-entrant, ROMable code. Can link programs that are larger than available memory for execution targeted on another machine. Full library capabilities. Input can be PSA Relocatable Binary Module, TDL Object Module or Microsoft REL files. Output can be a COM file, Intel hex file, TDL Object Module or PSA Relocatable file .... $129/$25

☐ *New* **BUG*** and **μ BUG***—Z80 interactive machine level debugging tools for program development. BUG has full symbolic trace and interactive assembly (mnemonics compatible with PASM). Dynamic breakpoints and conditional traps while tracing (even through ROM!). μ BUG is a subset of BUG and is used in memory limited situations .... $129/$25

DIGITAL RESEARCH

☐ **MP/M**—Installed for single density MDS-800. Multi-processing derivative of the CP/M operating system. Manual includes CP/M2 documentation .... $300/$50

☐ **MAC-8080**—Macro assembler. Full Intel macro definitions. Pseudo Ops include RPC, IRP, REPT, TITLE, PAGE, and MACLIB. Produces absolute hex output plus symbol table file for use by SID and ZSID (see below) $120/$15

☐ **SID-8080**—Symbolic debugger. Full trace, pass count and breakpoint program testing. Has backtrace and histogram utilities. When used with MAC, provides full symbolic display of memory labels and equated values . $105/$15

☐ **ZSID-Z80**—Symbolic debugger with all features of SID .... $130/$15

☐ **TEX**—Text output formatter to create paginated, page-numbered and justified copy. Output can be directed to printer or disk ... $105/$15

☐ **DESPOOL**—Utility program to permit simultaneous printing from text files while executing other programs .... $80/$10

☐ **tiny C**—Interactive interpretive system for teaching structured programming techniques. Manual includes full source listings . $105/$50

☐ **BDS C COMPILER**—Supports most features of language, including Structures, Arrays, Pointers, recursive function evaluation, overlays. Includes linking loader, library manager, and library containing general purpose, file I/O, and floating point functions. Lacks initializers, statics, floats and longs. Documentation includes "The C PROGRAMMING LANGUAGE" by Kernighan and Ritchie .... $145/$25

☐ **WHITESMITHS C COMPILER**—The ultimate in systems software tools. Produces faster code than a pseudo-code Pascal with more extensive facilities. Conforms to the full UNIX* Version 7 C language, described by Kernighan and Ritchie, and makes available over 75 functions for performing I/O, string manipulation and storage allocation. Linkable to Microsoft REL files. Requires 60K CP/M .... $630/$30

MICROSOFT

☐ **BASIC-80**—Disk Extended BASIC, ANSI compatible with long variable names, WHILE/WEND, chaining, variable length file records .... $325/$25

☐ **BASIC COMPILER**—Language compatible with BASIC-80 and 3-10 times faster execution. Produces standard Microsoft relocatable binary output. Includes MACRO-80. Also linkable to FORTRAN-80 or COBOL-80 code modules .... $350/$25

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☐ **FORTRAN-80**—ANSI 66 (except for COMPLEX) plus many extensions. Includes relocatable object compiler, linking loader, library with manager. Also includes MACRO-80 (see below) .... $425/$25

☐ **COBOL-80**—Level 1 ANSI '74 standard COBOL plus most of Level 2. Full sequential, relative, and indexed file support with variable file names. STRING, UNSTRING, COMPUTE, VARYING/UNTIL, EXTEND, CALL, COPY, SEARCH, 3-dimensional arrays, compound and abbreviated conditions, nested IF. Powerful interactive screen-handling extensions. Includes compatible assembler, linking loader, and relocatable library manager as described under MACRO-80 .... $700/$25

☐ **MACRO-80**—8080/Z80 Macro Assembler. Intel and Zilog mnemonics supported. Relocatable linkable output. Loader, Library Manager and Cross Reference List utilities included .... $149/$15

☐ *New* **muSIMP/muMATH**—muSIMP is a high level programming language suitable for symbolic and semi-numerical processing. Implemented using a fast and efficient interpreter requiring only 7K bytes of machine code. muMATH is a package of programs written in muSIMP. The package performs sophisticated mathematical functions. Keeps track of up to 611 digits. Performs matrix operations on arrays: transpose, multiply, divide, inverse and other integer powers. Logarithmic, exponential, trigonometric simplification and transformation, symbolic differentiation with partial derivatives, symbolic integration of definite and indefinite integrals. Requires 40K CP/M .... $250/$20

☐ *New* **muLISP-79**—Microcomputer implementation of LISP. The interpreter resides in only 7K bytes of memory yet includes 83 LISP functions. Has infinite precision integer arithmetic expressed in any radix from 2 to 36. muLISP-79 includes complete trace facility and a library of useful functions and entertaining sample programs .... $200/$15

☐ **XMACRO-86**—8086 cross assembler. All Macro and utility features of MACRO-80 package. Mnemonics slightly modified from ASM86. Compatibility data sheet available .... $275/$25

☐ **EDIT-80**—Very fast random access text editor for text with or without line numbers. Global and intra-line commands supported. File compare utility included .... $89/$15

☐ **PASCAL/M***—Compiles enhanced Standard Pascal to compressed efficient Pcode. Totally CP/M compatible. Random access files. Both 16 and 32-bit integers. Runtime error recovery. Convenient STRINGs. OTHERWISE clause on CASE. Comprehensive manual (90 pp. indexed). SEGMENT provides overlay structure. INPORT, OUTPORT and untyped files for arbitrary I/O. Requires 56K CP/M. Specify 1) 8080 CP/M, 2) Z80 CP/M, or 3) Cromemco CDOS .... $175/$20

☐ **PASCAL/Z**—Z80 native code PASCAL compiler. Produces optimized, ROMable re-entrant code. All interfacing to CP/M is through the support library. The package includes compiler, relocating assembler and linker, and source for all library modules. Variant records, strings and direct I/O are supported. Requires 56K CP/M .... $395/$25

☐ **PASCAL/MT**—Subset of standard PASCAL. Generates ROMable 8080 machine code. Symbolic debugger included. Supports interrupt procedures. CP/M file I/O and assembly language interface. Real variables can be BCD, software floating point, or AMD 9511 hardware floating point. Includes strings enumerations and record data types. Manual explains BASIC to PASCAL conversion. Requires 32K .. $250/$30

☐ *New* **APL/V80**—Concise and powerful language for application software development. Complex programming problems are reduced to simple expressions in APL. Features include up to 27K active workspace, shared variables, arrays of up to 8 dimensions, disk workspace and copy object library. The system also supports auxiliary processors for interfacing I/O ports. Requires 48K CP/M and serial APL printing terminal or CRT .... $500/$30

☐ **ALGOL-60**—Powerful block-structured language compiler featuring economical run-time dynamic allocation of memory. Very compact (24K total RAM) system implementing almost all Algol 60 report features plus many powerful extensions including string handling direct disk address I/O etc. .... $199/$20

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MICRO FOCUS

☐ **STANDARD CIS COBOL**—ANSI '74 COBOL standard compiler fully validated by U.S. Navy tests to ANSI level 1. Supports many features to level 2 including dynamic loading of COBOL modules and a full ISAM file facility. Also, program segmentation, interactive debug and powerful interactive extensions to support protected and unprotected CRT screen formatting from COBOL programs used with any dumb terminal .... $850/$50

Software with Manual / Manual Alone

☐ **FORMS 2**—CRT screen editor. Output is COBOL data descriptions for copying into CIS COBOL programs. Automatically creates a query and update program of indexed files using CRT protected and unprotected screen formats. No programming experience needed. Output program directly compiled by STANDARD CIS COBOL .... $200/$20

EIDOS SYSTEMS

☐ **KISS**—Keyed Index Sequential Search. Offers complete Multi-Keyed Index Sequential and Direct Access file management. Includes built-in utility functions for 16 or 32 bit arithmetic, string/integer conversion and string compare. Delivered as a relocatable linkable module in Microsoft format for use with FORTRAN-80 or COBOL-80, etc. .... $335/$23

☐ **KBASIC**—Microsoft Disk Extended BASIC version 4.51 integrated by implementation of nine additional commands in language. Package includes KISS. REL as described above, and a sample mail list program. ... $585/$45
To licensed users of Microsoft BASIC-80 (MBASIC) .... $435/$45

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Integer CP/M	$350/$25
Extended ROM squared	$450/$25
Extended CP/M	$450/$25
Extended Disk CP/M	$550/$25
Integer CP/M Run Time Compiler	$350/$25
Extended CP/M Run Time Compiler	$450/$25

☐ **RECLAIM**—A utility to validate media under CP/M. Program tests a diskette or hard disk surface for errors, reserving the imperfections in invisible files, and permitting continued usage of the remainder. Essential for any hard disk. Requires CP/M version 2. .... $80/$5

☐ **BASIC UTILITY DISK**—Consists of: (1) CRUNCH-14—Compacting utility to reduce the size and increase the speed of programs in Microsoft BASIC 4.51, BASIC-80 and TRS-80 BASIC. (2) DPFUN—Double precision subroutines for computing nineteen transcendental functions including square root, natural log, log base 10, sine, arc sine, hyperbolic sine, hyperbolic arc sine, etc. Furnished in source on diskette and documentation .... $50/$35

☐ **STRING/80**—Character string handling plus routines for direct CP/M BDOS calls from FORTRAN and other compatible Microsoft languages. The utility library contains routines that enable programs to chain to a COM file, retrieve command line parameters and search file directories with full wild card facilities. Supplied as linkable modules in Microsoft format. $95/$20

☐ **STRING/80** source code available separately $295/NA

☐ **THE STRING BIT**—FORTRAN character string handling. Routines to find, fill, pack, move, separate, concatenate and compare character strings. This package completely eliminates the problems associated with character string handling in FORTRAN. Supplied with source .... $65/$15

☐ **VSORT**—Versatile sort/merge system for fixed length records with fixed or variable length fields. VSORT can be used as a stand-alone package or loaded and called as a subroutine from CBASIC-2. When used as a subroutine, VSORT maximizes the use of buffer space by saving the TPA on disk and restoring it on completion of sorting. Records may be up to 255 bytes long with a maximum of 5 fields. Upper/lower case translation and numeric fields supported .... $175/$20

☐ **CPM/374X**—Has full range of functions to create or re-name an IBM 3741 volume, display directory information and edit the data set contents. Provides full file transfer facilities between 3741 volume data sets and CP/M files .... $195/$10

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☐ **STANDARD TAX**—As above for schedules A, B, C, D, E, G, R/RP, SE, TC and forms 2106 and 2441. Also, does not maintain client history files .... $495/$30

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Software with Manual / Manual Alone

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New

☐ **BSTAM**—Utility to link one computer to another also equipped with BSTAM. Allows file transfers at full data speed (no conversion to hex), with CRC block control check for very reliable error detection and automatic retry. We use it! It's great! Full wildcard expansion to send *. COM, etc. 9600 baud with wire. 300 baud with phone connection. Both ends need one. Standard and Ⓗ versions can talk to one another. .$150/$10

☐ **WHATSIT?***—Interactive data-base system using associative tags to retrieve information by subject. Hashing and random access used for fast response. Requires CBASIC-2 .$175/$25

☐ **SELECTOR III-C2**—Data Base Processor to † create and maintain multi-key data bases. Ⓗ Prints formatted sorted reports with numerical summaries or mailing labels. Comes with sample applications, including Sales Activity, Inventory, Payables, Receivables, Check Register, and Client/Patient Appointments, etc. Requires CBASIC-2. Supplied in source .... $295/$20

☐ **GLECTOR**—General Ledger option to SELECTOR III-C2. Interactive system provides for customized COA. Unique chart of transaction types insure proper double entry bookkeeping. Generates balance sheets, P&L statements and journals. Two year record allows for statement of changes in financial position report. Supplied in source. Requires SELECTOR III-C2, CBASIC-2 and 56K system. .... $350/$25

☐ **CBS**—Configurable Business System is a comprehensive set of programs for defining custom data files and application systems without using a programming language such as BASIC, FORTRAN, etc. Multiple key fields for each data file are supported. Set-up program customizes system to user's CRT and printer. Provides fast and easy interactive data entry and retrieval with transaction processing. Report generator program does complex calculations with stored and derived data, record selection with multiple criteria, and custom formats. Sample inventory and mailing list systems included. No support language required .... $295/$40

MICRO DATA BASE SYSTEMS

☐ **HDBS**—Hierarchical Data Base System. CODASYL oriented with FILEs, SETs, RECORDs and ITEMs which are all user defined. ADD, DELETE, UPDATE, SEARCH, and TRAVERSE commands supported. SET ordering is sorted, FIFO, LIFO, next or prior. One to many set relationship supported. Read/write protection at the FILE level. Supports FILEs which extend over multiple floppy or hard disk devices.

☐ **MDBS**—Micro Data Base System. Full network data base with all features of HDBS plus multi-level read/write protection for FILE, SET, RECORD and ITEM. Explicit representation of one to one, one to many, many to many, and many to one SET relationships. Supports multiple owner and multiple record types within SETs. HDBS files are fully compatible.

☐ HDBS-Z80 version .... $250/$40**

☐ MDBS-Z80 version .... $750/$40**
8080 version available at $75 extra.

When ordering, specify one of the language interfaces listed below. Additional language interfaces available at time of purchase for $100 or $125 if purchased later.

**The single manual covering HDBS and MDBS when purchased alone comes without specific language interface manual. Manuals are also available for the following Microsoft languages:

1) MBASIC 4.51, 2) BASIC-80 5.0, 3) Compiled BASIC or FORTRAN-80, 4) COBOL-80, 5) MACRO-80. .... $NA/$10

MICROPRO

☐ **SUPER-SORT I**—Sort, merge, extract utility as Ⓛ absolute executable program or linkable module in Microsoft format. Sorts fixed or variable records with data in binary, BCD, Packed Decimal, EBCDIC, ASCII, floating & fixed point, exponential, field justified, etc. Even variable number of fields per record! .... $225/$25

☐ **SUPER-SORT II**—Above available as abso- Ⓛ lute program only .... $175/$25

☐ **SUPER-SORT III**—As II without SELECT/ Ⓛ EXCLUDE .... $125/$25

☐ **DATASTAR**—Professional forms control entry Ⓛ and display system for key-to-disk data capture. Menu driven with built-in learning aids. Input field verification by length, mask, attribute (i.e. upper case, lower case, numeric, auto-dup, etc.). Built-in arithmetic capabilities using keyed data, constant and derived values. Visual feedback for ease of forms design. Files compatible with CP/M-MP/M supported languages. Requires 32K CP/M .... $350/$35

Software with Manual / Manual Alone

☐ **WORD-STAR**—Menu driven visual word pro- Ⓛ cessing system for use with standard terminals. Text formatting performed on screen. Facilities for text paginate, page number, justify, center and underscore. User can print one document while simultaneously editing a second. Edit facilities include global search and replace, Read/Write to other text files, block move, etc. Requires CRT terminal with addressable cursor positioning .... $445/$40

☐ **WORD-STAR-MAIL-MERGE**—As above with Ⓛ option for production mailing of personalized documents with mail lists from DATASTAR or NAD .... $575/$40

☐ **WORD-STAR Customization Notes**—For sophisticated users who do not have one of the many standard terminal or printer configurations in the distribution version of WORD-STAR .... $NA/$95

☐ **WORD-MASTER** Text Editor—In one mode Ⓛ has superset of CP/M's ED commands including global searching and replacing, forwards and backwards in file in video mode, provides full screen editor for users with serial addressable-cursor terminal .... $145/$25

☐ **TEXTWRITER III**—Text formatter to justify and Ⓗ paginate letters and other documents. Special features include insertion of text during execution from other disk files or console, permitting recipe documents to be created from linked fragments on other files. Has facilities for sorted index, table of contents and footnote insertions. Ideal for contracts, manuals, etc. Now compatible with Electric Pencil* and Word-Star prepared files .... $125/$20

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APARTMENT MANAGEMENT	$805/$40
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☐ **POSTMASTER**—A comprehensive package Ⓗ for mail list maintenance that is completely menu driven. Features include keyed record extraction and label production. A form letter program is included which provides neat letters on single sheet or continuous forms. Includes NAD file translator. Requires CBASIC-2 .... $150/$20

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New Manual

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ACCOUNTS PAYABLE	$820/$40
PAYROLL	$820/$40
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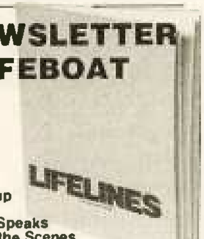

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CONDIMENTS

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☐ **FLIPPY DISK KIT**—Template and instructions to modify single sided 5¼" diskettes for use of second side in single sided drives $12.50

☐ **FLOPPY SAVER**—Protection for center holes for 5" and 8" floppy disks. Only 1 needed per diskette. Kit contains centering post, pressure tool and tough 7 mil mylar reinforcing rings for 25 diskettes.

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☐ **PASCAL USER MANUAL AND REPORT**—By Jensen and Wirth. The standard textbook on the language. Recommended for use by Pascal/Z, Pascal/M and Pascal/MT users $12

☐ **THE C PROGRAMMING LANGUAGE**—By Kernighan and Ritchie. The standard textbook on the language. Recommended for use by BDS C, tiny C, and Whitesmiths C users . $12

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Hearty Appetite.

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† Recommended system configuration consists of 48K CP/M, 2 full size disk drives, 24 x 80 CRT and 132 column printer.

Ⓗ Modified version available for use with CP/M as implemented on Heath and TRS-80 Model I computers.

Ⓛ User license agreement for this product must be signed and returned to Lifeboat Associates before shipment may be made.

Ⓘ This product Includes/eXcludes the language Ⓧ manual recommended in Condiments.

Ⓢ Serial number of CP/M system must be supplied with orders.

Ⓩ Requires Z80 CPU.

Ordering Information

MEDIA FORMAT ORDERING CODES
When ordering, please specify format code.

LIFEBOAT ASSOCIATES MEDIA FORMATS LIST
Diskette, cartridge disk and cartridge tape format codes to be specified when ordering software for listed computer or disk systems. All software products have specific requirements in terms of hardware or software support, such as MPU type, memory size, support operating system or language.

Computer system	Format Code
Altair 8800 Disk	See MITS 3200
Altos	A1*
Apple + SoftCard 13 Sector	RG
Apple + SoftCard 16 Sector	RR
BASF System 7100	RD
Blackhawk Single Density	Q3
Blackhawk Micropolis Mod II	Q2
CDS Versatile 3B	O1
CDS Versatile 4	Q2
COMPAL-80	Q2
Cromemco System 3	A1*
Cromemco Z2D	R6
CSSN BACKUP (tape)	T1 #
Delta	A1*
Digi-Log Microterm II	RD
Digital Microsystems	A1*
Discus	See Morrow Discus
Durango F-85	RL
Dynabyte DB8/2	R1
Dynabyte DB8/4	A1*
Exidy Sorcerer + Lifeboat CP/M	Q2
Exidy Sorcerer + Exidy CP/M	Q4
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Heath H89 + Magnolia CP/M	P7
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iCOM 3712	A1
iCOM 3812	A1*
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IMSAI VDP-80	A1**
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Meca 5¼"	P6
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Tarbell	A1*
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TEI 8"	A1*
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TRS-80 Model I + Omikron 5¼"	RM
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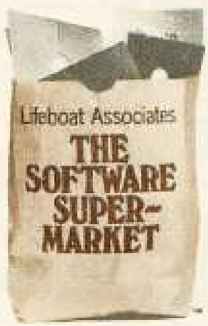

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Assembly language is *the* most powerful language available to a given processor. Within the limitations of time and human patience, it allows the most intricate manipulation of data, the smallest program size, and the fastest execution time possible. The drawback is that writing programs in assembly language is very tedious, often involving repeated writing of either identical code or code that is similar to previously written code.

One software tool that can help to decrease the tedium of assembly-language programming is the *macro assembler*. A macro assembler allows you to write one line of assembly-language code (called a *macro instruction* or just *macro*) that is *expanded* to (or replaced by) a predefined sequence of assembly-language statements; this saves you from entering the same code a second time. The original assembly-language file containing the macro statements generates the new expanded assembly-language file; this second file, which contains only valid assembly-language statements, can then be assembled, modified, or stored by the user.

The flowcharts in this article detail the process of defining and using macro instructions. The flowcharts can be used either to incorporate a macro facility into an assembler that you are designing or to write a macro-preprocessing program, the output of which is an expanded assembly-language source listing that can be assembled by your existing assembler.

How a Macro Instruction Works

Your first question might well be, "What on earth is a macro instruction, anyway?" To answer this question, consider the following simple example: you are writing a program that manipulates character strings and you have a series of instructions for moving a string of characters from one location to another. You need this routine in many places in your coding. You can store the sending and receiving field addresses, and the length, then call a common subroutine to perform the move.

> One software tool that can help to decrease the tedium of assembly-language programming is the *macro assembler*.

However, suppose you need this routine in several different programs; or maybe memory is not a concern and you have decided to code the statements in-line whenever needed in order to speed up your execution. After writing that move routine over and over, your hand is aching and you are looking for a better way. That better way is called a *macro assembler*. The macro assembler lets you define a new operation code, called MOVE in this example. This new operation code will generate the required sequence of instructions every time it is encountered in your programs by the macro assembler.

There are several advantages to using macro instructions. One advantage, as pointed out in the previous example, is that you need to write the macro definition only once; you can then enter one line of source code to generate the sequence of instructions that you have previously defined. This makes it easier for you, as a programmer, to write your program. It can also reduce program errors, since you know that the generated instructions will work after you test them the first time.

Macro instructions make possible a greater standardization of code, ensuring that a set sequence of source statements is used to perform a desired operation. Almost all highly developed assembly languages have macro expansion facilities. My article is based primarily upon the macro language used in the IBM System/360 and 370 assemblers.

Basically, a macro processor takes the place of an assembler's text input routine. It is a preprocessor of text statements, replacing a macro statement with its defined sequence of instructions. This generation of source text may also include substitution of operands within the macro statement. In addition to text generation and substitution, a macro facility might handle *conditional assembly*. This is the ability to vary the sequence of statements generated at assembly time, either within a macro definition or in the normal source code of the program.

Before using a macro instruction in a source program, you must first provide the assembler with a definition

Listing 1: *Example of a macro-instruction definition for an 8080 macro assembler. A macro definition is delineated by the first statement, MACRO, and the last statement, MEND (macro end). MACRO and MEND are pseudo-operation codes, which provide instructions to the assembler rather than generate machine code. The second line is called a prototype statement because it gives the name of the macro definition (here, MOVE) and the names of the variable symbols that will be used within the macro definition (denoted by an ampersand, &).*

```
 1.          MACRO
 2.  &JUMP   MOVE     &TO,&FROM,&LENGTH
 3.          LXI      B,&TO           POINT TO FROM AND TO FIELDS
 4.          LXI      D,&FROM
 5.          MVI      H,&LENGTH       SET MOVE LENGTH
 6.  &JUMP   LDAX     D               PICK UP "FROM" BYTE
 7.          STAX     B               STORE IN "TO" FIELD
 8.          INX      B               INCR FROM AND TO ADDRESSES
 9.          INX      D
10.          DCR      H               DECREMENT COUNT
11.          JNZ      &JUMP           LOOP BACK IF MORE
12.          MEND
```

of the macro instruction. This definition includes the macro name (the new operation code you have assigned), the label entry (if used), and the possible operands that can be used. The definition also includes the statements to be generated. The macro definition, then, consists of four parts: the macro header, the macro prototype, a sequence of model statements, and a macro trailer. The header and trailer define the beginning and the end of the macro definition. The macro prototype specifies the label entry, operation code, and operands permitted in the macro statement. The model statements are the assembler statements to be generated by the macro statement; the model statements eventually replace each occurrence of the macro statement.

Listing 1 shows a macro definition for the MOVE macro instruction discussed earlier. The numbers to the left of each statement are not a part of the definition, but are there solely for ease in discussing the definition itself. Also, the code shown is not necessarily the best way to perform a move operation, but serves only as an example. In this definition, statements 1 and 12 are the macro header and trailer, respectively. Statement 2 is the prototype, which defines the operation code (MOVE), the label entry (&JUMP), and the allowable operands (&TO, &FROM, &LENGTH). Statements 3 thru 11 are the model statements that will be generated.

Defining and Using Variable Symbols

As you can see, a macro definition is quite easy to write. The only thing that may seem new or unusual at this point are those four names that begin with an "&", known as *variable symbols*. While they may look strange, variable symbols are the single most important part of a macro definition, because they allow you to change the generated code. Without them, the uses of a macro assembler would be severely limited.

A variable symbol is a symbol that can take on many values. These values may be assigned by the assembler, or the programmer may assign them when he or she codes a macro instruction (or *macro call*) in the source program. When the macro processor expands a macro statement into its generated code, all variable symbols found in the model statements are replaced with the current values assigned to them. Referring to listing 1, when you code the MOVE macro instruction in your program, the first variable symbol, &TO, is given the value that you coded for your first operand, and so on.

To illustrate this operation, listing 2a shows a MOVE macro definition you might have coded in your program. Listing 2b shows the code generated by the MOVE macro definition of listing 1. Notice that in the generated code, &JUMP, &TO, &FROM, and &LENGTH in the model statements have been replaced by LOOP, FIELDA, FIELDB, and 14, respectively, from the macro-call statement.

Some variable symbols are assigned values by the assembler itself. Referring to listing 3a, use of the INCR macro definition in several places in your coding will result in the label LABEL being defined more than once, a condition that your assembler is likely to interpret as an error. One way to prevent this is to have a special variable symbol, *called* &SYSNDX, for *system index*. This variable symbol has a numeric value that is incremented by one every time a macro instruction is used. By combining this with a letter (known as *concatenating*), as in listing 3b, we can create unique labels. Listings 3c and 3d show the generated code from this macro instruction the first two times it is used. Notice that the two labels are different.

This brings up one more point concerning variable symbols. In listing 3b is the concatenation L&SYSNDX,

Listing 2: *Example of macro-instruction expansion. When the one-line macro call of the macro definition MOVE (listing 2a) is processed within a larger assembly-language program, it is replaced with the expanded macro code, as in listing 2b. Compare this with the macro definition in listing 1.*

```
(a)  LOOP   MOVE   FIELDA,FIELDB,14

(b)         LXI    B,FIELDA POINT TO FROM AND TO FIELDS
            LXI    D,FIELDB
            MVI    H,14 SET MOVE LENGTH
     LOOP   LDAX   D PICK UP "FROM" BYTE
            STAX   B STORE IN "TO" FIELD
            INX    B INCR FROM AND TO ADDRESSES
            INX    D
            DCR    H DECREMENT COUNT
            JNZ    LOOP LOOP BACK IF MORE
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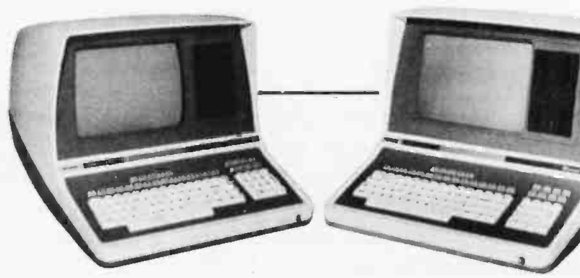

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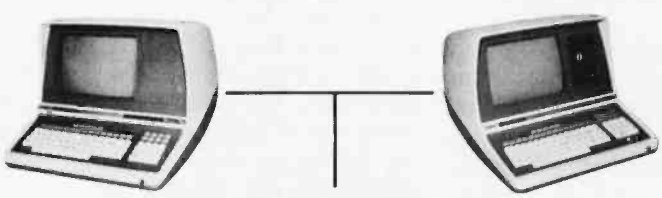

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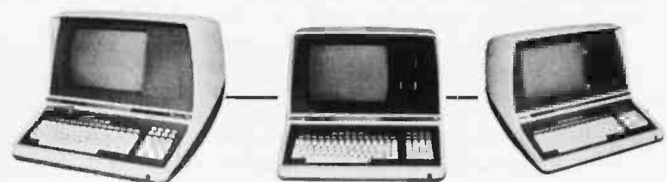

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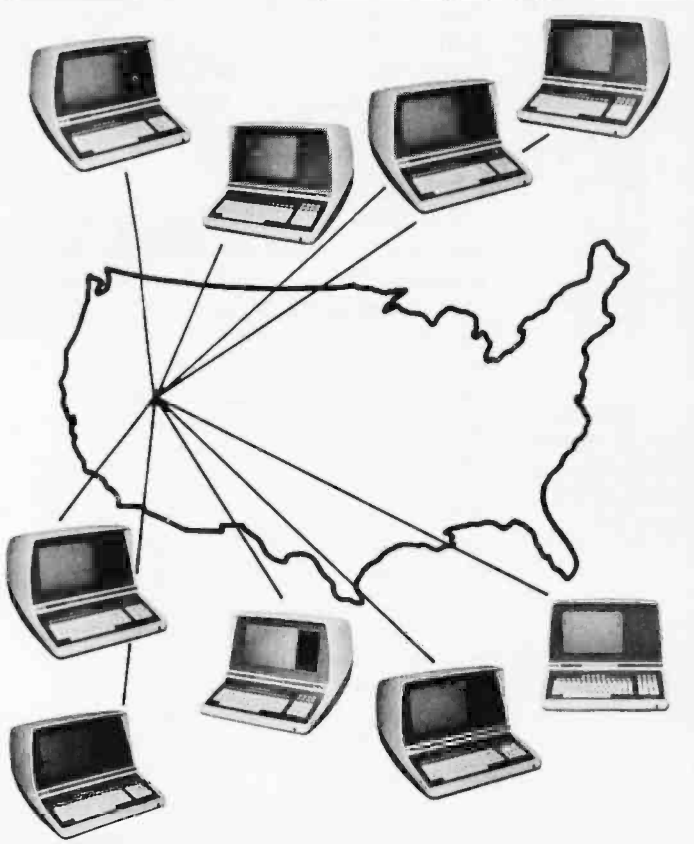

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The macro processor is itself a smaller assembler within the main assembler.

which generated L0001. Suppose we wanted to generate L0001A. Our first thought might be to code it as L&SYSNDXA. However, this presents a problem to the macro processor; it has no way of knowing that you wanted the variable symbol &SYSNDX with an A concatenated behind it. The macro processor thinks you want a variable symbol called &SYSNDXA.

To circumvent this problem, we will set a rule that a variable symbol must be followed by a blank, a special character other than a letter or number, or a period to mark its end. If the variable symbol is followed by a period, both the variable symbol and the period will be replaced in the generated code. Thus, we would now code L&SYSNDX.A in order to generate L0001A, or L&SYSNDX(1) to generate L0001(1).

Details of the Macro Assembler

Now that we have defined a macro call and discussed how it is used, we should look at the process of implementing macro-expansion facilities in an assembler. First, however, it would be useful to compare a macro processor to an assembler, for the macro processor is itself a smaller assembler within the main assembler. Both the assembler and the macro processor need a symbol table. In the assembler, this symbol table stores names associated with specific memory locations. Defining a name more than once is usually an error, so the symbol table need store only one entry for each name. For best storage usage, the assembler normally uses a hashing function to store names randomly but evenly distributed in the symbol table, and the symbol table is usually a constant length.

In a macro processor, the symbol table is handled quite differently. The macro processor stores variable symbols and pointers to their current values as entries in the symbol table. If we allow inner macro capability (where a macro definition contains a call to another macro definition), it is possible to have the same variable symbol defined more than once, each definition pointing to a different value.

As an example of this, listing 4a shows a macro definition, SAVE, which stores a specified register at the address in the HL register pair. Line 4 contains a call of the INCR macro definition, listing 4b, to increment the HL pair and count the number of calls to it in the specified register. Both macro definitions refer to &REG, but there are actually two different &REGs, each with a different value. If the macro call is coded as shown in listing 4c, &REG gets replaced with a D in line 1 of the generated code in listing 4d, and with a B in line 3 of listing 4d.

To allow this capability, we will use a *stack*, or pushdown list, for the macro processor's symbol table. The pushdown list is a last-in, first-out list; when a macro expansion needs to find the value associated with a given variable symbol, it will start with the last (or most recent) entry, looking backwards for the most recent definition of the symbol. In this way, &REG can be put on the symbol table with a value of D, and later put on the symbol table again with a value of B. When the inner INCR macro statement has completed its expansion, it will delete its entries from the end of the symbol table. This uncovers the old &REG and resets it back to a value of D, as shown in line 4 of listing 4d.

One major difficulty encountered by an assembler is in resolving forward references. These occur when a symbol being used has not yet been defined. The assembler cannot get the memory location of the symbol from its symbol table since the definition has not yet been processed. The nor-

Listing 3: *Fixed and assembler-assigned labels. In the macro definition of INCR in listing 3a, each macro call results in a line generated with the label LABEL. This would give the same label to two statements if INCR were called twice within the same program. To bypass this program error, we can use the variable symbol &SYSNDX in the creation of label names, as in listing 3b. Since the value of &SYSNDX is incremented after each macro call, successive calls of INCR will result in different labels being generated, as in listings 3c and 3d.*

```
(a)             MACRO           (b)             MACRO
                INCR                            INCR
     LABEL      INX  B               L&SYSNDX   INX  B
                INX  D                          INX  D
                MEND                            MEND

(c)  L0001      INX  B          (d)  L0002      INX  B
                INX  D                          IND  D
```

Listing 4: *Variable symbols and nested macros. Given the two macro definitions of SAVE and INCR in listings 4a and 4b, the macro call of SAVE in listing 4c, and the resulting expansion in listing 4d, it is obvious that variable symbol &REG has the value "D" during the expansion of SAVE and has the value "B" during the expansion of INCR. When macro calls are allowed to be nested, this situation must be allowed for.*

```
(a) 1.          MACRO
    2. &LAB     SAVE       &REG
    3.          MOV        M,&REG      MOVE REG TO ADDRESS IN HL
    4.          INCR       B           CALL INCR TO INCR HL AND COUNT IN B
    5.          MOV        A,&REG      MOVE REG TO A
    6.          MEND

(b) 1.          MACRO
    2.          INCR       &REG
    3.          INX        H           INCREMENT HL PAIR
    4.          INR        &REG        ADD 1 TO REGISTER
    5.          MEND

(c)             SAVE       D

(d) 1.          MOV        M,D MOV REG TO ADDRESS IN HL
    2.          INX        H INCREMENT HL PAIR
    3.          INR        B ADD 1 TO REGISTER
    4.          MOV        A,D MOVE REG TO A
```

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Listing 5: *An example of conditional assembly. Given the macro definition of MOVE in listing 5a and the macro call in listing 5b, the expanded code is given in listing 5c. Because the &LENGTH variable equals 1 in the macro call, the AIF (assemble-if) statement is executed in line 8 of the macro definition, causing lines 9 thru 12 to be omitted in the macro expansion of 5c.*

```
(a)  1.             MACRO
     2.  &JUMP      MOVE      &TO,&FROM,&LENGTH
     3.             LXI       B,&TO
     4.             LXI       D,&FROM
     5.             MVI       H,&LENGTH
     6.  &JUMP      LDAX      D
     7.             STAX      B
     8.             AIF       (&LENGTH EQ '1').END
     9.             INX       B
    10.             INX       D
    11.             DCR       H
    12.             JNZ       &JUMP
    13.  .END       MEND

(b)                 MOVE      A1,B1,1

(c)  1.             LXI       B,A1
     2.             LXI       D,B1
     3.             MVI       H,1
     4.             LDAX      D
     5.             STAX      B
```

mal approach to handling this problem in an assembler is to use two-pass processing. This means that the source program is read twice. The first time, all definitions are placed in the symbol table. The second time, the assembler generates the actual code, with the definitions of all symbols known as a result of pass one.

A macro processor does not really have this problem. All variable symbols are defined in the prototype statement, which comes *before* the model statements that reference these variables. Values are assigned to the variable symbols when the macro call is encountered, which is also prior to using the symbols for generation of code. All symbols other than variable symbols are left untouched by the macro processor and remain the problem of the main assembler, which will handle them in its two-pass processing, as mentioned earlier.

The only exception to this is if we try to implement conditional-assembly facilities. *Conditional assembly* allows us to alter the sequence of a macro definition's generated code. For example, we might not want to generate a group of instructions depending upon the value of a certain variable symbol.

As an example, listing 5a is a modification of the MOVE macro definition of listing 1. Statement 8 shows how conditional assembly can be used; if &LENGTH is a 1 at the point of expansion of line 8, the macro processor resumes expansion with the model statement which has .END as a label, in this case the MEND statement of line 13. Therefore, as in listing 5c, a length of 1 will not generate instruction lines 9 thru 12.

At first glance, this situation might look like a forward-reference problem, but it really is not. Since all model statements are stored in the internal macro definition, the macro processor needs only to point to the first model statement and loop through all model statements to find the one that starts with .END. In conditional assembly, the sequence code (.END in this example) would not appear on the generated code, thus allowing a sequence symbol to be placed on an instruction without worrying about the main assembler rejecting a label beginning with a period.

Earlier, I mentioned that an assembler is normally a two-pass system. In reality, so is a macro processor. The first pass occurs when reading in and storing the macro definition. The second pass occurs when a macro call is made, resulting in an expansion of the code defined for the macro statement being replaced.

The last major point of difference between the assembler and the macro processor is the method used for storing and scanning the source text. The assembler is interested in statement

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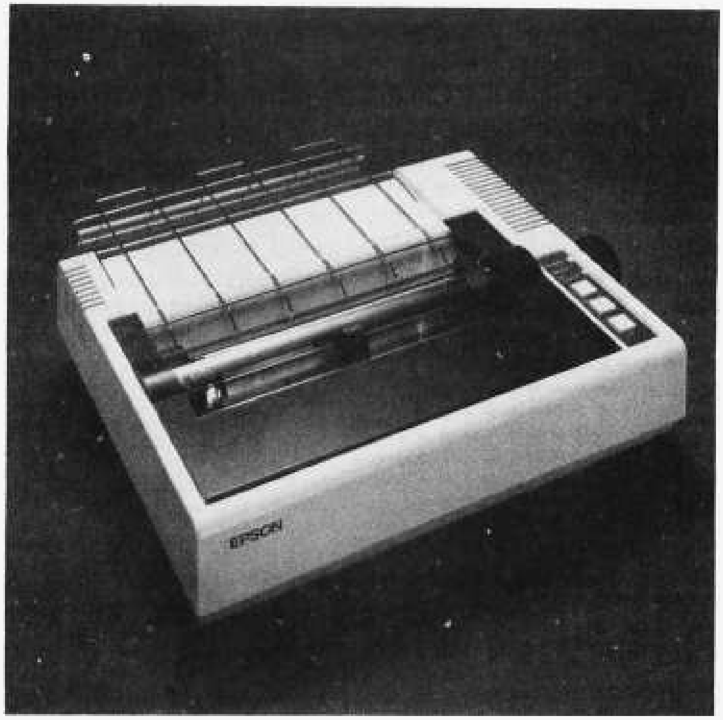

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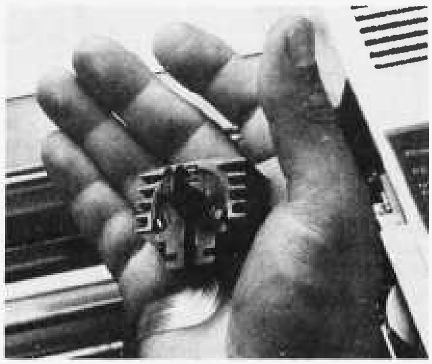

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labels, operation codes, operands, and variables. It is not interested in blanks, comments, punctuation, and so on. The assembler normally has a scanning routine to search each statement for the parts it needs. The scanner usually builds a list of descriptors, which are pointers to the beginning of each piece of the statement. The descriptor also contains the length of the label, variable, etc, and a code that identifies what is pointed at. In this manner, a typical statement to the assembler consists of a list of four descriptors, pointing to the label, the operation code, and the two operands.

While the descriptor system is advantageous to the assembler, which processes only one statement at a time, it is both cumbersome and inefficient for use in a macro processor. In the first place, the macro processor must store all statements of the macro definition, not just the current statement. Secondly, the macro processor need only search for the character "&" to locate the data in which it is interested. A complex scanner is unnecessary, as is a descriptor system, especially when we consider that the macro processor's output will be a series of complete assembler statements.

Instead of descriptors, we will take the approach of text compression. In most assembler languages, the programmers typically start labels in column one, operation code in column ten, operands in column sixteen, and comments separated from operands by one or more blanks. With this in mind, we can compress the model statements of the macro definition by eliminating all blanks but the ones between labels, operation codes, operands, and comments. The end of each statement in the compressed macro definition will be marked by a special character, such as a carriage return. To save even more space, we can eliminate the storing of comments in a macro definition, although this will also eliminate the comments on the generated source statements as well.

Implementing the Macro Assembler

So much for the more theoretical aspects of macro processors. Now let us look at the practical implementation of this facility, starting with the macro definition itself. Macro definitions can be either in-line or referred to from a library. An in-line macro definition is a macro definition coded at the beginning of the file containing the source statements for your program. It contains the macro header, macro prototype, model statements, and macro trailer. Obviously, it must be defined before it can be used in the program. All in-line macro definitions are stored in compressed format by the macro processor.

If certain macro definitions are used frequently, having a macro library is useful. This library will contain the macro definition, preferably with the model statements already in compressed format. When a macro call is encountered in the source program, the in-line macro definitions

1a

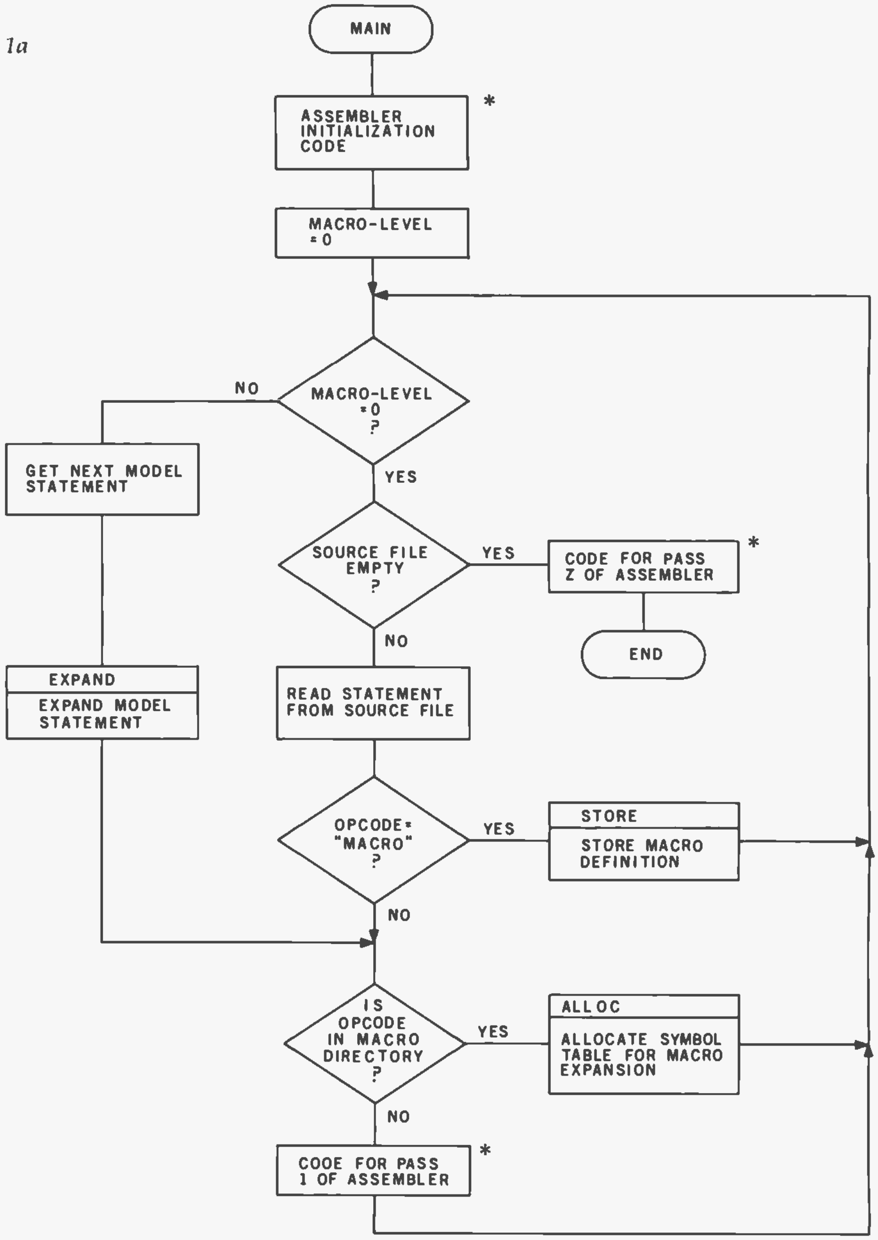


Figure 1: *High-level flowcharts of macro use. Figure 1a shows a high-level flowchart for the entire assembler program, which includes the functions of a macro facility. The boxes marked with an asterisk represent the code that performs the assembler functions; the remaining boxes represent the code that is added (through modification of the assembler's "read source" routine) to implement the macro facility. Figure 1b gives the STORE routine, used to store the statements defining a new macro instruction (all those statements between a MACRO statement and the next MEND—macro end—statement). Figure 1c, the ALLOC routine, stores variable-name information about the macro instruction that is currently being expanded. Figure 1d on page 164, the EXPAND routine, shows how a macro instruction is expanded.*

will first be searched. If the macro definition is not found, the macro library will then be searched. If found in the library, the definition will be read into memory and treated in the same fashion as an in-line definition. By searching the in-line macro definitions first, we allow the ability to enter an in-line macro definition for a macro already defined in the library and have the in-line macro definition take precedence over or override the library temporarily.

The flowchart of figure 1a shows an overview of macro definition and use. When the macro processor encounters a source statement that contains the pseudo-operation code MACRO, it knows that a macro definition is to follow. The first step to be performed is to add an entry to the macro directory identifying the new macro. The format of the directory entry is shown in figure 2a. The directory entry is of variable length. It will always be at least 12 bytes long, containing the macro name, the model address, the label indicator, and the parameter count. This fixed portion will be followed by as many 8-byte variable symbols as are defined in the prototype statement. The length of the directory entry is therefore $8P+12$, where P is the number of parameters.

The prototype statement in the macro definition contains most of the information necessary to build a new directory entry. The macro name is taken from the operation code of the prototype statement. The parameter count is the number of variable symbols in the prototype; the variable symbols themselves are stored in variable symbols 1 thru N of the directory entry. The model address is a pointer or address of where the first model statement is to be stored. The label indicator will be a 0 if the prototype statement has no label, or a 1 if the prototype has a variable symbol for a label.

The size of the model-storage area determines the number of macro definitions your macro processor can handle. Since the model statements are compressed, this will vary somewhat with the lengths of the macro definitions themselves. If you retain comments on the models in order to have them appear in the generated code, this will noticeably reduce the number of macro definitions that can be handled. The model statements are moved one character at a time to the storage area. When a blank is moved, all consecutive blanks after it are bypassed.

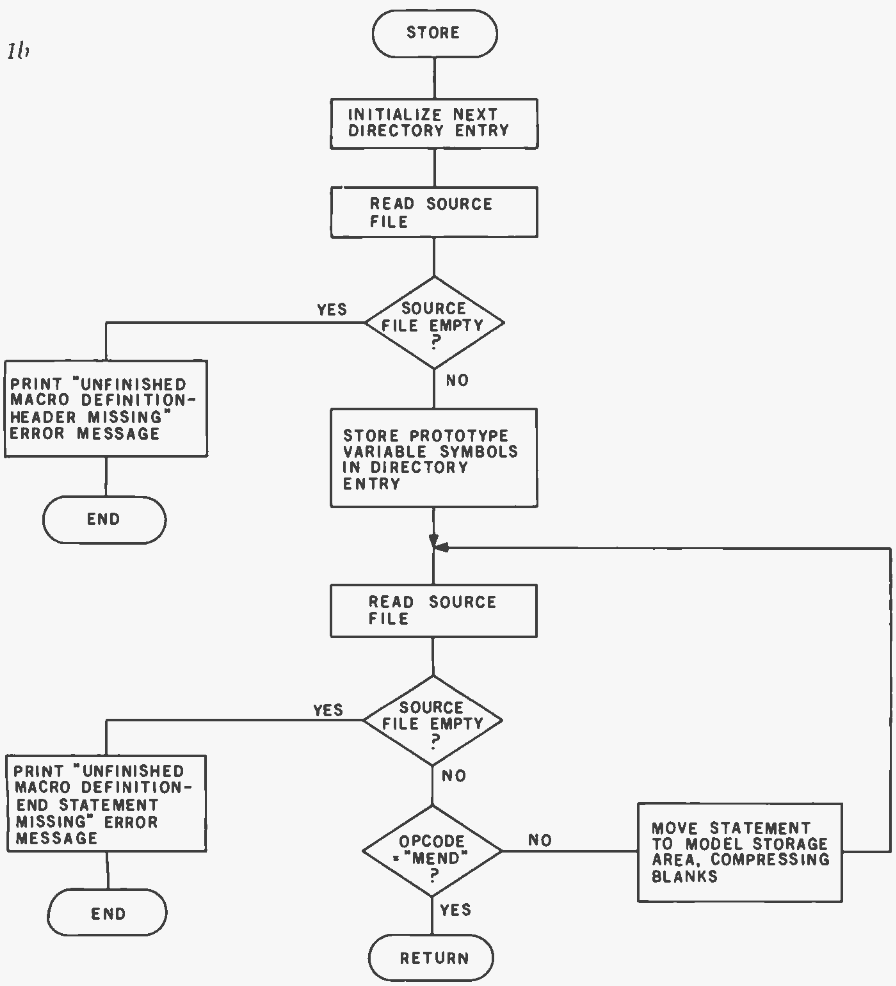
If desired, comments can be dropped to reduce storage space, as was mentioned previously. After each statement, a special character is put in the model-storage area so that the macro processor knows when the end of a statement has been reached. A good choice might be a carriage return.

When a MEND (macro end) statement is encountered, the end of the macro definition has been reached. A form feed or other special character is placed in the model-storage area to mark the end of the model statements. The pointer to the model-storage area is set to the position following the special character; its value is stored in the next available directory entry for use by the next macro definition. Figure 2b shows the format of the model-storage area.

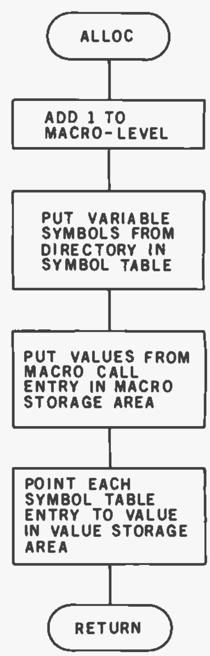
Expanding the Macro Instruction

Now that we have the macro definition stored, we can consider the process of macro expansion. However, we still need a few more

1b



1c



items. So far, we have directory entries and a model-storage area. To this we must add a symbol table, a macro stack, and a storage area for variable-symbol values, as shown in figure 3. As mentioned earlier, the symbol table will be a last-in, first-out stack. It will contain the variable-symbol name, the length of its current value, an indicator for the data format, and a pointer to the value.

The values of variable symbols will be stored in the value-storage area much as the model statements were stored, with the symbol-table entry pointing to it. When a variable symbol is found in a model statement, we will start at the end (most recent entry) of the symbol-table stack and search backwards for the proper entry. This will in turn point to the current value. As previously discussed, this allows inner macro calls and allows the same variable symbol to be used by different macro definitions to refer to different values. The entries are placed in the symbol table when the macro expansion begins and are

1d

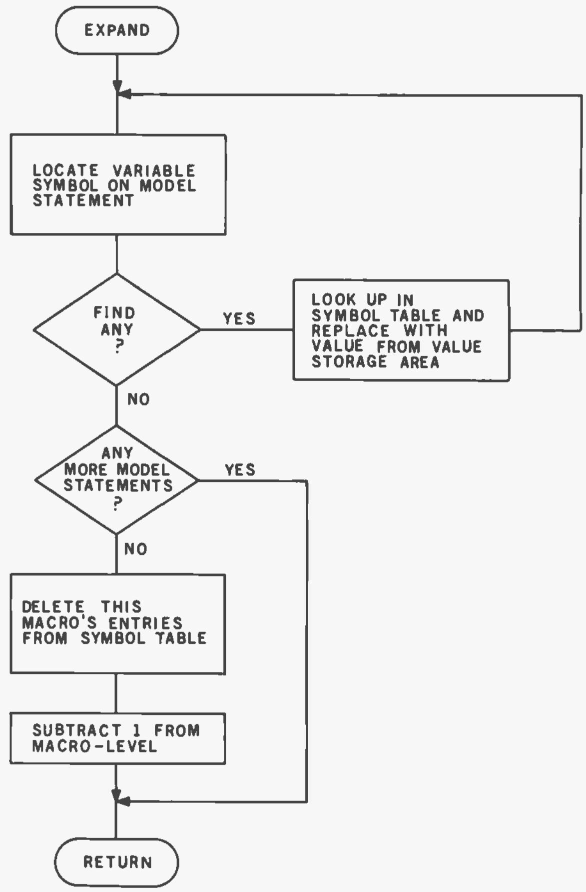


Figure 1d: *The macro-instruction EXPAND routine.*

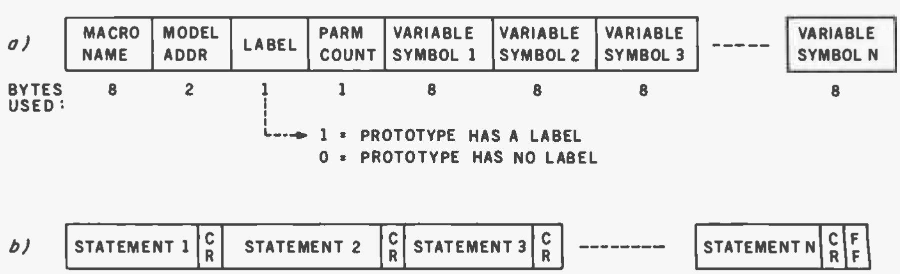


Figure 2: *Data areas associated with macro definition. When a MACRO statement, indicating the beginning of a macro definition, is encountered, the first line (which defines the macro name and the names of its variable symbols) is stored as in figure 2a. Once this is done, all successive statements up to but not including the MEND macro-end statement are stored sequentially as in figure 2b.*

deleted at the end of the macro expansion.

The macro stack is used to control the inner macro definition and symbol-table process. It contains a pointer to the directory entry of the macro statement currently being expanded, a pointer to the next model statement to be expanded, a pointer to the next available byte in the value-storage area, a pointer to the next available symbol-table entry, and a variable holding the depth of macro nesting. If this variable, called the *macro level,* is zero, the next statement in the source file is read. If the macro level is not zero, then a macro expansion is in progress and

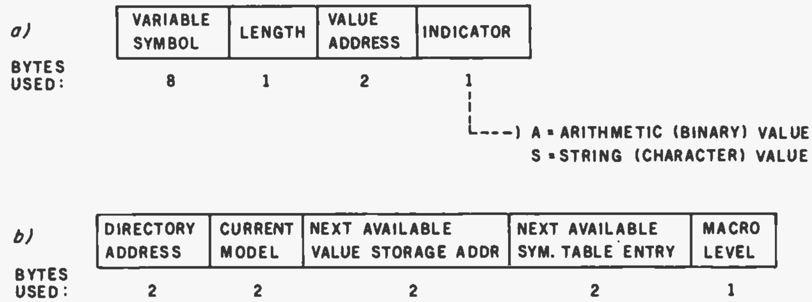


Figure 3: *Data areas associated with macro expansion. When a macro statement is encountered in the assembly-language program, one entry with a layout as in figure 3a is pressed onto the symbol-table stack for each variable symbol in the macro-definition header line (directory entry). Also, the calling macro statement pushes one entry (with a layout as in figure 3b) onto the macro stack to represent the current macro instruction being expanded. Refer to figure 4 for a graphic representation of the interrelationships of these fields.*

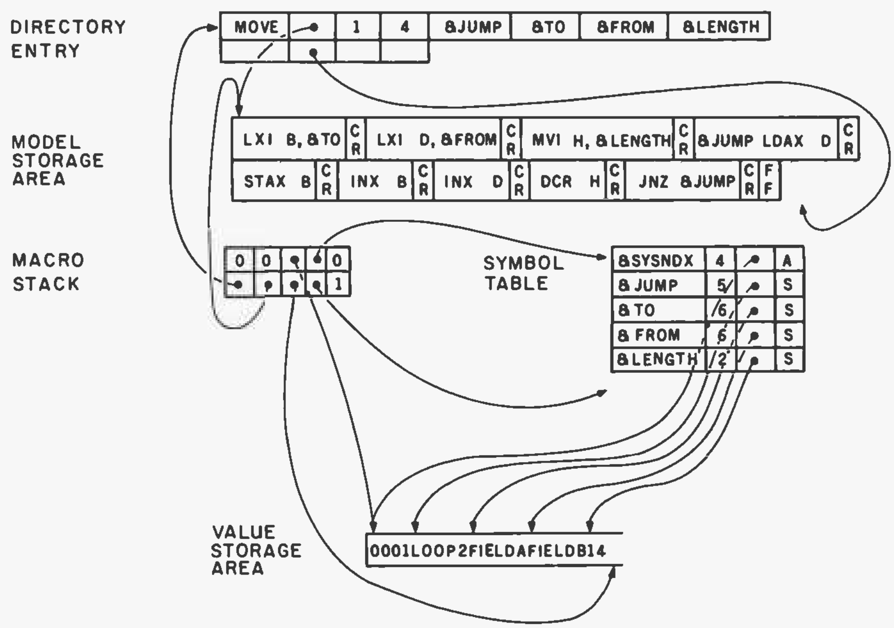


Figure 4: *Interrelationship of data areas during macro expansion. Processing of the macro definition results in the directory entry and the entries shown in the model-storage area. When a macro instruction is encountered in the assembly-language program, the second entry in the macro stack is made, along with the entries shown in the symbol table. The first entry in the macro stack, the line with the zeros, is used to denote that the macro stack is empty and that there are no macros currently being expanded. The entries belonging to the current macro are pointed to by the pointer originating in the second row, fourth column of the macro stack. Variable symbols found in the model-storage statements are searched for in the symbol table starting with the last entry in the table and going backwards. The third field in each symbol-table entry points to the first character (or byte) of the variable symbol's value as stored in the value-storage area. The macro statement being expanded is "LOOP2 MOVE FIELDA,FIELDB,14".*

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the model statement pointed to by the current model address is processed.

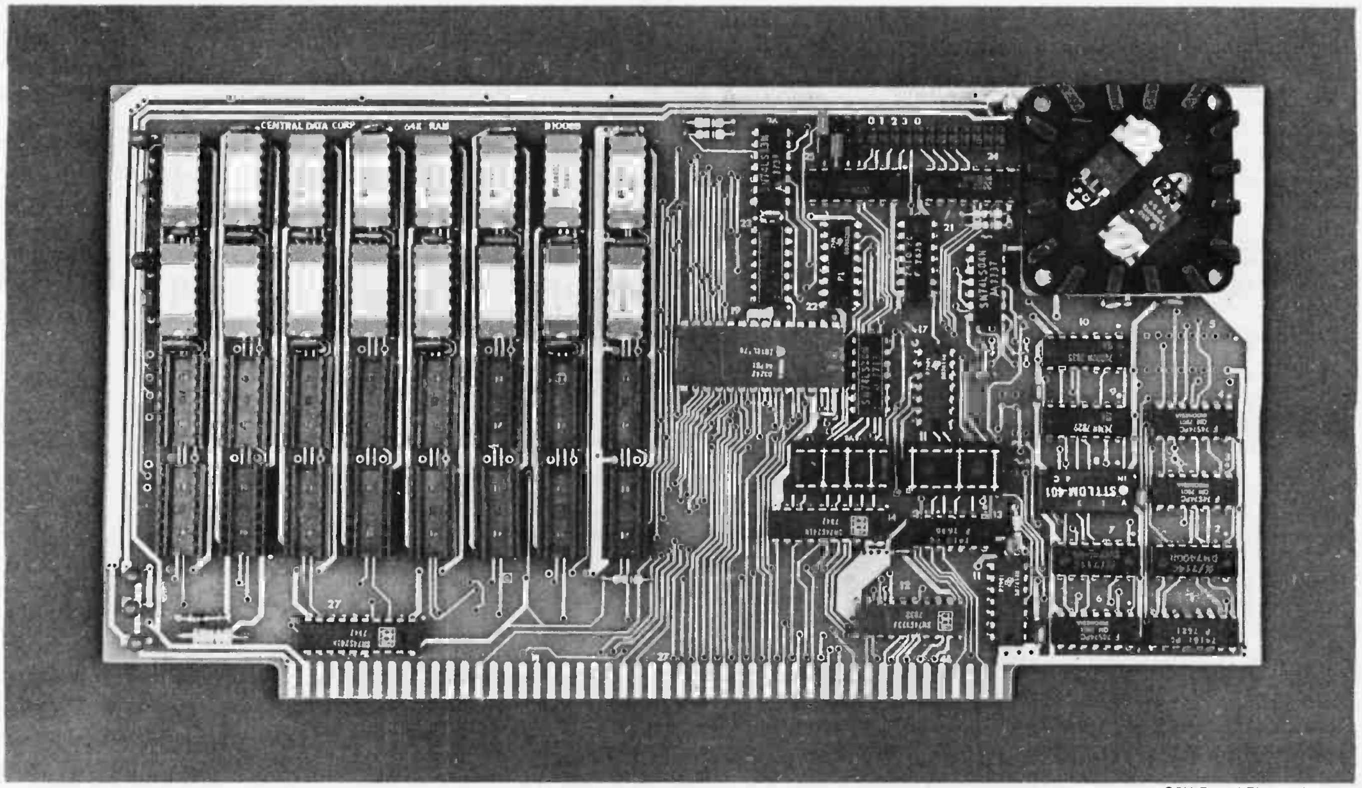
The macro stack will always contain one entry at the bottom with everything set to zero to allow initial and non-macro-definition statements to be read under control of the macro level indicator. The only other areas of memory that we need are an area in which to accumulate the value of &SYSNDX (which is incremented every time a macro definition is expanded) and an 80-byte area in which to expand the current model statement before passing it to the assembler.

At this point, it might be helpful to refer back to figure 1. The STORE routine was discussed earlier. Now that we have defined the symbol table and macro stack, we can look at the ALLOC (figure 1c) and EXPAND (1d) routines. Bear in mind that the actual process is considerably more complex than the simple diagram of the flowchart in figure 1a.

When an operation code is recognized to be a macro call, the first step is to build a new macro-stack entry. Both the addresses of the current macro model and its directory entry are stored. We also store the address of the next available value-storage area and symbol-table entry, and finally add 1 to the old macro level and store it as the macro level of the current macro-stack entry. At this time we also want to increment to &SYSNDX.

Next, we must put the current values for the variable symbols in the symbol table. To do this, we take the first variable symbol from the current macro-directory entry and enter it in the symbol table. We take the first operand (or the label if the LABEL indicator is a 1, indicating that a label is present) from the macro instruction and put it in the value-storage area, also pointing the symbol-table entry to it; this is repeated for every variable symbol in the directory entry. We also put the current value of &SYSNDX into the symbol table. Figure 4 shows how all of the tables, stacks, and storage areas are interconnected for the MOVE macro definition of listing 1. Note that the comments have not been stored in the model-storage area.

One additional complexity should be mentioned concerning the filling of the symbol table from the directory entry and macro call. The SAVE



Listing 6: *Passing macro parameters to an inner macro call. Some additional code must be added to the macro-evaluation routine in order to enable a macro call within a macro definition to pass the value of one of the parameters of the outer macro. Given the two macro definitions of SAVE and INCR in listings 6a and 6b, the macro call of SAVE in listing 6c, and the resulting expansion in listing 6d, the intent of this code is for the SAVE macro definition to pass its parameter into INCR. Note that the parameter names for the two macro definitions must be different to accomplish this. In line 3 of listing 4d, the operand of the INR instruction (here, D) will always be the same as the argument of the SAVE macro call in listing 6c.*

```
(a)  1.           MACRO
     2.  &LAB     SAVE   &REG
     3.           MOV    M,&REG                  MOVE REG TO ADDRESS IN HL
     4.           INCR   &REG                    CALL INCR TO INCR HL AND COUNT
     5.           MOV    A,&REG                  MOVE REG TO A
     6.           MEND

(b)  1.           MACRO
     2.           INCR   &REGISTR
     3.           INX    H                       INCREMENT HL PAIR
     4.           INR    &REGISTR                ADD 1 TO REGISTER
     5.           MEND

(c)      LABEL1   SAVE   D

(d)  1.  LABEL1   MOV    M,D MOVE REG TO ADDRESS IN HL
     2.           INX    H INCREMENT HL PAIR
     3.           INR    D ADD 1 TO REGISTER
     4.           MOV    A,D MOVE REG TO A
```

macro definition given in listing 4a contains, on line 4, a call of the INCR macro definition with a constant operand of B. What if we wanted to use whatever value was coded for &REG on the SAVE macro call?

Listing 6a shows the SAVE macro definition again, but this time it calls INCR on line 4, passing a value of &REG. In listing 6b, we have the INCR macro definition again, but &REGISTR is used as its variable symbol instead of &REG. Now that the INCR macro definition has its own variable symbol, the expansion of line 4 of the SAVE macro instruction can be accomplished as if the *value* of &REG were in line 4 (instead of the characters "&REG").

When entering the variable symbols and their values in the symbol table during a macro expansion, we must now check the value for an "&". If found, we search back through the symbol table until we find the variable symbol. We use the length and value-storage pointer from that previous definition. in the new symbol-table entry that we are building. Therefore, when the macro call of listing 6c is expanded and gets to the INCR macro call within the SAVE macro definition, the symbol table is searched for &REG, and the value-storage pointer and length in the &REG entry are used in the &REGISTR entry of the symbol table. Now both &REG and &REGISTR are pointing to the value of D, and the generated code of listing 6d is produced.

By now the worst is over. All that remains is to expand each model statement in turn, replacing variable symbols with their values and putting back compressed blanks. When a variable symbol is encountered, we look it up on the symbol table, get the pointer to the value-storage area, and replace the variable symbol with the data from the value-storage area. Each model statement is scanned, expanded, and passed to the assembler until there are no more model statements to be processed. The final operation is to delete the most recent entry in the macro stack. This effectively deletes from the symbol table all of the symbols associated with the macro instruction just expanded; it also does the same for the value-storage area and macro-level variable.

As always, there are a few complications you should consider. For example, suppose you want to use an ampersand (&) character in your source, but not to denote a variable symbol. The normal solution to this problem is to require you to use two ampersands in this situation, much like the use of two quote symbols within a character string to represent a single quote character. Two ampersands then tell the macro processor that this is not really a variable symbol and that one of the ampersands should be deleted.

Also, before scanning a model statement for variable symbols, you should check to see if its operation code is itself a macro call. If it is, you want to do the entire expansion routine again, setting up another macro-stack entry, putting more variable symbols in the symbol table, and expanding the new macro call (which could contain yet another macro call within it). Once the inner macro instruction is expanded, you should return to the outer macro definition and resume its expansion. If a macro definition calls itself, this situation is referred to as *recursion*.

(Next month, part 2 of this article will present some fairly detailed flowcharts of the macro definition and expansion processes and discuss interfacing the macro processor with the rest of an existing assembler. In addition, I will discuss some enhanced facilities that you might want to add to your macro assembler.) ■

Product Description

Three New Computers from Radio Shack

Stan Miastkowski, Editor

Ever since the TRS-80 was introduced, there has been repeated speculation about its successor. Rumors have flown about the imminent demise of the Model I and the introduction of a "TRS-90" (or something of that sort). Last year the TRS-80 Model II was introduced. Even though its capabilities are much greater than the Model I, its price was aimed squarely at the small-business market.

The TRS-80 Model III

All the speculation, or at least most of it, can now come to an end. The TRS-80 Model III has arrived, and along with it come the TRS-80 Color Computer and the TRS-80 Pocket Computer. Even though the Radio Shack people say the Model III is *not* designed to replace the Model I, it *is* the successor and it seems likely to eventually push aside the Model I.

Several Radio Shack development people told me that the Model III was introduced because they saw a need for what was termed a "powerful" desk-top computer that would be smaller and less expensive than the Model II (which starts at $3450).

Cosmetically, the TRS-80 Model III bears a more-than-vague resemblance to the Model II. The entire unit is housed in a one-piece molded case sporting the familiar battleship-gray motif. One big change is that the keyboard (65 keys including keypad) is nondetachable. The high-resolution monitor measures 30.48 cm (12 inches) diagonally, and space has been left next to the monitor to mount one or two (optional) disk drives. The obvious reason for the one-piece design is to provide increased RF (radio frequency) shielding to comply with FCC (Federal Communications Commission) rules and regulations. This was confirmed by several Radio Shack people.

As for the internal design of the TRS-80 Model III, the only thing I was able to uncover is that the Z80 continues to be Radio Shack's microprocessor of choice. At a recent press conference introducing the products, none of the new products was shown with the cover removed. Requests to "take a look inside" were firmly, but politely, denied. Despite the myriad hobbyists waiting with hot soldering irons to get inside, the official policy of the Tandy Corporation is that its computers should be opened only by authorized service personnel.

The TRS-80 Model III is being marketed in three basic configurations ranging in price from $699 to $2495. Radio Shack says that all Model I software will run on the Model III without modification. You can purchase 4 K bytes of programmable memory, uppercase-only alphanumeric character set, and Level I BASIC for $699. An important addition to Level I BASIC is the inclusion of LPRINT and LLIST (since a printer interface is included).

Significantly, none of the Model III configurations include the familiar cassette recorder. Radio Shack is selling the optional CTR-80A for $59.95. Another new feature is that the cassette data-transfer speed is now a respectable 1500 bps (bits per second) even with Level I BASIC. No more time to go get a sandwich and coffee while a program is loading.

The next step up in the Model III progression is $999. Inasmuch as this buys you a *lot* of capability, it seems destined to be the most popular version of the new computer. Included are 16 K bytes of programmable memory, uppercase and lowercase alphanumerics, a real-time clock, and something called "Model III BASIC" (not to be confused with Level III BASIC which is marketed for the TRS-80 by an independent supplier). At press time, no details were available on how Model III BASIC differs from Level II BASIC. I did learn that a TIME$ function and several new statements are included.

The top of the TRS-80 Model III line is what Tandy is calling its "Desktop Business Computer." The price for this configuration jumps to $2495, but it adds two double-density 5¼-inch (12.7 cm) floppy-disk drives and an RS-232C interface. The drives give the Model III a

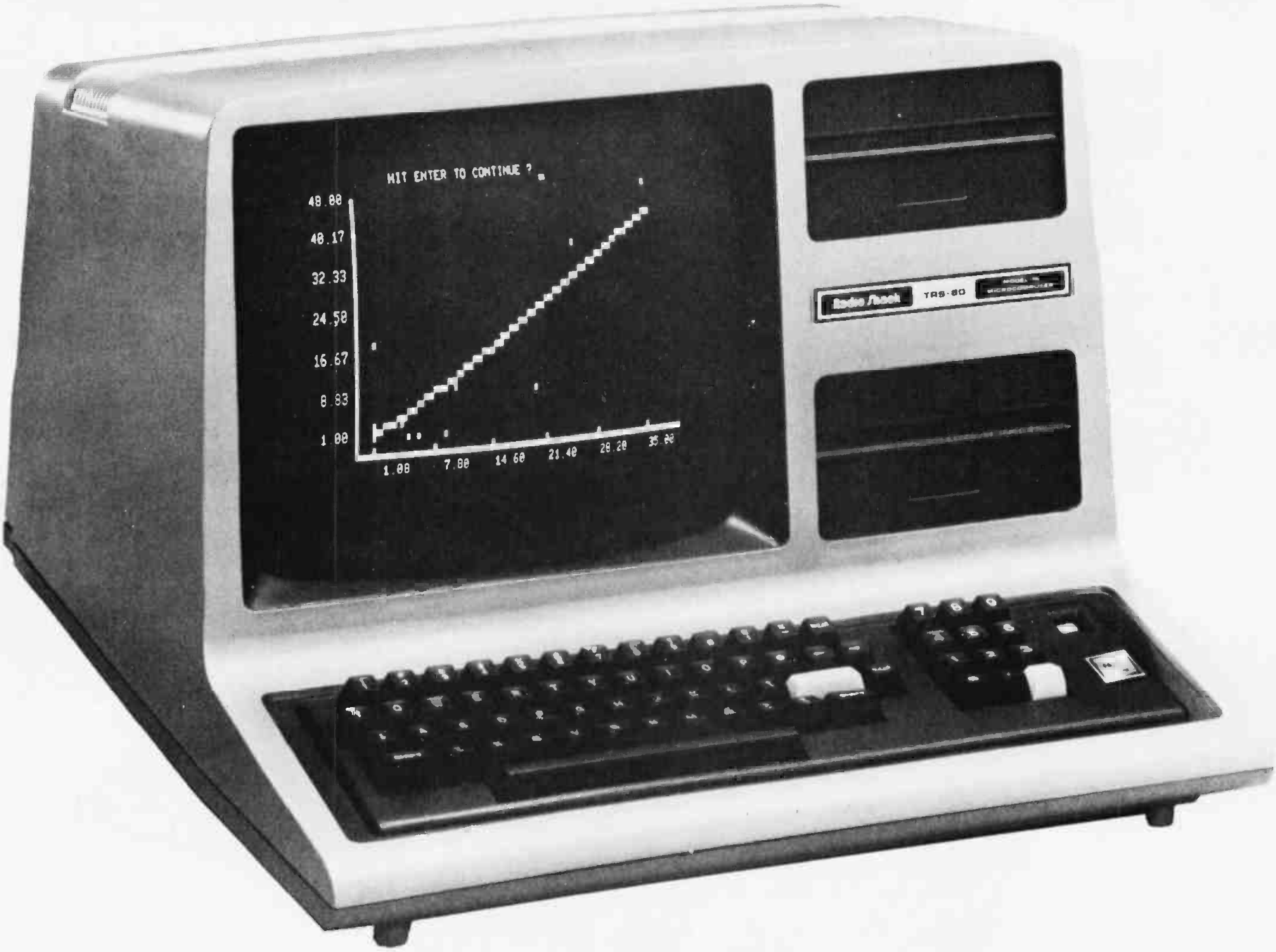


Photo 1: *The TRS-80 Model III is available in three configurations ranging in price from $699 to $2495. The Model III is housed in a one-piece case with a nondetachable keyboard. Utilizing a Z80 microprocessor, the Model III is available with uppercase and lowercase alphanumerics, real-time clock, RS-232C serial interface, and "Model III BASIC"—an expanded version of the familiar Level II BASIC.*

total storage capacity of 315 K bytes. Radio Shack has also introduced a new daisy-wheel printer for $1960 (more about the printer later). It's a natural to go with the Desktop Business Computer Model III configuration, and it brings the price of the Desktop Business System to $4455.

Although these are what Radio Shack calls its three basic configurations, you are not limited to them. As with the TRS-80 Model I, you can pick and choose. For example, adding 16 K bytes of programmable memory costs $199. Sixteen K bytes and the Model III BASIC are $299. The RS-232C serial interface can be installed in any of the Model III configurations for $99. If for some reason you want a single floppy-disk drive, it's available for $849, including a new TRSDOS (disk operating system). The second drive is $399.

The TRS-80 Color Computer

Of the three new computers that Radio Shack announced, the TRS-80 Color Computer will probably create the most interest in consumer markets. It's sure to create quite a few sales along the way. Radio Shack's copywriters call it "high-technology at low cost." For $399, you receive a full-fledged computer with color and sound, and it is programmable in BASIC. Included are 4 K bytes of programmable memory, a *built-in* television modulator, and a 53-key standard keyboard.

The TRS-80 Color Computer utilizes a Motorola 6899E microprocessor and supports several levels of color graphics, each using increasing amounts of memory. Eight colors are available—any one of which the user can select for the background color. The character format is 16 lines by 32 characters. The "standard" graphics format is 64 by 32. The highest-resolution graphics are 128 by 192 (using four colors) and 256 by 192 (one color only).

A unique *built-in* feature of the TRS-80 business computer is an RS-232C serial interface for modem or printer connection. Because of this, the Level I BASIC of the Color Computer includes LPRINT and LLIST. With the addition of a modem ($199) and a special software package ($29.95), the Color Computer becomes a Videotex terminal (Radio Shack's name for its connection to the CompuServe Information Services Network).

At present, seven games and a personal finance program (all full-color) are available in ROM (read-only memory) "Program Paks" that plug into the side of the unit. Several of the games require optional joysticks ($24.95).

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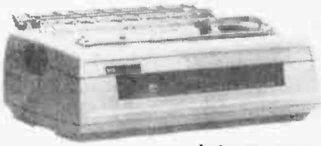

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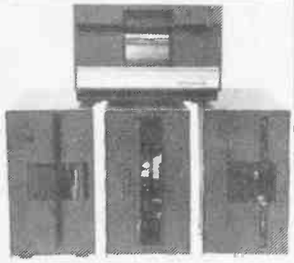

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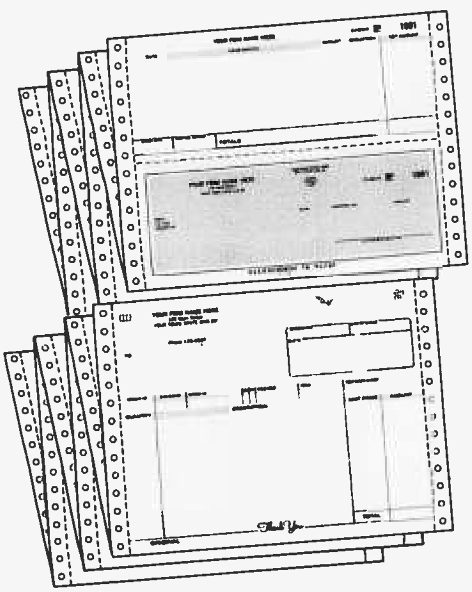
Photo 2: *The TRS-80 Color Computer sells for $399 with BASIC, 4 K bytes of user memory, and a built-in television RF modulator. It supports eight colors and several levels of graphics resolution. Eight game programs are currently available on ROM-based "Program Paks" that plug into the right side of the unit. Expansion is available with 16 K of programmable memory and Extended Color BASIC, which allows the creation of high-resolution graphics from within a BASIC program. The monitor shown receives standard television signals and sells for $399.*

The TRS-80 Color Computer can be expanded to 16 K bytes with a set of programmable memory processors that sell for $99 plus installation. Another option is the Extended Color BASIC package (in 8 K of ROM). It gives you the ability to create high-resolution graphics from within a BASIC program. The Color Computer with both the expanded memory and Extended Color BASIC can be purchased for $599, which is a reasonable price for its capabilities and should give some other personal-computer manufacturers a few sleepless nights.

One interesting point: the TRS-80 Color Computer can be programmed in machine language (for those so inclined).

For storing and loading programs, you will still need a cassette recorder, which is not included. As I previously mentioned, the CTR-80A sells for $59.95. If you want



still more storage, Radio Shack says a floppy-disk drive will be available for the Color Computer in early 1981.

You will also need a color monitor for the TRS-80 Color Computer. Since it has a built-in television RF modulator, you can use the family television. But if that draws complaints from the family, an option is available. Radio Shack is now selling its first-ever standard color television. The TRS-80 33 cm (13-inch) Color Video Receiver (made by RCA) sells for $399 and has full American-standard reception capabilities. It has digital channel display and push-button tuning. At the recent introduction of the Color Computer, it did an excellent job of displaying the high-resolution graphics.

The TRS-80 Pocket Computer

Radio Shack spent a great deal of time stressing the "breakthrough" of the TRS-80 Pocket Computer at this press conference. I have to admit that it *is* a very interesting product. If you sit back and think a minute, you'll realize that only a couple of years ago genuine pocket computers (not calculators) were something found only in the realm of science fiction.

The TRS-80 Pocket Computer ($249) is *not* a glorified calculator. It's a compact unit 17.78 by 7 by 1.27 cm (7 by 2¾ by ½ inches), that is programmed in Level I BASIC (without the graphics capability). The keyboard has 57 keys (many of them double function) with the standard "QWERTY" alphanumeric keys. Although the keys are placed very close together, even a high-speed touch-typist can get used to their spacing and feel in a very short time.

The Pocket Computer utilizes a liquid-crystal 24-character alphanumeric display (5-by-7 dot matrix). Lines longer than twenty-four characters can be entered and displayed, and program lines are scrolled automatically. There are 1.9 K bytes of user memory included. For obvious reasons, it is not expandable. An interesting feature is that, since CMOS (complementary metal-oxide semiconductor) programmable memory is used, programs are retained when the power is turned off. Also, automatic BASIC abbreviation eliminates spaces in the stored program to conserve memory space. For off-line program storage, a cassette interface ($49) is available. Although any cassette recorder is usable, Radio Shack has introduced the Minisette-9 as a logical companion to the Pocket Computer. It's compact (18.25 by 11.6 by 3.33 cm) and uses standard cassettes.

The TRS-80 Pocket Computer is, interestingly enough, Radio Shack's only computer that is not company-made in Fort Worth, Texas. It's a Japanese product with Radio Shack packaging. (Observant BYTE readers will notice that it bears a distinct resemblance to several other pocket computers which were recently introduced.)

Although I didn't get a look inside, I was able to learn that the Pocket Computer uses *two* 4-bit CMOS microprocessors (one for arithmetic calculations and the other for the BASIC interpreter). There is an 80-character input buffer and the built-in ROM uses 7 K bytes for the BASIC interpreter and 4 K bytes for the monitor.

Not unlike a sophisticated calculator, fifteen mathematical functions are available, including trigonometric and inverse trigonometric with readout in degrees, radians, and gradians, plus logarithms, exponents, angular conversion, integer, and absolute value. The Pocket

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- Jumper selectable 2 or 4 MHz. operation.
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SYSTEMS

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- Z-8000 series 16 BIT CPU S-100 Board - see above

SOFTWARE (Provided with system)
- CP/M 2.2[1] operating system
- Basic
- Z-80/8080 Emulator
- Monitor, Debugger, Disassembler software
- Optional software: Pascal
- UNIX[2] operating system coming

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QDP-100 WITH 2 MEGABYTES STORAGE STANDARD (OPTIONAL 4 MEGABYTES)

- Z-80 series 8 BIT CPU S-100 Board (4 MHz. Z-80, Double density disk Controller, 2716 Prom Burner 2 Parallel & 2 Serial Ports, real time clock)

SOFTWARE (Provided with system)
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- Basic
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Photo 3: *The TRS-80 Pocket Computer. Measuring 17.78 by 7 by 1.27 cm (7 by 2¾ by ½ inches), the hand-held unit sells for $249 and can be programmed in Level I BASIC. The display is 24-character liquid-crystal type utilizing a 5-by-7 dot matrix. There are 1.9 K bytes of programmable memory included, and a cassette interface (list price $49) is available for off-line storage. Eight software packages are currently available, including Aviation, Real Estate, Engineering, Finance, Games, and Math.*

Computer has 10-digit accuracy. It uses four 67S mercury batteries for a total life of about 300 hours. The Pocket Computer automatically shuts off after seven minutes of inactivity to conserve the batteries.

The Pocket Computer is fun to use, even for hardcore computer enthusiasts. There is something very different about banging in a quick BASIC program on a hand-held unit. If you're used to the pseudo-assembly language of programmable calculators, you'll find using the TRS-80 Pocket Computer an exhilarating experience. Single-step, debug, and edit modes are available to make things easier. It's also useful as a "pocket notebook"—since strings of up to seven characters can be stored as data and then sorted and searched.

Radio Shack has put a good deal of thought and work into eight software tapes that are currently available for the Pocket Computer. They've promised many more to come. Those available now are: Real Estate, Civil Engineering, Aviation, Math Drill, Games I, Business Statistics, Business Financial, and Personal Financial. All of the software has been especially designed for the capabilities of the Pocket Computer. More information fits into that 1.9 K than you might expect. For instance, the Business Statistics software contains eight programs, including forecasting, seasonal variations, moving average, multiple regression, and more. The Management Decisions package also contains eight programs including break-even analysis, optimum order quantity, profit margin, and random sample.

Although there has already been criticism of the TRS-80 Pocket Computer as a "toy," it is a very sophisticated computer for its size and price. Radio Shack is counting on this computer to be a best seller that will help further Radio Shack's hold on the personal-computer market.

The Printers

Complementing its three new computers, Radio Shack has introduced four new printers, bringing its printer line to seven units at prices ranging from $219 to $1960.

The most interesting new arrival is the Daisy Wheel Printer II. Selling for $1960, it's specifically designed for word-processing applications. It features 10- or 12-pitch as well as proportional spacing and operates at 43 cps (characters per second). A pinchfeed roller takes paper widths from 10.16 to 37.8 cm (4 to 14⅞ inches) and a tractor feed will also be available. At present, one character wheel is available, but, because they are easily interchangeable, more can probably be expected in the future.

Another new and different arrival is the Plotter/Printer ($1460). As the name implies, it can be used as either a normal line printer (uppercase only) or a plotter. It takes 20.3 cm (8-inch) tractor-feed paper and prints at an average speed of 10 cps.

The Line Printer IV sells for $999, and it is Radio Shack's lowest-cost "letter-quality" printer. It prints both uppercase and lowercase alphanumerics in 80- or 132-character columns and handles roll paper, fanfold, or single sheets.

Rounding out the line of new printers is the Line Printer VI. It is a medium-cost business printer designed for reports, checks, invoices, etc. It sells for $1160. It utilizes a bidirectional printhead (7-by-9 matrix) that operates at 100 cps. It takes 10.16 to 38.1 cm (4- to 15-inch) fanfold, roll, or single sheet paper, and comes with a removable tractor mechanism. ■

Technical Forum

Radio Shack's Modifications to the TRS-80

Terry Li, POB 481, Peterborough NH 03458

Contrary to the opinion of many TRS-80 Model I owners, Radio Shack is constantly improving and upgrading its computers. Two recent improvements are an uppercase-and-lowercase capability, achieved by replacing the character-generator ROM (read-only memory device), and a new set of Level II BASIC ROMs.

Unfortunately, both of these alterations result in changes that require modifications to much of the currently available TRS-80 software. Here's what to expect.

Uppercase and Lowercase

A number of users have expressed disappointment with the TRS-80 uppercase-and-lowercase modification because it does not include the addition of a Control key to the keyboard. Remember, though, there are always two solutions to a computer problem: change the hardware or change the software.

Hardware modifications that require soldering and cutting have a higher element of risk than simply replacing ROMs. Since the character-generating software is contained in ROM, the obvious means of modifying it is to replace the ROMs. This is what the Radio Shack people have done.

The actual software modification for uppercase and lowercase is relatively simple. Whenever an alphabetic key is pressed, the sixth bit of the character is set high. If an alpha key and the shift key are pressed at the same time, the sixth bit is set low.

There are two distinct disadvantages to the technique that Radio Shack has used:

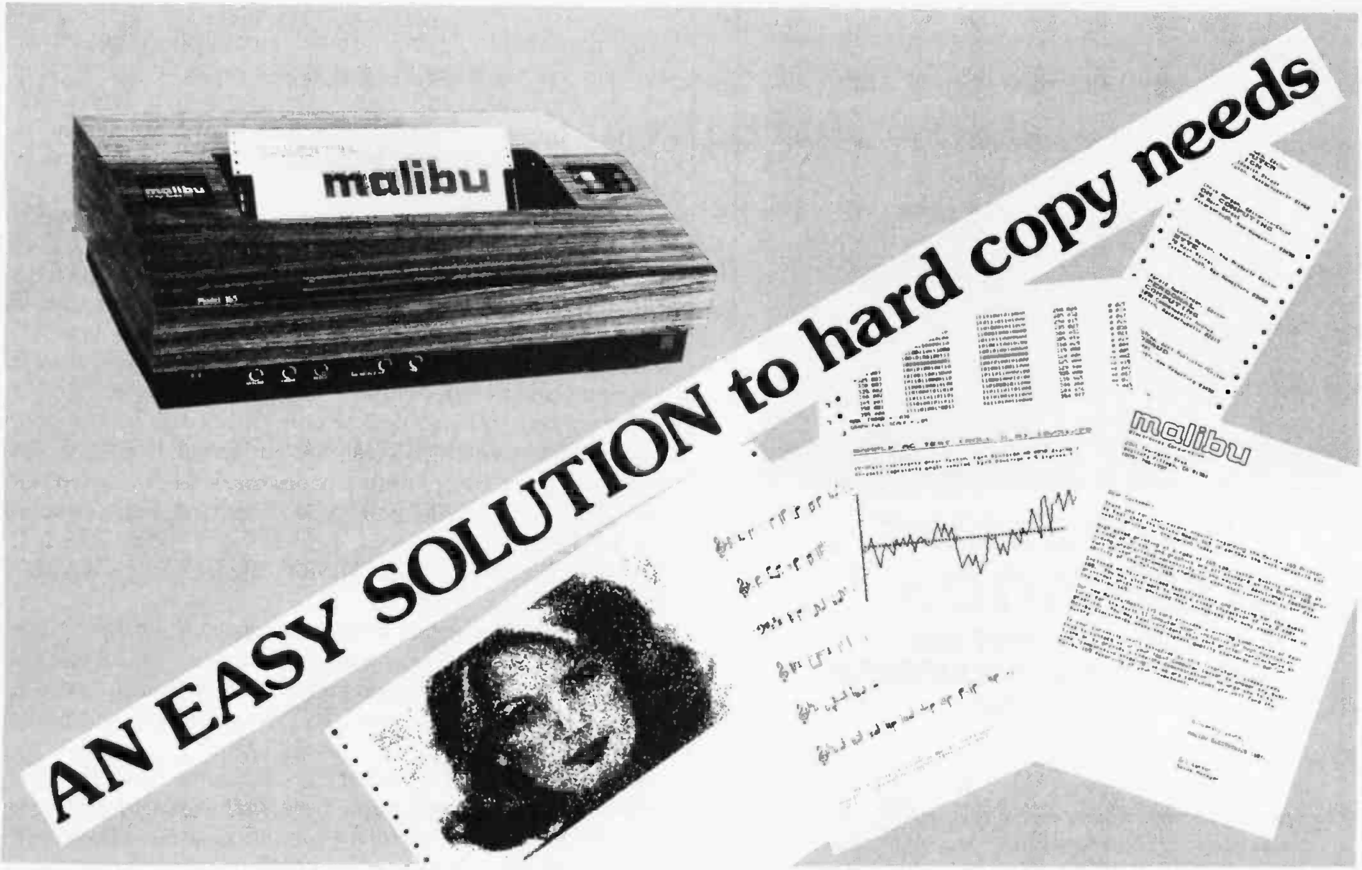
- INKEY$ malfunction: The INKEY$ function receives all letters directly from the keyboard, noting whether the key pressed is uppercase (bit 6 low) or lowercase (bit 6 high). When a program uses the INKEY$ function for one-letter input (eg: Y for *yes*, N for *no*) and that program was written for an unmodified (nonlowercase) TRS-80, the program is looking for an uppercase letter, and the keyboard returns a lowercase letter (unless the user remembers to give a shifted letter as input). The program will then behave unexpectedly because no match was made.

  The only way around this problem is to either rewrite the program to look for lowercase letters from INKEY$ input or to tell the user to always use shifted letters.
- LPRINT malfunction: In most cases, the LPRINT command will operate correctly. However, if you're attempting to use the PEEK command to read the video memory, then when LPRINTing the results (which some programmers do), your printer will go berserk, printing carriage returns, form feeds, and garbage. There appears to be no rhyme or reason to this alteration. You cannot PEEK and LPRINT one character, and you cannot PEEK characters, store them in a string variable, and LPRINT the variable without getting this result.

Radio Shack does warn you that not all software will run correctly after the uppercase-and-lowercase modification. This includes some of their own. [*However, Radio Shack will exchange old versions of its software for new versions that will work with the modified TRS-80s at no cost; see your local Radio Shack dealer....GW*] Some non-Radio Shack word-processing systems (such as Electric Pencil) will not work correctly because of the lack of a Control key on the TRS-80. If some ambitious soul could figure out how to fix Electric Pencil to accept @ as a control character, the problem would be solved.

The New Level II BASIC ROMs

It's not generally known that Radio Shack has come out with a new set of Level II BASIC ROMs. The new ROMs do not include any new features, however, they do fix a few bugs and make the computer a little more reliable. The TRS-80 was originally intended to be a Level I machine, with a small number of users moving up to Level II. Because of this, the TRS-80 circuit board was designed to use only two sockets for the ROMs. For those



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who upgraded to Level II, a small circuit board with three sockets (for the three Level II ROMs) was on the left side of the keyboard unit under the panel that has Radio Shack's name stamped in it; this board connected to ROM socket number 1 on the main printed-circuit board, through a long ribbon cable.

As everyone knows, Tandy Corporation drastically underestimated the consumer interest in computers. Level II became the vastly more popular model. Since the long cable is a source of electrical noise to the computer, this is an awkward position for machines using the Level II ROMs, especially if the keyboard has the numeric keypad added to it.

To correct this problem, Radio Shack has been working upon a two-chip ROM set for Level II BASIC. In order for there to be enough room on these devices for all the code, some things had to be shortened. For example, on powerup the user sees "MEM SIZE?" and "R/S L II BASIC" instead of "MEMORY SIZE?" and "RADIO SHACK LEVEL II BASIC."

One disadvantage of these new two-chip ROMs is that some of the machine-language routines in the BASIC interpreter have been moved from their previous locations. This could make some ROM-dependent programs malfunction.

[In fact, TRS-80 owners with machines that give the abbreviated messages should be suspicious of all commercially available software for the TRS-80. Many software packages make use of machine-language routines within the TRS-80 Level II ROMs. If the entry points of these routines have been changed or if the routines have been eliminated, the software will not work and may not be modifiable....GW]

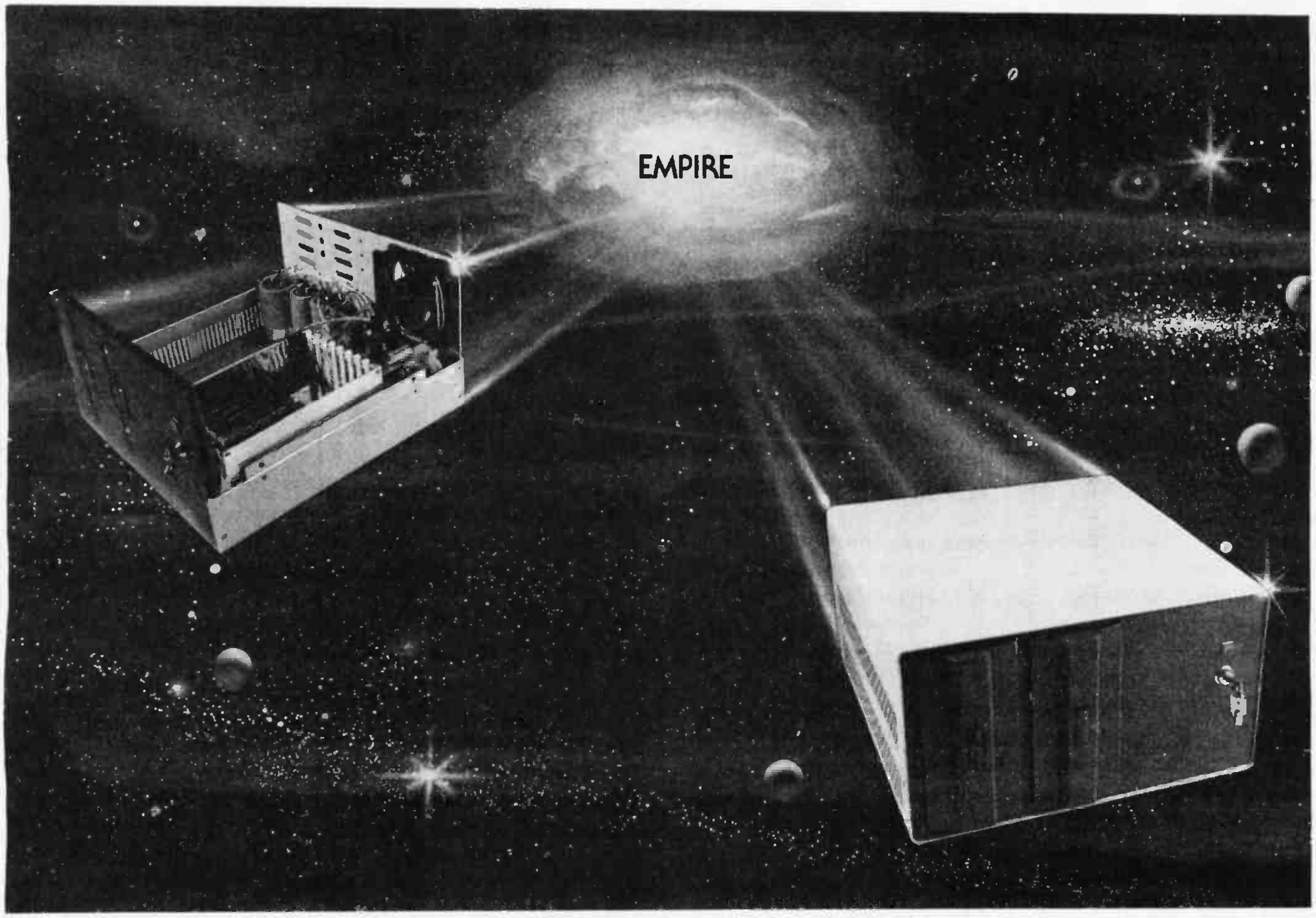
One nice feature of the new ROMs is the elimination of key bounce (the delay loop used in the original ROM was incorrectly calculated).

Another difference is in the keyboard memory map. Tandy has decided to redefine the *shift-down-arrow* key to be a null instead of its former value of decimal 26. This was done to fix an error in the original ROM. Any programs (I know of several) that use the shift-down-arrow to emulate a Control key will no longer work correctly. There is no response at all to this key input.

Radio Shack made this change to allow the user to enter control characters from the keyboard. Hitting shift-down-arrow and *then* hitting the A key will return the standard ASCII Control-A character (decimal 01), hitting shift-down-arrow and then the B key will return the Control-B character, with a value of 02, and so forth through the alpha keys. For those programs that need the value that *used* to be returned by the shift-down-arrow in the old ROM, you should be able to simulate that input by hitting a *shift-down-arrow followed by the Z key* (which will return a value of 26). If this feature had been implemented correctly in the old ROM, then the Electric Pencil word processor would not have needed a separate Control key added to the keyboard in order to function.

The regular unshifted down-arrow still returns its normal value in the new ROM. Since I work with several TRS-80s for a living, I think I have discovered *all* the unpleasant surprises that result from using the uppercase and lowercase TRS-80 and the improved Level II BASIC. I hope this information will alleviate most frustration that may otherwise result when using these machines.■

The Empire has expanded!

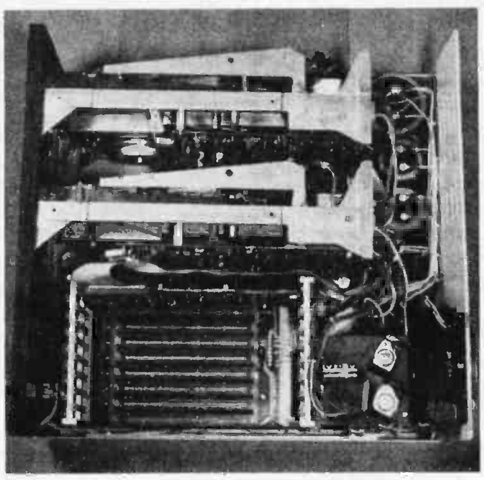


New Mainframe opens more areas for development

In one quantum leap Tarbell has expanded its popular Empire (the vertical disk subsystem) into a full line. This entire series now encompasses 5 variations. Each one contains different components so the S-100 system designer, hobbyist, or serious business user can arrive at the exact custom state he wants and needs.

The basic Empire still includes two Shugart or Siemens 8" disk drives; the compact cabinet with fan and power supply; a Tarbell floppy disk interface; CP/M*; Tarbell BASIC; the necessary cables, connectors and complete documentation. Naturally, it's fully assembled and Tarbell tested.

The new, top of the line Empire contains the basic model's components with the Tarbell design-approved Mainframe. Beside the *8-slot* S-100 motherboard with an active terminated bus, there's a cardcage with card guides and a double-density interface.



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BYTELINES

NEWS AND SPECULATION ABOUT PERSONAL COMPUTING

Conducted by Sol Libes

Floating-Point Standard Released: The IEEE floating-point standard has finally come out of committee. Basically, it is the Intel standard. Integrated-circuit manufacturers will now start producing mathematical-processing integrated circuits to follow this standard. It should come as no surprise to learn that Intel has already announced the 8087 Numeric Processor, the first to meet the standard. It will perform mathematical operations on signed and unsigned integers, real, binary-coded decimal, and floating-point numbers in 80-bit wide registers at a speed one hundred times faster than modern software. Intel expects to have samples of the device in early 1981.

Microprocessor-Controlled House Built: In Phoenix, Arizona, Motorola has created a microcomputer-controlled demonstration house. The computer manages interior climate, electrical consumption, security, and provides data-base functions. The computer automatically opens and closes doors and windows, and it controls an electrical and solar heating and cooling system to achieve optimum comfort with minimum electrical consumption. It also manages a fire/smoke detection system and motion detectors. There are no door keys; keypads, with a code assigned to each entrant, are used. Power consumption is tracked and reported regularly. A keyboard control console is provided. The display is a standard television. A calendar of events (appointments, birthdays, etc) can be maintained with a time/date function.

The system uses a Motorola 68000 (16-bit) microprocessor in the host computer. Five Motorola 6800 (8-bit) microprocessor-based computers communicate with the host in a five-node network. Each node controls a different part of the house, minimizing the effects of hardware failure.

Toy Robots Gaining Intelligence: Although toy robots have been around for many years, toy manufacturers are beginning to place microprocessors in them and provide keyboards for programmed control. Toy robots due to be introduced next year will include sensors and voice I/O (input/output).

Milton-Bradley (MB), one of the largest toy manufacturers in the US, currently sells a programmable toy tank called "Big Trak." It includes a Texas Instruments TMS1000 4-bit microprocessor, a twenty-key keyboard, 1 K-byte read-only memory (ROM) program, and a sixteen-instruction command set. The microprocessor controls the motor-driven wheels, lights, and produces sound effects. Over one million Big Traks were sold during the past year.

MB is spending $600,000 this year to develop new robotic toys. (Incidentally, that figure is comparable to the entire NASA robot research budget.) MB is adding a voice-synthesis integrated circuit that will generate twenty-two different words (costing a little over $3) with an additional twenty-two-word read-only memory (ROM) to be added (costing $1.65 per ROM). MB later plans to add sonic and contact sensing and possibly a manipulator.

Amateur robot builders should look into these toys as an inexpensive source of parts.

Slot Machines To Be Computerized: It was bound to happen! The State of Nevada's Gaming Commission has approved microprocessor-based slot machines. They will require less maintenance, and users will find it hard to cheat on them. Further, computerized slot machines will provide cost-accounting functions. Most of a slot machine's components are for security and anti-cheating. Next they may be plugged into a time-sharing network.

Is An Operating System Standard Possible? There are currently a number of problems caused by the lack of microcomputer operating-systems standards. People who use several different types of computers have the most problems. Standardization would help. However, according to Dr Robert Stewart, Chairman of the IEEE Computer Standards Committees, there doesn't appear to be much interest in developing such a standard. Dr Stewart is currently pursuing an alternative: a possible standard for interfacing software to operating systems. He is currently trying to set up a working group for the standard. Those interested in participating or learning more about the effort should call or write: Dr Robert G Stewart, Stewart Research Enterprises, 1658 Belvoir Dr, Los Altos CA 94022, (415) 941-6699.

Controller Applications At IECI-80: Every year since 1975, the IEEE's Industrial Electronic and Control Society has held a conference on computer applications for process control, automation, and data acquisition. Over the years the computers used have changed from minicomputers to microcomputers. Over eighty papers were presented at the most recent conference, with 50% written by persons from outside the US (a growing trend).

Some of the more interesting applications included the control of an experimental lumber kiln using a TRS-80 (University of New Hampshire); control of a natural-gas converter using a 6800-based processor (Hungary); automation of a sugar crystallization process using an 8085A microprocessor (Japan); a modular temperature controller

using an Intel 8048 (Georgia Tech); a machine controller using an Intel SDK-80 microcomputer; an industrial robot using a 16-bit Texas Instruments SP-990/16 microcomputer (Italy); an amusement ride controller using an Intel MCS-85 microcomputer; a diesel-engine generator controller using a Motorola 6800; and an automobile highway-type cruise control using an RCA 1802. Copies of the proceedings are available for $25 from the IEEE, 445 Hoes Ln, Piscataway NJ 08854.

32-Bit Personal Computer? Now that Intel is about to start shipping samples of its new 32-bit microprocessor, when can we expect to see a 32-bit personal computer? This is very far off, if it ever becomes a reality. The 32-bit machine would be "overkill" for a personal computer. Intel has defined the following applications for the device: as a front-end processor for large systems, controller for large PABX (private automated branch exchange) systems, sophisticated scientific processor, computer-aided design processor, data-base computer, large multi-user data processing, and graphics.

Intel has released only sketchy details on the device. It will have 4-gigabyte addressing, virtual-memory support, 32-bit integer and 64-bit floating-point mathematics processing, multi-operand instructions with vector and record addressing modes, memory-protection facilities, and high-level language compilation and execution. It will contain approximately 450,000 transistors.

Intel also has other interesting integrated circuits in development due for introduction next year. There are 8 K by 8, 16 K by 8 and 32 K by 8 EPROMs (erasable programmable read-only memories), and a 2 K by 8 electrically reprogrammable EPROM. Memory-error-correction and data-encryption integrated circuits and a system for networking up to thirty-two users are also in development.

The IBM "Gotcha": IBM has introduced a new word-processor system, called "Displaywriter," with an advertised $7895 price tag. This puts IBM in a strong competitive position. Competitors are charging $12-15,000 for stand-alone word-processing systems. In fact, IBM has a very good price compared to most personal-computer-based word-processing systems, which generally sell in the $5-8000 range. But there are some hidden "gotchas."

The IBM system does not include training or installation. If you need help, there is a thirty-day toll-free help number to call. If you need on-site help, it costs $56 per hour.

The biggest "gotcha" is that the purchase price does not include software. In fact, the software is not for sale. It must be rented at $15 to $50 per month. In other words, if you keep the word processor five years, the system will cost another $900 to $3000. The likelihood is that all word-processor makers will follow suit with a similar unbundled pricing policy.

A Buyer's Market In Personal Computers: In southern California, Texas Instruments (TI) has increased the rebate on its Model 99/4 personal-computer from $100 to $200. There are rumors that the rebate may go higher. Apparently TI is having some problems marketing the 99/4. Some dealers are discounting the 99/4 as much as 27%. Thus the 99/4, with a $950 list price (less monitor), can be bought for $695, and you still get the $200 rebate.

Texas Instruments is not alone. The California area has a proliferation of computer stores, and competition is keen. Apple IIs are being discounted as much as $250 below list price ($1195), the Atari 800 is selling for a low of $699 (list price $1080), and the Atari 400 as low as $449 (list price $630). The HP-85 is also being discounted and is selling for $2875 or less (list price $3250).

Radio Shack is also discounting. The TRS-80 Model I with 16 K bytes of programmable memory is being sold for $100 off the list price, and one Radio Shack dealer, TSE/Hardside of Milford, New Hampshire, is offering a 21% discount off the $849 list price (ie: $699).

16-Bit Microcomputer Hardware and Software Now Available: The new Intel 8086 and Zilog/AMD Z8000 16-bit microprocessors are now available for S-100-based microcomputers. So far, only Texas Instruments has introduced an integrated 16-bit personal computer. The new Apple III continues to use the 6502A 8-bit microprocessor, and it appears that the new systems from Radio Shack and Commodore will also continue to use 8-bit microprocessors. Microcomputer users who wish to step up to 16-bit systems will be limited to S-100 systems. There are several 16-bit processors currently available including the Intel 8086, Zilog Z8002, Texas Instruments TMS9900, Digital Equipment Corporation LSI-11, and the Western Digital Micro-Engine. Also available are the Intel 8088 and Motorola 6809, which are really 16-bit microprocessors with 8-bit I/O. Samples of the Motorola 68000 are currently being sent to original-equipment manufacturers. Limited production is slated to begin soon.

Some 16-bit microcomputer software is already available. Single-user 8086 BASIC and disk operating systems are available from Microsoft, and 8086 CP/M will soon be released by Digital Research. Pascal is available for both the 8086 and Z8000. A limited implementation of the UNIX operating system for both 8086 and Z8000 will shortly be available from Microsoft. The suppliers of these software packages developed them on large computers with sophisticated cross-assemblers and simulators, permitting the introduction of this software at the same time that the hardware became available. As yet, no personal-computer software supplier has available resident 8086 or Z8000 assemblers and software development programs. Microsoft does have an 8086 assembler that runs on an 8080 system, and Quasar is selling an 8080 emulator to run on its Z8000 system.

Commodore Introduces $199 Computer: A new low price in personal computers has been reached by Commodore Business Machines (CBM). CBM is about to market the "Video Interface Computer" (VIC) with a list price of $199. The VIC will use the old PET keyboard, an external television monitor, have limited PET BASIC, a light pen, a joystick, a 32-character by 25-line display, 184-by-200 point graphics, and a sound synthesizer. It will be sold as a "hobbyist" computer with no software support. A color unit will be available for $299.95. A unit with more memory and a better keyboard will sell for $399.95.

Backing Up Winchesters: Although Winchester hard-disk systems have provided the advantage of megabyte data storage, they have created a new problem of

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backup storage. With the floppy disk, backup was easy: just make a copy on another floppy disk in the same drive. However, the Winchester disks, with few exceptions, are fixed-disk-type drives, and the disks are not removable.

Manufacturers are turning back to magnetic tape for economical backup systems. Currently the quarter-inch tape cartridge is proving the most popular for under 30 megabytes of backup. The newer systems use a "streaming" technique of nonstop recording and playback. Data is transferred in a continuous stream with no starts and stops until all the data has been transferred to or from the disk. This allows for a low-cost system since searching for and transferring single records is eliminated. However, the trend will no doubt be to include the tape-cartridge controller as part of the disk controller. For example, Shugart Associates is incorporating a tape-cartridge backup controller into its new SA1400 hard-disk drive controller.

Pixel Corporation of Belmont, Massachusetts, expects to introduce a 270-megabyte backup tape system that uses an inexpensive consumer-grade videotape transport. Several copies of the disk data will be made on one videotape reel to ensure data integrity against bit dropouts. Also rumored to be in development is a 1-gigabyte tape drive integrated with an 8-inch Winchester disk system.

Ada May Be Available Next Year: Ada is a new language which is a superextension of Pascal. The US Defense Department has funded development of Ada as a standardized language. Next year will likely see the availability of the first Ada compilers. SofTech Inc, Waltham, Massachusetts, has undertaken the development of what promises to be the first Ada compiler. SofTech is presently defining environmental requirements and developing sets of tests and tools for validating Ada compilers. Its first implementation will be hosted on a Digital Equipment Corporation VAX-11 and will generate code for the VAX-11, PDP-11, and AN/GYK-12 machines.

Meanwhile, Dr Ken Bowles, the "father" of UCSD Pascal, has disclosed that he plans to implement Ada on a microcomputer using the same p-code approach used in UCSD Pascal.

Intel has announced that its new 32-bit microprocessor will execute Ada code directly. Samples of the microprocessor should be available early next year. However, no company has yet disclosed plans for a compatible Ada compiler.

Mail: I receive a large number of letters each month, as a result of this column. If you write to me and wish a response, please enclose a self-addressed, stamped envelope.

Sol Libes
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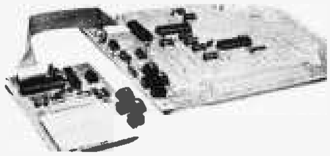

Level "A" With Hex Keypad/Display.

LEVEL "A" SPECIFICATIONS

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PC Board: Glass epoxy, plated through holes with solder mask. • **I/O:** Provisions for 25-pin (DB25) connector for terminal serial I/O, which can also support a paper tape reader . . . cassette tape recorder input and output . . . cassette tape control output . . . LED output indicator on SOD (serial output) line . . . printer interface (less drivers) . . . total of four 8-bit plus one 8-bit I/O ports. • **Crystal Frequency:** 6.144 MHz. • **Control Switches:** Reset and user (RST 7.5) interrupt . . . additional provisions for RST 5.5, 6.5 and TRAP interrupts onboard. • **Counter/Timer:** Programmable, 14-bit binary. • **System RAM:** 256 bytes located at F800, ideal for smaller systems and for use as an isolated stack area in expanded systems . . . RAM expandable to 64K via S-100 bus or 4k on motherboard.

System Monitor (Terminal Version): 2k bytes of deluxe system monitor ROM located at F000, leaving 0000 free for user RAM/ROM. Features include tape load with labeling . . . examine/change contents of memory . . . insert data . . . warm start . . . examine and change all registers . . . single step with register display at each break point, a debugging/training feature . . . go to execution address . . . move blocks of memory from one location to another . . . fill blocks of memory with a constant . . . display blocks of memory . . . automatic baud rate selection to 9600 baud . . . variable display line length control (1-255 characters/line) . . . channelized I/O monitor routine with 8-bit parallel output for high-speed printer . . . serial console in and console out channel so that monitor can communicate with I/O ports.

System Monitor (Hex Keypad/Display Version): Tape load with labeling . . . tape dump with labeling . . . examine/change contents of memory . . . insert data . . . warm start . . . examine and change all registers . . . single step with register display at each break point . . . go to execution address. Level "A" in this version makes a perfect controller for industrial applications, and is programmed using the Netronics Hex Keypad/Display. It is low cost, perfect for beginners.

HEX KEYPAD/DISPLAY SPECIFICATIONS

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Explorer/85 With Level "C" Card Cage.

LEVEL "D" SPECIFICATIONS

Level "D" provides 4k of RAM, power supply regulation, filtering decoupling components and sockets to expand your Explorer/85 memory to 4k (plus the original 256 bytes located in the 8155A). The static RAM can be located anywhere from 0000 to EFFF in 4k blocks.

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Level "E" adds sockets for 8k of EPROM to use the popular Intel 2716 or the TI 2516. It includes all sockets, power supply regulator, heat sink, filtering and decoupling components. Sockets may also be used for 2k x 8 RAM IC's (allowing for up to 12k of onboard RAM).

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APL Makes Life Easy (and Vice Versa)

Selby Evans, PhD, Texas Christian University, Forth Worth TX *76129*

With the APL language becoming available on Z80 systems, staunch players of John Horton Conway's game of Life won't be left out and neither will any new or prospective players. Here's a new APL version of the game you can use to discover *blinkers, spaceships, glider guns, puffer trains, burloaferimeters,* and many of this favorite pastime's other inherent beasts. (See the December 1978 BYTE theme articles about Life, a game derived from the field of automata theory.) This APL version is much easier to follow than the one-line program presented by Mark Niemiec in his article "Life Algorithms" (January 1979 BYTE, page 90). It is written not to show the language's suitability for compact expression, but to illustrate the ease of programming in APL.

Listing 1 presents the functions. GEN takes one generation and maps it into the next. Lines 1 thru 3 count the neighbors of each cell by rotating the matrix to bring each neighbor over the cell. Assuming that live cells are represented by 1s and dead cells represented by 0s, the sum of these rotated matrices counts the live neighbors for each cell. The rotations wrap around at the borders, so that the Life space (or universe) has no borders. (The surface is a donut or torus.) Line 4 of GEN specifies a new set of live cells according to the following rules of Life:

> A dead cell becomes live in the new generation if it has three neighbors in the current generation. A live cell stays live if it has exactly two or three neighbors in the current generation. All other cells will be dead.

The LIFE function iterates over generations, provides a display of the result, and puts the generation number in the upper-left corner. It requires as right argument X a matrix of 1s and 0s giving the starting state. An array of any size may be used as long as it will fit in the workspace. Because the life space is a closed surface, the size of the matrix influences what happens. A glider crossing the left edge, for example, will reappear at the right edge. With a matrix of appropriate size, a glider gun might promptly shoot itself in the back.

Listing 2 illustrates the output of the LIFE program and shows what happens to BYTE after a few generations of Life. The BYTE editors will no doubt be pleased to see that a heart is revealed after eleven generations. [*Hmm.... There's a moral here, but I'm not sure I know what it is....*GW]

After displaying one generation, the LIFE program pauses and waits for a carriage return. It is sometimes convenient to skip the output of some generations in order to follow the development through more generations. If you type a number before pressing carriage return, the program will skip ahead that many generations before displaying a new generation. Entering a 0 at that point will end the function.

So have some fun with automata theory and learn something new about APL. ■

Listing 1: *APL functions for Life program. See text for details.*

```
      ∇ L←GEN X
[1]     R←1⌽X
[2]     R←(L←¯1⌽X)+(1⊖X)+(¯1⊖X)+R+(1⊖R)+¯1⊖R
[3]     R←R+(1⊖L)+¯1⊖L
[4]     L←(R=3)∨X∧R=2
      ∇

      ∇ LIFE X;R;N;C
[1]     N←0
[2]     ST:R←,(⍴X)⍴' '
[3]     R[(1=,X)/⍳⍴R]←'○'
[4]     C←'|',('-',[1]((⍴X)⍴R),[1]'-'),'|'
[5]     C[1;1+⍳5]←,1⌽'I5'ΔFMT N
[6]     C
[7]     →0×⍳0=C←1↑⍎⍞,' 1'
[8]     N←N+C
[9]     GN:X←GEN X
[10]    →(ST×⍳0≥C←C-1),GN
[11]    ⍝THE MONADIC ⍎ IN LINE 7 IS THE EXECUTE FUNCTION.
      ∇
```

Listing 2: *An example of the APL function LIFE at work. The frames shown here are from successive generations of a Life colony that begins as a collection of cells that spell the word BYTE. The generation number of each frame is shown in the upper left-hand corner.*

```
0 ------------------------------------


  OOOO     O   O    OOOOO    OOOOO
  O   O    O   O      O      O
  OOOO     O   O      O      OOOO
  O   O    OO OO      O      O
  O   O      O        O      O
  OOOO       O        O      OOOOO

--------------------------------------
1 ------------------------------------

   OO                OOO      OOO
  OOOO               OOO     OOOO
 O    O   OOO OOO           O    O
 OO OOO   OO   OO    OOO    OO O
 OO O O    OOOOO     OOO    OO O
 OO O O      O       OOO    OO OO
  OOOO                       OOOO
   OO                         OOO

--------------------------------------
2 ------------------------------------
                      O        O
  O  O               O O     O  O
  O  O     O   O     O O     O   O
 O    O   O O O O           O
O   O OO             O O   O    O
O   O OO  OO O OO   O   O  O   O
      O      O       O O
 O                    O     O    O
  O  O                       O  O
                               O
--------------------------------------
```

```
10 -----------------------------------
  OOO     O
 O   O   O O
O     O  O O
   O      O
                 O   O
OO O OO         OO   OO
 O   O         OO     OO
  O O           OO   OO
   O             OOOOO
                  OOO
                   O
--------------------------------------
11 -----------------------------------
   O
  OOO     O
 OOOOO   O O
         O O
          O

  O O           OO   OO
OOO OOO        O O   O O
OO O OO        O       O
  OOO          O   O   O
   O            O     O
                 O   O
                  OOO
--------------------------------------
12 -----------------------------------
  OOO              O
 O   O    O
 O   O   O O
  OOO    O O
          O
  O O           OO   OO
O     O        O O   O O
O     O       OO       OO
 O   O         OO     OO
  OOO           O     O
                 OOOOO
                  OOO
--------------------------------------
```

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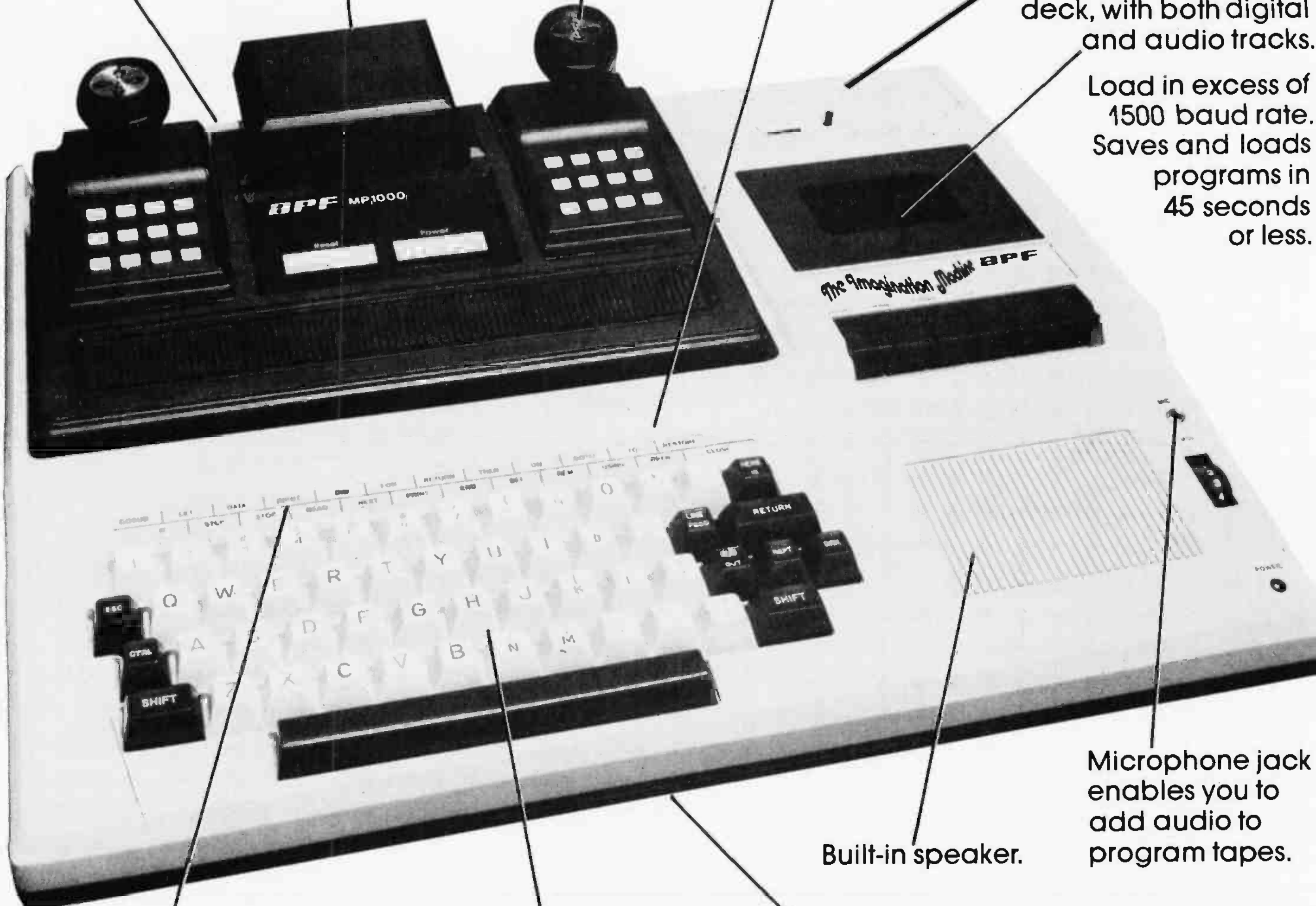

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FLOPTRAN-IV: A Tiny Compiler

Mark Zimmermann
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These "programmers' programs" allowed a user to write in a language that is more compact and meaningful for humans than machine language.

In the beginning, computers were programmed in machine language. To execute a simple equation, such as A=B, a user had to write dozens of instructions. He had to tell the machine, "load the accumulator with the first byte of the number B," and "store the accumulator in the memory location assigned to the first byte of A," *ad nauseam*. A more complicated equation like C=LOG(D) required hundreds or even thousands of instructions! It's no wonder, therefore, that among the first programs developed were programs to make it easier to write other programs. These "programmers' programs" allowed a user to give the computer instructions in a higher-level language, one that is more compact and meaningful for humans than machine language.

High-level computer languages are nonsense to a machine until they have been translated into fundamental commands that the system can understand and execute. There are two principal methods used to perform this translation: interpretation and compilation. An *interpreter* is a machine-language program that scans through a higher-level program, line by line. As each statement is encountered, the interpreter figures out which operations are necessary to execute that statement, then goes ahead and performs the operations. The interpreter then moves on to the next statement, translates it, and executes it. This process is repeated, with each statement being interpreted (or reinterpreted) *every* time it is executed.

A compiler acts rather differently. Like an interpreter, it scans through a high-level program and figures out what fundamental operations are necessary to execute each line. But, instead of performing those operations, a compiler just writes out (ie: onto a cassette tape drive) the sequence of machine-language instructions that do the job when executed. An interpreter executes a program statement by statement, as it interprets it, so that the interpreter and the program execute concurrently. But, when a compiler is finished with a program, the result is a machine-language program that represents the higher-level program; the machine-language program must be loaded back into the computer and executed before the problem being programmed is solved.

The two approaches, compilation and interpretation, have different strengths and weaknesses. An interpreter, interpreting and executing line by line, can stop at the first sign of an error and give a helpful and specific error message. The interpretation can also be interrupted at any point (to be later resumed) allowing the human operator to look at the partial results of the calculation and see whether everything is going as planned. This interactive technique makes program development and debugging relatively easy.

On the other hand, when an interpreter has finished running a job, the machine is no "smarter" than when it began. Executing the program a second time will take just as long as it did the first time. In fact, if there is looping within the program so that some lines are executed more than once, these lines are completely reinterpreted, as if they had never been seen before, each time they are encountered. This redundant interpretation wastes a lot of computer time, making interpreted programs somewhat slower than compiled ones.

However, once a compiler has finished with a program, the result is a pure machine-language series of instructions that can be executed without further translation. Although this results in more vague error messages, the advantage to compilation is speed. Depending on the problem, a compiled program typically executes several times faster than an interpreted one—sometimes, the speed advantage is as large as a factor of 100. Once a program has been compiled, it never needs to be compiled again.

The output of a compiler does tend to be larger than the original source program (which the interpreter uses), so that interpreters may seem to have the advantage in terms of memory usage. But, when one remembers that the interpreter must be continuously resident in the computer's memory while the program is running, whereas the compiler can be removed after the program has been compiled, the apparent memory advantage of interpretation over compilation shrinks and often vanishes.

Operator	Meaning
+	add
−	subtract
*	multiply
/	divide
↑	exponentiation
ABS	absolute value
ATN	arctangent
COS	cosine
EXP	powers of e
FRE	memory available
INT	integer portion of argument
LOG	base-e logarithm
PEEK	look at contents of memory
POS	position of cursor
RND	random number
SGN	sign of argument
SIN	sine
SQR	square root
TAN	tangent

Table 1: *Available operators and functions in FLOPTRAN-IV.*

Some languages, such as FORTRAN, are usually compiled and are hardly ever interpreted. Other languages, like BASIC, are generally interpreted. Many small-computer systems come with a built-in or easily-loaded BASIC interpreter, but to get a compiled language, it is necessary to pay hundreds of dollars (or more) for extra memory, disk storage, and a compiler.

But there is no reason why a language like BASIC should not be compiled instead of interpreted. Also, there is no reason to ignore or throw away the wonderful resource that a typical BASIC in read-only memory represents. In those read-only memories are hidden dozens of useful, thoroughly tested, efficient machine-language subroutines; it would be a shame not to take full advantage of them.

What I've done is to write a tiny compiler for a language I call FLOPTRAN-IV, which stands for *FLOating-Point TRANslator, version 4*. The compiler is written in Microsoft (PET) BASIC and is presented in full in listing 1. As written and debugged, the FLOPTRAN-IV compiler runs on an original-version 8 K-byte Commodore PET. The new PETs, which have a different set of read-only memory chips, have moved many of the subroutine entry points so that, to run FLOPTRAN on such a machine, it will be necessary to find the new addresses and change them as they appear in the program of listing 1.

Other 6502-microprocessor machines using Microsoft BASIC, such as the Apple and Ohio Scientific systems, will require more extensive changes in the FLOPTRAN compiler in order to make it operational, although the overall structure of the compiler should still be applicable. In fact, the idea of a tiny compiler that uses the resident BASIC subroutines to do the bulk of its work is extremely general and applicable to systems using *any* microprocessor. Once I had thought of the concept, it took me only a couple of days to get the compiler up and running; anyone with an intimate knowledge of his personal system should be able to do as well.

Introduction to FLOPTRAN-IV

FLOPTRAN, the floating-point translator, is so named because it is heavily oriented toward floating-point mathematical operations. For compatibility with the PET's read-only memory routines, it uses the standard Microsoft format for storing numbers: five 8-bit bytes, with 1 byte for the exponent (power of 2) and 4 bytes for the fractional part (or mantissa) of the number and its sign. Built into FLOPTRAN are the functions given in table 1; the ability to call a user-defined machine-language function USR is also included, although it may be used infrequently. [*Several articles on computer representation of floating-point numbers may be found in the book* Numbers in Theory and Practice, *which is edited by Blaise W Liffick and is available from BYTE Books....***RSS**]

A FLOPTRAN program looks like a BASIC program and, with one particular exception, it *is* a legal BASIC program. That exception is the use of the RETURN statement to end the program, as well as to signal a return-from-subroutine. This is done so that the compiled FLOPTRAN program ends with the 6502 instruction RTS (return-from-subroutine); thus, after the compiled program is run using the SYS command, control will return to the PET operating system.

Because FLOPTRAN is essentially BASIC, it is easy to test and debug a FLOPTRAN program by using the BASIC interpreter built into the PET. When the program has been fully debugged, the compiler program need only be executed once; thereafter, the compiled machine-language program can be executed directly.

Note that the PET's Microsoft BASIC interpreter stores the reserved words (ie: keywords) of the BASIC language as single bytes in memory: GOTO is stored as the single-

Text continued on page 212

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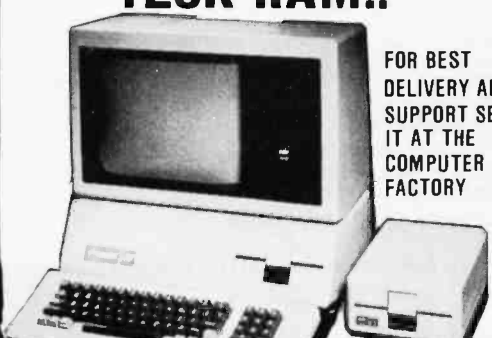

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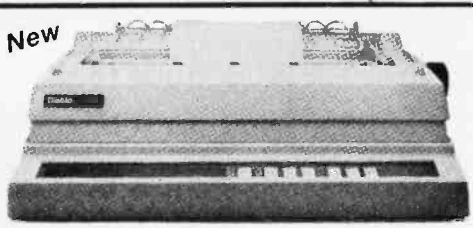

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How to Use the FLOPTRAN-IV Compiler

To write and compile a program:

1) *Load the FLOPTRAN-IV compiler program of listing 1.*
2) *Write the program to be compiled in FLOPTRAN (see summary of syntax in table 2) giving statements line numbers in the range 0 thru 255, and terminating the FLOPTRAN program with a RETURN statement instead of END.*
3) *Optional: you may want to test the uncompiled FLOPTRAN program using the BASIC interpreter; if you change the terminal RETURN to an END or STOP for that purpose, be sure to change it back before compiling.*
4) *To compile, place a blank cassette in the PET tape drive and type RUN 50000. The compiled program will be written to the cassette.*

To load and execute a compiled program:

1) *Type NEW, then load and run the program in listing 3. This loads the compiled program's origin (the first thing FLOPTRAN writes to tape), then loads the program until it hits the "—1" signal that marks the end of the first pass. It then loads the addresses of JMP or JSR targets to be corrected until it hits the final "—1" marking the end of the second pass; this is the end of the data file.*
2) *To run the compiled program now in memory, type SYS(nnnn), where nnnn is the decimal number given in the "BEGIN AT nnnn" message from listing 3.*

Note: FLOPTRAN-IV as presently designed is for old PET read-only-memory computers only. Many addresses will have to be changed for this compiler to work with new PETs.

Listing 1: *FLOPTRAN-IV compiler program for the original-version PET. This program will convert a FLOPTRAN-IV program (actually a subset of BASIC) to an executable machine-code program, which is written to the PET cassette tape drive to be loaded at a later time. When typing this listing into a PET, all the statements associated with one line number are to be typed on the same line, separated by colons.*

```
49000 X=                                              ;;;leave at least 60 blanks here
     :RETURN                                          ;;;to be filled in during a 'LET' operation

49100 TP=TP+1                                         ;;;subroutine to get next nonblank character
     :CH=PEEK(TP)                                     ;;;and return it in CH
     :IF CH=32 GOTO 49100

49120 RETURN

49190 IF (CH>64) AND (CH<91) GOTO 49300               ;;;64<CH<91 means alphabetic, legal variable name

49200 PRINT                                           ;;;abort if unexpected character found
     :PRINT "***ERROR IN LINE";LI;"***"
     :GOTO 61000

49300 Z=5*(CH-65)+OV                                  ;;;return the address (5 byte location) of the variable
     :ZH=INT(Z/256)                                   ;;;'CH'...high and low parts of address in ZH & ZL
     :ZL=Z-256*ZH
     :RETURN

49400 PRINT#1,169                                     ;;;LDA #ZL
     :PRINT#1,ZL
     :PRINT#1,160                                     ;;;LDY #ZH
     :PRINT#1,ZH

49420 PRINT#1,32                                      ;;;JSR $DA74 with A & Y  set up as above
     :PRINT#1,116                                     ;;;transfers the value of the variable being
     :PRINT#1,218                                     ;;;pointed at to the primary accumulator for floating-
     :PC=PC+7                                         ;;;-point operations, 'PRI'
     :RETURN                                          ;;;add 7 bytes to the program-counter & return

49600 DATA 11,219,158,219,42,219,0,0,98,210,133,210   ;;;data for floating-point ROM subroutine calls, 2-byte pairs
                                                      ;;;SGN,INT,ABS,USR,FRE,POS
49640 DATA 36,222,69,223,191,216,160,222,158,223,165,223
                                                      ;;;SQR,RND,LOG,EXP,COS,SIN
49680 DATA 238,223,72,224,230,214,60,215,40,215,253,216,228,217,46,222
                                                      ;;;TAN,ATN,PEEK,+,-,*,/,^
```

Listing 1 continued on page 202

Listing 1 continued:

```
49720 FOR X=0 TO 19
      :READ MLZ(X,0),MLZ(X,1)                    ;;;load addresses into MLZ array, low byte, then high
      :NEXT X

49740 FOR X=0 TO 255
      :LNZ(X)=-32767                             ;;;initialize LNZ array of line numbers so that nonexistent
      :NEXT X                                    ;;;lines will be flagged later
      :RETURN

50000 DIM X,LNZ(255),GOZ(127,1),MLZ(19,1)        ;;;RUN 50000 to enter program here & compile code
      :P=1025                                    ;;;dimension X first so make it easy to find later
      :GC=0                                      ;;;initialize pointer P & GOTO/GOSUB counter GC

50040 L=PEEK(P+2)+256*PEEK(P+3)                  ;;;look up line number & scan
      :IF L<>49000 THEN P=PEEK(P)+256*PEEK(P+1)  ;;;to locate subroutine 49000 to be used in 'LET'
      :GOTO 50040                                ;;;assignments during later compilation

50100 XL=P+6                                     ;;;store location  of first space after '=' in line 49000 in XL
      :GOSUB 49600                               ;;;initialize MLZ and LNZ arrays
      :INPUT "COMPILED DATA FILE NAME";C$
      :OPEN 1,1,1,C$                             ;;;get file name & open data file for compiled program

50120 INPUT "ORIGIN FOR CODE";OC                 ;;;OC stores starting location for compilation
      :PRINT#1,OC                                ;;;write it to tape to begin data file
      :PC=OC                                     ;;;initialize program counter PC

50140 INPUT "VARIABLE TABLE ORIGIN";OV           ;;;variables occupy 26*5 contiguous locations beginning at OV
      :TP=1028                                   ;;;initialize text pointer to first line number of BASIC program

50200 LI=PEEK(TP-1)+256*PEEK(TP)                 ;;;put line number in LI
      :IF LI>255 GOTO 60000                      ;;;compiling program has lines in range 0-255----exit when finished

50220 LNZ(LI)=PC-32767                           ;;;store current PC in LNZ(LI) to be used in GOTOs or GOSUBs later
      :PRINT "COMPILING LINE";LI                 ;;;announce to screen what line is being compiled now

50240 GOSUB 49100                                ;;;get next nonblank character in CH

50260 IF CH=0 THEN TP=TP+4                       ;;;'0' is end-of-line marker----move text pointer forward and
      :GOTO 50200                                ;;;loop to get next line number

50280 IF CH=58 GOTO 50240                        ;;;'58' is ':'----loop back to allow multiple statements/line

50300 IF CH=136 GOTO 58000                       ;;;'136' is 'LET'

50320 IF CH=153 GOTO 59000                       ;;;'153' is 'PRINT'

50340 IF CH=133 GOTO 59500                       ;;;'133' is 'INPUT'

50360 IF CH=139 GOTO 58500                       ;;;'139' is 'IF'

50380 IF (CH=137) OR (CH=141) GOTO 58700         ;;;'137' is 'GOTO' and '141' is 'GOSUB'

50400 IF CH=143 GOTO 56500                       ;;;'143' is 'REM'

50420 IF CH=142 THEN PRINT#1,96                  ;;;'142' is 'RETURN', the 6502 'RTS' instruction, 96 decimal
      :PC=PC+1                                   ;;;'RETURN' also ends the compiled program & returns to BASIC after
      :GOTO 50240                                ;;;a 'SYS' command starts machine-language

50440 GOSUB 49190                                ;;;if none of the above, it better be a variable name----check it


      :VL=ZL                                     ;;;and store the storage address in VL, VH
      :VH=ZH

50460 GOSUB 49100                                ;;;get next character
      :IF CH<>178 GOTO 49200                     ;;;it had better be an '=' sign...abort if not!

50480 GOSUB 49100                                ;;;next character
      :IF (CH>179) AND (CH<195) GOTO 51000       ;;;179<CH<195 means a monadic function

50500 IF CH=171 GOTO 55600                       ;;;'171' is a '-' sign

50520 GOSUB 49190                                ;;;otherwise, it better be a variable name....
      :WL=ZL                                     ;;;store the address of the variable in WL, WH
      :WH=ZH
```

Listing 1 continued on page 204

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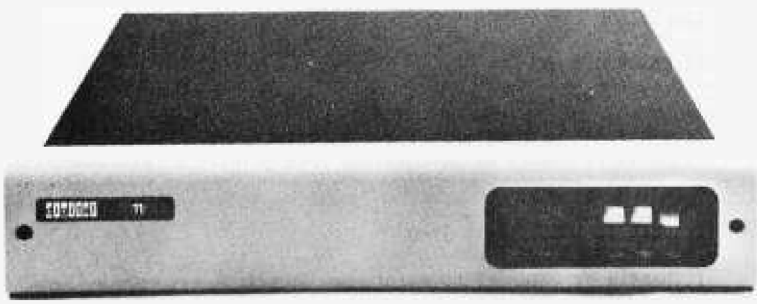

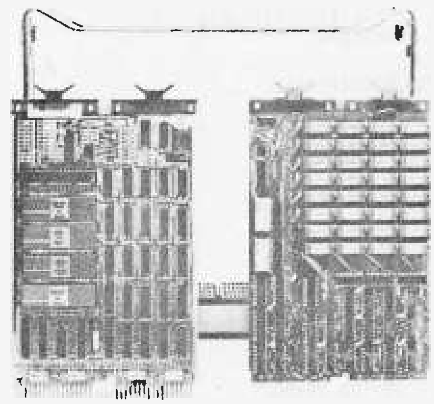

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Listing 1 continued:

```
50540 GOSUB 49100
      :IF (CH=0) OR (CH=58) GOTO 58300              ;;;if 'end-of-line' or ':', equation is of the form 'V=W'

50560 IF (CH<170) OR (CH>174) GOTO 49200             ;;;otherwise, expect +,-,*,/,^ and abort if not

50580 FU=CH-155                                      ;;;FU now records what operator it was
      :GOSUB 49100                                   ;;;get next character
      :GOSUB 49190                                   ;;;better be variable name...address in ZL, ZH
      :GOSUB 49400                                   ;;;write out code to transfer it to primary accumulator

50660 PRINT#1,169                                    ;;;LDA #WL
      :PRINT#1,WL
      :PRINT#1,160                                   ;;;LDY #WH
      :PRINT#1,WH
      :PC=PC+4                                       ;;;count the bytes and increment program counter

50700 IF (FU=15) OR (FU=17) GOTO 51080               ;;;take shortcut for '+' or '*' functions

50720 PRINT#1,32                                     ;;;JSR $D95E transfers 'W' to secondary accumulator
      :PRINT#1,94                                    ;;;and sets up for dyadic operation subroutine call
      :PRINT#1,217
      :PC=PC+3                                       ;;;count the bytes...
      :GOTO 51080                                    ;;;jump down to output code to do the operation & store result

51000 FU=CH-180                                      ;;;arrive here to perform a monadic function
      :GOSUB 49100
      :IF CH<>40 GOTO 49200                          ;;;next character better be a '(', else abort!

51040 GOSUB 49100
      :GOSUB 49190                                   ;;;get argument  of function, address in ZL, ZH
      :GOSUB 49400                                   ;;;fetch it to primary floating accumulator

51060 GOSUB 49100
      :IF CH<>41 GOTO 49200                          ;;;expect to see a ')' here!!!

51080 PRINT#1,32                                     ;;;JSR to ROM function
      :PRINT#1,ML%(FU,0)
      :PRINT#1,ML%(FU,1)
      :PC=PC+3

51100 PRINT#1,162                                    ;;;LDX #VL
      :PRINT#1,VL
      :PRINT#1,160                                   ;;;LDY #VH
      :PRINT#1,VH

51120 PRINT#1,32                                     ;;;JSR $DAA6 with target in X & Y registers
      :PRINT#1,166                                   ;;;to store result of calculation from primary accumulator
      :PRINT#1,218
      :PC=PC+7
      :GOTO 50240                                    ;;;back to top of main loop

55600 GOSUB 49100                                    ;;;handle monadic '-' operator
      :GOSUB 49190
      :GOSUB 49400                                   ;;;transfer number to be negated to primary floating accumulator
      :PRINT#1,169                                   ;;;LDA #$FF
      :PRINT#1,255

55660 PRINT#1,69                                     ;;;EOR $B5 (sign storage for primary accumulator)
      :PRINT#1,181
      :PRINT#1,133                                   ;;;STA $B5....now sign is flipped
      :PRINT#1,181
      :PC=PC+6
      :GOTO 51100                                    ;;;go store negated number in target

56500 GOSUB 49100                                    ;;;handle 'REM' statement
      :IF CH>0 GOTO 56500                            ;;;loop until end-of-line encountered

56540 GOTO 50260                                     ;;;back to top of main loop

58000 GOSUB 49100                                    ;;;handle 'LET' assignment operation
      :GOSUB 49190                                   ;;;get address for result to be stored into
      :GOSUB 49100                                   ;;;this character better be an '=' sign
      :VL=TP+1                                       ;;;save pointer to first character after '=' in VL
      :IF CH<>178 GOTO 49200                         ;;;abort if it wasn't '='

58080 GOSUB 49100
      :IF (CH<>58) AND (CH<>0) GOTO 58080            ;;;scan until ':' or 'end-of-line' terminates assignment
```

Listing 1 continued on page 206

CP/M* compatible software

SYSTEM MAINTENANCE

DIAGNOSTICS I: Easily the most comprenensive set of CP/M compatible system check-out programs ever assembled. Finds hardware errors in your system, confirms suspicions, or just gives your system a clean bill of health.
Tests:

- Memory
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ACCOUNTING

ACCOUNTS PAYABLE/RECEIVABLE: A complete, user oriented package which features:

automatic postings to general ledger (optional)

accounts payable: • check printing with invoice • invoice aging

accounts receivable: • progress billing • customer statements • partial invoice payments • invoice aging

The entire package is menu driven and easy to learn and use. It incorporates error checking and excellent user displays. This package can be used stand alone or with the General Ledger below.

Supplied with extensive user manual: $200.00. Manual alone: $20.00.

GENERAL LEDGER: A complete, user oriented package which features:

- Accepts postings from external programs (i.e. AP/AR above)
- Accepts directly entered postings
- Maintains account balances for current month, quarter, and year and previous three quarters
- Financial reports: trial balance, income statement balance sheet, and more.

Completely menu driven and easy to learn and use. Excellent displays and error checking for trouble free operation. Can be used stand alone or with Accounts Payable/Receivable above.

Supplied with extensive user manual: $200.00. Manual alone: $20.00.

Both require 48K CP/M, terminal with cursor positioning, home and clear home, one 8" disk or Two 5" disks. CBASIC2 required.

TEXT PROCESSING

TFS—Text Formatting System: An extremely powerful formatter. More than 50 commands. Supports all major features including:

- left & right margin justification
- user defined macros
- dynamic insertion from disk file
- underlining and backspace

TFS lets you make multiple copies of any text. For example: Personalized form letters complete with name & address & other insertions from a disk file. Text is not limited to the size of RAM making TFS perfect for reports or any big job.

Text is entered using CP/M standard editor or most any CP/M compatible editor. TFS will link completely with Super-M-List making personalized form letters easy.

Requires: 24K CP/M.

Supplied with extensive user manual: $85.00. Manual alone: $20.00.

Source to TFS in 8080 assembler (can be assembled using standard CP/M assembler) plus user manual: $250.00.

MAILING LIST

SUPER-M-LIST: A complete, easy to use mailing list program package. Allows for two names, two address, city, state, zip and a three digit code field for added flexibility. Super-M-List can sort on any field and produce mailing labels direct to printer or disk file for later printing or use by other programs. Super-M-List is the perfect companion to TFS. Handles 1981 Zip Codes!

Requires: 48K CP/M.

Supplied with complete user manual: $75.00. Manual alone: $10.00

UTILITIES

Utility pack #1: A collection of programs that you will find useful and maybe even necessary in your daily work (we did!). Includes:

CMP: Compare two files for equality.
ARCHIVER: Compacts many files into one, useful when you run out of directory entries.
SORT: In core sort of variable length records.
XDIR: Extended, alphabetical directory listing with groupings by common extension.
PRINT: Formatted listings to printer.
PG: Lists files to CRT a page at a time
. . . plus more . . .

Requires 24K CP/M.

Supplied with instructions on discette: $50.00.

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Please specify CPU type: Z80 or 8080

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- recursive procedures/functions
- integer arithmetic
- CASE
- FOR (loop)
- sequential disk I/O
- one dimensional arrays
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- WHILE
- 'PEAK' & 'POKE'
- READ & WRITE
- REPEAT . . . UNTIL
- more

'Tiny' Pascal is fast. Programs execute up to ten times faster than similar BASIC programs.

SOURCE TOO! We still distribute source, in 'Tiny' Pascal, on each discette sold. You can even recompile the compiler, add features or just gain insight into compiler construction.

'Tiny' Pascal is perfect for writing text processors, real time control systems, virtually any application which requires high speed. Requires: 36K CP/M. Supplied with complete user manual and source on discette: $85.00.

Manual alone: $10.00.

SOFTWARE SECURITY

ENCODE/DECODE: A complete software security system for CP/M. Encode/Decode is a sophisticated coding program package which transforms data stored on disk into coded text which is completely unrecognizable. Encode/Decode supports multiple security levels and passwords. A user defined combination (One billion possible) is used to code and decode a file. Uses are unlimited. Below are a few examples:

- data bases
- general ledger
- inventory
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- accounts pay/rec
- programs
- tax records
- mailing lists

Encode/Decode is available in two versions:

Encode/Decode I provides a level of security suitable for normal use. Encode/Decode II provides enhanced security for the most demanding needs. Both versions come supplied on discette and with a complete user manual.

Encode/Decode I: $50.00

Encode/Decode II: $100.00 Manual alone: $15.00

INTERCOMPUTER COMMUNICATIONS

TERM: a complete intercommunications package for linking your computer to other computers. Link either to other CP/M computers or to large timesharing systems. TERM is comparable to other systems but costs less, delivers more and source is provided on discette!

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Requires: 32K CP/M.

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Listing 1 continued:

```
58100 IF TP-VL>60 THEN PRINT "LINE TOO LONG!"            ;;;subroutine 49000 only has room for 60 characters----sorry!
      :GOTO 49200

58120 FOR L=VL TO TP-1                                   ;;;take the whole expression to be evaluated for the 'LET'
      :WL=PEEK(L)
      :POKE XL+L-VL,WL                                   ;;;and POKE it into subroutine 49000
      :NEXT L

58160 GOSUB 49000                                        ;;;go evaluate the expression!----result returns in variable X



      :FOR L=VL TO TP-1
      :POKE XL+L-VL,32                                   ;;;and clean up (fill with blanks again) subroutine 49000
      :NEXT L

58180 PRINT#1,24                                         ;;;CLC
      :PRINT#1,144                                       ;;;BCC .+5   (a forced branch over the following 5 bytes)
      :PRINT#1,5
      :PC=PC+3
      :VL=256*PEEK(125)+PEEK(124)+2                      ;;;point VL to the place where X is stored now

58220 FOR L=VL TO VL+4                                   ;;;fetch all 5 bytes of the current value of X
      :PRINT#1,PEEK(L)                                   ;;;and write them into the compiled file
      :NEXT L
      :WH=INT(PC/256)                                    ;;;store their location in the compiled code in WH, WL
      :WL=PC-256*WH

58240 VL=ZL                                              ;;;put the address for the result of the 'LET' to be stored into
      :VH=ZH                                             ;;;in VL, VH, and fall into the 'assignment' handling routine
      :PC=PC+5

58300 PRINT#1,162                                        ;;;handle simple assignments of the form 'V=W' here
      :PRINT#1,4                                         ;;;LDX #4
      :PRINT#1,189                                       ;;;LDA W,X
      :PRINT#1,WL
      :PRINT#1,WH

58340 PRINT#1,157                                        ;;;STA V,X
      :PRINT#1,VL
      :PRINT#1,VH
      :PRINT#1,202                                       ;;;DEX

58360 PRINT#1,16                                         ;;;BPL .-9
      :PRINT#1,247
      :PC=PC+11                                          ;;;transfer finished...count bytes & back to main loop top
      :GOTO 50260

58500 GOSUB 49100                                        ;;;handle 'IF' statements
      :GOSUB 49190                                       ;;;get variable following the 'IF' ---- address in Z
      :PRINT#1,173                                       ;;;LDA Z
      :PRINT#1,ZL
      :PRINT#1,ZH
      :PRINT#1,240                                       ;;;BEQ .+3    (if variable = 0, skip over following 3 bytes)

58580 PRINT#1,3
      :PC=PC+5
      :GOSUB 49100                                       ;;;get next character
      :IF (CH<>137) AND (CH<>141) GOTO49200              ;;;abort if not 'GOTO' or 'GOSUB'----else, fall into following....

58700 IF CH=141 THEN PRINT#1,32                          ;;;handle  'GOSUB' or 'GOTO' statements
      :GOTO 58760                                        ;;;'GOSUB' becomes 'JSR'

58740 PRINT#1,76                                         ;;;and 'GOTO' becomes 'JMP'

58760 GO%(GC,0)=PC-32766                                 ;;;store in GO% array the address of the compiled-code's bytes after
      :PRINT#1,0                                         ;;;the opcode, to be filled in later (second-pass)
      :PRINT#1,0                                         ;;;print zeroes for now, to hold the spaces
      :PC=PC+3
      :TL=0                                              ;;;initialize target line number TL

58800 GOSUB 49100
      :IF (CH<48) OR (CH>57) GOTO 58840                  ;;;read in ASCII target line number

58820 TL=10*TL+CH-48                                     ;;;and convert it to a number in TL
      :GOTO 58800
```

Listing 1 continued on page 210

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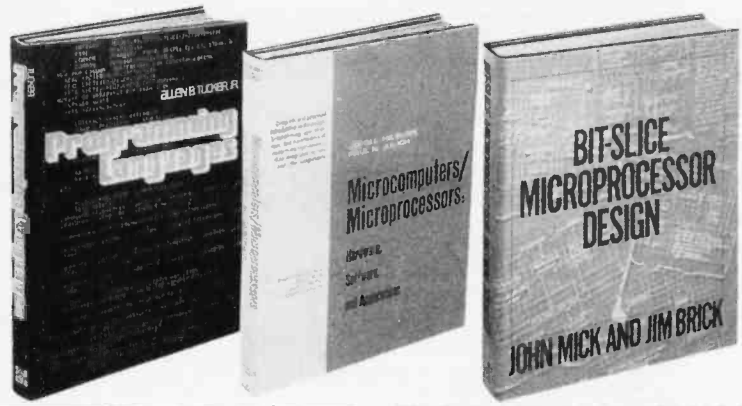

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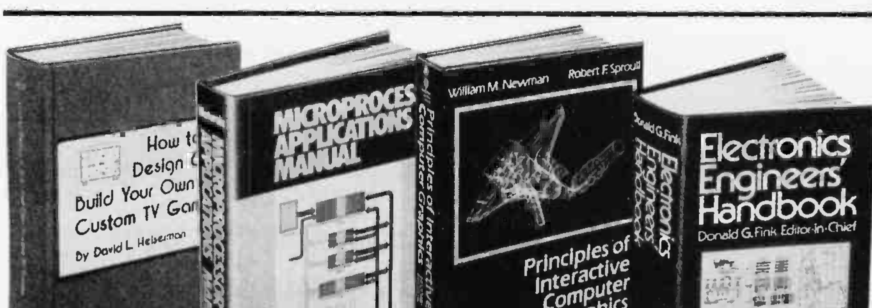

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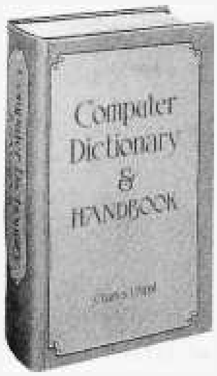

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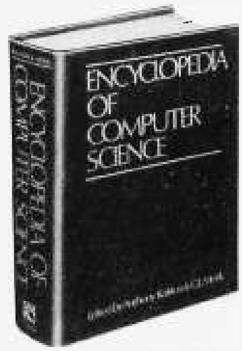

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Listing 1 continued:

```
58840 GO%(GC,1)=TL                              ;;;record target line number in GO%
      :GC=GC+1                                  ;;;increment GOTO/GOSUB counter GC
      :GOTO 50260                               ;;;back to top of main loop

59000 GOSUB 49100                               ;;;handle a 'PRINT' statement
      :IF (CH=0) OR (CH=58) GOTO 59400          ;;;when done with line or statement, print a <CRLF> before quitting

59040 IF (CH=44) OR (CH=59) GOTO 59000          ;;;keep going if ',' or ';' encountered within 'PRINT'

59080 GOSUB 49190                               ;;;get address of variable to be printed
      :GOSUB 49400                              ;;;transfer it to primary accumulator
      :PRINT#1,32                               ;;;JSR $DCAF converts it to ASCII string at top of page 1
      :PRINT#1,175
      :PRINT#1,220

59100 PRINT#1,162                               ;;;LDX #0
      :PRINT#1,0
      :PRINT#1,189                              ;;;LDA $100,X
      :PRINT#1,0
      :PRINT#1,1

59120 PRINT#1,240                               ;;;BEQ .+6   (end of string is marked by a zero)
      :PRINT#1,6
      :GOSUB 59300                              ;;;subroutine outputs code to print accumulator on screen
      :PRINT#1,232                              ;;;INX
      :PRINT#1,208                              ;;;BNE .-$B (always loop back...number is never longer than 16 bytes)
      :PRINT#1,245

59160 PRINT#1,169                               ;;;LDA #32   (ASCII blank space)
      :PRINT#1,32
      :GOSUB 59300                              ;;;print accumulator out
      :PC=PC+21                                 ;;;count bytes
      :GOTO 59000                               ;;;and continue with print statement, looping to above

59300 PRINT#1,32                                ;;;JSR $FFD2 prints out accumulator onto screen
      :PRINT#1,210
      :PRINT#1,255

      :RETURN

59400 PRINT#1,169                               ;;;LDA #$D   (<CRLF>)
      :PRINT#1,13
      :GOSUB 59300                              ;;;print it
      :PC=PC+5
      :GOTO 50260                               ;;;back to top of main loop

59500 GOSUB 49100                               ;;;handle 'INPUT' statement
      :IF (CH=0) OR (CH=58) GOTO 50260          ;;;finished when 'end-of-line' or ':'

59540 IF (CH=44) OR (CH=59) GOTO 59500          ;;;keep going if ',' or ';'

59560 GOSUB 49190
      :PRINT#1,169                              ;;;LDA #CH
      :PRINT#1,CH
      :GOSUB 59300                              ;;;print prompting letter on screen before input request.

59580 PRINT#1,169                               ;;;LDA #$3F   (ascii '?')
      :PRINT#1,63
      :GOSUB 59300                              ;;;print it

59600 PRINT#1,162                               ;;;LDX #0   (to initialize counter for input characters)
      :PRINT#1,0
      :PRINT#1,32                               ;;;JSR $FFCF  (inputs, with cursor for user to edit)
      :PRINT#1,207
      :PRINT#1,255

59620 PRINT#1,149                               ;;;STA $A,X   (store input stuff in BASIC input buffer)
      :PRINT#1,10
      :PRINT#1,232                              ;;;INX
      :PRINT#1,201                              ;;;CMP #$D   (check for <CRLF>)
      :PRINT#1,13

59660 PRINT#1,208                               ;;;BNE .-$A   (loop and keep inputting)
      :PRINT#1,246
      :GOSUB 59300                              ;;;echo <CRLF>
```

Listing 1 continued on page 212

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Listing 1 continued:

```
59680 PRINT#1,169                                          ;;;LDA #0
      :PRINT#1,0
      :PRINT#1,133                                         ;;;STA $72
      :PRINT#1,114
      :PRINT#1,169                                         ;;;LDA #$A
      :PRINT#1,10

59700 PRINT#1,133                                          ;;;STA $71  (set up string pointer to beginning of input)
      :PRINT#1,113
      :PRINT#1,202                                         ;;;DEX
      :PRINT#1,138                                         ;;;TXA    (transfer number of characters in string to A)
      :PRINT#1,32                                          ;;;JSR $D68D   (convert string to floating-point in primary accum.)
      :PRINT#1,141

59760 PRINT#1,214
      :PRINT#1,162                                         ;;;LDX #ZL
      :PRINT#1,ZL
      :PRINT#1,160                                         ;;;LDY #ZH   (point to target location to store result)
      :PRINT#1,ZH

59780 PRINT#1,32                                           ;;;JSR $DAA6   (store primary memory contents in target)
      :PRINT#1,166
      :PRINT#1,218
      :PC=PC+45                                            ;;;count bytes (a lot!!)
      :GOTO 59500                                          ;;;and loop

60000 PRINT "FIRST PASS FINISHED!!!"                       ;;;compiling program finished
      :PRINT"PROGRAM OCCUPIES";OC;"THROUGH";PC-1           ;;;print statistics

60020 PRINT"VARIABLES OCCUPY";OV;"THROUGH";OV+129

60060 PRINT#1,-1                                           ;;;mark end of first pass on tape file
      :IF GC=0 GOTO 61000                                  ;;;skip if no jumps to be corrected

60080 FOR X=0 TO GC-1
      :PRINT#1,GO%(X,0)+32767                              ;;;print byte to be fixed
      :L=GO%(X,1)                                          ;;;look up desired line number to branch to
      :Z=LN%(L)+32767                                      ;;;find what the program counter was there

60100 IF Z=0 THEN PRINT "TRANSFER TO NONEXISTENT LINE #";L
      :GOTO 61000                                          ;;;catch errors

60120 ZH=INT(Z/256)
      :ZL=Z-256*ZH
      :PRINT#1,ZL                                          ;;;record correct jump (JMP or JSR) target
      :PRINT#1,ZH
      :NEXT X                                              ;;;for all that need fixing

61000 PRINT#1,-1                                           ;;;mark end of file
      :CLOSE 1                                             ;;;that's all, folks!!!!!
```

Text continued from page 198:

byte value 137, COS is stored as 190, etc. This encoding system saves memory within BASIC programs; when a line is listed to the display, it is decoded so that it can be read in its original form. Encoding also makes the job of the FLOPTRAN compiler easier. Because BASIC encodes reserved words as 1-byte values rather than a sequence of letters, there is, for example, no confusion as to whether the letter G is a variable name or the first letter of a GOTO or GOSUB statement.

Compiler Program Analysis

Because the FLOPTRAN compiler is rather tiny, the language in its present version is a restricted subset of BASIC. The following paragraphs will describe each type of statement that FLOPTRAN understands and explain how it works. The line numbers refer to the statements in the BASIC program of listing 1 that process a given type of statement.

The LET Statement

Lines 58000 thru 58360: To assign a value to a variable during compilation, most BASIC systems allow us to use a statement like:

$$X=1.234E-5$$

In most BASICs, however, it is also legal to say:

$$\text{LET } X=1.234E-5$$

In fact, in the original BASIC language, the use of the word LET was compulsory.

FLOPTRAN demands the presence of the reserved word LET. When the compiler sees LET, it notes the immediately following variable name, which will receive the assigned value on the right side of the equals sign. The compiler then literally copies the right-hand side of the equation into the blank space available in the subroutine

at line 49000, and calls that subroutine to evaluate the expression. Thus, statements such as:

LET P=17*LOG(π/137E8)+ATN(−2)

are perfectly legal ways to initialize a variable, as long as the right-hand side will fit into line 49000.

A LET assignment cannot, however, use variable names in its equation unless those variables have been defined at compilation time; it would *not* be legal to say:

LET A=−44:LET B=A

since A will take on its value of −44 only when the program is executed. (In this case, unless A were defined before running the compiler, B would be assigned the value 0.) The use of variables on the right-hand side of the assignment is covered later, under arithmetic operations.

After evaluating the expression that is to be assigned to some variable, the compiler writes out code (to device 1, the PET's cassette tape drive) which, in 6502 machine language, instructs the microprocessor to skip 5 bytes. Those 5 bytes are filled with the floating-point number to be assigned to the variable; then the compiler executes lines 58300 thru 58360, which takes the stored number and transfers it to the proper target location.

FLOPTRAN allows only single-letter variable names, A thru Z, and reserves storage for each variable, whether it is used or not. This simplifies storage of variables considerably and allows easy and instant access to any variable. The typical BASIC interpreter must scan through a table of variables to find the one it wants to access; the interpreter necessarily wastes a lot of time doing so.

The PRINT Statement

Lines 59000 thru 59400: To get numeric values to the display, statements of the form:

PRINT A

or

PRINT X,Y,Z

are used in FLOPTRAN. When multiple variables are printed by a single statement, they may be separated by either commas or semicolons. In both instances, the numbers that have been requested are translated from floating-point binary radix to ASCII-encoded decimal radix and are printed with a space between them. After the final variable is printed (or if no variables are to be printed) a carriage return and line feed (CR,LF) are printed to the screen.

The PET read-only-memory subroutine at location hexadecimal DCAF does the hard work of converting from binary to ASCII (American Standard Code for Information Interchange) decimal once the value to be converted is placed in the "floating-point accumulator" on memory page 0 (hexadecimal addresses 00B0 thru 00B5); the ASCII string to be displayed is left at the top of page one and ends with a byte of 00. The 6502 code that the compiler generates to take this string and print it out (using the subroutine at hexadecimal address FFD2) is documented in the comments with the FLOPTRAN compiler listing (listing 1).

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The INPUT Statement

Lines 59500 thru 59780: To read in numbers from the keyboard during program execution, statements of the form:

INPUT P

or

INPUT Q;R,S

are used. As with the PRINT statement, either commas or semicolons are valid delimiters to separate several variable names. (In fact, you can leave out the commas or semicolons and FLOPTRAN will not mind; but then BASIC will misunderstand you.)

The compiler generates code that prompts the user by printing out the variable name awaiting input, followed by a question mark. It then accepts input via the standard subroutine (hexadecimal location FFCF) and puts the input string into the BASIC input buffer on page 0. The read-only-memory subroutine at hexadecimal location D68D converts this string to a floating-point number, which is then stored in its proper location.

The IF Statement

Lines 58500 thru 58840: The only allowed forms of IF statement in FLOPTRAN-IV are the simplest ones:

IF W GOTO 252

and

IF J GOSUB 30

These statements test the variable whose name follows the IF; if that variable's value is nonzero, the statement is considered to be true, and the GOTO or GOSUB is executed. If the value of the variable is exactly 0, the statement is false, and the GOTO or GOSUB is skipped. Program execution proceeds with the next *statement*; note that, in the event of multiple statements per line, FLOPTRAN does *not* skip the rest of the line—unlike Microsoft BASIC, which executes the rest of the line only when the IF statement is true. (It is wise, therefore, to avoid using statements following an IF on the same line, to avoid incompatibility with BASIC.)

After testing for zero versus nonzero, this routine can do one of two things: if the expression is true (nonzero), control transfers to the appropriate GOTO or GOSUB routine; otherwise, control transfers to the next statement.

GOTO or GOSUB Statements

Lines 58700 thru 58840: Both of these statements are handled in identical ways; the only difference is whether a 6502 JMP (jump) instruction or a JSR (jump-to-subroutine) instruction is compiled to the tape file. Since the compiler, during its first scan through the FLOPTRAN source program, cannot know the correct absolute address to go to, it temporarily fills the 2 bytes following the JMP or JSR with 0s. It also records, in column 0 of array GO%, the location of those temporary filler 0s, so that the missing addresses can be added later. Since integer arrays use much less space than do floating-

point arrays in PET BASIC, GO% is an integer-type two-dimensional array. Inasmuch as integers must be within the range −32,767 to +32,767, FLOPTRAN subtracts 32,767 from the actual address before storing it and adds the same value when reading the address out (in line 60080).

Column 1 of GO% stores the target line number for the GOTO or GOSUB. After the compilation is finished, the target line numbers will be looked up in table LN% (lines 60000 thru 61000), which contains the actual address of the compiled code corresponding to the desired line number. Then, the address of the first of the pair of bytes to be replaced is written to tape, followed by the 2 correct bytes for the branch. When the contents of the tape are loaded to memory, these bytes have the effect of correctly filling in the previously incomplete addresses in the body of the compiled program.

Because the original PET read-only-memory routines limit arrays to 256 elements, FLOPTRAN-IV is set up to handle programs with line numbers in the range 0 thru 255 only. This restriction, however, can be removed with additional programming if more lines are needed.

The REM Statement

Lines 56500 thru 56540: Remarks, preceded by the reserved word REM, are not compiled; the compiler skips over them to the beginning of the next line of the program, just as is done in interpreted BASIC.

The RETURN Statement

Line 50420: This statement simply causes a 6502 RTS (return-from-subroutine) instruction to be written to tape.

Arithmetic Operations

Arithmetic operations with variables comprise the remainder of the FLOPTRAN-IV compiler's repertoire. Because this is such a tiny compiler, it does *not* handle multiple arithmetic operations per assignment. The program to be compiled, therefore, must have its arithmetic broken up into elementary operations. For example, a statement like:

```
D=(A-B)/LOG(C)
```

must be written out as:

```
D=A-B:E=LOG(C):D=D/E
```

(assuming that E is not being used otherwise).

Because of this restriction on the permissible forms of arithmetic statements, the part of the compiler which handles them is simple and consists only of lines 50440 thru 51120. One special type of equation, which is of the form:

```
V=W
```

is so simple that it is handled separately in lines 55600 thru 55660. The extensive comments included with the listing make this part of the compiler rather straightforward.

This completes our description of the FLOPTRAN-IV compiler program as given in listing 1. The compiler checks for most errors as it works through the source pro-

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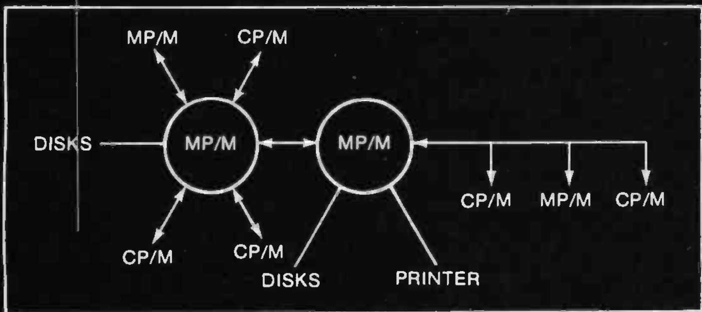

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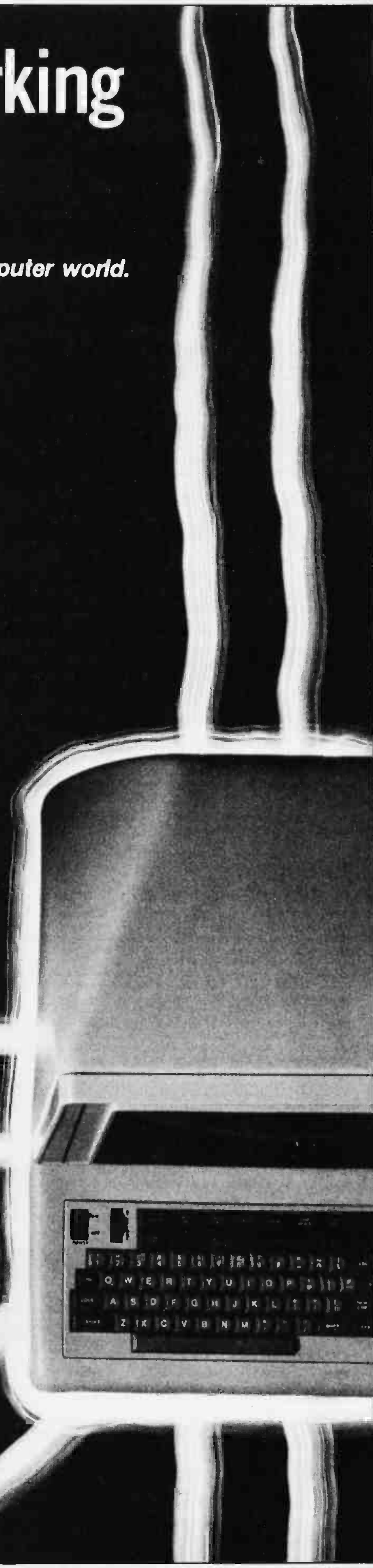

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FLOPTRAN does not allow the appearance of uncompiled constants in an arithmetic statement.

gram; when it finds an unrecognizable statement or a branch to a nonexistent line number, it closes the output file and displays the line number containing the erroneous statement number. This makes one part of the debugging task easy. FLOPTRAN's compatibility with BASIC makes preliminary program testing possible (though perhaps slow) using the PET's BASIC interpreter; this debugging option helps in the discovery and elimination of many other types of errors.

In abbreviated form, table 2 gives a summary of FLOPTRAN-IV syntax. Table 3 presents a very compact summary of the critical read-only-memory subroutine addresses in the original-style PET. (It is probably *too* compact to be useful to a novice user, but for the experienced assembly-language enthusiast, table 3 should make sense and be a valuable guide to the important entry points. The table is entirely in hexadecimal; P refers to the primary floating-point accumulator, where a 6-byte floating-point binary number is stored in hexadecimal locations 00B0 thru 00B5. S refers to the secondary accumulator, located at hexadecimal locations 00B8 thru 00BF; and A, X, and Y are internal registers of the 6502 microprocessor.) It is unnecessary, however, to understand table 3 or, indeed, to understand *anything* about 6502 machine-language programming to successfully use FLOPTRAN-IV. The compiler as given does all the necessary translation.

Sample FLOPTRAN-IV Program

Listing 2 is a sample program written entirely in the FLOPTRAN-IV language. It solves a simple problem from the Parker Brothers game *Risk*: if an attacker rolls three dice and a defender rolls two, what are the odds of each of the possible outcomes? This puzzle was analyzed and discussed in detail recently by Bruce D Barnett (see reference 1). If you don't play *Risk*, however, don't be concerned—the important thing for our purposes here is that this problem provides a good sample task to exercise the capabilities of the FLOPTRAN-IV compiler.

There are a few significant items to note in the FLOPTRAN-IV program of listing 2. First, since FLOPTRAN does not allow the appearance of uncompiled constants in an arithmetic statement, the first statement in line 3 could not be written as "A=A−1". Instead, it was necessary to define a variable name with the letter O (for "One") to be equal to one, as in the assignment "LET O=1" in line 1. Then the arithmetic statement to decrement A can be correctly written as "A=A−O" (line 3).

While the necessity to define constants in arithmetic statements is an occasional inconvenience, it gives the compiler a great speed advantage. In fact, one of the slowest and most wasteful operations in an interpreted BASIC program is the conversion of every written-out ASCII numeric constant into binary each time it is encountered. Because of this, it is a recommended practice in BASIC to define a variable for any constant that is repeatedly used, in order to avoid repeatedly converting the constant from ASCII-encoded decimal to binary. FLOPTRAN forces the user to follow this efficient procedure.

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Statement Type	Description	Examples
LET	initialize a variable during compilation; must be 60 characters or less, cannot use variables	LET A = 1 LET B = EXP(2)/2
PRINT	output a variable's value to screen; gives 1 space between values printed and a "return" at end	PRINT X PRINT P,Q;R PRINT
INPUT	read in a number from keyboard (prompts with variable name)	INPUT Z INPUT J;K,L
IF	conditional branch: the GOTO or GOSUB following will be executed if the variable after the IF is nonzero; skipped otherwise	IF S GOTO 0 IF T GOSUB 255
GOTO	unconditional transfer to line number	GOTO 89
GOSUB	subroutine call; returns to statement following GOSUB when done	GOSUB 176
REM	remarks; skip to next line number	REM THIS IS A TEST
RETURN	return from subroutine, and return to BASIC control at program end	RETURN
arithmetic	perform the specified floating-point arithmetic operation, statements can have only one operation to right of equals sign	C = D E = F + G H = − I J = ATN(K)

Notes:
1. All variables must have single-letter alphabetic names.
2. All lines must be numbered 0 thru 255.
3. Variables must be initialized before use; failure to do this results in a random initial value.

Table 2: *Summary of FLOPTRAN-IV syntax. Due to the nature of the compiler, the LET statement can be an expression of up to sixty characters but can use only arithmetic operators, functions, and constants. The arithmetic statement (which must not use the word LET) can use variables only and can contain, at most, one operator or function.*

A second item to note is the method used (in lines 25, 29, 33, 39, 43, 45, and 51) to compare the relative magnitudes of two variables. In line 25, for example, the real question being asked is: "Is X less than W?" Since FLOPTRAN-IV can only test for zero versus nonzero in its IF statement, the programmer must set up a test variable, Q in this case, that will answer the desired question by being either nonzero for *true* or zero for *false*. For example, after the assignment "Q=X−W" in line 25, the statement "Q=SGN(Q)" returns the value +1 if Q is positive, 0 if Q is zero, and −1 if Q is negative. By adding one in the statement "Q=Q+O", the ultimate result is that Q equals zero if and only if X is less than W. Within the framework of statements 25 and 27, this means that line 27 will be executed only when X is less than W.

Finally, note the "extra" RETURN statement at the end of the program (line 120). In BASIC, this statement is wrong and gives a RETURN WITHOUT GOSUB error message when the interpreter executes it; however, in FLOPTRAN-IV, the RETURN is necessary. It tells the microprocessor that the machine-language routine, which was called by either SYS or USR, is finished and that control now returns to the BASIC operating system. I neglected to include the RETURN in my first compilation of this sample program and was rather embarrassed when, after executing perfectly and printing out the correct answers, the machine "crashed" and had to be reset for further use.

Comparison of FLOPTRAN-IV and PET BASIC

A sophisticated optimizing compiler can usually generate extremely efficient machine-language programs; a common result is a program that runs ten to a hundred times faster than an equivalent interpreted version. FLOPTRAN doesn't do quite that well, although its performance is significantly better than that of PET BASIC in all my tests.

For the *Risk*-odds-calculation program of listing 2, for example, the program took 890 seconds (almost 15 minutes) to reach the answer using the BASIC interpreter. The FLOPTRAN-IV compiled version finished in only 97 seconds, which gives a speed advantage of better than 9 to 1! (Although it is possible that some speed could be gained by rewriting the BASIC program to use FOR-NEXT loops and other structures unavailable in FLOPTRAN-IV, I estimate it would be a small improvement, probably less than a factor of 2.)

The original BASIC program used as the FLOPTRAN source code occupies 627 bytes plus 126 bytes for variables, for a total of 753 bytes. The compiled FLOPTRAN program is bigger, taking 1437 bytes plus its standard 130-byte table of twenty-six variables (not all of which are used in this program), for a total of 1567 bytes. The compilation time for this program is about 4.5 minutes, most of which is spent writing to tape.

Another simple test program, one that doesn't show such a great speed advantage for the FLOPTRAN compiler, is a program to factor a large odd number by trying

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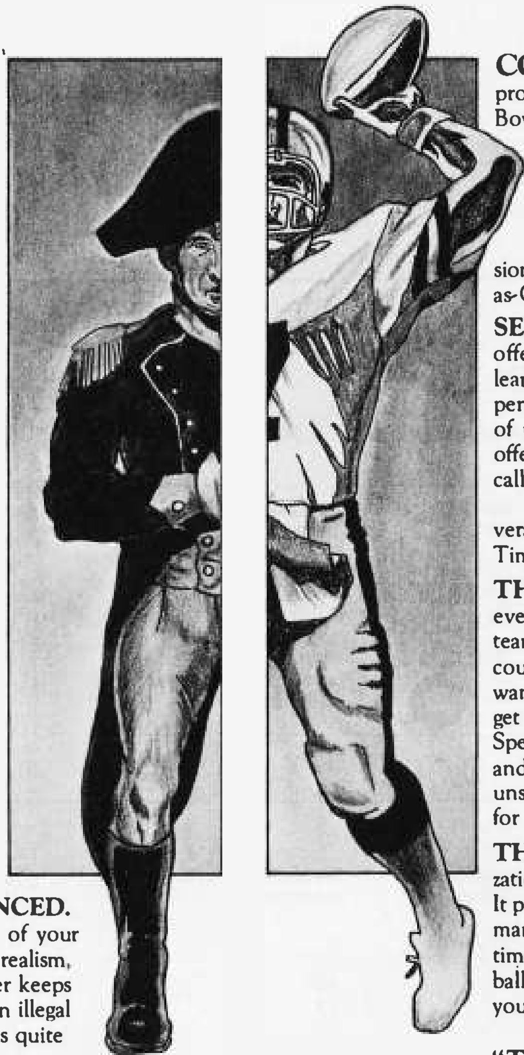

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3a

Hexadecimal Address	Function of Routine	Hexadecimal Address	Function of Routine
0000	USR(P)	D95E	[(A) + 100(Y)]→S, separating sign, set sign comparison, return with (B0) in A
CED6	S OR P		
CED9	S AND P	D9E4*	S / P
D264	FRE(P)	DA74	[(A) + 100(Y)]→P, separating sign
D285	POS(P)	DAA6	roundoff(P)→[(X) + 100(Y)], merging sign
D349	STR$	DACE	S→P
D5C4	CHR$	DADE	P→S, with rounding
D5D8	LEFT$	DAE1	P→S, without rounding
D604	RIGHT$	DAED	roundoff(P)
D60F	MID$	DAFD	SGN(P)→A
D654	LEN	DB0B	SGN(P)
D663	ASC	DB2A	ABS(P)
D685	VAL	DB9E	INT(P)
D6E6	PEEK	DE24	SQR(P)
D728*	S − P	DE2E*	S ↑ P
D73C	JSR D95E, then S + P	DEA0	EXP(P)
D73F*	S + P	DF45	RND(P)
D7AC	normalize P	DF9E	COS(P)
D8BF	LOG(P)	DFA5	SIN(P)
D8FD	JSR D95E, then S * P	DFEE	TAN(P)
D900*	S * P	E048	ATN(P)

3b

Hexadecimal Address		Contents	Examples: Hexadecimal Values of Bytes for	
S pseudoregister	P pseudoregister		S = e = 2.71828...	P = π/2
B8	B0	exponent + 80	82	81
B9	B1	fraction, most significant byte	AD	C9
BA	B2	fraction, byte 2	F8	0F
BB	B3	fraction, byte 3	54	DA
BC	B4	fraction, least significant byte	59	A2
BD	B5	sign	00	FF
BE	—	sign comparison	FF	—
BF	—	roundoff byte	00	—

3c

Hexadecimal Address	Value stored in floating (merged sign) notation
CDBC	π
DDE3	1/2
E01A	π/2
E01F	2π
E024	1/4

Table 3: *Overview of useful addresses and constants used by the original-version PET. Table 3a is a list of entry points to subroutines within the PET's read-only-memory firmware. Table 3b explains the makeup of the two floating-point pseudoregisters P and S. Table 3c gives the locations of five constants stored in the read-only-memory area of the PET. In table 3a, the routines marked with an asterisk (ie: all arithmetic operations) must be set up before execution as follows: hexadecimal location 00BE must contain the exclusive-OR of the contents of hexadecimal locations 00B5 and 00BD. Also, the contents of hexadecimal location 00B0 must be placed in the 6502 accumulator.*

all odd numbers as potential divisors, from 3 up to the square root of the number. The compiled FLOPTRAN code takes 60 seconds to factor the number 567,890,123; the same program run in PET BASIC requires 201 seconds, a speed advantage of better than 3 to 1 for the FLOPTRAN compiler. But, after the BASIC program has been rewritten for speed, the revised program executes in 101 seconds, giving a speed advantage of 1.7 to 1 for compiled FLOPTRAN.

One of the reasons that the BASIC interpreter does not have much of a disadvantage in this factorization problem is that the BASIC program needs to use only a few variables, so that little time is wasted scanning through a variable table. Also, this program performs very little decimal-to-binary conversion and a small amount of branching from one line number to another (which requires more BASIC scanning to find the target line). These three factors contribute to this problem's lower

Listing 2: *Sample FLOPTRAN-IV program. This program calculates the possible outcomes of a dice roll in the game* Risk, *with the attacker rolling three dice and the defender rolling two dice. See text for details.*

```
LIST -120

  1 LET F=0
   :LET G=0
   :LET H=0
   :LET J=0
   :LET A=7
   :LET B=6
   :LET C=6
   :LET O=1

  3 A=A-O
   :IF A GOTO 9

  4 GOTO 100

  5 LET B=6

  7 LET A=6

  9 LET D=7
   :LET E=6

 11 D=D-O
   :IF D GOTO 21

 13 E=E-O
   :IF E GOTO 17

 15 GOTO 3

 17 LET D=6

 21 I=I+O

 23 V=A
   :W=B
   :X=C
   :Y=D
   :Z=E

 25 Q=X-W
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 29

 27 T=X
   :X=W
   :W=T

 29 Q=W-V
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 39

 31 T=W
   :W=V
   :V=T

 33 Q=X-W
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 39

 35 T=X
   :X=W
   :W=T

 39 Q=Z-Y
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 43

 41 T=Z
   :Z=Y
   :Y=T

 43 Q=Z-X
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 51

 45 Q=V-W
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 53

 47 GOTO 61

 51 Q=Y-W
   :Q=SGN(Q)
   :Q=Q+O
   :IF Q GOTO 71

 53 G=G+O
   :GOTO 11

 61 F=F+O
   :GOTO 11

 71 H=H+O
   :GOTO 11

100 B=B-O
   :IF B GOTO 7

110 C=C-O
   :IF C GOTO 5

120 PRINT F,G,H
   :F=F/I
   :G=G/I
   :H=H/I
   :PRINT F,G,H
   :RETURN
```

Notes on CHEEP PRINT

CHEEP PRINT is a software/hardware combination invented by Charles A McCarthy (1359 W Idaho Ave, St Paul MN 55708) to print the listings given in this article; it allows a user with a printer and modem to interface the two to a personal computer. Functionally, CHEEP PRINT produces a rapid sequence of 2025 and 2225 Hz tones (via a short machine-language program) that are converted into RS-232C ASCII character data by a standard Bell-103a-type modem. When storing programs, a simple low-pass filter is inserted between the computer and the cassette recorder to smooth the output waveform for the cassette recorder. A BASIC driver program formats the program listing and passes characters, one at a time, to the machine-language subroutine that generates the tones.

In this implementation, a Commodore PET microcomputer and a Teletype Model 43 are used. The machine-language subroutine for the PET is shortened by the use of the internal clock and programmable shift register of a 6522 VIA (Versatile Interface Adapter) chip within the PET; these are used to generate the required square-wave tones, which are made available on the CB2 pin of the PET's user port.

execution time. On the other hand, the *Risk* program uses many variables and branches, giving the FLOPTRAN compiled program more of an edge there.

Final Remarks

When the FLOPTRAN-IV compiler program is run, the result is a set of numbers that have been written to the PET's cassette tape drive. This tape, which contains the location and contents of the machine-language program that is the compiled equivalent of the given FLOPTRAN-IV source program, must be loaded into memory before the compiled program can be run. This is done by running the FLOPTRAN-IV loader program in listing 3.

This short BASIC program reads in the starting address for the compiled code (in the variable PC, which serves as a program counter), POKEs the following numbers into consecutive memory locations until it encounters a −1 end-of-program marker (written to the tape by line 60060 of listing 1), then reads in the addresses and correction-bytes to put into those GOTO and GOSUB instructions that need them. A final −1, written to tape by line 61000 of listing 1, ends the loading process.

The loader program prints out the starting and ending addresses of the compiled code so that the user can check that no data blocks were dropped by the PET's tape recorder. I did not include a subroutine in the FLOPTRAN compiler to force the PET's tape-recorder motor to leave extra gaps between data blocks (if necessary, this can be done with a POKE 59411,53 instruction). Instead, I have added a 5000 to 10,000 μF capacitor which is connected across the motor terminals during recording; this automatically causes the recorder to leave enough space. The discharging capacitor makes the motor run on for some time after it would normally stop. If your machine needs longer gaps, you may add the above POKE statement, perhaps between lines 49100 and 49120 (this is within the frequently called subroutine which fetches the next nonblank character).

By choosing the starting address for the compiled program appropriately, you can load the compiled program into memory and then load a monitor program that will allow you to save the compiled code as a binary machine-language file. Generally these binary files are much more reliable than ASCII data files, and of course, they load much faster.

You can also locate a compiled program in the video-display area of memory, locations decimal 32,768 thru 33,791, provided that the program is small enough to fit. Running such a program gives very interesting visual effects.

Listing 3: *FLOPTRAN-IV loader program. This program is executed to transfer the compiled FLOPTRAN-IV program from the PET cassette tape drive into memory. See the "How to Use the FLOPTRAN-IV Compiler" text box for details.*

```
10 OPEN 1: INPUT #1, PC: PRINT "BEGIN AT"; PC
20 INPUT #1, A: IF A = >0 THEN POKE PC,A:
      PC = PC + 1: GOTO 20
30 PRINT "END AT"; PC - 1
40 INPUT #1, PC: IF PC < 0 THEN CLOSE 1: END
50 INPUT #1,A: POKE PC,A: INPUT #1,A:
      POKE PC + 1,A: GOTO 40
```

What other logical improvements can be made to make FLOPTRAN faster and more useful? String-handling capabilities sometimes come in handy; it would not be hard to allow the compiled program to recognize string variables and print them when requested, though I'm not sure how you would go about manipulating strings.

Perhaps the compiler should not allocate a fixed amount of space to a table of only twenty-six variables; instead, it might define variables when needed by the program. Arrays of variables, which are also valuable to have, should not be hard to implement.

FLOPTRAN suffers from the simplicity of its conditional-branching structure; an IF statement that could test for conditions other than zero/nonzero would be a profitable addition. It also would be good to have a looping structure available, similar to BASIC's FOR...NEXT, or perhaps like FORTRAN's DO-loop. Even a simple decrement-and-skip-on-zero calculator-type instruction would save time and space in many programming situations. Simple integer variables and integer arithmetic might also be worth having for many tasks.

I've resisted pursuing some of the above modifications to FLOPTRAN-IV in order to retain the language's compatibility with BASIC; perhaps that compatibility should be given up in exchange for more power and efficiency.

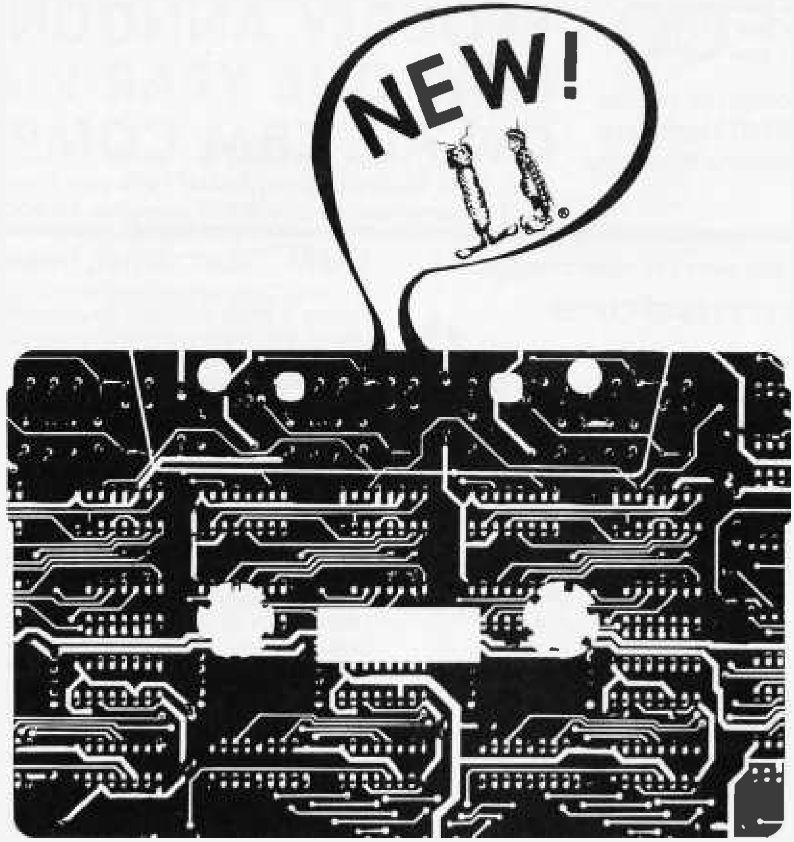
I would be interested to hear from readers who have used or improved upon FLOPTRAN or who have adapted it to other machines. The idea of a tiny compiler that uses an existing BASIC interpreter (especially one that permanently resides in read-only memory) is a simple idea, but I haven't seen it discussed in print. It is possible that if a manufacturer were to have a few hundred to a couple of thousand bytes of read-only memory available beyond the BASIC interpreter, he could put a better version of a FLOPTRAN-like compiler in that space so that it would always be available. Interpreted BASIC is wonderful, but there are some programming jobs that need more speed and efficiency — jobs only a compiled language can fill. ■

Reference

Barnett, Bruce D, "How to Program a Complex Problem," *Personal Computing*, September 1979, pages 26 to 30.

Acknowledgments

I would like to thank Jim Butterfield and Charles A McCarthy for helpful ideas and programming tools, without which FLOPTRAN would have taken far longer to develop.



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Symbolic Math Using BASIC

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The Soft Warehouse
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This article describes a simple BASIC program that expands polynomials. For example, when given an expression such as:

$$(5x+7)\ (2x+3)^3$$

the program produces as output the corresponding fully expanded polynomial:

$$40x^4+236x^3+522x^2+513x+189$$

Written in ANSI (American National Standards Institute) minimal BASIC, this program requires only a single small one-dimensional numeric array, integer arithmetic, and room for 110 simple BASIC statements. In fact, the program can be adapted to the HP-41C and TI-59 programmable pocket calculators.

Symbolic-mathematics systems have long been available for large computers. The muMATH-79 software developed by The Soft Warehouse and distributed by Microsoft, 10800 NE 8th, Suite 819, Bellevue WA, 98004, brought sophisticated symbolic math to microcomputers based on the Intel 8080, 8085 and Zilog *Z80* microprocessors. However, symbolic-math systems are currently unavailable for microcomputers and minicomputers based on other processors, and many 8080-, 8085-, or Z80-based installations lack the requisite minimum of 32 K bytes of programmable memory, a floppy-disk drive, and the TRSDOS, CP/M, CDOS, or IMDOS operating system currently necessary to run muMATH. Consequently, to make some symbolic math available on those computers for which a full-fledged system is not yet available, this article presents a compact polynomial expansion program written in BASIC. Though nowhere near as flexible, general, or robust as muMATH, this program is useful, nonetheless, and it provides an educational exposure to the idea of computer symbolic math.

Program Outline

Many BASIC programs include mathematical expressions intended for numerical evaluation, but for a symbolic-math program we also want the ability to input and print *data* consisting of mathematical expressions. One way to accomplish this is to input and print expressions as character strings. For example, letting the variable named A$ store a string representing an unexpanded expression and letting the variable named B$ store the corresponding expanded polynomial derived by the program, a symbolic-math program could have the following outline:

```
100   INPUT A$
...     derive B$ from A$
900     PRINT B$
910   GO TO 100
920   END
```

The interactive input would be a sequence of string expressions (written in BASIC style) such as:

```
X * (2*X + 1) ↑ 2
```

The program could use substring extraction to dismantle A$ for analysis, while using insertion or catenation to construct the corresponding B$. Equivalently, A$ and B$ could be arrays of one-character strings, using subscripts to dismantle the input and assemble the output.

However, many of the most prevalent small BASIC implementations do not provide substring extraction, insertion, catenation, or arrays of characters. For example, TRS-80 Level I BASIC lacks these facilities.

About the Author,

David Stoutemyer, a partner of The Soft Warehouse, is a professor of electrical engineering at the University of Hawaii. The author of over twenty technical articles, he received bachelor's and master's degrees in engineering from the California Institute of Technology and MIT, followed by a doctorate in computer science from Stanford.

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x	$y=(2x-1)(x+1)^2$
-2	$(-4-1)(-2+1)^2 = -5$
-1	$(-2-1)(-1+1)^2 = 0$
0	$(0-1)(0+1)^2 = -1$
1	$(2-1)(1+1)^2 = 4$
2	$(4-1)(2+1)^2 = 27$

Table 1: *Sample evaluations of a factored polynomial. As part of the expansion process of the factored equation $y=(2x-1)\ (x+1)^2$, the right-hand side is evaluated for each of five sampled values of x. These results are used in table 2.*

K	x_k	y_k	Values of d			
1	-2	-5				
2	-1	0	5			
3	0	-1	-1	-6		
4	1	4	5	6	12	
5	2	27	23	18	12	0

Table 2: *Difference table of evaluated polynomial. In this example, the right-hand side of $y=(2x-1)\ (x+1)^2$ is evaluated at each of five points x_k, giving the resulting y_k values. A given number in the d section is calculated as the difference of the number to the immediate left of the given number and the number immediately above the given number; for example, the number 23 equals 27 minus 4. For each row, d_1 is the rightmost number in the d section, d_2 is the number (if any) to its left, and so on.*

This interpolation algorithm allows us to determine the coefficients for the expanded polynomial.

Actually, insertion or catenation is not really necessary. As they are derived, we can print the pieces that would otherwise successively be catenated onto the right side of B$, using semicolons to suppress line feeds and carriage returns between these pieces.

The need for substring extraction or an array of characters cannot be eliminated as conveniently for expression input. However, the program in this article uses an indirect *evaluation-interpolation* technique to circumvent the need for string variables. This makes the program suitable for virtually every version of BASIC. The technique is applicable to more general expressions, but to keep the program small and educational, let us consider only polynomials in a variable named x of a degree less than some specified positive integer constant, n.

Given a set of n distinct values of x, together with the corresponding values of a function $y(x)$:

$$(x_1, y_1), (x_2, y_2), \ldots, (x_n, y_n),$$

there is a unique polynomial of a degree less than n that passes through these points:

$$p = a_m x^{m-1} + a_{m-1} x^{m-2} + \ldots + a_2 x + a_1, \text{ with } m \leq n$$

Moreover, there is a relatively simple and fast algorithm for determining m and the coefficients of the expanded form, $a_1, a_2, \ldots, a_m$, from the pairs (x_1, y_1), (x_2, y_2), ... (x_n, y_n). Thus, no matter how $y(x)$ is written, if $y(x)$ is equivalent to a polynomial of a degree less than n, then evaluation of the expression at n points followed by application of this interpolation algorithm allows us to determine the coefficients for the expanded form of this polynomial.

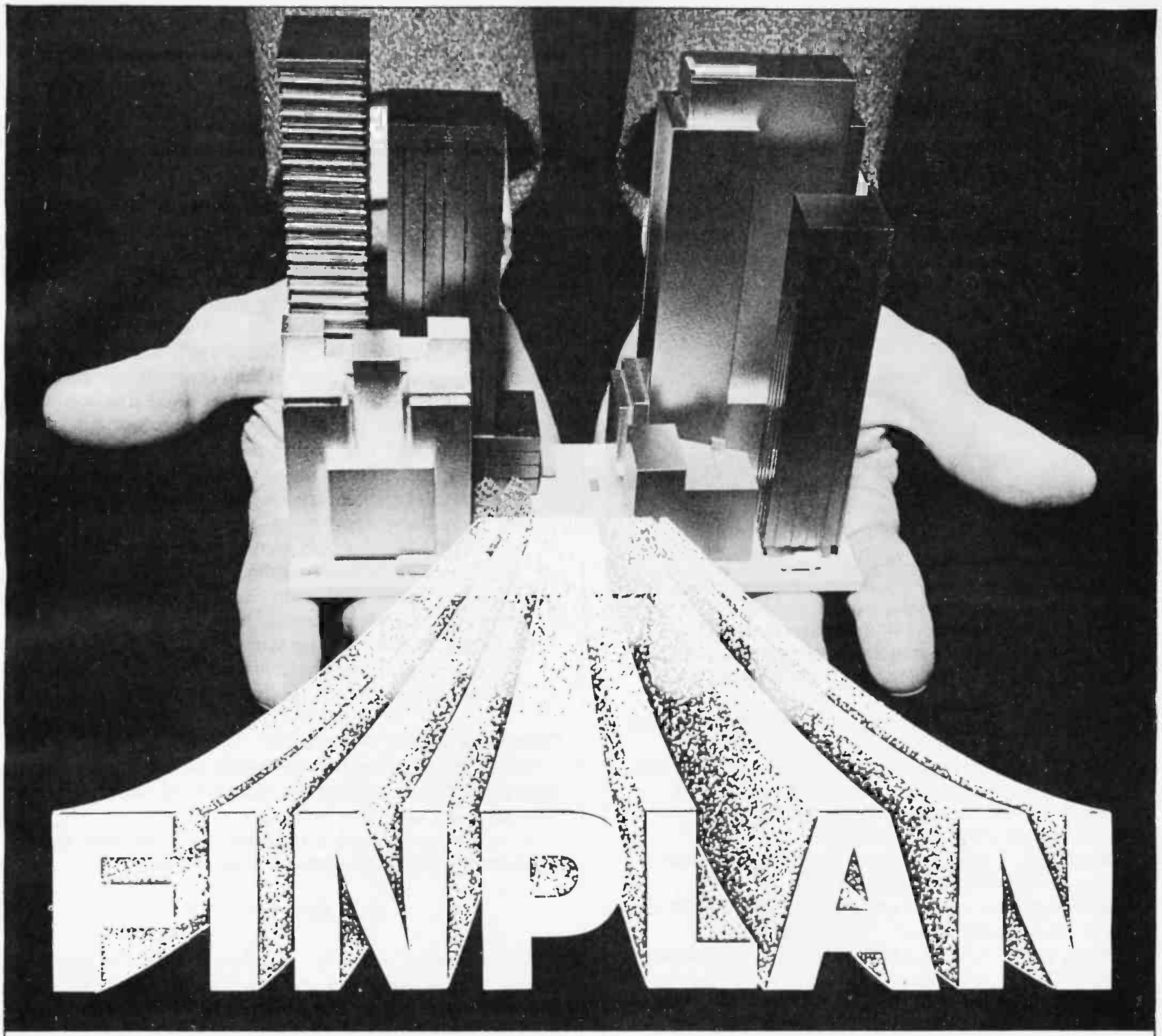
For example, suppose we specify $n=5$ and $y=(2x-1)$ $(x+1)^2$. We are free to choose any distinct values of x. Let us make them small-magnitude integers centered around zero, in order to simplify calculating the corresponding values of y. The results of these calculations are given in table 1.

The interpolation algorithm determines that the unique polynomial of a degree less than 5 applied to these five pairs is described as:

$$p = 2x^3 + 3x^2 - 1.$$

Since y is also a polynomial of a degree less than 5, p and y must be different forms of the same polynomial. Note that:

- We never formally expanded the expression for y. Although such an expansion is trivial for this example, manual expansion is increasingly laborious and fraught with opportunities for blunders with increasing degree and size of coefficients.
- The algorithm works even when n exceeds the degree



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The algorithm is adapted so that only integer arithmetic is involved.

of the result by more than 1, albeit at the expense of computing space and time. The space requirements grow only linearly with n, and the time requirements grow quadratically with n, so even the slowest BASIC interpreters on the slowest microcomputers can generally treat values of n of at least 10 in a few seconds. As will be demonstrated, a more serious consequence of having n much larger than necessary is the possibility of overflow or excessive roundoff error due to the limited range and precision of typical BASIC integer or floating-point arithmetic. A simple strategy for minimizing such evils is to choose successive integers centered around zero for x values, as we have done.

- When $y(x)$ is not a polynomial of a degree less than n, then p is merely a polynomial *approximation* of $y(x)$. However, even such approximations are often of interest. Moreover, it should usually be clear to a user whether or not an expression can be expanded into a polynomial. If so, there is also usually an obvious reasonable bound on its degree to use for n.

Overview of the Algorithm

Before proceeding to the details of the interpolation algorithm, let us outline the program to summarize the discussion so far. (See listing 1.)

In order to expand an expression, the user merely replaces the line in the program containing:

$$y = (2x-1)(x+1)^2$$

with the desired example. The line setting n in step 1 of listing 1 may also require adjustment. Then the user simply types the BASIC command RUN. To expand a sequence of polynomials, the user repeatedly modifies these one or two lines of the program between runs.

This technique is not as interactive as our original string-based outline because the unexpanded expression must occur as a line of the program rather than as a response to an INPUT request. The line containing the unexpanded expression could be made into a subroutine to divorce it from the rest of the program, but the line would still be part of the program rather than data. Nevertheless, given the semi-interactive nature of BASIC interpreters, and the fact that only one or two lines need to be changed between runs, the interpolation technique is tolerably interactive.

Interpolation Details

The interpolation step is relatively simple in comparison with most scientific computations, but those who are intimidated by detail may prefer to postpone reading this section until after reading the subsequent ones and trying the program. The program can be typed in and used without understanding how it works.

First, we construct a *difference table* for the values of y. (See table 2.)

In table 2, k represents the consecutive integers 1 thru

Text continued on page 242

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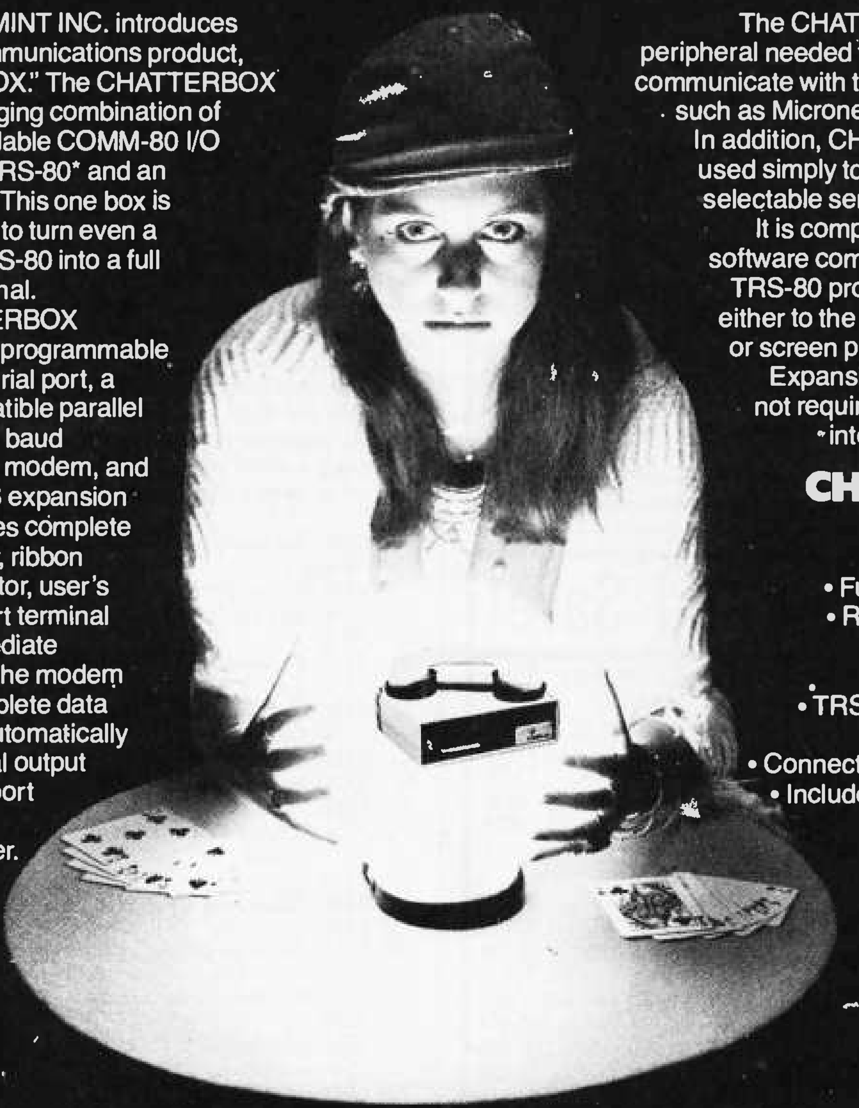

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Listing 1: *Outline of an evaluation-interpolation algorithm for expanding a factored polynomial.*

1. Set n to a sufficiently large but not extravagant positive integer.
2. Initialize x to − INT(n/2).
3. For k = 1 to n
   Evaluate y from an unexpanded formula such as
   $y = (2x-1)(x+1)^2$
   Increment x by 1
   Next k.
4. Construct the coefficients of the interpolated polynomial having degree less than n.
5. Print the polynomial in algebraic form.
6. End program.

Listing 2: *Algorithm for computing the coefficients of an expanded polynomial, given its forward differences.*

```
for k = 1 to m − 1
    for j = m − 1 to k step − 1
        d_j = d_j − d_(j+1) x_(j−k+1)
    next j
next k
```

Listing 3: *Listing for polynomial-expansion routine. Many of the most prevalent versions of BASIC are incompatible with even ANSI minimal BASIC, so minor changes may be necessary to run this program on some installations. However, this program uses such elementary features that any necessary changes will almost certainly be merely syntactic. For example, the DIM statement and the word THEN in IF statements must be deleted for TRS-80 Level I BASIC. The program can even be adapted to a BASIC that supports no arrays by expanding the loops for a particular N, using M = N, and using a scalar named A1 for A(1), A2 for A(2), etc, or using any other unemployed names.*

```
10  REM, Simple polynomial expansion program.
20  REM,
30  REM, Copyright © 1980 by The Soft Warehouse,
40  REM, Box 11174, Honolulu, Hawaii 96828.
50  REM,
60  REM, Permission hereby granted to freely modify, duplicate,
         and
70  REM, use, provided all remarks with leading commas are re-
         tained,
80  REM, and provided all deletions, insertions and modifications
90  REM, are indicated by remarks without leading commas.
100 REM,
110 REM, Write for info about more powerful symbolic math pro-
         grams.
120 REM,
130 REM, Reference, BYTE magazine, October 1980.
140 REM,
150 REM, To use, replace the right side of the assignment
160 REM, "LET Y = ..." near the beginning of the program with
170 REM, the desired unexpanded polynomial in X, then RUN.
180 REM,
190 REM, Declare X, Y, C, and array A to be maximum allowable
         precision.
200 REM,
210 REM, Set N to 1 more than maximum allowable degree of
         result:
220 REM, (increase if insufficient; decrease if overflow, excessive
230 REM, roundoff, or excessive time). N must be at least 2.
240 REM,
250 REM, --------------------------------------------------------
260      LET N = 5
270 REM, --------------------------------------------------------
280 REM,
290 REM, Dimension array A to have at least N elements:
300 REM,
310      DIM A(15)
320 REM,
330 REM, Sample polynomial at N points:
```

Listing 3 continued on page 240

Listing 3 continued:

```
340 REM,
350     LET L = -INT(N/2)
360     LET X = L
370     FOR K=1 TO N
380 REM, ***********************************************
390       LET Y = (2*X - 1) * (X + 1) ↑ 2
400 REM, ***********************************************
410       LET A(K) = Y
420       LET X = X+1
430     NEXT K
440 REM,
450 REM, Compute forward differences:
460 REM,
470     LET M =1
480     FOR K=2 TO N
490       FOR J=N TO K STEP -1
500         LET A(J) = A(J) -A(J-1)
510       NEXT J
520       IF A(K)=0 THEN 540
530       LET M = K
540       NEXT K
550 REM,
560 REM, Scale coefficients:
570 REM,
580     LET C = 1
590     FOR K = M-1 TO 1 STEP -1
600       LET C = C*K
610       LET A(K) = C*A(K)
620     NEXT K
630 REM,
640 REM, Compute coefficients of expanded polynomial:
650 REM,
660     LET U = L+M-1
670     FOR K=1 TO M-1
680       LET U = U-1
690       LET X = U
700       FOR J = M-1 TO K STEP -1
710         LET A(J) = A(J) - X*A(J+1)
720         LET X = X-1
730       NEXT J
740       LET A(K) = A(K)/C
750     NEXT K
760     LET A(M) = A(M)/C
770 REM,
780 REM, Print polynomial:
790 REM,
800     LET Z = 1
810     IF M=1 THEN 1040
820     FOR K=M TO 2 STEP -1
830       IF A(K)=0 THEN 1000
840       IF Z=0 THEN 920
850       IF A(K)< > -1 THEN 870
860       PRINT "-";
870       IF ABS (A(K))=1 THEN 960
880       GOTO 940
890       PRINT " - ";
900       A(K) = -A(K)
910       GOTO 940
920       IF A(K)<0 THEN 890
930       PRINT " + ";
940       IF A(K)=1 THEN 960
950       PRINT A(K); "*";
960       PRINT " X ";
970       IF K=2 THEN 990
980       PRINT " ↑ "; K-1;
990       Z=0
1000    NEXT K
1010    IF A(1)<0 THEN 1070
1020    IF A(1)=0 THEN 1050
1030    PRINT " + ";
1040    PRINT A(K);
1050    PRINT
1060    STOP
1070    PRINT " - ";
1080    A(1) = -A(1)
1090    GOTO 1040
1100    END
```


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PAY 4 - reports all outstanding Accounts Payables for a single customer or for all customers, and computes Cash Requirements.
PAY 5 - reports all outstanding Accounts Payables for a single date or for a range of dates and computes the Cash Requirements.
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REC 4 - reports all outstanding Accounts Receivables for a single customer, or for all customers and computes Cash Projections.
REC 5 - produces reports for all outstanding Accounts Receivables for a single date or for a range of dates and computes Cash projections.
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Text continued from page 236:
n. Each entry in the four d columns is equal to the entry to its left minus the one above that. If we designate the rightmost entry in each row by d_1, d_2, ..., d_n, beginning with $d_1 = y_2 - y_1$, then the interpolated polynomial can be expressed as:

$$d_1 + \frac{d_2(x-x_1)}{1} + \frac{d_3(x-x_1)(x-x_2)}{1\times 2}$$
$$+ \ldots + \frac{d_n(x-x_1)(x-x_2)\ldots(x-x_{n-1})}{1\times 2\times 3\times \ldots \times n}$$

Thus, for our example,

$$p = -5 + 5(x+2) - \frac{6(x+2)(x+1)}{2}$$
$$+ \frac{12(x+2)(x+1)x}{6} + \frac{0(x+2)(x+1)x(x-1)}{24}$$

Note that, since we are only interested in the rightmost element in each row, we can avoid wasting space on a two-dimensional array by letting d_k generally represent the current rightmost computer entry in row k, provided we compute the entries one column at a time, from the bottom up. (See listing 3, lines 450 thru 550.)

The above so-called *Newton-forward-difference* form of the interpolated polynomial is fine for numerical evaluation of p for any specific value of x, which is the usual purpose of interpolation. However, we seek the coefficients of the fully-expanded form, so a further processing phase is necessary.

Using appropriate multipliers to avoid divisions and possible fractions at this point (see listing 3, lines 560 thru 630), we then apply the algorithm given in listing 2. (See listing 3, lines 640 thru 770.) This gives us the desired expanded polynomial coefficients, which can be expressed by:

$$a_k = \frac{d_k}{(m-1)!}, \quad \text{for } k = 1, 2, \ldots, m.$$

As a practical matter, we can use the same array to store y_k, d_k and a_k for $k = 1$ to n.

Most numerical-analysis texts outline the theory behind the Newton-forward-difference formula. *Elementary Numerical Analysis*, by Conte and de Boor (McGraw-Hill, 1972), is one of the few texts that also presents an algorithm for transforming the polynomial to its fully expanded form. The above algorithm is adapted from theirs so that only integer arithmetic is involved if the coefficients of the original unexpanded polynomial are all integers. This permits the program to work even on integer-arithmetic versions of BASIC. Moreover, it often reduces or eliminates round-off error on BASIC implementations that use floating-point arithmetic.

Limitations

The finite-precision arithmetic of most BASIC implementations imposes some important limitations on this program. For example, on a version of BASIC offering about eight decimal digits of precision, using $n=10$,

$$(2x + 6)^8$$

yields the exact result:

$$256x^8 + 6144x^7 + 64512x^6 + 387072x^5 + 1451520x^4$$
$$+ 3483648x^3 + 5225472x^2 + 4478976x + 1679616$$

but both of the "slightly larger" polynomials $(3x + 6)^8$ and $(2x + 6)^9$ yield expanded results having absolute coefficient errors as large as 22. The sample values of x are all exactly representable integers of small magnitude, and the same is true of the unexpanded coefficients for these examples.

The problem is that the sample values of y, their differences, the product of these differences with the appropriate multipliers, and the final expanded coefficients can be too large to be exactly representable. Moreover, relatively small, consequent roundoff errors committed at intermediate stages can easily propagate into relatively large roundoff errors only one step later.

Unexpanded expressions having fractional coefficients are liable to behave worse in this regard, particularly if any of the fractions are not exactly representable in the number base employed by the interpreter. For example, expanding the expression:

$$(x + 1/3)^2$$

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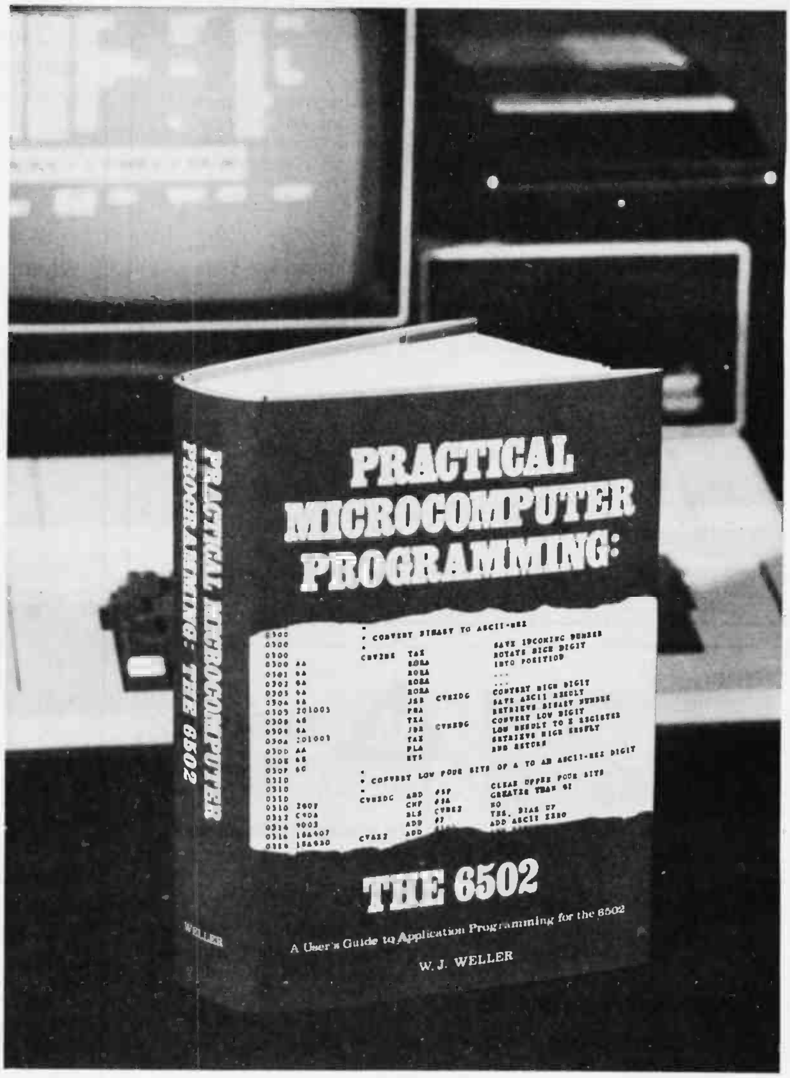

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when $n = 5$, on a binary implementation of BASIC having about eight decimal digits of accuracy, gives us:

$$2.48353\times10^{-9}x^4 + 4.96705\times10^{-9}x^3 + x^2 + 0.666667x + 0.111111$$

Although their coefficients are admittedly small, the appearance of apparent terms where none should occur is somehow far more annoying than a modest, relative error in the coefficient of a truly nonzero term.

Unexpanded coefficients that are fractions exactly representable in the underlying number base are less likely to wreak havoc. For example:

$$(x + 1/2)^2$$

yields

$$x^2 + x + 0.25$$

when $n = 5$, on the same version of BASIC. These difficulties can be minimized by:

- declaring the relevant program variables to have the maximum allowable precision offered by the BASIC being used;
- avoiding setting n much larger than necessary;
- phrasing problems to have small magnitude, integer coefficients insofar as possible (For example, perhaps a common denominator can be removed along with a common divisor of the resulting coefficients);
- phrasing the problem to have the smallest possible degree (For example, perhaps there is an obvious common factor x^3, which can be removed, or perhaps the polynomial can be regarded as a polynomial in x^2).

However, even practicing all of these frugalities, the limitations are substantial. For example, it is optimistic to set n larger than a value found by dividing the underlying number of significant digits in the arithmetic by the largest number of digits in any coefficient of the unexpanded expression. Thus, the program is usable only for relatively modest problems on a typical seven-digit BASIC, and the program is primarily an educational curiosity on a typical four-digit integer BASIC.

It gives one pause to realize that even traditional applications of floating-point arithmetic can entail similar sensitivity to roundoff error and, worse yet, it is more likely to go unnoticed. Indefinite-precision arithmetic, such as that provided by muMATH, overcomes this limitation. However, most symbolic-math systems, including muMATH, are based entirely or predominantly upon techniques other than evaluation and interpolation.

PICOMATH-80

After writing this article and the simple polynomial expansion program given in listing 3, I decided to determine how much further the evaluation-interpolation technique could be explored within the confines of a 4 K BASIC program. The results were:

- It was trivial to extend the polynomial-expansion program to also optionally perform symbolic differentiation or integration. It was also possible to

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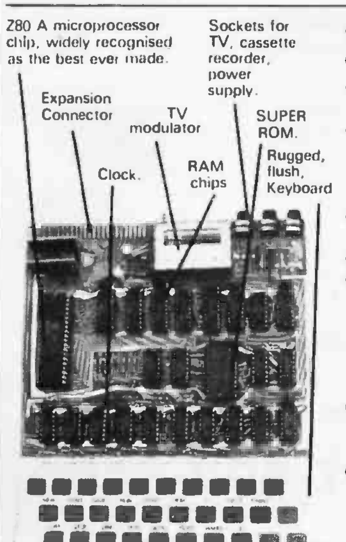

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City ____________ State ____________ Zip ____________ extend the program to work with three variables.

- Some less trivial techniques reduced the sensitivity to roundoff error somewhat.
- Rational interpolation yields an analogous program that simplifies single-variable rational expressions over a common denominator, reduced to lowest terms. For example:

$$1 + \frac{1}{x-1} - \frac{1}{x+1} + \frac{2x}{x^2-1}$$

simplifies to

$$\frac{x+1}{x-1}$$

Although rational interpolation expands polynomials as a special case, polynomial interpolation is generally more accurate when applicable.

- Two trigonometric interpolation formulas yield a pair of analogous programs that perform many trigonometric simplifications. For example:

$$\frac{\sec x - \tan x - 1}{\tan x + \sec x - 1}$$

can be transformed into the equivalent

$$\tan x$$

and

$$\sin(3x) + 4\cos(x-\pi/2) - 4\sin x \cos^2 x$$

simplifies to:

$$3 \sin x$$

These programs are useful for Fourier analysis and proof of trigonometric identities. Here too it was trivial to optionally perform symbolic differentiation or integration.

Although limited by the underlying finite-precision arithmetic of BASIC, the similar but independent polynomial, rational, and trigonometric programs collectively span a large enough sample of problem classes to constitute a demonstration symbolic-math package. Accordingly, we have collected them together for distribution under the name PICOMATH-80. By the time this article appears, PICOMATH on tape cassettes with documentation should be available for at least the Apple, Atari 800, Exidy Sorcerer, Commodore PET, Texas Instruments 99/4, and Radio Shack TRS-80 Level II computers at most computer stores or from Programma International, 3400 Wilshire Blvd, Los Angeles CA 90010, for $19.95. The sixty-page manual contains usage directions, explanations of how the programs work, BASIC program listings, and an adaptation guide for various dialects of BASIC or other programming languages. The manual is available separately for $15.95 from Programma International. Thus, PICOMATH is easily installed on virtually any computer.

Conclusion

I still recall my disappointment when I first realized that the first programming language I learned, FORTRAN, was essentially arithmetic. The same was true of my second and third programming languages, so the first exposure to a symbolic-mathematics system was a delightful surprise. Though much of the world's scientific computation is (and probably always will be) numerical, it seems likely that many of those who experience symbolic mathematics will want their programming languages to fully support both types of computation. Therefore, beware of trying the symbolic-math program in listing 3. Though it is almost certainly the most trivial and least powerful program of its type, symbolic computer math can be addictive! ■

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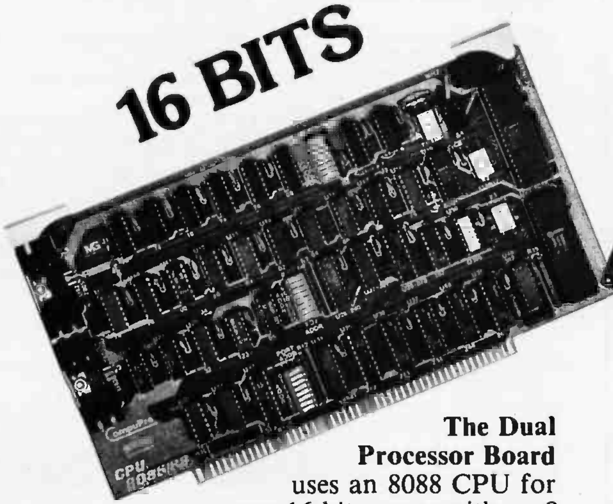

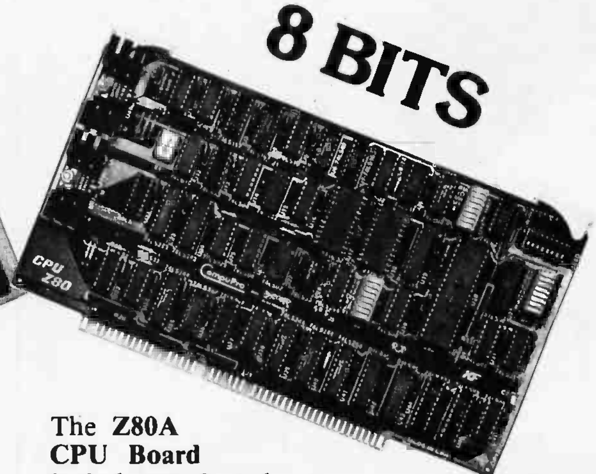

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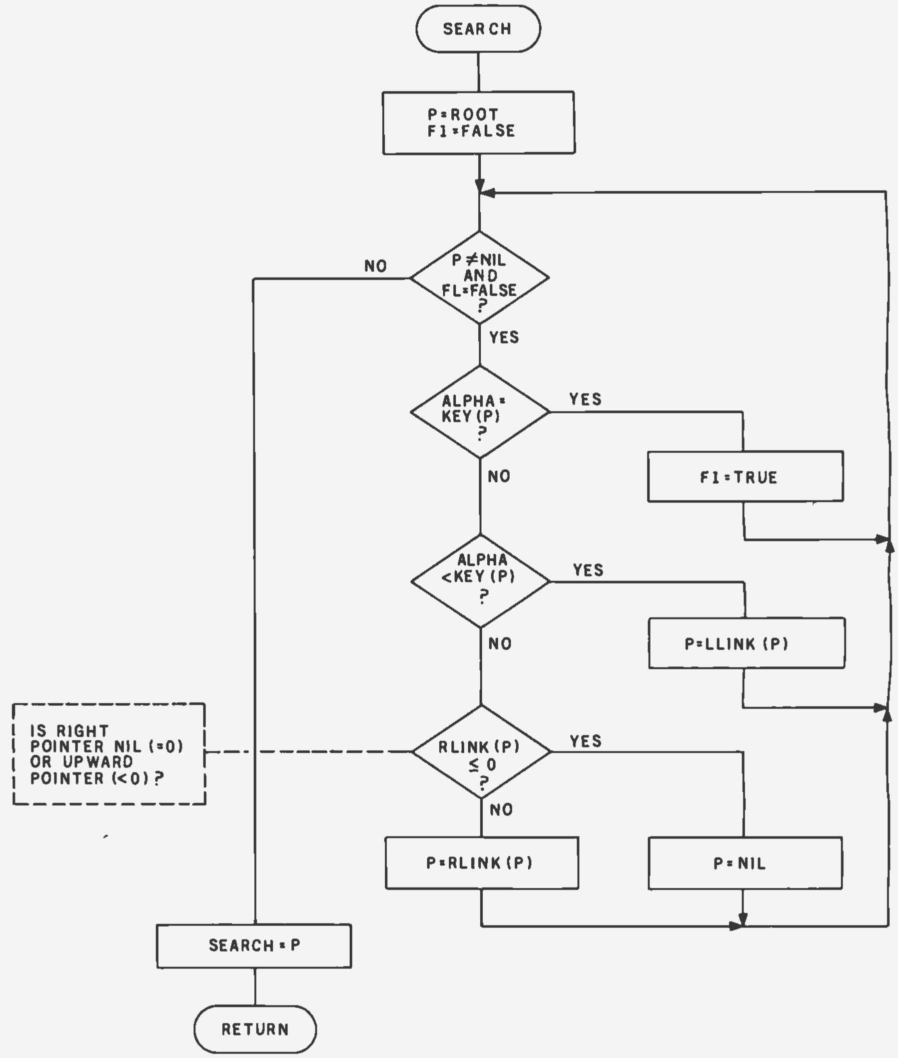

Figure 11: *Flowchart for subroutine SEARCH. This subroutine searches the binary tree for a node with a key value of ALPHA.*

Text continued from page 110:

will also refer to as NIL). This is node number 7, the one that contains 10 as its key. We print the value 10 and follow the right pointer back up the tree to node 2, which contains a 12. We print the 12 and follow the right pointer of this node to node 4.

Node 4 has no left child, therefore we print 14 and follow the right pointer back up the tree to node 1. At node 1, we print 15 and follow the right pointer to node 3. Node 3 has a left child, so we move from node 3 along the left pointer to node 6. Node 6 has no left child, so we print the contents of node 6, which is 20.

Following the right pointer of node 6 back to node 3, we print its value, 25. Following the right pointer of node 3 to node 5, we find the 26, which has no left child. So we print 26 and look at the right pointer of this node. Since the right pointer is NIL, the rightmost node must have no sucessor. This means it is the last node in the tree, so we end the sort.

This is certainly a lot of trouble—unless you want to do more than just sort your numbers once. And it is here that the binary tree shows its greatest advantage. In most sort procedures, if you add a number to the list to be sorted, you have to completely re-sort the new list. But with a binary tree, all you have to do is add one node and list the tree (both of which take much less time than a complete re-sort).

Figure 8 shows the addition of one node, a 13, to be added to the tree of figure 7. The 13, being the eighth number in our list, becomes node 8. It is added to the tree at the bottom of the appropriate branch, necessitating the change of only one pointer in the

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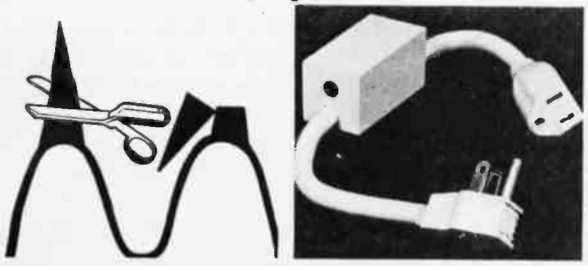

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See review in July 80 BYTE By Jerry Pournelle.

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Deletion of nodes from the tree is not as obvious a procedure as one might suppose.

old tree: the left pointer of node 4 now points to node 8. All the other pointers remain intact, thus keeping computer time to a minimum. Best of all, no key values of nodes have been altered in the least.

It is not hard to write a subroutine that will traverse a binary tree in the proper order. Nor is it difficult to write a subroutine to add a node to a tree—or, equivalently to add a number to a sorted list. Deletion of nodes from the tree, however, is not as obvious a procedure as one might suppose.

Detaching the node to be deleted is simply a matter of destroying the pointers from other nodes to the undesired node. But repair of the tree diagram—connecting nodes below the deleted node to the body of the tree—is not quite so easy. There are several cases to be considered, all of which are handled by the subroutine DEL.

The binary-tree-sort program in listing 1 was designed as a main routine and a collection of subroutines. A brief description of

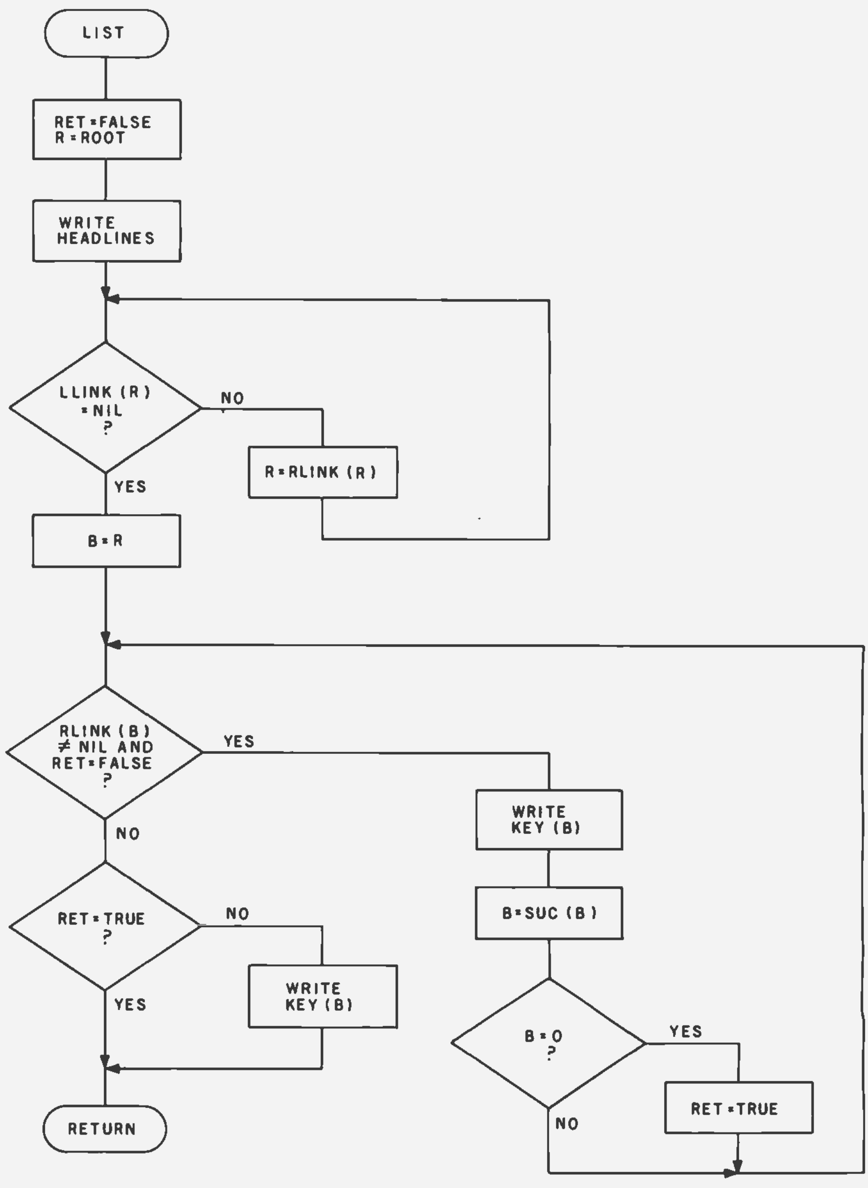

Figure 12: *Flowchart for subroutine LIST. This subroutine traverses the binary tree in sorted key order and prints the nodes as they are encountered.*

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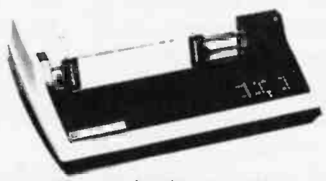

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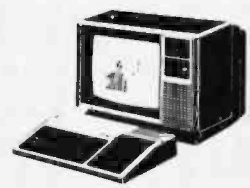

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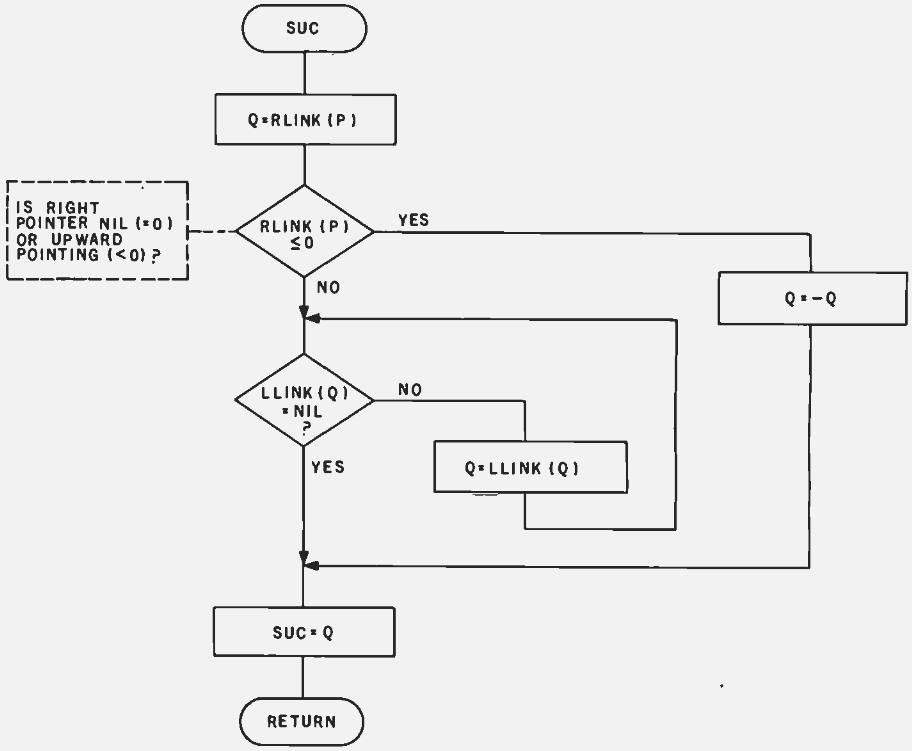

Figure 13: *Flowchart for subroutine SUC. This subroutine, given for a node P, finds the number of the node that is the successor of node P in the sorted-key sequence.*

each subroutine (given below) and a flowchart describe the operation of each of the subroutine modules. Each of the subroutines was written in structured fashion. Although the main routine is also structured, the current listing reflects a certain amount of modification and experimentation; in other words, it has not been rewritten for optimal structure.

The main routine of listing 1 contains the following sequence: an array of 100 random integers is created and used to create a sorted binary tree; the binary tree is listed; then the user is given the options of adding to the tree, listing the tree, or deleting from the tree. All the necessary subroutines are included in this listing.

This program was originially written in FORTRAN and was later translated to BASIC, running first on a PET, then on an Apple II. The program contains some redundancies so that the program will run as written on both machines; the only restriction is that line 5 must be deleted before running the program on the PET. The structured programming techniques used in writing the original FORTRAN version proved to be quite necessary when translating and debugging the BASIC version. I feel that structured programming techniques are essential to a program of any size.

Subroutine Descriptions

FIX: The purpose of the subroutine FIX (see flowchart in figure 9) is to initialize all the space to be used for tree nodes before the binary tree is built. The FIX subroutine must be presented with N, the maximum number of nodes to be available to the tree. Once the tree has N nodes, there are no provisions in this program to make additional space available.

BILDER: Subroutine BILDER adds a new data entry to the binary tree, placing it in correct relation to the other nodes in the tree. Within the BILDER routine, the node to be added is numbered Q and has a value of KEY(Q). The algorithm (see flowchart in figure 10) compares the node to be added, Q, with other nodes (starting with the root node and moving down the tree) until it can be placed in proper relation to a

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parent node (a node that has a NIL pointer pointing to where node Q should go).

SEARCH: The SEARCH subroutine (see figure 11) returns the node number of a key with value ALPHA. The node number (or zero if the node is not found) is returned in the variable SEARCH. The search done is not a linear search but rather a *binary search* like the one used in BILDER. A binary search is named such because each decision halves the area to be searched.

LIST: The LIST subroutine (see figure 12) lists the nodes of the tree in ascending key sequence by traversing the tree from its leftmost to its rightmost node. LIST follows an optimal path down the leftmost branch of the tree until it encounters a node the left pointer of which has value NIL; this node contains the smallest key value. Having found the smallest key value, LIST then calls SUC (the successor subroutine) repeatedly to find successor nodes; key values are printed in the order they are encountered. When a node is found that has a right pointer of value NIL, the node with the highest key value has been found, and the LIST subroutine has finished.

Text continued on page 260

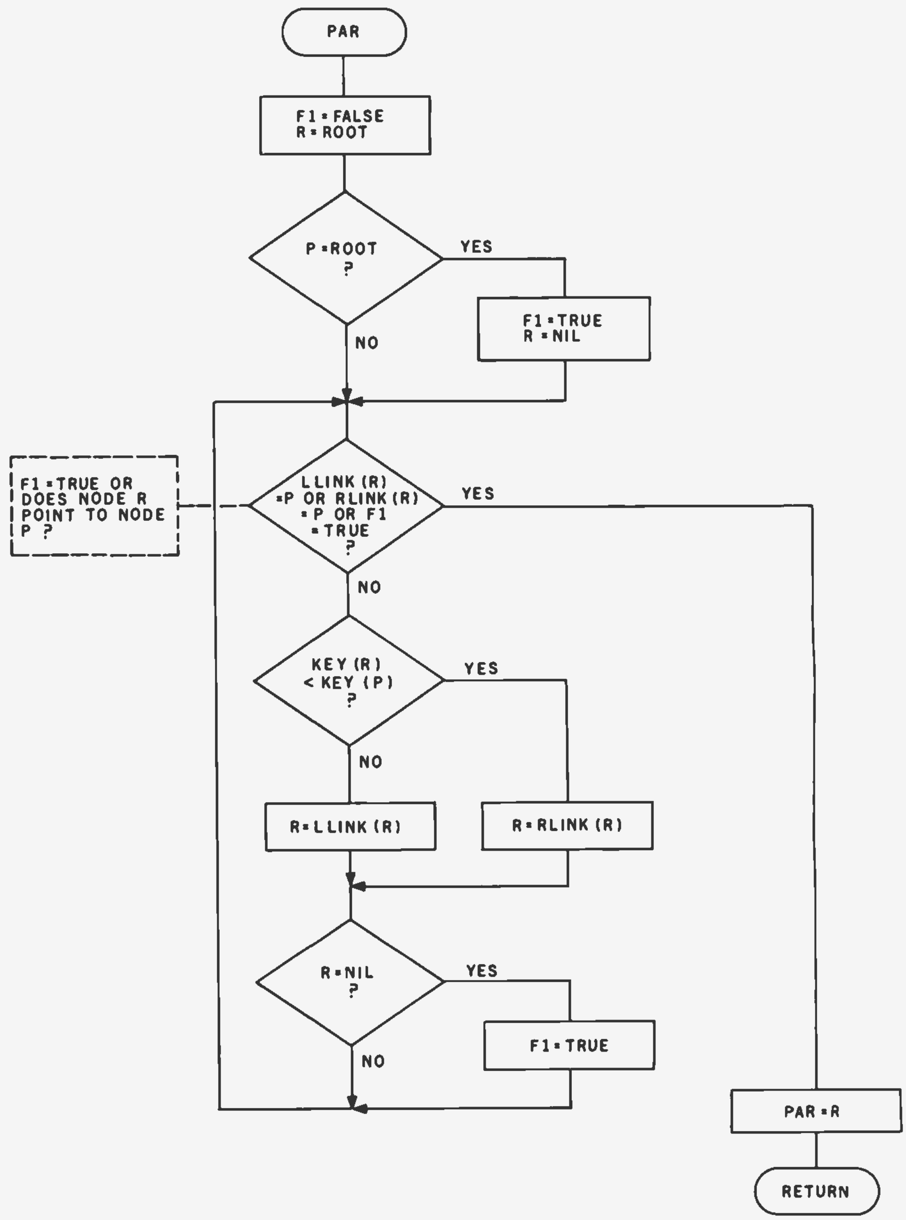
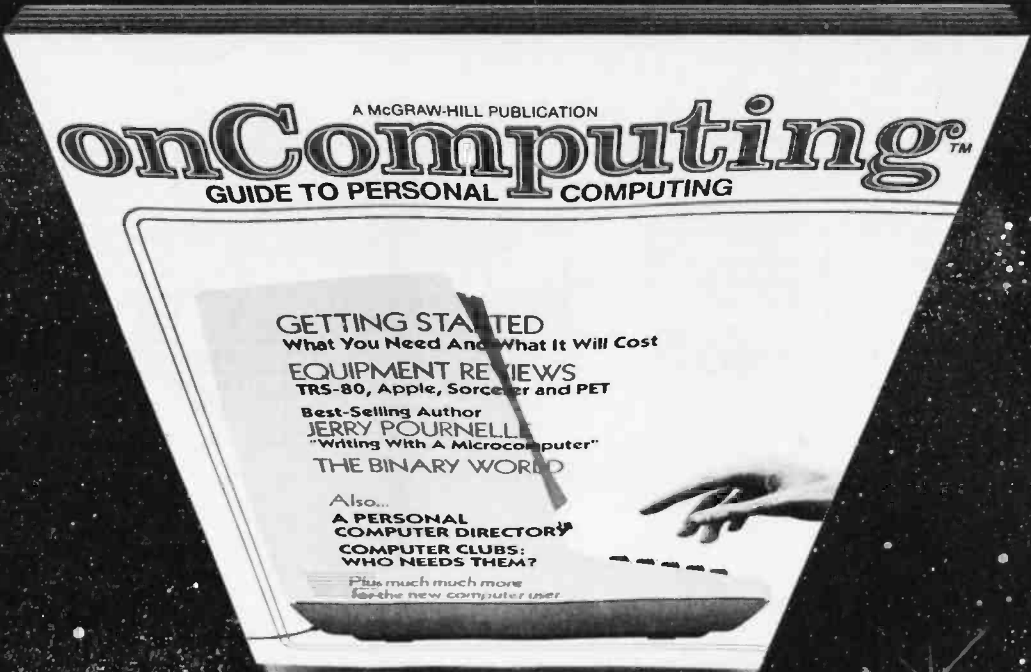


Figure 14: *Flowchart for subroutine PAR. This subroutine finds the parent node of a given node P.*



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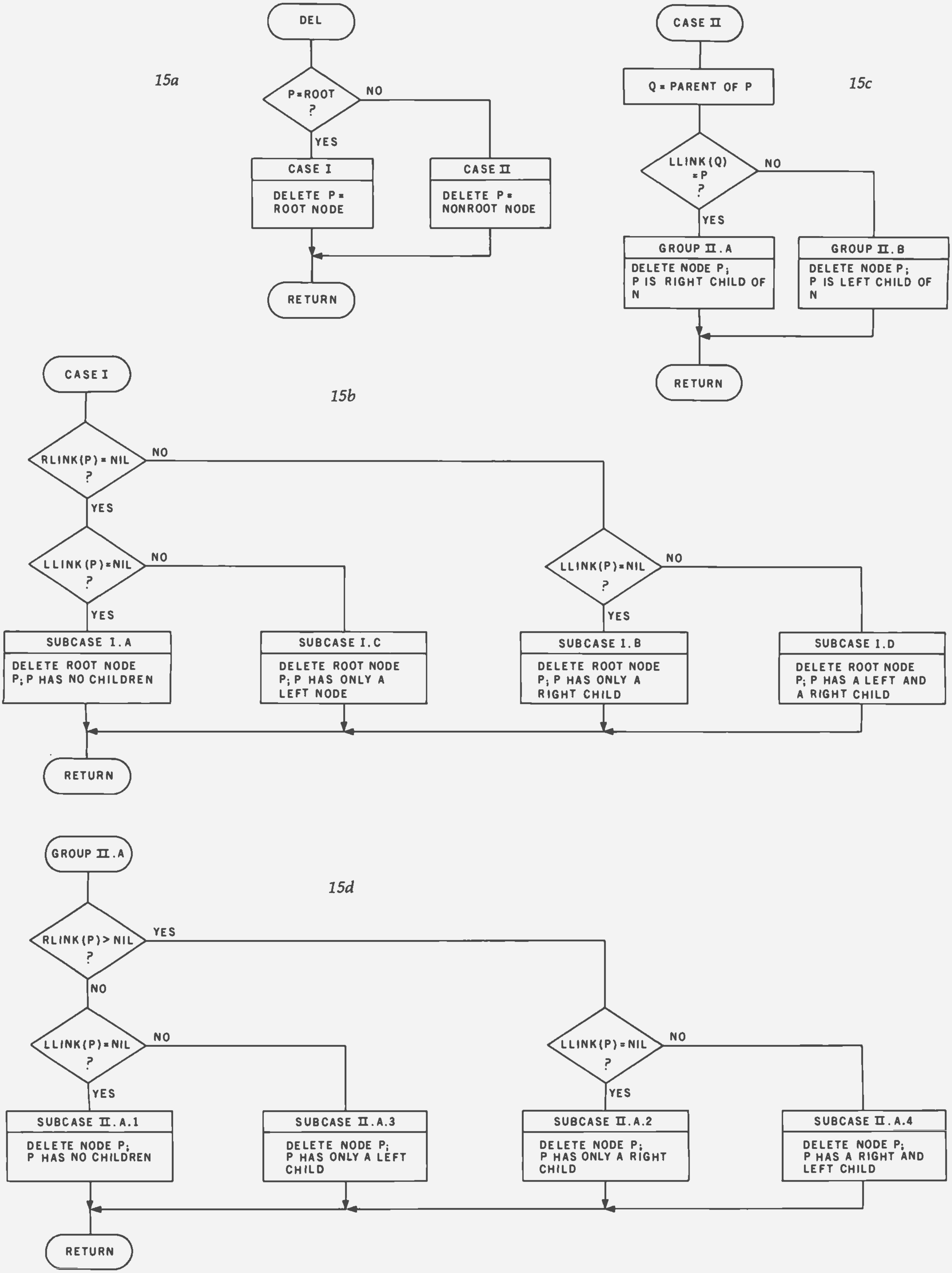
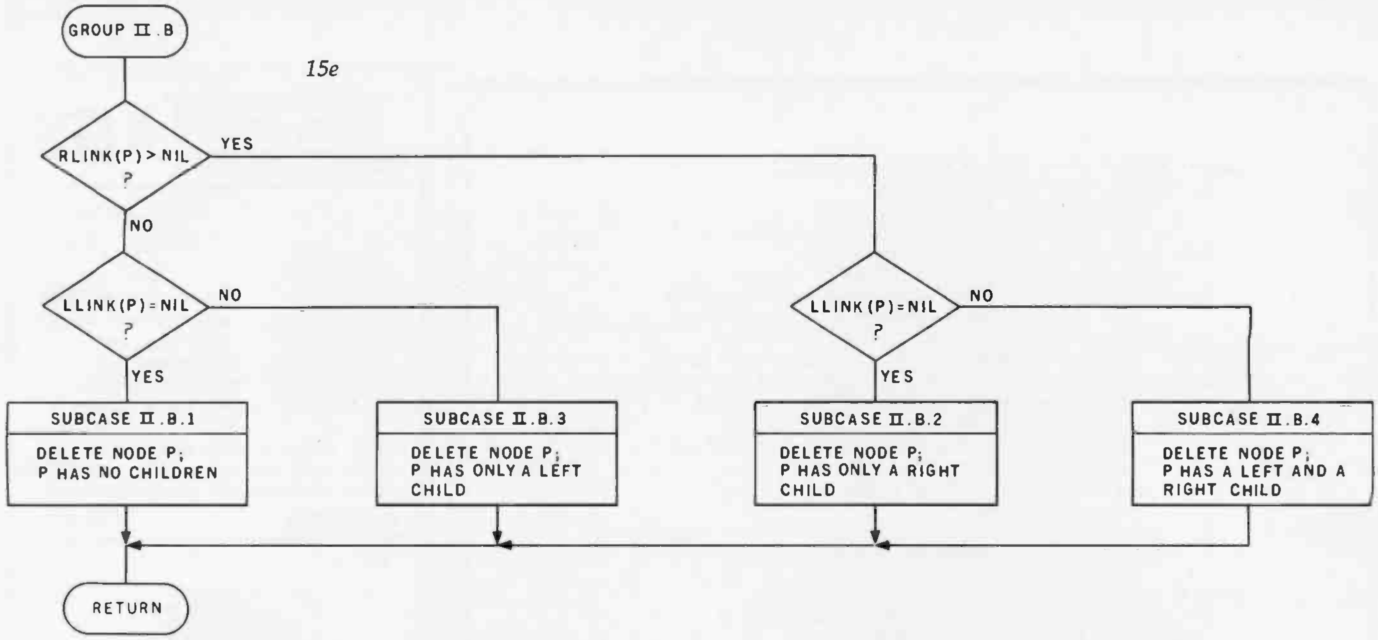


Figure 15: *Flowchart for subroutine DEL. Figures 15a thru 15e describe the algorithm, with further description given in table 1. Case I is executed when the node to be deleted, P, is the root node. Case II, group A is executed when the node to be deleted, P, is the left child of a parent node. Case II, group B is executed when the node to be deleted, P, is the right child of a parent node.*

15e


GROUP II.B
RLINK(P)>NIL ?
YES
NO
LLINK(P)=NIL ?
NO
YES
LLINK(P)=NIL ?
NO
YES
SUBCASE II.B.1
DELETE NODE P; P HAS NO CHILDREN
SUBCASE II.B.3
DELETE NODE P; P HAS ONLY A LEFT CHILD
SUBCASE II.B.2
DELETE NODE P; P HAS ONLY A RIGHT CHILD
SUBCASE II.B.4
DELETE NODE P; P HAS A LEFT AND A RIGHT CHILD
RETURN

Case I: Node P to be deleted is the root node.
- Subcase A: Node P has no children.
  1. Set EMPTY = TRUE.
  2. Set N (the number of nodes in the tree) to zero.
- Subcase B: Node P has only a right child.
  1. Set new root equal to right link of old root.
- Subcase C: Node P has only a left child (see figure 16a).
  1. Set new root equal to the left link of the old root.
  2. Search right branch of left child of P for its rightmost node R. Set the right pointer of R to NIL.
- Subcase D: Node P has a left and a right child (see figure 16b).
  1. Set new root equal to the right link of old root.
  2. Search left branch of right child of P for its leftmost node S. (S will have a left pointer of NIL.) Set left pointer of S to the left child of the old root (that is, to point to the left subtree of the old graph).
  3. Search right branch of left child of P for its rightmost node R. Set right pointer of R to point to S.

Case II: Node P to be deleted is not the root node.
- Group A: Node P is the left child of parent node Q.
  - Subcase 1: Node P has no children.
    a. Set LEFT link of parent Q to NIL.
  - Subcase 2: Node P has only a right child.
    a. Set LEFT pointer of parent node Q to right child of P.
  - Subcase 3: Node P has only a left child (see figure 16c).
    a. Set LEFT pointer of parent node Q to left child of P.
    b. Search right branch of left child of P for its rightmost node R; this node will have an upward right pointer to P. Assign the right pointer of R the value of the right pointer of P.
  - Subcase 4: Node P has a left and a right child (see figure l6d).
    a. Set LEFT pointer of parent node Q to right child of P.
    b. Search left branch of right child of P for its leftmost node S. (S will have a left pointer of NIL.) Assign the left pointer of S the value of the left pointer of P.
    c. Search right branch of left child of P for its rightmost node R. Assign the right pointer of R the value -S.
- Group B: Node P is the right child of parent node Q. (Subcases 1 thru 4 are the same if the word RIGHT is substituted for the capitalized word LEFT in each subcase.)

Table 1: *Analysis of node deletion in a threaded binary tree. This table details the operations necessary to delete a node, labeled P, from a threaded binary tree. This table is associated with figure 15, figure 16, and listing 1.*

Text continued from page 256:

SUC: The SUC subroutine, shown in figure 13, when given the node numbered P, returns the value SUC, which is the number of the node that follows node P in the ascending key sequence. If the right pointer of P, named Q, is an upward pointer (value less than zero), the absolute value of the pointer is the successor node. If Q is a downward pointer, the leftmost child of Q is the successor node. A SUC value of NIL is returned if node P is the rightmost node in the tree.

PAR: The PAR subroutine, shown in *figure 14*, returns in variable PAR the number of the parent node of node P. (Remember that every node in a binary tree except the root node has exactly one parent node.) As in BILDER and LIST, a binary search starting at the root uses the values of the current node key and the key of node P to guide the search down the tree until the parent of P is found. This method is much faster than linearly traversing the tree using the SUC subroutine.

DEL: The DEL subroutine to delete a node from the tree is the most complicated of the subroutines presented. This is due largely to the necessity of reestablishing the thread that runs through the tree. The algorithm for node deletion is given in figure 15 and table 1; the examples in figure 16 are referred to by table 1.

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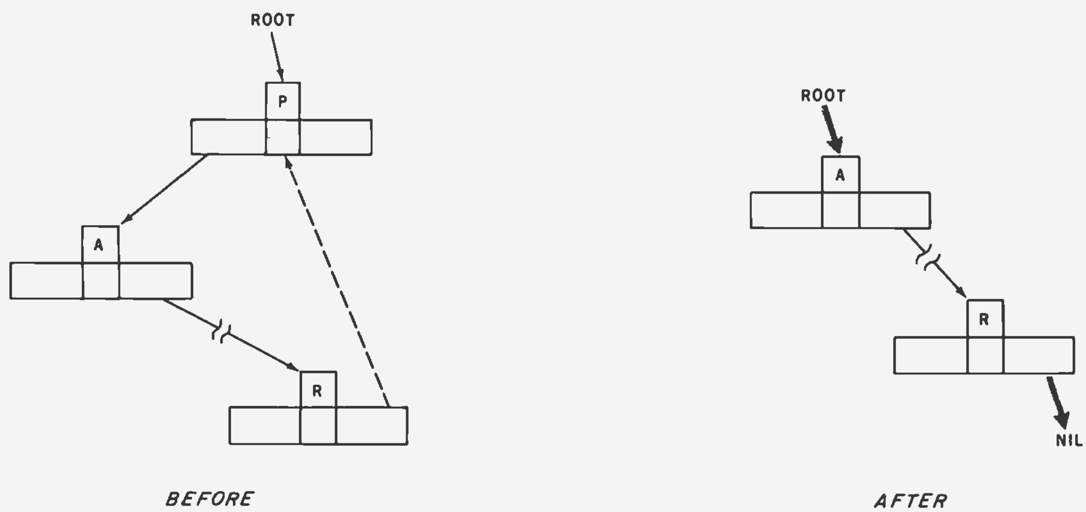


16b SUBCASE I.D

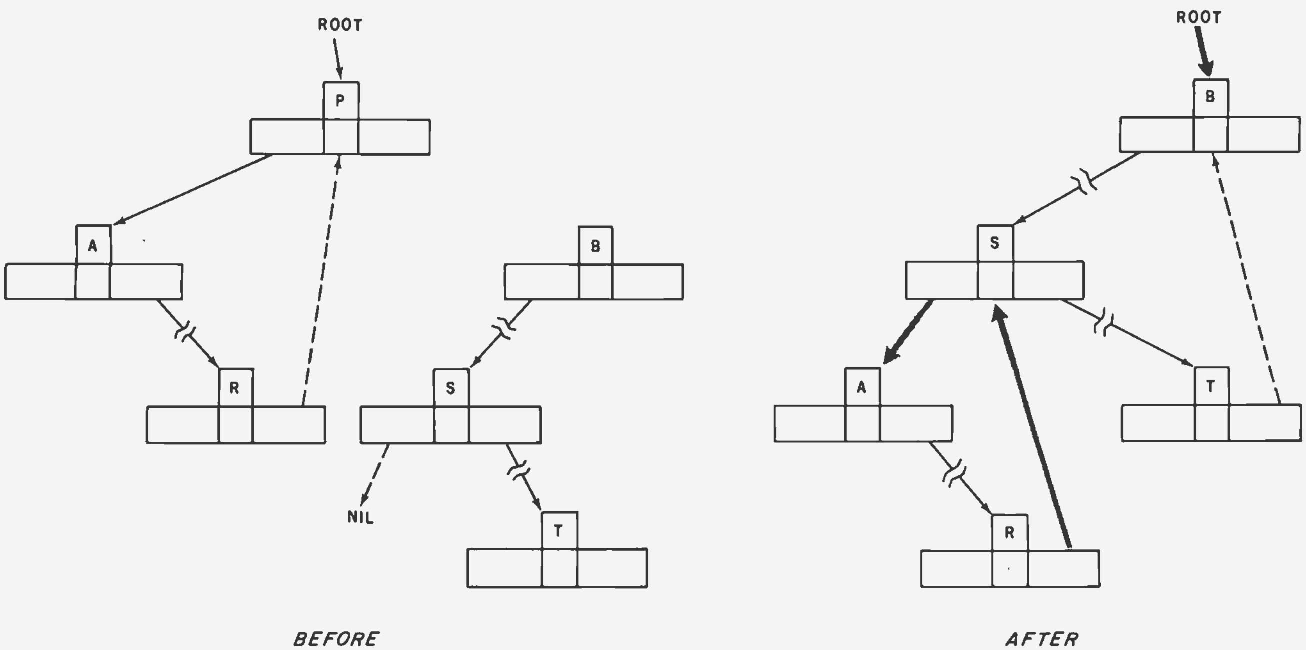


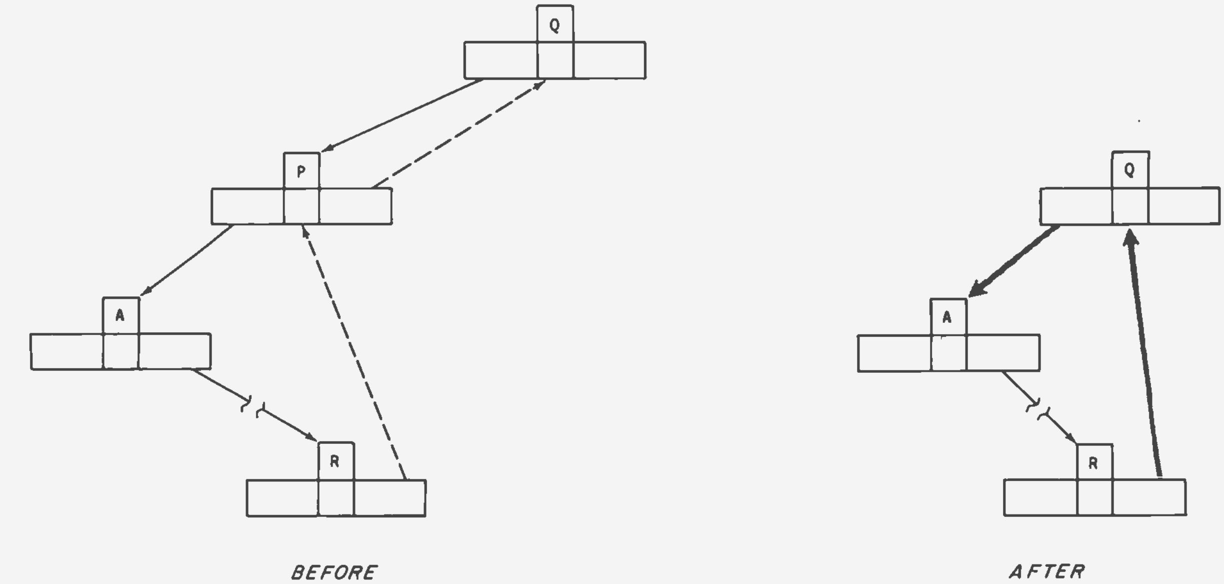
Figure 16: *Examples of node deletion. Figures 16a thru 16d are used to illustrate the structure of a binary tree before and after the deletion of node P; they are referred to by table 1. A broken arrow (for example, A to R) denotes an eventual connection through zero or more intermediate children. A dashed arrow denotes an upward right pointer to the next node in the sorted key sequence. A gray arrow in the "after" drawing denotes a pointer that has been changed by the deletion.*

version of the binary tree program is given in listing 3. This version does not use a threaded tree (ie: there are no upward right pointers). Because of this, the subroutine to add a node is almost trivial, and the delete routine is greatly simplified. This implementation is, in general, altogether nicer.

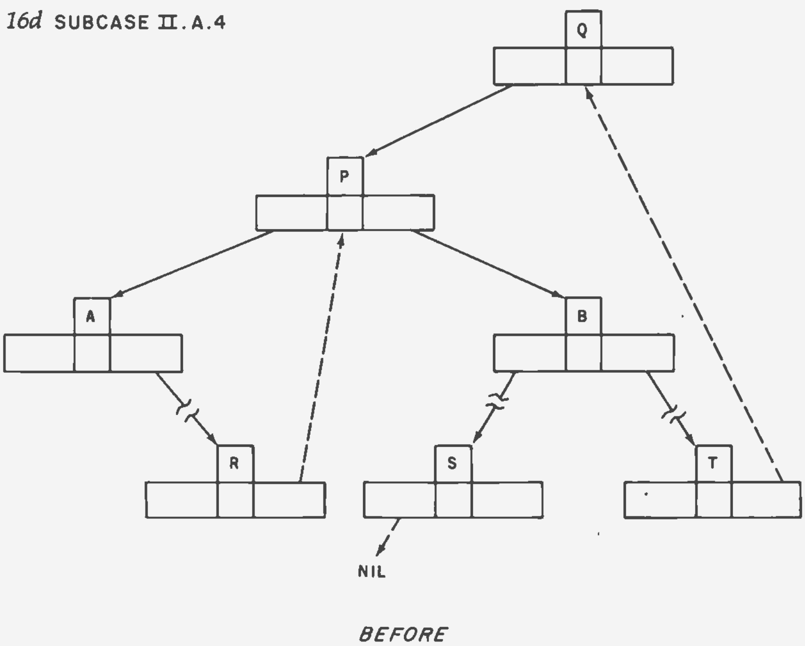
The main change in this listing (compared to the BASIC program of listing 1) is the use of the *scan* procedure to traverse and list the tree. The *scan* procedure uses a stack, which is maintained by the *initstack* and *push* procedures, along with the *pop* function. The *scan* algorithm is as follows:

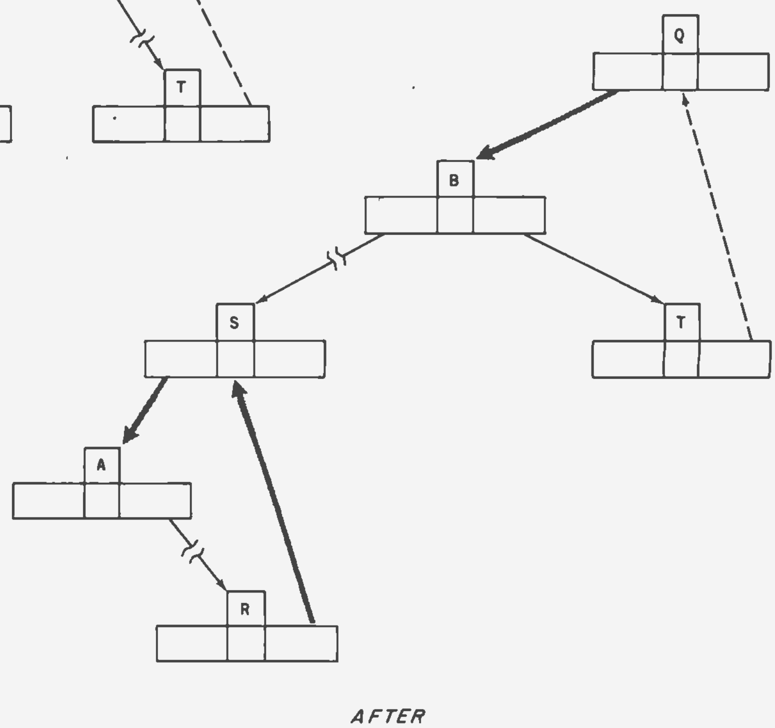
1) Move left along the branches of the tree, placing each node traversed onto the stack.
2) When a left pointer of NIL is reached, pop the stack and print what was just popped.
3) If you can, move right one node and go to step 1; otherwise, pop the stack, print the node popped, and repeat step 3.
4) Underflow of the stack represents the end of the algorithm.

16c SUBCASE II.A.3



16d SUBCASE II.A.4





Due to the nature of the Pascal language, the listing itself serves to document the algorithm. In all fairness to BASIC, it must be stated that the Pascal program of listing 3 is simpler partially due to the absence of the thread running through the binary tree. ■

Acknowledgements

I would like to thank the Computer Corner of Amarillo, Texas, for the use of their printer to produce listings 1 and 2.

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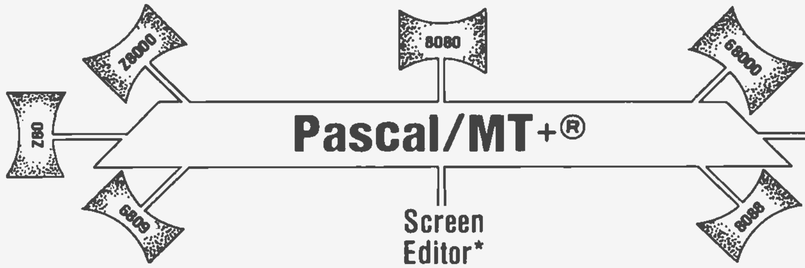

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Machine Problem Solving, Part 2:

Directed Search Using Cryptarithmetic

Professor Peter W Frey
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Cresap Neuroscience Laboratory
2021 Sheridan Rd
Evanston IL 60201

Insight into Problems

Those of us who teach courses on thinking and problem solving are always delighted to find an intellectual puzzle that is stated clearly and concisely, and yet still provides a real challenge for an intelligent problem solver. A number of years ago, Allen Newell discovered the fascination of cryptarithmetic and many of his pioneering ideas on human information processing were based on his research with these puzzles.

A *cryptarithmetic* puzzle consists of a group of letters arranged in the form of an arithmetic problem. Each letter is a code for a digit (0, 1, 2, ..., 9) and only one letter may represent each digit. The problem solver must determine how to assign digits to letters in such a way that the mathematical constraints are satisfied. For example, a popular cryptarithmetic puzzle is:

```
  S E N D
+ M O R E
---------
M O N E Y
```

If the appropriate digit is assigned to each letter, the numbers will add up to give the correct sum. This type of puzzle can be very challenging. If you doubt this, take a moment and try to solve the example given above.

Direct Logical Analysis

When humans attempt to solve these problems, they use a combination of logical inference and directed search. The values for some of the letters can be determined, or at least restricted to a subset of values, by direct logical analysis. The value of the remaining letters is then determined by a "generate and test" approach in which plausible values are examined until a suitable one is found. As more information is acquired, logical deduction can narrow the search to a limited number of potential solutions.

As an example, let us consider the SEND + MORE = MONEY puzzle. The first insight that most individuals have after considering the problem for a few moments is that the letter M can be easily deciphered. MONEY has five letters and SEND and MORE have only four. Therefore, one can deduce that S + M + the carry from the previous column = MO. The maximum possible values for S and M are 8 and 9 and the carry is at most 1, so therefore MO is 18 or less. It follows that M can be only 0 or 1. If it were 0, however, it would not be written as the first digit of a number since leading zeroes are not printed. Therefore, the letter M must represent the digit 1.

Armed with this knowledge, it is possible to make additional deductions. For example, if we substitute the digit 1 for the letter M in the equation given in the previous paragraph (ie: S + 1 + carry = O + 10) we can quickly deduce that S must represent a large digit and the letter O has to represent a small digit. In fact, since the maximum value for S is 9, the sum of the column can be no more than 11 if there is a carry and 10 if there is no carry. Therefore, the letter O must be 1 or 0. It is already known, however, that M represents 1 so the letter O represents 0. Given that the sum of the column is 10, then the letter S has to be either 8 (if there is no carry) or 9 (if there is a carry).

Searching Technique

Our detective work has determined that M is 1, O is 0, and S is 8 or 9. In addition, we can infer that the values of 1 and 0 cannot be assigned to any of the other letters. This narrows the search task considerably. A blind *trial-and-error* search process is not very efficient for this problem. There are eight letters in this cryptarithmetic puzzle and ten digits to draw upon. The number of possible assignments is $10\times9\times8\times7\times6\times5\times4\times3$ which equals 1,814,400. The trial-and-error search approach we employed last month for the missionaries-and-cannibals problem is not well-suited for this job. It would work, but it would take a very long time, especially if implemented in BASIC on a microcomputer.

By using logical deduction, however, we can reduce the size of the search space considerably. Since we discovered that M is 1, O is 0, and S is 8 or 9, the number of possible assignments is reduced to $8\times7\times6\times5\times4\times2$ which equals 13,440. This is a substantial improvement.

In addition, the nature of the cryptarithmetic problem permits the use of a specialized *directed search* instead of a nondirected trial-and-error search. The plan for this specific case is to assign digits to the numbers in the right-hand column of the problem, make the addition, and then see if the two top numbers add to give the value assigned to the letter at the bottom of that column.

A check is also made to see that these assignments do not contradict information we already know (ie: M=1, O=0, S=8 or 9), or produce the assignment of the same digit to more than one letter. If no contradictions exist, we then move one column to the left and repeat the process. If we are successful in repeating this generate-and-test approach all the way to the left-most column, we have successfully found a set of digit assignments which solve the problem. This approach avoids the necessity of assigning digits to all the letters before checking for arithmetic correctness.

Using Human Deduction

When humans grapple with cryptarithmetic problems, there is usually a dynamic interplay between deduction and search. As information is deduced concerning which assignments are feasible, the problem solver discards many of his previous working hypotheses and concentrates on specific possibilities which appear to be most promising. It is difficult to accurately simulate this complex process on a machine, but it is possible to emulate some of the key elements in a way that is sufficient to produce a reasonably efficient computer program for solving cryptarithmetic problems. In what follows, we will consider the details of such a program written in Level II BASIC for the Radio Shack TRS-80 microcomputer.

Our technique for solving these challenging puzzles can be considered in three parts: the *representation* for the specific problem, the *deduction of some of the values* on the basis of pattern analysis, and the *development of a complete solution* by directed search. As is often the case, the programming steps required to set up the problem and develop a representation constitute almost half of our effort.

The first steps are strictly preparatory. The video display is cleared, all variables are declared as integers, space is set aside for string storage, and a title is placed on the video display:

```
100 CLS: DEFINT A-Z:
  CLEAR 200: PRINT@150, "CRYPTARITHMETIC"
```

Next we have the machine ask for the specific puzzle for which a solution is desired:

```
110 PRINT@272, "CODE FOR FIRST NUMBER";:
  INPUT X$(1)
120 PRINT@336, "CODE FOR SECOND NUMBER";:
  INPUT X$(2)
130 PRINT@400, "CODE FOR SUM OF ABOVE";:
  INPUT X$(3)
```

We will need several arrays to store pertinent information. The C array will record whether a carry is present for each of the columns, given the letter values that are being tested at a given point in time. The D array will keep track of which digit assignments are feasible for each letter after the restrictions we discover from our initial detective work (ie: pattern recognition).

We will identify each letter by a number code and identify these codes by letter in the D$ array and by position in the puzzle with the S$ array. The digit that is being tested for each letter will be indexed by the K array (parallel to D$) and the S array (parallel to S$). The length of each of the code words is stored in the L array.

```
140 DIM C(8), D(10,10), D$(10), K(11), L(3), S(3,10),
  S$(3,10)
```

The processing task begins by determining the length of each code word and by breaking up each word into its individual letters:

```
160 FOR J=1 TO 3: L(J)=LEN(X$(J)):
  FOR I=1 TO L(J)
170 N=L(J)-I+1: S$(J,I)=MID$(X$(J),N,1,):
  NEXT I: NEXT J
```

The index J is used to represent the first word (J=1), second word (J=2), and third word (J=3), and the index I is used to represent the right-hand column (I=1), the column one over from the right (I=2), etc.

Our next objective is to assign an identifying number to each letter (the index of array D$) and associate each of these identifying numbers with a position in the cryptarithmetic puzzle by setting up the S array. The variable NL records the number of different letters in the puzzle:

```
200 NL=0: I=0
210 I=I+1: IF I>L(3) THEN 300 ELSE J=0
220 J=J+1: IF J>3 THEN 210
230 IF I > L(J) THEN 220 ELSE N=0
240 N=N+1: IF S$(J,I)=D$(N) THEN S(J,I)=N:
  GOTO 220
250 IF N<NL THEN 240
260 NL=NL+1: D$(NL)=S$(J,I): S(J,I)=NL:
  GOTO 220
```

It is also necessary to prepare the machine with the knowledge that blank spaces which precede letters in the first two rows should be treated as zeroes.

```
270 IF L(2)>L(1) THEN S(1,L(2)) = 11
280 IF L(1)>L(2) THEN S(2,L(1)) = 11
```

Now the machine is almost ready to begin processing. Before it gets started, however, a neatly arranged graphical display of the puzzle is needed as well as a list of the letters in the order that digits will be assigned:

```
300 CLS: PRINT CHR$(23):
  PRINT@226-4*L(2),"+";
310 FOR J=1 TO 3: FOR I=1 TO L(J):
  K=104+64*2↑(J-1)-4*I
320 PRINT@K, S$(J,I);: NEXT I: NEXT J
330 FOR I=1 TO L(3): PRINT@294-4*I,"---";:
  NEXT I
350 FOR I=1 TO NL: PRINT@636+6*I, D$(I);:
  NEXT I
```

Restricting Values

The first step in searching for a solution is to determine what values, if any, cannot be reasonably assigned to particular letters. In our present effort, we will not attempt anything as complex as trying to directly deduce this information. Instead we will use pattern analysis to identify certain obvious cases.

In order to use this information in our search, we will set up a special array, D(J, I), in which the first index, J, will represent each of the letters we are working with and the second index, I, will represent each of the digits (0 to 9) which might potentially be assigned to each of the letters:

```
380 FOR J=1 TO NL:
  FOR I=0 TO 9: D(J,I)=I: NEXT I:
  NEXT J
```

To indicate that a particular digit cannot be assigned to one of the letters, the machine will set the appropriate member of the D array to the value of 99. Two subroutines will be used for this purpose. When the machine has determined that a particular letter can be assigned only one digit, it will record this information by calling these subroutines. The first subroutine sets all the values for that letter to 99:

```
2000 FOR I=0 TO 9: D(Z,I)=99: NEXT I: RETURN
```

The second subroutine sets this digit in the arrays for the other letters to 99 and sets the digit value for the correct letter back to the proper value:

```
3000 FOR I=1 TO NL: D(I,X)=99: NEXT I:
  D(Z,X)=X: RETURN
```

With these subroutines in hand, the machine is ready to analyze letter patterns to determine if certain letters can only take on a restricted set of values.

Patterns

The first pattern the program looks for is the one we described at the beginning of this article when discussing the SEND + MORE = MONEY cryptarithmetic puzzle:

```
400 F=0: IF L(3)=L(1) OR L(3)=L(2) THEN 500
410 J=S(3,L(3)): Z=J: GOSUB 2000: X=1:
  GOSUB 3000
420 Z=0: IF J=S(1,L(1)) THEN Z=S(2,L(2))
430 IF J=S(2,L(2)) THEN Z=S(1,L(1))
440 IF Z=0 THEN 500
450 GOSUB 2000: D(Z,8)=8: D(Z,9)=9
460 Z=S(3,L(3)-1): IF J=Z THEN 500
470 GOSUB 2000: X=0: GOSUB 3000: F=1
```

This block of code checks to see if the bottom line of the puzzle is longer than both the first and second lines. If so, the first letter of the bottom line has to be 1, and the D array is altered accordingly. The machine then checks to see if one of the first two lines starts with the same letter as the bottom line. If so, it can further restrict the values which are allowed for the remaining letters in this column.

The next pattern the machine looks for is the case of a column where one of the letters in the first two lines is identical to the letter at the bottom of the column. In this case, the odd letter in the column must be either 0 or 9. If the digit 0 was assigned previously (ie: line 470), then the odd letter has to be 9. If this pattern is discovered, the D array is modified appropriately.

```
500 FOR P=1 TO L(1): Z=0
510 IF S(1,P)=S(3,P) THEN Z=S(2,P)
520 IF S(2,P)=S(3,P) THEN Z=S(1,P)
530 IF Z=0 THEN 570 ELSE GOSUB 2000
540 IF P=1 THEN X=0: GOSUB 3000: GOTO 570
550 IF F=1 THEN X=9: GOSUB 3000: GOTO 570
560 D(Z,0)=0: D(Z,9)=9
570 NEXT P
```

Both of the above patterns are easy to detect. Other informative letter arrangements are more complex and involve recursive IF ... THEN reasoning. The structure of the present program is such that these additional analyses can be added to increase the "intelligence" of the program. In each case, the information would be used to modify the D array such that certain letter-digit combinations would be eliminated from the search procedure that follows.

The Directed Technique

The heart of our cryptarthmetic problem solver is the directed-search process. Although this process is highly mechanical, it gives the program the appearance of being intelligent. It would work even if lines 400 thru 570 were eliminated from the program. The solution times, however, would be much slower without these lines.

The search process is somewhat similar to the blind trial-and-error procedure we employed last month for the missionaries-and-cannibals problem. The major enhancement is that digits are first assigned to the letters in the right column of the problem and then the addition is checked for accuracy. If it is incorrect, a new value is

Text continued on page 271

Listing 1: *A BASIC program to solve cryptarithmetic puzzles. This program, written for the Radio Shack TRS-80 computer with Level II BASIC, solves problems similar to SEND + MORE = MONEY, where each letter of each word represents exactly one of the decimal digits 0, 1, 2, ... , 9. This program decreases the solution time by incorporating several human-derived insights that decrease the solution space.*

```
100 CLS: DEFINT A-Z: CLEAR 200:
      PRINT@ 150, "CRYPTARITHMETIC"
110 PRINT @272 "CODE FOR FIRST NUMBER";: INPUT X$(1)
120 PRINT@336, "CODE FOR SECOND NUMBER";:
      INPUT X$(2)
130 PRINT@400, "CODE FOR SUM OF ABOVE";: INPUT X$(3)
140 DIM C(8), D(10,10), D$(10), K(11), L(3), S(3,10), S$(3,10)
160 FOR J=1 TO 3: L(J)=LEN(X$(J)): FOR I=1 TO L(J)
170 N=L(J)-I+1: S$(J,I)=MID$(X$(J),N,1): NEXT I:  NEXT J
200 NL=0: I=0
210 I=I+1: IF I>L(3) THEN 300 ELSE J=0
220 J=J+1: IF J>3 THEN 210
230 IF I > L(J) THEN 220 ELSE N=0
240 N=N+1: IF S$(J,I)=D$(N) THEN S(J,I)=N: GOTO 220
250 IF N<NL THEN 240
260 NL=NL+1: D$(NL)=S$(J,I): S(J,I)=NL: GOTO 220
270 IF L(2)>L(1) THEN S(1,L(2)) = 11
280 IF L(1)>L(2) THEN S(2,L(1)) = 11
300 CLS: PRINT CHR$(23): PRINT@226-4*L(2), "+";
310 FOR J=1 TO 3: FOR I=1 TO L(J):
      K=104+64*2*(J-1)-4*I
320 PRINT@K, S$(J,I);: NEXT I: NEXT J
330 FOR I=1 TO L(3): PRINT@294-4*I, "---";: NEXT I
350 FOR I=1 TO NL: PRINT@636+6*I, D$(I);: NEXT I
380 FOR J=1 TO NL: FOR I=0 TO 9: D(J,I)=I:
      NEXT I: NEXT J
400 F=0: IF L(3)=L(1) OR L(3)=L(2) THEN 500
410 J=S(3,L(3)): Z=J: GOSUB 2000: X=1: GOSUB 3000
420 Z=0: IF J=S(1,L(1)) THEN Z=S(2,L(2))
430 IF J=S(2,L(2)) THEN Z=S(1,L(1))
440 IF Z=0 THEN 500
450 GOSUB 2000: D(Z,8)=8: D(Z,9)=9
460 Z=S(3,L(3)-1): IF J=Z THEN 500
470 GOSUB 2000: X=0: GOSUB 3000: F=1
500 FOR P=1 TO L(1): Z=0
510 IF S(1,P)=S(3,P) THEN Z=S(2,P)
520 IF S(2,P)=S(3,P) THEN Z=S(1,P)
530 IF Z=0 THEN 570 ELSE GOSUB 2000
540 IF P=1 THEN X=0: GOSUB 3000: GOTO 570
550 IF F=1 THEN X=9: GOSUB 3000: GOTO 570
560 D(Z,0)=0: D(Z,9)=9
570 NEXT P
800 FOR I=0 TO NL: K(I)=-1: NEXT I
810 P=1: I=0: C(0)=0: K(11)=0
820 I=I+1: K(I)=-1
830 K(I)=K(I)+1: IF K(I)>9 THEN 1000
840 IF D(I,K(I))=99 THEN 830 ELSE J=0
850 J=J+1: IF J=I THEN 870
860 IF K(J)=K(I) THEN 830 ELSE 850
870 PRINT@762+6*I, K(I);
880 Z=K(S(3,P)): IF Z=-1 THEN 820
890 Y=K(S(2,P)): IF Y=-1 THEN 820
900 X=K(S(1,P)): IF X=-1 THEN 820
910 TS=X+Y+C(P-1)
920 IF TS>9 THEN C(P)=1 ELSE C(P)=0
930 IF TS<>Z+10*C(P) THEN 830
940 IF P<L(1) THEN P=P+1: GOTO 880
950 IF L(3)=L(1) AND C(P)=1 THEN 830
960 IF L(3)>L(1) AND C(P)=0 THEN 830
970 PRINT@960, "SUCCESS";: GOTO 970
1000 K(I)=-1: PRINT@762+6*I, " ";: I=I-1: P=1
1010 IF I>0 THEN 830
1020 PRINT@960, "FAILURE";: GOTO 1020
2000 FOR I=0 TO 9: D(Z,I)=99: NEXT I:  RETURN
3000 FOR I=1 TO NL: D(I,X)=99:
      NEXT I: D(Z,X)=X: RETURN
```

Text continued from page 269:

assigned to the most recently modified letter. If the addition is correct, values are then assigned to the letters in the second column from the right. The addition for this column, including the carry when present for the right-hand column, is then checked. If incorrect, a new assignment is made. If correct, the machine goes over to the next column. The machine continues this process until it finds a solution or until all letter-digit combinations have been tried without success.

Because there are so many possible combinations, solution time is much shorter if some of the potential assignments can be eliminated during the preliminary analysis of letter patterns. The search occurs much more rapidly with addition checks made column by column rather than through assigning a digit to all letters before checking to see if the digits add up correctly. These preliminary checks provide considerable direction to an otherwise unstructured search.

Program Operation

The primary actor in the machine's search process is array K. This array keeps track of which digit is currently being tested for each letter. When no assignment has been made to a letter, the value of K will be set at −1. The variable NL, as you recall, represents the number of letters in the puzzle. The index P will represent which column of the puzzle is currently in the spotlight. The array C will keep a record of whether a carry has occurred for each of the columns. The index I keeps track of the letter to which the machine is currently assigning a digit.

The first step is to initialize the key variables:

```
800 FOR I=0 TO NL: K(I)=-1: NEXT I
810 P=1: I=0: C(0)=0: K(11)=0
```

Then we establish the main loop:

```
820 I=I+1: K(I)=-1
830 K(I)=K(I)+1: IF K(I)>9 THEN 1000
```

A branch to line 1000 occurs when all ten digits (0 to 9) have been tried for a letter without success.

The code at line 1000 provides a means to back up and try a new digit for the letter immediately preceding (in the assignment sequence) the current letter:

```
1000 K(I)=-1: PRINT@762+6*I, " ";: I=I-1:
  P=1
1010 IF I>0 THEN 830
1020 PRINT@960, "FAILURE";: GOTO 1020
```

Each time the machine backs up, the index I is decremented by 1, the column analysis reverts back to the right-hand column, and the last digit appearing on the display is erased. If the value of I decreases to zero, all combinations have been tried and found lacking. The machine then makes its failure public by executing line 1020.

If K(I) is assigned a number at line 830 of 9 or less, the program continues by seeing if the new value is an acceptable one by checking the D array for feasible values (line 840) and then makes sure that this digit has not already been assigned to another letter (lines 850 and 860):

```
840 IF D(I,K(I))=99 THEN 830 ELSE J=0
850 J=J+1: IF J=I THEN 870
860 IF K(J)=K(I) THEN 830 ELSE 850
```

If the new assignment passes both of these tests, the machine prints the digit on the display to let the observer know its current "thinking." It then checks to see whether it has assigned a digit to each of the letters in the column that is presently under consideration:

```
870 PRINT@762+6*I, K(I);
880 Z=K(S(3,P)): IF Z=-1 THEN 820
890 Y=K(S(2,P)): IF Y=-1 THEN 820
900 X=K(S(1,P)): IF X=-1 THEN 820
```

If one or more of the letters have not been assigned a digit, the machine branches to line 820 and takes care of this oversight. Otherwise, it calculates the sum of the column (line 910), determines whether or not there is a carry (line 920), and then checks to see if the addition of the two top numbers matches the digit which has been assigned to the bottom letter (line 930):

```
910 TS=X+Y+C(P-1)
920 IF TS>9 THEN C(P)=1 ELSE C(P)=0
930 IF TS<>Z+10*C(P) THEN 830
```

If the numbers do not add up properly, the machine branches to line 830 to try another digit assignment for the letter currently being tested. If the addition is correct,

The pattern-analysis portion of the program provides a capability that mirrors human problem-solving skills.

the TRS-80 checks to see if all columns have been tested. If not, it increments P and jumps to line 880. If all columns have been tested, then it makes sure the carry for the left-hand column is correct. If all is in order, the machine announces to the world that it has found a solution:

```
940 IF P<L(1) THEN P=P+1: GOTO 830
950 IF L(3)=L(1) AND C(P)=1 THEN 830
960 IF L(3)>L(1) AND C(P)=0 THEN 830
970 PRINT@960, "SUCCESS";: GOTO 970
```

A Useful Technique

This program provides an interesting example of problem solving by combining man-like and machine-like techniques. The search process (lines 800 to 1020) is clearly not meant for human use. A systematic, patient search such as this is just not the thing a human would do. On the other hand, it is a highly effective technique for a computer.

The pattern-analysis portion of the program (lines 400 to 520) provides a capability that mirrors human problem-solving skills. Once you have worked with several cryptarithmetic problems, you will learn to recognize these patterns immediately and will use the relevant information to speed the solution process. By programming the machine to recognize these same patterns, we provide a useful mechanism for hastening the search.

In many instances, the most effective program for solving a complex problem is one which uses efficient mechanical algorithms in combination with a knowledge base which is triggered by pattern recognition. It is difficult to write a computer program that accurately imitates human problem-solving methods. However, programs that ignore the domain-specific knowledge used by humans in finding a solution are often very inefficient. The best technique often consists of combining useful features from both approaches into a single mechanical strategy.

To test the generality of our procedure, the reader is encouraged to try additional cryptarithmetic puzzles on the program. Some common puzzles that are worth considering are:

```
  C R O S S     D O N A L D      L E T S
+ R O A D S   + G E R A L D    + W A V E
-----------   -------------    ---------
D A N G E R     R O B E R T    L A T E R
```

As mentioned earlier, the program should be able to solve any puzzle of this type. Try your favorite puzzle and see how long the solution takes. You may wish to add some pattern-recognition information to the program to increase the efficiency of the search.

Next month, we will consider the search process which is commonly employed for two-person, perfect-information, zero-sum games such as chess or checkers. Instead of simply talking about the alpha-beta ($\alpha - \beta$) algorithm, we will present the real thing in its modern form. ■

Book Reviews

Microprocessors and Digital Systems

by Douglas V Hall, Gregg/McGraw-Hill, 1980, 426 pages, hardcover, $15.95

Microprocessors and Digital Systems by Doug Hall is written for people interested in expanding their practical knowledge of electronics. While obstensibly written for technicians and based on an electronics training program at Herald Engineering College in San Francisco, the book brings together a wide variety of subjects which are of significant value to engineers as well as hobbyists.

This book is based upon the premise that it does little good to know the theory of a design without knowing how to assemble, connect, and test a circuit. It is important to recognize and understand how the choice of components and test equipment can affect the success of any project. In a classic bottom-up approach, the reader first becomes familiar with prototyping techniques, wire wrapping, and typical test equipment. Presuming a knowledge of basic electronics and transistor theory, Mr Hall advances through subjects such as digital logic families, logic gates, interfacing, signal conditioning, analog-to-digital and digital-to-analog conversion, and microcomputers.

In the sections on microprocessors, the 8080, 6800, and 6502 receive considerable exposure. Included are sample schematic diagrams for small systems that incorporate these processors, as well as illustrative programs for each. In keeping with the premise of the entire book, the examples presented are programs for a microprocessor-controlled weight scale and an EPROM (erasable programmable read-only memory) programmer. Readers interested in larger computers can gain some insights on BASIC, FORTRAN, and Pascal in a chapter on high-level languages.

There are objectives listed at the beginning of each chapter, and review questions and problems at the end of each chapter.

Mr Hall makes extensive use of manufacturers' data sheets, application notes, and schematic diagrams. *Microprocessors and Digital Systems* is thoroughly oriented toward people who *handle* electronic circuits rather than think about them.

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Z80 Microprocessor Programming and Interfacing

Volumes 1 and 2
by Nichols, Nichols, and Rony
Volume 1: 302 pages, softcover, $10.95
Volume 2: 496 pages, softcover, $12.95
Blacksburg Continuing Education Series
Howard W Sams & Company Inc, 1979.

Z80 Microprocessor Programming and Interfacing is a two-volume series designed to teach the reader how to program and interface the Z80 processor chip. The use of the term *chip* rather than microcomputer is intentional here; this series is very concerned with hardware. Volume one covers how to program the Z80; volume two covers how to use it.

Both volumes are texts intended for use in a laboratory course or for laboratory-based self-study. Each chapter begins with a series of objectives and ends with a series of graduated experiments. The experiments involve both hardware and software development, and stress the trade-offs involved in substituting one for another. Between the experiments and the appendices, much good reference material is included, both hardware and software. Overall, the two volumes make up a very useful text either for class use or for self-study.

There is one glaring problem with both texts, however. All of the experiments assume that the student has one of two single-board computers manufactured by SGS-ATES. This is an Italian company whose products are not widely available in the US, at least from hobbyist sources. Fortunately, almost all of the software experiments can be performed on any Z80-based computer which has either a front panel or a monitor in read-only memory. Many of the hardware experiments can also be performed (with minor changes) on other machines. The exclusive use of this single-board computer along with the consistent use of SGS-ATES data sheets throughout the second volume leads one to believe that the series was sponsored by SGS-ATES. This is all very well, but unfortunately it renders the series useless for self-study by a novice who does not own an SGS-ATES Nanocomputer and who is not knowledgeable enough to make the required changes. On the positive side, full schematic diagrams and software listings are given for the Nanocomputer, which is an admirable little unit, suitable for use in a number of controller-type applications.

Now for a number of more or less random comments. The interfacing section contains the circuitry for a breadboarding station which could be used with most Z80 systems. This plus the listing of a 2 K-byte monitor and the inclusion of quite a few data sheets are some of the little extras in the book. On the negative side, there is no good index to the data sheets, on page 106 the data sheet for a 74LS138 is mistitled 74LS139, and there is only one blank page at the back for notes.

All in all, this is a useful series to have if you want to learn how to use the Z80 for hardware designs. The series will not teach you about program design, and it assumes a certain amount of sophistication if you do not use the particular computer for which the experiments have been written. But it contains the best discussion that I have seen of machine programming (as opposed to assembler) of the Z80, and the clearest discussion of exactly how the device functions when you make it perform various tasks. The two volumes would be ideal for a class, and belong on the shelf of anyone planning to design systems which contain the Z80. ■

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The FORTH Standards Team

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How can a standard be created for a computer language when every programmer freely adds his own procedures, data structures, and compilation methods? This dilemma continually faces the FORTH Standards Team as each user creates extensions to the language as the fundamental act of programming!

The recently published FORTH-79 Standard offers a uniform vehicle for interchange of FORTH programs across all computer architectures and models. Additionally, it provides programmers the ability to communicate with other programmers and host computers, as they ply their craft. FORTH was created by Mr Charles Moore from 1960 thru 1970, to meet his real-world programming needs. The standards team has developed the current standard through three generations, to match increasingly broader requirements.

Why a Standard?

The true cornerstone of standards work is *cost reduction*. This applies to all standards, not just those developed for computer languages. Instead of optimizing the language for each application and computer, we team members accept programs that are a bit slower and a bit bulkier in memory usage. Our reward is less cost for creating and maintaining specific application programs, less cost for personnel training, and less cost for the host operating system itself.

When analyzed in detail, language standards offer five components of cost and efficiency improvement:

- If an application is portable between computers, its cost may be spread over a larger number of installations. Likewise, a standard host system offers a larger potential market.
- A uniform computer language allows programmers to communicate concepts to one another. The concepts may be more efficiently shared if their standard components are clearly known.
- People move from one job to another. Personnel trained at one site are more quickly productive at another site when standard usage exists. It isn't any quicker to learn a standard language dialect, but naturally, standardized skills have a broader marketplace.
- The evaluation time spent for purchased application or system software is reduced if its components are standardized. Only the new elements need to be analyzed.
- If someone does desire a nonstandard system or application, the standard portion provides a known point of departure for documentation of the differences.

About the Author

William Ragsdale settled on FORTH in 1977, after a year-long search for high-level software tools to enhance programmer productivity. He is a graduate of the University of California at Berkeley and is president of a communications company. Bill attended the FORTH-78 Standards Team meeting, created the FORTH Interest Group model of the language, and contributes to FORTH Dimensions, *the FIG Newsletter. He is currently chairman of the FORTH-79 Team.*

The Early History of FORTH Standards

FORTH's professional usage began in 1970 with one programmer, Charles Moore, at NRAO (the National Radio Astronomy Observatory). Soon after that, Elizabeth Rather and others joined him. When FORTH came into use at Kitt Peak National Observatory, the number of users grew even larger: finally the users recognized the need for standardization.

Specifically, as FORTH's usage increased in astronomical research, that user community recognized the need for a common dialect. An ad hoc team within the International Astronomical Union, hosted by Kitt Peak National Observatory, and with Jim Brault as chairman, met in May, 1977. This group produced the document AST.1, a glossary of definitions for the minicomputer versions then in use. Extension levels were outlined, but not detailed, for double-length numbers, floating-point numbers, and system extensions.

The work begun as AST.1 was then carried forward with a series of European meetings, again, in the astronomical-research community. The final meeting was held in Utrecht, The Netherlands, in February, 1978. The attendees were Jim Brault, Phil Hill, Robbie Spruit, Paul Bartholdi, Charles Moore, Elizabeth Rather, Hans Nieuwenhuijzen, and Terrel Miedaner. This group's report FST-780314 became the FORTH-77 standard. It is directed toward word-addressing computers, specifically the Data General Nova, the Hewlett-Packard HP-2100, and the Varian 620.

The standards meeting on Catalina Island, Avalon, California, in October, 1978, found the team expanded to eighteen, and the chairman was Terrel Miedaner of Kitt Peak. A broadened constituency was drawn from the FORTH Users Group based in Europe, FIG (FORTH Interest Group), and FORTH Inc, a company started by Charles Moore.

This meeting was the first that considered byte-addressing computers. Work continuing from FORTH-77 resulted in an increased clarity of word-naming and provided a minimum set of defined words that were collectively more powerful than those of previous standards. However, there were no rules of usage, arithmetic overflow was unspecified, and the byte/word-addressing specification was ambiguous.

The FIG Model

In March, 1979, the FORTH Interest Group published an implementation model of FORTH written in FORTH. This became a test bed for the current standard and was used to test portability of the language. (See the accompanying "FORTH Connotations" text box.) Applications were transported among computers using the Intel 8080, Digital Equipment LSI-11, Motorola 6800, National Semiconductor PACE, MOS Technology 6502 and Texas Instruments 9900 microprocessors. This public-domain research vehicle was most valuable as preparation for the next standards team meeting.

A team charter was proposed and accepted in October, 1979. Member eligibility, responsibilities, and organizational functions were outlined: new members are observers at their first team meeting; they are eligible to join at the next team meeting. Procedural matters are decided by a simple majority, and standards proposals must be accepted by a two-thirds majority.

FORTH-79

A FORTH Standards Team of twenty-six people, with me, William Ragsdale, as chairman, met again at Catalina Island in October of 1979. The general goal was to increase the portability of FORTH programs by language specifications in addition to the current glossary definitions.

Each of the four days of meetings was structured by a morning general session lasting until noon, subteam working sessions until 5:00 PM, and a general session concluding at 6:00 PM. Two evenings had informal subteam meetings (until 1:00 AM). Technical proposals were "captured" on work forms; a total of 120 were presented. These were organized and filtered by the subteams, and formally reviewed by the full standards team. Working documents and all team actions were maintained by secretary Jon Spencer.

Proposal decisions, subteam reports, and draft mark-ups were used by four technical referees to prepare the final-draft standard. Referees Charles Moore, Robbie Spruit, Hans Nieuwenhuijzen, and I presented this final draft before the full team for final acceptance in August, 1980.

Oddities of FORTH

FORTH is an incomplete language—by definition. Each user's program adds new word definitions until all functions demanded by the application exist. (See the "FORTH Connotations" text box.) The programmer specifies the exact procedure for calculating the desired result rather than simply describing that result.

This means that some of the difficult programming is left to the user. Sixteen-bit integer math is standard; some 32-bit primitives and some mixed-mode primitives are provided. However, a greater burden is placed on the programmer, who must create *application-specific* functions. This characteristic is tolerated, even cherished, by FORTH programmers: but who better understands the demands of the application, the application programmer or a distant compiler writer?

Dr C A R Hoare has said that the most difficult problem of language design is deciding what to leave out. The standards team faces the task of selecting a balance between primitive functions and directly usable functions, enabling the user to complete the software tools to solve his application problem. FORTH allows word definitions to be in higher-level form or in machine code. To maintain portability among computers, the language should be defined so the use of machine-languge code can be avoided. Therefore, the provided primitives must be sufficient to solve all problems without use of machine-specific code.

In review, several of the features of FORTH-79 have been pointed out as "novel" for computer-language standards; to those involved in the effort, these features seemed to be natural and necessary. Each of these features was introduced as needed, in response to problems as encountered.

Foremost is the section of *trade-offs*. The FORTH Standards Team members are working FORTH programmers and realize that compromises must be made among their various preferences. The priority of certain language and program characteristics has been formalized for current use and future reference:

1. correctness — most important to a user
2. portability
3. simplicity — most important to FORTH
4. clarity
5. generality
6. execution speed
7. memory compactness
8. compilation speed
9. historical continuity
10. pronounceability
11. teachability

The *pronunciation* of FORTH words must be considered since FORTH allows any ASCII text (without blanks) as definition names. Many of the common words have short names, such as:

! , pronounced "store"
@ , pronounced "fetch"
#S , pronounced "sharp-s"
BLK , pronounced "b-l-k"

and so on.

Each word name that is not directly pronounceable has a standard pronunciation given. There is a commitment from the FORTH Users Group (Europe) that standard words will be spelled in English but that application definitions can be named in any language. Therefore, there will be no need for renaming the standard words

FORTH Connotations

Some English words have specific connotations when referring to FORTH. Here are some examples.

word: Any sequence of ASCII (American Standard Code for Information Interchange) characters (except "return," "rubout," and "blank") terminated with a blank or return. Thus letters, numbers, and punctuation may be used freely to form words. Use of control characters is possible but is frowned upon. The internal representation of "return" is conventionally "null."

definition: The execution procedure assigned to a named word. Definitions begin as source text on a mass storage device and are compiled into the dictionary for execution. Programming consists of creating new definitions from the existing definitions, whether resident within the host FORTH system or defined by the user.

dictionary: When compiled into memory, FORTH word definitions are usually organized into linked lists and further segmented into smaller lists called vocabularies. *Each definition may be located by its word name, for execution or compilation. This dictionary expands as the user adds his own definitions.*

extensibility: The ability to add operators, functions, and data structures that are indistinguishable from those of the host language, both at the compilation and execution levels.

portability: A characteristic that allows a standard FORTH program to run on numerous standard FORTH installations, each having a different host computer.

with non-English equivalents.

Word definitions controlled by the standard have been *given serialized* numeric identifiers. Assigned integers between 100 and 999 will be changed when the definition is functionally altered within future standards. (This has been borrowed from the languages M6 by Doug McIlroy and SAM76 by Claude A R Kagan. See "The SAM76 Language" by Ancelme Roichel, *Dr Dobb's Journal,* volume 3, number 1, 1978, page 18.) No other use of these identifiers is required, although they may be of use for calling library functions and archiving evolutionary changes.

Just as FORTH is extensible, so is its standard. (Refer to the "FORTH Connotations" text box.) An experimental-proposals section is a showcase for anticipated change. Inclusion of these proposals allows testing and refinements, leading to future standards consideration.

Standard System Versus Standard Program

Standards for other contemporary languages generally concern the compiler, not the applications. FORTH-79, however, includes requirements for both a standard system (such as address representation, mathematical overflow, mass-storage access, and execution of standard words) as well as a standard program (such as allowed areas of memory access and rules of use of standard words). A standard program must use standard definitions within the rules of usage, but its production is ultimately the programmer's, not the compiler's, responsibility.

The classical compilation process of high-level languages consists of:

- a syntactical and semantic analysis of correctness of the source code text
- the translation of this text into an executable code form.

In FORTH, program correctness is not the responsibility of the compiler but of the programmer. Since the language and compiler are extensible, new constructs may be introduced at all levels. Therefore, the programmer must work in a responsible manner to decompose his problem into successively smaller components (ie: words). He must define these words as combinations of words from the required-word set; and he must test his new words individually and collectively for program correctness. But as the programmer can extend the compilation process, he may also add to the compile-time and run-time checking. Users are quite grateful that the language gives them the choice of where and when to add execution-time costs.

Much of FORTH's power results from its simplicity and generality. The user may add new compile-time operations as easily as new run-time operations. Traditionally, few resources have been devoted to the detection of compile-time errors. The newer versions tend to increase compile-time checking, and future standards work will reflect this trend.

It is quite correct and compliant with the FORTH-79 standard to offer increased error-checking. The standard expresses a uniform minimum; vendors of standard systems will probably be rated by their customers on compile-time diagnostics, with the higher-quality vendors prospering.

Labeling

Good Housekeeping Magazine and Underwriters' Laboratory Inc have established their own labeling for enforcement of product quality. We hope a series of validation programs will be developed for verification against the FORTH-79 standard. The team has reserved the following labels for their use:

- FORTH-79 Standard
- FORTH-79 Standard Subset
- FORTH-79 Standard with *xxxxx* Standard Extension(s)

where *xxxxx* names the already-standardized extension(s) included in the package.

Future Work

Work is still needed to improve compile-time error detection and text string handling, and to broaden support of input/output devices. Note that these functions are all available on some installations but are so new that standardization is still in process. They can be compiled on top of standard systems, and thus are not necessarily required: instead, such capabilities may be implemented as library functions which are loaded as desired.

FORTH derives its speed by operating very close to machine-code level while presenting to the user an abstract and uniform high-level notation. This balance must be preserved, otherwise performance would drop, causing some users to return to more specialized and nonstandard versions of FORTH.

A research group named FORML (FORTH Modification Laboratory) has begun as a clearinghouse for research areas and future standards material. It coordinates the efforts of regional groups and individuals.

Transportation

We now have the FORTH-79 standard, which is useful and transportable. To the user, the memory space appears as byte-addressed. This imposes some execution-speed reductions on word-addressing computers, but the trade-off was made favoring application portability and simplicity. Except for the usual machine-code definitions, the standard contains all the fundamental elements of FORTH as created by Charles Moore. The quality of the standards team's efforts will be judged by how few disputes are caused by alleged standard programs that do not execute correctly on a vendor's alleged standard system.

The FORTH Standards Team has requested an interlude of at least eighteen months before the next full-team meeting. This should allow updating of the standard and subsequent evaluation. During this period, regional meetings will be held for user comment.

The FORTH-79 standard-specification document is available from the FORTH Interest Group (POB 1105, San Carlos CA 94070) for $10 (surface mail to USA or Canada) or $13 (airmail to all other countries). ■

The FORTH Standard follows the general outline below:

0. Forward
1. Purpose
2. Scope
3. Organization
4. Definition of Terms
5. References
6. Standard System Requirements
7. Compliance and Labeling
8. Usage Requirements
9. Glossary Notation
10. Required Word Set (130 definitions)
11. Extension Word Sets
a. 32-bit Word Set
b. Assembler Word Set
12. Experimental Proposals.

Programming Quickies

A Quiz on Exclusive-OR

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Exchanging the content of two memory locations or registers is a very common operation, and every novice programmer learns that the proper way to do it is not:

$$A \leftarrow B$$
$$B \leftarrow A$$

Every programming book for the beginner tells us that the proper way is:

$$T \leftarrow A$$
$$A \leftarrow B$$
$$B \leftarrow T$$

This is fine except that an extra register, T, is required. Since a number of 16-bit machines have register-to-register arithmetic and logical operations, can we then make use of these to exchange the content of two registers with three operations and without involving an extra register?

Another related problem concerns the pointers of a doubly-linked list. A number of records are linked together to form a chain. In each record there are two pointers, a forward pointer pointing to the next record, and a backward pointer pointing to the previous record. Therefore, we can scan the chain from record to record in either direction. If there is enough room in the record for only one pointer, can we still have a doubly-linked list?

Solutions

The first problem is to exchange the contents of two registers without involving a third register. The solution, as the user can guess from the title, involves the exclusive-OR operation. Let us first review some of the properties of the exclusive-OR function, $\oplus$:

$$A \oplus (A \oplus B) = B$$
$$B \oplus (A \oplus B) = A$$
$$A \oplus B = B \oplus A$$

Now we can make use of the above identities to exchange the content of two registers, A and B:

$$A \leftarrow A \oplus B$$
$$B \leftarrow B \oplus A$$
$$A \leftarrow A \oplus B$$

To see how it works, let A_0 and B_0 be the original contents of registers A and B respectively. After the first step the content of A is $A_0 \oplus B_0$. After the second step the content of B is $B_0 \oplus (A_0 \oplus B_0)$, the $(A_0 \oplus B_0)$ now being the content of A. Since $B_0 \oplus (A_0 \oplus B_0) = A_0$, the original content of A has been transferred to B. After the third step the content of A will become $(A_0 \oplus B_0) \oplus A_0$, since the contents of A and B after the first two steps are $A_0 \oplus B_0$ and A_0. Since $(A_0 \oplus B_0) \oplus A_0 = B_0$, the original content of B is transferred to A.

The second problem is to save a pointer in a doubly-linked list. When we access a record in a doubly-linked list, we get the address of the record by scanning the linked list in one direction or the other, therefore we know either its predecessor or its successor, and it can be used as the forward pointer (FP) or the backward pointer (BP). If we store (FP ⊕ BP) in the record, we can find the other unknown pointer by:

$$FP = BP \oplus (FP \oplus BP)$$
$$BP = FP \oplus (FP \oplus BP)$$

To use this scheme, we need to use the addresses of two successive records as the header, otherwise we can never access more than one record.

The Towers of Hanoi in BASIC09

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Steven Switzer's article "The Towers of Hanoi" (March 1980 BYTE, page 240) brought back fond memories. A Towers of Hanoi game has been available as a plastic toy for a number of years, and I can remember spending hours playing the game as a child. Mr Switzer's analysis of the Towers of Hanoi solution is both elegant and correct, but he is unfortunately hampered in using a nonrecursive BASIC to demonstrate a recursive algorithm. The algorithm is simple (once you know it!), but his BASIC gets in the way.

Listing 1 shows the advantage of expressing the Towers of Hanoi algorithm in a modern, structured, high-level language. The language used in BASIC09, a structured BASIC for the Motorola MC6809 microprocessor. Notice that the solution algorithm is unchanged from the original article; the high-level language allows the programmer to express the algorithm in a more natural manner. The numbers on the left of listing 1 are not line numbers (although line numbers can be used). Instead, they represent the I-code location for the start of each line (relative to the start of the procedure). [*BASIC09 compiles into a machine language for an ideal machine, much like the p-code of UCSD Pascal; this allows the language to be more easily transported to other microprocessors....*GW] The PARAM statement describes the passage of parameters from the calling routine, while RUN calls a procedure by name.

A number of features of BASIC09 offer advantages to the programmer. The BASIC09 development environment is multiprocedure oriented; procedures are called by name, and the call may include parameters. Procedures are easily modified and debugged: a powerful editor allows global changes; the TRACE mode displays each program line before execution and prints out the result of any expression evaluation. Control structures (*IF...THEN...[ELSE...]...ENDIF, FOR...NEXT, REPEAT...UNTIL, WHILE...DO...ENDWHILE, LOOP...ENDLOOP, EXITIF...THEN...ENDEXIT*, etc) are fully bracketed and have unique closure elements. All loops are automatically indented in the listing, and all keywords are automatically capitalized. Long identifiers allow the programmer to select names that imply the use of the variable or procedure, making the system easy to understand without constant reference to documentation. And variables are always local to a particular procedure invocation, allowing the language to directly express a recursive algorithm, such as Towers of Hanoi.

Listing 2 shows the results of executing Towers of Hanoi in BASIC09. By including a parameter in the procedure call which is the number of disks to be moved, the special case of moving one disk is easily identified. (If the task is to move the top four disks from left to right, the solution is to move the top three to the center, move the fourth, then move the three from the center onto the fourth.) Furthermore, that same number can be used to identify the disk to be moved: number 1 is the smallest. The spindle positions are sent to the procedure as string parameters so that letters or names may be used for the spindles.

Listing 1: *The algorithm for solving the Towers of Hanoi problem expressed recursively in BASIC09.*

```
PROCEDURE hanoi
0000        PARAM n:INTEGER, from,to_,other.STRING[8]
001A
001B        IF n=1 THEN
0027          PRINT "move # "; n, " from "; from, " to ", to_
004E        ELSE
0052          RUN hanoi(n-1,from,other,to_)
006D          PRINT "move # "; n, " from "; from; " to ", to_
0094          RUN hanoi(n-1,other,to_,from)
00AF        ENDIF
00B1
00B2        END
READY
B
```

Listing 2: *A sample run of the Towers of Hanoi algorithm shown in listing 1. The parameters following "run hanoi" are the number of disks to be moved and the position of the spindles.*

```
B: run hanoi(4,"l","r","c")
move # 1 from l to c
move # 2 from l to r
move # 1 from c to r
move # 3 from l to c
move # 1 from r to l
move # 2 from r to c
move # 1 from l to c
move # 4 from l to r
move # 1 from c to r
move # 2 from c to l
move # 1 from r to l
move # 3 from c to r
move # 1 from l to c
move # 2 from l to r
move # 1 from c to r
READY
B:
```

Most of those who criticize BASIC should understand where programming difficulties arise. Even BASIC is amenable to high-level tasks, as long as the particular BASIC implementation involved includes modern, high-level, programming features. A similar program could, of course, be written in Pascal. When compared to "backward BASIC," the result of using BASIC09 is an easier expression of the algorithm; clearer to the computer, and, most importantly, clearer to people. ■

The Age of Affordable Per

In 1978 Ohio Scientific introduced a revolutionary new low cost computer — the Superboard II. This computer provides all important personal computer features on a single board at a cost of under $300. The Superboard II received rave reviews by microcomputer experts such as:

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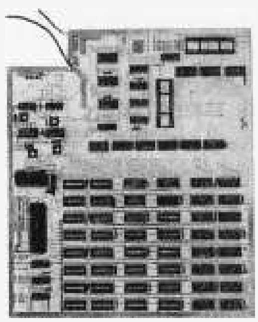
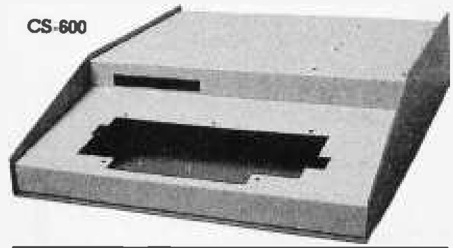


610 Board



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The 6502 Gets Microprogrammable Instructions

Dennette A Harrod
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Rochester NY 14604

"Every programmer is part of a collective mind, and progress demands that he educate and be educated by others." So states H T Gordon in a letter published in the October 1977 issue of *Dr Dobbs Journal of Computer Calisthenics and Orthodontia*.

In this article I shall attempt to educate others by detailing a hardware approach to adding sixty-four user-defined instructions to the MOS Technology 6502 microprocessor. The 6502 device is used in the Apple II, PET, KIM-1, SYM-1, Rockwell, Ohio Scientific, and Atari microcomputers to name a few.

My own research concerning 6502 operation codes (ie: op codes) has closely paralleled the efforts of Dr Gordon (see his Technical Forum article "The XF and X7 Instructions of the MOS Technology 6502" December 1977 BYTE, page 72). Close investigation reveals that sixty-four of the unimplemented op codes can be detected by a simple circuit such as that shown in figure 1. Unimplemented op codes are any of the op codes with the two least significant bits set to 1.

About the Author

Dennette A Harrod is a systems programmer at Xerox Corp in the Computer Aided Drafting (CAD) Department.

A similar circuit, by C W Moser ("Add a Trap Vector for Unimplemented Op Codes" *Dr Dobbs Journal of Computer Calisthenics and Orthodontia* January 1979, volume 4, issue 1, pages 32 thru 34) can be used to detect *all* undefined op codes, but it requires a programmable read-only memory programmer and does not appear to be as cost-effective in its use of components. My circuit uses only three integrated circuits.

Simple Hardware Appendage

The circuit in figure 1 is deceptively simple. Its purpose is to cause the 6502 to receive an interrupt signal whenever it attempts to execute one of the sixty-four undefined op codes in which the right nybble (ie: 4-bit segment) has a hexadecimal value of 3, 7, B, or F. (The left nybble can have any value.) These values correspond to the situation where both of the two least significant bits are high.

The software interrupt-service routine then examines the instruction and jumps to a routine to perform the operation specified by that code. This facility enables the user to add instructions not available on the 6502 as supplied. With certain added instructions, 16-bit arithmetic and logical operations can be performed, or string comparison and move operations may be implemented. These added instructions are called *virtual operation codes*, or *v-codes*.

When the 6502 is in the op-code-fetch phase of the instruction cycle, the normally low SYNC line goes high. When the processor attempts to fetch an op code which has both of the two least significant bits set to 1, the three-input NAND gate (IC2a, 74LS10) output goes low. (Note: one of the NAND gates on the 74LS10 is wired as an inverter.) As a result, the data-bus transceiver (IC4, 74LS245) is disabled, and the 6502 never receives the op code. Instead, a buffer (IC3, 74LS244) is enabled, forcing all 0 values onto the data-bus lines by pulling them to ground potential.

The net effect is that the 6502 thinks it fetched a BRK (break) instruction (hexadecimal 00). The BRK instruction causes the microprocessor to go through an interrupt sequence under program control.

Three things happen when the 6502 executes a BRK instruction.

- The program counter (PC) is incremented by 2 and is pushed onto the stack (thus the processor treats BRK as a two-byte instruction).
- The BREAK bit (B) in the processor status word (PSW) is set to 1, and the PSW is pushed onto the stack.
- The 6502 transfers control to the

Number	Type	+5 V	GND
IC1	6502		
IC2	74LS10	14	7
IC3	74LS244	20	10
IC4	74LS245	20	10

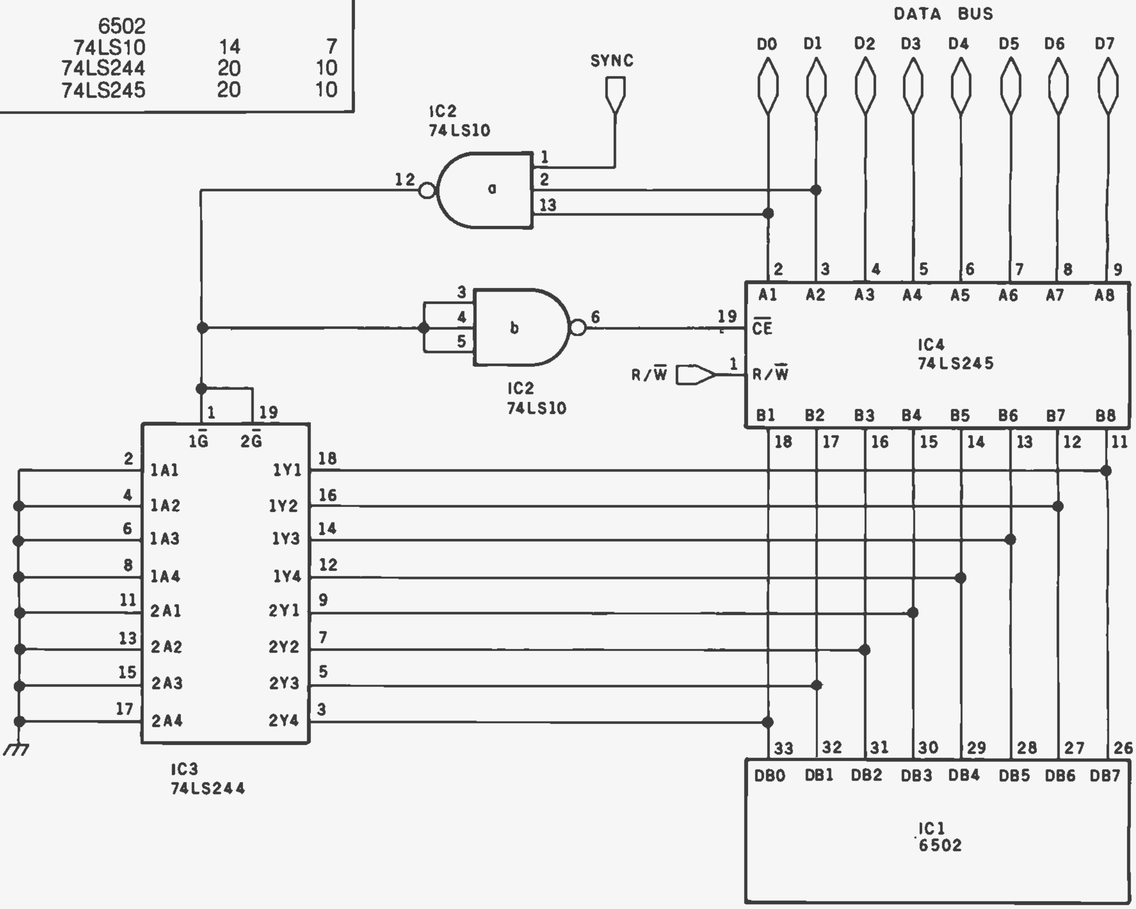

Figure 1: *Schematic diagram of a circuit that forces all lines on the data bus into a logic 0 (ie: low) condition whenever the 6502 attempts to fetch an operation code with the two least significant bits both set to 1. The low-order hexadecimal digit of such an op code will be 3, 7, B, or F. When all data bus lines are forced low, the 6502 executes the BRK (break) instruction, for which the op code is 00. The BRK instruction causes the processor to go through an interrupt sequence under program control.*

address stored in the highest locations in memory (FFFE and FFFF), the IRQ interrupt vector. This address must indicate the starting location of the interrupt-service routine.

Software Action

The first thing the interrupt-service routine must do is determine whether it was invoked by a hardware or a software interrupt. This is accomplished by examining the B bit in the processor status word. Having determined that it was a software interrupt (B=1), the program uses the stack pointer as an index to get the return address off of the stack. This is accomplished with the help of the TSX instruction to transfer the stack pointer to the X index register. Then it can load the accumulator using the indirect address mode and examine the actual instruction that caused the interrupt. Since the processor is not fetching the op code for *execution*, the circuit of figure 1 does not interfere.

Once the interrupt-service routine has established that it was not an actual BRK instruction that caused the interrupt, the v-code can be used as an index into a table of addresses of subroutines. There is one entry in the table for each of the v-codes. The subroutine performs the v-code operation.

By using the byte following the v-code as an additional instruction byte to be decoded by the v-code executing subroutine, each v-code can act as a gateway to 256 more virtual instructions.

Do not be intimidated by the prospect of over 16,000 user-defined instructions. Instead, welcome the ability to microprogram any or all of your favorite machine architectures into the virtual machine now available.

Instruction Characteristics

At this point I should probably clarify a poorly documented fact about the 6502 BRK instruction. One reason the processor treats BRK as a 2-byte instruction is that the BRK can be followed by a 1-byte code to be interpreted by the interrupt-service routine, much the same way that a supervisor call (SVC) instruction works in the IBM 360/370 computers. Using the circuit of figure 1 enables you to save one byte of code by eliminating the BRK instruction itself. This allows the interrupt-service routine and v-code subroutine to access 2 bytes of user data (the v-code and a data byte) without having to adjust the return address on the stack.

Taking a tip from Steve Wozniak (see "SWEET16: The 6502 Dream Machine" November 1977 BYTE, page 150), you can reserve 16 bytes on page 0 of memory to serve as eight 16-bit registers, each of which may be used to contain either data or the address of data. The byte following the v-code can then be divided into two 4-bit nybbles to specify *source* and *destination* registers for the virtual operation. The low-order 3 bits of the nybble contain the register number (0 thru 7), while the high bit indicates direct or indirect mode. When the high-order bit has a value of 0, it means the register contains the *data*; a value of 1 means the register contains the *address* of the data.

If you wish, you can use 2 bytes for source and destination information, in which case 1 nybble of each byte can be used as an index-pointer (meaning it specifies which register to use as an index register). However, this requires the user to assume responsibility for fixing up the return address from the interrupt. On the other hand, if you use a real BRK instruction followed by a v-code and one or more data-bytes, the return address has to be manipulated anyway.

Hardware Interrupt Vectors

If you are truly ambitious, a circuit based on one by Yogesh M Gupta ("True Confessions: How I Relate to KIM" August 1976 BYTE, page 44) intended for the vectoring of hardware interrupts, which the 6502 lacks, can be modified and added to the circuit in figure 1 to provide hardware vectoring of the software interrupts. Gupta's circuit generates vectored addresses that are 4 bytes apart. This is a compromise. All you really need is 3 bytes to contain a JMP op code and a 16-bit destination address, but hardware-generated addresses are most conveniently generated in positive powers of 2.

I suggest that the addresses from such a device be 16 bytes apart, so that the service routines can be entered with three assumptions:

- The routine was called by a jump to subroutine (JSR) instruction, which is not strictly true, but this will be clarified in a moment.
- All of the 6502 registers are stored on the stack, directly beneath the return address, so that any register may be used with impunity.
- The routine can exit from anywhere by a return from subroutine (RTS) instruction, and all registers will be restored to the pre-interrupt state before a return from interrupt (RTI) instruction is executed.

Listing 1: *Example of an interrupt-service routine. It saves the contents of the 6502 registers on the stack, calls a subroutine (by JSR) to operate the interrupting device, restores the registers, and finally returns to the interrupted task. Some instruction mnemonics are from a macro-assembler of the author's own design. For example, the PSH X instruction mnemonic causes the macro-assembler to generate two machine instructions, TXA and PHA.*

```
        ABCD      SRVRTN   EQU    $ABCD

XX00                       ORG    $XX00
        XX00      ENTRY    EQU    .
XX00    48                 PSH    A          ;SAVE REGISTERS
XX01    8A 48              PSH    X
XX03    98 48              PSH    Y
XX05    20 CD AB           JSR    SRVRTN     ;CALL SERVICE ROUTINE
XX08    68 A8              PUL    Y          ;RESTORE REGISTERS
XX0A    68 AA              PUL    X
XX0C    68                 PUL    A
XX0D    40                 RTI               ;RETURN FROM INTERRUPT
        XX0E               END    ENTRY
```

Listing 2: *An interrupt-service routine that uses the* soft-coded vector *technique of subroutine calling. To call a subroutine, this routine places a return address on the 6502 stack, and then branches to the subroutine by executing a JMP instruction in the indirect addressing mode. The subroutine can return normally to this calling routine by executing an RTS instruction. This procedure compensates for the inability of the 6502 processor to execute the JSR instruction using the indirect addressing mode.*

```
YY00                       ORG    $YY00
        YY00      SRVADR   EQU    .
        ABCD      SRVRTN   EQU    $ABCD
YY00    CD AB              ADR    SRVRTN

XX00                       ORG    $XX00
        XX00      ENTRY    EQU    .
XX00    48                 PSH    A          ;SAVE REGISTERS
XX01    8A 48              PSH    X
XX03    98 48              PSH    Y
XX05    20 8B XX           JRS    JMPAT      ;SIMULATE JSR @ADDR
XX08    4C 00 ZZ           JMP    COMRTI     ;GOTO REGISTER RESTORE
        XX0B      JMPAT    EQU    .
XX0B    6C 00 YY           JMP    @SRVADR    ;GOTO SERVICE ROUTINE
        XX0E               END    ENTRY

ZZ00                       ORG    $ZZ00
        ZZ00      COMRTI   EQU    .          ;COMMON RTI ROUTINE
ZZ00    68 A8              PUL    Y          ;RESTORE REGISTERS
ZZ02    68 AA              PUL    X
ZZ04    68                 PUL    A
ZZ05    40                 RTI               ;RETURN FROM INTERRUPT
        XX06               END    COMRTI
```

Interrupt Service Routines

The program of listing 1 is an example of how to service an interrupt. It first saves the contents of the 6502 registers on the stack. Next, it calls a subroutine to service the interrupt, restores the registers, and finally returns to the interrupted task. My example is for a 6502, but the instruction mnemonics are for a macro-assembler of my own design; for example, the push X index register on stack (PUSH X) mnemonic generates two instructions: transfer X to register A (TXA) and push A onto stack (PHA).

The program in listing 2 also saves the registers on the stack, but instead of calling a subroutine in the normal fashion, this program places a return address on the stack. It then executes a jump (JMP) instruction in the indirect addressing mode to reach the subroutine. This means that the program in listing 2 will look in a location in memory to find the address of the subroutine to jump to. The implicit assumption is made that the subroutine will exit with an RTS instruction. Thus, the subroutine thinks it was entered by a JSR instruction, when actually, the way there was wormed by a circuitous path.

This method for simulating use of the JSR instruction in indirect mode was developed by Tom Pittman, and I thank him for suggesting this *soft-coded vector* technique.

Benefits of Indirect-Mode Entry

There are several good reasons for entering an interrupt-service routine (or any monitor-service routine, for that matter) with a JMP indirect rather than by a JSR instruction. The first is that the choice of routine to service a given interrupt can be easily changed. Instead of being forced to use a particular routine in response to a particular interrupt, you need alter only the address value contained in the JMP-indirect vector location, which can be located in programmable memory. Thus, a string of characters to any of several different peripheral devices can be output using the same microcoded v-code. Simply place the starting address of the desired device-driver routine in the appropriate vector location.

Another reason is that if the locations of service routines are to be changed (perhaps because of additions that make a routine too big for the space it used to occupy), only the entry in the vector address table need be updated. The vector address table can be stored in an inexpensive 256-byte programmable read-only memory. Should the need arise, it is much easier to replace the 256-byte device containing the table than to find all references to a routine in a 2,048-byte programmable read-only memory, change them, and burn a new 2 K-byte device.

The reason for having each routine utilize a common return sequence is that the user may desire to have classes of routines which all need different sets of common operations done before returning to the calling routine. Such an operation could be to transfer the saved register values from the stack into the registers before returning. It may also be used to check if completion of an interrupt service (or v-code instruction) should reset a timer/counter or initiate some other action before truly returning to the pre-interrupt state.

Other Ideas

A truly innovative approach, and one that saves software overhead at the cost of more circuitry, is to *latch* the v-code, using the same circuit that detects the v-code, so that when the 6502 attempts to fetch the IRQ vector address from hexadecimal locations FFFE and FFFF, it gets an address that has been stored in a 128 by 8 programmable read-only memory. This approach, while limited in its flexibility, is ideally suited to "black box" or turnkey systems, where it is assumed that the end user has no desire to know (let alone alter) the internal operations of the machine.

I have set forth these ideas to enlighten my fellow computer experimenters. I owe a debt to the authors of the other articles I have mentioned; without their work, I could not have completely developed the ideas discussed here. I assume that many of you will improve on my work. I merely ask that you write to me and keep me informed of your progress. ■

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Vector Graphics for Raster Displays

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Many personal computers on the market today use raster graphics displays. These consist of devices that display a rectangular matrix of points (actually small rectangles) on a standard raster scan video monitor. The points are stored in a memory, which can be accessed by a computer. Plotting random points is easy, but there is no built-in provision for plotting line segments (vectors). This article describes a method for solving that problem.

In a video monitor, the electron beam moves across the screen in a fixed pattern called a *raster*. This is different from a true X,Y display (eg: an oscilloscope using horizontal and vertical inputs), where the position of the electron beam is under user control. To keep these types of display separate, I'll call the first a *raster* display.

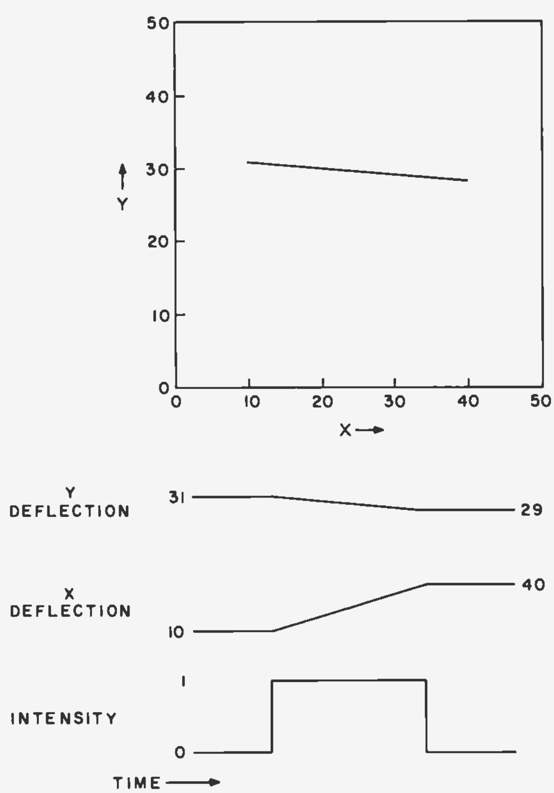

Figure 1: Example of plotting segment from (10,31) to (40,29) on an X, Y display. Note the simple waveforms; we have full control over X and Y deflections.

Neither X,Y nor raster display has trouble plotting points on the screen, but the X,Y display can plot line segments much more easily than a raster display. All the X,Y display has to do is move the beam position from one endpoint (the origin) to the other endpoint (the endpoint) in a linear path (see figure 1). When a line is to be drawn on the screen, the beam is intensified during this motion, leaving a bright trail on the screen. In contrast, the raster display has no control over the beam's position, so it must intensify the beam at the right points on the raster when the beam gets there (see figure 2). The raster display's data is stored in memory, so it is necessary to set the bits in memory corresponding to the intersections of the desired vector and the raster.

Plotting Vectors

There are many methods for plotting a vector into a point matrix. The one which most often comes to mind is computing the slope of the line and using a similar triangles method. Trigonometric methods exist. None of these are very good for a small computer, as many slow multiplications and divisions are needed. We would like a method which avoids such operations. Such a method follows.

It is easy to plot a vector when the endpoints are the same point. We simply plot a point. If the endpoints are not the same, divide the line in half (by computing the midpoint), save one half, and work with the other. This new line is half

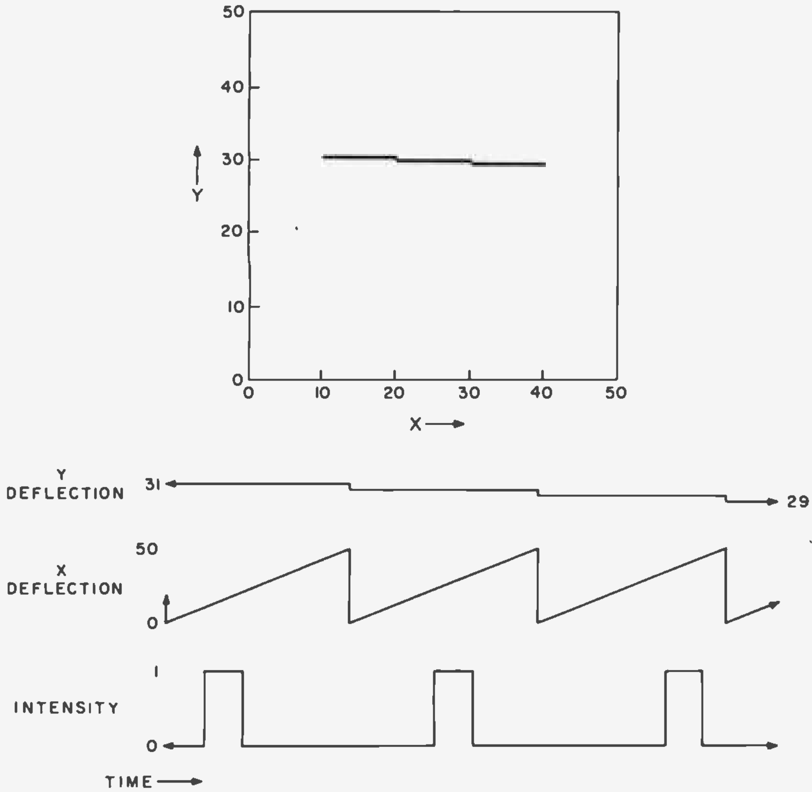

Figure 2: Example of plotting segment from (10,31) to (40,29) on a raster display. Since we have no control over the X and Y deflections, the intensity waveform is complicated. Also note the digitizing on the output display.

as long as the original. Repeat the last step until the vector becomes a point (this *will* happen because integer arithmetic is used). This point can be plotted. Then get the last segment stored and work with it. Eventually all the segments will be plotted! Figure 3 shows the first few steps of this process.

The only arithmetic done is for computing the midpoints. Storage of segments to be worked on later is done on a stack, so that the most recently stored segment will be worked on next. The flowchart in figure 4 describes the algorithm in more detail.

An example of plotting a one-dimensional line segment is given as table 1 to clarify the procedure. Everything following involves two dimensions, although the method is valid for any number of dimensions.

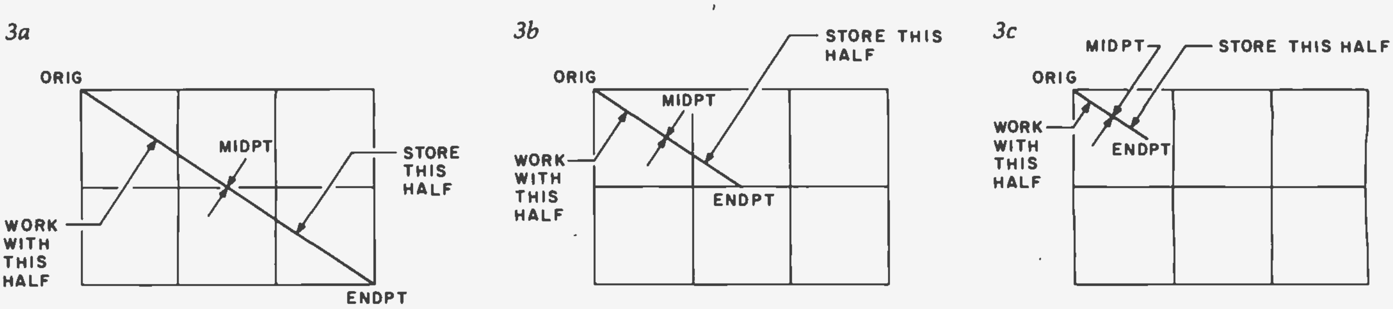

Figure 3: Example of plotting a vector using the method described in text. First the original segment is divided into two parts as in figure 3a. Then a second division is performed as in 3b. The third division (3c) produces a very short segment. Note how quickly a short segment is created. Recursive application of this procedure can be used to plot every point on the line, using a stack oriented algorithm shown in figure 4.

Midpoints

The midpoint is that point which divides a line segment into two equal segments. It is easy to compute. If a line segment's endpoints are (X_1, Y_1) and (X_2, Y_2) in Cartesian coordinates, then the midpoint is ($[X_1+X_2]/2$, $[Y_1+Y_2]/2$), that is, each coordinate is the average of each of the endpoints' coordinates. This is easy to do on a computer; division by 2 is simply a shift right, dropping the low bit into the "bit bucket."

There is a subtle problem with computing the midpoint, however. Note that the midpoint is pushed onto the stack *and* assigned to the endpoint, so that it is plotted *twice*. We must be careful how we compute the midpoint else the program may enter an infinite loop.

A solution is as follows: we compute two midpoints, one where the average is rounded down (truncated), and one where it is rounded up. For each component (X or Y), the higher average is paired with the greater of the endpoints, the lower with the lesser. Thus, if the origin's X component is less than the endpoint's, then the low average is assigned to the endpoint (see figure 4) while the average plus 1 is pushed onto the stack. Of course, if a component of one endpoint is the same number *m* as that component of the other endpoint, then the component of the midpoint is simply *m*.

Software Implementation

The problems of storage of coordinates, stack operations, and midpoint handling must be solved to implement the algorithm. These respective problems were solved for the 8080 processor as described below.

- *Storage of coordinates.* I chose to store one coordinate per byte. This allows greater use of registers, which increases speed. The assignment of registers is as follows:

D	=	ORIG.X	(origin's X coordinate)
E	=	ORIG.Y	
B	=	ENDPT.X	(endpoint's X coordinate)
C	=	ENDPT.Y	
H	=	MIDPT.X	(midpoint's X coordinate)
L	=	MIDPT.Y	

Since each register can hold eight bits, this implementation can handle raster arrays only up to 256 by 256 points. This

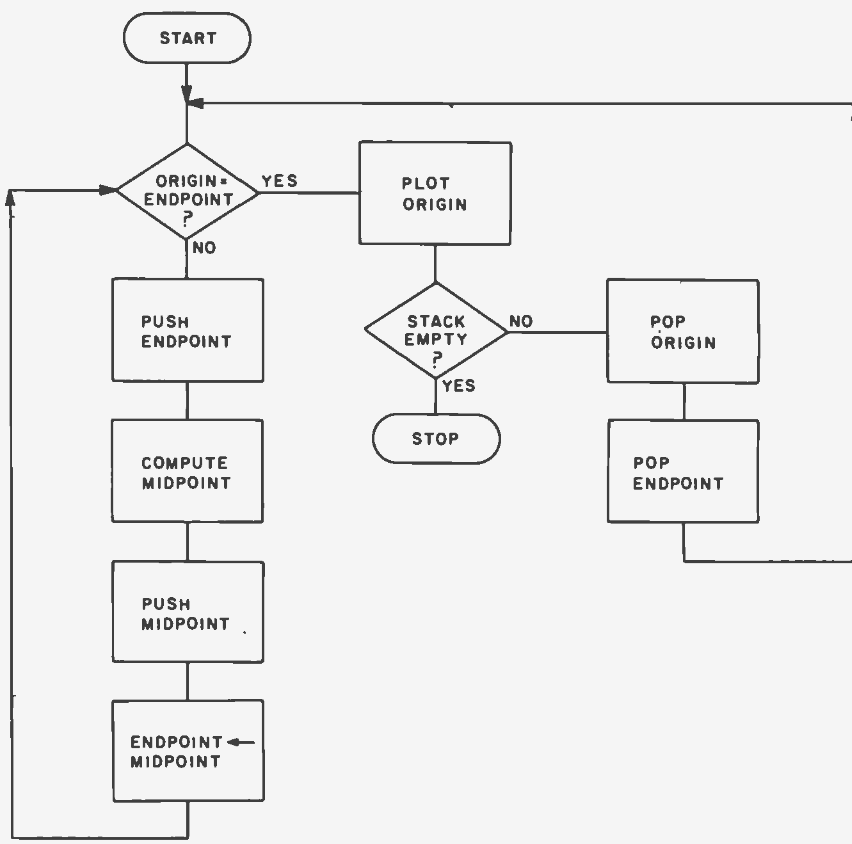

Figure 4: Flowchart for plotting a line segment. This flowchart assumes that integer arithmetic will be used, so that an exact "origin = endpoint" condition will obtain to terminate the algorithm's inner loop.

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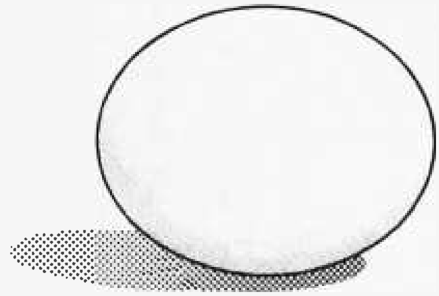

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ORIGIN	ENDPOINT	MIDPOINT	Contents of Stack	Commentary
5	13			ORIG ≠ ENDPT.
5	13		13	Push ENDPT.
5	13	9	13	Compute MIDPT.
5	13	9	13 10	Push MIDPT + 1.
5	9		13 10	ENDPT: = MIDPT.
5	9	7	13 10 9	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
5	7		13 10 9 8	Push MIDPT + 1; ENDPT: =MIDPT.
5	7	6	13 10 9 8 7	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
5	6		13 10 9 8 7 7	Push MIDPT + 1; ENDPT: = MIDPT.
5	6	5	13 10 9 8 7 7 6	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
5	5		13 10 9 8 7 7 6 6	Push MIDPT + 1; ENDPT: = MIDPT.
5	5 *		13 10 9 8 7 7 6 6	Plot 5.
6	6		13 10 9 8 7 7	Pop ORIG, ENDPT.
6	6 *		13 10 9 8 7 7	Plot 6.
7	7		13 10 9 8	Pop DRIG, ENDPT.
7	7 *		13 10 9 8	Plot 7.
8	9		13 10	Pop ORIG, ENDPT.
8	9	8	13 10 9	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
8	8		13 10 9 9	Push MIDPT + 1; ENDPT: = MIDPT.
8	8 *		13 10 9 9	Plot 8.
9	9		13 10	Pop ORIG, ENDPT.
9	9 *		13 10	Plot 9.
10	13			Pop ORIG, ENDPT.
10	13	11	13	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
10	11		13 12	Push MIDPT + 1; ENDPT: = MIDPT.
10	11	10	13 12 11	DRIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
10	10		13 12 11 11	Push MIDPT + 1; ENDPT: = MIDPT.
10	10 *		13 12 11 11	Plot 10.
11	11		13 12	Pop ORIG, ENDPT.
11	11 *		13 12	Plot 11.
12	13			Pop ORIG, ENDPT.
12	13	12	13	ORIG ≠ ENDPT; Push ENDPT; Compute MIDPT.
12	12		13 13	Push MIDPT + 1; ENDPT: = MIDPT.
12	12 *		13 13	Plot 12.
13	13			Pop ORIG, ENDPT.
13	13 *			Plot 13. Stack Empty, end of algorithm.

*ORIG = ENDPT condition is true.

Table 1: An example of plotting a one-dimensional line segment using the algorithm of figure 4. The points are plotted in the order: 5, 6, 7, 8, 9, 10, 11, 12, 13. The maximum depth of the stack is eight.

gives excellent resolution on a small display. The next step up in dimensions complicates this program by an order of magnitude; it would be better to use a 16 bit processor.

- *Stack operations.* On the 8080, only register pairs can be pushed or popped, which is the reason for the HL midpoint register pair. It acts as a buffer to the stack. The hardest part of stack operations is detecting stack empty, as there is no compare stack pointer instruction. The most efficient way is to push a stack empty flag, hexadecimal 0000 or FFFF, and test for it on pop operations. If such a method is used, the user must be absolutely sure that the flag code is never pushed as an actual datum, or the program will "bomb." (Any program which makes large use of the stack runs the risk of wiping out all writable memory, so be careful!) This implementation uses 0000 as the flag and makes sure there are no problems at the beginning of the program. If the program is used for a smaller matrix, then simplifications can be made by pushing FFFF instead.

- *Midpoint handling:* Choosing the right midpoint to increment involves comparing the coordinates. This is not something we want to do each time (waste of time), and we don't have to, since the method preserves the order of the endpoints. (IF ORIG.X < ENDPT.X at the beginning, it will stay that way throughout the algorithm.) What we do is as follows:

(1) Make sure ORIG.X is less than ENDPT.X, switching them if necessary. Then we always increment the MIDPT.X pushed onto the stack.
(2) If ORIG.X is equal to ENDPT.X, make sure ORIG.Y is not greater than ENDPT.Y (This insures that 0000 is not pushed on the stack as a piece of data.)
(3) If ORIG.Y is less than ENDPT.Y, then increment the midpoint pushed onto the stack, else increment the midpoint to be assigned to ENDPT.Y. This last operation can be done by modifying one instruction (a bad technique) or by duplicating most of the code (a waste of space).

Listing 1 is 8080 subroutine VECTOR for plotting a line segment between two endpoints. The points are passed through the DE and HL register pairs where D and H are X components and E and L are Y components. The contents of registers A, B, and C are destroyed.

The first two instructions initialize the stack so we can tell when it is empty. Hexadecimal 0000 on the top means the stack is empty. The next eight instructions are used to insure that DE is less than HL, so that it is easy to compute MIDPT.X. Then BC is loaded from HL so as to free HL for the next step.

The next step sets up the midpoint handling for the Y coordinates. Memory location INRAL can have one of two instructions in it: INR A if E < C, or INR C if E > C. Again this is to make it easy to compute midpoints. Instruction modification is a poor technique, as programs become nonreentrant, unable to be stored in read only memory, and nondebuggable, but it is used here to save space. It is possible to get rid of this step by duplicating the rest of the subroutine.

The rest of the program plots according to the algorithm. DE is the origin, BC the endpoint, and HL the midpoint. The code is simply a realization of the flowchart in figure 4. Note the method for detecting 0000 on the top of the stack.

PLOT is a subroutine for plotting a point on your graphics interface. X is passed through B and D, Y through C and E. All registers may be destroyed by your PLOT subroutine (you don't have to save any). PLOT is the only part of VECTOR which is device dependent (within

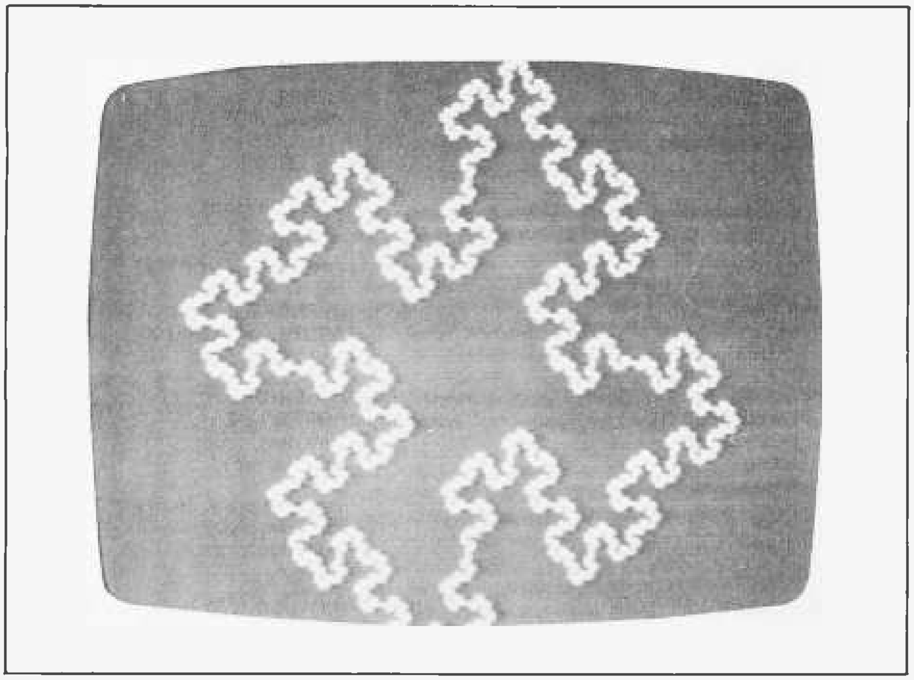

Photo 1: Example output using the line drawing algorithms presented in listing 1.

```
Label         Mnemonic                     Commentary

VECTOR:   LXI    B,0000H        ;Push stack empty flag.
          PUSH   B
          MOV    A,D            ;Make DE less than HL.
          CMP    H
          JC     NOXG
          JNZ    XG
          MOV    A,E
          CMP    L
          JC     NOXG
XG:       XCHG                  ;Exchange HL with DE if necessary.
NOXG:     MOV    B,H            ;BC: = HL.
          MOV    C,L
          LXI    H,INRAL        ;point to instruction INRAL.
          MVI    M,3CH          ;Make INRAL the instruction "INR A".
          MOV    A,E            ;If E less than C
          CMP    C
          JC     LOOP           ;Then leave INRAL alone
          MVI    M,0CH          ;Else change INRAL to the instruction "INR C".

;ORIGIN = DE
;ENDPT = BC
;MIDPT = HL

LOOP:     MOV    A,D            ;If ORIG.X ≠ ENDPT.X.
          CMP    B
          JZ     EQX
          PUSH   B              ;Then (Push ENDPT
          ADD    B              ;          compute MIDPT.X
          RAR
          MOV    B,A            ;          ENDPT.X: = MIDPT.X
          INR    A              ;          Adjust midpoint:
          MOV    H,A            ;          MIDPT.X: = MIDPT.X+1).

          MOV    A,E            ;If ORIG.Y ≠ ENDPT.Y
          CMP    C
          JZ     EQY
NEQY:     ADD    C              ;Then (Compute MIDPT.Y
          RAR
          MOV    C,A            ;          ENDPT.Y: = MIDPT.Y
INRAL:    INR    A              ;          Adjust MIDPT.Y).
EQY:      MOV    L,A
                                ;If ORIGIN ≠ ENDPT in general
          PUSH   H              ;Then (push MIDPT
          JMP    LOOP           ;          continue loop).

EQX:      MOV    A,E            ;If ORIG.X = ENDPT.X
          CMP    C              ;     and ORIG.Y ≠ ENDPT.Y
          JZ     EQXY
          PUSH   B              ;Then (push ENDPT
          MOV    H,D            ;          MIDPT.X: =ORIG.X
          JMP    NEQY           ;          treat as above).

                                ;If ORIGIN = ENDPT
EQXY:     CALL   PLOT           ;then (plot ORIGIN
          POP    D              ;          pop new origin
          MOV    A,D            ;          stack empty?
          ORA    E
          RZ                    ;          return if stack empty.
          POP    B                        pop new ENDPT
          JMP    LOOP           ;          continue loop).
```

Listing 1: Subroutine VECTOR plots a line segment between two points. Point number 1 is stored in register pair DE and point number 2 is stored in register pair HL. The contents of registers A, B, and C are destroyed.

the 256 by 256 limit). PLOT can use any coordinate system: (0, 0) can be in the center, any corner, etc. VECTOR "doesn't care" as long as it is rectangular. A sample subroutine PLOT for the Polymorphics Video Board is included as listing 2.

How much stack space does this program take? Since we are pushing things from all over the place onto the stack, it seems considerable at first glance. However, this is not the case. If your vector has a length of 256, then it only takes eight midpoint operations to reduce its length to 1, so we only need about that many segments on the stack. Each segment takes four bytes, so we only need about 32 bytes for the stack (give it a little more). This is a small price to pay in storage for a large benefit in program efficiency.

Another use of this program (other than a raster display) might be to drive an X,Y display or a plotter. All you have

Label	Mnemonic		Commentary
PLOT:	XRA	A	;Clear carry.
	MOV	A,D	;Get X.
	RAR		;Divide X by 2 to get horizontal character position.
	MOV	L,A	;Store in L.
	SBB	A	;Get remainder (R).
	MOV	D,A	;D: =0 if R=0; D: =FFH if R=1.
	MVI	H,0F8H	;H points to video memory offset by X.
	LXI	B,0040H	;Increment = 64.
	MOV	A,E	;Get Y.
L1:	SUI	03H	;Divide Y by 3.
	JM	P1	
	DAD	B	;HL contains quotient times 64.
	JMP	L1	
P1:	MOV	E,A	;Store residue of Y (Res = Remainder − 3).
	XRA	A	;Clear Carry.
	DCR	A	;A: =0FFH.
L2:	RAL		;Rotate zero into A per Residue.
	INR	E	
	JM	L2	
	INR	D	;Test remainder of X.
	JZ	P2	;If it was zero
	RAL		;then rotate zero bit three times.
	RAL		
	RAL		
P2:	ANA	M	;Set Memory bit.
	MOV	M,A	
	RET		;Return.
;Polymorphics Clear Screen			
CLEAR:	LXI	H,0F800H	;Video Memory.
CL1:	MVI	M,03FH	;Clear Character.
	INX	H	;Next location.
	MOV	A,H	;Last Location?
	CPI	0FCH	
	JNZ	CL1	
	RET		;Return.

Listing 2: A typical PLOT subroutine, this one for the Polymorphics Video Board. The Polymorphics board displays graphics by cutting a character position into six rectangles. The sign bit is 0 for graphics and 1 for characters. There are 16 lines of 64 characters each, or 48 lines of 128 rectangles each. The low 6 bits are used to set the bits as in the following example.

If a byte has its bits numbered: 76543210, the rectangles within a byte corrrespond to:

5	2
4	1
3	0

The PLOT subroutine plots the rectangle corresponding to X=D, Y=E.

to do is have PLOT send the X,Y data to latching digital-to-analog converters. VECTOR itself is not changed.

Hardware Implementation

The method is valid for hardware also. A circuit utilizing this method would be an excellent addition to a graphics interface board. As we have seen, the stack need not be deep; some 7489 type memories would be adequate, addressed by an up/down counter. Comparators are no problem, nor is the averaging circuitry. The comparators could control the midpoint manipulation (which would be a pain), eliminating the hardware analog of the instructions before LOOP. Stack empty is trivial. There are lots of integrated circuits in such a dedicated hardware approach, but this would be *fast*, great for plots and games. Some simplification might be obtained using LSI (large scale integration) microcontroller chips such as those in the 2900 series or their equivalents. Again, digital-to-analog converters could be used for X,Y display. (It sure gets rid of a lot of analog circuitry needed to generate straight lines on traditional X,Y displays.)

Summary

This article described a general method for plotting a line segment, given its endpoints, on a raster scan display. The method uses a recursive technique: lines are subdivided until they are short enough to plot as a point. The method can be used in both software and hardware applications. ■

Letters

Letters continued from page 22:

More Significant Digits for Pascal

A reader inquired in the June 1980 BYTE about the significant-digits limitation in UCSD Pascal. (See "Numerical Precision in UCSD Pascal," by Martin Berman, page 17.)

Vejur Software Systems has software packages which allow the precision of 14-, 18-, and 36-decimal digits under the North Star version of UCSD Pascal. Each package has two instructions for converting BCD (binary-coded decimal) numbers to binary form and vice versa, and four instructions for performing binary arithmetic. The 14-digit package stores numbers in 6 bytes; the 18-digit package uses 8 bytes, and the 36-digit package, 15 bytes.

Each package is supplied on a North Star double-density floppy disk for $20 in object form. Source assembly-language code for the Z80 microprocessor is also available for possible use on other systems.

Arne Paulsen
Vejur Software Systems
257 Fifth Ave
San Francisco CA 94118

Information Needed

The Psychology Department at the University of North Carolina at Chapel Hill is currently in the planning stages of a computer-based laboratory for undergraduates. We have chosen the Apple II microcomputer and Pascal as the programming language. As such, we would appreciate learning of the availability of any applicable software.

If there are any BYTE readers that know of such products, please let me know.

R F Genovese
University of North Carolina at Chapel Hill
Department of Psychology
Davie Hall 013 A
Chapel Hill NC 27514

Shared Files for Education

The special July 1980 BYTE with the Education theme was an excellent overview of the relationship between microcomputers and education, although it leaves readers with some incorrect impressions about the state of the art.

Dr Arthur Luehrmann's Education Forum ("Computer Illiteracy—A National Crisis and a Solution for It," page

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88) stressed the importance of a personal-computer shared-file system in providing a workable environment for computer education, and indicated this is a problem unsolved by the computer industry.

For several years, Nestar Systems has dedicated itself to providing add-on networks for the popular Apple, Commodore, and Tandy/Radio Shack family of computers. Known as the Cluster/One Model One and Model A, these systems substantially satisfy the features described as needed by Dr Luehrmann in his article. Indeed, one outstanding installation of a Cluster/One Model One system, with twenty-seven microcomputers coupled in a high-speed network, has been running under Dr Luehrmann's guidance at the University of California's Lawrence Hall of Science for over a year.

Readers interested in the details of Nestar's product offerings should contact us at the address below.

**Dr Harry J Saal
President
Nestar Systems Inc
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Palo Alto CA 94306**

Disputes Heath Software Compatibility

I was appalled to read Barry Watzman's (Heath Company's computer product line manager) statement in the July 1980 BYTE that, "...the S-100 bus has nothing at all to do with software, and it is obvious that Mr Libes is referring to 'CP/M' systems, and not to 'S-100' systems." (See "Statement from the Heath Company," page 14.) Does Mr Watzman really believe that, or did he simply miss the point of the statement he was ostensibly refuting? Does this mean that Heath really doesn't understand why their systems are not compatible with the rest of the world?

While it is true that software could not care less about the bus structure of its host processor, the problem is that most of the 8080/Z80 software available in object form requires contiguous user memory starting at location 0. None of the Heath systems can meet this requirement, while virtually all of the S-100 systems can. It would seem that, in practice, the S-100 bus has a great deal to do with software! The difference is purely one of hardware configuration and has nothing to do with whether or not Digital Research Corporation's CP/M is chosen as the operating system, although standard CP/M and all the programs designed to run with it fall into the class of affected programs. No doubt many Heath owners would appreciate a modification (albeit it would not be simple!) that would move their

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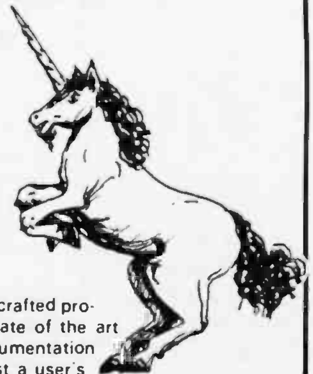

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user memory to the bottom of the address space and their read-only memory to the top.

Gordon R Smith
632 University St
Salt Lake City UT 84102

Barry Watzman Replies

Thank you BYTE for the opportunity to reply to Mr Smith's letter.

In the July 1980 BYTE, I said "the S-100 bus has nothing at all to do with software, and it is obvious that Mr Libes is referring to 'CP/M' systems, and not to S-100 systems." Mr Libes replied that "although CP/M has now been adapted to run on the H-8, there are still many other operating systems, languages, etc that still run only on S-100-based systems." Mr Smith then says that "while it is true that software could not care less about the bus structure of its host processor, the problem is that most of the 8080/Z80 software available in object form requires contiguous user memory starting at location 0."

Both Mr Libes and Mr Smith have attacked not what I actually *said, but rather their own (incorrect)* interpretations *of what I said. I can readily appreciate that both gentlemen assumed that as product line manager for Heath computers I was defending the H-8, but in fact the machines I had in mind were systems such as the Altos, the Onyx, and other non-S-100 systems which will run any software that an S-100-bus system will run. My point was that the bus structure is independent of the software used, which is true. I neither said nor even implied that the memory map of a computer is independent of the software used, yet that is precisely how both Mr Libes and Mr Smith interpreted my remarks.*

Having said that, let me go a step further with regard to Heath computers. Many vendors will maintain vociferously that their products are "perfect," even when they know this is not the case. However, there are very few "perfect" products in this world, and a more mature approach is to recognize, admit, and correct a product's shortcomings. The H-8 and H-89 have admittedly suffered to a degree because the presence of ROM (read-only memory) at address 0 has prevented the use of the standard Digital Research Corporation CP/M operating system and much of the available 8080/Z80 software.

My own background prior to coming to Heath had been with CP/M software and S-100 hardware, so I fully appreciate both the restricted software availability for Heath computers (although there is more Heath software available than most non-Heath users would suspect), and the hesitance of a

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A Division of Computer Tax Service Inc. *Distributed by* **Lifeboat Associates,** 1651 Third Avenue, N.Y., N.Y. 10028 (212) 860-0300 Telex: 220501 *significant portion of the user community to consider Heath computer systems. One of my goals as product line manager has been to change this. Thus, while Heath will continue to offer, enhance, and fully support its own operating system (HDOS), beginning this fall Heath will also offer and fully support the standard version 2.2 address-zero-based CP/M operating system and a full 64 K-byte all-programmable-memory address space on both the H-8 and the H-89 computers. At the same time, we will also begin offering an 8-inch floppy-disk system (double-sided, double-density, IBM-compatible, and capable of running in an IBM 3740 single-density mode), with the result that Heath systems will become totally software- and media-compatible with most of the other 8080/Z80 computer systems on the market. It is our hope that this will both increase the software available to our current customers (since the new configuration is fully retrofitable), and at the same time encourage those who have previously rejected Heath systems to give us a second look.*

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I have been unable to locate a manufacturer or a peripheral device for any readily available personal computer that enables the computer to perform the following telephone-related functions:

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4. to place outgoing calls using Touch-Tone signaling;
5. to initiate other ESS (electronic switching system) custom-calling services.

I would appreciate receiving any information on such a device from any reader of BYTE. Thank you.

Steven Schochet
POB 14073
San Francisco CA 94114

Two Requests for Video Brain Information

I am looking for any information on the programming module, cassette interface, memory expansion module, schematic, or anything to do with the Video Brain computer. Any information

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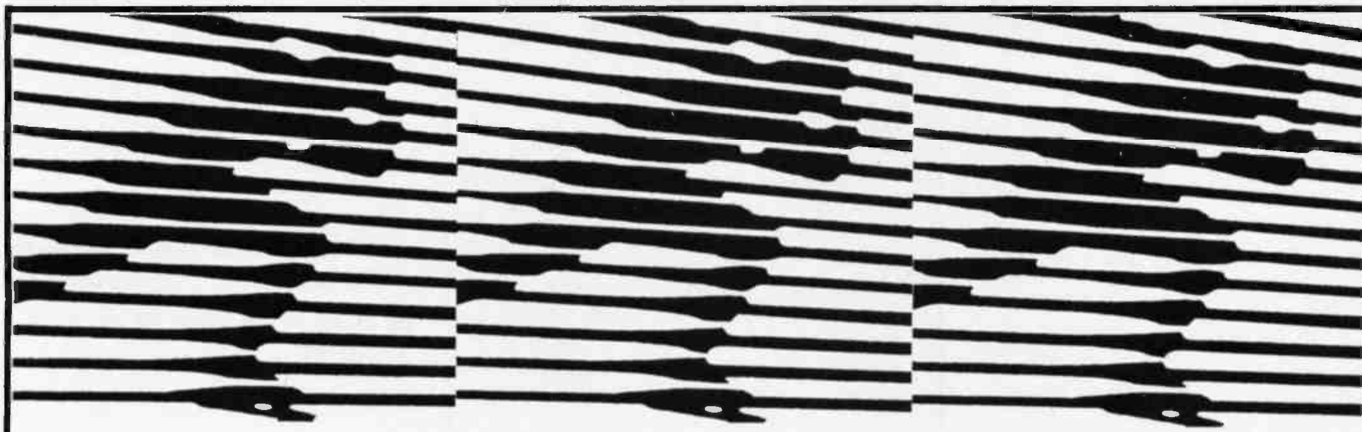

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that BYTE readers could send me about where I might find these items would be very helpful. Thanks for your cooperation.

Brent Dix
774 South 1110 W
Cedar City UT 84720

Since the Video Brain Computer Company went out of business and you can now readily pick up this computer (which has a color display) for around $88 (from COMB Liquidators in Minneapolis, Minnesota), I would like to suggest that BYTE and BYTE readers develop a few "how to" articles on modifying this computer. Some of these articles could include:

- adding a full-sized keyboard to the Video Brain computer;
- adding language capabilities;
- expanding the programmable and read-only memories in the computer;
- hooking up a cassette tape recorder to store programs.

I know there are certain limitations in the F8 design, but I think the price of the system and the interest to experimenters and other readers would make it an enjoyable and worthwhile project. And if all the above ideas were possible, you could have a pretty good system at a very cheap price. I hope you will consider these suggestions.

Paul Bazylewicz
843 Loomis St
Jackson MI 49202

*Any readers with information on the Video Brain system or its components are encouraged to write to the above readers. In addition, we at BYTE would be interested in seeing any articles on the Video Brain—either full-length articles or shorter articles that could be placed in our new upcoming column, "System Notes.". . .*GW■

BYTE's Bugs

A Financial Problem

In my article "A Financial Analysis Program" (February 1980 BYTE, page 192) several errors appeared in the glossary which, unfortunately, I did not receive with my proofs. On page 198, under the heading Accounts Receivable in Days, both occurrences of *divided by* should have read *divided into*. This correction should also be made for the

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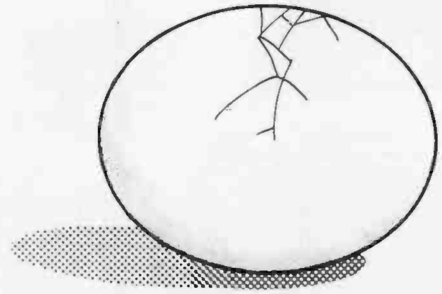

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Circle 223 on inquiry card.

definition of *inventory turnover* on page 200.

Also, I had not realized that some of the following abbreviations would be incomprehensible to nonaccountants:

Abbreviation	Meaning
CGS	cost of goods sold
SGA	salaries and general administrative expenses
PPD items	pre-paid items
Bldg/Equ	buildings and equipment
Cur LT	current portion of long-term liabilities
C-Stk	common stock
APIC	additional paid-in capital
RE	retained earnings
TOT CR	total credits

I have received many requests for information on converting the program to run on other systems. Perhaps readers who have adapted this concept to their own machines would like to share their versions by sending a note to BYTE.

John A Lehman
716 Hutchins #2
Ann Arbor MI 48103

BYTE's Bugs

An Omission in "Varieties of Threaded Code"

A paragraph was inadvertently omitted from the first page of "Varieties of Threaded Code for Language Implementation," by Terry Ritter and Gregory Walker (September 1980 BYTE, page 206). The following should be inserted between the first and second full paragraphs on the right-hand column, just before the paragraph that begins, "Any form of interpretation...":

The run-time overhead of any interpretation technique depends on the relative complexity of the machine-language routines actually invoked. If the functions performed in machine language are similar in complexity to that of a single machine instruction, then the overhead of even a hardware subroutine call and return operation will be quite high. On the other hand, if the machine-language routines are made complex, the overhead of even slow interpretation can be made insignificant.

This paragraph explains a pivotal point in the article. We apologize for the omission.■

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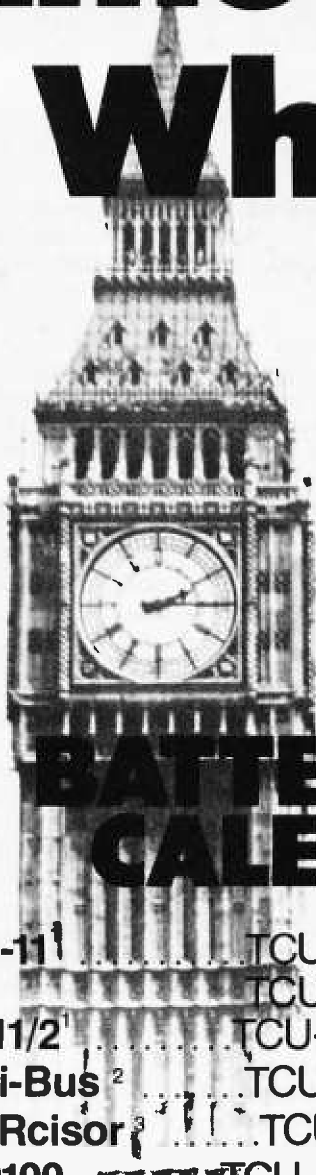

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DIGITAL PATHWAYS

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Ask BYTE

Conducted by Steve Ciarcia

Terminal Expense

Dear Steve,

Why can't I buy a simple video terminal for less than $700, when a portable black and white television receiver (including radio- and audio-frequency electronics) costs as little as $70 and a complete microcomputer system (including video display and keyboard) costs around $600? I own a KIM-1 and don't use it as much as I would like to because the keypad and LED (light-emitting diode) display are inconvenient. It seems to me that, considering the simplicity and availability of the component parts required for a no-frills "glass Teletype," the price should be between $150 and $200.
Rob Fullerton

A high-grade video terminal and a television set are different animals. The terminal has a much wider bandwidth and usually better component tolerances. Granted, this may make it worth $200 (instead of $100 for a television), but look at what else you are getting: case, power supply, fan, printed-circuit board with electronics, gold-plated connectors, Hall-effect or reed-switch keyboard, nonglare bezel, etc. These things add up. The reason why the KIM-1 is so inexpensive is that it is just a printed-circuit board with components on it. Most likely the printed-circuit board in a video terminal is as complex as the KIM-1 and worth about the same if sold separately.

When a manufacturer produces a television set, he can be satisfied with a 5% or 10% return on investment because he will probably make over a million of each model. An American video-terminal manufacturer gears up for a production run of perhaps 10,000, if he is lucky (there have been a few 100,000 sellers). The effort involved is about the same as designing a television, but all the costs are amortized over 10,000 rather than 1,000,000 units. To stay in business, terminal manufacturers must have a much higher profit margin, and the overall price is therefore higher.

As the demand for video terminals grows, you will see the television manufacturers attempt to meet the market needs. With the added volume and competition, I think you can expect to see a $300 video terminal within a year or two. In the meantime, all you can do is look for a good used terminal for about $300.
Steve

Radio Shack Bounce

Dear Steve,

No doubt you have heard many cries from frustrated TRS-80 users about keyboard bounce! I took basic programming at a Keene, New Hampshire, high school. There, I heard my complaint multiplied by 15. Our instructor, Charles Tousley, has the software keyboard fix sold by Radio Shack. I don't have to tell you about the complications involved with that and 15 students! Do you know of, or can you design a hardware keyboard-debounce circuit that can be installed?

I looked at the keyboard data on my oscilloscope. The bounce occurs when the key is released. I tried simple tricks with no luck. I have thought of flip-flops and various timing circuits, but I'm afraid to try them. My technical experience isn't in design. Also, the +5 V series voltage-regulator transistor in the power supply runs hot. I fear that it is being worked to capacity, and I don't want to damage the computer.
James L Siewert

Contact bounce is an aggravating situation when it occurs, and not only the TRS-80 suffers from it. Most keyboards with unsealed contacts are susceptible, and the remedies are sometimes no better than the problem.

In the case of the TRS-80, it is due to tarnish and oxidation on the key contacts. When you press the key down, you lower an insulator that is situated between the contacts. The contacts then touch together and close the circuit (the process is reversed when the key is released). However, if the contacts are dirty it takes longer for them to make satisfactory contact. This extended time is called bounce *because on a scope it appears as if the contacts are opening and closing rapidly or "bouncing." In circuits where there is a high current flowing through the contacts, most of this oxidation would be burned away (or if the contacts were gold they would not tarnish).*

One solution is to wait longer for the contact bounce to settle. This is accomplished in the older versions of the TRS-80 by loading in the keyboard-fix *program you mentioned. Entering this tape every time you power up is tedious, and on the first humid day when the contact resistance changes everything goes haywire once again. Rather than only using your TRS-80 in a clean room at NASA, it's easier to attack the problem at the source.*

If you have an older version TRS-80 (prints "MEMORY SIZE?" when powered up), you can clean the contacts. Remove the top of the keys one at a time and depress the spring. Using a very light-abrasive paper with a few drops of alcohol on it, run it up and down between the closed contacts a couple times. Repeat it for any keys that continue to bounce.

In the newer TRS-80s (prints "MEM SIZE?" when powered up), there is a patched keyboard routine with a debounce value located at 011C in hexadecimal. Change this byte to increase the delay.

Finally, most experimenters don't appreciate the fact that commercial components very often run hot. Most integrated circuits have a 0°C to 70°C operating range. Transistors usually have an even broader range that may have an upper limit of 125°C to 150°C. The question then is not whether it is hot, but how hot? Series regulators generally run hot because that is the nature of the beast. Switching regulators, such as used on the Apple II, dissipate very little power, but they cost considerably more to manufacture. If the heat still bothers you, add a larger heatsink. Personally, I'd try a little forced air cooling (a fan) first. It's not as messy.
Steve

Radio Shack Memory Upgrade

Dear Steve,

I recently subscribed to BYTE, and my first copy was the June 1980 issue. I enjoyed reading your fine article on page 40, "I/O Expansion for the TRS-80, Part 2: Serial Ports." I found the article very informative. I am a "new kid in town" when it comes to electronics and all the various equipment available for microcomputers. I have a Radio Shack TRS-80, Level I, with 4 K bytes of memory, and I am just getting used to it. I'm really crazy about computers and plan to become deeply involved with them as a hobby at home.

The reason I am writing is because I am wondering if you could provide me with a reprint of Part 1 of your article which appeared in the May 1980 BYTE, page 22, which dealt with parallel ports. I will be glad to pay you for it if necessary. I am sure the article will be useful to me in the future.

I would like to expand the memory in my TRS-80 to 16 K bytes and would naturally like to do it as cheaply as possible. I have seen all the various advertisements regarding add-on memory for TRS-80s with prices ranging from $55 to $80, for expansion kits consisting of "4116-200 ns (8 pcs)." The advertisements say no special skills or tools are required, and if a person can change spark plugs in a car then they can add the memory kit to their system. As I said, I am a novice to any type of electronics and have no idea what "4116-200 ns (8 pcs)" means. I assume "ns" is nanoseconds.

Could you please advise me about these expansion kits? Will my TRS-80 still function the same, are the kits really easy to install, or will I be risking permanent damage to my system? I would greatly appreciate your comments and help.
Michael H Bunt

There is nothing better than the real thing. If you refer to page 229 of the June 1980 BYTE, you will see that it is easy to obtain the May BYTE (and other back issues) in its entirety.

Concerning 16 K-byte memory add-ons for the TRS-80, it isn't too much of a problem to upgrade your system, but it is not as sim-

ple as pulling eight 4 K-byte integrated circuits and replacing them with 16 K-byte 4116s. Hardside (6 South St, Milford NH 03055) sells an upgrade kit that includes eight 200 ns 4116s and two DIP shunts. The following is an excerpt from their kit installation instructions:

"Locate Z13 through Z20 on the logic board....These are the 4 K [programmable memory] chips which you will remove and then replace with the 16 K [memory] chips in your upgrade kit....Remove the 4 K [memory] chips by gently and gradually prying them loose....Now, install the 16 K [memory] chips....Locate the sockets for Z3 and Z71 on the logic board. On "A" Revision boards, note that Z3 is blank. Remove any jumper circuits (DIP shunts) at Z3 and Z71. The numbers Z3 and Z71 should be silk-screened next to the corresponding components on the logic board. Install the DIP shunts which are supplied....Reassemble the case, place the logic board and the keyboard on the posts of the lower half of the case, with the keyboard face up so that the posts stick through the holes in the logic board and the keyboard rests on these posts. Carefully lift the keyboard about one inch above the posts upon which it rests. FLEX THE CONNECTING RIBBON CABLE AS LITTLE AS POSSIBLE.

Replace the spacers on the posts and let the keyboard rest back on the posts....Turn the computer on. The screen should display 'READY'. Type 'PRINT MEM' and hit 'ENTER'. Your 16 K-byte computer will display '15871' or '15872'."

As you can see, adding the memory is not a great problem and it will not damage your system.
Steve

COMM-80

Dear Steve,

I read with great interest your article "I/O Expansion for the TRS-80, Part 2: Serial Ports" (June 1980 BYTE, page 42). However, I have a few questions before I can decide whether or not the COMM-80 is the answer to my problems.

I own a Radio Shack TRS-80, Level II, with 16 K bytes of programmable memory. I want to eventually expand it to include 32 K bytes, a parallel printer, a telephone modem, and an 8-inch floppy-disk system. Since the Radio Shack floppy-disk system is only a 5-inch disk, I knew I'd eventually need to use equipment from another manufacturer.

Could you please tell me if it is possible to use a disk system with the COMM-80? Would that use the RS-232 port? Could I use both the extra 16 K bytes of memory and a disk system at the same time?
Richard L Jamison

The COMM-80 is a serial and parallel port. It can be used with any hardware that will plug into a TRS-80, but it has nothing logically to do with a disk system. However, if you purchase a stand-alone disk controller or memory-expansion module, they would be TRS-BUS driven and could be plugged into the expansion bus connector of the COMM-80.

It is also my understanding that most disk operating systems for the TRS-80 require a 32 K-byte system to run effectively. The question should be whether you can live without the extra 16 K bytes.
Steve

Dear Steve,

My colleagues and I who have worked in computer-controlled laboratories over the years are intrigued with teaching and research possibilities with modern microcomputers. The Radio Shack TRS-80 is in some senses a bargain, but as you rightly point out, the I/O (input/output) problem is serious. Your May and June 1980 articles in BYTE are suggestive, but questions remain:

- How can the COMM-80 plug into the J2 connector on the Expansion Interface since J2 is the place in the Expansion Interface where it connects *itself* to the TRS-80? (You must mean the J3 40-pin bus-extension edge connector.)
- How *can* COMM-80 be used with TRS-80 Expansion Interface? How are sixteen units connected to one another, *and* to the TRS-80? Your photo 1 shows only 3 connections: one to TRS-80 keyboard, one for serial printer (RS-232), and one for parallel printer interface.

If sixteen units are indeed all "chainable" to the Expansion Interface and one has a 16-unit bus-extension capacity, we would appreciate literature and specs.

J P Rosenfeld PhD

Sorry about that, but you are correct. The signals on J2 and J3 are the same, but the COMM-80 attaches to J3 when using an Expansion Interface. This is also called the screen-printer port in some of Radio Shack's literature.

The COMM-80 is a bus-driven device and can be connected either to the keyboard connector or to J3 as I mentioned. The COMM-80 contains a parallel (Centronics-compatible) and a serial (RS-232C) port. Internally, it has a 4-bit address-selection switch. If you keep the address setting as shipped, the COMM-80 will perform as if it were the serial TRS-232 board installed within the Expansion Interface. However, if you already have a TRS-232 board and want to just add another printer to the system or drive a serial printer in addition to the modem, you would set the COMM-80 to one of the other sixteen addresses. Whether you use two or four COMM-80s, as long as they have different switch settings, they are independent I/O (input/output) channels to the computer.

With a 4-bit address code, up to 16 COMM-80s (or 15 and a TRS-232 board) can conceivably be attached to a TRS-80. Each COMM-80 has an auxiliary TRS-BUS connector that is the same as J3. This means that the second COMM-80 is plugged into the auxiliary connector (creating a daisy chain), since J3 on the expansion interface is already occupied. As a practical matter, however, the cable lengths get to be a problem with over ten units connected together. Some extra buffering might be needed at the TRS-80 end to drive thirty or so feet of bus. I believe Radio Shack sold such a device at one time.

As far as photo 1 (June 1980 BYTE, page 42) goes, that was my prototype and it did not have the auxiliary expansion-bus connector. The photo on page 62 of the same issue is of a production COMM-80 board. The three connectors you see are (clockwise from bottom left) for the auxiliary TRS-BUS, RS-232, and parallel printer. The connections missing in this photo include the 1.5 feet of ribbon cable and the 40-pin expansion-bus edge connector. They would have

obscured the picture.
Steve

WTRS-80

Dear Steve,

I am the manager of a radio station in New Jersey, and I'm contemplating a microcomputer system to perform a variety of tasks at the station. Specifically, I want the computer to do:

- program logs—random selection of public-service announcements;
- information retrieval from our record library;
- word processing;
- computations of transmitter output power;
- automatic transmitter control based on plate current, plate voltage, and power output readings.

The last entry in the list above is, perhaps, my main concern. Is there interfacing available to take analog readings and perform corrective action by way of contact closures using a microcomputer such as the Radio Shack TRS-80 Model I or Exidy Sorcerer?

Should I be looking at putting together a process controller, or can I do what I want by using the off-the-shelf computers mentioned above with interfacing hardware?

Ideally, I would like to have a computer doing station functions in real time, and simultaneously use the computer for other functions. I would appreciate your direction in this matter.

P Michael Zeimann

Your question is legitimate, but it is a little like saying, "I want to drive to California next week. What kind of car should I buy?"

The Radio Shack TRS-80 Model I is adaptable to a number of control applications as well as standard bookkeeping; however, unless you are running these functions sequentially rather than concurrently, you will require more than one TRS-80. You could try to write a multiprocessing operating system, but that would put too much dependence on one piece of equipment and the entire radio station could "make like a slow record" when you try to print out your program log.

First of all, let me suggest that you create functional subsystems with common equipment and software. Just program them for the different applications. In the case of the transmitter, you will, in fact, need to configure a closed-loop process-control system. It will probably require an analog and relay interface for reading input sensors and setting output controls. Any computer can be used. How effectively it will perform is a function of the application software and it will require obtaining the necessary peripherals. Of course, you could build everything and write your own software.

You could try another source for information before jumping in. The May 1980 Kilobaud Microcomputing *has an article on using a TRS-80 for the programming logs at a radio station; and NAPCO Inc of Terryville, Connecticut, uses a TRS-80 to control a $250,000 dip-plating line. They manufacture their own front-end equipment (ie: 12-bit A/D [analog-to-digital] and 10-bit D/A [digital-to-analog] converters) and the application may be similar enough for*

you to use some of their ideas.
Steve

[Software directed toward the needs of radio stations, such as logs, billing, and payroll, is available from The Management, POB 111, Aledo TX 76008. . . .CPF]

Remote Supplier

Dear Steve,

After reading your article "Handheld Remote Control for Your Computerized Home" (July 1980 BYTE, page 22), I was very impressed with the many ways remote control can be accomplished. I am particularly interested in the CMOS (complementary metal-oxide semiconductor) LSI (large-scale integration) remote-control devices made by Motorola—the MC14422 and the MC6525. After reading your article, I was delighted to find that *someone* had built a working circuit using these devices.

One problem I have is finding a supplier that carries these integrated circuits; can you tell me your source? Can I use the same type of 40 kHz transducers that you specified in "Computerize a Home" (January 1980 BYTE, page 28)?
Nicholas Vasil

I usually buy my components through distributors such as Impact (617) 444-3971, Hamilton-Avnet (800) 952-0851, or Schweber Electronics (800) 952-1075. All three of these distributors carry Motorola products, and, depending upon whether they have any of these devices in stock, they should sell you a pair. Be aware, however, that the current price for the MC14422 is $8.74 and the MC6525 is $10.50. You may also find yourself with a $25 minimum-order requirement.

The 40 kHz transducer I used on the Busy Box home controller may not respond quite as well at 35 kHz, but you shouldn't have any real problems.
Steve

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If you are a subscriber to The Source, send your questions by electronic mail or chat with Steve (TCE317) directly. Due to the high volume of inquiries, personal replies cannot be given. Be sure to include "Ask BYTE" in the address.

Circle 233 on inquiry card.

Book Reviews

Interfacing and Scientific Data Communications Experiments

by P R Rony, D G Larsen, J A Titus, and C A Titus
Howard W Sams & Company Inc,
Indianapolis IN, 1978
Softcover, 157 pages
$5.95

Most communication, whether it is person to person, machine to machine, computer to peripheral, or person to computer; is serial in nature. Words, signals, data, or other basic units of information are sent and received one unit at a time. The opposite type of communication, the parallel format, would require that, for example, all words in a thought be spoken at the same time. That technique is clearly impractical.

To communicate effectively, the words, signals, data, etc must be in the proper format. The term *format*, as used in serial data communications, covers three areas. First is the method by which the data are transferred. Are they sent asynchronously or synchronously? In other words, does the transmitting device assume that the receiver is always available to receive the data, or must a synchronization method be used to keep data in step? If the latter is used, that method of serial data transfer is synchronous, which is beyond the scope of this book.

Following some introductory comments on the scope and objectives of the book, and the fact that the reader is assumed to have a basic understanding of TTL (transistor-transistor logic) electronics (some knowledge of transistor theory would be helpful, too), the reader is given illustrations of situations where asynchronous serial data communications would be used. Anyone who has ever priced multiconductor cable for a remote parallel-data format terminal knows that asynchronous serial communication over a twisted pair or twisted triple is much less expensive.

Since TTL integrated circuits can readily be used for asynchronous serial data transfer, shift registers are discussed briefly. The bit format for asynchronous serial data transfer is illustrated and discussed. Universal Asynchronous Receiver/Transmitters (UARTs) have replaced many TTL building blocks, and their function is discussed at length. Since a device cannot be used effectively until the user understands it thoroughly, the control pins of a generalized UART (ie: the TMS6012, TR1602, or AY-3-1015 are all pin-compatible) are explained in detail. Since the UART is a hardware-programmable device (as opposed to the software-programmable USART discussed later), the function of each pin in the UART transmitter, receiver, and control blocks is explained fully. CMOS (complementary metal-oxide semiconductor) UARTs such as the Intersil IM6403 are touched on because of their use in low-power applications.

The second area covered by the term format is data transfer rate. The UART requires a clock from which to generate the serial bit timing, so various clock generators are discussed next. Two requirements of the clock generator for a UART are given: first, it must be able to provide a square wave of sixteen times the desired serial data rate in bits per second. Secondly, the accuracy of the clock must be 3% or better to ensure accurate transmission and reception of serial data. Motorola's MC4024 oscillator and MC14411 bit rate generator are explained, and circuit diagrams are given. The ubiquitous NE555 is also discussed as a bit-rate generator, and a circuit diagram is given once again.

Presumably the reader now fully understands how a UART works, and, if so, the next logical step is to use it. In the "Microcomputer-UART Interfacing" section, an example is given which shows the TR1863A inter-

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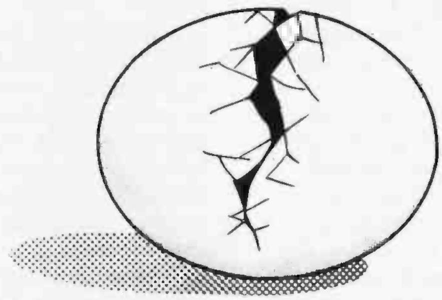

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faced to an 8080-based system. The device-control requirements for the processor have already been explained, so this section is devoted to explaining how to generate the required signals from the 8080's $\overline{\text{I/O RD}}$ and $\overline{\text{I/O WR}}$ (input/output read and write) signals. Once the reader has wired the UART into his system, the programs given in the text can be entered into the machine, and the UART is ready to transmit and receive serial data.

In the same section on interfacing, the Intel 8251A Universal Synchronous/Asynchronous Receiver Transmitter (USART) is covered. A block diagram, pinout diagram, and truth table for control inputs are given. Additionally, a circuit diagram is given showing how to interface this device to an 8080 system, along with explanations in tabular form for the mode-control instruction and the command instruction.

As the terms *mode control* and *command* imply, the 8251A is software programmable. This significantly improves system flexibility because, unlike the UART, no wiring changes are needed to change the number of stop bits, even/odd/no parity, character length, and data rate. Also initialization input and output programs are given.

Now that you have wired your UART or USART on an I/O board, you're ready to connect a teletypewriter and start typing, right? Wrong! A vital link between the UART and the peripheral is missing. The third area covered under the term format is signal level of the serial bit stream. The UART outputs are TTL level signals. An interface is required to convert the TTL level signals to signals capable of being transmitted over longer distances than a foot or so. Both 20 mA current loops (used by teletypewriters) and RS-232C interface signal levels are discussed.

In contrast to the discussion of RS-232C voltage levels (where no circuit diagrams for voltage level converters are given), the discussion of 20 mA current loops has a number of circuits and optically isolated converter circuits (the latter require a current source). If you do not feel like designing your own 20 mA interface, these circuits alone are well worth the price of the book. A brief discussion of teletypewriter interfacing is the last topic covered in the text.

Following the text are ten experiments, which are based on UARTs. The experiments assume that the reader has available a solderless breadboard (although the experiments may be hardwired), a UART, some 7400 series TTL chips, and a teletypewriter. If the reader chooses, the experiment modules used may be purchased from E & L Instruments Inc. Their use makes breadboarding easier.

If the reader does not have a teletypewriter, a lot can still be gained from the book since the experiments are tutorial in nature. The authors describe exactly how each experiment is to be performed, then proceed to ask a number of in-depth questions. Following each question is a space to jot down an answer, then the answer is given. Following some of the more involved experiments, a review is given that covers the high points learned.

Simplex, half-duplex, and full-duplex asynchronous serial data communications are discussed in this book. The transmitter in each case is a UART. The receivers range from lamp monitors (to reconvert the serial data back to parallel data for comparison with the transmitted data) to teletypewriters.

Nine appendices follow the experiments. The ASCII (American Standard Code for Information Interchange) code is listed, data rates and clock frequencies are tabulated, a list of UART and USART manufacturers is given, and data sheets for several are included. The last appendix gives an overlay for the LR-21 outboard module, should the reader choose to buy it rather than breadboard his or her own.

In summary, the book fulfills its intended purpose very well. If you have a serial data communication requirement, this book will provide all the information needed to design a UART/USART-based asynchronous serial data communications interface. Even if you do not perform the experiments, a lot of information can be derived from this book.

J C Hassall
H & H Enterprises
1201 Highland Cr
Blacksburg VA 24060

An Introduction to Database Systems

by C J Date
Addison-Wesley, Reading MA, 1977
Hardcover, 536 pages
$19.95

This is the second edition of one of the many books in the IBM-sponsored Systems Programming Series. Don't run away because I said IBM. This is not an IBM manual, nor does it say that IBM computers are the answer. Each book in this series is written as a collection of important topics and concepts in a particular area. The books reflect the ideas and opinions of the author, not necessarily those of IBM. This book was written by C J Date of IBM (UK) Laboratories Ltd.

This book, like all the others in the Systems Programming Series, is not for the beginner. It is designed as a text and reference for a systems programmer. I found it to be hard reading. This is not because of its style, but because it contains large amounts of information that were new to me. I found myself continually going back and rereading sections that I had initially read hastily.

This book is divided into six parts, with each part containing several chapters. Part 1 covers the basic concepts of a data base. It addresses the necessity of a data-base management system, and it explores storage structures and data models. Also introduced are the three types of data-base management systems: the relational, the hierarchical, and the network systems. These three types of data-base management systems emerge as the subjects of the next three parts of the book. Each part addresses in detail the capabilities of one type of system and explores it using a current system as an example.

Over three hundred pages later, the book returns from the discussion of these three approaches to discuss data-base security and integrity.

Finally, Part 6, using the information previously presented, compares the three types and presents a conclusion. The conclusion, by the way, is a compromise approach, and still does not say to buy an IBM product.

My conclusion: if you are a computer user who wants to know how a data-base system works, don't read this book. However, for anyone seriously interested in developing a data-base management system, this book is excellent. Until you can understand the concepts presented in this book, you are not ready to develop a data-base system. There is certainly more presented than will be implemented on a microcomputer in the next few years, but it's important to know the concepts so you can select the best approach.

Phil Hughes
POB 2847
Olympia WA 98507

TRS-80 Interfacing

by Jonathan A Titus
Howard W Sams & Company Inc,
Indianapolis IN, 1979
Softcover, 190 pages
$8.95

TRS-80 Interfacing is one of the new books available on interfacing the Radio Shack TRS-80 to external devices. This book, which is part of the Blacksburg Continuing Education Series, is written in the same style as the popular *Bugbooks*; ie: the first half covers general interfacing techniques, while the second half deals with hands-on experiments. If you are interested in interfacing your TRS-80 to external devices, this book is a good place to commence.

Chapter 1 begins by describing the pins on the Z80 processor. Level II BASIC is reviewed, and examples are given showing how to move information in and out of the TRS-80 using BASIC commands. The chapter ends by briefly comparing BASIC with assembly language.

Chapter 2 describes various methods of I/O (input/output) address decoding. This is accomplished through diagrams of various integrated circuits and by showing how these circuits are used to select one or more I/O ports. The three decoding methods discussed are gating, decoding, and comparing. After reading Chapter 2, you will know how to decode any I/O address.

While I/O devices are very slow, the TRS-80 is very fast; this problem is discussed in Chapter 3. Latches and three-state bus drivers are shown that can be used with the TRS-80. Although most of the chapter is concerned with standard I/O decoding, memory-mapped I/O is briefly mentioned.

"Flags and Decisions" is the title of Chapter 4. Flags are used for device synchronization and, thus, involve both hardware and software. Hardware circuits that are used for flag detection, along with the necessary Level II software, are discussed.

The construction of a TRS-80 breadboard is covered in Chapter 5. Regardless of whether you plan to actually build the breadboard or not, it is good to review the schematic of the breadboard and make sure you understand how it operates. Included on the breadboard is

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a 5 V power supply, logic probe, device and memory decoders, bus buffers, and control circuitry; a description is given of each.

Chapter 6, which is approximately one-half of the book, contains eighteen experiments. The first eleven experiments provide basic interfacing techniques, while the last seven experiments are more advanced. Topics such as I/O port applications, traffic-light controllers, and A/D (analog-to-digital) conversion are covered in detail.

I recommend *TRS-80 Interfacing* to anyone who is interested in the hardware aspect of the TRS-80. Although the book is not as thorough as I would have liked, it will serve as a good starting place for the beginner. My biggest complaint was that Level II BASIC was the only language used; assembly language and the problems that it can help solve—interrupts, fast I/O, etc— were only briefly mentioned. You may be interested to know that the major topics discussed in the book are covered in a 3-part article in *Radio-Electronics*, beginning with the November 1979 issue.

Norman McEntire
323 Tram Rd
Columbia SC 29210

Pascal: An Introduction to Methodical Programming

by W Findlay and D A Watt
Computer Science Press, Potomac MD, 1979
Softcover, 306 pages
$12.95

Findlay and Watt have organized this book as a text. It presents all of standard Pascal but is arranged so that you can get started, and thereafter learn new concepts and features as you progress. The preface states that the book was written to be used in conjunction with a first course in programming using Pascal. Although initially I was skeptical, after reading the book, I decided that it does clearly present everything necessary to start from scratch and learn Pascal. Pascal is a complicated language, and any book that promises to be easy will not be able to present all of the language.

I can recommend this book for use in two places; first, in its intended use as a classroom text for teaching Pascal to computer science beginners. Here, the help of an instructor would assist the student in learning the many new concepts. Second, I feel the book makes an excellent text for anyone with some background in another programming language.

In either case, I feel that it is very important to have a Pascal compiler available to try the concepts presented in this book. It would be virtually impossible to learn the details of a language as complex as Pascal without having an opportunity to try ideas on a computer.

For those who feel that this book may be what they need, here are the details of its contents. The book is divided into six parts plus five appendices. Part 1, entitled "First Steps in Programming," presents the notation used in the book and the concept of data, then explores the data type INTEGER. The basic I/O (input and output) statements are presented and a complete program is developed using only integer data, I/O statements, and the assignment statement.

From this point on, new concepts are presented in such a way that they build on the basic ideas. Part 1 ends by presenting the BOOLEAN data type, WHILE and IF control structures, and some concepts on program refinement, testing, and documentation.

Part 2 introduces the data types CHAR and REAL, enumerated and subrange types, and arrays. Part 3 presents the remaining flow-of-control statements (CASE, FOR, REPEAT, and GOTO). Part 4 introduces the concept of subprograms; this part also presents chapters on functions, procedures, and their uses. Part 5 presents the data structures of Pascal, which include records, packed data and strings, files, sets, and pointers.

Part 6 is entitled "Programming Methodology." It reviews the concept of stepwise refinement presented earlier in the book and does an excellent job of showing its usefulness with two examples. For those of us who can write programs faster than anyone else, but can never quite get them to work or cannot figure out how to add a new feature to the program that we just wrote, this section is required reading. The first example is the development of a simple text formatter. It is developed through four levels of refinement showing why each developmental path was chosen at each level. The second example is a program to tabulate the winner of a transferable vote election. This example is equally well done.

Finally, the appendices

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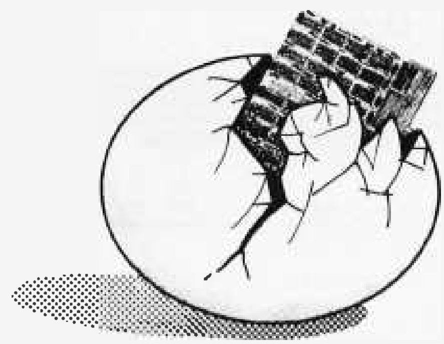

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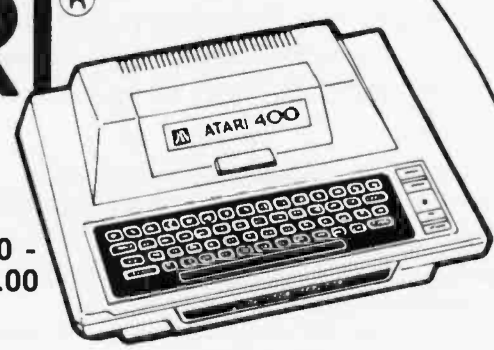

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present Pascal syntax diagrams, reserved word and special symbol lists, predeclared entities (like arithmetic functions and I/O procedures), and character sets. The final section of the book contains answers to selected exercises.

In conclusion, if you want to learn Pascal, and if you have some knowledge of computing along with access to a Pascal compiler, I feel this book can help you. If you are an instructor, this book would be an excellent choice for the text in a Pascal programming class.

Phil Hughes
POB 2847
Olympia WA 98507

Microcomputer Interfacing

by Bruce A Artwick
Prentice-Hall Inc,
Englewood Cliffs NJ
1980
Hardcover, 341 pages
$18.95

At one time or another, most of us have wanted to use our microcomputer to control items such as lights, appliances, air conditioners, and other things in our "real world." If you are one of these people and have gone through the frustrating chore of trying to put together a suitable interface, this book is for you.

Between the covers of this long-needed book, Bruce A Artwick has compiled a very useful collection of data, technical facts, and advice for the microcomputer user who is interested in interfacing computers to the real world.

The greatest strength of this book is that the author not only covers the advanced topics related to current, technically sound interfacing techniques, but he also takes the time to explain the fundamental theories and information that are generally skipped over in publications geared toward those readers who possess more technical knowledge and skill. Mr Artwick makes liberal use of drawings, charts, graphs, and schematics to highlight his well-written text.

While this book is easy to read and comprehend, I can assure you that the information contained within it is complete and to the point.

Chapter 1 is an orientation to interfacing. It gets things off to a good start for those readers who are new to this technical area. The chapter details general computer architecture and system design. It also explains how interfaces are used in these systems and gives examples of several types of practical interface applications.

Chapter 2 gives tips on selecting the best microprocessor for the task to be done. The discussion includes most of the popular microprocessors. This chapter lists advantages and disadvantages of each type of microprocessor.

Chapter 3 is devoted to memory. Included is information on several types of memory and the pros and cons of each. This chapter also discusses medium- and long-term storage devices and techniques. The chapter concludes with tips on selecting the best memory device for the user's particular application.

Chapter 4 covers, in great detail, I/O (input/output) methods and devices. The highlights of this chapter include: I/O standards, buses, DMA (direct memory access), and the transfer of data over long distances.

Chapter 5 is devoted to hardware. The author covers in depth the actual parts that are used to accomplish the interface of a microprocessor to the real world. Conventional items such as transistors, SCRs (silicon-controlled rectifiers), LEDs (light-emitting diodes), and relays are detailed as well as the more recent devices such as UARTs (universal asynchronous receiver/transmitters), modems (modulator/demodulators), and cassette controllers.

Chapter 6 guides the reader in going from theory, learned in the first five chapters, to applications. This chapter gives tips and design rules to help the reader design a workable interface.

Chapter 7 covers interfacing to popular standard buses such as the S-100, SS-50, those used in LSI-11 and TRS-80 computers, and others.

Chapter 8 shows the reader how to take a completed design and actually construct it. This chapter discusses enclosures, connectors, circuit boards, wire-wrap, layout, and assembly. Here, Mr Artwick gives some very good advice on purchasing parts and the pitfalls of some "bargain" buys.

Chapter 9 discusses interface software. This chapter covers software basics in general, but it does not go into any detail on the writing of actual software routines for handling the interface. However, the author does give the reader some tips on obtaining software design information from outside sources.

Although the text concludes with Chapter 9, I am compelled to mention the excellent glossary at the end of the book. It contains more than 200 concise, well-written definitions of the technical terms used throughout the book. The glossary is a wealth of information in itself.

In conclusion, I highly recommend this book as a valuable addition to your technical library. It is the best source of interfacing information in one volume that I have yet come across. I am sure that you will be consulting it as often as I do. ■

Clifford R Mosley
410 Campus
Jonesboro AR 72401

BYTE's Bits

Call for Papers

Papers are being solicited for the 1981 Summer Computer Simulation Conference to be held July 21-23, 1981, in Washington DC. The conference theme is "Simulation: Foundations and the Future." Accepted papers will be published in bound proceedings distributed at the conference. Five hundred word summaries or complete drafts of original papers must be submitted by November 15, 1980, to L G Culhane, The MITRE Corporation, 1820 Dolley Madison Blvd, McLean VA 22102, (703) 827-6000.

Call for Papers

A November 15, 1980, deadline has been set for submitting papers to the Eighth International Colloquium on Automata Languages and Programming (ICALP 81), The Technion, Haifa, Israel, July 13-17, 1981. Send four copies of an extended abstract to the Chairman of the Program Committee, Professor S Even, ICALP 81, Computer Science Dept, The Technion, Haifa, Israel. The papers can be on topics concerning automata theory, formal languages, analysis of algorithms, computational complexity, computability theory, mathematical aspects of programming-language definition, and more.

Microcomputers in Primary Schools Project

The University College, Cardiff Science Mathematics and Technology Centre, in Wales, is working on a project designed to evaluate the use of microcomputers and the currently available software for primary schools. The project has been funded in part by the British Department of Industry, and to obtain the greatest benefit from the project, the college is asking industrial concerns for contributions in cash or support. Doctors Thorne and Wharry of the computing mathematics and education departments would like to ask any individuals or organizations that have appropriate educational software to forward copies to them. The results of their work will be published and made available to all primary schools in the United Kingdom. For more information, contact Doctors M Thorne and D Wharry, University College, Cardiff Science Mathematics and Technology Centre, Dept of Education, Senghennyd Rd, Cardiff CF2 4AG, Wales.

Computer War Games Announced

Avalon-Hill, well known in the war-gaming field for its historical simulation games, has announced five games in its new Avalon-Hill Microcomputer Games series. Four of these games, *B-1 Nuclear Bomber*, *Midway Campaign*, *North Atlantic Convoy Raider*, and *Nukewar*, are games for one player against the computer. The fifth game, *Planet Miners*, is a game for one to four players. The games, priced at $15 each, will run on a Radio Shack TRS-80 with Level II BASIC, an Apple II, or a Commodore PET or CBM, each with 16 K bytes or more of free memory. Avalon-Hill's address is 4517 Harford Rd, Baltimore MD 21214.

In addition, The Software Exchange, 6 South St, POB 68, Milford NH 03055, has three war games on cassette for the TRS-80 running Level II BASIC: *Kriegspiel II*, *Up Periscope*, and *Warpath*; price is $14.95 each.

Strategic Simulations, 450 San Antonio Rd, Suite 62, Palo Alto CA 94306, offers two games, *Computer Bismarck* ($49.95 for the TRS-80 and $59.95 for the Apple II) and *Computer Ambush*, a World War II war game ($59.95 for the Apple II). ■

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[1]One reader-noted impression in the average McGraw-Hill publication. [2]The Dartnell Institute of Business Research. [3]"Telephone Marketing" by Murray Roman. P. 87, McGraw-Hill 1976. [4]Laboratory of Advertising Performance Report #8013.4, McGraw-Hill Research.

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Software Received

The following is a list of software packages that have been received by BYTE Publications during the past month. The list is correct to the best of our knowledge, but it is not meant to be a full description of the product or the forms in which the product is available. In particular, some packages may be sold for several machines or in both cassette and floppy-disk format; the product listed here is the version received by BYTE Publications.

This is an all-inclusive list that makes no comment on the quality or usefulness of the software listed. We regret that we cannot review every software package we receive. Instead, this list is meant to be a monthly acknowledgement of these packages and the companies that sent them. Companies sending software packages should be sure to include the list price of the packages and (where appropriate) the alternate forms in which they are available.

Unless otherwise listed, "floppy disk" refers to a 5-inch single-sided, single-density floppy disk; "TRS-80" refers to a Radio Shack TRS-80 Model I; and "Apple II" refers to the Apple II, the Apple II Plus, or the Apple III running in Apple II emulation mode.

Address Book, address and mailing label utility for the Apple II, floppy disk, $49.95, from MUSE Software, 330 N Charles St, Baltimore MD 21201.

Adventure, game for the TRS-80 (other versions exist), floppy disk, $29.95, from Microsoft Consumer Products, 10800 NE 8th Ave, Suite 819, Bellevue WA 98004.

APL80, subset of APL (programming language) for the TRS-80, floppy disk (available on tape), $39.95, from Ramware, 6 South St, Milford NH 03055.

Computer Bismarck, computer-assisted war game for the Apple II (version for TRS-80 also exists), floppy disk, $59.95, from Strategic Simulations, 450 San Antonio Rd, Suite 62, Palo Alto CA 94306.

Death Dreadnought, adventure game for the TRS-80, floppy disk, $14.95, from The Programmer's Guild, POB 66, Peterborough NH 03458.

EasyWriter, word-processing system for the Apple II, floppy disk, $99.95, from Information Unlimited Software, 793 Vincente Ave, Berkeley CA 94707.

Editor/Assembler-Plus, Z80 assembler and editor for the TRS-80, cassette, $29.95, from Microsoft Consumer Products (see above).

Elementary Math, arithmetic tutorial for the Apple II, floppy disk, $39.95, from MUSE Software (see above).

Higher Text, character font generator for the Apple II, $35, from Synergistic Software, 5221 120th Ave SE, Bellevue WA 98006.

IRV, keyboard shorthand utility for the TRS-80, cassette, $25, from The Programmer's Guild (see above).

Level III BASIC, utility for the TRS-80, cassette, $49.95, from Microsoft Consumer Products (see above).

Lost Dutchman's Gold, adventure game for the TRS-80, floppy disk, $14.95, from The Programmer's Guild (see above).

Odyssey, adventure game for the Apple II, floppy disk, $30, from Synergistic Software (see above).

Sargon II, chess-playing program for the TRS-80, floppy disk, $34.95, from Hayden Book Company, 50 Essex St, Rochelle Park NJ 07662.

SAT TRAK, graphic satellite observation program for the Apple II (other versions available), floppy disk, $45, from SAT TRAK International, Computerland of Colorado Springs, 4543 Templeton Gap Rd, Colorado Springs CO 80909.

SL5, version of FORTH (programming language) for selected CP/M machines, 8-inch floppy disk, $150, from The Stackworks, POB 1596, 321 E Kirkwood Ave, Bloomington IN 47402.

Softronics APL, programming language for any CP/M machine, 8-inch floppy disk, $350, from Softronics, 36 Homestead Ln, Roosevelt NJ 08555.

Spider Mountain Adventure, game for the TRS-80, floppy disk, $14.95, from The Programmer's Guild (see above).

Stellar Trek, graphics game for the Apple II, floppy disk, $24.95, from Rainbow Computing Inc, 9719 Reseda Blvd, Northridge CA 91324.

Typing Tutor, educational package for the TRS-80, cassette, $14.95, from Microsoft Consumer Products (see above).

Write-On I, word-processing system for the Apple II, floppy disk, $99.50, from Rainbow Computing Inc (see above). ■

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Clubs and Newsletters

Software Exchange for PDP-11 Users

A free software exchange service is available to Digital Equipment Corporation PDP-11 users. This service allows the user to submit software for software credits that may be used to obtain other software listed in the *Monthly Software Exchange Bulletin*. Write to the PDP-11 Software Exchange, 1101 Noble Forest Dr, Norcross GA 30092.

The Maryland Apple Corps

The Maryland Apple Corps now has over fifty members. Hardware and software demonstrations, program exchanges, bugs and fixes, and new uses of the Apple computer are interests of the group. A monthly newsletter, a software library, and membership in Apple International are also features of the group. The annual fee is $12. For information, contact Maryland Apple Corps, POB 5430, Towson MD 21204, Atten: Art Blumberg.

North Star Users Group

The North Star Users Group of the Boston Computer Society will hold meetings at 7:30 PM on the second Thursday of odd-numbered months, starting in November. The meetings will be held at the Computer Mart, 1395 Main St, Waltham MA. Contact Gary Saxton at (617) 861-6600, extension 2707.

REM Interest Group

A REM (Recognition Memory) Interest Group has been formed. The group is soliciting articles, information, and ideas from REM users for its newsletter. Initial dues are $10 payable to REM Interest Group, POB 23317, Honolulu HI 96822.

VTOS Group

TCUG Inc, a nonprofit computer club, is organizing and chairing a national users group for TRS-80 owners using the Virtual Technology Operating System (VTOS). The purpose of the group is to improve upon the documentation of VTOS by sharing knowledge derived from experience with VTOS. There is a $15 annual fee to join the VTOS Users Group, which entitles the member to the newsletter. Contact TCUG Inc, VTOS Sub-Group, POB 2235, Reston VA 22090, Attn: Bill Beall. The TCUG Bulletin Board is available at (703) 620-4990.

National Association of Computer Stores

The National Association of Computer Stores, a trade association representing retail computer stores, has recently been formed with the assistance of IntraCom Inc, an association and organizational management firm. The purposes of the trade association are to ensure prosperity and expansion of stores, to cooperate with applicable government agencies and legislative bodies, and to represent and advance the economic and educational interests of retail computer stores. Information is available from National Association of Computer Stores, 3255 S US 1, Ft Pierce FL 33450, (305) 465-9450.

Detroit Interact Group

Interact Electronics Corporation went out of business in early 1980, with over 5000 Interact systems in use and over 1000 on dealers' shelves. In order to see that these owners get support, the Detroit Interact Users Group has gone national. They encourage development of new software and hardware by independent sources. A monitor and a serial port are now available because of this group's efforts. The group also supports a software library. They are trying to locate schematics, documentation, and reliable sources for software, parts, and service for the Interact. The club newsletter, *Interaction*, is bimonthly with information, ideas, and programs. Contact Detroit Interact Group, 15356 Prevost, Detroit MI 48227. ■

Books Received

The following is a list of books received at BYTE Publications during this past month. Although the list is not meant to be exhaustive, its purpose is to acquaint BYTE readers with recently published titles in computer science and related fields. We regret that we cannot review or comment on all the books we receive; instead, this list is meant to be a monthly acknowledgement of these books and the publishers who sent them.

The Architecture of Microcomputers, S E Greenfield; Winthrop, Cambridge MA, 1980; 18.5 by 24.5 cm, 366 pages, hardcover, ISBN 0-87626-037-7, $24.95.

Basic Computer Programs in Science and Engineering, Jules H Gilder; Hayden Book Company, Rochelle Park NJ, 1980; 18 by 25 cm, 256 pages, softcover, ISBN 0-8104-0761-2, $8.95.

Computer Logic, Testing, and Verification, J Paul Roth; Computer Science Press, Potomac MD, 1980; 16 by 24.5 cm, 176 pages, hardcover, ISBN 0-914894-62-5, $23.95.

Digital Computer Simulation, Fred J Maryanski; Hayden Book Company, Rochelle Park NJ, 1980; 15.5 by 23 cm, 336 pages, softcover, ISBN 0-8104-5118-2, $15.95.

Digital Hardware Design, John B Peatman; McGraw-Hill Book Company, New York NY, 1980; 18 by 25 cm, 438 pages, hardcover, ISBN 0-07-049132-1, price not available at this time.

Dr Dobb's Journal of Computer Calisthenics & Orthodontia: Running Light Without Overbyte, The People's Computer Company Series, Hayden Book Company, Rochelle Park NJ, 1980; 21 by 28 cm; volume 1: 368 pages, ISBN 0-8104-5475-0; volume 2: 480 pages, ISBN 0-8104-5484-X; volume 3: 480 pages, ISBN 0-8104-5490-4; softcover, $18.95 each.

An Introduction to Microcomputers: Volume 1 Basic Concepts, Adam Osborne; Osborne/McGraw-Hill, Berkeley CA, 1980; 19 by 23 cm, 480 pages, softcover, ISBN 0-931988-34-9, $12.50.

Mathematical Modeling with Computers, Samuel L S Jacoby, Janusz S Kowalik; Prentice-Hall, Englewood Cliffs NJ, 1980; 16 by 23.5 cm, 292 pages, hardcover, ISBN 0-13-561555-0, $21.50.

Microcomputer Management and Programming, Carol Anne Ogdin; Prentice-Hall, Englewood Cliffs NJ, 1980; 18.5 by 24.5 cm, 348 pages, softcover, ISBN 0-13-580936-3, $16.95.

Microprocessors and Logic Design, Ronald L Krutz; Wiley & Sons, New York NY, 1980; 15.5 by 23.5 cm, 467 pages, hardcover, ISBN 0471-02083-4, $24.95.

Microprocessor Software Design, Max Schindler; Hayden Book Company, Rochelle Park NJ, 1980; 22 by 28 cm, 304 pages, softcover, ISBN 0-8104-5190-5, $11.95.

The Practical Guide to Structured Systems Design, Meilir Page-Jones; Yourdon Press, New York NY, 1980; 15.5 by 23 cm, 354 pages, softcover, ISBN 0-917072-17-0, $19.50.

Programmable Pocket Calculators, Mullish, Kochan; Hayden Book Company, Rochelle Park NJ, 1980; 15.5 by 23 cm, 264 pages, softcover, ISBN 0-8104-5175-1, $8.95.

TRS-80 BASIC; A Self-Teaching Guide, Albrecht, Inman, Zamora; Wiley & Sons Inc, New York NY, 1980; 18.5 by 23.5 cm, 351 pages, softcover, ISBN 0-147-06466-1, $8.95. ■

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The PMC-80 is a "work-alike" computer to the popular TRS-80* Model I, Level II by Tandy, Radio Shack. The PMC-80 has 16K bytes of RAM and the complete Level II 12K BASIC ROM by Microsoft that makes it 100% software compatible with programs from Radio Shack and from the hundreds of other independent suppliers. The built-in cassette player reads standard Radio Shack programs for the TRS-80.*

Sold through computer stores.

The PMC-80 will operate with any of the many peripherals Radio Shack and other independent vendors have invented to plug into the TRS-80.* Most importantly, the Interface Adapter permits Expansion Interfaces with memory expansion to 48K to be added. An Expansion Interface will also permit the addition of Radio Shack compatible 5¼″ disks and disk operating systems, RS 232, printers, etc.

*TRS-80 is a registered trademark of Tandy, Radio Shack.

Personal Micro Computers, Inc.
475 Ellis Street, Mountain View, CA 94043 (415) 962-0220

Circle 175 on inquiry card.

Book Reviews

Structured Programming

by O J Dahl, E W Dijkstra and C A R Hoare, Academic Press, London, 1972 Hardcover, 220 pages $18.00

The term "structured programming" is no longer novel. If you were to encounter this slender volume on a bookstore shelf, you might easily pass it by as yet another how-to book, and a not very eye-catching one at that. In reality, this book is a collection of brilliant ideas about program construction, program structure, and data structuring by three internationally renowned computer scientists. *Structured Programming* is already a classic in computer science literature and should be read by everyone seriously interested in programming.

Structured Programming is a collection of three essays. The first is Dijkstra's "Notes on Structured Programming." These notes were first circulated in mimeograph form and were the intellectual catalyst for almost the entire structured programming viewpoint. The essay itself is a collection of short notes concerning topics such as program structures, proving the correctness of programs, stepwise program composition, and many more. The concepts are exemplified by many exercises and examples which are themselves quite challenging and thought provoking. One of the more interesting examples is Dijkstra's solution to the *eight-Queens problem.*

Whereas Dijkstra's essay will strike many resonant chords for those already familiar with structured approaches to programming, Hoare's essay will have an air of familiarity for Pascal programmers. Hoare's "Notes on Data Structuring" is a brilliant analysis of the concept of abstract data types in programming. Hoare advocates the use of high-level data abstractions. He systematically examines unstructured or scalar data types such as enumerated sets and subranges. Next he discusses structured or compound data types (called structures in many languages) such as the Cartesian product, the discriminated union (variant records), the array (in a very generalized form), and the power-set. Finally, he treats more complex data types such as sequences, recursive data structures, and sparse data structures. He introduces the basic concepts for each data type and a notation for syntactic expression. He discusses the general operations that can be performed on each data type and discusses suggestions for achieving workable and efficient data representations and operations.

Hoare's stated objective is not simply to create another programming language that tries to include all data types and operations. Instead, he endeavors to give the reader an understanding of data abstraction. Hoare's suggestion is that the reader adopt and adapt his notation for use as a personal pseudolanguage in the initial stages of top-down design. By keeping the data objects in an abstract, conceptually meaningful form and by delaying choice of representation until later in the design several advantages are obtained. A program expressed in a high-level abstract language is more easily read and understood. Details of the algorithm can be worked out at an abstract level which facilitates ensuring the correctness of the algorithm. Finally, alternative representations for the data objects can be explored without the basic algorithm being changed. In essence, the use of abstract data types represents a stepwise refinement of the algorithmic code.

The final essay, "Hierarchical Program Structures," is coauthored by Dahl and Hoare. This essay represents a synthesis of the ideas from the previous two essays. Although not as clearly written as the other two essays, it discusses the ideas on structured programming presented in the others by showing how they are achieved in the SIMULA language. The most enlightening part of this essay is the description of SIMULA. SIMULA is a powerful general-purpose programming language derived from ALGOL 60 that introduces several novel programming concepts. The most important of these is the "class" concept. Classes are a means for creating not only abstract data objects but also the operations for manipulating them. This idea of providing a means within a language for creating new data objects and operations has been refined and incorporated into many of the most modern programming languages.

Structured Programming will introduce you to a wealth of excellent ideas about programming and program construction. It's a book that not only belongs on every serious programmer's library shelf, but belongs among those volumes that become worn from repeated reading. ■

Glen A Taylor
19 June Pl
Mattawan NJ 07747

BYTE's Bugs

It's Greek to Me!

An error of character substitution took place in a figure in Steve Ciarcia's article "A Build-It-Yourself Modem for Under $50" (August 1980 BYTE, pages 22 thru 38).

In figure 3 on page 32, two equations should have contained lowercase Greek omega "ω" characters; lowercase Roman-alphabet "w" characters were substituted.

The proper form of the center-frequency equation is:

$$\omega^2_0=1/R_3C^2(1/R_1+1/R_2).$$

The proper form of the equation under the op amp in the schematic diagram is:

$$\omega_0=2\pi f_0.$$

The center-of-passband frequency of the "typical bandpass filter response curve" in the graph should have been indicated by ω_0 not w_0.

Data Flub on the Dubber

The price for the Data Dubber in the "What's New?" section of the July 1980 BYTE, page 251, should have read $49.95, not $39.95.

Mix-uprocessors

The August 1980 BYTE "In The Queue" page lists Theron Wierenga's video terminal as based on the Zilog Z80. The project actually uses an Intel 8085. ■

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Programming Techniques is a series of collected articles concerned with the art and science of computer programming. The first volume in the Programming Techniques series is entitled **Program Design.** The purpose of the book is to provide the personal computer user with the techniques needed to design efficient, effective, maintainable programs.
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Simulation is the second volume in the Programming Techniques series. Both theoretical and practical applications are included. Particularly stressed is simulation of motion, including wave motion and flying objects, and the use of simulation for experimentation.
ISBN 0-07-037826-6 Pages: 126
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Numbers in Theory and Practice is the third book in the series. It includes information of value to both the novice and the experienced personal computer user. The mechanics of the binary system are discussed, including software division and multiplication, as well as floating point numbers, numerical methods, random numbers, and the mathematics of computer graphics.
ISBN 0-07-037827-4 Pages: 192
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The 4th volume of the Programming Techniques series, **Bits and Pieces,** covers various topics of interest to programmers. It is a collection of the best articles from past issues of BYTE magazine plus new material collected specifically for the series, on subjects such as multiprogramming, stacks, interrupts optimation, and real time processing.
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Event Queue

October 1980

October-November

Thinking Small—Using Small Computers to Increase Business Productivity. These conferences will feature leading authorities and small-business computer users in a program designed to explore the opportunities presented by small computers for productivity improvement of the small business. For a schedule of times and places, contact The Information Exchange, 1730 N Lynn St, Suite 400, Arlington VA 22209, (703) 521-6209.

October-December

APL Classes. STSC Inc has announced its fall schedule of classes and seminars in APL and related applications. Financial planning, manufacturing and materials management, insurance analysis, and data-base design and management will be covered. Classes will be held in major cities in the US and Europe. Contact Joan Gurgold, STSC seminar manager, 11 Clearbrook Rd, Elmsford NY 10523, (914) 347-5560.

October-December

Hartford Graduate Center Courses, Hartford CT. Assembly language, minicomputers, Pascal, microprocessors, and computer-aided graphics are courses being offered by the Hartford Graduate Center, 275 Windsor St, Hartford CT 06120, (203) 549-3600, extension 254 or 252.

October-December

Fairchild's Microcomputer Education Center, San Jose CA. A series of technical training courses are offered for design engineers who must learn to incorporate the microprocessor into a working system. The curriculum includes courses on data communications and the 6856, the 3870 single integrated circuit microcomputer and its family, 6800 microprocessors, bit slice techniques. Contact the Center at MS 42-2120, 101 Bernal Rd, San Jose CA 95119, (408) 224-7096.

October-January 1981

Twenty-nine Seminars from DPMA Education Foundation. The Data Processing Management Association (DPMA) is sponsoring a series of two-day computer-oriented seminars. Data processing, software configuration management, computer-aided design and manufacturing, computers and data communications, data base, integrated circuits, and software engineering are some of the topics being covered. For details on site locations and times, contact DPMA Education Foundation Coordinator, 5959 W Century Blvd, Los Angeles CA 90045, (213) 670-2975.

October 1-2

Choosing and Using Microprocessor Development Systems, London Press Centre, London EC4, England. The seminar will present information and practical experience on which to base the selection and use of microprocessor development systems. It will provide guidelines to answer questions on the definition of microprocessor development systems, what features should be looked for, how to analyze particular requirements, and what systems are commercially available. The program is intended for senior engineers and engineering managers who have some knowledge of microprocessors. Contact the Conference and Course Unit, Sira Institute Ltd, South Hill, Chislehurst, Kent BR7 5EH, England.

October 1-3

The Tenth International Symposium on Fault-Tolerant Computing, Kyoto, Japan. This meeting is devoted to the theory and practice of reliable computing and will cover design of fault-tolerant circuits and sytems; analysis of system performance and reliability; applications of coding techniques; software reliability and testing; and more. For information and traveling arrangements, contact Secretary of FTCS-10, Dept of Applied Mathematics and Physics, Faculty of Engineering, Kyoto University, Kyoto 606, Japan.

October 6-7 and October 8-10

Microprocessor-Based Equipment Design and Development, Cudham Hall, Cudham, Sevenoaks, Kent, England. Contact Sira Institute Ltd, South Hill, Chislehurst, Kent BR7 5EH, England, for information on this two-part course.

October 6-8

APL Users Meeting, Toronto, Ontario, Canada. This conference is aimed at APL users as well as those considering the use of APL in their systems. Speakers will present papers that discuss the practical use of APL. Managing APL resources, teaching APL, and APL programming techniques will be covered. The registration fee is $180 (in Canadian funds), which includes a copy of the proceedings. For a brochure and registration material, contact Rosanne Wild, I P Sharp Associates Ltd, 145 King St W, Toronto, Ontario M5H 1J8, Canada.

October 8-10

Circulation Computer Systems Symposium, Chicago Marriott Hotel, Chicago IL. More than 425 newspaper publishers, general managers, circulation directors, controllers, and data-processing managers are expected to attend. Workshop sessions will be held for participants who already have or are considering automated circulation systems. For more information, contact American Newspaper Publishers Association, The Newspaper Center, POB 17407, Dulles Airport, Washington DC 20041, (703) 620-9500.

October 14-16

Minicomputer and Microcomputer Conference and Exposition, Brooks Hall/Civic Auditorium, San Francisco CA. For complete details, contact the Managing Director, Mini/Micro Conference and Exposition, 32302 Camino Capistrano, Suite 202, San Juan Capistrano CA 92675, (714) 661-3301.

October 16-19

Midwest Computer Show McCormick Place, Chicago IL. Admission for adults is $5. For more information on the exposition, contact National Computer Shows, POB 678, Brookline Village MA 02147, (617) 739-2000.

October 20-22

Applied Microprocessors: A Basic Introduction, University of Houston Hotel, Houston TX. For information on the course, contact the Continuing Education Institute, 10889 Wilshire Blvd, Suite 1030, Los Angeles CA 90024, (213) 477-8379.

October 26-28

The Eleventh ACM North American Computer Chess Championship, Opryland Hotel, Nashville TN. This is a four-round, Swiss-style tournament with participation restricted to computers. All of the best chess programs in North America are expected to be present. A maximum of twelve teams will participate. Contact Monty Newborn, School of Computer Science, McGill University, 805 Sherbrooke St W, Montreal, Quebec, H3A 2K6, Canada, (514) 392-8274.

October 26-29

International Data-Processing Conference and Business Exposition, Philadelphia Sheraton Hotel, Philadelphia PA. This conference is being sponsored by the Data Processsing Management Association (DPMA). Contact the Conference Coordinator, DPMA International Headquarters, 505 Busse Hwy, Park Ridge IL 60068, (312) 825-8124.

October 27-29

Fundamentals of Data Communications, New York NY. This course is designed for personnel who want an introduction to data communications concepts and systems. The course covers all the elements of data communications systems. Contact American Management Associations, 135 W 50th St, New York NY 10020, (212) 246-0800.

October 27-30

The Fifth International Conference on Computer Communication, Peachtree Plaza Hotel, Atlanta GA. The theme for ICCC/80 is "Computer Communications: Increasing Benefits for Society." More than 100 speakers will present papers on applications and technical developments of computer communication and its worldwide implications for the 1980s. Fees are $175 for pre-registration and $200 at the conference. Contact ICCC/80, POB 280, Basking Ridge NJ 07920, (201) 221-8800.

November 1980

November 8-9

Personal Computer Fair, Pacific Science Center, Seattle WA. The theme of this year's fair is "Hands On." The booths and exhibits will reflect this idea, and the public will have access to as many computers and terminals as possible. Contact The Northwest Computer Society, POB 4193, Seattle WA 98119, (206) 284-6109.

November 10-14

The Fourth Annual Data-Entry Management Conference, Orlando FL. This conference will cover data entry, distributed processing, and word processing with emphasis on data entry, including human-machine interface. Contact Data Entry Management Association, POB 3231, Stamford CT 06905, (203) 322-1166.

November 11-13

Canadian Computer Show and Conference, International Centre, 6900 Airport Rd, Toronto, Ontario, Canada. For information, contact the Show Manager, Industrial Trade Shows of Canada, 36 Butterick Rd, Toronto, Ontario M8W 3Z8, Canada, (416) 252-7791.

November 13-16

The 1980 International Computer Music Conference, Queens College, Flushing NY. This conference is for persons interested in computer applications in music. Conference activities include presentation of papers, concerts, workshops, panel discussions, meetings of special interest groups, demonstrations, and an exhibition of computer music equipment. For information, contact Dr Hubert S Howe Jr, Director 1980 International Computer Music Conference, Queens College, Flushing NY 11367, (212) 520-7340.

November 18-20

The Third Industrial Revolution, McCormick Place, Chicago IL. This show is an exposition and conference devoted to development by manufacturing companies of systems for information management. Information may be obtained from Banner and Grief Ltd, 110 E 42nd St, New York NY 10017, (212) 687-7730.

November 19-21

Comdex, Las Vegas Convention Center, Las Vegas NV. Comdex is a conference and exposition for independent sellers of small-computer and word-processing systems, peripherals, media, and supplies. Address inquiries to The Interface Group, 160 Speen St, Framingham MA 01701, (800) 225-4620.

November 20-21

Western Educational Computing Conference, San Diego CA. This conference will feature papers and seminars on the use of computers in higher education for instruction, administration, and research. Contact Ron Langley, Director, Computer Center, California State University, Long Beach, 1250 Bellflower Blvd, Long Beach CA 90840, (213) 498-5459.

November 20-23

Northeast Personal and Business Computer Show, Hynes Auditorium, Boston MA. This is an annual exposition open to the general public. The admission will be $5. Contact National Computer Shows, POB 678, Brookline Village MA 02147, (617) 739-2000.

November 21-23

National Home Entertainment Show, New York Coliseum, New York NY. Exhibits will cover video, photography, audio, games, and home computers. Seminars and demonstrations will be featured in this show. Contact United Business Publications Inc, 475 Park Ave South, New York NY 10016, (212) 725-2300.

December 1980

December 2-5

The Eleventh International Conference of the Computer Measurement Group, Sheraton-Boston Hotel, Boston MA. This conference is entitled "Computer Performance Evaluation in the 80s." Contact Judith G Abilock, Price Waterhouse & Company, Office of Government Services, 1801 K St, NW, Washington DC 20006, (202) 296-0800.

December 3-5

The 1980 Winter Simulation Conference, Orlando Marriott, Orlando FL. This conference will feature papers, panel discussions, tutorials, and review sessions on discrete and combined simulations. Contact Professor Tuncer I Ören, Chairman, Dept of Computer Science, University of Ottawa, Ottawa, Ontario K1N 9B4, Canada, (613) 231-5420.

December 4

California Computer Shows, Hyatt-Palo Alto, Palo Alto CA. Show hours are from 1 to 7 PM. OEM (original equipment manufacturers) and end-user computer and peripheral products will be exhibited and demonstrated by over 60 companies. Contact Norm De Nardi Enterprises, 95 Main St, Los Altos CA 94022, (415) 941-8440.

December 10

1980 Computer Networking Symposium, Gaithersburg MD. This symposium is sponsored by the IEEE Computer Society, Technical Committee on Computer Communications, and the Institute for Computer Sciences and Technology of the National Bureau of Standards. The focus is on office automation, office system components, and the computer networks required to interconnect them. For information, contact Executive Secretary, POB 639, Silver Spring MD 20901, (301) 439-7007. ■

In order to gain optimal coverage of your organization's computer conferences, seminars, workshops, courses, etc, notice should reach our office at least three months in advance of the date of the event. Entries should be sent to: Event Queue, BYTE Publications, 70 Main St, Peterborough NH 03458. Each month we publish the current contents of the queue for the month of the cover date and the two following calendar months. Thus a given event may appear as many as three times in this section if it is sent to us far enough in advance.

What's New?

MISCELLANEOUS

High-Speed Cassette for the TRS-80

The TC-8 allows the TRS-80 user to load programs five times faster than the standard cassette recorder allows. It runs at over 3000 bps (bits per second) with an error rate of less than one bad load in a million bytes, with the volume control anywhere between two and eight. The TC-8 cassette recorder supports the saving, loading, and verifying of BASIC programs, system programs, and data files. Features of this system include eight-character names for files and the ability to list the directory of all files on a tape. It is available in kit form for $90 and fully assembled for $120 from J P C Products Company, 12021 Paisano Ct, Albuquerque NM 87112, (505) 294-4623.

Circle 609 on inquiry card.

Microplot 44

The Microplot 44 is a 44-column fixed-head thermal graphic printer for use with microprocessor-based systems. The printer features individual dot addressing, enhanced vector plotting, 256-dot resolution, manual and programmable mode selection, 96-character ASCII double-height and double-density characters, programmable tabs, and IEEE-488 and RS-232 interfaces. The price is under $1000 from Gulton Industries Inc, Measurement and Control Systems Division, Gulton Industrial Park, East Greenwich RI 02818, (401) 884-6800.

Circle 610 on inquiry card.

Heavy-Duty Printer from TEI

TEI Inc, 5075 S Loop E, Houston TX 77033, (713) 738-2300, has announced its Model 3431 heavy-duty, 150 cps (characters per second), dot-matrix printer. The printer offers up to 136-column printing using a 9-by-7 dot format to form ninety-four ASCII (American Standard Code for Information Interchange) characters, including lowercase letters with descenders, symbols, double-wide characters, and more. It also offers bidirectional printing. The pin-feed tractor accepts continuous and multipart forms. A parallel interface is standard and RS-232 serial interfaces are available. The unit price is $1695.

Circle 611 on inquiry card.

1 to 1000 MHz Signal Generator

The Wavetek Model 3010 Signal Generator covers the entire frequency spectrum from 1 to 1000 MHz. It features 100 Hz resolution, 0.001% accuracy, complex modulation capabilities, and four internal modulation frequencies. Also featured are standard frequency programmability, Vernier controls for frequency and output level, and four FM (frequency modulation) and two AM (amplitude modulation) modulation scales. RF (radio frequency) power level is +13 to -137 dBm. Flatness is ±0.75 dBm. Frequency is set via seven lever/indicator switches to a resolution of 100 Hz. The Model 3010 is useful for tests of two-way radio, mobile telephones, paging receivers, and other systems that utilize techniques which superimpose subaudible tones or tone-coded signals on voice or other channels. The price is $4750, from Wavetek Indiana Inc, 66 N First Ave, POB 190, Beech Grove IN 46107, (317) 783-3221.

Circle 612 on inquiry card.

Computer System from GNAT

The System 10, developed by GNAT Computers Inc, features a Z80 processor, 64 K bytes of programmable memory, 700 K bytes of floppy-disk storage, a hard-disk interface, a DMA (direct memory address) controller, interrupt controller, and three serial I/O (input/output) channels. The system can also be configured with a 9511 arithmetic processor and an IEEE-488 GPIB interface. Software support consists of CP/M 2.0 and a screen editor. BASIC, FORTRAN, C, COBOL, Pascal, and other software are available. Application programs include word processing, accounting, and a mainframe telecommunication package. The price is $4950 from GNAT Computers Inc, 7895 Convoy Ct, Bldg 6, San Diego CA 92111, (714) 560-0433.

Circle 613 on inquiry card.

Where Do New Products Items Come From?

The information printed in the new products pages of BYTE is obtained from "new product" or "press release" copy sent by the promoters of new products. If in our judgement the information might be of interest to the personal computing experimenters and homebrewers who read BYTE, we print it in some form. We openly solicit releases and photos from manufacturers and suppliers to this marketplace. The information is printed more or less as a first in first out queue, subject to occasional priority modifications. While we would not knowingly print untrue or inaccurate data, or data from unreliable companies, our capacity to evaluate the products and companies appearing in the "What's New?" feature is necessarily limited. We therefore cannot be responsible for product quality or company performance.

MISCELLANEOUS

Ultraviolet EPROM Eraser

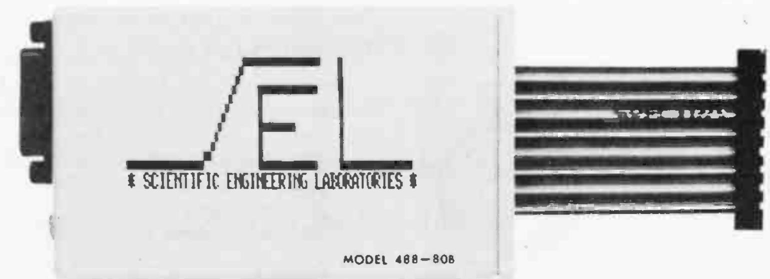
The QUV-T8 EPROM (erasable programmable read-only memory) eraser allows hobbyists to erase most industry standard ultraviolet EPROMs such as 2708, 2564, 2716, 2532, and 2704 series EPROMs. The device is capable of erasing up to twenty EPROMs at a time, with an erase time of approximately 25 minutes. The lamp has an estimated life of 7700 hours. It is available from Logical Devices Inc, 1525 N E 26th St, Ft Lauderdale FL 33305, (305) 566-6252.

Circle 619 on inquiry card.

Speech Circuits Offered by Texas Instruments

The TI TMS5000-series speech-processing integrated circuits provide one hundred words of synthetic speech, and cost approximately $13 in production quantities. Speech encoding on the TMS5100 speech synthesis circuit is achieved through pitch-excited Linear Predictive Coding (LPC). LPC is based on a linear equation to formulate a mathematical model of the human vocal tract and an ability to predict a speech sample based on previous ones. Codes for twelve synthesis parameters serve as inputs to the synthesizer device. Inputs to the digital filter take two forms: periodic and random. The periodic inputs are used to reproduce voiced sounds that have a definite pitch, such as vowel sounds or voiced fricatives such as Z, B, or D. A random input is used to model fricative sounds such as S, F, T, and SH. Output of the filter drives a converter, which in turn drives a speaker. The circuit can generate up to 10,000 speech samples per second. Contact Texas Instruments Inc, Inquiry Answering Service, POB 1443, M/S 653, Houston TX 77001.

Circle 620 on inquiry card.



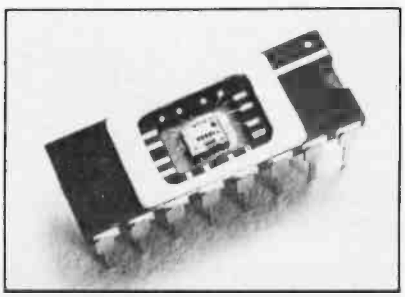
Interface Adaptor for the TRS-80

Scientific Engineering Laboratories, 11 Neil Dr, Old Bethpage NY 11804, (516) 694-3205, has announced a device for interfacing the GPIB-488 instrument-control bus to the TRS-80 Model I. The Model 488-80B enables a TRS-80 Model I with a minimum of 16 K bytes of programmable memory and Level II BASIC to be used as a GPIB-488 controller. A machine-level driver program that is provided with the unit interacts with Level II, Level III, or Disk BASIC. The price is $225.

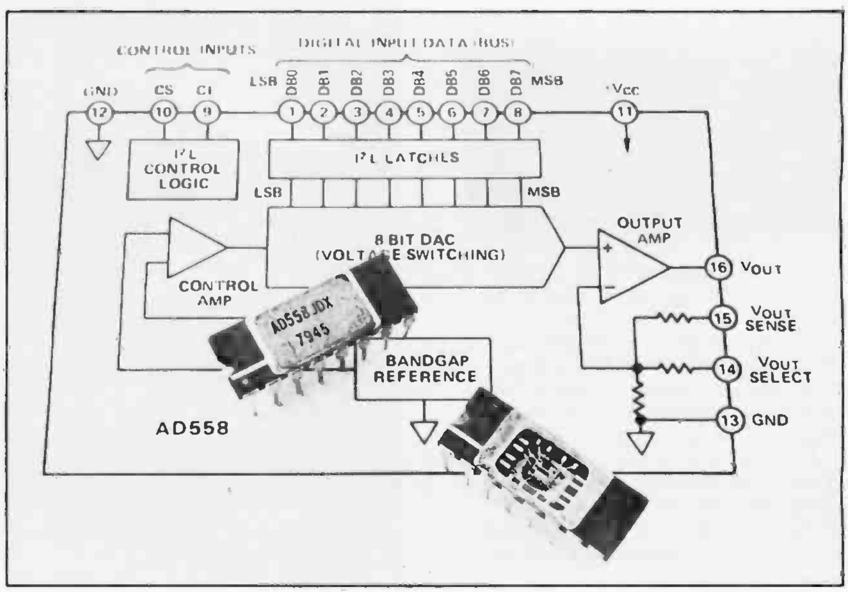
Circle 621 on inquiry card.

8-Bit D/A Converter

The AD558 D/A (digital-to-analog) converter features 1 ms maximum voltage output settling time and operation from a single +5 to +15 V supply. The monolithic device is guaranteed to operate accurately over its entire temperature range without any user-supplied trimming resistors. Two output ranges of 0 to 2.55 V and 0 to 10 V are pin selectable and require no external components. The AD558 is available in four grades and two package types featuring direct microprocessor interface capability. The prices start from $5.95 for single units in quantities of 100. Contact Analog Devices, Rt 1 Industrial Park, POB 280, Norwood MA 02062, (617) 329-4700.



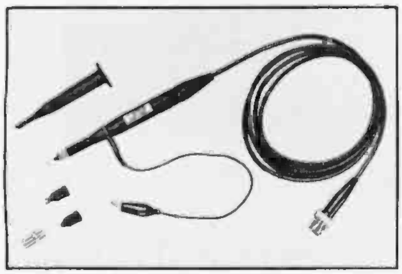
Circle 622 on inquiry card.



What's New?

MISCELLANEOUS

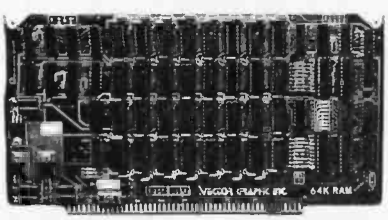
Instrument Probe from B & K



A wideband instrument probe has been announced by B & K-Precision/Dynascan Corporation, 6460 W Cortland St, Chicago IL 60635, (312) 889-9087. The Model PR-40 is designed for use with oscilloscopes and frequency counters in applications through 100 MHz. The PR-40 features a three-position switch which selects either a 10:1, direct mode, or a reference position that grounds the tip through a 9 megohm resistor. Accessories supplied include a spring-loaded retractable tip cover, insulating tip, a snap-on ground clip, BNC tip adapter, and an integrated circuit tip. The BNC adapter converts the probe tip into a push-on BNC connector for interfacing with test points or output jacks. The integrated circuit tip guide eliminates the possibility of shorting the pins of the circuit. The PR-40, with all the accessories, is priced at $34.

Circle 614 on inquiry card.

Two Products from Vector Graphic



The Vector Graphic MP is a 5-by-7 dot-matrix, software-driven printer that can print at a speed of 150 cps (characters per second). The price of the MP is under $1000 from Vector Graphic Inc, 31364 Via Colinas, Westlake Village CA 91361, (213) 991-2302. The Vector Graphic 64 K dynamic memory board is an 8-bit memory board which can be used with most Z80-based S-100 systems. The system offers bank selecting capability, allowing up to eight boards to be used in a system at the same time.

Circle 615 on inquiry card.

Small-C Compiler for CP/M Systems

The Small-C compiler from The Code Works is available to CP/M users on a single-density 8-inch floppy disk. The compiler supports a large subset of the C programming language, and provides an interface to assembly language. The disk includes an executable Small-C compiler, the complete source code for Small-C, and a demonstration program; the run-time support library and CP/M input/output functions as assembly-langauge source. The price is $15 including a manual. Contact The Code Works, POB 550, Goleta CA 93017, (805) 967-0905.

Circle 616 on inquiry card.

Switching Power Supply for Diablo Printers

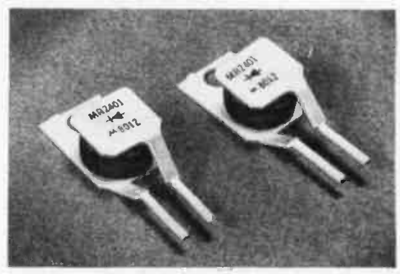
Boschert Inc, 834 Santa Trinita Ave, Sunnyvale CA 94086, (408) 732-2440, has introduced the OL 152, a power module for all Diablo printers. The OL 152 provides up to 170 watts of continuous power. Standard models are available in 110 and 220 V AC. Other standard features include reverse voltage protection, a series thermistor that reduces line surges at turn-on, and over-voltage and short-circuit protection. The OL 152 for 110 V AC lists for $179 in 1000-unit quantities, and the OL 152 for 220 V AC is $186 per unit for 1000 units.

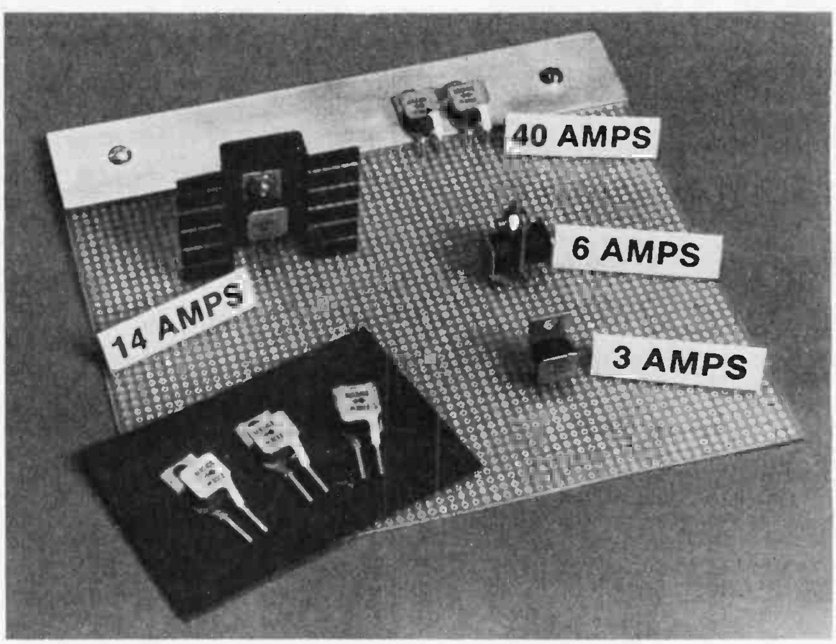
Circle 617 on inquiry card.

Standard and Fast Rectifiers from Motorola

The MR2400 series of TO-220 configured packages of standard and fast-recovery power rectifiers has been introduced by Motorola Semiconductor Products Inc, POB 20912, Phoenix AZ 85036, (602) 244-4624. The series ranges from 50 to 600 volts and can handle from 3 to 40 amps. The fast-recovery rectifiers are designed for applications such as switching power supplies, inverters, and converters. The fast-recovery types have a soft-recovery time of 200 ns maximum. The standard rectifiers are designed for applications requiring a high current surge. Prices range from $0.82 to $2 in quantities of 100.

Circle 618 on inquiry card.





What's New?

MISCELLANEOUS

Z8000 Business Computer

Onyx Systems Inc has introduced the Z8000 processor-based C8002 system. The C8002 supports eight users and both peripheral and communication devices; the computer supports a high-speed local network that allows many C8002s to be linked. The system combines Zilog's Z8000 16-bit microprocessor, a Winchester hard-disk drive, a cartridge tape drive, and up to 512 K bytes of programmable memory.

The Z8000 features 110 distinct instructions, eight addressing modes, and seven data types, including BCD (binary-coded decimal), string, and long word (32 bits). The main processor contains the Z8000 microprocessor, a direct memory address channel, serial and parallel I/O (input and output) ports, memory-management controller, floating-point processor, and support circuitry.

The operating system and all user programs are executed by the main processor. The mass-storage controller uses a Z80 processor and 64 K bytes of programmable memory to handle all disk and tape transactions. Bell Laboratories's UNIX timesharing operating system has been adapted for use on the C8002. This system enables users to share files, process text, and compile or execute programs written in BASIC, COBOL, FORTRAN, C, and Pascal. The C8002 is priced at $16,000. Write or call Onyx Systems Inc, 37 E Trimble Rd, San Jose CA 95131, (408) 946-6330.

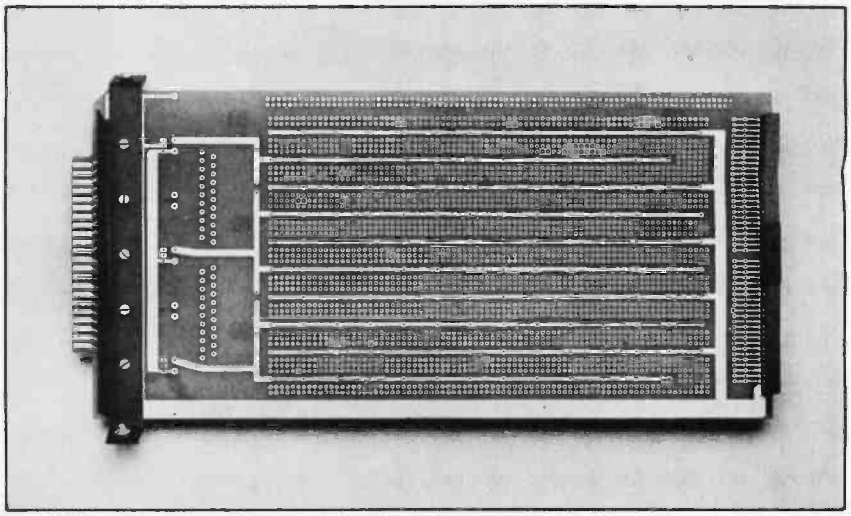
Circle 623 on inquiry card.

Memory Board for Heathkit/Digital H-11

The CI-1103 memory board is designed for the Heathkit/Digital H-11, LSI-11/2, and PDP-11/03 computers. The new memory features an 8 K by 16 bit (dual width) board using 200 ns 4027 (4 K by 1 bit) dynamic memory devices. The CI-1103 is available with either on-board distributed refresh or external refresh control logic. Data-access time is 300 ns, and cycle time is 525 ns. On-board memory-select is available in 2 K increments up to 128 K words of memory. Power consumption is under seven watts. The 8 K by 16 board is $390 and the 32 K by 16 board is $750. Contact Chrislin Industries Inc, 31352 Via Colinas #102, Westlake Village CA 91361, (213) 991-2254.

Circle 624 on inquiry card.

Prototype Board for the H-8 Bus



This prototype board will allow personal-computer users to build custom electronic interfaces for their Zenith/Heathkit H-8 personal computers. It is designed for use with a forty-four-pin edge-cable connector opposite the bus connector, or with many different Molex connectors from holes along the board top. There are locations for 3 V to 5 V regulators, with locations for two filter capacitors, and extra holes for other voltage regulators. The price is $46 per kit, from Mullen Computer Products, POB 6214, Hayward CA 94545, (415) 783-2866.

Circle 625 on inquiry card.

Office Computer Under $5000

The ALPHAsprint system includes 64 K bytes of programmable memory, a 45 K-byte display buffer, high-resolution 12-inch video display, and two double-density 5-inch floppy-disk drives capable of storing 330 K bytes of data. A Selectric II-type keyboard incorporates seventy-two character and function keys and a full numeric keypad. The optional 660-word-per-minute letter quality printer can be shared by up to three ALPHAsprints. Word-processing functions are oriented toward long document preparation. Other standard features include multispeed unlimited bidirectional scrolling, eight cursor commands, and intercharacter right justification. Printing functions are under program control. Editing can occur in the foreground while other documents are being printed in the background. Automatic centering, boldface, underline, automatic pagination and repagination are standard. Applications software and CP/M, BASIC, FORTRAN, COBOL, and Pascal are available. The single quantity price for the ALPHAsprint is $4990 from Alpha Professional Systems Inc, 9465 Wilshire Blvd, Suite 518, Beverly Hills CA 90212, (213) 272-3032.

Circle 626 on inquiry card.

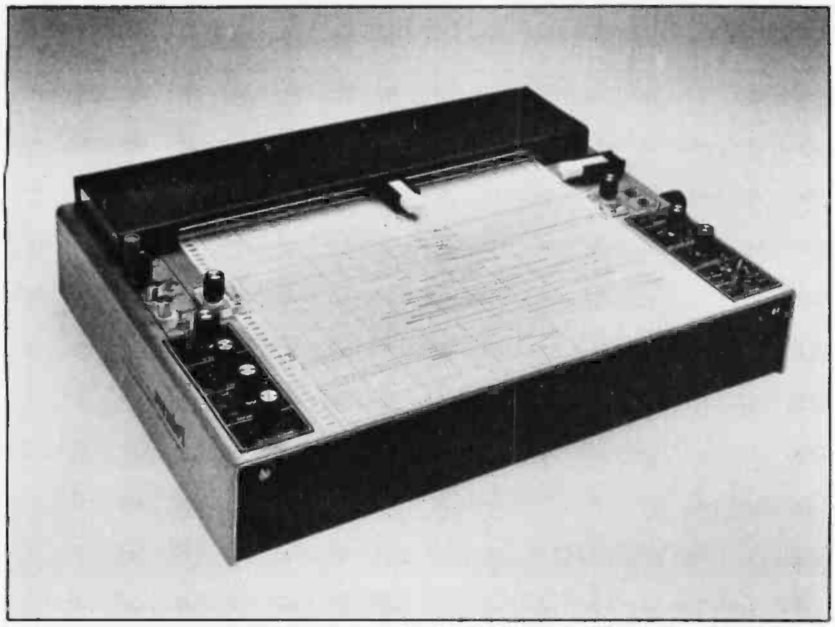
Direct Connect Modem for Multi- or Single-Line Phones

The D-CAT is an Federal Communications Commission (FCC) approved, Bell 103-compatible modem (modulator/demodulator) that can function on either a multi- or single-line phone. It works with a single-line phone or fifty-pin, six-line business phones. The modem offers full-duplex capability, a voice/data monitor, a hold function, privacy button, and self-test features. The unit has a mode switch to allow the user to monitor whether voice or data is being transmitted. The D-CAT is priced at $199 from Novation, 18664 Oxnard St, Tarzana CA 91356.

Circle 627 on inquiry card.

What's New?

MISCELLANEOUS



High-Speed Transient Recorder

The Model 57-TR is a transient recorder that provides hard-copy output of recurring or single-shot transients. With switch-selectable conversion rates from 50 to 200 Hz, the 57-TR will convert analog input data into 10-bit digital words. Upon receiving a preselected trigger signal, the recorder will plot the information which has been stored. The operator can use an oscilloscope to view the analog input signal prior to, during, or after recording. Additional features include plotting rates of 20, 50, or 100 words per second; ±trigger level control; variable input off-set of 0 to full scale; and chart speeds of 30 inches per minute when plotting. The list price is $3300 from Pedersen Instruments, 2772 Camino Diablo, Walnut Creek CA 94596, (415) 937-3630.

Circle 658 on inquiry card.

Books from Prentice-Hall

The list of computer books from Prentice-Hall includes *Structured System Programming; Software Development: A Rigorous Approach; 16-Bit Microprocessor Architecture; Microprocessors and Programmed Logic; Microcomputer Management and Programming*, and more. For information and a catalog, contact Prentice-Hall Inc, Englewood Cliffs NJ 07632.

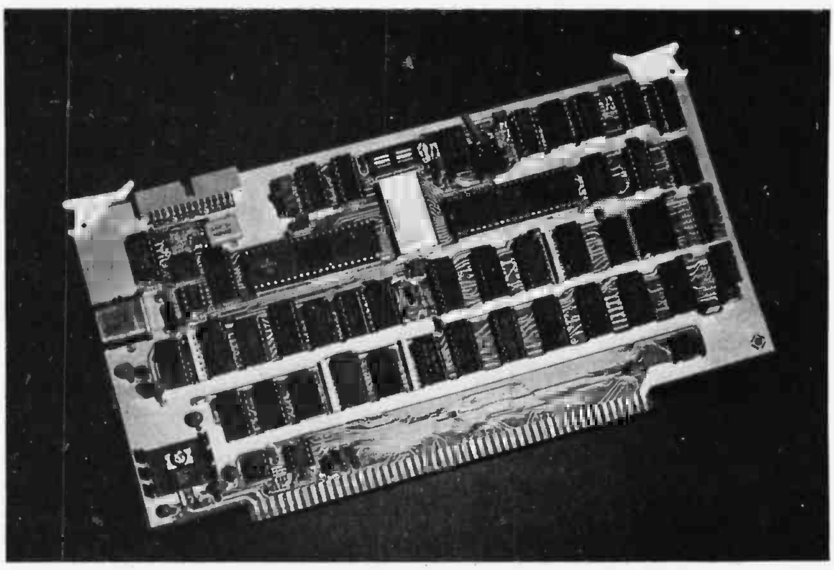
Circle 659 on inquiry card.

Graphics Terminal

A Tektronix Plot-10 software-compatible graphics terminal that provides four operating modes has been introduced by Continental Resources Inc, 175 Middlesex Tpk, Bedford MA 01730, (617) 275-0850. The Continental CPG-4010 graphics terminal provides automatic scaling to allow use of graphics, and compatible status read back that returns alpha cursor position and graphic status information upon receipt of an ESC ENQ. Using a Z80 microprocessor, the CPG-4010 operates in the ADM-3A Alpha, 4010 Alpha, vector, and point modes. Allowing full screen usage, the Plot-10 graphic grid is automatically scaled to the CPG-4010 grid. The terminal is priced at $1995.

Circle 660 on inquiry card.

Z80 Board from California Computer Systems



The 2810 Z80 single-board computer is designed for S-100 bus systems. It supports front panel operations and is fully compatible with the Altair and IMSAI computers. The board features easily selectable options including an RS-232 serial port that can be used for a console interface. Other options include I/O (input/output) address mirroring, a power-on jump to any location in memory, and wait states with optional wait state generation. Standard features for the 2810 include a 2 K-byte ROM (read-only memory) containing monitor firmware. A switch allows the user to select a clock rate of 2 or 4 MHz. The board also features microprocessor and data rate integrated circuits with separate crystal controls, and LEDs (light-emitting diodes) to indicate a Halt state, ROM enabled, and Interrupt enabled. The 2810 is available for $300 from California Computer Systems, 250 Caribbean Dr, Sunnyvale CA 94086, (408) 734-5811.

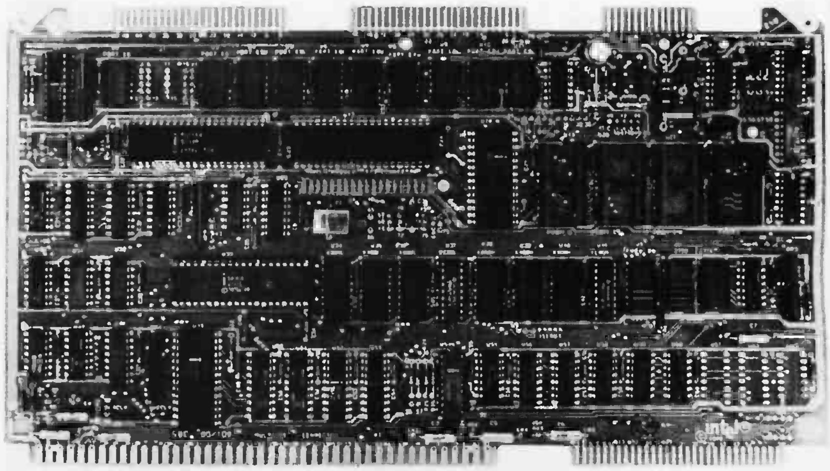
Circle 661 on inquiry card.

What's New?

SYSTEMS

Intel's iSBC 80/10B Single-Board Computer

The iSBC 80/10B is fully compatible with the 80/10A board from Intel, and is expandable from 4 K to 16 K bytes of EPROM (erasable programmable read-only memory) and ROM (read-only memory). One K bytes of programmable memory are included and may be extended up to 4 K bytes. The iSBX parallel 350 and serial 351 I/O (input/output) boards provide expansion identical to on-board I/O. Two programmable, 16-bit BCD (binary-coded decimal) and binary timers are available for general use. Another multimodule board is the floating-point math board. This unit is compatible with the IEEE (Institute of Electrical and Electronics Engineers) format and offers single- and double-precision arithmetic functions. The 80/10B system provides a battery backup in the event of a power failure.



The price for the board is $560. Prices for the parallel and serial I/O boards and the floating-point board range from $155 to $450. Contact Intel Corporation, 5200 NE Elam Young Pky, Hillsboro OR 97123, (503) 640-7147.

Circle 644 on inquiry card.

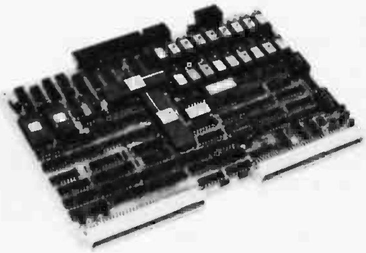
Vector System 2800 Makes Its Debut

The System 2800 consists of a Vector 3 terminal with the ZCB single-board computer, together with 64 K bytes of programmable memory, a floppy-disk controller, and a Flashwriter II video board featuring an 80-character by 24-line display. The second major feature is the Dualstor 8-inch floppy-disk drive unit, which has a total capacity of 2 megabytes. The formatting is IBM compatible. The drives have an access time of 91 ms and a transfer rate of 500 K bps (bits per second). The standard software on the system is CP/M. Microsoft BASIC-80, RAID debugger, SCOPE editor, and the five Peachtree Software accounting packages are optional. The suggested retail price for the System 2800 is $7295. Contact Vector Graphic Inc, 31364 Via Colinas, Westlake Village CA 91361, (213) 991-2302.

Circle 645 on inquiry card.

Zilog Introduces a Z8000 Board

A microcomputer board based on the Z8001 microprocessor is now on the market. The Z8000 board features 32 K bytes of programmable memory with parity protection, 8 K bytes of additional ROM (read-only memory) or PROM (programmable read-only memory) space, two communication channels, and a real-time clock. The Z8001 microprocessor is a segmented unit characterized by a 414-member instruction set. The Z8001 can address up to 8 megabytes of memory. In addition, the board employs the Z80A serial I/O controller to incorporate two serial channels. Each channel is individually programmable to support synchronous or asynchronous protocols, including IBM Bisync, SDLC, HDLC, and CCITT-X.25. Other features include a parity-error detection circuit, three types of interrupts, and three LEDs (light-emitting diodes) to indicate when the microprocessor is in system mode, WAIT state, and I/O reference. The Z8000 microprocessor board is priced at $2295. Other members of the family will be introduced later and are to include programmable memory, a single-board terminal, floppy-disk controller, and digital and analog I/O boards. For more information, contact Zilog, 10460 Bubb Rd, Cupertino CA 95014, (408) 466-4666.



Circle 646 on inquiry card.

System 80-W from NNC

NNC Electronics has recently announced its System 80-W computer, a complete S-100 system built around the newly released 10-megabyte Shugart 8-inch Winchester hard disk. The system includes a floppy-disk controller and one Shugart 801R double-density floppy disk, a two-board hard-disk controller, a Z80A microprocessor running at 4 MHz, 64 K bytes of bank-selectable dynamic memory, eight-level vectored interrupts, a real-time clock, three parallel ports with line drivers for interfacing to all parallel printers, and two RS-232C serial ports with complete handshaking and programmable data-transfer rates. In addition, the computer conforms completely to the IEEE S-100 bus standard. For more information, contact NNC Electronics, 15631 Computer Ln, Huntington Beach CA 92649.

Circle 647 on inquiry card.

Microsette Gets New Name and New Product

Microsette Company has changed its name to Personal Micro Computers Inc. One new product from Personal Micro Computers is Fastload, which is an interface between the Radio Shack CTR-41 cassette recorder and the TRS-80 parallel port. Fastload permits standard cassettes in BASIC or SYSTEM formats to be loaded at 8000 bps (bits per second), sixteen times faster than the usual rate. Personal Micro Computers Inc is located at 475 Ellis St, Mountain View CA 94043, (415) 968-1604.

Circle 648 on inquiry card.

What's New?

SOFTWARE

Real Estate Package for the TRS-80 and CP/M Systems

The Key Realty Management System is for TRS-80- and CP/M-based computers. The system includes listing control, escrow control, sales control, general ledger, and property management subsystems. Accounts payable and payroll are optional. The minimum system provides for up to 300 listings, 100 sales associates, and 10 offices. The entire package is $2500. Each subsystem is $500. Contact Key Systems Inc, 16 Ocean East, Marathon FL 33050, (305) 743-5890.

Circle 639 on inquiry card.

Pascal and FORTRAN for OSI Systems

Ohio Scientific, 1333 S Chillicothe Rd, Aurora OH 44202, (216) 831-5600, is offering UCSD Pascal and a FORTRAN based on a subset of the ANSI 77 standard. (ANSI is the American National Standards Institute.) The software runs on Ohio Scientific systems with 48 K bytes of memory and two floppy-disk drives. The system includes a screen-oriented text editor and a Pascal compiler. An assembler and run-time linker allow machine-code subroutines in either Pascal or FORTRAN. The software package also includes utilities for file maintenance, disk initialization, and disk duplicating. The package was developed and produced by SofTech Microsystems Inc and is sold through Ohio Scientific dealers. The package includes several disks, a Pascal primer, and manuals; price is $450.

Circle 640 on inquiry card.

FMS-80

Systems Plus, 1921 Rock St, Suite 2, Mountain View CA 94043, (415) 969-7047, is distributing FMS-80, a database management system. This system allows users to program applications in less time than it normally takes with higher-level languages. It is completely menu driven and is written in assembly language. It runs on CP/M, MP/M, or Cromemco's CDOS operating systems. FMS-80 features screen formatting, report generation, multiple field handling, and arithmetic manipulation of multiple data records. There is no limit to the size of records or the number of fields.

Circle 641 on inquiry card.

HDOS Package for North Star Horizon

Southwest Computer Center has developed a hard-disk operating system for use with the Corvus hard disk and the North Star Horizon computer. HDOS is completely compatible with North Star's DOS 5.0. The hard disk is accessed through two drives that are capable of storing 8.4 and 1.6 megabytes. An incremental backup and recovery system for security (known as IBARS) has also been added. HDOS sells for $125, and IBARS sells for $75. The packages can be purchased from Southwest Computer Center, 121 Wyatt Dr, Suite 7, Las Cruces NM 88001, (505) 526-2842.

Circle 642 on inquiry card.

A Bookkeeping Program

The DTI Bookkeeper I runs under CP/M and the TRSDOS operating systems and is written in Microsoft BASIC. The package includes general ledger, accounts receivable and payable, and payroll. Programs may be used separately, but they share consistent screen formats for user prompting. Maintenance for tax tables, W-2 forms, quarterly tax reports, financial statement headings, and other reports can be generated. One version of the package is for the TRS-80 Model I with 32 K bytes of progammable memory and dual disk drives; and the other version is for CP/M operating systems. The DTI Bookkeeper I is available for $95 per module or $335 for the entire package. Contact Data Train Inc, 840 NW 6th St, Suite 3, Grants Pass OR 97526, (503) 476-1467.

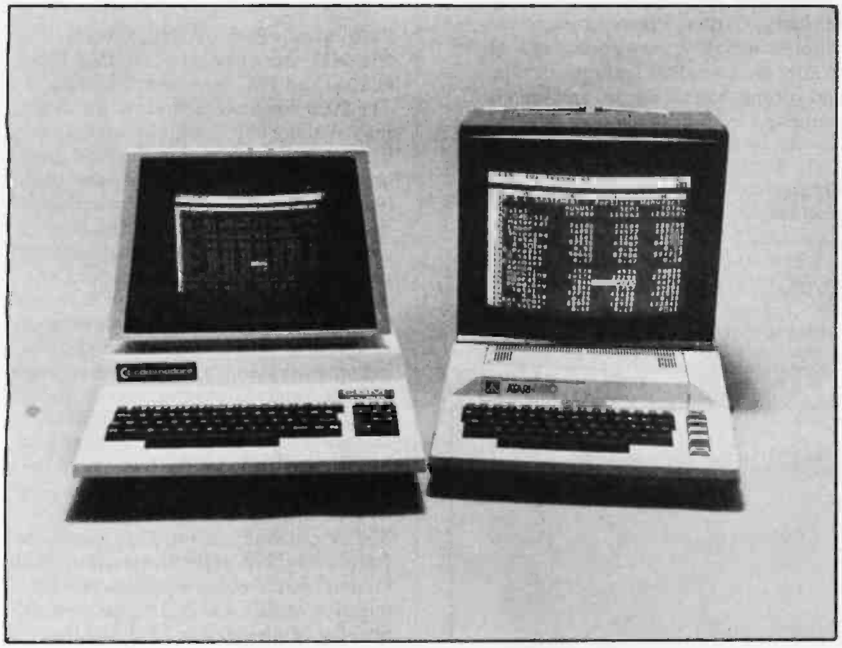
Circle 643 on inquiry card.

![What's New?]

What's New?

SOFTWARE

VisiCalc Now Runs on PETs and Atari Machines



VisiCalc, from Personal Software Inc, 1330 Bordeaux Dr, Sunnyvale CA 94086, (408) 745-7841, is a software package that turns a personal-computer display into an interactive electronic worksheet. It is now available for the Commodore PET and CBM Model 8032 and Atari 800 computers. VisiCalc creates a 64-column wide, 254-row high matrix on the screen. It is used instead of a calculator in businesses for inventory planning, sales forecasts, financial analyses, and modeling. Prices are available from local computer stores.

Circle 633 on inquiry card.

Cross Assemblers

These development systems feature a macroassembler, an interactive editor/assembler, and a text editor. They enable CP/M systems to serve as development stations for the Intel 8048 series, RCA COSMAC 1802/1804, National COP400 series, and the Zilog Z8 processors. The development systems share a common operational structure. The assemblers feature instruction mnemonics and syntax as defined by the processor manufacturers. The macroassembler includes full macroassembly and conditional assembly features, as well as the ability to chain a series of source files together during a single assembly. Programs developed under these systems must be off-loaded to the target processor for testing. Each development system is available for $150 on CP/M 8-inch floppy disks, 5-inch North Star or Micropolis Mod II disks. Contact Allen Ashley, 395 Sierra Madre Villa, Pasadena CA 91107, (213) 793-5748.

Circle 634 on inquiry card.

Data Base for the Hewlett-Packard HP-85A

The EDIT Division of Physiologic Corporation, 3800 Woodward Ave, Detroit MI 48201, (313) 831-8800, has introduced EDIT-85 for the HP-85A computer. This data-base management system supports all standard EDIT features such as validity and range checking during data entry, unlimited user viewing of the data, output-format control, data compression, nested data relations within files, and menu-oriented user prompts. EDIT applications include check/request, invoice, mail list, purchase order/request, and quote functions. The EDIT-85 and EDIT-4050 tape cartridge-based systems purchase price is $1750, and the lease/equity plan is $110 a month. The introductory applications are $50 each or $200 for all five on one tape. All EDIT systems receive 1 year of update privileges and the EDIT newsletter.

Circle 635 on inquiry card.

Programs for Home Control

The Soft-Sonic programs provide for home control. They run on the Apple microcomputer with a BSR Ultrasonic System X-10 (Sears Home Controller). The package includes the transducer hardware, interface cable, and the programs on a floppy disk. The programs allow for control of lighting, appliances, and more, through user-defined timed sequences or by voice command using Heuristics Speech Lab. The price is $39.95 from John Blankenship, BACE, POB 52785, Atlanta GA 30355.

Circle 636 on inquiry card.

The Dow Jones Connection

The Dow Jones Connection is a stock-management system that interfaces the TRS-80 to the Dow Jones computer in Princeton, New Jersey. Interaction with the Dow Jones network is automatic and virtually instantaneous. The first step is to create one or more portfolios of up to twenty-five stocks each. When the portfolio is completed, a second progam requests the user password and prepares the data for interrogation of the Dow Jones computer. A telephone call connects the two systems. Hard copy of the data can also be obtained through the user's printer. The Dow Jones Connection requires a TRS-80 Model I or II disk system or a Model I cassette system with a minimum of 32 K bytes of memory, and a Micro Connection modem which has an RS-232 output that can be used to drive a serial printer. For additional information, contact The MicroPeripheral Corporation, POB 529, Mercer Island WA 98040, (206) 454-3303.

Circle 637 on inquiry card.

Color-Enhanced Business Packages

Peachtree Software has announced a color-enhanced version of its general business packages. The packages have been modified for the CP/M-compatible Intecolor unit at Intelligent Systems Corporation of Norcross, Georgia. Initially offered are the Accounting, Inventory, and Mailing Address systems. For more information, contact the marketing department, Retail Sciences Inc, 3 Corporate Sq, Suite 700, Atlanta GA 30329, (404) 325-8533.

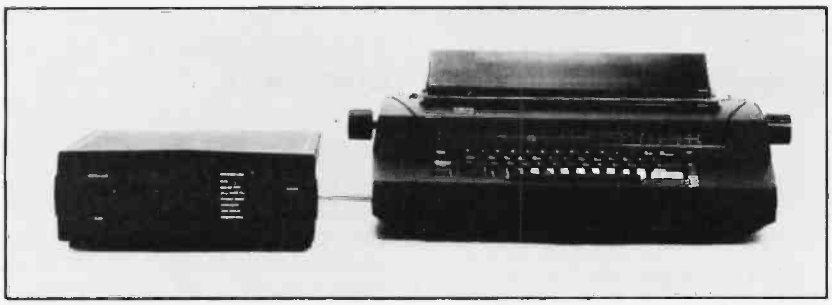
Circle 638 on inquiry card.

What's New?

PERIPHERALS

Floppy-Disk Attachment for Typewriters

The Phrasestore is a floppy-disk storage system that attaches directly to an IBM Model 50, 60, or 75 electronic typewriter. It includes two temporary working storage memories with edit capabilities. No modifications are made to the typewriter. When power to the Phrasestore is off, the typewriter is electrically isolated. Edit features include add, delete, insert, merge, and search commands. An optional feature provides RS-232 asynchronous communications up to 9600 bps (bits per second). The Phrasestore is priced at $1810. The communications option is $350. Contact California Micro Computer, 9323 Warbler Ave, Fountain Valley CA 92708, (714) 968-0890.



Circle 628 on inquiry card.

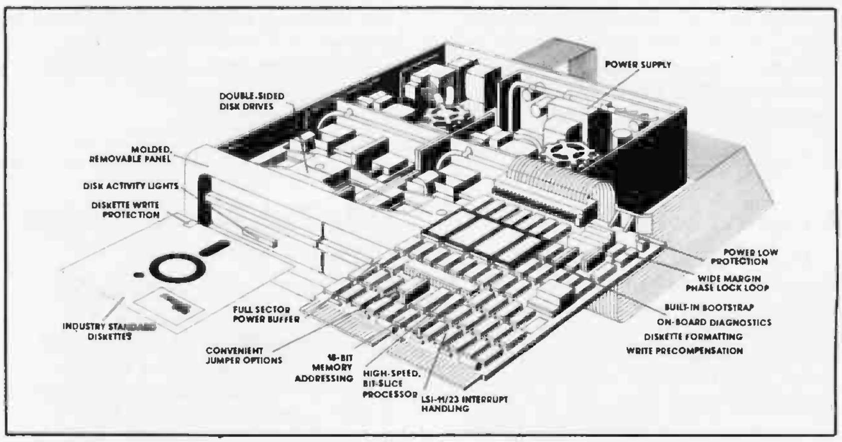
Intelligent Modems

Business Computer Corporation, POB 7498, Menlo Park CA 94025, (415) 854-5434, has unveiled BIZCOMP Model 1030 and 1031 Intelligent Modems. The 1030 combines a modem, an automatic calling unit, and microcomputer into an FCC-registered unit with auto-answer, auto-dial, and auto-repeat dial features. BIZCOMP's code-multiplexed design allows intelligent modem control using the same terminal as that for data communication. Code-multiplexing enables software to be written in high-level languages. Applications include computer/terminal networking, financial transaction entry, store and forward message routing, remote data-base access, and remote computer diagnostics. RS-232 and current-loop interfaces are standard. Model 1031 includes the features of the 1030 plus command-selectable dial pulse or tone dialing, and self-test. The tone dialing capability of the 1031 is suitable for a CPT-TWX network interface. Both models feature automatic data-rate acquisition at 110, 134.5, 150, 200, or 300 bps. the Model 1030 is $395 and the 1031 is $495.

Circle 631 on inquiry card.

Modules Control AC and DC Circuits

This I/O (input/output) system allows direct microprocessor control of industrial AC and DC circuits. Any mix of AC or DC, input or output solid state plug-in modules can be used in any position on the universal mount. All modules are optically isolated, fused, and have LED (light-emitting diode) indicators. Applications include energy management, machine and process control, and lighting systems. The price is $10 to $20 per circuit depending on configuration. Contact Wintek Corporation, 1801 South St, Lafayette IN 47904, (317) 742-8428. Circle 629 on inquiry card.



6502 Development System

Microproducts has introduced a 6502 development system. This system contains a text editor, assembler, disassembler, and symbolic debugger. It is available for the Apple II on a floppy disk and resides in 8 K bytes of programmable memory. The system is also available on EPROM (erasable programmable read-only memory) with socket adapters to replace Integer BASIC. The text editor supports the entry and maintenance of 6502 assembler text files. The assembler has been designed to process all 6502 op codes designated by MOS Technology, and other pseudo op codes.

The disassembler will disassemble a specified portion of machine-resident code and produce a text file that is compatible with the assembler. The debugger executes programs step-by-step and displays each instruction along with the microprocessor registers, as well as values contained in up to five hundred user-selected memory locations. The disk version is $125, a plug-in card of the system on EPROMs is $395, and socket adapters that plug into the Apple II main board are $249. Contact Microproducts at 30420 Via Rivera, Rancho Palos Verdes CA 90274, (213) 541-5131.

Circle 630 on inquiry card.

Two-Megabyte Floppy-Disk System

A double-sided double-density Digital Equipment Corporation (DEC) RX02-compatible floppy-disk system has been introduced by Data Systems Design Inc, 3130 Coronado Dr, Santa Clara CA 95051, (408) 727-9353. The DSD 470 is compatible with DEC LSI-11 computers and doubles the capacity of other DEC-compatible floppy-disk systems; it also provides LSI-11/23 multiple-level interrupt support. The DSD 470 is priced at $4295.

Circle 632 on inquiry card.

What's New?

PUBLICATIONS

Computer Supplies and Accessories

A thirty-six-page issue of the *MISCO Minicomputer Supplies & Accessories Catalog* offers the company's computer products, plus an expanded section of stock, custom and Digital Equipment Corporation-compatible cables; multipoint paper shipping for the lowest shipping costs; and the addition of BASF floppy disks to the selection of products. Catalog merchandise can be ordered by mail, TWX, or by a toll-free telephone number. The free catalog is available from MISCO Inc, POB 399, 963 Holmdel Keyport Rd, Holmdel NJ 07733, (201) 946-3500.

Circle 649 on inquiry card.

Opto-Electronic Devices Detailed in Catalog

Ferranti Electric Inc has put together a catalog that details its line of solar cells, photodiodes, phototransistors, programmable integrated circuit photoswitches, and infrared detectors. A full product description, table of principal characteristics, and list of applications are provided for each device. Also featured is a section on Ferranti's custom design service. For a free copy, contact Ferranti Electric Inc, Semiconductor Products, 87 Modular Ave, Commack NY 11725, (516) 543-0200.

Circle 650 on inquiry card.

Design of VMOS Circuits

Design of VMOS Circuits, With Experiments, by Robert T Stone and Howard M Berlin, features eleven chapters on the VMOS (vertical metal-oxide semiconductor), and its characteristics. The VMOSFET (vertical metal-oxide semiconductor field-effect transistor) is introduced, and some of its characteristics, such as high input impedances, nanosecond switching times, and low feedback capacitances, are explained. The theory of semiconductor operation and applications and limitations of VMOS devices are also covered. Audio, RF (radio frequency), power supply, and microcomputer applications are illustrated and discussed. The authors set up nine experiments using VMOSFETs. The book lists for $8.95 from Howard W Sams and Company Inc, 4300 W 62nd St, Indianapolis IN 46268, (317) 298-5400.

Circle 651 on inquiry card.

Brochure on Speech Technology Products from Texas Instruments

The *Solid State Speech Products and Services Brochure* provides information on voice-synthesis technology available from TI. The brochure describes linear predictive coding technology, vocabulary development for user applications, and solid state speech products. Included are TI's LSI (large-scale integration) voice-synthesis processors and voice synthesis memories, the TM990/306 speech module, and custom speech modules. The brochure is free from Texas Instruments Inc, Inquiry Answering Service, POB 225012, M/S 308, (Attn:CL-501), Dallas TX 75265.

Circle 652 on inquiry card.

Manual for OSI BASIC Users

All About OSI Microsoft BASIC in ROM is a reference manual for Ohio Scientific computers that use Microsoft BASIC Version 1.0, Revision 3.2. Detailed descriptions of BASIC commands, statements, and functions are illustrated with short programs and sample runs. The book explains loops, tapes, and the USR(X) function. Some bugs and their fixes are discussed. Topics on the machine-language level include source code and variable storage, floating-point and two's complement numbers, maps of subroutine locations, and a description of the monitor and support ROMs (read-only memory) at $FE and FF. The price is $8.95 from E H Carlson, 3872 Raleigh Dr, Okemos MI 48864.

Circle 653 on inquiry card.

Catalog from Synertek Systems

A catalog from Synertek Systems Corporation, 150 S Wolfe Rd, Sunnyvale CA 94086, (408) 988-5689, features descriptions and prices of SYM, KIM, and Superjolt products. Single-board computers, video displays, BASIC ROMs (read-only memory), programmable memory kits, and more, are featured.

Circle 654 on inquiry card.

Catalog of Computer Forms

Moore Business Forms Inc, 1205 N Milwaukee Ave, Glenview IL 60025, (312) 291-8227, has published an eight-page brochure describing its products and services. Products featured are sales books, register forms and registers, snap-apart unit sets, self-mailing systems, print continuous and stock forms. Products for data-processing installations as well as word processing systems are included. Services such as Moore Creative Graphic Centers, Idea Centers, and worldwide sales are also covered.

Circle 655 on inquiry card.

Nibble for the Apple

Nibble Magazine is focused on the Apple II and Apple II Plus computers. Each issue contains a central theme such as home finance, games, simulation, and data-base management. It also features hardware and software reviews, graphics, programming tips, games, and a hardware construction project. *Nibble* is published eight times a year by MicroSPARC Inc, POB 325, Lincoln MA 01773, (617) 259-9710. The subscription rate is $15.

Circle 656 on inquiry card.

PET Printout from Europe

PET Printout is a magazine from England published every five weeks. It includes news and technical reviews of PET-related products, programming articles and listings, questions and answers, applications stories, and a gossip column about PET personalities on both sides of the Atlantic. *Printout* is published ten times a year and costs $30. Contact *Printout*, Greenacre, North St, Theale, Berkshire, RG7 5EX, England.

Circle 657 on inquiry card.


COMPUTERS: the INSIDE STORY
BY TOM SLOAN
OH BOY, IS THIS GREAT.
PRINT "SPACE"; PRINT "GAME" RUN
I WONDER WHAT MAKES THIS THING WORK.
SPACE GAME
COMMAND
ITS AN ELECTRONIC MARVEL
6502
A SILICON SPLENDOR
NMI
CPU
HOW'S IT GOING?
OK. THE GUY IS WRITING A SPACE WAR GAME.
OH NO!
TILT
POKE
WHAT DID HE DO?
HE POKED A STRING ARRAY TO THE WRONG ADDRESS!
ERROR
RATS, WHAT NOW
POKE@,A$
ERROR
SEE IF MEMORY KNOWS ANYTHING.
WHAT'S THE EXTENSION?
2114
HECK. THE LINE'S DEAD!
THIS HAS GOT TO BE ONE OF HIS ALL-TIME FOUL UPS!
MMM.
I'LL GO DOWN TO MEMORY MYSELF.
IRQ INC.
ROM BLVD
MEMORY LN
HERE I AM
DID YOU GUYS FIGURE IT OUT YET?
We'LL HAVE IT FIXED IN A NANO-SECOND.
NUTS. NOW I'M TOO BORED TO CONTINUE.
ERROR
COMMAND
I'LL QUIT FOR AWHILE
SPACE
SHIFT
RETURN
CLICK
ON
OFF
AWWWWWWWWW
SYSTEM OFF
WELL, THAT GIVES US TIME TO PLAY WITH OUR COMPUTER.
YA
GEE. I WONDER WHAT MAKES THIS THING WORK.
ALIENS
TOM SLOAN

WE LOST OUR LEASE . . . ($500 REWARD FOR THE SAFE RETURN THEREOF).

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Some suppliers offer only hardware and call that complete. At Micropolis complete means everything: hardware and software and documentation.

The hardware set is complete with S-100/8080/Z-80 compatible controller, drive(s), cable-even a built-in Autoload bootstrap ROM to eliminate tiresome button pushing.

Our full Disk Extended BASIC and DOS, assembler and editor software comes complete, too. On its own diskette, ready to go. Software from Micropolis includes a DOS and Disk Extended Basic designed for 8080/Z80-based microcomputers.

DOS is a complete package, including an assembler, editor, file management functions and utilities, which provides total support for 8080 programming. BASIC is a self-contained package which provides a powerful set of tools for developing, testing, executing, and maintaining BASIC programs.

BASIC is designed for microcomputers with at least 24K bytes of RAM and a Micropolis MetaFloppy disk system. DOS can be used alone in a 16K bytes memory system.

Activating the built-in Auto load ROM brings up the system under control of the DOS executive. BASIC can be accessed by issuing a simple DOS command.

The 1053 MOD II Subsystem is designed for flexible, efficient programming. 8080 programs created under DOS can be loaded and accessed from BASIC. Data files created under BASIC can be processed by user written application programs running under the DOS.

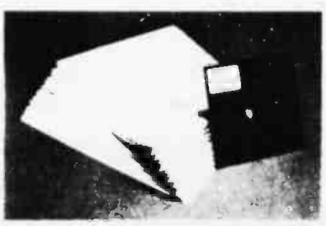
Imagine getting all the capacity of an 8-inch floppy in a 5¼-inch format.

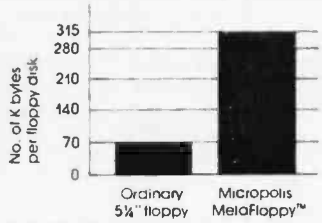
MetaFloppy can give you this higher capacity because it packs more data into every disk. You get the capacity of larger 8-inch drives with the lower price and smaller packaging of 5¼-inch drives.

An ordinary 5¼-inch floppy provides just 35 tracks/drive and stores only 70K bytes. Not nearly enough for anything useful. So instead, we use 77 tracks-each with 16 sectors of 256 bytes/sector—to yield a capacity of 315K bytes/drive. That's more than four times an ordinary 5¼-inch floppy! And why we call this one "quad density."

Combine two of these drives in a compact dual module and you can copy diskettes from one drive to the other, or rearrange data files, or whatever. The dual unit stores 630K bytes. Enough for almost anything. But just in case that isn't enough, our controller can handle two duals (or four singles). That means your micro can have more than a million bytes of formatted disk storage.

If that still isn't enough, on special order you can add a second controller with up to four more drives. That will give you a grand total of over 2,500,000 bytes of storage on-line. This means, if your application keeps growing, we've got you covered in easy steps. And you get all these bytes at surprisingly low cost.





Each one of our floppy disks has a remarkable storage capacity, eliminating the need to keep bothersome stacks of paper.

Faster than a speeding bullet.

At Micropolis, we don't skimp on performance to deliver maximum capacity. So you can expect professional operating speed and efficiency. Like checks and balances, such as automatic read verification after writing, that you would expect in a sophisticated data processing system.

Like last track-to-track positioning time of only 30 milliseconds. And a data transfer rate of 250,000 bits per second.

Up. Up. and away!

Metafloppy gets along well with almost everyone.

So choose the microcomputer you want. MetaFloppy's controller is completely compatible with the S-100/8080/Z-80 buss. It just plugs into your MITS 8800, IMSAI 8080, COMPAL-80, SOL-20, Polymorphic 88, CROMEMCO, TDL, or similar micro and it's ready to go. The memory mapped controller/bootstrap may be origined at any 1K byte boundary in the 48K to 64K byte region of memory.

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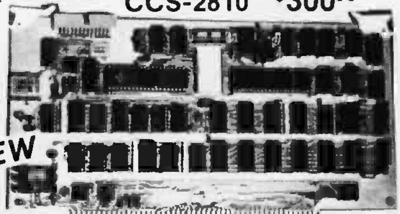
- Responds to Wait State Generation
- M1 Wait State
- Front Panel Supported
- I/O Address Mirror
- 1-RS232 Serial Port, Selectable I/O Address with 100% Disable Option

NEW



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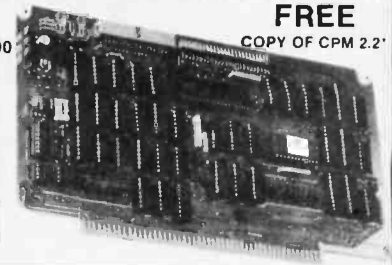
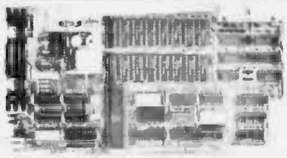


NEW SPECTRUM S-100 COLOR GRAPHICS BOARD



Includes 8K of IEEE-compatible static RAM; full duplex bi-directional parallel I/O port for keyboard, joystick, etc. interface; and 6847-based graphics generator that can display all 64 ASCII characters. 10 modes of operation, from alphanumeric/semi-graphics in 8 colors to ultra-dense 256 x 192 full graphics. 75 Ohm RS-170 line output and video output for use with FCC approved modulators. **Introductory prices:**

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Don't settle for black and white graphics or stripped-down color boards; specify the CompuPro Spectrum.

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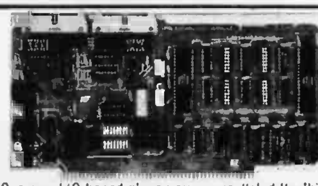
CK022 S-100 INTERFACER



Our new I/O board gives you unparalleled flexibility and operating convenience. We include such features as:

- 2 independently addressable serial ports (dip switch selectable addresses)
- Real LSI hardware UARTs for minimum CPU housekeeping
- RS232C, current loop (20mA), & TTL signals on both ports
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- Industry standard RS232 level converters with five RS232 handshaking lines per port
- Optically isolated current loop with provisions for both on-board & off-board current sources
- UART parameters, interrupt enables & RS232 handshaking lines are software programmable with power-on hardware default to customer specified hard-wired settings for maximum flexibility
- Port connectors male directly to ribbon cable & DB25 connectors in standard pinouts
- RS232 lines will conform to either master or slave configurations
- Board gives full feature operation with both 2 & 4 MHz systems
- Low power consumption: +8V @ 450mA; +16V @ 150mA; -16V @ 70mA max.
- No software initialization required for board operation, although board parameters may be altered by software 2 lbs.

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INTERFACER II

The new Interfacer II I/O board incorporates one channel of serial I/O with all the features of the INTERFACER dual RS232 serial board, plus 3 full duplex Parallel ports. The serial section includes all the features you've come to expect - a hardware UART, on-board crystal controlled Buad rate generator, hardware/software programmability, RS232 handshaking lines with real RS232 drivers, current loop & TTL drivers, full interrupts and more!!! The parallel selection utilizes LSTTL octal latches for latched input & output data with 24mA drive current, attention, enable & strobe bits for each parallel port (each with selectable polarity), interrupts for each input port, separate 25 pin connectors with power for each channel and a status port for interrupt mask and port status. All in all - an Incredibly flexible and easy to use board.

		Reg.	Sale
GBT-150U	INTERFACER II UKT	$199.00	$189.00
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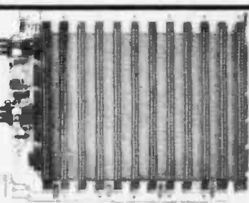

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MOTHERBOARDS

A Must for Reliable System Operation!!!

NEW

These are third generation micro-motherboards set up to exceed the latest S-100 specs. Designed with operation of the newest 5 to 10 MHz MPUs in mind — with any of these motherboards, you won't have to start from scratch when you want to upgrade your system from 2 or 4 MHz operation.

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All boards are double sided fiberglass epoxy, G10/FR4, with plated through holes & solder mask on both sides. A parts legend on the component side makes assembly a snap.

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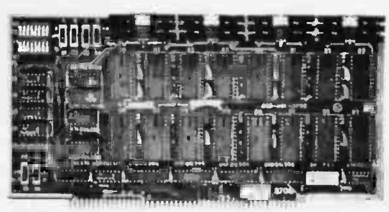
GODBOUT

ECONOROM 2708



Has provisions for wait states for 4MHz operations. Configured as four 4K blocks - each independently addressable and disable-able. Power-on jump. Does **NOT** include 2708s. Includes all support chips, sockets, regulators, heat sinks, etc. Sold in UNKIT form **only**. Shipping Weight 2 lbs.

GBT-125U ECONOROM 2708 UKT ... $85.00

NEW

NEW

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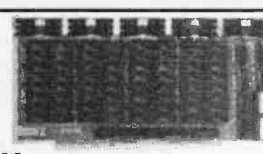
GODBOUT

ECONORAM XA 32K RAM



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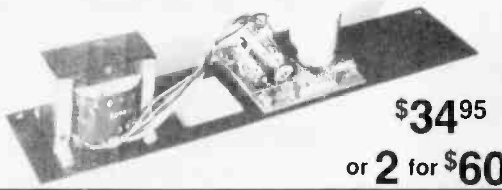

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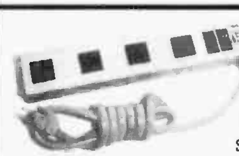

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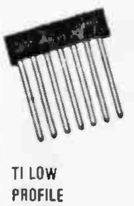

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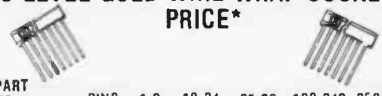

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RNS-18WWG	18	.85	.75	.70	.65	.60
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CNO-DE9S	9 PIN FEMALE	\$ 2.70	\$ 2.40	\$ 2.10
CNO-DE9C	9 PIN COVER	\$ 1.50	\$ 1.25	\$ 1.10
CNO-DA15P	15 PIN MALE	\$ 2.75	\$ 2.45	\$ 2.15
CNO-DA15S	15 PIN FEMALE	\$ 3.95	\$ 3.60	\$ 3.20
CNO-DA15C	15 PIN COVER	\$ 1.50	\$ 1.30	\$ 1.10
CNO-DB25P	25 PIN MALE	\$ 3.50	\$ 3.25	\$ 3.00
CNO-DB25S	25 PIN FEMALE	\$ 4.60	\$ 4.35	\$ 4.20
CNO-DB51212	1 PC. GREY HOOD	\$ 1.60	\$ 1.45	\$ 1.30
CNO-P25H	2 PC. GREY HOOD	\$ 1.50	\$ 1.25	\$ 1.10
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CNO-DC37P	37 PIN MALE	\$ 5.80	\$ 5.10	\$ 4.45
CNO-DC37S	37 PIN FEMALE	\$ 8.70	\$ 7.70	\$ 6.70
CNO-DC37C	37 PIN COVER	\$ 1.80	\$ 1.55	\$ 1.30
CNO-DD50P	50 PIN MALE	\$ 8.75	\$ 7.75	\$ 6.70
CNO-DD50S	50 PIN FEMALE	\$11.65	\$10.25	\$ 8.90
CNO-DD50C	50 PIN COVER	\$ 2.00	\$ 1.80	\$ 1.60
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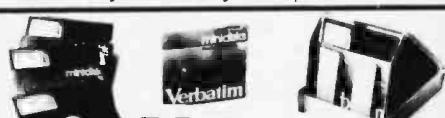
CNO-5730360	CENT. 700 SERIES PRINTER CONNECTOR	\$ 9.00	\$ 7.50	\$ 6.00



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VRB-MD 525 16	Hard 16 Sector	Micropolis	\$ 8.95	\$29.95
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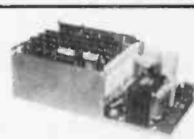

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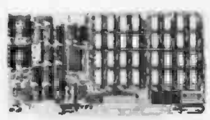

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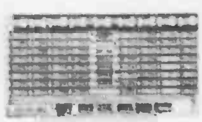

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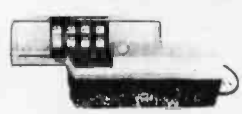

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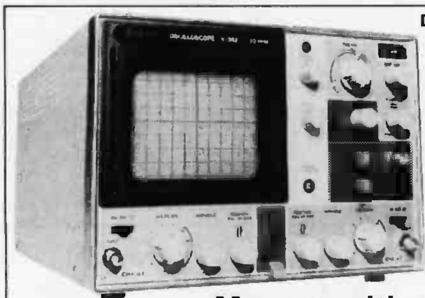

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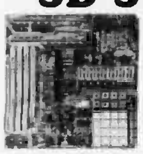

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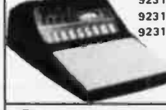

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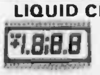

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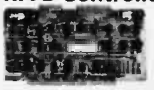

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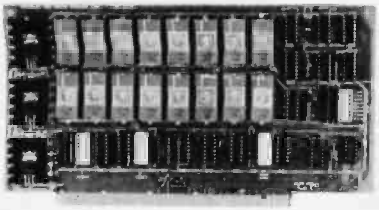

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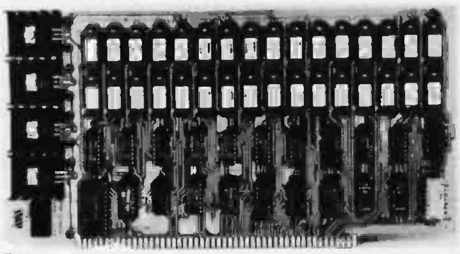

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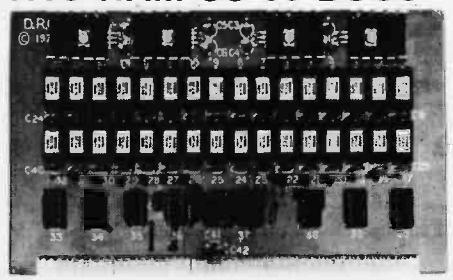

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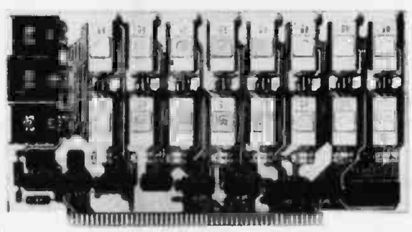
16K EPROM CARD-S 100 BUSS



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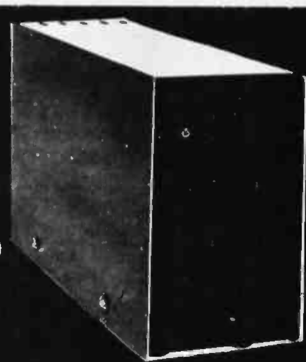

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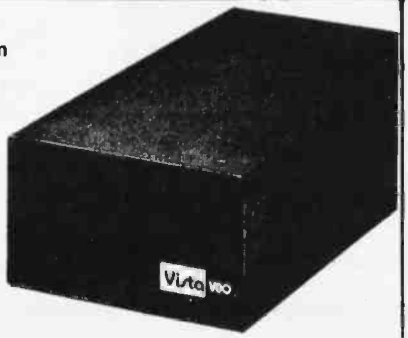

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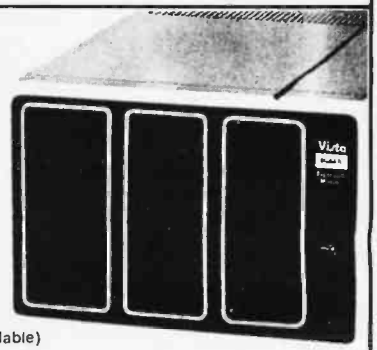

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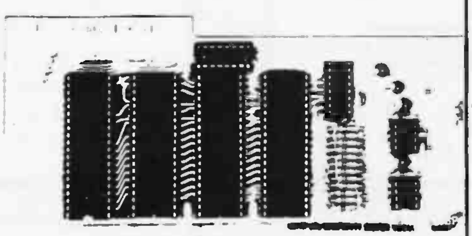

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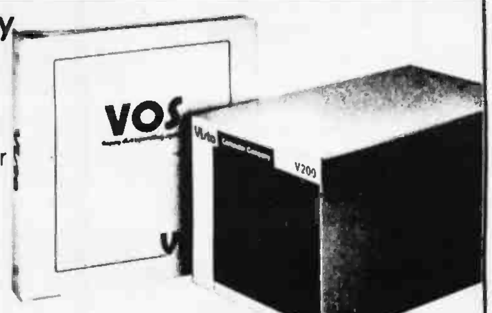

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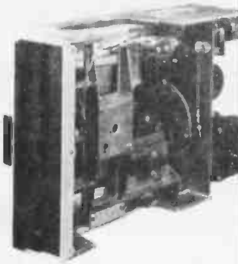

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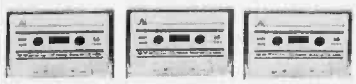

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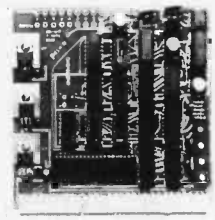

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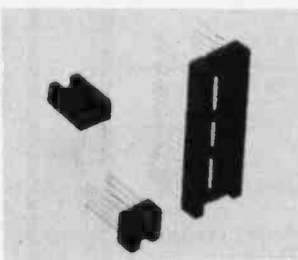

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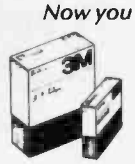

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3.000-A	6.72530-B	11.2186-B	28.6276-B	39.8768-B	43.4078-B	50.2505-B
3.087-B	6.75840-B	11.2880-B	28.7538-B	39.9628-B	43.4378-B	51.0556-B
3.200-B	6.9003-B	11.4776-B	29.8758-B	40.4448-B	43.4448-B	51.3128-B
3.2768-A	7.0063-B	11.6566-B	29.9370-B	40.5028-B	43.5558-B	51.7778-B
3.500-B	7.0336-B	11.6816-B	30.0648-B	40.8178-B	43.6298-B	51.8506-B
3.579-B	7.0916-B	12.440-B	30.3806-B	40.8336-B	43.6668-B	52.8128-B
4.000-B	7.1836-B	14.3182-B	30.6258-B	40.8758-B	43.7778-B	56.7506-B
4.1943-B	7.2586-B	14.4308-B	30.8768-B	40.8888-B	43.8128-B	60.6006-B
4.3426-B	8.000-B	15.000-B	31.4370-B	40.9258-B	43.8148-B	60.7508-B
4.4803-B	8.0556-B	15.4408-B	31.7538-B	41.0008-B	43.8518-B	66.7506-B
4.6103-B	8.1416-B	15.5068-B	31.9008-B	41.1666-B	43.8888-B	70.4006-B
4.6503-B	8.1818-B	16.000-B	32.000-B	41.3768-B	43.9258-B	75.0006-B
4.8303-B	8.3303-B	16.3848-B	33.2006-B	41.8376-B	44.0008-B	90.8338-B
4.9152-B	8.4998-B	17.2248-B	33.6258-B	42.0008-B	44.0378-B	99.9668-B
5.000-B	8.5766-B	17.2422-B	34.5568-B	42.5806-B	44.3768-B	100.6668-B
5.0688-B	8.6056-B	18.000-B	34.7538-B	42.6268-B	44.7778-B	101.4668-B
5.1203-B	8.9608-B	18.4320-B	34.9776-B	42.7006-B	45.1256-B	103.0668-B
5.1850-B	8.9906-B	19.4680-B	35.9256-B	42.7538-B	46.3006-B	103.4668-B
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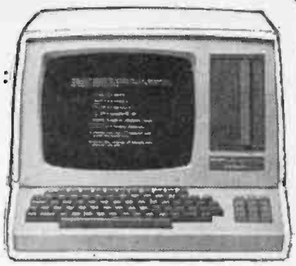

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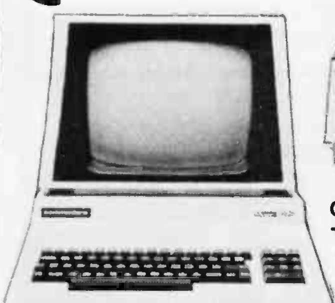

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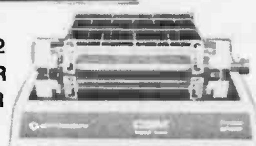

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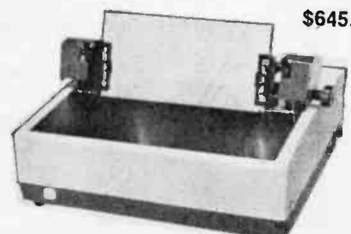

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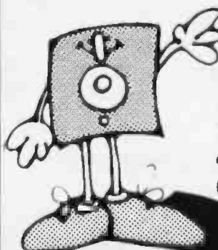

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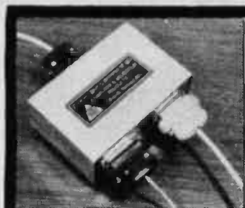

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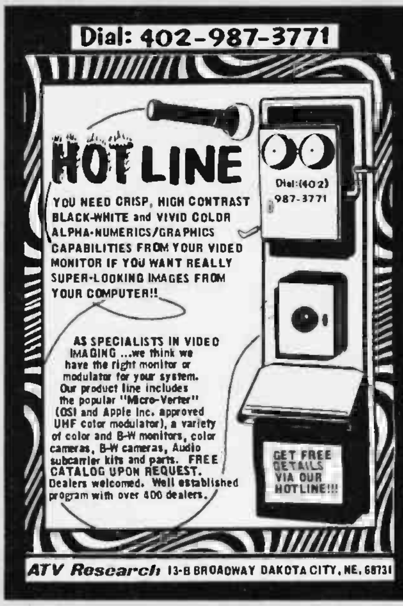

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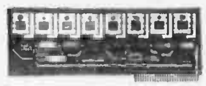

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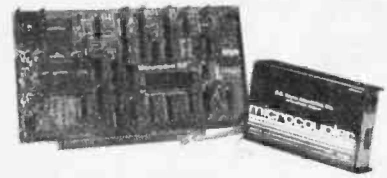

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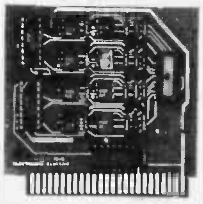
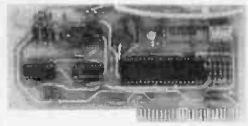


There are 8 inputs that can be driven from TTL logic or any 5 volt source. The circuit board can be plugged into any of the 8 sockets of your Apple II. It has a 16 pin socket for standard dip ribbon cable connection. Board only $15.00. Part No. 120, with parts $69.95. Part No. 120A.

APPLE II※ SERIAL I/O INTERFACE



Baud rate is continuously adjustable from 0 to 30,000 • Plugs into any peripheral connector • Low current drain. RS-232 input and output • On board switch selectable 5 to 8 data bits, 1 or 2 stop bits, and parity or no parity either odd or even • Jumper selectable address • SOFTWARE • Input and Output routine from monitor or BASIC to teletype or other serial printer • Program for using an Apple II for a video or an intelligent terminal. Also can output in correspondence code to interface with some selectrics. • Also watches DTR • Board only $15.00 Part No. 2, with parts $42.00 Part No. 2A, assembled $62.00 Part No. 2C

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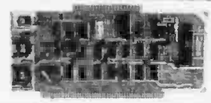

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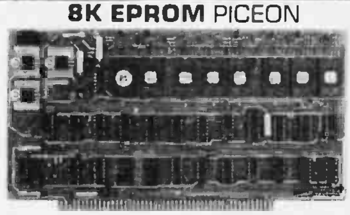

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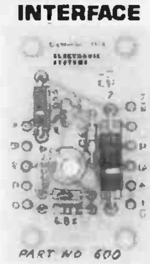
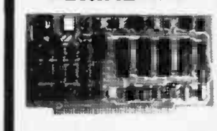
RS-232/TTY INTERFACE



This board has two active circuits, one converts RS-232 to 20 mA, the other converts 20 mA to RS-232. Requires +12 and −12 volts. $9.95 Part No. 600A Kit.

SERIAL I/O



Four Serial I/O RS-232 ports. S-100 Bus. Software or jumper selectable baud rate (110, 300, 600, 1200, 2400, 4800, 9600, 19.2K), on board Xtal baud rate generator. Addressing, switch selectable. Parity or no parity (odd or even) switch selectable. 1 or 2 stop bits, 5 to 8 bits/character. Board only $29.95, Part No. 7908. With parts (kit) $199.95, Part No. 7908A.

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Order Line: (408) 448-0800

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for

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• Reverse Video • Blinking/blank fields • Upper/lower case character • Protected fields • Non-glare screen • Underlining • 12 x 10 character resolution • Single stroke editing keys • Function keys • Blinking cursor • TTY keyboard • Numeric pad • 9 Baud rates (75-9600 Baud) • Self-test • Printer port

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KASETTE LIBRARY

Part No.
CAS-10-8
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8" Diskette Holder .... **$4.50 or 3/$10.00**
CAS-10-5
Blue/Grey/Beige/Black
5" Diskette Holder .... **$4.25 or 3/$10.00**

CONNECTORS

RS232 Set	$6.50
.1 Male DB-25, 1 Female DB-25, 1 Cover	
DB25P	$2.95
DB25S	$3.60
Cover	$1.50
S-100 (IMSAI STYLE)	$2.50 ea.
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SEE QT PRODUCTS AT THE NORTHEAST PERSONAL & BUSINESS COMPUTER SHOW IN BOSTON - NOV. 20-23 ISLAND BOOTH #408

PARTS

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Z80A (4MHz)	$12.95
6502	$11.25
6800	$12.50
6802	$18.00
8035	$20.00
8080A	$ 3.50
8085A	$20.00
8086-4	$60.00
8088	$60.00
8748-8	$70.00

8080A SUPPORT

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8214	$ 4.50
8216	$ 2.95
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8228	$ 6.00
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8243	$ 5.00
8251	$ 7.00
8253	$19.00
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8255	$ 6.25
8257	$17.95
8257-5	$19.00
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AY5-2376	$13.75
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MC14411	$11.00
1-8432 XTAL	$ 4.95
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2532	$55.00
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D3205	$ 3.00
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DM8131	$ 3.00

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MC6845P	$22.00

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TR1602B	$ 3.75

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2513 (Upper case)	$10.95
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2513 Upper (5 v)	$ 9.75
2513 Lower (5 v)	$10.95

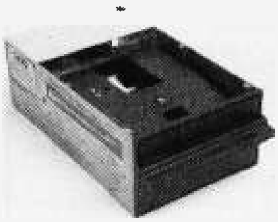
6800 PRODUCTS

6802P	$18.00
6821P	$ 5.25
6845P	$22.00
6850P	$10.00
6860P	$11.55
6875P	$ 7.40

Circle 337 on inquiry card.

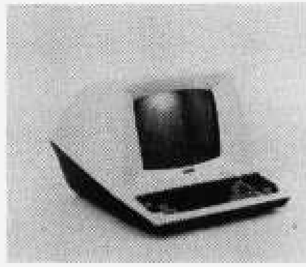
Contact us for new prices

Qume Datatrak 8



Double sided floppy with NO HEADACHES. Although many think this an impossibility, seeing is believing, and this drive is really something! Shugart compatible, fully optioned, reliable, and rapidly becoming the standard in double-sided diskdom.

$599. Two/$549.



Electrolabs' Monthly Special!!!

TELEVIDEO 912C $699
TELEVIDEO 920C 799

Features typewriter keyboard, microprocessor controls, Upper/lower case, adjustable baud rates (75-9600 baud), special function keys, much much more.

Second page memory option $29.00

Siemens FDD 100-8D

Single sided 8" floppy drive, the latest & greatest revision. Features double density plus much more. An extremely reliable drive $439 2/$409

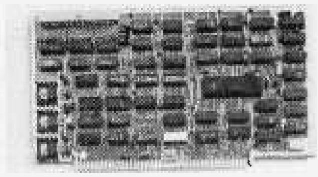
Hard sector option kit... $9.95
Data separator option kit... $9.95

The following 5¼" mini-floppies share most features with their 8" cousins, so without further ado...

Siemens FDD 100-5D............ $279.
Qume Datatrak 5 (double sided).... 399.
BASF Mini mini................. 279.
SA 400........................ 299.

All the above mini-floppies are fully SA400 compatible.

Manuals for all drives are $10, refundable against future purchase of drives. Also, all 8" drives can be ordered with 220 v/50 hz for worldwide use.



Disk controllers

Delta Products double density	$349
Micromation doubler	439
Tarbell single density, A & T	225
Tarbell single density, kit	184
Tarbell double density, DMA	425
Sorrento Valley 8" single density for Apple	375

Data Display Monitors

used 12" Sylvania monitors. Composite video, 12 MHz, 120 VAC. with new P-39 or P-4 tube, $79, used tube $59, OEM style (without case), subtract $12. U-fix model, 10/$300.

Hard Disk

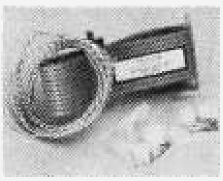
CII HB 10 MBY fully REMOVEABLE cartridge drive. Complete with controller, personality card, media, power supply, cabling, connectors and documentation. Highlighted by stylish & modern cabinetry. $6995.

Shugart SA4008 20MBY fixed disk system. S-100, includes controller, power supply, and all that is necessary to run $6995.

4116 dynamic RAM, 16K Bonanza!!

Set of 8, 16K, for Apple, TRS-80, Exidy, Heath & more. 200 Ns., prime parts, at the unheard of $49/8.
Large discounts available for quantity & dealers (500 & up). Offer limited while supply lasts, as these will vanish quickly!!!

Accessories



Cable kits for 8" drives with 10' 50 cond. flat cable, power cable, and all connectors. Assembled if desired. One drive 27.50, two 33.95, three 38.95
for mini floppies (34 cond): one 24,95, two, 29.95

CP-206 Power-one power supply. Powers two drives more than adequately, top quality. 2.8A/24V, 2.5A/5V,.5A/-5V................ $99.

mini-floppy power supply $79

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8" ...$39.99 SS/SD
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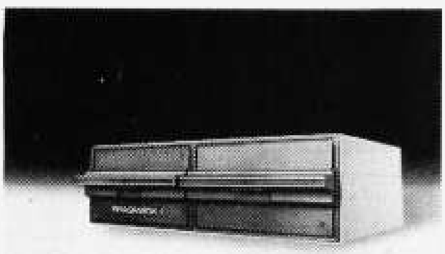
8" ...$59.00 DS/DD
5¼" $34.95 SS
5¼" $59.00 DS

Verbatim, Memorex, Scotch, or equivalent name brand

Special Introductory Offer!!!
Wabash 8" diskettes $29.00 SS
$39.00 DS
Price is cheap, but they run like champs!!!!

Diskette head cleaning kit for 5¼" or 8" $28.75 includes everything for 1 drive for 1 year. Alignment Diskette for Floppy Drives.......... $39.00



PRAGMATIX 1

Incredible!! – Two 8" Shugart compatible single sided floppy disk drives (double density), CP-206 power supply, in handsome color coordinated cabinet, with full cabling, connectors, and documentation, plus one box diskettes!!! All for an unprecedented $1295. Up to one MBY of storage.

with Qume Datatrak 8" double-sided drive $1695

ENCLOSURES

Rackmount Mainframe MT-200. This gorgeous beast is so appealing that it can easily function also as stand-alone mainframe. Very modern styling with fully actively terminated S-100 bus.

With two 8" single-sided disk drives... $1899.
With two 8" double sided disk drives in place of single-sided variety............ $2499.

Desktop Mainframe MT-100. Contemporary styling, a handsome cabinet coated with durable epoxy finish colors (blue, beige, off-white & silver). Easy to fit into an office environment. The proper way to start your system.

Above plus two 8" single sided disk drives.............. $1599.
Above with two 8" double sided disk drives in place of single-sided variety....................................... $2199.

$25 min. order. Calif. residents add 6% sales tax. Orders under $75, add 5% shipping and handling, over $75 add 2.5%. All pricing subject to change without notice.

Circle 338 on inquiry card.

Keyboard Special 2 !!

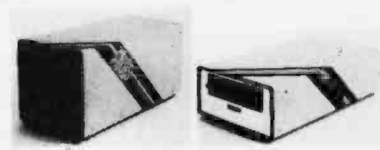
Keytronics 1660	$149.00
Hard Plastic enclosure	49.00
BOTH only	$152.00

Keyboard Special 1 !!

CHERRY "PRO" Keyboard	$119.00
Streamlined Custom Enclosure	34.95
BOTH only	$134.95

Disk Subsystem

Matchmaker Technology
TURNKEY DISK SUBSYSTEMS



APPLE ...... Single density disk controller. Expanded Apple DOS

TRS-80 .... Single or double density. Expansion interface necessary. Space for 48K dynamic RAM on controller card RS232 port

SORCERER .. Full RS-232 Interface. One S-100 slot for memory expansion. Single or double density

All above units come as follows: Complete, assembled and tested, with two 8" floppy disk drives (Apple available in one drive model). Includes all cabling, connectors and documentation in a stunning color coordinated cabinet with power supply. Ready to go, plug in and run!!!

• • •

When ordering specify single or double sided drives

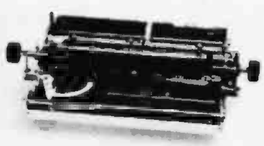
• • •

Software available for above disk add-ons

• • •

TRS-80 & Sorcerer operate on all CP/M compatible software

Daisy Wheel Printers



NEC Spinwriter 5510/2	$2899
NEC Spinwriter 5520/2	call
NEC Spinwriter 5530/2	for prices

ESAT 200B

BI-LINGUAL 80x24 Communicating Terminal
Scrolling, full cursor, bell, 8x8 matrix, 110-19,200 baud, Dual Front Applications. Arabic & Hebrew, Multilingual Data Entry Forms Drawing, Music, & Switchyards.

Alone	$279.
with Cherry Pro keyboard & custom metal case	$399.

Qume S/5

Sprint 5/45 RO	$2699
Sprint 5/55 RO	2829
Sprint 5/45 KSR	3029
Sprint 5/55 KSR	3159
Forms Tractor	$210
Pinfeed platen	155
paper guide	30
paper basket	50

many print wheels, ribbons, & more available

Qume Sprint 3\45

(requires self assembly)

printer mechanism	$1499
power supply	349
combination special	1699
cases	200
S-100 interface card	149

Circle 338 for Electrolabs

Electrolabs

POB 4436, Stanford, CA 94305
415-321-5601 800-227-8266
Telex: 345567 (Electrolab Pla)
Visa MC Am. Exp.

Contact us for new prices

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Hiplot Plotter	$875.
Hipad Digitizer	715.
IDS 440 Paper tiger	899.
SD Expandoram II (A&T, 64K)	560.
Imsai 65K dynamic RAM III	399.
DC Hayes Micromodem 100 ..	399.
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DC Hayes Micromodem 11 (for apple) $344
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Database Management Systems

HDBS A hierarchical Database Management System featuring fixed length records, read/write protection at file level and one to many set relationships.

Z-80 Optimized	250.00
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6502 Optimized	325.00

MDBS A large computer DBMS with hierarchical and full network data structures (CODASYL Oriented). Explicit representation of one to one, one to many, many to one and many to many sets. Routines are callable from BASIC, PASCAL' COBOL or Machine Language.

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BISYNC-80/3780 A full function IBM 2780/3780 emulator that provides one of the most widely used communications protocols. 550.00

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BISYNC-80/3270 A full function IBM 3275 or 3271/3277 terminal emulator that converts a "dumb" terminal into a very smart one. 550.00

Multiple License Pricing

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*LSI-11, PDP-11 TM DEC, UNIX TM Western Electric, CP/M TM Digital Research

High Level Languages

8080, 8085, Z-80 (Under OS-1 or CP/M)

BASIC

Microsoft Compiler	395.00
Microsoft "BASIC 80"	350.00

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Microsoft "COBOL 80"	750.00

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Whitesmith's "C"	600.00

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Z-80 Optimized (Under OS-1 or CP/M)

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R-M Z-80 COBOL ANSI '74 750.00

LSI-11*/PDP-11* Under RT-11 or RSTS

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Available in R-M COBOL, COBOL 80 and RJ-11. (Source Included)

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Why COBOL?
It's portable (ANSI '74) it's universal!

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OS-1™ A breakthrough in microcomputer software from Electrolabs! UNIX*-like OS with virtual I/O, bank-select memory control to 16 MBY and optional memory protection! Totally compatible with all CP/M programs. You will be amazed at the difference! Excellent brochure available. Includes editor, linker-loader, debugger, and one year update. 249.00

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CP/M Version 2.2	150.00
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CP/M - MCZ Version 2.2. Runs on **ZILOG MCZ** and **PDS-8000** systems.

Only from Software Labs!	200.00
Manuals only	35.00

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*Price of manuals applied against software purchase.

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Important Note: Please specify complete system hardware and software configuration with each order.

California Digital

Post Office Box 3097 B • Torrance, California 90503

Introducing the

ANACOM 150

DOT MATRIX PRINTER

Mfg. suggested list $1350

California Digital Introductory Price

$995

Full 136 Characters for the price of 80

DURABILITY... is the key component of the new Anacom 150. No bells, no whistles, no problems, just consistent high quality output.

This nine wire dot matrix printer features a ballistic type print mechanism guaranteed for three million characters. Low count (16) integrated circuits add to the reliability of the printer.

Microprocessor controlled logic seeking bi-directional head allows the Anacom to print up to speeds of 150 characters per second. 136 columns wide.

Adjustable tractors and variable head gap permit the Anacom to accept fifteen inch wide multi-part forms.

Switch selectable: skip paper perforation, carriage return/line feed and six or eight lines per inch.

Lexan paper shield and enclosure sound proofing add to the overall quality of the printer.

The Anacom 150 is definitely the best value in todays extremely competitive world of micro-printers.

If you are in the market for a "Quality Engineered" dot matrix printer, please consider the Anacom 150 before purchasing a less reliable machine.

Available either RS-232 serial 9600 baud. PRA-150S or Centronic parallel PRA-150P. Field exchange. UPS shipping weight 40 pounds.

IBM 3101 DISPLAY TERMINAL

The new 3101 display terminal is the IBM entry into the plug compatable micro computer industry.

This modularly constructed CRT terminal has been engineered with the user in mind. The video display modules swivels and tilts to provide the operator with a comfortable viewing posture.

Twelve inch P-39 green phosphor screen boasts a crisp 7 by 14 character matrix.

Standard 80 by 24 line screen format with a 25th line to display machine status and aid in the diagnostics in the event of a system malfunction.

87 key Selectric style keyboard arrangement along with numeric entry pad. Eight user definable function keys.

The 3101 video terminal is RS232 compatable and displays all 128 ASCII characters including control codes.

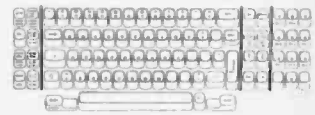
Accessible customer setup switches aid in choosing such options as line speed, parity scroll, and reverse video.

But most of all, built into every 3101 terminal is the quality that you have learned to expect from the IBM Corporation. VDT-3101

IBM direct price $1295

CALIFORNIA DIGITAL discount price

$1195 Immediate delivery

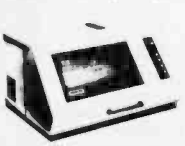


Local Data $4,300

The Quiet 300 from Local Data incorporates the field proven Teletype Model 40 line printer mechanism. The unit attains print speeds upto 300 lines per minute. Switch selectable between RS-232 serial and Centronics parallel interfacing. 132 column full character belt printer with vertical forms control. PRL-300A, 125 lbs.

NEC Spinwriter 5510P/S $2495

The word processing quality Spinwriter prints at speeds upto 55 characters per second. The Model 5510 P/S is supplied with both parallel and RS-232 serial interfacing. Also included is the tractor feed mechanism, along with print thimble and ribbon. PRN-5510PS 70 lbs. Keyboard (KSR) Model 5520 P/S available $2995. PRN-5520PS 75 lbs.



PRINTRONIX $4500

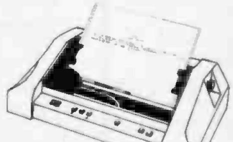
P-300

Forty-four separate print heads shuttle to provide overlapping dots. This unique feature allows a resolution of 60 dots per inch horizontal and 72 vertical.

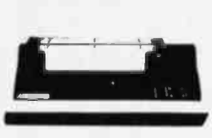
The Printronix P-300 has the capability of outputing pictures, bar codes and large labels, a feature not provided with band or chain printers. PRP-300 200 lbs.

Anadex

$1395 PRX 9500



DP-9500



TI-810

Basic Printer List ~~1895~~

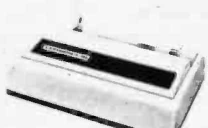
1495 save $400

PRT-810

CENTRONICS

730 $595

737 $795



Both the Centronics 730 and the 737 are capable of accepting standard office letterhead or pin feed continuous forms. For higher resolution the 737 implements a nine wire dot matrix print head. Parallel interfacing. Add $65 for RS232. PRC-730P (S). PRC-737P (S) 17 lbs.

Applied Digital Data Systems Inc

ADDS

REGENT 25 $850
80 character by 24 line twelve inch screen. 18 key numeric-entry cluster. Reverse video. Displayable control characters. VDT-R25 ship. 60 lbs.

REGENT 30 $950
Additional features. Special function keys. High resolution graphics. 25th status line. Multi-intensity screen. Superior quality keyboard. VDT-R30

REGENT 40 $1195
Insert/delete line feature. Eleven special graphic symbols. VDT-R40

REGENT 60 $1495
Buffered display. Block mode transmission. Protected fields. VDT-R60

TELEVIDEO

912B $739

920B $795

920C 875

SOROC

120 $695

140 $995

HAZELTINE

VDT-H

1400 — $695

1410 — 725

1420 — 895

1500 — 950

1510 — 1025

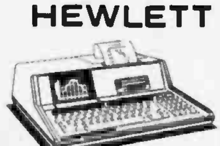
1520 — 1295

BMC VIDEO MONITOR $259

Green phosphor with 18 MHz bandwidth, composit video input make the BMC KG-12C an ideal monitor for anyone requiring a high resolution 12" display.

High impact plastic enclosure assures that the BMC monitor is a rugged take anywhere instrument. For added protection the unit is equipped with a removable smoked non-glare plexiglas screen. VDM-BMC 18 lbs.

HEWLETT PACKARD $2650

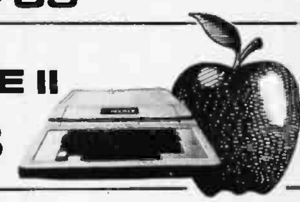


HP 85

The Hewlett Packard HP-85 is a complete, low cost portable computer system. This self contained package includes CPU, keyboard, printer, CRT display and cassette tape drive. SYS-HP85 30 lbs.

APPLE II

$988



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S-100 16K (S-100 Compatible)
- Low Power
- 2 MHz or 4 MHz
- Assembled & Tested

2 MHz....$250.00
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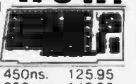

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ASSEMBLED 450 ns. 149.95 KIT 450ns. 125.95
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Vector Graphic 8K Kit $139.95
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- Centronics complete printer
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9629	32K Static RAM 450ns	695.00
9629A	32K Static RAM 200ns	895.00
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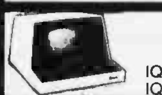

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IQ 140 .... 995.00

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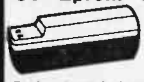

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Professional Industrial Model

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6530-002,003,004,005 .... 21.95
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21L02 250ns.	1.59	1.55	1.15
2111	3.75	3.65	3.55
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Set of 8 416's 49.95
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14	19	36	59
16	20	38	62
18	24	59	84
20	29	69	99
22	24	79	1.10
24	38	85	1.20
28	43	1.10	1.49
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FND500	500	Red	Comm Cathode (+1)	.99
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FND507(510)	500	Red	Comm Anode	.99
FND503	500	Red	Comm Anode (+1)	.99
FND530	500	Green	Comm Cathode	1.49
FND550	500	Orange	Comm Cathode	1.49
FND803(800)	800	Red	Comm Cathode	1.75
FND807(810)	800	Red	Comm Anode	1.75
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HP5082-7300	600	Red	4 x 7 Sgl. Digit RHD	18.95
HP5082-7731	300	Red	Comm Anode	.99
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TIL308	270	Red	Numerical Display	10.95
TIL309	270	Red	Numerical Display	9.95
TIL311	270	Red	4 x 7 Hexidecimal	10.95
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XAN3052	300	Green	Comm Anode Left DP	1.99
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577-10	10 Hole Hard NS, Apple etc	32.75
577-16	16 Hole Hard Micropolis	32.75
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550-16	16 Hole Hard Micro?	39.50
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CTS206-5	1.75	CTS206-9	1.95
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SN7400N	.20	SN7470N	.29	SN74160N	.89
SN7401N	.20	SN7472N	.29	SN74161N	.89
SN7402N	.25	SN7473N	.35	SN74162N	.89
SN7403N	.25	SN7474N	.35	SN74163N	.89
SN7404N	.25	SN7475N	.49	SN74164N	.89
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SN7410N	.25	SN7485N	.89	SN74173N	1.25
SN7411N	.25	SN7486N	.35	SN74174N	.99
SN7412N	.35	SN7489N	1.75	SN74175N	.89
SN7413N	.40	SN7490N	.49	SN74176N	.79
SN7414N	.85	SN7491N	.59	SN74177N	.79
SN7416N	.29	SN7492N	.43	SN74179N	1.95
SN7417N	.29	SN7493N	.43	SN74180N	.79
SN7420N	.29	SN7494N	.65	SN74181N	1.95
SN7421N	.29	SN7495N	.65	SN74182N	.79
SN7422N	.39	SN7496N	.65	SN74184N	2.25
SN7423N	.29	SN7497N	3.00	SN74185N	2.25
SN7425N	.29	SN74100N	1.49	SN74186N	9.95
SN7426N	.29	SN74107N	.35	SN74188N	3.95
SN7427N	.25	SN74109N	.39	SN74190N	1.25
SN7429N	.39	SN74116N	1.95	SN74191N	1.25
SN7430N	.25	SN74121N	.39	SN74192N	.89
SN7432N	.25	SN74122N	.39	SN74193N	.89
SN7437N	.25	SN74123N	.59	SN74194N	.89
SN7438N	.40	SN74125N	.49	SN74195N	.69
SN7439N	.25	SN74126N	.49	SN74196N	.89
SN7440N	.20	SN74132N	.75	SN74197N	.89
SN7441N	.89	SN74136N	.75	SN74198N	1.49
SN7442N	.59	SN74141N	.79	SN74199N	1.49
SN7443N	.75	SN74142N	2.95	SN74S200	4.95
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SN7445N	.75	SN74144N	2.95	SN74279N	.79
SN7446N	.79	SN74145N	.79	SN74283N	2.25
SN7447N	.69	SN74147N	1.95	SN74284N	3.95
SN7448N	.79	SN74148N	1.29	SN74285N	3.95
SN7450N	.20	SN74150N	1.25	SN74365N	.69
SN7451N	.20	SN74151N	.59	SN74366N	.69
SN7453N	.20	SN74152N	.59	SN74367N	.69
SN7454N	.20	SN74153N	.79	SN74368N	.69
SN7459A	.25	SN74154N	1.25	SN74390N	1.95
SN7460N	.20	SN74155N	.79	SN74393N	1.95
		SN74156N	.79		
		SN74157N	.65		

CMOS

CD4000	.39	CD4028	.89	CD4070	.55
CD4001	.39	CD4029	1.49	CD4071	.49
CD4002	.39	CD4030	.49	CD4072	.49
CD4006	1.19	CD4035	.99	CD4076	1.39
CD4007	.25	CD4040	1.49	CD4081	.39
CD4009	.49	CD4041	1.49	CD4082	.39
CD4010	.49	CD4042	.99	CD4093	.99
CD4011	.39	CD4043	.89	CD4098	1.19
CD4012	.25	CD4044	.89	MC14409	14.95
CD4013	.49	CD4046	1.79	MC14410	14.95
CD4014	1.39	CD4047	2.50	MC14411	14.95
CD4015	1.19	CD4048	1.35	MC14419	4.95
CD4016	.59	CD4049	.49	MC14433	13.95
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CD4018	.99	CD4051	1.19	MC14507	.99
CD4019	.49	CD4053	1.19	MC14562	11.95
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CD4021	1.39	CD4059	9.95	CD4508	3.95
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CD4023	.29	CD4066	.79	CD4511	1.29
CD4024	.79	CD4068	.39	CD4515	2.95
CD4025	.23	CD4069	.45	CD4518	1.79
CD4026	2.95			CD4520	1.29
CD4027	.69			CD4566	2.25

74C00

74C00	.39	74C85	1.95	74C163	1.69
74C02	.39	74C90	1.29	74C164	1.59
74C04	.39	74C93	1.29	74C173	1.39
74C08	.39	74C95	1.59	74C192	1.69
74C10	.39	74C107	1.09	74C193	1.69
74C14	.75	74C151	2.95	74C195	1.69
74C20	.39	74C154	3.95	74C922	5.49
74C30	.39	74C157	2.25	74C923	5.75
74C42	1.39	74C160	1.69	74C925	7.50
74C48	1.95	74C161	1.69	74C926	7.50
74C73	.79			80C95	.79
74C74	.79			80C97	.79

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LM300H	.80	LM340T-5	1.25	LM723N/H	.55
LM301CN/H	.35	LM340T-6	1.25	LM733N	1.00
LM302H	1.75	LM340T-8	1.25	LM739N	1.19
LM304H	1.49	LM340T-12	1.25	LM741CN/H	.35
LM305H	.79	LM340T-15	1.25	LM741-14N	.39
LM307CN/H	.45	LM340T-18	1.25	LM747N/H	.79
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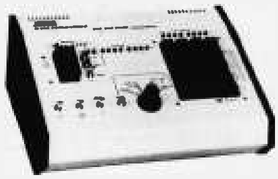
LM320K-24	1.35	NE544N	4.95	LM3909N	1.25
LM320T-5	1.25	NE550N	1.30	MC5558V	.59
LM320T-5.2	1.25	NE555V	.39	8038B	4.95
LM320T-8	1.25	NE556N	.99	LM75450N	.49
LM320T-12	1.25	NE560B	5.00	75451CN	.39
LM320T-15	1.25	NE562B	5.00	75452CN	.39
LM320T-18	1.25	LM565N/H	1.25	75453CN	.39
LM320T-24	1.25	LM566CN	1.75	75454CN	.39
LM323K-5	5.95	LM567V/H	.99	75491CN	.79
LM324N	.99	NE570N	4.95	75492CN	.89
LM339N	.99	LM703CN/H	.69	75493N	1.25
LM340K-5	1.35	LM709N/H	.29	75494CN	1.25
LM340K-6	1.35			RC4136	1.25
LM340K-8	1.35			RC4151	3.95
LM340K-12	1.35			RC4194	4.95
LM340K-15	1.35			RC4195	4.49

74LS00TTL

74LS00	.35	74LS51	.29	74LS139	1.05
74LS01	.35	74LS54	.29	74LS151	1.05
74LS02	.35	74LS55	.29	74LS155	1.05
74LS03	.35	74LS73	.54	74LS157	1.05
74LS04	.42	74LS74	.54	74LS160	1.15
74LS05	.42	74LS75	.71	74LS161	1.39
74LS08	.35	74LS76	.54	74LS162	1.39
74LS09	.42	74LS78	.49	74LS163	1.39
74LS10	.35	74LS83	1.05	74LS164	1.50
74LS11	.75	74LS85	1.50	74LS175	1.25
74LS13	.59	74LS86	.54	74LS181	2.49
74LS14	1.25	74LS90	.71	74LS190	1.25
74LS15	.35	74LS92	.90	74LS191	1.25
74LS20	.35	74LS93	.90	74LS192	1.39
74LS21	.35	74LS95	.99	74LS193	1.39
74LS22	.35	74LS96	1.15	74LS194	1.39
74LS26	.35	74LS107	.54	74LS195	1.39
74LS27	.35	74LS109	.54	74LS253	1.25
74LS28	.35	74LS112	.54	74LS257	1.05
74LS30	.35	74LS123	1.50	74LS258	1.75
74LS32	.42	74LS125	1.05	74LS260	.83
74LS37	.45	74LS132	.99	74LS279	.90
74LS40	.35	74LS136	.59	74LS367	.75
74LS42	1.05	74LS138	1.05	74LS368	.75
74LS47	1.05			74LS670	2.49

JE608 PROGRAMMER

2704/2708 EPROM PROGRAMMER



- 3 separate Display Registers: 8 LED's for Hex Key entries, 16 LED's (2" 2") for Address Register and 8 LED's for Data Memory Register. The Data Memory Register displays the content of the RAMs from the EPROM Chip.
- Development of microprocessor systems by means of a ribbon cable from the programmer panel test socket to the EPROM socket on the microprocessor board.
- Rapid checking verification of programmed data changes.
- User may move data from a master to RAM's or write into RAM's with keyboard entries.
- Allows manual stepping manipulation (up and down) at any address location.
- Stand alone EPROM Programmer consisting of: A 19-key Hexadecimal Keyboard assembly, Programmer Board assembly with 4 power supplies and a LED/Test Socket Panel Board assembly. The Test Socket is zero force insertion type. Power requirements: 115VAC, 60Hz, 6W.
- Compact desk-top enclosure: Color-coordinated designer's case with light tan panels and molded end pieces in mocha brown. Size: 3¼"H x 11"W x 8¼"D. Weight: 6 lbs.

The JE608 EPROM Programmer is a completely self contained unit which is independent of computer control and requires no additional systems for its operations. The EPROM can be programmed from the Hexadecimal Keyboard or from a pre programmed EPROM. The JE608 Programmer can emulate a programmed EPROM by the use of its internal RAM circuits. This will allow the user to test or pretest a program, for a system, prior to programming a chip. Any changes in the program can be entered directly into the memory circuits with the Hexadecimal Keyboard so that rewriting the entire program will not be necessary. The JE608 Programmer contains a Programmer/Board with 25 IC's and including power supplies of −5V, +5V, +12V and +26V. The Hexadecimal Keyboard and LED/Test Socket Panel Board are separate assemblies within the system.

JE608K KIT $399.95
JE608A Assembled and tested $499.95

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XC556R	.200"	red	5/$1	MV50	.085"	red	6/$1	XC111R	.190"	red	5/$1
XC556G	.200"	green	4/$1	XC209R	.125"	red	5/$1	XC111G	.190"	green	4/$1
XC556Y	.200"	yellow	4/$1	XC209G	.125"	green	4/$1	XC111Y	.190"	yellow	4/$1
XC556C	.200"	clear	4/$1	XC209Y	.125"	yellow	4/$1	XC111C	.190"	clear	4/$1
XC22R	.200"	red	5/$1	XC526R	.185"	red	5/$1				
XC22G	.200"	green	4/$1	XC526G	.185"	green	4/$1	INFRA-RED LED			
XC22Y	.200"	yellow	4/$1	XC526Y	.185"	yellow	4/$1	¼"x¼"x1/16" flat			
MV10B	.170"	red	4/$1	XC526C	.185"	clear	4/$1	1RL — 5/$1			

DISPLAY LEDS

C.A. — Common Anode | C.C. — Common Cathode

Type	Polarity	Ht	Price	Type	Polarity	Ht	Price
MAN 1	C.A.—red	.270	2.95	DL707	C.A.—red	.300	.99
MAN 2	5x7 D.M.—red	.300	4.95	DL728	C.C.—red	.500	1.49
MAN 3	C.C.—red	.125	.25	DL741	C.A.—red	.600	1.25
MAN 4	C.C.—red	.187	1.95	DL746	C.A.—red ± 1	.630	1.49
MAN 7G	C.A.—green	.300	1.25	DL747	C.A.—red	.600	1.49
MAN 7Y	C.A.—yellow	.300	.99	DL750	C.C.—red	.600	1.49
MAN 72	C.A.—red	.300	.75	DL338	C.C.—red	.110	.35
MAN 74	C.C.—red	.300	1.25	FND70	C.C.	.250	.69
MAN 82	C.A.—yellow	.300	.49	FND358	C.C. ± 1	.357	.99
MAN 84	C.C.—yellow	.300	.99	FND359	C.C.	.357	.75
MAN 3620	C.A.—orange	.300	.49	FND503	C.C. (FND500)	.500	.99
MAN 3630	C.A.—orange ± 1	.300	.99	FND507	C.A. (FND510)	.500	.99
MAN 3640	C.C.—orange	.300	.99	5082-7730	C.A.—red	.300	.99
MAN 4610	C.A.—orange	.400	.99	HDSP-3400	C.A.—red	.800	1.50
MAN 4810	C.A.—yellow	.400	.99	HDSP-3403	C.C.—red	.800	1.50
MAN 4840	C.C.—yellow	.400	.99	5082-7613	C.C., R.H.D.—red	.300	1.25
MAN 6610	C.A.—orange—DD	.560	.99	5082-7620	C.A., L.H.D.—yel.	.300	1.25
MAN 6630	C.A.—orange ± 1	.560	.99	5082-7623	C.C., R.H.D.—yel.	.300	1.25
MAN 6640	C.C.—orange—DD	.560	.99	5082-7730	C.A., L.H.D.—red	.300	.99
MAN 6650	C.C.—orange ± 1	.560	.99	5082-7731	C.A., R.H.D.—red	.300	1.25
MAN 6660	C.A.—orange	.560	.99	5082-7750	C.A., L.H.D.—red	.430	1.25
MAN 6710	C.A.—red—DD	.560	.99	5082-7751	C.A., R.H.D.—red	.430	1.25
MAN 6750	C.C.—red ± 1	.560	.99	5082-7760	C.C., R.H.D.—red	.430	1.25
MAN 6760	C.A.—red	.560	.99	5082-7300	4x7 sgl. dig. RHDP	.600	19.95
MAN 6780	C.C.—red	.560	.99	5082-7302	4x7 sgl. dig. LHDP	.600	19.95
DL701	C.A.—red ± 1	.300	.99	5082-7304	Overnge. char. (±1)	.600	15.00
DL704	C.C.—red	.300	.99	5082-7340	4x7 sgl. dig. hex.	.600	22.50

RCA LINEAR

CA3013T	2.15	CA3082N	2.00
CA2023T	3.25	CA3083N	1.60
CA3035T	2.48	CA3086N	.85
CA3039T	1.35	CA3089N	3.75
CA3046N	1.30	CA3130T	1.39
CA3059N	3.25	CA3140T	1.25
CA3060N	3.25	CA3160T	1.25
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DM8865	1.00
DM8887	.75
DM8889	.75
9374 7-seg. LED driver	1.50
MM5309	4.95

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MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5377	4.95
MM5387/1998a	4.95

MOTOROLA

MC1408L7	4.95
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MC3022P	2.95
MC3061P	3.50
MC4016(74416)	7.50
MC4024P	3.95
MC4040P	6.95
MC4044P	4.50

LOW PROFILE (TIN) SOCKETS

	1-24	25-49	50-100
8 pin LP	.17	.16	.15
14 pin LP	.20	.19	.18
16 pin LP	.22	.21	.20
18 pin LP	.29	.28	.27
20 pin LP	.34	.32	.30
22 pin LP	.37	.36	.35
24 pin LP	.38	.37	.36
28 pin LP	.45	.44	.43
36 pin LP	.60	.59	.58
40 pin LP	.63	.62	.61

SOLDERTAIL STANDARD (TIN)

	1-24	25-49	50-100
14 pin ST	.27	.25	.24
16 pin ST	.30	.27	.25
18 pin ST	.35	.32	.30
24 pin ST	.49	.45	.42
28 pin ST	.99	.90	.81
36 pin ST	1.39	1.26	1.15
40 pin ST	1.59	1.45	1.30

SOLDERTAIL (GOLD) STANDARD

	1-24	25-49	50-100
8 pin SG	.39	.35	.31
14 pin SG	.49	.45	.41
16 pin SG	.54	.49	.44
18 pin SG	.59	.53	.48
24 pin SG	.79	.75	.69
28 pin SG	1.10	1.00	.90
36 pin SG	1.65	1.40	1.26
40 pin SG	1.75	1.59	1.45

WIRE WRAP SOCKETS (GOLD) LEVEL #3

	1-24	25-49	50-100
8 pin WW	.59	.54	.49
10 pin WW	.69	.63	.58
14 pin WW	.79	.73	.67
16 pin WW	.85	.77	.70
18 pin WW	.99	.90	.81
20 pin WW	1.19	1.08	.99
22 pin WW	1.39	1.35	1.23
24 pin WW	1.49	1.26	1.14
28 pin WW	1.69	1.53	1.38
36 pin WW	2.19	1.99	1.79
40 pin WW	2.29	2.09	1.89

1/4 WATT RESISTOR ASSORTMENTS – 5%

ASST. 1	5 ea.	10 OHM / 27 OHM	12 OHM / 33 OHM	15 OHM / 39 OHM	18 OHM / 47 OHM	22 OHM / 56 OHM	50 PCS	$1.95
ASST. 2	5 ea.	68 OHM / 180 OHM	82 OHM / 220 OHM	100 OHM / 270 OHM	120 OHM / 330 OHM	150 OHM / 390 OHM	50 PCS	$1.95
ASST. 3	5 ea.	470 OHM / 1.2K	560 OHM / 1.5K	680 OHM / 1.8K	820 OHM / 2.2K	1K / 2.7K	50 PCS	$1.95
ASST. 4	5 ea.	3.3K / 8.2K	3.9K / 10K	4.7K / 12K	5.6K / 15K	6.8K / 18K	50 PCS	$1.95
ASST. 5	5 ea.	22K / 56K	27K / 68K	33K / 82K	39K / 100K	47K / 120K	50 PCS	$1.95
ASST. 6	5 ea.	150K / 390K	180K / 470K	220K / 560K	270K / 680K	330K / 820K	50 PCS	$1.95
ASST. 7	5 ea.	1M / 2.7M	1.2M / 3.3M	1.5M / 3.9M	1.8M / 4.7M	2.2M / 5.6M	50 PCS	$1.95

ASST. 8R Includes Resistor Assortments 1-7 (350 PCS.) $10.95 ea.

$10.00 Min. Order — U.S. Funds Only
Calif. Residents Add 6% Sales Tax
Postage — Add 5% plus $1 Insurance (if desired)

Spec Sheets — 25¢
1981 Catalog Available — Send 41¢ stamp

NEW 1981 CATALOG

Jameco ELECTRONICS

PHONE ORDERS WELCOME (415) 592-8097

MAIL ORDER ELECTRONICS — WORLDWIDE
1355 SHOREWAY ROAD, BELMONT, CA 94002
PRICES SUBJECT TO CHANGE

10/80

TELEPHONE/KEYBOARD CHIPS

AY-5-9100	Push Button Telephone Dialler	$14.95
AY-5-9200	Repertory Dialler	14.95
AY-5-9500	CMOS Clock Generator	4.95
AY-5-2376	Keyboard Encoder (88 keys)	11.95
HD0165	Keyboard Encoder (16 keys)	7.95
74C922	Keyboard Encoder (16 keys)	5.49
74C923	Keyboard Encoder (20 keys)	5.75

ICM CHIPS

ICM7045	CMOS Precision Timer	24.95
ICM7205	CMOS LED Stopwatch/Timer	19.95
ICM7207	Oscillator Controller	7.50
ICM7208	Seven Decade Counter	19.95
ICM7209	Clock Generator	6.95

NMOS READ ONLY MEMORIES

MCM6571	128 X 9 X 7 ASCII Shifted with Greek	13.50
MCM6574	128 X 9 X 7 Math Symbol & Pictures	13.50
MCM6575	128 X 9 X 7 Alpha Control Char. Gen	13.50

MISCELLANEOUS

TL074CN	Quad Low Noise bi-fet Op Amp	2.49
TL494CN	Switching Regulator	4.49
TL496CP	Single Switching Regulator	1.75
11C90	Divide 10/11 Prescaler	14.95
95H90	Hi-Speed Divide 10/11 Prescaler	11.95
4N33	Photo-Darlington Opto-Isolator	1.25
MK50240	Top Octave Freq. Generator	17.50
DS0026CH	5MHz 2-phase MOS clock driver	3.75
TIL308	.27" red num. display w/integ. logic chip	10.95
MM5320	TV Camera Sync. Generator	14.95
MM5330	4½ Digit DPM Logic Block (Special)	3.95
LD110/111	3½ Digit A/D Converter Set	25.00/set
MC14433P	3½ Digit A/D Converter	13.95

LITRONIX ISO-LIT 1
Photo Transistor Opto-Isolator
(Same as MCT 2 or 4N25)
49¢ each

SN 76477
SOUND GENERATOR
Generates Complex Sounds
Low Power - Programmable
$3.95 each

TV GAME CHIP AND CRYSTAL
AY-3-8500-1 and 2.01 MHZ Crystal (Chip & Crystal includes score display, 6 games and select angles, etc.) $7.95/set

EXAR

XR205	$8.40	JE2206KB	19.95	XR2242CP	1.50
XR210	4.40	XR1800	3.20	XR2264	4.25
XR215	4.40	XR2206	4.40	XR2556	3.20
XR320	1.55	XR2207	3.85	XR2567	2.99
XR-L555	1.50	XR2208	5.20	XR3403	1.25
XR555	.39	XR2209	1.75	XR4136	1.25
XR556	.99	XR2211	5.25	XR4151	3.95
XR567CP	.99	XR2212	4.35	XR4194	1.45
XR567CT	1.25	XR2240	3.45	XR4202	3.60
XR1310P	1.95			XR4212	2.05
XR1468CN	3.85			XR4558	.75
XR1488	1.95			XR4739	1.15
XR1489	1.95			XR4741	1.47

DIODES

TYPE	VOLTS	W	PRICE	TYPE	VOLTS	W	PRICE
1N746	3.3	400m	4/1.00	1N4002	100 PIV	1 AMP	12/1.00
1N751	5.1	400m	4/1.00	1N4003	200 PIV	1 AMP	12/1.00
1N752	5.6	400m	4/1.00	1N4004	400 PIV	1 AMP	12/1.00
1N753	6.2	400m	4/1.00	1N4005	600 PIV	1 AMP	10/1.00
1N754	6.8	400m	4/1.00	1N4006	800 PIV	1 AMP	10/1.00
1N757	9.0	400m	4/1.00	1N4007	1000 PIV	1 AMP	10/1.00
1N759	12.0	400m	4/1.00	1N3600	50	200m	6/1.00
1N959	8.2	400m	4/1.00	1N4148	75	10m	15/1.00
1N965	15	400m	4/1.00	1N4154	35	10m	12/1.00
1N5232	5.6	500m	4/1.00	1N4733	5.1	1w	4/1.00
1N5234	6.2	500m	4/1.00	1N4734	5.6	1w	4/1.00
1N5235	6.8	500m	4/1.00	1N4735	6.2	1w	4/1.00
1N5236	7.5	500m	4/1.00	1N4736	6.8	1w	4/1.00
1N5242	12	500m	4/1.00	1N4738	8.2	1w	4/1.00
1N5245	15	500m	4/1.00	1N4742	12	1w	4/1.00
1N456	25	40m	6/1.00	1N4744	15	1w	4/1.00
1N458	150	7m	6/1.00	1N1183	50 PIV	35 AMP	1.60
1N485A	180	10m	5/1.00	1N1184	100 PIV	35 AMP	1.70
1N4001	50 PIV	1 AMP	12/1.00	1N1185	150 PIV	35 AMP	1.70
				1N1186	200 PIV	35 AMP	1.80
				1N1188	400 PIV	35 AMP	3.00

SCR AND FW BRIDGE RECTIFIERS

C36D	15A	@	400V	SCR(2N1849)	$1.95
C36M	35A	@	600V	SCR	2.25
C106B1	3.6A	@	200V	SCR	.50
2N2328	1.6A	@	300V	SCR	.50
MDA 980-1	12A	@	50V	FW Bridge Rec.	1.95
MDA 980-3	12A	@	200V	FW Bridge Rec.	2.25

TRANSISTORS

MPSA05	3/1.00	2N3055	.89	2N3904	4/1.00
MPSA06	3/1.00	MJE3055	1.00	2N3905	4/1.00
TIS97	4/1.00	2N3392	4/1.00	2N3906	4/1.00
TIS98	4/1.00	2N3398	4/1.00	2N4013	.65
40409	1.75	PN3567	3/1.00	2N4123	4/1.00
40410	1.75	PN3568	4/1.00	PN4249	4/1.00
40673	1.75	PN3569	4/1.00	PN4250	4/1.00
2N918	2/1.00	MPS3638A	4/1.00	2N4400	4/1.00
2N2219A	2/1.00	MPS3702	4/1.00	2N4401	4/1.00
2N2221A	3/1.00	2N3704	4/1.00	2N4402	4/1.00
2N2222A	3/1.00	MPS3704	4/1.00	2N4403	4/1.00
PN2222 Plastic	6/1.00	2N3705	4/1.00	2N4409	4/1.00
2N2369A	2/1.00	MPS3705	4/1.00	2N5086	4/1.00
MPS2369	4/1.00	2N3706	4/1.00	2N5087	4/1.00
2N2484	4/1.00	MPS3706	4/1.00	2N5088	4/1.00
2N2906	2/1.00	2N3707	4/1.00	2N5089	4/1.00
2N2907	3/1.00	2N3711	4/1.00	2N5129	4/1.00
2N2925	4/1.00	2N3724A	.65	PN5134	4/1.00
MJE2955	1.25	2N3725A	1.00	PN5138	4/1.00
2N3053	2/1.00	2N3772	2.25	2N5139	4/1.00
		2N3823	1.00	2N5210	4/1.00
		2N3903	4/1.00	2N5449	3/1.00
				2N5951	2/1.00

CAPACITOR CORNER

50 VOLT CERAMIC DISC CAPACITORS

	1-9	10-99	100-		1-9	10-99	100-
10 pf	.08	.06	.05	.001µF	.08	.06	.05
22 pf	.08	.06	.05	.0047µF	.08	.06	.05
47 pf	.08	.06	.05	.01µF	.08	.06	.05
100 pf	.08	.06	.05	.022µF	.09	.07	.06
220 pf	.08	.06	.05	.047µF	.09	.07	.06
470 pf	.08	.06	.05	.1µF	.15	.12	.10

100 VOLT MYLAR FILM CAPACITORS

.001mf	.12	.10	.07	.022mf	.13	.11	.08
.0022	.12	.10	.07	.047mf	.21	.17	.13
.0047mf	.12	.10	.07	.1mf	.27	.23	.17
.01mf	.12	.10	.07	.22mf	.33	.27	.22

+20% DIPPED TANTALUMS (SOLID) CAPACITORS

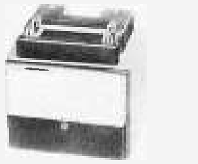
.1/35V	.39	.34	.29	1.5/35V	.41	.37	.29
.15/35V	.39	.34	.29	2.2/25V	.51	.45	.34
.22/35V	.39	.34	.29	3.3/25V	.53	.47	.37
.33/35V	.39	.34	.29	4.7/25V	.63	.56	.45
.47/35V	.39	.34	.29	6.8/25V	.79	.69	.55
.68/35V	.39	.34	.29	15/25V	1.39	1.25	.95
1.0/35V	.39	.34	.29	22/6V	.79	.69	.56

MINIATURE ALUMINUM ELECTROLYTIC CAPACITORS

Axial Lead				Radial Lead			
.47/50V	.16	.14	.10	.47/25V	.15	.13	.12
1.0/50V	.19	.16	.12	.47/50V	.16	.14	.13
3.3/50V	.17	.15	.11	1.0/16V	.15	.13	.12
4.7/25V	.18	.15	.11	1.0/25V	.16	.14	.13
10/25V	.18	.15	.11	1.0/50V	.17	.15	.14
10/50V	.19	.16	.12	4.7/16V	.15	.13	.12
22/25V	.19	.16	.12	4.7/25V	.16	.14	.13
22/50V	.24	.20	.18	4.7/50V	.17	.15	.13
47/25V	.25	.21	.19	10/16V	.15	.13	.12
47/50V	.29	.25	.23	10/25V	.16	.14	.13
100/25V	.28	.24	.22	10/50V	.17	.15	.14
100/50V	.41	.37	.34	47/50V	.25	.21	.19
220/25V	.39	.34	.30	100/16V	.21	.17	.14
220/50V	.49	.45	.41	100/25V	.25	.23	.21
470/25V	.54	.49	.45	100/50V	.37	.34	.31
1000/16V	.79	.69	.61	220/16V	.29	.25	.22
2200/16V	.89	.79	.69	470/25V	.35	.31	.27

Circle 342 on inquiry card.

BLAK-RAY Ultraviolet Intensity Meter



TWO MODELS: LONG WAVE AND SHORT WAVE

Meter consists of a sensor cell attached to a compact (3" x 3¼" x 3") metering unit. Can be hand-held or placed directly on surface for measuring. Can be used remotely, while connected to a meter housing by a 4-foot extension cord. Two models available — one for long wave and one for short wave ultraviolet. Readings are in microwatts per square centimeter. Weight: 1 lb.

Completely assembled (includes sensor cell, reduction screen, extension cord, contrast filter and certification report.)

J-221 LONG WAVE (300nm-400nm) **$242.00**

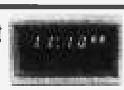
J-225 SHORT WAVE (200nm-280nm) **$260.00**

EPROM Erasing Lamp

- Erases 2708, 2716, 1702A, 5203Q, 5204Q, etc.
- Erases up to 4 chips within 20 minutes
- Maintains constant exposure distance of one inch
- Special conductive foam liner eliminates static build-up
- Built-in safety lock to prevent UV exposure
- Compact — only 7-5/8" x 2-7/8" x 2"
- Complete with holding tray for 4 chips

UVS-11E **$79.50**

Jumbo 6-Digit Clock Kit



- Four .630"ht. and two .300"ht. common anode displays
- Uses MM5314 clock chip
- Switches for hours, minutes and hold functions
- Hours easily viewable to 30 feet
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hour operation
- Includes all components, case and wall transformer
- Size: 6¾ x 3⅛ x 1¾

JE747 .... **$29.95**

- Bright .300 ht. comm. cathode display
- Uses MM5314 clock chip
- Switches for hours, minutes and hold modes
- Hrs. easily viewable to 20 ft.
- Simulated walnut case
- 115 VAC operation
- 12 or 24 hr. operation
- Incl. all components, case & wall transformer
- Size: 6¾" x 3-1/8" x 1¾"

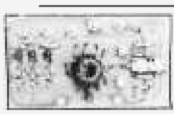
JE701

6-Digit Clock Kit $19.95

Regulated Power Supply

Uses LM309K. Heat sink provided. PC board construction. Provides a solid 1 amp @ 5 volts. Can supply up to +5V, ±9V and ±12V with JE205 Adapter. Includes components, hardware and instructions. Size: 3½" x 5" x 2"H

JE200....... **$14.95**



ADAPTER BOARD —Adapts to JE200— ±5V, ±9V and ±12V

DC/DC converter with +5V input. Toriodal high-speed switching XMFR. Short circuit protection. PC board construction. Piggy-back to JE 200 board. Size: 3½" x 2" x 9/16"H

JE205 .... **$12.95**

MICROPROCESSOR COMPONENTS

8080A/8080A SUPPORT DEVICES		
8080A	CPU	$ 7 95
8212	8-Bit Input/Output	3.25
8214	Priority Interrupt Control	5.95
8216	Bi-Directional Bus Driver	3.49
8224	Clock Generator/Driver	3.95
8226	Bus Driver	3 49
8228	System Controller/Bus Driver	·4 95
8238	System Controller	5.95
8251	Prog Comm. I/O (USART)	7.95
8253	Prog Interval Timer	14 95
8255	Prog Periph. I/O (PPI)	9.95
8257	Prog DMA Control	19.95
8259	Prog Interrupt Control	14.95

6800/6800 SUPPORT DEVICES		
MC6800	MPU	$14.95
MC6802CP	MPU with Clock and Ram	19.95
MC6810API	128X8 Static Ram	4.95
MC6821	Periph Inter. Adapt (MC6820)	7.49
MC6828	Priority Interrupt Controller	10.95
MC6830L8	1024X8 Bit ROM (MC68A30-8)	14.95
MC6850	Asynchronous Comm. Adapter	6.95
MC6852	Synchronous Serial Data Adapt	6.95
MC6860	0-600 bps Digital MODEM	10.95
MC6862	2400 bps Modulator	12.95
MC6880A	Quad 3-State Bus. Trans (MC8T26)	2.25

MICROPROCESSOR CHIPS—MISCELLANEOUS		
Z80(780C)	CPU	$13.95
Z80A(780-1)	CPU	15.95
CDP1802	CPU	19.95
2650	MPU	16.95
6502	CPU	11 95
8035N6	8-Bit MPU w/clock, RAM, I/O lines	19.95
P8085	CPU	19 95
TMS9900JL	16-Bit MPU	49 95

SHIFT REGISTERS		
MM500H	Dual 25 Bit Dynamic	$ 50
MM503H	Dual 50 Bit Dynamic	50
MM506H	Dual 100 Bit Static	.50
MM510H	Dual 64 Bit Accumulator	.50
MM5016H	500/512 Bit Dynamic	89
2504(1404A)	1024 Dynamic	3 95
2518	Hex 32 Bit Static	4 95
2522	Dual 132 Bit Static	2 95
2524	512 Bit Dynamic	.99
2525	1024 Dynamic	2 95
2527	Dual 256 Bit Static	2 95
2528	Dual 250 Static	4 00
2529	Dual 240 Bit Static	4 00
2532	Quad 80 Bit Static	2 95
3341	Fifo	6 95
74LS670	4X4 Register File (TriState)	2.49

UART'S		
A-Y-5-1013	30K BAUD	5 95

MICROPROCESSOR MANUALS		
M-Z80	User Manual	$7.50
M-CDP1802	User Manual	7.50
M-2650	User Manual	5.00

ROM'S		
2513(2140)	Character Generator(upper case)	$9.95
2513(3021)	Character Generator(lower case)	9.95
2516	Character Generator	10.95
MM5230N	2048-Bit Read Only Memory	1.95

RAM'S			
1101	256X1	Static	$1.49
1103	1024X1	Dynamic	.99
2101(8101)	256X4	Static	3.95
2102	1024X1	Static	1.75
21L02	1024X1	Static	1.95
2111(8111)	256X4	Static	3.95
2112	256X4	Static MOS	4.95
2114	1024X4	Static 450ns	5.95
2114L	1024X4	Static 450ns low power	6.95
2114-3	1024X4	Static 300ns	7.49
2114L-3	1024X4	Static 300ns low power	7.95
5101	256X4	Static	7.95
5280/2107	4096X1	Dynamic	4.95
7489	16X4	Static	1.75
UPD414 (MK4027)	4K	Dynamic 16 pin	4.95
MM5290-2	16K	Dynamic 16 pin 150NS (UPD416/MK4116)	6.95
TMS4044-45NL	4K	Static	14.95
TMS4045	1024X4	Static	14.95
2117	16,384X1	Dynamic 350ns (house marked)	9.95
MM5262	2KX1	Dynamic	4/1.00

PROM'S			
1702A	2048	FAMOS	$5 95
2716	16K*	EPROM (Intel)	29.95
TMS2516	16K*	EPROM (2716)	19.95
	*Requires single +5V power supply		
TMS2532	4KX8	EPROM	89.95
2708	8K	EPROM	10.95
2716 T	16K**	EPROM	29.95
	**Requires 3 voltages. —5V. +5V. +12V		
5203	2048	PROM	4.95
6301-1(7611)	1024	Tristate Bipolar	3.49
6330-1(7602)	256	Open C Bipolar	2.95
82S23	32X8	Open Collector	3.95
82S115	4096	Bipolar	19.95
82S123(5610)	32X8	Tristate	3.95
74186	512	TTL Open Collector	9.95
74188	256	TTL Open Collector	3.95
74S287	1024	Static	4.95

Function Generator Kit

Provides 3 basic waveforms: sine, triangle and square wave. Freq. range from 1 Hz to 100K Hz. Output amplitude from 0 volts to over 6 volts (peak to peak). Uses a 12V supply or a ±6V split supply. Includes chip, P.C. Board, components & instructions.

JE2206B....**$19.95**

DIGITAL THERMOMETER KIT

- Dual sensors—control switch for indoor/outdoor or dual monitoring—extension up to 500 feet
- Continuous LED .8" ht. display
- Range: -40°F to 199°F / -40°C to 100°C
- Accuracy: ±1° nominal
- Calibrate for Fahrenheit/Celsius reading
- Sim. walnut case—AC wall adapter incl.
- Size: 3¼"H x 6-5/8"W x 1-3/8"D

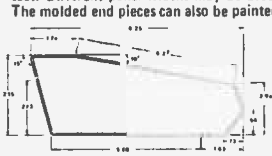
JE300 ....**$39.95**

DESIGNERS' SERIES
Blank Desk-Top Electronic Enclosures

- High strength epoxy molded end pieces in mocha brown finish.
- Sliding rear/bottom panel for service and component accessibility.
- Top / bottom panels .080 thk alum. Alodine type 1200 finish (gold tint color) for best paint adhesion after modification.
- Vented top and bottom panels for cooling efficiency.
- Rigid construction provides unlimited applications.

CONSTRUCTION:

The "DTE" Blank Desk Top Electronic Enclosures are designed to blend and complement today's modern computer equipment and can be used in both industrial and home. The end pieces are precision molded with an internal slot (all around) to accept both top and bottom panels. The panels are then fastened to ¼" thick tabs inside the end pieces to provide maximum rigidity to the enclosure. For ease of equipment servicing, the rear/bottom panel slides back on slotted tracks while the rest of the enclosure remains intact. Different panel widths may be used while maintaining a common profile outline. The molded end pieces can also be painted to match any panel color scheme.



Enclosure Model No.	Panel Width	PRICE
DTE-8	8.00"	$29.95
DTE-11	10.65"	$32.95
DTE-14	14.00"	$34.95

$10.00 Min. Order — U.S. Funds Only
Calif. Residents Add 6% Sales Tax
Postage — Add 5% plus $1 Insurance (if desired)

Spec Sheets — 25¢
1981 Catalog Available — Send 41¢ stamp

NEW 1981 CATALOG

Jameco ELECTRONICS

PHONE ORDERS WELCOME (415) 592-8097

MAIL ORDER ELECTRONICS — WORLDWIDE
1355 SHOREWAY ROAD, BELMONT, CA 94002
PRICES SUBJECT TO CHANGE

10/80

National Semiconductor

RAM SALE

MM5290J-2 (MK4116/UPD416)... **$6.95 each**
16K DYNAMIC RAM (150NS)
(8 EACH $49.95) (100 EACH $550.00/lot)

MM5298J-3A .... **$3.25 each**
8K DYNAMIC RAM (LOW HALF OF MM5290J) 200NS
(8 EACH $23.95) (100 EACH $250.00/lot)

MM2114-3 .... **$5.95 each**
4K STATIC RAM (300NS)
(8 EACH $43.95) (100 EACH $450.00/lot)

MM2114L-3 .... **$6.25 each**
4K STATIC RAM (LOW POWER 300NS)
(8 EACH $44.95) (100 EACH $475.00/lot)

ok®

Vacuum Vise

Vacuum-based light-duty vise for small components and assemblies. ABS construction. 1½" jaws, 1½" travel. Can be permanently installed.

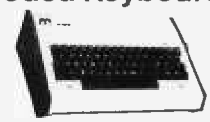
VV-1...... **$3.49**

TRS-80 16K Conversion Kit

Expand your 4K TRS-80 System to 16K.
Kit comes complete with:
- 8 each MM5290-2 (UPO416) (16K Dynamic Rams) 150NS
- Documentation for conversion

TRS-16K **$49.95**

JE610 ASCII Encoded Keyboard Kit



The JE610 ASCII Keyboard Kit can be interfaced into most any computer system. The kit comes complete with an industrial grade keyboard switch assembly (62-keys), IC's, sockets, connector, electronic components and a double-sided printed wiring board. The keyboard assembly requires +5V @ 150mA and −12V @ 10mA for operation. Features: 60 keys generate the 126 characters, upper and lower case ASCII set. Fully buffered. Two user-define keys provided for custom applications. Caps lock for upper-case-only alpha characters. Utilizes a 2376 (40-pin) encoder read-only memory chip. Outputs directly compatible with TTL/DTL or MOS logic arrays. Easy interfacing with a 16-pin dip or 18-pin edge connector.

JE610 (Case not included) **$79.95**

Desk-Top Enclosure for JE610 ASCII Encoded Keyboard Kit

Compact desk-top enclosure: Color-coordinated designer's case with light tan aluminum panels and molded end pieces in mocha brown. Includes mounting hardware. Size: 3½"H x 14½"W x 8¾"D.

DTE-AK **$49.95**

SPECIAL: JE610/DTE-AK PURCHASED TOGETHER (Value $129.90) $124.95

JE600 Hexadecimal Encoder Kit

FULL 8-BIT LATCHED OUTPUT 19-KEY KEYBOARD

The JE600 Encoder Keyboard Kit provides two separate hexadecimal digits produced from sequential key entries to allow direct programming for 8-bit microprocessor or 8-bit memory circuits. Three additional keys are provided for user operations with one having a bistable output available. The outputs are latched and monitored with 9 LED readouts. Also included is a key entry strobe. Features: Full 8-bit latched output for microprocessor use. Three user-define keys with one being bistable operation. Debounce circuit provided for all 19 keys. 9 LED readouts to verify entries. Easy interfacing with standard 16-pin IC connector. Only +5VDC required for operation.

JE600 (Case not included) **$59.95**

Desk-Top Enclosure for JE600 Hexadecimal Keyboard Kit

Compact desk-top enclosure: Color-coordinated designer's case with light tan aluminum panels and molded end pieces in mocha brown. Includes mounting hardware. Size: 3½"H x 8¾"W x 8¾"D.

DTE-HK **$44.95**

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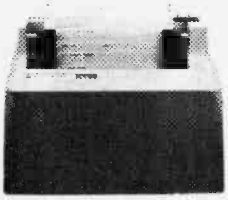
The Paper Tiger Printer From Integral Data



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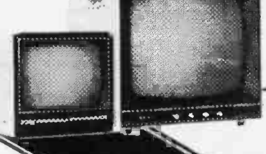

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2/4 MHz Z-80A CPU w/serial I/O port
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- MEM-48132A *48K Jade A & T* $355.00
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- MEM-32631A *32K Jade A & T* $339.95
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- MEM-48631A *48K Jade A & T* $374.95
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- CPK-50165 *1K AIM* $374.95
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- PSX-030A *Power supply* $59.95
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- CPS-30010K *Kit* $319.95
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12" B & W video monitor with 12 MHz bandwidth
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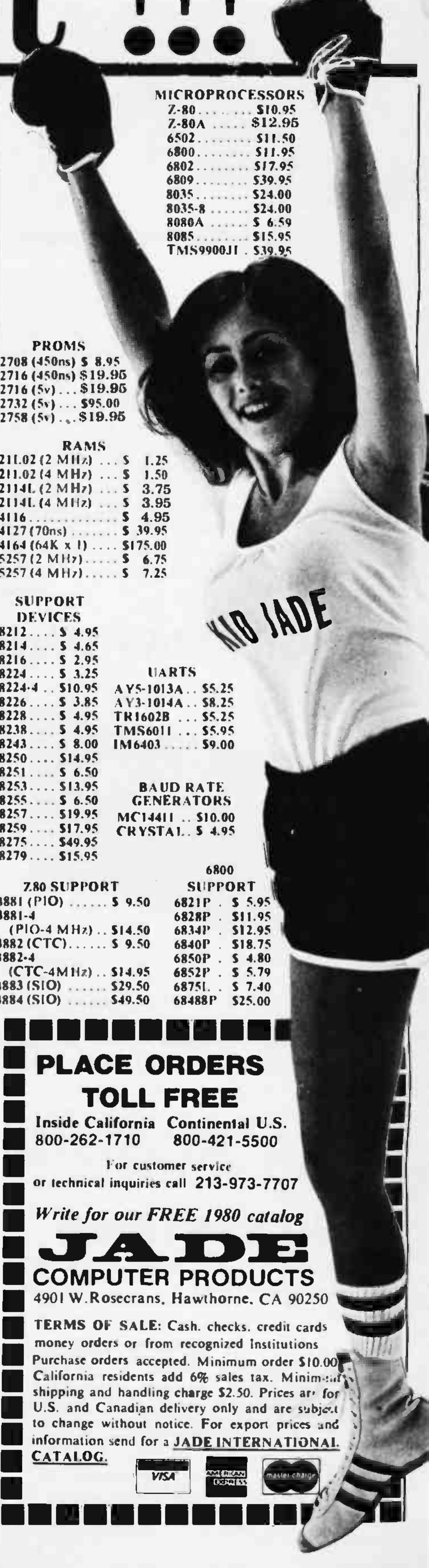

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IOS-2015A *A & T* $275.00

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CPX-30800A *A & T* $298.00

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MMD-8120103 *Soft sector* $55.95
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Z-80A $12.95
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6809 .... $39.95
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8035-8 ...... $24.00
8080A .... $ 6.59
8085 .... $15.95
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2716 (450ns) $19.95
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3882 (CTC) ...... $ 9.50
3882-4 (CTC-4MHz) .. $14.95
3883 (SIO) $29.50
3884 (SIO) $49.50

6800 SUPPORT
6821P . $ 5.95
6828P . $11.95
6834P . $12.95
6840P . $18.75
6850P . $ 4.80
6852P . $ 5.79
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68488P $25.00

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Computers, Disk Systems

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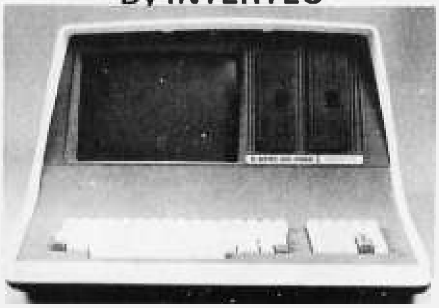
By INTERTEC



32K or 64K (Double or Quad Density units available). Uses two Z-80 CPU's. Commercial-type terminal with 12" monitor. Dual double density minifloppies. Over 350 kilobytes of storage (twice that with quad density drives). Two serial RS232 ports, I/O ports standard. Expandable with optional S-100 S-100 interface. Comes with CP/M™ 2.2 operating system. MiniMicroMart includes BASIC interpreter and can supply a wide range of CP/M Development and Application software.

w/32K Double Density, List $2995 . **$2685**
w/64K Double Density, List $3345 ..... $2883
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W/64K Quad — MiniMicroMart Upgrade Special..................... $3395

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A 64K complete computer with dual density 8" floppies (1 megabyte). Rack or vertical mounting. Systems with double-sided drives, hard disks, and multi-user (MP/M).

Z + 100 64K RAM, Computer, $2495.. **$2099**
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"Z" system features new distributed processing multi-user concept with one Z-80 per user, with Z-80 for MP/M (Master Satellite concept).

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26 megabytes of formatted storage
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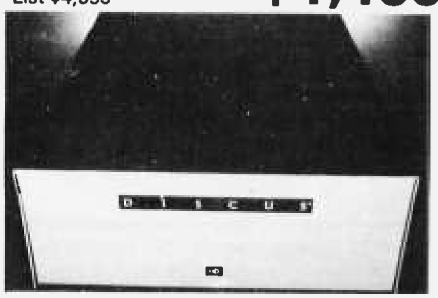

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All Morrow systems now include CP/M® 2.2

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In Stock — First Time in 2 Years!

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North Star Double Density Controller Board (see above) and a quad density MPI-52 (features superior disk handling and door mechanism.

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ɔper and lower case, 15 baud rates: 75 to ı,000 baud, dual intensity, 24 x 80 character splay, 12 x 10 resolution. Numeric pad. Pro-ammable reversible video, auxiliary port, lf-test mode, protect mode, block mode, ɔbing, addressable cursor. Microprocessor ntrolled, programmable underline, line and aracter insert/delete. "C" version features ɔewriter-style keyboard. List $950

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oftware compatible with a Soroc IQ-120, azeltine 1500, ADM-3A or DEC VT-52. Fea-res block mode transmission and printer port; " anti-glare screen; 18-key numeric keypad; ll cursor control. List $895

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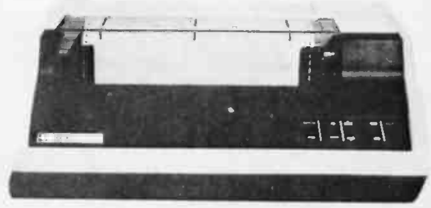

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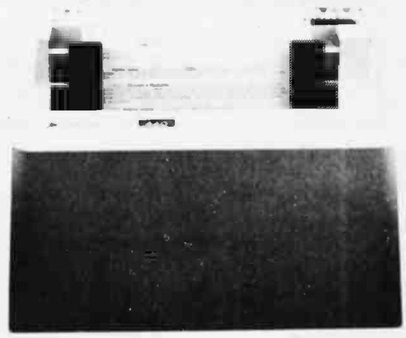

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ONLY $2619

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32K, DD, List $1999	1684	32K, QD, List $2995	2539
32K, QD, List $2199	1869	**HORIZON 2, 32K, DD**	$2619
HORIZON 2, 16K, DD	$1824	32K, QD, List $3595	3049
32K, DD, List $2399	2034	48K, DD, List $3590	3039
32K, QD, List $2779	2359	48K, QD, List $4090	3469
		64K, DD, List $3830	3239
		64K, QD, List $4330	3669

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18 megabytes, plugs into parallel port of North Star Horizon. Utilizes tried-and-proven 14" Century Data Marksman. List $4999. **OUR PRICE $4199**

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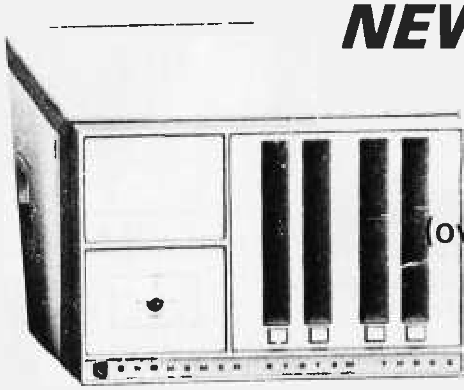

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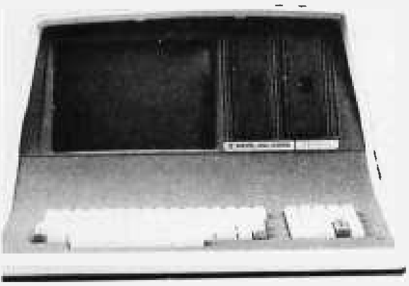

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KIDATA Microline 80, List $949 649
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Complete w/microprocessor controller and power supply. Factory built. User installs solenoid assembly or it can be done at Escon factory at nominal cost.

Parallel (TRS-80, Sorcerer, etc.), $575 $514
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32K, 4 MHz, List $699 .... $629
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8K Static 2 MHz, A&T, List $165 ...... $149
8K Static 4 MHz, A&T, List $195 ...... $176
16K Static 2 MHz, A&T, List $475 ..... $427
16K Static 4 MHz, A&T, List $495 ..... $445
64K Dynamic, List $995 .... $895
CALIFORNIA COMPUTER
16K Static, A&T, List $349.95 .... $259

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Disk Jockey 2D, A&T, List $479 ...... $429
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Versafloppy II, DD Kit, List $350 ...... $297 †
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CONDUCTOR, double density A&T ... $269
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MICROMATION Doubler, DD, A&T ... $399
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FOR SALE OR TRADE: PET monitor with schematic for monitor and interface to Commodore PET computer. Re*quires* horizontal and vertical drive and composite video, all are TTL levels. Has built-in power supply. Trade for composite video only monitor or sell for $70. Works great. Lynn Sim, 113B Tyndall Ave, Colorado Springs CO 80916, (303) 574-5810.

FOR SALE: Heathkit H8 computer, H9 video terminal, 20 K static memory, H8-5 serial I/O and cassette interface, Benton Harbor Extended BASIC software, and all manuals. Assembled, tested, and running. Original cost $1370, best offer over $850. Louis F Latilla, 61 Turf Rd, Staten Island NY 10314.

FOR SALE: Two S-100 16 K static-memory boards. Both use TMS 4044-25 chips. These are fast boards and have logged over 1000 hours on a 4 MHz Z80 system with zero faults. Will sell either board alone for $225, or both for $400. Shipping paid within continental USA. Call after 5 CT weekdays. Richard Kruse, (316) 744-1548.

FORTRAN: I want to do FORTRAN on an Apple II Plus. Who could help? Oen Sek Hong, 13939 Carnell St, Whittier CA 90605.

HELP: Need back issue magazines desperately. These include BYTE, *Creative Computing*, *Personal Computing*, *Recreational Computing*, etc. Paying up to $10 each. John J Liska, POB 98, Brandywine MD 20613.

FOR SALE: IMSAI 8080 with 4 K board; $700, Processor Tech VDMI; $100, Godbout 8 K board; $100, Morrow Speakeasy board with ATE; $120, IMSAI MIO board; $150, TV monitor; $125. I will pack; you pay the freight. Dwight Hebert, 2053 Willowick St, Lake Charles LA 70605, (318) 436-7563.

FOR SALE: Brand-new TRS-80 16 K/Level II. Has not been taken out of original carton. $700 plus shipping. Fariborz Hamzel, 26911 Fond du Lac Rd, Palos Verdes CA 90274.

FOR SALE: Model 15 Teletype with built-in loop supply and RS-232 interface; $50 local pickup. SwTPC CT-1024 terminal in metal cabinet with built-in keyboard and cassette interface. Modified for 64 characters, scrolling, and two pages of display; $175. SwTPC 4 K programmable-memory boards; $40 each or 3/$105. 2102 memory chips; 8/$3.00. Joe Dubner, 865 S Haskett St, Mountain Home ID 83647, (208) 587-9383.

FOR SALE: Datapoint 3300P thermal printer, 80-column, RS-232 serial input at 300 bps. Uses TI 745 paper. Case is 15 by 14 by 5 and color matches Apple. Quiet, reliable, and attractive printer. 30-day guarantee. $500 freight collect, $550 with Apple serial interface. Also, have some S-100 equipment for sale. Dave Valliere, 207 Edgewood Dr, Wilmington DE 19809, (302) 764-7210.

FOR SALE: Xitan Alpha II computer with complete TDL cassette software (Z80 Macroassembler, Editor, and 12 K BASIC). Hardware includes Z80 processor board, 16 K programmable memory, and System Monitor Board II (SMB). SMB board contains two serial and one parallel ports. Monitor software in read-only memory. Asking $1200 or best reasonable offer, cost $1700 new. John E Parsons, 3118-A Avent Ferry Rd, Raleigh NC 27606, (919) 851-0411.

FOR SALE: Altair dual-disk drives with controller and eprom boot boards. Drives just back from factory overhaul. All for $1500. Original cost over $3000. Dick Whipple, 305 Clemson Dr, Tyler TX 75703, (214) 561-1648.

FOR SALE: Printer-terminal: GTE Novar 5560, IBM 72 Selectric, and tape drive. TI Silent 700 printer and H9 video terminal. In excellent condition with documentation. Best offer. R A Ackerman, 2 Hillside St, Red Bank NJ 07701, (201) 291-0680, 741-0923.

FOR SALE: One Wameco EPM-2, 2708/2716, eprom S-100 card. Assembled but never used. $45 or best offer. D Snyder, c/o Buell Div Envirotech, 200 N 7th St, Lebanon PA 17042, (717) 272-2001 ext 527 days, (412) 287-1625 evenings.

FOR SALE OR TRADE: SwTPC 6800 computer with 12 K memory, CT-64 terminal, and AC-30 cassette interface. Sold separately or as a unit to first reasonable offer. Will consider trade for Apple hardware, especially Disk II without controller, printer, etc. Art Boice, 14 Beech St, Norwich NY 13815, (607) 334-5746.

FOR SALE: TI 99/4 computer, 16 K programmable memory, 26 K read-only memory, 30 K add-on read-only memory (preprogrammed) available. Five months old. Comes with RS-232 interface and modem (300 bps). Interface and modem are one month old, hardly used. Also, comes with GE tape recorder and dual recorder interface. Originally $2000, now $1500. Carl Hewitt, 958 Woodthrush Ct, San Jose CA 95120, (408) 268-9761.

FOR SALE: Two Hazeltine 1500 video terminals; $825 apiece. Dust covers included with both, maintenance manual available. Both terminals one-year-old. Will ship UPS for certified check. T Stowe or J Boniakowski, POB 1126, Neptune NJ 07753, (201) 295-9105, (201) 922-3460.

FOR SALE: Amphenol 50 pin connectors, male and female with one metal hood per pair. All contacts are gold-plated. $15 per pair with hood. Also, some 86 pin industrial wire-wrap edge connectors, gold-plated, $5 each. Marc Samson, 4355 Royal Ave, Montreal Quebec, H4A 2M7 Canada.

FOR TRADE: Gas-panel display and power supply by Digivue. 512-by-512 dots, for 51 lines of 85 characters each. Simple to interface and control. Perfect for graphics. Buffered; no regeneration required. Uses X/Y addressing. New cost $7000. Interested in Apple, TRS-80, and programs/information on ELF II (1802). E W Kilby, 1904 Lewis St, Tarboro NC 27886, (919) 823-3775.

FOR SALE: Radio Shack Level II, 32 K expansion interface, two disk drives. Excellent condition. $1800. Will sell separately. Robert Webster, 3221 Riverside Dr #147, Tulsa OK 74105, (918) 742-2538.

WANTED: TRS-80, KIM. Complete unit. Give full details and your lowest price for the unit. John Waskowitz, 35-30 73rd St, Flushing NY 11372.

FOR SALE: TI-59 programmable calculator and some software. Must sell. Software includes accurate stopwatch program and *Master Mind* game. Mitch Wyle c/o Taffy's Inc, 701 Beta Dr, Cleveland OH 44143, (216) 461-3360.

FOR SALE: 6800 system (MSI) with 32 K programmable memory, two Siemens SSSD floppy-disk drives (300 K bytes each), Centronics 306 impact printer, and Beehive B-100 terminal. Software Dynamics BASIC compiler and MSI BASIC interpreter included. System can be upgraded to 6809 with FLEX if desired. All offers considered; best offer takes. Will consider selling computer and disk drives separately. Gary Patrick, 4110 Clark #1, Kansas City MO 64111, (816) 753-2293.

FOR SALE: SOL-20, 32 K static programmable memory (Dynabyte), and North Star disk. Excellent condition. Sacrifice for $2250. Yannick Benitah, 2626 Stanford Ct, Indianapolis IN 46268, (317) 299-5202.

FOR SALE: ELF II microcomputer, 4 K static programmable memory, Giant Board (tape interface, Monitor/Editor, RS-232C/TTY interface, 8-bit parallel I/O), ASCII keyboard, and Tiny BASIC. All units are assembled. Worth over $300 in kit form. Only $250. Power supply for the unit; $40. Extra ASCII keyboard can be purchased separately for $55. First reasonable offer with a money order takes it postpaid. Amit Solomon, 7 Yair Stern St, Herzlia, Israel 46425, (011) 972-52-88127.

WANTED: Persons interested in cooperative life in Washington DC area directed towards designing, programming, and construction of artificial intelligence beings. AIB, 6504 Democracy Blvd, Bethesda MD 20034.

FOR SALE: TRS-80 Scripsit Disk Word Processor. Brand new and unused. Complete with program disks, instructional cassettes, manual, binder, etc. The regular price for this word-processing program is $99.95, but I will sell mine for $50, including first class postage. W L Pierce, 703 23rd St S, Arlington VA 22202.

FOR SALE: Heath H-11 16-bit computer with 8 K bytes of programmable memory and parallel interface card. Fully assembled. Users manual included. $2300 value; will sell for $1600. Craig Altenburg, 328 Taldan Ave, Virginia Beach VA 23462, (804) 499-6254 evenings.

FOR SALE: BYTE issue #1 thru May 1977. Best offer takes the lot. Philip F Curtiss, 2146 Lost Tree Way, Bloomfield Hills MI 48013.

FOR SALE: Heath Zenith H-89 microcomputer. Brand new, fully assembled and tested, floppy disk, cassette-tape interface, 16 K programmable memory, software, and full documentation. List over $2500; sell for $1700. Robert E Martin, 2505 Cherrywood Ln, Titusville FL 32780, (305) 268-1164.

FOR SALE: Texas Instruments TI-59 programmable calculator and PC-100 printer with four library modules, 80 magnetic cards, PPX bulletins, PPX catalog, all documentation, and many programs. $525 value for $395. H D Moxness, 14 McGregor Ave, Mt Arlington NJ 07856, (201) 663-2402.

FOR SALE: Tutorial on Pattern Recognition ideas that will make your computer smarter (and which might make its entrepreneurial user wealthier). Send $0.45 in stamps. G Butler, 475 Selby Ln, Atherton CA 94025.

FOR SALE: S-100: Wameco MEM-1A 8 K-by-8 static 450 ns programmable memory, $120; SSM I/O-4 2 parallel + 2 serial, $120. All circuits socketed, full documentation. Surplus keyboard, keypunch style, metal case, one 5-by-7 display, thumbwheels, counter, no documentation, $25. Douglas Zimmerman, 2824 St Paul St, Baltimore MD 21218, (301) 889-1698.

FOR SALE: A copy of the first issue of BYTE. In mint condition. Max Guze, 1201 Mill St, Montreal Quebec, H3K 2B2 Canada.

FOR SALE: Nearly new Gimix computer, excellent condition. 6800 processor card, 16 K static memory card (Gimix). $800. Also, Smoke Signal Broadcasting disk-controller card. $250. Paul Lamar, 123 S Juanita St, Redondo Beach CA 90277, (213) 374-1673 work, (213) 316-8351 home.

FOR SALE: Exidy Sorcerer with 32 K programmable memory; $895. S-100 expansion unit; $250. Both for $1100. Larry Shelton, 2470 Hummingbird Rd, Dalzell SC 29040, (803) 499-2763.

FOR SALE: North Star Horizon 48 K with two double-density floppies. Built from kit and working perfectly. Includes extra blank diskettes, full assembly manuals, BASIC software and documentation, and Z80 assembler programming manuals. $2000 firm. John Perez, 1946 Winterport Cluster, Reston VA 22091, (703) 620-5961 evenings.

FOR TRADE: Drake 2-A receiver and Q multiplier plus Heath DX 60-B and V.F.O. for best AIM-65 offered. Also, exchanging programs, etc for OSI Challenger. Henry Etchason, Box 147, Sage AR 72573.

FOR SALE: 16 K Apple II like brand new. In original carton. Super Mod with extra box. New recorder with counter. Four 6502 books by Zaks and MOS. ADC/DAC and RS-232 interface. The new *Apple II Reference Manual*. Many materials, magazines, and notes (old and new BYTEs). MicroChess 2.0. Big software library. My cost over $1450 and twelve months. Asking $1100. Lee Gillie, 1804 Elk #140, Rock Springs WY 82901, (307) 382-5998 after 5 PM MST.

WANTED: Graduate student on small budget would like quotes on used Houston Instruments HIPLOT DMP-2 and/or Apple graphics pad. Arthur B Busbey, 1025 E 57, Dept of Anatomy, University of Chicago, Chicago IL 60637, (312) 955-5934.

BOMB

BYTE's Ongoing Monitor Box

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User's Column Towers Over Circuit Cellar in July

Jerry Pournelle's first installment of The User's Column, entitled "Omikron TRS-80 Boards, NEWDOS+, and Sundry Other Matters" (page 198), produced a favorable response from readers of the July BYTE who voted in the BOMB tally. Dr Pournelle won the first-place prize of $100.00.

Steve Ciarcia, for his July Ciarcia's Circuit Cellar article, "Handheld Remote Control for Your Computerized Home," received second place in the voting. Steve was awarded $50.00.

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B ☐ Our custom forms have a guarantee that speaks for itself. Our time on forms range from two to five weeks for custom work and before we start a job we now give a guaranteed shipping date and price, depending on art work, from two to five weeks and for every day we're late we give you a 10% discount. To get a quote just mail the detached portion of this ad with sample of form or layout and we will call you the day we get the information with a price and guaranteed day of shipment.

C ☐ The swingline table top decollator is a portable unit which separates both carbon and carbonless continuous computer forms into stacks. The separated carbon is easily and neatly removed from carbon pick-up spool. Form size is up to 15" wide. Wt. is 10 to 110 lb. bond paper, and the speed is variable from 75 to 200 feet per minute and takes only 120 volts AC 60 hertz to operate.

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D ☐ The Datatech Intimus 007 shredder works for Scotland Yard, for government authorities, for important corporations, banks and embassies. The cutting capacity is 12 to 14 sheets at one pass. Cross cut is 1/35 x 3/8. It has a 2 H.P. motor and runs off of 220/380 V 3 phase.

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E ☐ The Intimus 306 is designed for trouble free operation and has a switch for forward and reverse rotation. It has 2 motors with terminal overload. Housing consists of coated steel, mounted on rubber cushions for noiseless shredding. The 306 can sit on a table or a stand. Cutting width is ⅛" or ¼" and has two 150 watt 110 V 60 cycle, 1 phase motors.

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