Spectral Moment Estimators: A New Approach to Tone Detection

By J. N. DENENBERG

Classical tone detectors use narrow bandpass filters to isolate tones. A comparison of a filter's output power against the total input signal power determines whether or not a particular tone is present. This paper considers an alternate method for tone detection. It is based on estimating the first three moments of the signal's band-limited power spectrum. These three moments (zeroth, first, and second) measure the power, power mean frequency, and RMS power bandwidth, respectively, of the signal. If these three moments are available, it is easy to deduce whether or not a tone is present. Since the estimators have a simple digital implementation, this approach should have economic advantages in many applications.

I. INTRODUCTION

The use of tones is proliferating with the growth of the direct-distance-dialing (DDD) network. Tones are used for multifrequency signaling, *Touch-Tone®* signaling, etc.; for milliwatt tone testing, testing in carrier transmission maintenance,[1] etc.; and as audible ring indicators, reorder indicators, etc.

The DDD network is now evolving toward an integrated system of digital transmission and digital switching. Continued use of analog tone detectors in this digital environment is impractical because of the expense of interfacing analog and digital systems. Classical tone detectors do not lend themselves to efficient digital implementation. Therefore, new approaches to tone detection are necessary.

Several methods are currently under investigation including classical digital filters,[2] the discrete Fourier transform,[3,4] and the use of counting techniques.[5] This paper details another approach to tone detection which is amenable to digital implementation: spectral moment estimation.

II. TONE DETECTION

2.1 Classical tone detectors

The classical approach to tone detection uses a narrow bandpass filter, centered at the expected tone frequency, to isolate the tone. A comparison of the power passed by this filter against the power that is input to the filter (and some absolute level requirements) determines the presence or absence of the tone.

This classical decision algorithm is based on the fact that a simple tone has a narrow bandwidth. A tone can, therefore, readily pass through a narrow filter with little loss in power. Several assumptions are implicit. First, a tone's spectrum is narrow only if the tone is present for a long time. If the detection must be made quickly, the filter's bandwidth must be increased to pass all the tone's power. The second assumption concerns the tone's spectral purity. Rapid variations in frequency and amplitude will also effectively widen the bandwidth.

The decision algorithm can be restated in terms of three signal parameters: power, mean frequency, and bandwidth. Thresholds are set by the filter characteristic for the signal's mean frequency and bandwidth (these thresholds are interrelated). Additional limits are placed on signal power. All these criteria must be met if the signal is to be recognized as a tone.

2.2 Spectral moments as tone indicators

A heuristic argument that is similar to that described above can be used to derive an alternate approach to tone detection. Devices can be built to measure the signal's first three spectral moments:* power (P), power mean frequency (f_a), and mean square bandwidth (b^2). These spectral moments are defined in terms of the signal's power spectrum, $S(f)$, as

$$P = \int_f S(f)\,df,$$

$$f_a = \frac{1}{P} \int_f f S(f)\,df,$$

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* Practical schemes for measuring spectral moments exist. One is described in later sections of this paper.

and

$$b^2 = \frac{1}{P} \int_f (f - f_a)^2 S(f) df,$$

where the region of integration is limited to the range of interest.

Then, for any given tone, thresholds can be set: the power must lie within a required range, the mean frequency must be within tolerances of the expected frequency, and the bandwidth must be less than a specified amount. If these requirements are all satisfied, then the expected tone is declared to be present.

Detection of an unknown tone within a given range of frequencies is also possible. Whenever a tone is present, the bandwidth indication alone can detect it. The other moments can then be used as measurement tools. This demonstrates the power of the spectral moment estimator algorithm.

III. SPECTRAL MOMENT ESTIMATION

3.1 The classical approach

In the past, spectral moments have been estimated by first estimating the spectrum $S(f)$ itself and then substituting this estimate into the definitions of the desired parameters. This classical approach is well documented in the literature.[6]

There are two approaches to the estimation of $S(f)$ from a time-limited segment of the input signal. In one method, it is assumed that the signal is periodic outside the known interval, while in the other, the signal is assumed zero outside that interval. An assumption of periodicity leads to a complex exponential Fourier series that is equal to the input over the known interval. This spectral estimate is discrete in frequency. It consists of weighted impulses at each frequency; the weighting factor for an impulse is the magnitude squared of the corresponding coefficient in the series. Each integral defining the spectral moments becomes a sum.

Either spectral estimate may be used in practice. For long measurement intervals (large T), they give identical results. The remainder of this paper is based on the continuous spectral estimate that assumes zero input outside the measurement interval. This choice does not affect the final form of the digital estimators.

3.2 Direct estimation

3.2.1 Motivation

The classical methods for estimating spectral moments require a spectrum analyzer. This expensive apparatus can take various forms including a filter bank, a Fast Fourier Transform (FFT) processor, etc.

However, since many applications require real-time spectrum analysis, the classical methods are often impractical.

Complete information about spectral shape is not required in tone detection. So why take the expensive step of calculating this detailed information? A system that calculates the desired parameters directly from the input data should be more efficient and, therefore, less costly.

Direct spectral parameter estimators exist in the literature. They have been used in applications including communication channel measurement,[7] radar meteorology,[8-10] and frequency-modulation detection.[11]

3.2.2 Signal representation

The received signal $s(t)$ described in Section II is a narrow-band signal. It can be represented by its complex envelope,

$$x(t) = \alpha(t) + j\beta(t), \tag{1}$$

as

$$s(t) = \alpha(t) \cos (2\pi f_0 t) - \beta(t) \sin (2\pi f_0 t), \tag{2}$$

where f_0, the reference frequency, lies near the center of the signal's spectrum. This representation is also well documented in the literature.[12]

Since it is easy* to determine $\alpha(t)$ and $\beta(t)$, the signal's quadrature components, from $s(t)$ and f_0 is determined at the receiver, the signal's spectral moments can be determined from its complex envelope, $x(t)$.

3.2.3 Estimation algorithms

If an estimate, $\hat{S}(f)$, of the signal's power spectrum is based on $x(t)$, the three spectral moment estimates are, classically,

$$\hat{P} = \int_f \hat{S}(f) df, \tag{3}$$

$$\hat{f}_a = \frac{1}{\hat{P}} \int_f f \hat{S}(f) df^\dagger \tag{4}$$

and

$$\hat{b}^2 = \frac{1}{\hat{P}} \int_f [f - \hat{f}_a]^2 \hat{S}(f) df, \tag{5}$$

where the integrals are only computed over frequencies of interest.

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* The method of extracting the signal's quadrature components is discussed in Section IV.

† $\hat{f}_a$ is shifted from f_a by the known quantity f_0 since $\hat{S}(f)$ is an estimate of the power spectral density of $x(t)$ instead of $s(t)$.

Earlier work[13] has shown that direct calculation of these three quantities from $x(t)$ is possible. The algorithms are

$$\hat{P} = \frac{1}{T} \int_0^T [\alpha^2(t) + \beta^2(t)] dt, \tag{6}$$

$$\hat{f}_a = \frac{1}{2\pi T \hat{P}} \int_0^T [\alpha(t)\dot{\beta}(t) - \beta(t)\dot{\alpha}(t)] dt, \tag{7}$$

and

$$\hat{b}^2 = \frac{1}{4\pi^2 T \hat{P}} \int_0^T \{[\dot{\alpha}(t)]^2 + [\dot{\beta}(t)]^2\} dt - [\hat{f}_a]^2, \tag{8}$$

where the dot over a quantity indicates the derivative with respect to time.

3.3 Estimate error analysis

Since the direct estimators were derived from the classical estimators, their performance will be equal. Therefore, an analysis of the statistical behavior of the classical estimators can be applied to the direct estimators.

Miller and Rochwarger[14] have done such an analysis. They assume that the error in each measurement is small enough so that a power series expansion converges rapidly. Their results, however, are difficult to apply in practice and do not address the time-limited nature of the measurement. A similar analysis, which takes into account the time-limited nature of the measurement, was done by the author.[18] It also assumes convergence of the power series. In that analysis, the input is a complex sample function from a gaussian random process with total power P, a power spectral density $S(f)$, power mean frequency f_a, and mean square bandwidth b^2. The results are given below.

Estimator bias and variance are of interest for each of the three spectral moments. For the power estimator, the results agree with those found in textbooks.[15] Its expected value is

$$E[\hat{P}] = P. \tag{9}$$

It is therefore unbiased and yields, on the average, the total received power. The power estimator's variance is given by

$$\text{var}[\hat{P}] = \frac{1}{T} \int_f S^2(f) df. \tag{10}$$

The expected value of the power mean frequency estimator is

$$E[\hat{f}_a] = (f_a - f_o) - \frac{1}{P^2 T} \int_f f S^2(f + f_a) df. \tag{11}$$

It is therefore biased in the general case. An unbiased estimate occurs when the power spectral density is symmetrical about its mean. A similar equation gives the variance of $\hat{f}_a$:

$$\operatorname{var}\left[\hat{f}_a\right] = \frac{1}{P^2T} \int_f f^2 S^2(f + f_a)df. \tag{12}$$

It is clear from

$$E[\hat{b}^2] = b^2 + \frac{1}{P^2T} \int_f (b^2 - 2f^2)S^2(f + f_a)df \tag{13}$$

that $\hat{b}^2$ is also biased. Its variance is given by

$$\operatorname{var}[\hat{b}^2] = \frac{1}{P^2T} \int_f (f^2 - b^2)^2 S^2(f + f_a)df. \tag{14}$$

Note that all the biases and variances are independent of the actual mean frequency. They are functions of the measurement interval, spectral width (b^2), and shape. All of them decrease to zero as the measurement interval increases or as b^2 decreases.

3.4 Computer simulation

The equations in Section 3.3 provide simple theoretical expressions for the bias and variance of the power mean frequency and mean square bandwidth estimators. These expressions are valid for reasonably long time measurements. Since the equations for f_a and b^2 are new, a computer simulation was conducted to substantiate the validity of these expressions. A sequence of independent, complex, gaussian processes was generated. These complex, independent time samples were then transformed by an FFT to yield a flat, or white noise, spectrum on the average. The flat spectrum was then shaped by a gaussian frequency response function. This yielded a set of random spectral coefficients with a gaussian shape in the mean. These frequency coefficients were then used to generate independent estimates of f_{ag} and b_g^2 from each member of the sequence, where f_{ag} and b_g^2 are the mean frequency and variance of the chosen gaussian shape.

Fifty pairs of estimates, $\hat{f}_{ag}$ and $\hat{b}_g^2$, were obtained from 50 independent spectral estimates. Each spectral estimate was derived from 512 complex time samples, thus yielding 512 line resolution. The results of the simulation are shown in Table I where the bar over the quantities of interest indicates the average over the 50 estimates. The mean square error of the quantity of interest, $\epsilon(\ )$, was also obtained by an average over the 50 estimates, i.e., $\epsilon(\hat{f}_a)$ is given by

$$\epsilon(\hat{f}_a) = \overline{(\hat{f}_a - f_a)^2}. \tag{15}$$

Table I — Computer simulation

	$f_{ag} = 0$ $b_g^2 = 400$	$f_{ag} = 128$ $b_g^2 = 400$	Theoretical Values
$\overline{f_{ag}}$ $\epsilon(f_{ag})$	−0.07 4.05	127.8 2.56	0, 128 2.8
$\overline{b_g^2}$ $\epsilon(b_g)$	414 1.51	395.4 1.48	400, 400 1.06, 1.06*

* This row is adjusted to be in Hz² using

$$\epsilon(b_g) = \frac{\epsilon(\hat{b}_g^2)}{4b_g^2}.$$

Specifically, the gaussian spectral shape is given by

$$S_g(f + f_a) = \frac{1}{\sqrt{2\pi}b_g} \exp\left[-\frac{f^2}{2b_g^2} \right]; \quad -\infty < f < +\infty. \quad (16)$$

Evaluating the equations in Section 3.3 for this example yields

$$E[\hat{f}_a] = f_a, \quad (17)$$

$$\text{var}\,[\hat{f}_a] = \frac{b_g}{4\sqrt{\pi}\,T}, \quad (18)$$

$$E[\hat{b}^2] = b_g^2, \quad (19)$$

$$\text{var}\,[\hat{b}^2] = \frac{3b_g^3}{8\sqrt{\pi}\,T}. \quad (20)$$

Note that both estimates are unbiased in this example.

Two cases were simulated. The first had a mean frequency of zero and an RMS bandwidth of 20 Hz. The second case also had a bandwidth of 20 Hz; however, it was centered at 128 Hz. Both estimates were accurate on the average. Their mean square error was predicted with 50 percent accuracy by the equations in Section 3.3.

IV. A DIGITAL TONE DETECTOR

4.1 The application

As noted in Section I, the evolution of the voiceband DDD network toward an integrated system of digital switching and digital transmission makes the use of digital service circuits attractive. In this environment, several assumptions can be made about the form of the input signal. These assumptions are: the sampling rate of the input signal is that of the T-carrier systems (8 kHz), the approximate frequency of the tone is known, and (although the digital encoding is logarithmically compressed in practice) the code is linear. The second

assumption allows the tone detector to search for the tone in a narrow band of frequencies and makes the techniques of Sections II and III applicable.

4.2 Quadrature detection

4.2.1 Analysis

In Section III, a narrow-band signal was expressed in terms of its complex envelope as

$$s(t) = \alpha(t) \cos (2\pi f_0 t) - \beta(t) \sin (2\pi f_0 t). \tag{2}$$

Multiplying $s(t)$ by a locally generated cosine wave with a peak amplitude of 2 and a frequency of f_0 yields

$$2 \cos (2\pi f_0 t) \cdot s(t) = \alpha(t)[1 + \cos (4\pi f_0 t)] - \beta(t) \sin 4\pi f_0 t. \tag{21}$$

If this result is passed through a low-pass filter to remove the components near $2f_0$, $\alpha(t)$ is the output. Similarly, if the input is multiplied by another locally generated signal, 90 degrees out of phase from the first reference,

$$-2 \sin (2\pi f_0 t) \cdot s(t) = -\alpha(t) \sin (4\pi f_0 t) + \beta(t)[1 - \cos (2\pi f_0 t)], \tag{22}$$

the result can be filtered to produce $\beta(t)$.

Figure 1 shows a block diagram of the quadrature detection process. The low-pass filters, in addition to eliminating the undesired terms due to mixing, perform an effective bandpass filtering operation on the input. If f_m is the highest frequency passed by the filters, only
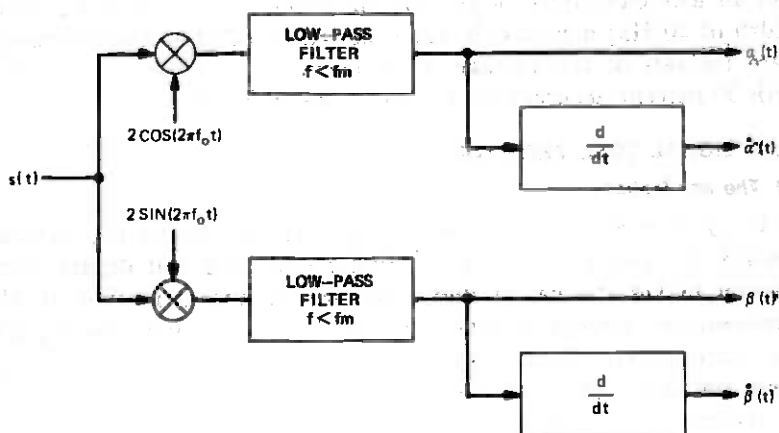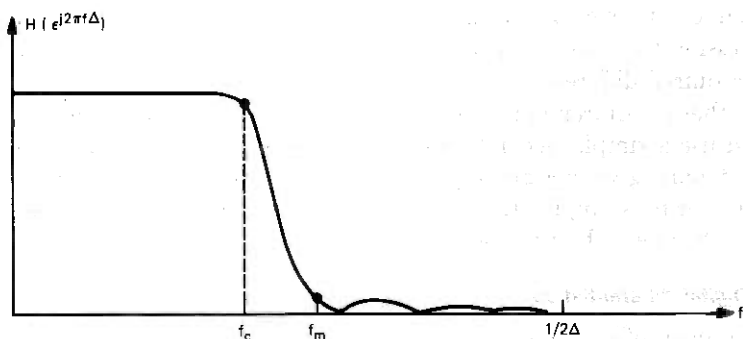

Fig. 1—Quadrature detection.

Fig. 2—Typical low-pass filter response.

frequencies in the range

$$f_0 - f_m \leqq f \leqq f_0 + f_m \tag{23}$$

have any effect on the resulting measurements. Differentiation required for the remaining calculations is also shown in Fig. 1. It is not really part of the quadrature detection process and is discussed in Section 4.3.

4.2.2 Low-pass filter requirements

Two parameters of the filters used in quadrature detection are important. They are the cutoff frequency f_c and the maximum frequency f_m. Figure 2 shows a typical low-pass filter frequency characteristic defining its two parameters f_c and f_m.

The parameter f_c sets the frequency limits on the measurement. It should be high enough to allow for any possible allowed frequency offset plus some margin since the tone's bandwidth is spread by the time-limited measurement (on the order of 100 Hz for a 10-ms interval). f_c has an upper limit which is determined by several factors. First, it cannot crowd f_m. This would raise the complexity of the filter and make this approach impractical. It also should not be so high as to allow an unnecessary amount of the background noise to disturb the measurement. An f_c between 200 and 350 Hz will be the usual compromise.

The maximum frequency f_m determines the immunity of the detector to interfering signals. If it is low enough, it also allows the use of resampling which results in considerable savings in the processing after detection. Considerations of immunity usually set an upper limit on f_m of 1 kHz*, while the likelihood of resampling reduces this to 500 Hz. If an f_m of 500 Hz or less is used, the output sample rate can

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* One possible application, translating the output of a *Touch-Tone* phone, requires an f_m of 350 Hz for the lower group tone detector. f_c for this detector is at least 175 Hz.

be reduced to once every millisecond. This alone reduces the remaining processing by a factor of 8. It also allows a simple implementation of the required differentiators.

If these requirements are specified, some noncritical applications could use a simple, second-order, digital, low-pass filter. But since this would only give marginal performance, a fourth-order filter is suggested for most applications. Note that two of these filters are required for each tone to be processed.

4.3 Digital differentiation

An ideal differentiator for this application has a frequency response which is proportional to frequency for all frequencies below f_c and rolls off rapidly above f_c. It also has a phase shift of 90 degrees for all frequencies below f_c.

The simplest form for a digital differentiator is the difference between two input samples. This approximates the input's derivative at a time midway between the sample times. More complex differentiator structures are possible; they are usually unnecessary.[16]

In this application, it is necessary to get the derivative at the sample time. Therefore, the differentiator should calculate

$$y_k = x_{k-1} - x_{k+1}, \tag{24}$$

where y_k is the approximate derivative at the time input sample x_k appeared. Note that if only every eighth sample of the input is going to be used in the subsequent processing, the computation of a derivative every millisecond uses two of the other seven samples during that interval.

The accuracy of this approximation can be easily calculated. Taking the z transform of (24), restricting z to the unit circle, and simplifying result in

$$H(\epsilon^{j2\pi f\tau}) = j2 \sin (2\pi f\tau), \tag{25}$$

where τ is the time between samples and f is the frequency input to the differentiator.

In most voiceband tone-detection applications, τ is 125 μs and f is less than 500 Hz.* Therefore, the transfer function can be approximated by the first term of its power series

$$H(\epsilon^{j2\pi f\tau}) \cong j4\pi f\tau. \tag{26}$$

For the numbers stated, this is only a 3-percent error in the worst case. Therefore, the simple differentiator usually suffices.

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* The frequency input to the differentiator is the difference between the signal's frequency and f_o, the reference frequency.

4.4 Calculation of the spectral moment estimates

Quadrature detection, as developed in Section 4.2, yields samples of the input signal's quadrature components $\alpha(t)$ and $\beta(t)$ each millisecond. The differentiators discussed in Section 4.3 give corresponding samples of $\dot{\alpha}(t)$ and $\dot{\beta}(t)$ each millisecond. Calculation of the three estimates from this sequence of four samples each millisecond is straightforward.

The power estimate is given by (6) as:

$$\hat{P} = \frac{1}{T} \int_0^T \left[\alpha^2(t) + \beta^2(t) \right] dt. \tag{6}$$

Since $\alpha(t)$ and $\beta(t)$ are only available as samples each millisecond, the integral reduces to an equivalent summation,

$$\hat{P} = \frac{1}{N} \sum_{k=0}^{N-1} \left[\alpha_k^2 + \beta_k^2 \right], \tag{27}$$

where T, the measurement interval, is given by

$$T = N\tau. \tag{28}$$

Similarly, the estimate of the power times the power mean frequency can be obtained from (7).

$$\widehat{Pf_a} = \frac{1}{2\pi T} \int_0^T \left[\alpha(t)\dot{\beta}(t) - \beta(t)\dot{\alpha}(t) \right] dt. \tag{29}$$

The equivalent sum is

$$\widehat{Pf_a} = \frac{1}{4\pi N\tau} \sum_{k=0}^{N-1} \left[\alpha_k(\beta_{k-1} - \beta_{k+1}) - \beta_k(\alpha_{k-1} - \alpha_{k+1}) \right]. \tag{30}$$

Finally, the estimate giving bandwidth information is derived from (8):

$$\widehat{P(b^2 + f_a^2)} = \frac{1}{4\pi^2 T} \int_0^T \left\{ [\dot{\alpha}(t)]^2 + [\dot{\beta}(t)]^2 \right\} dt. \tag{31}$$

The corresponding equivalent sum is

$$\widehat{P(b^2 + f_a^2)} = \frac{1}{16\pi^2 N\tau^2} \sum_{k=0}^{N-1} \left[(\alpha_{k-1} - \alpha_{k+1})^2 + (\beta_{k-1} - \beta_{k+1})^2 \right]. \tag{32}$$

Algorithms for the three spectral parameters of interest are now available. $\hat{P}$ is given by (27). Dividing (27) into (30) yields

$$\hat{f}_a = \frac{\widehat{Pf_a}}{\hat{P}}. \tag{33}$$

Similarly, $\hat{b}^2$ is obtained using (27), (30), and (32):

$$\hat{b}^2 = \frac{\widehat{P(b^2 + f_a^2)}}{\hat{P}} - (\hat{f}_a)^2. \tag{34}$$

4.5 Tone detection

The system developed in Sections 4.1 through 4.4 gives estimates of the three spectral parameters P, f_a, and b^2 over a time interval of T seconds. Thresholds must now be set, as discussed in Section II, to determine the presence or absence of a valid tone during that interval. Values for these thresholds are dependent on the particular application and, therefore, are not calculated here. It is suggested, however, that they be determined experimentally rather than through the use of the analysis of Section III. This experimental determination can be made either through simulation or by breadboarding the design. It will give a more reliable result because the approximations needed for the statistical analysis are eliminated.

One final point needs discussion. Many applications have requirements on the measurement interval which are near theoretical limits.[17] Meeting these specifications will require tone detection during overlapping time intervals. This increases the storage requirements of the system.

An approximation can be made which eliminates this increase in storage. Recall that a low-pass filter performs the weighted integral given by

$$y(t) = \int_{-\infty}^{t} x(\lambda)h(t - \lambda)d\lambda, \tag{35}$$

where $h(t)$, the filter's impulse response, is controlled by the filter structure. Therefore, a filter can be used to do the averaging necessary for tone detection. Although this approximation can be made as accurate as desired, the filter's complexity increases rapidly. A simple "lossy integrator" suffices for many applications.

V. CONCLUSIONS

Spectral moment estimators have been used to develop a viable alternative structure for a digital tone detector. The resulting digital system is flexible and can adapt to any tone detection application in which a single tone lies somewhere in a fixed bandwidth. It is easily programmable to cover multiple uses. This system has one additional feature that is not present in most other detector structures: the incoming tone frequency need not be known *a priori*.

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A Simple Description of an Error-Correcting Code for High-Density Magnetic Tape

By N. J. A. SLOANE

Hong and Patel have described an efficient error-correcting code for magnetic tape, which has been successfully used on the IBM 6250 bits-per-inch nine-track magnetic tape units. This paper gives a simple description of the code, without using Galois fields.

I. INTRODUCTION

The latest IBM tape units use $\frac{1}{2}$-in., nine-track tape with the very high density of 6250 bits per in. This is made possible, in part, by the use of an efficient error-correcting code, which can correct errors in one or two tracks.

The code was described by Patel and Hong[1] (see also Ref. 2), and is a straightforward extension of earlier IBM codes (see Refs. 3 and 4). The purpose of this paper is to give a simple description of the code and its many nice features, without using Galois fields.

II. ENCODING

A code-word consists of 72 bits arranged on the tape in a 9×8 rectangle, as shown in Fig. 1. The ninth track is simply an overall parity check on the other eight tracks, i.e., it is equal to the modulo 2 sum of the other eight tracks. The left-hand column of each code-word also consists of check bits. Thus 16 out of the 72 bits are checks and 56 are information bits. The rate or efficiency of the code is 56/72 = 0.778. Data are read on and off the tape by vertical columns (Fig. 2). The ith column consists of eight bits (denoted by B_i) together with an overall parity check bit. $B_7, B_6, \cdots, B_1$ are the information columns and are written on the tape in this order. Finally the check column B_0 is written on the tape. B_0 is chosen so that the code-word satisfies the vector equation

$$B_0 + TB_1 + T^2B_2 + \cdots + T^7B_7 = 0, \qquad (1)$$
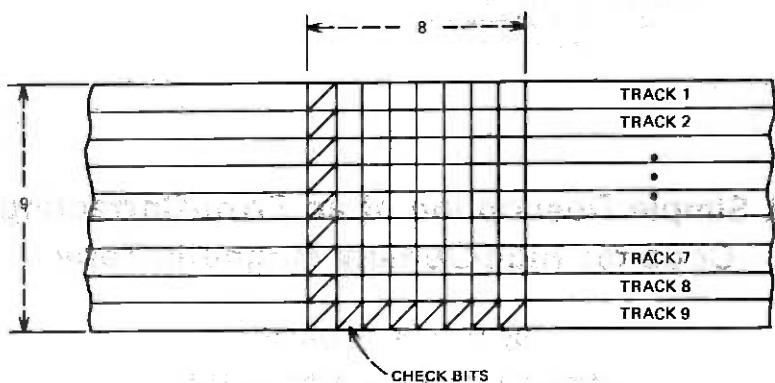
Fig. 1—A code-word is a rectangle of 9×8 bits.

where T is the matrix

$$T = \begin{bmatrix} & & & & & & & 1 \\ 1 & & & & & & & \\ & 1 & & & & & & \\ & & 1 & & & & 1 & \\ & & & 1 & & & 1 & \\ & & & & 1 & & 1 & \\ & & & & & 1 & & \\ & & & & & & 1 & \end{bmatrix},$$

Note the special shape of T: there are 1's only below the main diagonal and in the last column. In fact, T describes the action of the linear feedback shift register shown in Fig. 3. If the contents of the register are

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ \vdots \\ a_7 \end{bmatrix},$$

then one time unit later it contains

$$\begin{bmatrix} a_7 \\ a_0 \\ a_1 \\ a_2 + a_7 \\ a_3 + a_7 \\ a_4 + a_7 \\ a_5 \\ a_6 \end{bmatrix} = T \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_3 \\ a_4 \\ a_5 \\ a_6 \\ a_7 \end{bmatrix}.$$
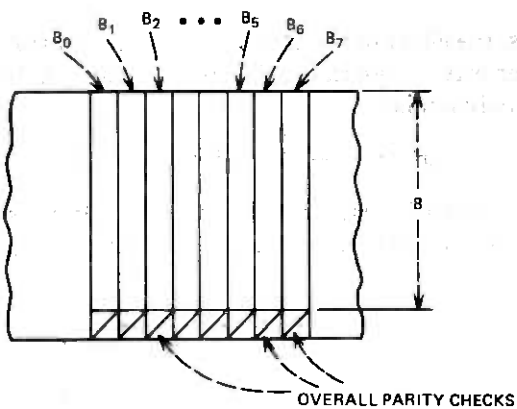
Fig. 2—A code-word divided into eight columns.
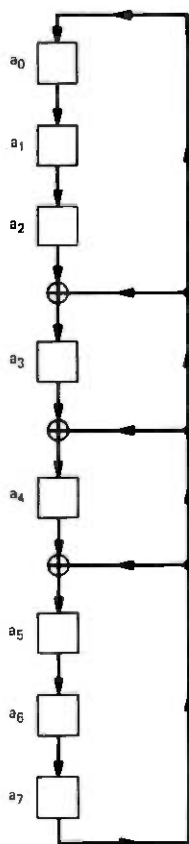
Fig. 3—A shift register which multiplies by T.

In other words, the effect of the shift register is to multiply its contents by T. [Another way of describing T is to say that T is the companion matrix of the polynomial

$$g(x) = x^8 + x^5 + x^4 + x^3 + 1.]$$

Encoding is now easily carried out with this shift register, as shown in Fig. 4. The seven column vectors of information, B_7, B_6, $\cdots$, B_1,
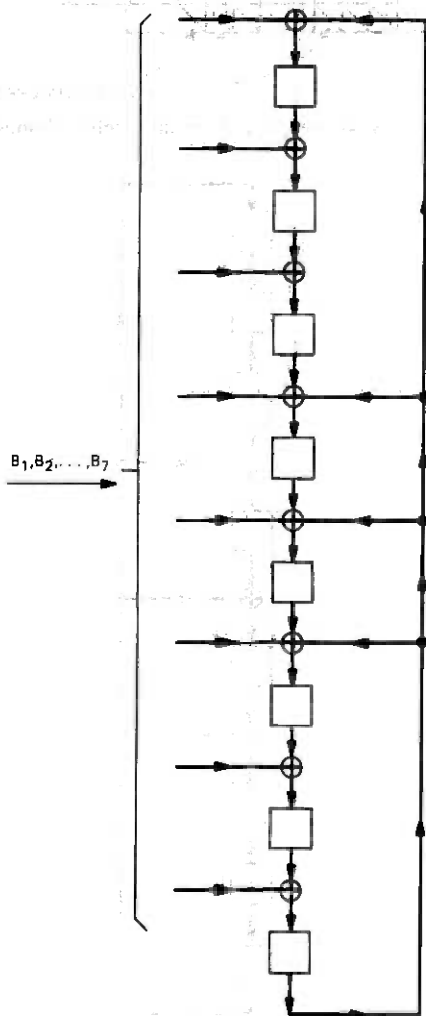
Fig. 4—Encoding circuit.

are fed into the register, which successively contains

$$B_7,$$
$$B_6 + TB_7,$$
$$B_5 + TB_6 + T^2B_7,$$
$$\cdots$$

and finally

$$TB_1 + T^2B_2 + \cdots + T^7B_7,$$

which from eq. (1) is B_0, the check column that we wanted. B_0 is then written directly on the tape (together with the overall parity check in track 9).

III. DECODING

When the code-word is read back from the tape, it may contain errors. Since the bit density in the horizontal direction is much greater than that in the vertical direction, the commonest type of error is a horizontal burst along a track. Often the erroneous tracks can be identified by a loss of signal in the tape-reading head, or by other electronic indications.

To describe the decoding process, some further notation is required. Let $Z_0, Z_1, \cdots, Z_8$ be defined as in Fig. 5. The Z_i's are the horizontal slices of the same code-word we had before. The last row Z_8 is the overall parity check row, defined by

$$Z_8 = Z_0 + \cdots + Z_7$$

or equivalently (all calculations are carried out modulo 2):

$$Z_0 + Z_1 + \cdots + Z_7 + Z_8 = 0. \tag{2}$$
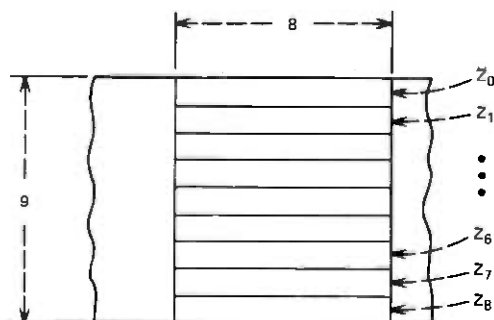
Fig. 5—A code-word divided into nine rows.

Of course the Z_i's and B_j's are related. If we write

$$Z_i = (Z_{i0}, Z_{i1}, \cdots, Z_{i7}), \qquad B_j = \begin{bmatrix} B_{0j} \\ B_{1j} \\ \vdots \\ B_{7j} \end{bmatrix},$$

then

$$Z_{ij} = B_{ij} \tag{3}$$

are both names for the bit in position (i, j), $0 \leq i, j \leq 7$, of the top eight rows of the code word.

The B_j's must satisfy eq. (1). How does this constrain the Z_i's? The answer is a nice surprise: they must satisfy essentially the same equation, namely

$$Z_0' + TZ_1' + T^2Z_2' + \cdots + T^7Z_7' = 0, \tag{4}$$

where the prime denotes transpose. This equation is derived in the appendix.

Now suppose that errors have occurred, and the distorted vectors

$$\hat{Z}_i = Z_i + e_i, \qquad i = 0, \cdots, 8$$

have been read off the tape, where e_i is the eight-bit error vector in the ith horizontal slice (or track). We wish to find the e_i's so that we can recover the original code-word using

$$Z_i = \hat{Z}_i + e_i, \qquad i = 0, \cdots, 8.$$

The decoder begins by computing the *syndromes*

$$S_1 = \hat{Z}_0' + \hat{Z}_1' + \cdots + \hat{Z}_8'$$

and

$$S_2 = \hat{Z}_0' + T\hat{Z}_1' + \cdots + T^7\hat{Z}_7'$$
$$= \hat{B}_0 + T\hat{B}_1 + \cdots + T^7\hat{B}_7.$$

From eqs. (2) and (4) we see that S_1 and S_2 are zero if there are no errors and, in general, give the "symptoms" of the errors. In fact,

$$S_1 = \sum_{i=0}^{8} Z_i' + \sum_{i=0}^{8} e_i'$$
$$= \sum_{i=0}^{8} e_i' \qquad \text{from (2),} \tag{5}$$

and similarly

$$S_2 = \sum_{i=0}^{7} T^i e_i'. \tag{6}$$

S_1 is easily found: it is simply the sum of all the rows. S_2 is obtained by feeding $\hat{B}_7$, $\hat{B}_6$, $\cdots$, $\hat{B}_0$ into the shift register of Fig. 4 as they are read off the tape. After $\hat{B}_0$ has been fed in, by eq. (1) the register contains $\sum_{j=0}^{7} T^j \hat{B}_j = S_2$.

After the decoder has found S_1 and S_2, there are two ways of proceeding.

Mode I. To correct an error in one track.

Suppose the ith track is in error, and e_i is the error vector in the ith track. The decoder knows [from eqs. (5) and (6)]

$$S_1 = e_i'$$

and

$$S_2 = \begin{cases} T^i e_i' & \text{if } 0 \leq i \leq 7 \\ 0 & \text{if } i = 8, \end{cases}$$

since S_2 only involves tracks 0 through 7. Thus S_1 tells us e_i. To find i, we use S_2. If $S_2 = 0$, $i = 8$. Otherwise S_2 is successively multiplied by T^{-1} until e_i' is reached, and i is the number of multiplications required. A circuit which multiplies by T^{-1} is simply obtained by reversing the direction of the arrows in Fig. 3 and is shown in Fig. 6. In Mode I, any error pattern which is confined to one track can be corrected, for a total of $1 + 9(2^8 - 1) = 2296$ error patterns.

Mode II. To correct errors in two tracks, if it is known which tracks are in error.

Suppose it is known (for instance, by a loss of signal in the tape-reading head) that tracks i and j are in error, where i and j are known. Assume $i < j$.

The decoder first finds

$$S_1 = e_i' + e_j'$$

and

$$S_2 = \begin{cases} T^i e_i' + T^j e_j' & \text{if } j \leq 7 \\ T^i e_i' & \text{if } j = 8. \end{cases}$$
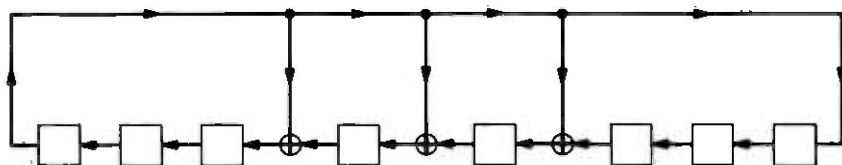
Fig. 6—A shift register which multiplies by T^{-1}.

We allow $e_j = 0$, to include the case where only one track is in error. Solving these equations, we have

$$e_i' = S_1 + e_j'$$

$$e_j' = \begin{cases} (T^i + T^j)^{-1}(T^iS_1 + S_2) & \text{if } j \leq 7 \\ T^{-i}(T^iS_1 + S_2) & \text{if } j = 8 \end{cases}$$

$$= \begin{cases} (I + T^{j-i})^{-1}(S_1 + T^{-i}S_2) & \text{if } j \leq 7 \\ S_1 + T^{-i}S_2 & \text{if } j = 8 \end{cases}$$

$$= M_{i,j}(S_1 + T^{-i}S_2),$$

where

$$M_{i,j} = \begin{cases} (I + T^{j-i})^{-1} & \text{if } j \leq 7 \\ I & \text{if } j = 8 \end{cases}$$

is a matrix which can be calculated in advance (and is written out in Ref. 1). Note that, if $j \leq 7$, $M_{i,j}$ only depends on $j - i$, so only eight different M's are required.

Decoding in Mode II proceeds as follows. First, S_1 and S_2 are found. Then S_2 is multiplied i times by T^{-1}, added to S_1, and the sum is fed into a circuit which multiplies by $M_{i,j}$ to produce e_j'. Then $e_i' = S_1 + e_j'$. Finally the errors are corrected by adding e_i to track i and e_j to track j.

Observe that in this mode the number of error patterns corrected is $2^8 \cdot 2^8 = 2^{16}$ (for there are 2^8 possibilities each for e_i and for e_j). On the other hand, there are *exactly* $2^8 \cdot 2^8 = 2^{16}$ distinct syndromes. Therefore this code is optimal.

IV. REMARKS

(*i*) This description has neglected certain details of how the data are actually written on the tape—see Ref. 1 for further information.

(*ii*) A similar code exists for n-track tape, for any value of n. The code-words contain $n(n - 1)$ bits, arranged in an $n \times (n - 1)$ rectangle. There are $n^2 - 3n + 2$ information bits and $2n - 2$ check bits in each code word, for an efficiency of $(n - 2)/n$. For example, the efficiency drops to 0.6 if $n = 5$. The code is constructed in exactly the same way, the only difference being in the matrix T. For n-track tape, T should be chosen to be the companion matrix of an irreducible polynomial $g(x)$ of degree $n - 1$. The code will still correct $(n - 1)$-bit error patterns in one or two tracks. (There will be several different irreducible polynomials $g(x)$ to choose from. Patel and Hong chose one which was symmetrical about the middle, had the lowest possible exponent, and contained the fewest terms.)

V. SUMMARY

This paper describes the Patel-Hong code for nine-track tape. A code-word contains 72 bits, arranged in a 9×8 rectangle, with 56 information bits and 16 check bits. Encoding and decoding can be done using fairly simple circuitry. There are two modes of decoding. In Mode I, any eight-bit error in any one track can be corrected (even if it is not known which track is in error). In Mode II, eight-bit errors in any two tracks can be corrected, provided it is known which tracks are in error. The generalization of this code to n-track tape is briefly described.

APPENDIX

Proof of Eq. (4)

Define the column vector $s^{(0)} = (1, 0, 0, 0, 0, 0, 0, 0)'$, and let $s^{(i)} = T^i s^{(0)}$. Then the jth column of T^i is $s^{(i+j-1)}$. Equation (1) can be written as

$$[I, T, T^2, \cdots, T^7] \begin{bmatrix} B_0 \\ B_1 \\ \vdots \\ B_7 \end{bmatrix} = 0.$$

Taking the columns of the left-hand matrix in the order 1, 9, 17, $\cdots$, 57; 2, 10, 18, $\cdots$ and remembering eq. (3), we can rewrite the last equation as

$$[I, T, T^2, \cdots, T^7] \begin{bmatrix} Z_0' \\ Z_1' \\ \vdots \\ Z_7' \end{bmatrix} = 0.$$

This is eq. (4).   Q.E.D.

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A 10-W, 6-GHz, GaAs IMPATT Amplifier for Microwave Radio Systems

By I. TATSUGUCHI and J. W. GEWARTOWSKI

An experimental 10-W, three-stage, GaAs IMPATT amplifier has been developed with transmission characteristics suitable for use in 6-GHz long-haul radio-relay systems. The amplifier uses five flat-doping-profile GaAs IMPATT diodes in three cascaded, circulator-coupled stages. The dc input power is 153 W with a nominal 10 W of output power and an overall noise figure of less than 35 dB. The overall amplifier efficiency is 6.5 percent. The major portion of the amplifier is constructed in strip transmission line using suspended alumina substrate in an aluminum housing. Small, integrated, coaxial sections with coaxial transformers connect the diodes to the strip transmission line circuits. The amplifier is cooled by free convection.

I. INTRODUCTION

IMPATT diodes provide a practical means of generating watts of cw microwave power. These devices are now commonly used in transmitter power amplifiers at 6 GHz and higher frequencies. For short-haul radio systems, an output power of 1 to 2 W, which can be obtained using a single diode,[1] is often sufficient. However, for long-haul systems, 10 W is a typical output power requirement, and the traveling-wave tube has been the indispensable selection. This much power can be obtained from multiple-IMPATT-diode circuits, especially when GaAs diodes are used. GaAs diodes have greater efficiency and lower noise than Si diodes, and this latter quality is equally important in meeting long-haul objectives.

This paper describes the circuit configuration used to meet the long-haul transmission objectives with a minimum number of IMPATT diodes, corresponding to highest overall efficiency. The diodes have conventional flat-doping profiles. The higher-efficiency, modified-Read-profile diodes were not available at the onset of this development, so they are not included in this study.[2]

II. MICROWAVE RADIO SYSTEM

The microwave radio system under consideration is a 6-GHz FM system with 1800-message circuit capability. It currently uses a 10-W traveling-wave tube as an rf amplifier in the transmitter. The thermal noise for a typical hop with 1800-message circuit loading should not exceed 15 dBrnc0.* The contribution of the amplifier to the total thermal noise level should be less than 6 dBrnc0. This corresponds to a double-sideband carrier-to-noise ratio, C/N (DSB-FM, 1-Hz BW), of 147 dB. N is defined as the total noise power in two 1-Hz bands, 8.5 MHz on each side of the carrier, whose power is C.

The performance of the amplifier in the system can be evaluated by the use of system thermal noise performance contours. These contours were derived assuming average values for all parameters in a single hop of a typical radio repeater system. Such contours in dBrnc0 as a function of rf output power and C/N of the transmitter amplifier[4] are given in Fig. 1. These curves assume that the amplifier contributes only thermal noise, with essentially no contribution of intermodulation and cross-modulation noise. The horizontal and vertical asymptotes of the curves of Fig. 1 indicate the regions of receiver noise and transmitter noise domination, respectively. When transmitter noise dominates (vertical asymptotes), improving the output power of the amplifier does very little to improve the system performance. Similarly, if the receiver noise is the dominant factor, improving the noise of the transmitter amplifier does not improve the overall performance.

The curves indicate that 15 dBrnc0 can be achieved with an amplifier whose C/N is 147 dB and output power is 40 dBm. It also indicates the power and noise trade-off that can be made and still get the overall performance of 15 dBrnc0.

III. CALCULATED PERFORMANCE

The design goals of the amplifier were a C/N of 147 dB with an output power of 40 dBm. Such a performance cannot be realized with a single-stage device. The power-noise characteristic of a typical GaAs diode is given in Fig. 2 for 32-W dc input power. Maximum power and minimum noise cannot be realized simultaneously. The maximum usable added power of a reliable flat-doping-profile 6-GHz GaAs diode is on the order of 36 dBm with a corresponding noise figure of approximately 51 dB and an efficiency of about 12.5 percent.

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* dBrnc0 is a measure of message circuit noise expressed in decibels relative to a reference level of −90 dBm. It is measured using a C-message weighting network and referred to the 0 transmission level point (Ref. 3).
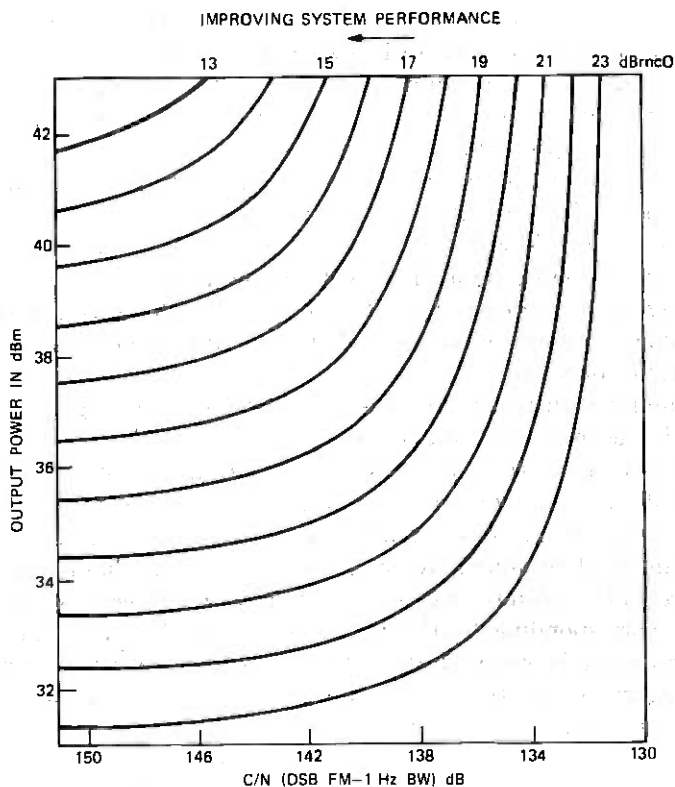
Fig. 1—Lines of constant system thermal-noise performance appropriate for evaluating the output amplifier for a 6-GHz long-haul microwave radio system.
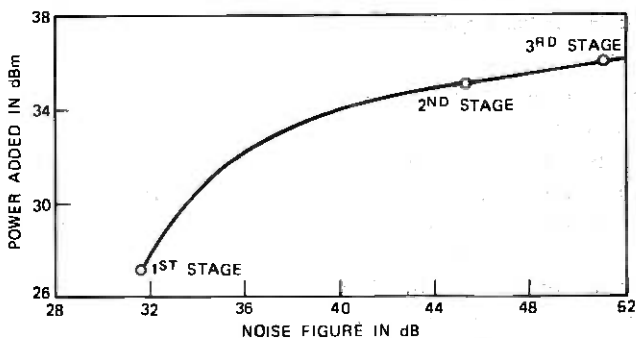
Fig. 2—Power-noise characteristic of a typical 6-GHz GaAs diode with 32 watts dc input showing the operating levels used in the three-stage amplifier.

The nominal breakdown voltage is 83 V, and the nominal zero-bias junction capacitance is 12.5 pF. Using these diodes, a power of 10 W can be realized by cascading two stages of amplification with two diodes in each stage. A suitably low overall noise performance can be obtained by preceding the power stages with a low-noise high-gain stage. A diode with the power-noise characteristic shown in Fig. 2 when operated at 27 dBm output in the first stage will meet the noise objective. To reduce the overall dc power requirement for the amplifier, a smaller area diode with lower doping was used in the first stage and operated at 21 W of dc power. This was a diode with a nominal breakdown voltage of 100 V, and a nominal zero-bias capacitance of 8.5 pF.

Assuming realistic circuit losses (1 dB) between stages and operating the second- and third-stage diodes at the levels shown in Fig. 2, we can calculate the overall system performance of the amplifier. The diodes are operated in a conventional single-tuned coaxial circuit using a movable quarter-wavelength coaxial transformer. The nominal gain can be determined by proper choice of the characteristic impedance. The second stage is operated at 1 dB less power added with a corresponding 6-dB lower noise figure than the third stage. The first stage is operated at 27 dBm of added power with a nominal noise figure of 30 dB. The optimum second-stage operating point was determined from a series of calculations made with a fixed first- and third-stage power added and noise and a variable power and noise combination of the second stage. The overall calculated output power was 40.3 dBm with a noise figure of 33 dB. This corresponds to a C/N of 146.5 dB when the input power is 8.5 dBm, the nominal input level available. The corresponding system performance is better than 15 dBrnc0.

IV. THREE-STAGE AMPLIFIER

4.1 Description of the amplifier

Figure 3 is a schematic of the amplifier. The input and output are in WR-159 waveguide. To satisfy the input match requirement, a terminated circulator is used as an isolator. A 10-dB directional coupler is used to power the input monitor diode. This diode provides a dc signal that triggers a squelch network to remove the dc power from the IMPATT diodes when the input signal decreases a predetermined amount. This prevents the first stage, which is an injection-locked oscillator, from unlocking and free-running at a frequency other than the desired frequency. The first stage consists of a circulator and the diode network. A terminated circulator is used as an isolator between the first and second stages to provide isolation
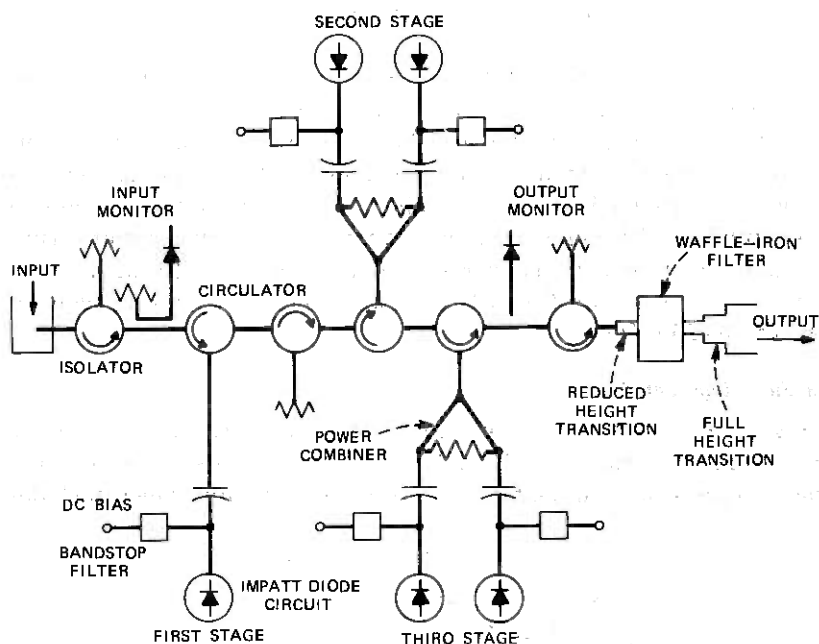
Fig. 3—Schematic representation of a three-stage, five-diode, 6-GHz IMPATT amplifier.

between them. This is especially important here because of the relatively high gain of the first stage. Any doubly-reflected amplified signal from the first stage could combine with the low-level incoming signal and introduce distortion.

The second and third stages are similar. Each consists of a circulator, resistively terminated power-combiner network, and a diode network. There is no isolator between the second and third stages because of the relatively low gain of the second stage.

The output circuit consists of an output monitor, a terminated circulator used as an isolator, a stripline-to-reduced-height transition, a waffle-iron filter, and a full-height transition. The waffle-iron filter is used to prevent any higher harmonic signals from appearing at the output.

4.2 Circuit fabrication

The circuit is fabricated on 24-mil-thick alumina substrate suspended between ground planes spaced 124 mils apart. The thin-film transmission line pattern is deposited on the ceramic substrate using photolithographic techniques. The ceramic substrates are suspended

in a channel 0.580-in. wide to prevent moding and cross-coupling problems.

The Y-junction circulator[5] consists of yttrium-iron-garnet discs bonded to both sides of the ceramic, filling the space between the ceramic and the ground planes. The ferrites are biased with permanent magnets located outside the ground-plane housing. Tuning screws are provided at each circulator port. Six circulators are in the amplifier. These circulators are capable of providing input return loss and isolation between ports of greater than 33 dB with a forward loss of less than 0.15 dB per pass over the operating band of 5.925 to 6.425 GHz.

4.3 First-stage amplifier

Figure 4 is a sketch of the first-stage amplifier. Many elements are common to the second- and third-stage circuits. The amplifier stage consists of a circulator and the diode network, which includes
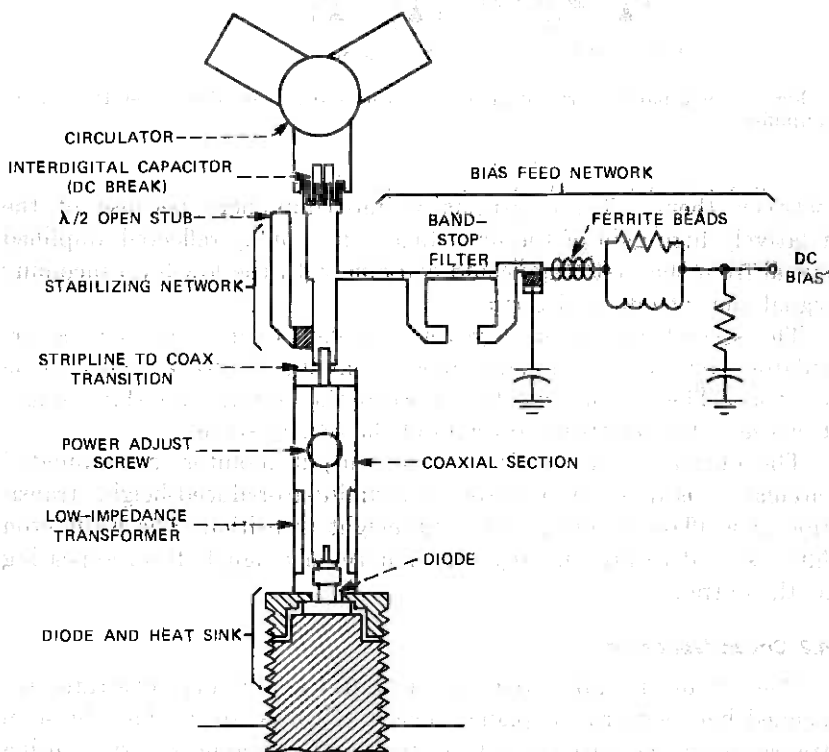
Fig. 4—Components of the first stage of the amplifier.

a dc break, a bias-feed network, a stabilizing network, a stripline-to-coax transition, a low-impedance transformer, and the diode.

4.3.1 DC break

An interdigital capacitor is used to provide a dc break, keeping the high voltage confined to the diode circuit. A detailed view is shown in Fig. 5. The total capacitance measured at 1 MHz was approximately 2.3 pF. This series reactance is incorporated into the circulator design such that, at point A, the impedance looking toward the circulator is 50 ohms. When the interdigital capacitor is used in the circuit, resonances can exist when the gap length is a multiple of a half wavelength. This can be acceptable if these resonances can be made to straddle the operating frequency band. The resonance
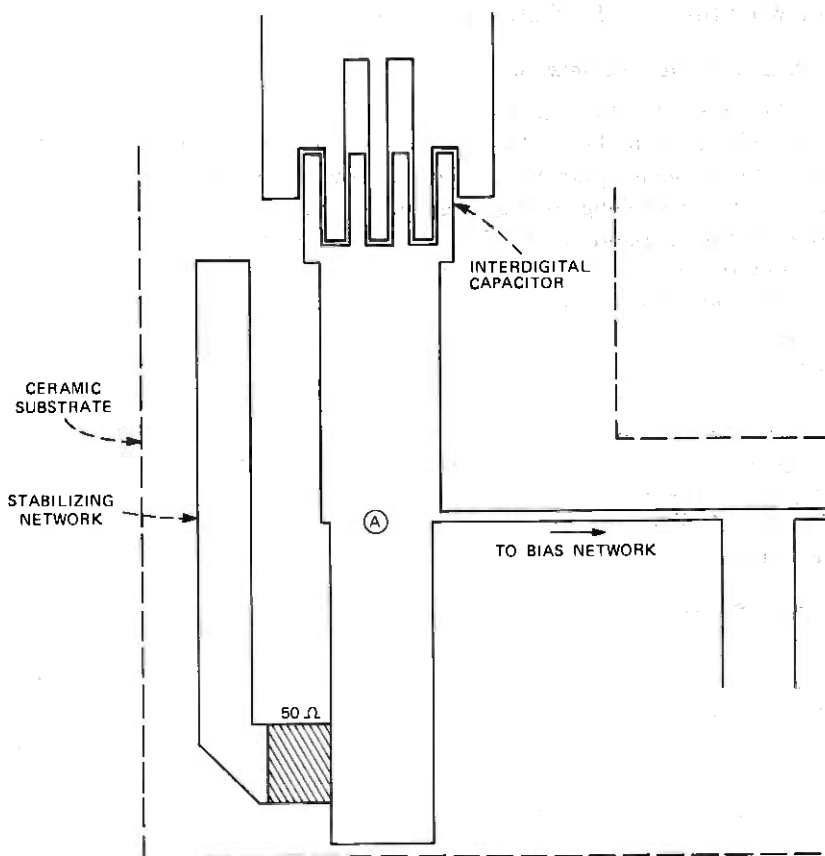
Fig. 5—Conductor pattern on ceramic substrate showing detail of the interdigital capacitor and the stabilizing network.

can be controlled by adjusting the total length of the gap, but this length also determines the total capacitance, which in turn affects the impedance match of the circulator. A simpler means of controlling the resonant frequency is to reactively load the gap.[6] This is shown in the figure as the slot in series with the transmission line formed by the gap. If the length of the slot is less than a quarter-wavelength long, the gap is inductively loaded, which essentially increases the gap length and thereby lowers the resonant frequency. By such a technique, the slot resonant frequency can be controlled without affecting the total gap capacitance. The gap was coated with a dielectric material to prevent any accidental short circuit. The coating increased the total capacitance slightly. A method of actually eliminating the slot resonance is to resistively load the series slot.[7] This is the most satisfactory method if one can tolerate a few tenths of a dB additional loss in the circuit.

4.3.2 Bias filter and network

The bias filter in Fig. 4 is a band-stop filter. It prevents any in-band signal from being lost to the bias circuit. It consists of two sections of open, quarter-wavelength, low-impedance lines separated by quarter-wavelength-long, high-impedance lines. The rejection in the operating band of 5.925 to 6.425 GHz is greater than 40 dB. At low frequencies, this filter circuit can be represented as a low-pass circuit consisting of L-C components. The circuit is terminated with a 50-ohm resistor in series with a 22-pF chip capacitor, which is grounded.

The bias network continues further in lumped elements. The purpose of the network is to provide a high resistance in the low-frequency spectrum together with a low resistance at dc. This will prevent bias-circuit oscillations of the type described by C. A. Brackett.[8] The bias is supplied from a constant-current-regulated dc supply.

4.3.3 Stabilizing network

The stabilizing network shown in Fig. 5 consists of a half-wavelength, open-circuited line connected in series with a 50-ohm resistor. This network is in shunt with the main line and helps to control the impedance presented to the oscillator outside the operating frequency band. At the operating frequency, the half-wavelength line appears as an open circuit and the resistor is essentially not connected to the circuit. At the half frequency, the line is a quarter-wavelength long and presents a short circuit to ground behind the resistor. The circuit is then shunted by the 50-ohm resistor. This

network lowers the impedance presented to the diode at the sub-harmonic frequency and helps to increase the margin of stability when properly located in the circuit.[9,10] It takes a larger rf drive before spurious oscillations appear. The penalty paid using this network is the addition of about 0.15-dB insertion loss at the band edges. The stability margin can be increased further by adding a second resistor-stub network but at the expense of additional loss.

4.3.4 Coaxial circuit

Figure 6 is the side view of the coaxial circuit. A transition is made from stripline to coax at the end where a dielectric bead is located. A tuning screw is provided for matching purposes. The diode is located at the end of the 50-ohm coaxial circuit whose center conductor is spring-loaded to take up variations owing to mechanical tolerances. A movable transformer is located in the 50-ohm coaxial circuit. The characteristic impedance of the transformer is chosen to provide the correct resistive load component to the diode. The reactive load is varied by moving the transformer to cancel the reactance of the diode. To adjust the oscillation rf level for different diodes, the resistive component is made adjustable by adding a capacitive screw approximately an eighth wavelength from the nominal end position of the transformer. As the screw penetration is increased, the equivalent transformer characteristic impedance is increased by a factor of up to 1.6.
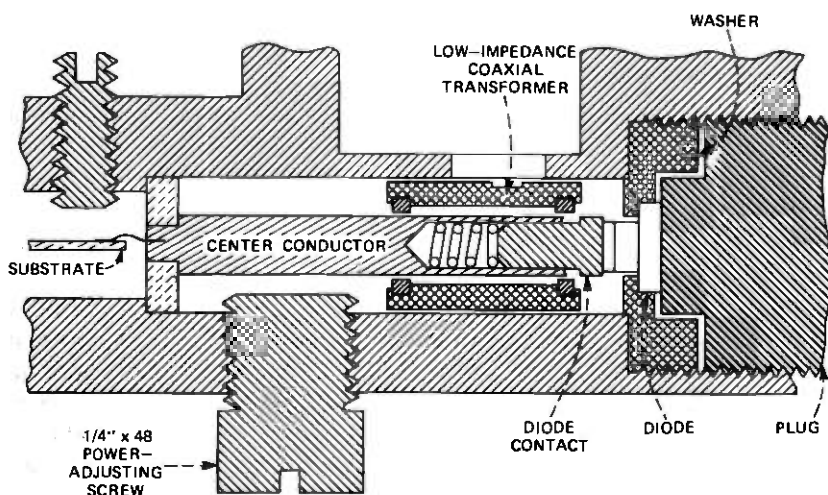
Fig. 6—Cross-sectional view of the coaxial amplifier circuit.

The diode rests in a diode washer which is screwed into the housing. A plug is screwed into the housing behind the diode, and the front surface makes contact to the back surface of the diode. One major problem of the amplifier is heat transfer from the diode to the housing. The heat must be transferred from the diode to the plug and through the threads to the housing. Some heat is transferred from the diode to the washer to the housing. The threaded washer is made as short as possible, permitting a short length for the narrow tip of the threaded plug. The plug is made as large in diameter as possible. To ensure good heat transfer, heat-sink compound is used in the threads.

4.3.5 Transformer

Figure 7 is a photograph of the coaxial transformers. The first-stage transformer is a noncontacting transformer with Teflon* beads located at both ends to center the center conductor. The transformer is insulated from ground with three Teflon strips placed longitudinally on the outer circumference spaced 120 degrees apart. The other transformers have only one Teflon bead used for centering the center conductor. The Teflon strips are located on the circumference of the transformers. An additional slot is cut in the outer circumference for the purpose of moving the transformer in the line. The characteristic impedances of the first, second, and third stage transformers were 8.3, 11.8, and 20.0 ohms, respectively. Noncontacting types of transformers were used instead of the spring-finger contacting type because of the cost advantage.

4.4 Second- and third-stage amplifiers

The second- and third-stage amplifiers are similar. Each consists of a circulator, hybrid power-combiner, dc break, bias-feed network, stabilizing network, and a coaxial section containing the IMPATT diode. Other than the hybrid power-combiner, the elements are similar to those of the first stage. The conductor pattern on ceramic substrate is shown in Fig. 8. In the hybrid power-combiner, the connecting lines are 70.7-ohm characteristic impedance and are both a quarter-wavelength long. A 100-ohm resistor provides an internal termination. All ports are matched to 50 ohms. A signal entering the port connected to the circulator (input) divides equally between the other two arms with no signal appearing across the 100-ohm resistor. A signal applied to either of the latter two arms divides

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* Trademark of Dupont Corporation.

0.400

0.375

FIRST STAGE

SECOND & THIRD
STAGES
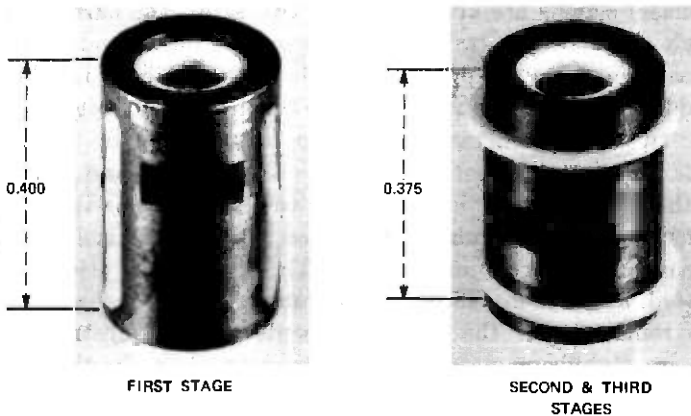
Fig. 7—Photograph of the low-impedance, noncontacting-type coaxial transformers.

CERAMIC SUBSTRATE

100 Ω

50 Ω

22pF

50 Ω
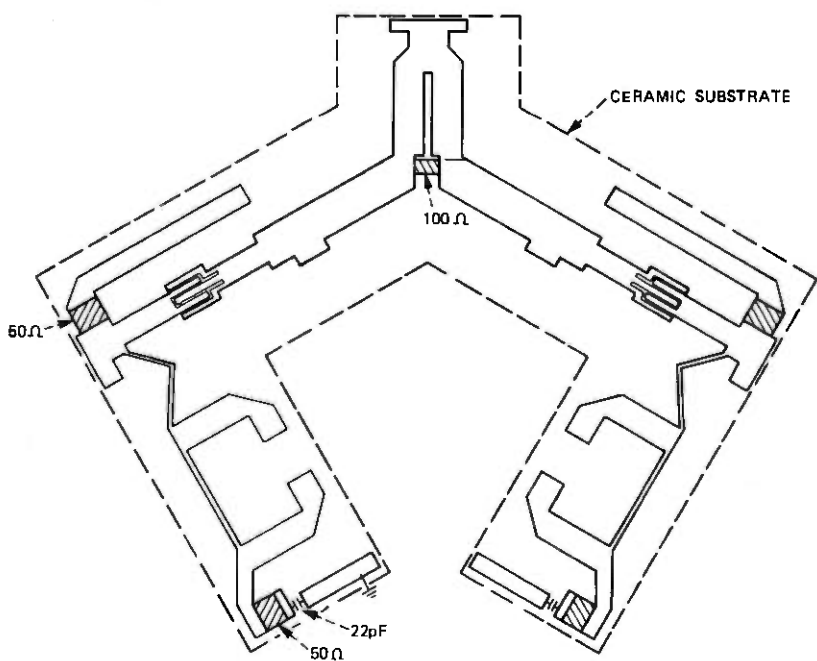
Fig. 8—Detail of the conductor pattern showing the hybrid power-combiner, interdigital capacitors, stabilizing networks, and bias networks used in the second and third stages of the amplifier.

between the 100-ohm resistor and the input. If equal (amplitude and phase) signals are applied to the two arms, the currents flowing through the 100-ohm resistor will be out of phase and will cancel, whereas the currents appearing at the input will be in phase and will add. Any difference in magnitude or phase of the signals applied to the two arms will cause power to be absorbed in the 100-ohm resistor. The isolation between the two arms was greater than 27 dB, with the balance from input to the two side arms within 0.1 dB. This type of power-combiner was used because the isolation allows independent tuning of each diode. The diodes are also physically separated, and a more efficient heat transfer can be realized.

The remainder of the circuit elements on the substrate are the dc break, stabilizing network, and the bias filter. In the bias-filter network at the dc bias-connection point, a chip capacitor is soldered onto the conductor and a spring-finger grounding clip is used to provide a connection to both ground planes.

V. PERFORMANCE OF THE AMPLIFIERS

Six prototype amplifiers were built for system evaluation and tested at two frequencies. Figure 9 shows the result of the measurement at 6.125 GHz as plotted on the power—C/N coordinates.
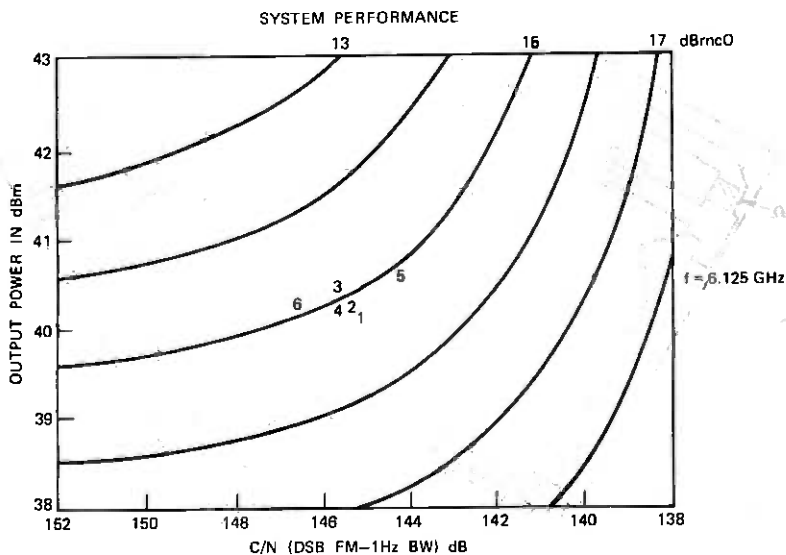
Fig. 9—Measured power and noise characteristics of the six amplifiers and their corresponding one-hop system thermal-noise performance. The numbers represent the measured data points.

(C/N of 147 dB corresponds to a noise figure of 32.5 dB for an input power of 8.5 dBm.) The numbers on the figure indicate the measured performance of each amplifier. The average power output and noise figure were 40.4 dBm and 34.1 dB, respectively. When tuned for the other test frequency, 6.375 GHz, the power output was lower but the noise was better. The average power output was 39.6 dBm with an average noise figure of 32.6 dB. The locking bandwidth of all the amplifiers was greater than ±60 MHz. The average one-hop system thermal noise performance at both frequencies was about 15 dBrnc0. System tests indicated that the amplifiers were thermal-noise limited with negligible intermodulation distortion.

The amplifier is retuned for each channel frequency. Tuning consists of :

- (*i*) Tune power output and free-running frequency on the first stage.
- (*ii*) Adjust gain and center frequency of second stage. This required iteration of the four adjustments to obtain a prescribed output power.
- (*iii*) Adjust center frequency of the third stage for maximum power output.

The power and overall noise figure were measured at other frequencies in the operating band, and Fig. 10 shows the results for one amplifier. The power output of the first stage alone, P_1, and first and second stages alone, P_{1-2}, are also shown. The power decreases at the high end of the band with an improvement in noise performance. The noise peak near the high end of the band was due to a subharmonic oscillation. In all the amplifiers, a subharmonic oscillation was generated in the third stage when driven by a high-level signal. The subharmonic oscillation introduces some excess noise but, because of the high gain existing before the third stage, the overall effect on the amplifier noise performance is minimal if the subharmonic oscillation is well established. In some amplifiers, the subharmonic does not exist at the low end of the frequency band, but it does exist at the high end of the band. At some intermediate frequency, a threshold of subharmonic oscillation is encountered. The noise at this threshold point is high enough to have an effect on the overall amplifier noise in spite of the high gain preceding the third stage. The solution to the problem is to eliminate the subharmonic oscillation completely or, if this is not easily accomplished, to have it well established at all times.

All measurements were made at room temperature ambient. The output power decreased with increasing ambient temperature at a
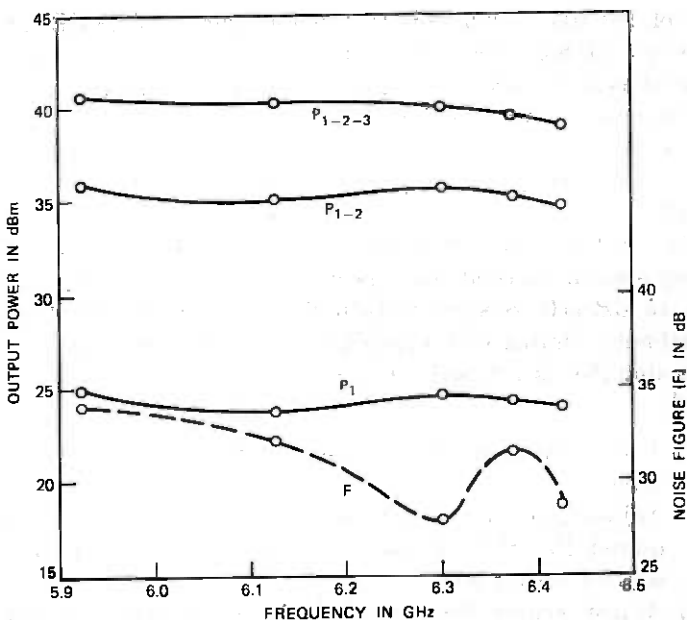
Fig. 10—Power and overall noise figure of a prototype amplifier measured as a function of frequency. $P_n(n = 1, 1\text{--}2, 1\text{--}2\text{--}3)$ indicates the output power with only the n stages turned on.

rate of about 0.05 dB/°F. This decrease was almost entirely due to variation of the first-stage amplifier gain. Temperature compensation of the first-stage gain would be necessary for uncontrolled environments.

Figure 11 is a photograph of the amplifier showing the top and bottom housing with the ceramic substrate and circuit elements. The amplifier is 11 in. wide × 14 in. long × 5 in. thick and weighs 12.5 lbs. The cooling fins can be seen on the top housing. Similar fins are also located on the bottom housing. The fins are spaced at three fins per in. The total surface area is 1286 sq. in. The measured thermal impedance of the amplifier from diode case to air was 1.5°C per W for free-convection cooling. With a diode junction-to-case thermal impedance of 5°C per W and a 25°C ambient, the junction temperature would be about 210°C. From aging studies, the predicted life would be in the order of 10^6 hours per diode. Even with five diodes, the amplifier should provide adequate reliability.

VI. CONCLUSIONS

A 10-W IMPATT amplifier has been developed whose transmission characteristics are suitable for use in 6-GHz long-haul radio relay
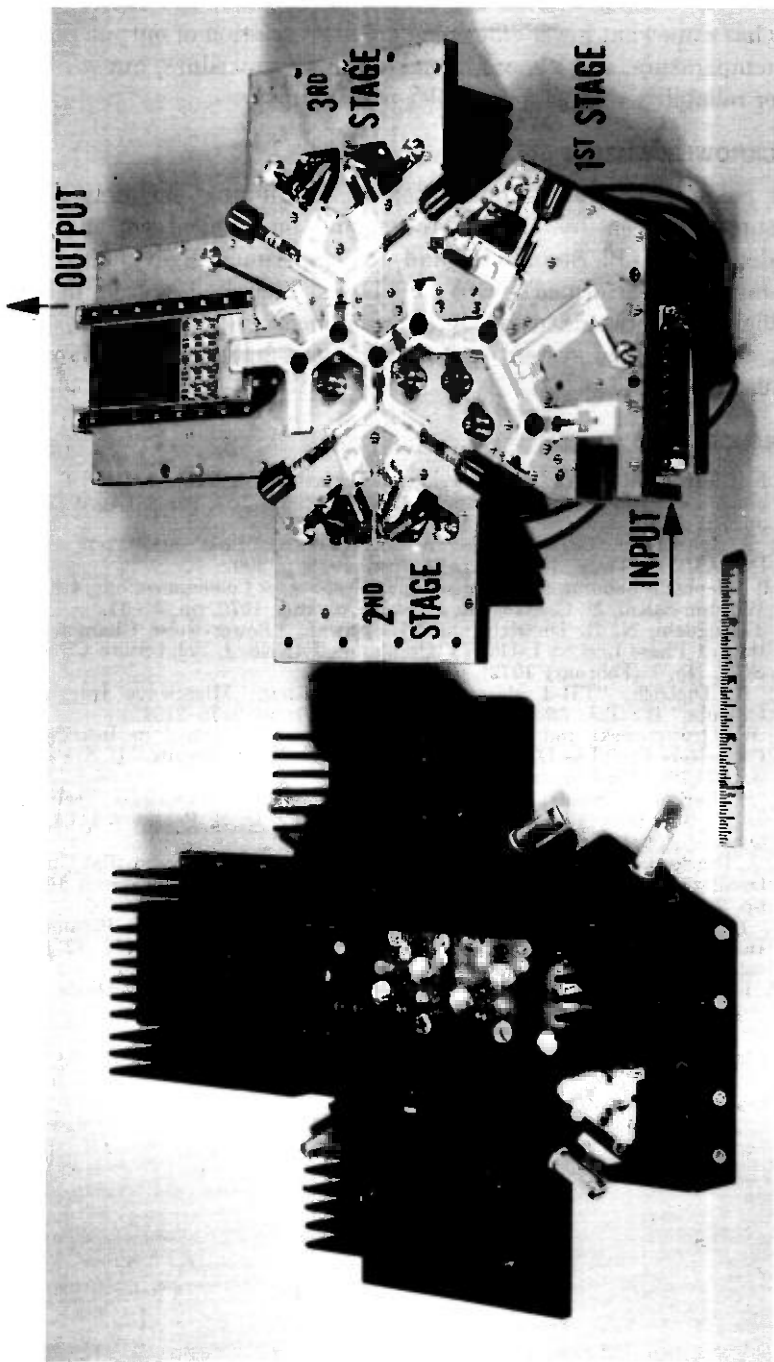
Fig. 11—Top and bottom housing of the amplifier with the ceramic substrate, diodes, and circuit elements shown.

systems. As compared with a traveling-wave tube, the IMPATT amplifier has somewhat lower efficiency, greater variation of output power with temperature, and a more intricate tuning procedure, but it offers greater reliability and uses a simpler power supply.

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Design of a Microprogram Control for a Processor in an Electronic Switching System

By T. F. STOREY

The processor in an electronic telephone switching system must be designed to efficiently and reliably process telephone calls. Because of the extended life span of a telephone switching system and the nature of the function it provides, it is advantageous to build a great deal of flexibility into the processor design. This paper provides details of a microprogram control design philosophy for the development of a medium-size processor* that provides the required flexibility. The aspects of the microprogram control that make it very suitable for the design of a processor in a fault-tolerant system are also described.

I. MICROPROGRAMMING BACKGROUND

In the 22 years since M. V. Wilkes proposed the concept of micro-program control,[1] the basic implementation has not varied significantly. Wilkes recognized even then that replacing the complex, irregular structure of the control section with a series of elementary and sequential microinstructions could result in the following advantages:

(i) A more regular and systematic approach to the design of the control section of a machine.

(ii) The ability to evolve the details of the implementation until late in the design state of the machine.

(iii) The ability to change or add to the instruction set after construction of the machine has been completed.

(iv) A simplified architecture that more readily lends itself to machine maintenance.

Because of the flexibility of a microcontrol design, many uses and variations of the design can be made to optimize the particular design

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* The name of this processor is the 3A cc. It will be used in No. 3 ESS, No. 2B ESS, and other applications where a fault-tolerant system is required.

criteria involved. The design of a microprogram control architecture that utilizes this flexibility to implement additional features in a processor is covered in detail. This processor is used in small- to medium-sized telephone switching systems[2] that must be fault-tolerant. These features provide a processor design that is

(i) Self-checking.
(ii) Highly maintenance-oriented.
(iii) An efficient microstore (i.e., minimizes number of microstore words).
(iv) Efficient in real time.
(v) Amenable to system interconnection to provide a fault-tolerant system.

II. GENERAL SYSTEM DESCRIPTION

In an electronic switching system (ESS) that performs a telephone switching function, the processor complex[3-7] must have almost 100-percent uptime. (The goal is 2 hours downtime in 40 years.) To provide such reliability, redundancy must be built into the system since hardware failures are inevitable. With redundancy available, the
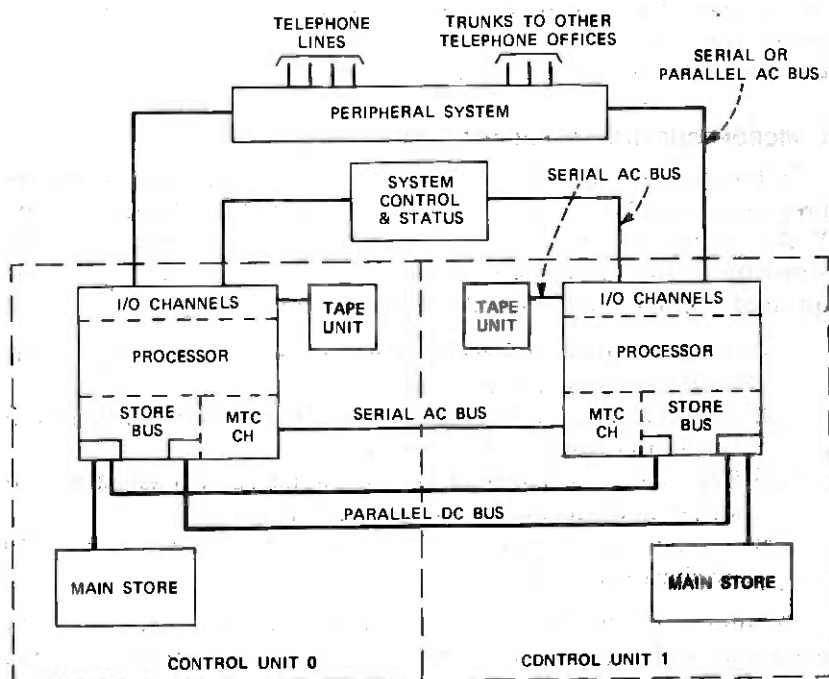
Fig. 1—System block diagram.

system can provide immediate detection of an error, a quick and efficient recovery from error (i.e., it can switch to a functioning unit), and the ability to diagnose and repair the failing unit before a second error can cause complete system failure.

The system environment in which the microprogram-controlled processor operates is shown in Fig. 1. The processor, main store, and tape unit are duplicated for reliability. These control units are treated as a single switchable entity since the quantity of equipment within each switchable block is small enough to meet the reliability requirement.

One system-design goal was to make each functional unit as autonomous and self-checking as possible with a minimum number of external signal leads. This provides sufficient flexibility to make the units expandable and changeable without much difficulty.

A simple dc store bus is used for communication between the stores and processors. The main store uses a semiconductor memory design and is contained within a small area. Even though the processors are not run synchronously, both the on-line and off-line stores are kept up to date by having the on-line processor write into both stores simultaneously. Because of the volatile nature of the semiconductor (dynamic IGFET) writeable memory, bulk storage backup (the tape unit) is required to reload program and translation data after a store failure.

III. GENERAL PROCESSOR DESCRIPTION

Figure 2 shows a detailed block diagram of the processor. It is functionally divided into six parts. There are 16 general-purpose registers and more than 30 special-purpose registers. Five of the special registers are used as the interface to the semiconductor main store. The interface is an asynchronous and relatively simple design. The microcontrol loads an address, data (if a write), and a control register. It then initiates a store cycle by issuing a start signal. Later the microcontrol tests for a store completion.

The microprogram control portion provides the complex control functions required to implement the instruction set and other sequencing functions, e.g., program reloading from the tape unit, trouble initialization, interrupt control, and man-to-machine interface functions.

The data-manipulation orders are designed specifically for implementing call-processing programs. Therefore, the orders include bit manipulation, testing, logical operations, etc., rather than complex arithmetic operations. A binary add is included to allow indexing and other simple arithmetic operations to be easily implemented. The data-manipulation logic includes rotation, all Boolean functions of two variables, first zero detection, and fast binary add.
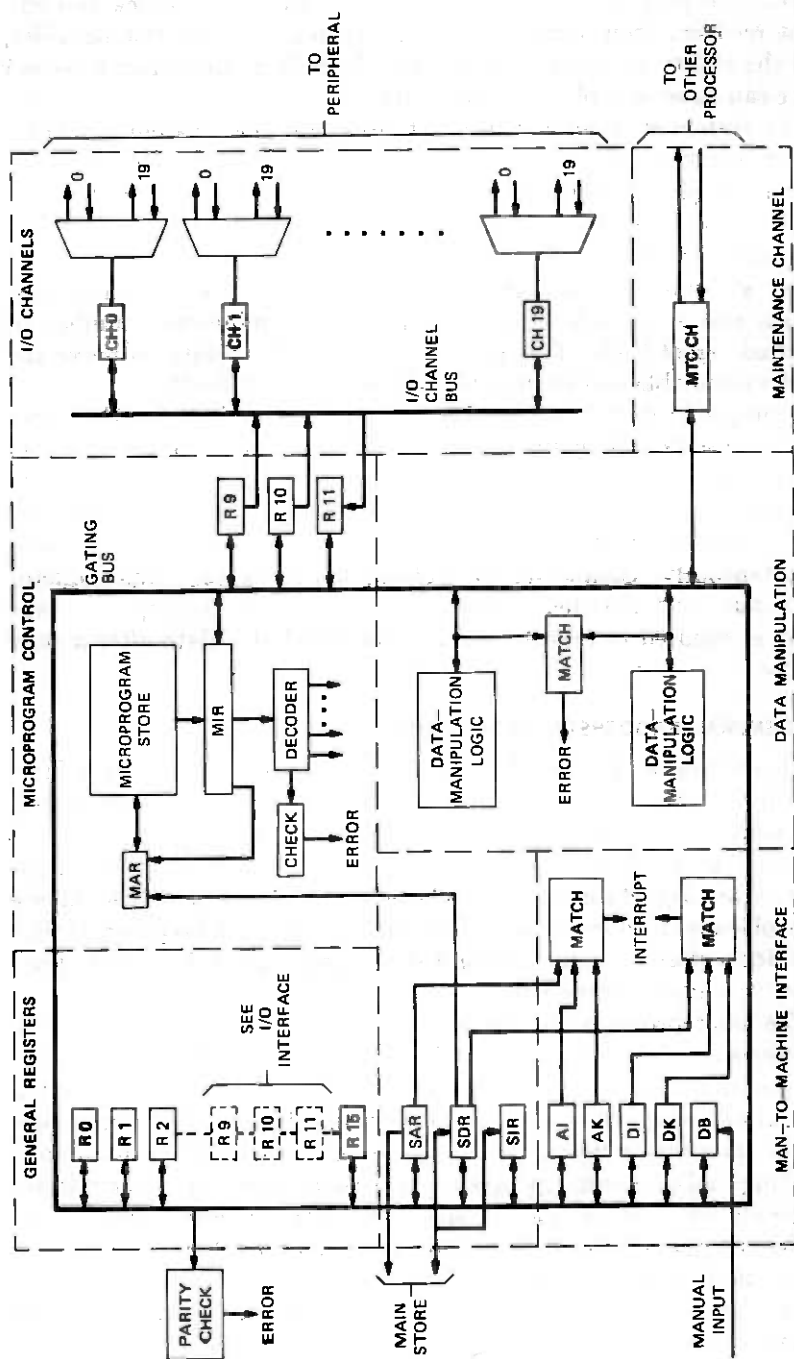
Fig. 2—Processor block diagram.

The remaining functional blocks in Fig. 2 are concerned with the interface of external units. The 20 main I/O channels, each with 20 subchannels, allow the processor to control and access up to 400 peripheral units by means of the serial data link. The serial subchannel transmits a 16-data-bit message using a 6.7-MHz bit rate. The tape unit is accessed by one of these serial channels. In addition, a man-to-machine interface with displays and manual inputs is integrated into the processor and executed under microprogram control. Finally, a maintenance channel can access the standby processor for diagnostic and control purposes. The maintenance channel transmits a switch message when an error is detected in the on-line processor. Control is then transferred to the standby processor. The use of a serial channel reduces the number of leads interconnecting the two processors and causes them to be loosely coupled. In addition to being more economical, this channel facilitates a split mode or stand-alone configuration for factory test or system test.

The basic execution of a macro-level instruction (OP code) by the processor is as follows (Fig. 3):

(*i*) The microcontrol issues a request to the main store and then executes a previously fetched instruction.

(*ii*) This request is performed and the access instruction is placed in a store-instruction register (SIR).

(*iii*) The microcontrol, having completed the previous macro-level instruction, tests for main store completion.

(*iv*) If the main store has not completed the requested cycle, the microcontrol loops.

(*v*) When the main store has completed, the microcontrol loads the SIR into an instruction buffer (IB) and a portion of the SIR into the microstore address register (MAR).

(*vi*) The portion of the SIR loaded into the MAR is the OP code field and it points to a starting address of a sequence of microinstruction that will perform or interpret the function of that OP code.

(*vii*) One of the functions of each OP code sequence is to fetch the next instruction from the main store, thus enabling the process to repeat itself.

The processor is designed using a new ESS logic gate[8] with 5- to 6-ns delay. An entire packaging technology is built around this gate. The packaging allows 200 to 300 gates to be placed on a single, small circuit pack. On each pack the gates are interconnected in a customized manner. The processor design requires 55 of these logic packs to implement a 16,000-gate design. The microstore is implemented on additional
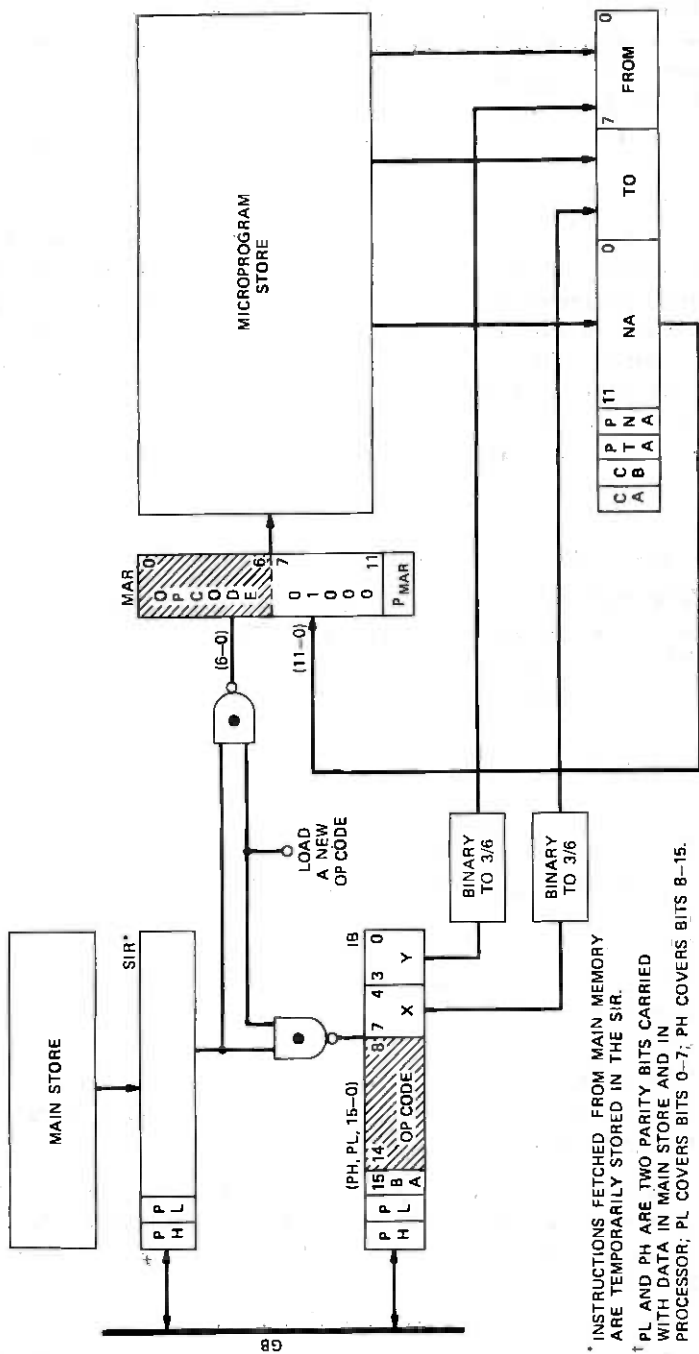
Fig. 3—Instruction buffer and its operation.

* INSTRUCTIONS FETCHED FROM MAIN MEMORY ARE TEMPORARILY STORED IN THE SIR.

† PL AND PH ARE TWO PARITY BITS CARRIED WITH DATA IN MAIN STORE AND IN PROCESSOR; PL COVERS BITS 0–7, PH COVERS BITS 8–15.

packs of which there are two for each group of 512 words (each word is 32 bits wide).

3.1 Microprogram control in an ESS environment

As in previous electronic switching systems, the goal is to provide a highly reliable switching system. The use of stored program control in ESS machines has provided easy implementation of customized features, system changes, or new services by changing the contents of the stored program. In addition, the microprogram memory provides a second level of flexibility, which creates further advantages.

The use of microprogram control permits designing a processor that is very regular in structure. This is achieved by centralizing the normally complex control section of a processor into one distinct unit or portion. Then, by segmenting each control function into a series of relatively simple microprogrammed steps, it is possible to achieve a uniform control entity. Control is easier to design through a systematic approach, and the rest of the processor is also made less complex. This results from the removal of most of the control and timing leads dispersed throughout each functional part in earlier types of processors.

Overall uniformity allows a self-checking design to be implemented without difficulty. One of the benefits of the self-checking machine in the ESS environment is that when an error is detected, the processor known to be faulty can be switched off-line immediately. That is, in a system where error detection is achieved through the synchronized operation of the *on-line* and *off-line* processors, the error indication from the match function between the two processors is unable to identify the faulty unit. As a result, other means must be provided to identify it.

In each processor, the logic is partitioned in such a way that maximum error detectability and immediate error indications are provided. For example, data registers are bit-sliced onto individual circuit packs so that multiple failures within a circuit pack will not go undetected by the parity check carried on each data register. As a result, the error circuit gives an immediate failure indication, and the problem of resolving which processor is faulty does not arise. In addition, immediate diagnostic results are achieved by sending the output of each error circuit to individual bits in an error register for easy analysis by diagnostic programs. Twenty-two error circuits in the processor are monitored by the error register. Because of the regular structure of the processor, each of these error bits tends to point to a unique portion of the machine (within a few circuit packs) that has failed and caused an error.

The use of a read-only memory (ROM) for the microstore in the microprogram control has facilitated additional simplifications in the control structure of the processor. In the event of a hardware failure or a start-up procedure caused by software problems, it is necessary to evoke a predetermined sequence of control functions. The use of a nonvolatile microstore permits the start-up procedure or initialization to be microcoded and initiated easily when required. Hence, even if initialization is caused by a power interruption, these control sequences are available. This initialization may vary from a simple transfer to a starting location in main memory to full initialization that requires reloading main memory from the tape unit. The ability to microcode this sequence of functions not only eliminates complex sequencing logic but also provides the initialization procedures with all the advantages of microprogram control (e.g., self-checking, flexibility, and easy modification).

The ability to easily modify the macro-level instruction set even after the processor has been designed is a very attractive feature, especially in an ESS environment. Due to their function, ESSs must have an extended life. This extended life makes them vulnerable to increasing demands for more capacity and new features. Therefore, it is advantageous to be able to add to or modify the instruction set of the processor if increased throughput or other significant improvements can be obtained.

Another advantage is the potential to adapt to applications where a highly reliable stored program processor is required. This potential provides a step toward standardization of processors, or at least a reduction in the number of processors used in ESS applications. This adaptability, for example, could take the form of emulation of another processor's OP code set.

Most of the man-machine interface functions, which in past designs consisted of irregular and difficult-to-maintain logic, have been incorporated into the microprogram control (i.e., displaying register and/or memory contents). The use of microprogram control in this instance not only provides a relatively maintenance-free console panel but also provides a flexible man-machine interface.

The primary peripheral communication link in this processor is a serial I/O channel. There can be 20 autonomous I/O channels. With microprogramming, the I/O interfaces can be customized to the I/O task or the application. In addition, as other peripheral communication interfaces evolve (e.g., a parallel I/O bus is used), the microcode can easily be adapted to accommodate them.

Although this is a relatively small processor, significant real-time improvements can be attained with microprogramming. That is, register-to-register gating takes only 150 ns in the microcontrol, and

transfers take place concurrently with microinstructions. As a result, there is about an 8-to-1 real-time improvement over main memory operations. As a result, the speed and flexibility of microprogram control can be customized to meet diverse requirements in an on-line, real-time, fault-tolerant control system.

3.2 General structure of the microprogram control

The self-checking microprogram control design is built around a high-speed ROM. The microstore has a 32-bit output and a maximum size of 4096 words (32 bits) and grows in increments of 512 words. The maximum access time is 65 ns. As shown in Fig. 4, the output of the microstore has three major fields:

(*i*) A TO field which normally defines a source register for a gating operation to be performed on each microcycle (a 150-ns interval).
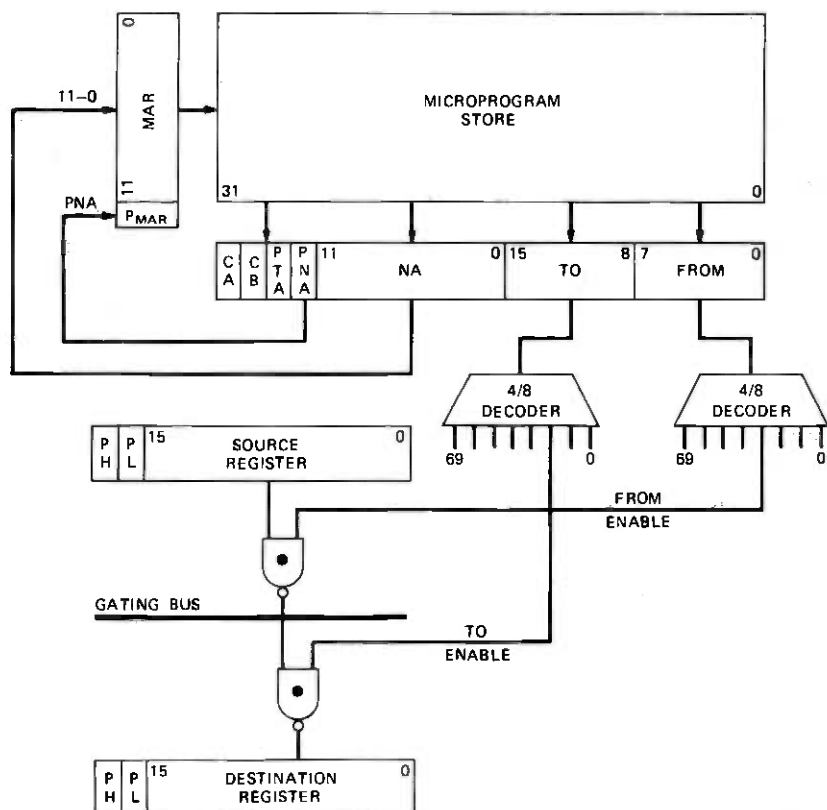
Fig. 4—Normal microinstruction execution.

(*ii*) A FROM field which defines a destination register under the same conditions.

(*iii*) A next address (NA) field that defines the location of the next microinstruction to be performed.

The correct sequencing of the microcontrol is checked by carrying a parity bit with the next-address field (PNA) and matching it with the parity of the accessed location (PTA). The TO and FROM fields are checked by encoding the control information in the microstore using a 4-out-of-8 code in each field. The control information is then decoded into a 1-out-of-70 code to enable a particular function and then re-encoded to a 4-out-of-8 code and checked.[9] The combination of these two checking techniques provides a microcontrol design that is highly self-checking.[10]

In this processor, the basic microinstruction set is centered around a register-to-register gating operation. In its simplest form, this gating function may be to set or clear individual flip-flops. To perform the gating operation, the TO and the FROM encoded control fields are read out of the microstore on each microinstruction. These fields are decoded and are used to enable a source and destination register for the normal gating command. Because an ESS environment emphasizes data processing rather than arithmetic operations, the register-to-register oriented microcommand set is very efficient. It is also useful in implementing the self-checking design of the processor. That is, by bit-slicing the processor's data registers (including the control and data access to each bit on individual circuit packs), the operation of a data transfer can easily be checked. This is done by performing the hardware check of the correct operation of the TO and FROM field decoders on each microcycle. The "checked" control signals are then fed to the bit-sliced data register circuit packs. By maintaining parity over the registers, a single failure of either the control or the data paths will result in a parity check failure.

A single failure in this context implies the failure of a single circuit pack. This could, of course, be caused by multiple failures within the circuit pack. The data registers as well as all of main store are, in fact, 2-bit-sliced to minimize the replication of the control signals to each bit of the respective registers and memory cells. As a result, there are two parity bits associated with each data word, PL, and PH (see Fig. 3). PL covers bits 0 through 7, and PH covers bits 8 through 15. In the actual partitioning, bits are paired on each circuit pack as follows: bits 0 and 8, 1 and 9, etc., and PL and PH. If a parity check error fires, either PL or PH or both could be in error.

When nongating types of microinstructions such as arithmetic or Boolean functions are to be performed, a different strategy is used.

These functions are performed in a separate entity in the processor called the data manipulation logic (DML). The DML is operated by first gating from the bit-sliced data registers to its operand fields which are buffered internally in the DML. A control field is loaded into the DML which defines the function to be performed on the operands previously loaded. The control field comes directly from the microstore and is defined by the microinstruction to be executed. Since the control field and the operands are buffered internally to the DML, the execution of a particular function is independent of the microsequence timing. In this way, functions that take longer than the basic register-to-register gating operation do not penalize the normal microinstruction execution time, nor do they require any special timing sequence. At a predetermined number of microcycles after the DML has been loaded, the microcontrol returns to the DML and gates the resultant data, as determined by the DML internal control states, to a data register.

Operations in the DML are checked by duplicating this section of the processor and matching. This approach has a number of advantages:

(*i*) Duplication is the most complete and most efficient check on the DML functions.

(*ii*) Since there is complete duplication in the DML, the logic partitioning can be optimized without concern for the failure modes for a given partitioning.

(*iii*) Duplication allows one uniform check to be performed on all miscellaneous functions that can be conveniently placed in the DML.

(*iv*) The match circuitry needs to be enabled only when gating out of the DML, and synchronization does not need to be applied to the duplicated copies of the DML other than when loading them with identical copies of operands and control states. The resulting functional execution of the DML as well as the parity generation of the resultant data can be performed independently of microsequence timing. As a result, duplicating and matching are easy to implement.

The processor's interface with main memory and I/O devices is performed in an asynchronous manner similar to that found in the DML operation. That is, interface or buffer registers are loaded with the normal register-to-register gating microinstructions. Then an execution signal is given, and a main memory cycle or an I/O cycle is started. The termination of the cycle is indicated by a completion signal which is then tested directly by the microcontrol. The result of this asynchronism is that the processor design is independent of the memory or I/O device execution times. The obvious advantage is that a variety

of memory systems and I/O units can be used with this processor. With rapidly changing technology and the cost savings that may result, this is a major benefit of the processor's architecture.

In this microcontrol design, the microinstruction to be performed and an address are included each time a word is read out of the microstore. The address is then used to transfer to the next microinstruction in a particular sequence. To maintain simplicity in the design, the 12-bit address field can transfer to any word in the microstore address range (i.e., maximum size of microstore is 4096).

To provide a flexible and efficient microcontrol design, a number of alternative methods are provided for sequencing the microcontrol. The options or alternative ways that the next address can be obtained in a microinstruction sequence are as follows:

(i) The initial microinstruction of a machine OP code is initiated by having the microcontrol sitting in a microloop waiting for the main memory to fetch an instruction. The loop is excited when the main memory fetch is completed. The result of the fetch is gated into MAR, starting the microinstruction sequence that will perform that OP code.

(ii) On a number of microinstructions, it is desirable to obtain data constants from the microstore. To efficiently use the microstore, it is advantageous to store these data in the NA field and to obtain the next address by incrementing the previous contents of the MAR. This type of operation has been used as follows:

(1) To obtain data constants. Data constants, for example, can be used to generate target addresses in main memory.

(2) To obtain additional control constants. The main use of this is the simultaneous loading of the control states into the DML with a normal microinstruction loading of the operand fields. This not only reduces the amount of microcode required, but also increases the speed of DML functions.

(3) To load a return-address register (RAR) that is used in conjunction with the microcontrol to implement microsubroutine returns. This also reduces the amount of microcode needed.

(iii) Conditionally branching on a number of status bits allows convenient testing of various machine states such as adder overflows from the DML or completion states from external units. The latter is most useful for providing the asynchronous timing between the processor and its memory, as well as between the processor and peripheral units.

(*iv*) The ability to index into microstore is provided by ORing a 4-bit binary field into the address in MAR. Indexing effectively utilizes the microstore by providing an efficient method of extracting data or control from table structures in the microstore.

(*v*) Interrupts are initiated by jamming a hard-wired address into the MAR. This address points to a microinstruction sequence which interrogates various machine states and then determines what action is to be taken. This feature simplifies implementation and checking of complicated and difficult logic. It also provides a highly flexible and easily modified interrupt structure.

(*vi*) Through the maintenance reset function (MRF), a hard-wired address is jammed into the MAR. The MRF produces a series of microinstructions that perform the bootstrapping operation of the processor during a start-up procedure.

The preceding list of alternative methods for sequencing the microcontrol represents an economic compromise. The increased cost and complexity of more exotic, more powerful microcontrol sequencing would not be offset sufficiently by reduced microstore requirements. Of course, if real time is the prime concern, the increased speed of a more powerful microcontrol would justify the increased cost. Since this machine is intended for the small- to medium-sized ESS offices, cost is the dominant factor. To minimize cost, sufficient microsequencing flexibility has been implemented to reduce costly microstore and at the same time achieve a reasonably good throughput. The standard microcode provided with this processor will be implemented with about 1000 words. For those applications that need additional real time or other features, the ability to expand to 4096 words is provided.

The microcontrol uses a high-speed ROM which has a read access range of 30 to 65 ns. The minimum cycle time of a microinstruction sequence is determined by the maximum access time of the ROM plus the time necessary to calculate the address of the word to be accessed and/or the maximum time to execute each microinstruction. The processor has a gate with a 5- to 6-ns delay. The use of the gate, its associated technology, and the 65-ns ROM results in a microcycle execution time of 150 ns.

The design of the main memory for this processor uses a dynamic IGFET refreshable cell with an access time of about 750 ns as seen at the store itself. Taking into account the control and data delays between the processor and the store, the effective main memory access time will. be about 1 μs. It should be again noted that the timing between the processor and the store is completely asynchronous and, if faster or

cheaper memories become available, they will be readily adaptable to the architecture of the processor.

The effective execution rate of main memory OP codes is, therefore, determined by three main variables:

(i) A 150-ns microinstruction cycle time.
(ii) A 1-μs main store access time.
(iii) The number and type of microinstructions that are used to implement a main memory OP code.

As far as the architecture of the processor is concerned, the 150-ns microinstruction cycle time is a constant. The memory cycle time is a variable since it depends upon the main memory chosen. The number and type of microinstructions for each OP code is a function of how the microcode sequences are designed. The use of subroutines in the microcode, as well as other techniques to limit the total amount of microstore, minimizes the initial cost of the processor. The resulting mix of the number of microinstructions per OP code tends to make the effective execution rate of OP codes processor-limited, assuming the 1-μs access time for the IGFET refreshable main memory. It can be shown that by recoding the microprogram of the OP codes using more straight in-line coding and more microstore, it is possible to make the effective execution main-memory bound rather than processor bound.

IV. DETAILS OF THE MICROPROGRAM CONTROL DESIGN

4.1 Microinstructions

The processor, excluding the microcontrol, consists of a collection of distinct sets of registers. The set partitioning is done on a functional basis with each set optimized to provide a particular task (see Fig. 2). The various sets and the number of registers included are:

(i) General registers (16). These registers provide a set of general-purpose program-addressable registers that are used for high-speed buffer storage for the macro-level (main-memory) programmer.
(ii) Special registers (16). These registers are used for a number of special-purpose functions such as generating interrupts, providing error indications, displaying system status, and interfacing with main memory.
(iii) DML registers (3). These registers provide the buffer storage required to hold the operands and control states in the DML so that the DML execution timing is asynchronous with respect to the microcontrol timing.

(*iv*) Main memory registers (4). These registers provide addresses to main memory and receive instructions and data coming from main memory.

(*v*) I/O registers (3). One of these registers buffers the control information needed to access the I/O channels. The other registers provide the means of transmitting data to and from the I/O channels.

(*vi*) Console associated registers (5). These registers are used in conjunction with the console panel to load and display various other registers in the machine and to provide match functions on address and data constants associated with main-memory operations.

With the use of the microcontrol, most of the irregular machine structure has been removed. In its place is the collection of register sets just listed. Special functions such as additions, subtractions, Boolean operations, or other operations not easily handled in a single microcycle are performed by attaching combinational logic to the outputs of some of the register sets. The outputs of this logic are then gated under microprogram control to other registers or to status bits in the microcontrol where they can be easily tested by the microcontrol.

In the description to follow, the microinstructions that control the data flow in and out of the registers are partitioned into functional groups. Each group function is described. It should be noted that the set partitioning of the registers previously listed is not related to the functional grouping of the microinstructions that control the registers, although in some cases the partitioning corresponds with them.

4.2 Register-to-register gating

Because of the machine's dependence on register-to-register gating, the microcontrol architecture is centered around this microinstruction. On each microcycle, a TO field and a FROM field are gated out of the microstore and buffered in the microinstruction register (MIR). These fields are decoded and then are used to enable a source and a destination register (see Fig. 4). The control fields are encoded in a 4-out-of-8 code so that faults in the microstore, the MIR, or the decoder will be detected. One of the methods of obtaining the 4-out-of-8 codes that enable the gating TO and FROM registers is to read them directly from the microstore. A disadvantage of this approach is that to provide all the gating combinations between the 16 general registers requires 256 entries in the microstore. Because of the relatively high cost of the microstore, which in turn influences the limited amount of microstore available for use, an alternative method is desirable. The following

implementation appears to be the most flexible and requires a minimum amount of circuitry.

It should first be noted that when an op code is obtained from main memory, it is loaded into the MAR and the IB. (See Fig. 3.) In addition to the 7-bit op code, two 4-bit binary operand fields may be loaded into the IB, as shown in Fig. 5. These two fields, X and Y, have binary to 3-out-of-6 translators attached to their outputs. The outputs of X and Y 3-out-of-6 translators are conditionally gated to the low 6 bits of the TO and FROM field in the MIR. This conditional gating is enabled when all zeros are detected coming from the microstore in the same 6-bit positions. In the upper 2 bits coming from the microstore, a 1-out-of-2 code is normally supplied. This code, which is determined by the op code, can be used to select either the general register set or the special register set in either the TO or the FROM field. This permits gating of
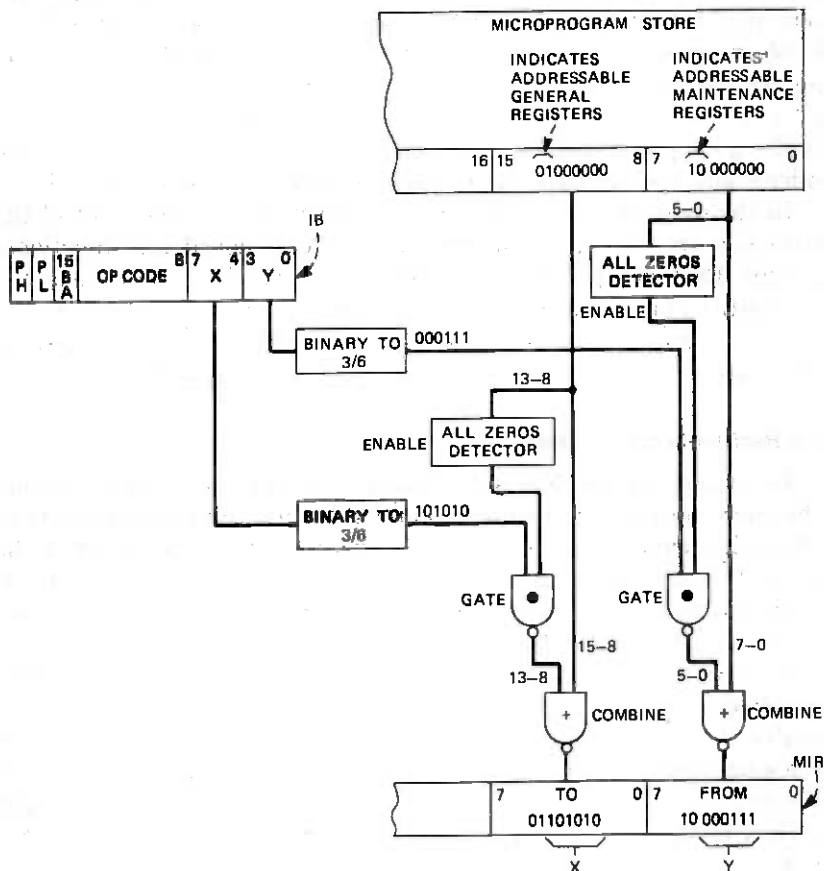
Fig. 5—OPERAND translation (normal).

any general register to any special register in a single microinstruction. One word of microstore provides the enabling signal. As indicated in Fig. 5, the signal coming from the microstore is not inhibited. The result is the logical OR of the microstore output and the 3-out-of-6 translators.

In a number of instances, it is desirable to exchange the roles of the X and Y operand fields. This is useful when the contents of various general registers are to be exchanged or swapped. Again, a number of solutions to this problem are possible. The following solution is preferred because it offers simplicity and speed, resulting from an extension of the method described previously. By storing 1s in the upper 2 bits of the TO or FROM field, and using a 2-input gate to detect this condition, a swap of the 3-out-of-6 codes coming from the X and Y fields can be implemented (Fig. 6). Note that the swap is not performed unless the low 6 bits of the respective TO or FROM coming from the microstore are zeros. It is also necessary in this instance to clear the high-order bit in the MIR field in which a swap is enabled. Because of this, the only combination allowed in the swap operation occurs when the swap involves general registers (01 in the upper 2 bits of the field).

Complete independence exists between the TO and FROM fields relative to the circuitry involved in the operand translation just described. It is therefore possible, for example, to have a 4-out-of-8 code loaded directly from the microstore in the FROM field and to have 11000000 in the TO field from the microstore. The latter results in swapping of the binary to 3-out-of-6 translator from the Y field into the TO field. As a result, most combinations of control signals for the microinstructions that involve register gating can be provided efficiently with a minimum amount of circuitry. Also, because of the use of the m-out-of-n checking techniques on the 4-out-of-8 decoders, all of the circuitry involved in the operand translations described are checked by circuitry that has already been provided.

4.3 DML operation

The DML is that portion of the machine that performs the arithmetic, Boolean, rotates, and other miscellaneous functions. These functions are collected into one entity, duplicated, and matched. The grouping of these functions is advantageous for the microcontrol design as well. A number of the operations that are to be performed in the DML take longer to execute than the basic gating cycle, and, therefore, a single and unified approach can be used for all the DML functions.

A function (FN) register is provided internal to each duplicated copy of the DML (Fig. 7). When the DML function to be performed is not a gating operation, the FN register is loaded with a control constant.
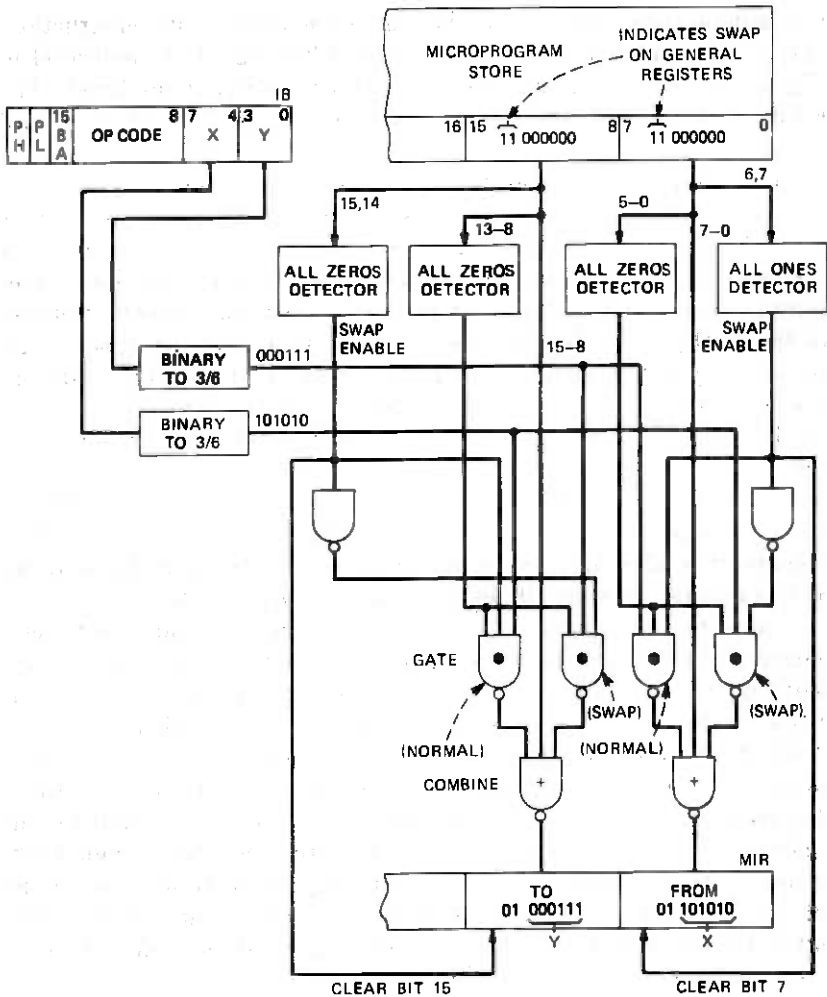
Fig. 6—OPERAND translation (swapping).

This control enables the appropriate control signals to execute the desired function. The function to be performed is executed on the operands which have been loaded into buffer registers AR and BR in the DML. Not only does the FN register set up the combinational logic to perform the logic operation on these registers, but it also determines what status bits are to be gated to the microcontrol status (MCS) register. In this way, the microcontrol can easily test for adder overflows, low-order zero test failures, etc. The use of the FN register and the buffer register for operands makes the DML execution asynchronous

Fig. 7—Microstore-DML interface.

with respect to the microcontrol. That is, the appropriate register in the DML can be loaded, and at a predetermined number of microcyles later, depending upon the function to be performed, the results of DML operation can be gated to some destination register with the normal gating microinstruction.

To increase the efficiency of the DML and to reduce the amount of microcode needed to set up DML functions, the FN register and one of the operand buffers can be loaded in parallel. The operand register is loaded in the usual manner over the data bus with the TO and FROM control signals.

The FN register is loaded over a dedicated path directly from the NA field in the MIR. This data path is 8 bits wide. The remaining 4 bits of the NA field are used to enable a decoder which enables this gating path. To check that the data coming from the microstore are correct, a parity tree is attached to the output of one of the copies of the FN register (Fig. 7) and is checked against a parity bit (PTA) that is stored with this data constant in microstore. Note that the status outputs from each copy of the microcontrol are gated to associated duplicated copies of the microcontrol status register in the microcontrol.

4.4 Setting and clearing miscellaneous flip-flops and enabling dedicated gating paths

Scattered throughout the machine are a number of miscellaneous flip-flops that must be set and cleared under microprogram control. Because of the number of flip-flops, it is desirable to use a more efficient method of controlling them than dedicating a TO or FROM decoder crosspoint for each clear or set function. The 4-out-of-8 codes themselves generate only 70 possible combinations. By assigning, for example, only ten crosspoints from each of the TO and the FROM field decoders and using these two sets of 1-out-of-10 codes to drive a third decoder (designated the miscellaneous decoder), 100 miscellaneous crosspoints can be easily generated. In addition to setting or clearing flip-flops, the miscellaneous decoder outputs are used to enable dedicated gating paths. That is, in places where both a source and a destination do not have to be simultaneously defined for a gating operation, a miscellaneous decoder crosspoint can be used. This is advantageous for I/O interfaces where, for example, an external register can be gated to the processor with a miscellaneous decoder crosspoint. Note that this minimizes any timing restrictions between the processor's basic microcycle and any I/O timing requirements.

4.5 Control bits (CA, CB) and the auxiliary control decoder

In addition to the TO and FROM set, there is another set of control signals. The method of implementing this set of control functions is shown in Fig. 7. As indicated, there are 12 bits in the NA field. Two parity check bits (PNA, PTA) check the address sequencing of the microstore. The remaining two bits of the 32-bit readout of the microstore are control bits. They are encoded into four binary states which correspond to the following:

(i) The null state is used for the normal sequencing where no control function is required and the NA field is gated to the MAR.

(ii) The main-memory instruction fetch is used to initiate a new main-memory operation.

(*iii*) The data control is used to control the gating of the NA field to the MAR. This is for data operations when the NA field contains data to be gated to some destination register other than the MAR. The data control thus inhibits the normal sequencing and adds a 1 to the previous microstore address contained in the MAR.

(*iv*) The auxiliary control is used to enable an auxiliary decoder attached to the upper four bits of the NA field. This is a 2-out-of-4 decoder and, as such, has six possible control states, four of which are presently used.

(1) The first state enables the gating of the low 8 bits of the NA field directly into the function register in the DML. As a result, the function register can be loaded at the same time that the TO and FROM fields are loading one of the operand registers in the DML. Therefore, both time and microcode are saved on DML operations.

(2) The second state, I/O parity divert, checks the parity on incoming I/O messages. As outlined in Appendix A, incoming serial messages from the peripheral world are autonomously shifted into a serial channel buffer (IOD). Then a miscellaneous decoder instruction gates the IOD to register R11 over a dedicated path. After the data from the periphery are in the machine, they must be checked for correct parity. Note that if these data had bad parity and they were gated from R11 to any other register over the processor's gating bus (GB), a processor parity error would result. This would stop the processor and switch control to the standby processor. To avoid this condition, the output of the bus parity checker is diverted to a nonfatal error which causes an interrupt rather than an error. The control to divert this check is implemented by the auxiliary control decoder. Although its use is intended for unloading R11, it can be used to divert the parity check on any source register using the GB.

(3) The third state, I/O DML match divert, performs a similar function. Again referring to Appendix A, the operation of the I/O channel is such that a microcoded loop-around check is made of the correct loading of the IOD. As such, it is necessary to match R10, which was the source register to load the IOD, and R11, into which the IOD is returned. The following design implements this matching without adding a special hardware matcher. It uses a matcher attached to the outputs of the duplicated DML units.

The match on these two registers is performed by loading R10 into AR1 of DML1 and R11 into AR0 of DML0 and then gating the AR register onto the gating bus. As was the case for the parity check on these two registers, the normal DML match error represents a hardware fault within the machine. As a result, the machine stops, and a switch is performed to the good machine. Again, the state of the auxiliary control decoder diverts the fatal error to an error condition which is handled by an interrupt. In this way, even if a switch of machines is to take place, the software chooses the appropriate point in the processing to initiate the switch. This minimizes the information lost in an initialization procedure.

(4) The fourth state, disable GB parity checker, permits the microprogrammer to turn off parity checks on individual microinstructions. The hardware is such that parity checks are normally suspended for all microinstructions that do not use the GB. In addition, the use of this state in the auxiliary decoder allows turning off the checker when the GB is being used. This is especially valuable during maintenance programming. When it is known that a register has bad parity or when there is a question concerning parity, the register contents can be gated over GB to the DML, for instance, without causing a parity error. Once in the DML, the register parity can be checked, or it can be regenerated.

4.6 Main-memory control

The use of the microprogram control presents a number of possible alternatives in controlling the main store operation. As in the design of the microstore sequencing itself, a compromise between a design that would optimize the real-time capabilities of the memory operations and the economics of such an implementation was made. As such, the main-memory control is, for the most part, sequenced by the microcontrol. This implementation removes the complex sequencing logic, which not only reduces the hardware required but also eliminates circuitry that would be difficult to make self-checking. The control interface between the microprogram control and the main store is performed by a logic entity called the processor's bus controller (PBC). Microprogram control loads a register in the PBC [the main-memory state (MMS) register] with a control constant that defines the basic static mode of operation of the memory bus. For example, if writes are to be issued to both the on-line and off-line store, an appropriate

bit in this control register is set. The microcontrol also loads an address register and a data register (if a write). With the static mode of the memory bus defined and the address and data (if necessary) loaded, the microcontrol can then initiate a main-store operation. The type of operation (i.e., instruction fetch, data fetch, or data write) is determined by the microinstruction that is used to initiate the main-store request. The microinstruction will set a request (REQ) flip-flop, set or clear the instruction or data (I.D) flip-flop, set or clear the read or write (R.W) flip-flop, and clear the main-memory cycle complete flip-flop [i.e., data ready (DR) flip-flop]. The I.D flip-flop determines to which register the accessed data are returned. The functions of the R.W flip-flop is obvious. Once the REQ flip-flop is set, the microcontrol can perform other functions. The main-store cycle will be performed concurrently, asynchronously, and autonomously to the processor. When the main store has completed the requested cycle, it will set the DR flip-flop. After the appropriate interval, the DR flip-flop is tested by the microcontrol, and the procedure is repeated.

The only major autonomous function built into the PBC is the ability to time-share the memory bus. This time-sharing capability allows the processor to be used in a multiprocessor configuration or in situations where a direct memory access device (DMA) time-shares the memory resources. This time-sharing capability consists of buffering the main-store request in the REQ flip-flop and testing the memory bus for its occupancy. If the bus is busy, the main-store cycle is delayed. When the bus is idle, the request is placed on the memory bus and the main-store cycle begins. The asynchronous nature of the processor and the main-store interface makes this design very straightforward.

Four registers are used to buffer address and data to and from the memory. These registers, together with a portion of the control that is used to operate them, are shown in Fig. 8. The operation of these registers as it relates to the microcontrol is outlined below.

4.7 Normal instruction fetch

An instruction is fetched from main memory by adding a 1 to the last instruction address located in the PA register. The control to initiate this fetch is performed by the CA, CB control decoder, as previously described. The active CA, CB combination is normally read out of the microstore on the first microcycle of the previously fetched OP code. Thus, if this OP code is, for example, an absolute transfer, the main memory control does not have to initiate the fetch for the next sequential instruction. If the next address is to be accessed, the CA, CB control enables the output of the PA + 1 logic to be gated into the store address register (SAR). It also sets two flip-flops in the memory
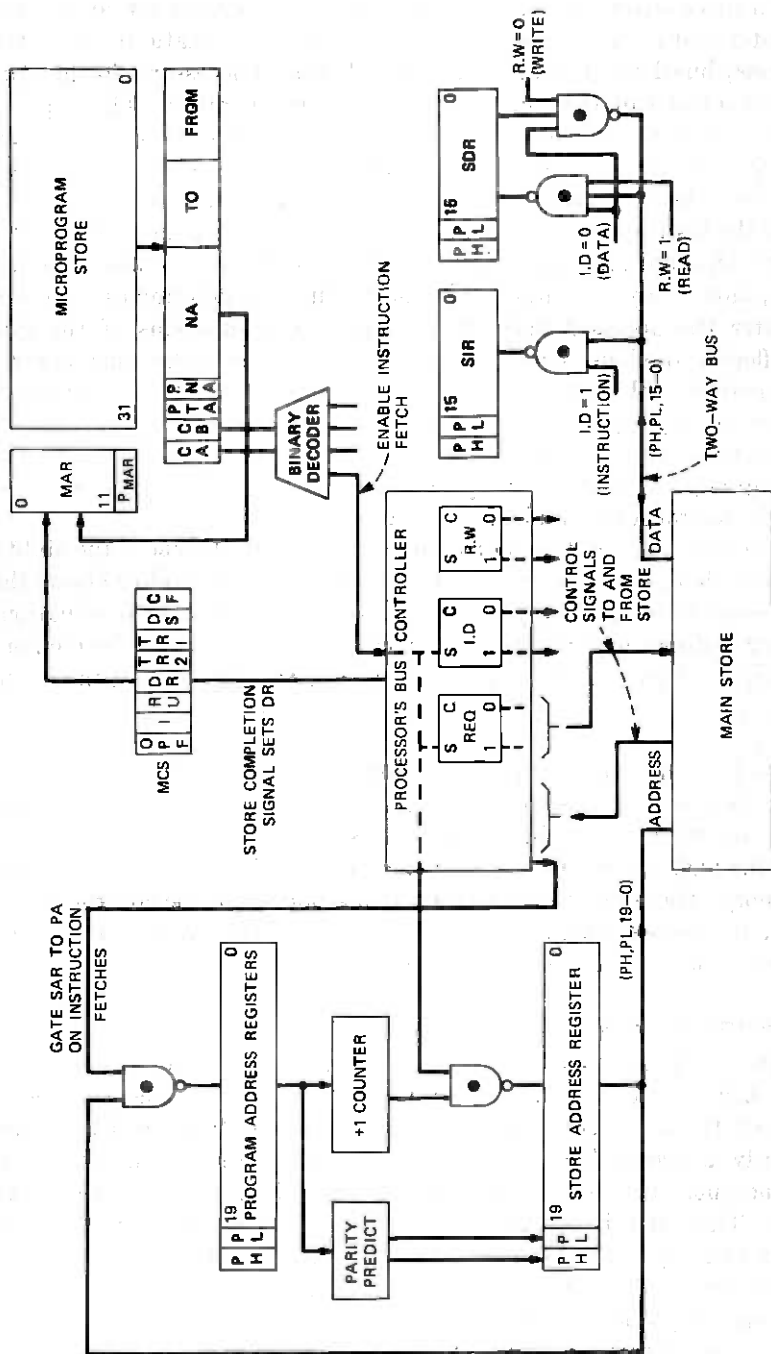
Fig. 8—Microprogram control–main-memory interface.

controller. The REQ flip-flop buffers the request for the store in case the bus is busy. The I.D flip-flop steers the return memory contents into the SIR or SDR. As a result of buffering the request, the microcontrol can continue executing the present OP code. When the memory bus becomes idle, the memory controller issues a request to the store. In addition, the controller gates the contents of SAR back around to the PA. This enables the PA + 1 counter to formulate the next address while the memory fetch is being performed. As a result, the design of the counter can be simplified. The counter is a slow ripple type that takes about 400 ns to increment. The counter is composed only of combination logic, which is attached to the output of the PA, because the PA and the SAR are bit-sliced. The resulting design provides a counter which can be easily checked by a parity predict circuit because of the partitioning which tends to force single-bit errors. It should be noted that most of the logic associated with the counter pertains to a given bit and the failure of even multiple gates within a circuit pack will cause an immediate parity error.

4.8 Data requests

When an OP code data requires a data operation, the microcontrol is used to load the data address in the SAR. If the data address must be calculated, the microcontrol uses the DML logic where additions may be performed. Once the data address is loaded in the SAR, a microinstruction crosspoint is used to initiate the store request. This memory request is again buffered in the request flip-flop, but the I.D flip-flop is put in the data state. Because the I.D is in the data state, the SAR-to-PA gating is inhibited so that the PA is preserved. The only distinction between data reads and data writes is that, for write instruction, the SDR is loaded with the data word before issuing the store request. The loading of the SDR sets the R.W flip-flop. This flip-flop is used by the bus controller and results in writing the contents of the SDR into main memory at the address defined by the SAR.

4.9 Central control panel operation

In keeping with the design goal of self-checking, each processor is assigned its own man-machine interface. This interface is called the central-control (CC) panel. The CC panel provides the ability to set and display registers in the processor, to read or write locations in main store, and to single-cycle macro-level instructions. In addition, the CC panel provides the ability to perform address-matching and data-matching functions on main-store programs. All of these functions are performed under microprogram control with only a few additional registers that provide buffer storage. The registers that are added for

these panel functions are bit-sliced and incorporated into the basic self-checking architecture of the processor.

The microcontrol executes panel functions by receiving a panel interrupt when the processor is in the MANUAL mode and off-line. The interrupt begins by gating the contents of a set of three switch input registers into the display buffer (DB) (Fig. 2) with one of three possible microinstructions. The microcontrol then interrogates the switch inputs and translates them into the appropriate panel functions. Thus, the normally complex control functions of the CC panel are incorporated into the self-checking microprogramming structure of the machine, which results in a very flexible and relatively maintenance-free CC panel.

V. SEQUENCING

Several attributes characterize the design goals of the microcontrol sequencing logic.

(i) Self-checking. Since the machine is self-checking, the microcontrol sequencing must also be self-checking.

(ii) Flexible. To provide all the advantages of microprogram control, the sequencing scheme must be flexible. For example, the ability to conditionally transfer on a number of status bits provides an efficient means to loop or branch in the microcode. The flexibility in the sequencing logic also reduces the amount of store needed to perform a given task. Indexing, the use of the next address field for the auxiliary control, and the subroutine capability are examples of this.

(iii) Simplistic. To make the sequencing logic as fast as possible, as well as to make checking easier, it is necessary to keep the design simple and straightforward. This is accomplished by restricting the microstore addresses that can be incremented. When a 1 is added to the MAR, the MAR must contain a 0 in the low-order bit and, as a result, 1 can be jammed into that bit position to avoid the use of the inherently slow and/or complex carry-propagate circuitry. The same approach is taken for indexing by forcing the indexing table to fall on restricted boundaries.

With these characteristics as design criteria, each of the various methods for obtaining the next address (sequencing) will be examined individually.

5.1 Loading an OP code

As previously indicated, a fetched instruction at the completion of a main-store cycle is loaded into SIR. Simultaneously, the DR bit is

set asynchronously to the microcontrol. While the main store is fetching the instruction, the microcontrol is operating on the previously fetched instruction. At the termination of the series of microinstructions that constitute this instruction, ALL ZEROS is encountered in the NA field of the microstore. ALL ZEROS is placed in the MIR NA field of the last microinstruction of all OP codes. A special all-zeros detector is used to monitor this condition. The coincidence of the all zeros and the DR bit set results in a new instruction or OP code being loaded into the microcontrol (Fig. 9). If the main store has not completed the instruction fetch (i.e., DR = 0), then the ALL ZEROS in the NA field is gated into the MAR. At the ALL ZEROS location in the microstore, ALL ZEROS is also placed in the NA field. As a result, the microstore will loop on ALL ZEROS waiting for the main store to complete the instruction fetch. Note that null (no operation) microinstructions (NOPs) are placed in the TO and FROM fields of the ALL ZEROS location. These NOPs are valid 4-out-of-8 codes required to keep the 4-out-of-8 checks "happy." If the main store is ready when the last microinstruction of the previous OP code is read out of the microstore, the next OP code will be loaded immediately. As a result, microinstruction NOPs will not be executed between main-memory instructions.

When an OP code is loaded into the MAR from the SIR, it is also gated into the IB and the RAR. The IB is loaded with the complete contents of the SIR. Although the OP code is loaded into the IB, it is not used there. This feature was implemented to preserve bit-slicing. In addition to loading the OP code into the IB, the branch allowed (BA) bit is also loaded into the IB (Fig. 3). This bit must equal a 1 for target addresses on branch instructions. An OP code that calls for a branch performs a microinstruction that sets a BA check bit which in turn enables a check for the BA = 1 on the next instruction fetch.

5.2 Normal sequencing

Each time a word is read out of the microstore on a normal microinstruction, an address is read into the NA field. After being gated to MAR, this address points to the next microinstruction in that sequence. Thus, loading an OP code into MAR initiates a sequence of microinstructions that is programmed to perform that OP code. The last microinstruction of that sequence contains all zeros in its NA field. Consequently, a new OP code is loaded into the MAR, and the process is repeated. The inherent simplicity of the sequencing scheme permits a simple parity check code to verify the proper operation.

Each time a word is read out of the microstore, two parity check bits are included. One check bit (PTA) is matched against the parity of the address that accessed the word (see Fig. 3). The other parity bit (PNA) is associated with the 12-bit NA field and is gated into the MAR
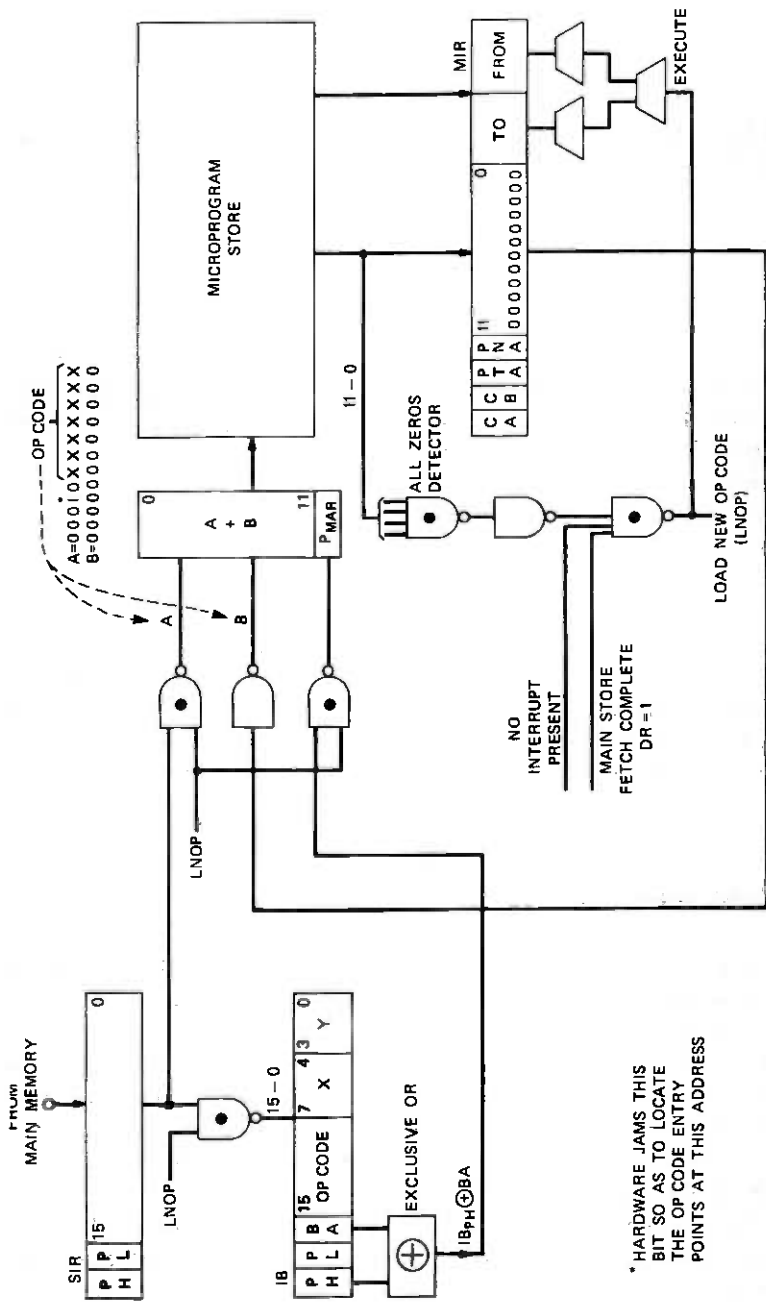
Fig. 9—Loading a new op code.

parity (PMAR) to check the next word to be accessed. Two control bits, CA and CB, are also included in the parity check of the accessing.

5.3 Data

It is useful to be able to store data constants in the microstore so that they can be easily and quickly generated by the microcontrol. For example, the machine has 16 hardware interrupt levels. Using microprogram control and the data facility, these interrupt levels can be translated from a bit position in the interrupt set (IS) register into address locations in main memory where the appropriate software can implement each one of the individual interrupts. The microcontrol tests for the bit position and then provides access to the word in micromemory that corresponds to this bit. Residing in this word is a data constant which points to a main-memory location. Because the contents of micromemory are changeable, the implementation is a flexible one.

When data are read out of the microstore, they are contained in the NA field. As shown in Fig. 10, the data can be gated on either the high 12 or the low 8 bits of the GB. The FROM decoder determines which bits are used, and the TO decoder selects an arbitrary destination register.

Since the NA field contains data, the next address must be obtained from another source. In this instance, it is generated by saving the last address and adding a 1 to it. As previously outlined, data words are forced to be on even word boundaries. As a result, a 1 is jammed into bit 0 to implement an add. In addition, the parity for this data address can be easily predetermined. It is formed by complementing the present parity bit PMAR in MAR. The CA and CB control bits save the contents of MAR, add a 1 to it, and complement PMAR.

5.4 Auxiliary control

The sequencing of the next address for auxiliary control is identical to the data operation just outlined. In this instance, the NA field contains control information and, in the case of the loading the FN register, data as well. Thus, the next address is obtained by adding a 1 to the address saved in MAR. As with data, the auxiliary control functions must occur on even word boundaries. The CA bit equals 1 for both data and auxiliary control operations. This bit is used as the control to save the MAR and to jam a 1 into it. In checking the operation of the CA, CB control decoder, the data and auxiliary control decoder leads are used to complement the MAR parity bit.
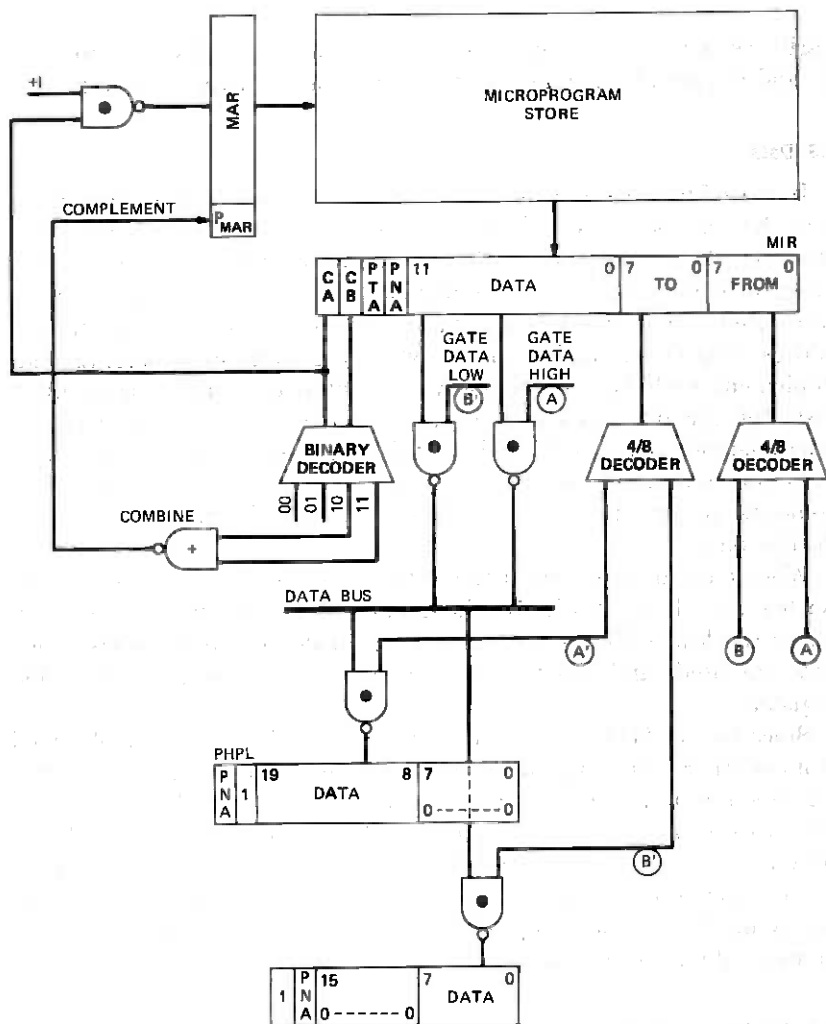
Fig. 10—Data command.

5.5 Microsubroutine

To describe the function of a microsubroutine, it is necessary to outline the normal operation of the return address register (RAR). Each time a word is read out of the microstore, the NA field is gated into the RAR. As outlined in Appendix B, this provides an additional check on the address sequencing at a very minimum cost. When a subroutine is to be entered, a data command is used (see Fig. 11). This data command contains the return address in its NA field, which is then gated both into the MIR and the RAR. Contained in this same
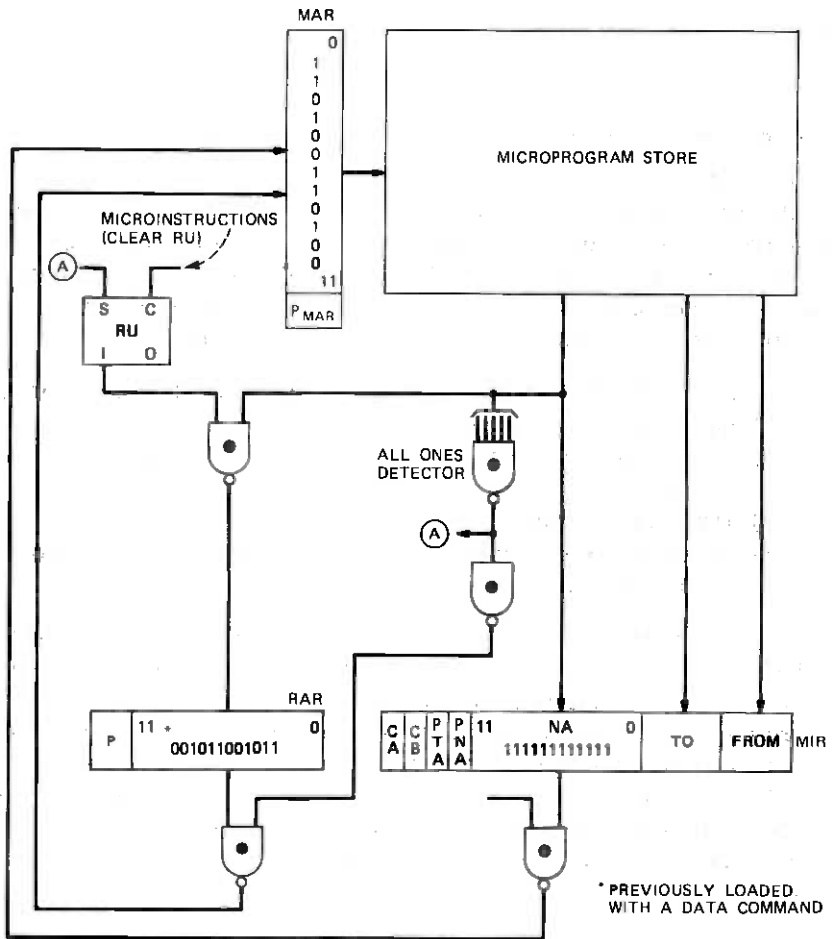
Fig. 11—Subroutine return.

command is a microinstruction which clears the RAR update (RU) flip-flop. This flip-flop saves the contents of the RAR and therefore inhibits gating into the RAR on the subsequent microcycles. As with normal data operations, the first address for the subroutine is obtained by jamming a 1 into the old contents of the MAR. The subroutine continues to sequence the microstore in the normal manner. Except for calling another subroutine, all sequencing operations of the micro-control can be performed in the subroutine. On the last microinstruction of the subroutine, ALL-ONES are placed in the NA field. An ALL-ONES detector placed on the output of the NA field results in the return address in RAR being gated to the MAR, and the subroutine is excited.

In addition, the ALL-ONES detector sets the RU flip-flop so that it is again in the update mode.

5.6 Conditional branches

The ability to conditionally branch within a microsequence is one of the basic operations of the microcontrol. To facilitate this operation, a microcontrol status (MCS) register was implemented (see Fig. 12). Each of the bits of the MCS can be individually tested: a conditional transfer is performed as a function of their respective states. Some of the bits and their primary function in this register are:

(*i*) DS—Stores the results of DML operations (i.e., adder overflows).

(*ii*) DR—Indicates the completion of main store cycles.

(*iii*) TR1—General-purpose status bit intended for use by microcontrol.

(*iv*) TR2—Same as TR1.

(*v*) CF—Passes status information between macro-level program sequences (i.e., condition flip-flop).

On a conditional branch instruction, a microinstruction selects which MCS bit is to be tested. The state of this bit is then gated into the MAR bit 0. By forcing conditional branch instructions to fall on even word boundaries, the implementation is simple. The NA field from the MIR is gated into the MAR in the normal manner. If the MCS bit is a one, the branch is made to address $X + 1$, and if not, the address X is chosen. The MCS is duplicated. One copy of the MCS feeds the MAR bit 0, and the other copy feeds the MAR parity bit which, if the branch is taken, is complemented.

5.7 Indexing

Indexing is used to permit the microprogram to easily branch into blocks of microstore so that operations like binary to m-out-of-n code conversions can be easily performed. The index operation results in either of the two 4-bit binary fields X or Y in the IB being ORed into the lower four bits of the MAR, as shown in Fig. 13. Again, to provide simplification, indexing tables are forced to start on 16-word boundaries. The implementation is then analogous to the conditional branch. A microinstruction selects either X or Y and jams it into the low four bits of the MAR, which are guaranteed to be zero. The parity for this address is generated by using the parity trees attached to the X and Y fields. If X_P or Y_P is odd, the PNA bit is complemented when it is gated to the MAR register (PMAR).

Fig. 12—Conditional transfers.

Fig. 13—Microstore indexing.

Interrupts are buffered in the IS register, which contains 16 bits; 16 different levels of interrupts are possible. An interrupt mask (IM) register is also provided. This register can selectively block any one of the 16 interrupts. When an interrupt enters the IS register and is not masked by the IM register, this condition is monitored by the micro–program control. This monitoring or testing is performed at the end of each microinstruction sequence when ALL ZEROS is read out of the microstore.

Before a new OP code is loaded into the MAR, the state of the interrupt lead is checked. If an interrupt is present, whether a main-memory fetch is completed (DR = 1) or not, an interrupt address constant is hard-wired jammed into the MAR. At this address in the microcontrol, an interrupt microroutine is initiated. It tests which of the 16 interrupt levels is present and transfers the control to the appropriate program in main memory. This transfer consists of translating a bit position in the IS to a data constant in the microstore that points to the main-memory program that handles the interrupt. Before control is passed to software in the main store, the interrupt microcode saves critical registers and states of the processor in a save area in main memory. Thus, when control is returned from the interrupt, the processor can be returned to its original state.

If real time is critical, high usage or frequently called interrupts can be handled entirely with microprogram control. Because of the 8-to-1 speedup of microcycles versus main-memory cycles, this capability represents a very powerful feature. The only change is an increase in the amount of microcode used.

A block interrupts (BIN) flip-flop inhibits the interrupt mechanism. BIN inhibits additional interrupts from being serviced before the interrupt-handling software has recorded the presence of the original interrupt (Fig. 14).

5.9 *Maintenance reset functions (MRF)*

Several conditions require the processor to be initialized. The source of the initialization may vary from a processor error, where the processor is on-line, to turning on the power in the off-line. All these varied conditions are funneled into a state which results in a hard-wired address being jammed into the MAR. In addition, a few processor state flip-flops must be initialized to ensure that the machine will start up correctly. For example, the clock must be initialized before the microcontrol will sequence. At the MRF address, a microroutine (bootstrap sequence) performs all the complex decisions concerning what caused the initialization and what actions are to be taken. The ability to reduce
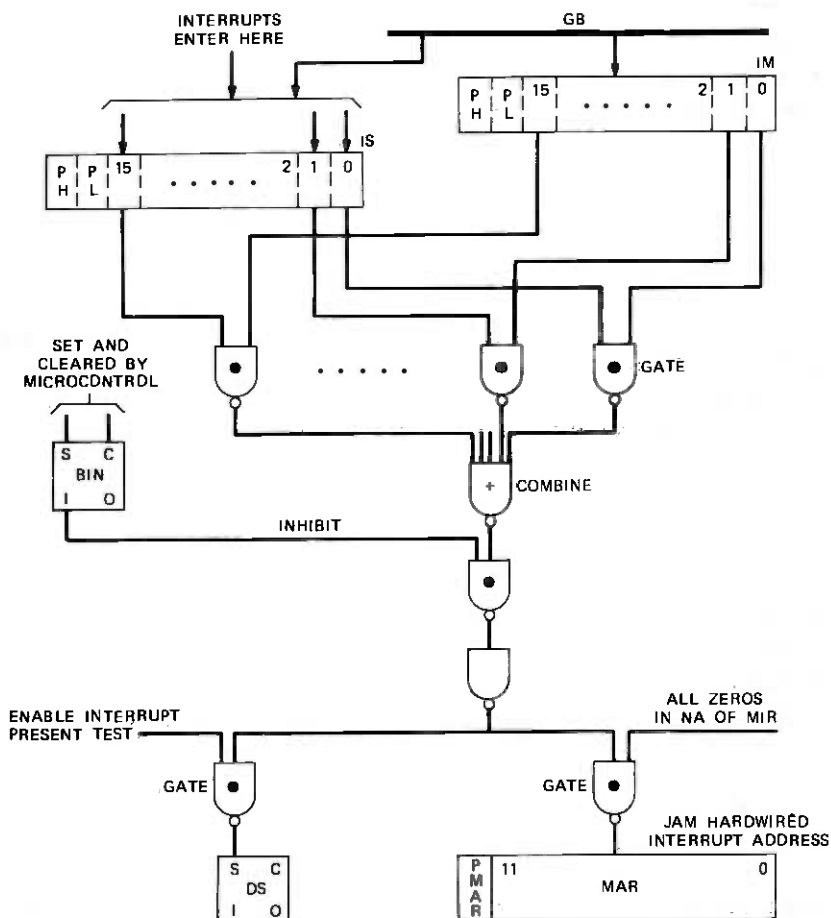
Fig. 14—Interrupt hardware.

the circuitry required to initialize the processor to a flip-flop, a few gates, and a couple of clock phases is a very significant advantage provided by microcontrol. In addition, the use of the bootstrap microsequence provides the ability to implement a very versatile initialization start-up procedure. For example, the bootstrap sequence may be changed to suit the application, such as using a disk instead of a tape unit for backup storage.

VI. MAINTENANCE OF THE MICROCONTROL

The microstore for the standard processor consists of about 1000 words 32 bits each, and it grows in 512-word blocks up to 4096 words. Because of the size and the different applications containing dissimilar
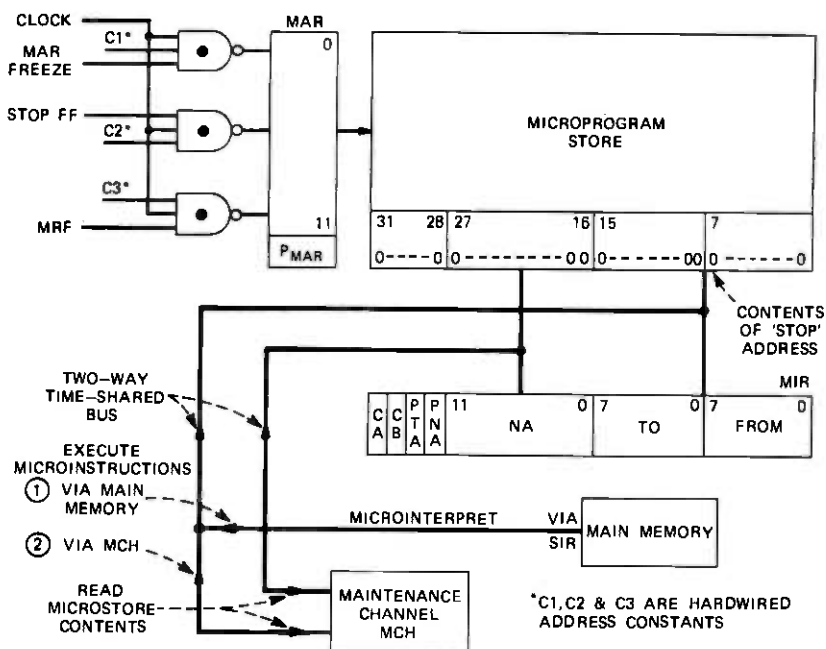
Fig. 15—Maintenance access to microcontrol.

contents, it is necessary to provide maintenance access to verify the operation and contents of the microstore. It is also quite useful to be able to exercise the machine without using the microstore itself. The most useful tool for maintenance access to the processor is via the maintenance channel (Fig. 15). The maintenance channel inhibits the microcontrol and loads microinstruction directly into the MIR. This permits the on-line processor to perform maintenance operations on the off-line processor. The feature also allows microinstructions stored in the on-line main memory to be executed in the off-line processor. This ability to access and control a unit at its most elementary level of control allows a very high degree of diagnostic access. In addition to executing microinstructions, the maintenance channel can load the MAR with an arbitrary address and in turn read the contents of that microstore location. Thus, an image of the microstore contents kept in main store can be matched against the contents of the off-line processor.

6.1 Maintenance-channel access

Before the maintenance channel can gain access to the processor, it is necessary to stop the microsequencing. Also, if a processor error is

detected, that processor must be stopped so that it does not attempt to interfere with the healthy processor, which is then switched on-line. To implement this, a STOP flip-flop is used. Setting the STOP flip-flop results in a hard-wired address being jammed and held in the MAR. This prevents the microstore from sequencing until the STOP is cleared. At the STOP address in the microstore, all zeros are contained in the 32 bits. The effect of this is to remove the microstore from the input gating to the MIR. This allows the output of the maintenance channel to be ORed directly onto the output of the microstore. As a result, no additional control signals or gates are needed. The data that are ORed onto these leads, using a NAND gate collector-tie, are clocked into the MIR in the normal manner.

The maintenance channel gains access to the standby processor by setting the STOP flip-flop. With the STOP flip-flop set, the maintenance channel has access to the MIR. As such, it has almost complete control to exercise the processor since all microinstructions emanate from the MIR.

The description and operation of the maintenance channel are covered in other material,[7] but two of its more important functions and one that is implemented for the most part within the microcontrol itself are covered here.

6.2 Single-cycling a microinstruction

With the processor held in the stopped state (STOP FF = 1), all microsequencing ceases, and zeros are read out of the microstore. The stopped state, however, does not inhibit the processor's clock. Consequently, on each microcycle, the data presented to the input of the MIR are clocked into that register. For the stopped state, these data are all zeros, but no errors are registered by the error register because the output of the STOP flip-flop inhibits the 4-out-of-8 checkers on the TO and FROM fields, as well as other checks that are normally performed on each cycle of the microcontrol. Thus, the maintenance channel needs only to gate data onto the inputs of the MIR TO and FROM fields for the duration of the clock phase, which loads the MIR. The result is the execution of a single microinstruction, which uses all of the normal timing and hardware within the machine. To turn on the decoder checkers, the maintenance channel also needs to activate a control lead to the TO and FROM checkers that will override the STOP flip-flop inhibit function of the checker for that single microinstruction.

6.3 Freeze and read microstore

The ability to read the microstore is provided by the freeze state. As has been indicated for single cycling, the input to the MIR represents

the key to gaining access to the microcontrol and to the processor. To execute a microinstruction, it is necessary to load the low 16 bits of the MIR. To access a particular word in the microstore, the upper 16 bits of the 32-bit register are loaded. Similar to loading a microinstruction, the same type of operation of the maintenance channel is required for loading the upper 16 bits (NA field). Once in the MIR NA field, the microstore address is gated up to the MAR by the normal clock timing. At this point, the processor uses a control signal from the maintenance channel to set the freeze flip-flop and also to clear the STOP flip-flop. Note that the STOP flip-flop must be cleared because, in its set state, it jams a hard-wired address into the MAR. When set, the freeze flip-flop inhibits further clearing of the MAR after the register contains the address loaded from the maintenance channel via the upper half of the MIR.

One of the added benefits of this implementation is that the inhibiting circuitry on the MAR is already provided. As previously described, the data command functions by inhibiting the clearing of the MAR and adding a 1 to it to obtain its next address. Thus, only a single flip-flop is required to buffer the freeze control signal from the maintenance channel. The output of this freeze flip-flop is ORed into the inhibit circuitry already implemented on the MAR.

Once an address has been loaded and frozen in the MAR, the contents of this address are presented on the outputs of microstore on a dc basis. The maintenance channel can now read the upper and lower halves in succession and send the response back to the controlling source (i.e., the other processor). If another word is to be read out of the microstore, the maintenance channel must first put the processor back into the stopped state so that the output of microstore will return to all-zeros state, allowing the ORing into the input of the MIR again.

6.4 Start microcontrol sequencing

When an arbitrary address has been frozen in the MAR, the maintenance channel can easily implement a start (beginning at this address) of the normal microsequencing by clearing the freeze flip-flop. The ability to start the microcontrol at an arbitrary address gives the maintenance programmer added flexibility, but the primary source of initiating a microcontrol startup is via the MRF hardware. The advantage of using MRF hardware is that it jams a number of key flip-flops in the machine to a predetermined state and then transfers control to the microcode by use of a hard-wired constant into the MAR. The result is an MRF sequence that can start from an unknown state and go first to a known state determined by initializing flip-flops and then to a

running condition using minimal hardware. This MRF sequence is invoked by the maintenance channel when a fatal or serious error is detected in the on-line processor. When this error is detected, the on-line processor stops. In turn, maintenance initiates a switch message which results in an MRF or start-up to the off-line processor.

6.5 Microinterpret

Microinterpret allows microinstructions to be stored in main memory of the on-line processor to be executed by the microcontrol of that processor (Fig. 16). One of the advantages of microinterpret is that maintenance instructions (being nonreal-time critical) can be performed without using microinstruction sequences stored in the costly microstore. The maintenance programmer, therefore, has the full use of the microcontrol and yet has the freedom to write microinstruction in a manner best suited to his needs. Not only does the microinterpret reduce microstore requirements, but, as described later, its implementation is such that a very minimal amount of additional hardware is needed to design it into the processor's architecture.

The microinterpret mode essentially allows the enhancement of the instruction set in the on-line processor to perform maintenance-oriented or seldom-needed functions at a minimal cost. The maintenance channel, on the other hand, provides the diagnostic capability to detect and locate troubles in the off-line processor as well as to monitor the general state of affairs in that off-line processor.

The initiation of the microinterpret mode is performed by one of two macro-level OP codes which are executed in the normal manner by the microcontrol. One OP code indicates a single-cycle microinterpret; the other indicates a multiple-cycle microinterpret instruction. The microsequence of each OP code first sends the main memory on for the next instruction located at PA + 1. This fetch request is performed in the usual manner by the CA, CB bit combination set to the fetch state. At this PA + 1 address, a microinstruction is stored (i.e., two 4-out-of-8 codes instead of an OP code). The next step of the microcode is to set or clear the general-purpose microcontrol test bit, TR1. The microinterpret OP code determines whether TR1 is set or cleared. If only a single microinterpret instruction is to be fetched from main memory, the TR1 bit is set.

The third and last function of the microinterpret OP codes results in setting the microinterpret (MINT) flip-flop. Setting the MINT flip-flop enables the next word fetched from main memory to be gated directly from the SIR to the MIR TO and FROM fields. As shown in Fig. 16, this gating is also conditioned on the NA = ALL ZEROS and the DR bit = 1, exactly analogous to the loading of a new OP code. As a result, the microstore loops on the all-zeros address until the main memory has
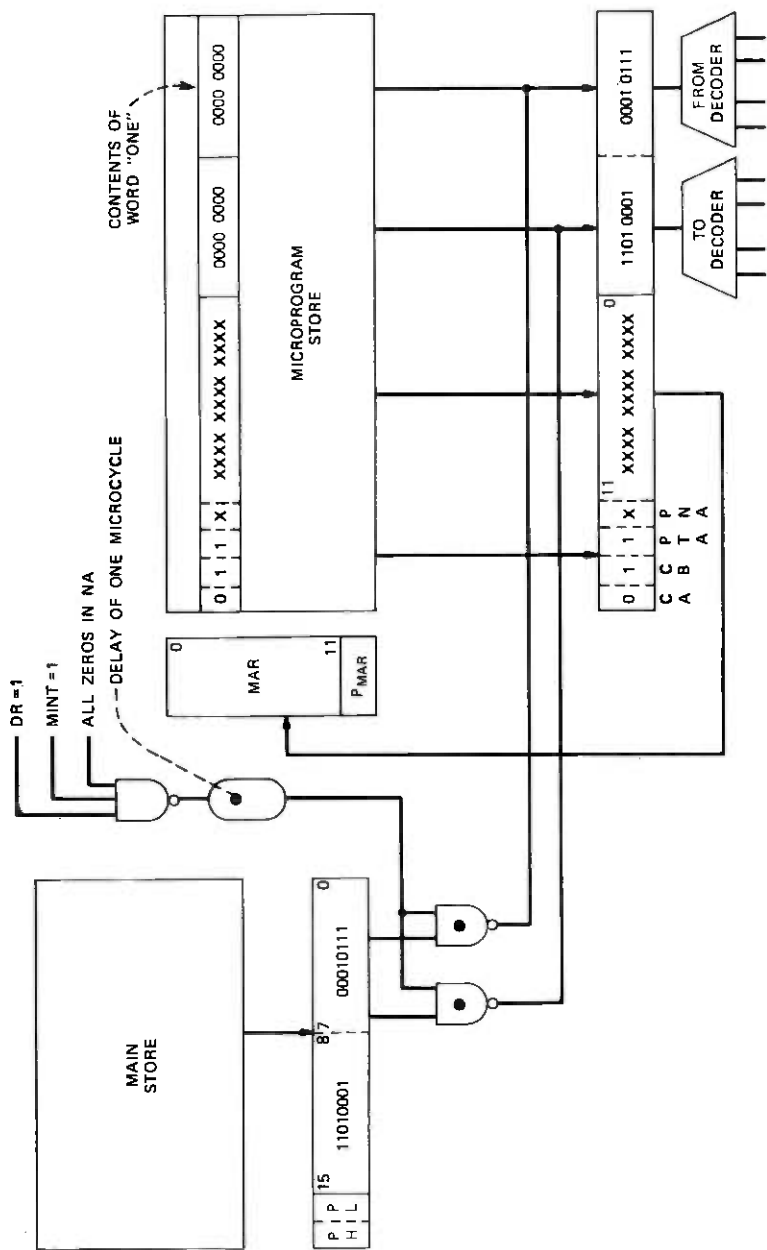
Fig. 16—Microinterpret implementation.

completed the fetch for the microinterpret instruction. When the store has indicated a completion, a 1 is jammed into the MAR, and the gating from the SIR to the MIR is initiated (see next paragraph). The next address for the microcontrol is then at location "1" where the start of the special microsequence handles the microinterpret operation. At word "1," the CA, CB bits are again in the fetch state. They result in the PA + 1 being loaded in the SAR so that the next instruction will be fetched. This instruction can either be a microinterpret instruction or a normal OP code which is determined by the TR1 bit. The microcontrol tests this bit and, if it is set to the single-cycle microinterpret, a microinstruction clears the MINT flip-flop. When this flip-flop is cleared, the microcontrol is returned to its normal state and loops on all zeros. At the completion of the store request in progress, the contents of the SIR are loaded to the MAR to begin the next OP code cycle. If TR1 $\neq$ 1, then a multiple-cycle microinterpret is assumed. Each time the main memory fetches a new microinstruction, the contents of the SIR are gated to the MIR and the cycle is repeated. The termination of the multiple-cycle microinterpret is indicated by clearing the MINT flip-flop. This is accomplished by having the last microinstruction of a microinterpret multiple sequence clear it.

When a microinstruction is performed by microinterpret, the two 4-out-of-8 codes representing that instruction are gated from the SIR to the MIR TO and FROM fields. This gating takes place only once. It is coincident with the reading of the contents of the microstore word located at address "1." Address "1" is unique in that it contains all zeros in its TO and FROM fields. As a result, the contents of SIR can be gated into the MIR TO and FROM fields. In this way, a gating signal need only be applied to the SIR, and no new circuitry or critical timing is required to gate the control fields into the MIR itself, as shown in Fig. 16. Note that a delay of 1 microcycle is required from the time the completion signal is given (i.e., DR = 1) to the time the gating is enabled from the SIR to the MIR. The all-zeros location cannot contain all zeros in its TO and FROM fields since the ALL ZEROS is used as a looping address to await main-memory completions. All zeros in the TO and FROM fields would cause the 4-out-of-8 checker to indicate an error, stopping the processor.

The operation of the microinterpret instructions is also self-checking. It must sequence properly and provide valid 4-out-of-8 codes to the TO and FROM fields or the already-described check circuits will fire.

6.6 Maintainability

One of the most beneficial results of microprogram control design from a maintenance aspect is the absence of complex timing circuitry.

The clock consists of only an oscillator and a simple circuit to generate four clock phases. In addition, these clock phases are used almost entirely within the microcontrol itself. Use within the microcontrol is limited for the most part to gating or strobing data and control information into the MAR, MIR, and RAR registers. The loss of these gating pulses will typically cause the contents of the affected register cells to be stuck in a "1" or "0" state, resulting in immediate fault conditions in the check circuit monitoring these registers and their outputs. This is contrasted to a conventional machine that uses complex timing and clock pulses to avoid race conditions and the like in such areas as the command decoder. In addition, in a conventional machine, the clock is typically distributed throughout the entire processor, making fault analysis difficult. If a fault does occur in a clock phase that is designed to eliminate spikes or race conditions, the problem of fault diagnosis becomes very difficult. A fault of this kind is hard to reproduce consistently and may clude the diagnostic programmer because of its possible transient nature. In addition to the simplified clocking scheme, the inherent regular structure of a microprogram control machine lends itself not only to a self-checking philosophy but also to the diagnosis of the fault.

VII. LOGIC IMPLEMENTATION OF THE MICROCONTROL

The microcontrol is contained on eleven 1A-type logic-circuit packs. A total of 2948 gates are used to implement the microcontrol. Of these, 1158 gates are used in the microinstruction decoders and the check circuits. The remaining 1790 gates are used to design the sequencing logic and its check circuits. Approximately 30 percent of the gates in both the decoders and sequencing logic are associated with check logic. The 2948 gates used in the microcontrol represent approximately 20 percent of the total gates used in the processor.

The standard processor will use approximately one-quarter of the microstore's maximum address space (4K* 32-bit words). These 1K words are used as follows:

Function	Words
Implementation of the OP code set	560
Central control (man-machine interface) panel function	200
Initialization sequencing	75
Initial program load from bulk storage	125
Interrupt handling function	60

* $K \cong 1024$.

VIII. ADVANTAGES OF THE MICROPROGRAM CONTROL DESIGN

The use of microprogram control in this processor provides the following advantages:

    (*i*) A uniform processor architecture. This uniformity is very amenable to the self-checking design incorporated into the processor complex.

    (*ii*) An easily maintainable processor. The microprogram control design allows external access via a maintenance channel with a minimal amount of circuitry. Access at the most elementary level of control of the processor provides diagnostic access to the entire machine.

    (*iii*) A very flexible design. This flexibility is present in many aspects of the processor design. Some of this flexibility is the capability to easily change control features; some of it is the ease in which complex control sequences are incorporated into the micro-control itself. For example, there are

        (1) An easily changed macro-level instruction set.
        (2) Speed-independent interfaces to main memory and to peripheral units.
        (3) An extensive and complete interrupt structure that can be adapted to each application.
        (4) A complex and yet versatile initialization procedure.
        (5) A powerful and easily maintainable console panel.

    (*iv*) Easy integration into an ESS environment to provide a system that can immediately detect faults, recover quickly from them, and then provide the necessary diagnostic access and repair.

IX. ACKNOWLEDGMENTS

APPENDIX A

I/O and Its Microcontrol Interface

The interface between the processor and its periphery is primarily performed by serial I/O channels. The interface between the micro-

control and the autonomous circuitry that controls the i/o sequencing is described in the subsequent paragraphs.

The i/o control for the processor consists of expandable, semi-autonomous, functional units called i/o main channels. The architecture of the processor provides the ability to add as many as 20 i/o main channels. Figure 17 shows a single i/o main channel and the major data paths that connect it to the processor. A favorable attribute of the interconnections between the processor and the i/o main channels is the relatively loose coupling between them. Within the processor, three general registers, R9, R10, and R11, provide interface with i/o channels. R9 and R10 send control and data, respectively, to the channels. R11 receives data from the channels. The direct outputs of registers R9 and R10 are presented directly to the i/o channels.

The channel select (cs) field of R9 selects which one of the 20 main channels is to be enabled. The decoding of this 3-out-of-6 channel select results in gate cs becoming enabled. Once a main channel is enabled, microinstruction enables the low-order 12 bits of R9 to be gated into the selected i/o status (ios) register. Similarly, another microinstruction enables R10 to be gated into the i/o data (iod) register. The advantage of such a gating scheme is that the timing problem in the interface is greatly simplified. That is, R9 and R10 can be loaded with a normal register-to-register gating instruction and on subsequent microcycles, microinstructions can be used to gate the contents of these registers in the selected i/o main channel. In this way, as soon as R9 and R10 are loaded, the data ripples out to the designated i/o channel. Then, when the microinstruction that gates these registers into the channel becomes active, the data are stable at the input to the designation point. In an analogous way, the output of the iod of the selected channel is gated into R11 with a miscellaneous decoder crosspoint. Elimination of the timing problem also means that the variability of the fanout, seen when i/o main channels are added, does not pose a problem. The flexibility afforded by this gating scheme and the use of microprogram control also facilitate the design of completely different i/o interfaces, such as a parallel-to-parallel interface rather than the standard parallel-to-serial.

The actual operation of the channel consists of loading the ios and the iod and then issuing a microinstruction crosspoint that starts the autonomous sequencing. It should first be noted that each main channel consists of 20 subchannels which provide fanout to the peripheral units and time-share the control and sequencing logic of the main channel. The sequencing consists of shifting the data loaded into the iod, together with a start code that is prefixed onto the front of the message, and into a serial data link. The serial message is transmitted
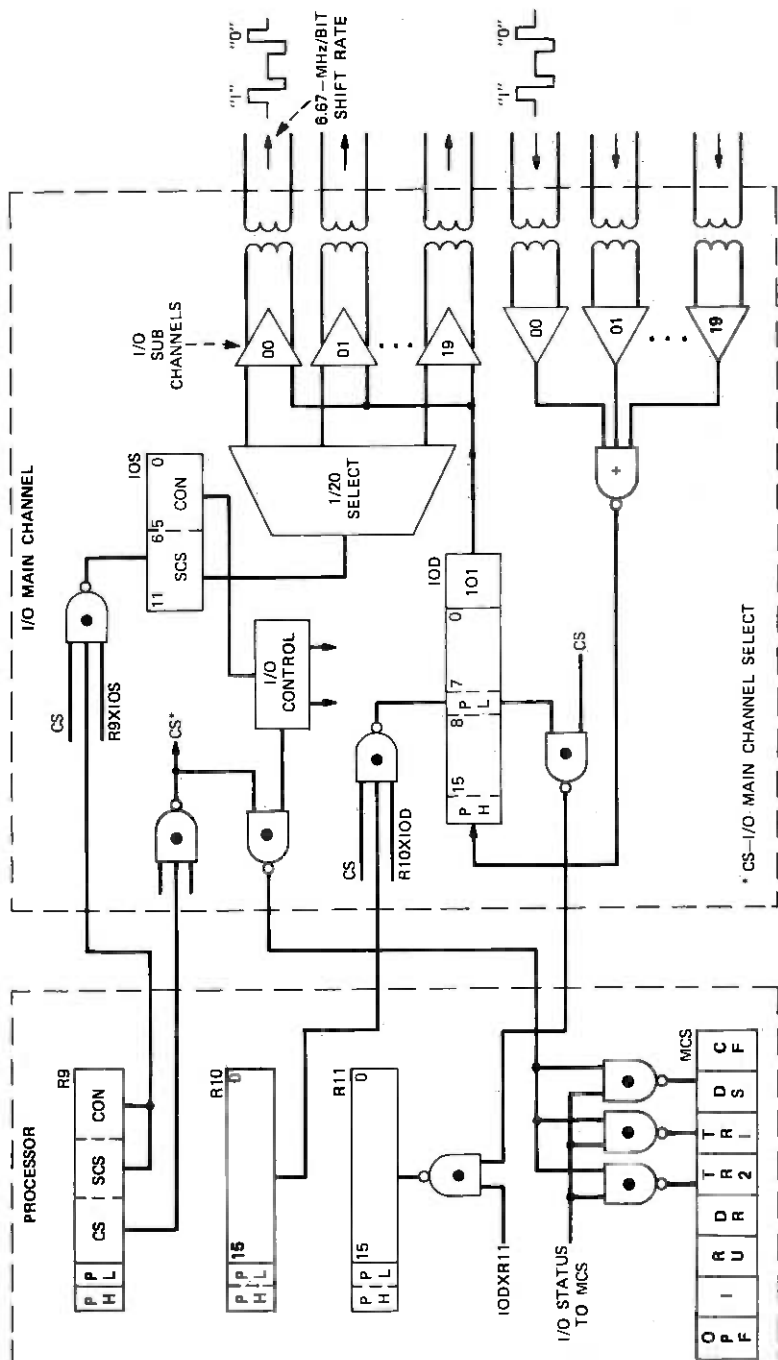
Fig. 17—I/O interface.

on the serial data link using a phase-encoded bit stream (6.67 MHz per bit) so that a separate clock signal is not required at the receiving end. Once the message has been shifted out of the 21-bit IOD, the I/O control continues to send a pulse stream out on the serial link. This pulse stream is used to provide the timing information for the peripheral unit and is required to send a response message back to the sending I/O channel. Therefore, as soon as the outgoing data are shifted out, the I/O control begins to monitor the incoming port. When a leading one is detected on the incoming message, the I/O control stops and sets a flag which the processor can interrogate. The processor can either return to executing other instructions or it can go into a loop, testing the completion flag just described. The microcontrol actually tests the state of the I/O channel by again using a microinstruction to gate the output of three states of the channel directly to the MCS register.

In the processor design, self-checking was achieved by partitioning the logic to obtain certain failure modes so that the check circuits could ensure fault detection. In instances where this partitioning became an unworkable solution, duplication was used, such as for the DML. For the implementation of the I/O channels, it is impractical to partition the logic to force single bit errors; however, it is also not economical to duplicate the channels. Three solutions were used to solve the detection problem. First, m-out-of-n codes were used in the control fields. Second, a loop-around test is performed on the data paths. Third, the parity check code carried with data within the processor is transmitted to and from the periphery as well. The m-out-of-n codes are checked using the same method as for the TO and FROM codes in the processor. The data check is performed by gating R10 to IOD and then returning the IOD to R11. Then a match is performed between R10 and R11 using the DML match hardware as previously outlined. This matching technique results in trading speed for hardware. Since the overhead for performing the match does not represent a significant real-time penalty, the choice is well justified. Parity is checked when data are received at the peripheral units and also when data are returned to the processor, as previously described.

APPENDIX B

MAR-RAR Matching

When the microprogram control was designed, an analysis was done to determine the type of faults that were most probable. Check schemes were then designed to detect these faults. A complete report of this work is given in Ref. 10. One of the areas of the microcontrol where it was difficult to use coding techniques to detect multiple faults was in the sequencing logic. That is, it would be disadvantageous to use any-

thing other than a normal binary code to implement microstore addressing. As outlined in the reference, a check of the binary decoding of the address in the microstore address register (MAR), the access of the correct word in the microprogram store, and the proper readout are performed by using a simple parity check scheme and by interleaving binary-encoded words with m-out-of-n encoded words in the microprogram store.

However, to ensure that the proper address is loaded into the MAR, duplication is required for detection. The amount of hardware required to implement the duplication is minimized by time-sharing some circuitry. As a result, only the addition of an 11-bit matcher was required to perform the duplication-and-match function.

The hardware involved and the data flow are indicated in Fig. 18. As described in the section on microcontrol sequencing, when a new OP code is loaded from the SIR, it is gated into IB, MAR, and into RAR. The OP code is loaded into the IB because the operand fields X and Y are normally used directly by means of the translators attached to the outputs of the IB. The OP code is loaded into the MAR to access the first word of the microsequence for that OP code. The OP code is loaded into
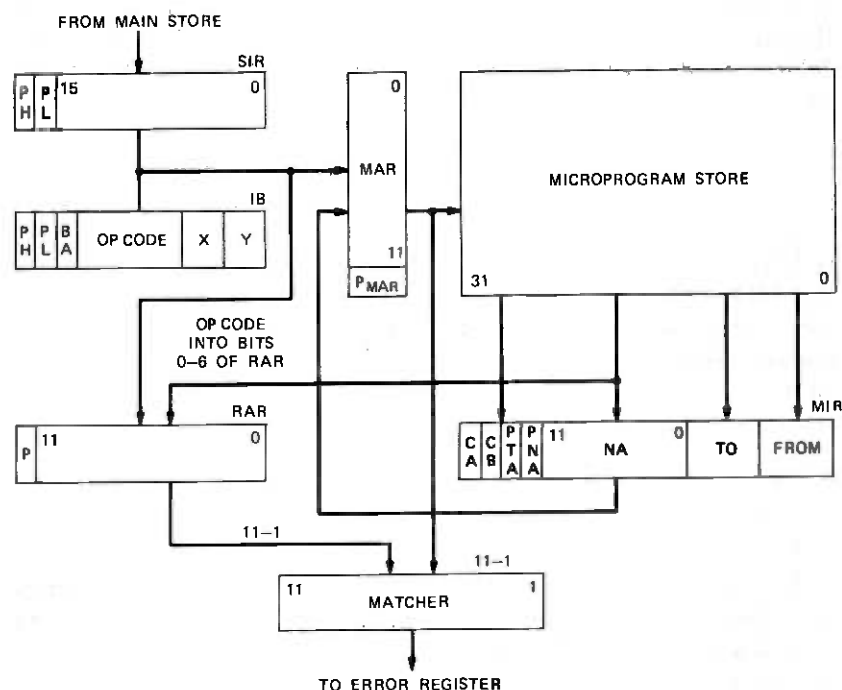
Fig. 18—MAR-RAR matching.

RAR to check that the OP code is correctly loaded into the MAR. This is achieved by the matcher being placed between the outputs of the MAR and RAR. The reason for duplication and matching is that it is not possible to predict the type of multiple fault that might exist when loading the MAR if it is not bit-sliced. The SIR and the IB are bit-sliced. Therefore, any multiple fault within a single bit-sliced circuit pack will be guaranteed to cause a parity failure if the data are indeed in error. For the MAR and MIR, it is not economical or, for that matter, practical to bit-slice them. Thus, the bit-slicing of the SIR and its parity check code together with the duplication and matching of the MAR provide a complete check on the loading of the new OP code into the MAR.

As each word is accessed and read out of the microstore, it is gated into the MIR. The NA field of the MIR is then gated into MAR. To check that this gating is correct, the NA field when gated out of the microstore is also gated into the RAR. As a result, a match can again be performed between the MAR and RAR to check for error-free operation. This same technique of loading the RAR with the same contents as the MAR is performed for indexing and loading the interrupt constant, the MRF constant, and the STOP constant.

Note that the match is performed only over bits 1 through 11 of the MAR and RAR. This simplifies implementation because of the number of operations that can change the state of bit 0. For example, conditional transfers alone have nine different ways of jamming bit 0 to a 1. The result is that the RAR is loaded exactly the same way for conditional transfers as for the normal sequencing case, and again the match is performed. If bit 0 is in error, the parity check on the sequencing will detect it.

The data and auxiliary control sequencing cases are slightly different. As described in Section 5.3, the next address for these commands is obtained by saving the previous contents of the MAR and jamming a 1 into bit 0. The fact that the address presently residing in the MAR was checked when first loaded into the MAR simplifies the design. The CA bit, which, when equal to 1, indicates either a data or auxiliary control is to be performed, is also used to inhibit the MAR-RAR matching for that cycle since the RAR has data in it for these two cases. Since data are loaded into the RAR as well as into the MIR (NA) field for a data command, a subroutine return can be easily implemented as described in Section 5.2. During the subroutine, the MAR-RAR matching is disabled. As a result, if a sequencing error occurred during a subroutine, it may go undetected for a few microcylces. However, as soon as the microcontrol exits the subroutine and returns to the update mode (RU = 1), the matching will again be enabled and a "stuck at fault" will quickly be detected.

GLOSSARY

AR	General-purpose buffer register in the DML logic	MCS	Microcontrol status
BA	Branch allowed	MINT	Microinterpret
BIN	Block interrupts	MIR	Microinstruction register
BR	General-purpose buffer register in the DML logic	MMS	Main-memory state
		MRF	Maintenance reset function
CA⎱ CB⎰	Control bits	NA	Next address
		NOP	Null microinstruction
CC	Central control	PA	Program address
DB	Display buffer	PBC	Processor's bus controller
DML	Data-manipulation logic	PMAR	Parity for the MAR
DR	Data ready	PNA	Parity bit with next-address field
FN	Function register		
GB	Gating bus	PTA	Parity of the accessed location
IB	Instruction buffer		
I.D	Instruction or data	RAR	Return address register
IM	Interrupt mask	REQ	Request
I/O	Input/output	ROM	Read-only memory
IOD	I/O data register	R.W	Read or write
IOS	I/O status register	RU	RAR update
IS	Interrupt set	SAR	Store address register
MAR	Microstore address register	SDR	Store data register
		SIR	Store-instruction register
MCH	Maintenance channel		

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Temperature Rise at a Constriction in a Current-Carrying Printed Conductor

By A. J. RAINAL

This paper presents some basic equations for predicting the maximum temperature rise at an isolated constriction in a current-carrying printed conductor. The equations apply to general configurations of printed conductors, since they are based on the heat equation in the steady state. A variety of numerical results concerning the maximum temperature rise and the runaway or critical current are presented in tables for the case of printed conductors of nominal widths 8, 25, and 100 mils. The numerical results include the case of 1-, 2-, and 3-oz copper conductors at an ambient temperature of 20 or 50°C. A few experimental results are presented which show that the numerical results concerning the maximum temperature rise are conservative from the point of view of design. The results are useful for determining whether an isolated constriction in a printed conductor is of any significance. Also, the results can be used to help develop rational criteria for rejecting printed conductors when isolated nicks are present.

I. INTRODUCTION

During the design and manufacture of printed conductors to interconnect electrical circuits, one is often confronted with the task of determining whether an isolated constriction in a printed conductor is of any significance. A constriction is sometimes designed into a printed conductor to help alleviate some particular routing problem. Also, during the manufacturing process, such a constriction can arise in the form of an isolated nick in the printed conductor.

In general, the maximum allowable temperature rise at the isolated constriction imposes definite limits on the allowable dimensions of the constriction. The relationship between the dimensions of the isolated constriction and the maximum temperature at the constriction is useful for both design purposes and for determining the maximum allowable nick in a printed conductor. As the maximum allowable nick in a printed conductor is increased, the manufacturing yield increases and the time necessary to visually examine the printed conductor decreases. Thus, the cost of manufacturing printed wiring boards can perhaps be decreased by increasing the maximum allowable nick.

W = WIDTH OF CONDUCTOR
W_C = WIDTH OF CONSTRICTION
L = LENGTH OF CONDUCTOR
L_C = LENGTH OF CONSTRICTION
T_1 = AMBIENT TEMPERATURE

ΔT_C (X) = TEMPERATURE DIFFERENCE (WITH RESPECT TO AMBIENT) AT THE CONSTRICTION
I = CURRENT FLOW
R', R'_C = RESISTANCE PER UNIT LENGTH AT AMBIENT TEMPERATURE

Fig. 1—A current-carrying printed conductor constricted in the middle and constrained to the ambient temperature at both ends.

The purpose of this paper is to develop some basic equations that are useful for predicting the maximum temperature rise at an isolated constriction in a current-carrying printed conductor. Figure 1 presents a sketch of an isolated constriction and some notation used in this paper. We only consider the problem of characterizing the steady-state thermal behavior of a current-carrying printed conductor that may contain a constriction. Some constrictions may produce such effects as impedance changes and mechanical vulnerability, and these are not considered in this paper.

II. BASIC EQUATIONS

Consider the partitioning of the x axis in Fig. 1 into the following three intervals:

$$\left[-\frac{L}{2}, -\frac{L_0}{2} \right], \quad \left[-\frac{L_0}{2}, \frac{L_0}{2} \right], \quad \text{and} \quad \left[\frac{L_0}{2}, \frac{L}{2} \right].$$

Let $T(x)$ denote the temperature distribution along the current-carrying conductor. In the steady state, the temperature difference $\Delta T(x) = [T(x) - T_1]$ in the first and last intervals must satisfy the linear differential equation[1] (a one-dimensional heat equation) of the form:

$$\frac{d^2 \Delta T}{dx^2} - \frac{2H \Delta T}{kt_0} + \frac{I^2 R'[1 + \alpha_1 \Delta T]}{kW t_0} = 0, \tag{1}$$

where

H^* = coefficient of surface heat transfer
k = thermal conductivity of the conductor
t_0 = thickness of the conductor
I = current flow

---

* We shall follow Ref. 1 and denote the coefficient of surface heat transfer by the letter H. However, many other references use the letter h.

R' = resistance of the conductor per unit length at ambient temperature

α_1 = temperature coefficient of resistivity of the conductor at ambient temperature

W = width of the conductor.

The second derivative in eq. (1) represents the rate of heat accumulation per unit volume. The negative term in eq. (1) accounts for the heat "radiated" per unit volume from both the top and bottom surfaces of the conductor.[*] The term involving the current I represents the heat generated per unit volume.

At the isolated constriction, the temperature difference $\Delta T(x)$ must satisfy an equation similar to eq. (1) except that W and R' are replaced by W_c and R'_c, respectively. Equation (1) has been applied to the case when the constriction is absent in Refs. 1 and 2.

After the boundary conditions are imposed that $\Delta T(x) = 0$ when $x = \pm L/2$, and $\Delta T(x)$ and its derivative[†] are matched at the two discontinuities located at $x = \pm L_c/2$, one can solve for the temperature difference in the region of the constriction which we shall denote as $\Delta T_c(x)$. The explicit result is that

$$\Delta T_c(x) = \frac{\gamma_1^2}{\beta_1^2}$$

$$- \frac{\{(\gamma^2/\beta^2)\,\text{sech}\,[(\beta/2)(L - L_c)] + [(\gamma_1^2/\beta_1^2) - (\gamma^2/\beta^2)]\}\cosh\beta_1 x}{(\beta_1/\beta)\sinh(\beta_1 L_c/2)\tanh[(\beta/2)(L - L_c)] + \cosh(\beta_1 L_c/2)},$$

(2)

where

$$\gamma_1^2 = \frac{\rho}{k}\left(\frac{I}{W_c t_0}\right)^2$$

$$\gamma^2 = \frac{\rho}{k}\left(\frac{I}{W t_0}\right)^2$$

$$\beta_1^2 = \frac{2HW_c - \alpha_1\left(\dfrac{\rho}{W_c t_0}\right)I^2}{kW_c t_0}$$

$$\beta^2 = \frac{2HW - \alpha_1\left(\dfrac{\rho}{W t_0}\right)I^2}{kW t_0}$$

k = thermal conductivity of the conductor

ρ = resistivity of the conductor at ambient temperature.

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[*] In general, the amount of heat radiated from the top and bottom surfaces of the conductor will differ because of the substrate. This difference can be absorbed in the definition of the coefficient of surface heat transfer, H.

[†] Matching the derivative assures that the rate of heat accumulation per unit volume is finite for all x (see Ref. 1, page 4).

The solutions in the other regions of the x axis can be obtained in a similar manner. However, they are not of interest in this paper, and they are not presented here.

The maximum temperature difference, max ΔT_c, at the constriction occurs at $x = 0$; thus,

$$\text{max } \Delta T_c = \Delta T_c(0).\tag{3}$$

In the absence of a constriction, $L_c = 0$, the maximum temperature difference, max ΔT_{c0}, is given by

$$\text{max } \Delta T_{c0} \equiv \text{max } \Delta T_c\Big|_{L_c=0} = \frac{\gamma^2}{\beta^2}\left[1 - \text{sech}\left(\frac{\beta L}{2}\right)\right].\tag{4}$$

This latter result is convenient for normalization purposes.

III. SOME SPECIAL CASES

3.1 Longest possible constriction

When $L_c = L$, eq. (2) yields

$$\Delta T_c(x) = \frac{\gamma_1^2}{\beta_1^2}\left[1 - \frac{\cosh \beta_1 x}{\cosh\left(\dfrac{\beta_1 L}{2}\right)}\right].\tag{5}$$

This latter equation agrees with the result in Refs. 1 and 2.

3.2 Thermal runaway at the constriction

If the current flow through a printed conductor increases above a value called the critical current, I_c, thermal runaway results. That is, the temperature of the printed conductor increases beyond the tolerable limits of the substrate and permanent damage results. This phenomenon is discussed in Refs. 2 and 3. Let us now determine the value of I_c for a printed conductor having a constriction.

In the case of the longest possible constriction, eq. (5) shows that max $\Delta T_c = \Delta T_c(0)$ increases without bound only when $\beta_1^2 < 0$. If we set $\beta_2^2 = -\beta_1^2 > 0$, we find that max ΔT_c increases without bound when

$$\frac{\beta_2 L}{2} = \frac{\pi}{2}\tag{6}$$

or

$$I = W_c\sqrt{\frac{2Ht_0 + (\pi/L)^2 k t_0^2}{\alpha_1 \rho}}\tag{7}$$

In the absence of a constriction, eq. (4) shows that max ΔT_{c0} can increase without bound only when $\beta^2 < 0$. If we set $\beta_3^2 = -\beta^2 > 0$, we find that max ΔT_{c0} increases without bound when

$$\frac{\beta_3 L}{2} = \frac{\pi}{2}\tag{8}$$

or

$$I = W \sqrt{\frac{2Ht_0 + (\pi/L)^2 kt_0^2}{\alpha_1 \rho}}. \tag{9}$$

Thus, when the length of the constriction is bounded by $0 \leq L_c \leq L$, the runaway or critical current I_c must be bounded by

$$W_c \sqrt{\frac{2Ht_0 + (\pi/L)^2 kt_0^2}{\alpha_1 \rho}} \leq I_c \leq W \sqrt{\frac{2Ht_0 + (\pi/L)^2 kt_0^2}{\alpha_1 \rho}}. \tag{10}$$

The value of I_c can be found by setting $\beta_2^2 = -\beta_1^2 > 0$ in eq. (2) and solving for the current I which makes max $\Delta T_c = \Delta T_c(0)$ increase without bound. The result is that the critical current I_c equals the value of I that satisfies the transcendental equation

$$\frac{\beta_2}{\beta} \tan \left(\frac{\beta_2 L_c}{2} \right) \tanh \left[\frac{\beta}{2} (L - L_c) \right] = 1. \tag{11}$$

Some numerical results obtained from eqs. (2), (3), (4), and (11) are presented in Section 5.1.

3.3 Small * current flow in a long conductor

As $I \to 0$ and $L \to \infty$, eq. (2) yields

$$\Delta T_c(x) = \frac{\gamma_1^2}{\beta_1^2} - \left(\frac{\gamma_1^2}{\beta_1^2} - \frac{\gamma^2}{\beta^2} \right) \exp \left(-\frac{\beta_1 L_c}{2} \right) \cosh \beta_1 x. \tag{12}$$

Also, as $I \to 0$ and $L \to \infty$, eqs. (3), (4), and (12) yield the interesting relationship

$$\frac{\max \Delta T_c}{\max \Delta T_{c0}} = \left(\frac{W}{W_c} \right)^2 - \left[\left(\frac{W}{W_c} \right)^2 - 1 \right] \exp \left[-\frac{L_c}{2} \sqrt{\frac{2H}{kt_0}} \right]. \tag{13}$$

Some numerical results obtained from eq. (13) are presented in Section 5.2.

3.4 Effects of the ambient temperature †

Equation (2) shows that the temperature difference $\Delta T_c(x)$ at the constriction depends on the ambient temperature T_1, since both α_1 and ρ depend on T_1. However, a somewhat unexpected result is that the critical current I_c, as defined by (11), is independent of the ambient temperature T_1. This result follows from the fact that both β^2 and $\beta_2^2 = -\beta_1^2$ are independent of T_1, since they are functions of the product $\alpha_1 \rho$. This product is independent of T_1 as can be verified by using the temperature-dependent expressions for α_1 and ρ given in Table II in the appendix.

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* "Small" refers to currents that are less than about $(W_c/4) \sqrt{2Ht_0/\alpha_1 \rho}$.
† In this paper, we are mainly interested in an ambient temperature, T_1, in the range $|T_1| \leq 50°C$.

In a very similar manner, one can show that the ratio max $\Delta T_c/$ max ΔT_{c0} is also independent of the ambient temperature T_1, while the value of max ΔT_{c0} depends on the ambient temperature T_1.

It is difficult to predict these effects of the ambient temperature without a mathematical argument, because, as the ambient temperature T_1 increases, ρ increases while α_1 decreases.

IV. THE COEFFICIENT OF SURFACE HEAT TRANSFER, H, FOR A PRINTED CONDUCTOR

4.1 Theoretical expression for H

Consider the case when $L \gg W$. For this case, the maximum temperature, max ΔT_{c0}, in the absence of a constriction is approximately equal to the average temperature rise, $\overline{\Delta T}$, along the current-carrying conductor. Thus, by equating eq. (4) to the theoretical expression for $\overline{\Delta T}$, which was presented in Ref. 3, we have

$$\frac{\gamma^2}{\beta^2} = \frac{I^2 R_1 R_T}{1 - I^2 R_1 R_T \alpha_1}, \tag{14}$$

where

$R_1 = \rho L / W t_0 =$ resistance of the conductor at ambient temperature
$R_T =$ thermal resistance of the conductor.

Equation (14) yields

$$H = \frac{1}{2 W L R_T}. \tag{15}$$

Reference 3 also presents a theoretical expression for the thermal resistance R_T as

$$R_T = \frac{1}{2\pi k_m L} \ln\left(\frac{4L}{W}\right), \tag{16}$$

where

$k_m =$ thermal conductivity of the medium surrounding the conductor.

Equations (15) and (16) yield a theoretical expression for H as

$$H = \frac{\pi k_m}{W \ln (4L/W)}. \tag{17}$$

Since we have assumed that $L \gg W$, eq. (17) shows that H is, approximately, inversely proportional to W. This inverse behavior together with eq. (13) shows that, as $I \to 0$ and $L \to \infty$, max $\Delta T_c/$max ΔT_{c0} remains constant when

$$\frac{W_c}{W} = \text{constant} \tag{18}$$

and

$$\frac{L_c}{\sqrt{W_c t_0}} = \text{constant}. \tag{19}$$

4.2 Experimental value of H

Some recent work[4] concerning the current-carrying capacities of various remreed backplane designs contains a table which gives the measured thermal resistances R_T for a pair of parallel printed conductors. The conductors were each about 12-in. long and 8 mils wide, and they were spaced 9 mils apart. For this particular conductor configuration, $R_T{}^*$ turned out to be about 10°C/watt. By applying eq. (15) to this conductor configuration, we have

$$H = \frac{1}{2W_t L R_T} = \frac{1}{(2)(25)(12{,}000)10} = \left(\frac{1}{6}\right) 10^{-6} \frac{\text{watts}}{\text{mil}^2\,{}^\circ\text{C}}, \quad (20)$$

where

W_t = total "radiating" width of the parallel conductor configuration = 25 mils.

This particular value of H, and some scaled values based on $H \sim 1/W$, will now be used to obtain some numerical results.

V. NUMERICAL RESULTS

Tables I through XXVI are presented in Appendix A[†] of this paper. To help ease the task of locating the numerical results pertaining to a specific set of parameters, Table I contains a listing of the contents of all the numerical tables appearing in the appendix. For example, Table I indicates that Table II contains the parameter values that were used to obtain all the numerical results presented in this paper.

5.1 The general case [eqs. (2), (3), (4), (11)]

Tables III through V present values of the critical currents, I_c, as computed from eq. (11). For example, Table III shows that, for the case $t_0 = 2.8$ mils (2-oz Cu), any T_1, $W = 6$ mils, $W_c/W = 0.5$, $L_c = 4W = 24$ mils, and $L = 12{,}000$ mils, the critical current I_c is about 6.1 A. If a current greater than the critical current is applied, max ΔT_c will increase without bound until permanent damage of the substrate results.

Tables VI, VII, and VIII present the values of max ΔT_{c0} as computed from eq. (4). For example, Table VI shows that, for the case of $t_0 = 2.8$ mils, $T_1 = 50$°C, $W = 6$ mils, $L = 12{,}000$ mils, and $I = 2$ amperes, the maximum temperature difference in the absence of a constriction, max ΔT_{c0}, is about 32°C. This result agrees well with the corresponding result given in Table VIII of Ref. 4, when one takes into

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[*] The value of R_T varies somewhat depending on the type of covercoat, the type of substrate (rigid or flex), and the presence or absence of cooling lines. A detailed tabulation is given in Table 1 of Ref. 4.

[†] The numerical results presented in the appendix contain a few more decimal places than accuracy considerations justify. These additional decimals are useful for comparing the numerical evaluations resulting from eqs. (2) and (13).

account eq. (10) of Ref. 3, which implies that a current flow of 2 A in a single conductor produces the same temperature rise as a current flow of $\sqrt{2}$ A in both the tip and ring conductors of the remreed backplane.

Tables IX through XXIII present the values of the ratio max ΔT_c/max ΔT_{c0} as computed from eqs. (2), (3), and (4). For example, Table XIII shows that, for the case of $t_0 = 2.8$ mils, any T_1, $W = 6$ mils, $W_c/W = 0.5$, $L_c = 4W = 24$ mils, $L = 12,000$ mils, and $I = 2$ A, the ratio max ΔT_c/max ΔT_{c0} is about 1.23. Since, in the absence of a constriction, the maximum temperature difference, max ΔT_{c0}, was seen to be about 32°C when $T_1 = 50$°C, the maximum temperature difference at this constriction, max ΔT_c, is about $(1.23)(32) = 39.4$°C, above the ambient temperature of $T_1 = 50$°C.

5.2 The special case [$I \to 0$, $L \to \infty$, eq. (13)]

Tables XXIV, XXV, and XXVI present the values of the ratio max ΔT_c/max ΔT_{c0} as computed from eq. (13). For example, Table XXIV shows that, for the case $t_0 = 2.8$ mils, $W = 6$ mils, $W_c/W = 0.5$, and $L_c = 4W = 24$ mils, the ratio max ΔT_c/max ΔT_{c0} is about 1.21. This value agrees with the more accurate value 1.23 given above for the case $I = 2$ A in spite of the fact that this current is not really small.

In general, by comparing the numerical results for the special case (Tables XXIV, XXV, and XXVI) with the corresponding numerical results for the general case (Tables IX through XXIII), one can verify that the results for the special case serve as good approximations for a wide variety of parameter values. Notice that the numerical entries in Tables XXV and XXVI are identical in accordance with eqs (18) and (19).

VI. A FEW EXPERIMENTAL RESULTS

To obtain some experimental confirmation concerning the numerical results presented in the tables, a few experiments were performed on 2- and 3-oz copper conductors (no covercoat) having the approximate dimensions of $W = 30$ mils, $W_c/W = 0.5$, $L_c = 4W = 120$ mils, and $L = 8000$ mils. In these experiments, the maximum temperature difference, max ΔT_c, at the constriction was estimated by observing the behavior of a thin coating of temperature-indicating paint of known melting temperature T_m. When the indicating paint first began to melt, the average temperature difference $\overline{\Delta T}$ along the current-carrying conductor was measured by using the resistance thermometer method described in Ref. 3. In this manner, the ratio max ΔT_c/max ΔT_{c0} is given, approximately, by

$$\frac{\max \Delta T_c}{\max \Delta T_{c0}} \doteq \frac{T_m - T_1}{\overline{\Delta T}}. \tag{21}$$

For the 2-oz copper conductor (measured $t_0 = 3.6$ mils), we found that when $T_m = 52°C$, and $T_1 = 26.5°C$, a current flow of 2.75 A for a duration of 5 min produced an average temperature difference, $\overline{\Delta T}$, of 17.7°C when the indicating paint first began to melt. Thus,

$$\frac{\max \Delta T_c}{\max \Delta T_{c0}} \doteq \frac{52 - 26.5}{17.7} = 1.44. \tag{22}$$

This experimental value is somewhat smaller than the corresponding value extrapolated from Tables XVI and XVII, which is about 1.52.

Similarly, for the case of the 3-oz copper conductor (measured $t_0 = 4.9$ mils), we found that, when $T_m = 52°C$ and $T_1 = 26°C$, a current flow of 3.5 A for a duration of 5 min produced an average temperature difference, $\overline{\Delta T}$, of 19.7°C when the indicating paint began to melt. Thus,

$$\frac{\max \Delta T_c}{\max \Delta T_{c0}} \doteq \frac{52 - 26}{19.7} = 1.32. \tag{23}$$

This experimental value is again somewhat smaller than the corresponding value extrapolated from Tables XVII and XVIII, which is about 1.42.

Thus, it appears that the numerical values of $\max \Delta T_c / \max \Delta T_{c0}$ presented in the tables are conservative from the point of view of design.

VII. SOME APPLICATIONS

7.1 Printed conductors of nominal widths 8, 25, 100 mils

The numerical results presented in Tables III through XXVI are useful in helping to determine whether an isolated constriction in a printed conductor is of any significance. For example, if the current flow $I \geq I_c$, the critical current listed in Tables III through V, then permanent damage of the substrate is certain to occur. Also, for the case of a small current flow in a long conductor, Table XXIV indicates that, for an isolated constriction of length $L_c = 4W$ and a constriction width $W_c = 0.5W$ in a fine-line printed conductor of width $W = 6$ mils and a thickness $t_0 = 2.8$ mils (2 oz Cu), the maximum temperature rise at the constriction will be about 1.21 times the maximum temperature rise when the constriction is absent. If a 1-oz copper conductor is used, then the corresponding result is 1.29.

The numerical results presented in the tables and eqs. (18) and (19) can also be used to help determine rational criteria for rejecting printed conductors when isolated nicks are present. If one can tolerate the presence of relatively large nicks in a printed conductor, then the manufacturing yield will increase and the time necessary to visually examine the printed conductors will decrease.

7.2 *Printed conductors of other dimensions*

Although we have only presented numerical results for the sets of parameters listed in Table II, the methods described in this paper also apply to other sets of parameters. The only elusive parameter one needs to determine is the value of H, the coefficient of surface heat transfer. An approximate value of H can be calculated from eq. (17). Also, H can be determined experimentally, as was described in Section 4.2. Finally, the value of H used in this paper can be scaled to other widths by using the approximate law $H \sim 1/W$, which was discussed in Section 4.1. Once the value of H is determined, eqs. (2), (3), (4), and (11) can be applied to obtain numerical results similar to those presented in Tables III through XXIII. Also, for the case of a small current flow in a long conductor, a simplified equation, (13), can be applied to obtain numerical results similar to those presented in Tables XXIV, XXV, and XXVI.

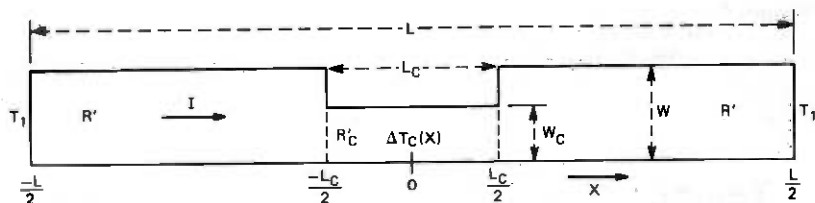## VIII. SUMMARY

This paper presents some basic equations for predicting the maximum temperature rise at an isolated constriction (e.g., a nick) in a current-carrying printed conductor. A transcendental equation is also presented which can be used to predict the thermal runaway or critical current. The equations apply to general configurations of printed conductors, since the underlying differential equation is the heat equation in the steady state. Numerical results depend on a number of parameters which are readily available, and the value of the coefficient of surface heat transfer H. An equation is presented that can be used to estimate the value of H for a relatively long conductor. A method is also described for determining the value of H experimentally. H was measured to be about $(1/6)10^{-6}$ watts/mil^2°C for a 25-mil-wide printed conductor. Based on this value of H, a variety of numerical results concerning the critical current and the maximum temperature rise at the constriction are presented in tables. A few experimental results are presented which show that the numerical results concerning the maximum temperature rise are conservative from the point of view of design. The results in this paper are useful for determining whether an isolated constriction in a printed conductor is of any significance. The results can also be used to help determine rational criteria for rejecting printed conductors when isolated nicks are present.

IX. ACKNOWLEDGMENTS

The author also wishes to thank D. E. McCumber for many stimulating discussions concerning appropriate boundary conditions, and his preliminary results for the more difficult, two-dimensional analysis of this problem.

APPENDIX A

Numerical Results

Table I — Contents of the numerical tables

Table No.	Contents
II	Parameter values
III	Values of critical currents, I_c, for $W = 6, 8, 10$, and all W_c/W, L_c, L, t_0, T_1
IV	Values of critical currents, I_c, for $W = 20, 25, 30$, and all W_c/W, L_c, L, t_0, T_1
V	Values of critical currents, I_c, for $W = 80, 100, 120$, and all W_c/W, L_c, L, t_0, T_1
VI	Values of max ΔT_{c0} for $W = 6, 8, 10$, and all I, L, t_0, T_1
VII	Values of max ΔT_{c0} for $W = 20, 25, 30$, and all I, L, t_0, T_1
VIII	Values of max ΔT_{c0} for $W = 80, 100, 120$, for all I, L, t_0, T_1
IX	Values of (max ΔT_c/max ΔT_{c0}) for $W = 6, 8, 10$, $I = 0.1$, and all W_c/W, L_c, L, t_0, T_1
X	Values of (max ΔT_c/max ΔT_{c0}) for $W = 6, 8, 10$, $I = 0.5$, and all W_c/W, L_c, L, t_0, T_1
XI	Values of (max ΔT_c/max ΔT_{c0}) for $W = 6, 8, 10$, $I = 1.0$, and all W_c/W, L_c, L, t_0, T_1
XII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 6, 8, 10$, $I = 1.5$, and all W_c/W, L_c, L, t_0, T_1
XIII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 6, 8, 10$, $I = 2.0$, and all W_c/W, L_c, L, t_0, T_1
XIV	Values of (max ΔT_c/max ΔT_{c0}) for $W = 20, 25, 30$, $I = 0.5$, and all W_c/W, L_c, L, t_0, T_1
XV	Values of (max ΔT_c/max ΔT_{c0}) for $W = 20, 25, 30$, $I = 1.0$, and all W_c/W, L_c, L, t_0, T_1
XVI	Values of (max ΔT_c/max ΔT_{c0}) for $W = 20, 25, 30$, $I = 2.0$, and all W_c/W, L_c, L, t_0, T_1
XVII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 20, 25, 30$, $I = 3.0$, and all W_c/W, L_c, L, t_0, T_1
XVIII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 20, 25, 30$, $I = 4.0$, and all W_c/W, L_c, L, t_0, T_1
XIX	Values of (max ΔT_c/max ΔT_{c0}) for $W = 80, 100, 120$, $I = 1.0$, and all W_c/W, L_c, L, t_0, T_1
XX	Values of (max ΔT_c/max ΔT_{c0}) for $W = 80, 100, 120$, $I = 2.0$, and all W_c/W, L_c, L, t_0, T_1
XXI	Values of (max ΔT_c/max ΔT_{c0}) for $W = 80, 100, 120$, $I = 4.0$, and all W_c/W, L_c, L, t_0, T_1
XXII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 80, 100, 120$, $I = 6.0$, and all W_c/W, L_c, L, t_0, T_1
XXIII	Values of (max ΔT_c/max ΔT_{c0}) for $W = 80, 100, 120$, $I = 8.0$, and all W_c/W, L_c, L, t_0, T_1
XXIV	Values of (max ΔT_c/max ΔT_{c0}) for the special case $I \to 0$, $L \to \infty$, for $W = 6, 8, 10$, and all W_c/W, L_c, t_0, T_1
XXV	Values of (max ΔT_c/max ΔT_{c0}) for the special case $I \to 0$, $L \to \infty$, for $W = 20, 25, 30$, and all W_c/W, L_c, t_0, T_1
XXVI	Values of (max ΔT_c/max ΔT_{c0}) for the special case $I \to 0$, $L \to \infty$, for $W = 80, 100, 120$, and all W_c/W, L_c, t_0, T_1

Table II — Parameter values

Units	Set I	Set II	Set III
mils	$L = 1000, 6000, 12{,}000$	$L = 1000, 6000, 12{,}000$	$L = 1000, 6000, 12{,}000$
mils	$L_c = 2W, 4W, 6W, 8W$	$L_c = W, 2W, 3W, 4W$	$L_c = 0.5W, W, 1.5W, 2W$
mils	$W = 6, 8, 10$	$W = 20, 25, 30$	$W = 80, 100, 120$
dimensionless	$W_c/W = 1, 0.8, 0.75, 0.50, 0.25$	$W_c/W = 1, 0.8, 0.75, 0.50, 0.25$	$W_c/W = 1, 0.8, 0.75, 0.50, 0.25$
$\dfrac{\text{watts}}{\text{mil}^2{}^\circ\text{C}}$	$H = \left(\dfrac{25}{8}\right)\left(\dfrac{1}{6}\right)10^{-6}$	$H = \left(\dfrac{1}{6}\right)10^{-6}$	$H = \left(\dfrac{25}{100}\right)\left(\dfrac{1}{6}\right)10^{-6}$
$\dfrac{\text{watts}}{\text{mil}^\circ\text{C}}$	$k = (1.0338)10^{-2}$	$k = (1.0338)10^{-2}$	$k = (1.0338)10^{-2}$
mils	$t_0 = 4.2, 2.8, 1.4$	$t_0 = 4.2, 2.8, 1.4$	$t_0 = 4.2, 2.8, 1.4$
ohm-mil	$\rho = (0.67878)10^{-3} \cdot [1 + 0.00393(T_1 - 20)]$	$\rho = (0.67878)10^{-3} \cdot [1 + 0.00393(T_1 - 20)]$	$\rho = (0.67878)10^{-3} \cdot [1 + 0.00393(T_1 - 20)]$
per °C	$\alpha_1 = [T_1 + 234.45]^{-1}$	$\alpha_1 = [T_1 + 234.45]^{-1}$	$\alpha_1 = [T_1 + 234.45]^{-1}$
°C	$T_1 = 20, 50$	$T_1 = 20, 50$	$T_1 = 20, 50$
amperes	$I = 0.1, 0.5, 1.0, 1.5, 2.0$	$I = 0.5, 1, 2, 3, 4$	$I = 1, 2, 4, 6, 8$

Table III — Values of critical currents I_c

$T(Q) = 4.2$ — $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	W=6.00					W=8.00					W=10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	9.129	9.067	9.043	8.800	7.594	12.171	12.062	12.020	11.589	9.575	15.214	15.043	14.977	14.307	11.368
L(C)=2W L= 6000	7.728	7.718	7.715	7.668	7.121	10.303	10.287	10.280	10.187	9.108	12.879	12.853	12.842	12.683	10.908
L(C)=2W L=12000	7.695	7.690	7.688	7.655	7.121	10.260	10.251	10.247	10.177	9.108	12.825	12.810	12.803	12.678	10.908
L(C)=4W L= 1000	9.129	9.005	8.958	8.479	6.506	12.171	11.953	11.869	11.033	7.980	15.214	14.873	14.783	13.467	9.290
L(C)=4W L= 6000	7.728	7.708	7.700	7.575	6.281	10.303	10.268	10.252	9.993	7.763	12.879	12.823	12.796	12.338	9.077
L(C)=4W L=12000	7.695	7.684	7.679	7.572	6.281	10.260	10.240	10.229	9.992	7.763	12.825	12.791	12.772	12.338	9.077
L(C)=6W L= 1000	9.129	8.944	8.874	8.176	5.768	12.171	11.845	11.721	10.527	6.989	15.214	14.706	14.514	12.731	8.079
L(C)=6W L= 6000	7.728	7.698	7.684	7.450	5.625	10.303	10.287	10.220	9.737	6.847	12.879	12.788	12.741	11.909	7.935
L(C)=6W L=12000	7.695	7.677	7.668	7.450	5.625	10.260	10.225	10.204	9.737	6.847	12.825	12.765	12.727	11.909	7.935
L(C)=8W L= 1000	9.129	8.883	8.790	7.895	5.242	12.171	11.738	11.576	10.078	6.316	15.214	14.583	14.294	12.103	7.281
L(C)=8W L= 6000	7.728	7.686	7.665	7.303	5.136	10.303	10.224	10.183	9.456	6.207	12.879	12.788	12.676	11.468	7.167
L(C)=8W L=12000	7.695	7.669	7.653	7.303	5.136	10.260	10.207	10.173	9.456	6.207	12.825	12.733	12.669	11.468	7.167

$T(Q) = 2.8$ — $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	W=6.00					W=8.00					W=10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	7.082	7.034	7.016	6.822	5.827	9.443	9.357	9.324	8.980	7.315	11.803	11.670	11.618	11.080	8.652
L(C)=2W L= 6000	6.298	6.290	6.287	6.248	5.653	8.377	8.365	8.362	8.282	7.155	10.496	10.478	10.468	10.299	8.505
L(C)=2W L=12000	6.280	6.276	6.274	6.238	5.653	8.373	8.371	8.351	8.282	7.155	10.466	10.458	10.447	10.299	8.505
L(C)=4W L= 1000	7.082	6.986	6.954	6.542	5.537	9.443	9.271	9.205	8.526	5.967	11.803	11.536	11.832	10.391	8.002
L(C)=4W L= 6000	6.298	6.270	6.265	6.141	4.868	8.377	8.366	8.351	8.070	5.967	10.496	10.446	10.420	9.921	6.942
L(C)=4W L=12000	6.280	6.270	6.265	6.141	4.868	8.373	8.354	8.361	8.070	5.967	10.466	10.434	10.412	9.921	6.942
L(C)=6W L= 1000	7.082	6.918	6.882	6.318	4.352	9.443	9.186	9.087	8.111	5.259	11.803	11.403	11.250	9.790	6.072
L(C)=6W L= 6000	6.298	6.271	6.254	6.003	4.311	8.377	8.306	8.319	7.796	5.220	10.496	10.412	10.360	9.479	6.032
L(C)=6W L=12000	6.280	6.263	6.252	6.003	4.311	8.373	8.339	8.315	7.796	5.220	10.466	10.405	10.360	9.679	6.032
L(C)=8W L= 1000	7.082	6.889	6.815	6.084	3.945	9.443	9.102	8.971	7.745	4.746	11.803	11.274	11.017	9.283	5.439
L(C)=8W L= 6000	6.298	6.260	6.239	5.847	3.915	8.377	8.323	8.280	7.513	4.716	10.496	10.371	10.294	9.058	5.439
L(C)=8W L=12000	6.280	6.254	6.236	5.847	3.915	8.373	8.319	8.278	7.513	4.716	10.466	10.368	10.293	9.058	5.439

$T(Q) = 1.8$ — $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	W=6.00					W=8.00					W=10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	4.731	4.698	4.686	4.547	3.767	6.308	6.250	6.227	5.976	4.677	7.884	7.793	7.758	7.360	5.487
L(C)=2W L= 6000	4.445	4.439	4.436	4.387	3.748	5.926	5.915	5.910	5.802	4.663	7.408	7.390	7.381	7.183	5.475
L(C)=2W L=12000	4.438	4.435	4.433	4.387	3.748	5.918	5.911	5.907	5.802	4.663	7.397	7.386	7.378	7.183	5.475
L(C)=4W L= 1000	4.731	4.665	4.639	4.350	3.112	6.308	6.190	6.143	5.627	3.771	7.884	7.700	7.625	6.828	4.360
L(C)=4W L= 6000	4.445	4.431	4.424	4.263	3.107	5.926	5.900	5.884	5.547	3.767	7.408	7.362	7.333	6.756	4.356
L(C)=4W L=12000	4.438	4.429	4.423	4.263	3.107	5.918	5.898	5.883	5.547	3.767	7.397	7.361	7.333	6.756	4.356
L(C)=6W L= 1000	4.638	4.631	4.591	4.158	2.715	6.308	6.129	6.058	5.309	3.267	7.884	7.605	7.493	6.375	3.767
L(C)=6W L= 6000	4.731	4.623	4.407	4.107	2.712	5.926	5.879	5.847	5.266	3.265	7.408	7.328	7.266	6.337	3.767
L(C)=6W L=12000	4.445	4.420	4.406	4.107	2.712	5.918	5.878	5.847	5.266	3.265	7.397	7.324	7.266	6.337	3.765
L(C)=8W L= 1000	4.438	4.597	4.543	3.981	2.450	6.308	6.069	5.973	5.036	2.944	7.884	7.512	7.363	6.009	3.198
L(C)=8W L= 6000	4.731	4.409	4.385	3.949	2.448	5.926	5.865	5.800	5.009	2.943	7.408	7.276	7.184	5.985	3.396
L(C)=8W L=12000	4.445	4.409	4.385	3.949	2.448	5.918	5.852	5.800	5.009	2.943	7.397	7.276	7.184	5.985	3.396

Table IV — Values of critical currents I_c

T(0)=4.2

W= 20.00

W(C)/W=	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	21.904	21.660	21.567	20.648	16.815
L(C)=1W L= 6000	14.745	14.717	14.706	14.578	13.528
L(C)=1W L=12000	18.553	18.539	18.533	18.457	13.520
L(C)=2W L= 6000	21.904	21.420	21.240	19.528	13.986
L(C)=2W L=12000	14.745	14.687	14.664	14.370	12.010
L(C)=2W L= 1000	14.553	14.510	14.510	14.303	12.009
L(C)=3W L= 1000	21.904	21.187	20.923	18.551	12.288
L(C)=3W L= 6000	14.745	14.656	14.619	14.125	10.794
L(C)=3W L=12000	18.553	18.506	18.483	18.091	10.794
L(C)=4W L= 1000	21.904	20.961	20.620	17.707	11.056
L(C)=4W L= 6000	14.745	14.624	14.572	13.853	9.873
L(C)=4W L=12000	14.553	14.486	14.453	13.836	9.873

W= 25.00

1.00	0.80	0.75	0.50	0.25
27.380	26.999	26.856	25.443	19.943
18.431	18.369	18.369	18.162	16.819
18.192	18.169	18.155	18.031	16.414
27.380	26.629	26.350	23.777	16.279
18.431	18.340	18.302	17.814	14.199
18.192	18.143	18.121	17.755	14.199
27.380	26.271	25.868	22.383	14.746
18.431	18.290	18.230	17.408	12.600
18.192	18.114	18.076	17.379	12.600
27.380	25.929	25.413	21.220	12.734
18.431	18.238	18.153	16.960	11.452
18.192	18.082	18.024	16.949	11.452

T(1)=20.0 (OR ANY OTHER VALUE) W= 30.00

1.00	0.80	0.75	0.50	0.25
32.857	32.309	32.103	30.104	22.814
22.118	22.053	22.027	21.718	19.117
21.830	21.737	21.703	21.582	19.114
32.857	31.781	31.385	27.827	18.366
22.118	21.984	21.928	21.187	16.190
21.830	21.758	21.725	21.137	16.190
32.857	31.276	30.710	25.992	15.886
22.118	21.911	21.655	20.567	15.243
21.830	30.083	30.083	20.549	14.243
32.857	30.800	30.083	24.513	10.279
22.118	21.838	21.706	19.919	12.896
21.830	21.664	21.534	19.912	12.896

T(0)=2.8

W= 20.00

W(C)/W=	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	16.121	15.941	15.873	15.188	12.296
L(C)=1W L= 6000	11.970	11.947	11.937	11.824	10.755
L(C)=1W L=12000	11.865	11.853	11.852	11.778	10.754
L(C)=2W L= 6000	16.121	15.764	15.630	14.248	10.180
L(C)=2W L=12000	11.970	11.922	11.902	11.623	9.125
L(C)=2W L= 1000	11.865	11.839	11.827	13.605	8.325
L(C)=3W L= 1000	16.121	15.595	15.382	13.374	8.325
L(C)=3W L= 6000	11.970	11.855	11.861	11.368	8.204
L(C)=3W L=12000	11.865	11.853	11.801	11.368	8.204
L(C)=4W L= 1000	16.121	15.423	15.169	12.081	8.027
L(C)=4W L= 6000	11.970	11.867	11.819	11.096	7.533
L(C)=4W L=12000	11.865	11.804	11.771	11.094	7.533

W= 25.00

1.00	0.80	0.75	0.50	0.25
20.152	19.870	19.764	18.710	16.562
14.963	14.926	14.911	14.724	12.957
14.831	14.812	14.804	14.675	11.835
20.152	19.596	19.389	17.460	11.835
14.963	14.886	14.853	14.373	10.950
14.831	14.788	14.768	14.366	10.950
20.152	19.331	19.201	15.955	10.250
14.963	14.742	14.788	13.958	10.271
14.831	14.762	14.765	13.958	9.625
20.152	19.153	18.683	13.547	9.244
14.963	14.796	14.716	13.514	8.711
14.831	14.729	14.669	13.513	8.711

T(1)=20.0 (OR ANY OTHER VALUE) W= 30.00

1.00	0.80	0.75	0.50	0.25
24.182	23.778	23.625	22.132	16.637
17.955	17.902	17.880	17.596	14.991
17.798	17.770	17.757	17.550	14.990
24.182	23.386	23.092	20.422	13.303
17.955	17.802	17.793	17.061	12.026
17.798	17.738	17.702	17.052	12.426
24.182	23.012	22.590	19.050	11.532
17.955	17.699	17.695	16.428	10.848
17.798	17.681	17.651	16.428	10.848
24.182	22.658	21.630	17.950	10.049
17.955	17.707	17.586	15.797	9.794
17.798	17.680	17.542	15.797	9.798

T(0)=1.8

W= 20.00

W(C)/W=	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	9.398	9.886	9.843	9.404	7.482
L(C)=1W L= 6000	8.415	8.398	8.390	8.288	7.155
L(C)=1W L=12000	8.378	8.368	8.366	8.282	7.155
L(C)=2W L= 6000	9.398	9.774	9.689	8.853	6.120
L(C)=2W L=12000	8.415	8.378	8.361	8.070	5.967
L(C)=2W L= 1000	8.378	8.356	8.344	8.069	5.967
L(C)=3W L= 1000	9.398	9.664	9.539	8.372	5.124
L(C)=3W L= 6000	8.415	8.355	8.326	7.796	5.220
L(C)=3W L=12000	8.378	8.340	8.315	7.796	5.220
L(C)=4W L= 1000	9.398	9.558	9.394	7.961	4.798
L(C)=4W L= 6000	8.415	8.360	8.280	7.513	4.516
L(C)=4W L=12000	8.378	8.319	8.278	7.513	4.516

W= 25.00

1.00	0.80	0.75	0.50	0.25
12.498	12.322	12.255	11.575	8.024
10.518	10.491	10.479	10.302	8.505
10.472	10.457	10.449	10.298	8.505
12.498	12.149	12.017	10.755	7.095
10.518	10.459	10.430	9.921	6.982
10.472	10.435	10.413	9.921	6.982
12.498	11.900	11.787	10.072	6.141
10.518	10.421	10.369	9.479	6.032
10.472	10.421	10.360	9.479	6.032
12.498	11.818	11.571	9.515	5.528
10.518	10.377	10.297	9.050	5.439
10.472	10.368	10.293	9.050	5.439

T(1)=20.0 (OR ANY OTHER VALUE) W= 30.00

1.00	0.80	0.75	0.50	0.25
14.997	14.798	14.648	13.681	10.048
12.622	12.582	12.565	12.284	9.736
12.566	12.544	12.532	12.281	9.736
14.997	14.497	14.308	12.558	7.986
12.622	12.533	12.498	11.694	7.830
12.566	12.509	12.473	11.694	7.830
14.997	14.258	13.987	11.669	6.894
12.622	12.474	12.393	11.066	6.780
12.566	12.461	12.386	11.066	6.780
14.997	14.033	13.688	10.971	6.207
12.622	12.406	12.287	10.505	6.111
12.566	12.399	12.278	10.505	6.111

Table V — Values of critical currents I_c

$T(0)=4.2$, $T(1)=20.0$ (OR ANY OTHER VALUE)

W(C)/Wm	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	71.817	70.239	69.654	64.183	46.653	89.772	87.322	86.421	78.222	54.416	107.726	104.224	102.947	91.622	61.478
L(C)=0.5W L=6000	30.978	30.861	30.815	30.330	27.430	38.723	38.539	38.468	37.701	13.169	46.467	46.202	46.099	44.984	18.525
L(C)=0.5W L=12000	29.490	29.438	29.411	29.156	21.056	36.863	36.774	36.738	36.324	32.692	44.236	44.107	44.055	43.436	38.233
L(C)=1.0W L=1000	71.817	68.751	67.653	58.389	37.059	89.772	85.056	83.399	70.058	42.692	107.726	101.051	98.748	80.997	47.855
L(C)=1.0W L=6000	30.978	30.742	30.649	29.640	24.134	38.723	38.352	38.206	36.608	28.493	46.467	45.932	45.721	43.394	32.462
L(C)=1.0W L=12000	29.490	29.374	29.327	28.739	24.019	36.863	36.680	36.604	35.618	28.399	44.236	43.969	43.857	42.375	32.381
L(C)=1.5W L=1000	71.817	71.367	65.632	53.998	31.903	89.772	83.003	80.733	64.221	36.658	107.726	98.252	95.160	73.798	41.071
L(C)=1.5W L=6000	30.978	30.621	30.480	28.250	21.641	38.723	38.162	37.940	35.495	25.286	46.467	45.657	45.335	41.905	28.528
L(C)=1.5W L=12000	29.490	29.238	30.303	28.219	21.587	36.863	36.580	36.459	34.000	25.908	44.236	43.822	43.642	41.135	28.687
L(C)=2.0W L=1000	71.817	66.095	64.193	50.605	28.621	89.772	81.170	78.411	59.906	32.908	107.726	95.830	92.180	68.652	36.939
L(C)=2.0W L=6000	30.978	30.305	28.219	19.778		38.723	37.971	37.671	34.409	22.933	46.467	45.380	44.945	40.295	25.819
L(C)=2.0W L=12000	29.490	29.248	29.148	27.707	19.746	36.863	36.476	36.306	33.920	22.904	44.236	43.668	43.412	39.839	25.792

$T(0)=2.8$, $T(1)=20.0$ (OR ANY OTHER VALUE)

W(C)/Wm	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	49.789	48.287	48.478	44.478	32.249	62.236	60.536	59.910	54.198	37.600	74.683	72.252	71.365	63.074	42.470
L(C)=0.5W L=6000	24.761	24.667	24.630	24.226	21.607	30.951	30.803	30.745	30.102	25.990	37.141	36.928	36.844	35.899	30.040
L(C)=0.5W L=12000	23.910	23.873	23.875	23.649	21.509	29.925	29.862	29.822	29.448	28.915	35.910	35.803	35.759	35.192	29.981
L(C)=1.0W L=1000	49.789	47.660	46.896	40.441	25.594	62.236	58.653	57.809	48.856	28.985	74.683	70.048	68.446	56.079	33.050
L(C)=1.0W L=6000	24.761	24.649	24.504	23.627	18.650	30.951	30.653	30.530	29.161	21.915	37.141	36.706	36.530	34.488	24.864
L(C)=1.0W L=12000	23.910	23.843	23.803	23.246	18.650	29.925	29.771	29.705	28.758	21.905	35.910	35.685	35.586	34.121	24.852
L(C)=1.5W L=1000	49.789	46.698	45.637	37.186	22.033	62.236	57.535	55.956	44.459	25.322	74.683	68.404	65.953	51.077	28.378
L(C)=1.5W L=6000	24.761	24.471	24.353	22.992	16.576	30.951	30.494	30.307	28.118	19.250	37.183	36.325	35.390	33.055	21.701
L(C)=1.5W L=12000	23.910	23.790	23.724	22.708	16.568	29.925	29.684	29.575	27.918	19.259	35.910	36.185	36.205	33.055	21.697
L(C)=2.0W L=1000	49.789	45.815	44.492	35.032	19.772	62.236	56.263	54.344	41.470	22.742	74.683	66.145	62.861	35.390	25.539
L(C)=2.0W L=6000	24.761	24.369	24.269	22.351	15.071	30.951	30.334	30.079	27.161	17.427	37.141	36.245	35.872	32.071	19.592
L(C)=2.0W L=12000	23.910	23.733	23.638	22.193	15.066	29.925	29.591	29.433	27.027	17.423	35.910	35.414	35.172	31.595	19.588

$T(0)=1.4$, $T(1)=20.0$ (OR ANY OTHER VALUE)

W(C)/Wm	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	27.562	26.954	25.728	24.592	17.698	34.853	33.509	33.160	29.953	20.614	41.343	39.993	39.498	35.068	23.267
L(C)=0.5W L=6000	17.124	17.057	17.031	16.716	14.314	21.405	21.300	21.258	20.742	17.012	25.686	25.534	25.471	24.698	13.473
L(C)=0.5W L=12000	16.829	16.795	16.781	16.577	14.310	21.037	20.983	20.959	20.605	17.010	25.294	25.165	25.129	24.568	19.471
L(C)=1.0W L=1000	27.562	26.379	25.952	22.323	11.934	34.853	32.632	31.987	26.763	16.139	41.343	38.764	37.868	30.924	19.095
L(C)=1.0W L=6000	17.124	16.987	16.929	15.193	11.934	21.405	21.187	21.095	19.882	11.883	25.686	25.368	25.230	23.019	15.650
L(C)=1.0W L=12000	16.829	16.756	16.651	16.140	11.934	21.037	20.860	20.956	19.882	11.883	25.294	25.066	26.739	23.389	15.659
L(C)=1.5W L=1000	27.562	25.803	25.246	20.616	12.063	34.853	31.837	30.956	24.507	13.872	41.343	37.682	36.480	28.152	15.559
L(C)=1.5W L=6000	17.124	16.912	16.420	15.613	10.440	21.405	21.067	20.918	18.972	12.064	25.686	25.190	24.960	22.181	11.550
L(C)=1.5W L=12000	16.829	16.711	16.651	15.593	10.440	21.037	20.842	20.738	18.958	12.064	25.294	24.949	24.785	22.131	13.560
L(C)=2.0W L=1000	27.562	25.351	25.339	19.309	10.834	34.853	31.129	30.057	22.858	12.476	41.343	36.749	35.317	26.204	13.560
L(C)=2.0W L=6000	17.124	16.834	16.705	15.036	9.431	21.405	20.981	20.731	18.121	10.878	25.686	25.003	24.691	21.014	12.222
L(C)=2.0W L=12000	16.829	16.660	16.569	15.027	9.431	21.037	20.754	20.599	18.116	10.878	25.294	24.812	24.561	21.010	12.222

Table VI — Values of max delta T_{c0}

$T(0)=8.2$, $T(1)=20.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.036	0.020	0.013	0.896	0.503	0.322	3.617	2.023	1.291	8.270	4.593	2.922	15.046	8.270	5.238
L=6000	0.043	0.024	0.016	1.082	0.608	0.388	4.384	2.448	1.561	10.081	5.574	3.539	18.492	10.081	6.361
L=12000	0.043	0.024	0.016	1.082	0.608	0.388	4.384	2.448	1.561	10.081	5.574	3.539	18.492	10.081	6.361

$T(0)=2.8$, $T(1)=20.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.058	0.033	0.021	1.463	0.827	0.525	5.948	3.314	2.112	13.755	7.572	4.798	25.441	13.755	8.648
L=6000	0.065	0.036	0.023	1.626	0.912	0.583	6.633	3.689	2.349	15.427	8.454	5.346	28.783	15.427	9.662
L=12000	0.065	0.036	0.023	1.626	0.912	0.583	6.633	3.689	2.349	15.427	8.454	5.346	28.783	15.427	9.662

$T(0)=1.4$, $T(1)=20.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.126	0.073	0.045	3.177	1.778	1.135	13.108	7.258	4.599	31.633	16.910	10.579	61.967	31.633	19.411
L=6000	0.129	0.073	0.047	3.274	1.831	1.169	13.621	7.487	4.741	32.846	17.488	10.922	64.909	32.846	20.088
L=12000	0.129	0.073	0.047	3.274	1.831	1.169	13.621	7.487	4.741	32.846	17.488	10.922	64.909	32.846	20.088

$T(0)=4.2$, $T(1)=50.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.040	0.022	0.014	1.001	0.562	0.360	4.043	2.261	1.444	9.245	5.135	3.267	16.820	9.245	5.855
L=6000	0.048	0.027	0.017	1.210	0.679	0.434	4.901	2.736	1.745	11.270	6.231	3.957	20.672	11.270	7.111
L=12000	0.048	0.027	0.017	1.210	0.679	0.434	4.901	2.736	1.745	11.270	6.231	3.957	20.672	11.270	7.111

$T(0)=2.8$, $T(1)=50.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.065	0.037	0.023	1.636	0.938	0.587	6.650	3.705	2.361	15.377	8.464	5.360	28.441	15.377	9.667
L=6000	0.072	0.041	0.026	1.818	1.020	0.652	7.415	4.124	2.626	17.246	9.450	5.977	32.177	17.246	10.802
L=12000	0.072	0.041	0.026	1.818	1.020	0.652	7.415	4.124	2.626	17.246	9.450	5.977	32.177	17.246	10.802

$T(0)=1.4$, $T(1)=50.0$

	I=0.1 W=6.0	8.0	10.0	I=0.5 W=6.0	8.0	10.0	I=1.0 W=6.0	8.0	10.0	I=1.5 W=6.0	8.0	10.0	I=2.0 W=6.0	8.0	10.0
L=1000	0.140	0.079	0.051	3.552	1.987	1.269	14.339	8.113	5.142	35.363	18.904	11.826	69.272	35.363	21.700
L=6000	0.145	0.081	0.052	3.660	2.047	1.307	15.227	8.369	5.300	36.718	19.550	12.210	72.562	36.718	22.056
L=12000	0.145	0.081	0.052	3.660	2.047	1.307	15.227	8.369	5.300	36.718	19.550	12.210	72.562	36.718	22.456

Table VII — Values of max delta T_{c0}

T(0)=4.2, T(1)=20.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.160	0.103	0.071	0.643	0.411	0.285	2.587	1.651	1.144	5.886	3.740	2.587	10.629	6.716	4.631
L=6000	0.303	0.194	0.135	1.217	0.778	0.540	4.940	3.140	2.172	11.391	7.175	4.940	20.980	13.041	8.917
L=12000	0.303	0.194	0.135	1.218	0.778	0.540	4.943	3.181	2.173	11.398	7.179	4.943	20.999	13.048	8.922

T(0)=2.8, T(1)=20.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.294	0.188	0.130	1.178	0.753	0.522	4.770	3.035	2.101	10.957	6.919	4.770	20.065	12.532	8.590
L=6000	0.455	0.291	0.202	1.831	1.169	0.811	7.486	4.741	3.276	17.486	10.922	7.486	32.081	20.086	13.620
L=12000	0.455	0.291	0.202	1.831	1.169	0.811	7.487	4.741	3.276	17.488	10.922	7.487	32.086	20.088	13.621

T(0)=1.4, T(1)=20.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.747	0.478	0.332	3.014	1.921	1.331	12.453	7.865	5.402	29.650	18.287	12.453	57.358	34.227	22.924
L=6000	0.912	0.583	0.405	3.689	2.349	1.626	15.527	9.665	6.603	37.557	22.824	15.527	75.828	43.619	28.783
L=12000	0.912	0.583	0.405	3.689	2.349	1.626	15.527	9.662	6.633	37.551	22.824	15.527	75.828	43.619	28.783

T(0)=4.2, T(1)=50.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.179	0.115	0.080	0.718	0.459	0.319	2.892	1.845	1.279	6.580	4.181	2.892	11.882	7.507	5.177
L=6000	0.339	0.217	0.151	1.361	0.869	0.603	5.522	3.510	2.428	12.734	8.021	5.522	23.463	14.567	9.968
L=12000	0.339	0.217	0.151	1.362	0.870	0.604	5.525	3.512	2.429	12.741	8.025	5.525	23.469	14.567	9.974

T(0)=2.8, T(1)=50.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.328	0.210	0.146	1.317	0.892	0.584	5.333	3.393	2.349	12.249	7.735	5.333	22.830	14.009	9.602
L=6000	0.509	0.326	0.226	2.047	1.307	0.906	8.369	5.300	3.660	19.588	12.209	8.369	36.713	22.458	15.226
L=12000	0.509	0.326	0.226	2.047	1.307	0.906	8.369	5.300	3.660	19.550	12.210	8.369	36.718	22.456	15.227

T(0)=1.4, T(1)=50.0

	I=0.5 W=20.0	25.0	30.0	I=1.0 W=20.0	25.0	30.0	I=2.0 W=20.0	25.0	30.0	I=3.0 W=20.0	25.0	30.0	I=4.0 W=20.0	25.0	30.0
L=1000	0.816	0.523	0.351	3.369	2.148	1.488	13.921	8.770	6.039	33.105	20.443	13.921	64.121	38.263	25.627
L=6000	1.020	0.652	0.452	4.124	2.626	1.818	17.246	10.802	7.415	41.985	25.515	17.246	84.321	48.762	32.177
L=12000	1.020	0.652	0.452	4.124	2.626	1.818	17.246	10.802	7.415	41.985	25.515	17.246	84.321	48.762	32.177

Table VIII — Values of max delta T_{o0}

T(0)=4.2 T(1)=20.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.061	0.039	0.027	0.262	0.155	0.108	0.972	0.621	0.431	2.195	1.401	0.972	3.925	2.500	1.732
6000	0.294	0.188	0.131	1.179	0.754	0.523	4.781	3.040	2.104	11.007	6.941	4.781	20.221	12.596	8.622
12000	0.303	0.194	0.135	1.217	0.778	0.540	4.940	3.180	2.172	11.391	7.175	4.940	20.980	13.081	8.917

T(0)=2.8 T(1)=20.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.126	0.080	0.056	0.503	0.322	0.224	2.024	1.292	0.896	4.592	2.923	2.028	8.261	5.235	3.616
6000	0.450	0.288	0.200	1.808	1.154	0.801	7.387	4.680	3.232	17.234	10.773	7.387	32.300	19.789	13.430
12000	0.455	0.291	0.202	1.831	1.169	0.811	7.406	4.741	3.274	17.486	10.921	7.486	32.841	20.086	13.620

T(0)=1.6 T(1)=20.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.407	0.261	0.181	1.637	1.045	0.725	6.656	4.226	2.922	15.406	9.680	6.656	28.533	17.655	12.042
6000	0.911	0.582	0.404	3.685	2.345	1.628	15.399	9.646	6.622	37.467	22.778	15.399	75.157	43.506	28.721
12000	0.912	0.583	0.405	3.689	2.349	1.626	15.027	9.662	6.633	37.557	22.824	15.427	75.428	43.619	28.783

T(0)=4.2 T(1)=50.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.068	0.043	0.030	0.271	0.173	0.120	1.086	0.694	0.482	2.454	1.566	1.086	4.387	2.795	1.936
6000	0.329	0.210	0.146	1.310	0.842	0.585	5.345	3.399	2.352	12.305	7.759	5.345	22.605	14.081	9.638
12000	0.339	0.217	0.151	1.361	0.865	0.603	5.522	3.510	2.428	12.734	8.021	5.522	23.453	14.578	9.968

T(0)=2.8 T(1)=50.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.141	0.090	0.062	0.563	0.360	0.250	2.262	1.444	1.002	5.133	3.267	2.262	9.235	5.853	4.043
6000	0.503	0.322	0.223	2.021	1.291	0.895	8.258	5.232	3.613	19.266	12.043	8.258	36.108	22.122	15.013
12000	0.509	0.326	0.226	2.087	1.307	0.906	8.369	5.300	3.660	19.548	12.209	8.369	36.713	22.458	15.226

T(0)=1.4 T(1)=50.0

	I=1.0			I=2.0			I=4.0			I=6.0			I=8.0		
L	W=80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0	80.0	100.0	120.0
1000	0.456	0.291	0.202	1.830	1.169	0.811	7.081	4.724	3.267	17.223	10.821	7.181	31.898	19.736	13.462
6000	1.018	0.651	0.452	4.117	2.622	1.815	17.214	10.783	7.403	41.888	25.463	17.214	84.018	48.636	32.107
12000	1.020	0.652	0.452	4.124	2.626	1.818	17.246	10.802	7.415	41.985	25.515	17.246	84.321	48.762	32.177

Table IX — Values of (max delta T_c)/(max delta T_{c0})

$I = 0.1$, $T(0) = 4.2$, $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	N=6.00 1.00	0.80	0.75	0.50	0.25	N=8.00 1.00	0.80	0.75	0.50	0.25	N=10.00 1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.019	1.027	1.103	1.517	1.000	1.026	1.036	1.137	1.685	1.000	1.032	1.044	1.170	1.852
L(C)=2W L= 6000	1.000	1.016	1.023	1.087	1.434	1.000	1.022	1.030	1.115	1.576	1.000	1.027	1.037	1.143	1.717
L(C)=2W L=12000	1.000	1.016	1.023	1.087	1.434	1.000	1.022	1.030	1.115	1.576	1.000	1.027	1.037	1.143	1.717
L(C)=4W L= 1000	1.000	1.038	1.053	1.204	2.018	1.000	1.050	1.070	1.269	2.304	1.000	1.062	1.086	1.333	2.663
L(C)=4W L= 6000	1.000	1.032	1.044	1.171	1.856	1.000	1.042	1.059	1.226	2.131	1.000	1.052	1.073	1.280	2.400
L(C)=4W L=12000	1.000	1.032	1.044	1.171	1.856	1.000	1.042	1.059	1.226	2.131	1.000	1.052	1.073	1.280	2.400
L(C)=6W L= 1000	1.000	1.056	1.078	1.301	2.505	1.000	1.074	1.102	1.395	2.977	1.000	1.091	1.126	1.490	3.435
L(C)=6W L= 6000	1.000	1.047	1.066	1.253	2.266	1.000	1.062	1.086	1.333	2.664	1.000	1.077	1.106	1.410	3.050
L(C)=6W L=12000	1.000	1.047	1.066	1.253	2.266	1.000	1.062	1.086	1.333	2.664	1.000	1.077	1.106	1.410	3.050
L(C)=8W L= 1000	1.000	1.074	1.102	1.395	2.977	1.000	1.097	1.134	1.517	3.585	1.000	1.119	1.164	1.639	4.169
L(C)=8W L= 6000	1.000	1.062	1.086	1.333	2.664	1.000	1.082	1.113	1.435	3.177	1.000	1.100	1.138	1.534	3.669
L(C)=8W L=12000	1.000	1.062	1.086	1.333	2.664	1.000	1.082	1.113	1.435	3.177	1.000	1.100	1.138	1.534	3.669

$I = 0.1$, $T(0) = 2.8$, $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	N=6.00 1.00	0.80	0.75	0.50	0.25	N=8.00 1.00	0.80	0.75	0.50	0.25	N=10.00 1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.022	1.030	1.117	1.586	1.000	1.029	1.040	1.155	1.777	1.000	1.036	1.050	1.193	1.965
L(C)=2W L= 6000	1.000	1.020	1.028	1.106	1.530	1.000	1.026	1.036	1.141	1.703	1.000	1.033	1.045	1.175	1.873
L(C)=2W L=12000	1.000	1.020	1.028	1.106	1.530	1.000	1.026	1.036	1.141	1.703	1.000	1.033	1.045	1.175	1.873
L(C)=4W L= 1000	1.000	1.039	1.060	1.230	2.042	1.000	1.057	1.079	1.303	2.517	1.000	1.070	1.097	1.339	2.873
L(C)=4W L= 6000	1.000	1.039	1.054	1.208	2.042	1.000	1.051	1.071	1.275	2.373	1.000	1.064	1.088	1.339	2.696
L(C)=4W L=12000	1.000	1.039	1.054	1.208	2.042	1.000	1.051	1.071	1.275	2.373	1.000	1.064	1.088	1.339	2.696
L(C)=6W L= 1000	1.000	1.058	1.088	1.339	2.697	1.000	1.083	1.115	1.444	3.222	1.000	1.102	1.141	1.546	3.729
L(C)=6W L= 6000	1.000	1.058	1.080	1.307	2.536	1.000	1.075	1.104	1.402	3.012	1.000	1.093	1.128	1.494	3.471
L(C)=6W L=12000	1.000	1.058	1.080	1.307	2.536	1.000	1.075	1.104	1.402	3.012	1.000	1.093	1.128	1.494	3.471
L(C)=8W L= 1000	1.000	1.083	1.115	1.444	3.223	1.000	1.109	1.150	1.579	3.894	1.000	1.133	1.183	1.707	4.538
L(C)=8W L= 6000	1.000	1.075	1.104	1.402	3.013	1.000	1.098	1.136	1.524	3.621	1.000	1.120	1.166	1.640	4.201
L(C)=8W L=12000	1.000	1.075	1.104	1.402	3.013	1.000	1.098	1.136	1.524	3.621	1.000	1.120	1.166	1.640	4.201

$I = 0.1$, $T(0) = 1.4$, $T(1) = 20.0$ (OR ANY OTHER VALUE)

W(C)/W=	N=6.00 1.00	0.80	0.75	0.50	0.25	N=8.00 1.00	0.80	0.75	0.50	0.25	N=10.00 1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.029	1.040	1.153	1.767	1.000	1.038	1.053	1.203	2.013	1.000	1.047	1.065	1.251	2.256
L(C)=2W L= 6000	1.000	1.026	1.039	1.149	1.745	1.000	1.037	1.051	1.197	1.985	1.000	1.046	1.063	1.244	2.220
L(C)=2W L=12000	1.000	1.026	1.039	1.149	1.745	1.000	1.037	1.051	1.197	1.985	1.000	1.046	1.063	1.244	2.220
L(C)=4W L= 1000	1.000	1.056	1.078	1.299	2.496	1.000	1.073	1.102	1.392	2.905	1.000	1.090	1.125	1.482	3.310
L(C)=4W L= 6000	1.000	1.054	1.075	1.290	2.453	1.000	1.071	1.099	1.381	2.905	1.000	1.088	1.121	1.468	3.342
L(C)=4W L=12000	1.000	1.054	1.075	1.290	2.453	1.000	1.071	1.099	1.381	2.905	1.000	1.088	1.121	1.468	3.342
L(C)=6W L= 1000	1.000	1.082	1.113	1.437	3.189	1.000	1.107	1.147	1.569	3.846	1.000	1.130	1.180	1.675	4.471
L(C)=6W L= 6000	1.000	1.080	1.110	1.425	3.127	1.000	1.104	1.143	1.553	3.766	1.000	1.126	1.175	1.674	4.373
L(C)=6W L=12000	1.000	1.080	1.110	1.425	3.127	1.000	1.104	1.143	1.553	3.766	1.000	1.126	1.175	1.675	4.373
L(C)=8W L= 1000	1.000	1.107	1.148	1.569	3.848	1.000	1.138	1.190	1.734	4.678	1.000	1.157	1.210	1.689	5.446
L(C)=8W L= 6000	1.000	1.104	1.143	1.553	3.768	1.000	1.134	1.185	1.713	4.570	1.000	1.162	1.224	1.864	5.320
L(C)=8W L=12000	1.000	1.104	1.143	1.553	3.768	1.000	1.134	1.185	1.713	4.570	1.000	1.162	1.224	1.864	5.320

Table X — Values of (max delta T_c)/(max delta T_{c0})

$T(0) = 4.2$, $I = 0.5$, $\Sigma(1) = 20.0$ (OR ANY OTHER VALUE)

	N = 6.00					N = 8.00				N = 10.00				
W(C)/W	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.019	1.027	1.104	1.519	1.026	1.036	1.137	1.687	1.000	1.032	1.044	1.171	1.854
L(C)=2W L=6000	1.000	1.016	1.023	1.087	1.436	1.022	1.030	1.115	1.578	1.000	1.027	1.037	1.144	1.718
L(C)=2W L=12000	1.000	1.016	1.023	1.087	1.436	1.022	1.030	1.115	1.578	1.000	1.027	1.037	1.144	1.718
L(C)=4W L=1000	1.000	1.038	1.053	1.204	2.024	1.050	1.070	1.269	2.349	1.000	1.062	1.086	1.333	2.648
L(C)=4W L=6000	1.000	1.032	1.045	1.172	1.861	1.042	1.059	1.227	2.135	1.000	1.053	1.073	1.280	2.404
L(C)=4W L=12000	1.000	1.032	1.045	1.172	1.861	1.042	1.059	1.227	2.135	1.000	1.053	1.073	1.280	2.404
L(C)=6W L=1000	1.000	1.057	1.078	1.302	2.516	1.078	1.103	1.396	2.987	1.000	1.091	1.126	1.488	3.444
L(C)=6W L=6000	1.000	1.048	1.066	1.254	2.275	1.062	1.086	1.333	2.672	1.000	1.077	1.106	1.411	3.058
L(C)=6W L=12000	1.000	1.048	1.066	1.254	2.275	1.062	1.086	1.333	2.672	1.000	1.077	1.106	1.411	3.058
L(C)=8W L=1000	1.000	1.074	1.103	1.397	2.995	1.097	1.134	1.518	3.601	1.000	1.119	1.164	1.635	4.184
L(C)=8W L=6000	1.000	1.063	1.086	1.334	2.679	1.082	1.113	1.436	3.190	1.000	1.100	1.139	1.535	3.682
L(C)=8W L=12000	1.000	1.063	1.086	1.334	2.679	1.082	1.113	1.436	3.190	1.000	1.100	1.139	1.535	3.682

$T(0) = 2.8$, $I = 0.5$, $\Sigma(1) = 20.0$ (OR ANY OTHER VALUE)

	N = 6.00					N = 8.00				N = 10.00				
W(C)/W	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.022	1.030	1.118	1.590	1.028	1.040	1.156	1.780	1.000	1.035	1.050	1.193	1.968
L(C)=2W L=6000	1.000	1.020	1.028	1.106	1.534	1.026	1.037	1.141	1.706	1.000	1.033	1.045	1.175	1.876
L(C)=2W L=12000	1.000	1.020	1.028	1.106	1.534	1.026	1.037	1.141	1.706	1.000	1.033	1.045	1.175	1.876
L(C)=4W L=1000	1.000	1.043	1.060	1.231	2.163	1.057	1.079	1.304	2.527	1.000	1.064	1.097	1.375	2.883
L(C)=4W L=6000	1.000	1.039	1.054	1.209	2.052	1.052	1.071	1.275	2.382	1.000	1.064	1.088	1.340	2.704
L(C)=4W L=12000	1.000	1.039	1.054	1.209	2.052	1.052	1.071	1.275	2.382	1.000	1.064	1.088	1.340	2.704
L(C)=6W L=1000	1.000	1.064	1.088	1.341	2.718	1.083	1.115	1.486	3.242	1.000	1.102	1.142	1.547	3.747
L(C)=6W L=6000	1.000	1.058	1.080	1.309	2.555	1.076	1.105	1.404	3.029	1.000	1.093	1.128	1.495	3.487
L(C)=6W L=12000	1.000	1.058	1.080	1.309	2.555	1.076	1.105	1.404	3.029	1.000	1.093	1.128	1.495	3.487
L(C)=8W L=1000	1.000	1.081	1.116	1.447	3.258	1.109	1.150	1.581	3.926	1.000	1.133	1.184	1.709	4.563
L(C)=8W L=6000	1.000	1.076	1.105	1.405	3.044	1.098	1.136	1.526	3.649	1.000	1.120	1.166	1.642	4.227
L(C)=8W L=12000	1.000	1.076	1.105	1.405	3.044	1.098	1.136	1.526	3.649	1.000	1.120	1.166	1.642	4.227

$T(0) = 1.4$, $I = 0.5$, $\Sigma(1) = 20.0$ (OR ANY OTHER VALUE)

	N = 6.00					N = 8.00				N = 10.00				
W(C)/W	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.029	1.040	1.155	1.779	1.038	1.053	1.208	2.024	1.000	1.047	1.065	1.252	2.266
L(C)=2W L=6000	1.000	1.028	1.039	1.150	1.756	1.037	1.051	1.199	1.995	1.000	1.046	1.063	1.245	2.230
L(C)=2W L=12000	1.000	1.028	1.039	1.150	1.756	1.037	1.051	1.199	1.995	1.000	1.046	1.063	1.245	2.230
L(C)=4W L=1000	1.000	1.056	1.078	1.302	2.533	1.072	1.099	1.363	2.937	1.000	1.083	1.125	1.484	3.441
L(C)=4W L=6000	1.000	1.055	1.076	1.293	2.489	1.072	1.099	1.383	2.894	1.000	1.091	1.122	1.470	3.372
L(C)=4W L=12000	1.000	1.055	1.076	1.293	2.489	1.072	1.099	1.383	2.894	1.000	1.091	1.122	1.470	3.372
L(C)=6W L=1000	1.000	1.083	1.114	1.443	3.262	1.107	1.148	1.573	3.912	1.000	1.131	1.180	1.698	4.531
L(C)=6W L=6000	1.000	1.080	1.111	1.430	3.197	1.104	1.144	1.557	3.829	1.000	1.127	1.175	1.678	4.430
L(C)=6W L=12000	1.000	1.080	1.111	1.430	3.197	1.104	1.144	1.557	3.829	1.000	1.127	1.175	1.678	4.430
L(C)=8W L=1000	1.000	1.108	1.149	1.577	3.967	1.138	1.191	1.741	4.779	1.000	1.167	1.231	1.894	5.540
L(C)=8W L=6000	1.000	1.104	1.185	1.560	3.882	1.134	1.186	1.720	4.671	1.000	1.162	1.225	1.869	5.411
L(C)=8W L=12000	1.000	1.104	1.185	1.560	3.882	1.134	1.186	1.720	4.671	1.000	1.162	1.225	1.869	5.411

Table XI — Values of (max delta T_c)/(max delta T_{c0})

I= 1.0 T(0)=-0.2

W(C)/W=	W= 6.00					T(1)=20.0 (OR ANY OTHER VALUE) W= 8.00					W= 10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.020	1.027	1.108	1.525	1.000	1.026	1.036	1.138	1.693	1.000	1.032	1.084	1.171	1.859
L(C)=2W L= 6000	1.000	1.016	1.023	1.088	1.441	1.000	1.022	1.030	1.116	1.582	1.000	1.027	1.037	1.144	1.722
L(C)=2W L=12000	1.000	1.016	1.023	1.088	1.441	1.000	1.022	1.030	1.116	1.582	1.000	1.027	1.037	1.144	1.722
L(C)=4W L= 1000	1.000	1.032	1.053	1.206	2.042	1.000	1.051	1.070	1.271	2.365	1.000	1.063	1.087	1.334	2.683
L(C)=4W L= 6000	1.000	1.032	1.045	1.173	1.876	1.000	1.043	1.059	1.228	2.149	1.000	1.053	1.073	1.281	2.416
L(C)=4W L=12000	1.000	1.057	1.079	1.305	2.551	1.000	1.075	1.103	1.399	3.018	1.000	1.092	1.127	1.490	3.473
L(C)=6W L= 1000	1.000	1.048	1.066	1.257	2.305	1.000	1.063	1.087	1.335	2.699	1.000	1.077	1.107	1.412	3.082
L(C)=6W L= 6000	1.000	1.048	1.066	1.257	2.305	1.000	1.063	1.087	1.335	2.699	1.000	1.077	1.107	1.412	3.082
L(C)=6W L=12000	1.000	1.075	1.106	1.401	3.052	1.000	1.098	1.135	1.532	3.692	1.000	1.119	1.165	1.638	4.230
L(C)=8W L= 1000	1.000	1.063	1.087	1.338	2.727	1.000	1.082	1.114	1.439	3.233	1.000	1.100	1.139	1.537	3.721
L(C)=8W L= 6000	1.000	1.063	1.087	1.338	2.727	1.000	1.082	1.114	1.439	3.231	1.000	1.103	1.139	1.537	3.721

I= 1.0 T(0)=-2.0

W(C)/W=	W= 6.00					T(1)=20.0 (OR ANY OTHER VALUE) W= 8.00					W= 10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.022	1.031	1.119	1.602	1.000	1.029	1.041	1.157	1.791	1.000	1.036	1.050	1.194	1.978
L(C)=2W L= 6000	1.000	1.020	1.028	1.108	1.545	1.000	1.027	1.037	1.142	1.715	1.000	1.033	1.046	1.176	1.885
L(C)=2W L=12000	1.000	1.020	1.028	1.108	1.545	1.000	1.027	1.037	1.142	1.715	1.000	1.033	1.046	1.176	1.885
L(C)=4W L= 1000	1.000	1.044	1.061	1.235	2.199	1.000	1.057	1.079	1.307	2.559	1.000	1.071	1.098	1.378	2.912
L(C)=4W L= 6000	1.000	1.040	1.055	1.212	2.065	1.000	1.052	1.072	1.278	2.411	1.000	1.064	1.088	1.342	2.731
L(C)=4W L=12000	1.000	1.065	1.089	1.347	2.790	1.000	1.084	1.116	1.451	3.305	1.000	1.103	1.142	1.551	3.805
L(C)=6W L= 1000	1.000	1.058	1.081	1.314	2.619	1.000	1.076	1.105	1.406	3.086	1.000	1.093	1.129	1.499	3.539
L(C)=6W L= 6000	1.000	1.058	1.081	1.314	2.619	1.000	1.076	1.105	1.408	3.086	1.000	1.093	1.129	1.499	3.539
L(C)=6W L=12000	1.000	1.085	1.117	1.456	3.375	1.000	1.110	1.152	1.588	4.028	1.000	1.133	1.184	1.715	4.656
L(C)=8W L= 1000	1.000	1.077	1.106	1.412	3.148	1.000	1.099	1.137	1.532	3.761	1.000	1.121	1.167	1.647	4.311
L(C)=8W L= 6000	1.000	1.077	1.106	1.412	3.148	1.000	1.099	1.137	1.532	3.741	1.000	1.121	1.167	1.647	4.311

I= 1.0 T(0)=1.0

W(C)/W=	W= 6.00					T(1)=20.0 (OR ANY OTHER VALUE) W= 8.00					W= 10.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L= 1000	1.000	1.030	1.041	1.159	1.820	1.000	1.039	1.053	1.207	2.059	1.000	1.048	1.066	1.255	2.297
L(C)=2W L= 6000	1.000	1.029	1.040	1.154	1.795	1.000	1.038	1.052	1.201	2.028	1.000	1.046	1.064	1.247	2.260
L(C)=2W L=12000	1.000	1.029	1.040	1.158	1.795	1.000	1.038	1.052	1.201	2.028	1.000	1.046	1.064	1.247	2.260
L(C)=4W L= 1000	1.000	1.054	1.080	1.312	2.662	1.000	1.075	1.104	1.403	3.106	1.000	1.091	1.098	1.491	3.542
L(C)=4W L= 6000	1.000	1.056	1.078	1.303	2.613	1.000	1.073	1.101	1.391	3.044	1.000	1.089	1.123	1.477	3.469
L(C)=4W L=12000	1.000	1.085	1.117	1.460	3.526	1.000	1.109	1.151	1.588	4.136	1.000	1.132	1.182	1.710	4.731
L(C)=6W L= 1000	1.000	1.082	1.134	1.447	3.451	1.000	1.106	1.146	1.570	4.065	1.000	1.128	1.177	1.689	4.623
L(C)=6W L= 6000	1.000	1.082	1.134	1.447	3.451	1.000	1.106	1.146	1.570	4.065	1.000	1.128	1.177	1.689	4.623
L(C)=6W L=12000	1.000	1.117	1.153	1.603	4.309	1.000	1.145	1.195	1.762	5.148	1.000	1.169	1.234	1.912	5.063
L(C)=8W L= 1000	1.000	1.107	1.159	1.585	4.308	1.000	1.136	1.189	1.740	5.027	1.000	1.164	1.227	1.866	5.723
L(C)=8W L= 6000	1.000	1.107	1.159	1.585	4.308	1.000	1.136	1.189	1.740	5.027	1.000	1.164	1.227	1.886	5.723

Table XII — Values of (max delta T_c)/(max delta T_{c0})

$I = 1.5$

$T(0) = 4.2$

			W= 6.00				W= 8.00				T(1)=-20.0 (OR ANY OTHER VALUE)				W= 10.00		
W(C)/W=		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W	L= 1000	1.000	1.020	1.027	1.106	1.536	1.000	1.026	1.036	1.139	1.702	1.000	1.032	1.045	1.172	1.667
L(C)=2W	L= 6000	1.000	1.017	1.023	1.089	1.451	1.000	1.022	1.030	1.117	1.590	1.000	1.027	1.037	1.145	1.729
L(C)=2W	L=12000	1.000	1.017	1.023	1.089	1.451	1.000	1.022	1.031	1.117	1.590	1.000	1.027	1.037	1.145	1.729
L(C)=4W	L= 1000	1.000	1.033	1.045	1.176	1.903	1.000	1.043	1.059	1.230	2.172	1.000	1.053	1.073	1.283	2.437
L(C)=4W	L= 6000	1.000	1.033	1.045	1.176	1.903	1.000	1.043	1.059	1.230	2.172	1.000	1.053	1.073	1.283	2.437
L(C)=4W	L=12000	1.000	1.056	1.091	1.361	2.614	1.000	1.073	1.104	1.403	3.073	1.000	1.092	1.127	1.493	3.523
L(C)=6W	L= 1000	1.000	1.049	1.067	1.261	2.358	1.000	1.063	1.087	1.339	2.745	1.000	1.078	1.107	1.415	3.124
L(C)=6W	L= 6000	1.000	1.049	1.067	1.261	2.358	1.000	1.063	1.087	1.339	2.745	1.000	1.078	1.107	1.415	3.124
L(C)=6W	L=12000	1.000	1.076	1.105	1.409	3.155	1.000	1.098	1.136	1.528	3.781	1.000	1.120	1.166	1.643	4.311
L(C)=8W	L= 1000	1.000	1.064	1.108	1.344	2.813	1.000	1.083	1.114	1.444	3.308	1.000	1.107	1.140	1.542	3.789
L(C)=8W	L= 6000	1.000	1.064	1.108	1.344	2.813	1.000	1.083	1.118	1.444	3.308	1.000	1.107	1.140	1.542	3.789

$I = 1.5$

$T(0) = 2.8$

			W= 6.00				W= 8.00				T(1)=20.0 (OR ANY OTHER VALUE)				W= 10.00		
W(C)/W=		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W	L= 1000	1.000	1.023	1.031	1.122	1.625	1.000	1.030	1.041	1.159	1.809	1.000	1.037	1.051	1.196	1.994
L(C)=2W	L= 6000	1.000	1.021	1.028	1.110	1.564	1.000	1.027	1.037	1.144	1.731	1.000	1.033	1.046	1.177	1.899
L(C)=2W	L=12000	1.000	1.021	1.028	1.110	1.564	1.000	1.027	1.037	1.144	1.731	1.000	1.033	1.046	1.177	1.899
L(C)=4W	L= 1000	1.000	1.045	1.062	1.241	2.266	1.000	1.058	1.080	1.312	2.616	1.000	1.071	1.098	1.382	2.963
L(C)=4W	L= 6000	1.000	1.040	1.056	1.217	2.143	1.000	1.052	1.073	1.282	2.461	1.000	1.064	1.089	1.345	2.776
L(C)=4W	L=12000	1.000	1.040	1.056	1.217	2.143	1.000	1.052	1.073	1.282	2.461	1.000	1.064	1.089	1.345	2.776
L(C)=6W	L= 1000	1.000	1.066	1.091	1.357	2.924	1.000	1.085	1.118	1.459	3.419	1.000	1.108	1.144	1.558	3.907
L(C)=6W	L= 6000	1.000	1.060	1.082	1.322	2.738	1.000	1.077	1.106	1.415	3.188	1.000	1.094	1.130	1.505	3.630
L(C)=6W	L=12000	1.000	1.087	1.120	1.599	3.599	1.000	1.111	1.154	1.600	4.216	1.000	1.138	1.186	1.725	4.823
L(C)=8W	L= 1000	1.000	1.078	1.108	1.825	3.348	1.000	1.100	1.139	1.542	3.910	1.000	1.122	1.168	1.656	4.450
L(C)=8W	L= 6000	1.000	1.078	1.108	1.825	3.348	1.000	1.100	1.139	1.542	3.910	1.000	1.122	1.168	1.656	4.460

$I = 1.5$

$T(0) = 1.4$

			W= 6.00				W= 8.00				T(1)=20.0 (OR ANY OTHER VALUE)				W= 10.00		
W(C)/W=		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W	L= 1000	1.000	1.031	1.043	1.167	1.899	1.000	1.039	1.055	1.213	2.123	1.000	1.048	1.067	1.260	2.354
L(C)=2W	L= 6000	1.000	1.030	1.041	1.161	1.870	1.000	1.038	1.053	1.206	2.089	1.000	1.047	1.065	1.252	2.314
L(C)=2W	L=12000	1.000	1.030	1.041	1.161	1.870	1.000	1.038	1.053	1.206	2.089	1.000	1.047	1.065	1.252	2.314
L(C)=4W	L= 1000	1.000	1.060	1.084	1.331	2.936	1.000	1.077	1.106	1.417	3.323	1.000	1.093	1.129	1.503	3.730
L(C)=4W	L= 6000	1.000	1.058	1.081	1.321	2.874	1.000	1.074	1.103	1.405	3.253	1.000	1.090	1.125	1.488	3.649
L(C)=4W	L=12000	1.000	1.058	1.081	1.321	2.874	1.000	1.074	1.103	1.405	3.253	1.000	1.090	1.125	1.488	3.649
L(C)=6W	L= 1000	1.000	1.089	1.123	1.493	4.137	1.000	1.112	1.150	1.594	4.691	1.000	1.136	1.185	1.731	5.121
L(C)=6W	L= 6000	1.000	1.086	1.119	1.478	4.037	1.000	1.108	1.150	1.594	4.607	1.000	1.130	1.180	1.710	4.999
L(C)=6W	L=12000	1.000	1.116	1.161	1.678	4.937	1.000	1.144	1.200	1.800	5.451	1.000	1.172	1.238	1.910	5.518
L(C)=8W	L= 1000	1.000	1.112	1.156	1.653	5.380	1.000	1.143	1.194	1.776	5.954	1.000	1.167	1.231	1.916	6.355
L(C)=8W	L=12000	1.000	1.112	1.156	1.632	5.396	1.000	1.143	1.194	1.776	5.605	1.000	1.167	1.231	1.916	6.355

Table XIII —Values of (max delta T_c)/(max delta T_{c0})

I = 2.0 , T(0) = 4.2 , T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W*		M = 6.00					M = 8.00					M = 10.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.020	1.028	1.108	1.553	1.000	1.026	1.036	1.141	1.716	1.000	1.032	1.045	1.173	2.079
L(C)=2W L=6000	1.000	1.017	1.023	1.091	1.464	1.000	1.022	1.031	1.118	1.601	1.000	1.027	1.038	1.166	1.739
L(C)=2W L=12000	1.000	1.017	1.023	1.091	1.464	1.000	1.022	1.031	1.118	1.601	1.000	1.027	1.036	1.146	1.739
L(C)=4W L=1000	1.000	1.040	1.055	1.214	2.124	1.000	1.052	1.071	1.277	2.434	1.000	1.063	1.088	1.288	2.745
L(C)=4W L=6000	1.000	1.033	1.046	1.180	1.944	1.000	1.043	1.060	1.233	2.206	1.000	1.053	1.074	1.285	2.468
L(C)=4W L=12000	1.000	1.033	1.046	1.180	1.944	1.000	1.043	1.060	1.233	2.206	1.000	1.053	1.074	1.285	2.468
L(C)=6W L=1000	1.000	1.059	1.081	1.318	2.712	1.000	1.076	1.105	1.409	3.155	1.000	1.093	1.128	1.499	3.596
L(C)=6W L=6000	1.000	1.049	1.068	1.267	2.439	1.000	1.064	1.088	1.344	2.813	1.000	1.078	1.108	1.420	3.185
L(C)=6W L=12000	1.000	1.049	1.068	1.267	2.439	1.000	1.064	1.088	1.344	2.813	1.000	1.078	1.108	1.420	3.185
L(C)=8W L=1000	1.000	1.077	1.107	1.421	3.317	1.000	1.099	1.138	1.537	3.876	1.000	1.121	1.167	1.651	4.430
L(C)=8W L=6000	1.000	1.065	1.090	1.353	2.951	1.000	1.084	1.116	1.452	3.422	1.000	1.102	1.181	1.548	4.691
L(C)=8W L=12000	1.000	1.065	1.090	1.353	2.951	1.000	1.084	1.116	1.452	3.422	1.000	1.102	1.181	1.548	4.694

I = 2.0 , T(0) = 2.8 , T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W*		M = 6.00					M = 8.00					M = 10.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.023	1.032	1.126	1.659	1.000	1.030	1.042	1.162	1.837	1.000	1.037	1.051	1.198	2.018
L(C)=2W L=6000	1.000	1.021	1.029	1.113	1.594	1.000	1.027	1.038	1.146	1.755	1.000	1.033	1.046	1.179	1.920
L(C)=2W L=12000	1.000	1.021	1.029	1.113	1.594	1.000	1.027	1.038	1.146	1.755	1.000	1.033	1.046	1.179	1.920
L(C)=4W L=1000	1.000	1.046	1.064	1.250	2.374	1.000	1.059	1.082	1.319	2.703	1.000	1.072	1.100	1.388	3.030
L(C)=4W L=6000	1.000	1.041	1.057	1.225	2.238	1.000	1.053	1.074	1.288	2.538	1.000	1.065	1.090	1.350	2.844
L(C)=4W L=12000	1.000	1.041	1.057	1.225	2.238	1.000	1.053	1.074	1.288	2.538	1.000	1.065	1.090	1.350	2.844
L(C)=6W L=1000	1.000	1.068	1.094	1.373	3.150	1.000	1.087	1.120	1.471	3.599	1.000	1.105	1.145	1.568	4.062
L(C)=6W L=6000	1.000	1.061	1.085	1.336	2.939	1.000	1.078	1.108	1.425	3.348	1.000	1.095	1.131	1.513	3.770
L(C)=6W L=12000	1.000	1.061	1.085	1.336	2.939	1.000	1.078	1.108	1.425	3.348	1.000	1.095	1.131	1.513	3.770
L(C)=8W L=1000	1.000	1.089	1.124	1.494	3.994	1.000	1.099	1.157	1.618	4.522	1.000	1.136	1.188	1.740	5.082
L(C)=8W L=6000	1.000	1.081	1.112	1.445	3.703	1.000	1.102	1.141	1.558	4.185	1.000	1.123	1.170	1.669	4.691
L(C)=8W L=12000	1.000	1.081	1.112	1.445	3.703	1.000	1.102	1.141	1.558	4.185	1.000	1.123	1.170	1.669	4.694

I = 2.0 , T(0) = 1.8 , T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W*		M = 6.00					M = 8.00					M = 10.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=2W L=1000	1.000	1.033	1.045	1.179	2.043	1.000	1.041	1.056	1.222	2.228	1.000	1.049	1.068	1.267	2.442
L(C)=2W L=6000	1.000	1.032	1.044	1.173	2.006	1.000	1.039	1.055	1.215	2.189	1.000	1.048	1.066	1.259	2.397
L(C)=2W L=12000	1.000	1.032	1.044	1.173	2.006	1.000	1.039	1.055	1.215	2.189	1.000	1.048	1.066	1.259	2.397
L(C)=4W L=1000	1.000	1.064	1.089	1.363	2.520	1.000	1.079	1.110	1.440	3.716	1.000	1.095	1.132	1.521	4.046
L(C)=4W L=6000	1.000	1.062	1.086	1.350	2.432	1.000	1.077	1.107	1.428	3.630	1.000	1.092	1.128	1.505	3.953
L(C)=4W L=12000	1.000	1.062	1.086	1.350	2.432	1.000	1.077	1.107	1.428	3.630	1.000	1.092	1.128	1.505	3.953
L(C)=6W L=1000	1.000	1.095	1.132	1.550	5.755	1.000	1.116	1.161	1.653	5.540	1.000	1.137	1.191	1.764	5.827
L(C)=6W L=6000	1.000	1.092	1.128	1.530	5.591	1.000	1.112	1.156	1.632	5.396	1.000	1.133	1.185	1.740	5.680
L(C)=6W L=12000	1.000	1.092	1.128	1.530	5.591	1.000	1.112	1.156	1.632	5.396	1.000	1.133	1.185	1.740	5.680
L(C)=8W L=1000	1.000	1.125	1.174	1.780	9.493	1.000	1.150	1.209	1.861	7.809	1.000	1.177	1.245	1.993	7.798
L(C)=8W L=6000	1.000	1.120	1.166	1.714	9.209	1.000	1.145	1.202	1.834	7.595	1.000	1.171	1.238	1.963	7.592
L(C)=8W L=12000	1.000	1.120	1.166	1.714	9.209	1.000	1.145	1.202	1.834	7.595	1.000	1.171	1.238	1.963	7.592

Table XIV — Values of (max delta T_c)/(max delta T_{c0})

I= 0.5   T(0)=4.2   T(I)=20.0 (OR ANY OTHER VALUE)

L(C)/W	L	M= 20.00					M= 25.00					M= 30.00				
		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W	L= 1000	1.000	1.026	1.035	1.137	1.683	1.000	1.032	1.046	1.170	1.850	1.000	1.038	1.053	1.203	2.016
L(C)=1W	L= 6000	1.000	1.015	1.021	1.082	1.411	1.000	1.019	1.027	1.102	1.511	1.000	1.023	1.032	1.122	1.611
L(C)=1W	L=12000	1.000	1.015	1.021	1.082	1.410	1.000	1.019	1.026	1.102	1.511	1.000	1.023	1.032	1.122	1.611
L(C)=2W	L= 1000	1.000	1.050	1.074	1.285	2.315	1.000	1.062	1.086	1.333	2.668	1.000	1.074	1.103	1.397	2.905
L(C)=2W	L= 6000	1.000	1.030	1.042	1.162	1.810	1.000	1.038	1.052	1.201	2.006	1.000	1.045	1.062	1.239	2.198
L(C)=2W	L=12000	1.000	1.030	1.042	1.162	1.810	1.000	1.038	1.052	1.201	2.005	1.000	1.045	1.062	1.239	2.198
L(C)=3W	L= 1000	1.000	1.074	1.103	1.317	2.987	1.000	1.092	1.127	1.690	3.453	1.000	1.109	1.151	1.501	3.909
L(C)=3W	L= 6000	1.000	1.045	1.062	1.240	2.199	1.000	1.056	1.077	1.296	2.483	1.000	1.066	1.091	1.352	2.761
L(C)=3W	L=12000	1.000	1.045	1.062	1.240	2.195	1.000	1.056	1.077	1.296	2.483	1.000	1.056	1.091	1.352	2.760
L(C)=4W	L= 1000	1.000	1.098	1.135	1.521	3.609	1.000	1.120	1.166	1.641	4.209	1.000	1.142	1.196	1.757	4.789
L(C)=4W	L= 6000	1.000	1.059	1.082	1.315	2.578	1.000	1.073	1.101	1.369	2.995	1.000	1.086	1.119	1.460	3.302
L(C)=4W	L=12000	1.000	1.059	1.082	1.315	2.578	1.000	1.073	1.101	1.388	2.994	1.000	1.086	1.119	1.460	3.301

I= 0.5   T(0)=2.8   T(I)=20.0 (OR ANY OTHER VALUE)

L(C)/W	L	M= 20.00					M= 25.00					M= 30.00				
		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W	L= 1000	1.000	1.027	1.038	1.145	1.725	1.000	1.034	1.047	1.180	1.902	1.000	1.040	1.056	1.215	2.078
L(C)=1W	L= 6000	1.000	1.019	1.026	1.100	1.501	1.000	1.023	1.032	1.125	1.624	1.000	1.028	1.039	1.149	1.745
L(C)=1W	L=12000	1.000	1.019	1.026	1.100	1.501	1.000	1.023	1.032	1.125	1.624	1.000	1.028	1.039	1.149	1.745
L(C)=2W	L= 1000	1.000	1.053	1.078	1.285	2.426	1.000	1.066	1.091	1.353	2.765	1.000	1.079	1.109	1.419	3.099
L(C)=2W	L= 6000	1.000	1.037	1.051	1.197	1.987	1.000	1.046	1.063	1.244	2.223	1.000	1.054	1.075	1.291	2.454
L(C)=2W	L=12000	1.000	1.037	1.051	1.197	1.987	1.000	1.046	1.063	1.244	2.222	1.000	1.054	1.075	1.291	2.454
L(C)=3W	L= 1000	1.000	1.079	1.109	1.420	3.103	1.000	1.097	1.138	1.517	3.591	1.000	1.115	1.159	1.612	8.066
L(C)=3W	L= 6000	1.000	1.055	1.075	1.291	2.457	1.000	1.067	1.093	1.359	2.797	1.000	1.080	1.110	1.425	3.129
L(C)=3W	L=12000	1.000	1.055	1.075	1.291	2.457	1.000	1.067	1.093	1.359	2.797	1.000	1.080	1.110	1.425	3.129
L(C)=4W	L= 1000	1.000	1.103	1.142	1.550	3.755	1.000	1.126	1.175	1.675	4.380	1.000	1.149	1.206	1.795	3.981
L(C)=4W	L= 6000	1.000	1.071	1.099	1.381	2.912	1.000	1.088	1.121	1.469	3.349	1.000	1.104	1.143	1.553	3.771
L(C)=4W	L=12000	1.000	1.071	1.099	1.381	2.912	1.000	1.088	1.121	1.469	3.348	1.000	1.104	1.143	1.553	3.770

I= 0.5   T(0)=1.4   T(I)=20.0 (OR ANY OTHER VALUE)

L(C)/W	L	M= 20.00					M= 25.00					M= 30.00				
		1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W	L= 1000	1.000	1.032	1.044	1.159	1.847	1.000	1.039	1.054	1.210	2.051	1.000	1.047	1.065	1.230	2.252
L(C)=1W	L= 6000	1.000	1.026	1.037	1.141	1.706	1.000	1.033	1.045	1.175	1.876	1.000	1.039	1.054	1.209	2.044
L(C)=1W	L=12000	1.000	1.026	1.037	1.141	1.706	1.000	1.033	1.045	1.175	1.876	1.000	1.039	1.054	1.209	2.044
L(C)=2W	L= 1000	1.000	1.062	1.086	1.330	2.657	1.000	1.064	1.088	1.407	3.043	1.000	1.090	1.125	1.483	3.419
L(C)=2W	L= 6000	1.000	1.052	1.071	1.275	2.382	1.000	1.064	1.088	1.340	2.704	1.000	1.075	1.108	1.403	3.019
L(C)=2W	L=12000	1.000	1.052	1.071	1.275	2.382	1.000	1.064	1.088	1.340	2.704	1.000	1.075	1.108	1.403	3.019
L(C)=3W	L= 1000	1.000	1.091	1.125	1.484	3.432	1.000	1.111	1.154	1.593	3.979	1.000	1.131	1.151	1.584	3.929
L(C)=3W	L= 6000	1.000	1.076	1.105	1.404	3.029	1.000	1.093	1.128	1.495	3.467	1.000	1.109	1.151	1.584	3.929
L(C)=3W	L=12000	1.000	1.076	1.105	1.404	3.029	1.000	1.093	1.128	1.495	3.467	1.000	1.109	1.151	1.584	4.507
L(C)=4W	L= 1000	1.000	1.118	1.153	1.630	4.172	1.000	1.146	1.199	1.768	4.862	1.000	1.169	1.233	1.900	5.519
L(C)=4W	L= 6000	1.000	1.098	1.136	1.526	3.649	1.000	1.120	1.166	1.642	4.227	1.000	1.161	1.195	1.752	8.778
L(C)=4W	L=12000	1.000	1.098	1.136	1.526	3.649	1.000	1.120	1.166	1.642	4.227	1.000	1.161	1.195	1.752	8.778

Table XV — Values of (max delta T_c)/(max delta T_{c0})

X = 1.0 T(0) = 4.2 T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W=	W= 20.00					W= 25.00					W= 30.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.026	1.035	1.137	1.685	1.000	1.032	1.044	1.170	1.652	1.000	1.038	1.053	1.203	2.017
L(C)=1W L= 6000	1.000	1.015	1.021	1.082	1.612	1.000	1.019	1.027	1.102	1.512	1.000	1.023	1.032	1.122	1.612
L(C)=1W L=12000	1.000	1.015	1.021	1.082	1.612	1.000	1.019	1.027	1.102	1.512	1.000	1.023	1.032	1.122	1.612
L(C)=2W L= 1000	1.000	1.050	1.070	1.269	2.350	1.000	1.063	1.087	1.334	2.672	1.000	1.074	1.103	1.397	2.990
L(C)=2W L= 6000	1.000	1.030	1.042	1.162	1.814	1.000	1.038	1.052	1.201	2.009	1.000	1.045	1.062	1.240	2.201
L(C)=2W L=12000	1.000	1.030	1.042	1.162	1.814	1.000	1.038	1.052	1.201	2.009	1.000	1.045	1.062	1.240	2.201
L(C)=3W L= 1000	1.000	1.075	1.103	1.398	2.937	1.000	1.092	1.127	1.491	3.463	1.000	1.109	1.151	1.582	3.918
L(C)=3W L= 6000	1.000	1.045	1.062	1.240	2.207	1.000	1.056	1.077	1.297	2.490	1.000	1.066	1.091	1.352	2.768
L(C)=3W L=12000	1.000	1.045	1.062	1.240	2.206	1.000	1.056	1.077	1.297	2.489	1.000	1.066	1.091	1.352	2.767
L(C)=4W L= 1000	1.000	1.098	1.132	1.522	3.626	1.000	1.120	1.166	1.642	4.224	1.000	1.142	1.196	1.758	4.804
L(C)=4W L= 6000	1.000	1.059	1.085	1.322	2.590	1.000	1.073	1.101	1.389	2.956	1.000	1.086	1.119	1.461	3.312
L(C)=4W L=12000	1.000	1.059	1.082	1.316	2.589	1.000	1.073	1.101	1.389	2.955	1.000	1.086	1.119	1.460	3.311

X = 1.0 T(0) = 2.8 T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W=	W= 20.00					W= 25.00					W= 30.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.027	1.038	1.145	1.729	1.000	1.034	1.047	1.181	1.906	1.000	1.040	1.056	1.216	2.081
L(C)=1W L= 6000	1.000	1.019	1.026	1.101	1.504	1.000	1.023	1.032	1.125	1.626	1.000	1.028	1.039	1.149	1.747
L(C)=1W L=12000	1.000	1.019	1.026	1.101	1.504	1.000	1.023	1.032	1.125	1.626	1.000	1.028	1.039	1.149	1.747
L(C)=2W L= 1000	1.000	1.054	1.074	1.286	2.437	1.000	1.066	1.092	1.354	2.775	1.000	1.079	1.109	1.420	3.108
L(C)=2W L= 6000	1.000	1.037	1.051	1.198	1.995	1.000	1.046	1.063	1.245	2.230	1.000	1.055	1.075	1.291	2.461
L(C)=2W L=12000	1.000	1.037	1.051	1.198	1.995	1.000	1.046	1.063	1.245	2.230	1.000	1.055	1.075	1.291	2.461
L(C)=3W L= 1000	1.000	1.079	1.109	1.421	3.123	1.000	1.097	1.134	1.519	3.610	1.000	1.115	1.159	1.614	4.088
L(C)=3W L= 6000	1.000	1.055	1.076	1.292	2.473	1.000	1.067	1.093	1.360	2.811	1.000	1.080	1.110	1.426	3.142
L(C)=3W L=12000	1.000	1.055	1.076	1.292	2.472	1.000	1.067	1.093	1.360	2.811	1.000	1.080	1.110	1.426	3.142
L(C)=4W L= 1000	1.000	1.103	1.143	1.552	3.789	1.000	1.127	1.175	1.677	4.411	1.000	1.149	1.206	1.797	5.010
L(C)=4W L= 6000	1.000	1.072	1.099	1.383	2.937	1.000	1.088	1.122	1.470	3.372	1.000	1.104	1.144	1.555	3.792
L(C)=4W L=12000	1.000	1.072	1.099	1.383	2.937	1.000	1.088	1.122	1.470	3.372	1.000	1.104	1.144	1.555	3.792

X = 1.0 T(0) = 1.8 T(1) = 20.0 (OR ANY OTHER VALUE)

W(C)/W=	W= 20.00					W= 25.00					W= 30.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.032	1.044	1.170	1.858	1.000	1.039	1.055	1.211	2.061	1.000	1.047	1.065	1.251	2.262
L(C)=1W L= 6000	1.000	1.027	1.037	1.142	1.715	1.000	1.033	1.046	1.176	1.885	1.000	1.039	1.054	1.209	2.052
L(C)=1W L=12000	1.000	1.027	1.037	1.142	1.715	1.000	1.033	1.046	1.176	1.885	1.000	1.039	1.054	1.209	2.052
L(C)=2W L= 1000	1.000	1.062	1.086	1.333	2.691	1.000	1.077	1.106	1.410	3.078	1.000	1.091	1.125	1.485	3.449
L(C)=2W L= 6000	1.000	1.052	1.072	1.278	2.411	1.000	1.064	1.088	1.342	2.731	1.000	1.076	1.105	1.405	3.044
L(C)=2W L=12000	1.000	1.052	1.072	1.278	2.411	1.000	1.064	1.088	1.342	2.731	1.000	1.076	1.105	1.405	3.044
L(C)=3W L= 1000	1.000	1.091	1.126	1.489	3.499	1.000	1.112	1.154	1.598	4.041	1.000	1.131	1.182	1.703	4.564
L(C)=3W L= 6000	1.000	1.076	1.105	1.408	3.086	1.000	1.093	1.129	1.499	3.533	1.000	1.110	1.152	1.587	3.977
L(C)=3W L=12000	1.000	1.076	1.105	1.408	3.086	1.000	1.093	1.129	1.499	3.533	1.000	1.110	1.152	1.587	3.977
L(C)=4W L= 1000	1.000	1.119	1.164	1.637	4.282	1.000	1.145	1.200	1.775	4.962	1.000	1.169	1.234	1.905	5.611
L(C)=4W L= 6000	1.000	1.099	1.137	1.532	3.741	1.000	1.121	1.167	1.647	4.311	1.000	1.181	1.196	1.757	6.855
L(C)=4W L=12000	1.000	1.099	1.137	1.532	3.741	1.000	1.121	1.167	1.647	4.311	1.000	1.181	1.196	1.757	6.855

Table XVI — Values of (max delta T_c)/(max delta T_{c0})

I = 2.0, T(0) = 4.2

	N= 20.00					N= 25.00					N= 30.00 (T(t)=20.0 OR ANY OTHER VALUE)				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L=1000	1.000	1.026	1.036	1.138	1.692	1.000	1.032	1.044	1.171	1.858	1.000	1.038	1.053	1.204	2.023
L(C)=1W L=6000	1.000	1.016	1.021	1.083	1.417	1.000	1.019	1.027	1.103	1.517	1.000	1.023	1.032	1.123	1.617
L(C)=1W L=12000	1.000	1.016	1.021	1.083	1.417	1.000	1.019	1.027	1.103	1.517	1.000	1.021	1.032	1.123	1.616
L(C)=2W L=1000	1.000	1.051	1.070	1.271	2.372	1.000	1.038	1.087	1.336	2.692	1.000	1.085	1.103	1.359	3.008
L(C)=2W L=6000	1.000	1.031	1.042	1.164	1.830	1.000	1.038	1.052	1.203	2.023	1.000	1.045	1.062	1.241	2.215
L(C)=2W L=12000	1.000	1.031	1.042	1.164	1.829	1.000	1.038	1.052	1.203	2.023	1.000	1.045	1.062	1.241	2.214
L(C)=3W L=1000	1.000	1.075	1.104	1.401	3.040	1.000	1.052	1.078	1.394	3.502	1.000	1.066	1.151	1.554	3.954
L(C)=3W L=6000	1.000	1.045	1.063	1.283	2.237	1.000	1.056	1.077	1.299	2.517	1.000	1.066	1.092	1.358	2.794
L(C)=3W L=12000	1.000	1.045	1.063	1.283	2.237	1.000	1.056	1.077	1.299	2.517	1.000	1.066	1.092	1.354	2.791
L(C)=4W L=1000	1.000	1.060	1.086	1.328	2.694	1.000	1.073	1.167	1.647	4.287	1.000	1.143	1.197	1.762	4.662
L(C)=4W L=6000	1.000	1.060	1.083	1.320	2.639	1.000	1.073	1.101	1.393	3.001	1.000	1.087	1.120	1.464	3.354
L(C)=4W L=12000	1.000	1.060	1.081	1.320	2.638	1.000	1.073	1.101	1.392	3.000	1.000	1.087	1.120	1.463	3.353

I = 2.0, T(0) = 2.8

	N= 20.00					N= 25.00					N= 30.00 (T(t)=20.0 OR ANY OTHER VALUE)				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L=1000	1.000	1.028	1.038	1.147	1.744	1.000	1.034	1.047	1.182	1.919	1.000	1.041	1.056	1.217	2.093
L(C)=1W L=6000	1.000	1.019	1.026	1.102	1.515	1.000	1.024	1.033	1.126	1.636	1.000	1.028	1.039	1.150	1.757
L(C)=1W L=12000	1.000	1.019	1.026	1.102	1.515	1.000	1.024	1.033	1.126	1.636	1.000	1.028	1.039	1.150	1.756
L(C)=2W L=1000	1.000	1.038	1.075	1.290	2.481	1.000	1.067	1.092	1.357	2.815	1.000	1.079	1.109	1.423	3.145
L(C)=2W L=6000	1.000	1.038	1.052	1.201	2.028	1.000	1.046	1.064	1.247	2.260	1.000	1.055	1.076	1.293	2.489
L(C)=2W L=12000	1.000	1.038	1.052	1.201	2.028	1.000	1.046	1.064	1.247	2.260	1.000	1.055	1.076	1.293	2.489
L(C)=3W L=1000	1.000	1.055	1.110	1.428	3.210	1.000	1.068	1.135	1.525	3.689	1.000	1.116	1.160	1.619	4.157
L(C)=3W L=6000	1.000	1.055	1.077	1.297	2.538	1.000	1.068	1.094	1.364	2.871	1.000	1.080	1.111	1.430	3.197
L(C)=3W L=12000	1.000	1.055	1.077	1.297	2.538	1.000	1.068	1.094	1.364	2.871	1.000	1.080	1.111	1.430	3.197
L(C)=4W L=1000	1.000	1.105	1.185	1.562	3.931	1.000	1.128	1.177	1.686	4.539	1.000	1.150	1.208	1.805	5.129
L(C)=4W L=6000	1.000	1.073	1.101	1.391	3.044	1.000	1.089	1.123	1.477	3.469	1.000	1.104	1.185	1.560	3.882
L(C)=4W L=12000	1.000	1.073	1.101	1.391	3.044	1.000	1.089	1.123	1.477	3.469	1.000	1.104	1.185	1.560	3.882

I = 2.0, T(0) = 1.8

	N= 20.00					N= 25.00					N= 30.00 (T(t)=20.0 OR ANY OTHER VALUE)				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L=1000	1.000	1.033	1.045	1.175	1.907	1.000	1.040	1.056	1.215	2.106	1.000	1.048	1.066	1.255	2.301
L(C)=1W L=6000	1.000	1.027	1.038	1.146	1.755	1.000	1.033	1.046	1.179	1.920	1.000	1.040	1.055	1.212	2.085
L(C)=1W L=12000	1.000	1.027	1.038	1.146	1.755	1.000	1.033	1.046	1.179	1.920	1.000	1.040	1.055	1.212	2.085
L(C)=2W L=1000	1.000	1.064	1.089	1.385	2.845	1.000	1.078	1.108	1.420	3.210	1.000	1.092	1.127	1.494	3.573
L(C)=2W L=6000	1.000	1.053	1.074	1.288	2.538	1.000	1.065	1.090	1.350	2.884	1.000	1.077	1.106	1.412	3.148
L(C)=2W L=12000	1.000	1.053	1.074	1.288	2.538	1.000	1.065	1.090	1.350	2.884	1.000	1.077	1.106	1.412	3.148
L(C)=3W L=1000	1.000	1.098	1.130	1.510	3.811	1.000	1.114	1.157	1.615	4.315	1.000	1.133	1.184	1.718	4.813
L(C)=3W L=6000	1.000	1.078	1.108	1.425	3.348	1.000	1.095	1.131	1.513	3.770	1.000	1.111	1.158	1.600	4.187
L(C)=3W L=12000	1.000	1.078	1.108	1.425	3.348	1.000	1.095	1.131	1.513	3.770	1.000	1.111	1.158	1.600	4.187
L(C)=4W L=1000	1.000	1.122	1.170	1.669	4.806	1.000	1.187	1.204	1.801	5.415	1.000	1.172	1.238	1.929	6.016
L(C)=4W L=6000	1.000	1.102	1.181	1.558	4.185	1.000	1.123	1.170	1.669	4.698	1.000	1.143	1.198	1.776	5.199
L(C)=4W L=12000	1.000	1.102	1.181	1.558	4.185	1.000	1.123	1.170	1.669	4.698	1.000	1.143	1.198	1.776	5.199

Table XVII — Values of (max delta T_c)/(max delta T_{c0})

I= 3.0 T(0)=4.2 T(1)=20.0 (OR ANY OTHER VALUE)

	W= 20.00					W= 25.00					W= 30.00				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.026	1.036	1.139	1.705	1.000	1.032	1.045	1.172	1.870	1.000	1.038	1.053	1.205	2.034
L(C)=1W L= 6000	1.000	1.016	1.022	1.084	1.427	1.000	1.019	1.027	1.104	1.526	1.000	1.023	1.032	1.124	1.628
L(C)=1W L=12000	1.000	1.016	1.022	1.084	1.427	1.000	1.019	1.027	1.104	1.525	1.000	1.023	1.032	1.124	1.628
L(C)=2W L= 1000	1.000	1.051	1.071	1.275	2.410	1.000	1.063	1.087	1.339	2.727	1.000	1.075	1.104	1.401	3.040
L(C)=2W L= 6000	1.000	1.031	1.043	1.167	1.858	1.000	1.038	1.053	1.205	2.048	1.000	1.045	1.063	1.243	2.237
L(C)=2W L=12000	1.000	1.031	1.043	1.167	1.857	1.000	1.038	1.053	1.205	2.047	1.000	1.045	1.063	1.243	2.237
L(C)=3W L= 1000	1.000	1.076	1.105	1.408	3.114	1.000	1.093	1.129	1.499	3.569	1.000	1.110	1.152	1.589	4.016
L(C)=3W L= 6000	1.000	1.046	1.064	1.248	2.292	1.000	1.056	1.078	1.303	2.566	1.000	1.067	1.092	1.358	2.838
L(C)=3W L=12000	1.000	1.046	1.064	1.247	2.291	1.000	1.056	1.078	1.303	2.566	1.000	1.067	1.092	1.358	2.837
L(C)=4W L= 1000	1.000	1.100	1.138	1.536	3.816	1.000	1.122	1.168	1.654	4.397	1.000	1.143	1.198	1.769	4.963
L(C)=4W L= 6000	1.000	1.061	1.084	1.327	2.729	1.000	1.074	1.102	1.398	3.081	1.000	1.087	1.121	1.469	3.427
L(C)=4W L=12000	1.000	1.061	1.084	1.327	2.728	1.000	1.074	1.102	1.398	3.080	1.000	1.087	1.121	1.468	3.426

I= 3.0 T(0)=2.8 T(1)=20.0 (OR ANY OTHER VALUE)

	W= 20.00					W= 25.00					W= 30.00				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.028	1.039	1.150	1.771	1.000	1.035	1.048	1.185	1.942	1.000	1.041	1.057	1.219	2.114
L(C)=1W L= 6000	1.000	1.019	1.027	1.104	1.535	1.000	1.024	1.033	1.128	1.654	1.000	1.028	1.039	1.152	1.772
L(C)=1W L=12000	1.000	1.019	1.027	1.104	1.535	1.000	1.024	1.033	1.128	1.653	1.000	1.028	1.039	1.152	1.772
L(C)=2W L= 1000	1.000	1.055	1.076	1.297	2.562	1.000	1.068	1.093	1.363	2.887	1.000	1.080	1.110	1.428	3.210
L(C)=2W L= 6000	1.000	1.038	1.053	1.206	2.089	1.000	1.047	1.065	1.252	2.314	1.000	1.055	1.077	1.297	2.538
L(C)=2W L=12000	1.000	1.038	1.053	1.206	2.089	1.000	1.047	1.065	1.252	2.314	1.000	1.055	1.077	1.297	2.538
L(C)=3W L= 1000	1.000	1.081	1.113	1.440	3.372	1.000	1.099	1.137	1.535	3.832	1.000	1.117	1.161	1.628	4.287
L(C)=3W L= 6000	1.000	1.057	1.078	1.307	2.662	1.000	1.069	1.095	1.372	2.979	1.000	1.081	1.112	1.437	3.296
L(C)=3W L=12000	1.000	1.057	1.078	1.307	2.662	1.000	1.069	1.095	1.372	2.979	1.000	1.081	1.112	1.437	3.296
L(C)=4W L= 1000	1.000	1.107	1.148	1.580	4.201	1.000	1.129	1.179	1.701	4.775	1.000	1.152	1.210	1.818	5.342
L(C)=4W L= 6000	1.000	1.074	1.103	1.405	3.253	1.000	1.090	1.125	1.488	3.650	1.000	1.106	1.146	1.570	4.045
L(C)=4W L=12000	1.000	1.074	1.103	1.405	3.253	1.000	1.090	1.125	1.488	3.649	1.000	1.106	1.146	1.570	4.045

I= 3.0 T(0)=1.4 T(1)=20.0 (OR ANY OTHER VALUE)

	W= 20.00					W= 25.00					W= 30.00				
W(C)/W=	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.034	1.047	1.185	2.002	1.000	1.041	1.057	1.223	2.184	1.000	1.048	1.067	1.261	2.372
L(C)=1W L= 6000	1.000	1.028	1.039	1.154	1.835	1.000	1.034	1.048	1.185	1.986	1.000	1.040	1.056	1.217	2.144
L(C)=1W L=12000	1.000	1.028	1.039	1.154	1.834	1.000	1.034	1.048	1.185	1.986	1.000	1.040	1.056	1.217	2.143
L(C)=2W L= 1000	1.000	1.067	1.093	1.369	3.172	1.000	1.080	1.111	1.439	3.481	1.000	1.094	1.130	1.510	3.811
L(C)=2W L= 6000	1.000	1.056	1.077	1.307	2.815	1.000	1.067	1.093	1.365	3.072	1.000	1.078	1.108	1.425	3.348
L(C)=2W L=12000	1.000	1.056	1.077	1.307	2.815	1.000	1.067	1.093	1.365	3.072	1.000	1.078	1.108	1.425	3.348
L(C)=3W L= 1000	1.000	1.099	1.137	1.550	4.547	1.000	1.117	1.163	1.648	4.900	1.000	1.136	1.189	1.746	5.314
L(C)=3W L= 6000	1.000	1.082	1.114	1.458	3.977	1.000	1.098	1.136	1.540	4.267	1.000	1.114	1.157	1.623	4.612
L(C)=3W L=12000	1.000	1.082	1.114	1.458	3.977	1.000	1.098	1.136	1.540	4.267	1.000	1.114	1.157	1.623	4.612
L(C)=4W L= 1000	1.000	1.129	1.179	1.729	6.180	1.000	1.153	1.212	1.850	6.451	1.000	1.176	1.244	1.970	6.875
L(C)=4W L= 6000	1.000	1.107	1.149	1.608	5.369	1.000	1.127	1.176	1.709	5.582	1.000	1.147	1.203	1.811	5.933
L(C)=4W L=12000	1.000	1.107	1.149	1.608	5.369	1.000	1.127	1.176	1.709	5.582	1.000	1.147	1.203	1.811	5.933

Table XVIII — Values of (max delta T_o)/(max delta T_{co})

I= 4.0   T(0)=4.2

W(C)/WM	W= 20.00					W= 25.00					W= 30.00 T(1)=20.0 (OR ANY OTHER VALUE)				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.026	1.037	1.142	1.724	1.000	1.033	1.045	1.174	1.886	1.000	1.039	1.053	1.207	2.049
L(C)=1W L= 6000	1.000	1.016	1.022	1.086	1.441	1.000	1.020	1.027	1.105	1.538	1.000	1.023	1.032	1.125	1.635
L(C)=1W L=12000	1.000	1.016	1.022	1.085	1.441	1.000	1.020	1.027	1.105	1.537	1.000	1.023	1.032	1.125	1.635
L(C)=2W L= 1000	1.000	1.052	1.072	1.280	2.467	1.000	1.064	1.088	1.343	2.777	1.000	1.076	1.104	1.405	3.086
L(C)=2W L= 6000	1.000	1.032	1.044	1.171	1.900	1.000	1.039	1.054	1.208	2.085	1.000	1.046	1.063	1.246	2.270
L(C)=2W L=12000	1.000	1.032	1.044	1.171	1.899	1.000	1.039	1.054	1.208	2.084	1.000	1.046	1.063	1.246	2.270
L(C)=3W L= 1000	1.000	1.077	1.107	1.416	3.228	1.000	1.094	1.130	1.507	2.640	1.000	1.111	1.153	1.596	4.108
L(C)=3W L= 6000	1.000	1.047	1.065	1.254	2.377	1.000	1.057	1.079	1.309	2.639	1.000	1.067	1.093	1.363	2.905
L(C)=3W L=12000	1.000	1.047	1.065	1.254	2.376	1.000	1.057	1.079	1.308	2.639	1.000	1.067	1.093	1.362	2.904
L(C)=4W L= 1000	1.000	1.101	1.140	1.549	4.007	1.000	1.123	1.170	1.665	4.564	1.000	1.144	1.200	1.778	5.538
L(C)=4W L= 6000	1.000	1.062	1.086	1.337	2.872	1.000	1.075	1.104	1.407	3.204	1.000	1.088	1.122	1.475	3.537
L(C)=4W L=12000	1.000	1.062	1.086	1.336	2.871	1.000	1.075	1.104	1.406	3.203	1.000	1.088	1.122	1.475	3.537

I= 4.0   T(0)=2.8

W(C)/WM	W= 20.00					W= 25.00					W= 30.00 T(1)=20.0 (OR ANY OTHER VALUE)				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.029	1.040	1.155	1.811	1.000	1.035	1.049	1.188	1.976	1.000	1.041	1.057	1.222	2.164
L(C)=1W L= 6000	1.000	1.020	1.028	1.108	1.567	1.000	1.024	1.034	1.131	1.680	1.000	1.029	1.040	1.154	1.795
L(C)=1W L=12000	1.000	1.020	1.028	1.108	1.567	1.000	1.024	1.034	1.131	1.680	1.000	1.029	1.040	1.154	1.795
L(C)=2W L= 1000	1.000	1.057	1.079	1.308	2.690	1.000	1.069	1.095	1.372	2.996	1.000	1.081	1.112	1.436	3.308
L(C)=2W L= 6000	1.000	1.039	1.055	1.215	2.189	1.000	1.048	1.066	1.259	2.397	1.000	1.056	1.078	1.303	2.613
L(C)=2W L=12000	1.000	1.039	1.055	1.215	2.189	1.000	1.048	1.066	1.259	2.398	1.000	1.056	1.078	1.303	2.613
L(C)=3W L= 1000	1.000	1.084	1.116	1.459	3.641	1.000	1.101	1.140	1.550	3.155	1.000	1.118	1.164	1.641	4.480
L(C)=3W L= 6000	1.000	1.058	1.081	1.321	2.874	1.000	1.070	1.097	1.384	3.155	1.000	1.082	1.114	1.447	3.451
L(C)=3W L=12000	1.000	1.058	1.081	1.321	2.674	1.000	1.070	1.097	1.383	3.155	1.000	1.082	1.114	1.447	3.451
L(C)=4W L= 1000	1.000	1.110	1.152	1.607	4.678	1.000	1.132	1.183	1.723	5.163	1.000	1.158	1.213	1.837	5.680
L(C)=4W L= 6000	1.000	1.077	1.107	1.426	3.630	1.000	1.092	1.128	1.505	3.954	1.000	1.107	1.149	1.585	4.308
L(C)=4W L=12000	1.000	1.077	1.107	1.426	3.630	1.000	1.092	1.128	1.505	3.953	1.000	1.107	1.149	1.585	4.308

I= 4.0   T(0)=1.4

W(C)/WM	W= 20.00					W= 25.00					W= 30.00 T(1)=20.0 (OR ANY OTHER VALUE)				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=1W L= 1000	1.000	1.037	1.051	1.201	2.176	1.000	1.043	1.060	1.235	2.318	1.000	1.050	1.069	1.271	2.866
L(C)=1W L= 6000	1.000	1.030	1.042	1.167	1.982	1.000	1.036	1.049	1.195	2.098	1.000	1.041	1.057	1.225	2.238
L(C)=1W L=12000	1.000	1.030	1.042	1.167	1.982	1.000	1.036	1.049	1.195	2.098	1.000	1.041	1.057	1.225	2.238
L(C)=2W L= 1000	1.000	1.072	1.100	1.407	3.087	1.000	1.084	1.117	1.468	3.509	1.000	1.097	1.134	1.534	4.229
L(C)=2W L= 6000	1.000	1.060	1.083	1.338	3.436	1.000	1.070	1.097	1.389	3.509	1.000	1.081	1.112	1.485	3.703
L(C)=2W L=12000	1.000	1.060	1.083	1.338	3.436	1.000	1.070	1.097	1.389	3.509	1.000	1.081	1.112	1.485	3.703
L(C)=3W L= 1000	1.000	1.106	1.148	1.618	6.580	1.000	1.123	1.171	1.700	6.171	1.000	1.141	1.195	1.789	6.283
L(C)=3W L= 6000	1.000	1.088	1.123	1.515	5.792	1.000	1.102	1.142	1.583	5.391	1.000	1.117	1.163	1.658	5.046
L(C)=3W L=12000	1.000	1.088	1.123	1.515	5.792	1.000	1.102	1.142	1.583	5.391	1.000	1.117	1.163	1.658	5.046
L(C)=4W L= 1000	1.000	1.140	1.195	1.835	11.388	1.000	1.160	1.223	1.929	9.096	1.000	1.182	1.253	2.036	8.718
L(C)=4W L= 6000	1.000	1.116	1.162	1.697	10.214	1.000	1.134	1.186	1.776	7.920	1.000	1.152	1.211	1.865	7.538
L(C)=4W L=12000	1.000	1.116	1.162	1.697	10.214	1.000	1.134	1.186	1.776	7.920	1.000	1.152	1.211	1.865	7.538

Table XIX — Values of (max delta T_d)/(max delta T_{c0})

K = 1.0

T(0)=4.2

		W= 80.00					W=100.00				T(I)=20.0 (OR ANY OTHER VALUE) W=120.00				
W(C)/Wm		0.25	0.50	0.75	0.80	1.00	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25

T(0)=2.8

		W= 80.00					W=100.00				T(I)=20.0 (OR ANY OTHER VALUE) W=120.00				
W(C)/Wm		0.25	0.50	0.75	0.80	1.00	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25

T(0)=1.4

		W= 90.00					W=100.00				T(I)=20.0 (OR ANY OTHER VALUE) W=120.00				
W(C)/Wm		0.25	0.50	0.75	0.80	1.00	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25

Table XX—Values of (max delta T_c)/(max delta T_{c0})

I= 2.0   T(0)=4.2   T(1)=20.0 (OR ANY OTHER VALUE)

M(C)/kW	W= 80.00					W=100.00					W=120.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.046	1.053	1.248	2.221	1.000	1.057	1.079	1.303	2.517	1.068	1.094	1.362	2.809
L(C)=0.5W L= 6000	1.000	1.016	1.022	1.085	1.425	1.000	1.020	1.027	1.106	1.529	1.028	1.033	1.126	1.632
L(C)=0.5W L=12000	1.000	1.015	1.021	1.082	1.412	1.000	1.019	1.027	1.102	1.512	1.023	1.032	1.122	1.612
L(C)=1.0W L= 1000	1.000	1.089	1.128	1.477	3.398	1.000	1.110	1.153	1.589	3.948	1.131	1.181	1.698	4.498
L(C)=1.0W L= 6000	1.000	1.031	1.043	1.167	1.860	1.000	1.039	1.054	1.208	2.061	1.046	1.064	1.240	2.239
L(C)=1.0W L=12000	1.000	1.030	1.042	1.162	1.818	1.000	1.038	1.052	1.201	2.009	1.045	1.062	1.287	2.201
L(C)=1.5W L= 1000	1.000	1.131	1.181	1.699	4.502	1.000	1.161	1.222	1.657	5.296	1.189	1.262	2.010	6.057
L(C)=1.5W L= 6000	1.000	1.046	1.064	1.240	2.245	1.000	1.056	1.077	1.297	2.537	1.068	1.091	1.352	2.823
L(C)=1.5W L=12000	1.000	1.045	1.062	1.240	2.207	1.000	1.056	1.077	1.297	2.490	1.066	1.094	1.352	2.760
L(C)=2.0W L= 1000	1.000	1.170	1.236	1.909	5.562	1.000	1.208	1.287	2.109	6.557	1.243	1.316	2.297	7.500
L(C)=2.0W L= 6000	1.000	1.061	1.084	1.326	2.640	1.000	1.075	1.104	1.402	3.017	1.089	1.123	1.475	3.305
L(C)=2.0W L=12000	1.000	1.059	1.082	1.316	2.590	1.000	1.073	1.101	1.389	2.956	1.086	1.119	1.461	3.312

I= 2.0   T(0)=2.8   T(1)=20.0 (OR ANY OTHER VALUE)

M(C)/kW	W= 80.00					W=100.00					W=120.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.047	1.064	1.249	2.245	1.000	1.058	1.080	1.309	2.545	1.069	1.095	1.368	2.841
L(C)=0.5W L= 6000	1.000	1.019	1.026	1.102	1.510	1.000	1.024	1.033	1.127	1.634	1.028	1.039	1.151	1.757
L(C)=0.5W L=12000	1.000	1.019	1.026	1.101	1.504	1.000	1.023	1.032	1.125	1.626	1.028	1.039	1.149	1.747
L(C)=1.0W L= 1000	1.000	1.091	1.126	1.485	3.435	1.000	1.112	1.155	1.598	4.000	1.133	1.184	1.709	4.552
L(C)=1.0W L= 6000	1.000	1.037	1.051	1.200	2.007	1.000	1.046	1.064	1.248	2.245	1.055	1.076	1.295	2.479
L(C)=1.0W L=12000	1.000	1.037	1.051	1.198	1.995	1.000	1.046	1.063	1.245	2.230	1.055	1.075	1.291	2.461
L(C)=1.5W L= 1000	1.000	1.133	1.184	1.710	4.563	1.000	1.163	1.225	1.870	5.368	1.192	1.265	2.023	6.124
L(C)=1.5W L= 6000	1.000	1.055	1.077	1.296	2.491	1.000	1.068	1.094	1.364	2.834	1.081	1.112	1.431	3.169
L(C)=1.5W L=12000	1.000	1.055	1.076	1.292	2.473	1.000	1.067	1.093	1.360	2.811	1.080	1.110	1.426	3.142
L(C)=2.0W L= 1000	1.000	1.173	1.239	1.923	5.648	1.000	1.210	1.291	2.123	6.648	1.246	1.340	2.313	7.592
L(C)=2.0W L= 6000	1.000	1.073	1.100	1.388	2.961	1.000	1.089	1.123	1.476	3.401	1.105	1.145	1.561	3.627
L(C)=2.0W L=12000	1.000	1.072	1.099	1.383	2.937	1.000	1.088	1.122	1.470	3.372	1.104	1.144	1.565	3.792

I= 2.0   T(0)=1.4   T(1)=20.0 (OR ANY OTHER VALUE)

M(C)/kW	W= 80.00					W=100.00					W=120.00			
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.049	1.068	1.262	2.320	1.000	1.061	1.084	1.325	2.632	1.072	1.100	1.386	2.941
L(C)=0.5W L= 6000	1.000	1.027	1.037	1.142	1.716	1.000	1.033	1.046	1.176	1.886	1.039	1.054	1.210	2.054
L(C)=0.5W L=12000	1.000	1.027	1.037	1.142	1.715	1.000	1.033	1.046	1.176	1.885	1.039	1.054	1.209	2.052
L(C)=1.0W L= 1000	1.000	1.095	1.132	1.510	3.585	1.000	1.117	1.162	1.627	4.168	1.139	1.192	1.741	4.735
L(C)=1.0W L= 6000	1.000	1.052	1.072	1.278	2.413	1.000	1.064	1.089	1.342	2.733	1.076	1.105	1.405	3.047
L(C)=1.0W L=12000	1.000	1.052	1.072	1.278	2.411	1.000	1.064	1.088	1.342	2.731	1.076	1.105	1.405	3.044
L(C)=1.5W L= 1000	1.000	1.139	1.192	1.745	4.795	1.000	1.170	1.235	1.906	5.608	1.199	1.275	2.065	6.386
L(C)=1.5W L= 6000	1.000	1.076	1.105	1.408	3.089	1.000	1.093	1.129	1.500	3.543	1.110	1.152	1.587	3.982
L(C)=1.5W L=12000	1.000	1.076	1.105	1.408	3.086	1.000	1.093	1.129	1.499	3.539	1.110	1.152	1.588	3.977
L(C)=2.0W L= 1000	1.000	1.180	1.249	1.966	5.948	1.000	1.218	1.302	2.169	6.954	1.254	1.352	2.360	7.899
L(C)=2.0W L= 6000	1.000	1.099	1.137	1.533	3.745	1.000	1.121	1.167	1.648	4.316	1.142	1.196	1.758	4.861
L(C)=2.0W L=12000	1.000	1.099	1.137	1.532	3.741	1.000	1.121	1.167	1.647	4.311	1.143	1.196	1.757	4.855

Table XXI — Values of (max delta T_c)/(max delta T_{c0})

$I = 4.0$ — $T(0) = 4.2$ / $T(I) = 20.0$ (OR ANY OTHER VALUE)

$L(C)$	L	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
0.5W	1000	1.000	1.046	1.063	1.245	2.226	1.000	1.057	1.079	1.304	2.523	1.000	1.068	1.094	1.362	2.815
0.5W	6000	1.000	1.016	1.022	1.086	1.431	1.000	1.020	1.028	1.106	1.534	1.000	1.024	1.033	1.127	1.636
0.5W	12000	1.000	1.016	1.021	1.083	1.417	1.000	1.019	1.027	1.103	1.517	1.000	1.023	1.032	1.123	1.617
1.0W	1000	1.000	1.090	1.124	1.479	3.410	1.000	1.111	1.153	1.590	3.968	1.000	1.131	1.181	1.699	4.513
1.0W	6000	1.000	1.032	1.044	1.169	1.856	1.000	1.039	1.053	1.209	2.056	1.000	1.047	1.064	1.249	2.253
1.0W	12000	1.000	1.031	1.042	1.164	1.830	1.000	1.038	1.052	1.203	2.023	1.000	1.045	1.062	1.241	2.215
1.5W	1000	1.000	1.131	1.182	1.702	4.545	1.000	1.161	1.223	1.860	5.334	1.000	1.189	1.262	2.012	6.094
1.5W	6000	1.000	1.047	1.065	1.251	2.277	1.000	1.058	1.080	1.309	2.518	1.000	1.068	1.095	1.366	2.850
1.5W	12000	1.000	1.045	1.063	1.243	2.237	1.000	1.056	1.077	1.299	2.566	1.000	1.066	1.092	1.354	2.790
2.0W	1000	1.000	1.171	1.236	1.918	5.632	1.000	1.208	1.288	2.112	6.621	1.000	1.243	1.337	2.301	7.559
2.0W	6000	1.000	1.062	1.085	1.330	2.692	1.000	1.076	1.105	1.405	3.064	1.000	1.089	1.124	1.478	3.228
2.0W	12000	1.000	1.060	1.083	1.320	2.639	1.000	1.073	1.101	1.393	3.001	1.000	1.087	1.120	1.464	3.354

$I = 4.0$ — $T(0) = 2.8$ / $T(I) = 20.0$ (OR ANY OTHER VALUE)

$L(C)$	L	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
0.5W	1000	1.000	1.047	1.065	1.250	2.260	1.000	1.058	1.080	1.310	2.559	1.000	1.069	1.096	1.369	2.854
0.5W	6000	1.000	1.019	1.026	1.103	1.522	1.000	1.024	1.033	1.126	1.604	1.000	1.028	1.039	1.152	1.766
0.5W	12000	1.000	1.019	1.026	1.102	1.515	1.000	1.024	1.033	1.126	1.636	1.000	1.028	1.039	1.150	1.757
1.0W	1000	1.000	1.103	1.126	1.489	3.402	1.000	1.113	1.156	1.602	4.004	1.000	1.133	1.184	1.712	4.593
1.0W	6000	1.000	1.038	1.053	1.204	2.041	1.000	1.047	1.065	1.247	2.276	1.000	1.056	1.077	1.297	2.508
1.0W	12000	1.000	1.038	1.052	1.201	2.028	1.000	1.046	1.065	1.247	2.260	1.000	1.055	1.076	1.293	2.489
1.5W	1000	1.000	1.134	1.185	1.716	4.663	1.000	1.164	1.226	1.875	5.453	1.000	1.192	1.266	2.028	6.214
1.5W	6000	1.000	1.056	1.078	1.301	2.558	1.000	1.069	1.094	1.369	2.895	1.000	1.081	1.112	1.435	3.225
1.5W	12000	1.000	1.055	1.077	1.297	2.538	1.000	1.068	1.094	1.364	2.871	1.000	1.080	1.111	1.430	3.197
2.0W	1000	1.000	1.174	1.241	1.933	5.800	1.000	1.211	1.292	2.132	6.786	1.000	1.247	1.341	2.320	7.718
2.0W	6000	1.000	1.074	1.102	1.396	3.071	1.000	1.090	1.124	1.483	3.500	1.000	1.106	1.146	1.567	3.918
2.0W	12000	1.000	1.073	1.101	1.391	3.084	1.000	1.089	1.123	1.477	3.469	1.000	1.104	1.145	1.560	3.882

$I = 4.0$ — $T(0) = 1.4$ / $T(I) = 20.0$ (OR ANY OTHER VALUE)

$L(C)$	L	W=80.00 1.00	0.80	0.75	0.50	0.25	W=100.00 1.00	0.80	0.75	0.50	0.25	W=120.00 1.00	0.80	0.75	0.50	0.25
0.5W	1000	1.000	1.050	1.069	1.268	2.376	1.000	1.061	1.085	1.329	2.602	1.000	1.073	1.101	1.390	2.987
0.5W	6000	1.000	1.027	1.038	1.146	1.757	1.000	1.033	1.046	1.180	1.921	1.000	1.040	1.055	1.213	2.086
0.5W	12000	1.000	1.027	1.038	1.146	1.755	1.000	1.033	1.046	1.179	1.920	1.000	1.040	1.055	1.212	2.085
1.0W	1000	1.000	1.097	1.134	1.524	3.763	1.000	1.119	1.164	1.638	4.328	1.000	1.140	1.193	1.751	4.862
1.0W	6000	1.000	1.053	1.074	1.288	2.541	1.000	1.065	1.090	1.351	2.847	1.000	1.077	1.106	1.413	3.148
1.0W	12000	1.000	1.053	1.074	1.288	2.538	1.000	1.065	1.090	1.350	2.844	1.000	1.077	1.106	1.412	3.148
1.5W	1000	1.000	1.142	1.196	1.768	5.155	1.000	1.172	1.238	1.928	5.928	1.000	1.201	1.278	2.082	6.677
1.5W	6000	1.000	1.078	1.108	1.426	3.352	1.000	1.095	1.132	1.513	3.774	1.000	1.111	1.154	1.601	4.192
1.5W	12000	1.000	1.078	1.108	1.425	3.388	1.000	1.095	1.131	1.513	3.770	1.000	1.111	1.154	1.600	4.187
2.0W	1000	1.000	1.184	1.255	2.000	6.546	1.000	1.221	1.306	2.198	7.475	1.000	1.257	1.355	2.385	8.364
2.0W	6000	1.000	1.102	1.142	1.559	4.190	1.000	1.123	1.171	1.670	4.700	1.000	1.144	1.199	1.777	5.206
2.0W	12000	1.000	1.102	1.141	1.558	4.185	1.000	1.123	1.170	1.669	4.694	1.000	1.143	1.198	1.776	5.199

Table XXII — Values of $(\text{max delta } T_o)/(\text{max delta } T_{co})$

I = 6.0, T(0) = 4.2

W(C)/W	W=80.00					W=100.00					T(1)=20.0 (OR ANY OTHER VALUE) W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	1.000	1.046	1.064	1.296	2.241	1.000	1.057	1.079	1.305	2.538	1.000	1.068	1.094	1.363	2.825
L(C)=0.5W L=6000	1.000	1.016	1.022	1.087	1.441	1.000	1.020	1.028	1.107	1.543	1.000	1.024	1.033	1.128	1.644
L(C)=0.5W L=12000	1.000	1.016	1.022	1.084	1.427	1.000	1.019	1.027	1.104	1.526	1.000	1.023	1.032	1.124	1.624
L(C)=1.0W L=1000	1.000	1.090	1.124	1.482	3.448	1.000	1.111	1.153	1.593	4.003	1.000	1.131	1.182	1.702	4.585
L(C)=1.0W L=6000	1.000	1.032	1.044	1.172	1.886	1.000	1.039	1.055	1.242	2.082	1.000	1.047	1.065	1.251	2.237
L(C)=1.0W L=12000	1.000	1.031	1.043	1.167	1.858	1.000	1.038	1.053	1.235	2.048	1.000	1.045	1.063	1.243	2.237
L(C)=1.5W L=1000	1.000	1.135	1.182	1.707	4.619	1.000	1.165	1.231	1.865	5.402	1.000	1.193	1.261	2.016	6.157
L(C)=1.5W L=6000	1.000	1.048	1.066	1.256	2.314	1.000	1.058	1.078	1.303	2.617	1.000	1.067	1.092	1.369	2.897
L(C)=1.5W L=12000	1.000	1.046	1.064	1.248	2.292	1.000	1.056	1.078	1.303	2.566	1.000	1.067	1.092	1.358	2.838
L(C)=2.0W L=1000	1.000	1.172	1.238	1.922	5.753	1.000	1.209	1.294	2.119	6.731	1.000	1.244	1.338	2.307	7.659
L(C)=2.0W L=6000	1.000	1.063	1.087	1.337	2.785	1.000	1.076	1.106	1.411	3.148	1.000	1.090	1.125	1.484	3.505
L(C)=2.0W L=12000	1.000	1.061	1.084	1.327	2.729	1.000	1.074	1.102	1.398	3.081	1.000	1.087	1.131	1.469	3.427

I = 6.0, T(0) = 2.8

W(C)/W	W=80.00					W=100.00					T(1)=20.0 (OR ANY OTHER VALUE) W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	1.000	1.047	1.065	1.253	2.287	1.000	1.058	1.081	1.312	2.583	1.000	1.069	1.096	1.371	2.876
L(C)=0.5W L=6000	1.000	1.020	1.027	1.106	1.543	1.000	1.024	1.033	1.130	1.662	1.000	1.029	1.040	1.154	1.782
L(C)=0.5W L=12000	1.000	1.019	1.027	1.104	1.535	1.000	1.024	1.033	1.128	1.654	1.000	1.028	1.039	1.152	1.772
L(C)=1.0W L=1000	1.000	1.092	1.128	1.495	3.565	1.000	1.113	1.157	1.607	4.120	1.000	1.134	1.185	1.716	4.663
L(C)=1.0W L=6000	1.000	1.039	1.054	1.209	2.104	1.000	1.047	1.066	1.255	2.314	1.000	1.056	1.078	1.297	2.558
L(C)=1.0W L=12000	1.000	1.038	1.053	1.206	2.089	1.000	1.047	1.065	1.252	2.331	1.000	1.055	1.077	1.301	2.538
L(C)=1.5W L=1000	1.000	1.135	1.187	1.727	4.830	1.000	1.165	1.228	1.885	5.604	1.000	1.193	1.267	2.037	6.353
L(C)=1.5W L=6000	1.000	1.057	1.079	1.311	2.684	1.000	1.070	1.097	1.377	3.005	1.000	1.082	1.114	1.442	3.326
L(C)=1.5W L=12000	1.000	1.057	1.078	1.307	2.662	1.000	1.069	1.095	1.372	2.979	1.000	1.081	1.112	1.437	3.296
L(C)=2.0W L=1000	1.000	1.176	1.243	1.949	6.077	1.000	1.213	1.294	2.146	7.031	1.000	1.248	1.343	2.332	7.940
L(C)=2.0W L=6000	1.000	1.075	1.104	1.410	3.283	1.000	1.091	1.126	1.495	3.684	1.000	1.107	1.148	1.578	4.084
L(C)=2.0W L=12000	1.000	1.074	1.103	1.405	3.253	1.000	1.090	1.125	1.488	3.650	1.000	1.106	1.146	1.570	4.045

I = 6.0, T(0) = 1.4

W(C)/W	W=80.00					W=100.00					T(1)=20.0 (OR ANY OTHER VALUE) W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L=1000	1.000	1.051	1.071	1.277	2.479	1.000	1.063	1.087	1.337	2.772	1.000	1.074	1.102	1.397	3.068
L(C)=0.5W L=6000	1.000	1.028	1.039	1.154	1.836	1.000	1.034	1.048	1.186	1.988	1.000	1.040	1.056	1.218	2.145
L(C)=0.5W L=12000	1.000	1.028	1.039	1.154	1.835	1.000	1.034	1.048	1.185	1.986	1.000	1.040	1.056	1.217	2.149
L(C)=1.0W L=1000	1.000	1.100	1.139	1.547	4.118	1.000	1.121	1.168	1.658	4.633	1.000	1.142	1.196	1.768	5.155
L(C)=1.0W L=6000	1.000	1.056	1.077	1.307	2.815	1.000	1.067	1.093	1.366	3.076	1.000	1.078	1.108	1.425	3.352
L(C)=1.0W L=12000	1.000	1.056	1.077	1.307	2.819	1.000	1.067	1.093	1.365	3.072	1.000	1.078	1.108	1.428	3.348
L(C)=1.5W L=1000	1.000	1.146	1.203	1.809	5.931	1.000	1.176	1.243	1.962	6.571	1.000	1.204	1.283	2.112	7.239
L(C)=1.5W L=6000	1.000	1.082	1.114	1.458	3.983	1.000	1.098	1.136	1.541	4.273	1.000	1.114	1.158	1.624	4.619
L(C)=1.5W L=12000	1.000	1.082	1.114	1.458	3.977	1.000	1.098	1.136	1.540	4.267	1.000	1.114	1.157	1.623	4.622
L(C)=2.0W L=1000	1.000	1.190	1.264	2.062	7.934	1.000	1.226	1.314	2.249	8.575	1.000	1.261	1.361	2.429	9.895
L(C)=2.0W L=6000	1.000	1.108	1.143	1.609	5.379	1.000	1.127	1.177	1.711	5.590	1.000	1.147	1.204	1.812	5.942
L(C)=2.0W L=12000	1.000	1.107	1.189	1.608	5.369	1.000	1.127	1.176	1.704	5.582	1.000	1.167	1.203	1.811	5.933

Table XXIII — Values of (max delta T_c)/(max delta T_{c0})

I = 8.0   T(I)=20.0 (OR ANY OTHER VALUE)   T(0)=.2

W(C)/W	W=80.00					W=100.00					W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.046	1.064	1.206	2.258	1.000	1.057	1.079	1.306	2.550	1.000	1.068	1.094	1.364	2.840
L(C)=0.5W L= 6000	1.000	1.017	1.023	1.089	1.456	1.000	1.020	1.026	1.109	1.555	1.000	1.028	1.033	1.129	1.656
L(C)=0.5W L=12000	1.000	1.016	1.022	1.086	1.441	1.000	1.020	1.027	1.105	1.538	1.000	1.023	1.032	1.125	1.635
L(C)=1.0W L= 1000	1.000	1.091	1.125	1.406	3.502	1.000	1.111	1.154	1.597	4.052	1.000	1.132	1.182	1.705	4.591
L(C)=1.0W L= 6000	1.000	1.033	1.045	1.177	1.931	1.000	1.040	1.055	1.215	2.120	1.000	1.047	1.065	1.246	2.312
L(C)=1.0W L=12000	1.000	1.032	1.044	1.171	1.900	1.000	1.039	1.054	1.208	2.085	1.000	1.046	1.063	1.246	2.270
L(C)=1.5W L= 1000	1.000	1.133	1.188	1.718	4.729	1.000	1.162	1.224	1.871	5.501	1.000	1.191	1.264	2.022	6.248
L(C)=1.5W L= 6000	1.000	1.049	1.067	1.263	2.423	1.000	1.059	1.082	1.309	2.694	1.000	1.070	1.096	1.374	2.967
L(C)=1.5W L=12000	1.000	1.047	1.065	1.254	2.377	1.000	1.057	1.079	1.309	2.640	1.000	1.067	1.093	1.363	2.905
L(C)=2.0W L= 1000	1.000	1.173	1.239	1.932	5.931	1.000	1.210	1.290	2.128	6.891	1.000	1.245	1.339	2.315	7.805
L(C)=2.0W L= 6000	1.000	1.064	1.089	1.348	2.935	1.000	1.078	1.107	1.420	3.276	1.000	1.091	1.126	1.491	3.620
L(C)=2.0W L=12000	1.000	1.062	1.086	1.337	2.872	1.000	1.075	1.104	1.407	3.204	1.000	1.088	1.122	1.476	3.538

I = 8.0   T(I)=20.0 (OR ANY OTHER VALUE)   T(0)=2.8

W(C)/W	W=80.00					W=100.00					W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.066	1.081	1.257	2.326	1.000	1.059	1.081	1.315	2.617	1.000	1.070	1.097	1.374	2.908
L(C)=0.5W L= 6000	1.000	1.020	1.028	1.109	1.575	1.000	1.025	1.034	1.133	1.689	1.000	1.029	1.040	1.156	1.806
L(C)=0.5W L=12000	1.000	1.020	1.027	1.108	1.567	1.000	1.024	1.034	1.105	1.580	1.000	1.029	1.040	1.154	1.795
L(C)=1.0W L= 1000	1.000	1.093	1.129	1.505	3.691	1.000	1.114	1.159	1.635	4.231	1.000	1.155	1.186	1.723	4.765
L(C)=1.0W L= 6000	1.000	1.040	1.055	1.218	2.207	1.000	1.048	1.067	1.263	2.417	1.000	1.058	1.079	1.307	2.634
L(C)=1.0W L=12000	1.000	1.039	1.055	1.215	2.189	1.000	1.048	1.066	1.259	2.398	1.000	1.056	1.078	1.303	2.613
L(C)=1.5W L= 1000	1.000	1.137	1.190	1.744	5.092	1.000	1.166	1.230	1.899	5.833	1.000	1.199	1.265	2.045	6.559
L(C)=1.5W L= 6000	1.000	1.059	1.081	1.325	2.902	1.000	1.071	1.093	1.388	3.185	1.000	1.082	1.115	1.452	3.483
L(C)=1.5W L=12000	1.000	1.058	1.081	1.321	2.874	1.000	1.070	1.092	1.388	3.155	1.000	1.082	1.118	1.447	3.451
L(C)=2.0W L= 1000	1.000	1.178	1.247	1.973	6.521	1.000	1.215	1.297	2.166	7.411	1.000	1.250	1.345	2.350	8.276
L(C)=2.0W L= 6000	1.000	1.078	1.108	1.432	3.669	1.000	1.093	1.129	1.512	3.954	1.000	1.159	1.151	1.593	4.352
L(C)=2.0W L=12000	1.000	1.077	1.107	1.426	3.630	1.000	1.092	1.128	1.505	3.958	1.000	1.107	1.149	1.585	4.308

I = 8.0   T(I)=20.0 (OR ANY OTHER VALUE)   T(0)=1.4

W(C)/W	W=80.00					W=100.00					W=120.00				
	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25	1.00	0.80	0.75	0.50	0.25
L(C)=0.5W L= 1000	1.000	1.053	1.078	1.292	2.651	1.000	1.064	1.089	1.349	2.918	1.000	1.075	1.104	1.407	3.194
L(C)=0.5W L= 6000	1.000	1.030	1.042	1.167	1.984	1.000	1.036	1.050	1.195	2.101	1.000	1.042	1.058	1.226	2.261
L(C)=0.5W L=12000	1.000	1.030	1.042	1.167	1.982	1.000	1.036	1.049	1.195	2.098	1.000	1.041	1.057	1.225	2.238
L(C)=1.0W L= 1000	1.000	1.108	1.145	1.583	4.795	1.000	1.124	1.173	1.687	3.515	1.000	1.145	1.200	1.793	5.607
L(C)=1.0W L= 6000	1.000	1.060	1.083	1.339	3.443	1.000	1.070	1.097	1.390	3.509	1.000	1.081	1.112	1.446	3.708
L(C)=1.0W L=12000	1.000	1.060	1.083	1.338	3.436	1.000	1.070	1.097	1.389	3.503	1.000	1.081	1.112	1.445	3.703
L(C)=1.5W L= 1000	1.000	1.153	1.213	1.874	7.658	1.000	1.181	1.251	2.014	7.808	1.000	1.208	1.289	2.156	8.236
L(C)=1.5W L= 6000	1.000	1.089	1.123	1.515	5.805	1.000	1.102	1.163	1.584	5.381	1.000	1.117	1.163	1.660	5.454
L(C)=1.5W L=12000	1.000	1.088	1.123	1.515	5.792	1.000	1.102	1.162	1.583	5.371	1.000	1.117	1.163	1.658	5.446
L(C)=2.0W L= 1000	1.000	1.209	1.278	2.162	11.625	1.000	1.233	1.325	2.329	10.925	1.000	1.267	1.370	2.496	11.068
L(C)=2.0W L= 6000	1.000	1.116	1.163	1.699	10.239	1.000	1.134	1.186	1.777	7.935	1.000	1.152	1.211	1.867	7.551
L(C)=2.0W L=12000	1.000	1.116	1.162	1.697	10.214	1.000	1.134	1.186	1.776	7.920	1.000	1.152	1.211	1.865	7.538

Table XXIV — Values of (max ΔT_c)/(max ΔT_{c0}) for the special case of a small current in a long conductor

$t_0 = 1.4$ (1-oz Cu)

L_c	$W=6$					$W=8$					$W=10$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
$2W$	1.000	1.028	1.039	1.149	1.744	1.000	1.037	1.051	1.197	1.984	1.000	1.046	1.063	1.244	2.220
$4W$	1.000	1.054	1.075	1.290	2.452	1.000	1.071	1.099	1.381	2.904	1.000	1.088	1.121	1.468	3.341
$6W$	1.000	1.080	1.110	1.425	3.124	1.000	1.104	1.143	1.553	3.763	1.000	1.126	1.175	1.674	4.371
$8W$	1.000	1.104	1.143	1.553	3.763	1.000	1.134	1.185	1.713	4.566	1.000	1.162	1.224	1.863	5.317

$t_0 = 2.8$ (2-oz Cu)

L_c	$W=6$					$W=8$					$W=10$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
$2W$	1.000	1.020	1.028	1.106	1.530	1.000	1.026	1.036	1.141	1.703	1.000	1.033	1.045	1.175	1.873
$4W$	1.000	1.039	1.054	1.208	2.042	1.000	1.052	1.071	1.275	2.373	1.000	1.064	1.088	1.339	2.696
$6W$	1.000	1.058	1.080	1.307	2.535	1.000	1.075	1.104	1.402	3.011	1.000	1.093	1.128	1.494	3.471
$8W$	1.000	1.075	1.104	1.402	3.011	1.000	1.098	1.136	1.524	3.620	1.000	1.120	1.166	1.640	4.201

$t_0 = 4.2$ (3-oz Cu)

L_c	$W=6$					$W=8$					$W=10$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
$2W$	1.000	1.016	1.023	1.087	1.434	1.000	1.022	1.030	1.115	1.576	1.000	1.027	1.037	1.143	1.717
$4W$	1.000	1.032	1.044	1.171	1.856	1.000	1.042	1.059	1.226	2.131	1.000	1.053	1.073	1.280	2.400
$6W$	1.000	1.048	1.066	1.253	2.266	1.000	1.062	1.086	1.333	2.664	1.000	1.077	1.106	1.410	3.050
$8W$	1.000	1.062	1.086	1.333	2.664	1.000	1.082	1.113	1.435	3.176	1.000	1.100	1.138	1.534	3.669

Table XXV — Values of $(\text{max } \Delta T_c)/(\text{max } \Delta T_{c0})$ for the special case of small current in a long conductor

$t_0 = 1.4$ (1-oz Cu)

L_c	$W = 20$					$W = 25$					$W = 30$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
W	1.000	1.026	1.036	1.141	1.703	1.000	1.033	1.045	1.175	1.873	1.000	1.039	1.054	1.208	2.042
$2W$	1.000	1.052	1.071	1.275	2.373	1.000	1.064	1.088	1.339	2.696	1.000	1.075	1.104	1.402	3.011
$3W$	1.000	1.075	1.104	1.402	3.011	1.000	1.093	1.128	1.494	3.471	1.000	1.109	1.151	1.583	3.914
$4W$	1.000	1.098	1.136	1.524	3.620	1.000	1.120	1.166	1.640	4.200	1.000	1.141	1.195	1.751	4.753

$t_0 = 2.8$ (2-oz Cu)

L_c	$W = 20$					$W = 25$					$W = 30$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
W	1.000	1.019	1.026	1.100	1.501	1.000	1.023	1.032	1.125	1.623	1.000	1.028	1.039	1.149	1.744
$2W$	1.000	1.037	1.051	1.197	1.984	1.000	1.046	1.063	1.244	2.220	1.000	1.054	1.075	1.290	2.452
$3W$	1.000	1.054	1.075	1.290	2.452	1.000	1.067	1.093	1.359	2.792	1.000	1.080	1.110	1.425	3.124
$4W$	1.000	1.071	1.099	1.381	2.904	1.000	1.088	1.121	1.468	3.341	1.000	1.104	1.143	1.553	3.763

$t_0 = 4.2$ (3-oz Cu)

L_c	$W = 20$					$W = 25$					$W = 30$				
	$W_c/W=1$	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25	1	0.8	0.75	0.50	0.25
W	1.000	1.015	1.021	1.082	1.410	1.000	1.019	1.027	1.102	1.511	1.000	1.023	1.032	1.122	1.611
$2W$	1.000	1.030	1.042	1.162	1.809	1.000	1.038	1.052	1.201	2.004	1.000	1.045	1.062	1.239	2.196
$3W$	1.000	1.045	1.062	1.239	2.196	1.000	1.056	1.077	1.296	2.480	1.000	1.066	1.091	1.352	2.758
$4W$	1.000	1.059	1.082	1.315	2.574	1.000	1.073	1.101	1.388	2.941	1.000	1.086	1.119	1.460	3.297

Table XXVI — Values of $(\max \Delta T_c)/(\max \Delta T_{c0})$ for the special case of small current in a long conductor

$t_0 = 1.4$ (1-oz Cu)

L_c	$W_c/W = 1$	W = 80 0.8	0.75	0.50	0.25	1	W = 100 0.8	0.75	0.50	0.25	1	W = 120 0.8	0.75	0.50	0.25
$W/2$	1.000	1.026	1.036	1.141	1.703	1.000	1.033	1.045	1.175	1.873	1.000	1.039	1.054	1.209	2.042
W	1.000	1.052	1.071	1.275	2.373	1.000	1.064	1.088	1.339	2.696	1.000	1.075	1.104	1.402	3.011
$3W/2$	1.000	1.075	1.104	1.402	3.011	1.000	1.093	1.128	1.494	3.471	1.000	1.109	1.151	1.583	3.914
$2W$	1.000	1.098	1.136	1.524	3.620	1.000	1.120	1.166	1.640	4.200	1.000	1.141	1.195	1.751	4.753

$t_0 = 2.8$ (2-oz Cu)

L_c	$W_c/W = 1$	W = 80 0.8	0.75	0.50	0.25	1	W = 100 0.8	0.75	0.50	0.25	1	W = 120 0.8	0.75	0.50	0.25
$W/2$	1.000	1.019	1.026	1.100	1.501	1.000	1.023	1.032	1.125	1.623	1.000	1.028	1.039	1.149	1.744
W	1.000	1.037	1.051	1.197	1.984	1.000	1.046	1.063	1.244	2.220	1.000	1.054	1.075	1.290	2.452
$3W/2$	1.000	1.054	1.075	1.290	2.452	1.000	1.067	1.093	1.359	2.792	1.000	1.080	1.110	1.425	3.124
$2W$	1.000	1.071	1.099	1.381	2.904	1.000	1.088	1.121	1.468	3.341	1.000	1.104	1.143	1.553	3.763

$t_0 = 4.2$ (3-oz Cu)

L_c	$W_c/W = 1$	W = 80 0.8	0.75	0.50	0.25	1	W = 100 0.8	0.75	0.50	0.25	1	W = 120 0.8	0.75	0.50	0.25
$W/2$	1.000	1.015	1.021	1.082	1.410	1.000	1.019	1.027	1.102	1.511	1.000	1.023	1.032	1.122	1.611
W	1.000	1.030	1.042	1.162	1.809	1.000	1.038	1.052	1.201	2.004	1.000	1.045	1.062	1.239	2.196
$3W/2$	1.000	1.045	1.062	1.239	2.196	1.000	1.056	1.077	1.296	2.480	1.000	1.066	1.091	1.352	2.758
$2W$	1.000	1.059	1.082	1.315	2.574	1.000	1.073	1.101	1.388	2.941	1.000	1.086	1.119	1.460	3.297

Comments on the Conservative Nature of the Results

D. E. McCumber has suggested[5] that the boundary conditions appropriate to eq. (1) at the step discontinuity in conductor width are:

(*i*) $\Delta T(x)$ be continuous.

(*ii*) $[d\Delta T(x)/dx]$ be discontinuous such that $W(x)[d\Delta T(x)/dx]$ be continuous.

These boundary conditions derive from the one-dimensional heat continuity equation:

$$kt_0 \frac{d}{dx}\left(W(x)\frac{d\Delta T(x)}{dx}\right)$$
$$- 2HW(x)\Delta T(x) + I^2 R'[1 + \alpha_1 \Delta T(x)] = 0. \quad (24)$$

Equation (24) is identical to eq. (1) in the regions away from the discontinuity. McCumber's boundary conditions conserve integrated heat flux but neglect fringing in the transition region. These lead to a solution

$$\Delta T_c(x) = \frac{\gamma_1^2}{\beta_1^2}$$
$$- \frac{\{(\gamma^2/\beta^2)\,\text{sech}\,[(\beta/2)(L - L_c)] + [(\gamma_1^2/\beta_1^2) - (\gamma^2/\beta^2)]\}\cosh\beta_1 x}{(W_c/W)(\beta_1/\beta)\sinh(\beta_1 L_c/2)\tanh\,[(\beta/2)(L - L_c)] + \cosh(\beta_1 L_c/2)},$$
$$(25)$$

which is identical to eq. (2) except for the factor W_c/W in the first term of the denominator.

McCumber has shown by a full two-dimensional analysis of a simplified system similar to that considered here that eq. (25) is more accurate than eq. (2) but tends slightly to underestimate the temperature rise $\Delta T_c(x)$, whereas eq. (2) is conservative and always overestimates $\Delta T_c(x)$. As the results reported in this paper show, even these conservative estimates of $\Delta T_c(x)$ indicate substantial thermal latitude for nicks or constrictions in printed wiring circuits.

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