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Integrated Circuit Process and Design Rule Evaluation Techniques*

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Abstract—A technique is described for determining the applicability of a particular process for the fabrication of large-scale integrated (LSI) circuits. Test arrays were developed to isolate various critical processing steps in a fabrication sequence and a statistical evaluation of these steps was carried out that related yield or success in achieving a desired result to the number of times the results were attempted. It was found that, in general, yield is a sensitive function of physical dimensions as is the packing density of a particular array. It is, therefore, possible to generate an optimum set of physical dimensions or design rules that maximize the expected number of working circuits on a wafer.

1. Introduction

At present, large-scale integration (LSI) means the fabrication of semiconductor arrays containing several thousand devices in an area less than a quarter of an inch on a side, with yield values in excess of 2%. These three factors, density, size, and yield, are, of course, all interrelated and depend, in turn, on two interdependent areas, process technology and physical dimensions (or design rules). It should be pointed out that this is not the case in small- or medium-scale integration, where the degree of complexity is low and, hence, the yield is high and relatively independent of physical dimensions.

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This study was concerned with large-scale integration, and, therefore, it was necessary to consider the impact of both the process technology and the physical dimensions on packing density, chip size, and array yield. This, in turn, required an in-depth study of the particular process of interest, the silicon-gate deep-depletion CMOS/SOS process, to determine which steps or sequence of steps should be analyzed. It was also necessary to develop techniques for determining the interrelationships of various process sequences as well as the dimensional dependence of these sequences.

Once the process analysis was complete, the necessary test structures were designed and masks were generated. Three test structures were produced: the process analysis structure (PAS), the spacing array (SPAR), and the contact array (CAR). In addition, various processing sequences were developed to analyze the particular steps and sequence of steps of interest.

The test structures and procedures were then used to initiate a comprehensive program of process analysis and the design-rule–process interaction. Yield data were generated for various critical process steps as well as the yield variation of the process step with physical dimensions. From these yield data it was possible to generate a set of curves relating the physical dimensions associated with a particular process sequence to the expected number of working LSI arrays producible from these dimensions. In general the curves showed a peak value associated with a particular dimension indicating an "optimum" value. It was possible, therefore, to generate an optimum set of LSI design rules.

It was demonstrated that the various test structures were useful in evaluating new process techniques as well as new processing equipment, and yield data were generated comparing the old with the new. Also included in this paper is an analysis of various yield models being studied in the literature of their applicability to the data generated in this study.

2. Process Analysis and Evaluation Structures

Random defects can be generated by any of the various process steps used in the fabrication of integrated circuits. There are, however, certain specific steps of a critical nature that are used repeatedly and can be grouped together. These are:

(1) Thin-film deposition or growth:
- Semiconductor layers
- Dielectric layers
- Metal layers

(2) Photoresist techniques

(3) Etching techniques
(4) Doping techniques

Nearly all integrated-circuit process technologies contain these categories. Different specific approaches, however, are used by different companies in each of these categories. Etching, for instance, may be the result of a wet-chemical technique in one company, while another may use a gaseous plasma approach. Ion implantation may be used as the doping source for some, while others use high-temperature gaseous sources. The number of different photoresist techniques is endless. The need to examine these steps to determine the degree to which they have been successfully accomplished is extremely important and returns one to the problem at hand.

In general, a process sequence involves depositing, growing or doping a thin film, defining the film, and etching it. These three sequential steps comprise one block which can be interrogated for defects, and, if the number is found to be high, the film can be stripped and the steps repeated. Analyzing the CMOS/SOS silicon-gate process, one finds that the first sequence of steps is the deposition and patterning of the thin silicon film. The process analysis structures must, therefore, be able to check for

(1) silicon island discontinuities
(2) silicon island to silicon island short-circuits.

The next step is the oxidation of the islands followed by the deposition of the polycrystalline silicon film. The polysilicon layer is then patterned, and, hence, the test structure must examine for

(3) polycrystalline silicon discontinuities,
(4) polycrystalline-silicon island short-circuits,
(5) polysilicon to polysilicon short-circuits.

A layer of silicon dioxide is deposited, and contact holes are etched in the layer to permit the metal interconnect pattern to make electrical contact to the silicon islands and polysilicon gates. A test must be performed, therefore, to describe

(6) contact hole open-circuits.

The last layer deposited and defined is the metal interconnect pattern. The process analysis structure must, therefore, examine for

(7) metal discontinuities,
(8) metal-to-island short-circuits,
(9) metal-to-polysilicon short-circuits,
(10) metal-to-metal short-circuits.

All of these data *must* be compiled on a statistical basis so that, for instance, the "probability" of opening a certain number of contacts can be ascertained. The test structures used to analyze these problem areas

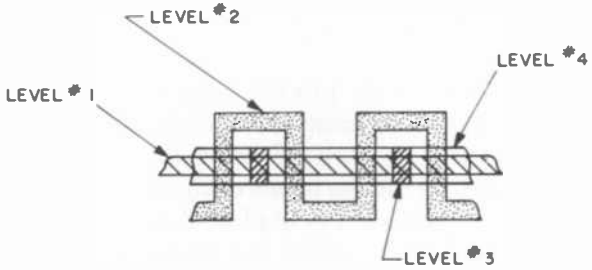

Fig. 1—PAS test cell

as well as to determine their dependence on physical dimensions will now be described.

2.1 Process Analysis Structure (PAS)

The PAS test cell is Shown in Fig. 1. Listed in Table 1 are the corresponding dimensions for each level. A photomicrograph of a typically processed PAS is shown in Fig. 2. The basic concept inherent in this test structure is that the number of effective defects that are generated by a particular process step and are detrimental to the definition of a particular physical dimension can be determined by "sequentially" interrogating the defined pattern. For this reason the array was laid out so that an increasing number of cells could be analyzed and a pass or fail condition determined as a function of the number of cells. The number of cells accessible for analysis and brought out to external pads were 200, 400, 600, 1200, 2400, 4800, and 7200. The total array, therefore, contained 14,400 cells. The array dimensions are 170 × 200 mils permitting approximately 100 test chips to be fabricated on a two inch wafer. A three-inch wafer contains about 150 arrays.

The levels listed in Table 1 can be used individually or in various combinations to determine the continuity of different types of conduc-

Table 1—PAS Test Cell Dimensions

Level No.	Length (mils)	Width (mils)
1	200, 400, 600, 1200, 2400, 4800, 7200	0.2
2	400, 800, 1200, 2400, 4800, 9600, 14400	0.2
3	0.4	0.2
4A	200, 400, 600, 1200, 2400, 4800, 7200	0.4
4B	200, 400, 600, 1200, 2400, 4800, 7200	0.3
4C	200, 400, 600, 1200, 2400, 4800, 7200	0.25
4D	200, 400, 600, 1200, 2400, 4800, 7200	0.20
4E	200, 400, 600, 1200, 2400, 4800, 7200	0.15
4F	200, 400, 600, 1200, 2400, 4800, 7200	0.10

tors on the interaction of one layer with another. Applications of this array will be discussed later.

2.2 Spacing Array (SPAR)

This array is concerned with the ability of a given process sequence to define conducting lines spaced a given distance apart. The SPAR cell is shown in Fig. 3 where it is seen that two masks levels can be used. The first level is used to define steps, if desired, over which the conducting lines are defined (level 2). The dimensions are given in Table 2.

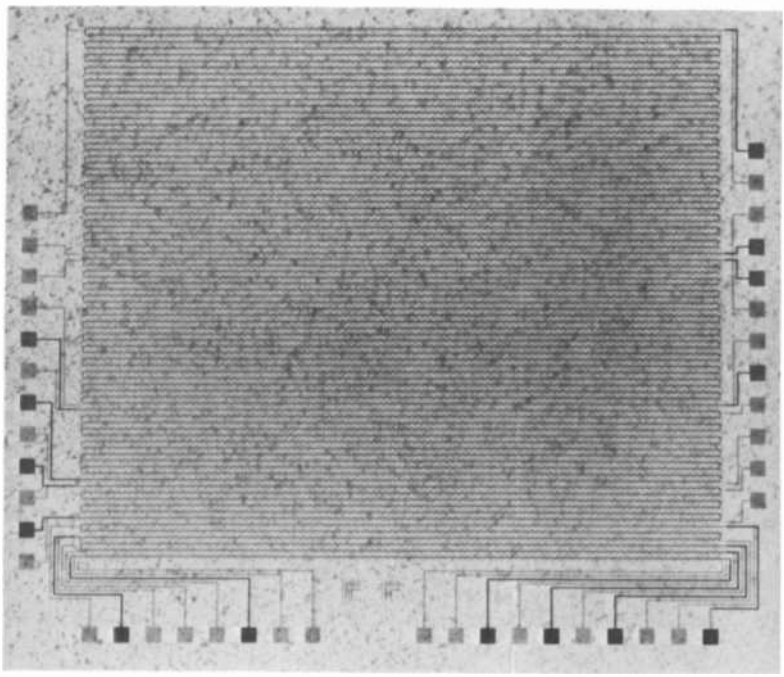

Fig. 2—Photomicrograph of typical process analysis structure (PAS).

The width of the conducting lines was made greater than 0.7 mil in order to minimize the probability of discontinuities. A photomicrograph of level 2 is shown in Fig. 4. The SPAR array contains two crossovers per mil and, hence, the continuity of conducting lines crossing over from 400 to 38400 crossovers can be determined. Since the overall array size is 200 × 200 mils, about 75 chips can be fabricated on a two-inch wafer, and about 125 chips on a three-inch substrate.

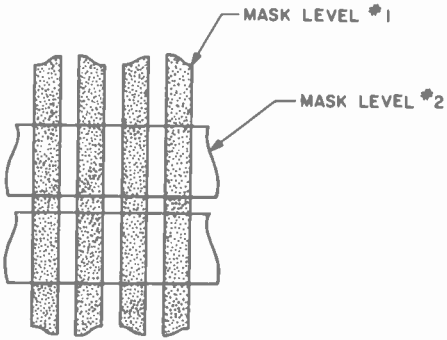

Fig. 3—Line-to-line spacing array (SPAR)

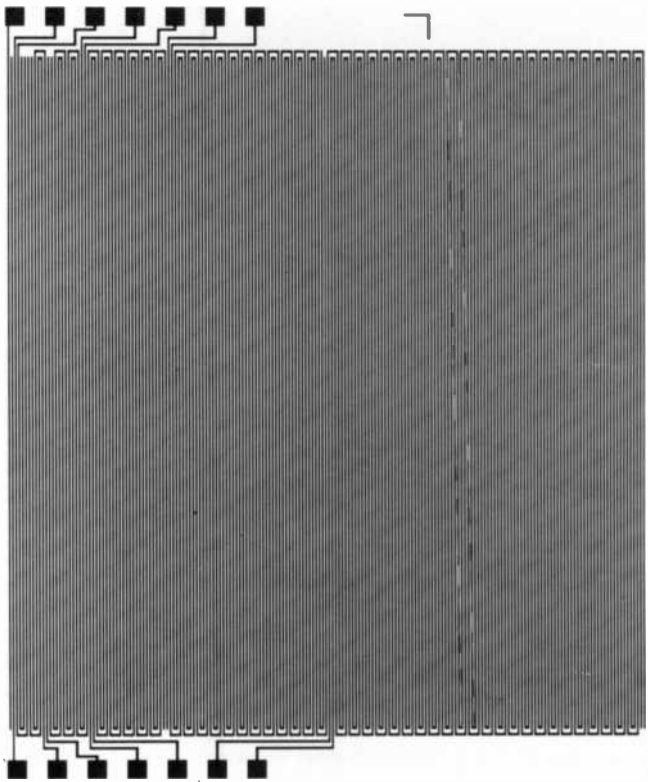

Fig. 4—Photomicrograph of SPAR level

Table 2—SPAR Dimensions

Level No.	Width (mils)	Length (mils)	Separation (mils)
1	0.3	— — — — — — —	0.20
2A	0.7	200, 400, 600, 1200, 2400, 4800, 9600	0.30
2B	0.75	200, 400, 600, 1200, 2400, 4800, 9600	0.25
2C	0.80	200, 400, 600, 1200, 2400, 4800, 9600	0.20
2D	0.85	200, 400, 600, 1200, 2400, 4800, 9600	0.15
2E	0.90	200, 400, 600, 1200, 2400, 4800, 9600	0.10

2.3 Contact Array (CAR)

This mask set contains an array of SOS islands upon which contacts may be defined. The islands are then interconnected with metal, and the continuity of each contact string is interrogated. A cell of the CAR is shown in Fig. 5. The function and dimensions of each level are given in Table 3.

Level 2 can be used to define a material that allows control of the spacing between the contact mask and the photoresist to be patterned. The numbers of contacts that can be independently analyzed and that are connected together to form a single string are listed below.

String No.	1	2	3	4	5	6	7	8
No. of Contacts	200	400	600	1200	2400	4800	9600	19,200

A photomicrograph of the metal pattern is shown in Fig. 6. The chip size is 200 × 200 mils, and the number of arrays that can be fabricated on two-inch and three-inch wafers is about 75 and 125 chips, respectively.

Table 3—CAR Level Functions and Dimensions

Level No.	Function	Dimensions (mils)
1	Islands	0.6 × 1.4
2	Polysilicon	0.2 × 1.0
3A	Contacts	0.3 × 0.4
3B	Contacts	0.3 × 0.3
3C	Contacts	0.25 × 0.25
3D	Contacts	0.20 × 0.40
3E	Contacts	0.20 × 0.30
3F	Contacts	0.20 × 0.25
3G	Contacts	0.20 × 0.20
3H	Contacts	0.20 × 0.15
3I	Contacts	0.20 × 0.10
4	Metal	0.7 × 1.4

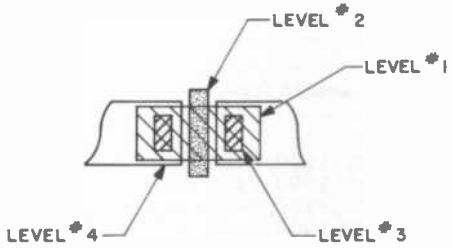

Fig. 5—Contact array (CAR)

These three test structures can be used in a wide variety of applications in the areas of process analysis, integrity, and control as they relate to physical characteristics. They are obviously not intended to permit an in-depth analysis of transistor characteristics, but, as will be described in later sections, some interesting device-related electrical parameters can be obtained as they relate to physical dimensions and yield statistics.

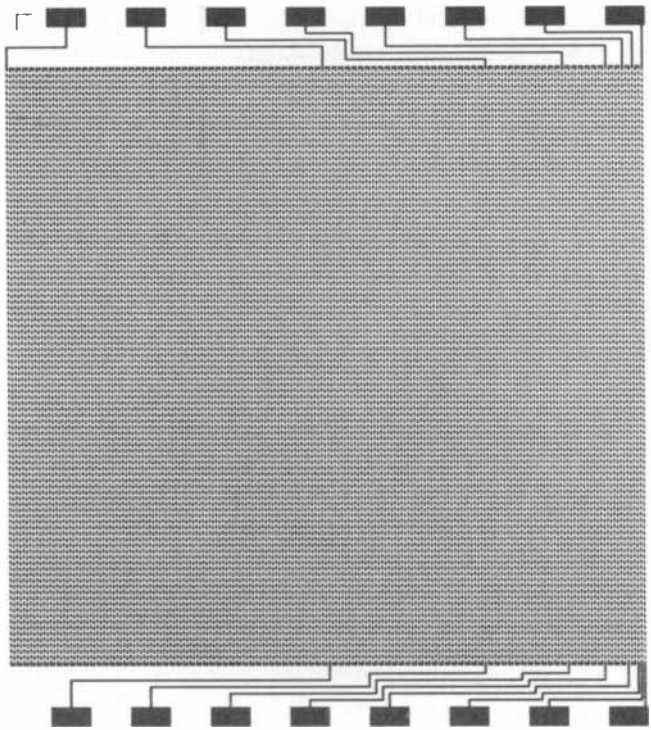

Fig. 6—Photomicrograph of CAR metal pattern

3. CMOS/SOS Process Characterization

The silicon-gate deep-depletion CMOS/SOS process has been described in the literature[1] and is shown diagramatically in Fig. 7. This process will now be discussed in detail to ascertain the process/dimension interaction as expressed in terms of yield curves, the object being to demonstrate the applicability of the various test arrays for process analysis and characterization.

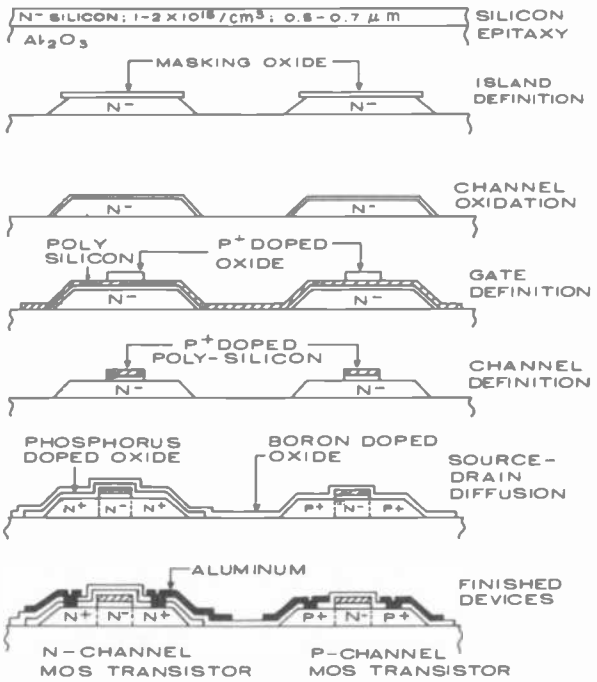

Fig. 7—Silicon-gate deep-depletion CMOS/SOS process

3.1 Epitaxial Silicon Integrity

Various questions have been raised concerning the physical integrity of SOS films as well as the processing techniques that have been used to define them. Patterns were defined, therefore, using both the PAS and the SPAR masks to determine the yield associated with defining various lengths, widths, and spacings in single-crystal silicon films on sapphire. The fabrication steps are listed below.

(1) Deposition of 0.6-μm silicon films on $(1\bar{1}02)$ sapphire[2]

(2) Thermal oxidation (900°C, HCl steam, 10 minutes)
(3) Photoresist (Waycoat 43 or GAF)
(4) Oxide etch (buffered HF)
(5) Silicon etch (KOH-n-propanol-H_2O)[3]
(6) Strip masking oxide (HF)
(7) Dope silicon pattern with boron ($1 \times 10^{20}/cm^3$)
(8) Electrically test

Various process techniques can be used to define the initial silicon pattern; our choice was a short thermal oxidation followed by the application of a positive resist (GAF). A 30-second etch in buffered HF which minimized undercutting defined the oxide pattern, and the silicon was patterned in an anistropic KOH solution.[3]

Mask levels 4B through 4F of the PAS were used to determine the integrity of epitaxial silicon lines while levels 2A through 2E of the SPAR permitted the evaluation of epi-to-epi spacings. The results are shown in Fig. 8. The numbers in parentheses are the nominal mask dimensions, while the other number is the dimension actually printed in the silicon. It is interesting to note that

(1) Even the loosest dimensions (i.e., 0.3-mil width and 0.3-mil spacing) do not result in a length-independent yield value out to 12 inches ($Y > 0.9$).
(2) The yield values for the dimensions studied were relatively tightly clustered (i.e., slight variations with width).

It will be shown later that this situation is not always the case. It was initially thought that mask defects were the cause for yield reduction with narrower dimensions. Later results with aluminum metallization, however, show that this was not so. The results, therefore, appear to indicate that (1) the silicon films contain defects that are rather large in size and (2) the density of smaller defects does not appear to increase rapidly as the size of the defect (or dimension) is reduced.

3.2 Polycrystalline Silicon Technology

After the epitaxial silicon has been defined, the channel oxide is grown, polycrystalline silicon is deposited, and defined. Before examining the interaction of the polycrystalline silicon with the epitaxial silicon, the integrity of the polysilicon was examined without the presence of the epi-layer. The process sequence was:

(1) Chemically vapor deposited silicon from SiH_4 in H_2 at 700°C (5000 Å).
(2) Deposition of boron-doped SiO_2 (1000 Å)
(3) Deposition of undoped SiO_2 (1000 Å)
(4) Photoresist (Waycoat)

(5) Etch oxides (buffered HF)
(6) Diffusion (1050°C, 15 minutes, He)
(7) Strip glass (buffered HF)
(8) Etch polysilicon (KOH-n-propanol-H_2O)
(9) Test wafers

This is a P+ polysilicon process incorporating P+ doped SiO_2 as the diffusion source. The disadvantage of this process is that the pattern

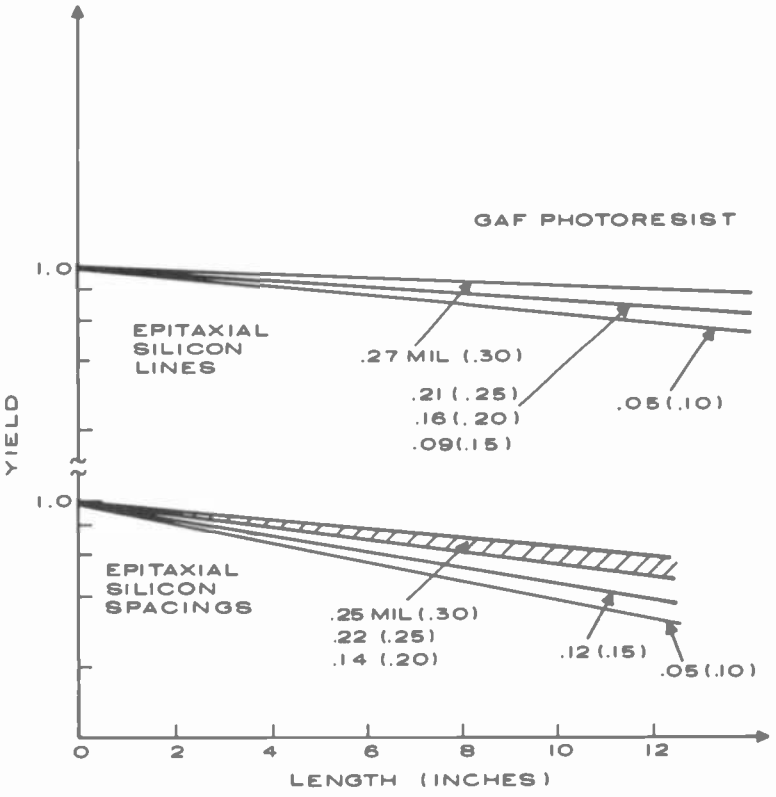

Fig. 8—Yield as a function of length, epi-silicon

must be defined in the two SiO_2 layers before being transferred to the polycrystalline silicon. The advantage is that the P+ doped silicon is unetchable in KOH, and, hence, the etching process is a self-limiting one. Again, as with the epi-silicon layer, the PAS and SPAR masks were used to define various lengths, widths, and spacings. The integrity of the

various polycrystalline silicon patterns is shown in Fig. 9. In general, the results show that:

(1) Large area defects do not appear to be present.
(2) A substantial increase in defect density with decreasing defect size (or physical dimension).
(3) Process techniques for defining fine-line geometries produce a lower yield on polycrystalline silicon then on epitaxial silicon.

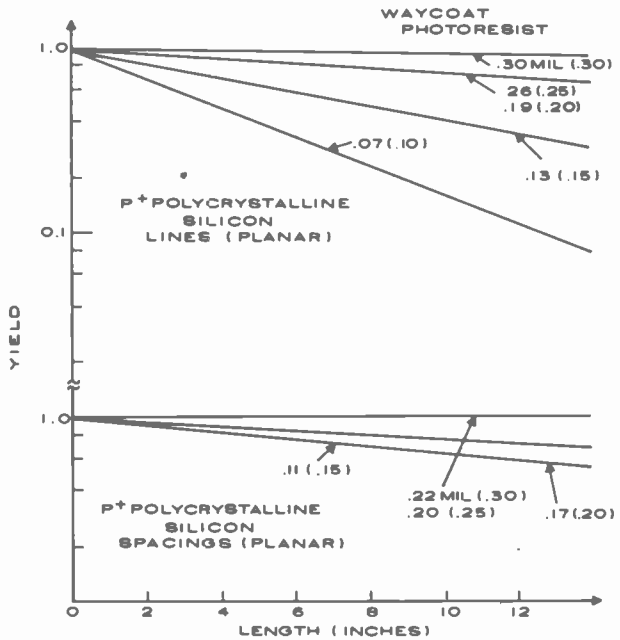

Fig. 9—Yield as a function of length, polycrystalline silicon

As is evident in Fig. 9 the defects are line-width limiting rather than spacing limiting. In addition, the relatively wide lines and spacing show little yield dependence on length over the region investigated. The present design rules limit the polysilicon width and spacing to 0.2 mil which, as shown in Fig. 9, are high yield dimensions.

3.3 Epitaxial Silicon–Polycrystalline Silicon Interaction

The integrity of polycrystalline silicon lines defined over epitaxial steps is, of course, the most important practical consideration and several of these investigations remain to be carried out. Using the PAS, however,

tests have been carried out where mask level 1 was used to define single-crystal islands using the process defined in 3.1. After the integrity of these patterns was determined, the islands were oxidized (900°C, HCl steam, 45 minutes) and the polysilicon process was applied using mask level 2. It was possible, therefore, to determine the integrity of 0.2-mil polycrystalline silicon lines as a function of length. These data are given in Fig. 10. Comparing Fig. 10 with Fig. 9 shows that for 0.2-mil polysilicon lines, there is no measurable yield reduction due to the nonplanarity of the polysilicon layer. It is felt, however, that this will not be the case for narrower widths.

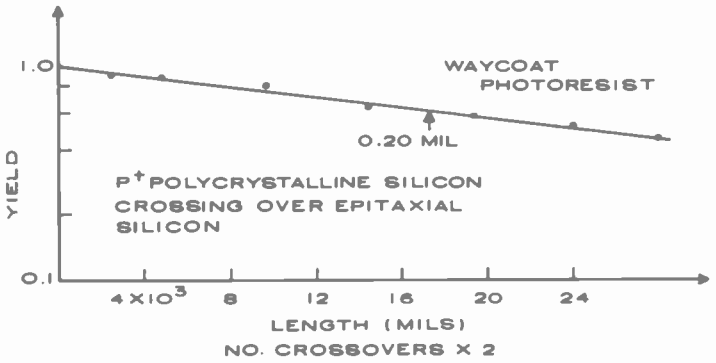

Fig. 10—Yield as a function of length, polycrystalline silicon crossing over epi silicon

Once the integrity of the epitaxial and polycrystalline silicon lines had been ascertained, it was possible to examine the integrity of the channel oxide. Since the epitaxial layer was doped prior to oxidation, it was possible to test for polysilicon-to-island short circuits both before and after the self-align etch of the channel oxide that removes it from the sources and drains of the devices. It has been found that the integrity of the channel oxide, as determined by the number of short circuits present between the epitaxial silicon island and the P+ doped polysilicon gate, is extremely variable. This is shown in Fig. 11. It has been shown previously[4] that the dielectric strength of the channel oxide on the edge of a silicon island is poor but can be improved in any of several ways. In Fig. 11, case 1 is a standard channel oxide grown in HCl steam at 900°C for 45 minutes. Case 2 was oxidized in the same manner followed by the deposition of 500 Å of SiO_2. The resulting dielectric strength increased substantially and, as shown in Fig. 11, the yield was also substantially improved. Other techniques such as depositing Si_3N_4 in place of the SiO_2 or replacing the deposited SiO_2 with oxidized polycrystalline silicon have shown similar results.

It is clear, therefore, that both the dielectric strength of SOS/MOS devices and the yield associated with LSI arrays can be substantially improved by the proper process modification. In addition to the edge-related yield-reducing mechanism, there are other problem area associated with the self-align etch of the channel oxide. The yield, therefore, can be further increased if the channel oxide is not removed. Case 3 demonstrates the improved integrity of the channel oxide that has not been removed from the source-drain areas. To fabricate devices by this technique, it is necessary to incorporate ion-implantation to achieve

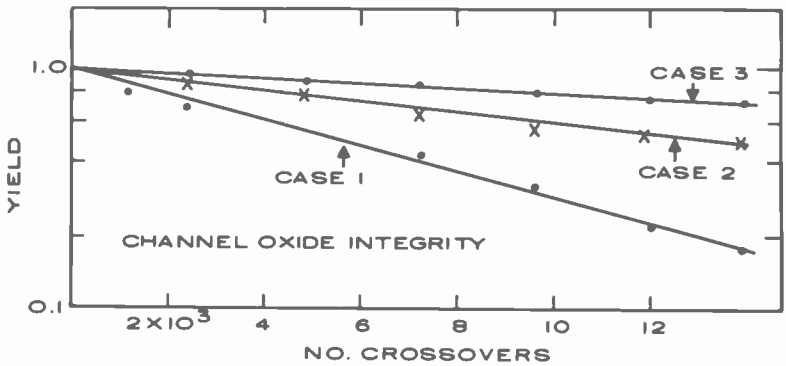

Fig. 11—Channel oxide integrity; yield as a function of the number of crossovers

source-drain doping. It should be noted that the channel-oxide integrity varies widely from run to run, and hence the data presented here indicate typical results. Further study in this area is needed to achieve consistently high oxide integrity.

3.4 Contact Integrity

Several runs have been completed using the CAR masks. Attempts were made to print and etch levels 3C, 3F, 3G, 3H, and 3I (see Table 3) on thermally oxidized silicon islands as well as on islands covered by deposited oxides. A negative photoresist (Waycoat 43) was used for pattern definition, and, in general, it was found that the printed contact opening had each dimension reduced by approximately 0.05 mil when compared with the mask dimension. Using the usual control techniques, the pattern, as defined in the photoresist, could be replicated in the oxide to a high degree of precision. Some typical results are shown in Fig. 12. It is seen that there appears to be a rapid reduction in yield for contact openings less than 0.16 × 0.16 mil.

3.5 Interconnect Metal Integrity

As described in Sec. 2 several aspects of the metallization step must be analyzed. We will discuss first metal discontinuities, then metal-to-metal short circuits, and, last, metal crossover short circuits.

Concerning metal continuity, 1.4 μm of aluminum was evaporated, in an ion-pumped evaporation with a Sloan planetary system and electron-beam source, onto various surfaces. Both Shipley 1350 and Waycoat 43 photoresists were used in conjunction with PAS mask levels 4A through 4F (see Table 1) to define various metal widths and lengths. The pattern was transferred to the aluminum using the standard, commer-

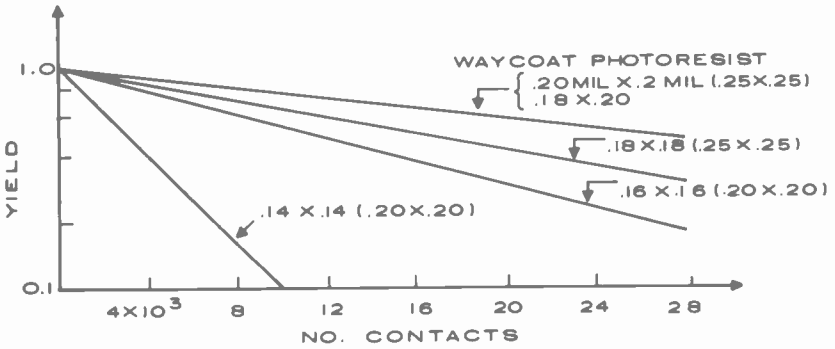

Fig. 12—Contact integrity; yield as a function of the number of contacts

cially available aluminum etch. The types of surfaces considered were:

- planar (bare sapphire)
- epitaxial silicon steps (0.6 μm)
- polycrystalline silicon steps (0.5 μm)
- multiple doped oxide steps (0.72 μm)

Mask level 2 was used to define the initial step pattern in the various materials. Typical results for Waycoat 43 photoresist are shown in Fig. 13. As expected the best results were obtained from the planar surface. This was the only surface that had continuous lines (although low yield ones) in the 2-μm width range. Results obtained on surfaces containing epi-silicon steps or polysilicon steps were approximately the same.

The lowest continuity yields were measured for the case where steps were etched in multiple-doped deposited oxides. These steps were fabricated by first depositing 800 Å of N+ doped oxide ($\approx 10^{20}/cm^3$) followed by 800 Å of undoped oxide. Next, 800 Å of P+ doped oxide ($\approx 10^{20}/cm^3$) were deposited followed by 4000 Å of undoped oxide. These layers were

then densified at 1050°C in He for 15 minutes. As shown in Fig. 7, this closely duplicates the source-drain doping schedule. Defining mask level 2 of the PAS, therefore, is analogous to opening contacts through these oxide layers. The continuity of metal lines which run over these doped oxide steps is a measure of the integrity of a metal line that must make contact to silicon through an opening that is "wider" than the metal line. In various SOS/LSI arrays, metal lines make contact with several silicon islands through contact openings that may be wider than the width of the metal, and, hence, its integrity must be quantitively determined. It should be noted that this measurement is different from that made using the CAR. The contact array (CAR) interrogates the contact opening only; the metal interconnect is extremely wide (0.7 mil) and covers the contact

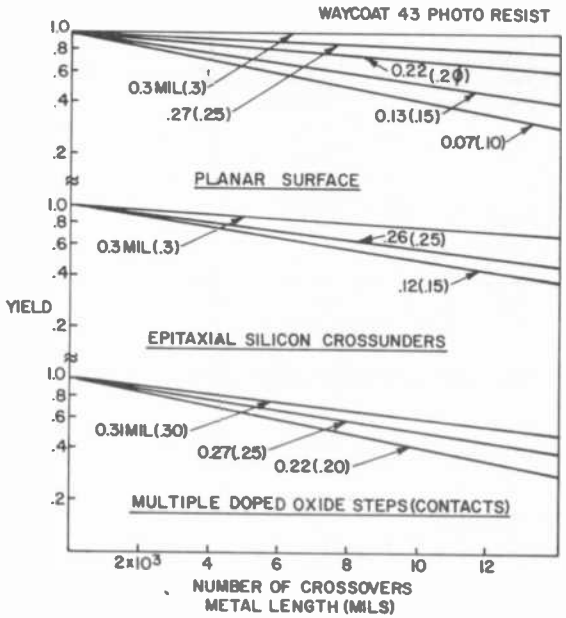

Fig. 13—Interconnect metal integrity using CAR; yield as a function of the number of crossovers

opening on all four sides; hence, the probability of metal continuity into the opening is essentially unity. In review, best results were obtained on planar surfaces, with epi and poly steps causing measurable yield reductions, and multiple, doped, deposited oxides producing the worst yield figures.

To test metal-to-metal short circuits, aluminum patterns were defined using the SPAR masks, and, again, data were generated with and without steps. The results are shown in Fig. 14. As in the case for metal widths,

best results (i.e., highest yields) were obtained on planar surfaces. It is interesting to note that even on a planar surface it was not possible to etch a spacing of 0.10 mil, even though the photoresist definition looked extremely good. This is consistent with the general conclusion that pattern definition in aluminum produces substantially lower yield values for width and spacing than pattern definition in polycrystalline silicon which, in turn, produces lower yield values than pattern definition in single-crystal silicon.

Similar data were generated using Shipley 1350J photoresist and it was found that, for our photoresist procedure, substantial undercutting of the resist occurred during etching, producing at least a 0.1-mil re-

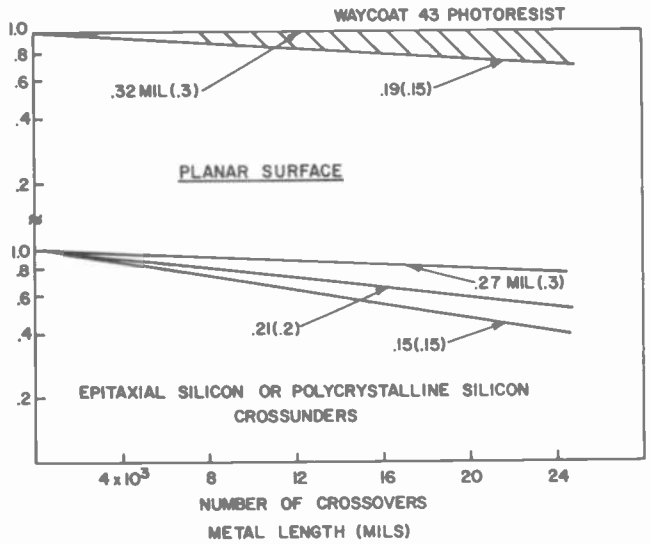

Fig. 14—Interconnect metal integrity using SPAR; yield as a function of the number of crossovers

duction in metal widths, i.e., an increase in metal-to-metal spacings. Figure 15 shows typical results using Shipley. It is interesting to note, however, that for a given printed metal width, the yield values were higher for Shipley (positive) than Waycoat (negative). The use of Shipley for fine line geometries, however, is questionable because of the severe undercutting that results.

The final area of interest is in the integrity of the field oxide that separates the metal conductors from polycrystalline or epitaxial silicon crossunders. This field oxide is again the multiple doped oxide previously described in detail. Mask level 2 of the PAS was used to define the

crossunders followed by the deposition of the doped oxides. Mask level 4B delineated the metal lines, and measurements were performed to determine the number of metal-to-crossunder short circuits. The yields in general were in the 90% vicinity.

Worst-case results were obtained using mask level 1 to define single-crystal silicon lines. These were then oxidized and doped following the procedure in Sec. 3.1; polycrystalline silicon was then deposited and defined using mask 2 and the procedure outlined in Sec. 3.2; the field oxide was deposited; and the metal pattern was defined using mask level

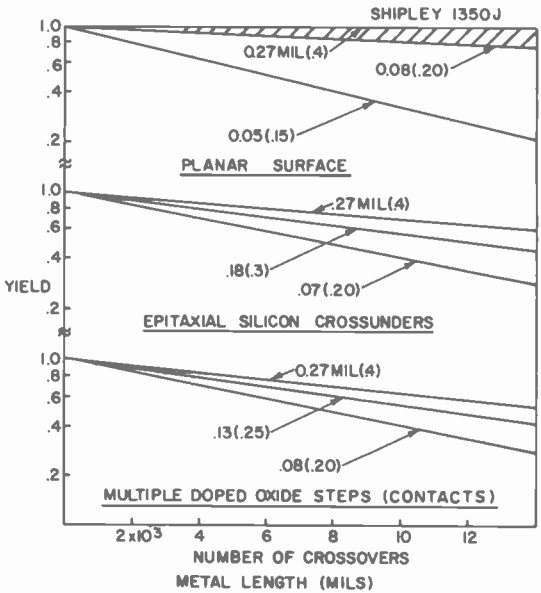

Fig. 15—Interconnect metal integrity using SPAR; yield as a function of the number of crossovers (Shipley 1350J photoresist).

4B. The number of short-circuits between the various sublayers was determined and the results are shown in Fig. 16. This is analogous to running metal conductors over the gates of SOS/MOS transistors. It is seen from Fig. 16, however, that the integrity of the field oxide, even under these conditions is extremely good and does not represent a substantial yield-limiting factor.

3.6 Summary of Test Results

The three test arrays described in Sec. 2 have been used to analyze a particular process, namely, the silicon-gate deep-depletion CMOS/SOS

process. From the data generated to date, three problem areas have been uncovered that warrant future investigation. The first, which is strictly process related, concerns the integrity of the channel oxide. The yield curves showing the number of gate-to-island short-circuits have been widely variable and, for LSI arrays, can dominate the final yield.

The second area is process-dimension related and involves the nonplanar nature of the present process. As can be seen from the yield curves, a substantial yield reduction is incurred due to steps. Our ability to pattern various layers (epi-silicon, polysilicon, aluminum) on a planar surface is substantially better than it is on a nonplanar surface.

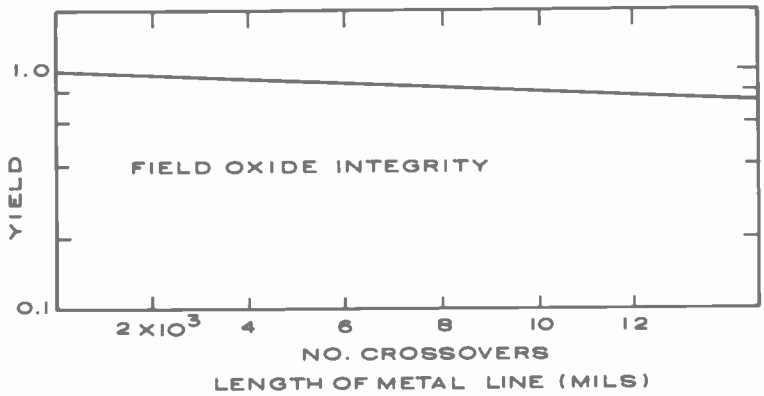

Fig. 16—Field oxide integrity; yield as a function of number of crossovers

The third area is also process-dimension related and is concerned with contact openings. At present, fine line patterns can be defined (at least on a planar surface) with decent yield, but the size of the contact that must be used to connect one layer to another must be larger than either level to have a relatively high probability of opening. The physical dimensions of the array and, hence, the packing density, are dominated by the size of the contact opening.

All of these problem areas are essentially yield related. With the advent of new process techniques, yield values, as related to a fixed set of dimensions, will increase, and for a given set of yield values, it will be possible to reduce dimensions and, correspondingly, increase packing density.

4. Design Rule Optimization

The previous section related process technology to physical dimensions through the generation of yield curves. In general, as physical dimensions

are reduced, the yield associated with producing that dimension is reduced. As dimensions are reduced, however, the packing density, or number of chips per wafer, is increased. An extremely important parameter, therefore, is the number of "functioning" chips per wafer, which is dependent upon both the yield and packing density. Consider the expression:

$$\text{number of chips/wafer} = \frac{\text{wafer area}}{\text{chip area}} \qquad [1]$$

and

$$\text{number of good chips/wafer} = \frac{\text{yield} \times \text{wafer area}}{\text{chip area}} \qquad [2]$$

The chip area is, of course, proportional to the various physical dimensions used to lay out the array. There are three cases of interest. (1) Both the length and width of the array may be functions of a particular physical dimension (or design rule); this will be referred to as the two-dimensional design limitation. (2) Either the length or the width alone may vary with a particular design rule; this is the case of one-dimensional design limitation. (3) The array area may not be a function of the particular design rule being considered.

For the case of two-dimensional design limitations, Eq. [2] becomes:

$$\text{number of good chips/wafer } (2D) = a \frac{\text{yield}_d}{(\text{dimension})^2}, \qquad [3]$$

where a is the constant of proportionality. In the one-dimensional case,

$$\text{number good chips/wafer } (1D) = b \frac{\text{yield}_d}{(\text{dimension})}. \qquad [4]$$

For the third case, of course,

$$\text{number of good chips/wafer} = C\ (\text{yield}_d) \qquad [5]$$

and, hence, is simply a function of yield (i.e., the looser, the better). In some applications it is convenient to consider the width of a particular line as well as the spacing between the particular lines, and, hence, Eqs. [3], [4], and [5] become:

$$\text{relative number of good chips/wafer } (2D) = \frac{Y_w \times Y_s}{(w + s)^2}, \qquad [6]$$

where Y_w is the yield associated with a particular line width, Y_s is the yield associated with a particular line-to-line spacing, w is the line width, and s is the line-to-line spacing. Correspondingly,

$$\text{relative number of good chips/wafer } (1D) = \frac{Y_s \times Y_w}{(w+s)} \qquad [7]$$

and

$$\text{relative number of good chips/wafer} = Y_s \times Y_w. \qquad [8]$$

The yield data as given in Sec. 3 will now be inserted into the suitable expressions, and curves relating the relative number of good chips per wafer to the specific physical dimensions will be generated.

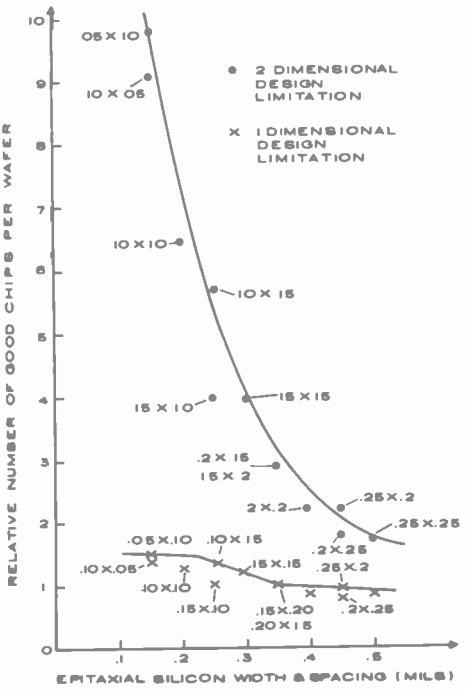

Fig. 17—Good chips per wafer as a function of width and spacing, epi-silicon

4.1 Epitaxial Silicon on Sapphire Films

Using the data from Fig. 8 and Eqs. [6] and [7], the curves relating the relative number of good chips per wafer to the epitaxial silicon width and spacing are given in Fig. 17. It is interesting to note that neither curve in Fig. 17 exhibits a peak value. This is directly related to the relatively small variation in yield with episilicon widths or spacings. As will be seen later, this is not typical. It also indicates that mask dimensions smaller

than 0.1 mil are necessary to find optimum values for these particular parameters. The figure also shows substantial increases in the relative number of good chips obtainable per wafer for the case where both the length and width of the array are a function of the epi-width and spacing. This is not the case for the one-dimensional situation where the increase in packing density is almost balanced by the corresponding decrease in yield.

From the data presently available, it appears that the use of 0.1-mil epitaxial silicon lines separated by 0.1 mil is close to optimum values. A variation in either parameter of ±0.05 mil will not substantially reduce the yield of an array fabricated with these dimensions. It should be noted that these are "actual printed dimensions," and care must be taken when selecting mask or layout dimensions that the process will produce these dimensions as the end result.

4.2 Polycrystalline Silicon Layers

For the case of planar polysilicon lines and spacings, there is sufficient data from Fig. 9 to generate a similar set of curves to that obtained for epi-silicon. Fig. 18 shows the results of applying Eqs. [7] and [8] to the data from Fig. 9. The non-dimensional case, of course, simply reflects the yield variation which, as shown in Fig. 9, tends to saturate at a value of 0.3 mil. For the one-dimensional case, it is seen that widths and spacings in the 0.2- to 0.3-mil range tend to flatten, indicating an optimum value of about 0.25 mil for P+ polysilicon widths and spacings. The two-dimensional case, using Eq. (6), is shown in Fig. 19, and a peak is observed at a polysilicon width of 0.2 mil and a spacing of 0.15 mil. As shown in Fig. 9, the dimensional control using the process described in Sec. 3.2 is quite good, and the 0.2-mil width and 0.15-mil spacing should be reproducible from mask to defined poly-line. Again, it should be pointed out that the numbers in Figs. 18 and 19 are actual printed dimensions in the P+ polysilicon.

Additional data must be generated for nonplanar polysilicon lines and spacings. Also, data will need to be generated for the case of N+ doped polysilicon layers since, in some applications, these are advantageous.

4.3 Contact Openings

In the area of contact openings, the data are too preliminary to generate an optimization curve. Applying Eq. [6] to the data in Fig. 12 indicates that for the two-dimensional case, the optimum contact size (square opening) appears to be between 0.15 × 0.15 and 0.20 × 0.20. The data yield essentially the same value for the relative number of good chips

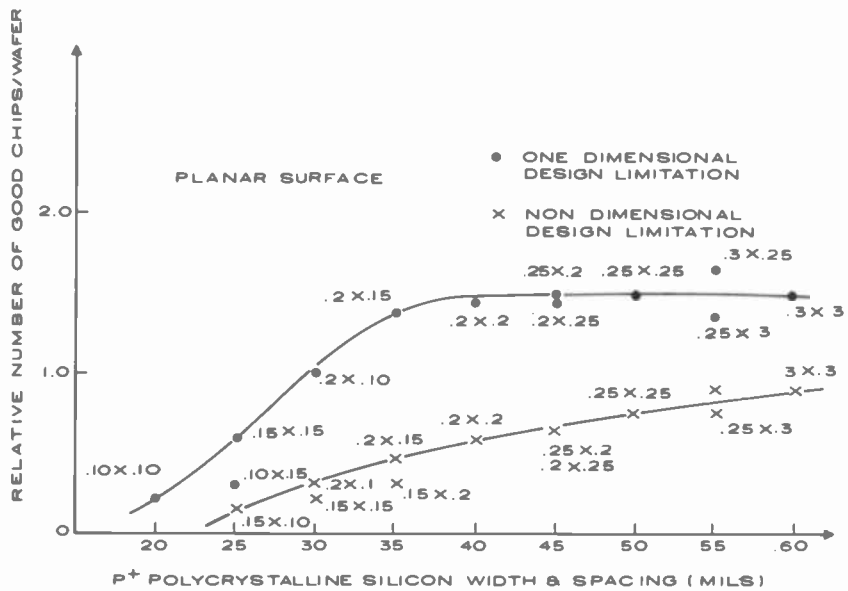

Fig. 18—Good chips per wafer as a function of width and spacing, polycrystalline silicon

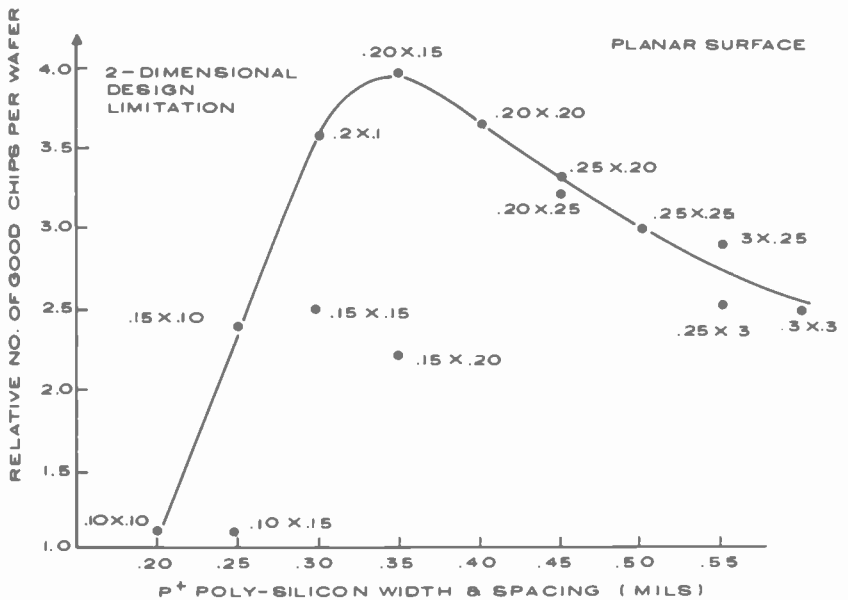

Fig. 19—Good chips per wafer as a function of width and spacing, polycrystalline

per wafer for contact sizes between 0.20 × 0.20 and 0.16 × 0.16 mils. For the one-dimensional case, the optimum size is greater than 0.20 × 0.20.

4.4 Metallization

Considering, first, the two-dimensional case (Eq. [6]), the results for optimizing aluminum on a planar surface are shown in Fig. 20. The results show a flat portion with a center value of 0.3 × 0.2 mil. It is felt, therefore, that this represents an optimum value, especially on planar

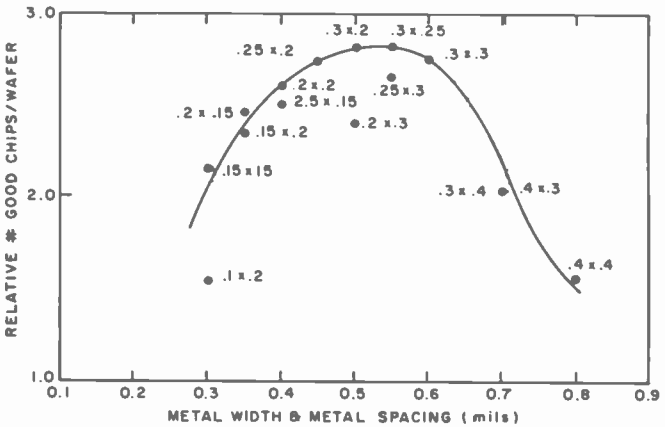

Fig. 20—Good chips per wafer as a function of width spacing, planar surface, metal limited in both directions

surfaces. When compared with optimum epi-silicon or polysilicon dimensions, it is seen that metal represents the single most dominant element in SOS/MOS packing density. This is also true in other technologies as well, and shows the advantage of silicon-gate technology, especially that incorporating double layer polysilicon.

Using Figs. 13 and 14, a similar curve for nonplanar surfaces can be generated and a comparison of this relationship with that shown in Fig. 20 is given in Fig. 21. It is seen that the data show considerably less variation for nonplanar surfaces, and it would, therefore, be more difficult to determine an optimum value. It is felt, however, that the planar optimum value is a suitable estimate for the nonplanar value, and, hence, 0.3 × 0.2 mil is considered the optimum width and spacing for aluminum metallization.

Another significant result is the substantial reduction in the relative number of working chips per wafer that can be expected due to the

nonplanarity of the surface. This is, of course, due to the lower yield values as given in Figs. 13 and 14. This points up the second technique, that of planar technology, which is being used in the industry to increase packing density through reduced dimensions. As can be seen from Fig. 21, it is possible to produce more working chips using 0.15 × 0.15 metal width and spacing on a planar surface than by using 0.3 × 0.2 mil dimensions on a nonplanar surface. To take advantage of this improvement in aluminum metallization, however, it is necessary to have an MOS planar metal gate process.

There are two contrasting viewpoints, therefore, concerning the di-

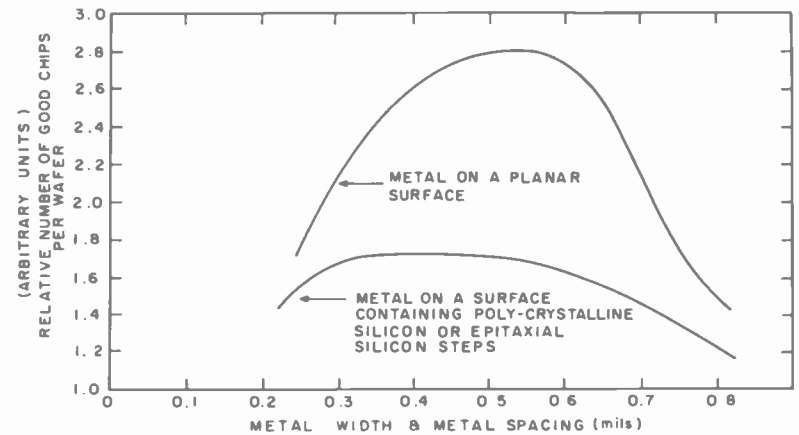

Fig. 21—Good chips per wafer as a function of width and spacing, planar and nonplanar surfaces, metal limited in both directions

rection that high density LSI will take in the future; one improves packing density by using more layers of polycrystalline silicon with its improved yield characteristic and, in essence, builds vertically. The second relies on reducing dimensions significantly by having a planar surface. One can only speculate on which approach will dominate, since the data presented here clearly demonstrate that both techniques will give improved packing density for a given yield figure.

Calculations have also been carried out for the one-dimensional case using the data in Figs. 13 and 14, and inserting them in Eq. [7]. Fig. 22 shows the results for the planar case, where it is seen that the peak has shifted to 0.3 × 0.3 mil. This is to be expected since the reduction in chip area occurs more slowly with the decrease in the metal width and spacing (linear) than it does for the two-dimensional case (quadratic) and hence, is not able to offset the resulting yield reduction at the tighter dimen-

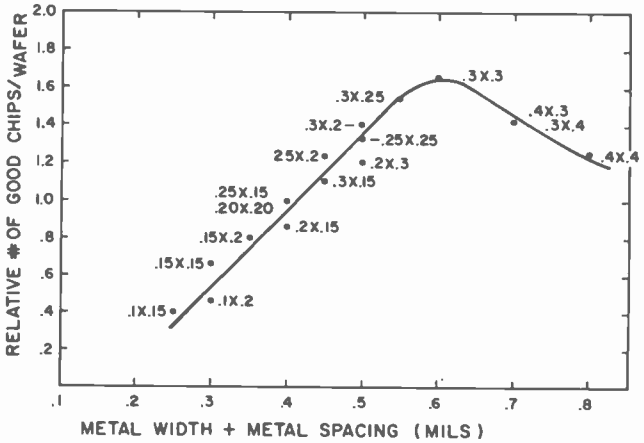

Fig. 22—Good chips per wafer as a function of width and spacing, planar surface, metal limited in one direction

sions. A comparison with the nonplanar case is shown in Fig. 23. The optimum values are represented by a range of dimensions from 0.3 × 0.3 mil to 0.4 × 0.4 mil where, again, the number of good chips producible on a planar surface is substantially higher than on the nonplanar surface.

For the condition where the number of good chips is only related to yield (Eq. [8]), the results are given in Fig. 24. This shows the advantage of using extremely loose dimensions when laying out areas of an array that are not metal-limited.

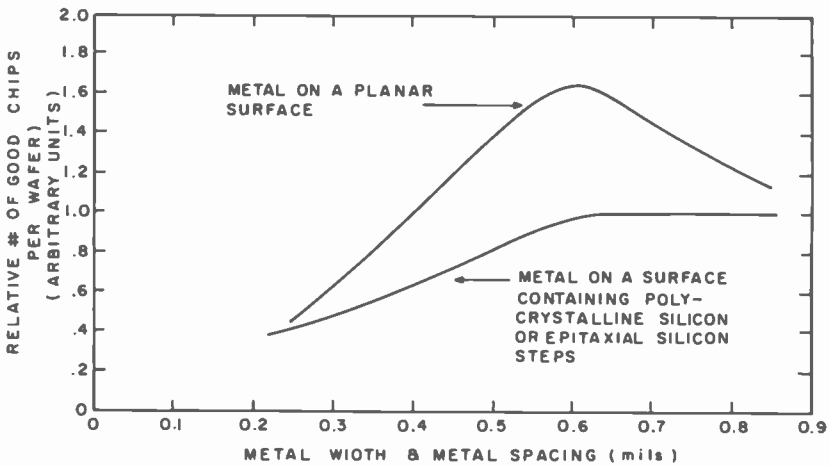

Fig. 23—Good chips per wafer as a function of width and spacing, planar and nonplanar surface, metal limited in one direction

5. Conclusions

A set of design rules can be generated using this mask set that are considered optimum for a particular technology. In the case of the silicon-gate deep-depletion CMOS/SOS process, the data indicate that the dimensions listed below are close to optimum values.

Definition	*Dimension (mils)*
Epi-silicon width	0.10
Epi-silicon to silicon spacing	0.10
Polysilicon width	0.20
Polysilicon-to-silicon spacing	0.15
Contact opening (square)	$0.16 \times 0.16 - 0.18 \times 0.18$
Metal width	0.30
Metal-to-metal spacing	0.20

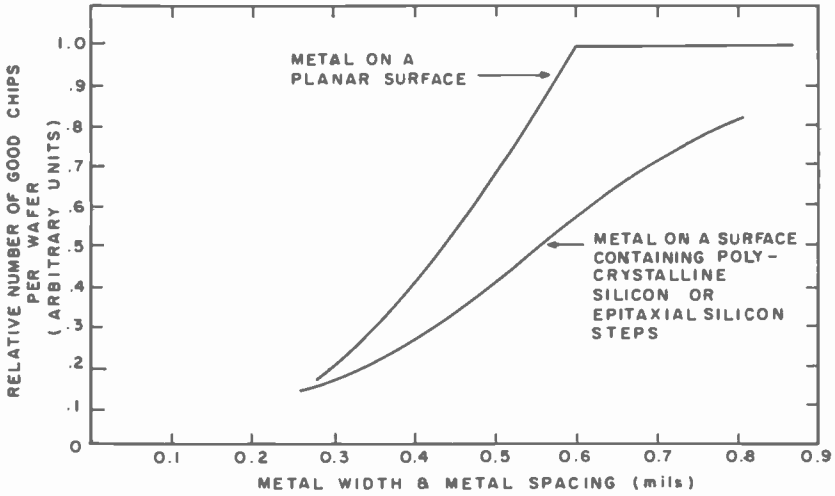

Fig. 24—Same conditions as Fig. 23 with number of good chips only related to yield (Eq. [8]).

It should be noted that the curves were generated using the combined values of level width plus level spacing. Since, in general, an array is limited by both the width and spacing, this is a legitimate combination. These are cases, however, where an array may only be limited by a width or spacing and the optimum value would, therefore, be slightly different.

It is also evident from the curves in this section that there are certain directions that process technology is likely to take in the future. The ability to define chemically vapor deposited (CVD) layers has been

shown to be substantially better than that using evaporated films. In addition, it is possible to take advantage of the crystallographic nature of silicon to define extremely small patterns. Multiple CVD layers, therefore, seem to be a promising avenue for improving packing density. The results presented here clearly demonstrate the advantages of planar technologies as a substantially different direction toward increased packing density.

The last question worth addressing concerning the results is whether the dimensions determined to be optimum represent a physical limitation on any of the process techniques used to obtain them. As described in Sec. 2 we are analyzing a process sequence comprising

(1) Thin film deposition or growth
(2) Photoresist techniques
(3) Etching techniques
(4) Doping techniques

It is felt that one or more of these techniques limit the minimum dimension associated with various layers. Photoresist appears to be the area of least limitation, especially with planar geometries. Concerning epitaxial silicon, film deposition appears to be the major limitation. For polysilicon, etching techniques seem to dominate as is the case for contact openings. Aluminum definition appears to be a function of both the deposition system (or technique) and the etching technique.

In conclusion, the various test patterns described in Sec. 2 were used to generate process-dimension yield data that were transcribed into design curves showing optimum values for circuit layout. These curves also pointed to directions that future technologies may take in order to obtain increased packing density while maintaining present yield levels.

Acknowledgements

The support and guidance of N. Goldsmith are acknowledged. Test samples were processed in the Solid State Technology Center by J. Fabula, S. Policastro, and D. Woo, and in the Solid State Division by C. S. Kim. The fabrication facilities and personnel at the RCA Laboratories including J. Sokoloski, R. Gilchrist, and A. Herrgott were extensively utilized.

References:

[1] A. C. Ipri and J. C. Sarace, "Low-Threshold Low Power CMOS/SOS for High Frequency Counter Applications," *IEEE J. Solid State Circuits*, SC-11, p. 329 (1976).

[2] G. W. Cullen, "The Preparation and Properties of Chemically Vapor Deposited Silicon on Sapphire and Spinel," *J. Crystal Growth*, 9, p. 107 (1971).

[3] C. Raetzel, S. Schild, and H. Schlotterer, "Etching Properties of Different Silicon Films," Fall MTG of The Electrochem. Soc. Abstract #142, Oct., 1974.

[4] A. C. Ipri, 1975 SOS Workshop, Lake Tahoe, Calif.

The Study of Microcircuits by Transmission Electron Microscopy

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Abstract—The use of transmission electron microscope (TEM) methods, especially in cross section, for detailed physical examination of the components of microcircuits is discussed from a device engineer's point of view. Careful attention is given to the type of problem that can best be studied by this method. Details of the required sample preparation process are shown and suggestions are made for ensuring a high probability of success with the samples. Since many readers will be unfamiliar with the mechanisms of TEM image formation, a brief discussion of the features of the sample that cause contrast is included. Specific examples showing use of the method on samples of interest to silicon-on-sapphire technology are presented. These samples show an anomalous thinning effect in the thermal oxide grown on silicon island edges that has not previously been noted. They also clearly demonstrate the capability of seeing layers as thin as 10 Å, as well as the interfaces between almost every material commonly used for the manufacture of microcircuits. Defect distributions within the single-crystal silicon and near the edges of the silicon islands are clearly shown, as is the grain size distribution present in heavily doped polycrystalline silicon used for gate metalization. A possible anomalous boron diffusion phenomenon in polycrystalline silicon due to the grain size distribution is suggested. An example using oxide isolation methods shows that accurate modelling of such processes is possible from the excellent profiles obtained by cross sectional TEM methods.

1. Introduction

Microcircuits, like the solid-state devices from which they by and large evolved, depend upon the electronic and thermal properties of silicon

together with modern microlithographic methods. Much is known about the various methods for altering the electrical properties of silicon, such as variable crystal pull rates, solid-state diffusion processes, and ion implantation. Much is also known about the methods for forming dielectric films on silicon, such as thermal oxidation in various ambients (gases, temperatures, and pressures), chemical conversion by massive ion implantation, and chemical vapor deposition. Studies have been done to determine the properties of the energy bands and of the mechanical and optical properties of silicon. Whole industries are built up around the formation of images on polished wafers of silicon. Treatments that affect the crystallographic perfection of silicon are well known and are continually being studied. Many other details could no doubt be listed. Despite all this knowledge, the actual detailed internal microstructure of the critical operating regions of the individual devices of the microcircuit has rarely, if ever, been observed as it exists in an operating device. For example, the MOS transistor operates by electrostatically inducing a charge into the silicon within some hundred angstroms of the actual silicon surface. Typically this surface is covered with a thermally grown SiO_2 layer. Theories of current transport in such surface layers have been developed without benefit of knowing the structure of the silicon near the oxide. For the bipolar transistor the entire action may occur in a narrow (<1 μm), though sometimes physically complex, base region. The junctions on both sides of this region as well as the base region itself are normally considered very important to the current gain obtained. Once again these regions of the device have rarely, if ever, been microscopically observed as they actually exist in a device and theories have developed without benefit of the knowledge of the actual physical structure.

This is not to say that attempts to observe such regions have not been made. It is sufficient to say that most attempts have relied on assumptions that are difficult, if not impossible, to prove. For example, one might grow a thermal SiO_2 layer on silicon and subsequently remove it by a chemical or mechanical means such as with HF or by sputtering. Whereas it is *reasonable* to expect that these techniques will expose the silicon surface as it existed with the oxide on it, there is no guarantee that the oxide removal technique will not in itself alter the silicon. Other attempts to observe this type of structure by using low-angle sections in the hope of "amplifying" the nonuniformity present in the interface have two fundamental problems. The first of these is illustrated in Fig. 1 where a hypothetical low-angle section is shown. Cursory observation of the top view of the sections might lead one to believe that "bubbles" of progressively increasing size exist as one proceeds deeper into the film. This is an extreme example, but it demonstrates that this method, as other methods that attempt to use geometrical amplification, relies on

exact uniformity throughout the original sample plane. The second problem is that the sectioning method itself will very likely introduce a "fuzziness" into the interface observed. This is particularly true of sections produced by the typical angle lapping or polishing procedures. We therefore conclude that any method that includes material removal in a direction substantially parallel to the interface of interest will suffer loss of resolution because of lateral nonuniformities of one type or another, or because of nonuniform material removal rates.

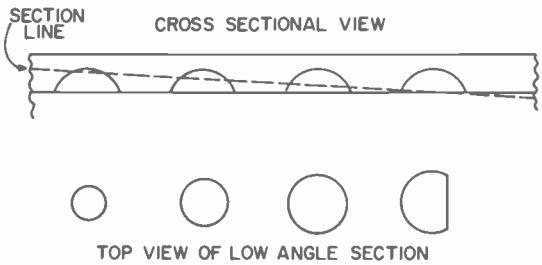

Fig. 1—Effects of lateral nonuniformities on low angle sections.

In this paper, we discuss the use of transmission electron microscopy, with which it is possible to observe physical features of integrated circuit structures as they actually exist in a device to a resolution of a few angstroms and with no geometrical amplification. With transmission electron microscopy, only those materials that diffract (i.e., are at least partially crystalline) or that have different electron absorption properties from their neighbors can be distinguished. Most materials used for manufacturing microcircuits fall into one of the above categories. TEM methods provide at least a factor of 20–100 improvement over the resolution obtained with conventional methods. More importantly, TEM samples allow crystallographic perfection, subsurface features, and interfacial regions to be seen.

We do not mean to imply that the use of transmission electron microscopy methods on materials of interest to microcircuits is new nor do we wish to imply that this is the first use of TEM for examining IC structures. Such work by others and by the authors has already been published. This paper, however, presents much more detail concerning the types of sample that are likely to have the best success, shows more complicated and interesting structures than have heretofore been published, and shows correlation between the microscopic structure and electrical performance of devices.

We also do not mean to imply that coarser measurements than those available by TEM are of no value; quite the contrary is true. Etching studies, X-ray topography, and scanning electron microscopy (SEM) are invaluable preliminary steps to TEM. These methods are faster and more convenient than TEM and serve to indicate possible areas of interest and often to help in the interpretation of the TEM work. The spirit of the present article is that such preliminary examinations are made as a matter of routine and we therefore focus on the greater detail available in TEM. We do give an example of a complementary and mutually reinforcing examination by SEM and TEM in Sec. 4.

In Sections 2 and 3 we discuss sample preparation for TEM and the information content of TEM micrography respectively. Both these topics are extremely complex. Our presentation is addressed not to the practicing electron microscopist but to the device engineer. We, therefore, attempt to give a physical feeling for what can be done, how it is to be done, and what type of interpretations (and misinterpretations) can be made. Detailed discussions of some practical examples are included.

2. Suitable Sample

The basic requirements for a suitable sample are that it be thin enough to pass an electron beam through and that the materials or structures of interest be present in the thin region. Typically, for the electron beam energy levels used for TEM work, the samples must be less than a few thousand Å thick. This thickness can be achieved by an ion milling method and this is the method most frequently used. Thinning by chemical etching is also a well known and useful method for TEM sample preparation. For preparing cross sections of typical microcircuits that contain layers such as Si/SiO_2 or Si/Si_3N_4, it is obviously not suitable because of the difference in the chemical reactivity of the materials present. The key to achieving a successful sample, however, lies in the preparation of the sample prior to ion thinning.

To thin a sample parallel to the plane of the wafer, the wafer is first ground and polished from the back to a thickness of $\sim 25\ \mu m$ and then ion thinned from one or both sides until the desired thickness is reached. (It is nearly impossible to determine the depth from the top surface being examined if thinning from both sides is used.) In most cases these parallel thinned samples are not of the greatest interest for IC work because the features, which are defined by photoresist methods, typically are $>2\ \mu m$ and most interfaces are parallel to the wafer plane. Furthermore, those interfaces that are not parallel to the wafer plane tend *not to* be perpendicular either. One is left with a situation not unlike that of the low-angle sectioned samples wherein the extent and nature of the in-

terfaces may appear broadened as shown in Fig. 2. If the viewing angle is adjusted so that one of the interfaces has minimal width, then the other will be even broader and multiple images may be necessary. These effects are discussed more fully in the next section.

In most cases a strong tendency exists for the interfaces to be parallel to the wafer plane simply because the layers used in IC's are usually much wider than they are thick and are formed from processes that uniformly affect the wafer surface. Since the interfaces are parallel to the wafer surface, they can best be observed from the side, i.e., perpendicular to the wafer plane. This type of observation requires greatly increased sophistication in sample preparation.

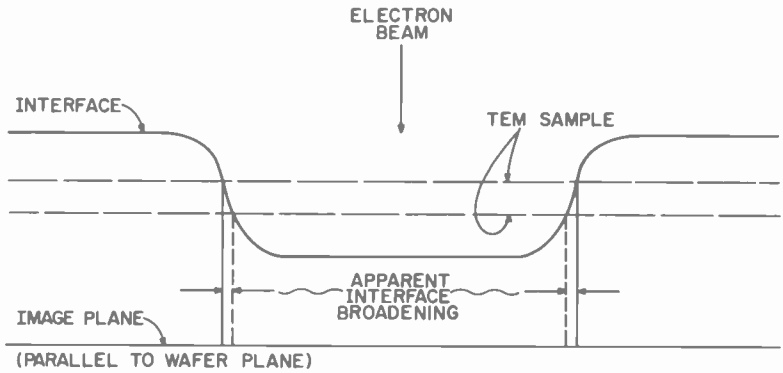

Fig. 2—Cross-sectional view of an arbitrary interface in a microcircuit structure and the interface broadening that appears to exist when viewed from the top.

The basic method used for the samples shown here was developed several years ago.[1] The cross sectional samples are restricted to be no wider (see Fig. 3) than the wafer thickness. The typical initial thickness is 0.4 mm which after very careful mechanical polishing is reduced to 0.025 mm. The length can be arbitrary but must be such that it will fit into available ion thinning fixtures. The region of interest on these samples is the extreme edge of the thin side as shown in Fig. 3. It does not require a great deal of imagination to appreciate the extremely delicate nature of these samples and the absolute precision required in both the mechanical and ion thinning processes. In general, it is necessary to provide the edge with a protective coating in order to avoid removing the entire region of interest during the thinning process.

When one is interested in a particular area of a wafer (for example, an area in which a circuit failed), he must dedicate the sample prepara-

tion effort from the beginning toward this area. The first step is a sawing operation, and consideration must be given to the direction of the cut to be made in order to expose the best possible cross section. The final sample will be <0.2 μm thick, and the saw can be guided to no better than $\sim\pm$25 μm. The region of interest must remain in the nominal center of the sample in order to be preserved through the subsequent steps. After the sawing operation, the sample will be typically 250 μm wide. At this point one must carefully measure the distance of the area of interest to the edges of the saw cuts. The next thinning step proceeds by polishing both sides approximately equally until the final thickness is $\sim$25 μm. This must be done with great care or the desired area is likely to be lost.

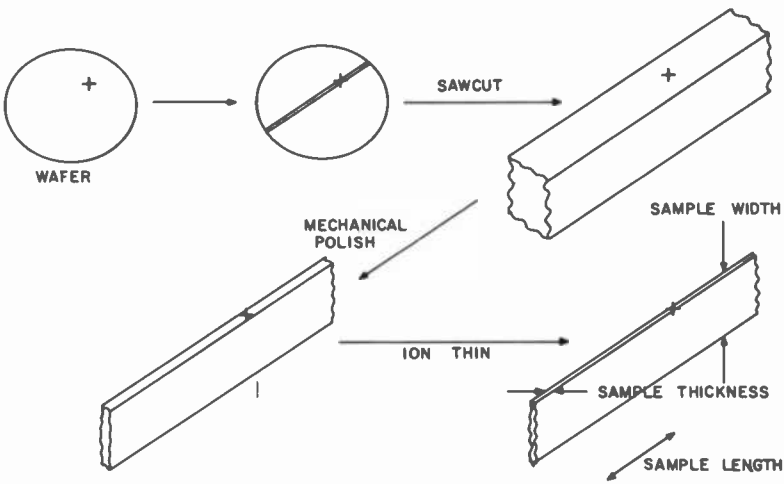

Fig. 3—Schematic of process of forming a TEM sample from a wafer. The x indicates the location of interest.

The sawed sample is embedded in a wax such as Apiezon* and the polishing is begun. Care must be taken to note the time when the sample itself begins to polish and the material removal rate must be known. The polishing is stopped approximately 10 μm before the area of interest is reached. At this point, one must again carefully measure the distance from the area of interest to the edges of the saw cuts. If the sample was not exactly parallel to the polishing plane, the area of interest may have been removed and this can be noted after dismounting. An iterative process may be required to isolate the desired region to within 10 μm of

* Trade name.

the polished edges. Each iteration produces manifold opportunities for breakage and is very time consuming.

Assuming the area of interest is successfully isolated in this 25 μm polished sample, the sample is then mounted for ion thinning. A side view of the sample at this point is shown approximately to scale in Fig. 4. This thinning process is usually carried out from both sides. The primary control on the ion thinning is the optical density of the sample, as the thinning rates and sample thickness are not generally known with suf-

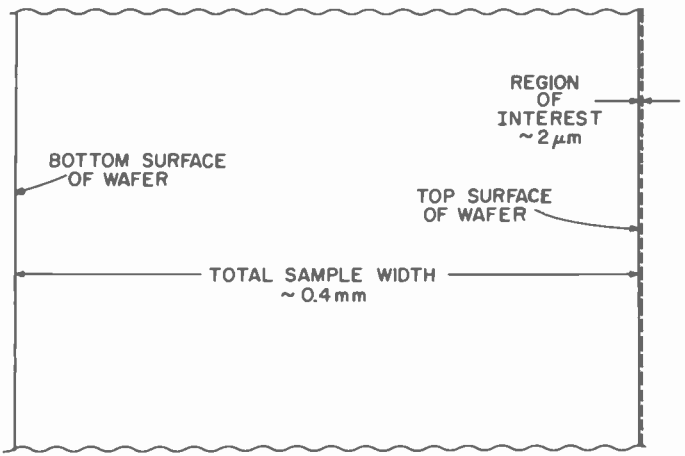

Fig. 4—Section of a TEM sample drawn approximately to scale. The electron beam would normally be perpendicular to the page.

ficient accuracy to use time as the basic controlled parameter. One can therefore expect to isolate the thinned region to perhaps ± 5 μm in the direction perpendicular to the original polished surfaces. Isolation in a direction parallel to this surface can be done with great precision if the sample still contains the region of interest after the thinning process. It is sometimes found that the optical density of the total sample (which is mostly substrate material, as shown in Fig. 4) does not accurately reflect the situation on the edges. Thus, it is possible for entire sections of the edges to be missing or to be too thick for electron penetration after ion thinning. In general, however, suitable surface regions will exist somewhere on the sample, as shown in Figure 5. Obviously, it is difficult to guarantee that the portions of the sample that are suitable for good TEM images will in fact be those regions of interest. Clearly, therefore, the process required to examine a particular preselected portion of a

wafer produces a low chance of success and is quite involved. A great deal of effort must go into a single sample. Areas that need to be examined by this method must be very carefully documented and studied before attempting to form a TEM sample. The overall chance of forming a successful sample is greatly increased if several samples addressing the same phenomena are used. This requires of course very careful book-keeping and a linear increase in effort.

Fortunately many questions of interest in the physical structures of integrated circuits do not require examination of a specific area of a wafer

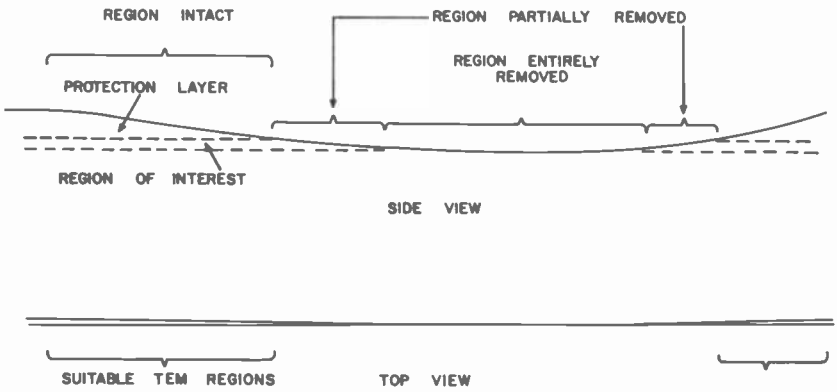

Fig. 5—Effects of non-ideal thinning on practical samples.

but rather need only a particular type of combination of materials. For these types of questions a *periodic* structure is ideal. If the variation in the direction perpendicular to the polished faces is not important, the process of obtaining a good TEM sample of the structure of interest is much more likely to be successful. In a typical circuit it may be difficult to identify the features of the TEM image, since in these cases the variation in a direction perpendicular to the polished faces is important. Some examples of TEM sections of circuits whose basic elements repeat have been shown by Sheng and Chang.[2] We will concentrate in this paper on periodic structures fabricated in the same way as a circuit as far as processing is concerned, but with geometries that are more favorable for TEM samples.

The periodic structures chosen are simply strips of repeating width and spacing. These strips can be used to form almost all structures of interest to IC's by using various spacings and by aligning the strips of one level to those of previous levels or by covering the entire surface with

a layer without forming the strips. A typical example of a structure that may be formed by this method is shown in Figure 6. Here we see that at least 25 unique features can be identified from each repeating unit and that nearly exact duplicates of these are present in the same sample for verification of the effects seen. Some of the labeled features might not seem to be unique. Examination of the actual TEM images shown later will reveal that many of the labeled areas are in fact unique and contain some of the more important information. It will also show that in some cases the schematic drawing is substantially incorrect when compared to the shapes actually existing.

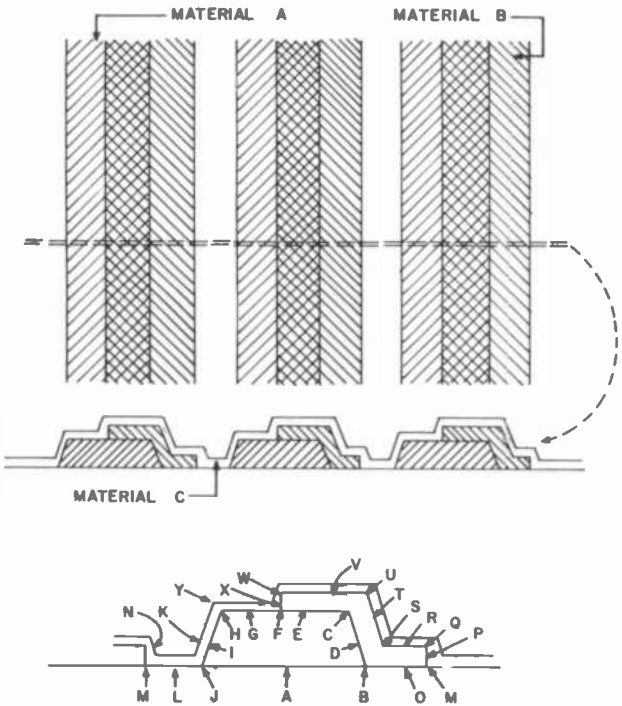

Fig. 6—Strip method used to form almost any desired microcircuit structure for TEM examination. The letters indicate possible points of interest.

The effects of greatest interest are usually where edges of one form or another exists. In some cases, particularly with crystalline materials such as silicon, the structure of the material away from the edges is also of interest and this is also available from the sample. In some cases, interaction between the edges may be present. For these types of investi-

gation a sample with more than one edge-to-edge spacing is suggested. If the effects are in fact due to edge interaction they will in general be strongly influenced by the edge-to-edge spacing. Only the spacings determined by the masks will be adjustable on the same samples. Thus, the possibility of determining the cause of the effects seen, of seeing many different kinds of interfaces and materials in the same sample, and of producing more than one observation of the same structure in the same sample is enhanced by using carefully constructed samples of the general type shown in Fig. 6.

3. Information Contained in TEM Micrographs of IC Structures

As mentioned earlier, we are dealing with the properties of a beam of electrons transmitted through solid phase material. The transmission process causes changes in the nature of the beam by absorption and/or diffraction. The actual processes occurring are very complicated and constitute an entire field of study in themselves. The reader is referred to reference texts[3–5] for more thorough discussions. A basic division must be made, however, between amorphous materials and crystalline materials, since the factors determining the transmitted intensities are completely different for the two cases. We will briefly discuss the salient factors affecting the images obtained so that an individual unfamiliar with TEM technology can obtain a reasonably accurate impression of the sample from the images.

3.1 Amorphous Materials

For amorphous materials, absorption is the most important consideration. The transmitted beam will be more intense where the absorption is the least and less intense where the absorption is greatest. The absorption is determined by the electronic properties of the material *and* by its thickness. (Thus, an internal measure of ion thinning uniformity exists.) The observed transmitted intensity is determined by integration of all absorbed electrons, regardless of how the absorption occurred. This can be important when one is concerned about the extent of interfacial regions as discussed below. An image of the transmitted intensity over the region of the sample that is in the beam can be obtained by expanding (magnifying) the transmitted beam (using electromagnetic lenses) and exposing a fluorescent (or more strictly, cathodoluminescent) screen or suitable electron sensitive film. The image observed is simply that of transmitted electron intensity and can be thought of as being a result of the many independent sub-beams that form the main beam. This

concept of sub-beams is particularly helpful in understanding the way in which the images from crystalline materials arise.

In the ideal case when the electrons are incident exactly parallel to a hyperabrupt planar interface the image will typically exhibit 10 Å of "fuzz." This fuzz is caused by nonideal lenses in the microscope and other factors characteristic of the particular microscope and sample in use and can be as low as 2 Å. This is also called the resolution limit and is at least 20–100 times better than typical scanning electron microscope resolution currently in use for examining the surface features of integrated circuits. If the beam is not exactly parallel to the hypothetical hyperabrupt interface a transition region will appear to exist as shown in Fig. 7. If the electron absorption coefficient is α_1 in the upper material of Fig. 7 and

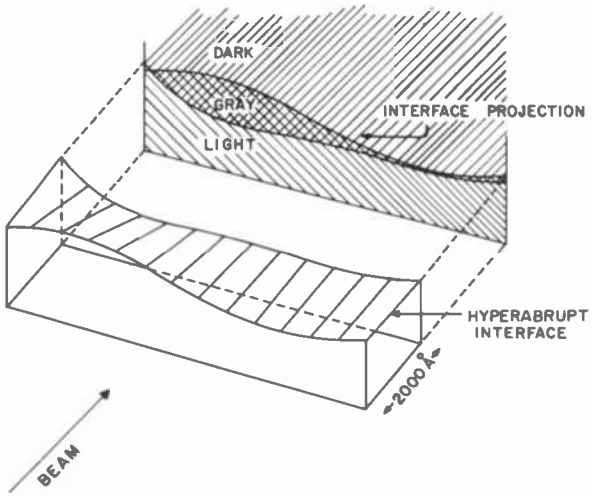

Fig. 7—Effects of intrasample interface tilt on the TEM image. An interface between two amorphous materials is shown.

α_2 in the lower material, the transmitted intensity is given by

$$I_{t1} = I_0 \exp(-\alpha_1 X_s)$$

for the upper layer and by

$$I_{t2} = I_0 \exp(-\alpha_2 X_s)$$

for the lower layer, where I_0 is the incident intensity and X_s is the total specimen thickness. Let us further assume that the interface is tilted with respect to the incident beam by an angle as shown in Fig. 8.

In the interface region the transmitted intensity is given by

$$I_{tI} = I_0 \exp(-\alpha_1 X_1) \exp(-\alpha_2 X_2)$$

where X_1, X_2 and other symbols are defined in Fig. 8. This equation can be readily rearranged to a more convenient form:

$$I_{tI} = I_0 \exp(-\alpha_2 X_s) \exp[-y \cot\theta(\alpha_1 - \alpha_2)].$$

Now $I_{t2} = I_0 e^{-\alpha_2 X_s}$ is the transmitted intensity at the bottom of the interface projection and $I_0 e^{-\alpha_1 X_s}$ is the transmitted intensity of the top

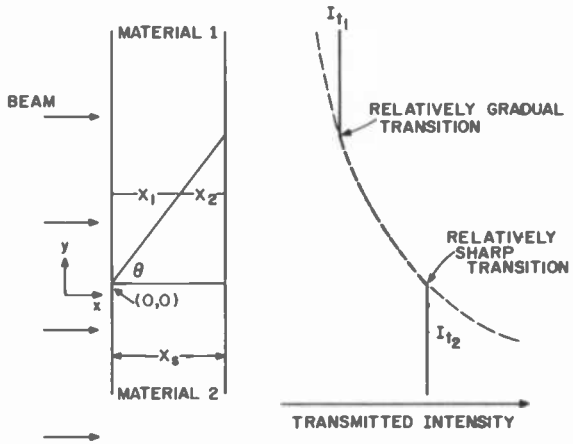

Fig. 8—Transmitted intensity in a tilted interface region similar to that of Fig. 7.

of the interface projection. If $\beta = (\alpha_1 - \alpha_2)\cot\theta$, the intensity in the projected interface region only is given by

$$I_{tI} = I_{t2} e^{-\beta y}.$$

Thus, the intensity in the projected region, as shown in Fig. 8, may or may not appear linearly graded. In general one would expect a relatively sharp transition from the region of low absorption to that of the interface projection and a less sharp transition from the region of high absorption to that of the interface projection. This is shown in Fig. 8. This difference in sharpness is greatest when I_{t1} is near zero and is minimum where $I_{t1} = I_{t2}$. The important point of this discussion is that precisely the same kind of image can exist when a hyperabrupt interface is tilted as can exist when a gradual transition between two materials exists, and that one would expect to see, with good resolution, the shape of the outline of the

interface projection if a tilt were purposefully introduced. The intersection of the interface with the sample surface should be visible.

Clearly if there are no "grey" areas visible, there is no possibility of a transitional type of interface whose width is greater than ~10 Å (typically ~3 atomic layers). If a grey area exists, one can attempt to minimize its width by tilting the sample. Thus, if the width can be reduced, a tilted interface must be assumed. On the geometrical scale of interest here, such transition regions may not be noticed until after development of the photographic plate and after the sample is removed from the microscope. In addition, tilting to reduce the observed interface width to a minimum will, in general, result in substantial distortion in the rest of the image due to complicated projections of the sample on the image plane of the microscope. In these cases, one can examine the envelope of the grey area and determine if the undulations occur over distances comparable to the sample thickness. If they do not or if no appreciable undulations exist, one can usually assume that no significant interface tilt is present. A situation is shown later where this is not true however.

Since the transmitted intensity is determined by the total material, it is not in general possible to determine a difference between a completely homogeneous transition region and one consisting of micro (<10 Å) islands of amorphous material. The shape of every interface between amorphous materials with substantially different electron absorption coefficients existing in a sample should be visible with a resolution of <10 Å. The absorption coefficients themselves are expected to be slowly increasing functions of the mean atomic number of the elements in the material and are sensitive to the density of the material.

3.2 Crystalline Materials

The image seen from the transmitted electrons is formed basically by a subtraction process. In the amorphous case discussed above, this subtraction was accomplished by absorption. Some of the electrons in each sub-beam of the image are removed, thereby reducing the strength of the transmitted beam. The sub-beam itself travels through the sample in a straight line and the absorbed electrons return to the system ground through the sample holder. In the case of crystalline materials, however, the sub-beam will be partially diffracted as it passes through the sample. In this case the intensity of the sub-beam is reduced by a deflection (by diffraction) process. This results in total conservation of electrons. The image obtained by expanding (magnifying) the directly transmitted beam will, therefore, be the least intense where the most diffraction has occurred and the most intense where the least diffraction has occurred. Since the process of diffraction is intensified as more and more planes

of the crystalline atoms are traversed by the beam, the process is not unlike that of absorption. However, since mono-energetic electrons are used, diffraction will occur only from those planes that satisfy the Bragg condition. Therefore, deviations in the micro-orientation of the crystal plane can cause large changes in the diffracted intensities. This feature is completely different from the amorphous case and is frequently the dominant cause of contrast in crystalline materials. The particular formulation of the intensity is much more complex than for simple absorption and will not be discussed here. The important point to note is that a transition between an amorphous material and a crystalline material will be sharply visible because of the different amounts of beam removal due to absorption and diffraction, respectively. For most specimens of interest diffraction is a stronger influence on the image than absorption. For samples that are too thick, absorption always dominates.

Defects in a crystalline material cause changes in the diffraction conditions near the defects and may, therefore, also be visible. For some types of defects that diffract, such as twins, it is possible to adjust the tilt of the sample such that a very strong diffraction exists from the twins. One can then expand (magnify) this *diffracted* beam to obtain an image that is most intense where the twins exist. This type of image is called dark field and is exactly analogous to an optical microscope dark field image. For most investigations of first-order interest to microcircuits, these dark field images are of secondary importance. They are, however, extremely important for determining, for instance, the type and location of defects or material with a specific orientation.

For a defect to be visible, it must occupy a significant fraction of the sample thickness so that it can interfere with the diffraction to a level that will be seen in the transmitted sub-beam. Not all defects in crystalline material will be visible. Usually a strain field exists near the defect, wherein the atoms are displaced slightly from their usual lattice position. This strain field aids in disturbing the diffraction and produces greater contrast.

It can be shown that the beam is deflected only very slightly by a typical diffraction. A typical deflection angle is perhaps ½°. Thus, very small bends in the lattice can cause very large changes in the diffracted intensity. It is not unusual to see large contrast changes over regions of apparently defect-free material that are due to very slight bending of the samples. These types of region must be interpreted with great care. Typically, defects show relatively sharp and distinct features. In the neighborhood of interfaces, however, intensity changes must be carefully studied before assuming the causes. Large intensity changes do not always mean that significant structural changes exist.

Since the crystalline materials diffract, they produce a typical diffraction pattern characteristic of the crystal orientation. If the lattice producing the diffraction is not in its equilibrium state, the atoms may be displaced slightly, and this strain can be detected by analyzing the position of the diffraction spots. Thus, a means for determining the average strain in the crystalline material over the entire imaged area also exists.

While this discussion is simplistic, it does contain the essence of most of the important ways that images are formed and should give the reader enough information to be able to interpret most of the features of TEM images that are important for IC applications. In summary these features and methods are (1) resolution of edges and interfaces with great accuracy, (2) observation of the detailed structure of the crystalline parts of the sample and (3) a measurement of the strain existing in the single crystalline parts of the sample.

Usually the only crystalline materials present are silicon, some metals, such as aluminum or tungsten, and substrate materials such as sapphire and spinel. Frequently, the silicon is present both as nominal single-crystalline material and as polycrystalline material. Defects in these materials may be of interest, since they can control properties of the material such as electrical transport, material transport (including diffusion and electromigration) and non-equilibrium effects such as lifetime and recombination of electrical charge carriers. Detailed observations of the defects in the devices can help greatly to understand which mechanisms are important in determining the electrical properties and, possibly, the long term stability of the devices.

4. Example Using Silicon on Sapphire Technology

We have chosen to use silicon on sapphire technology as a good example of a typical implementation of the methods described in this paper. Silicon on sapphire is used primarily for high performance digital integrated circuits. Typically, a thin film of silicon is epitaxially deposited on a polished single-crystal sapphire substrate, and this film is divided into islands of isolated silicon by an etching process. Other methods for forming the regions of isolated silicon also exist, such as converting the silicon into silicon dioxide between the islands by thermal oxidation or by selectively conditioning the sapphire surface so that relatively non-conducting silicon grows in the conditioned areas. We have used processes for forming the samples that are essentially the same as those currently used by RCA for manufacturing LSI circuits.

The silicon film is nominally 6000 Å thick at the beginning of the process. A thin oxide is grown or deposited on the silicon surface and is

defined into the shape desired for the silicon island. In this case we have chosen a nominal 13 μm (0.5 mil) island width for the grid mask (see Fig. 6), since this is a typical size. The silicon was etched using a potassium hydroxide-n-propanol solution, which is commonly used to form sloped edges in single-crystal silicon. This etch attacks {111} planes more slowly than others and therefore tends to leave {111} planes. Usually some over-etching, that is etching beyond the time required to remove the silicon from the sapphire, is employed to ensure that the entire wafer is sufficiently etched. This produces a degree of undercutting of the silicon beneath the oxide mask and produces some nonideal shapes on the edges of the islands. The oxide etch masks are chemically removed, and a thermal silicon dioxide layer is grown on the silicon to a thickness of approximately 1100 Å in a steam atmosphere. This channel oxide grows only on the silicon; the base sapphire remains nominally unaffected. At this point, a layer of silicon ~5000 Å thick is deposited on the entire wafer by chemical vapor deposition. The deposition is done at ~700°C by silane decomposition and the silicon deposit is polycrystalline. This polysilicon is nominally undoped at this point but is subsequently heavily doped by any of several methods and serves as a metallic-like electrode for the gates of MOS transistors and as an electrical connection between different areas of the circuit. For the samples discussed here the polysilicon was doped by diffusion from a boron doped oxide source at a temperature of ~1050°C. This produces P+ polysilicon beneath the doped oxide. After deposition, the boron-doped oxide is defined into strips using the same mask that was used to define the silicon islands, but the mask is intentionally misaligned to the islands in a manner similar to that shown in Fig. 6. After the diffusion, the boron doped oxide strips are chemically removed and the wafer is again exposed to the silicon etch solution. This etch will not attack silicon heavily doped with boron and, therefore, removes only the undiffused polysilicon. At this point, the wafer is coated with a 1μm layer of deposited oxide as a protection during ion thinning and to simulate a typical passivation layer for a circuit. The sample thus represents an entire cross section of an operating MOS transistor in its channel region (where the single crystal silicon is lightly doped), except that the poly does not cross the entire island. By not allowing the poly to completely cross the silicon island, it is possible to examine the structure existing at the edge of the gate electrode in terms of the poly shape and channel oxide structure near the poly edge. Since neither the poly nor the channel oxide is sensitive to orientation, this slight perturbation is reasonable. Thus, all of the features of interest to the central channel region of a transistor are contained in a single sample. This sample could have been processed further to contain information of interest about the heavily doped source

and drain regions by etching the channel oxide after etching the poly and diffusing or by implanting dopant through the channel oxide into the single-crystal silicon not under the poly. This was not done here because we wanted a sample with "uniform" properties throughout, so that the extent and reproducibility of the silicon structure seen could be determined. The intended structure is shown in Fig. 9.

A montage showing an actual TEM image of a sample of the form of Fig. 9 is shown in Fig. 10. This figure shows a single silicon island 13 μm long and contains a plethora of information. In this and in all succeeding

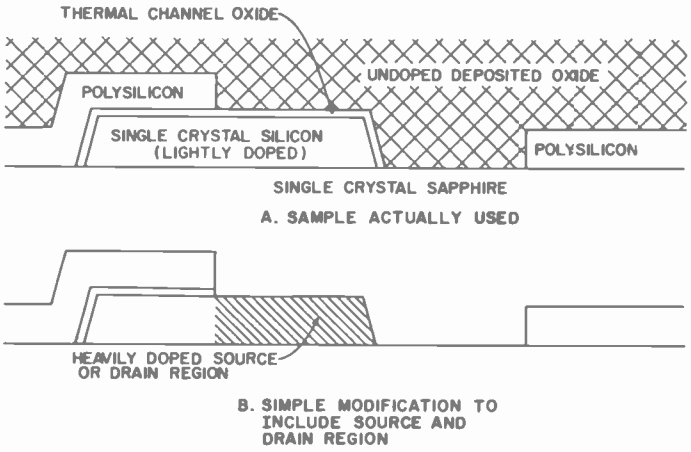

Fig. 9—Silicon on sapphire sample addressing the properties of MOS transistors. (A) Structure intended for images shown in Figure 10. (B) Modification of (A) to include heavily doped source and drain regions.

micrographs, the orientation of the single-crystal silicon is as shown in Fig. 10. We shall discuss the more important points one at a time. We note that the poly mask was not precisely aligned to the silicon island. The poly edges should have been in the center of the island.

The first point to make is that Fig. 10 shows a section 13 μm (0.5 mil) long. This represents approximately 1/250 of the length of one side of a typical single LSI circuit. It would take approximately 50 sections of the thickness of this sample to fill the space between the source and drain of a single 10 μm (0.4 mil) long MOS transistor. From the overall view of the entire image, one can immediately obtain a feeling for the "third" dimension of the circuit. A direct comparison of the z direction with the

x or y direction is available as it actually exists (i.e., without geometrical amplification or viewing angle distortion). The distance charge must travel from the source to the drain is put into perspective. The thickness of the channel oxide as compared to the silicon and the poly is clearly evident. As a point of calibration, typical circuit designs assume that the masking levels can be aligned to each other within an accuracy approximately equal to the extent that the poly overlaps onto the top of the silicon island. Typical minimum dimensions (line widths and spacings) are one-half to one-fourth the length of the silicon island. Attempts are continually being made to shrink these dimensions into the submicron range, largely by using nonoptical lithographic methods. Line widths of less than 0.5 μm can be obtained. If such dimensions were used to determine the silicon-island width, more than two-thirds of the surface area of the silicon would be on the edge of the islands, which is generally considered a parasitic region. Thus, a clear and accurate projection of the physical effects to be expected by changing the x or y dimensions can be made. These effects could include items of primary importance, such as crossover capacitance and total interconnection lengths (resistance). For example, a 0.5 μm polysilicon line crossing a 0.5 μm thick and 0.5 μm wide oxidized silicon island would be much longer in fact than an x, y plane view would indicate. Similarly, the capacitance of such a geometry would be dominated by the normally parasitic edge effects. With a clear picture of the geometry, an accurate calculation and prediction of effects of this type can be made.

Observation of the features of the image as a whole is comparable to that seen by using a good scanning electron microscope (SEM) in that resolution in the 100 Å range is available. The structure in Fig. 10 is seen in exact cross section, however, and the image contrast features are much sharper and are due to the internal rather than the external parts of the sample. For example, distinguishing the channel oxide from the silicon by SEM may require an oxide etching process, so that the topological features (rather than the electron-beam-transmission features) would be different from that of the other parts and would in general require nonstraightforward viewing angles. Even in this case, the resolution and structural information is usually inferior in the SEM case.

Two examples of SEM images obtained on structures similar to that of Fig. 10 without the polysilicon are shown in Fig. 11. Here the channel oxide was removed by etching using a photoresist mask (which was subsequently removed). Figures similar to those of Fig. 11 have been previously published by Lee and Kjar[6] and Ham[7]. We note that the etched oxide profile and the silicon island edge in Fig. 11 are not straight because of the nonideal photoresist exposure and development used to define these edges. It is very difficult to be sure of the structure of the

Fig. 10—Montag
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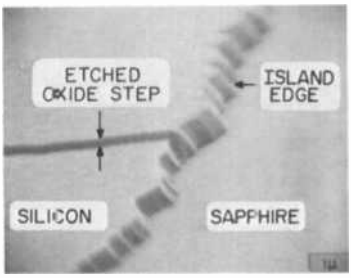
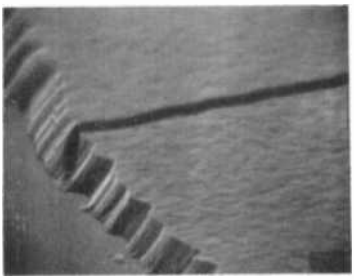
sample near the top or the bottom of the island edge from the SEM images. Cleaving samples to produce some improvement in the viewing angles, which is required frequently, does not allow determination of the structure of the interface regions and very often is destructive to the regions of interest. Moreover, it does not provide the desired detail for the SOS edge regions. On the other hand, a view of a much larger sampling of the wafer can be obtained from the SEM images and this can be very important for interpreting the TEM images. For example, be-



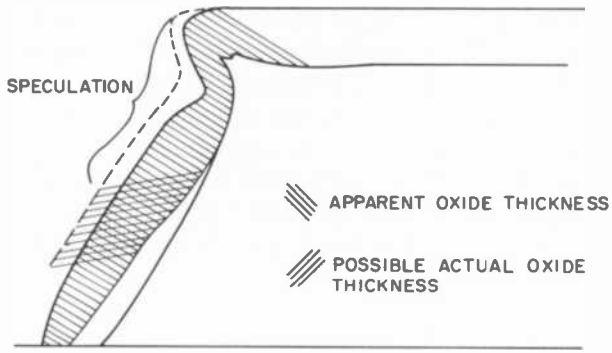
SILICON
≈0.5 μm



SILICON
≈0.75 μm

Fig. 11—SEM images of samples similar to that of Fig. 10. Two different silicon thicknesses are shown with a step etched into the (1100 Å) channel oxide. There is no polysilicon on these samples.

cause of the nonstraight silicon edge, a significant amount of "tilt" (see Fig. 7) might be expected in the silicon oxide interface region on the island edge even though the intersection of this interface with the surface of the TEM cross sectional sample would appear nearly straight. On the top silicon surface shown in Fig. 11, the undulations in the x direction are essentially the same as those in the y direction. In this case, an undulation in the TEM image would relate to the amount of tilt of the interfaces.



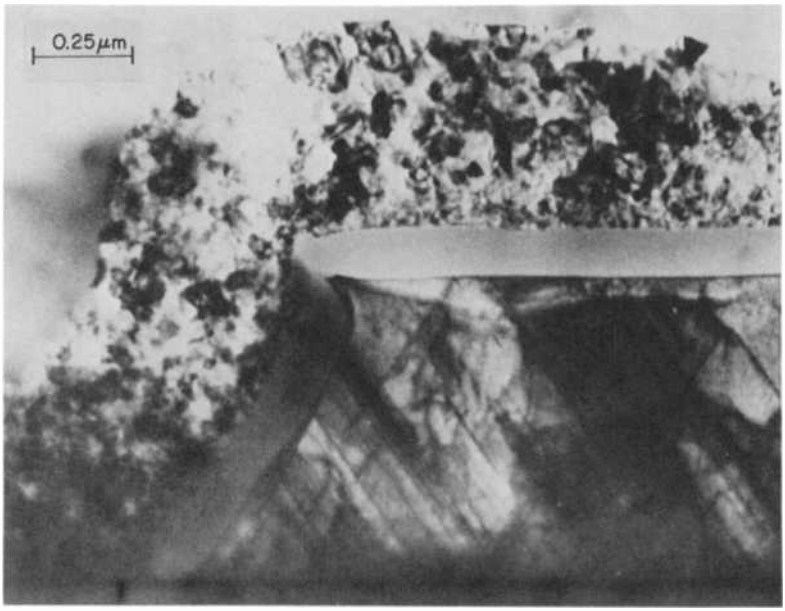
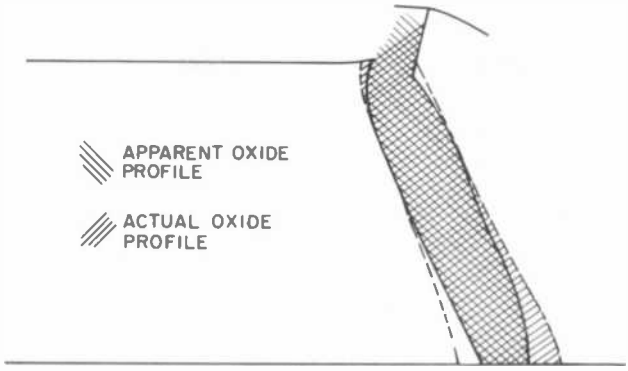


Fig. 12—High magnification XTEM image of the left end of the island shown in Fig. 10.

A magnified view of the left hand side of Fig. 10 is shown in Fig. 12. The right hand side of Fig. 10 is shown in Fig. 13 and an image of a similar edge from another sample is shown in Fig. 14. Fig. 14 shows better contrast near the bottom of the edge region than the other images. In these figures a resolution of perhaps 20 Å exists. A cursory examination of these images reveals that a very complex structure exists on the edges of the silicon islands. Perhaps the most obvious feature of interest is the apparent nonuniformity in the channel-oxide thickness on the edges while



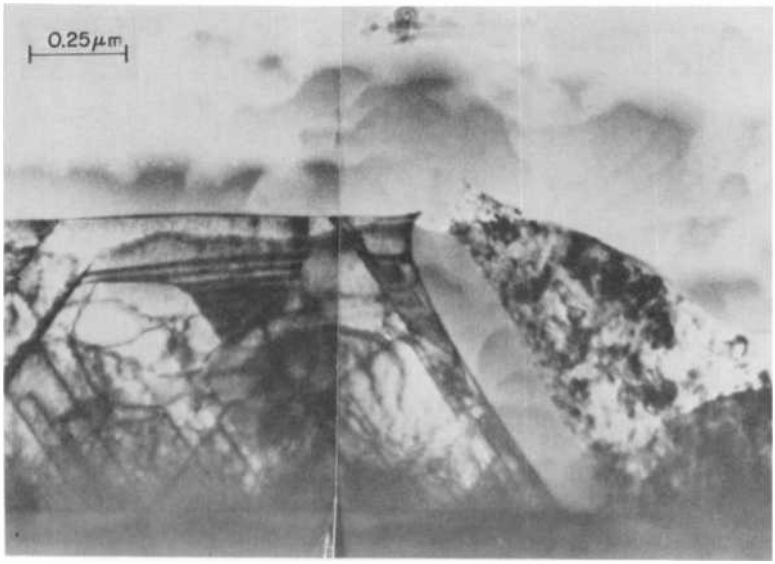
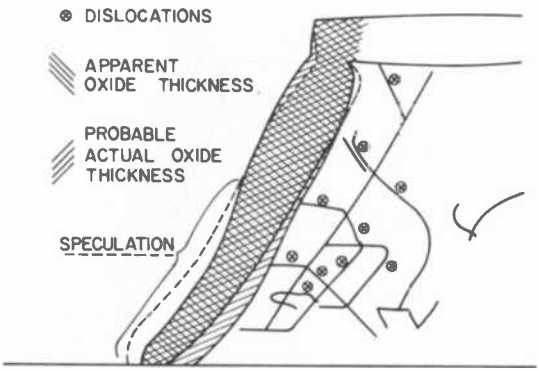


Fig. 13—High magnification XTEM image of the right end of the island shown in Fig. 10.

the thickness is almost constant on the top of the island. Preliminary examination of Figs. 12, 13, and 14 suggests that the edge oxide is preferentially thin near the top of the edge. Cursory inspection of Fig. 12 suggests that the oxide undergoes a very substantial thickness change approximately half way up the edge. Near the bottom it appears that a sharp reduction in the thickness exists. We also note the presence of very sharp silicon corners at the top of the island edge. None of this structure is clear from the SEM samples. On the other hand, some of the apparent structure in the edge oxide is due to an interface tilt phenom-



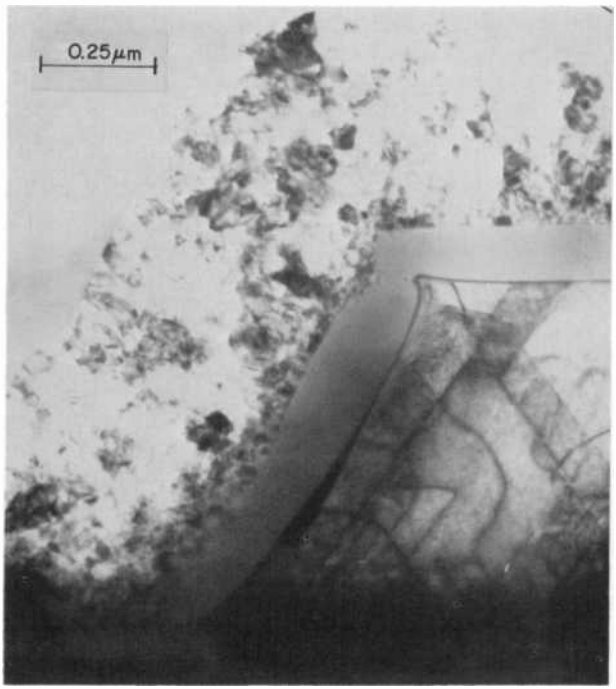


Fig. 14—High magnification XTEM image of an island edge showing dislocations and good contrast at the bottom of the island edge.

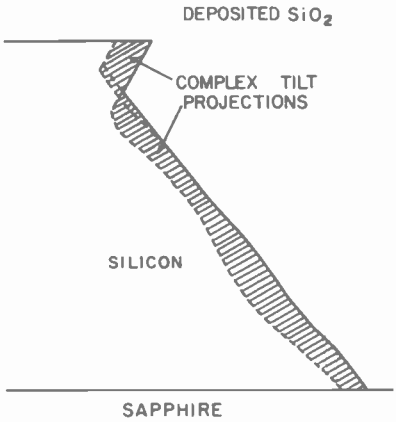
enon. All three highly magnified edge TEM images are seriously affected by different types of tilt as shown in the line drawings on the images. One must conclude after careful study that the oxide on the edge is approximately uniform in thickness except near the top and bottom and is thicker by approximately 20–30% than the oxide on the top. It is very

easy in this case to be misled by the tilted interface. The thin oxide sections near the top of the edge are real but they are not as thin as they first appear.

The phenomenon of interface tilt must be suspected any time one is dealing with a photolithographically defined edge, because the undulations present due to the nonideal photoresist edges cause preferential interface tilt in cross section. It may therefore be *necessary* to obtain high magnification images or purposefully tilted images of these types of region to be able to see the relatively faint contrast differences due to tilted interfaces and to be confident of the actual structure existing. We note that even with 20 Å resolution and optimum viewing angles, the exact structure at the bottom and top of the edge is not absolutely clear. It is, however, much clearer than from previous techniques.

The shape of the silicon edge determines, in part, the shape of the thermal oxide edge. In particular, the sharp point of silicon at the top of the edge deserves comment. The origin of this point is best seen by considering the shape of the silicon before the channel oxidation. A cross section of a typical island edge immediately prior to thermal oxidation is shown in Fig. 15. It is clear that a sharp point exists at the top of the edge. (We note that significant tilt projections are also seen in this figure.) This point is a result of the anisotropic silicon etch used to form the islands which, as stated above, tends to leave {111} planes. The defects (twins) in the silicon are on {111} planes and it is apparent that the slopes of the edges are approximately parallel to the defects. Thermal oxidation of a given volume of silicon produces approximately twice that volume of oxide. Since the oxide thickness is approximately 1000 Å, only approximately 500 Å of silicon was consumed. This is not enough to remove the point. Possible effects of this pointed structure are discussed later.

The oxide structure near the top of the edge is primarily a result of the starting silicon structure. The simplest models of thermal oxidation do not predict the preferential thinning observed immediately below the top of the edge, however, and such regions are not clearly in evidence from the SEM images. The concept of lateral material flow in the oxide during oxidation has been previously suggested for thermal oxidations of regions such as this.[7] For very thick thermal oxides on the island edges, large separations of the oxide from the sapphire have been previously noted[6,7] and a TEM image of such a thick oxide is shown in Fig. 16, in support of this concept. Detailed modeling of this type of oxidation is yet to be done, so the cause of the thin oxide region at the top of the edge is uncertain. We also note that the silicon–oxide interface on the top of the silicon near the edge is bent upwards in Figs. 12, 13, and 14. This is probably caused by differences in net oxidation rates rather than by



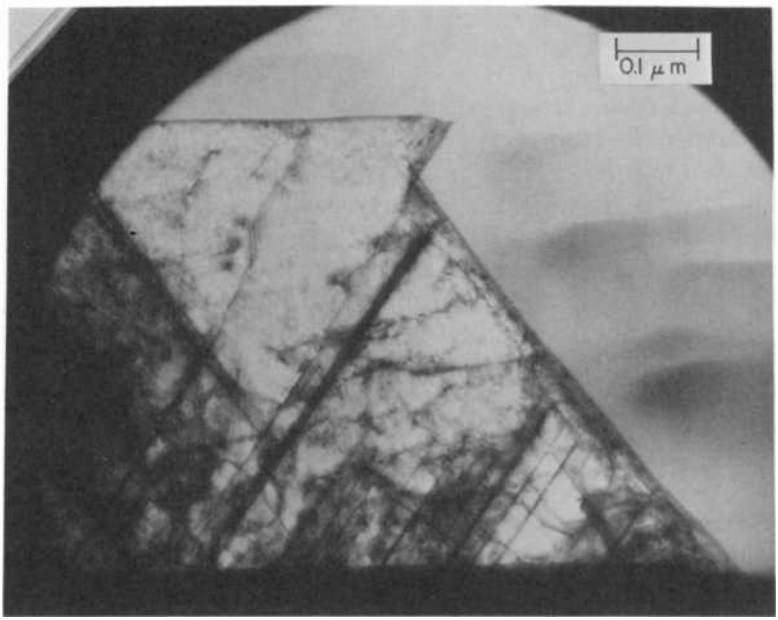


Fig. 15—XTEM image of an island edge after chemical etching.

mechanical bending due to forces in the oxide, since the contrast in the single crystal silicon is relatively uniform in this region. (Mechanical bending would cause large intensity charges as discussed earlier.) Such forces may have been present during growth and subsequently annealed, but they are not large in the sample as it existed during TEM imaging. A conceivable cause for this type of interface profile would be cooler

silicon at the tip (because of preferential thermal losses) during the oxidation.

In any case, the results of the very complicated processes involved for this structure are clearly visible and provide a good foundation from which an accurate model can develop.

The silicon structure near the bottom of the edge of the silicon island with thin channel oxides is also of interest. It is quite clear in Fig. 12, 13, 14, and 15 that the silicon smoothly joins the sapphire both before and

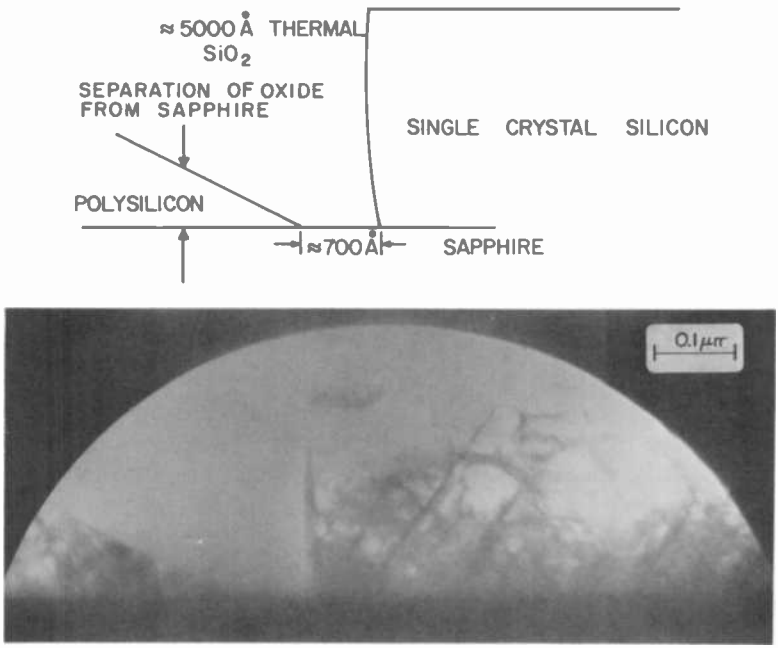


Fig. 16—XTEM image of the bottom of an island edge that has been heavily thermally oxidized. Note that the polysilicon, which was deposited after the oxidation, nearly touches the single-crystal silicon even though the oxide is ~5000 Å thick.

after oxidation. This question has been the subject of some informal debate with one suggestion point being that the silicon at the bottom of the edge is consumed faster than other silicon because of its more highly defected nature and because of its better exposure to the oxidizing ambient. This should cause thicker oxides at the bottom of the edge. Another point of view suggests that the silicon in this region is very highly stressed and should tend to separate from the sapphire under heat treatment or oxidation. It is clear that, for the thermal cycles and times

used for these samples, neither point of view describes the system for thin oxides. Instead, it appears that the oxidation of the bottom of the edge may proceed slightly more slowly than for other parts of the edge. There is no evidence of any separation of the oxide from the sapphire for the thin oxides. On the other hand, thick oxides (Fig. 16) separate from the sapphire after maintaining good contact for ~700 Å from the silicon. The thick oxides are electrically approximately as thick (in terms of dielectric strength) as the thin oxides because the poly is within ~700 Å of the silicon at the bottom of the edge. We also note that a sharp silicon corner remains at the top of the edges but that the retrograde slope has been removed. The slope of the silicon edge has changed markedly due to the nonplanar geometry and resulting nonuniform oxidation rates. These processes are currently under study. It is also clear that all surfaces are intimately in contact with the CVD layers (deposited oxides and polysilicon) everywhere, including on the retrograde slopes.

Another feature of interest in Fig. 10 is the shape of the edge of the polysilicon on the top of the silicon island. Recall that this edge was formed by the etch resistant properties of boron-doped silicon and that the boron was introduced by diffusion from a boron-doped oxide strip that was *not* in place during the poly etching process. It is not immediately clear why the observed edge profile should exist. The "tail" near the oxide is particularly noticeable. Since the boron-doped oxide was not in place during the etch, the only factors influencing the etch rate of the poly are those due to the boron content. If one assumes, for simplicity, that a boron concentration exists such that no etching takes place for boron levels above this concentration and that the etching proceeds at approximately the same rate as undoped silicon below this concentration, then the shape of the poly edge should be approximately the same as that of the locus of the critical concentration in the poly. One would not expect the profile observed in the poly from classical diffusion theory. A profile similar to that shown in Fig. 17A would be expected; the profile shown in Figure 17B is that obtained. The critical boron concentration exists farther from the doped-oxide edge at the bottom of the poly than at the top. The cause for this is uncertain, but it may be related to nonuniform diffusion coefficients in the poly.

Other relatively coarse features of Fig. 10 include the nonuniformity experienced in the ion thinning, particularly in the deposited oxide. It is sufficient to cause obvious intensity changes over relatively small areas. This suggests that any method that uses ion thinning as the basis for a profile by measuring the properties of the surface left (such as by Auger methods) or by analyzing the properties of the material removed (such as SIMS) may suffer considerable loss of depth resolution that will not be apparent in the data.

To this point, we have mostly discussed the information content of the images that is relevant to the mechanical properties of the structure. The relationships of the position of the various interfaces to each other have been only briefly discussed. Information is also available concerning the structure of the interfaces and materials present. In general, there is no evidence that any interface between any of the materials is other than completely abrupt to within the resolution and limitations of this method. Any transition regions that exist are not sufficient to cause intensity changes in the images. On the other hand, many structural features of the single-crystal silicon and the poly can be seen.

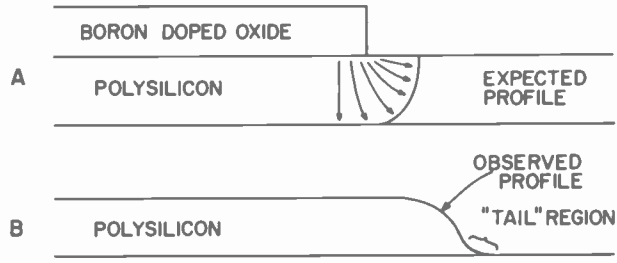


Fig. 17—Anomalous edge profile in polycrystalline silicon possibly caused by nonuniform diffusion of boron due to the grain size distribution in the poly.

The poly shows no evidence for being other than composed of random crystallites. A definite pattern in the distribution of the crystallite sizes was noted however. The grains found near the thermal oxide are sometimes smaller than those in the upper portion of the film. This can be seen in Fig. 10 in the poly on the top of the island. (Other TEM images not shown here have shown the presence of small grains near the oxide even more clearly.) Since the poly near the oxide can have very small grains it may be composed largely of grain boundaries. This poly therefore may not have the same properties (such as boron solubility limits and diffusion coefficients) that would be experienced in single-crystal silicon or in the upper portion of the poly film. The small grains may also provide a possible site for electrical charge trapping in the poly with resulting electrical instability. This type of instability could proceed rapidly at room temperature and appear as a dielectric charge in MOS structures using poly silicon as the gate metal. The very small grained poly might behave as poor dielectric since it is difficult to make small grained poly conductive. Alternatively one might suspect a high boron concentration near the poly oxide interface instead of the relatively low levels normally expected. Such boron concentrations could have major consequences on the injection of charge into the oxide and thus be a re-

liability concern. One might expect a high degree of sensitivity of these effects to the grain structure and thickness of the poly. Other poly films that have been examined do not show the preferential distribution of crystallite sizes. Such examples are shown later in this paper. Thus a mechanism exists that can cause small grains near the oxide in polycrystalline silicon but that does not always persist even throughout the extent of a single sample. A mechanism such as nonuniform surface cleanliness might be suspected. The fact that the poly shows no evidence of columnar growth may be of interest.

The single-crystal silicon is literally "loaded" with structure. Examples of microtwins and dislocations are shown in Fig. 10 along with other features, such as "bent sample" contrast. It is quite clear that this silicon is highly defected, especially in the region near the sapphire. Models of electrical conduction processes in this material must therefore be used with the knowledge that the material is highly imperfect and the traditional models may not apply. Detailed discussions of some of the effects of these defects can be found elsewhere.[8,9]

It is particularly interesting to note the behavior of the defects in the silicon near the edges of the islands. Upon initial examination of Fig. 12, 13, 14 and 15, one can see that no very large perturbation in the defect type or density is present near the edges compared to the regions of the films more remote from the edges. It is also seen, however, that the different edge regions of the various samples have very different densities of defects intersecting the edge regions. This difference is a result of the nonuniform distribution of defects throughout the x and y dimensions of the film, as can be readily seen by examination of Fig. 10. The electrical behavior of the edge regions has been observed to be highly nonideal[10] and can be erratic in some cases, even between "identical" devices on the same region of the same wafer. Other cases have been noted where relatively smooth changes in the edge properties exist between adjacent devices. This behavior could, in principle, be explained by the different defect densities intersecting the silicon oxide interface on the island edge. It must be recognized, however, that the TEM samples are only a few thousand angstroms thick at most and that it would require at least 10–50 times this thickness to represent a typical source-to-drain spacing. Therefore it is very difficult to be sure of the number of defects intersecting the edge region throughout the entire electrically active edge region of a typical device. It is clearly possible and likely that the number of defects intersecting the edge interface is substantially greater than those intersecting the top silicon–oxide interface. These defects could cause preferential generation of surface states, potential barriers, or scattering centers, and may have first order effects on the electrical properties of the edges.

In addition to the most populous planar defects that intersect the edge silicon–oxide interface, another class of defect is commonly seen near the edges. These are dislocations probably produced by processing the wafers at high temperatures. Examples of these can be seen clearly in Fig. 14. Many of these dislocations intersect the silicon–oxide interface on the island edge. In this particular sample, their density is $\sim 4 \times 10^9/cm^{-2}$ of interface area if the sample is assumed to be 3000 Å thick. The curvature of the dislocation lines indicates that they have been generated from the lower left corner of the island, although their precise source is not clearly evident. Once generated, these dislocations glide under the influence of the shear stress present at or near the edges of SOS films.[11] These shear stresses develop upon relaxation of the normal strains occurring because of differential thermal contraction or expansion. This is a general phenomenon expected to occur, for example, in most semiconductor composites and semiconductor–oxide systems.

It is of further interest that neither the nature nor the density of the planar defects present are substantially altered by the processes used to form the sample of Fig. 10, 12, 13, or 14. (For these samples the silicon was deposited at ~950°C and the samples were heated to 900°C for channel oxidation and to 1050°C for poly diffusion.) Fig. 15 shows the preprocessing silicon structure.

The reader may have noticed that the channel oxide does not exhibit any visible interface at all with the deposited oxide. This is the only example of any interface between two amorphous materials in Fig. 10. One would not necessarily expect to see this interface by TEM since the materials are chemically and structurally very much the same. It is important, however, to demonstrate that interfaces between amorphous materials can be readily seen by TEM if they *are* different. To this end and to demonstrate at the same time the ability to clearly see layers in the 10 Å thickness range, TEM images from another sample are shown in Figs. 18 and 19. This sample also shows the structure of a silicon island edge prepared by an oxide isolation method. It will be seen that this structure is entirely different from that of the chemically etched edges shown in Fig. 10.

The sample was prepared by first growing a channel oxide in steam to a thickness of ~700 Å on a SOS wafer with a 0.6 μm silicon layer. A thin layer of amorphous Si_3N_4 was then deposited and defined into strips ~5 μm wide. At this point, the channel oxide was etched using the nitride as the etch mask. This process left the wafer with strips of Si_3N_4 over channel oxide separated by regions of bare silicon. The silicon was etched with the same potassium hydroxide etch used to form the islands shown in Fig. 10 but for a reduced time, such that ~2000 Å of silicon remained in the regions between the nitride. The wafer was then placed in a 900°C

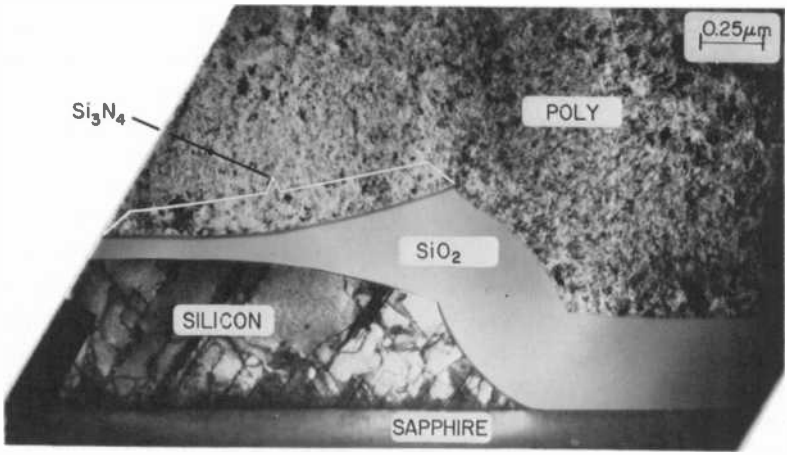


Fig. 18—XTEM image of the edge of an oxide isolated SOS island (see text).

steam furnace for a time sufficient to grow ~6000 Å of SiO_2 on bulk silicon. This schedule was intended to ensure that all of the silicon between the nitride regions was consumed and thus was somewhat longer than necessary. (The nitride acts as a barrier to oxidation of silicon.) A thick layer of polycrystalline silicon was then deposited so that the shape of the oxide and nitride surfaces would be clearly visible.

An image of the region near the edges of the nitride strips is shown in Fig. 18 and a complete island is shown in Fig. 19. It is clear that gross structural changes exist compared with the chemically etched edge. The oxide nearest the silicon edge is the thickest and is noticeably bowed outward. This is probably a result of the oxidation in this region continuing after the thin silicon was consumed. A sharp corner exists as the

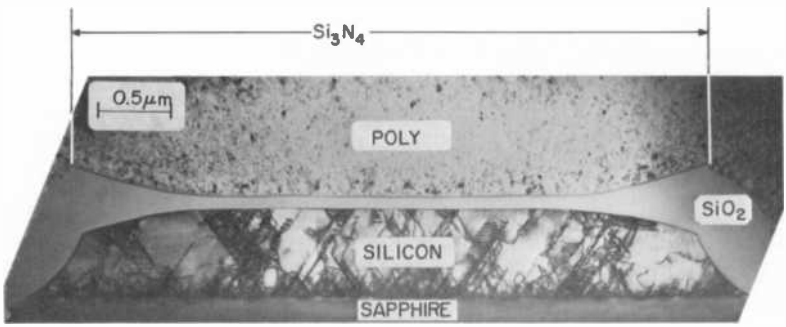


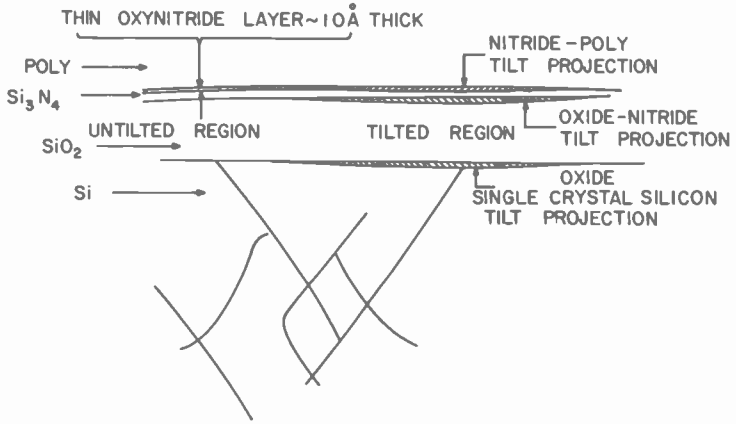
Fig. 19—Entire island from the same sample as shown in Fig. 18 (see text).

oxide approaches the edge region and again near the edge of the nitride. Very significant oxidation has occurred on the silicon under the Si_3N_4 as well as on the edge region. This oxidation has dramatically lifted the nitride above its original plane and has caused the top silicon edge to curve downward for ~1 μm from the edge of the Si_3N_4. The retrograde slope in the silicon on the edge shown in Fig. 14 has been removed and there is certainly no evidence for preferential thinning of the edge oxide. (We again note a small tilt projection on the most vertical part of the silicon edge.) The profile of the edge silicon is gradually curved and smoothly intersects the sapphire surface. Sufficient detail clearly exists to allow detailed accurate modeling of the oxidation mechanism for this type of system and such work is in progress. We also note a large intensity difference in the silicon near the edge in Fig. 18 as compared to away from the edge. This could be evidence for preferential edge forces and resulting sample bending, but microdiffraction studies would have to be performed to substantiate this contention. The image of the entire island shown in Fig. 19 does not show any consistent contrast changes near the edges and is a very good example of the value of having more than one example of the structure of interest available on the same sample.

This particular method of forming the islands produces a channel oxide thickness that gradually increases as one proceeds from the center of the island toward the edge. Any electrical effects that might be associated with the silicon on the edge would require that more potential on the gate be used. The edge region is, in a sense, gradually isolated from the main body of the device. It is clear that the island width cannot be arbitrarily reduced without serious effects occurring near the center of the island.

The Si_3N_4 appears as a dark band immediately above the oxide in Figs. 18 and 19; it is sharply visible and distinct from the oxide. A high magnification image of the region where the oxide is just beginning to thicken is shown in Fig. 20. This image shows even more clearly that the nitride layer is visible and, further that a layer exists on top of the Si_3N_4 whose thickness is approximately 10 Å. This seems to violate the claimed resolution limit of 10 Å. However, when a well-defined interface exists over extended regions, it is possible to obtain from the original plate a resolution somewhat better than 10 Å as shown, for example, in Ref. [12]. This resolution is normally lost during photographic processing and no attempt is made here to show a high resolution image. For such resolution, a region must be found where no tilt exists. This is done by carefully examining several areas for the minimum size and, if necessary, replacing the sample in the microscope for tilting experiments.

This thin layer on the nitride has been previously suggested[13] but not previously directly observed and is almost certainly caused by the ex-



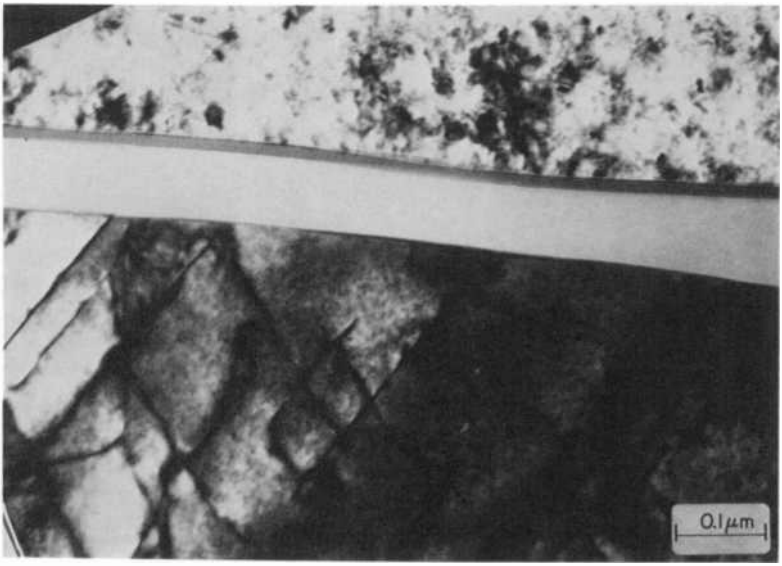


Fig. 20—High magnification XTEM image of the channel oxide region of the sample shown in Fig. 18.

posure of this surface to the oxidizing ambient during the island formation. Its presence or absence can have first-order effects on the transport of charge through the nitride layer and thereby on the stability of any MOS device incorporating a nitride in its gate dielectric. We note that it is difficult to see this thin layer in regions where the interface is tilted.

Every example shown in this paper is relevant to matters of practical importance. The shapes of the oxides on the edge of the islands are of first-order importance to the dielectric behavior of the channel oxide of practical MOS transistors. Unpublished data acquired at RCA Laboratories has shown that arbitrarily increasing the thickness of the channel oxide on the SOS edge does not continue to increase the dielectric strength. This is directly explained and predicted by the phenomenon shown in Fig. 16. This explanation does not appear to hold for thin oxides. For these thin oxides, which usually exhibit inferior dielectric strength properties, there are two points of weakness. Even though the oxide at the bottom of the edge is not appreciably thinner than the other oxides, it is present as an oxide surface contacted on one side by polysilicon and on the other side by single-crystal silicon. This structure has been shown to be prone to anomalous surface conduction effects[14] which, therefore, may be the cause of failure for some samples. The other point of weakness exists at the top of the island edge where thinner oxides are seen. Probably even more important than the thin oxides is the sharp silicon point. As the potential between the gate metal and the silicon is increased, the electric field will tend to concentrate at the silicon tip, thereby causing very high densities of surface charge in the silicon. These high densities of charge and high fields can cause locally enhanced injection of charge into the oxide with resulting lower dielectric breakdown potentials. A mechanism similar to this has been suggested by Kerr[15] for conduction in thermal oxide grown on polycrystalline silicon. Therefore, for a system of this type the dielectric strength may be determined by the unlikely process of silicon etching rather than by the more traditional processes of oxide growth or metallization. Transistors with edge-oxide profiles similar to those shown in Fig. 18 and 19 do not have inferior dielectric properties of the oxides on the edges of the islands.

We have shown here three cases where the TEM examination of structures found in typical integrated circuits has provided key information needed to understand electrical behavior that had previously been difficult to determine. These are:

(1) Determination of the detailed structure of the edge regions of silicon on sapphire islands. This includes phenomena related to the oxide profiles and to the possible effects of silicon defects on the silicon–oxide interface.

(2) Observation of a small crystallite region of the poly near the oxide. This region may be important in determining the diffusion properties of the poly. The poly structure can also provide a possible explanation for rapid room-temperature instabilities sometimes seen in boron-doped polysilicon MOS structures.

(3) The direct observation of a thin layer on the surface of Si_3N_4. This layer can be very important in the vertical transport of charge through Si_3N_4 layers and was found to be thinner in the actual structure than had been suspected from previous work.[13]

5. Discussion and Conclusions

We have discussed in this paper most of the features of sample preparation and of the TEM images that must be considered to obtain an accurate impression of the microphysical properties of microcircuits using cross sectional transmission-electron-microscope methods. It should be quite clear that these methods are not at present well suited to fast-turn-around applications. Routine use for specific failure analysis will require innovation in the methods of obtaining suitable samples. It is possible that the current process could be developed into a semi-production method. On the other hand, as demonstrated in Sec. 4, some of the most important physical features of the microcircuit structures cannot be seen with conventional methods and may require TEM examination. The decision whether or not to use TEM methods depends on the type of information sought. TEM is best suited for applications where examination of a specific local region of a wafer is not necessary and is particularly powerful for determining the internal structure of microcircuits without microphysical disruption. Many of the most important phenomena associated with microcircuits exist within the parts of the device that cannot be seen from surface features. We have shown in Sec. 4 that complex structural features of internal parts of microcircuit devices can be seen with very good resolution (<10 Å if needed).

Even in the case where large differences in hardness exist between the various constituents of the device, such as silicon, sapphire, or silicon nitride, the ion thinning rate is usually sufficently uniform in the narrow surface region of interest to allow simultaneous electron transmission through each constituent in this region. In fact the ion thinning ridges shown in Fig. 10 do not show discontinuity across material boundaries and strongly suggest that the *effective* thinning rate must be nearly identical for all materials in this region. This conclusion can also be arrived at by considering the thickness ratio of the samples before and after ion thinning. If any appreciable thinning-rate differences exist, one would certainly expect that they would be visible in the 1000–3000 Å layer left from the 250,000 Å starting thickness. The possibility of small thickness differences cannot be entirely ruled out, however, because local enhancement or retardation of the thinning rate of a given layer by adjacent layers may exist due to a low angle of incidence of the thinning

argon ions (15° from the sample plane). This will cause a shadowing effect. Therefore, harder layers must be removed before the ion beam can reach the softer layers behind them. This is probably the main reason that the observed degree of uniformity exists. In general, one would expect that the thickness of a given layer (in the electron beam direction) in a multilayer structure would not be more different from the thickness of neighboring layers than it would be from its own thickness in the growth direction.

There is invariably a question of the damage introduced to the samples by the ion thinning process. We can state with confidence that the methods used by the authors for ion thinning do not introduce any noticeable damage to the samples. This is demonstrated by relatively large areas of defect-free silicon seen in Fig. 10 and by the fact that very large areas of bulk single-crystal silicon prepared by this method (on other samples not included in this paper) do not show any evidence of structural damage. It is known that argon ion thinning can introduce very shallow surface damage in some cases. This damage is not revealed by the imaging techniques used in this paper and does not affect the observed features. The low-angle ion thinning method is a gentle way to remove excess material.

Among the methods used for obtaining microphysical information from microcircuits, only the cross-sectional-scanning electron-microscope method is close to cross sectional TEM methods in the total information content of the images. In the cross-sectional SEM case, the sample may be tilted to allow a perspective view of much more of the sample. This feature may be important for some applications. The image is determined entirely by the exposed surface properties of the sample and it is possible that an etching process may be needed to allow certain layers to become visible. The TEM method on the other hand allows unambiguous determination of the location of all interfaces between different materials and observation of the subsurface (intrasample) structure, but with reduced volume of sample available (compared to SEM) for examination. The resolution available with the TEM is at least 20–100 times better. A complete characterization of a sample will require both. (The SEM images of Fig. 11 are partial-cross-section images.)

We have also seen that interpretation of the TEM images is far from trivial in some cases because of the sensitivity of the transmitted intensity to properties of the sample that are not important in determining optical images. Thus careful study and examination of multiple samples may be required before concluding a cause of TEM contrast. Two of the most important anomalous (to untrained microscopists) effects are the "bent sample" contrast, which arises because of the sensitivity of electron diffraction to very small angular changes, and the "tilt projection" ef-

fects, which arise because of undulations within the sample. These can both cause severe misinterpretation if they are not understood.

We have demonstrated in this paper the ability to observe layers as thin as 10 Å and interfaces between the following materials with a resolution of <10 Å:

(1) Single-crystal silicon/Single-crystal sapphire
(2) Polycrystalline silicon/Single-crystal sapphire
(3) Thermal SiO_2/Single-crystal sapphire
(4) Thermal SiO_2/Single-crystalline silicon
(5) Thermal SiO_2/Polycrystalline silicon
(6) Thermal SiO_2/Silicon nitride
(7) Deposited SiO_2/Polycrystalline silicon

Many other interfaces can also be readily seen by TEM. The only interface the authors have found impossible to detect is the thermal SiO_2/deposited SiO_2 interface. These materials are too similar to produce contrast. Very good qualitative agreement with the simple absorption model for amorphous materials was found for the tilted interface between SiO_2 and Si_3N_4.

Acknowledgments

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References:

[1] M. S. Abrahams and C. J. Buiocchi, "Cross Sectional Specimens for Transmission Electron Microscopy," *J. Appl. Phys.*, 45 p. 3315, 1974.

[2] T. T. Sheng and C. C. Chang, "Transmission Electron Microscopy of Cross Sections of Large Scale Integrated Circuits," *IEEE Trans. Electron. Div.*, EP023, p. 531, 1976.

[3] R. D. Heidenreich, *Fundamentals of Transmission Electron Microscopy*, Interscience, New York, 1964.

[4] S. Amelinckx, *The Direct Observation of Dislocations*, Academic Press, New York, 1964.

[5] P. B. Hirsch, A. Howie, R. B. Nicholson, D. W. Pashley, and M. J. Whelan, *Electron Microscopy of Thin Crystals*, Butterworths, Washington, 1965.

[6] S. N. Lee and R. A. Kjar, "SOS Island Edge Profiles Following Oxidation," *Proc. IEEE Reliability Physics Symp.*, Las Vegas, p. 34, 1975.

[7] W. E. Ham, "High Speed Complementary Metal-Oxide Semiconductor/Silicon-on-Sapphire Development," Final Report Phase II, Contract No. N00014-73-C-0090, Office of Naval Research, 1975.

[8] W. E. Ham, "The Measurement and Interpretation of the Electrical Properties of SOS," *Electrochem. Soc. Extended Abstracts*, 76-2, Abstract No. 172, 1976.

[9] W. E. Ham, "The Electrical Characterization of Heteroepitaxial Semiconducting Films," in *Heteroepitaxial Semiconductors for Electronic Devices*, G. W. Cullen and C. C. Wang, Editors, Springer-Verlag, in press.

[10] D. W. Flatley and W. E. Ham, "Electrical Instabilities in SOS/MOS Transistors," *Electrochem. Soc. Extended Abstracts*, **74-2**, Abstract No. 198, 1974.

[11] M. S. Abrahams, J. Blanc, C. J. Buiocchi, and W. E. Ham, "Shear Strain Near Edges in Epitaxial Silicon on Sapphire," to be published in *J. Appl. Phys.* (1978).

[12] J. Blanc, C. J. Buiocchi, M. S. Abrahams and W. E. Ham, "The Si/SiO_2 Interface Examined by Cross Sectional Transmission Electron Microscopy," *Appl. Phys. Lett.*, **30**, p. 120, 1977.

[13] S. A. Abbas, C. A. Barile, and R. C. Dockerty, "Low-Leakage N-Channel Silicon Gate FET with a Self Aligned Field Shield," *Technical Digest International Electron Devices Meeting*, Abstract No. 18.5, P. 371, Wash., D.C. 1973.

[14] W. E. Ham and S. S. Eaton, "Anomalous Electrical Gate Conduction in Self-Aligned MOS Structures," *Technical Digest International Electron Devices Meeting*, Abstract No. 14.2, p. 323, Wash., D.C. 1976.

[15] D. R. Kerr, "Mechanism of Conduction in Oxide Grown on Polycrystalline Silicon," *Electrochem. Soc. Extended Abstracts*, **76-2**, Abstract No. 326, 1976.

Low-Resistance All-Epitaxial PIN Diodes for Ultra-High-Frequency Applications

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Abstract—Low resistance p-i-n diodes for low-power switching applications have been developed using an all-epitaxially-grown structure. With 1 pF diodes, a series resistance of less than 0.2 ohm was achieved at a forward-bias current level of only 10 mA. A reverse-bias voltage of only 10 to 15 volts is needed to deplete the diodes. The fabrication method as well as the performance tradeoffs of these p-i-n diodes are described.

1. Introduction

PIN diodes are used in numerous switching applications from very low frequencies into the microwave range.[1] The various circuit applications place different specifications on the diode capacitance, avalanche breakdown voltage, and sometimes the thermal resistance of the diode. These specific requirements coupled with the forward current and reverse-bias potential needed to operate the p-i-n diode constitute the constraints under which the design of the diode is finalized. This paper describes the structure of an all-epitaxial p-i-n diode and its performance, together with considerations of trade-offs between design and operating parameters for low-power switching applications.

The merit of a p-i-n diode is almost exclusively expressed in terms of the series resistance at a specific current level. This series resistance can be divided into two parts: the part due to the I layer, which is highly sensitive to current level, and the part due to the p^+ and n^+ layers and the two metal–semiconductor contacts, which is essentially independent

of current level. Since the metal–semiconductor resistance, which is independent of current density,[2] is ever present, it is extremely important to construct very low resistance ohmic contacts to silicon and to measure the resistance very accurately. Accurate measurements of contact resistance of metal–silicon systems under reverse-bias conditions have been reported previously.[3] The evaluation of the contact resistance in the forward-bias direction will be described. A considerable amount of work was concentrated on developing and evaluating various metal systems for constructing ohmic and very-low-resistance metal–silicon contacts readily and reproducibly. A scheme of gold-chromium-palladium silicide-silicon constructed through vacuum evaporation and low-temperature (250°C) annealing was found to give an excellent metal–silicon contact for both the reverse- and the forward-bias conditions.

In fabricating silicon p-i-n diodes, three alternative approaches are apparent: first, the all-epitaxially-grown structure scheme; second, the conventional and most used method involving an epitaxial layer and a bulk p^+ or n^+ substrate; and third, the double diffusion (such as the planar p^+ and n^+ diffused diode) of a bulk high-resistivity π or ν substrate approach. The last approach is not particularly suitable for low-power switching applications and, therefore, has not been examined experimentally. For convenience of description and with justification becoming clear later, we shall refer to the all-epitaxy approach as the thin-epitaxy method and the second approach as the thick-substrate method. Both approaches have been carried out experimentally and the performance of the resulting p-i-n diodes evaluated. Discussions on the desirability of these approachs will be made with respect to the diode performance and the ease of fabrication.

2. Diode Fabrication

2.1 Thin Epitaxy Method

A multi-layer p^+in^+ junction, shown in Fig. 1, is first grown epitaxially on a low-resistivity, (100) oriented, antimony-doped silicon wafer using the conventional silane pyrolysis in hydrogen. The 5 μm thick p^+ contact layer is first grown on the n^+ substrate at a temperature of 1100°C and doped to a resistivity equal to or less than 0.001 ohm-cm with diborane. The undoped I layer of a particular thickness l, typically from 1 to 15 μm, is then grown on top of the p^+ layer. A thin n^+ layer (usually 1 μm thick), is finally grown on top of the I layer with phosphorus and/or phosphorus-arsenic doping to a resistivity of 0.0015 ohm-cm. Then a metal–silicon ohmic contact to the n^+ layer is formed by evaporating

palladium, annealing at 250°C to form a 1000 Å palladium silicide layer, followed by a standard evaporation of chromium-gold. A 60 to 70 μm thick copper heat sink is electroplated onto the gold and covered by a very thin gold protective layer via electroplating. The n^+ (100) oriented substrate is then completely removed with the KOH-H_2O-n-propanol selective etch[4] and left with the epitaxially grown p^+ layer. The p^+ layer is next vacuum deposited with the palladium silicide-chromium-gold metallization in an identical fashion to that described above. Through standard photolithographic techniques, gold contact hemispheres with the diameter needed to achieve the desired diode capacitance and a

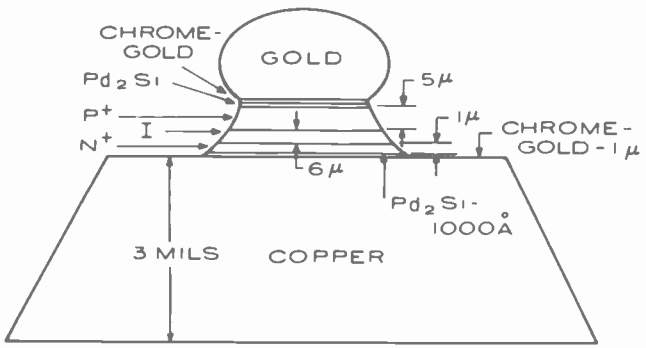

Fig. 1—Detail schematic drawing of a gold-chromium-palladium silicide contacted all-epitaxially-grown p-i-n diode chip.

height of 15 μm are formed on the p^+ side of the wafer. Inverted silicon p-i-n mesa diodes are then chemically etched to result in thousands of diodes on a 60 to 70 μm thick copper heat sink with the finished structure shown in Fig. 1. Diodes can then be separated either by cutting with appropriate tools or by chemical etching coupled with photolithography.

2.2 Thick Substrate Method

The (100) oriented p^+ substrate (0.006 ohm-cm resistivity, boron doped) and the (111) oriented p^+ substrate (0.004 ohm-cm resistivity, boron doped) both have been experimented with as the starting material. An epitaxial I layer of a thickness l is first grown on the p^+ substrate followed by an n^+ layer ($\approx$1 μm thick) at a resistivity of 0.0015 ohm-cm (phosphorus and arsenic doped) to complete the p^+in^+ structure. The layers are grown at a temperature of 1100°C using silane pyrolysis in hydrogen. The same palladium silicide-chromium-gold metallization as described

for the thin epitaxy method is then applied to the n^+ epitaxial layer. The p^+ substrate is thinned by chemical etching to a desired thickness. Then the same palladium silicide-chromium-gold metallization is made on top of the p^+ substrate, followed by electroplating gold and/or copper. Gold contact hemispheres are formed on top of the n^+ epitaxial layer via standard photolithography and electroplating techniques. Silicon p-i-n mesa diodes are defined in a manner similar to that outlined in the previous section, except that only a small fraction of the total thickness of the p^+ substrate is etched to form the mesa diode. The diode chips are separated by scribbing and cleaving like most silicon bulk devices.

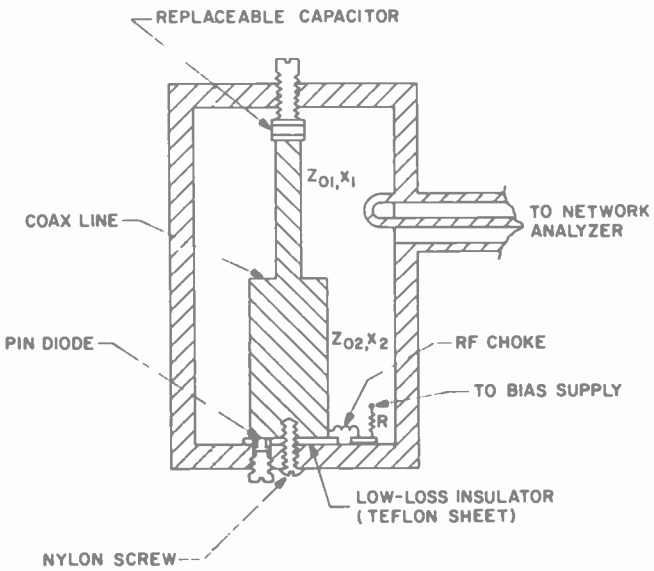

Fig. 2—Microwave cavity for forward-biased resistance measurements of diodes.

3. Packaging, Assembly, and Performance Evaluation

The p-i-n diodes (or diode chips) which we measured were mounted individually using soft solder into an alumina pill-type package. The performance of the p-i-n diodes were evaluated in a resonant-cavity at ultra-high frequencies (500 to 1000 MHz) using these packaged diodes. The reverse-biased diode measurement procedures have been described in an earlier paper;[3] we will concentrate here on the resistance measurement when the diode is forward biased. The coaxial microwave cavity used is shown in Fig. 2. With the diode replaced by a short, a reference

unloaded Q_0 of the cavity including the fixed capacitor is measured using a network analyzer reflection unit. The exact value of the capacitor C (including fringe capacitance) can be determined by knowing the resonant frequency F along with the characteristic impedance Z_0 and length x of the coaxial line sections. The capacitance is given by

$$C = \frac{1 - \frac{Z_{02}}{Z_{01}} \tan\beta x_2 \tan\beta x_1}{2\pi F(Z_{01} \tan\beta x_1 + Z_{02} \tan\beta x_2)} \quad [1]$$

where Z_{01}, Z_{02}, x_1, x_2 are the characteristic impedances and lengths of transmission lines shown in Fig. 2. To get the resistance of the packaged diode, the measured Q_m and resonant frequency of the diode-loaded cavity is used in the following equation:

$$R_P = \frac{1}{2\pi FC}\left(\frac{1}{Q_m} - \frac{1}{Q_0}\right). \quad [2]$$

The resistance of the pill-type package itself is determined by substituting a ball of gold for the diode chip and connecting it to the rim of the package in the same way (e.g., with a strap or bond wires). By subtracting out this package resistance R_{pk} from that obtained with the packaged p-i-n diode, we can determine the series resistance R_s of the diode chip itself.

4 Performance Analysis and Experimental Results

This section describes the characteristics of various metal–silicon contacts, the theoretical and experimental behavior of the diode's forward-bias resistance, and various performance trade-offs of PIN diodes.

4.1 Metal–Silicon Contact

A. Evaluation of Various Metal Systems

A metal–silicon contact of Au-Cr-Si has excellent properties under reverse-bias conditions, but behaves anomalously under forward-bias to prohibit its usage as an effective contact. For example, a minimum in the plot of series resistance versus bias current was observed as illustrated in Fig. 3. Au-Ti-Si in the particular scheme used for fabricating our diodes has very high metal–silicon contact resistance;[3] thus, it also is eliminated from usage. The gold-chromium-palladium silicide contacted p-i-n diode behaves normally as is evident in Fig. 4, which shows

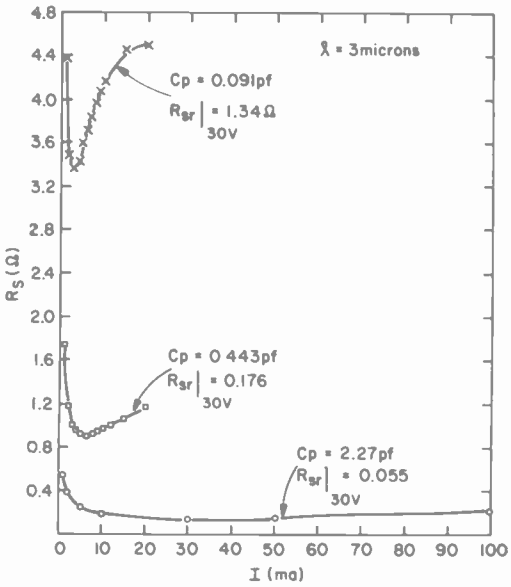

Fig. 3—Series resistance versus forward-bias current of gold-chromium contacted p-i-n diodes (I-layer thickness = 3 μm).

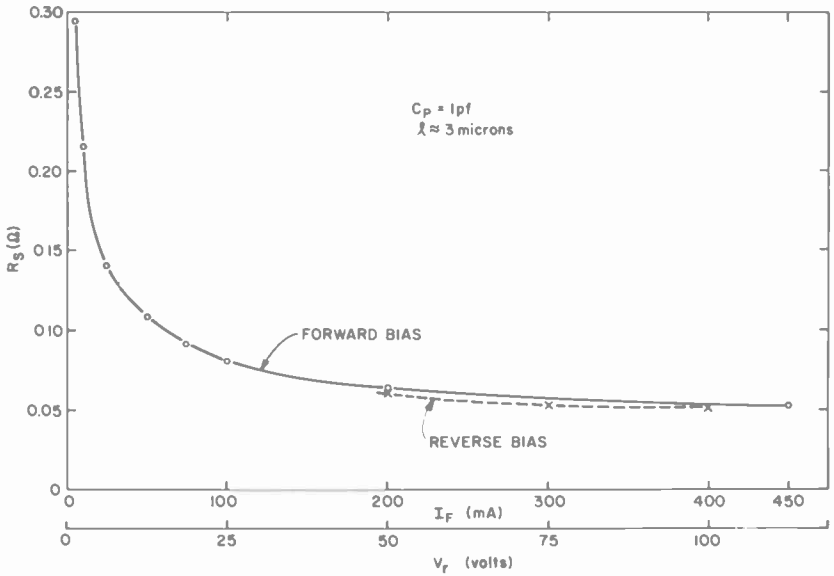

Fig. 4—Series resistance versus forward-bias current and reverse-bias voltage for a 1 pF gold-chromium-palladium silicide contacted p-i-n diode (I-layer thickness = 3 μm).

results for a diode made via the thin epitaxy method. The series resistance of the same diode at depletion under reverse-bias is also shown in Fig. 4. The forward-bias resistance gradually approaches the series resistance of the depleted diode measured under high reverse bias with increasing forward current, and finally merges into it at very high forward current. Thus, the limiting value of the resistance for both the forward- and reverse-biased conditions is the total equivalent contact resistance R_c. From the equation

$$R_c = \frac{\bar{\rho}_c}{A}, \qquad [3]$$

the total equivalent specific contact resistance $\bar{\rho}_c$ can be calculated, where A is the area of the diode. The parameters R_c and $\bar{\rho}_c$ are discussed further in Section 4.2.

B. Effect of n^+ Layer Doping on Forward-Bias Resistance R_s

It has been reported that the specific contact resistance between the metal and the n^+ silicon layer is very sensitive to the resistivity of the n^+ layer as measured under reverse-biased conditions.[3] A similar trend was observed with forward-bias resistance for the Au-Cr contacted p-i-n diodes, as shown in Fig. 5. No systematic investigations were undertaken for Au-Cr-Pd_2Si contacted diodes, since the n^+ layer with lowest possible resistivity was always used to optimize the performance. Phosphorus and phosphorus-plus-arsenic doped n^+ layers, both having a resistivity of 0.0015 ohm-cm, have been used in fabricating certain diodes with otherwise identical procedures. There seems to be a slight improvement in performance with the additional arsenic doping.

4.2 Mathematical Model of Forward-Bias Resistance

The series resistance R_s of a p-i-n diode under forward bias can be written as

$$R_s = R_i + R_c \qquad [4]$$

where

R_i = the resistance of the I region of the p-i-n diode;
R_c = the resistance of the n^+,p^+ layers and the two metal–semiconductor contacts = total equivalent contact resistance.

R_i under dc forward bias is given as[5]

$$R_i = \frac{l^2}{I\tau(\mu_e + \mu_h)}, \qquad [5]$$

where

l = thickness of I region;
τ = lifetime of electrical carriers in the I-region;
I = dc forward current
μ_e = electron drift mobility
μ_h = hole drift mobility.

Under high frequency conditions[6]

$$R_i = \frac{l^2}{I\tau(\mu_e + \mu_h)}\left[1 + \frac{I_{rf}/I}{\sqrt{1 + (\omega\tau)^2}}\cos(\omega t + \varphi)\right]^{-1}, \qquad [6]$$

where I_{rf} = rf current and

$$\varphi = \tan^{-1}\frac{1}{\omega\tau}.$$

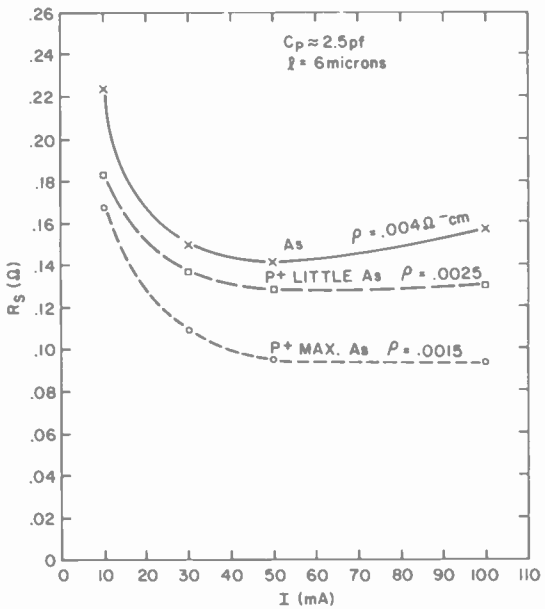

Fig. 5—Series resistance versus forward-bias current of gold-chromium contacted p-i-n diodes showing effect of n^+ layer doping.

For $\omega\tau \gg 1$, the rf term goes to zero and Eq. [6] becomes identical to Eq. [5].

The resistance R_c can be expressed as

$$R_c = \frac{\rho_{n^+} l_{n^+} + \rho_{p^+} l_{p^+}}{A} + \frac{\rho_{cn^+}}{A} + \frac{\rho_{cp^+}}{A} = \frac{\bar{\rho}_c}{A} \qquad [7]$$

where

ρ_{n^+}, ρ_{p^+} = resistivity of n^+ and p^+ layers;
l_{n^+}, l_{p^+} = thickness of n^+ and p^+ layers;
ρ_{cn^+} = specific contact resistance of metal to n^+ layer
ρ_{cp^+} = specific contact resistance of metal to p^+ layer
A = area of diode;
$\bar{\rho}_c$ = total equivalent specific contact resistance.

Combining the various equations, the series resistance R_s of the p-i-n diode can be written

$$R_s = R_i + R_c = \frac{l^2}{I\tau(\mu_e + \mu_h)} + \frac{\bar{\rho}_c}{A}. \qquad [8]$$

Using $\bar{\rho}_c/A$ obtained in the manner described previously, a $(\mu_e + \mu_h)$ value of 1800 cm^2/volt-sec,[7] and the value of τ independently measured

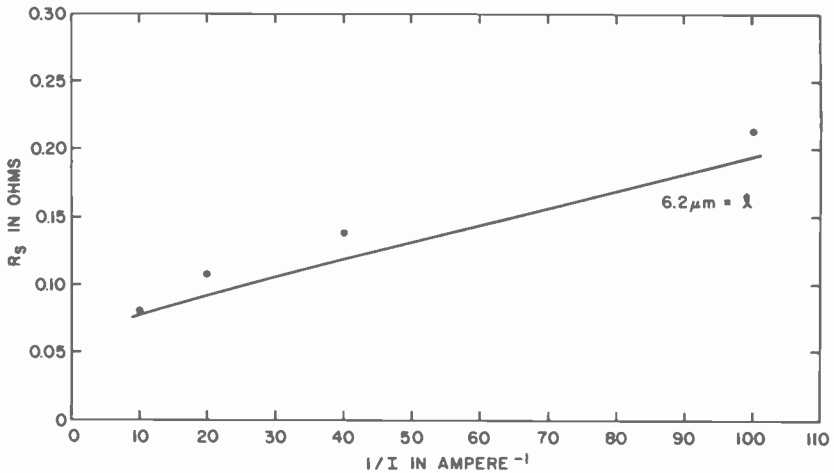

Fig. 6—Series resistance versus (forward-bias current)$^{-1}$ of a gold-chromium-palladium silicide contacted p-i-n diode (I-layer thickness = 6.2 μm) showing correlation between mathematical modeling and experimental results.

at various current levels, the series resistance of the diode R_s as a function of $1/I$ can be predicted through the use of Eq. [8]. The predicted results are plotted in Fig. 6, together with actual experimental data points for a diode with a 6.2 μm thick I layer. The value of τ used is from the measurement by Nuese[8] via the p-n junction step-recovery technique. The measured resistance is always higher than the value predicted by the mathematical model, but the agreement is surprisingly good considering the accuracy of measurements involved in obtaining the various parameters.

4.3 Design Trade-Offs

A. Trade-Offs for an All-Epitaxially-Grown PIN Diode

Generally speaking, the design of a p-i-n diode involves the optimization of the diode's I-layer thickness l with the following operating parameters: the forward current level, the reverse bias voltage needed to switch the diode to a constant-capacitance high-Q state, the series resistance and capacitance combination that is required, and the rf power to be handled.

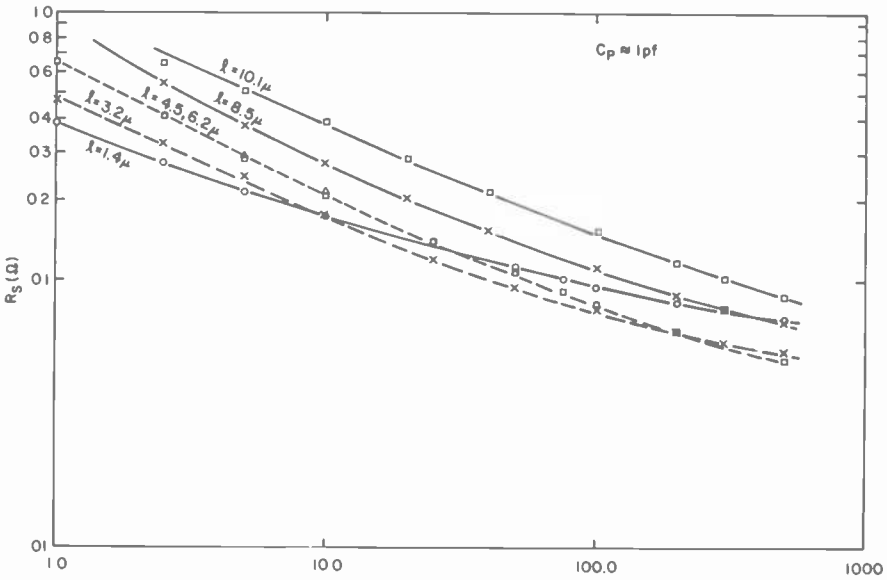

Fig. 7—Series resistance versus forward-bias current for 1 pF p-i-n diodes of various I-layer thicknesses.

The thinner l is, the lower is the resistance due to the I layer, but the higher is the contact resistance due to the metal–silicon contact and the n^+ and p^+ layers. Figs. 7 and 8 show experimentally derived trade-off curves between the diode's series resistance, its I-layer thickness, and the applied dc current in the forward biased direction. The measurement method is described earlier in Section 3. All of the diodes had capacitances of 1 pF ± 5% and their n^+ layer doped heavily with phosphorus and arsenic to a resistivity of 0.0015 ohm-cm. For dc currents ≤10 mA, the experimental results show that to achieve the lowest series resistance, it is beneficial to use as thin an I layer as possible. However, at higher

bias currents (e.g., 25 to 100 mA) the optimum I-layer thickness increases to about 4 μm. Since it is difficult to construct extremely thin I-layer p-i-n diode wafers with high yields, a good compromise for achieving <0.2 ohms resistance is a diode having an I-layer thickness of $\approx$3 μm. The reverse-bias characteristic of such a diode is shown in Fig. 9. Note that the diode's capacitance saturates at only 5 to 10 volts, which is far from the breakdown voltage of $\approx$75 volts. Beyond 10 volts, there is only a 3% further decrease in capacitance.

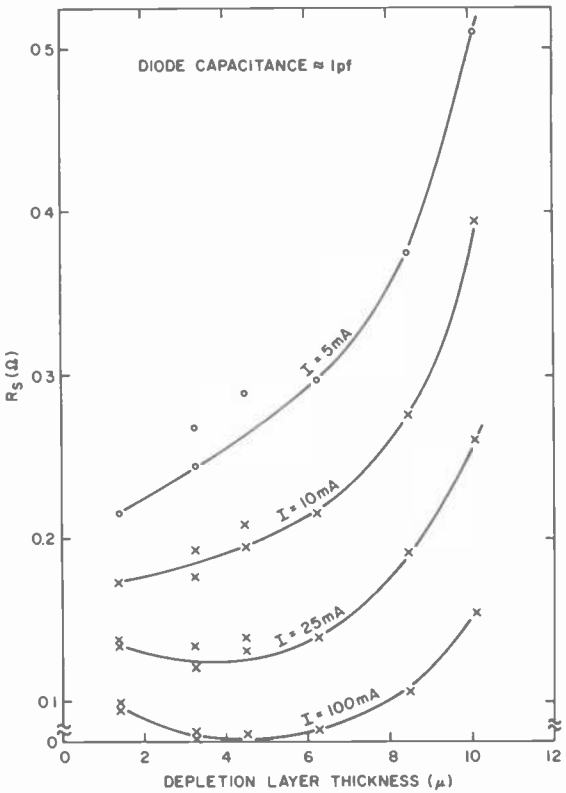

Fig. 8—Series resistance versus I-layer thickness for 1 pF p-i-n diodes at various forward-bias current levels.

B. Sensitivity of Series Resistance to Capacitance

The dependence of series resistance on diode capacitance was experimentally verified through measurements of diodes with capacitance values ranging from 0.07 to 2 pF. As shown in Fig. 10, the dependence of R_s on (area)$^{-1}$ for a fixed I-layer thickness is more and more linear as

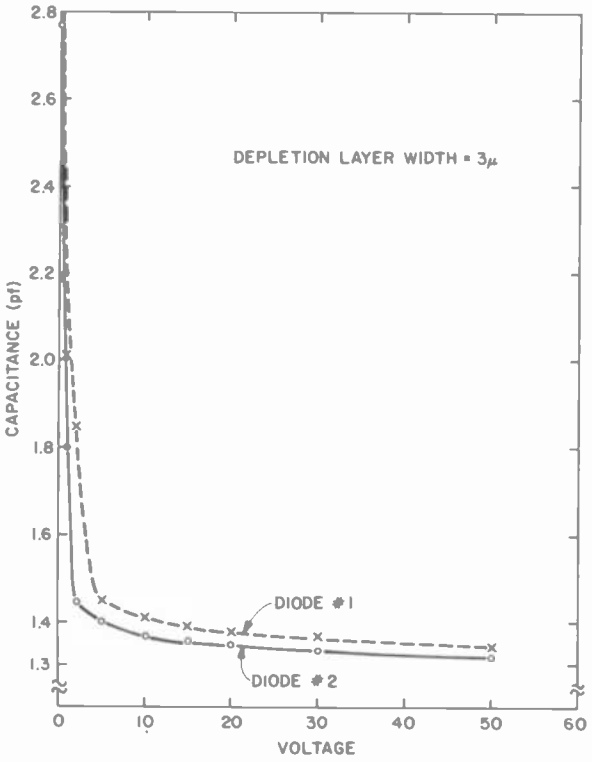

Fig. 9—Reverse-bias capacitance–voltage characteristics of two p-i-n diodes (I-layer thickness = 3 μm).

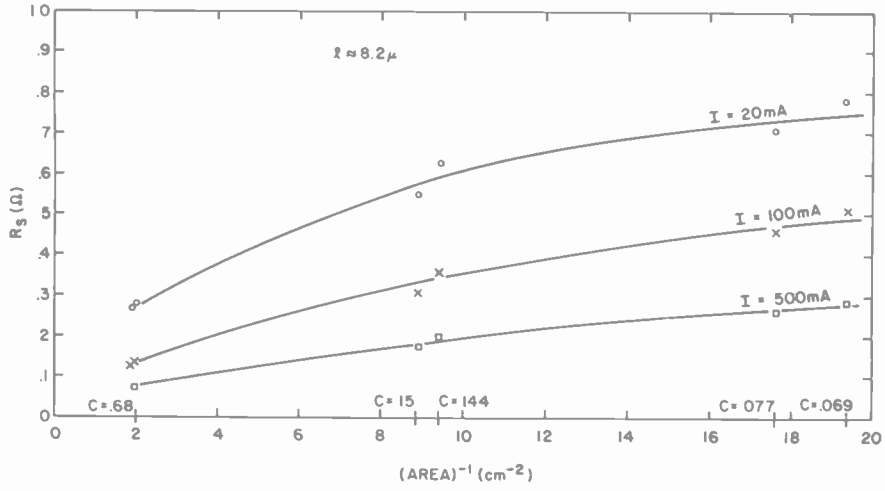

Fig. 10—Series resistance versus $(\text{area})^{-1}$ for a p-i-n diode at various forward-bias current levels (I-layer thickness = 8.2 μm).

the bias current is increased. At very high bias currents, the resistance is simply the contact resistance and, therefore, should be linear with $(\text{area})^{-1}$. These values of resistance correspond very closely to those measured with the diode reverse biased (see Fig. 4 and Ref. [3]). For a reasonable value of bias current (e.g., 20 mA), there is a nonlinear dependence of R_s on diode capacitance as shown in Fig. 11. However, only below about 0.5 pF is there a rapid change of R_s.

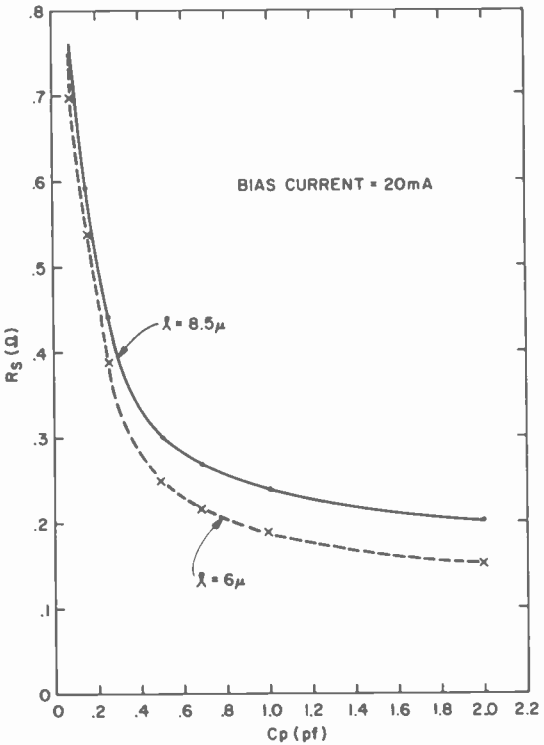

Fig. 11—Series resistance versus depletion capacitance of p-i-n diodes at a forward-bias current level of 20 mA.

C. Trade-Offs with Conventional Thick p^+ Substrate Diodes

PIN diodes constructed by using the thick substrate method described in Section 2.2. exhibited the forward-bias electrical characteristics shown in Fig. 12. The standard commercially available p^+ bulk substrate has a thickness t of about 7 mils (.18 mm) and a resistivity of 0.004 to 0.006 ohm-cm. For the tests described here, epitaxial layers were grown on a p^+ substrate and the wafer was broken into two pieces with one being

thinned down to a thickness of 2 mils (.05 mm) before metallization. The latter thickness represents the practical limit for handling. There is a substantial reduction in series resistance with an all-epitaxially-grown diode which has a p^+ layer thickness of only 4.5 μm.

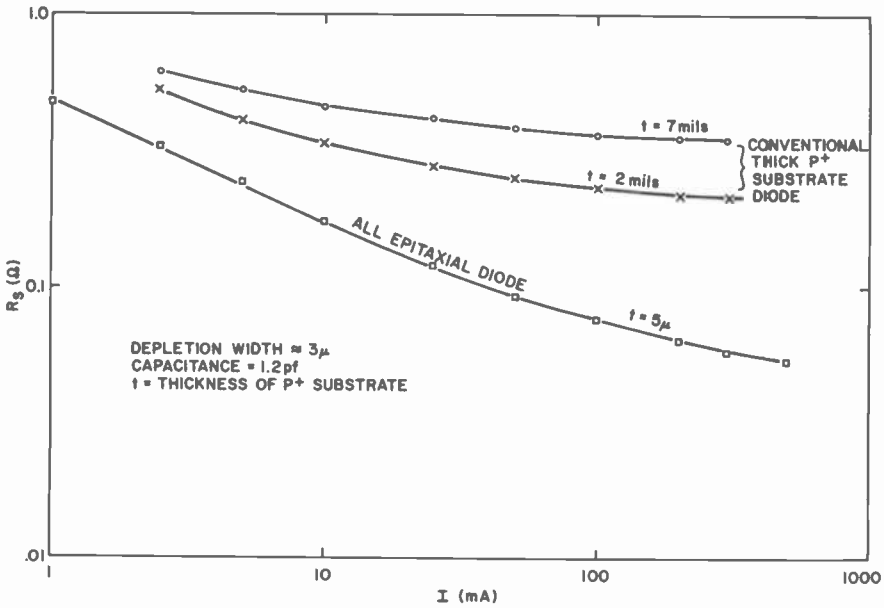

Fig. 12—Performance comparison of an all-epitaxially-grown diode with conventional thick substrate diodes.

5. Discussion

From the experimental results presented in the previous section, it is clearly evident that the all-epitaxially-grown p-i-n diode is superior in performance to the conventional diode using a thick p^+ substrate. However, there are certain advantages inherently associated with the thick-substrate method. Among them are the use of conventional silicon processing technology and the accompanying slight reduction in processing cost of the diode. This slight reduction in processing cost may be offset by the smaller number of diodes produced per wafer because the larger resistivity of the p^+ substrate must be compensated by the use of a larger size chip. Another advantage of the thick substrate method is the likelihood of a lower reverse-bias voltage for switching to the

low-loss capacitor state because of the possibility of obtaining a lower carrier concentration in the I region.

With regard to metal–semiconductor contacts on all-epitaxial-grown diodes, the Pd_2Si-Cr-Au system gave highly reproducible results no matter how the diode was mounted in the package (by thermocompression bonding, ultrasonic bonding, or soldering). In contrast, the Cr-Au system produced very unreliable results that depended very heavily on the method of mounting. Typical R_s versus I curves for diodes mounted by soldering or with top contact via ultrasonic bond wires were shown earlier to have a minimum at a current level that depended on the area of the diode. Diodes mounted in a package using only thermocompression bonding exhibited respectable values of series resistance. It appears that the Cr-silicon interface is unstable and may form an intermediate layer that affects the diode performance only in the forward-biased direction; in the reverse direction, the layer is depleted and therefore has no effect on the diode's series resistance.

Correlation between the mathematical model of the diode's series resistance and experimental results is considered quite good. This is particularly true in light of the fact that measurements of the diode's effective carrier lifetime and its series resistance were independently made, and each has an estimated error of approximately ±10%. In spite of this, the consistency of the measured performance of the all-epitaxially grown diodes is remarkably good. Three batches of diodes having the same I-layer thickness and fabricated with epitaxial structures grown more than five months apart, and with metallization as well as measurements made at different times, reproduce the performance of one another with an accuracy of ±5%.

All of our forward-bias series resistance measurements were made at a frequency close to 600 MHz. However, measurements made at 4 to 8 GHz[9] correspond very closely with those made at 600 MHz, indicating essentially no frequency dependence. This is in excellent agreement with the contention made by Eng,[10,11] Inal and Toker,[12] and Ohtomo[13] that frequency is independent of the series resistance measured under reverse bias.

Acknowledgments

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References

[1] P. Chorney, "Multi-Octave, Multi-Throw PIN-diodes Switches," *Microwave J.*, **17**, p. 39 (1974).

[2] J. P. Nougier and M. Rolland, "Metal-Semiconductor Contact-Resistivity and Noise," *Solid State Electronics*, **16**, p. 1399 (1973).

[3] Y. S. Chiang, E. J. Denlinger, and C. P. Wen, "Contact Resistance of Metal-Silicon Systems at Microwave Frequencies," *RCA Review*, **37**, p. 107 (1976).

[4] C. P. Wen and Y. S. Chiang, U.S. Patent No. 3,846,198, Nov. 5, 1974.

[5] H. A. Watson, Editor, *Microwave Semiconductor Devices and Their Circuit Applications*, McGraw-Hill Book Co., N.Y. (1969), p. 286.

[6] A. Kokkas, private communication.

[7] W. R. Runyan, *Silicon Semiconductor Technology*, McGraw-Hill Book Co., N.Y. (1965).

[8] Results supplied through the courtesy of C. J. Nuese.

[9] J. Rosen, private communication.

[10] S. T. Eng, "Characterization of Microwave Variable Capacitance Diodes," *IRE Trans. Microwave Theory Tech.*, **MTT-9**, p. 11 (1961).

[11] S. T. Eng and R. Solomon, "Frequency Dependence of the Equivalent Series Resistance for a Germanium Parametric Amplifier Diode," *Proc. IRE*, **48**, p. 358 (1960).

[12] K. Inal and C. Toker, "Accurate Determination of Varactor Resistance at UHF and its Relation to Parametric Amplifier Noise Temperature," *IEEE Trans. Microwave Theory Tech.*, **MTT-21**, p. 327 (1973).

[13] M. Ohtomo, "Broad-Band Small-Signal Impedance Characterisation of (Silicon) P^+-N^+-N^+ IMPATT Diodes," *IEEE Trans. Microwave Theory Tech.*, **MTT-22**, p. 709 (1974).

A CMOS/Buried-n-Channel CCD Compatible Process for Analog Signal Processing Applications*

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1. Introduction

This paper describes the results of a study to integrate charge-coupled device (CCD) structures and support circuitry into prototype equipment for use in government communications systems. The support circuitry that was integrated with CCD structures under this program constituted clock drivers and timing/logic circuitry along with CCD signal processing circuitry. The integrated circuit (IC) approach taken was a CMOS-CCD compatible approach that minimizes power dissipation, leads to a reduction in complexity of interface circuitry, and offers high reliability. This effort is expected to enable system users to employ CCD's to achieve substantial reductions in physical size and cost of communication-signal-processing functions as well as improved performance compared with what can be accomplished with either digital LSI or conventional analog approaches.

The CCD-IC array includes two 13-bit Barker-coded correlators; one has split gates while the other has floating gates. The split-gate correlator was intended to provide a standard for comparison, while the floating-

* This program was supported in part by the U.S. Army Electronics Command, Ft. Monmouth, N.J., under Contract DAAB07-75-C-1323, and this paper is a summary of two detailed reports submitted to that agency.[1,2]

gate correlator was intended to generate information pertaining to design of a programmable binary correlator. The IC chip also included two test vehicles. A CCD low-pass filter (anti-aliasing filter) and a long 500-stage register supported by clock drivers and a considerable amount of logic circuitry are integrated.

Both split-gate and floating-gate correlators operated with close to theoretical performance at 16 kHz. Correlation peaks were 13:1 for both a "1" and "0". The 504-stage test register was operated at 1 MHz with a no "fat-zero" transfer efficiency characterized by $\epsilon \leq 10^{-5}$.

In this paper, the CMOS-CCD compatible technology is discussed in Section 2, device design in Section 3, experimental results in Section 4, and summary and conclusions in Section 5.

2. Merged CMOS/Buried Channel CCD Process

To integrate drivers and peripheral logic on-chip with a CCD, it is necessary to develope a compatible CCD/driver/peripheral technology. Many options are possible. However, the requirements of a military communications system (i.e., battery operation, electrically noisy environments, and radiation exposure) indicated that a CMOS technology would be superior with its low power consumption, high noise immunity, and relatively high tolerance to radiation. The decision to use buried n-channel CCDs (N-BCCD) was made because of their high speed, efficiency, reliability, and radiation tolerance.

Certain problems in obtaining a compatible CMOS-CCD were anticipated at the outset, including that of substrate compatibility. One aspect considered was that the voltage of the substrate would simultaneously be the reference for the CCD and the bottom rail for the CMOS logic and clock drivers. This realization motivated the choice of a four-phase, "push" clock scheme and of a fabrication sequence, employing a silicon nitride layer, that ensured that all phase gates maintain the same oxide thickness and identical potential profile (details of fabrication will be discussed later). Another aspect of the compatible substrate problem was that of compatible concentrations and doping polarity. The standard substrate used at RCA for BCCDs is very lightly doped, i.e., $N_A \approx 6 \times 10^{14}$, while the standard CMOS well is 2 to 4×10^{15}. It was proposed initially that the standard p-type well could be implanted and diffused into the lightly doped CCD substrate (thereby electrically connecting the p well and p^- CCD substrate) and that the buried-channel implant of $N_D = 6 \times 10^{15}$, diffused to a thickness of 2 μm, could be used to simulate the standard n-substrate for the p-type devices. This proposal was especially attractive because the characteristics of both standard CMOS and BCCDs could be expected. However, after close examination, it was

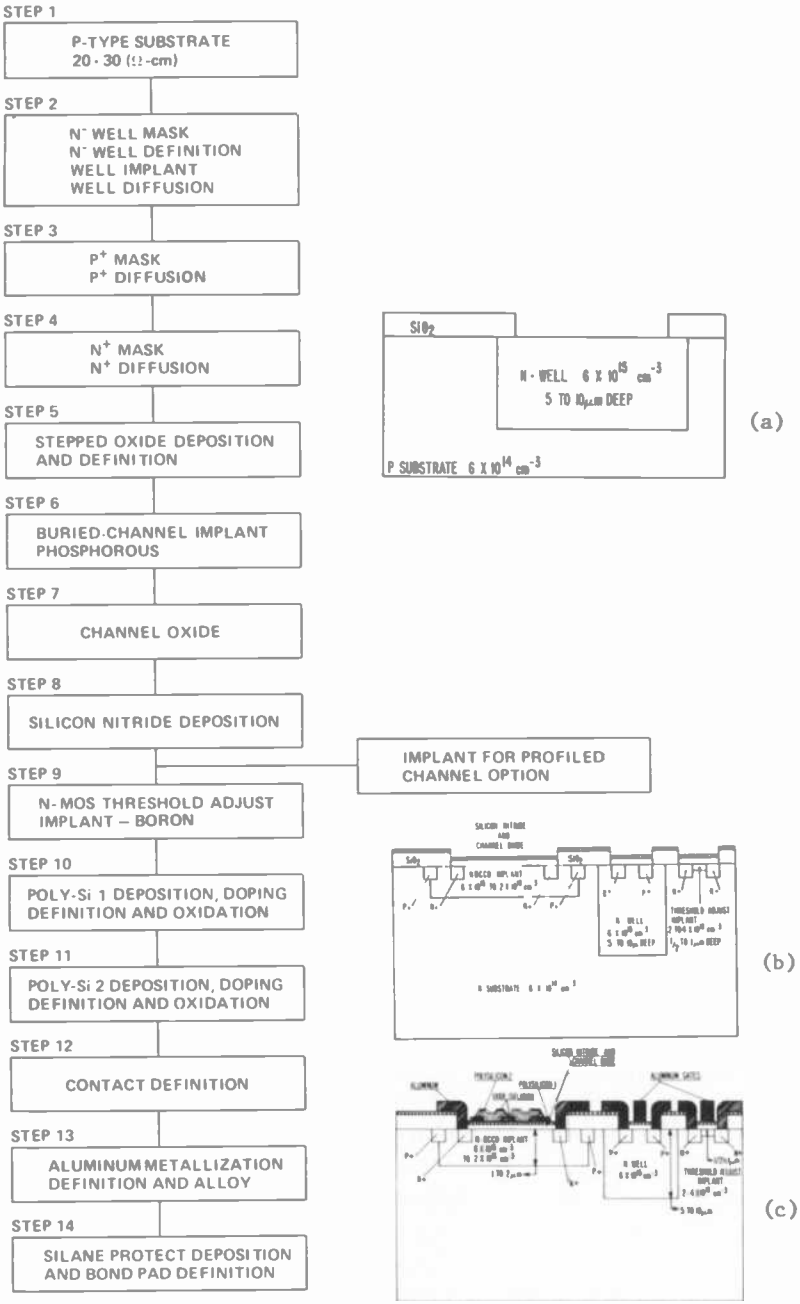

Fig. 1—Merged CMOS and buried n-channel CCD process steps.

realized that the thickness of the 2 μm, n-type buried layer would not be sufficient to contain the depletion layers of the p-type devices that would be operated at a maximum voltage of 15 V. With a diffusion depth of about 1 μm for standard p^+ diode diffusions, the maximum allowable depletion layer would then be only 1 μm; but the depletion width would be close to 2 μm to support a safe design voltage of 20 V. This requires a 3 μm depth for the n region, which is deeper than desired for many buried-channel devices.

The process that evolved was, in fact, a direct "inversion" of the standard CMOS process with an added threshold adjust implant, which is then merged with the basic N-BCCD process. This process is depicted in Fig. 1. The design parameters for the buried-channel implants used are discussed in Appendix A of Ref. [1]. The unusually large number of process steps results from the three implants, the two layers of poly-Si, and the deposited silicon nitride required. Though little attempt was made in the work described here, a great deal of consolidation is possible in a refinement of the process steps outlined. Our interest was to use standard design rules as much as possible. For example, the diffusions are not self-aligned, the CMOS devices are aluminum-gated, and each implant serves a specific function. A number of concepts recently developed for state-of-the-art poly-Si CMOS and NMOS ICs can be pursued in the future to simplify the merged CMOS-CCD process and simultaneously to give higher yield (from fewer process steps), improved packing density, and improved circuit and device performance.

There is a great deal of flexibility in the technology employed. The buried channels may be tailored for desired performance, and the CMOS devices can be independently tailored for particular requirements. The one constraint is that the substrate potential for the CCD and the bottom rail for the CMOS drivers be the same. However, the n-wells can be biased independently, i.e., biased to different positive voltages relative to the substrate. This feature proved to be advantageous in the operation of the floating and split-gate Barker-coded CCD structures, since the directly driven phase gates were driven with 10-V CMOS drivers while the floating gates were capacitively coupled to 15-V CMOS drivers. The common substrate potential could lead to some reduction in buried-channel well capacity because there is, in general, no guarantee that maximum well size occurs in the range from 0 to +10 V on the gates. It may be desirable to use a somewhat negative reference, possibly as negative as the pinning voltage,[3] which is −6 V, for these BCCD devices. However, it was found experimentally that maximum well size occurred with +12-V clock drive referenced to zero. Consequently, a 10-V swing relative to zero substrate potential, which was enforced by the common substrate, proved to be ideal for operation of these BCCDs.

3. Device Design

3.1 CCD Design

With the fabrication approach chosen for the merged buried-channel COS/MOS integrated circuit, the substrate of the CCD and of the transistor not located in a well are the same. This implies that *all* clocks must operate between substrate and some positive voltage for n-channel CCDs or substrate and some negative potential for p-channel CCDs. Thus, dc offsets between clocks would require major alterations to the standard COS/MOS process because additional isolation diffusions would be required. To simplify the clock driver requirements, therefore, it is desirable to operate in a mode in which all gates have the same dc level.

One approach, which accomplishes this but still uses the standard overlapping double poly-Si gate structure, is a four-phase clocking system. The devices are fabricated such that the oxide thicknesses under both poly-Si gates are the same, or nearly so. This can be accomplished by use of a silicon nitride layer to prevent differential channel oxide growth or by etching the oxide in the gaps between the first layer poly-Si and regrowing the gate oxide when these poly-Si gates are oxidized.

The four-phase system is illustrated in Fig. 2. Four separate clock waveforms are required. Each could be a symmetrical square wave, but device performance will improve if the trailing edges of the pulses have some finite slope. Phase 1 and phase 3 are essentially 180° out of phase. Phase 2 is the same as phase 1 except for a 90° phase lag. Phase 4 is 180° out of phase with phase 2. The lower part of Fig. 2 shows the potential wells at various times. At t_1, both phase 1 and phase 4 are ON, and the charge is stored in the region between the adjacent second layer poly-Si (phase 4) and first layer poly-Si (phase 1) gates. Between times t_1 and t_2, phase 2 is turned ON and phase 4 turned OFF. Thus by the time t_2, the charge has moved to the right a distance of one gate (0.2 mil) and is being shared under phase 1 and phase 2 gates. This sequence continues until, after one full period of the clock, the charge moves one full stage to the right..

There are several advantages to this four-phase clocking system. The most important, of course, is that no dc offsets are required between clock phases. All clock drivers can operate between the same dc levels and electrical isolation, and proliferation of a large variety of dc levels is no longer required. Another advantage of the four-phase system is the larger signal that can be propagated. This is especially important when buried-channel devices are being used, since the signal levels in these devices are already lower than those of an equivalent surface-channel structure.

The increased signal occurs because two adjacent gates are used to store charge, thereby doubling the charge-storage area. Also, the full potential difference between an ON channel and an OFF channel can be used to store charge. In two-phase operation only the potential difference between an ON first-layer polysilicon and an ON second-layer polysilicon gate can be used to store charge. Thus one would expect between two and four times the signal charge using the four-phase approach.

The price of using this four-phase system is that more clock waveforms have to be generated—four versus two.

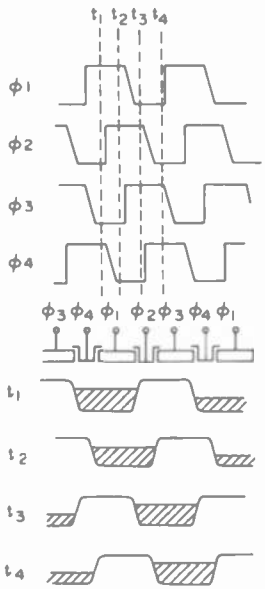

Fig. 2—Four-phase operation showing clock waveforms and potential profiles at the times indicated.

3.2 Split Gate Correlator Design

Perhaps the most straight-forward approach for tapping and weighting a CCD register with a Barker code is the split-gate technique.[4] Since the weighting pattern for a Barker code consists of a pattern of ones and zeros, with no values in-between, the split gates are organized such that they physically cover the full CCD channel width and are either brought out to one side of the CCD register and connected to the positive sum line, for a one, or to the other side and connected to the negative sum line, for a zero. Summing is done by directly coupling all floating gates that come out on the same side. The sum lines are fed to a differential am-

plifier. By arbitrary choice, the side representing correlated "ones" goes to the plus terminal and the side representing correlated "zeros" goes to the minus terminal of the differential amplifier. Since these gates are used not only to sense the presence or absence of charge, constituting patterned data, but also to establish the proper potential profiles in the CCD channel for transfer of charge, these gates must receive the proper phase clock signals. This requirement is accomplished in the specific design implemented by capacitively coupling the split floating gates to appropriate clock drivers.

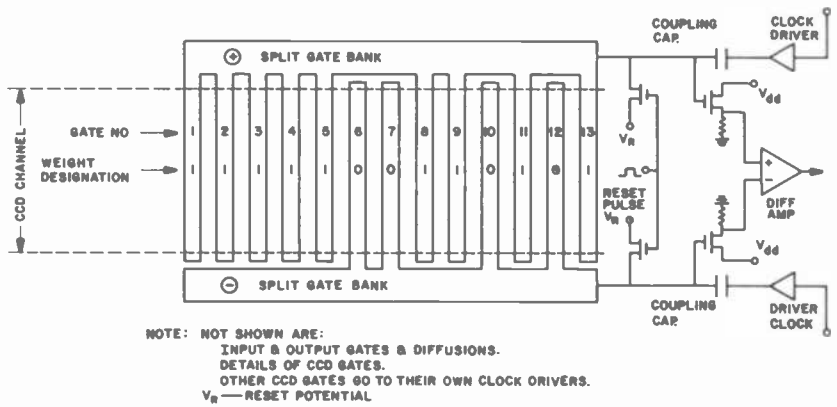

Fig. 3—Schematic of split-gate CCD Barker-coded structure.

The split-gate sensing and clock driving schematic is shown in Fig. 3. Details of the CCD gate structure, input and output gates, are not shown. Included in this schematic are transistors that reset the potential of the gates during the period when there is no charge under the split gates (this is depicted in the timing diagram of Fig. 11).

By inspection of Fig. 3, in which the 13-bit Barker-coded weighting pattern is depicted, it can be seen that there are nine gates with a "one" weighting but only four gates with a "zero" weighting. This leads to an imbalance in phase capacitance between the + and − terminals of the split-gate device. A solution to this problem was found by designing both banks of split gates to have equivalent values of capacitance that track with process variations. This solution was carried out by adding "dummy" fingers (gates) to the − bank of split gates, i.e., five fingers located over a parallel dummy channel were added to the split-gate side that has only four fingers attached. The dummy line is constructed according to the same design rules used for the Barker-coded line, and since the added fingers are fabricated along with the rest of the structure, the counterbalance capacitance will track from process run to run. This

ensures that the line capacitances of the + and − banks of split gates will be identical. A schematic of the counterbalanced structure is shown in Fig. 4 and a photomicrograph of the device is shown in Fig. 5.

In the split-gate and floating-gate vehicles (to be discussed in the next section), the clock drive is capacitively coupled to the floating phase gates. This allows the floating gates to be driven to the proper potential for optimum charge transfer while being simultaneously used to sense the presence of signal charge. The design of the coupling capacitor is

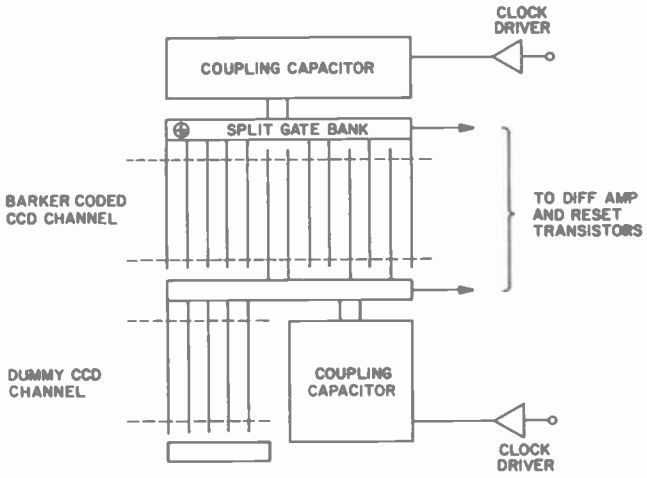

Fig. 4—Schematic of counterbalanced split-gate Barker-coded structure.

shown in Fig. 6. Unless special precautions are taken, the addition of the coupling capacitor unduly increases the parasitic capacitance, which tends to reduce the signal voltage. In this design, the clock drivers are connected to a first-level poly-Si drive plate. Overlying the first-level poly-Si drive plate is a second-level poly-Si plate that is connected by means of an aluminum metallization strap to the first-level poly-Si floating gates. Since the driven plate overlies the drive plate, it is shielded from substrate parasitic capacitance; the problem of competition between parasitic capacitance and active capacitance is thereby solved. An extension of this design provides a top aluminum plate connected to the bottom drive plate with the driven plate sandwiched between. For a given value of capacitance this design version can reduce the required area by a factor of two, but because of the additional complexity and a potential yield problem with a three-layer large-area structure, this feature was not incorporated in the design.

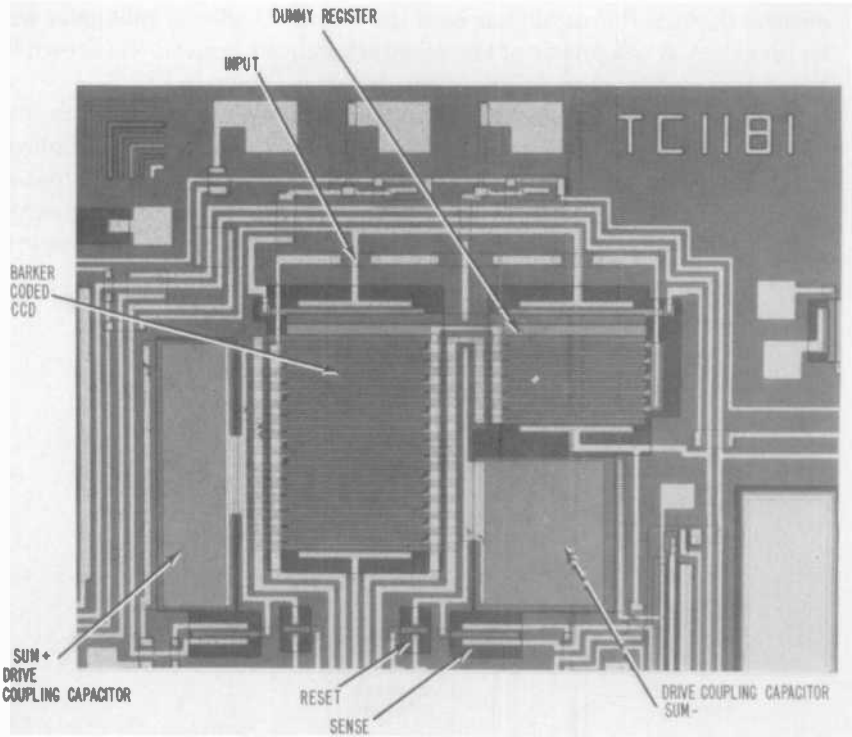

Fig. 5—Split-gate Barker-coded correlator.

3.3 Floating-Gate Correlator Design

While the split-gate tap design is a viable mask-programmable means of tapping, it does not provide an electronically programmable capability. Individual floating-gate taps are required if the individual tap weight

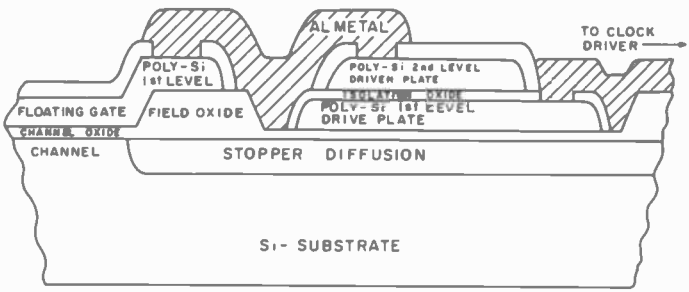

Fig. 6—Coupling capacitor design.

is to be altered electronically. Therefore, it was decided to test a floating-gate tap approach with a second Barker-coded correlator on the chip. No programmability feature is included, however.

One of the problems encountered in earlier floating-gate taps is the problem of setting the dc potential of the floating gate. Therefore, the present design includes a MOS switch to periodically set the dc potential. In addition, in order to increase the signal-handling capability, a capacitively coupled ac clock drive to the floating gate is included so that the channel potential at the floating gate will operate in normal CCD fashion between the same ON and OFF levels as the other CCD gates. The tap

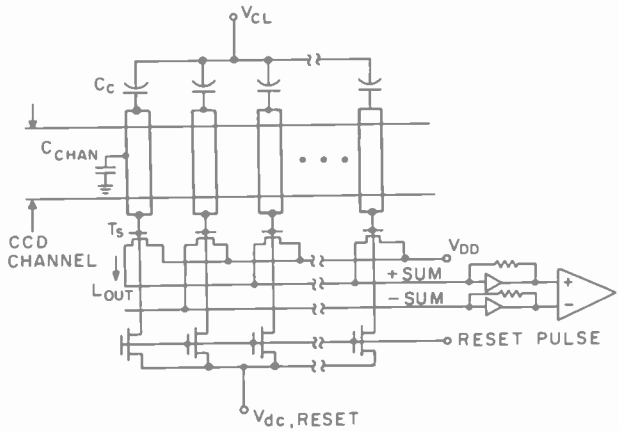

Fig. 7—Schematic of floating-gate tap.

will, therefore, be able to hold as much signal charge as the remainder of the register. This would not be the case if the floating gate were maintained at a dc potential midway between the ON and OFF levels of the other gates.

A schematic diagram of this floating-gate tap is shown in Fig. 7. The ac clock voltage, V_{CL}, is coupled to the floating gate through coupling capacitor C_C. The output current i_{out} through the sense transistor T_S depends upon the voltage of the floating gate which, in turn, depends on the signal-level-dependent channel capacitance C_{chan} of the floating gate. The transistor T_R is the reset switch. Whether the sense transistor source lead is connected to the +sum bus or the −sum bus depends upon the code sequence. A photomicrograph of the actual floating gate device is shown in Fig. 8.

3.4 High-Speed Register Design

While the present Barker-coded test vehicle is designed for 16-kHz clock operation as determined by system requirements, many CCD signal processing applications demand higher clock frequency operation. To provide a test of CMOS clock drivers at higher frequencies, a 500-stage delay line is also included on the chip. The device is a serpentine structure with five 100-stage straightaways with 1.0-mil-wide channels and four corners incorporating floating diffusion turns. CMOS clocks are

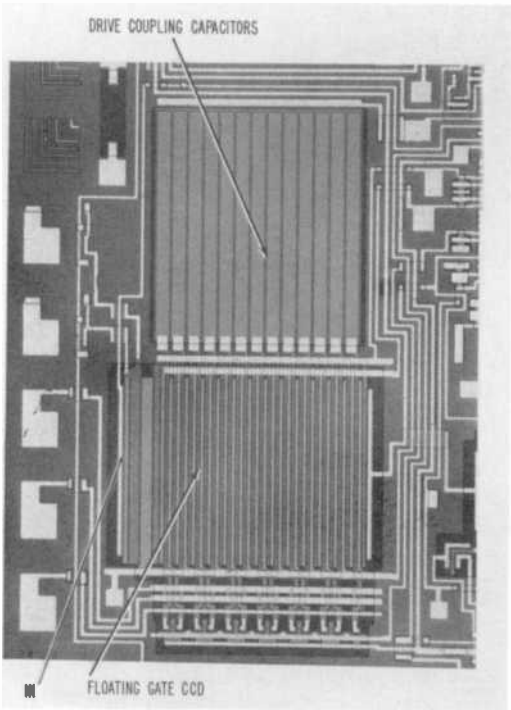

Fig. 8—Floating-gate Barker-coded correlator.

designed to drive the four-phase register at 10 MHz. Clock driver inputs go directly to bonding pads, and clock logic and trigger generation will be accomplished off-chip, as will input and output strobe generation. Bond pads are incorporated between the drivers and the register so that off-chip drivers can be used to establish baseline performance data to compare with on-chip driver performance.

The operation of the floating diffusion corner is illustrated in Fig. 9. A dc gate follows each diffusion. For efficient operation the potential

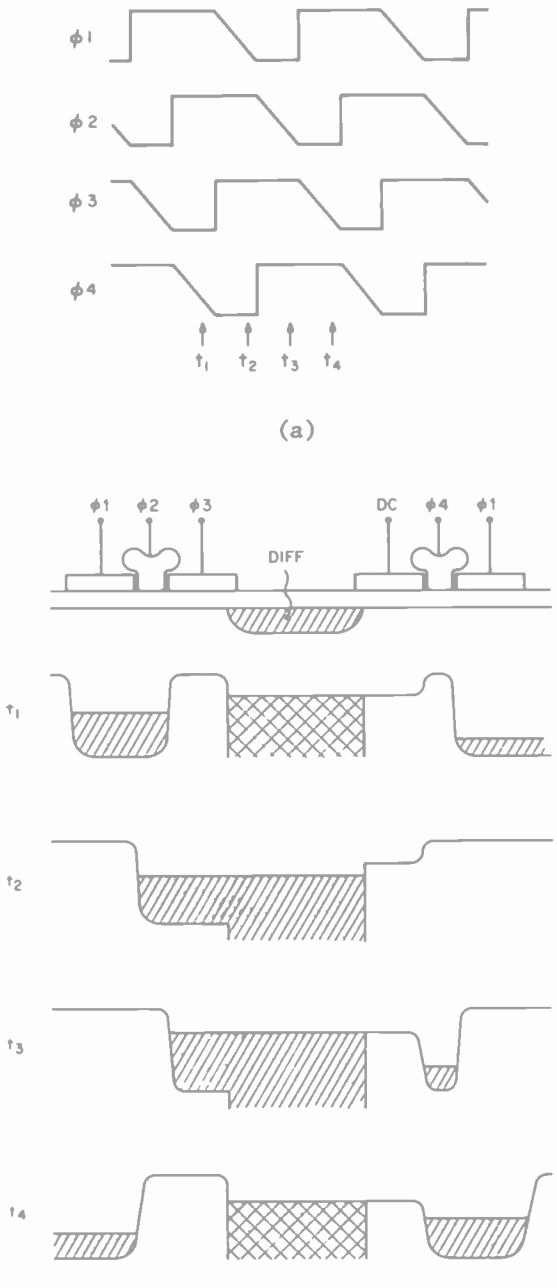

Fig. 9—Floating diffusion corner operation: (a) clock timing and (b) cross-sectional view of the floating diffusion and surface-potential diagrams.

wells in the register should not be filled to a level higher than the potential under the dc gate. A photomicrograph of the 500-stage register is shown in Fig. 10.

3.5 CMOS Logic and Driver Design

The CMOS logic for producing the clock, input strobe, and reset signals is integrated into the same array as the CCD devices. The transistors in the timing logic are all aluminum gates and are designed for 10-V operation. The design of the transistors is the same as the standard CMOS design except that the starting material is different as discussed in Section 2.

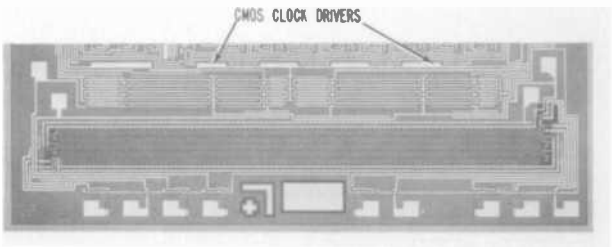

Fig. 10—500-stage test register.

There are three input signals to the timing logic. The first of these is the REF signal from which all the timing signals are formed. The second input signal, the PHASE CLOCK, is used to properly synchronize the timing logic in a system application. The third input signal, MODE, puts the timing logic into one of two possible configurations. When MODE is low, the clock and strobe signals for the input test (SID) device are formed. When MODE is high, clock signals for the higher frequency operation of the two 13-bit Barker-coded correlators are formed.

The frequency of the square-wave REF input signal determines the frequency of the clock and strobe signals generated on the array as shown in Fig. 11. The phase of these signals is determined by the PHASE CLOCK input. The capability to adjust the phase is necessary if synchronization with the input signal is to be obtained and maintained in a system application of the array. The PHASE CLOCK is used to generate the RESET pulse which resets all the registers in the timing logic. Registers A and B in Fig. 12 are used to produce this reset pulse.

A reset pulse R is required to reset the floating gates in the split-gate and floating-gate versions of the 13-bit Barker-coded correlators. The reset pulse is to occur shortly before phase 4 makes its positive transition.

The chosen time is the first half of the period when phase 3 is high and phase 4 is low. The logic for generating the R pulse is shown in Fig. 13. The transmission gates T3 and T4 are controlled by the same signal CLK which is used to clock the I and J registers (Fig. 12). Transmission gate T3 is off at this time. The output of G4 remains high until CLK goes low, turning on T3 and causing G2 to go high.

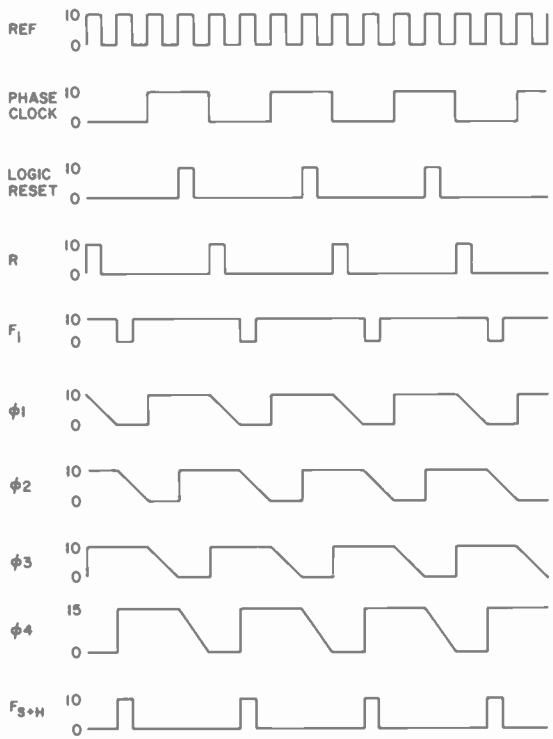

Fig. 11—Split-gate and floating-gate timing and clock signals.

The logic for producing the input strobe signal f_i for the two CCD correlators is the same as that for the R pulse, except for two changes. Since the f_i pulse occurs when phase 3 and phase 4 are high, the input signals to G1 of Fig. 13 become phase 3 and phase 4. Also, the f_i signal is normally high with the pulse going down to a variable V_{SS} voltage. Thus, the output of the pulse-generating circuit is passed through an inverter operating between the variable V_{SS} and V_{DD}. This inverter is the same type as used in generating the f_s signal.

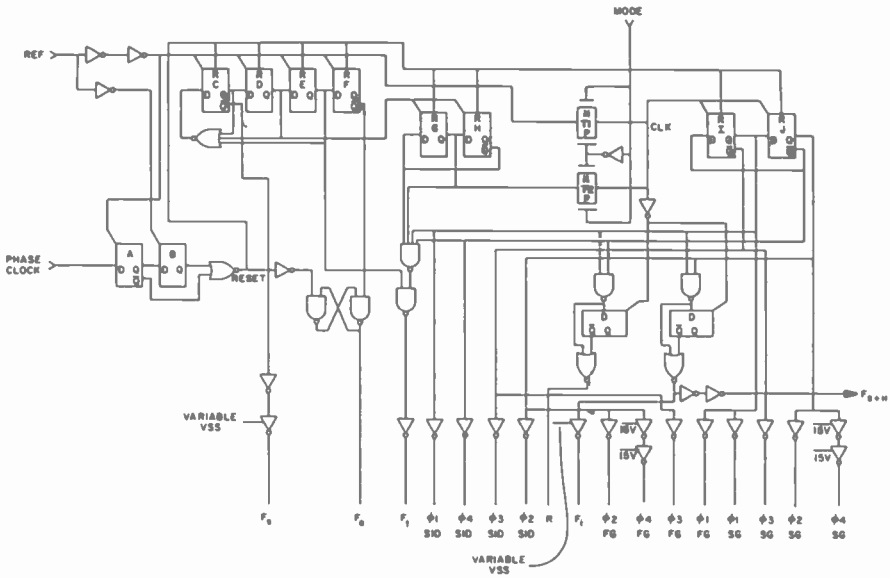

Fig. 12—Timing logic.

A sample-and-hold signal, f_{s+h} is generated and brough to an output pad on the array. This signal is required for the sample-and-hold circuit external to the array that samples the correlator output signal. This signal is the same as the f_i signal prior to its final inversion. The f_{s+h} is passed through an output driver, consisting of two inverters, prior to output from the array. This increases the output driver capability that is needed for the larger capacitive loads seen in going off the chip.

The MODE control permits the floating-gate and split-gate CCD correlators to be clocked at a higher rate than would otherwise be possible. The REF signal is normally reduced in frequency by a factor of 16 in registers C, D, E, F, G, and H before reaching the final Johnson center.

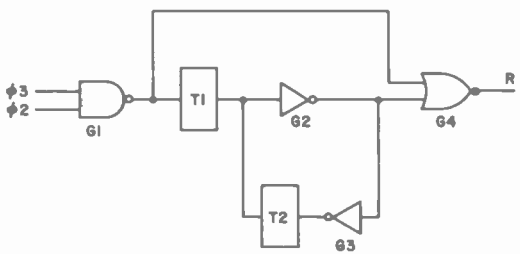

Fig. 13—Circuit for generating phase R.

The maximum frequency is limited by the maximum rate at which the C, D, E, and F registers can be clocked. This remains the case as long as MODE remains low. If MODE is high, the REF input is brought directly to the clock input of the final Johnson counter without being divided by 16. This is done by using the MODE input to control a pair of transmission gates, T1 and T2 of Fig. 12, which select either the output of register G or REF as the clock CLK for registers I and J. The CCD clock frequency is reduced from the REF frequency by a factor of 4 when MODE is high or by a factor of 64 when MODE is low. The signals for the input test circuit are not valid when MODE is high.

Each of the four phases (ϕ) of clock for each of the CCD devices has its own clock driver. The clock drivers take the clock signals as produced by the timing logic and form signals with the proper shape, voltage level, and drive capability.

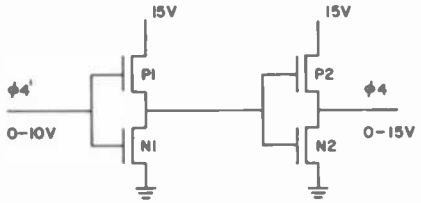

Fig. 14—Phase-4 clock driver with level translater.

A driver consisting of a single inverter is used on all the clock phases except for phase 4 in the split-gate and floating-gate correlators. The output of the inverter is a signal with a 10-V swing from ground to V_{DD}, and a fall time of 200 ns. The rise time is much faster. To obtain this fall time, the n-transistor in the inverter has a longer channel length and a shorter channel width than normal. The clock driver device sizes for each phase were determined by computer simulation of the driver, using the capacitive load presented by the CCD device.

The phase 4 clocks for the floating-gate and split-gate correlators need a different clock driver. The required voltage swing is from ground to 15 V rather than from ground to 10 V. In addition, the capacitive loads are greater, but the rise- and fall-time requirements remain the same. The driver shown in Fig. 14 is designed to meet these requirements.

The first inverter, consisting of transistors P1 and N1, translates the signal swing from 10 to 15 V. The P1 transistor is smaller than the N1 transistor, shifting the switching threshold to the middle of the input off, causing the output of this inverter to go to 15 V. When phase 4′ is high (10 V), both P1 and N1 are on. The gate voltage on P1 is 5 V below its

source, whereas the gate of N1 is 10 V above its source. As a result of the scaling of device sizes, the output of the inverter goes to ground. However, the inverter draws a constant current, which is determined by P1, when phase 4′ is high. This current is minimized by using a small transistor for P1.

The design of the second inverter, consisting of P2 and N2, is governed by the same considerations as those for the single inverter clock drivers. The device sizes to obtain the 200-ns fall time were determined by computer simulation.

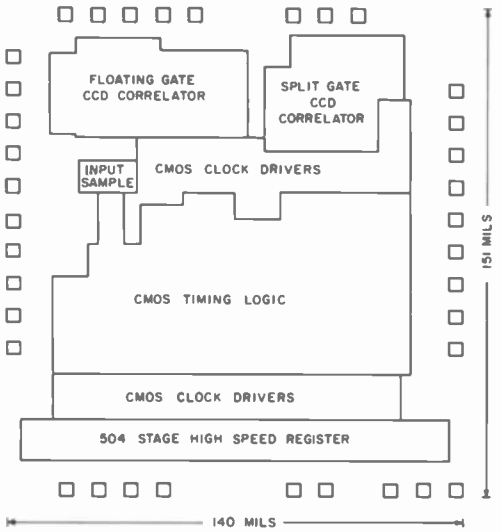

Fig. 15—Layout of CMOS/CCD test chip.

Clock drivers for a high-speed CCD test line are also included on the array. The inputs to these drivers come from off the array. Each driver consists of a single inverter designed for an ouput rise time of 20 ns and fall time of 25 ns. Phases 1 and 3 see a load of 50 pF, whereas phases 2 and 4 see a load of 100 pF. The drivers for phase 1 and 3 use a 20-mil n-transistor and a 50-mil p-transistor. The phase 2 and 4 drivers have 40-mil n-transistors and 100-mil p-transistors. Special care is taken in designing these drivers to keep the series resistance in the signal path to a minimum.

3.6 Array Layout

A block diagram of the CCD-IC test array is shown in Fig. 15. Overall chip dimensions are 159 × 148 mils (151 × 140, bond pad to bond pad).

A little more than one-third of the chip is used for CMOS timing and logic, somewhat less than one-third for CMOS drivers, and the final one-third for CCD devices. The area not blocked out on the chip accomodates test devices for process control. The total number of bond pads is 36, not including internal bond pads for test purposes. A photomicrograph of the entire chip is shown in Fig. 16.

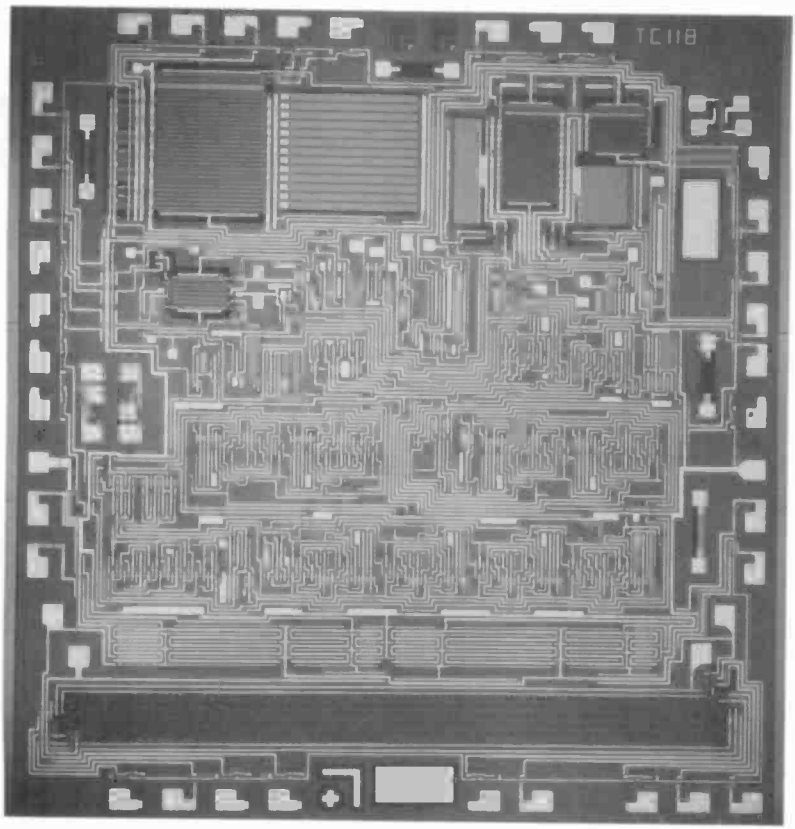

Fig. 16—CMOS/CCD array.

4. Experimental Results

4.1 General Device Characteristics

The transistor characteristics of the Al-gated CMOS transistors from the final two fabrication runs were nearly identical. A set of n and p characteristic curves are shown in Fig. 17. These devices have nominal design rules of: channel length = 0.3 mil, channel width = 4 mils, oxide

thickness is 1000 Å plus 400 Å silicon nitride. Typical characteristics are listed below:

$$V_{TN} = 1.2 \text{ V} \qquad V_{BN} = 23 \text{ V}$$
$$V_{TP} = -2.5 \text{ V} \qquad V_{BP} = 34 \text{ V}$$

The transistors exhibit close to standard characteristics with the exception that the p-type threshold is more negative than standard. This could be adjusted by the choice of a lighter n-well implant.

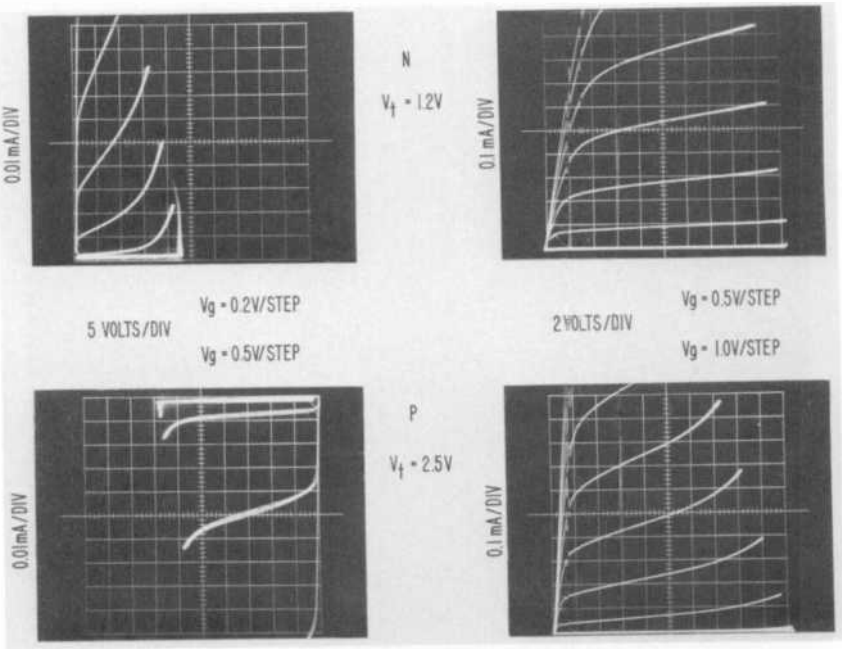

Fig. 17—CMOS transistor characteristics on array (25 to 50 ohm-cm), p-type substrate.

The CCD devices also exhibited the expected potential minima versus gate voltage characteristics as shown in Fig. 18. Both the first-level polysilicon gates (G-1) and second-level gates (G-2) exhibit the same characteristic. This is expected due to the silicon nitride layer, which results in the same gate oxide layer thickness for both levels of polysilicon. The trace in Fig. 18 shows only positive gate voltages because the protective diodes attached to the input gates prohibit a negative voltage swing relative to substrate.

The topological features of the CMOS-CCD array were examined using the scanning electron microscope. Features of interest are the

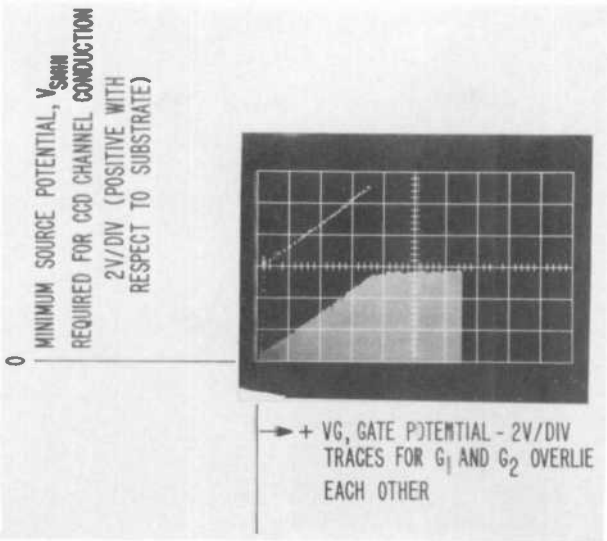

Fig. 18—Minimum potential of the source diode for the onset of CCD channel conduction CMOS/CCD-array lot 3, wafer A. The top dotted trace shows the actual data; the whitened trapezoidal area represents the actual data displaced vertically by 6 V.

poly-Si coverage, edge profiles, Al-metallization coverage, and continuity over the poly-Si and SiO_2 edge contours and contact regions. Fig. 19 shows the overall features obtained in CMOS-CCD array. A detail of the Al-metallization crossing a tapered field-oxide edge, two layers of poly-Si

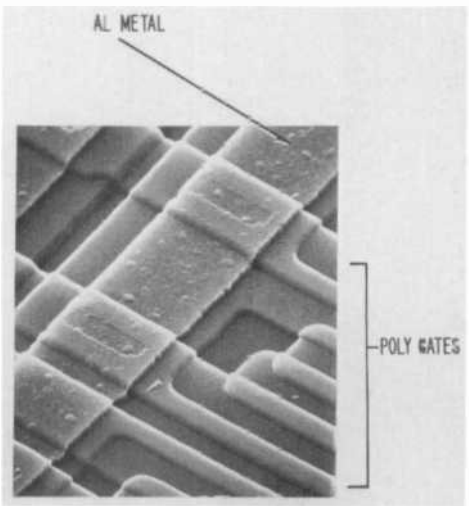

Fig. 19—SEM of double poly-Si CMOS/CCD structure.

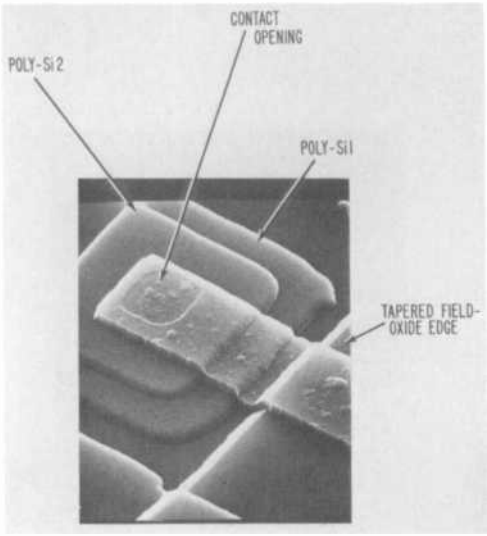

Fig. 20—Al-metal crossing a tapered field-oxide edge; two layers of poly-Si to a contact opening.

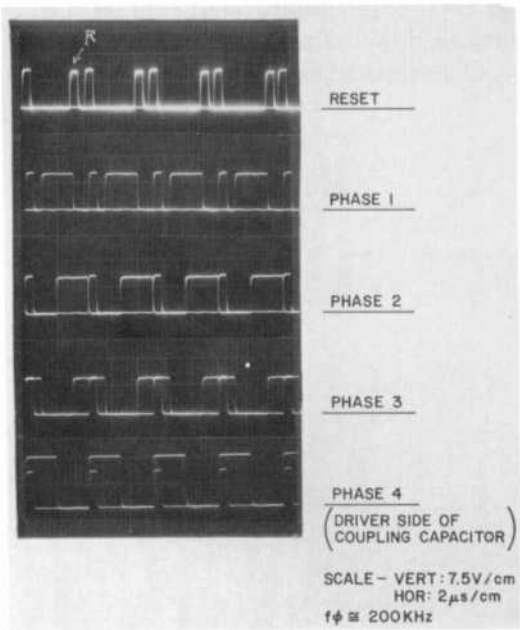

Fig. 21—Reset pulse and phase clocks relative to F_{S+H} (lot 2, wafer A).

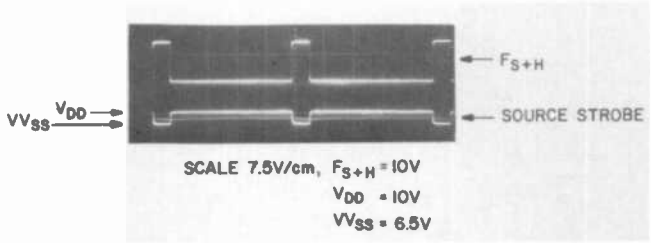

Fig. 22—Input source diode referenced to F_{S+H}.

to a contact opening, is shown in Fig. 20. The contours of the oxidized poly-Si edges are rounded, and the field-oxide edges are smoothly tapered.

4.2 Clock Logic and Driver Operation

All clock logic and driver circuits operated as designed. Fig. 21 shows scope trace photos of the reset pulse and phase clocks relative to the sample-and-hold pulse. Comparison with Fig. 11 indicates that the desired timing has been achieved. The reference frequency was 800 kHz; phase clocks were 200 kHz. Fig. 22 shows the input source strobe, the amplitude of which can be varied with VV_{SS}. All wave shapes appeared to be consistent with the design. The wave shape of the phase-four clock when operating at 200-kHz frequency is shown in Fig. 23 on an expanded scale. The rise time is about 100 ns, and the fall time is about 200 ns. The design value of the fall time was 200 ns, and the objective was to have a faster rise time than fall time. These conditions are necessary for operation of the correlator vehicles up to 1-MHz clock rates, the maximum design frequency for these vehicles.

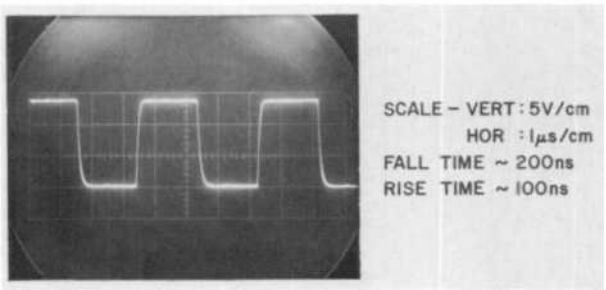

Fig. 23—Shape of clock waveforms.

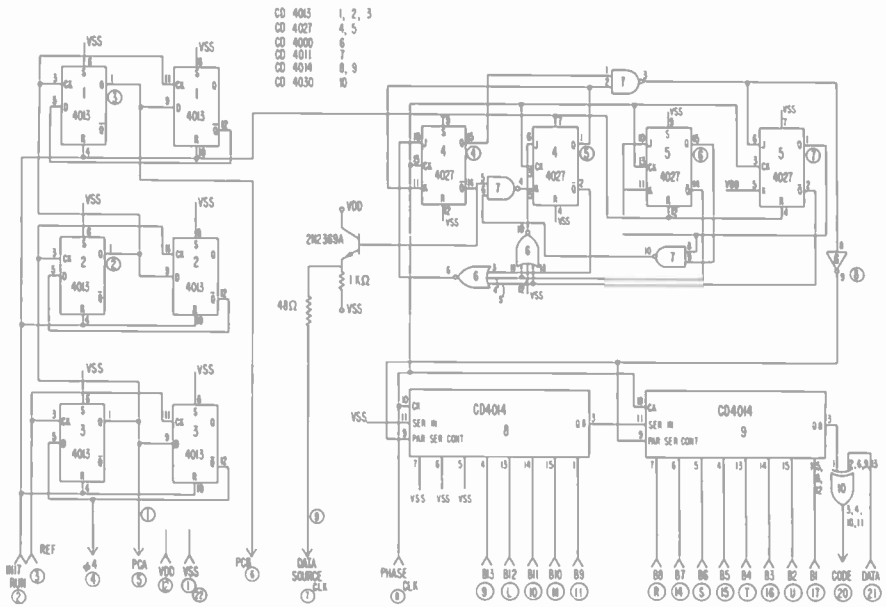

Fig. 24—Array exerciser for CMOS logic.

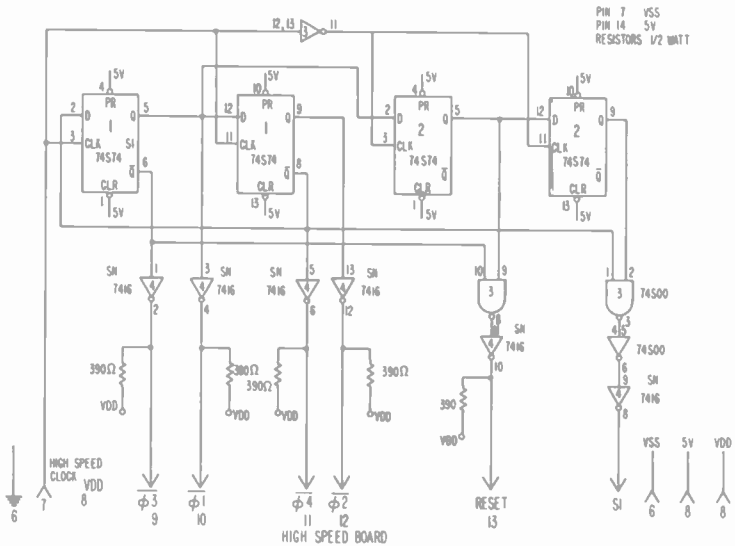

Fig. 25—High-speed register logic.

4.3 Array Exerciser Design

An array exerciser and test fixture were designed to provide a convenient means of demonstrating and evaluating the performance characteristics of the array. The array exerciser contains circuitry for encoding data bits into 13-bit Barker-coded sequences. These Barker-coded sequences may be applied to the inputs of either the split-gate correlator or the floating-gate correlator. Also produced by the exerciser are the phase clock and various bias voltages required for the correlator operation. Another portion of the exerciser is devoted to producing the four-phase clock and bias voltages for operating the high-speed test register.

The array exerciser was built using CMOS 4000 series logic is shown in Fig. 24. The high speed and reset register logic circuitry is shown in Fig. 25 using TTL.

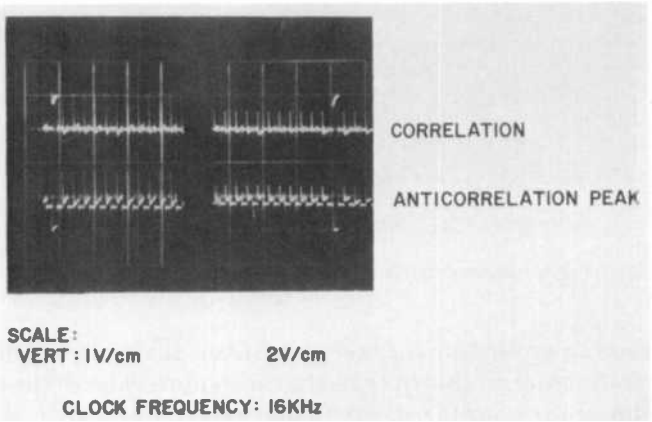

Fig. 26—Correlation response for floating-gate CCD as sensed with CMOS operational amplifiers.

4.4 Floating Gate Correlator Operation

Fig. 26 shows the correlation response for the floating-gate CCD correlator for 1-V and 2-V output correlation peaks as sensed with CMOS operational amplifiers. This response fully exercised the design concepts employed. Examination of the trace in Fig. 26 shows a sharp spike at the clock transition time. These spikes are due to mismatch in the leading and falling edges of the phase-four clock used to compensate the virtual-ground operational amplifiers. In application of the correlator, a sampling threshold detector would be used to detect the correlation peaks. With proper timing, the detector would not be influenced by the

spikes at transition points. Note that the side-lobe patterns do not change significantly under conditions where the output is changed by a factor of two. The ±2-V output corresponds to nearly full-well signal.

The anticorrelation response is shown in greater detail by Fig. 27. With the signal continuously repeated, the expected side-lobe pattern is all "1's" of the same polarity as the correlation peak with a ratio of 1 to 13. It is difficult to measure peak-to-side-lobe ratio with the type of pattern wherein the side lobes are all "1's", because the reference is difficult to establish. Note that the constant dashed level in the display of Fig. 27 is not the reference for the side-lobe pattern, but rather it is the level

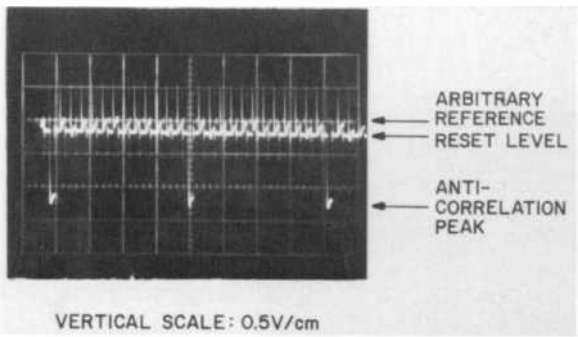

Fig. 27—Anticorrelation response of floating-gate CCD.

established by grounding the reset transistor. It should be pointed out that were the baseline chosen to be the constant reset level, the side lobes would appear in opposite polarity to that expected theoretically and the peak-to-side-lobe ratio would be only ≈ 6:1. If it is assumed that the peak is correct, i.e., 13 "1's", then the appropriate reference would be the baseline located 2 cm below the top of the trace. The side lobes, then, with noticeable fluctuations but on average, appear to be one small division below the baseline arbitrarily chosen. Another way to say the same thing is that if it is assumed that the side lobes do not have the opposite polarity relative to the peak, the peak should be 12 divisions above the average side-lobe peak. Then the baseline is located one division above the average-side-lobe peak which is approximately 2 cm (two large divisions) below the top of the trace. Certain irregularities in the side-lobe pattern can be explained by the observation that a modulation with the period of the 13-bit Barkar-coded appears to modulate the side-lobe pattern to some extent. The cause of this has not yet been determined.

Experiments were carried out to determine the maximum number of error bits allowed before detectability of the correlation peak is in jeopardy. Not all possibilities were covered, but the worse case at three "miss-hits" appeared to have a detectable correlation peak. However, worst case with four "miss-hits" did not exhibit a detectable correlation peak.

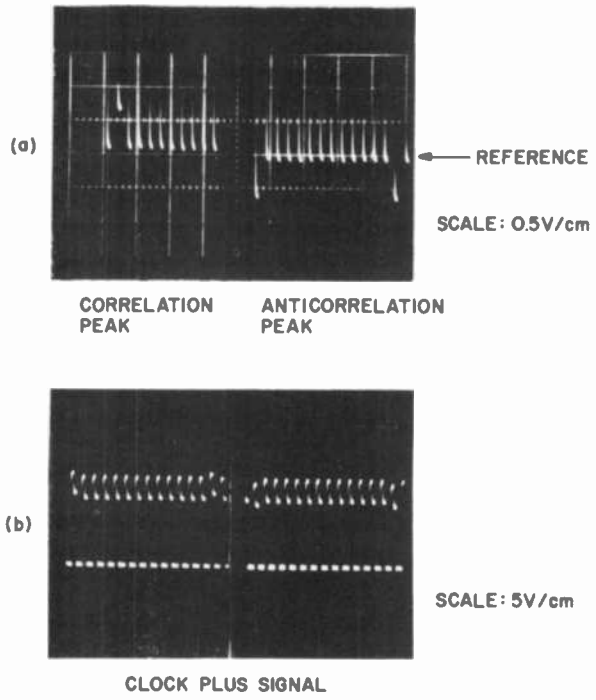

Fig. 28—Correlation and anticorrelation peaks for split-gate correlator and CMOS differential amplifier.

4.5 Split Gate Correlator Operation

Fig. 28(a) is a trace of the correlation and anticorrelation peaks obtained using the split-gate correlator and an off-chip CMOS differential amplifier. In view of the special design intended to capacitively balance both sides of the split phase, a rather large amount of capacitive imbalance was actually observed. This trace was taken by offsetting the display so that primarily signal content is shown. It can be observed that the side-lobe pattern is extremely uniform. Using the midpoint between the correlation and anticorrelation side-lobe levels as a reference, a corre-

lation peak to side lobe ratio of 13:1 is observed. As with the floating-gate vehicle, the reference is located slightly below the side-lobe pattern of the correlation peak. This pattern constitutes uniform "1's", as it should for a noninterrupted Barker-coded sequence. The reference is not actually visible but must be inferred. The total signal-plus-clock output is about 14 V when the differential amplifier is operated near the limit of its maximum dynamic range, as shown in Fig. 28(b). The correlation peak is 0.65 V above the 14-V level and the anticorrelation peak is 0.65 V below. Not all of the samples indicated as uniform a side-lobe pattern. Fig. 29 shows a strong correlation peak but also indicates a Barker-coded feedthrough pattern exhibited by the side lobes.

4.6 Test Register

The 504-stage test register was designed to test the effect of the merged CMOS-CCD process on fundamental CCD parameters, as well as to test the high-speed capability of this new technology. The integrated driver-delay line was designed to operate up to 10 MHz. All other vehicles on the TC1181 CMOS-CCD array were designed to operate up to 1 MHz. Testing of the CCD test register has been done at 1 MHz and tests at higher speed are to be conducted.

Fig. 30 is a trace of a signal comprising eight "1's" delayed through the 504-stage register when operated at 1 MHz. The transfer efficiency shown in this trace corresponds to an ϵ of 1×10^{-4}. This measurement was made without fat zero injection. Other devices have exhibited an ϵ of 1×10^{-5} without fat zero.

Operating biases corresponding to the results in Fig. 30 were

G1 = 1V	V_{DD} = 12.5V
G2 = 2V	+15 = 21.6 V
corner dc = 3V	S1 = 14.8 to 9 V

The test register was driven with the on-chip clock drivers, but the phase clock timing and predriving were obtained from pulse generators.

A further test of interest is to determine if the input stage, CCD well depth, or the corner diffusion well limit the maximum signal. Initial tests indicate that maximum signal is not determined by the corner diffusion well, but the maximum signal injection has not been identified as an input-related effect or a CCD-well capacity limit. In any event, with a 1-mil channel width, and a four-phase device, output signal levels (200 mV) are equivalent to those seen with two-phase 2-mil-channel-width CCD devices with the same source-follower output circuit.

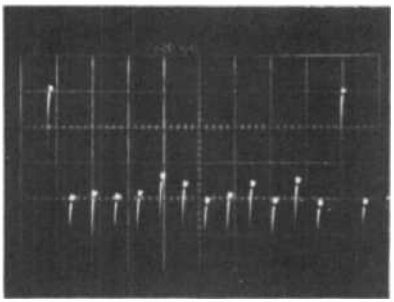

Fig. 29—Split-gate CMOS/CCD Barker-coded correlation at 16-kHz clock frequency with feed-through.

5. Summary and Conclusions

The most significant result reported in this paper is the development of a CMOS-CCD technology that offers low power dissipation, excellent performance, and the promise of high reliability due to the use of CMOS logic and buried n-channel CCDs. A complex CCD array (comprising split-gate and floating-gate 13-bit Barker-coded correlators), a low pass filter, and a 504-stage CCD register have been integrated along with supporting CMOS timing/logic, drivers, and signal processing circuitry.

In addition to the integration of CMOS timing/logic circuits and drivers, CMOS–IC amplifiers (TC1148) were used for sensing the correlator signals. These ICs could have been incorporated with the CMOS/CCD array, but to save time and expense, they were used in a

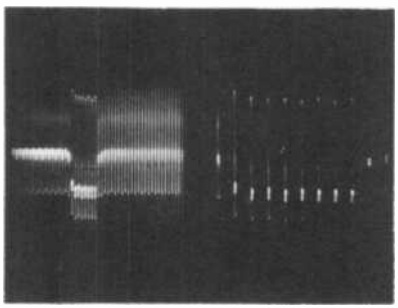

Fig. 30—Pulse response of 500-stage test register; clock frequency equals 1 MHz.

breadboard format. These CMOS–IC operational amplifiers can be used for applications up to 1-MHz signal frequency, and their use at 16 kHz, the frequency of interest for the correlator vehicles, was highly successful. Symmetric correlation peaks, representing a "1" and anticorrelation peaks, representing a data "0", were observed for both the split-gate and floating-gate correlators.

The floating-gate correlator developed was designed in a format that would allow its implementation in an electrically programmable configuration. Electrical programmability can be obtained simply by adding a programmable register that controls switches to connect the floating-gate taps through source-follower transistors to either the plus- or negative-sum buss.

The split-gate correlator produced the expected correlation response with a high degree of regularity in the side-lobe patterns; however, the + and − phase imbalance should be improved to obtain better clock cancellation. The side-lobe pattern in the floating-gate correlator was somewhat "irregular"; nevertheless, the expected correlation peak was observed. Detectability with up to any combination of three "miss-hits" (error-bits) appears to be entirely practical.

A transfer efficiency characterized by $\epsilon < 10^{-5}$ was measured with the 504-stage test register at 1 MHz using the pulse technique with no fat zero. This performance is remarkably good considering the rather long diffusion schedules required for the n-well formation prior to the CCD fabrication.

The successful results achieved in this study prove the feasibility of a compatible CMOS-buried n-channel CCD process. This makes possible the simultaneous incorporation of the inherent low power, high noise immunity, and high performance advantages of CMOS on-chip with high efficiency CCD devices to achieve self-contained signal processing components (such as analog delay and transversal filters) that will not require complex external support circuitry. Such arrays can now be designed to achieve a substantial reduction in cost, size, and power compared with standard analog or digital signal processing approaches.

Acknowledgments

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H. Kaiser for their assistance in the initial design phases. Others who contributed include D. Allesandrini, Harold James, and Glynn Gillette. A. Dingwall and B. Rosenthal provided the CMOS operational amplifiers used in some of these tests.

References:

[1] R. Dawson, J. Carnes, and J. Pridgen, "CCDs for Communication," Interim Report prepared for U.S. Army Electronics Command, Fort Manmouth, NJ, under Contract DAAB07-75-C-1323, May 1976.

[2] R. Dawson, J. Carnes, J. Pridgen, and J. Preisig, "Charge-Coupled Devices for Communication," Final Report prepared for U.S. Army Electronics Command, Fort Monmouth, NJ, under Contract DAAB07-75-C-1323, Oct. 1976.

[3] W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," *RCA Review*, **36**, p. 566, Sept. 1975.

[4] D. D. Buss, D. R. Collins, W. H. Bailey, and C. R. Reeves, "Transversal Filtering Using Charge-Coupled Devices," *IEEE J. of Solid-State Circuits*, **SC-8**, p. 207 (1973).

Suppression of Premature Dielectric Breakdown for High-Voltage Capacitance Measurements*

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Abstract—Surface-initiated premature dielectric breakdown is encountered in extended-range MIS C(V) measurements at applied-bias voltages above some sample-dependent threshold value, e.g., 3 to 5 kV across a 150-μm-thick wafer of sapphire. It is necessary to suppress this premature breakdown in order that a much larger applied-bias voltage may be used without damaging the sample. This may be accomplished by eliminating the air space adjacent to the sample surface at the junction of the dielectric and the electrode edge. A simple, easy-to-use apparatus (sample holder and probe assembly) that allows this to be done conveniently and quickly by using a silicone washer to cover the edge of the electrode and the adjacent area of the insulator is described.

1. Introduction

1.1 Description of the Problem

A recently developed modification of the MIS C(V) technique[1] has extended its useful range, allowing it to be used for the measurement of samples with insulating layers more than two orders of magnitude greater in thickness than was previously possible. This use, however, requires

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the application of large bias voltage to the capacitor sample to be measured. When the bias voltage exceeds some threshold value (e.g., 3 to 5 kV across a 150-μm-thick wafer of sapphire[2]) there exists the danger of breakdown in the critical region along the insulator surface or in air at an electrode edge as shown schematically in Fig. 1(a).

The breakdown at the surface or in air usually leads to breakdown of the dielectric under test (sapphire in the present work). This problem

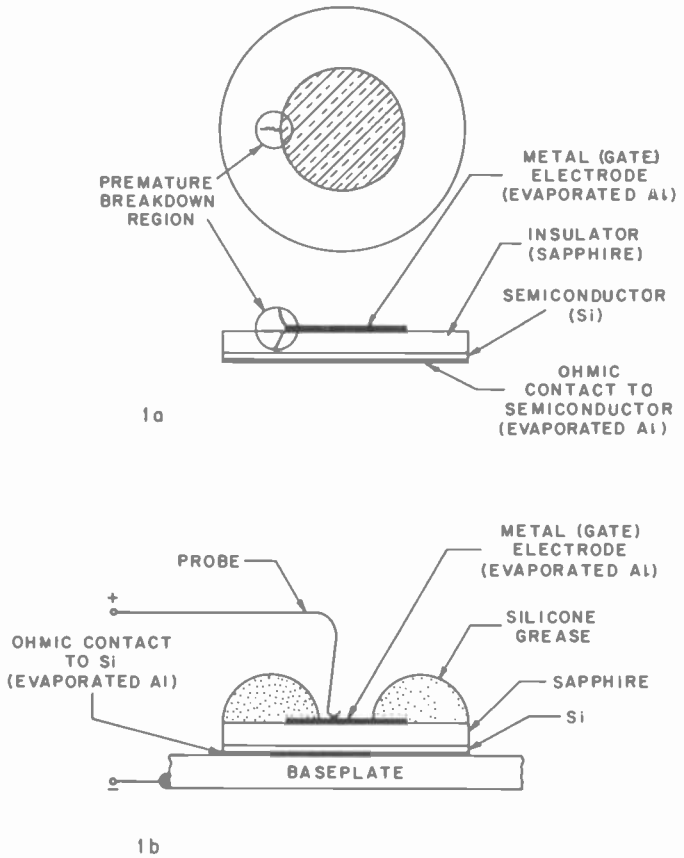

Fig. 1—Sample configuration illustrating (a) critical region where premature breakdown occurs and (b) use of silicone grease to suppress premature breakdown.

is similar to the one of "premature breakdown" encountered in the measurement of "breakdown strength" in dielectric media.[3] The present problem is different, however, in three respects. For C(V) measurements, (1) the high-field region should have a well-defined area, (2) the field

within this region should be as uniform as possible, and (3) there is no need to raise the applied field to the breakdown level.

1.2 Conventional Techniques for Suppression of Premature Breakdown

The known methods of preventing premature breakdown[3] can be roughly categorized as follows:

(1) Immersion of the sample or its critical region in
   (a) suitable gas at high pressure (e.g., N_2 at 100 atmospheres)
   (b) liquid, either insulating (e.g., oil) or partially conducting (e.g., aniline)
   (c) solid (e.g., silicone grease or elastomer)
(2) Shaping of sample geometry to reduce the electric field at the electrodes edges (e.g., "recessed specimen" or "McKeown specimen" technique).

Each of these methods in its conventional embodiments is undesirable in the present application for one or more reasons: 1(a) would be difficult and time-consuming to implement; 1(b) and 1(c) are messy and inconvenient to use; and 2 is inconsistent with our requirement of a uniform field over a well-defined area. Method 1(c) was used[2] with partial success up to about 8 kV. The solid used to immerse the critical region was a silicone grease (Dow Corning "4-Compound").* This is shown in schematic cross section in Fig. 1(b). The application of the silicone grease to the sample and its removal after the measurement were difficult, messy, and time-consuming. In addition, the technique did not consistently prevent breakdown above about 6 kV.

In one set of experiments half of the samples were destroyed by dielectric breakdown when voltages up to 8 kV were applied across 150-μm sapphire wafers during measurements. These and other equally catastrophic results made it clear that a better method for breakdown prevention was needed to make the measurement technique a practical one for everyday use rather than a research laboratory curiosity.

The new breakdown suppression technique and the associated apparatus and test chamber described in the following sections of this report were developed as part of a measurement system to be used for routinely carrying out high-voltage extended-range MIS C(V) measurements. The first part of that system (a capacitance meter bias-isolation unit) has been previously described.[4]

* Certain commercial equipment, instruments or materials are identified in this report to adequately specify the experimental procedure. In no case does such identification imply recommendation or endorsement by the National Bureau of Standards, nor does it imply that the material identified is necessarily the best available for the purpose.

2. A New Technique

2.1 Basic Description

It has been found that if an insulating silicone-rubber toroidal washer having appropriate properties is pressed over the sample surface including the electrode edge, premature breakdown can be effectively prevented. The surface of the rubber in contact with the sample must be smooth and the rubber itself must be very resilient. It is also important

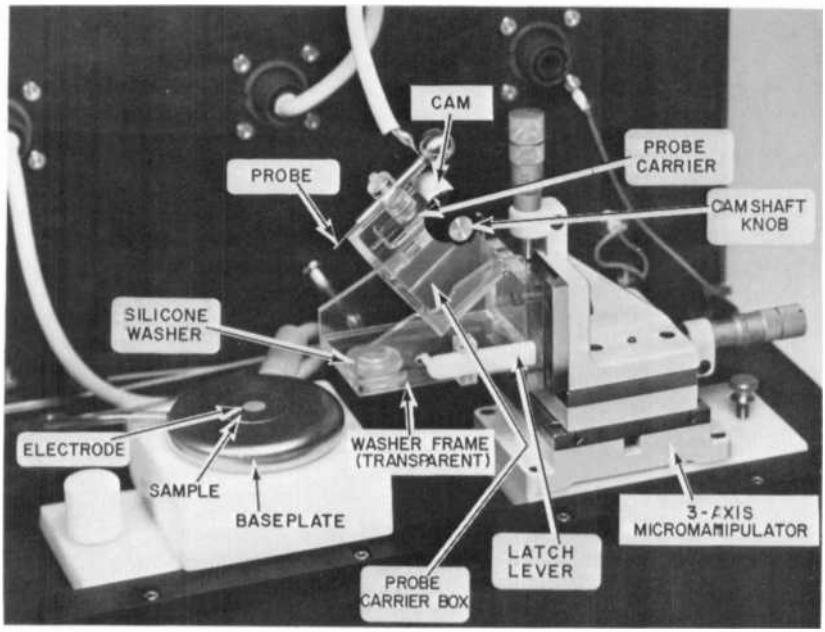

Fig. 2—Oblique view of apparatus. The washer frame is raised; the baseplate is moved to the side; and the probe-carrier box is partially raised on its hinge for visual clarity.

that the rubber contain no voids in the vicinity of the critical region and that it have both a very high resistivity and a low dissipation factor. The technique includes a means for pressing the washer uniformly and controllably over the surface of the sample. Washers molded from two silicone compounds have been used successfully, Dow Corning Sylgard #182 and #186. It has been found that a thin coating of silicone grease on the surface of the washer in contact with the sample gives even more reliable protection against breakdown than using just the washer alone.

Photographs of one version of the apparatus used for implementing the technique are shown in Figs. 2, 3, and 4.

In Fig. 2 an oblique view of the apparatus is shown. The washer frame has been raised and the baseplate has been moved to the side for visual clarity. The silicone washer is held in a recessed hole that has been counterbored in the bottom of the washer frame. The probe carrier box is shown unlatched and partially raised on its hinge. In Figs. 3 and 4, the sample is shown in place with the washer frame lowered and the washer pressed firmly against the sample.

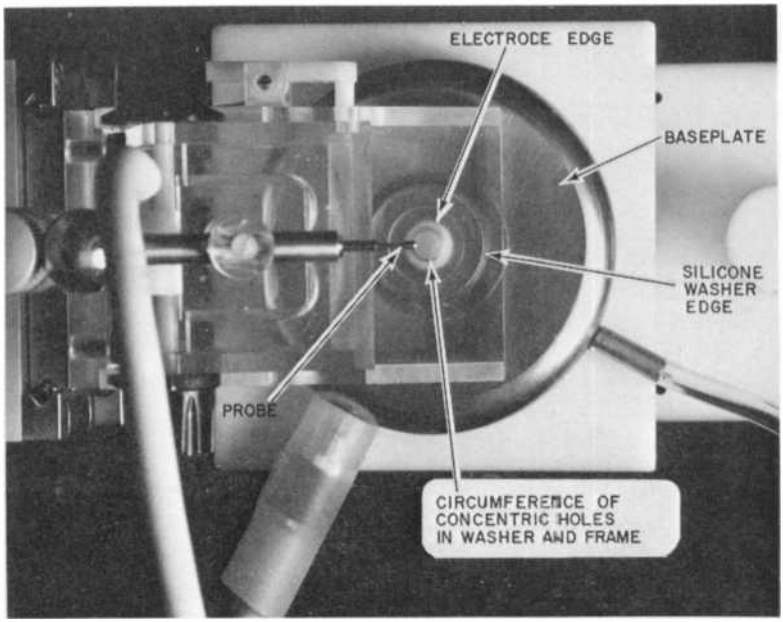

Fig. 3—Overhead view of apparatus with sample in place and probe-carrier box in extreme upward position.

2.2. Operation

In operation, the baseplate with the sample mounted on it is slid under the washer frame, and the two horizontal-axis micromanipulators are adjusted to make the washer concentric with the edge of the electrode on the sample. Both the washer and washer frame are transparent allowing this adjustment to be made quickly and easily. During this adjustment, the probe carrier box is swung up as far as it can go to allow the operator maximum visibility (see Fig. 3). The vertical-axis micro-

manipulator is then used to move the washer frame down, pressing the washer against the sample.

It is important that the washer be pressed against the sample hard enough to fill any air spaces or voids at the sample surface. This pressure extrudes the washer slightly as can be seen in Figs. 3 and 4.

The probe carrier box is then swung down and latched in place. The probe can then be lowered through the concentric holes in the washer and frame to make contact with the electrode. This is accomplished by

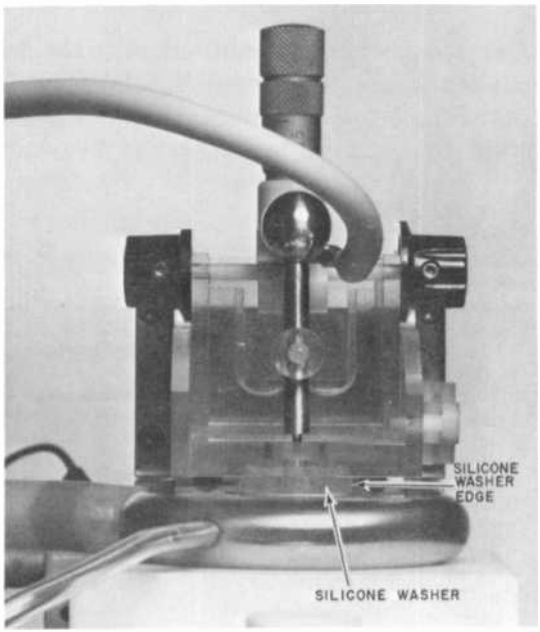

Fig. 4—Side view of apparatus with silicone washer pressed firmly against sample and probe lowered to contact sample electrode.

turning either of the two cam-shaft knobs, thereby rotating the cam against the probe carrier and forcing it down. The probe has a spring-loaded retractable tip to provide a reliable contact to the evaporated electrode on the sample without damaging it.

3. Experimental Results

The use of the technique described in the preceding section has virtually eliminated dielectric breakdown during MIS C(V) measurements at applied-bias voltages up to 12 kV across 150-μm-thick sapphire wafers.

In addition, further tests were carried out at higher voltages. A 125-μm-thick sapphire wafer was tested to breakdown at 16 kV. One 350-μm-thick sapphire wafer was tested without breakdown up to 30 kV, which was the approximate limit of our test capability.

In summary, a new, simple, easy-to-use technique for suppressing premature dielectric breakdown during high voltage C(V) measurements has been described. The technique allows the use of a much larger applied-bias voltage than was previously possible.

Acknowledgments

I am indebted to J. D. Morgan for his contributions to the design and construction of some of the essential hardware, to N. Capone, Jr. for drafting the plans of the apparatus described in this report, and to J. M. Breece for his help with the sample preparation and measurements.

References

[1]A. M. Goodman, "A Useful Modification of the Technique for Measuring Capacitance as a Function of Voltage," *IEEE Trans. Electron Devices*, **ED 21**, p. 753–757 (1974).

[2]A. M. Goodman, "An Investigation of the Silicon-Sapphire Interface Using the MIS Capacitance Method," *IEEE Trans. Electron Devices*, **ED-22**, p. 63–65 (1975).

[3]C. G. Garton, *Intrinsic and Related Forms of Breakdown in Solids, High Voltage Technology*, L. L. Alston, Ed., pp. 144–157, Oxford University Press, London, (1968).

[4]A. M. Goodman, "Semiconductor Measurement Technology: Safe Operation of Capacitance Meters Using High Applied-Bias Voltage," *NBS Special Publication 400-34 (Dec. 1976); also, RCA Review*, **37**, p. 491 (1976).

Photoelectroluminescence of $ZnS:TbF_3$

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Abstract—Optical generation of electron–hole pairs under an electrode causes a polarity-dependent enhancement of electroluminescence (EL) in $ZnS:TbF_3$. When holes are driven into the bulk of the ZnS, the optical enhancement of the EL is multiplicative; when holes are extracted from the bulk, the enhancement is additive.

1. Introduction

The purpose of the following experiment is to observe the influence of optically generated electron–hole pairs on the electroluminescence (EL) of the ZnS layer. Previous experiments have shown that EL in $ZnS:TbF_3$ results from the impact excitation of Tb-related centers.[1,2] Clearly, different results should be obtained, depending on the polarity of the applied voltage. When the pairs are generated near a cathode, holes can escape from the ZnS, whereas pair generation near an anode enhances hole trapping.

2. Experimental

A thin transparent layer of cermet was interposed between the sputtered $ZnS:TbF_3$ layer ($\sim$1 μm thick) and a transparent Al electrode (inset of Fig. 1). In_2O_3 formed the other electrode on the opposite side of the ZnS film. The high resistivity cermet was introduced to homogenize the current distribution and thus to prevent the formation of local spots of high current density that result in burnout.

A He-Cd laser provided the UV excitation (3.8 eV) through the Al dot, producing the photoluminescence characteristic of ZnS:TbF_3. The luminescence was detected by a photomultiplier (RCA 31025) that viewed the Al electrode through a narrow pass filter that transmitted the Tb emission. The photoluminescence was two orders of magnitude lower than the lowest level of electroluminescence shown in the data to be

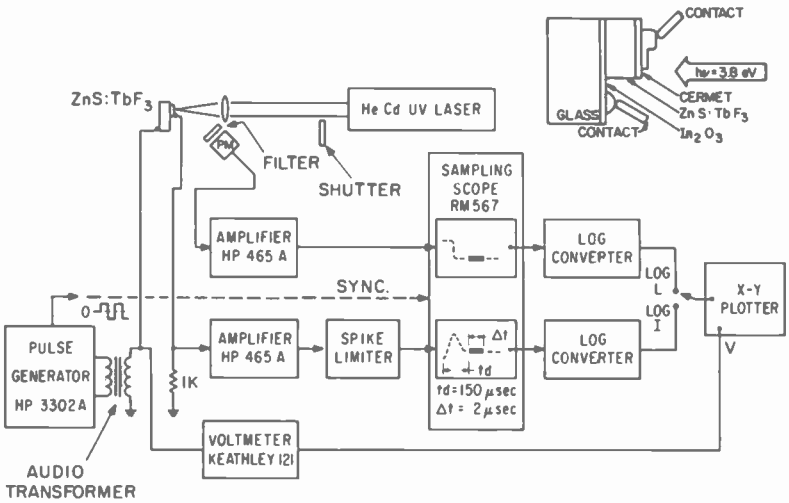

Fig. 1—Experimental set up for the study of PEL. Inset shows the structure of the EL cell.

presented below. Note that the photoconductivity spectrum and the excitation spectrum for photoluminescence are similar, which is not surprising since they both result from optical excitation across the energy gap.

The use of a bias across the layer resulted in polarizing effects and great susceptibility to burnout. To eliminate these effects and to get reproducible results, it was found convenient to apply the voltage in the form of an ambipolar square wave. At each polarity reversal, a large displacement current flows consisting of a gradual, but fast, rise as the ZnS depolarizes and then an equally fast decay as the ZnS repolarizes; this is followed by a slow decay. Light emission begins only after the depolarization reaches a plateau and then gradually decays. It is during this plateau period that all the observations reported here were made. Fig. 2 shows the time dependence of current and light with and without

UV excitation. The UV enhancement of EL, or photoelectroluminescence (PEL), is evident.

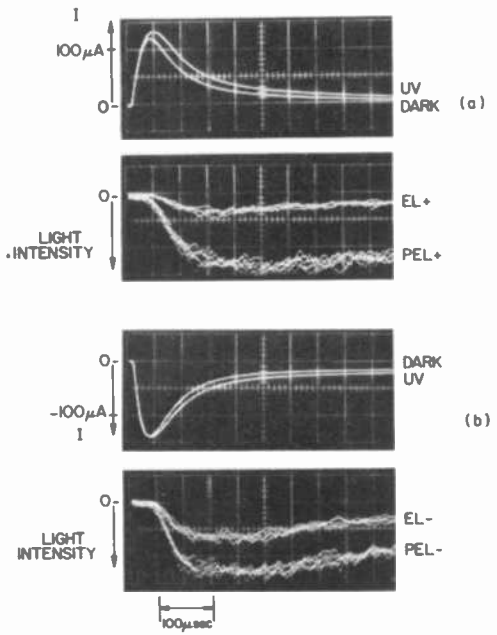

Fig. 2—Expanded views of current (top traces) and light intensity (lower traces) signals with and without UV irradiation: (a) positive bias, (b) negative bias.

3. Results and Discussion

This enhancement was studied by means of a sampling system (Fig. 1) which measured the light intensities, L(V), (under both biasing polarities) in a 2μsec window on the luminescence plateaus (Fig. 2). The logarithmic values of these two quantities were plotted versus the amplitude of the applied voltage. Figs. 3 and 4 show the recorded L(V) characteristics obtained in overlapping ranges of data.

When the Al electrode is positive, the EL is enhanced in a multiplicative fashion (curve translation along the log scale). When the Al electrode is negative, the enhancement decreases with increasing bias—an additive effect.

The electron–hole pairs are generated near the front surface of the ZnS, under the Al electrode, within one UV penetration depth (~2 ×

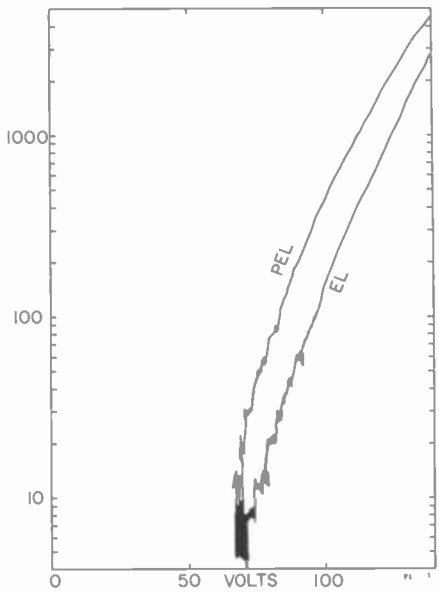

Fig. 3—EL(V) and PEL(V) dependences when the aluminum electrode is biased positively.

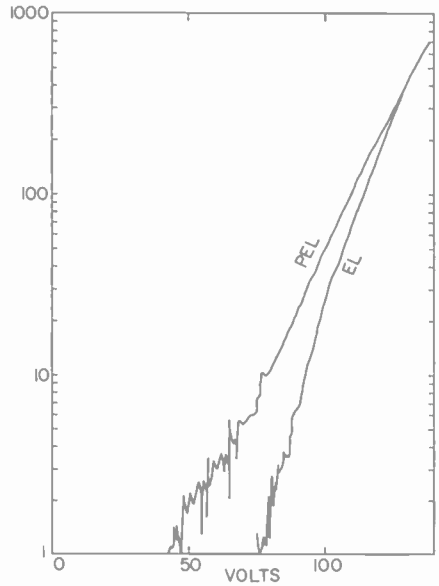

Fig. 4—EL(V) and PEL(V) dependences when the aluminum electrode is biased negatively.

10^{-5} cm). When the Al electrode is positive, the electric field drifts the holes into the ZnS:TbF_3. The holes are trapped, forming a positive space charge that increases the electric field near the cathode, thus increasing the impact excitation rate. Since the photoluminescence is two orders of magnitude lower than the lowest observed EL, the trapping of holes at Tb, or Tb-related centers does not, in itself, lead to significant radiative recombination. It leads to a nonradiative recombination which has not, to date, been analyzed. In the absence of UV illumination, the emission intensity is controlled by a steep function of applied voltage.

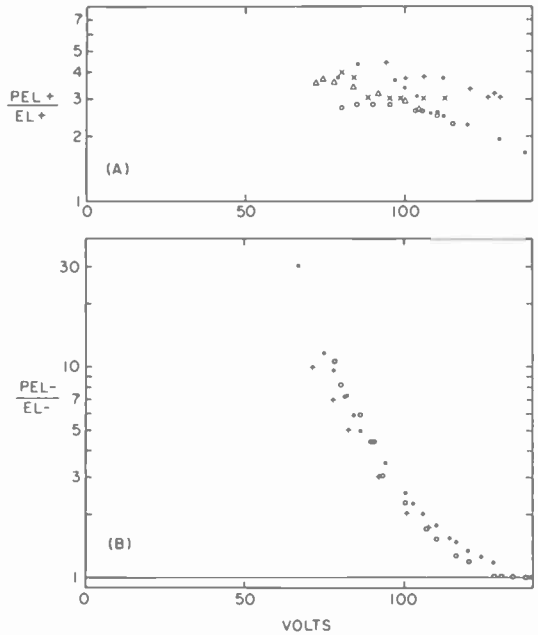

Fig. 5—Enhancement ratio PEL(V)/EL(V): (a) when the aluminum is positive, (b) when the aluminum is negative. (Different symbols represent measurements on different cells.)

The field enhancement by the UV flux, originating in charge trapping effects, appears to have a multiplicative effect on the luminescence intensity. The data of Fig. 5a shows a nearly constant enhancement by a factor of 3 for the experimental conditions used.

When the aluminum is negative, the electric field drives the holes out of the ZnS. The number of electrons at the cathode is proportional to the UV flux at low voltages and increases at high voltages until it becomes

dominated by the tunneling current, whereupon the ratio of PEL to EL tends to one, as seen in Fig. 5b. Note that PEL_- is observed at voltages much lower than those required to observe EL_-. This is presumably owing to the fact that UV excitation populates the conduction band and thus permits impact excitation before tunneling from the cathode becomes appreciable.

In conclusion, we have shown that optical injection of holes in ZnS:TbF_3 in the PEL experiment, greatly enhances the EL when the polarity of the bias is such as to drive the holes into the bulk. With the opposite polarity, the EL enhancement decreases with increasing bias.

References

[1] D. Kahng, "Electroluminescence of Rare-Earth and Transition Metal Molecules in II–VI Compounds Via Impact Excitation," *Appl. Phys. Letters*, **13**, p. 210 (1968).

[2] J. I. Pankove, M. A. Lampert, J. J. Hanak and J. E. Berkeyheiser, *J. Luminescence*, to be published.

Note added in proofs:

Earlier studies of photoelectroluminescence in ZnS:Mn can be found in:

B. Gudden and R. Pohl "Über elektrische Leitfähigkeit bei Anregung und Lichtemission von Phosphoren," *Z. Physik*, **21**, p. 1, (1924).

D. A. Cusano and F. E. Williams "Photoelectroluminescence-Electroluminescence Controlée par les Radiations," *J. Physique et le Radium*, **17**, p. 742 (1956).

R. Taagepera and F. Williams "Photoelectroluminescence of Single Crystals of Manganese-Activated Zinc Sulfide," *J. Appl. Phys.*, **37**, 3085 (1966).

Recent Papers by RCA Authors

Listing is alphabetical by name of primary author. For copies of reprints, the reader should contact the publication directly.

R. C. Alig and S. Bloom, "Cathodoluminescent Efficiency," **J. Electrochem. Soc.**, Vol. 124, No. 7, p. 1137, July 1977.

A. E. Bell, "Thermal Analysis of Single-Crystal Silicon Ribbon Growth Processes," **RCA Review**, Vol. 38, No. 1, p. 109, March 1977.

A. Bloom and E. B. Priestley, "Criteria for Evaluating Pleochroic Dye Liquid-Crystal Displays," **IEEE Trans. Electron Devices**, Vol. 24, No. 7, p. 823, July 1977.

A. Bloom, R. A. Bartolini, and P. L. K. Hung, "The Effect of Polymer Host on Volume Phase Holographic Recording Properties," **Polymer Engineering and Science**, Vol. 17, No. 6, June 1977.

D. E. Carlson, C. R. Wronski, J. I. Pankove, P. J. Zanzucchi, and D. L. Staebler, "Properties of Amorphous Silicon and a-Silicon Solar Cells," **RCA Review**, Vol. 38, No. 2, p. 211, June 1977.

R. B. Comizzoli, "Nondestructive, Reverse Decoration of Defects in IC Passivation Overcoats," **J. Electrochem. Soc.**, Vol. 124, No. 7, p. 1088, July 1977.

A. H. Firester, M. E. Heller, and P. E. Sheng, "Knife-Edge Scanning Measurements of Sub-Wavelength Focused Light Beams," **Appl. Optics**, Vol. 16, p. 1971, July 1977.

H. Fujita and K. Ametani, "Melting of a Latex Colloidal Crystal as a Function of Particle Packing Fraction," **Japanese J. Appl. Phys.**, Vol. 16, No. 7, p. 1091, July 1977.

A. M. Goodman and C. E. Weitzel, "The Effect of Electron-Beam Aluminization on the Si-Sapphire Interface," **Appl. Phys. Lett.**, Vol. 31, No. 2, p. 114, July 15, 1977.

L. A. Goodman, J. T. McGinn, C. H. Anderson, F. DiGeronimo, "Topography of Obliquely Evaporated Silicon Oxide Films and Its Effect on Liquid-Crystal Orientation," **IEEE Trans. Electron Dev.**, Vol. 24, No. 7, p. 795, July 1977.

R. J. Himics and D. L. Ross, "The Examination of Poly(5-Hexene-2-one Sulfone) as a Positive-Working Photoresist," **Polymer Engineering and Science**, Vol. 17, No. 6, June 1977.

R. J. Himics, M. Kaplan, N. V. Desai, and E. S. Poliniak, "The Synthesis, Characterization, Evaluation, and Processing of Selected Cyclo-Olefin Sulfone Copolymers as Electron Beam Resists," **Polymer Engineering and Science**, Vol. 17, No. 6, June 1977.

S. T. Hsu, "Drain Characteristics of Thin-Film MOS FET's," **RCA Review**, Vol. 38, No. 1, p. 139, March 1977.

S. T. Hsu, "Electron Trapping Noise in SOS MOS Field-Effect Transistors Operated in the Linear Region," **RCA Review**, Vol. 38, No. 2, p. 226, June 1977.

A. C. Ipri, "Lambda Diodes Utilizing an Enhancement-Depletion CMOS/SOS Process," **IEEE Trans. Electron Dev.**, Vol. 24, No. 6, p. 751, June 1971.

S. Jen, N. A. Clark, P. S. Pershan, and E. B. Priestley, "Polarized Raman Scattering Studies of Orientational Order in Uniaxial Liquid Crystalline Phases," **J. Chem. Phys.**, Vol. 66, No. 10, p. 4635, May 15, 1977.

I. Ladany, "The Influence of Stripe Width on the Threshold Current of DH Lasers," **J. Appl. Phys.**, Vol. 48, No. 5, p. 1935, May 1977.

L. S. Napoli, G. A. Swartz, S. G. Liu, N. Klein, D. Fairbanks, and D. Tamutus, "High Level Concentration of Sunlight on Silicon Solar Cells," **RCA Review**, Vol. 38, No. 1, p. 76, March 1977.

R. U. Martinelli and E. Jetter, "The Effects of Emitter Impurity Concentration on the High-Current Gain of Silicon n-p-n Power Transistors," **RCA Review**, Vol. 38, No. 1, p. 60, March 1977.

A. Okada, "Some Electrical and Optical Properties of Ferroelectric Lead-Zirconate-Lead-Titanate Thin Films," **J. Appl. Phys.**, Vol. 48, No. 7, p. 2905, July 1977.

G. H. Olsen and M. Ettenberg, "Calculated Stresses in Multilayered Heteroepitaxial Structures," **J. Appl. Phys.**, Vol. 48, No. 6, p. 2543, June 1977.

A. Pierrefeu, E. F. Steigmeier, and B. Domer, "Inelastic Neutron Scattering in SbSI Near the Ferroelectric Phase Transformation," **Phys. Stat. Sol. (b)**, Vol. 80, p. 167, 1977.

A. Rosen, H. J. Wolkstein, J. Goel, and R. L. Matarese, "A Dual-Gate GaAs FET RF Power Limiter," **RCA Review**, Vol. 38, No. 2, p. 253, June 1977.

A. Rosen, D. Mawhinney, and L. S. Napoli, "A Novel FET Frequency Discriminator," **RCA Review**, Vol. 38, No. 2, p. 238, June 1977.

F. N. Sechi and R. W. Paglione, "Design of a High-Gain FET Amplifier Operating at 4.4–5.0 GHz," **Solid State Circuits**, Vol. 12, No. 3, p. 285, June 1977.

S. Roth, W. Rehwald, and H. Mallle, "Acoustic Soft Modes of Nb_3Sn in High Magnetic Fields," **Solid State Communications**, p. 177, 1977.

P. Sheng and B. Abeles, "Temperature Dependence of the Electrical Conductivity of Granular Metal Films," **Thin Solid Films**, Vol. 41, p. L39, 1977.
E. K. Sichel, J. I. Gittleman, and J. Zelez, "Electrochromism in the Composite Material Au-WO_3," **Appl. Phys. Lett.**, Vol. 31, No. 2, p. 109, July 15, 1977.
H. S. Sommers, Jr., "Performance of Injection Lasers with External Gratings," **RCA Review**, Vol. 38, No. 1, p. 33, March 1977.
T. Takahashi and O. Yamada, "Cathodoluminescent Properties of Yttrium Aluminum Borate Yttrium Aluminum Borate $Y_{1-x}Tb_xAl_3B_4O_{12}$ Phosphors," **J. Electrochem. Soc.**, Vol. 124, No. 6, p. 956, June 1977.
M. Toda and S. Osaka, "Surface Acoustic Wave Absorber and Application to Low Spurious Mode SAW Device," **Trans. IECE of Japan**, Vol. E60, No. 5, p. 237, May 1977.
S. Tosima and M. Nishikawa, "Critical Field Variations for Domain-Wall Motion in Ferroelectric/Ferroelastic $Gd_2MoO_4)_3$," **J. Appl. Phys.**, Vol. 48, No. 7, p. 3169, July 1977.
J. Weisbecker, "COSMAC VIP—The RCA Fun Machine," **BYTE**, August 1977.
C. E. Weitzel and R. T. Smith, "Sapphire Substrate Misorientation and SOS/MOS Transistor Performance," **J. Electrochem. Soc.**, Vol. 124, No. 7, p. 1081, July 1977.
J. P. Wittke and I. Ladany, "Lateral Model Selection in Semiconductor Injection Lasers," **J. Appl. Phys.**, Vol. 48, No. 7, p. 3122, July 1977.
P. J. Wojtowicz, "Obituary—Lars Onsager," **Ferroelectrics**, Vol. 15, p. i–iii, 1977.

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J. A. van Raalte Electron Multiplier Image Display Device (4,028,575)
P. K. Weimer Charge Injection Device Arrays (4,032,903)
O. M. Woodward Broadband Turnstile Antenna (4,031,56)

AUTHORS

Marvin S. Abrahams received his Doctorate in Physical Metallurgy from Columbia University in 1958. He has been with RCA Laboratories since 1957. Dr. Abrahams has pioneered in the metallurgy of electronic materials, especially concerning the effects of crystalline imperfections of the electrical and mechanical properties of semiconductors. Most recently, his research has been involved with the relation of microstructure to properties in the silicon-on-sapphire system. In 1965 and 1971 he received RCA Achievement Awards and in 1967 shared in the David Sarnoff Outstanding Team Award for Science. Dr. Abrahams is a member of the American Physical Society, American Institute of Mining, Metallurgical and Petroleum Engineers, Electron Microscope Society of America, American Vacuum Society, and Sigma Xi.

James E. Berkeyheiser served in the U. S. Navy from 1942 to 1948 and from 1950 to 1952. He was with RCA Laboratories from 1948 to 1950, and returned there in 1952. He attended Drexel Evening College, Philadelphia, Pa., receiving his B.S. degree in Electrical Engineering, with an Electronics Option, in 1960. Mr. Berkeyheiser's early work involved flying spot scanners, projection color television, and panel light amplifiers. He has worked on thin silicon carbide films including deposition facilities, spectroscopic measurements, and a variety of specialized equipment for studying thin films. He took part in early work on room-temperature GaAs lasers. He has helped design and construct equipment for cathode luminescence studies down to 4.2° K and for making log-log plots of V-I characteristics of GaN diodes. Most recently, he has been involved in the study of amporphous silicon.

Joseph Blanc received his B.A. in 1954, M.A. in 1955 and Ph.D. in 1959, majoring in Physical Chemistry, all from Columbia University. His research in graduate school dealt with low temperature infrared spectra of molecular crystals. He joined RCA Laboratories in 1959. His research has been largely concentrated in the characterization of defects in semiconductors (GaAs, Si) and insulators ($SrTiO_3$) with occasional returns to molecular spectroscopy (rare-earth chelate lasers, photochromic indigoids). In 1967 he won an RCA Achievement Award for his work on photochromics, and in 1971 a similar award for his research on defects in III-V compounds. He spent the academic year 1974–1975 as a Research Associate at the Laboratoire d'Optique Electrounique, Toulouse, France. He now is focusing on studies, by transmission electron microscopy, of silicon-on-sapphire, and silicon dioxide grown on silicon. He is a member of the American Physical Society and Sigma Xi.

James E. Carnes received the B.S. degree from Pennsylvania State University, University Park, Pa., in 1961, and the M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, N. J., in 1967 and 1970, respectively. His Ph.D. dissertation was an investigation on photoinduced currents and charge transport in polyvinylcarbazole, an organic polymer. He was in the U. S. Navy from 1961 to 1965. During the summers of 1966 and 1967 he investigated metallic contacts and dc electroluminescence in strontium titanate at RCA Laboratories, David Sarnoff Research Center, Princeton, N. J., which he joined as a member of the technical staff in 1969. He has studied electrical breakdown, conduction, and interface properties of various insulating films on silicon. Dr. Carnes was appointed manager of RCA Consumer Electronics Integrated Circuit Development in June 1977. He is a member of the American Physical Society, Tau Beta Pi, Phi Kappa Phi, and IEEE.

Charles J. Buiocchi received his B.A. degree from University College, Rutgers University, New Jersey in 1971. In 1960, he joined Columbian Carbon Research Laboratory, in the paints, inks, and plastics department, working on the development of new products. Mr. Buiocchi joined RCA Laboratories in 1961 as a Research Technician and was appointed a Technical Staff Associate in 1971. He is presently associated with the Materials Research Laboratory and is engaged in the characterization and elimination of defects in silicon on sapphire materials by transmission electron microscopy. His previous activities included characterization and elimination of defects in semiconductors, their alloys, and granular ferromagnetic materials by transmission electron microscopy. He also developed chemical polish and etchant for GaAs, was instrumental in design and testing of the ion-bombardment device for producing thin samples and the beam-tilting apparatus, both necessary for transmission electron miscroscopy. He has worked on light microscopy characterization of semiconductivity measurements, crystal growth (gradient-freeze technique), plastic deformation of III-V and II-VII compounds, and radiation damage.

Yuen-Sheng Chiang received his B.S. degree in Chemical Engineering from National Taiwan University, Taipei, Taiwan, China, in 1956 and M.Ch.E. degree from the University of Louisville, Louisville, Ky., in 1959. In 1964 he was awarded the Ph.D. degree in Physical Chemistry by Princeton University, Princeton, N. J. His thesis research dealt with crystal growth. He served as a consultant to the Research Division of Burroughs Laboratories from 1962 through 1963, and was appointed as a research associate in the Chemistry Department of Princeton University in November 1963, upon completion of his Ph.D. studies. The research he engaged in at Princeton was in the area of electron paramagnetic resonance studies of fast reactions. In 1964 he joined the Fundamental Research Laboratory of Xerox Corporation as a Scientist and was made a Senior Scientist in 1968. He has worked in the field of surface physics and chemistry of solids, ultra-high vacuum technology, and electron microscopy and diffraction studies. Since joining the staff at RCA Laboratories in 1969, he has been in-

volved with low temperature gas phase growth of silicon and silicon microwave devices. He received a joint RCA Achievement Award in 1974 for work on high efficiency, low noise IMPATT. Dr. Chiang is a member of IEEE, American Chemical Society, Electron Microscopy Society of America, Sigma Xi and the Electrochemical Society.

Robert Dawson was awarded the B.S.E.E. degree from Rutgers University in 1963 and the M.S.E.E. from Brooklyn Polytechnic Institute in 1966. He joined the RCA David Sarnoff Research Laboratories in Princeton, N. J., where he entered the RCA Graduate Study and Research Training Program. At the RCA Princeton Laboratories, he worked on the microwave aspects of superconductivity and solid state devices. In 1964, he joined the Technical Programs Laboratory at RCA Solid State Division, Somerville, N. J., working on MOS transistors and integrated circuits. He contributed to the development of the high-frequency MOS dual-gate transistor and MOS linear integrated circuits. He has also investigated low-temperature performance of MOS transistors. Recently he has been an Engineering Leader for Linear MOS and Charge-Coupled Device Technology in the Solid State Technology Center. He has extensively investigated the reliability of buried-channel CCD structures for use in signal processing applications. This work with Si-gate MOS structures has led to the present involvement in C^2L reliability evaluations. He recently received an RCA Laboratories Outstanding Achievement Award for team contributions in CCD signal processing applications. He is a member of Eta Kappa Nu, Tau Beta Pi, and IEEE. Dr. Dawson is recently writing his thesis to complete Ph.D. studies at Cornell University which were started on a David Sarnoff Fellowship.

Edgar J. Denlinger was born in Lancaster, Pennsylvania on June 17, 1939. He received the B.S. degree in Engineering Science from Pennsylvania State University, University Park, Pa., in 1961, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Pennsylvania, Philadelphia, in 1964 and 1969, respectively.

From 1961 to 1963, he was in the RCA Graduate Study Program while working in the RCA Applied Research Department, Camden, New Jersey. Until 1965, he was engaged in research on solid-state traveling wave masers, superconducting magnets, and experimental transistors. From 1965 to 1967, he held a University of Pennsylvania Research Assistantship during which he did research on a bulk-effect oscillator. From 1967 to 1973, he was a Staff Member at Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, working in the areas of microwave integrated circuits, phased array antennas, and air traffic control. Since April 173, he has been a Member of the Technical Staff at RCA Laboratories, Princeton, New Jersey, engaged in research on millimeter wave avalanche diodes, microwave integrated circuits, low loss PIN diodes, and GaAs mixer diodes.

Dr. Denlinger is a member of IEEE, Sigma Xi, Tau Beta Pi, Sigma Tau, and Phi Kappa Phi. He is also a member of the Editorial Board for the IEEE Transaction on Microwave Theory and Techniques.

Alvin Malcolm Goodman received a B.S.E. in 1952 from the Drexel Institute of Technology, Philadelphia, Pa. He did graduate work at Princeton University, receiving an M.A. in 1955 and a Ph.D. in 1958. From June 1956 to January 1957 he served as Research Assistant at Princeton University, and then as Assistant Professor of Electrical Engineering at the Case Institute of Technology up to June 1959. He performed research at RCA Laboratories as a summer employee in 1954, 1955, and 1958. He has been a Member of the Technical Staff since June 1959. During the year 1970–71, Dr. Goodman engaged in postdoctoral studies at the Swiss Federal Institute of Technology. Dr. Goodman has specialized in solid-state physics. His thesis subject was "December Effect and Trap Levels in Silver Chloride," and he has worked extensively in the areas of photoconductivity, metal-semiconductor contacts, metal-insulator contacts, insulator properties, and tunnel diodes. He has received two RCA Laboratories Achievement Awards for work on metal-semiconductor contacts (1963) and MNOS (metal-nitride-oxide-silicon) memory devices (1969). Dr. Goodman is a member of the American Physical Society, Sigma Xi and the Institute of Electrical and Electronics Engineers.

William E. Ham received the B.S. and M.E. (electrical engineering) degrees from the University of Oklahoma, at Norman, both in 1966, and the Ph.D. degree in electrical engineering from Southern Methodist University, Dallas, Texas, in 1970. Since graduation he has been a Member of the Technical Staff at RCA Laboratories. His primary work has been with electrical characterization and MOS device properties of heteroepitaxial semiconductors for integrated circuit applications. His research has involved the effective use of various types of vehicles, testing, and data presentation for the optimal understanding of integrated circuit processes. Specifically, this involves the study of electrical instabilities and dielectric properties, correlation of physical structure with electrical performance, and spatial distribution of device parameters. Current studies also include dimensional instabilities of wafers and photomasks and analysis of circuit yield distributions.

Dr. Ham is a member of the Electrochemical Society, Sigma Xi, Eta Kappa Nu, Sigma Tau, and Tau Beta Phi.

Joseph J. Hanak received his B.S. in Chemistry at Manhattan College in 1953, his M.S. in Physical Chemistry at the University of Detroit in 1956, and his Ph.D. in Physical Chemistry at Iowa State University in 1959. He worked for the Ethyl Corporation in 1955, and was a Research Assistant at the AEC Institute for Atomic Research, Ames, Iowa, from 1955 to 1959. He has been a member of the technical staff at RCA Laboratories since 1959 and was appointed a Fellow of the Laboratories in 1971. Dr. Hanak's field of interest is the synthesis and characterization of electronically active materials. His materials studies have included such areas as rare earth elements, superconductors, ferrites, magnetic recording heads, dielectrics, ultrasonic delay lines, electrophotography, electroluminescence, displays, and metals and

dielectrics for video recording. He received three RCA Laboratories Achievement Awards for his work on the vapor deposition process for the superconductor Nb_3Sn, single-crystal ferrite recording heads, and ultra-high-frequency microwave ultrasonic transducers. He also received the David Sarnoff Award and the John Roebling ASM Award for his work on superconductivity. More recently, he has introduced novel methods of co-sputtering, compositional analysis, and materials testing that greatly increase productivity in materials research.

Dr. Hanak is a member of the American Vacuum Society, SID, Phi Lambda Upsilon, and Sigma Xi.

Alfred C. Ipri received a B.S. degree from Drexel Institute of Technology in 1965 and an M.S. in Electrical Engineering and a Ph.D. from the University of Pennsylvania in 1967 and 1972 respectively. Since joining the technical staff at RCA Laboratories, Princeton, N. J., in 1967, he has been involved in materials utilization, process development, device characterization, circuit design, and systems applications in the field of integrated circuits and this work has led to numerous presentations, publications and patents.

Dr. Ipri is a member of Eta Kappa Nu, the Institute of Electrical and Electronic Engineers, and the National Society of Professional Engineers.

Murray A. Lampert received the B.A. degree in mathematics and the M.A. degree in physics, both from Harvard University, Cambridge, Mass., in 1942 and 1945, respectively. He has been with the Optical Research Laboratory of Harvard University, the Radiation Laboratory of the University of California, and the Federal Telecommunications Laboratories. He was with RCA Laboratories, Princeton, N. J., from 1952 to 1966. In 1966 he became a Professor of Electrical Engineering at Princeton University, Princeton, N. J. He has done theoretical work on the electronic physics of insulators and semiconductors with particular emphasis on injection current in insulators, and bulk microwave effects in solids. He is presently studying biology and psychology.

Mr. Lampert is a fellow of the American Physical Society.

Jacques I. Pankove obtained his B.S. (1944) and M.S. (1948) degrees from the University of California and a doctorate from the University of Paris (1960). He joined the RCA Laboratories in 1948 where he has made many contributions to the understanding, technology and evolution, of various semiconductor devices, including large-area photocells, transistors, tunnel diodes, injection lasers and LED's. Dr. Pankove, a Fellow of RCA's Technical Staff, is a member of the American Association for the Advancement of Science, Sigma Xi, and Fellow of both the American Physical Society and Institute of Electrical and Electronics Engineers. He is an

associate editor of the Journal of Quantum Electronics and a member of the editorial board of Solid State Electronics.

Joseph O. Preisig received the electrical engineering degree from Oskar von Miller Polytechnium in Munich, Germany, in 1937, and in 1948, he obtained the Diplom-Engineer degree from the Technical University of Berlin. From 1948 to 1950, he was employed as technical assistant to Professor Leithauser at the Technical University of Berlin. From 1950 to 1951, Mr. Preisig was employed by Leonard Electrical Products in New York as electrical engineer for the design of electronic test equipment for the production line. In 1951, Mr. Preisig joined RCA Laboratories in Princeton, N. J., where he worked on the development of TV receiver circuits. In 1963, he transferred to RCA Astro Electronics in Hightstown, N. J., working on the development of electronic spacecraft circuits. In 1964, he moved to RCA Solid State Division, Somerville, N. J., to work on semiconductor applications. This work included MOS rf, small-signal, and power applications, horizontal deflection circuits, and laser pulse power supplies. Mr. Preisig has been responsible for reliability investigations of CCD structures and has investigated applications of CCDs to signal processing in video and communication systems.

J. I. Pridgen received the B.E.E. degree from the University of Virginia in 1964, and the M.S.E.E. degree from Georgia Institute of Technology in 1971. After being employed by Lockheed-Georgia Company from 1967 to 1970, Mr. Pridgen joined RCA in 1971 on the Graduate Rotational Program and was assigned to the Advanced Technology Laboratories in February 1972. Since joining RCA he has been involved primarily in the design, layout, and testing of bulk CMOS and CMOS/SOS arrays. Mr. Pridgen has had design responsibility for a number of custom cell CMOS/SOS arrays including an 8-bit X 8-bit plus sign mutliplier, a 32-stage correlator, a 19-stage sequence generator, a dual 9-stage retimer, a floating point logic array for an FFT arithmetic unit, and an expandable programmable 16-stage pseudorandom sequence generator. Mr. Pridgen was project engineer having complete design responsibility for the Saville Pipeline Key Generator bulk CMOS array. He also performed the design and layout of a Barker Code Correlator array incorporating CMOS and CCDs on the same substrate. Recent responsibilities include the logic design of a DCT (discrete cosine transform) and DPCM (differential pulse code modulation) subsystem for use in a video bandwidth reduction system based upon CMOS/SOS LSI, and the design of a radiation hardened CMOS/SOS LSI, code generator for the Global Positioning Satellite.

Mr. Pridgen is a member of Tau Beta Pi and Eta Kappa Nu.

J. C. Sarace recieved the B.S.E. degree in metallurgy in 1960 from the University of Michigan, Ann Arbor.

Since graduation he has been engaged in research and development activities in the semiconductor device and device processing field. While employed at Bell Laboratories he worked on compound semiconductor technology, namely, gallium arsenide injection luminescence and related device phenomenon. In addition he was instrumental in pioneering silicon gate technology for MOS applications. More recently at David Sarnoff Laboratories, Princeton, NJ, he has worked in the area of LSI processing utilizing silicon-on-sapphire substrate material. Currently, he is employed by Rockwell International, Anaheim, CA, and is engaged in LSI process development for military applications. He holds numerous patents on IC processing and novel device structures and has presented and published technical papers covering a wide variety of related work.