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RCA REVIEW

BOARD OF EDITORS

NEW PROCESS TECHNOLOGIES FOR MICROELECTRONICS

Foreword

Innovation and technological change are hallmarks of the electronics industry, especially in the fabrication of solid-state devices. Although silicon transistors today do not differ significantly in concept from those of a decade ago, striking advances have been made in their performance and reliability. In particular, the ability to prepare solid-state devices with high yields has steadily improved, leading to the fabrication of multitransistor silicon chip circuits of the "medium-scale integration" (MSI) and "large-scale integration" (LSI) variety. These increases in yield can be traced back directly to refinements and invention in the *processing* of semiconductor devices and their interconnections.

With the advent of additional new processing methods, still further increases in the yield, reliability, performance, and sophistication of solid-state arrays can be anticipated. Furthermore, as the techniques and concepts used in manufacturing transistors are introduced into other areas of electronic device fabrication, greatly improved electronic systems at significantly lower cost will become available. To investigate new processes potentially useful in electronic applications, the Process Research and Development Laboratory was set up at RCA's David Sarnoff Research Center in 1963. Ten of the papers in this issue of the RCA Review are based on the results of investigations carried out in that laboratory.

The first seven papers describe processes useful for fabricating improved silicon integrated circuits. The processing techniques employed are hot-pressing, chemical vapor deposition, and etching; the technologies involved are, respectively, dielectric isolation for monolithic circuits, more controllable diffusion sources, and the characterization of glass layers on a silicon substrate.

The next three papers deal with the interconnection of silicon chips into arrays, with or without additional passive components. Here the processing techniques include rf sputtering, electroless and electrodeposition of metals, offset printing, and hot-pressing.

The last two papers in this issue, both dealing with improved methods for fabricating semiconductor devices, are contributions from the Electronic Components devision of RCA. Chemical vapor deposition is the processing technique common to the two papers, the first being

a study of a particular process and the second illustrating an application of the technique.

The processes described in these twelve papers are based on chemistry, physics, metallurgy, ceramics technology, and computer programming. Just as for other issues of the RCA Review devoted to a single topic, i.e., the series of papers on "Epitaxial Growth" published in December 1963, the advances described here represent an interweaving of a variety of disciplines to effect a desired result. They thus illustrate once again the power of an interdisciplinary approach to research and the benefits to be gained by providing an environment in which scientists of different backgrounds can interact cooperatively and fruitfully.

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ISOLATION TECHNIQUES FOR FABRICATING INTEGRATED CIRCUITS

I. LAMINATE SUBSTRATES

By

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Summary—*Substrates comprising silicon regions separated from one another by a silicon dioxide or ceramic dielectric can readily be prepared by lamination in a hot press. The preparation of these substrates is described in detail and their properties are discussed briefly. These substrates are potentially useful for the fabrication of diode arrays or for arrays of MOS field-effect transistors.*

Introduction

THE FABRICATION of monolithic integrated circuits containing arrays of individual devices requires that the devices be electrically isolated from one another prior to metallization. Conventionally, this isolation is accomplished by forming "bathtub" junctions surrounding each device. When these junctions are reverse biased, the depletion layer serves as an insulator region. Improvements can be made in the electrical performance of arrays if the depletion layers are replaced by a true dielectric material. If this dielectric is sufficiently refractory, chemically inert, and a good enough match to silicon in thermal expansion, the isolated substrate can be processed in the same way as convential monolithic silicon substrates.

A variety of techniques have been successfully used to fabricate isolated arrays. One involves the lamination of slices of silicon under high temperature and pressure, using a high-melting-point dielectric as a cement. The substrates derived from this process are designated "laminate substrates."

Experimental

The processing sequence employed in the preparation of laminate substrates is similar to that described by Naymik.[1] Ideally, however,

[1] D. A. Naymik, "Silicon Mosaic for Integrated Devices," *IEEE Trans. on Electron Devices*, Vol. ED-12, p. 497, Sept. 1965.

a higher-temperature, higher-resistivity dielectric than the germanium–silicon oxide used by Naymik would be required, especially if the finished substrates are to undergo standard silicon processing, such as diffusion. Cave has found[2] that steam-grown silicon oxide layers, about 2 microns thick, serve as a satisfactory bonding medium if the oxidized wafers are pressed together at about 1250°C for perhaps 10 minutes at 2000 psi. If the pressing is conducted in vacuum, gas inclusions are minimized and a stack of wafers can be joined together into a rugged, monolithic block of material. On slicing through this block, wafers of silicon bars are obtained, each bar being electrically separated from, and bonded to, its neighbors by a thin, coherent silicon dioxide strip.

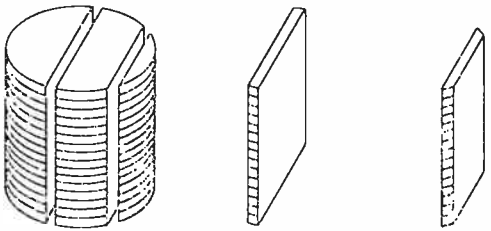

Fig. 1—Laminated block prepared from circular wafers and slices cut from this block.

Materials and Processing

Conventional (111) oriented silicon wafers were originally used in the preparation of laminated blocks. These nearly circular wafers have two principal disadvantages, however. Perhaps the most serious is the varying size of the slices that can be cut from such a block (Figure 1). Although all slices have one dimension in common (corresponding to the height of the block), the second dimension depends on whether the slice is cut from the edge or from the center of the block. Furthermore, in a crystal, the sets of (111) planes do not lie at right angles to one another. Therefore, it is not possible to cut perpendicularly through a (111) plane and end up with a newly exposed surface that also has (111) orientation. Since many factory processing steps have been designed for (111) oriented wafers, it was desirable to retain this orientation in the final substrate. If (100) oriented surfaces are desired, the crystal symmetry simplifies the preparation of substrates by this method.

[2] E. F. Cave, U. S. Patent 3,290,760 issued December 13, 1966; c.f. also J. A. Amick, U. S. Patent 3,354,354 issued November 31, 1967.

Both these disadvantages can be overcome by using rectangular wafers of silicon of appropriate orientation as starting materials. As shown in Figure 2a, a rectangular block 0.75 × 0.875 inch is first cut from a silicon boule. The orientations of the sides of this block are not critical, but the faces can conveniently be made (211) and (110) planes. The block is now sliced parallel to one of these two planes to give wafers 0.75 × 0.875 inch in area and having any desired thick-

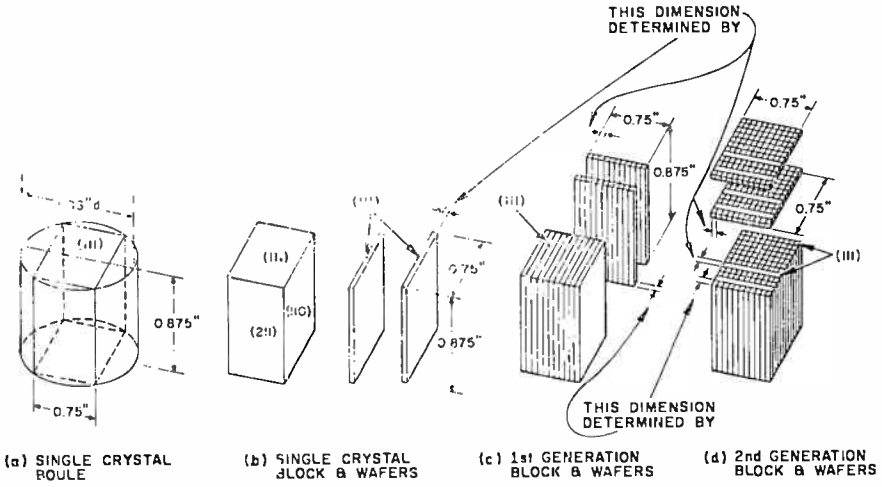

Fig. 2—Preparation of laminate substrates from rectangular silicon wafers.

ness. The ends of these slices are (111) planes (Figure 2b). Using oxidized wafers cut from several blocks, one can assemble a stack 0.75 inch high (Figure 2c). Following lamination and slicing, one then obtains "first-generation" substrates all identical in size, namely 0.75 × 0.875 × whatever thickness is chosen for the slice (Figure 2c). Since the two major dimensions for these first-generation slices are the same as for original slices, a "second-generation" block can be prepared from any combination of silicon slices and first-generation wafers. On slicing the second-generation block, one obtains substrates that are all the same size and in which each exposed silicon area is a (111) plane (Figure 2d).

The dimensions of the original block cut from the silicon boule are not critical. For the silicon boules normally available, i.e., 1.125 inches in diameter, a 0.75 × 0.75 inch (111) face is about as large as can be cut without rounding the edges of the block. By making the third dimension of the block longer (or shorter) than the other two, the

(111) end of the slices can readily be identified. When single-crystal slices and first-generation slices are assembled into a stack, it is then easy to remember how the stack should be sliced to give (111)-surface substrates.

For some applications, dielectric layers thicker than can be obtained with thermal oxides are desired. For this purpose, wafers of a suitable thermal-expansion-matching ceramic, such as Pyroceram† 9606, can be employed. This material is available in the recrystallized form and can be cut into suitably shaped wafers and polished. Again, thermal oxide, grown in steam, forms a satisfactory cement for bonding a silicon wafer to a Pyroceram wafer.

Composite substrates, either of silicon and silicon dioxide, or those including Pyroceram regions, can be satisfactorily polished with Lustrox,* an alkaline zirconium oxide slurry. Following polishing, very smooth surfaces are obtained in which the silicon regions have minimal work damage. Step-height differences, going from the Pyroceram to the silicon are less than 1 micron following Lustrox polishing.

Substrate Arrangement

Since each layer included in the preparation of a laminate can be a silicon wafer of different resistivity or resistivity type or a Pyroceram wafer, and since the thickness of all wafers is optional, a wide variety of first-generation (bar) substrates is possible. If slices from several different first-generation blocks are incorporated into a second-generation block, along with a variety of single-crystal silicon slices, almost any desired geometrical arrangement of silicon regions and Pyroceram regions can be obtained, with any desired resistivity and resistivity type for the silicon in any location. The dimensions of a given region are determined by (a) the thickness of the original wafer and (b) the thickness of the first-generation slice used to prepare the block (Figure 3). The only limitation, then, is that all areas must be either square or rectangular in outline. However, it is not necessary that any two adjacent areas be the same size.

Typical examples of laminate substrates prepared as described above can be seen in Figures 4 and 5. Figure 4 shows a simple silicon–silicon-dioxide laminate constructed of p-type and n-type wafers, some 0.025 and some 0.050 inch thick. The resultant isolated-bar configuration is suitable for forming ladder arrays of complementary MOS transis-

† Corning Glass Works, Corning, New York.
* Tizon Chemical Corp., Flemington, N. J.

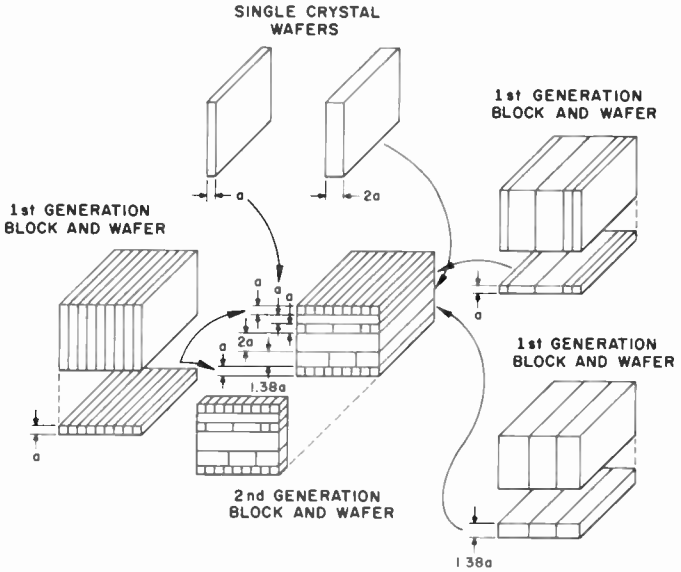

Fig. 3—A hypothetical "second-generation" substrate and its components.

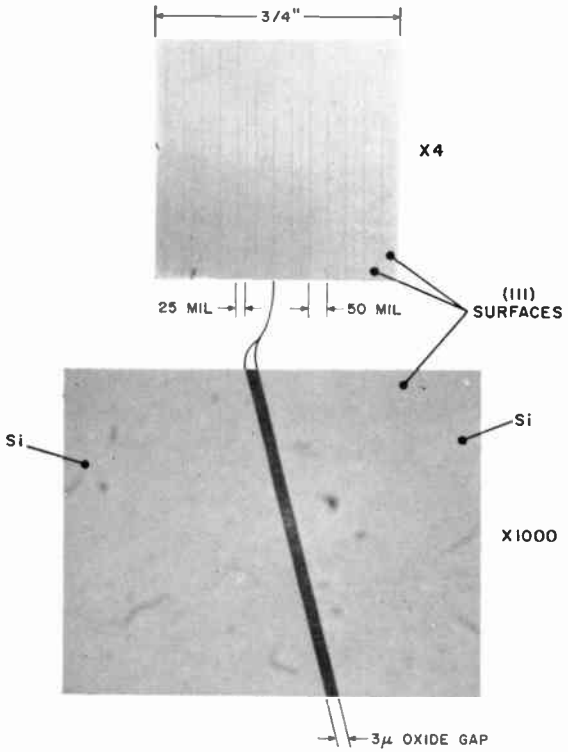

Fig. 4—Substrates for complementary MOS "ladder" arrays.

tors (Figure 6). In Figure 5, a laminate including Pyroceram regions and silicon bars is seen at the top. Below, a second-generation laminate containing bars and blocks of silicon in a Pyroceram matrix is shown. The wafer in Figure 5a, viewed end-on, forms one row of silicon and Pyroceram blocks for the substrate of Figure 5b.

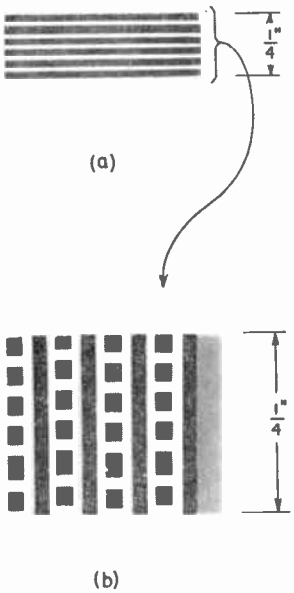

Fig. 5—Substrates composed of silicon and matching-coefficient Pyroceram. Top, "first-generation" substrate; bottom, "second-generation" substrate.

Electrical Properties of Diodes Formed in Laminate Substrates

The preparation of complementary diode arrays in laminate substrates has been carried out using doped-oxide diffusion sources deposited as described by Fisher and Amick.[3] Both mesa- and planar-type diodes have been formed successfully.

An array of mesa devices is shown schematically in Figure 7. These were prepared on laminate substrates comprised of nominally 15-ohm-cm n- and p-type bars. Stripes of doped oxide suitable for emitter diffusions were deposited over appropriate silicon regions

[3] A. W. Fisher and J. A. Amick, "Diffusion Characteristics of Doped Silicon Dioxide Layers Deposited from Premixed Hydrides," *RCA Review*, Vol. 29, p. 549, Dec. 1968.

through metal masks (Figure 7a). A diffusion step at 1200°C for 1 hour was then carried out, after which mesas were defined with hydrofluoric-nitric acid (Figure 7b). For this step, 0.01-inch-diameter mesas were defined with black wax. Individual diodes were probed to determine their electrical characteristics. As can be seen in Figure 7c, the voltage breakdown for both n-on-p and p-on-n diodes was in excess of 200 volts, while the reverse saturation currents were below 0.1 ma.

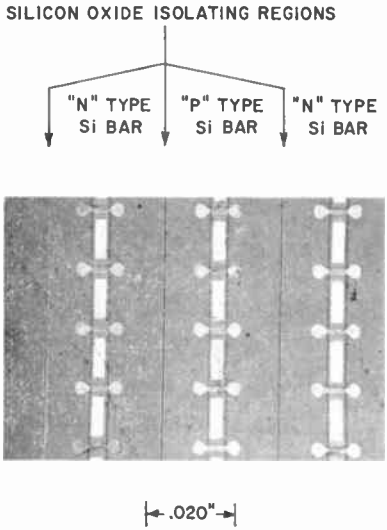

Fig. 6—MOS transistor arrays fabricated on a silicon/silicon dioxide laminate. Rectangular areas are source–drains, dumbbell-shaped areas are gates.

Arrays of complementary planar diodes have been prepared on 1-ohm-cm n- and p-type silicon–Pyroceram laminates. For these devices, a 0.5-micron thermal-oxide layer was first grown over the silicon surfaces. Openings 0.030 inch in diameter were then etched into this oxide above the p-type silicon regions only. A doped oxide containing phosphorus appropriate for base-level doping was next deposited over the entire surface. Openings 0.030 inch in diameter in the double-oxide layer were then formed above n-type regions and a doped-oxide source containing boron, appropriate for base-level doping, was deposited over the entire surface. A single diffusion, serving to drive in both n- and p-type dopants, was carried out at 1200°C for 2 hours, after which contacts were opened. Reverse-breakdown voltages for both types of diode were in the neighborhood

of 60 to 70 volts, with the reverse saturation current below 1 mA at a few volts, but with a somewhat rounded reverse characteristic at higher reverse biases. Junction depths were 3 microns, as expected.

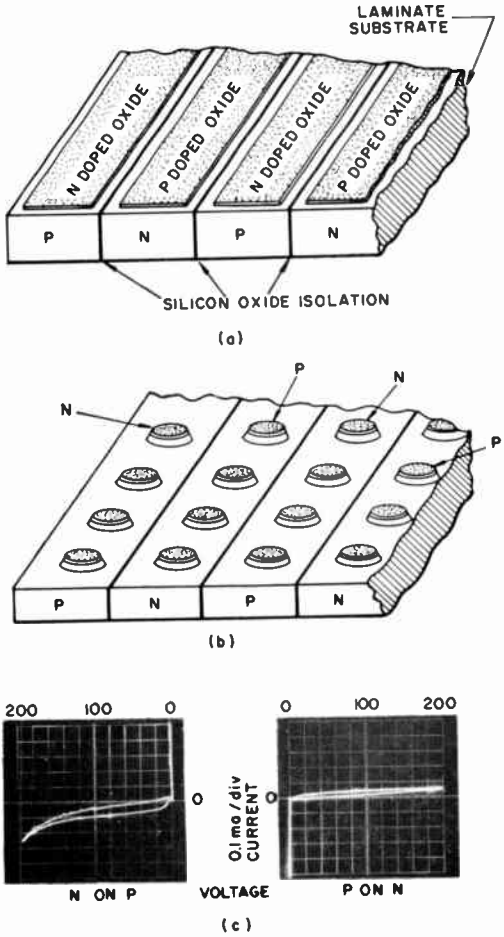

Fig. 7—Preparation and characteristics of complementary diode arrays.

When emitters were formed in these base-level doped regions, the current gains for the resultant transistors were found to be low, apparently because of a decreased minority-carrier lifetime in the base region compared with that in the original single-crystal silicon wafers from which the laminate substrates were prepared. This lowered lifetime can probably be attributed to the high dislocation density arising from plastic-flow during the hot pressing step, as described

subsequently. It is therefore concluded that until a method of reducing the dislocation density in these substrates is devised, they will not be useful for forming arrays of bipolar devices, but should be satisfactory for preparing diode arrays or arrays of MOS transistors (Figure 6). Junction characteristics and transconductances for arrays of MOS transistors are normal, i.e., comparable to arrays formed in single-crystal substrates.

Discussion

Because of the freedom to include silicon regions of almost any resistivity and type in almost any desired location, laminate substrates have certain advantages for the fabrication of complementary integrated circuits. Long rectangular regions can be provided for MOS ladder arrays, and small square areas can be provided for the preparation of individual diodes, diffused resistors, and the like. For diode arrays it is possible to form the cathode contact on either face of the wafer as desired. Passive components could be prepared in silicon regions by diffusion techniques or could be formed by deposition on insulating Pyroceram regions as desired.

An additional advantage of this freedom is the ability to provide feed-throughs in almost any desired location. Since the silicon regions extend completely through the substrate, contact can easily be made to the front and the back face of any region. A 0.015 × 0.015 × 0.015 inch silicon cube of 0.005-ohm-cm resistivity introduces a series resistance of only about 0.15 ohm. It may therefore be desirable to use both faces of the wafer to form circuits, with feed-throughs provided at suitable locations. Crossovers can conveniently be obtained by tying together two feed-throughs on the back surface by any suitable interconnection technique, such as evaporation of a metal through a mask.

The substrates prepared by the lamination process are mechanically rugged and can be handled and processed very much like single-crystal silicon. Both the thermally grown silicon dioxide and the Pyroceram withstand treatment in an oxidizing atmosphere at the temperatures required for diffusion into the silicon. The laminate substrates prepared in this work have been cycled several times from room temperature to 1200°C and back to room temperature with no cracking or mechanical deterioration.

The hot-pressing step does introduce dislocations into the silicon, which deforms plastically at the pressing temperature and pressure. Following Sirtl[4] etching, dislocation densities of as much as 5×10^6

[4] E. Sirtl and A. Adler, "Chromsäure-Flussäure als spezifisches System Zür Ätzgrubenentwicklung auf Silizium," *Z. Metallkde*, Vol. 52, p. 529, 1961.

cm^{-2} are observed both for laminates of silicon and silicon dioxide and for laminates incorporating Pyroceram.

Resistivity measurements made with a four-point probe reveal that changes in resistivity during lamination are negligible, both for lightly doped and for heavily doped starting material.

In the lamination process, the Pyroceram is sometimes partially reduced chemically. It can easily be restored by a thermal oxidation of the final substrate in steam at 1050° for a few hours. Since the first step in conventional device processing is the growth of an oxide layer on the silicon areas, this reoxidation of the Pyroceram would take place during normal processing. In any event, the resistivity of the partially reduced Pyroceram is extremely high and will probably not interfere with any circuitry fabricated in the substrates even if it is not reoxidized.

During lamination and subsequent high-temperature processing, impurities may diffuse from the Pyroceram into the silicon. In particular, p-type contamination, probably due to aluminum, can be found at depths of a few microns from the Pyroceram–silicon interface. Since the smallest silicon areas that can be made practically in these substrates are about 250 × 250 microns, this diffusion should not cause a problem as long as the outer 25-micron periphery of any silicon region is not included in the active device area. In certain applications, the use of a barrier layer, e.g., silicon nitride or aluminum oxide, may be desirable to minimize the diffusion of impurities into the silicon.

Conclusions

Laminate substrates can readily be prepared in a variety of configurations using silicon, thermally grown oxide layers, and suitable ceramics such as Pyroceram 9606. The substrates can undergo conventional silicon device processing with no deterioration of their mechanical properties. The dislocation density in the final substrates is high and, until ways of lowering the dislocation density can be devised, their usefulness will be limited to the fabrication of MOS devices and diodes. These substrates are especially suitable for applications that require unusually high voltage isolation between devices and for configurations of device arrays beyond the size limitations of single-crystal silicon wafers.

Acknowledgement

We would like to thank E. F. Cave for valuable discussions, as well as N. E. Wolff, who also critically read the manuscript.

ISOLATION TECHNIQUES FOR FABRICATING INTEGRATED CIRCUITS

II. DIELECTRIC REFILL TECHNIQUES AND DECAL AIR ISOLATION

By

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Summary—Three techniques are described for preparing silicon integrated circuits in which the individual components are separated from one another by a true dielectric rather than the p-n junctions that are presently used. Two of these techniques begin with wafers in which devices have already been formed, while the third involves a new type of isolating substrate capable of undergoing diffusion steps. In all cases the devices are precisely located with respect to one another and are essentially coplanar, so that interconnections can be formed in a single operation.

Introduction

Integrated circuits have found widespread use in computers and other applications where low voltages and low frequencies are encountered. These are mostly digital applications, although there has been some analog usage where present-day performance of integrated circuits can meet the requirements of the circuit.

Circuits made from discrete semiconductor devices can presently operate at frequencies greater than 1 GHz. Integrated circuits, however, are generally limited to operating frequencies in the 50 to 100 MHz range, due to parasitic capacitances between neighboring components and between components and the substrate. These are associated with the reverse-biased p-n isolation junctions that are normally used for electrically isolating the components from one another. Also, the maximum potential difference that can be supported between devices is limited to the reverse-breakdown potential of the isolation junction (in the range of 40–50 volts). Isolation junctions also have substantial leakage currents and poor radiation resistance.

For these reasons, it is apparent that a better method of isolation must be used if integrated circuits are to be employed for more de-

manding applications, such as microwave and radar circuits. Even for present applications, such as digital computer circuits, there is a performance advantage to be gained if circuits and systems were designed for, and used, dielectrically isolated integrated circuits.

A common approach to isolation (employed in some commercially made circuits) is based on the use of a thin layer (2–4 microns) of SiO_2 to provide isolation, and a polycrystalline silicon refill to provide useful circuits for certain applications. It does not, however, provide as good an isolation impedance at higher frequencies as does a true dielectric.

Therefore, isolation techniques based on the use of dielectrics such as glass and ceramics have been devised. Several of the methods and processes used for the purpose are described in this paper.

Approaches to Dielectric Isolation

There are three possible stages in the processing of a silicon integrated circuit at which device isolation could be accomplished:

(1) before the device diffusions are carried out;

(2) after the device diffusions are completed, but before metallization and interconnection;

(3) after the devices are metallized and interconnected.

Associated with each of these options are restrictions on the temperature that may be used in the isolation process and a requirement that the substrate be able to withstand the temperatures subsequently used in completing the device or circuit.

If isolation is provided before the device diffusions, temperatures as high as 1200–1300°C can be used to achieve isolation, since the only limitations are the melting point of the silicon and the degree to which defects are introduced into the structure of the silicon. Once isolated, however, the substrate must withstand diffusion temperatures of 1100–1200°C for appreciable periods of time.

If the diffusions are first completed conventionally in a single-crystal wafer, then the isolation process must be carried out at a temperature that will not affect diffusion profiles in the devices. For silicon devices, this means that the isolation temperature should not exceed 900–950°C. After isolation of diffused devices is completed, the only processing that remains to be done is the metallizing for interconnections. This is accomplished at temperatures well below 900°C. This technique provides the advantage of being able to carry out all the diffusion steps in single-crystal silicon wafers, thereby avoiding

any processing problems or contamination that the insulating substrate might introduce.

The third option is the isolation of devices that have been completely fabricated, metallized, and interconnected. The maximum allowable isolation temperature in this case depends on the type of metal that is used. Aluminum, which is the most common metal presently used for silicon semiconductor devices, does not withstand processing at temperatures beyond 450–500°C. This is a severe restriction, since glasses that soften below this temperature usually have high thermal expansion coefficients and contain ions that degrade the dielectric characteristics. However, if a more refractory metal such as tungsten[1] is used, this temperature restriction is relaxed and suitable glasses are available. An example of the latter isolation method, known as the "Decal" process, appears to be the most attractive from both a technical and an economic standpoint and is described later.

There are several possible variations of these methods, and the selection of an isolation scheme must be based on the many electrical and physical requirements of the particular circuit involved.

Dielectric Materials Suitable for Isolation

Two types of materials are used as the insulating dielectric in the isolation methods described here—a glass and a glass–ceramic composite.

Where the isolation is provided after the device diffusions are completed, the requirements for the dielectric include (1) a good thermal expansion match with the semiconductor and (2) good dielectric properties at high frequencies. It is not necessary, however, for the final composite substrate to withstand high-temperature diffusion conditions after the isolation is carried out. Glasses that meet these requirements and that can be processed below 900°C are readily available. Corning #7070 glass*, the glass discussed here, has a softening point of about 715°C.

Glass–ceramic compositions were devised for substrates that must undergo diffusion after the isolation step. Such a requirement places certain constraints on the dielectric material in the substrate.

(1) It must closely match the thermal coefficient of expansion of silicon.

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[1] A. I. Stoller, J. A. Amick, and N. E. Wolff, "Getting the Most Out of Circuits with Dielectric Isolation," *Electronics*, p. 97, March 20, 1967.

* Corning Glass Works, Corning, New York.

(2) It must be processable at temperatures and pressures that do not introduce excessive dislocations in the silicon and do not change the impurity profile of epitaxial layers. It is, in general, desirable to use temperatures that do not exceed 1300°C, and pressures that do not exceed 1000–2000 psi.

(3) The dielectric substrate must withstand the device diffusion and processing conditions without degradation or dimensional change. This normally requires exposure to temperatures of 1100°C or greater for several hours.

(4) It must remain a low-loss dielectric at GHz frequencies.

(5) It should have a high dielectric strength.

Although some glasses come close to meeting these requirements, none were found that have the proper thermal expansion and that also withstand the diffusion conditions without deformation. Crystalline ceramics, on the other hand, can have satisfactory expansion and mechanical properties. They do not deform or flow readily, however, and cannot be pressed and molded into an intricate shape. A substrate meeting all these requirements can be made by using a suitable combination of a glass and a crystalline ceramic material. The starting compositions are prepared as an intimate mixture of finely powdered materials. The glass provides a deformable phase that permits molding around intricate silicon shapes, leaving essentially no voids. The crystalline ceramic phase provides a skeletal structure that prevents distortion of the substrate at temperatures that would be too high for the glass alone. In addition, a partial crystallization of the glass is encouraged to take place slowly as the substrate is prepared and heat treated. In this way, the substrate material is relatively fluid during pressing, but is much more refractory when completed.

It is possible to obtain a similar glass–ceramic body by using only a devitrifying type of glass that can be pressed into a silicon structure and subsequently devitrified. There is, however, a small volume expansion of the substrate as the devitrification takes place. This causes the silicon to crack if the glass is devitrified to the extent required. On the other hand, if about one half of the volume of the starting composition is crystalline, the overall volume change, due to the partial devitrification of the glass, is so small that it does not cause cracking. The major constitutents of these materials are:

(1) A glass having a high softening point, and a thermal expansion coefficient closely matching that of silicon (about 31 to 36×10^{-7} cm/cm°C). A suitable glass for this purpose is a calcium

alumino-silicate glass, such as Corning #1715, which has a softening point of 1070°C.

(2) A crystalline ceramic material having a high melting point (>1200°C) and a thermal expansion coefficient closely matching that of silicon. Many materials undoubtedly could be used. Two material that have been found satisfactory are mullite ($3Al_2O_3 \cdot 2SiO_2$) and cordierite ($2MgO \cdot 2Al_2O_3 \cdot 5SiO_2$).

The glass and the ceramic are ball-milled together in distilled water for about 15 hours to give an average particle size of 1 to 5 microns. Typically, the material is hot pressed into the structure to be isolated at temperatures between 1100°C and 1200°C at 1000 to 2000 psi for 10-15 minutes in order to obtain a dense substrate. The temperature may then be held in this range for an additional period of time to afford partial crystallization of the glass. It is desirable to carry out this crystallization before the device processing is started. In this way, any resulting dimensional change is completed before the processing is begun, and problems of mask misregistration are avoided.

It is possible to influence the rate of crystallization by the use of certain additives. Titanium dioxide (TiO_2) provides nucleation sites and tends to accelerate the devitrification process. It was found that additions of 3 to 5% by weight of TiO_2 cause such rapid devitrification that the substrate loses its fluidity before it can be pressed to a suitable density. The addition of a few tenths of a percent of TiO_2, however, is beneficial. In this case, the devitrification of the glass is accelerated, but not to an objectionable degree.

Another additive that can be used to control the devitrification process and subsequent crystal structure is MgO. The rate of crystal growth is reduced by the presence of MgO, thereby allowing some compositions that would otherwise be too viscous for pressing to be pressed to a high density. This permits the addition of more of the crystalline material in the starting composition, which minimizes dimensional changes during the heating cycle.

MgO and TiO_2 can also be used together in a composition in order to obtain a better microstructure. In this way, a uniform, fine-grained substrate is obtained that has controllable devitrification characteristics. An MgO addition of 3% by weight and TiO_2 addition of 0.3% by weight has been found satisfactory, although a systematic variation of these quantities has not been made.

Substrate compositions of Corning #1715 glass and mullite were heat treated at various temperatures after they were pressed and

the resulting crystal phases were studied by x-ray diffraction. These studies showed that the glass crystallizes to form phases of crystalline SiO_2 and a low-symmetry alumino-silicate. In the absence of additives it was found that the rate of devitrification becomes significant at temperatures of 1100°C and higher.

Hot Pressing Apparatus Used in Preparing Substrates

All the isolation methods described in this paper employ hot pressing. A special apparatus was designed to allow the insulator component of the substrate to be molded and bonded to the silicon regions under heat and pressure in a vacuum or a controlled atmosphere. In this aparatus (Figure 1), a graphite die serves as both a pressing chamber and as a susceptor for rf heating of the sample. A graphite ball joint compensates for any non-parallel surfaces in the assembly. Polycrystalline silicon nitride blocks are ideal as spacers, since they are chemically inert, have a low thermal conductivity and high compressive strength, and are resistent to cracking or spalling.

For pressing the glass–ceramic material, a die liner of 0.005-inch-thick graphite is used in a split-collar die. This facilitates removal of the finished sample, and if there is any sticking of the ceramic to the graphite, the liner can be sacrificed and removed by lapping or by oxidation.

For isolation techniques in which a simple glass is used, die faces of pyrolitic* graphite are used, since there is no tendency for the glass to adhere to this material. In all cases, a thermocouple penetrates well into the die in order to sense the temperature as close to the wafer as possible. This thermocouple controls the output of the rf generator to maintain a constant, pre-set temperature.

"O" ring seals allow for relative motion of the press platens while maintaining the controlled atmosphere or vacuum in the pressing chamber.

Isolation Before Device Fabrication

The glass–ceramic material described previously can be used to fabricate isolated integrated circuits by a method known as the "handle-wafer" technique.[2] The process can be divided into three major

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* Metallurgical Products Department, General Electric Company, Detroit, Michigan.

[2] D. Kenny, U.S. Patent #3,332, 137, Method of Isolating Chips of a Wafer of Semiconductor Material.

steps: (A) preparation of the handle wafer structure, (B) glass–ceramic wafer preparation (isolation), and (C) fabrication of the devices.

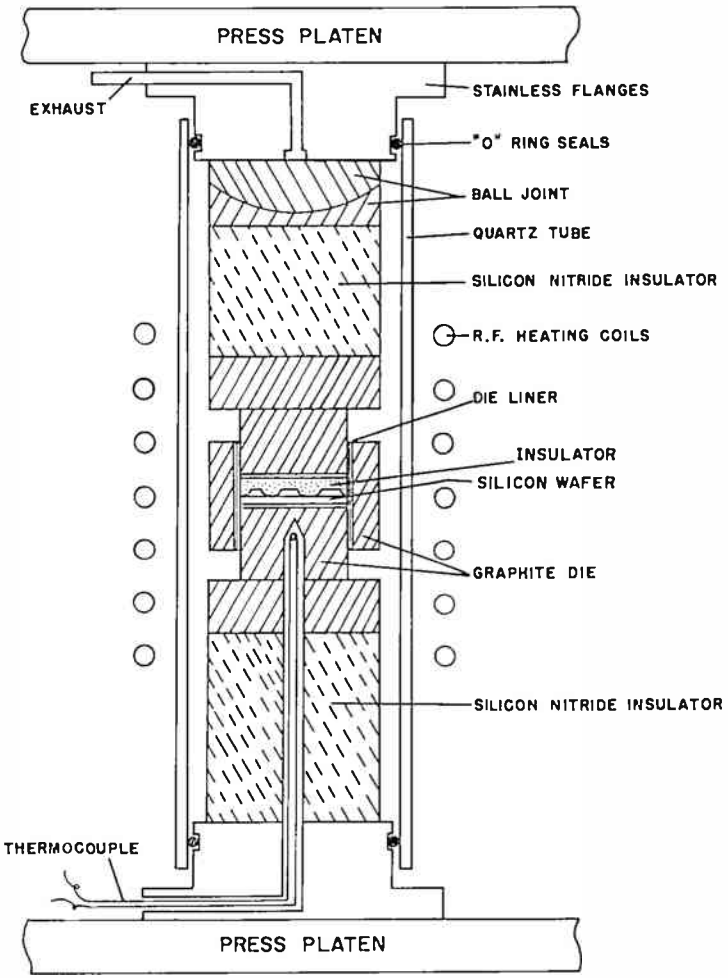

Fig. 1—Hot-pressing apparatus.

A. Preparation of the Handle-Wafer Structure

The preparation of the handle-wafer structure involves the bonding together of two wafers, one of which will be referred to as the mesa wafer and the other the handle wafer.

The mesa wafer is the wafer in which the devices will ultimately

be fabricated and may be of any desired type, resistivity, and epitaxial structure. First, about 1.5 microns of SiO_2 are thermally grown or deposited (and densified) on the surface (Figure 2a). The isolation pattern is then defined in photoresist on the surface, and the SiO_2 layer

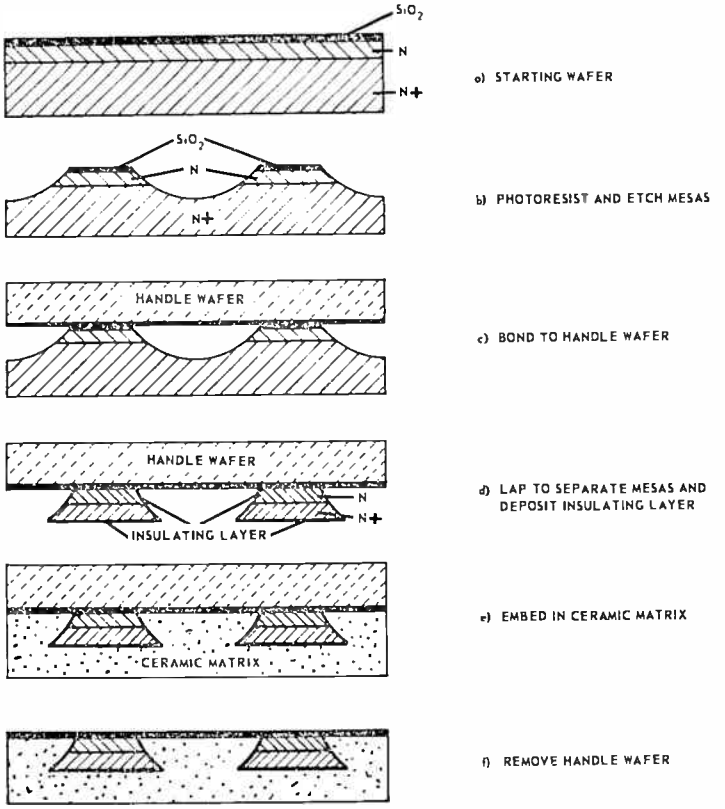

Fig. 2—Processing steps for making the ceramic-isolated integrated-circuit wafer.

is etched to this pattern with buffered HF. The photoresist is removed and the wafer is put into an $HF\text{-}HNO_3$ etchant to form mesas about 0.001 inch high (Figure 2b).

The handle wafer holds the mesas in their proper relative position during the isolation step. To prepare it, silicon wafers are polished flat and parallel and their thicknesses are accurately measured and recorded. These wafers are thermally oxidized to form about one micron of SiO_2 on the surface. The handle and mesa wafers are then

placed in the graphite die of the hot pressing apparatus described earlier. They are heated to 1200°C in a nominal vacuum and simultaneously pressed at 2000 psi for two minutes. The pressure is then released, the rf unit turned off, and the die allowed to cool. The wafers, which are shown schematically in Figure 2c, are then removed. Many wafers could be pressed simultaneously by stacking in the same die several sets of handle wafers and mesa wafers, the sets being separated by disks of carbon.

The backs of the mesa wafers are then lapped or ground off to separate the mesas (Figure 2d). Since the glass–ceramic would be readily attacked by the hydrofluoric acid used in subsequent processing, leaving a pitted surface on the ceramic substrate, an insulating layer of a material that is not attacked by HF is deposited over the wafer on the mesa side (Figure 2d). Two such materials are vapor-deposited silicon nitride and aluminum oxide. Alternatively, a thick layer (about 3 microns) of SiO_2 can be deposited over the back of the mesa array. This layer is not removed in subsequent etching steps, and provides protection for the underlying ceramic substrates.

B. Glass–Ceramic Wafer Preparation (Isolation)

The region around the mesas is filled with dry glass–ceramic powder. The pressing apparatus is set up as shown in Figure 1. For a standard 1.25-inch-diameter wafer, each gram of the glass–ceramic powder forms about 0.020-inch of finished substrate thickness.

The rf heater is turned on and the die is heated. When the temperature reaches about 1000°C, pressure is applied and slowly increased to 2000 psi. The pressure is held constant for 15 minutes with the temperature at 1175°C to allow the glass–ceramic to densify. It is imperative that the die be heated rapidly, or the glass in the mixture will devitrify during heating, viscosity will increase, and the structure will not be completely filled. It has been found that, for satisfactory results, the maximum temperature should be reached in two minutes or less. The rf power is then reduced and the die is allowed to cool. When it cools to 1100°C, the pressure is released and the die is further cooled to 860° C, where it is held for 15 minutes for annealing. At this time, further nucleation of crystallites in the glass also takes place.

The die is cooled, and the wafer (shown in Figure 2e) is removed. The handle, having served its purpose, is removed (Figure 2f) by heating the wafer in a tube furnace at 1000° with 5000 cm^3/min of anhydrous HCl and 100 cm^3/min of H_2 flowing through it. This removes

the silicon of the handle wafer at a rate of about 0.002 inch per minute and since SiO_2 is not attacked by HCl, the underlying silicon mesas are not etched.

The wafer is now put into hydrofluoric acid until the SiO_2 layer that had served to bond the mesa wafer to the handle wafer is removed. The wafer is cleaned by standard methods and the silicon is reoxidized to provide a layer that is suitable for device processing. For this oxidation, it has been found that two hours at 1050°C in steam, followed by one hour at 1100°C in O_2 and an hour at 1150°C in O_2 forms about 8000 Å of SiO_2 and, at the same time, completes the devitrification of the glass–ceramic insulator.

It has been found that the purity of the readily available commercial materials is adequate for preparing this substrate wafer. The substrate materials used can cause a slight p-type doping if they are in contact with silicon after prolonged heating at high temperatures. This is generally of no concern, however, since the substrate material is not in the junction region of the devices, and since a diffusion barrier such as an SiO_2 layer is interposed between the ceramic and the silicon.

C. Fabrication of the Devices

The composite wafer is now ready to undergo the fabrication of integrated circuits or other devices by standard planar techniques. There is, however, one important deviation from standard integrated-circuit processing procedures. The long isolation deposition and diffusion required to obtain the isolation in a standard monolithic wafer, typically a 16-hour heating cycle, is not required in glass–ceramic refill wafers.

Figure 3 shows a ceramic isolated CA-3005 rf-mixer substrate wafer, with a detailed inset of one circuit. The bottom half of the picture shows a cross section of the substrate. The silicon is seen to be "keyed" into the substrate as a result of the processing sequence. A completed, processed circuit chip is shown in Figure. 4.

Isolation After Device Fabrication

The same handle-wafer technique used for the glass–ceramic isolation technique described above can also be used, with a few modifications, to isolate diffused devices in a glass matrix.

(1) An isolation pattern is defined in the SiO_2 layer on a silicon device wafer that has the diffusion steps completed but lacks metalliza-

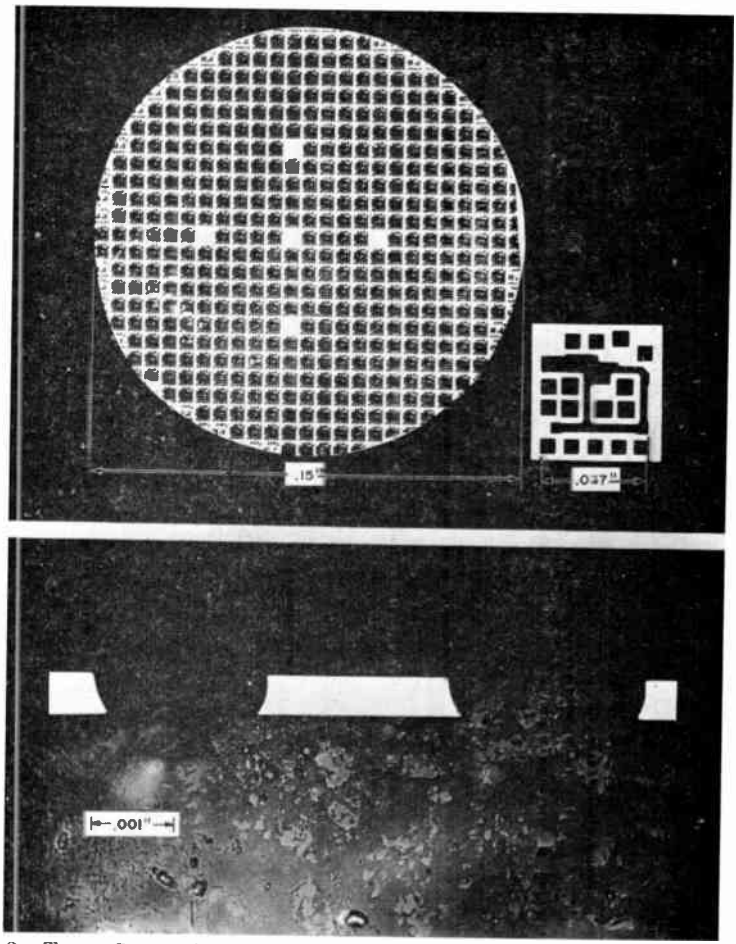

Fig. 3—Top: Composite substrate wafer; inset shows detail of circuit. (silicon dark)
Bottom: Cross-section through isolated wafer. (silicon light)

tion (Figure 5a). The isolation pattern is etched in this wafer to produce mesas that are about 0.001 inch high (Figure 5b).

(2) A thin layer of glass (0.5 — 2 microns thick) is vapor-deposited or rf-sputtered onto another flat, (100) oriented silicon wafer that is subsequently used as a temporary handle to hold the devices in their proper location during isolation. This glass layer serves as a bonding medium.

(3) The device wafer is bonded to the handle wafer, as shown in Figure 5c, by hot pressing. It has been found that 2 microns of sputtered Corning #7059 glass forms a good bond when pressed at 950°C for two minutes at 1000 psi.

(4) The back of the device wafer is lapped away so that device mesas remain bonded to the handle in proper registry (Figure 5d). At this point, the device mesas are only 0.0005 to 0.001 inch high.

(5) A glass that softens at about 700 to 750°C such as Corning #7070 is pressed into the back of the array, as shown in Figure 5e, at a few hundred psi. This is carried out in the rf-heated graphite die described above.

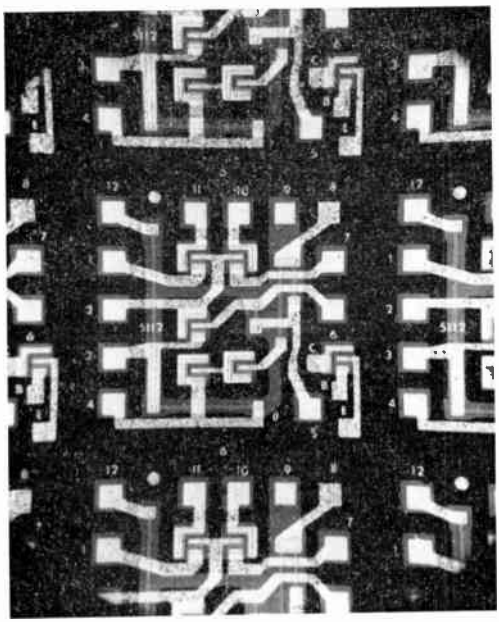

Fig. 4—Isolated circuit after diffusions and metallization have been completed.

(6) The handle can be removed (Figure 5f) by dissolving it in a hot 25% KOH solution. Etching stops when the layer of glass is reached, thereby protecting the underlying circuit from being attacked.

(7) The glass layer that had been used to bond the handle wafer to the device wafer is etched away, leaving only the original silicon dioxide layer on the wafer. When #7059 glass is used, it can be preferentially etched away from the silicon dioxide layer with a 25% hydrofluoric acid solution.

(8) The contact areas in the silicon dioxide layer are opened and the metal interconnect pattern is applied.

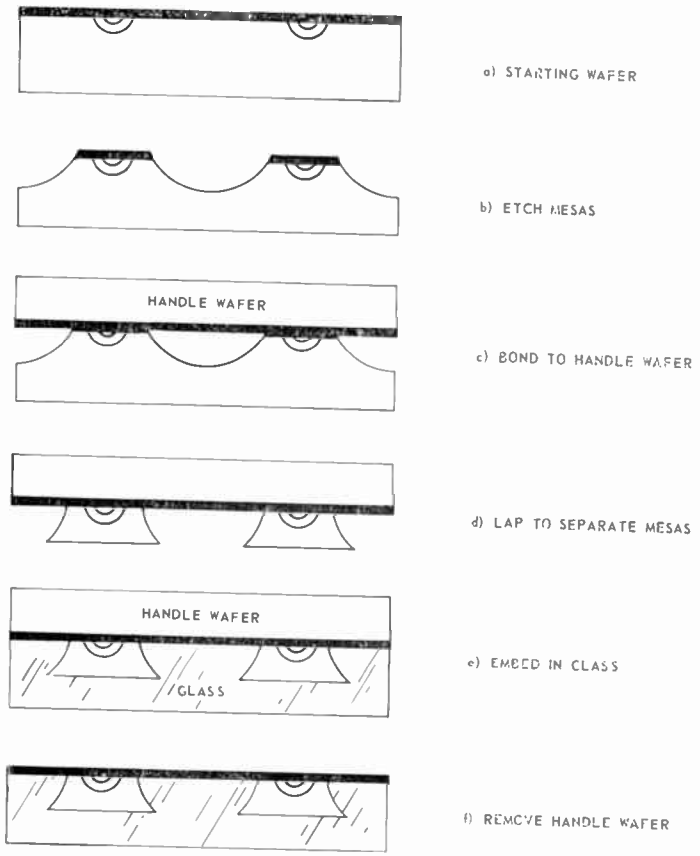

Fig. 5—Processing steps for making the glass-isolated integrated-circuit wafer.

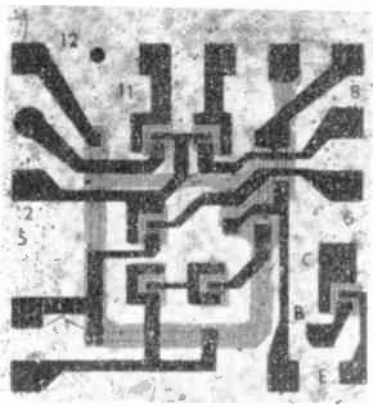

Fig. 6—RF-mixer circuit isolated by the handle wafer method using a glass refill.

A photograph of an rf-mixer circuit chip isolated in this way and interconnected with an aluminum metallization pattern is shown in Figure 6.

Isolation After Metallization

The scheme of isolation that we have named the "Decal" method is perhaps simpler and more versatile than the two methods previ-

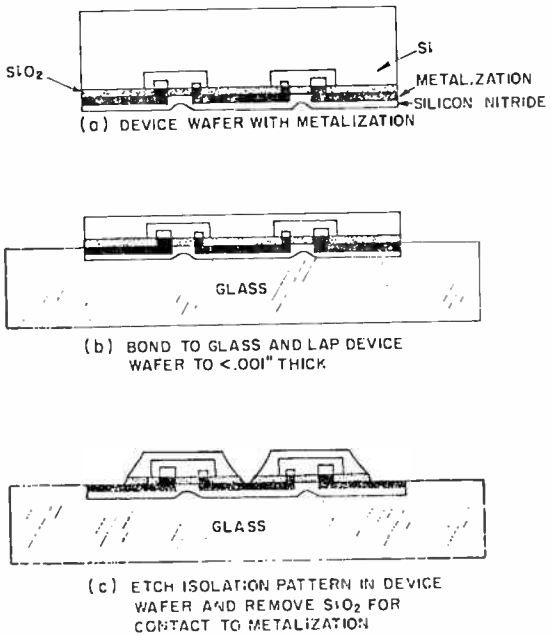

Fig. 7—Steps in the fabrication of the "Decal" structure.

ously described. Here, the devices are completely fabricated on the single-crystal wafer (Figure 7a), including all metallization and interconnection (single or multi-layer). When isolation is accomplished by the Decal method the isolation diffusion step in the monolithic process is, of course, omitted. The dielectric isolation is then carried out according to the following steps.

(1) The metallized device surface of the wafer is bonded to an insulating substrate. For a tungsten-metallized wafer, a layer of silicon nitride is first deposited over the device wafer to provide an improved barrier layer. The wafer is then bonded directly to a glass substrate, such as Corning #7070, at 700 to 800°C under a few hundred psi of pressure.

(2) The back of the device wafer is lapped so that only 0.0005-0.001 inch of silicon (containing the devices) remains bonded (face down) to the glass (Figure 7b). The back of the silicon is polished and a layer of chromium (about 5000 A thick) is evaporated over the back of the wafer.

(3) The mirror image of the isolation pattern, similar to that used for diffusion isolation in monolithic circuits, is defined in photoresist. The registration of this mask can be accomplished by etching a part of the silicon wafer away at the edges, leaving some of the metallization pattern exposed for registration.

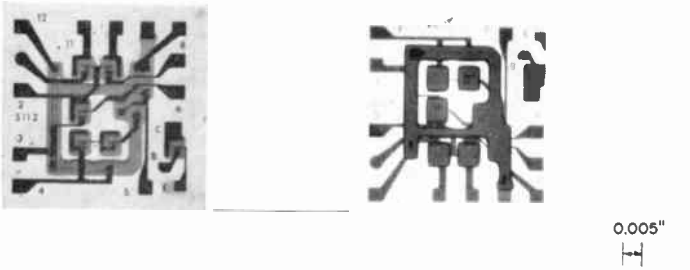

Fig. 8—An RF mixer circuit isolated by the "Decal" process. Left, looking through the glass, and, right, looking at the back of the circuit.

(4) The chromium is etched with HCl or potassium ferricyanide to form a resistant etch mask for the silicon. A solution of 10% concentrated hydrofluoric acid and 90% concentrated nitric acid is used to etch the silicon into the desired isolation pattern. Thus the silicon is divided into discrete regions, each containing an active or passive component, or a group of components (Figure 7c). The metallization pattern is covered with the SiO_2 layer that was originally on the silicon wafer, since this oxide is not dissolved by the etch used for the silicon.

(5) Openings are etched through the SiO_2 layer in the areas where contact is to be made to the metallization pattern.

(6) If contact is to be made to the resulting circuits by ultrasonic or thermocompression bonding, it is necessary to deposit a layer of aluminum or other ductile metal over the tungsten bonding pads. If a solder contact to the bonding pads is desired, then nickel or other solderable metal is deposited in the bonding-pad areas. These steps are necessary because refractory metals such as tungsten do not bond readily by conventional techniques.

Top and bottom views of an rf-mixer integrated circuit isolated by the Decal method are shown in Figure 8. The metallization pattern on this circuit is tungsten.

PROPERTIES OF DIELECTRIC SUBSTRATE MATERIALS

Electrical Characteristics of the Glass–Ceramic Refill

Electrodes were attached to both sides of a piece of a glass–ceramic substrate that was prepared from a 60% #1715 glass–40% mullite composition. The dielectric characteristics versus frequency were measured on a capacitance bridge at frequencies up to 250 MHz. A piece of the same substrate material was measured at 9 GHz in a microwave cavity. The results of these measurements, shown in Fig-

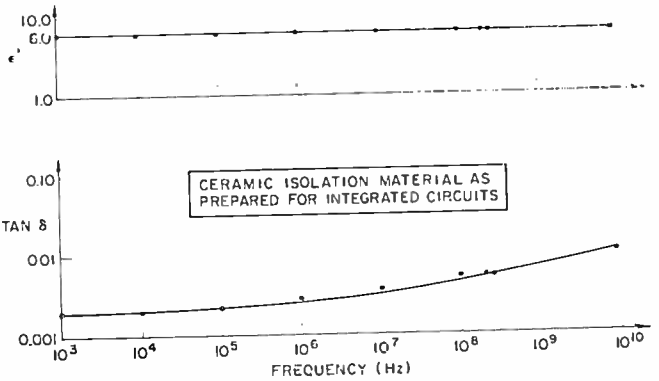

Fig. 9—Dielectric constant and loss tangent versus frequency.

ure 9, demonstrate that the substrate behaves as a low-loss dielectric over the frequency range covered. The relative dielectric constant is about 6, while the loss tangent rises from 0.003 to 0.01 over this frequency range.

In order to compare the glass and ceramic dielectrics with the commonly used polycrystalline silicon/SiO_2 isolation material, polycrystalline silicon wafers having a 4-micron coating of SiO_2 on each side were measured. Wafer thicknesses of 0.003, 0.006, 0.013 and 0.024 inch were used. They all had resistivities of about 50 ohm-cm, which is typical for this type of isolation material. Since essentially all of the field appears in the SiO_2, it is not possible to calculate a dielectric constant for such a composite independent of its thickness. However, for a 0.003 inch thickness (which is a typical isolation spacing in an integrated circuit), the effective dielectric constant is 48. This figure increases linearly with thickness. The low-frequency loss tangent was found to be about 0.001 for the polycrystalline silicon isolation material, but increased steadily with frequency as shown in Figure 10.

In the vicinity of 250 MHz, the losses increase so rapidly that the material is no longer useful as an isolation medium.

These measurements were confirmed by measuring the isolation impedance between identical silicon pads on CA 3005 rf-mixer-circuit pellets having both ceramic isolation and polycrystalline-silicon isolation. These results are shown in Figure 11. In this figure, an area

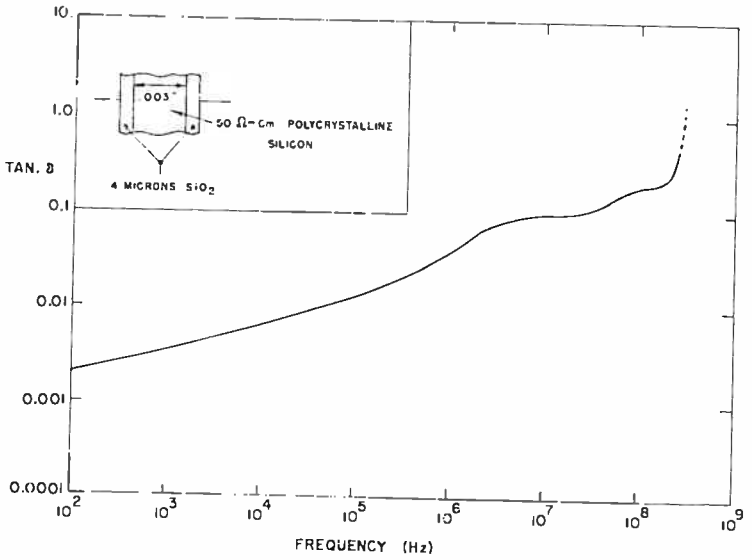

Fig. 10—Low-frequency loss tangent versus frequency.

corresponding to the estimated performance for a p-n junction isolation is indicated by shading. This estimate is based on the known frequency limitations of integrated circuits, and the data of Maxwell et al,[3] which show that the parasitic capacitance of a p-n junction is 10 times as great as it is for polycrystalline silicon/SiO_2 isolation.

Maxwell et al also found that the leakage current is reduced by a factor of 10^7 when polycrystalline silicon SiO_2 isolation is used in place of p-n junction isolation. In the case of ceramic isolation, one would expect another order of magnitude improvement due to the increased thickness of the dielectric.

The breakdown voltage of a 0.003-inch-thick sample of the glass–ceramic substrate was found to be in excess of 6000 volts. A sample

[3] D. A. Maxwell, R. B. Beeson, and D. F. Allison, "The Minimization of Parasitics in Integrated Circuits by Dielectric Isolation," *IEEE Trans. on Electron Devices*, Vol. ED-12, p. 20, Jan. 1965.

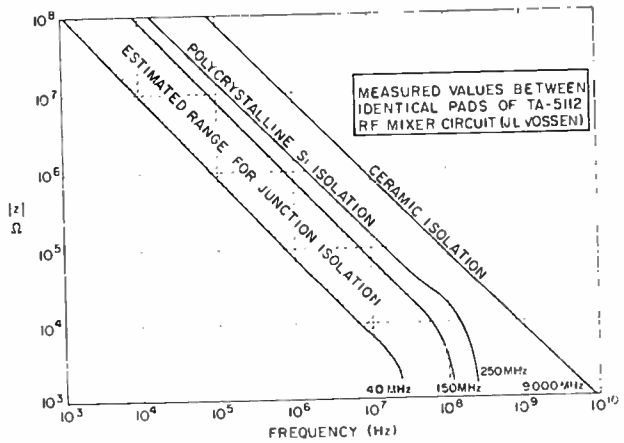

Fig. 11—Isolation impedance versus frequency for various types of isolation.

of polycrystalline silicon 0.003-inch thick having 4 microns of SiO_2 on each side was found to have a breakdown voltage of 1500 volts. This is in agreement with the results of Schnable et al[4] who found a breakdown strength of 200 volts/micron for SiO_2 isolation layers.

Table I summarizes the relative electrical characteristics of the three types of isolation that have been discussed. It should be noted that the breakdown voltage for both p-n junction isolation and Si/SiO_2 isolation is independent of the spacing between regions, while the breakdown voltage between regions in a ceramic-isolated structure can be made larger by increasing the space between devices. It may ultimately be limited by surface leakage.

Table I

	p-n junction	poly Si/SiO_2	Ceramic
Parasitic Capacitance (Relative)	80	10	1
Leakage Current (Relative)	10^8	10	1
Voltage Breakdown for 0.003 inch Spacing (Volts)	50	1500	6000
Maximum Usable Frequency (MHz)	150	250	>9000

[4] G. L. Schnable, A. F. McKelvey, and J. A. Hastings, "A Chemical Technique for Preparing Oxide-Isolated Silicon Wafers for Microcircuits," *Electrochemical Technology*, Vol. 4, p. 57, Jan.-Feb. 1966.

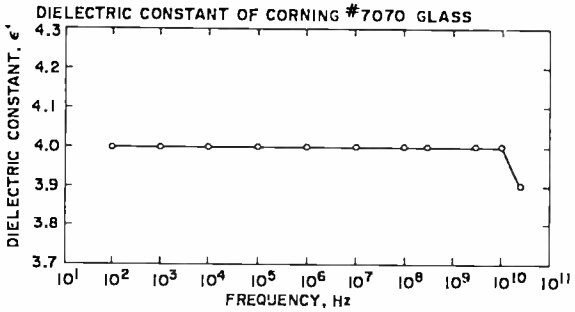

Fig. 12—Dielectric constant as a function of frequency between 20°—25°C.

Electrical Characteristics of the Glass Refill

The dielectric properties of the Corning #7070 borosilicate glass used as an isolation medium have been reported by von Hippel.[5] The properties compare favorably with those of the glass–ceramic material measurements reported above. Figures 12 and 13 show the dielectric constant ϵ' and the dissipation factor, tan δ, versus frequency as reported by von Hippel.

Electrical Characteristics of Decal Isolation

In the case of the Decal structure, the dielectric between the devices is a composite of air and Corning #7070 glass. For practical purposes, air is a perfect dielectric with $\epsilon' = 1$ and tan $\delta = 0$ from dc to at least 10^{10} Hz.

For air, glass, or glass–ceramic isolation, then, the performance as a dielectric is excellent from dc to the GHz region.

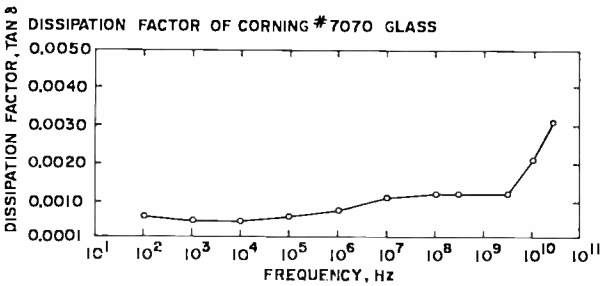

Fig. 13— Dissipation factor as a function of frequency between 20°—25°C.

[5] A. R. Von Hippel, Tables of Dielectric Materials in *Dielectric Materials and Applications*, p. 291, John Wiley & Sons, Inc., N.Y., 1954.

Electrical Performance of Dielectrically Isolated Circuits

As described above, operative rf-mixer circuits of the type shown in Figure 4 were prepared using glass–ceramic refill, glass refill, and Decal air isolation. As references, the same circuit was also constructed in p-n junction and polycrystalline silicon refill form. Although the circuit was not designed specifically for dielectric isolation, a modest improvement in the performance of the dielectrically isolated versions at high frequencies was obtained. Quantitative measurements have been made only for the glass–ceramic refill, the p-n junction and the polycrystalline refill circuits. For these versions the useful frequency range, defined as the frequency at which the real part of the forward transfer admittance (g_{21}) falls to 1 mmho is

standard p-n junction isolation	200 MHz
polycrystalline refill	280 MHz
glass–ceramic refill	300 MHz

The performance of the glass refill and the Decal air-isolated circuits should be comparable to that of the glass–ceramic refill circuits. Improved test vehicles are currently being designed and fabricated by these various isolation techniques so that a more detailed evaluation can be obtained. From even this preliminary data, however, it is clear that true dielectric isolation will afford a substantial improvement in performance at high frequencies, compared with conventional p-n junction or polycrystalline refill isolation.

Discussion

The handle-wafer method with either glass–ceramic or an all-glass dielectric refill is suitable for tightly packed, small-geometry arrays of randomly shaped devices, since the isolation grooves need only be 10–20 microns deep. The isolated array of devices is planar, thereby providing a surface on which passive components and the metallization can readily be fabricated.

This process also affords the possiblity of providing isolated silicon areas of different types and resistivities. This can be done by bonding and lapping the back off one mesa wafer and then bonding a second mesa wafer to the same handle and lapping the back off it.

The Decal structure (with its possible variations) provides a very simple and versatile approach to isolation, as well as opening attractive possibilities for low-cost packaging methods. The isolated units may be scribed, broken apart, mounted, and wire bonded in the same way that monolithic circuits are presently handled. Alternatively, the cir-

cuit pellets can be inverted and bonded directly to a circuit board or an inexpensive header that needs no hermetic sealing.

Large arrays can also be prepared by this process by letting an entire wafer or a substantial part of a wafer serve as a single, interconnected circuit. Outboard components can be readily connected into the circuit, since direct access to any lead in the circuit area can be provided.

The Decal process also offers the possibility of making a structure having a very low thermal resistance; the junctions are only 10–20 microns from the back of the silicon regions. In a conventional chip, the heat must be transferred through about 125 microns of silicon before it reaches the heat sink. Thus the thermal resistance between the junctions and a heat sink could be made lower for a Decal circuit than for its conventional counterpart.

It is possible to utilize the isolated circuits that have been described here in several ways. If large arrays are required, the circuits can be interconnected by a metallization pattern on the wafer. Alternatively, the wafers can be scribed and broken into circuit chips and then mounted and bonded in the same way that conventional circuit chips are handled.

It is also possible to leave space on the wafer for the fabrication of thin-film passive components that can be connected into the circuit when the devices are metallized. Since the dielectric portion of the wafer can be made larger than the silicon wafer, the passive components may be fabricated on the peripheral areas without using valuable silicon area in the center. Because of the general coplanarity of all components, one-shot interconnections can still be made.

Often it is desirable to use strip-line techniques in the interconnection of high-frequency circuits. In such cases, the dielectric could be brought to the required thickness by abrasion. The dielectric could then be coated with metal by evaporation or other suitable deposition methods to give controlled-impedance circuitry.

Conclusions

Three methods of providing dielectric isolation for silicon integrated circuits have been described.

In addition to the electrical benefits of dielectric isolation (i.e., extended frequency range, higher voltage breakdown and improved radiation resistance), new circuit configurations and packaging techniques are also made possible. Space can be made available for de-

positing passive components side by side with the semiconductor devices. It is feasible to provide precision microstrip lines and ground planes and to operate a large number of devices in parallel (to get high power at high frequencies) without the need for fabricating such interconnecting elements externally. This is particularly useful for solid-state microwave applications.

When isolating Decal circuits, it is possible to provide access to bonding pads anywhere on the wafer area. Bonding is not restricted to the periphery. The process results in a flip-type circuit package than can be batch fabricated and that can further be packaged into a low-cost conventional lead package without the need for wire bonding.

ACKNOWLEDGMENTS

The authors wish to acknowledge, and express their appreciation for, the many contributions to this work made by their colleagues. In particular, they are indebted to J. Vossen and T. Walsh for the dielectric measurements, to B. Tilley for the high-frequency circuit measurements, to F. Duigon for the fabrication of the device wafers, to J. Shaw for the tungsten metallization, and to W. Kern and R. Heim for their technical assistance concerning the glassing techniques. Also, the authors wish to thank J. Amick and N. E. Wolff for their guidance, support, and constructive review of the manuscript.

RELATIONSHIP BETWEEN THE PERFORMANCE OF A LINEAR AMPLIFIER MICROCIRCUIT AND THE ISOLATION TECHNIQUE USED IN ITS CONSTRUCTION

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Summary—The high-frequency-performance curves for a linear integrated circuit prepared in a variety of configurations employing dielectric or junction isolated components were evaluated. The response of the circuit, a 2-stage linear amplifier, is vastly improved in the 0.1 to 1 GHz range by use of a dielectrically isolated structure rather than the standard monolithic structure. A small improvement over the standard monolithic structure is also obtained if thin-film resistors rather than diffused resistors are employed in an otherwise monolithic integrated circuit.

Because of transistor package parasitics, the circuit assembled from discrete components is inferior to its dielectrically isolated counterpart, although it gives better performance than the monolithic version. This analysis has shown, however, that mounting an integrated-circuit chip in a standard package may lead to improved performance in some frequency ranges, since the series lead inductance of the package tends to compensate for the capacitive input impedance of the chip.

Introduction

IN THE PAST few years a great deal of work has been carried out[1-9] on techniques for providing dielectric isolation for integrated circuits. The principle motivation for this work is the desire to

[1] A. I. Stoller, J. A. Amick, and N. E. Wolff, "Getting the Most Out of Circuits with Dielectric Isolation," *Electronics*, Vol. 40, p. 97, March 20, 1967.

[2] A. I. Stoller and N. E. Wolff, "Isolation Techniques for Integrated Circuits," *Proc. 2nd Int. Cong. on Microelectronics*, p. 269, R. Oldenbourg, Munich, Germany, 1967.

[3] D. McWilliams, C. Fa. G. Larchian, and O. Maxwell, "A New Dielectric Isolation Technique for High Quality Silicon Integrated Circuits," *Jour. Electrochem. Soc.*, Vol. 111, p. 153C, July 1964.

[4] T. V. Sikina, B. D. Joyce, N. P. Formigoni, C. C. Roe, and F. Schliesing, "A Novel Oxide Isolation Process," *Int. Electron Devices Meeting*, Washington, D. C., Oct. 20-22, 1965.

[5] T. H. Ramsey and T. Smith, "A Process for Ceramic Dielectric Isolation for Integrated Circuits," *Int. Electron Devices Meeting*, Washington, D. C., p. 14, Oct. 26-28, 1966.

[6] B. L. Frescura, R. Rusert, and J. Schroeder, "Mesa Isolation—and Isolation Technique for Integrated Circuits," *Int. Electron Devices Meeting*, Washington, D. C., p. 13, Oct. 26-28, 1966.

[7] M. P. Lepselter, "Beam-Lead Sealed-Junction Technology," *Bell Laboratories Record*, Vol. 44, p. 298, Oct/Nov, 1966.

[8] D. A. Naymik, "Silicon Mosaic for Integrated Devices," *IEEE Trans. on Electron Devices*, Vol. ED-12, p. 497 (Correspondence) Sept. 1965.

[9] D. A. Maxwell and R. H. Beeson, "The Minimization of Parasitics in Integrated Circuits by Dielectric Isolation," *IEEE Trans. on Electron Devices*, Vol. ED-12(1), p. 20, Jan. 1965.

eliminate the parasitic capacitances associated with the p-n junctions used to isolate components in conventional monolithic integrated circuits. The performance of a circuit can be considerably improved, especially at high frequencies, if these parasitic capacitances are eliminated. This paper presents a quantitative evaluation of the relative performance of integrated circuits employing several different methods of isolation.

Circuit Design

The circuit chosen for the analysis is a 2-stage, common-emitter *RC*-coupled, wide-band amplifier. This uncomplicated type of circuit

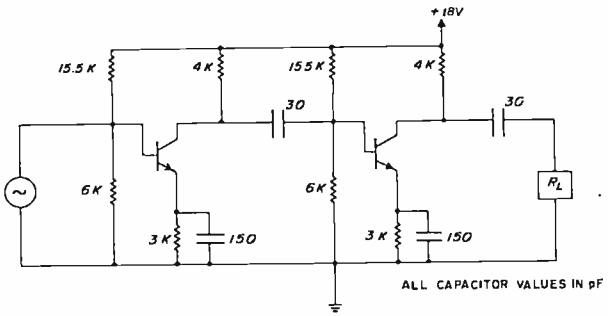

Fig. 1—Two-stage amplifier in dielectric isolation configuration.

was selected so that the performance curves could be readily interpreted. The design is such that the circuit can actually be fabricated in integrated form if desired. Also, in choosing a circuit vehicle for evaluating the effects of isolation parasitic capacitance, it is necessary to use transistors capable of performing at high frequencies. The dielectrically isolated form of the circuit is shown in Figure 1.

This circuit is not intended for any particular application, nor is it suggested that the design is optimum. It is intended only to represent a realistic linear circuit comprised of transistors, resistors, and capacitors. The significant aspect of the computations is the *relative* performance of several different forms of this circuit, rather than the absolute performance.

Circuit Elements

Transistors

The transistor type selected for the circuit is the 2N2857 rf tran-

sistor, which has a gain–bandwidth product (f_T) of 1 GHz. Since it is a silicon, n-p-n epitaxial planar device, it could be fabricated as an integrated-circuit component. No equivalent-circuit model for the transistor was devised; instead the more realistic, frequency-dependent y-parameters of the device were used directly in the computer simulation. Columns (A) in Table I give the parameters for the transistors in a standard metal package as shown in the published data sheets.[10] Columns (B) represent the parameters for the transistor in the chip form. The y-parameters for the transistor chip were estimated by correcting the values given in the published data sheet for the package parasitics using the technique described in Reference (11).

The y-parameters are given in the data sheet for the biasing conditions of 1.5 mA of collector current (I_C) which the biasing networks of the 2-stage amplifier were designed to provide.

Signal Source

The input signal is assumed to be from a small-signal voltage source having zero internal impedance. This eliminates any variations in gain arising from variations in the mismatch of the source to the circuit impedance as the circuit is modified. Such variations would arbitrarily mask the effects of the parasitics, since the source impedance of a real circuit could, in principle, be matched to the input impedance of the amplifier. Subsequent calculations were carried out using finite source impedances. These indicate that the conclusions arrived at by using the zero-impedance source are also valid for finite-impedance sources.

Bias Network

Resistor values much greater than the maximum of 15,500 ohms used here would give rise to inordinately high parasitics and occupy an impractically large area if they were fabricated in a monolithic integrated form and therefore were avoided.

Emitter-Bypass Capacitors

The value of 150 pF used for the emitter-bypass capacitors pro-

[10] File No. 61 (9-66) RCA Semiconductor Products Databook, Electronic Components, Harrison, N. J.

[11] A. I. Stoller, "Calculation of the Electrical Parameters of Transistor Chips from Measurements Made on Packaged Devices," *RCA Review*, Vol. 29, p. 600, Dec. 1968.

Table I— y-Parameters: Columns A Give Values in Package as Shown in Published Data Sheets; Columns B Give Values for the Chip (All Values Are in Millimhos).

Frequency (MHz)	y_{11}				y_{12}				y_{21}				y_{22}			
	g_{11}		b_{11}		g_{12}		b_{12}		g_{21}		b_{21}		g_{22}		b_{22}	
	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
100	1.0	.64	5.0	4.2	0	0	— .3	— .1	46	48	—18	—14	.1	.1	1.0	0
200	2.5	1.8	7.0	5.6	0	0	— .9	— .5	40	46	—27	—20	.2	.4	1.8	0
300	6.5	5.2	9.0	8.0	0	0	—1.4	— .7	32	43	—32	—22	.3	.9	2.5	0
400	10.0	7.7	10.5	10.4	0	0	—1.8	— .8	25	38	—34	—22	.4	1.0	4.0	0
500	13.5	9.7	12.0	13.1	0	0	—2.3	—1.0	19	35	—36	—22	.5	1.3	5.5	.3
600	15.5	10.0	13.5	14.3	—.2	0	—2.7	—1.0	13	28	—34	—20	.6	1.4	6.5	.4
700	18.0	10.3	15.0	15.3	—.3	0	—3.0	—1.0	8	22	—32	—18	.8	1.4	8.2	.7
800	20.0	9.8	17.0	15.6	—.35	0	—3.3	—1.0	4	16	—29	—16	1.0	1.4	9.5	.9
900	22.0	8.8	19.0	15.2	—.4	—.16	—3.6	—1.0	3	11	—25	—11	1.2	1.4	11.0	1.3
1000	23.0	7.9	21.0	14.0	—.5	—.26	—3.8	—1.0	2	7	—20	— 8	1.4	1.3	12.3	1.5

vides a 10.8-ohm bypass at 100 MHz, the lowest frequency used in the analysis. Lower values of bypass capacitance were found to result in input impedances having a large negative real component at the lower frequencies, which could lead to instability in the amplifier. Since one side of each of the bypass capacitors is grounded, any parasitic capacitances from the bottom electrodes to the substrate would be short circuited and would not affect the response of the amplifier. Also, the voltages across these capacitors are low and of constant polarity. These noncritical requirements for the bypass capacitors can readily be met in an integrated circuit by using standard integrated capacitor structures, such as diffused junction capacitors, diffused MOS capacitors, or thin-film capacitors.

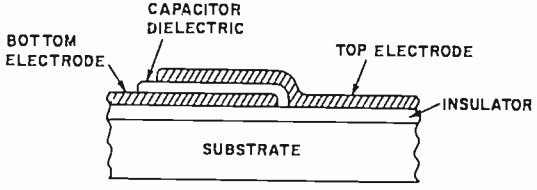

Fig. 2—Thin-film capacitance structure.

Coupling Capacitors

The requirements on the coupling capacitors are more restrictive than the requirements on the bypass capacitors. They should be low-loss capacitors capable of supporting the supply voltage, in this case 18 volts. Also, parasitic capacitances to the substrate must be kept small in order to avoid a shunting of the signal to ground at high frequencies. These requirements can be satisfied by a thin-film capacitance structure such as that shown in Figure 2.

Circuit Models Analyzed

The basic amplifier shown in Figure 1 was analyzed using the circuit analysis program compiled by Ressler,[12] assuming the various constructions described in the following paragraphs. The appropriate parasitics for each assumed construction technique were included in the computer program.

[12] D. G. Ressler, private communication.

Dielectrically Isolated Circuit

The dielectrically isolated model assumes that the circuit elements are completely isolated from each other and spaced and interconnected as if on a monolithic integrated-circuit chip. The Decal[1,2] or Air-Isolated Monolith (AIM)[8*] types of integrated circuit structures (in which the elements are essentially air isolated from each other) closely approximate the condition of ideal isolation. A discussion of the various types of dielectric isolation is beyond the scope of this paper, but can be found elsewhere.[1-9] For this analysis, the circuit of Figure 1 was used with no parasitics added. The transistor y-parameters for the chip (B columns of Table I) were used.

Discrete Transistor Circuit

The circuit of Figure 1 was re-analyzed, but this time the transistor y-parameters in the conventional hermetic package (A columns of Table I) were used. The purpose of this calculation is to determine the effect that the transistor package parasitics have on the circuit if packaged transistors are used in conjunction with an ideal thin-film passive network. Additional stray capacitances and inductances that are not taken into consideration here would be present in the interconnections of a discrete-component circuit. Therefore this model represents the most optimistic result possible for a discrete-component version of the amplifier.

Monolithic Integrated Circuit with Diffused Resistors

In a monolithic integrated circuit there are parasitic capacitances from the various components to the substrate that are associated with the p-n isolation junctions. The parasitic capacitances associated with the resistors typically have about 0.12 pF/mil^2 of isolation junction area. If we assume a resistor width of 0.0005 inch and a sheet resistance of 200 ohms/square, the parasitic capacitance to the substrate is 0.15 pF/kilohm of resistance.

For the transistors, the collector-to-substrate capacitance was estimated to be about 0.06 pF/mil^2 of isolation junction area. This corresponds to 1 pF/transistor, the value assumed in the calculations. It is also approximately the value that was both calculated and measured on the transistors of a commercially available rf integrated circuit.[13]

The value of the parasitic capacitance from the bottom electrode of

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* With beam leads.

[13] N. Rumin, private communication.

the coupling capacitor to the substrate depends on the area occupied by the capacitor, which in turn depends on the thickness and dielectric constant of the capacitor dielectric used. If the SiO_2 layer between the bottom capacitor electrode and the silicon is 1 micron thick and the capacitor dielectric (also SiO_2) is 0.1 micron thick, the parasitic capacitance will be 1/10 the value of the coupling capacitor, or 3 pF.

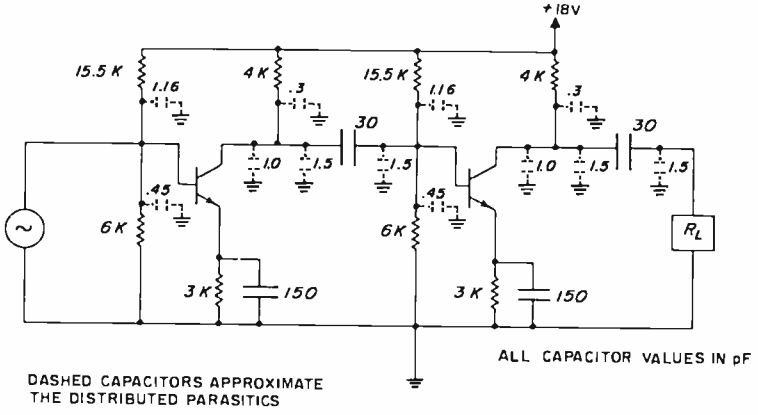

Fig. 3—Two-stage amplifier in monolithic configuration with diffused resistors.

In Figure 3 the circuit is shown with the parasitic capacitances added. A first-order approximation to the actual distributed nature of the parasitic is used, i.e., one half of the parasitic capacitance of each component is connected to each side of the component. Where one side of a component is ac grounded, that half-parasitic is not shown. Also the parasitics associated with the emitter resistors and bypass capacitors are assumed to be incorporated into the bypass-capacitor values, and these also are not shown.

Monolithic Integrated Circuit with Thin-Film Resistors

From Figure 3, it can be seen that a significant portion of the parasitic capacitance in the monolithic circuit is associated with the diffused resistors. Consequently, some improvement in the circuit performance can be achieved by using thin-film resistors rather than diffused resistors. This analysis assumes that the transistors are junction isolated, while the passive components, including the resistors, are all formed by thin-film techniques on the surface of a 1-micron-thick SiO_2 passivating layer. The resulting parasitic capacitance would be about 0.025 pF/mil^2 of resistor area, or, assuming the same resistor geometry as before, 0.031 pF/kilohm of resistance. This repre-

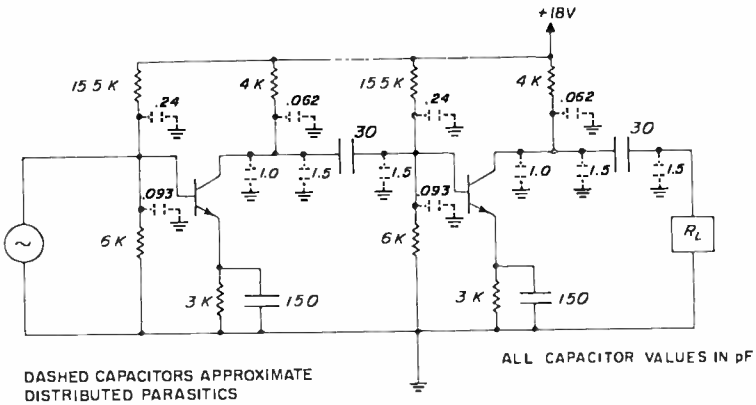

Fig. 4—Two-stage amplifier in monolithic configuration with thin-film resistors on top surface.

sents an 80% reduction in the resistor parasitics. Figure 4 shows the circuit with the appropriate parasitics, as used for this analysis.

Results of the Analyses

Each of the four circuit models described, was analyzed at intervals of 100 MHz from 100 MHz to 1 GHz. Each analysis was repeated using four different load resistors, 1000 ohms for the voltage gain computation, 50 ohms and 300 ohms for the power gain, and 1 ohm for the current gain. A 1-ohm load was used to determine the current gain, because the circuit-analysis program used in this work does not accept a short circuit.

For each type of gain computed, the response curves fell in the same sequence; dielectric isolation was best, followed in order by the discrete-transistor model, the thin-film resistor model, and the monolithic integrated circuit. The results are plotted in Figures 5-8.

Table II shows the relative gain at 500 MHz for each model of the circuit, with the dielectrically isolated model as a reference.

Table II—Relative Gain in dB at 500 MHz

	Voltage Gain (dB) R_L = 1000 ohms	Power Gain (dB) R_L = 50 ohms	Power Gain (dB) R_L = 300 ohms	Current Gain (dB) R_L = 1 ohm
Dielectric Isolation	0	0	0	0
Discrete Transistors	— 5	— 5	— 6.5	— 4
Monolithic Integrated Circuit with Thin Film Resistors	—14	— 6	—11.5	— 6
Monolithic Integrated Circuit, with Diffused Resistors	—16	—7.5	—13	—8.5

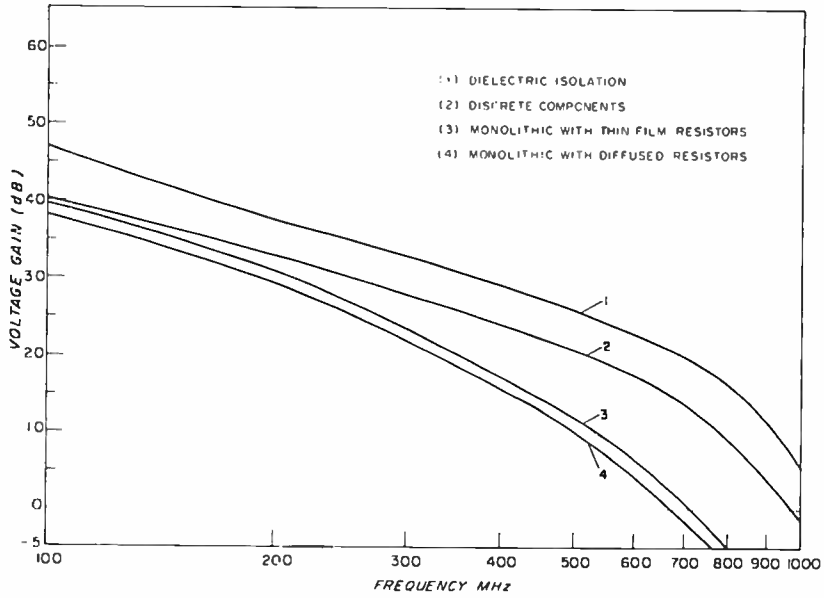

Fig. 5—Voltage gain versus frequency curves for various two-stage-amplifier constructions: $R_L = 1000$ ohms.

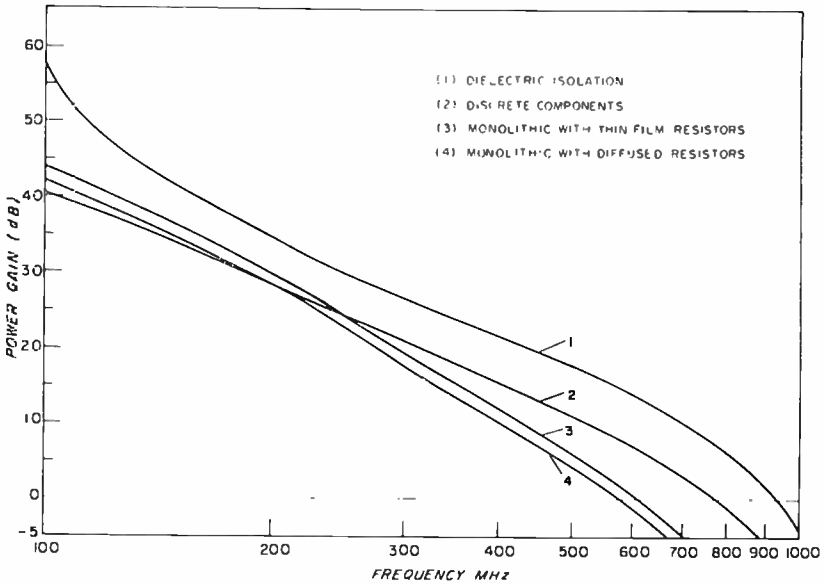

Fig. 6—Voltage gain versus frequency curves for various two-stage-amplifier constructions: $R_L = 300$ ohms.

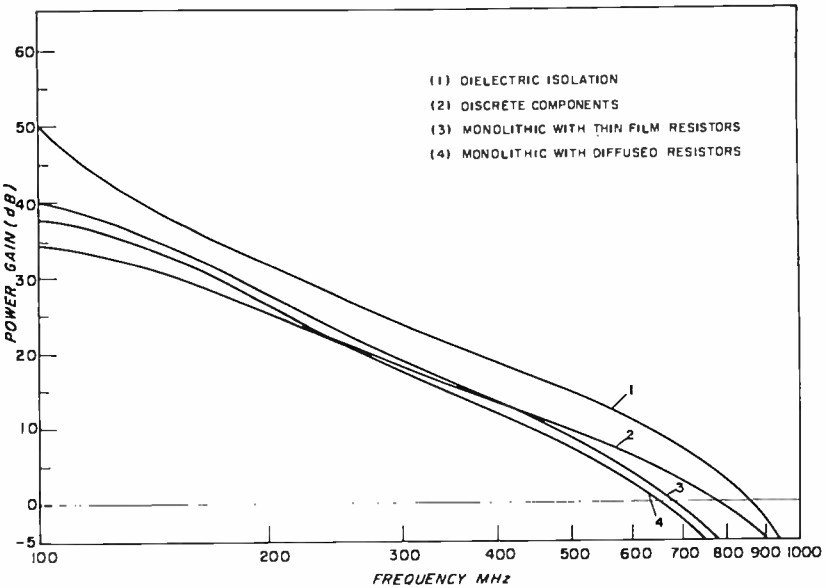

Fig. 7—Voltage gain versus frequency curves for various two-stage-amplifier constructions: $R_L = 50$ ohms.

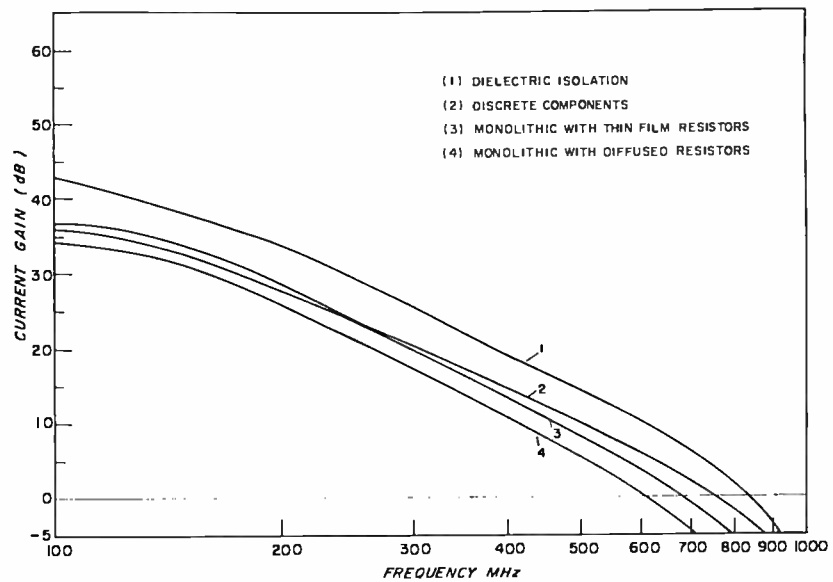

Fig. 8—Current gain versus frequency curves for various two-stage-amplifier constructions: $R_L = 1$ ohm.

Separation of the Parasitic Effects

There are three sources of parasitics contributing to the large spread between the curves for the dielectrically isolated circuit and the monolithic junction isolated circuit. The parasitics arise from the capacitors, transistors, and the resistors. To gain an appreciation for the relative importance of each group of parasitics, calculations were made of the effect on the voltage gain ($R_L = 1000$ ohms) versus frequency curves of the various parasitic components (see Figure 9).

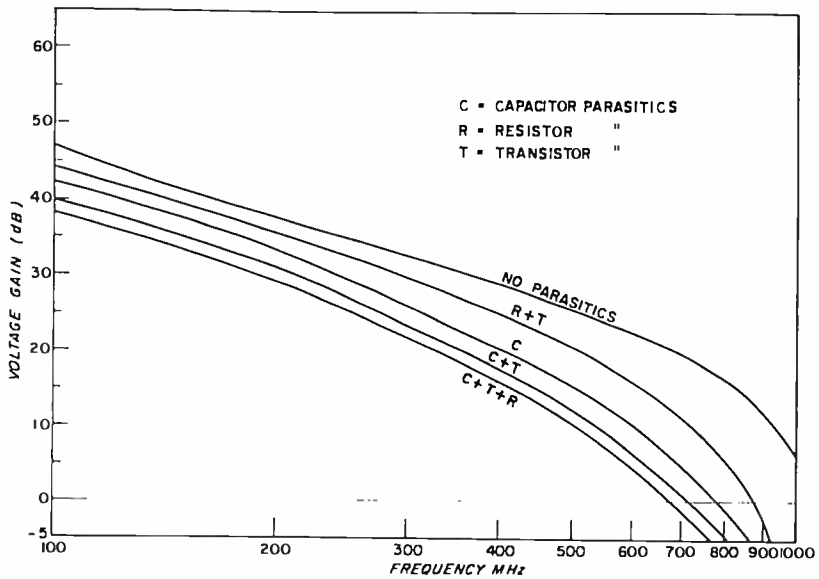

Fig. 9—Effect on various parasitics on voltage gain versus frequency curves ($R_L = 1000$ ohms).

These results, at 500 MHz and referred to the "ideal" isolation (case #1). are tabulated in Table III. The data provide evidence that the losses due to each type of component are additive to a first approximation, i.e., they are independent of the other losses present.

Table III—Loss Contribution by Component

Parasitics included	Relative gain in dB at 500 MHz	Loss due to each type of element
ideal isolation, no parasitics	— 0	
capacitor parasitics (C)	—10.5	C → —10.5 dB
capacitor + transistor parasitics (C + T)	—13.5	T → — 3.0 dB
capacitor + transistor + resistor parasitics (C + T + R)	—16.0	R → — 2.5 dB
transistor + resistor parasitics (T + R)	— 5.5	T + R → — 5.5 dB

Examination of these results leads to certain conclusions and design guide lines. Most of the parasitic loss in this circuit arises from the parasitics of the thin-film capacitors. Even if the resistors and transistors were isolated by an isolation technique based on the use of a polycrystalline silicon refill, most of the loss would still be present because of the parasitics from the lower capacitor plates to the polycrystalline silicon substrate. Therefore it would be best, when a circuit has such capacitors, to use an isolation technique, such as the Decal type of structure, that employs a true dielectric as the substrate.

If there were no capacitors to produce adverse parasitics in the circuit, a significant improvement could still be made by using a dielectric isolation technique to eliminate the transistor and resistor parasitics. Even without dielectric isolation for the transistors, some improvement can be made by using thin-film resistors to minimize the resistor parasitics.

The Effect of Resistor Width

The magnitude of the diffused resistor parasitics, and hence the extent to which they are deleterious to the circuit, depends strongly on the width of the resistors. Recent improvements in pattern delineation techniques have enabled integrated circuit designers to use resistor widths of 0.0005 inch or less, although in some cases wider resistors may be dictated by power-handling or tolerance requirements. Although the calculations thus far have been made on the basis of 0.0005 inch wide resistors, it would be instructive to examine the dependence of the results on resistor width. Table IV shows the influence of resistor width on the parasitic capacitance, again assuming a sheet resistivity of 200 ohms/square and an isolation junction capacitance of 0.12 pF/mil^2.

Table IV—Capacitive Contribution Due to Resistor Width

R width (mils)	mil^2 / 1000 ohms	pF / 1000 ohms
0	0	0 ← (Limit Values)
0.5	1.25	0.15
1.0	5.0	0.60
1.5	11.25	1.35

Using these values to determine the resistor parasitics, a set of voltage gain curves ($R_L = 1000$ ohms) were calculated for the case of monolithic, junction-isolated circuits. These curves (Figure 10) clearly show that the advantage of dielectric isolation increases with resistor width.

Packaging Effects

A discussion of performance versus circuit construction would not be complete without some consideration of how the circuit chip is interfaced with the rest of the circuit.

The traditional method of packaging integrated-circuit chips has been to mount them on a header, wire bond the contacts, and hermeti-

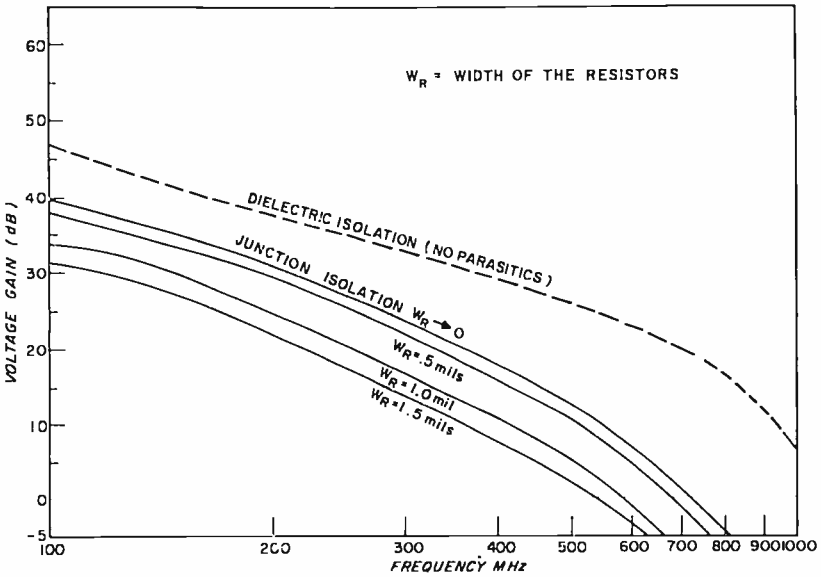

Fig. 10—Effect of resistor width on voltage gain versus frequency curves ($R_L = 1000$ ohms).

cally seal them in a can. There are, of course, several lead inductances and shunt capacitances associated with the package that have an effect on the overall performance of the circuit. To estimate the extent of this effect, we assumed that the circuit described earlier in this paper was mounted in a TO-72 package. This package was selected because it is the one commercially used for 2N2857 transistors. The parasitics associated with this package have been calculated previously.[11] The 2-stage amplifier with the package parasitics connected is shown in Figure 11. This configuration was analyzed both for dielectric isolation and for monolithic p-n junction isolation, each with 1-, 50-, 300-, and 1000-ohm loads. The results, which are compared to the unpackaged circuit data in Figures 12-15, demonstrate that one *cannot assume, a priori, that the package will always be harmful.* An improvement of the packaged circuit over the unpackaged version can be realized be-

cause the lead inductance of the package compensates for the input capacitance of the chip. This can be seen from the increase in voltage between the signal source and amplifier input in Figure 16. A small voltage increase between the amplifier output and the load resistor can also be seen. The same result, with a slightly increased output, is obtained when only the lead inductances are included and the package capacitances are omitted. Therefore, it appears that, for certain impedance conditions, it would actually be desirable to have the chip in a can, or to otherwise provide compensating inductances in series with the circuit terminals.

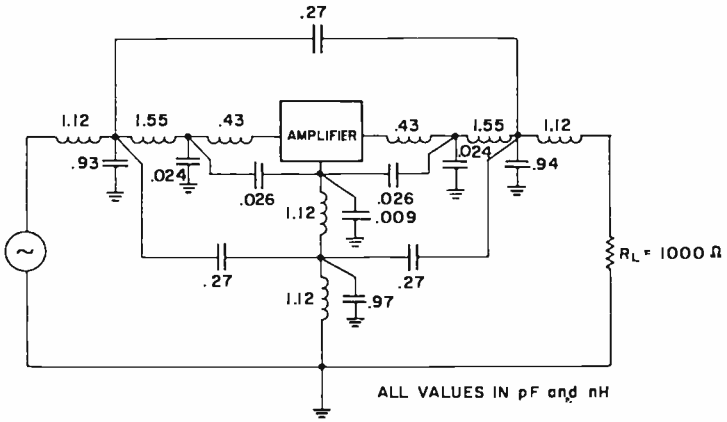

Fig. 11—Two-stage amplifier with parasitics of a TO-72 case added.

Where the surface-passivated chips are directly bonded, face down, to a circuit board,[14] it is possible to put a ground plane on the reverse side of the board to form a microstrip[15,16] interconnect pattern for impedance matching. Such a construction also permits some, or all, of the passive components to be fabricated on the circuit board by thick- or thin-film techniques. Because of this large number of possible wiring patterns and circuit-board materials, no attempt to calculate the effects of the parasitics of chips mounted on such circuits has been

[14] G. Sideris, "Bumps and Balls, Pillars and Beams: A Survey of Face-Bonding Methods," *Electronics*, Vol. 38, p. 68, June 28, 1965.

[15] M. Caulton, J. J. Hughes, and H. Sobol, "Measurements on the Impedances of Microstrip Transmission Lines for Microwave Integrated Circuits," *RCA Review*, Vol. 27, p. 377, Sept. 1966.

[16] A. Schwarzmann, "Microstrip Plus Equations Adds Up to Fast Designs," *Electronics*, Vol. 40, p. 109, Oct. 2, 1967.

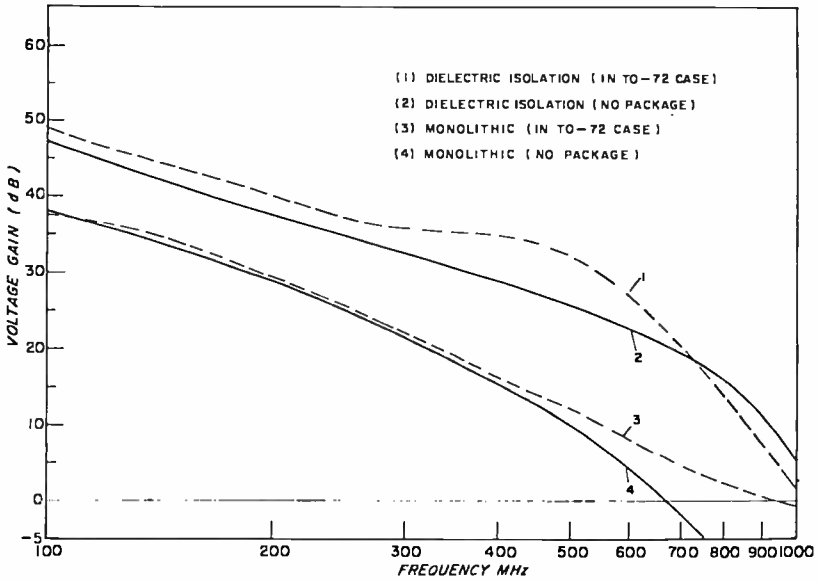

Fig. 12—Effect of TO-72 package on two-stage-amplifier performance: $R_L = 1000$ ohms.

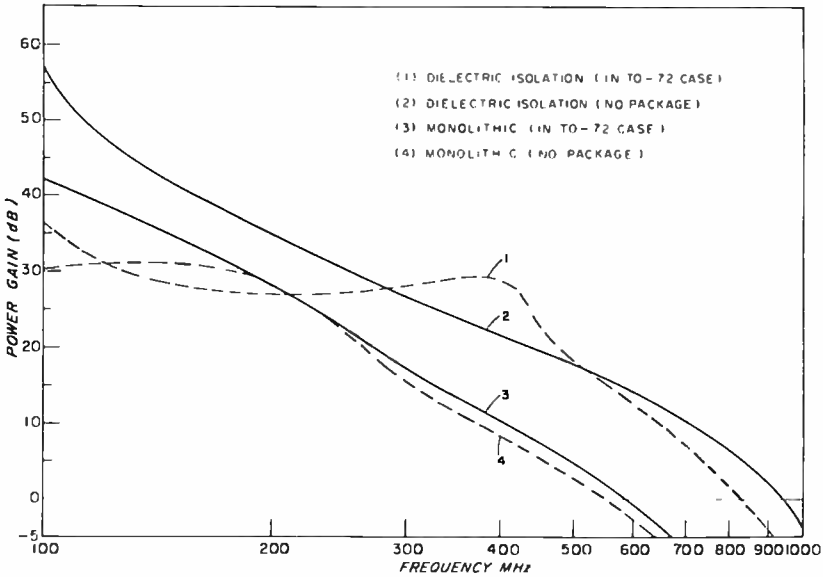

Fig. 13—Effect of TO-72 package on two-stage-amplifier performance: $R_L = 300$ ohms.

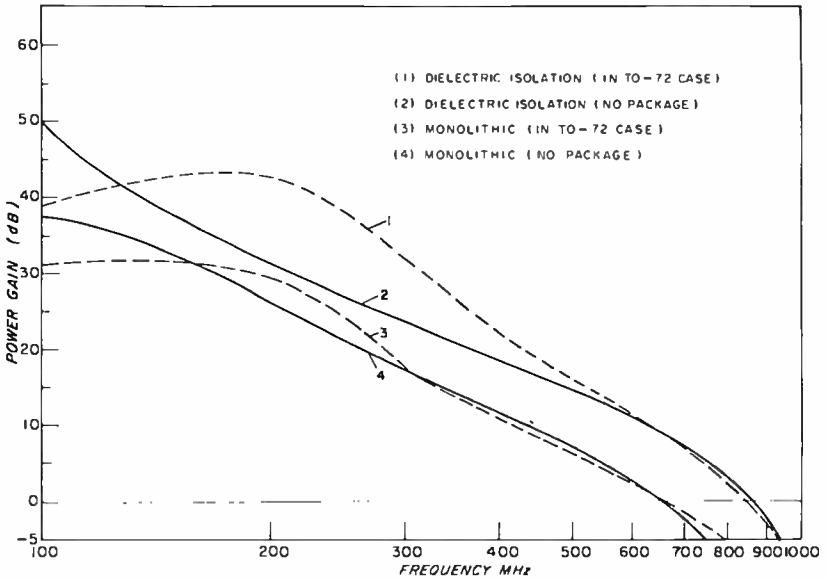

Fig. 14—Effect of TO-72 package on two-stage-amplifier performance: $R_L = 50$ ohms.

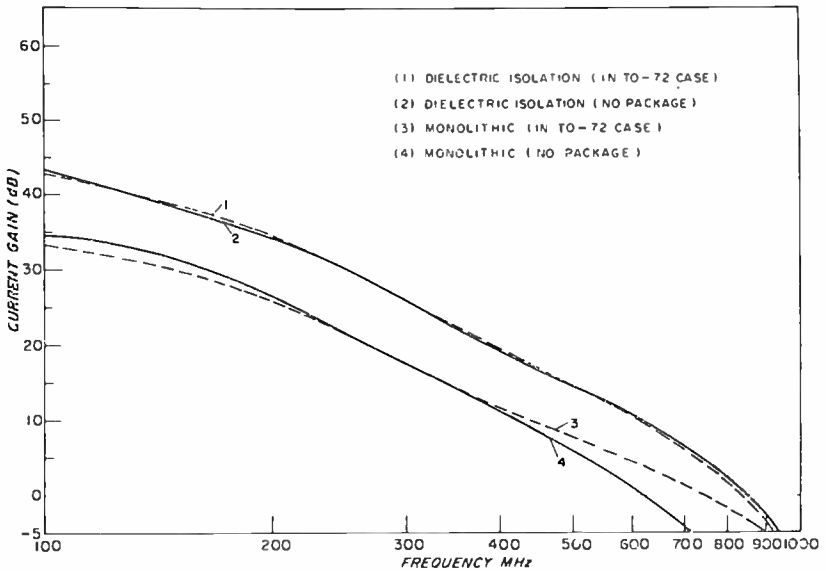

Fig. 15—Effect of TO-72 package on two-stage-amplifier performance: $R_L = 1$ ohm.

carried out. Such circuits do, however, afford the possibility of including in the wiring patterns compensating inductances with minimal parasitic shunt capacitances.

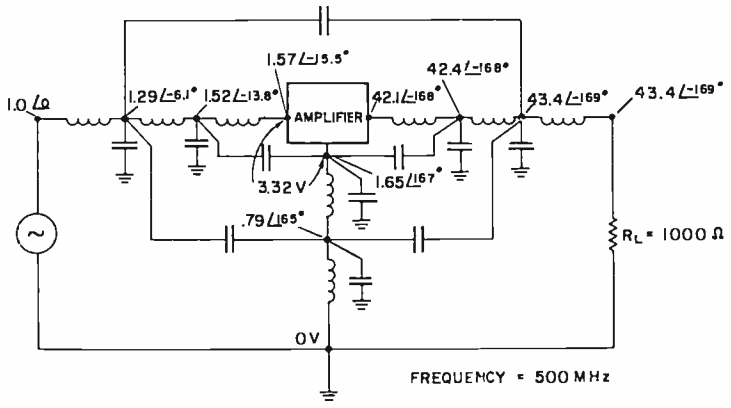

Fig. 16—Node voltages of a two-stage dielectrically isolated amplifier with parasitics of a TO-72 case added.

Discussion and Conclusions

The calculations described here demonstrate that a dielectrically isolated structure for a standard type of linear amplifier provides high-frequency performance substantially superior to the performance of the same amplifier in a monolithic integrated form. The voltage, current, and power gains are improved between 7 and 16 dB for the dielectrically isolated configuration, and the frequency at which the absolute value of the gain falls to unity is increased by approximately 40%.

It was also determined that a small improvement in gain (2-3 dB) over the monolithic circuit can be made by using thin-film resistors in the circuit rather than diffused resistors when the active devices are junction-isolated. This difference is greater if the diffused resistors are wider than 0.0005 inch, the dimension assumed in most of the calculations. Since thin-film resistors may provide other advantages as well, this approach should not be overlooked for applications where modest improvements over the monolithic structure are required.

An analysis was also carried out to determine the effect that the transistor package parasitics would have on the circuit performance if discrete packaged transistors were used. A degradation of 4 to 7

dB in gain, compared with the dielectrically isolated case, represents the most optimistic performance attainable for a discrete component circuit, since the parasitics of the interconnections and the discrete passive components would cause a further degradation in the response. If, however, an integrated-circuit chip is put into the same type of package as that used for the discrete transistor, the lead inductances actually improve the response in some frequency ranges by providing a compensation for the input capacitance of the circuit.

Although these results were obtained for a specific circuit, the conclusions should be generally applicable to linear integrated circuits.

Acknowledgments

The author gratefully acknowledges the cooperation of D. Ressler in providing and implementing the computer program used in this work, the helpful discussions with L. Napoli, and the support and critical review of the manuscript provided by N. E. Wolff and J. A. Amick.

APPARATUS FOR CHEMICAL VAPOR DEPOSITION OF OXIDE AND GLASS FILMS

By

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Summary—An apparatus is described for the formation of dielectric films by chemical vapor deposition reactions in the temperature range of 250 to 500°C. The apparatus consists essentially of a heated gear assembly that rotates the substrates in planetary fashion. A commercial high-temperature hot plate is used as the heat source. Reaction takes place in a glass chamber having several inlet ports for the gases. An opening between the chamber and the hot-plate surface serves for the exhaust.

The apparatus affords a high degree of control and reproducibility for depositions. It yields highly uniform films of a variety of oxides, especially doped silicon dioxide layers and various silicate glasses.

INTRODUCTION

IN RECENT YEARS the formation of dielectric films by chemical vapor deposition techniques has found many important applications in the fabrication and passivation of solid-state components.[1-3] Two outstanding advantages of this type of deposition process are the low temperatures at which dielectric films of high melting points can be prepared, and the high purity that can be achieved in the deposited layers.[4,5]

Chemical vapor deposition in semiconductor processing applications is usually conducted in resistance- or induction-heated quartz-tube furnaces. The device wafers are placed in the tube and the gaseous reactants are passed over them. Reaction conditions are optimized for heterogeneous nucleation on the substrate surface leading to uniform

[1] C. F. Powell, J. H. Oxley, and J. M. Blocher, Jr., Editors, *Vapor Deposition*, John Wiley & Sons, Inc., New York, 1966.

[2] T. L. Chu, "Chemical Deposition of Dielectrics for Thin Film Circuits and Components," *SCP and Solid State Tech.*, p. 36, May 1967.

[3] R. M. Burger and R. P. Donovan, Editors, *Fundamentals of Silicon Integrated Device Technology*, Vol. I, Prentice-Hall, Inc., Englewood Cliffs, N. J., 1967.

[4] N. Goldsmith and W. Kern, "The Deposition of Vitreous Silicon Dioxide Films from Silane," *RCA Review*, Vol. 28, p. 153, March 1967.

[5] W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Paper No. 92 presented at the 1968 Spring Mtg., ECS, Boston, Mass.

film deposits that possess the desired properties. It is usually difficult to achieve uniform deposits consistently, especially if several substrate wafers are processed simultaneously. Part of the difficulty is due to changes in composition of the reactant gas mixture as it passes through the tube. The creation of uniform turbulance in the gas mixture (to avoid stratification and the formation of symmetric gas-flow patterns) is also difficult.

The apparatus described in this paper was designed to overcome these problems. It utilizes inexpensive, commercially available resistance heating equipment and was so designed that it can readily be constructed from standard components.

The principle of the deposition technique upon which the apparatus is based is simple. The substrate wafers lie on a hot plate covered by a glass chamber. A mixture of reactant and diluent gases passes over them. On contact with the heated substrates, the gases react forming a deposit. Several apparatus built to different designs were tested for various applications. The parameters for depositing vitreous silicon dioxide from silane and oxygen in three different apparatus have been presented in a previous paper.[4]

The apparatus defined in that paper as an "intermediate-size system" has proven satisfactory for laboratory use and is described in detail in the present paper. It differs from the other two systems in several respects.

(1) During deposition, the substrates are rotated in a planetary fashion to give superior film uniformity,

(2) The substrates can be brought to higher temperatures,

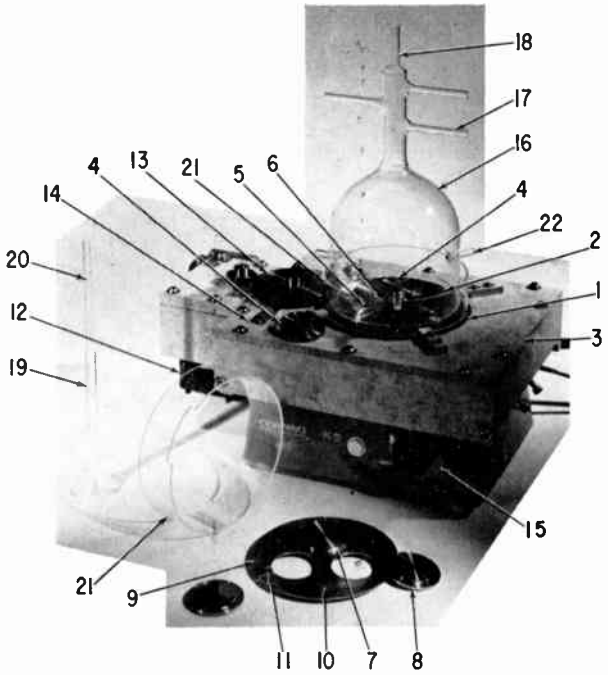
(3) Provision is made for various modes of gas introduction; this offers greater versatility in optimizing specific conditions for a given application,

(4) The reaction chamber does not include a fritted glass disk. Such disks, used on earlier apparatus, tend to clog during use and also lead to contamination.

(5) The gas exit opening of the reaction chamber is circularly symmetric, which leads to a more uniform gas flow over the substrate.

Description of Apparatus

The photograph in Figure 1 shows the partly assembled apparatus; the numbers refer various components to the discussion in the text. Figure 2 shows the fully assembled apparatus ready for connection to the gas distribution system.



1 Gear Anchoring Plate
2 Large Hot-Gear
3 Thermal Insulation Plate
4 Small Hot-Gear
5 Opening for Shaft of Small Hot-Gear
6 Stationary Pinion (covered)
7 Sample Holder
8 Base of Sample Holder
9 Gear Cover Disc
10 Positioning Post
11 Slot
12 Electric Motor
13 Intermediate Gear
14 Adjustable Gear Base
15 Temperature Dial
16 Reaction Chamber
17 Horizontal Gas Inlet Port
18 Vertical Gas Inlet Port
19 Adjustable Gas Inlet Funnel
20 Sliding Fit
21 Reaction Chamber Support Ring
22 Support Rod

Fig. 1—Partly assembled Apparatus showing component parts.

Heat Source

A 600-watt ceramic-top hot plate is used as heat source. Maximum operating temperatures can be obtained if a thermal insulation cover is used to minimize heat losses. The substrate temperature that the fully assembled apparatus is capable of achieving is typically 480°C.

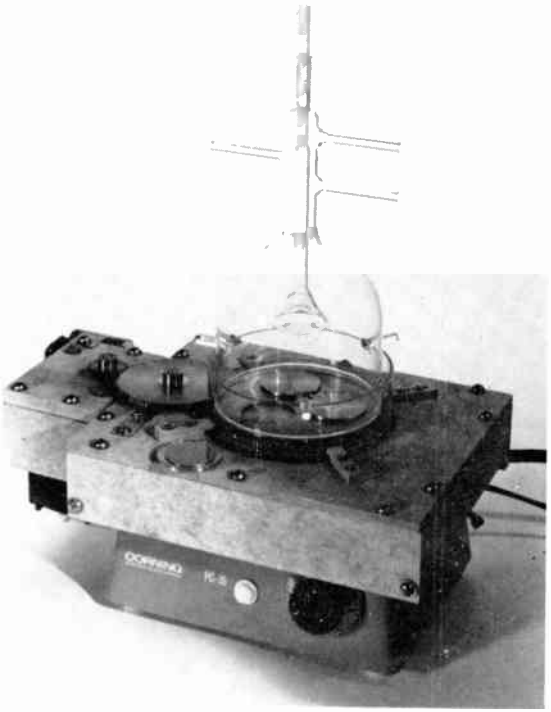


Fig. 2—Assembled apparatus.

Gear Anchoring Plate

A flat, polished steel disk (1 in Figure 1) with a slotted center hole anchors a pin on which the large hot-gear (2) rotates. The pin also supports the stationary pinion that drives the small hot-gears seen in Figure 1.

Originally, a sheet of oxidation-resistant graphite was used to attain maximum heat transfer as well as to provide lubrication for the sliding gears. However, the long-term stability of the graphite at high temperature was unsatisfactory. Thermally stable alloys containing copper have excellent thermal conductivities but are undesirable for

semiconductor applications because of potential copper contamination. Steel has proven to be a satisfactory alternative despite its considerably lower thermal conductivity.

The gear-anchoring plate is secured to a thermal insulator plate (3) with a circular cutout holding it in place. The plate is cut in two at the most narrow point to allow for thermal expansion on heating and covers the entire surface and the sides of the hot-plate top to minimize heat losses. It also acts as a safety cover to protect the operator in case of accidental contact.

Hot-Gear Assembly

A large-diameter metal gear (2) is loosely held in place by the pin and rotates on the anchoring plate. Three smaller gears (4) with shaft are loosely inserted in openings (5) spaced 120° apart on the large hot-gear. They are driven by the stationary pinion (6) attached to the fixed shaft of the large hot-gear. The resulting motion of the substrates on the small hot-gears is therefore a planetary rotation. Without this type of motion, uniformity of the deposits is poor. The small hot-gears have a narrow rim machined in the top surface to hold the sample pedestal in place.

Sample Holders

The pedestals (7) supporting the substrates are constructed with a rim that prevents the substrates from sliding off. The pedestals are designed to accommodate circular substrates up to 1.5 inch in diameter. The base (8) of these disks is smaller than the top so that they fit in the depressed surface of the small hot-gears where they are loosely held in place by the narrow rim.

One of the purposes for having separate, removable sample holders is to allow placing of substrates on the holder at room temperature outside the chamber. The loaded holders are then introduced in the preheated apparatus and are allowed to equilibrate thermally while being purged with nitrogen. This technique is essential in processing metallized device wafers that would oxidize if placed directly on the hot-gears.

Gear Cover Disk

To eliminate contamination of the substrates by particulate matter a thin disk (9) is used to cover the gear assembly within the deposition chamber. This disk is optional and is required only in the most exacting applications. It has three positional posts (10) that fit loosely in depressions in the large hot-gear to hold the disk in place. A slot (11)

is cut between the edge of the disk and each of the windows to avoid thermal warping.

Drive Mechanism

A synchronous motor (12) with a suitable gear train drives the large hot-gear. The motor is mounted on the side of the hot plate between thermal insulation plates and is attached to the hot-plate cover. This results in excellent thermal insulation between the motor and the hot plate. An intermediate gear (13) mounted on an adjustable base (14) transfers the motor motion to the large hot-gear.

It should be pointed out that all components of the turntable assembly are machined with loose fits to allow for thermal expansion during cycling; in this way binding or warping of the parts is avoided.

Temperature Control

A continuously variable dial setting (15) on the hot plate allows reasonably accurate and reproducible temperature control for applications where the temperature is not very critical. It is convenient to establish a calibration curve that relates various dial settings to the surface temperature of the substrates under thermal equilibrium conditions. Temperatures for a given calibrated setting were found reproducible to within approximately ±5°C over operating periods of several months. Calibrated bimetallic surface thermometers and thermocouples are used to check the surface temperature of the substrates.

For applications where a more accurate temperature control is required, or where fluctuations in the line voltage are known to occur, an auxiliary temperature controller can be used. A chromel–alumel thermocouple in a ceramic tube is inserted in a groove in the gear anchoring plate. The temperature between the substrate surface and the thermocouple are correlated and maintained constant by a suitable temperature controller.*

Reaction Chamber

The reactant gas mixture is introduced to the top of the bell-shaped glass reaction chamber (16) shown in Figures 1 and 2. The diameter of the reaction chamber is slightly smaller than that of the large hot-gear. The gases may be introduced separately through the inlet ports

* e.g., A Model 712 API, Type K, Time Proportioning Controller (API Instruments Co., Chesterland, Ohio) for a 0 to 800°C range employing chromel–alumel thermocouple sensors.

(17), or premixed. The vertical inlet (18) has an adjustable funnel (19) with a sliding fit (20) permitting different geometries to be achieved for various applications. This center inlet port is commonly used for introducing the oxygen.

Eight- to ten-inch lengths of Teflon tubing are used to connect the inlet ports of the reaction chamber to the stainless steel tubing of the gas-metering system. Because of their good thermal insulating efficiency, Teflon fittings are also recommended for connecting the flexible tubing to the glass tubing of the chamber inlet ports.

Reaction Chamber Support Ring

A glass ring (21) supports the reaction chamber on three horizontal support rods (22). The ring is positioned outside the large hot-gear and is of such a height that a nearly circularly symmetric opening of approximately 0.05 inch is formed between the bottom edge of the chamber and the surface of the hot gear. The support ring also prevents air drafts from entering the reaction chamber where they might disturb the gas flow.

Gas Distribution System

The gas metering, mixing, and distributing system is set up to meet the particular process requirements. Diagrams and relevant details for specific applications have been published in separate papers.[4-6,9] However, a few general remarks are included here.

Pure, diluted, or mixed gases, or carrier gases with vapors of liquid sources, are metered and distributed through glass and/or stainless steel tubing. Usually, oxygen (used as oxidizing agent) is introduced separately into the reaction chamber. Other gases and vapors are premixed either in the cylinder or just before entering the reaction chamber. Although the reaction chamber is open to the atmosphere, all gas distribution lines—from the source cylinders to the chamber inlet ports—should be leak tight to prevent prereaction of the gases in the lines. Back diffusion of air into the reaction chamber during operation is minimized by employing an inert diluent-gas flow rate of typically several liters per minute. Back diffusion in the lines during nonoperating conditions is avoided by use of shutoff valves and by maintaining the system under positive pressure of inert gas.

APPLICATIONS

This apparatus has been used for the controlled deposition of silicon dioxide from silane and oxygen, as described in an earlier paper.[4] The

deposition of binary and ternary silicate glasses using the apparatus has also been described recently,[5] and a description of the deposition of boron and phosphorus-doped silicon dioxide films is included in this issue of *RCA Review*.[6] Oxide films of tantalum and niobium have been deposited pyrolytically from their penta-ethylates by use of the apparatus.[7] The deposition and applications of aluminum oxide films by chemical vapor reaction of trimethyl aluminum and oxygen in this apparatus is described in a separate paper.[8] Films of zinc oxide have been deposited by oxidation of diethyl zinc.[5]

One of the more important advantages of the apparatus is the capability of depositing very uniform films. This is achieved mainly by the planetary substrate rotation, which tends to smooth out substrate temperature differences and gas flow differences near the substrate surface. Typical examples of the uniformity of film thickness that can be achieved on polished silicon wafers are: silicon dioxide deposited over a 1.5-inch-diameter substrate measured 6000 ± 200 Å;[4] a thick layer of borosilicate deposited over a 1.3-inch-diameter substrate measured 72,300 ± 1,500 Å.

Conclusions

An apparatus has been described for the controlled deposition of films by chemical vapor reactions for substrate temperatures up to 500°C. The apparatus is intended primarily for the deposition of oxide and glass films on semiconductor substrates up to 1.5 inches in diameter.

Particular advantages of the apparatus include the following: (1) highly uniform films ranging from a few hundred angstroms to several microns can be deposited; (2) substrate surface temperatures can be maintained constant to within a few degrees during deposition; (3) visual observation of the substrate during deposition is provided; and (4) films free of particulate contaminants are obtained.

Acknowledgments

I would like to thank W. H. Morewood for his contributions in the design of the mechanical parts and A. P. Goodlad for his suggestions for constructing glass reaction chambers.

[6] A. W. Fisher, J. A. Amick, H. Hyman, and J. H. Scott, Jr., "Diffusion Characteristics and Applications of Doped Silicon Dioxide Layers Deposited from Silane," *RCA Review*, Vol. 29, p. 533, Dec. 1968.

[7] M. T. Duffy, K. H. Zaininger, and C. C. Wang, "Preparation, Optical and Dielectric Properties of Tantalum Oxide and Niobium Oxide Thin Films," Paper No. 17 presented at the 1968 Spring Mtg., ECS, Boston, Mass.

[8] W. Kern and E. D. Savoye, "Deposition and Properties of Aluminum Oxide Films Deposited by Chemical Vapor Reaction from Trimethyl Aluminum," to be published.

DIFFUSION CHARACTERISTICS AND APPLICATIONS OF DOPED SILICON DIOXIDE LAYERS DEPOSITED FROM SILANE, (SiH_4)

BY

A. W. FISHER*, J. A. AMICK*, H. HYMAN†, AND J. H. SCOTT*, JR.

Summary—Oxide layers deposited from mixtures of silane, oxygen, argon, and a suitable hydride dopant, e.g., phosphine or diborane, serve as controlled, reproducible diffusion sources in the fabrication of silicon devices. The oxide layers behave essentially as constant-level reservoirs of dopant, and simplify the processing steps involved in device preparation.

INTRODUCTION

DIFFUSION techniques presently employed in the fabrication of silicon transistors and integrated circuits have a number of disadvantages. Diffusion sources are commonly deposited in essentially pure form, either as phosphorus oxide or boron oxide, on the surface of the wafer. Before a final drive-in heat treatment, this surface oxide layer is removed by etching, leaving a finite amount of the dopant in a shallow surface layer of the silicon. If the etching process is incomplete, if an oxide layer is present on the surface of the silicon prior to the deposition, or if the oxide layer is not uniform in composition, sheet resistivities across a wafer may vary significantly, and results from run to run will not be reproducible; as a result, device yields will be lowered. Furthermore, since concentrations approaching the solid solubility for the dopant in silicon are present, crystalline defects, especially edge dislocations, may be introduced in large numbers.[1] These, in turn, influence the diffusion coefficient for the dopant as well as minority-carrier lifetime and mobility in the surface regions.[2]

The use of solid–solid diffusion sources, such as vapor-deposited silicon dioxide layers containing controlled concentrations of doping

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[1] Cf. J. M. Fairfield and G. H. Schwuttke, "Strain Effects Around Planar Diffused Structures," *Jour. Electrochem. Soc.*, Vol. 115, p. 415, April 1968.

[2] K. H. Nickolas, "Studies of Anomalous Diffusion of Impurities in Silicon," *Solid-State Electronics*, Vol. 9, p. 35, Jan. 1966.

impurities, provides a means of overcoming many of these problems. The dopant concentration in a deposited oxide layer can be varied over a wide range to give any desired surface concentration in the silicon. This surface concentration is nearly independent of the length of the diffusion cycle since, for shallow diffusions, the oxide acts as a constant-level reservoir for the dopant. Surface concentrations in the silicon are always below the solid solubility for the dopant. As a result, a minimum number of dislocations is introduced during diffusion. Furthermore, the oxide containing the dopant is generally not etched away prior to a drive-in step. Instead, it is retained throughout the processing of the device, simplifying the fabrication procedure and making the device less sensitive to contaminants present in the furnace during diffusion.

Olmstead and Scott have reported on the use of doped oxides deposited from organo-silanes as diffusion sources.[3] In their work, deposition temperatures of about 700°C were employed and only one or two wafers at a time could be accommodated. To increase the number of wafers on which deposition occurs simultaneously and to simplify the deposition process, a reaction taking place at a lower temperature is desirable. A lower-temperature reaction would also minimize diffusion of dopants into the silicon during the deposition step. Preliminary data on the use of doped oxide layers deposited from silane has been given by Mecs.[4] The present paper gives more detail on a low-temperature technique for preparing solid-solid diffusion sources suitable for silicon device fabrication, based on the use of gaseous hydrides as reagents.[5]

Experimental

Reactions employed

The chemical vapor deposition of silicon dioxide layers from a silane–oxygen–inert-gas mixture has been described by Goldsmith and Kern.[6] They employed the reaction*

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O\uparrow$$

[3] J. Scott and J. Olmstead, "A Solid-to-Solid Diffusion Technique," *RCA Review*, Vol. 26, p. 357, Sept. 1965.

[4] B. M. Mecs, "Oxidized SiH_4 as a Diffusion Source," Abstract #93, Electrochem. Soc. Mtg., Boston, Mass., May 1968.

[5] Cf. also M. L. Barry and P. Olofsen, "Advances in Doped Oxides as Diffusion Sources," *Solid State Tech.*, Vol. 11, p. 39, Oct. 1968.

[6] N. Goldsmith and W. Kern, "The Deposition of Vitreous Silicon Dioxide Films from Silane," *RCA Review*, Vol. 28, p. 153, March 1967.

* Recent work by Strater suggests that the reaction is $SiH_4 + O_2 \rightarrow SiO_2 + H_2\uparrow$ at the dilutions employed in this work.

to form smooth, highly uniform layers of vitreous silicon dioxide at temperatures in the neighborhood of 400°C.

If a suitable hydride such as phosphine or diborane is introduced into the reactant gas stream, phosphorus or boron oxides are formed and incorporated uniformly into the silicon dioxide layer as it is deposited. Like silane, phosphine and diborane have low boiling points (Table I) and their vapor pressures at room temperature are high enough so that, even in cylinders pressurized at 2000 psi, they are still gaseous.

Table I

Reactant	Boiling Point
PH_3	— 87.7°C
B_2H_6	— 96.5°C
SiH_4	—111.9°C

If they are stored as diluted gas mixtures stored in cylinders, there is no chance of accidental contamination of the hydrides. Precise metering of gases is relatively easy so that doped oxide layers of controlled composition and high purity can be prepared readily.

Phosphine diluted in argon is stable in composition indefinitely. For diborane, however, a polymerization to higher molecular weight, lower vapor pressure boranes takes place slowly with time. The boron content of gas taken from a cylinder decreases with time, thus lowering the boron content in deposited oxide layers formed from the gas. When nitrogen is employed as a diluent, the diborane content is found to decrease by about 10% per year, independent of the initial diborane concentration. Changes of this order are not a serious problem if the cylinders are used within a reasonable time following their preparation, or if an analysis of the contents is obtained just prior to use.

The deposition rate for a deposited oxide layer may be lowered if there is an appreciable concentration of higher boranes in the cylinder as received. Consequently, the concentration of these higher boranes should be as low as possible, preferably below 5 mole% of the diborane content, when cylinders are ordered.

The temperatures employed in the deposition of doped oxide layers are in the neighborhood of 325°C, so that diffusion of the dopant into the silicon during deposition is negligible. If desired, oxide layers may be deposited directly on a silicon wafer and then removed by selective etching procedures without leaving appreciable quantities of dopant in the silicon.

The gaseous reagents used include:

silane (SiH_4) diluted to 10% by volume in argon†
phosphine (PH_3) diluted to 100 ppm by volume in argon*
phosphine diluted to 1000 ppm by volume in argon*
phosphine diluted to 100,000 ppm by volume in argon*
diborane (B_2H_6) diluted to 100 ppm by volume in argon*
diborane diluted to 1000 ppm by volume in argon*
diborane diluted to 100,000 ppm by volume in argon*
nitrogen (high purity cylinder gas)
oxygen (standard cylinder oxygen)

The silicon used in this work was in the form of 1-2 ohm-cm n- and p-type, Lustrox-polished wafers, about 1.125 inches in diameter#. Half wafers were normally used as samples, but where 1-hour and 2-hour diffusion results are given, the deposition was carried out on the complete wafer, which was then divided in two. This procedure eliminates potential variations in the oxide from run to run.

Apparatus

Oxide depositions were carried out in an apparatus similar to that described by Kern[7,8] with a thermocouple-controlled time-proportioning on–off relay circuit‡ controlling the hot plate. It is estimated that the substrate temperatures during deposition are controlled to ±5°C, depending on gas flow. Three separate deposition systems, one for phosphorus-doped SiO_2, one for boron-doped SiO_2, and one for undoped SiO_2, were installed in a single six-foot-wide fume hood with partitions between each of the systems to minimize cross contamination.

All gas flows were monitored with flowmeters$^\Delta$ and controlled with Teflon-tipped needle valves.$^\Delta$ The flowmeters were checked for accuracy against a wet-test meter and found to agree with the calibrations supplied by the manufacturer to better than ±10%.

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† Matheson Co., East Rutherford, N. J.

* Air Reduction Sales Co., Union Landing Rd., Riverton, N. J.

Texas Instruments Inc., Dallas, Texas

[7] W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Abstract #92, Electrochem. Soc. Mtg., Boston, Mass., May 1968.

[8] W. Kern, "Apparatus for Chemical Vapor Deposition of Oxide and Glass Films," *RCA Review*, Vol. 29, p. 525, Dec. 1968.

‡ Assembly Products, Inc., Newton Square, Pennsylvania

$^\Delta$ Fischer and Porter Co., Warminster, Pa.

All drive-in diffusions were carried out in a three-zone electrically heated furnace, each zone being independently temperature controlled by stepless controllers. Both phosphorus and boron diffusions were carried out in the same furnace in a nitrogen flow of 30 cm^3/min.

Sheet resistivities were measured with a 4-point probe; junction depths were determined by angle lapping and staining.

Procedure

(1) Wafer preparation

Inadequate or improper cleaning of silicon wafers prior to chemical vapor deposition of an oxide layer results in a visibly nonuniform deposit, and diffusions from such sources give nonuniform results. Sheet resistivity may vary by more than ±15% across a wafer. It is therefore important to employ procedures that minimize organic and inorganic residues. For this purpose, a treatment in hot organic solvents followed by immersion in hot chromic-sulfuric acid is satisfactory.

Following cleaning, approximately 20 Å of silicon dioxide is present on the silicon surface. If this oxide layer is left on the surface, a doped oxide layer is deposited over it and a drive-in diffusion is carried out, the resulting sheet resistivities will be about 20% higher than if the oxide layer is removed in an HF rinse immediately prior to the doped deposition. However, as long as one is consistent in including or omitting a terminal HF rinse, reproducible results are obtained for phosphorus-doped layers. For boron-doped layers the uniformity in sheet resistivity is much better if the HF rinse is included.

(2) Deposition

Depositions are carried out in the following sequence.

All gases are turned on in the sequence N_2, O_2, SiH_4, and dopant, and are adjusted to proper flow for the desired oxide composition. The hydrides are mixed together and introduced into the flowing nitrogen, upstream from the reaction chamber. At the entrance to the reaction chamber, the oxygen is introduced through a side tube into the diluted hydride mixture.[7]

For nearly all depositions, the nitrogen and oxygen flows were kept constant at 7 liters per minute and 25 cm^3 per minute, respectively. This high nitrogen to oxygen ratio minimizes pre-reaction in the gas phase. Silane flows were about 75 cm^3 per minute of 10% silane in

argon or about 7.5 cm^3 per minute based on pure silane. This gives an oxygen to silane ratio of about 3:1, as recommended by Goldsmith and Kern.[6] When deposited oxides very lightly doped with boron or phosphorus were prepared, the silane flow had to be increased. To maintain the 3:1 ratio under these conditions, the oxygen flow was raised correspondingly but never exceeded 45 cm^3 per minute.

To ensure that the gas composition is uniform, the system is allowed to purge at least 5 minutes. During this period, the reaction chamber is placed to one side and behind the apparatus so that the gases flowing out of it do not come into contact with the apparatus.

While the chamber is purging, test chips are loaded into position on the hot plate, the rotation of the holders is started and a 3-minute interval elapses to permit the wafers to reach a temperature of about 340°C in air.

With the gases still flowing, the reaction chamber is placed over the (moving) heated test chips; doped SiO_2 immediately begins depositing onto the surface of these chips.

After 3000 Å of doped oxide are deposited, as determined by visually monitoring the interference color, the doping gas is shut off and an additional 3200 Å of undoped "capping" oxide is deposited on top of the doped oxide.

The undoped capping oxide is employed for several reasons. First, the oxide tends to seal the surface so that out-diffusion of dopant during the drive-in step is minimized. Furthermore, the undoped oxide helps to prevent contamination of the doped oxide layer by material from the walls of the diffusion furnace. Finally, photoresist layers generally adhere better to the surface of an undoped oxide than to the surfaces of doped layers, especially when phosphorus is present as the dopant.

All test chips were diffused at 1200°C in nitrogen (30 cm^3 per minute) for intervals up to three hours. Following diffusion, the oxide was stripped from the surface with aqueous HF, and sheet resistivities were calculated from an average of 5 readings taken in representative edge and center areas.

Samples were then angle-lapped on a glass plate with Linde "C" abrasive,* a 3° angle lapping fixture being used. From the information obtained by measuring sheet resistivity and junction depth, the surface concentration of the diffused region was calculated assuming an error function (ERFC) relationship.

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* Electronics Division, Union Carbide Corp.

Results and Discussion

Phosphorus-Doped Oxide Layers

For preparing phosphorus-doped silicon dioxide films, phosphine concentrations ranging from .01 to 50 mole% phosphine to phosphine plus silane in the deposition gas stream have been used. When used as diffusion sources at 1200°C in nitrogen for 1 hour, these sources gave

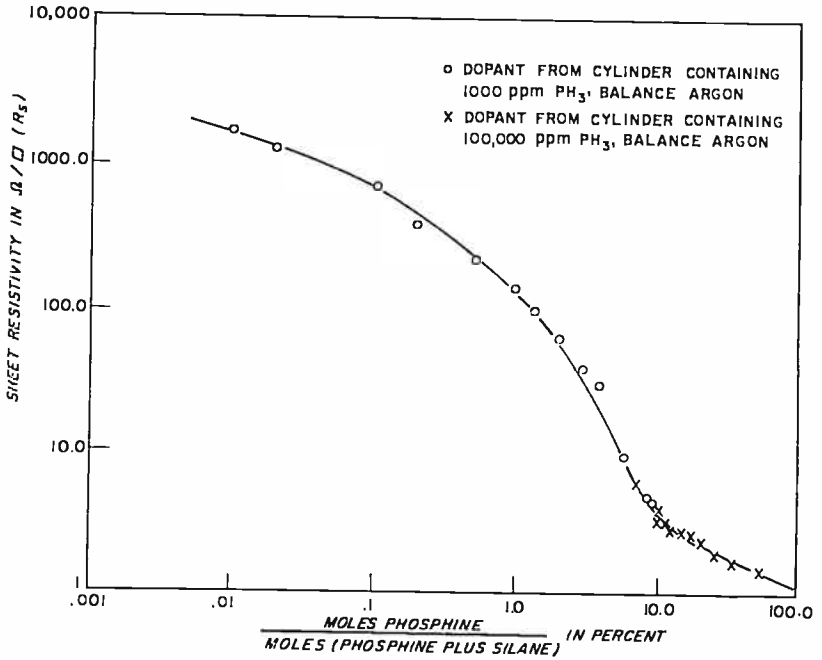

Fig. 1—Sheet resistivity following a 1-hour diffusion at 1200°C in nitrogen versus dopant concentration in the gas used to prepare the oxide diffusion source (phosphorus-doped silicon dioxide).

sheet resistivities from 1.5 to 1600 ohms/square, on the 1 to 2 ohm-cm p-type substrates (Figure 1). Junction depths ranged from 1 to 5.7 microns. Assuming an error-function distribution for the dopant, the corresponding surface concentrations ranged from 1.7×10^{17} to 1.4×10^{21} atoms/cm^3 for the different oxide compositions (Figure 2). From Figure 2, it can also be seen that, for a given oxide composition, the surface concentrations calculated for a 1-hour diffusion are the same as those for a 2-hour diffusion. Consequently, for the diffusion conditions employed, the doped oxide behaves like a constant-level reservoir of dopant. The squares in Figure 2 represent data for doped

oxides obtained with a different deposition apparatus and with different gas cylinders.

Best results were obtained in the range 2×10^{18} to 4×10^{20} atoms/cm^3. Reproducibility from day to day was better than ±10%. For the range 10^{18} to 10^{19} atoms/cm^3, reproducibility was better than ±6%. Uniformity of sheet resistivity across a given wafer was ±3%. Diffu-

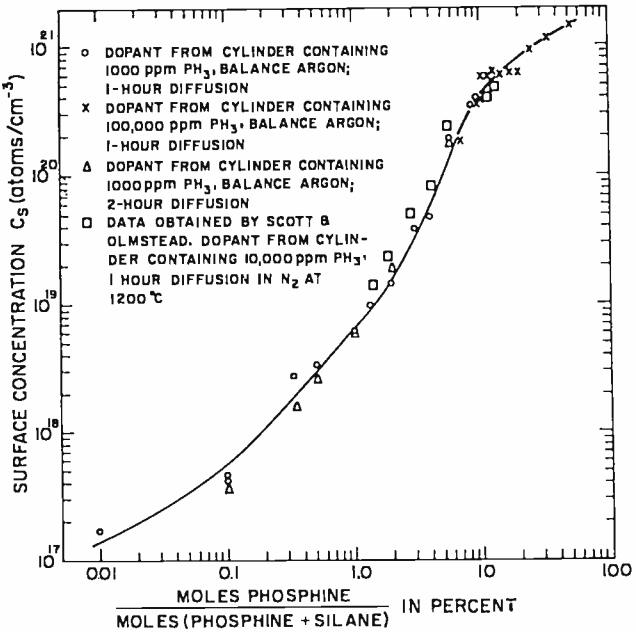

Fig. 2—Carrier concentration at the surface following 1- and 2-hour diffusions at 1200°C in nitrogen versus the dopant concentration in the gas used to prepare the oxide diffusion source (phosphorus-doped silicon dioxide).

sion results obtained for doping levels appropriate for the base region of a transistor are relatively independent of the oxide deposition temperature through the range 270 to 385°C, as shown in Figure 3. Even though the deposition temperature varies, the composition of the doped oxide layer and its diffusion characteristics remain substantially constant.

Boron-Doped Oxide Layers

In the deposition gas stream, diborane concentrations ranging from 0.005 to 15 mole% diborane to diborane plus silane have been used to prepare boron-doped oxide diffusion sources. These oxide layers, following a one-hour drive-in diffusion in nitrogen at 1200°C, yielded sheet resistivities ranging from 10,000 to 1.6 ohms/square (Figure 4).

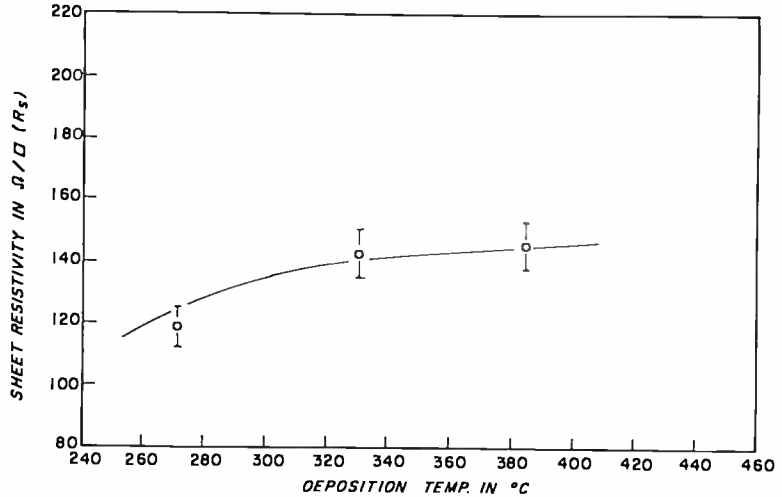

Fig. 3—Sheet resistivity versus deposition temperature following a 1-hour diffusion in nitrogen at 1200°C (phosphorus-doped silicon dioxide diffusion source prepared from a phosphine-silane gas mixture).

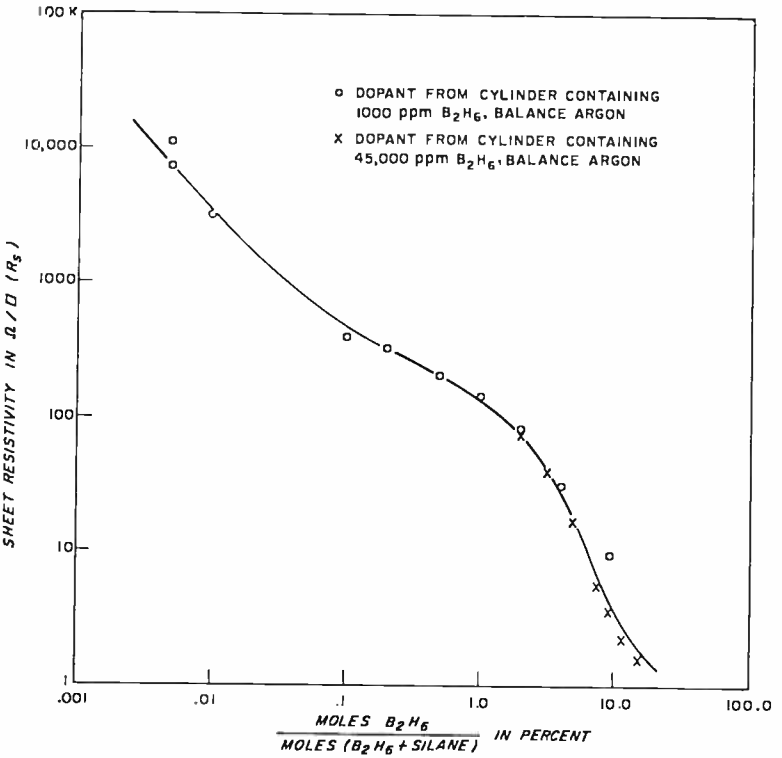

Fig. 4—Sheet resistivity following a 1-hour diffusion at 1200°C in nitrogen versus dopant concentration in the gas used to prepare the oxide diffusion source (boron-doped silicon dioxide).

The corresponding surface concentrations ranged from 3.6×10^{16} to 7.5×10^{20} atoms/cm^3 (Figure 5), and junction depths were from 1.6 to 6.2 microns. Just as for the phosphorus-doped oxides, the diffusion source behaves like a constant-level reservoir of dopant.

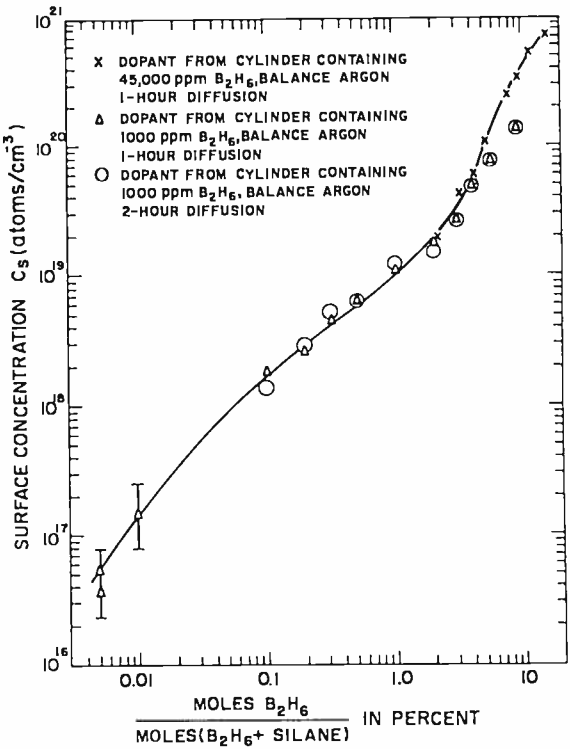

Fig. 5—Carrier concentration at the surface following 1- and 2-hour diffusions at 1200°C in nitrogen versus the dopant concentration in the gas used to prepare the oxide diffusion source (boron-doped silicon dioxide).

When these boron-doped oxide layers were used as diffusion sources on 1–2 ohm-cm n-type silicon, sheet resistivities were reproducible within about ±6% on a day-to-day basis for intermediate doping levels, i.e., in the range 2×10^{18} to 2×10^{19} atoms/cm^3. Again, variations of ±3% are obtained across a given wafer. Unlike the phosphorus-doped layers, however, the composition and diffusion properties of boron doped oxide layers are deposition-temperature dependent for surface concentrations in this range. It is therefore important that the deposition of these layers be carried out at a constant temperature, e.g., 325°C ± 10°C. The influence of deposition temperature on the diffusion properties of wafers diffused at 1200°C for 17 minutes in

air is shown in Figure 6. A minimum in sheet resistivity occurs at about 325°C.

For more heavily doped layers, i.e., concentrations of 10^{20} atoms/cm^3 or higher, sheet resistivity after diffusion is more variable. Ran-

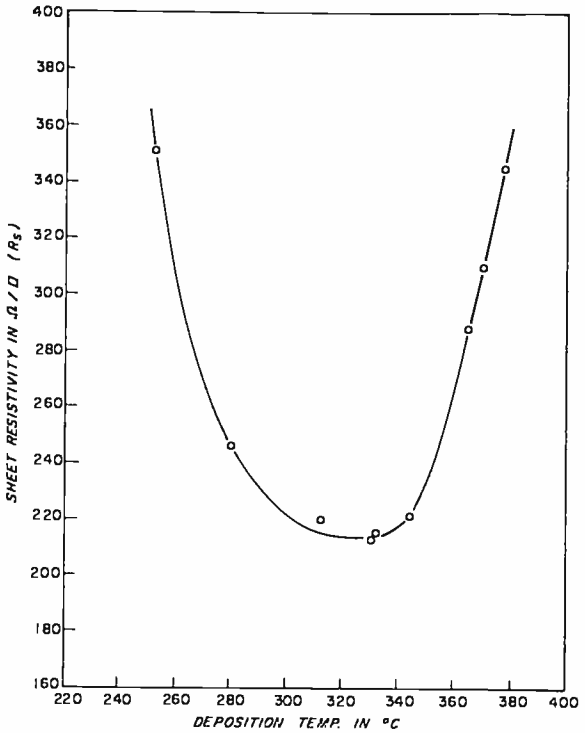

Fig. 6—Sheet resistivity following a 17-minute diffusion at 1200°C in air versus deposition temperature (boron-doped silicon dioxide diffusion source).

dom day-to-day variations of as much as ±25% were encountered with no satisfactory explanation being found. Variations of this magnitude would not be critical for some device applications, and much smaller variations are found when premixed cylinders are used.[9] The influence of deposition temperature on the diffusion characteristics of heavily doped oxides appears to be negligible in the range 300 to 400°C and the oxygen-to-silane ratio can be varied from about 3:1 to more than 6:1 with no perceptible influence on the surface concentration following diffusion.

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[9] A. W. Fisher and J. A. Amick, "Diffusion Characteristics of Doped Silicon Dioxide Layers Deposited from Premixed Hydrides," *RCA Review*, Vol. 29, p. 549, Dec. 1968.

Applications

Doped oxide diffusion sources have been successfully substituted for conventional diffusion sources in the fabrication of both n-p-n and

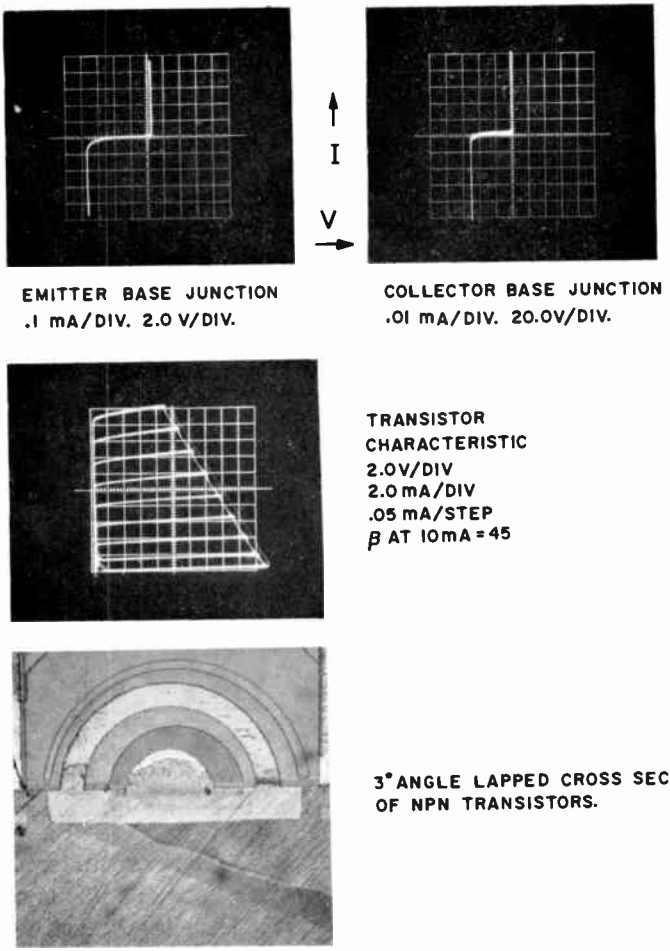

Fig. 7—NPN transistors prepared using doped-oxide diffusion sources.

p-n-p transistors, as shown in Figures 7 and 8. The procedure employed was similar to that normally used to prepare silicon devices. Substrate wafers were thermally oxidized, openings were formed in this oxide with conventional photoresist technology, and an appropriately doped oxide layer was deposited at 325°C over the entire wafer. For the base diffusion step, the gas composition was 0.5 mole% of either phosphine or diborane, based on total hydride, i.e., silane plus dopant. Diffusion was carried out in nitrogen to give the desired junction depth and surface concentration.

Since the doped oxide layer contains a dopant concentration appropriate to the surface concentration required in the base, the doped

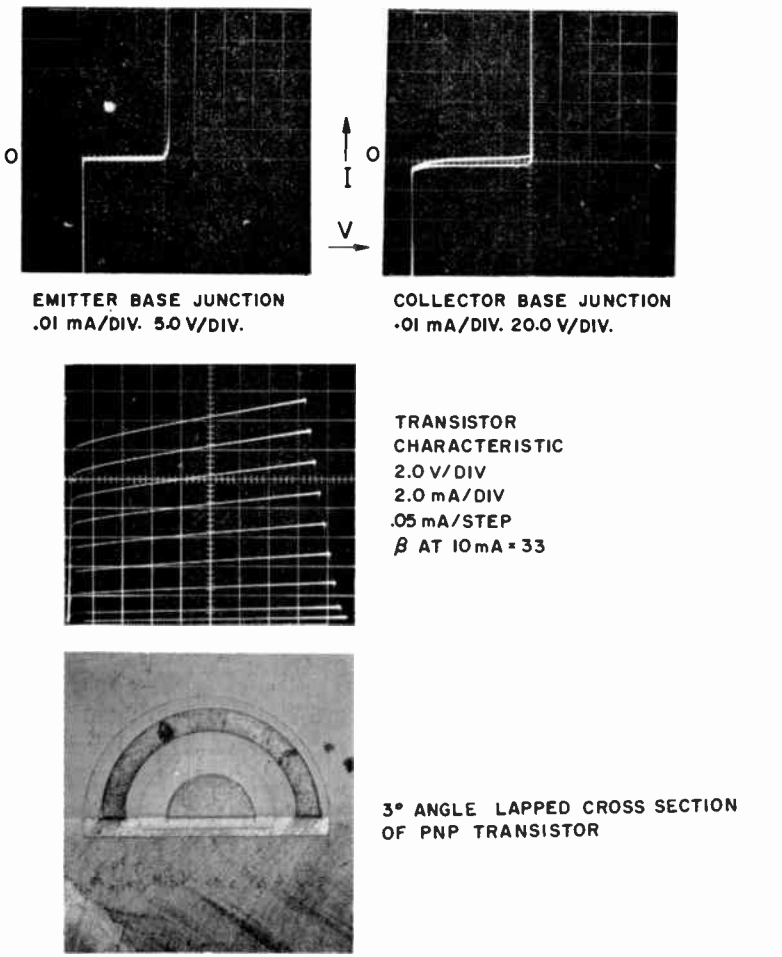

Fig. 8—PNP transistors prepared using doped-oxide diffusion sources.

oxide remains on the surface of the base region during subsequent processing. The emitter regions were opened and heavily doped oxide layers were deposited, again over the entire surface. Diffusions were carried out in nitrogen, as before, to give suitable junction depths and surface concentrations (cf. Figure 9). Gas compositions of 10 mole% dopant-hydride were employed for emitter formation. Breakdowns for the emitter–base and collector–base junctions were sharp for both the n-p-n and the p-n-p units. The electrical characteristics were those expected for the resistivity of the starting material and for the times,

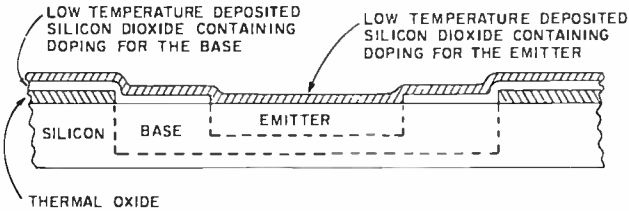

Fig. 9—Cross section of a transistor fabricated using sequential deposition of oxide diffusion sources.

temperatures, and doped oxide composition employed. Uniformity of device characteristics across a wafer was excellent. This is especially true for the phosphorus diffusions. When conventional phosphorus diffusion sources are employed results are usually somewhat nonuniform.

With doped oxide layers, efficient emitters can be controllably and reproducibly formed without exceeding the solid solubility limit for the dopant in silicon. Under these conditions no evidence of emitter "push-out" can be detected (Figures 10 and 11). Emitter push-out occurs when the solubility limit is exceeded and the surface region of the silicon is crystallographically damaged by the introduction of dislocations, increasing the local diffusion coefficient for the dopant.

Potential Advantages of Doped-Oxide Diffusion Sources

Doped-oxide diffusion sources afford improved uniformity and reproducibility in the fabrication of silicon devices. The surface is better protected from contamination during handling and during the diffusion step. Control of surface concentration is simplified, hence the electrical characteristics of devices can be held to tighter tolerances. Ultimately, these advantages lead to higher yields.

Doped oxides also offer promise for the preparation of monolithic arrays of complementary devices, e.g., n-p-n and p-n-p devices, on a

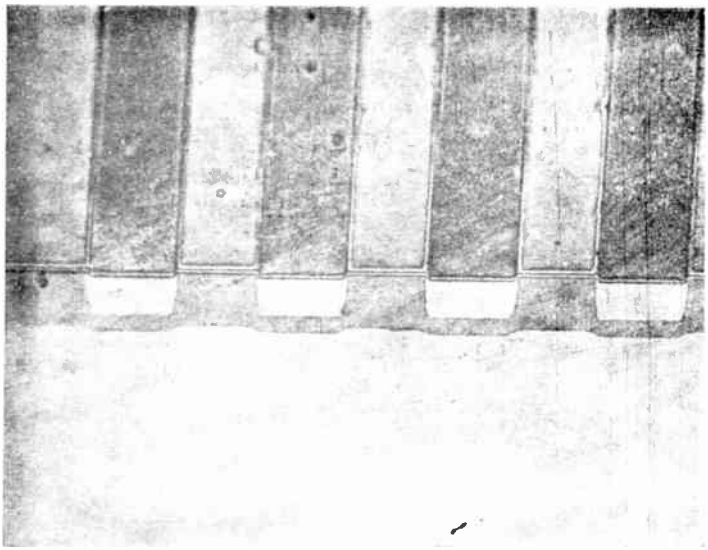

Fig. 10—Cross section of n-p-n transistor processed with conventional diffusion methods. The base layer is pushed out under the emitter stripes.

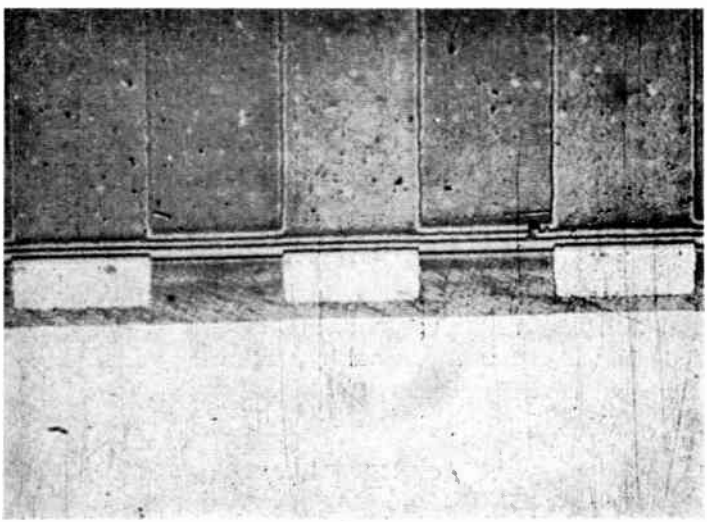

Fig. 11—Cross section of n-p-n transistor processed with doped silicon dioxide diffusion techniques. The bump under the emitter has disappeared for a surface concentration of 5×10^{20} cm^{-3}.

common substrate. The diffusion coefficients for boron and phosphorus in silicon are sufficiently similar that, with localized regions of boron-doped oxide and localized regions of phosphorus-doped oxide in a suitable substrate, one diffusion step can be employed to fabricate the base regions for both n-p-n and p-n-p devices. Selectively matched electrical parameters can be obtained by adjusting the dopant concentration in each oxide and the temperature and time of the diffusion. Similarly, emitter regions for both types of device can be formed in one heat treatment. The compromises currently required in the preparation of complementary arrays with sequential processing are nearly eliminated when simultaneous processing with doped oxides is employed.

Conclusions

Doped silicon dioxide layers deposited at 325°C from mixtures of nitrogen, oxygen, silane, and hydride dopants provide uniform, highly reproducible, and controllable diffusion sources for the preparation of silicon devices. For diffusion times of at least 2 hours at 1200°C both phosphorus- and boron-doped oxides serve as constant-level reservoirs of doping agents. Following a diffusion, variations in sheet resistivity across a wafer are generally within ±3% and from run to run are within ±10%.

Principal advantages of the doped-oxide sources are in improved control, lower sensitivity of the devices to contamination, and simplified device processing. Since the surface concentration of dopant can readily be held below the solid solubility limit for that dopant, the introduction of crystalline defects during diffusion can be minimized.

Phosphorus-doped oxides are especially satisfactory as diffusion sources. Phosphine remains stable in cylinders indefinitely, and control of the deposition temperature for phosphorus-doped layers is less critical than for boron-doped layers. Diborane–argon mixtures exhibit a decreasing boron content with time in the gas taken from the cylinders. If cylinders are used within 6 months of their preparation and analysis, the errors introduced by these changes should be negligible for most device processing.

Acknowledgment

For many helpful discussions we would like to thank W. Kern and N. Goldsmith. We are also grateful for the critical reading of the manuscript and the stimulating guidance of N. E. Wolff.

DIFFUSION CHARACTERISTICS OF DOPED SILICON DIOXIDE LAYERS DEPOSITED FROM PREMIXED HYDRIDES

By

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Summary—Doped silicon dioxide films containing known amounts of impurities serve as controlled, reproducible diffusion sources for the fabrication of silicon devices. The doped films are prepared by reacting (with oxygen) a mixture of diluted silane (SiH_4) and a suitable dopant gas such as diluted diborane (B_2H_6) or phosphine (PH_3), the mixture being stored in a cylinder under pressure. The concentration of dopant in the oxide is determined by the silane-to-dopant ratio in the cylinder. Doped oxide diffusion sources are easily prepared from premixed cylinders and yield more uniform diffusion results than can be achieved by mixing the individual components in the reaction chamber.

Introduction

Doped silicon dioxide films serve as excellent diffusion sources for the fabrication of discrete semiconductor devices and integrated circuits.[1] The dopant concentrations in the oxide layer are adjusted to yield the desired surface concentration in the silicon subsequent to diffusion. Initially, doped oxides were prepared by mixing gases from two cylinders, one containing diluted dopant and the other containing diluted silane. However, when a suitable ratio of dopant to silane for a particular application is established, the dopant, silane, and diluent can be purchased (premixed) in one cylinder, thus assuring a constant gas composition for the life of the cylinder. Oxides deposited from such a gas mixture are more reproducible in their characteristics and give more uniform diffusion results than those prepared from separate cylinders.

Materials and Equipment

Cylinders of premixed silane and dopant, either phosphine or

[1] A. W. Fisher, J. A. Amick, H. Hyman, and J. Scott, "Diffusion Characteristics and Applications of Doped Silicon Dioxide Layers Deposited from Silane," *RCA Review*, Vol. 29, p. 533, Dec. 1968.

diborane, diluted in argon were purchased from two suppliers†‡ subject to a certified gas analysis. High purity nitrogen and line oxygen were used for all experiments, each being passed through a 1.5 micron filter prior to entering the reaction chamber.

Oxide depositions were carried out using hot plate apparatus similar to that described by Kern,[2] but modified to accommodate six 1.5-inch-diameter wafers.

Diffusion studies were carried out using deposited oxide layers as sources on 1-2 ohm-cm Lustrox polished silicon wafers.#

Experimental

All wafers were cleaned by treatment in hot organic solvents followed by immersion in hot chromic-sulfuric acid. Wafers for boron-doped oxide depositions were also dipped in buffered HF, rinsed, and dried immediately before deposition. If the HF rinse is not used, non-uniform diffusion will result; i.e., sheet resistivity will vary ±15% across a wafer, as compared to a normal ±3%. The step is not required for *uniformity* when phosphorus doped layers are used. Sheet resistivities for both boron- and phosphorus-doped layers are decreased if the HF rinse is used.[1]

All test wafers had a 3000-Å layer of undoped "capping" oxide over the deposited source layer. Standard practice involved diffusing at 1200°C for one hour in nitrogen.

Phosphorus-Doped Layers Deposited from Premixed Gases

Cylinders containing premixed gases of dilute silane–phosphine with the following concentrations were tested:

silane 100,000 ppm (by volume), phosphine 10,000 ppm, balance ultra-pure argon;

silane 90,000 ppm, phosphine 10,000 ppm, balance ultra-pure argon;

silane 30,000 ppm, phosphine 3,500 ppm, balance ultra-pure argon;

silane 30,000 ppm, phosphine 95 ppm, balance ultra-pure argon;

silane 30,000 ppm, phosphine 150 ppm, balance ultra-pure argon

Tolerance on the silane content was held by the supplier to ±10% with

† Precision Gas Products, Linden, N. J.

‡ Matheson Company, E. Rutherford, N. J.

[2] W. Kern, "Apparatus for Chemical Vapor Deposition of Oxide and Glass Films," *RCA Review*, Vol. 29, p. 525, Dec. 1968.

Texas Instruments, Inc., Dallas, Texas.

±15% for phosphine. The gas compositions were chosen because these ratios yield doped oxides suitable for emitter and base diffusions.

Diffusion depths and surface concentrations obtained from oxides that were derived from the premixed gases in cylinders were equivalent to those obtained from oxides prepared from separate gas-cylinder sources. The premixed gases resulted in oxides that gave very reproducible sheet resistivities, usually within ±5% for diffusion in nitrogen and ±10% for diffusion in air. Uniformity across a given wafer is generally within ±3%. Table I shows the diffusion results from 20

Table I—Sheet Resistivity Following a 1-Hour Diffusion in Air at 120°C. (Doped oxide prepared from a cylinder containing 30,000 ppm silane, 150 ppm phosphine, balance argon.)

Run	Sheet Resistivity, R_s (ohms/square) Wafer #1	Wafer #2
1	155	156
2	163	156
3	163	154
4	165	165
5	139*	136*
6	172	178
7	161	167
8	162	160
9	166	163
10	150*	166

* wafers dipped in buffered HF prior to doped oxide deposition.

wafers prepared in ten separate runs over a period of one week. These particular diffusions were carried out in air at 1200°C for one hour, although most diffusions were carried out in nitrogen. Air can be used, but it does not give as reproducible results, perhaps because of the variable water-vapor content in air, which alters the oxidation rate for the silicon during drive-in. Where nitrogen is employed, there is no apparent oxidation of the silicon, and the sheet resistivities are about 20% lower than for a drive-in in air.

With premixed gases for the oxide source, experiments were carried out to determine sheet resistivity as a function of doped oxide thickness, using nitrogen as the diffusion ambient. Data given in Table II, show that, following diffusion, a doped oxide layer 1500 Å thick gives the same sheet resistivity as source layers up to 1 micron thick. The dopant concentration is evidentally not appreciably depleted following a one- or a three-hour diffusion. Furthermore, the

Table II—Sheet Resistivity as a Function of Doped Oxide Thickness. (Doped oxide deposited from a premixed cylinder with a concentration suitable for base doping.)

Wafer	Phosphorus Dopant Doped Oxide Thickness (Å)	Thickness of Undoped Oxide Cap (Å)	Sheet Resistivity, R_s R_s (ohms/square)
1-Hour Diffusion in N_2 at 1200°C			
1	1500	None	111
2	3000	None	113
3	4500	None	114
4	6200	None	102
5	10,000	None	108
6	1500	4700	111
7	3000	3200	112
8	4500	1700	104
9	3000	3200	103
10	3000	3200	107
3-Hour Diffusion in 4 to 1 N_2—O_2 at 1200°C			
1	1500	6000	87
2	3000	6000	87

results show that the capping oxide has no appreciable influence on diffusion results when diffusions are carried out in nitrogen.

Doped oxide layers containing doping levels appropriate for emitters were slightly depleted at thicknesses of 1500 Å and 3000 Å as shown in Table III and Figure 1.

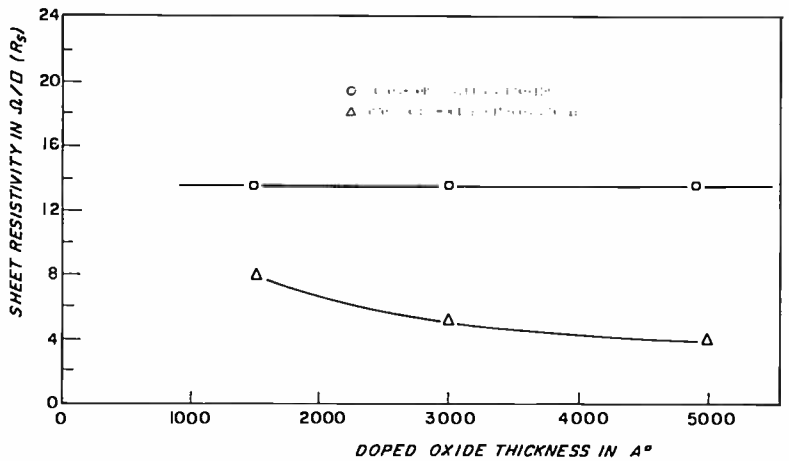

Fig. 1—Sheet resistivity versus doped oxide layer thickness following a 1-hour diffusion in N_2 at 1200°C.

Table III—Sheet Resistivity as a Function of Doped Oxide Thickness for Emitter Doping Levels. (Doped oxide deposited from premixed hydrides cylinder wih a concentration suitable for emitter dopant. Wafers diffused 1 hour in N_2 at 1200°C.)

Wafer	Phosphorus Dopant Doped Oxide Thickness (Å)	Thickness of Undoped Oxide Cap (Å)	Sheet Resistivity, R_s R_s (ohms/square)
1	1500	5000	7.9
2	3000	5000	5.0
3	4900	5000	3.8

The diffusion results obtained after a one-hour diffusion from an oxide prepared from premixed gases were used to check the concentration and stability of the silane–phosphine content of cylinders. The cylinders have been checked for composition as received and at one month intervals since. Over a time span of nearly one year, the diffusion results indicate that the composition in the cylinder is unchanged. Results from two cylinders are shown in Table IV.

Boron-Doped Layers Deposited from Premixed Cylinders

Cylinders containing premixed gases of dilute silane–diborane with the following concentrations have been ordered and evaluated:

Table IV—Monthly Check of Premixed Cylinders (Silane–Phosphine)

	Sheet Resistivity, R_s (ohms/square)	Surface Concentration, C_s (atoms/cm^3)
A. Cylinder containing 90,000 ppm silane, 10,000 ppm phosphine, balance argon (purchased from Precision Gas Co.)		
When Received	4	3×10^{20}
First Month	4.3	3×10^{20}
Second Month	4.3	2.5×10^{20}
Third Month	4.0	2.6×10^{20}
Seventh Month	3.3*	4.0×10^{20}
Eighth Month	3.4*	3.8×10^{20}
Tenth Month	3.6*	3×10^{20}
B. Cylinder containing 100,000 ppm silane, 10,000 ppm phosphine, balance argon (purchased from The Matheson Co.)		
When Received	5.1	2.2×10^{20}
First Month	5.2	2×10^{20}
Second Month	4.9	2×10^{20}

* Special care taken to minimize contact of hot wafers with air during deposition and diffusion.

30,000 ppm (by volume) silane, 7 ppm diborane, balance ultra-pure argon;

100,000 ppm silane, 10,000 ppm diborane, balance ultra-pure argon;

90,000 ppm silane, 10,000 ppm diborane, balance ultra-pure argon;

100,000 ppm silane, 250 ppm diborane, balance ultra-pure argon; and

30,000 ppm silane, 150 ppm diborane, balance ultra-pure argon.

Each cylinder was ordered subject to a certified gas analysis with a tolerance of ±10% for silane and ±20% for diborane.

Uniformity of sheet resistivity after diffusion from boron-doped oxide sources is generally within ±3% across a given wafer. Measurements of sheet resistance versus doped-oxide thickness show that a 1500-Å layer of heavily doped, capped boron oxide is effectively an infinite source for a one hour diffusion in nitrogen at 1200°C. Diffusion results for a 1500-Å layer are the same as for 3000- and 4900-Å layers (Figure 1), indicating that the source is not being depleted of dopant. Preliminary results also indicate that, like phosphorus-doped layers, boron-doped layers suitable for base diffusions behave like infinite sources for thicknesses of 1500 Å or greater.

Silane–diborane compositions are not as stable with time as phosphine–silane mixtures. The cylinder containing 7 ppm diborane as analyzed by the supplier was returned for reanalysis when diffusion results indicated that no diborane was present. This reanalysis confirmed that diborane was no longer present, and several attempts to purchase another cylinder with the same concentration were unsuccessful.

The other four cylinders, two having higher diborane content and two having lower diborane content, were checked when received and have been checked at monthly intervals since. When received, the diffusion results obtained from oxides prepared from these sources corresponded to those anticipated for the gas compositions. After one month, a check of both high-diborane-content cylinders indicated that the boron concentration had decreased about 10 to 20% from its original value, based on diffusion results. After a second month, it remained constant for both cylinders. After a third and fourth month, both cylinders had again changed (Table V). One cylinder was returned for reanalysis, which confirmed that the diborane content had dropped to 60–70% of its original value. The same behavior is exhibited by the two lower diborane content cylinders. This behavior is probably due to polymerization of diborane in the presence of silane,

The resulting higher boranes, having low vapor pressure, are retained in the cylinder. The mixture withdrawn from the cylinder would therefore have a boron content lower than its original value.

Discussion

The advantages of using premixed gases of silane and dopant for preparing diffusion sources are simplicity and control. With the ratio of silane to dopant predetermined, flow rates are much less critical.

Table V—Monthly Check of Premixed Cylinders (Silane-Diborane)

	Sheet Resistivity, R_s (ohms/square)	Surface Concentration, C_s (atoms/cm^3)
A. Cylinder containing 90,000 ppm silane, 10,000 ppm diborane, balance argon (purchased from Precision Gas Co.)		
When Received	4.2	3×10^{20}
First Month	6.4	2.2×10^{20}
Second Month	7.5	2×10^{20}
Fourth Month	10.1	1.4×10^{20}
Fifth Month	12.4	1.1×10^{20}
B. Cylinder containing 100,000 ppm silane, 10,000 ppm diborane, balance argon (purchased from The Matheson Co.)		
When Received	9.5	1.4×10^{20}
First Month	13.5	9×10^{19}
Second Month	13.8	1.1×10^{20}
Third Month	16.4	9×10^{19}
Fourth Month	21	6.5×10^{19}

The oxygen and argon are present in excess, so that, to a first approximation, the growth rate depends only on the flow of the premixed gases from a single cylinder. Furthermore, the composition of the oxide layer is nearly independent of small changes in temperature. As a result, the operation of the apparatus is simplified; only one flowmeter need be adjusted and the precision required in that one adjustment is not great.

Since a variety of transistors require almost the same surface concentration of dopant for the base (or emitter) region, one cylinder for base diffusions and one for emitter diffusions will generally be sufficient. For phosphine mixtures, these cylinders remain stable for an indefinite time. For diborane mixtures there will be slow changes, but the size of the change will often be negligible, since variations in surface concentration of a factor of two are generally tolerable. Where more precise control of the boron concentration is needed, cylinders must be used soon after they are analyzed, preferably within 3 months.

Conclusions

Silicon dioxide layers deposited from silane–phosphine–argon premixed in cylinders serve as controlled, reproducible diffusion sources for preparing silicon devices. Boron-doped oxide layers deposited from premixed silane-diborane-argon in cylinders form satisfactory diffusion sources for a variety of applications in spite of the instability of the diborane in such cylinders. Uniformity and reproducibility of the sheet resistivities is as good as, or better than, that obtained using conventional diffusion sources, usually ±3% across a given wafer and better than ±10% from run to run. Further, oxide diffusion sources are more easily prepared from premixed gases in a single cylinder than from the gas components in two separate cylinders.

Silane–phosphine mixtures are stable indefinitely. Thus a cylinder gives reproducible results during its lifetime. Premixed gases in cylinders of silane–diborane are unstable and have a useful lifetime of a few months or less, depending on the application.

Acknowledgment

For many helpful discussions and critical reading of the manuscript, we would like to thank N. E. Wolff and W. Kern.

A TECHNIQUE FOR MEASURING ETCH RATES OF DIELECTRIC FILMS

By

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Summary—A dielectric surface generally exhibits hydrophilic character in an aqueous solution containing hydrofluoric acid, whereas many semiconductor surfaces are hydrophobic under the same conditions. This difference in wettability for the two types of materials is used to determine the end point in the dissolution of the dielectric film. The sample is moved automatically in and out of the etch solution so that clear observation of the surface is readily possible. End points can be determined to within 0.5 second, which is typically ±1% of the film-dissolution time. The etch rate for a one-micron-thick, thermally grown silicon dioxide film in buffered etch, for example, can be estimated to within a few percent or less depending on the technique employed in measuring the original film thickness. Precise etch-rate data are useful not only for comparing film density, bond strain, and stoichiometry, but also for routine testing of film composition.

Introduction

FILMS of oxide dielectrics are widely utilized in semiconductor device fabrication, especially thermally grown films of silicon dioxide on silicon substrates, often several thousand angstroms thick. The monitoring of density and chemical composition of such films is an important requirement. In particular, the dissolution rate of an oxide film in a suitable liquid etchant is an informative quantity for comparing the relative density and structure, and for determining the film composition. Etch rate data are obtained readily by measuring the film thickness and its dissolution time. Several well-established and accurate optical methods for measuring the thickness of dielectric films are available. On the other hand, no accurate technique for determining the dissolution-time end point has been published. The accuracy of the etch rate is dependent upon both the film thickness and the film dissolution time. It is imperative, therefore, that both be measured with a high degree of precision. This paper describes a convenient technique to accomplish this.

Problems in the Conventional Measuring Techniques

In the usual determination of the dissolution time for a dielectric film on a semiconductor substrate, the end point is taken when the

optical interference colors on the surface of the submerged sample disappears. The precise moment of this occurrence is, however, difficult to ascertain. The angle of observation and the lighting conditions must be just right, and, since there is a gradual rather than an abrupt change in the interference color, the decision as to when the color has disappeared is somewhat subjective. Furthermore, in the typical case of silicon dioxide on silicon, film thicknesses below about 500 Å cannot be distinguished with certainty from the metallic grey background of the silicon substrate while the sample is in the etch bath. The potential uncertainty in a film of 2000 Å thickness, for example, can be as high as 25%. Regardless of the accuracy with which the film thickness has been determined, the accuracy of the resulting dissolution rate value is limited by this uncertainty in the dissolution time.

Principle of the Improved Technique for End-Point Determination

The approach described in this paper is based on the difference in wetting characteristics between a semiconductor surface and a dielectric surface on exposure to aqueous solutions containing hydrofluoric acid. Upon immersion in such a solution, a clear silicon surface becomes hydrophobic very rapidly due to the adsorption of fluoride ions.[1,2] According to Iler[1] the strongly hydrophobic surface is due to the nonpolar character of an Si-F surface. Hydrophobic behavior of this type is also true for several other semiconductor materials, as indicated in Table I. Silicon dioxide and other silicates, on the other hand, remain hydrophilic when exposed to, or while being dissolved in, such etchants (Table II). Therefore, a semiconductor substrate coated with a dielectric film remains wetted by the etch solution until the dielectric film has been completely dissolved. At the instant the semiconductor substrate becomes exposed to the etchant, it repels the solution, and the liquid, instead of forming a continuous envelope, no longer clings to the sample. This change provides a precise, definite, and convenient criterion for determining the end point in dissolution timing. Since the wettability of the surface can be seen only when the sample is out of the solution, it is necessary to withdraw it momentarily for observation. Short but frequent withdrawals are necessary to obtain a precise timing of the end point. An apparatus has been designed to perform the withdrawal and reinsertion automatically and

[1] R. K. Iler, *The Colloid Chemistry of Silica and Silicates*, Cornell University, Ithaca, New York, 1955.

[2] M. M. Atalla, E. Tannenbaum, and E. T. Scheibner, "Stabilization of Silicon Surfaces by Thermally Grown Oxides," *The Bell Syst. Tech. Jour.*, Vol. 38, p. 749 (1959).

Table I—Wettability of Polished Semiconductor Surfaces in Aqueous Hydrofluoric Acid

Initial Surface:	Organic contaminants normally present in room air cause hydrophobic surface properties and must therefore be removed (with $H_2O_2 + H_2SO_4$ or similar agents) to attain an initially hydrophilic surface.
Repelling Types:	Silicon, single crystal Germanium, single crystal Gallium Arsenide, (100) plane Indium Arsenide, (100) plane
Wetting Types:	Gallium Phosphide, polycrystalline Gallium Antimonide, (100) plane Indium Phosphide, (100) plane

regularly. Removing the sample from the etch solution for an instant does not affect dissolution, since a considerable amount of etchant adheres to the hydrophilic sample surface. Etching therefore continues outside the bath. Since the temperature of the solutions to which the sample is exposed affects the etch rate critically, tests are conducted under isothermal conditions, usually at 25.0°C. Furthermore, the volume of etch solution used is very large in relation to the quantity of the sample being dissolved, so that concentration changes in the etchant are negligible.

Apparatus

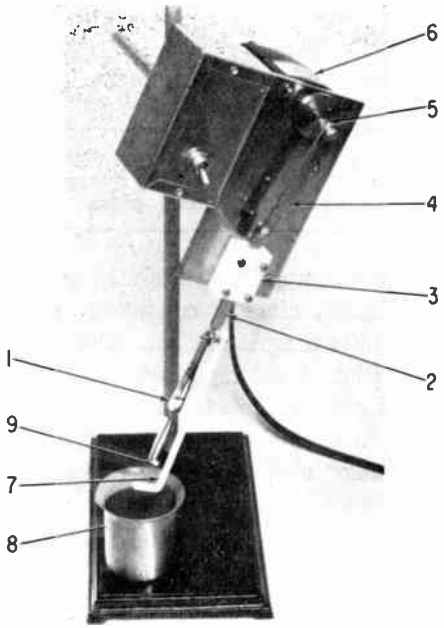
The apparatus used for moving the sample and for agitating the etch solution is seen in Figure 1. A pair of Teflon-coated reverse-

Table II—Dielectrics* Tested That Have Hydrophilic and Soluble Properties in Hydrofluoric Acid

Oxides	Silicates	Nitrides
Silicon Dioxide	Borosilicates	Silicon Nitride
Doped Silicon Dioxides	Phosphosilicates	
Aluminum Oxide	Lead Silicates	
Zinc Oxide	Aluminosilicates	
Boron Oxide	Zinc Silicates	
Lead Oxide	Many multicomponent silicates	

* All of these dielectrics were prepared by chemical vapor deposition, as described by W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Paper No. 92, 1968 Spring Meeting of the ECS, Boston, Mass.

action tweezers (1) is attached to a stainless steel rod (2) riding in a guide block (3) of Teflon. The upper part (4) of the rod is fastened excentrically to the motor crank shaft (5) so that the sample moves in a reciprocal motion over a distance of 0.5 inch. The variable-speed



1. Reverse-Action Tweezers
2. Stainless Steel Rod
3. Teflon Guide Block
4. Upper Rod Part
5. Motor Crank Shaft
6. Variable-Speed Motor
7. Stirrer
8. Polyethylene Beaker containing the etchant. It is inserted in a circulating water bath (not shown for clarity) to maintain a constant temperature.
9. Test Sample

Fig. 1—Apparatus for dissolution-time measurements

motor (6) is set to yield, typically, two strokes per second. A Teflon stirrer (7) fastened to the shaft provides agitation during cycling. The motor assembly is mounted on a rack and pinion so that it can be tilted easily and moved for positioning. An illuminated desk magnifier providing daylight fluorescent light is used to light the sample for viewing.

A circulating water bath maintains the stock etch solutions and the polyethylene beaker (8) containing the etchant at constant temperature. The complete system is placed in an exhaust hood for safety.

Test Procedure

The film thickness of the sample is measured optically by interference methods or by ellipsometry. The interference technique developed by Tolansky[3] and described in detail by Booker and Benjamin[4] for measuring oxide films on silicon is particularly suitable. Ellipsometry[5,6] is much more tedious to apply, but it is capable of providing more accurate data and is the method of choice for measuring very thin films of a few hundred angstroms or less.

The dissolution timing is carried out as follows. One end of a sample (9) measuring typically 0.4 × 1.5 cm is inserted in the tweezer so that it is positioned as shown in Figure 1. The motor assembly is tilted so that the sample surface can be conveniently viewed from a direction perpendicular to the surface (it is illuminated from the same direction); this condition results in maximum sensitivity for noting the wettability of the surface. The height of the motor is so adjusted that the sample is submerged in the etch solution for half the time, and out of it for the other half. Timing is started when the sample is first immersed into the etch solution and is terminated when the liquid envelope on the sample surface in air is disrupted; the sample surface is not necessarily free of all etch solution at this point of repelling.

The dissolution rate is calculated from the measured dissolution time and the film thickness. To obtain the most accurate and precise results, a substrate blank correction should be made as indicated in Table III. An example of a typical analysis is shown in Table IV.

Discussion

Dissolution End Point

The breaking up of the etchant solution on the sample surface indicates that the dielectric film has dissolved; it occurs usually in a fraction of one second and therefore provides a definite and precise end-point criterion.

Complete repelling by the sample surface usually takes longer and

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[3] S. Tolansky, *Multiple-Beam Interferometry of Surfaces and Films*, Clarendon Press, Oxford, 1948.

[4] G. R. Booker and C. E. Benjamin, "Measurement of Thickness and Refractive Index of Oxide Films or Silicon," *Jour. Electrochem. Soc.*, Vol. 109, p. 1206, (1962).

[5] R. J. Archer, "Determination of the Properties of Films on Silicon by the Method of Ellipsometry," *Jour. Opt. Soc. Amer.*, Vol. 52, p. 970, (1962).

[6] K. H. Zaininger and A. G. Revesz, "Ellipsometry—A Valuable Tool in Surface Research," *RCA Review*, Vol. 25, p. 85 (1964).

appears to be a function of the degree of fluoridation of the semiconductor surface. It therefore depends upon the HF concentration in the etchant, the physical and chemical nature of the semiconductor surface, and the rate of sample movement. In a strong solution of hydrofluoric

Table III—Example of Dissolution Timing Precision

Subtrate:	Mechanically polished silicon wafer, (111), n-type, 40 ohm-cm
Film:	Borosilicate glass film synthesized from $SiH_4 + B_2H_6 + O_2$;[7] 8250 Å thick
Etchant:	4.9% Hydrofluoric acid solution
Temperature:	25.0 ± 0.1°C

Etch Time of Coated Samples:		
	Sample 1	324.6 sec.
	2	324.5 sec.
	3	323.0 sec.
	4	317.0 sec.
	5	327.0 sec.
	Mean	323.2 sec.
	Mean Error	± 1.2 sec. (± .4%)

Etch Time of Chemically Cleaned Blank Samples:		
	Sample 1	2.0 sec.
	2	1.8 sec.
	3	2.1 sec.
	4	2.0 sec.
	5	1.8 sec.
	6	1.5 sec.
	7	1.6 sec.
	8	1.8 sec.
	Mean	1.8 sec.
	Mean Error	± 0.05 sec. (± .3%)

acid, for example, breaking up of the film and complete repellency appears to occur simultaneously. In a weak solution, on the other hand, complete repellency may not be obtained until considerably later. Complete dissolution is the important parameter. Hence the point of complete repellency is not considered critical, and is not used in end-point timing.

Sample Size

The size of the sample used in the test is not critical. Considerably smaller or larger pieces than the convenient standard size of 0.4 × 1.5 cm can be used. The reciprocal motion may have to be increased for larger samples by selecting a different eccentric setting for the rod. Smaller samples can be mounted on a support.

Table IV—Example of Etch Rate Analysis

Substrate:	Chemically polished silicon wafer, (111), n-type, 10 ohm-cm
Film:	SiO_2, grown in steam at 1250°C
Etchant:	Ammonium fluoride buffered hydrofluoric acid solution
Temperature:	25.0 ± 0.1°C
Film Thickness:	9490 Å; accuracy ± 20 Å (±0.2%) (by Ellipsometry)
Etch Time:	534.5 sec.
Etch Time Precision:	mean error ± 5.1 sec. (± 0.95%)
Etch Rate:	$\frac{9490 \pm 20 \text{ Å}}{534.5 \pm 5.1 \text{ sec.}} = 17.75 \pm 0.21 \text{ Å sec}^{-1}$ (± 1.2%)

Effect of Sample Motion

The etch rate is not affected appreciably by the rate of sample movement or by removal from the bath. No differences are found if the sample is submerged during 90% of the etch time or by testing it in the standard manner. The rate of sample motion should be such that clear observation of the sample surface is readily possible. The usual rate of 2 strokes per second is convenient. Much faster sample movement may obscure the end point, because the liquid film does not have sufficient time to be repelled from the hydrophobic surface before it is again submerged.

Effect of Film Nonuniformity

Since the etch rate obtained by this method represents an integrated value, nonuniformity in the film composition, e.g., composite layers, would lead to nonuniform etch rates. The end point could still be precisely determined, however.

Determination of Each Rates in Etchants for which no End Point is Visible

Etch rates in solutions other than those containing fluorides can be measured by the following modified technique. The etch time T_1 of the film in the regular hydrofluoric acid etchant is first determined. A second piece of the same sample is exposed to the non-fluoride etch for a measured period of time t until approximately two-thirds of the film thickness has dissolved. The remainder is then dissolved by the standard technique in the regular fluoride etchant, and the required length of time T_2 recorded. The etch rate R_t of the film in the non-fluoride etch is then given by

$$R_t = \frac{(T_1 - T_2)\,d}{T_1 t},$$

where d is the original film thickness. Application of this modified technique is particularly useful for determining etch rates of films such as silicon nitride in boiling phosphoric acid, or of aluminum oxide in hot potassium hydroxide solution.

Application of Etch Rate Data for Determining Film Composition and Thickness

A discussion of etch rate applications is beyond the scope of this paper. However, two particularly useful applications will be briefly noted. The etch rate in preferential etchants is sensitive not only to density,[7-9] bond strain,[8,9] and stoichiometry,[8,9] but can be critically affected by the composition of the film material.[7,10,11] For example, the etch rate of borosilicate glasses in hydrofluoric acid solutions increases with increasing boric oxide content in the film; in contrast, when ammonium fluoride buffered hydrofluoric acid is used as an etchant, the rate decreases steeply to a minimum and then increases with further increases

[7] W. Kern and R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," Paper No. 92 presented at the 1968 Spring Meeting of the ECS, Boston, Mass.

[8] W. A. Pliskin and H. S. Lehman, "Structural Evaluation of Silicon Oxide Films," *Jour. Electrochem. Soc.*, Vol. 112, p. 1013 (1965).

[9] N. Goldsmith and W. Kern, "The Deposition of Vitreous Silicon Dioxide Films from Silane," *RCA Review*, Vol. 28, p. 153 (1967).

[10] T. M. Eldridge and P. Balk, "Formation of Phosphosilicate Glass Films on Silicon Dioxide," *Transact. Metallurg. Soc. AIME*, Vol. 242, p. 539 (1968).

[11] F. C. Eversteijn, "Low-Temperature Deposition of Alumina-Silica Films", *Philips Res. Repts.*, Vol. 21, p. 379 (1966).

of boric oxide. Etch rate curves of this type were discussed in an earlier paper.[7] Once calibration curves of etch rate as a function of film composition have been established, the etch rate allows a rapid means of estimating the composition of a given layer. Etch rate data have also been utilized for determining the composition of phosphosilicate[7,10] and aluminosilicate[11] films. Similarly, etch times for films of known composition can be used for checking the film thickness, once a calibration has been made.

Conclusions

For end-point determination, the change from a hydrophilic dielectric surface to a hydrophobic semiconductor surface in the presence of hydrofluoric-acid-containing etchants is a readily observable phenomenon. Automation of the sample movement facilitates the procedure and contributes to the accuracy and precision of the method.

The etching time is not critically affected by the sample size or by the mode of agitation. Accuracy and precision of the analysis depends upon the length of etch time and the method used to measure thickness. For example, thermally grown silicon dioxide films 1-micron thick can be measured with a precision of ±2% if the thickness is determined by multiple-beam interferometry, or ±1% if the thickness values are obtained by ellipsometry.

The method is applicable for determining the etch rates of many types of oxide and silicate glass films on polished semiconductor substrates.

The determination of film composition when thickness is known or the film thickness when composition is known, can readily be carried out once calibration curves have been prepared.

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DC SPUTTERING WITH RF-INDUCED SUBSTRATE BIAS

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Summary—A technique has been developed that utilizes rf sputter-etching to clean substrate surfaces and dc sputtering to deposit metals. During dc deposition, a negative bias voltage can be impressed upon the substrates by coupling rf power through the substrates using the rf sputter-etching supply. The rf-induced substrate bias is especially valuable for deposition of very thin metal films, since the bias is impressed on the substrate from the onset of deposition. With dc bias, no effect is evident until a conducting film is achieved on an insulating substrate.

This technique produces highly adherent, pin-hole-free metal films on a variety of surfaces. The resistivity of these films closely approaches bulk value, even for very thin films. Metals having low crystallization temperatures undergo various changes in crystallinity. Preferred orientation in the closest packing plane occurs in metals that do not oxidize. Grain growth and grain-boundary oxidation occur in metals that tend to oxidize rapidly.

Introduction

IT IS OFTEN DESIRABLE to deposit pure metal films on very clean surfaces. In many cases, the rapid growth of surface oxides and the adsorption of contaminants on substrate surfaces during and after cleaning in aqueous or solvent media make it impossible to provide a truly clean surface. There are, however, numerous methods by which pure metals can be deposited on clean surfaces.

This paper discusses one of these methods—the sputtering process. In this case, because of the relatively high gas pressures used and because of outgassing from sputtering fixtures, substantial amounts of gas can be incorporated into sputtered films.[1,2] To eliminate, or at least reduce this phenomenon, bias sputtering[3] and asymmetric ac sputter-

[1] H. F. Winters and E. Kay, "Gas Incorporation into Sputtered Films," *Jour. Appl. Phys.*, Vol. 38, No. 10, p. 3928, Sept. 1967.

[2] J. Sosniak, "Mass Spectrometry of Background Gases in Glow-Discharge Sputtering of Tantalum Thin Films," *Jour. Vac. Sci. & Tech.*, Vol. 4, No. 2, p. 87, 1967.

[3] L. I. Maissel and P. M. Schaible, "Thin Films Deposited by Bias Sputtering," *Jour. Appl. Phys.*, Vol. 36, No. 1, p. 237, Jan. 1965.

ing[4-7] have been employed with success. However, gas adsorption is only part of the problem. The cleanliness of the substrate is not significantly enhanced by either of these sputtering techniques unless the substrate is an electrical conductor. If the substrate is a conductor, it is possible with the bias-sputtering technique to "sputter-etch" the surface immediately prior to deposition, thus ensuring a clean surface. The surface of the film is then "scrubbed" by relatively mild (50-200 eV) argon ions during deposition to outgas the film continuously while it is being deposited. The desirability of this simultaneous etching and deposition procedure has been confirmed by Winters and Kay[1] in a very direct fashion.

When insulating substrates are used, however, a small, nonuniform Langmuir sheath is formed initially on the substrate surface. Depending upon the discharge conditions, this sheath can be, at most, a few tens of volts in the dc-bias sputtering mode,[3,8] since the insulating surface is essentially a large-area floating probe.[9] Hence, little "sputter-etching" would be expected to occur.

Mattox and McDonald[10] were able to deposit adherent cadmium (Cd) films on iron (Fe) at dc-sputtering voltages above 1500 volts, but not below. This was attributed to a low particle density and low sticking coefficient of Cd on Fe. Optimum adherence was not achieved until the accelerating voltage was increased to 4000 volts. This work is significant in that Cd and Fe are mutually insoluble. It is quite likely that a thin oxide layer on the Fe substrate was, at least in part, responsible for the poor adhesion in the lower voltage range, in addition to the causes enumerated by Mattox and McDonald. At higher voltages, the arriving material is capable of penetrating the oxide surface.

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[4] R. Frerichs, "Superconductive Films Made by Protected Sputtering of Tantalum or Niobium," *Jour. Appl. Phys.*, Vol. 33, p. 1898, May 1962.

[5] R. Frerichs and C. J. Kircher, "Properties of Superconducting Niobium Films Made by Asymmetric AC Sputtering," *Jour. Appl. Phys.*, Vol. 34, No. 12, p. 3541, Dec. 1963.

[6] F. Vratny and D. J. Harrington, "Tantalum Films Deposited by Asymmetric A-C Sputtering," *Jour. Electrochem. Soc.*, Vol. 112, No. 5, p. 484, May 1965.

[7] Eric Kay, "Prevention of Oxidation in a Glow Discharge Environment with Sputtered Permalloy Films as an Example," *Jour. Electrochem. Soc.*, Vol. 112, No. 6, p. 590, June 1965.

[8] L. I. Maissel, "Deposition of Thin Films by Cathode Sputtering," *Physics of Thin Films*, Vol. 3, p. 61, ed. by G. Hass and R. E. Thun, Academic Press, New York (1966).

[9] Francis F. Chen, "Electric Probes," *Plasma Diagnostic Techniques*, p. 113, ed. by R. H. Huddlestone and S. L. Leonard, Academic Press, New York (1965).

[10] D. M. Mattox and J. E. McDonald, "Interface Formation During Thin Film Deposition," *Jour. Appl. Phys.*, Vol. 34, p. 2493, Aug. 1963.

Later, Maddox[11] reported on the "ion-plating" technique, which utilizes a glow discharge between an evaporation filament (at anode potential) and a substrate (at cathode potential). The evaporant is ionized and deposits at high energy while the substrate is being continuously cleansed by the ion bombardment from the Crooke's dark space. Again, when insulating substrates are used, initial cleaning of the substrate is minimal. Until a metal film is deposited on the surface so that the true cathode potential can exist on the surface, little "sputter-etching" can occur. In this case, as in many others, the high arrival energy of the depositing material allows penetration of the substrate surface, resulting in the observed high adhesive strengths.

In many cases, these high adhesive strengths are not achieved, because of the variability in composition and structure of surface oxides with time and environmental conditions and because of the random nature of adsorbed contaminants. This paper describes a technique for producing pure metal films on clean insulating or conducting surfaces. The method utilizes rf sputter-etching[12-14] to clean the surface in a low-pressure argon discharge and dc sputtering as the metal-deposition technique. The rf sputter-etching module is used as a means of applying a negative bias during deposition of the metal film, as has been suggested by Davidse.[15]

Apparatus

Figure 1 shows a cross section of the various sputtering fixtures in the system. The rf sputtering fixtures are identical to those described previously.[14] A metal cylinder is used in place of a bell jar, and an aluminum base plate with a dc sputtering module and shutter are located at the top of the cylinder. The two sputtering targets (dc and rf) are concentric.

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[11] D. M. Mattox, "Film Deposition Using Accelerated Ions," *Electrochem. Tech.*, Vol. 2, p. 295, Sept.-Oct. 1964.

[12] G. S. Anderson, W. N. Mayer, and G. K. Wehner, "Sputtering of Dielectrics by High-Frequency Fields," *Jour. Appl. Phys.*, Vol. 33, No. 10, p. 2991, Oct. 1962.

[13] P. D. Davidse, "RF Sputter Etching—A Universal Etch," Extended Abstracts, *13th Nat. Vacuum Symposium*, Amer. Vacuum Soc., San Francisco, Calif. (1966).

[14] J. L. Vossen and J. J. O'Neill, Jr., "R-F Sputtering Processes," *RCA Review*, Vol. 29, p. 149, June 1968.

[15] P. D. Davidse, "Theory and Practice of RF Sputtering," *SCP & Solid State Tech.*, Vol. 9, No. 12, p. 30, 1966; "Theory and Practice of RF Sputtering," *Vacuum*, Vol. 17, No. 3, p. 139, 1967; "Theory and Practice of RF Sputtering," *Proc. Symposium on Deposition of Thin Films by Sputtering*, Univ. Rochester, p. 75, June 9, 1966.

The dc target assembly is similar to the rf assembly, except that the anode shields are spaced quite closely to allow high-pressure dc sputtering without spurious discharges in the fixtures. In the cross section shown, the dc target is supported by clamps around the target edge to permit rapid target changes. If the dc target need not be changed, it would be preferable to attach the dc target to its backing plate in a permanent fashion by means of a vacuum adhesive or by

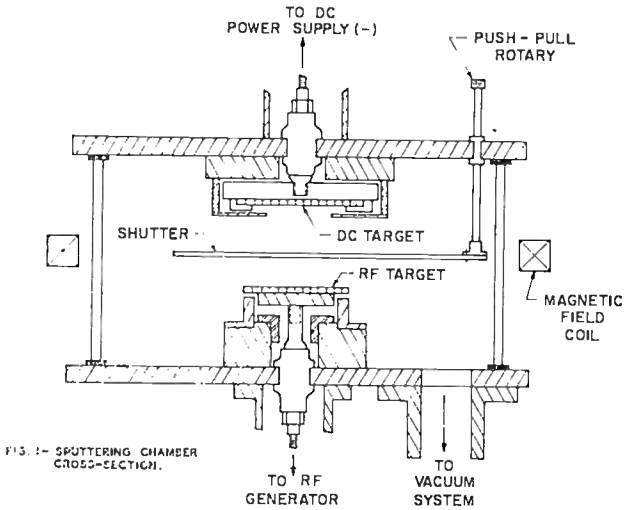


FIG. 1 — SPUTTERING CHAMBER CROSS-SECTION.

Fig. 1—Sputtering-chamber cross section.

cladding of the desired target metal onto a backing plate. This would allow elimination of the anode shield over the clamps (see Figure 1) and would provide complete use of the target surface area. It is well-known that anode shields in front of a target result in field distortions at the target surface in the vicinity of the shield. These can be eliminated by using a magnetic field to constrict the discharge from the shield edge.[16] For experimental purposes, using a variety of target metals, we have found no serious problems with the arrangement shown. The principal disadvantage of this arrangement is the necessity for careful outgassing of the interface between the dc target and its backing plate prior to starting a run.

The equivalent electrical circuit is shown in Figure 2. The capacitor, C_x, in the rf circuit serves as part of the matching network and

[16] W. N. Huss, "Advances in Sputtering Equipment Technology," *SCP & Solid State Tech.*, Vol. 9, No. 12, p. 50, 1966.

simultaneously isolates the dc voltage from the rf power source. L_s is an rf choke that isolates the rf voltage from the dc supply. The dc voltmeter is a VTVM with an input resistance of 1.1×10^9 ohms. The remainder of the circuit has been described previously.[14]

This system should not be confused with the one reported by Vratny[17] where the dc and rf voltages are superimposed on the same target surface. In the present case, the rf is connected to one target, which also serves as the substrate holder, and the dc power is connected to a different target. In the absence of rf power, the "sub-

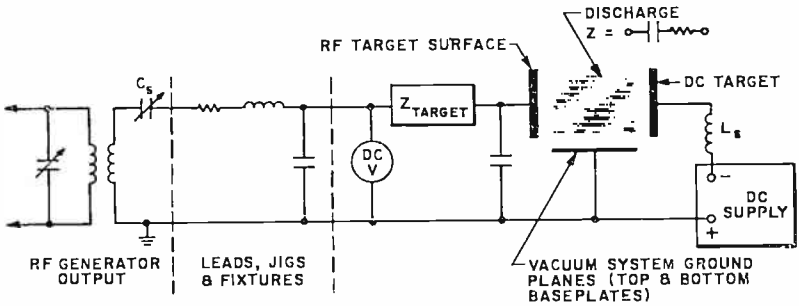


Fig. 2—Equivalent circuit.

strate platform" is a floating, large-area (approximately 45 cm^2) Langmuir probe in the dc discharge. In this condition, the sheath potential on the "substrate platform" (i.e., the rf target backing plate) varies with the discharge conditions and is relatively uncontrollable. It can vary with dc voltage, pressure, magnetic field, etc., from a few volts to about 30 volts. It varies also with the value of C_s since this capacitor is charged by the sheath potential.

When the rf power is applied to the substrate platform, the sheath voltage is increased to higher negative values.[15,18] The magnitude of the sheath voltage is almost exclusively determined by the time average of the rf generator output waveform; the other parameters mentioned above have a negligible effect on the sheath voltage. The rf generator used in these studies is a class-C power oscillator. The rf voltage is modulated by the generator power supply, which is full-wave

[17] F. Vratny, "Deposition of Tantalum and Tantalum Oxide by Superimposed RF and D-C Sputtering," *Jour. Electrochem. Soc.*, Vol. 114, No. 5, p. 505, May 1967.

[18] H. S. Butler and G. S. Kino, "Plasma Sheath Formation by Radio-Frequency Fields," *Phys. Fluids*, Vol. 6, No. 9, p. 1346, Sept. 1963.

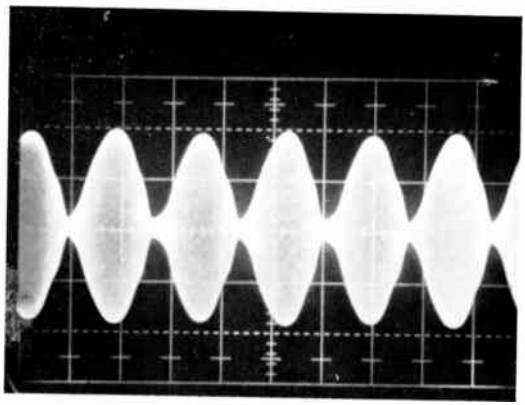


Fig. 3—RF-generator output waveform (17 MHz rf modulated by 120 Hz power supply).

rectified. The resulting output waveform is shown in Figure 3. The time average of this waveform at the rf target surface varies with the envelope peak-to-peak voltage as shown in Figure 4.

To utilize the apparatus shown in Figure 1 for the deposition of pure metals on clean surfaces, the substrates to be coated are set in place on the rf target. The target to be used for metal deposition is clamped into the dc module on the top baseplate. With the shutter interposed between the two targets, the dc target is first sputtered to clean its surface and to outgas the interface between the target and its backing plate. Second, with the dc discharge on and the shutter

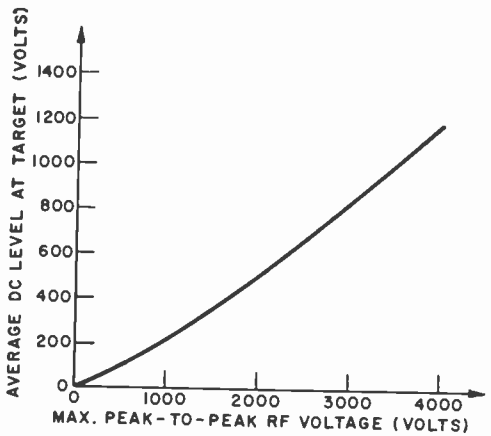


Fig. 4—Average dc level versus maximum peak-to-peak rf voltage.

still in place, the rf target is turned on and the substrates are sputter-etched, typically at an average surface potential of −600 volts. Next, the rf power is reduced to the desired substrate bias level, the shutter is opened, and deposition proceeds.

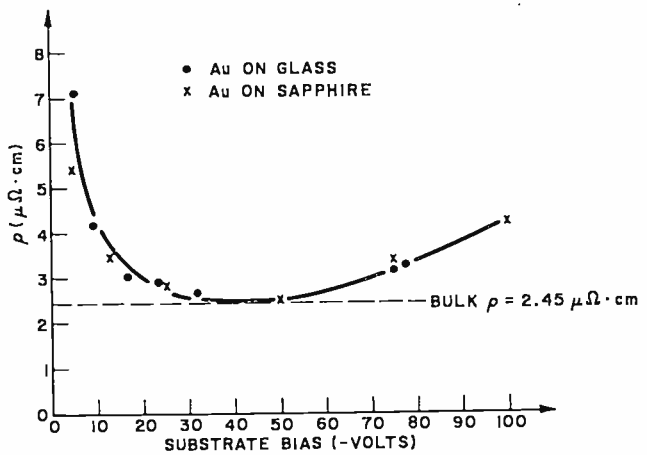


Fig. 5—Resistivity of Au films (6000 Å thick) versus substrate bias.

Results and Discussion

The metals that have been investigated to date are Al, Au, Cr, Cu, Ni, Pt, Ti and Ta. Representative data bearing on resistivity, adhesion, deposition rate, and crystallinity of films are given.

Resistivity

The resistivity of Au films as a function of the bias employed in the sputtering is typical for the noble metals investigated (Figure 5). The data for Au sputtered onto glass and onto sapphire substrates are essentially identical, and bulk metal properties are achieved at an average bias level of 40-50 volts. The fact that the substrate bias is applied continuously from the onset of deposition seems to be advantageous for very thin films. Figures 6 and 7 illustrate this for Cu and Ta on glass. Even at thicknesses of 700 Å, in the case of Cu, bulk properties are approximately achieved at 30-40 volts bias. In Figure 7, it is clear that 1600 Å films deposited with rf bias more nearly approach bulk properties than 3000 Å films deposited with dc bias. The shape of all these curves is similar to that obtained with dc bias sputtering and is primarily related to outgassing of the films during deposi-

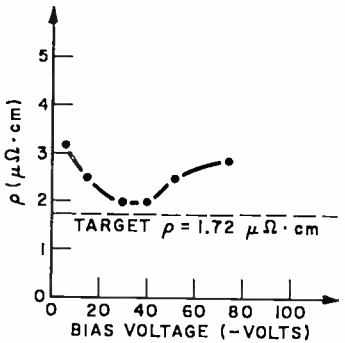


Fig. 6—Resistivity of Cu films (700 Å thick) versus substrate bias.

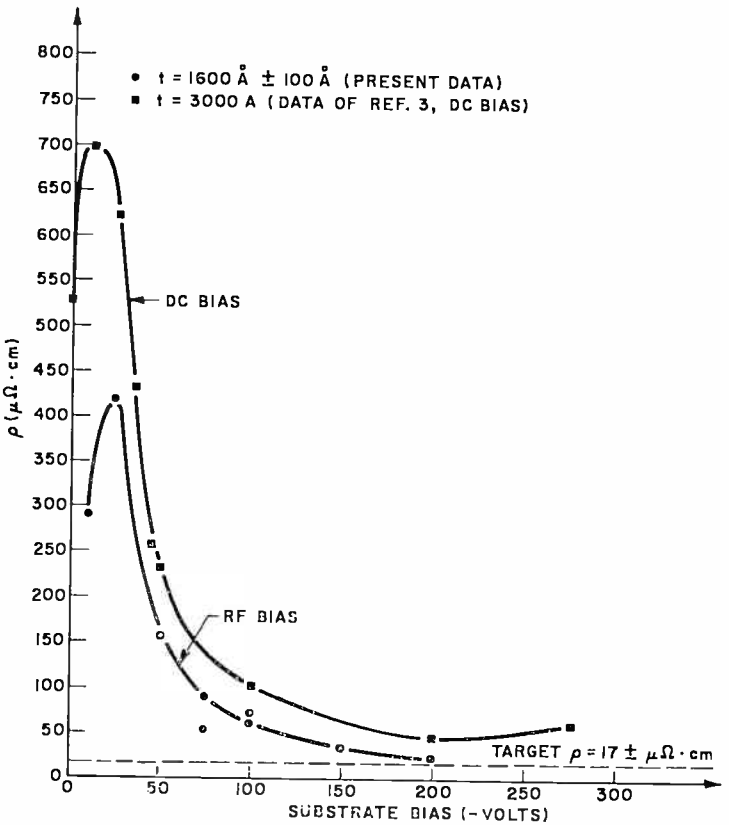


Fig. 7—Resistivity of Ta films versus substrate bias for both dc- and rf-induced bias.

tion.[1,3] The slight deviations from bulk value at the minima are thought to result from surface oxidation upon venting the system. Bulk values are achieved for noble metals.

Adhesion

Bond strengths were tested by sputtering 5000 Å layers of Pt, Ni, or Au onto W layers that had been deposited on polished silicon wafers. The sputtered layers and the tungsten layers were etched to leave 0.005-inch-diameter dots of metal. Nail-head wire bonds were made to the sputtered layers with 0.005-inch-diameter Au wires. The wires were then pulled normal to the substrate in a pull tester until a failure occurred. Approximately fifty pull tests were conducted on each of the three sputtered metals. In no case was failure observed at the sputtered-metal-tungsten interface. Ordinarily, either the Au wire broke or the W layer pulled a small piece of silicon from the substrate. Hence, we can say only that the pull strength of the sputtered-metal-to-W bond was greater than the maximum pull strengths measured, 22,000 psi.

It is especially interesting to note that there was no apparent difference in bond strengths among the three metals tested, even though Pt and Ni are soluble in W, while Au is not.

Deposition Rates

When high-sputtering-yield metals are deposited, there is a fairly large change in deposition rate with increasing substrate bias. This was found to be the case for Au, Cu, and Pt, for instance, but was not noticeable for Al, Ta, Ti, Ni or Cr. The results on Au and Cu films are typical (Figure 8). All other conditions being maintained as closely as possible, the deposition rate first increases to a maximum at a bias voltage somewhat above that producing a minimum in resistivity and then falls off as higher voltages are applied.

The initial rise is caused by the fact that the rf bias increases the dc discharge current linearly, as shown in Figure 9. This, coupled with increasing ion bombardment of the substrate surface, results in the curves shown in Figure 8. For lower-sputtering-yield metals, these two effects nearly cancel each other over the bias range investigated, resulting in no apparent change in the deposition rate. With the rf and dc power both connected to the same target, Vratny[17] observed increases in the plasma density that were higher than those shown in Figure 9.

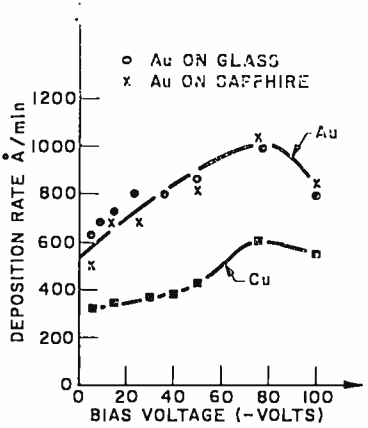


Fig. 8—Deposition rate versus substrate bias (for Au $V_{dc} = 3000$ volts; for Cu, $V_{dc} = 2000$ volts).

Crystallinity of Deposited Films

The substrates must be viewed both as receivers of material from the main dc target and as low-energy rf targets, since they are being ion bombarded. In a parallel-plate glow-discharge system, it is extremely difficult to obtain meaningful data on crystallographic effects because of numerous variables that cannot be controlled precisely.

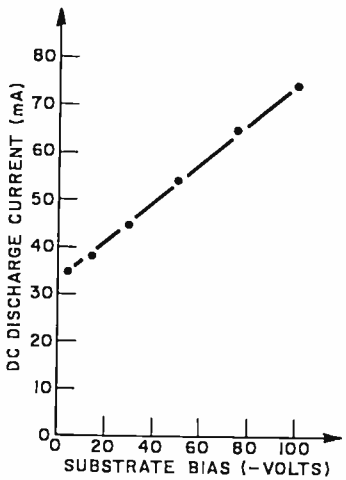


Fig. 9—DC discharge current versus substrate bias (Cu target, $V_{dc} = 2000$ volts).

These variables have been reviewed by Wehner[19,20] and Kaminsky,[21] among others. In addition to those variables that cannot be controlled in dc parallel-plate configurations (e.g., angle of incidence, uniformity of bombarding energy, multi-charged ions, and reflection of sputtered material back to the target), the use of rf-induced bias introduces yet another set of variables, namely nonuniform field strength and sheath thickness with time[12,18] and interactions between the dc and rf discharges that are difficult to measure.[17] The present system was built for reasons other than gathering quantitative information on the crystallinity of films. However, certain qualitative information can be reported.

Table I

Metal	Crystal Form	Bulk Recrystallization Temp.[22] °C
Al	fcc	150
Au	fcc	200
Cr	bcc	~640
Cu	fcc	200
Ni	fcc	600
Pt	fcc	450
Ti	hex	~550
Ta	bcc	1000

The substrates in our system are not cooled. Depending upon the plasma density, the substrate temperature can vary from 150°C to 300°C. With increasing substrate bias, (1) the substrate temperature increases, (2) the substrates are subjected to increasing bombardment, and (3) occluded gases are desorbed faster. The combination of these circumstances influences the crystallinity of metals whose bulk recrystallization temperatures are low. Table I lists the metals studied and their bulk recrystallization temperatures (the minimum temperature at which recrystallization can occur in bulk).

It is well known that sputtered films are usually polycrystalline with very small grain sizes (~200 Å). For deposition periods up to one hour, at dc target voltages up to 3000 volts and rf-induced bias levels up to −200 volts, this same behavior is noted for those metals

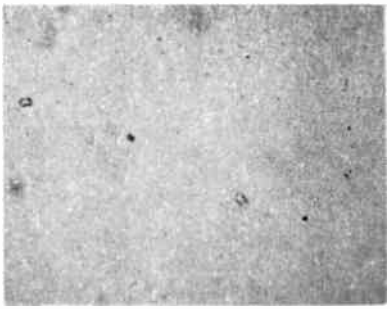
[19] G. K. Wehner, "Controlled Sputtering of Metals by Low Energy Hg Ions," *Phys. Rev.*, Vol. 102, p. 690, May 1, 1956.

[20] G. K. Wehner, "Sputtering by Ion Bombardment," *Adv. in Electronics & Electron Phys.*, Vol. 7, p. 239, 1955.

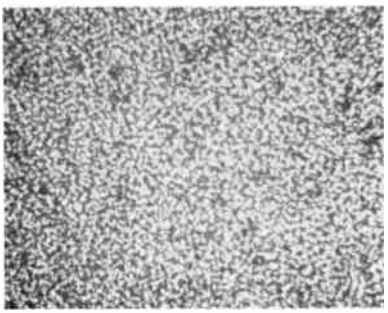
[21] M. Kaminsky, *Atom and Ionic Impact Phenomena on Metal Surfaces*, Chap. 10, Academic Press, New York (1965).

[22] Bruce Chalmers, *The Structure and Mechanical Properties of Metals*, pp. 68-72, John Wiley & Sons, New York (1961).

having bulk recrystallization temperatures greater than 300°C (Cr, Ni, Pt, Ti, and Ta). The films produced are fine-grained polycrystals, and no changes in crystallite size or orientation are observed with changing bias up to the limits studied.



A. FINE GRAINED AT 10 Å/MIN., 50 V. BIAS.



B. COARSE GRAINED WITH GRAIN BOUNDARY OXIDATION AT 50 Å/MIN., 50 V. BIAS.

Fig. 10—Microstructure of Al films.

In the cases of Au, Al, and Cu, however, certain changes are observed that seem to be related to the propensity of the metal to oxidize. Grain size, grain-boundary oxidation, and preferred orientation were examined by reflection and transmission electron diffraction, x-ray diffraction, or optical and electron microscopy, as the circumstances warranted.

Al has a very low bulk recrystallization temperature and is quite prone to oxidation. As the bias voltage is increased, the fine-grained structure of Al films (Figure 10(a)) gives way to increased grain growth and the grain boundaries oxidize when the system (Figure 10(b)) is vented. An analogous result is obtained in the "hot work-

ing" of Al when the hot working is stopped above the recrystallization temperature. Then, considerable grain growth and grain boundary oxidation are known to occur.[22] However, if the rf-induced bias is turned off near the end of a run, without stopping the dc discharge, and the dc discharge is then slowly reduced (100 volts/minute), the

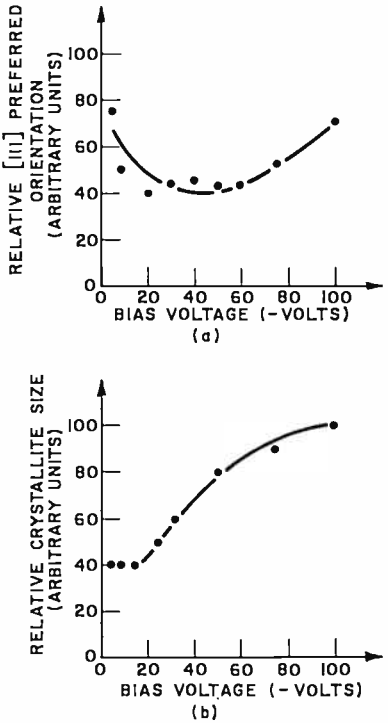


Fig. 11—Preferred orientation and crystallite size of 6000 Å Au films versus bias.

substrate is "hot worked" *through* the recrystallization point and the fine-grained structure is retained.

At the other end of the spectrum is Au, which has very little tendency to oxidize. In this case, the films exhibit preferred orientation, a {111} face being adjacent to the substrate surface—the tightest packing plane for fcc metals. The relative amount of {111} orientation is high at the floating potential (~5 volts), decreases to a minimum as the rf bias increases (because of ion bombardment, which tends to break up the lattice), and then increases again at higher bias levels because of the higher substrate temperatures (Figure 11). Simul-

taneously, the crystallites grow in size and the morphology of the surface changes from rough to smooth to rough (Figure 12). The roughness here, however, is far less than that evidenced in Al films. In the case of Al, the grain-boundary oxidation must expand the structure locally, producing gross roughness; with Au, however, it is necessary to resort to the scanning electron microscope to perceive the differences in morphology.

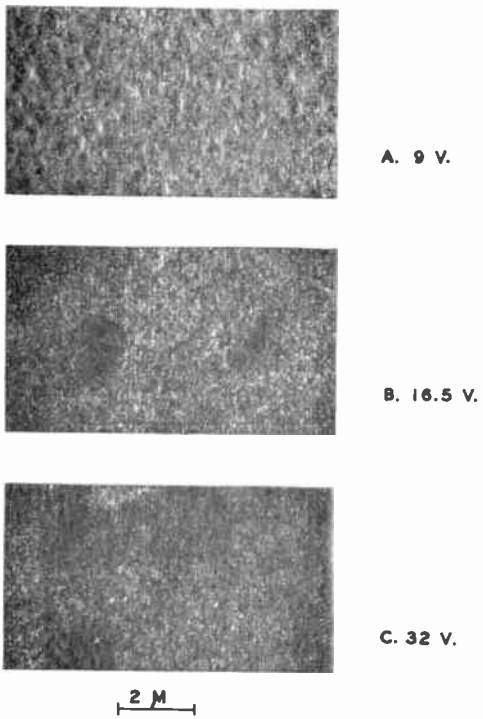


Fig. 12—Morphology of 6000 Å Au films versus substrate bias.

For very thin Au films (~600 Å) examined by transmission electron diffraction and microscopy, there was no indication of preferred orientation and no variation of crystallite size with bias. All films (up to 100 volts bias) were fine grained and polycrystalline. The only change occurring with bias in these films was in film continuity, which was greatest at 50 volts bias (corresponding to the resistivity minimum) and less at higher and lower voltages (Figure 13). Here again, the advantages of rf-induced bias are evident for very thin films.

Cu represents an intermediate case. Some slight {111} preferred

orientation is observed, and grain growth and grain-boundary oxidation can occur, but not as obviously as in the case of Al.

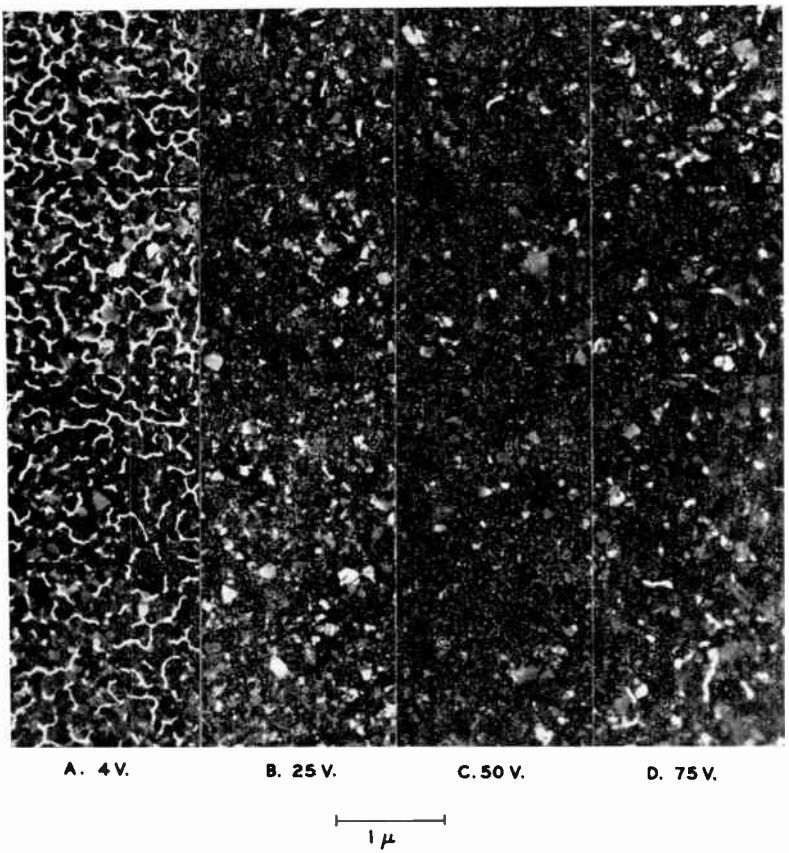


Fig. 13—Transmission electron micrographs of 500 Å Au films.

Summary

The combination of rf sputter-etching to clean substrate surfaces and rf-induced substrate bias during deposition has been shown to improve the quality of dc-sputtered metal films. This technique is particularly useful for very thin films, since the bias voltage can be applied from the onset of deposition, whereas with a dc bias, no effect of the bias is evident until a conducting film is achieved on an insulating substrate.

Metals having low recrystallization temperatures undergo various

changes in crystallinity as a function of substrate bias. From the preliminary qualitative data given here, it is difficult to draw any general conclusions. However, preferred orientation in the closest packing plane seems to be the main dependent variable in metals that do not oxidize readily, while grain growth and grain-boundary oxidation occur in metals that tend to oxidize rapidly. Further work is being undertaken to clarify these conclusions.

ACKNOWLEDGMENTS

We express our gratitude to P. Sahm for evaluating the adhesion of these films and for many helpful discussions; to W. C. Roth, who ran the electron diffraction, x-ray diffraction, and electron microscopic analyses; and to J. M. Shaw, who deposited the tungsten layers.

ADDITIVE PROCESSING TECHNIQUES FOR PRINTED-CIRCUIT BOARDS

By

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Summary—Additive process techniques are described that permit the fabrication of single-sided, double-sided, and multilayer circuit boards. Offset-printing techniques are used to delineate the patterns for conductor build-up; nonflow adhesives are employed in the assembly of boards prior to final interconnection. The additive approach provides considerable flexibility in the choice of dielectric and conductive materials and in the variety of configurations that can be employed to give buried connections from layer to layer.

Introduction

THE MATERIALS and processes used in the fabrication of conventional printed-circuit boards have not changed appreciably in the last several years. Although satisfactory boards can be prepared by these conventional methods, the reliability and the yield of boards could be greatly improved by introducing new technology. Furthermore, the need for multilayer circuit boards suitable for direct attachment of integrated-circuit chips is becoming more apparent, especially with the development of hermetically sealed chips, such as "beam-lead" circuits.

Accordingly, for the last few years a program has been under way to study new materials and to devise new and improved methods of preparing multilayer printed-circuit boards. The principal technologies used include: (1) new polymer materials as the dielectric element of the board, (2) punching rather than drilling of via holes, i.e., holes through individual boards, (3) additive (plating-up) rather than etch-down techniques to form the conductor patterns, (4) new methods of improving adhesion of the plating to the polymer, (5) offset printing rather than screen printing or photoresisting to form patterns, (6) lamination of the individual punched boards using nonflow adhesives and (7) final plating of the through-holes to provide continuity from front to back.

The advantages of this approach to preparing circuit boards are given in more detail in the discussion below. Briefly, they include: (1) finer line definition than conventional screening processes, (2) less

expensive processing than conventional photoresist processing, (3) more reliable through-hole connections, and (4) no need for drilling assembled boards, a frequent source of failure. In addition, more economical boards can be obtained than with conventional etch-down processing, in part because of higher yields.

Description of the Additive Processing Method

Two basic methods are available for the fabrication of printed-circuit boards, the subtractive (etch-down) method and the additive (build-up) method.

The majority of the printed circuits manufactured today are processed using the subtractive method, i.e., chemical etching of copper-clad insulating boards. Resist patterns are formed with photoresists, photoresists in combination with plated gold or solder, or screen printing with acid-resist inks.

This processing method, has a number of limitations. Only a small variety of copper-clad polymer materials are available; thus, the choice of starting materials is limited. In the etching of patterns, the presence of pinholes in the resist pattern may lead to open circuitry, especially when fine lines are to be defined. Undercutting of the resist occurs during etching, particularly when plated etch resists are used, causing a line to be thinned or opened.

Additive processing, the technique described here, offers a number of advantages over the subtractive method. The key steps in additive processing, illustrated in Figure 1, comprise:

(a) Pretreatment of the substrate surface to promote adhesion of plated metal;

(b) Electroless plating with copper followed by a thin uniform electroplating. In this step holes through the substrate are also plated;

(c) Printing of a negative plating resist by offset or other technique to define the circuit pattern;

(d) Electroplating of exposed areas to the required copper thickness;

(e) Stripping of the resist and flash etching of the thin copper layer between the built-up pattern.

A schematic cross section of a resulting board element is shown in the last sketch of Figure 1. Double-sided boards are processed by forming holes in the substrate prior to step (a) and printing resist

patterns in registration with the holes on both sides in step (c). All circuitry and through-hole connections are formed simultaneously during the plating step.

Additive processing permits almost any plastic, vitreous, or ceramic material to be used as a starting point. Since conductor patterns are built up by plating (a resist pattern determining where plating should not occur), pinholes are much less troublesome. The slender

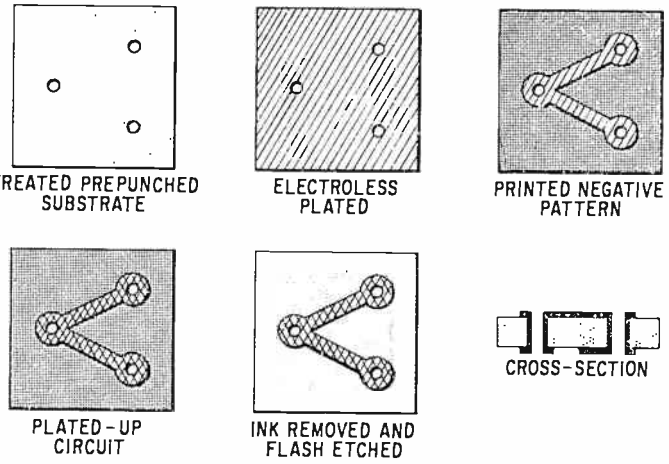


Fig. 1—Sequence of steps used in additive (build-up) process to form conducting patterns on a dielectric support.

columns of metal formed in a pinhole are usually etched free during the final flash-etching step. Furthermore, because the plated material tends to spread laterally as it increases in thickness, small discontinuities in a conductor line tend to be closed in the plating process. The additive method also offers potentially lower cost, since unclad boards are used and copper waste is eliminated.

The principal disadvantage in additive processing has been the difficulty of obtaining metal films that are sufficiently adherent to suitable dielectric substrates. Improved adhesion can be obtained, however, through the use of a surface pretreatment step prior to plating. For example, chemical treatments have been developed for a variety of plastic materials that give higher peel strengths for plated-copper layers than are obtained with conventional clad boards. Details of the materials, processes, and fabrication techniques for the additive process are discussed in the following sections.

Materials Used for Additive Processing of Circuit Boards

Dielectrics

In selecting dielectric materials for use in a printed-circuit board, an initial choice must be made between ceramic and organic materials. Ceramics have good high-temperature characteristics, excellent electrical properties, reasonable thermal dissipation, and a thermal coefficient of expansion more closely matching that of silicon, a property useful for direct attachment of integrated-circuit chips. With ceramic materials, however, the formation of large flat substrates with precision registered arrays of through-holes is difficult.

Polymer materials, such as glass-reinforced epoxy and phenolics, have been widely used in preparing single and multilayer circuit boards. They are more easily machined than ceramics and are less brittle. Their electrical and thermal characteristics are often satisfactory and they are considerably less expensive and lighter in weight than ceramics. Glass-reinforced materials, however, require critical drilling of holes and do not lend themselves readily to punching, particularly for small hole diameters.

An investigation of new organic polymer materials was carried out to determine their applicability to circuit fabrication. High-temperature plastics such as polysulfone, polyphenyleneoxide and polyimides offer several attractive features. Precise arrays of small-diameter via-holes can easily be punched in layers as thin as 0.002 inch without appreciable wear of the punch assembly. The electrical, mechanical, and physical properties are adequate for most circuit requirements. These materials have lower dielectric constants than standard reinforced materials, enabling thinner layers to be used for strip-line circuitry. Polysulfone has a major advantage in that, after suitable surface treatment, extremely adherent films of copper can be plated on electrolessly.

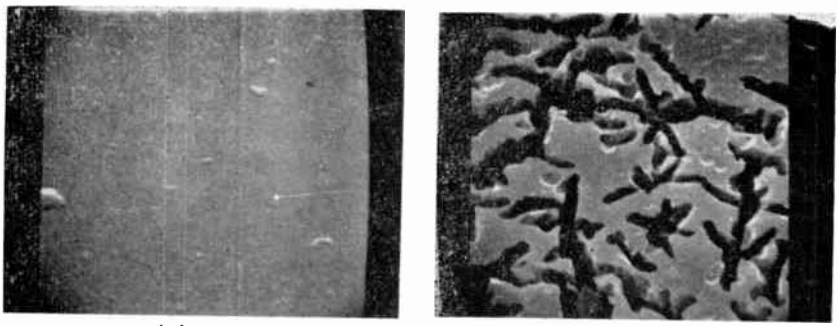
Surface Modifiers

The surfaces of most plastic sheets are smooth and nonporous. Metallization of this type of surface by electroless plating or vacuum deposition produces weakly bonded films that are not suitable for conductor circuitry. The surfaces must be modified by physical or chemical roughening or by the application of an adhesive coating to improve bond strength.

A program has been carried out to determine the effectiveness of bonds between plated metals and various plastics, and to study the

influence of various surface treatments on the bond strength. Results of this investigation, made with a scanning electron microscope,* are summarized below.

With copper-clad laminates, which were used as the reference standard, good adhesion is obtained by bonding oxidized foil to the plastic laminate with a suitable adhesive. The oxidized copper has a large convoluted surface, and strong mechanical bonds are produced due to embedding of the adhesive within the oxide structure. Peel strengths of 10 pounds per inch are typical.† Fracture of the interface occurs within the adhesive layer.



(a) UNTREATED POLYSULFONE 10,000X (b) TREATED POLYSULFONE 10,000X

Fig. 2—Scanning-electron-miscroscope photographs of a polysulfone surface: (a) untreated polysulfone × 10,000; (b) treated polysulfone × 10,000.

Adhesion of plated layers on most commercially available plastics is poor. Improved adhesion to a variety of thermoplastics can be provided, however, by special chemical surface treatments prior to plating. These treatments produce a microporous surface structure. In the subsequent metallization of these surfaces by electroless plating, metal is deposited within the surface pores producing a strong mechanical bond. Heat treatment after metallization further increases bond strength by tightening the porous surface around the deposited metal. Photographs of untreated 0.010-inch-thick polysulfone sheets and sheets treated with an adhesion promoter are shown in Figure 2. The treatment produces microcracks on the surface ranging from 1500 to 6000 angstroms wide and up to 8 microns in length. After plating to a copper thickness of 0.0015 inch, test data for these samples

* Cambridge Instrument Company, Cambridge, England.

† Measured with a 90° pull at a rate of two inches per minute.

showed a peel strength of 9 pounds per inch. This increased to 16 pounds per inch after heat treating for five minutes at 150°C.

Chemical treatments do not, however, function effectively for all polymer materials. Alternative methods of achieving adherent metal layers include physical abrasion of the surface, or coating the polymer surface with a suitable modifier that bonds both to the metal and to the polymer.

Conductors

Because of its high conductivity, platability, and relatively low cost, copper is almost universally used as the conductor material in the fabrication of printed-circuit boards. Copper is compatible with both ceramic and organic polymer materials and can be deposited in adherent films by either electroless or electrolytic methods. In the additive process, electroless deposition is used to coat the nonconducting substrate with an initial thin layer of copper. Copper of the required thickness is then built up by electroplating. As an alternative to copper, electroless nickel can be used to provide an initial conductive surface on the substrate. Also, other electroplated metals, such as nickel, solder, gold, rhodium and silver, could be used in the build up of conductors to impart special properties to the circuits.

Laminating Adhesives

Both double-sided boards and multilayer boards can be prepared by additive processing methods. When multilayer boards are required, individual layers having via-holes are laminated in registry.

In the lamination of prepunched layers, it is imperative that lamination be carried out with a controlled-flow adhesive material to prevent closing of the holes during the lamination step. The adhesive must be capable of providing a continuous firm bond between the layers and exhibit minimum flow into hole areas. Alternative approaches include coating the individual layers with a suitable adhesive, or including between adjacent boards a prepunched film coated on both surfaces with an adhesive layer. Examples of suitable adhesives are given in Appendix I.

Processes Used in the Fabrication of Additive-Process Circuit Boards

Prepunching of Substrates

One of the principal disadvantages of conventional multilayer-board processing is that through-holes are formed by drilling through

the laminated board. During the drilling step, the thin exposed edge of copper conductors on interior layers may be partially or completely covered over by polymer material ("epoxy smear") resulting in an open contact when the hole is finally plated through. Furthermore, even if a successful contact is made, the small contact region may open up during subsequent thermal cycling. Failures at the junction of internal conductors and plated-through holes are a major reason for failure of conventional boards.

These problems can be avoided and a more reliable board can be obtained if holes are formed in individual substrate layers prior to plating and lamination. Holes can either be drilled or punched in the dielectric material and, in an additive process, are then plated-through while the conductors are formed. When the individual boards are finally laminated, with holes in registry, a plating-through step provides a conductive "lining" in all holes. In this plating, which is described in more detail below, the contact area between the plating in the hole and the internal conductors is large, guaranteeing a good mechanical and electrical connection.

The simplicity of a punching operation for forming via-holes and the cleanliness and economy with which holes can be formed are major advantages for punching rather than drilling. In order to investigate the punching process and the use of punched circuit layers, a single-stage multiple punch-and-die set was designed and constructed for simultaneously punching 64 holes, each 0.010 inch in diameter, in a dielectric film. This punch was employed in the fabrication of the experimental multilayer boards described below.

Resist Pattern Formation

In the preparation of circuit boards, one of the most critical steps is the formation of resist patterns that define the conducting lines in the final board. Conventionally, this resist pattern is formed either by silk-screen or by photoresist techniques. In production, conventional silk-screen processes are limited in resolution to line widths of approximately 0.010 inch or wider. This limitation rules out screening when fine-line patterns are required, as for instance, when unpackaged integrated circuit chips, having contact pads 0.006 inch or less in their major dimension, are to be attached directly to the board. Commercial photoresists will provide the requisite fine lines, but are expensive from both the materials and the processing standpoints.

For many applications, dry offset printing appears more nearly ideal than either screening or photoresist processing. The major ad-

vantage of offset printing is the ability to form a pattern directly, with no further processing being required (such as developing a photoresist). Printing is an established art widely used in industry. Studies have shown that lines as narrow as 0.004 inch separated by as little as 0.002 inch can be defined successfully on a board. Large areas, up to

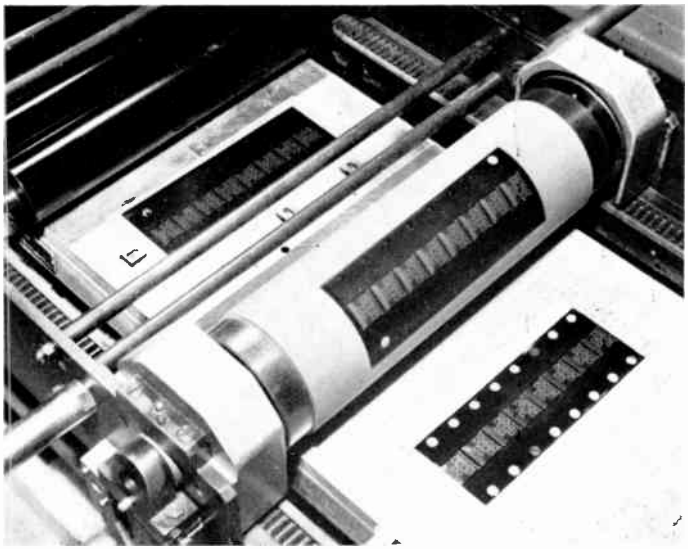


Fig. 3—Hand-operated offset-printing press showing (foreground vacuum chuck for holding substrates and (center) cylindrical transfer blanket with ink pattern from printing plate.

12 × 12 inches or greater, can be printed in one operation, while dimensional tolerances are held to less than 0.001 inch over the entire area.

Plating resist inks have been prepared that perform very satisfactorily as resists in an additive process. For this work, a manually operated offset printing press* modified for precise adjustment has been used, as shown in Figure 3. Examples of the definition obtainable with this press are given later.

The formation of printing plates for use with the offset press is greatly simplified by the availability of photopolymer materials especially made for the printing industry (for example, Dycril ** photopolymer plates). Master artwork is first prepared in a transparency

* Grauel model RO

** E. I. DuPont de Nemours, Inc., Wilmington, Delaware.

positive as described below. Contact exposure and development of the Dycril printing plate is carried out with commercial equipment, giving a relief image on the plate that is immediately usable for printing. Total time from exposure of the plate stock to the finished printing plate is about 20 minutes, and the cost of the Dycril plate is nominal.

Artwork masters are prepared in standard Rubilith, for simple patterns, or are generated with the help of an automatic coordinatograph.*

Conductor Pattern Processing

Any suitably treated and properly sensitized insulating substrate can be plated with a metal film by standard electroless deposition techniques. Normally 5 to 10 minutes is sufficient to deposit about 10 microinches of copper uniformly over the surface of the substrate. Although this electroless layer is reasonably conductive, a thin flash of electroplated copper can be employed to improve the physical and electrical properties of the metal film.

The metal-coated substrates are then offset printed with a negative resist pattern. Circuits are generally printed in an array on a single large substrate, and the resist patterns are dried by infrared or other means. The substrates are then racked for plating, dip-cleaned, rinsed, and electroplated with copper at a current density of 250 to 350 mA/inch^2. During the plating, conductor line width increases slightly with build-up thickness. This increase, a characteristic of additive processing, has the advantage that slight defects such as notches in the edge of a line or pin holes are filled-in during plating. A flash coating of gold or solder can be plated over the copper, if desired, to protect the circuitry during subsequent flash etching. The negative ink image is removed and the thin areas of exposed copper are etched away. An etching time of 5 to 15 seconds in ferric chloride is sufficient to remove the thin metal for fine-line circuit patterns having line and space dimensions of 0.004 inch.

The additive method described above has been used to fabricate conductor circuits on a wide variety of reinforced and non-reinforced plastic, ceramic, and glass substrates with equally good results. An electroless nickel deposit is also suitable as the initial metal film. Copper can then be plated over the nickel by the process described above.

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* Gerber Scientific Co., Hartford, Conn.

Examples of Circuit Boards Formed by Additive Processing

Double Layer Boards

Except for the lamination step, similar processing is involved in the fabrication of both double-layer and multilayer circuit boards. Double-sided boards require only that via-holes be punched in a single sheet of insulator prior to plating. After the thin, continuous copper layer is deposited, resist patterns are printed on both sides of the board. The wiring and the through-holes are then plated up in one operation.

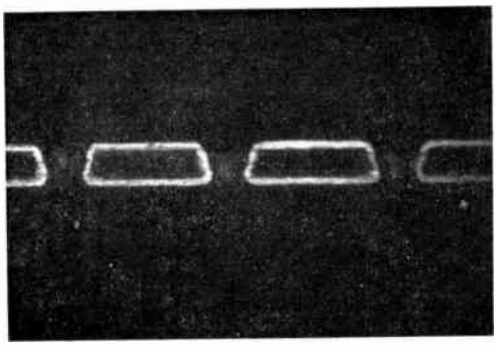

Fig. 4—Copper-coated 0.010-inch-thick polysulfone showing plated 0.010 inch through-holes.

For a double-sided board, additive processing has a considerable advantage over substractive processing. In the additive process, all circuitry is formed while the through-hole connections are being plated. The subtractive method begins with a more expensive starting material, requires the same plating step to form the through-hole interconnections and, in addition, requires the plating of a solder or gold etch-resist so that patterns can be delineated in the thick copper (cladding) layer. The copper removed in this step is expensive to recover and may cause disposal problems.

The additive-process double-sided board is the building block for multilayer circuits. As an illustration of boards formed by this process, photographs of a double-layer copper pattern on a polysulfone board are shown in Figures 4, 5, and 6. An interconnection pattern is shown in Figure 5, and a ground plane is shown in Figure 6. If desired, conductor line patterns could be formed on opposite sides of the board, providing jumpers.

This board was formed from a polysulfone sheet, 0.010-inch thick,

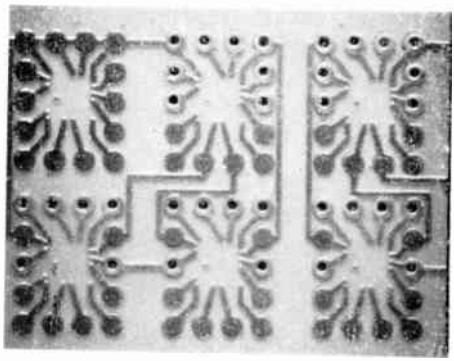

Fig. 5—Detail photograph of front signal plane showing 20-mil pads for via-holes and 10-mil holes punched through selected pads. Each rectangular fan-out pattern interfaces directly to pads on one integrated-circuit chip.

by additive processing and offset-printing techniques. The 64 via-holes are each 0.010 inch in diameter. The circuit interconnection pattern consists of 0.004-inch-wide conductor lines having a thickness of 0.001 inch. Adhesion of the copper to the polysulfone is greater than 10 pounds per inch. The copper is easily wet with eutectic lead–tin solder with no harmful effect on the mechanical strength of the copper–polysulfone bond or the polysulfone substrate itself.

Multilayer Board Fabrication

The same additive processing method described above for single- and/or double-layer boards can be used in the fabrication of multilayer

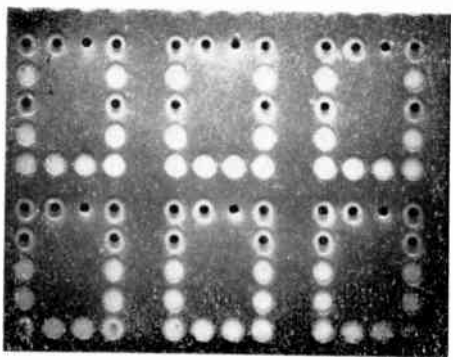

Fig. 6—Detail photograph of ground-plane wiring pattern showing, in each rectangular array, five holes that pass through the ground plane without making connection and one that connects to the ground plane.

boards. Two approaches can be used to form multilayer circuit boards. The first involves lamination of double-sided boards, all via-holes in registry, followed by plating through of all holes to provide front-to-back interconnections. The second approach involves a sequence of lamination and additive processing steps.

Future-generation circuitry will require tighter packaging densities and circuit patterns containing fine lines and spaces and small-diameter interconnecting holes. To test the feasibility of these methods for preparing complex multilayer circuit boards, a four-layer board was de-

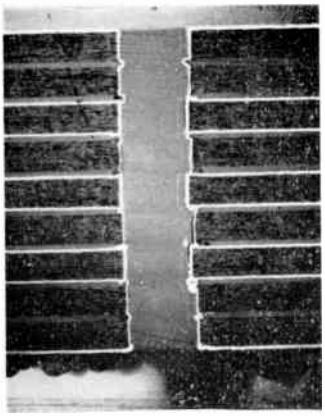

Fig. 7—Cross section of an eight-conductive-layer board.

signed as a test vehicle. The board was designed to accommodate up to 10 face-down bonded integrated-circuit chips and consists of two outer circuit planes having 0.004-inch-wide conductor lines, and two inner planes—a ground plane and a voltage plane. Overall final board dimensions are $0.65 \times 0.67 \times 0.025$ inch.

a. Laminated Double-Sided Board Method

The choice of approach is guided by the circuit design and materials required. Both require controlled laminating techniques and special adhesives to ensure registered lamination of the prepunched circuit boards, while preventing flow of adhesives into the hole areas. Boards designed with holes in the order of 0.030 to 0.040 inch in diameter can be laminated using controlled-flow thermosetting adhesives, as previously described, with good control of the adhesive (see Figure 7). The adhesive is applied to a support sheet or to a dielectric laminating

sheet by doctor blading a layer equivalent to a dry film thickness of 0.001 to 0.003 inch. A uniform thickness is required to prevent excess flow in high spot areas due to excess pressure on lamination. The film should be approximately 0.0005 inch thicker than the conductor-metal thickness to allow complete embedment of the circuitry. Adhesive films coated on thin plastic layers or reinforced layers can be used to laminate two or more double-sided circuit layers by prepunching the layers in the required hole pattern.

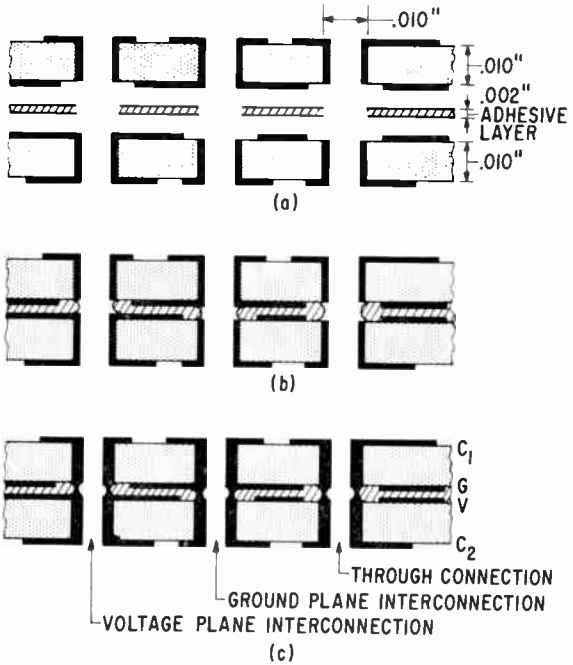

Fig. 8—Cross section of experimental four-layer circuit board showing circuit planes, (C_1, C_2); ground (G) and voltage (V) planes.

The fabricating sequence is shown in Figure 8 and is summarized as follows:

(a) Two double-sided circuit boards are individually prepared (as described previously) from 0.010-inch-thick polysulfone sheets having prepunched 0.010-inch-diameter via-holes. All 0.010-inch through-holes and 0.25-inch-diameter registration holes are punched simultaneously, using the multiple punch described earlier.

(b) A thin plastic sheet, coated on both sides with an adhesive layer, is also punched with the same hole pattern.

(c) The two double-sided boards, with the adhesive film between them, are assembled in registry in a laminating jig and laminated under heat and pressure.

(d) The laminated board is then coated with a thin layer of electroless copper, masked on both sides with a plating resist ink, and the interconnections are provided by plating a copper lining in all through-holes.

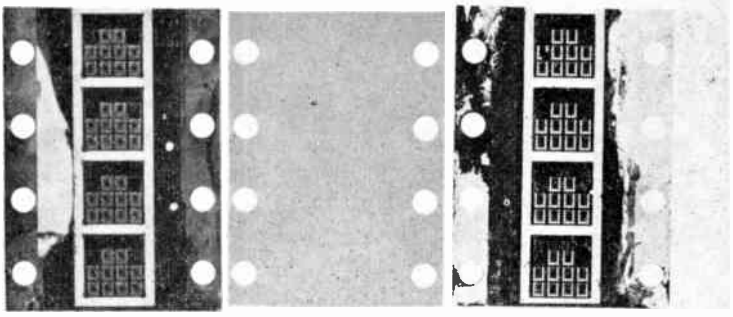

Fig. 9—Double-sided circuit layers showing circuit plane, ground plane, and punched adhesive layer.

(e) The ink is removed, and the thin electroless copper layer is flash etched to complete the circuit.

As an alternative procedure, the outside circuit planes can be defined in step (d) and the circuits built-up along with the interconnections.

Circuit interconnections made by this method should be more reliable than those made in conventional drilled and plated through-hole boards, since the connections are made to regions *previously plated* during the preparation of the individual double-sided boards. Since individual boards can be pre-tested electrically prior to lamination, the number of rejects for final boards can be minimized.

Boards were fabricated by this process using a modified polyester adhesive supported on 0.001- and 0.002-inch-thick polyimide film. Two double-sided circuit layers were prepared as shown in Figure 9 and laminated with prepunched adhesive layers at a temperature of 330 to

350°F and 50 to 100 psi. The circuits were completed as in steps (d) and (e) above. Test results showed that precise control of the materials and processing steps was required to obtain good boards, namely, control of adhesive-film thickness and punching, parallelism of the laminating jig, and control of the laminating cycle. Handling and control of thin, supported, adhesive layers is difficult and may necessitate designing with thicker layers to achieve a high-yield process. No difficulty was experienced in plating using standard electroless copper compositions and a copper pyrophosphate electroplating bath. Samples of individual layers and completed boards are shown in Figure 9 and 10.

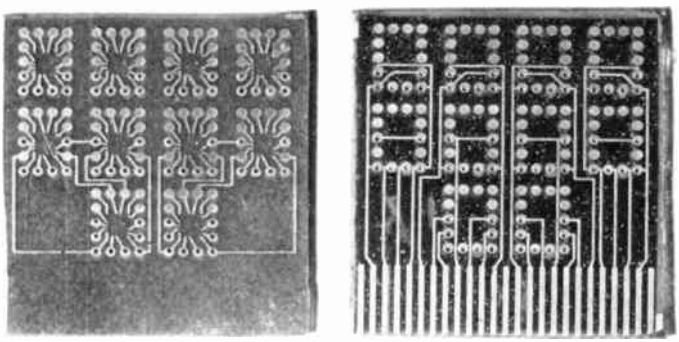

Fig. 10—Completed four-layer circuit boards showing outer circuit patterns.

b. Sequential Laminating and Plating Method

Multilayer boards can also be processed using a sequential-lamination technique, starting with a double-sided board as a core. The processing sequence for this method is illustrated in Figure 11 for the four-conductor-layer board previously described. A double-sided board is processed initially by the additive technique. Punched, adhesive-coated insulating layers are then laminated in registration with the core layer. The laminate is then plated with a thin layer of copper, negative circuit patterns are printed, and circuit layer C_1 and C_2 plated-up. In this method, interconnections are made by sequentially plating from one layer to the next.

Fabrication studies of four-layer circuit boards showed similar re-

sults to those obtained using the first method. Processing of the adhesive layer is easier when it is supported on the thicker circuit layers, and better control is indicated.

Both of the outlined methods can be extended to the fabrication of boards with a greater number of circuit layers and to providing open-

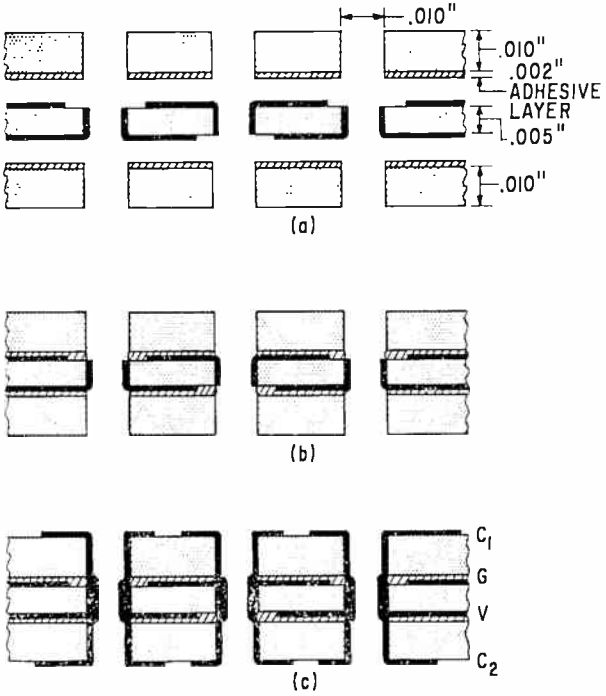

Fig. 11—Cross section of experimental four-layer circuit board fabricated with a sequential laminating technique.

access-hole connections and buried interconnections. This is illustrated for the sequential technique in Figure 12. As board thickness is increased, hole diameters must be chosen to provide adequate plating within the hole. Variations of the above methods can also be developed to include different conductor and insulator materials and the lamination of two or more separate multilayer structures.

CONCLUSIONS

Studies to date have shown that the additive method offers great versatility in the fabrication of printed circuits. A wide choice of materials is available and different types of interconnections can be

provided for multilayer designs. The adhesion of plated metals to certain plastics is greater than that obtainable with conventional clad laminates. Methods of improving the adhesion of plated metals are being developed for other materials. The offset-printing process can be used effectively to produce fine-line patterns directly for the additive process. These processes should also lead to greater reliability and lower cost for future circuit boards.

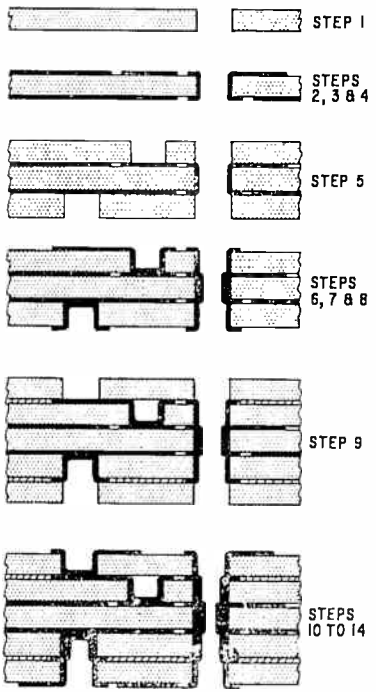

Fig. 12—Sequence for multilayer-board fabrication starting with double-sided circuit boards.

Appendix—Resin Systems for Controlled-Flow Adhesives

Two general types of resin systems can be used in controlled-flow adhesives: thermosetting resin systems with a controlled cure cycle, and modified thermoplastics. In our work, a variety of thermosetting epoxy-resin systems were formulated. These perform satisfactorily in the lamination of conventional reinforced circuit materials having holes in the order of 0.040 inch in diameter. Figure 7 shows the cross section of several 0.015-inch-thick phenolic layers laminated with a difunctional epoxy-resin adhesive system that was cycled through a controlled pre-

cure prior to lamination. The adhesive was applied to both sides of bare insulating layers; the layers were then punched, laminated alternately with double-sided copper conductor boards, and finally plated to interconnect all layers. A typical adhesive formulation is as follows:

Dicyandiamide	6 g
Benzyldimethylamine (.15 g/ml in carbitol acetate)	5 ml
Dimethylacetamide	60 ml
Carbitol Acetate	90 ml
Epoxy Resin—ERR-2010*	105 g
Epoxy Resin—ERR-0100*	45 g

Laminating schedule: 20 minutes precure of adhesive layer at 144°C followed by 10-30 minutes at 170°C and 50-100 psi.

Controlled-flow laminating resins similar to the one cited above and impregnated on glass cloth are available commercially.

In the second type, the flow of thermoplastic base adhesives can be controlled during lamination by regulating the temperature to prevent excess flow. Certain thermoplastics such as polyesters can be modified to exhibit thermosetting properties. These modified resins soften under heat and pressure with little lateral flow. Thin polyimide and polyester films coated with these adhesives have been used in the lamination of circuit layers prepunched with 0.010-inch holes.

* Union Carbide Corp., Plastics Division, N.Y., N.Y.

CALCULATION OF THE ELECTRICAL PARAMETERS OF TRANSISTOR CHIPS FROM MEASUREMENTS MADE ON PACKAGED UNITS

By

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Summary—*A method for calculating the electrical parameters of an unpackaged transistor chip from data given for the packaged device is described. The parasitic elements due to the package are estimated and an LC network comprised of negative-valued inductive and capacitive elements that cancel the effect of these parasitics is constructed.*

Once a parasitic model is established for a given package, the electrical parameters for any device chip in that package can be obtained at any frequency without changing the values of the negative elements. This technique should be helpful in the selection of devices for use in circuits employing directly bonded device chips, and should provide a more realistic set of device parameters for use in the design of such circuits. The technique should also be helpful in the design and selection of packages for semiconductor devices.

Introduction

In THE last few years the unpackaged transistor chip has come into use as a circuit component. This has been brought about by technological advances such as surface glassing[1-3] and/or the use of silicon nitride layers[4] that allow the transistor chip to be passivated, eliminating the need for an external hermetic package. Also, as improvements in switching speed and frequency response are required, and as circuit boards shrink, it becomes apparent that for many applications it is desirable or necessary that the transistor chips be mounted

[1] W. Kern, R. C. Heim, "Chemical Vapor Deposition of Silicate Glasses for Semiconductor Devices," presented at the Electrochemical Society Meeting, Boston, Mass., May 5-9, 1968.

[2] J. A. Perri, "Glass Encapsulation," *Semiconductor Products and Solid State Technology*, Vol. 8, p. 19, May 1965.

[3] S. S. Flaschen, R. J. Gnaedinger, Jr., "Surface Passivation Techniques for Microelectronics," in *Metallurgy of Semiconductor Materials 15*, Vol. 15, (1962), J. B. Schroeder, Edit., Interscience Publ., N. Y., 1962.

[4] G. H. Schneer, et al," A Silicon Nitride Junction Seal on Silicon Planar Transistors," presented at the October 1966 International Electron Devices meeting, Washington, D. C.

directly on the circuit boards to eliminate the physical bulk as well as the parasitic capacitances and inductances that are introduced by the packages. Much work has been done lately on the "flip-chip" or face-down, direct bonding of semiconductor chips to circuit boards.[5]

To design a circuit that uses a transistor in chip form, the designer must know certain characteristics of the chip. The electrical characteristics of the device (such as the h or y parameters) that are available to him have been measured on the packaged device. Included in the characteristics, then, are several parasitic capacitances and inductances that will not be present in the chip itself. At lower frequencies, these parasitics are of little consequence; but, for most packaged devices, the difference between the electrical parameters of the chip itself and those of the packaged device becomes significant at frequencies above 100 MHz.

A method of obtaining an estimate of the chip parameters from these data was therefore devised, and computations were carried out using as a vehicle a 2N2857 transistor, a high-frequency device capable of operation in the GHz region.

Method

The general method of making these corrections can be outlined as follows. A circuit model of the parasitic elements for a particular package is obtained. This model may be computed from the geometry of the package and or obtained by direct measurements of a package having a dummy chip mounted in it. Once a model of these parasitics is obtained for a particular package, that model can be used to correct any transistor mounted in that package, for any frequency.

A cancellation network is then designed, in which inductors having negative values of inductance are put in series with the parasitic inductances, and capacitors having negative values of capacitance are put in parallel with the parasitic capacitances. For example, if an inductor of value $-L$ is put in series with an inductor of value $+L$, the net result is a short circuit. Likewise, if a capacitor of value $-C$ is put in parallel with a capacitor of value $+C$, an open circuit results.

A circuit combining a transistor (having the parameters as measured in the package) and the appropriate cancellation network of negative elements is then analyzed by computer. The equivalent parameters

[5] G. Sideris, "Bumps and Balls, Pillars and Beams: A Survey of Face Bonding Methods," *Electronics*, Vol. 38, p. 68, June 28, 1965.

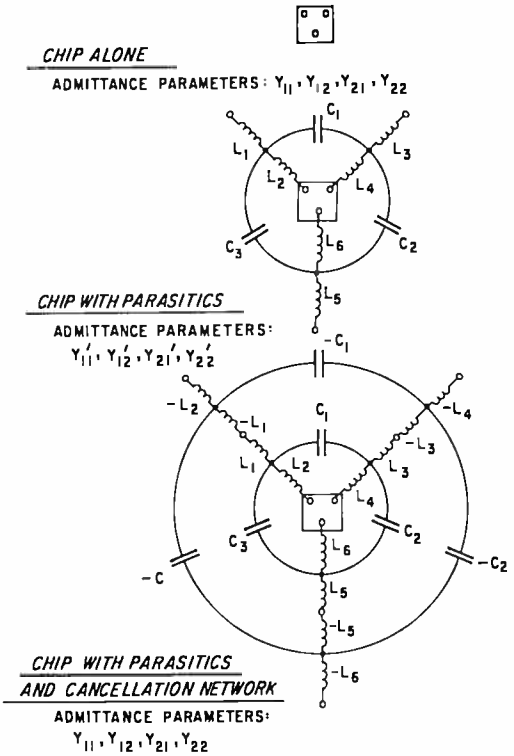

Fig. 1—Application of cancellation network to transistor chip in parasitic environment.

of the analyzed circuit are the parameters of the chip alone. An example illustrating this approach is given in Figure 1.

The admittance (y) parameters used throughout this paper are defined, as shown in Figure 2 as

$$I_1 = y_{11}V_1 + y_{12}V_2$$
$$I_2 = y_{21}V_1 + y_{22}V_2$$

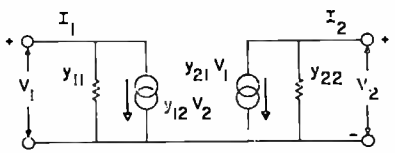

Fig. 2—Admittance (y) parameters.

The circuit analysis program used for this work was written by D. Ressler[6] for use with an RCA-601 computer.

Calculation of Chip Parameters for the 2N2857 Transistor

The 2N2857 transistor, a silicon n-p-n epitaxial planar transistor having a gain–bandwidth product of 1 GHz, was selected to demonstrate the method. Figure 3 shows the transistor chip mounted in a

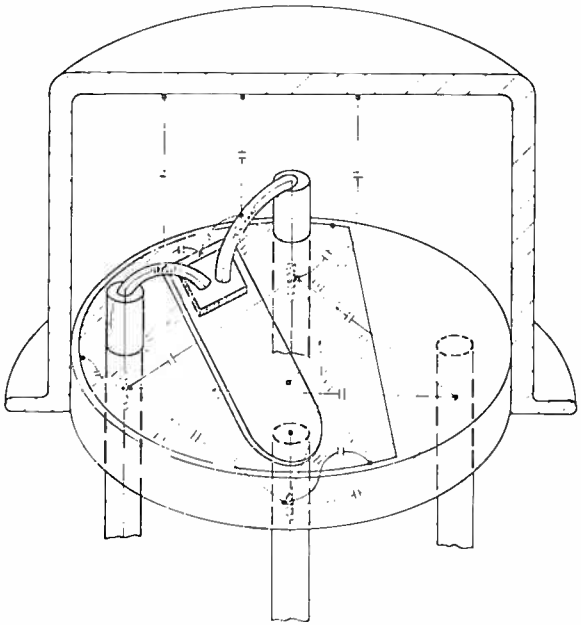

Fig. 3—Configuration of the 2N2857 transistor in a TO-72 package showing parasitic components.

TO-72 case, the parasitics to be considered being sketched in conventional symbols. A circuit diagram of the parasitics is given in Figure 4, and Table I shows the values calculated for the parasitics from purely geometrical considerations.

The diagram in Figure 4 is only a first-order approximation to the actual distributed nature of most of the parasitics, but it is believed that any resultant error would be small compared to the normal variation in parameter values among transistors of the same type. Of course, a better model could be obtained by dividing the inductances

[6] D. G. Ressler, Private Communication.

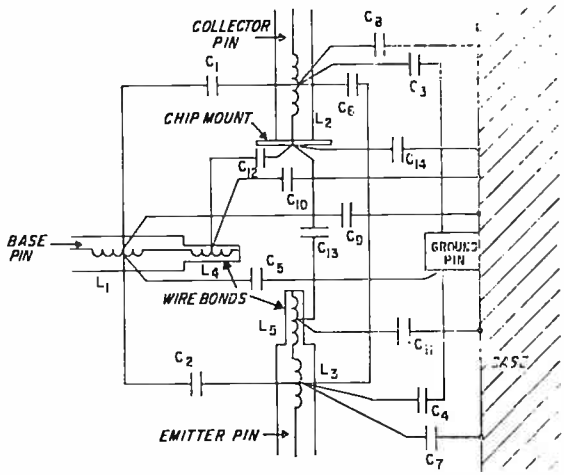

Fig. 4—Circuit diagram of parasitics of configuration shown in Figure 3 (2N2857 in TO-72 package).

Table I—Parasitics Calculated for the TO-72 Case

A. Inductances	Value (nH)
L_1 Base Pin	2.24
L_2 Collector Pin	2.24
L_3 Emitter Pin	2.24
L_4 Base Wire Bond	0.86
L_5 Emitter Wire Bond	0.86
B. Capacitances	**Value (pF)**
C_1 Base Pin to Collector Pin	0.27
C_2 Base Pin to Emitter Pin	0.27
C_3 Collector Pin to Ground Pin	0.27
C_4 Emitter Pin to Ground Pin	0.27
C_5 Base Pin to Ground Pin	0.23
C_6 Emitter Pin to Collector Pin	0.23
C_7 Emitter Pin to Side of Case	0.70
C_8 Collector Pin to Side of Case	0.70
C_9 Base Pin to Side of Case	0.70
C_{10} Base Wire Bond to Top of Case	0.024
C_{11} Emitter Wire Bond to Top of Case	0.024
C_{12} Base Wire Bond to Chip Mount	0.026
C_{13} Emitter Wire Bond to Chip Mount	0.026
C_{14} Chip Mounting Pad to Top of Case	0.009

into more segments and proportioning the capacitances between them. The calculation of these parasitics is shown in the Appendix.

The schematic diagram of the parasitics with the emitter grounded is shown in Figure 5. Here, the emitter is grounded to the case because this is the condition under which the parameters for this device (as given in published data sheet)* were measured.

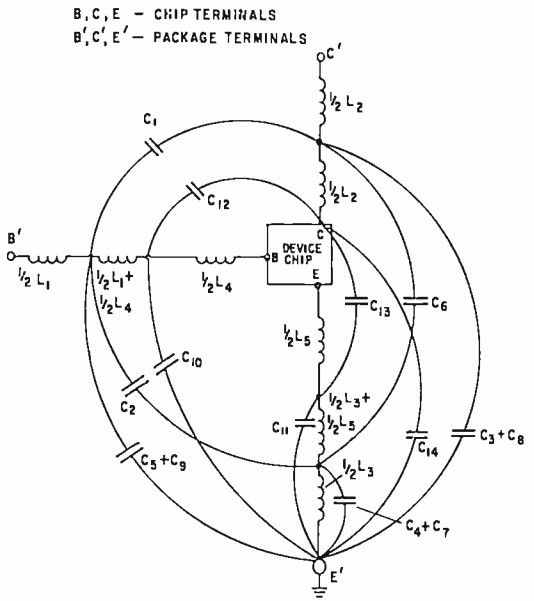

Fig. 5—Circuit diagram of parasitics of Figures 3 and 4 with the emitter grounded to the case.

Before a cancellation network technique can be applied, however, a few modifications to the schematic are necessary. First, the capacitors C_{11} and $C_4 + C_7$ must be eliminated, since there is no way to cancel them by shunting. This is permissible with a negligible loss of accuracy, since C_{11} has a reactance of 675 ohms in parallel with a reactance of 16.7 ohms at 1 GHz, the highest frequency in this analysis. Similarly, $C_4 + C_7$ has a reactance of 160 ohms in parallel with 7 ohms at this frequency.

The other modification that must be made is the elimination of crossovers to make a flat network. Since the inductive reactance of

* File No. 61, (9-66) RCA Semiconductor Products Databook, EC, Harrison, N. J.

$L_3/2$ is small compared to the shunt reactances of the capacitances over the range of calculation, the connections of C_{10} and C_{14} to the emitter terminal may be shifted to the other side of $L_3/2$ without significantly changing the admittance matrix of the model. The resulting network (Figure 6) can now be cancelled by the addition of a negative element network as shown in Figure 7. The use of a negative-

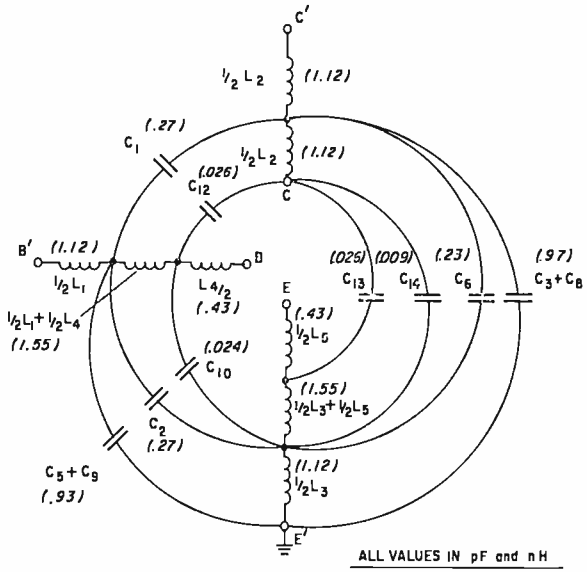

Fig. 6—Revised circuit diagram of Figure 5.

element network allows the correction to be done at any frequency without changing the network. The correction computation was carried out by analyzing the network comprising only the negative elements shown in Figure 7, with the transistor parameters (as measured in the package) inserted between the terminals marked B′, C′, and E′. In this case, the initial y parameter values were taken from the published data sheets for the 2N2857 transistor, measured in a common-emitter configuration biased for a collector current (I_C) of 1.5 mA, and a collector–emitter voltage (V_{CE}) of 6 volts. The computer program will also accept h, hybrid-Pi, or s parameters for the transistor. The computation was carried out using the RCA-601 computer, data being calculated at every 100-MHz interval over the range 100 MHz to 1 GHz. The resulting y parameters of the analyzed circuit and, hence, the chip parameters, are printed out for each frequency. The

original packaged transistor parameters are compared to the computed chip parameters in Table II and Figure 8. The differences in admittance between the packaged device and the chip parameter are reasonable in terms of what one would expect qualitatively after removing the package parasitics.

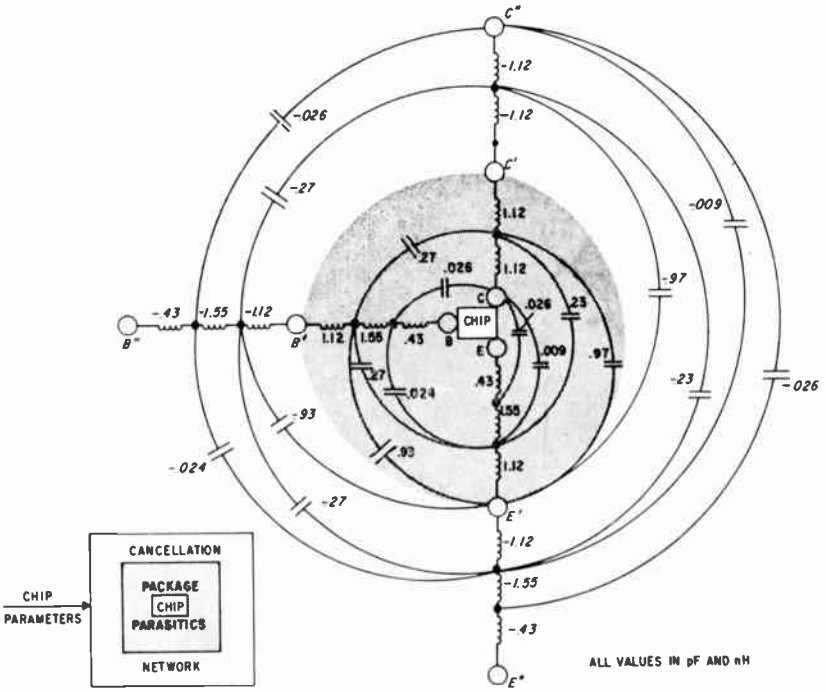

Fig. 7—Cancellation network added to the revised circuit diagram of Figure 6 (2N2857 in TO-72 case).

The following general statements can be deduced from this data. For the chip alone,

(1) y_{11} is reduced, especially at higher frequencies;

(2) y_{21} increases, while b_{21} decreases, but the absolute value of y_{21} is not changed appreciably (the values for $\beta = (y_{21}/y_{11})$ are increased);

(3) the feedback components b_{12} and y_{12} are both reduced;

(4) the output admittance y_{22} is substantially reduced.

The values obtained for the output susceptance b_{22} provide evidence that the computed parasitic capacitance values are reasonable. The values are small and positive, corresponding to the small capaci-

Table II—y Parameters. Columns A Give Values in package, from data sheet; Columns B Give Values for the chip calculated from the model shown in Figure 7. All values are in millimhos.

	y_{11}				y_{12}				y_{21}				y_{22}			
	g_{11}		b_{11}		g_{12}		b_{12}		g_{21}		b_{21}		g_{22}		b_{22}	
Frequency (MHz)	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
100	1.0	0.64	5.0	4.2	0	0	—0.3	—0.1	46	48	—18	—14	0.1	0.1	1.0	0
200	2.5	1.8	7.0	5.6	0	0	—0.9	—0.5	40	46	—27	—20	0.2	0.4	1.8	0
300	6.5	5.2	9.0	8.0	0	0	—1.4	—0.7	32	43	—32	—22	0.3	0.9	2.5	0
400	10.0	7.7	10.5	10.4	0	0	—1.8	—0.8	25	38	—34	—22	0.4	1.0	4.0	0
500	13.5	9.7	12.0	13.1	0	0	—2.3	—1.0	19	35	—36	—22	0.5	1.3	5.5	0.3
600	15.5	10.0	13.5	14.3	—0.2	0	—2.7	—1.0	13	28	—34	—20	0.6	1.4	6.5	0.4
700	18.0	10.3	15.0	15.3	—0.3	0	—3.0	—1.0	8	22	—32	—18	0.8	1.4	8.2	0.7
800	20.0	9.8	17.0	15.6	—0.35	0	—3.3	—1.0	4	16	—29	—16	1.0	1.4	9.5	0.9
900	22.0	8.8	19.0	15.2	—0.4	—0.16	—3.6	—1.0	3	11	—25	—11	1.2	1.4	11.2	1.3
1000	23.0	7.9	21.0	14.0	—0.5	—0.26	—3.8	—1.0	2	7	—20	— 8	1.4	1.3	12.3	1.5

tive output impedance that would be expected for the chip itself. If higher values of parasitic capacitance were assumed, the corrected values of b_{22} would become inductive, an unreal situation. Figure 9 shows the effect on b_{22} of multiplying the calculated parasitic capacitances by various factors.

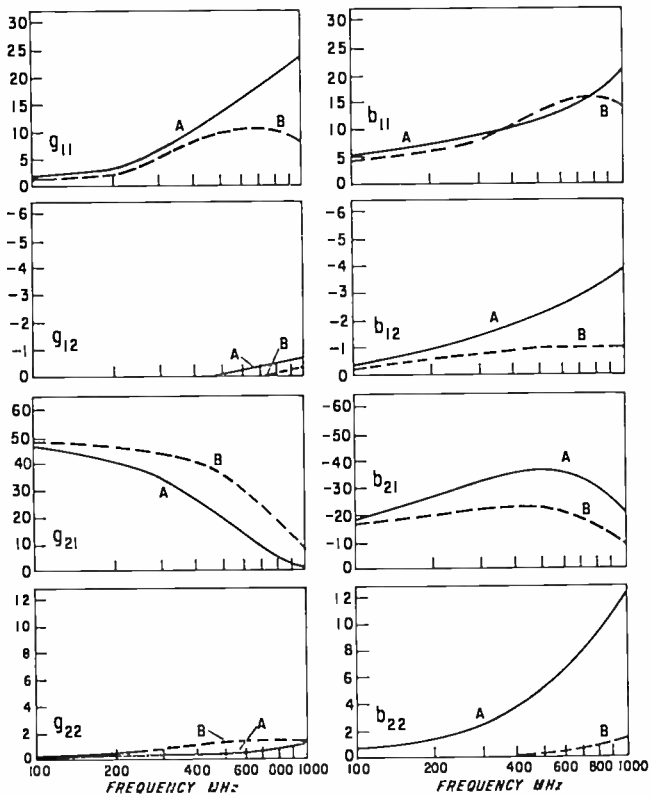

Fig. 8—y parameters of the 2N2857 transistor (in millimhos: curves A show values in packages (from date sheet) and curves B show calculated values for the chip.

Transistor Performance

In order to show the effects of the package on the performance of this transistor, calculations of voltage, current, and power gain are made for the chip and for the packaged chip using the same computer program. A small signal was impressed on the base of the transistor in a common-emitter configuration, with a load resistor from the collector to the emitter. For the calculation of voltage gain, a 1000-ohm

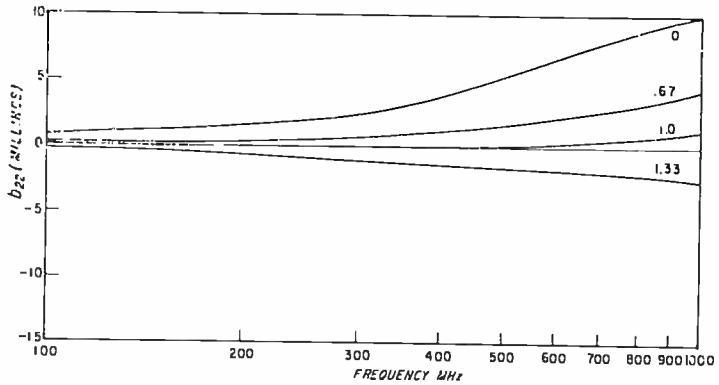

Fig. 9—b_{22} versus frequency. Corrections were computed using capacitances equal to the calculated parasitic capacitances multiplied by the factors shown on the curves.

load was used, 50- and 300-ohm loads were used for power gain, and a 1-ohm load for the current gain. (The program does not accept a short circuit). These calculations were run using both the packaged and unpackaged transistor parameters from Table II. The results, shown in Figures 10 through 13, indicate that the following approximate improvements in performance in the 100–1000 MHz range are obtained as a result of removing the package parasitics:

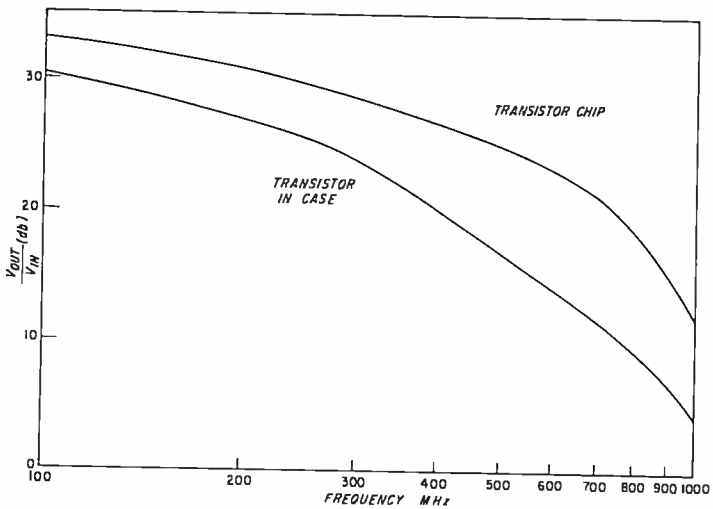

Fig. 10—Voltage gain versus frequency ($R_L = 1000$ ohms).

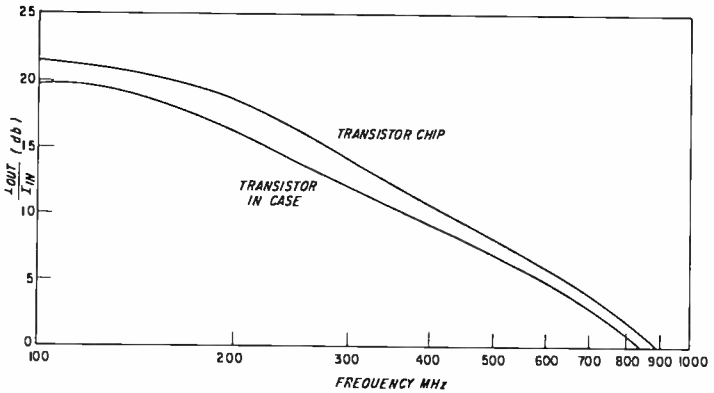

Fig. 11—Current gain versus frequency ($R_L = 1$ ohm).

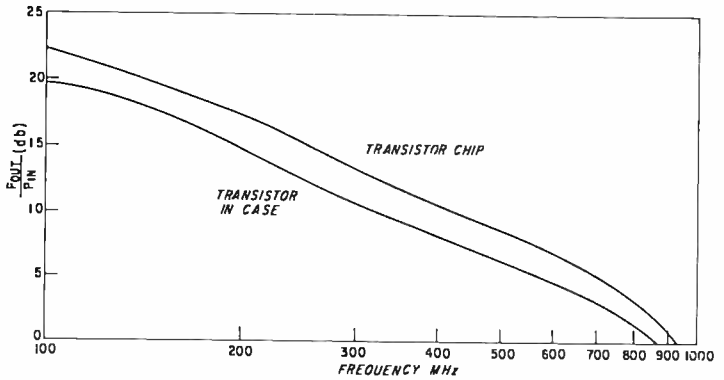

Fig. 12—Power gain versus frequency ($R_L = 50$ ohms).

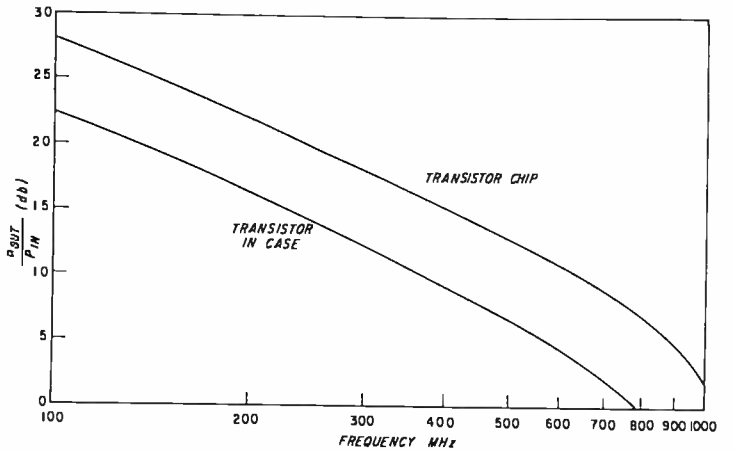

Fig. 13—Power gain versus frequency ($R_L = 300$ ohms).

		Improvement
(a)	voltage gain (1000-ohm load)	3 to 10 dB
(b)	current gain (1-ohm load)	2 dB
(c)	power gain (50-ohm load)	3 dB
(d)	power gain (300-ohm load)	5 to 7 dB

Use of a Corrective Network in Package Design

In Table I, it can be seen that the parasitic capacitances existing between the header feed-throughs and the remainder of the metal package (case) account for about 60% of the total parasitics in the TO-72 package. These high values arise from the close spacing (0.025 inch) from the center of the pins to the case. These parasitic capacitances could be reduced by holding the positions of the pins fixed and increasing the diameter of the case, without having a first-order effect on any of the other parasitics. Calculations of the pin-to-case parasitics from Equation (3) of the Appendix gives the following results:

Pin-to-Case Spacing (Inches)	Capacitance (pF)
0.025	0.70
0.050	0.48
0.100	0.37
∞	0

The expected improvement in the transistor gains (voltage, current, and power) at 500 MHz were computed by adding the parasitic network (Figure 6) to the corrected chip parameters (Table II). The values of C_x and C_y in the parasitic network were changed to reflect the various pin-to-case spacings as shown above.

These results, plotted in Figure 14, show the expected effect of this variation. It appears that an improvement of about 2 dB in voltage gain could be realized at 500 MHz by increasing the pin-to-case spacing to 0.1 inch, while the power and current gains would be affected to a lesser extent. This would mean that the diameter of the can would have to be increased from its present 0.185 inch to 0.335 inch.

This analysis illustrates how the limitations imposed by a proposed package on the performance of a given device may be readily evaluated, and how a suitable package design can be achieved by choosing the right compromises between performance, size, and convenience.

Conclusions

A procedure for obtaining the electrical parameters for a transistor chip itself, given the parameters measured on the chip in a package, has been described. As an example, the parameters for the 2N2857 transistor are calculated. The method can also be applied to integrated

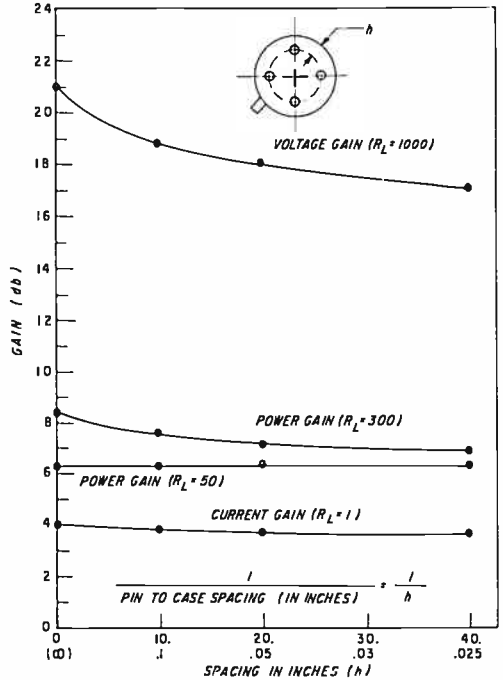

Fig. 14—Gain versus pin-to-case spacing at 500 MHz.

or hydrid circuits if the overall admittance matrix of the circuit in the package is known.

If a compilation of parasitic cancellation networks were available for each package in commercial use, then, given a set of parameters measured on a packaged device, the chip parameters could be readily computed for any desired frequency range. It is believed that the following advantages might be realized by this procedure.

a) It could serve as an aid in the selection of transistor chips for direct bonding to a circuit board.

b) It would enable a circuit designer to use more realistic values

in designing circuits incorporating such directly bonded transistor chips.

c) It could assist in package design and selection. Once the chip parameters are computed, the effects of other packages or package modifications on the performance of the device can readily be computed by adding the appropriate parasitics for the proposed package.

Appendix—Calculation of the Parasitic Elements

A. Parasitic Inductances

The magnitude of the series inductances of the pins and bond wires were calculated from the equation for the self inductance of a straight wire[7]

$$L = 0.002\, l \left[\ln \frac{2l}{r} - \frac{3}{4} \right] \tag{1}$$

where l is the length of the wire in centimeters and r is the radius of the wire in centimeters.

For the pins, $l = 0.4$ cm and $r = 0.023$ cm; thus, $L_{\text{pin}} = 2.24$ nH.

For the bonding wires, $l = 0.1$ cm and $r = 0.0013$ cm; thus $L_{\text{bonding wires}} = 0.86$ nH

B. Pin-to-Case Capacitances

The lead pins are embedded for about 2 mm in a glass having a relative dielectric constant (ϵ_r) of about 4.5. An additional 1 mm of the pin projects above the glass. For the purpose of this calculation, the equivalent length l_{eff} of a pin completely embedded in a medium of $\epsilon_r = 4.5$ was computed to be 2.2 mm or 2.2×10^{-3} m:

$$\frac{l_1\epsilon_1 + l_2\epsilon_2}{\epsilon_1} = l_{\text{eff}} \tag{2}$$

The metal case was assumed to be an infinite plane, and the capacitance between the pin and the case was calculated using the

[7] F. W. Grover, *Inductance Calculations, Working Formulas, and Tables*, p. 35, Dover Publications, N. Y., 1946.

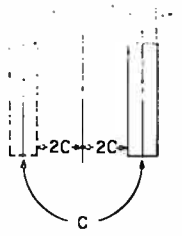

Fig. 15

method of images and applying the following equation[8] to the configuration shown in Figure 15 to find the capacitance between two finite segments of wire:

$$C = \frac{\pi\epsilon l}{\ln\left(\frac{h}{r} + \sqrt{\frac{h^2}{r^2} - 1}\right)} \quad \text{(mks)} \qquad (3)$$

When

$$l = l_{\text{eff}} = 2.2 \times 10^{-3}\ \text{m}$$
$$h = 0.635 \times 10^{-3}\ \text{m}$$
$$r = 0.23 \times 10^{-3}\ \text{m},$$

the resulting pin-to-case capacitance ($2C$) is 0.70 pF.

C. *Pin-to-Pin Capacitances*

A top view of the pin arrangement in the TO-72 case is shown below. Six pin-to-pin capacitances exist among the four pins, which are

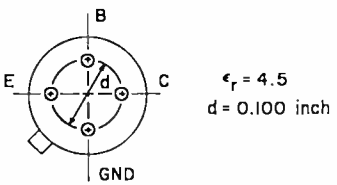

Fig. 16

[8] E. C. Jordon, *Electromagnetic Waves and Radiating Systems*, p. 56, Prentice Hall, 1950, Englewood Cliffs, N.J.

spaced either 0.071 or 0.100 inch apart. They were also calculated using Equation 3 and the values

$$l = l_{\text{eff}} = 2.2 \times 10^{-3} \text{ m}$$
$$r = 0.23 \times 10^{-3} \text{ m}$$

For the 0.100-inch separations ($h = 1.27 \times 10^{-3}$ m), the parasitic capacitance is 0.23 pF; for the 0.071-inch separations ($h = 0.9 \times 10^{-3}$ m), the capacitance is 0.27 pF.

D. Bonding-Wire-to-Case Capacitances

The base and emitter bonding wires, about 1 mm long, run in approximately a horizontal plane parallel to the top of the transistor case and at a distance of about 1.5 mm from the case. The capacitances these represented were calculated to be 0.024 pF, again using Equation (3) and the method of images with the values

$$h = 1.5 \times 10^{-3} \text{ m}$$
$$r = .0217 \times 10^{-3} \text{ m}$$
$$l = 10^{-3} \text{ m}$$
$$\epsilon_r = 1$$

E. Bonding-Wire-to-Collector-Pad Capacitances

A capacitance also exists between the bonding wires and the metal pad on which the transistor is mounted. The calculation of Section D, above, was repeated, using a value of $h = 0.7 \times 10^{-3}$ m or the estimated average spacing between the bonding wire and the collector mounting pad. The capacitance calculated is 0.026 pF.

F. Collector-Pad-to-Case Capacitance

The collector mounting pad, which is 0.100 × 0.030 inch, forms a parallel-plate capacitance with the top of the transistor case. Using the parallel-plate capacitor equation,

$$C = \frac{\epsilon_0 \epsilon_r A}{d} \text{ (mks)}$$

where $A = 1.94 \times 10^{-6}$ m^2, $d = 2 \times 10^{-3}$ m, and $\epsilon_r = 1$, the capacitance is 0.009 pF.

Acknowledgments

The author gratefully acknowledges the cooperation of D. Ressler in providing and implementing the computer program used in this work, the helpful discussions with L. Napoli, and the support and critical review of the manuscript provided by N. E. Wolff and J. A. Amick.

CONTROLLED OXIDATION OF SILANE

By

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Summary—*The study of SiH_4–oxidant systems was undertaken to gain insight into reaction mechanisms that could cause the formation of SiO_2 in the gas phase or on the reactor wall, rather than on the surface of the silicon wafers to be coated.*

A gas reactor system was designed and built to determine the relative stabilities of various SiH_4–oxidant combinations and to monitor the oxidation of SiH_4 to SiO_2 by observing the change in absorption of the 925 cm^{-1} peak of the SiH_4 spectrum. Stability, as defined by the initiation temperatures for the oxidation reaction, indicated that at silane concentration of 0.8% or less, N_2O–SiH_4–N_2 mixtures begin to react from 370 to 525°C and O_2–SiH_4–N_2 between 140 to 270°C. CO_2–SiH_4–N_2 was stable to 520°C.

All of the above oxidant–SiH_4–N_2 combinations could be premixed at room temperature without reacting. In order to obtain kinetic data, the decay of SiH_4 concentration as a function of temperature was obtained by determining the relationship between infrared transmittance and SiH_4 concentration. From these data the apparent activation energies for the SiH_4–O_2 and SiH_4–N_2O reactions were found to be 8 kcal and 32 kcal, respectively. Analysis of reaction products between 240 and 450°C indicated that hydrogen rather than water vapor was formed. The most probable reaction equation is $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$.

Introduction

VAPOR deposition of SiO_2 films by the thermal oxidation of SiH_4 is widely used in the manufacture of solid-state devices and integrated circuits. It is used, for example, to deposit protective layers and electrical insulation,[1] as a means of adjusting capacitance, and as a diffusion source of dopants.[2,3] The normal deposition temperature is 250 to 475°C.[4]

[1] A. Mayer, et al, "Surface Passivation Techniques for Compound Solid-State Devices," Air Force Contract F33(657)-11615, Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio.

[2] A. W. Fisher, J. A. Amick, H. Hyman, and J. H. Scott, Jr., "Diffusion Characteristics and Applications of Doped Silicon Dioxide Layers Deposited from Silane (SiH_4)," *RCA Review*, Vol. 29, p. 533, Dec. 1968.

[3] J. A. Amick, and A. W. Fisher, "Isolation Techniques for Fabricating Integrated Circuits—I. Laminate Substrates," *RCA Review*, Vol. 29, p. 475, Dec. 1968.

[4] N. Goldsmith and W. Kern, "Deposition of Vitreous Silicon-Dioxide Films from Silane," *RCA Review*, Vol. 29, p. 153, March 1967.

A characteristic of the process is that the rate of SiO_2 deposition is quite sensitive to changes in the SiH_4 concentration and changes in the feed stream flow patterns within the reactor. This sensitivity is reflected in significant changes in the deposition rate.

In practice, the SiH_4 oxidation reaction has been observed to occur in the gas phase and on all heated surfaces with the reactor. Depending on reactor design and flow conditions, a variable amount of SiH_4 can be stripped from the feed stream and deposited on reactor walls. For this reason, operating conditions are adjusted so that SiH_4 concentration is as dilute as possible consistent with a reasonable deposition rate (600 to 1500 Å per minute).

To incorporate controlled amounts of boric or phosphoric oxide in the deposit by the simultaneous oxidation of PH_3 or B_2H_6 with SiH_4, an insight into the oxidation mechanism is desirable. Close control of the doping process is made difficult by differences in the stability of the hydrides in oxygen. This can result in differences in the composition of the deposited layer depending upon the geometry of the reactor and the initiation temperature of the dopant species.

One method of obtaining better control over the SiH_4–SiO_2 deposition process would be to obtain a SiH_4–oxidant combination that would permit the temperature at which the reaction is initiated to be increased. This temperature is determined by the reaction kinetics rather than by the free energy of reaction, because the free energy of formation of SiO_2 is so high, relative to practical oxidants, that the reaction should go to completion at room temperature. Thus, in the practical systems examined, which consist of SiH_4 reacting with O_2, N_2O, or CO_2, the free energy of reaction ranges from 190 to 94 kcals/mole.[5] The pronounced differences in initiation temperatures observed here as a function of specific reactants and their concentration levels indicate that the kinetics were affected perhaps by a change from a reaction-controlled mode to a diffusion-controlled mode. Similar considerations may then be applied to oxidation of PH_3 and B_2H_6. An examination of the reaction of SiH_4 with O_2, N_2O, and CO_2 was made and is described here.

Apparatus

A method of monitoring the SiH_4 concentration as a function of time and temperature was developed. A Beckman IR8 Spectrophoto-

[5] C. E. Wicks and F. E. Block, *Thermodynamic Properties of Elements, Their Oxides, Halides, Carbides, and Nitrides*, Bulletin 605, Bureau of Mines.

meter was used to determine the infrared spectrum of SiH_4 (Figure 1). The spectrum indicated useable peaks in the 2200 cm^{-1} and 900 cm^{-1} regions. The absorption spectra for some of the oxidants (N_2O, CO_2, etc.) and reaction products were found to be limited to the 2200 cm^{-1} region, while the 900 cm^{-1} region was occupied only by the SiH_4 lines. The optics of the spectrophotometer, therefore, were aligned on the 925 cm^{-1} absorption peak, and the variation in peak height as

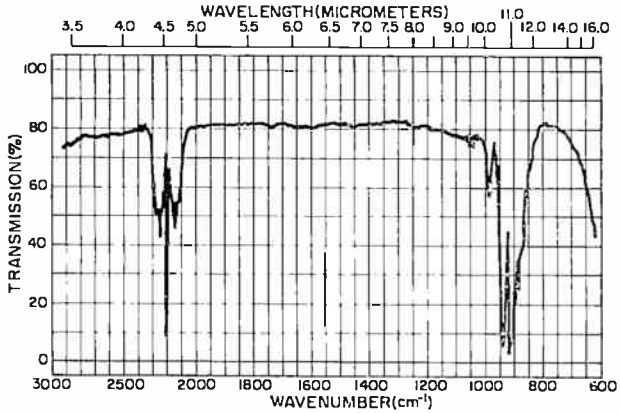


Fig. 1—Infrared spectrum of SiH_4.

percent transmission through a 10-cm gas cell was monitored. An expanded profile of this part of the infrared spectrum is shown in Figure 2.

The monitoring equipment was part of a simplified gas reactor system (Figure 3) consisting of

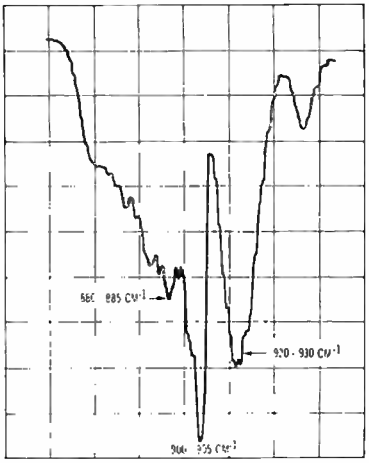
(1) flow controls for SiH_4, oxidant, and nitrogen;

(2) the gas reactor, filled with quartz chips, in a resistance-wound furnace;

(3) a 10-cm gas cell mounted in a Beckman IR8 Spectrophotometer;

(4) a dual-channel strip-chart recorder.

The combined gases were piped into the reactor and were exhausted through the 10-cm gas cell. The dc output of the spectrophotometer at 925 cm^{-1} and the dc output of the chromel–alumel thermocouple inserted in a quartz tube within the reactor were recorded on a dual-channel strip-chart recorder. Thus, SiH_4 concentration was monitored as a function of temperature and time.



PARTIAL SiH_4 SPECTRUM

Fig. 2—Partial SiH_4 spectrum.

Reaction Temperatures

The test procedure was to adjust the SiH_4 and N_2 gas streams to the required concentration within the reactor at room temperature. The 925 cm^{-1} absorption peak was used to establish a base line on a strip-chart recorder for SiH_4 in N_2 at room temperature. Oxidant was

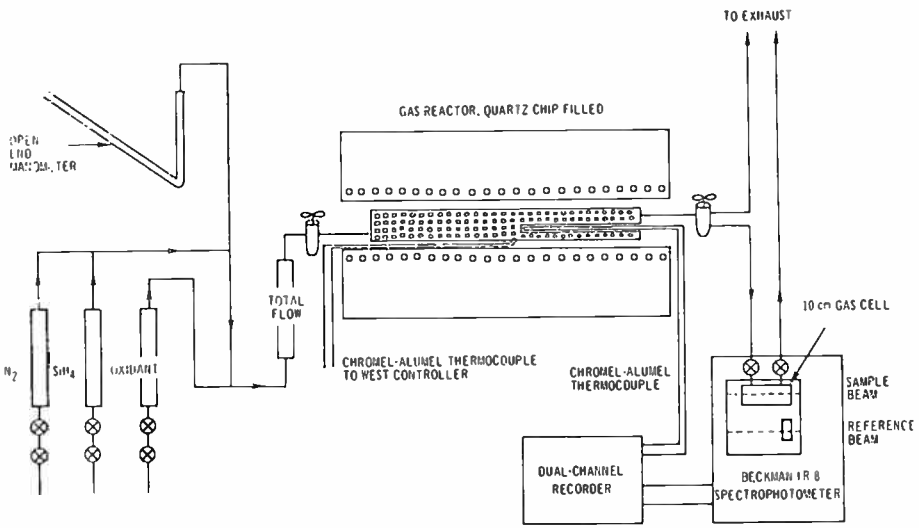


Fig. 3—Gas reactor system for SiH_4-oxidant reaction.

then added. If no change occurred, the furnace was turned on and concentration and temperature rise were monitored as a function of time. The concentration range examined for most of the tests was 0.2 to 0.8% SiH_4 and an oxidant/SiH_4 ratio between approximately 2 and 20.

Test results indicated that at room temperature no reaction takes place between SiH_4 (0.2-0.8%) and O_2, N_2O, or CO_2. Table I gives the reaction initiation temperatures observed for the 0.2-0.4% SiH_4 range.

Table I—Reaction Initiation Temperatures

Mixture	Reaction Initiation Temperature (°C)	Conditions
$SiH_4 + O_2 + N_2$	140—270	0.2-0.4 SiH_4, Oxidant/SiH_4 = 2-20 at 0.4% SiH_4
$SiH_4 + N_2O + N_2$	370—540	0.2-0.4 SiH_4, Oxidant/SiH_4 = 2-20 at 0.4% SiH_4
$SiH_4 + CO_2 + N_2$	520	0.2% SiH_4, Oxidant/SiH_4 = 5

Thus, contrary to prediction, SiH_4–O_2–N_2, SiH_4–N_2O–N_2, and SiH_4–CO_2–N_2 mixtures are stable up to at least 0.8% SiH_4 at room temperature. This was found to be the case whether the gases were transported in Pyrex, copper, or stainless-steel lines.

Measurement of Silane Concentration

To examine the kinetics of the oxidation of SiH_4 for different SiH_4–oxidant combinations, it was necessary to determine the relationship between infrared transmittance and SiH_4 concentration. Mass-spectrometer analysis of SiH_4 samples were taken over a concentration range of from 0.05 to 0.75%, which corresponds to a transmittance range of from 80 to 15% in the 10-cm cell. These data, plotted in Figure 4, indicate that the relationship between the SiH_4 concentration and log $1/T$ generally approximates the prediction of linearity from Beer's Law:

$$\log \frac{I_o}{I} = \log \frac{1}{T} = K \cdot C_{SiH_4}$$

where I_o = intensity of incident beam
I = intensity of emerging beam
T = transmittance
K = constant (absorptivity, cell length)
C_{SiH_4} = molar concentration of SiH_4

Reaction Kenetics

A thermal arrest technique (temperature and concentration held constant) was used to obtain each datum point, and the reaction of SiH_4 with O_2 and N_2O were compared. The decay of a 0.4% SiH_4 concentration at an oxidant/SiH_4 ratio of 7 was monitored. The data, shown in Figure 5, are consistent with previous data in that the initiation temperature for the SiH_4–N_2O reaction is significantly higher than for the SiH_4–O_2 reaction.

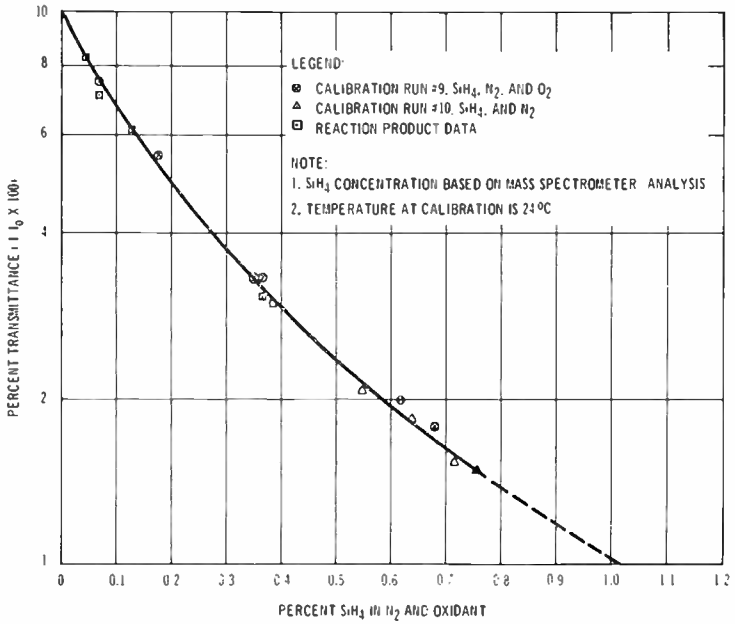


Fig. 4—SiH_4 concentration versus infrared transmittance of the 920 to 930 cm^{-1} (10.8 μm) peak.

With a calibration curve (IR transmittance versus SiH_4 concentration), the transmittance data was converted to percent SiH_4 reacted as a function of gas temperature. This curve is shown in Figure 6.

The concentration versus temperature curves shown in Figure 6 are not linear, however, and can not be accurately extrapolated to the initial reaction temperature. Since it is difficult to quantitatively compare the two oxidation reactions, a theoretical basis for determining an "apparent activation energy" was considered.

The reaction is bimolecular and would normally be described by a second-order kinetic expression. However, since the oxidant con-

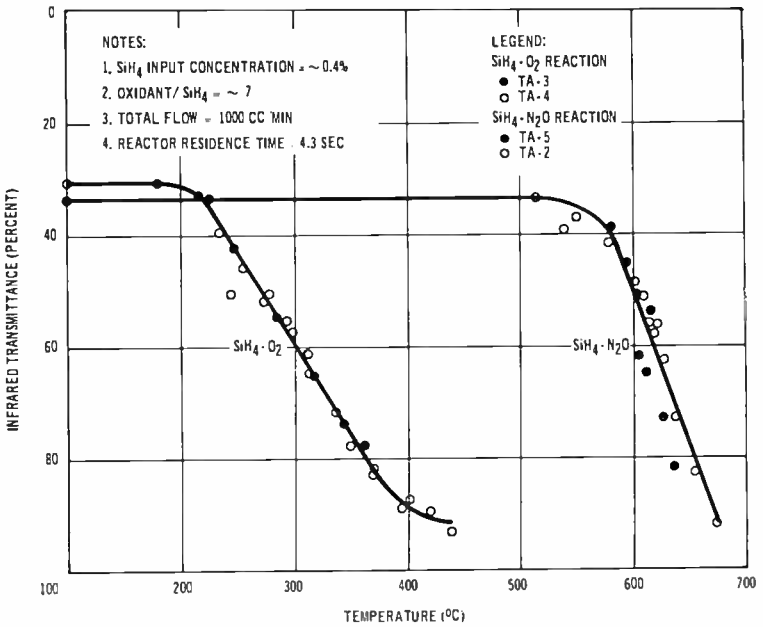


Fig. 5—Infrared monitoring of oxidation of SiH_4.

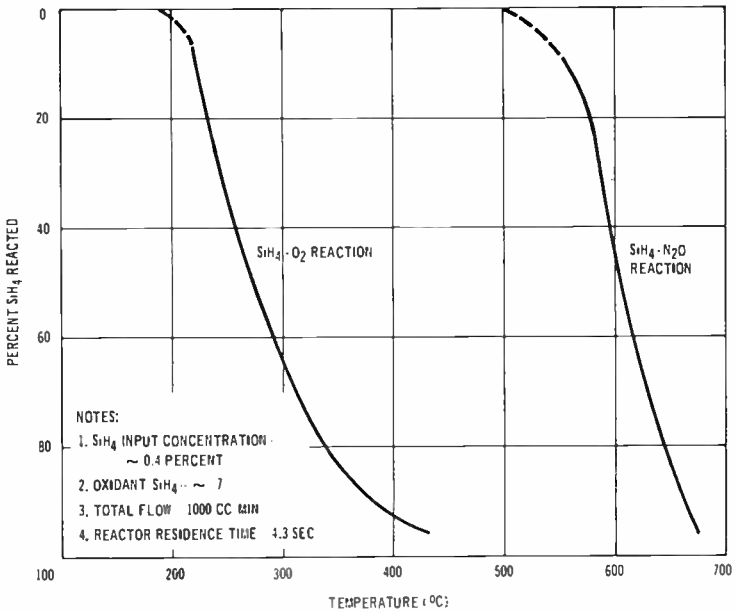


Fig. 6—Reaction of SiH_4 with O_2 and N_2O.

centration is high relative to the amount that reacts, the reaction rate would appear to be predominantly a function of SiH_4 concentration rather than both SiH_4 and oxidant concentrations. Therefore, a unimolecular reaction might describe the reaction kinetics better than a bimolecular reaction.

In the tests plotted in Figure 5, a uniform gas-temperature profile was obtained within the reactor by holding the total gas-flow rate constant (1000 cm^3/min) for all tests. This resulted in a calculated reaction or residence time of 4.3 seconds. However, since kinetic data are usually obtained by monitoring a concentration change as a function of time rather than temperature, an unconventional manipulation of the kinetic expressions was required.

For a first-order reaction, the relationships between concentration, time, and temperature[6] are:

$$-\frac{dC_{SiH_4}}{dt} = kC_{SiH_4} \tag{1}$$

$$k = k_o \exp\left\{-\frac{\Delta E_A}{RT}\right\} \tag{2}$$

By integrating and combining these equations, an expression is derived that relates a change in reactant concentration and gas temperature to an activation energy:

$$\ln\left(t^{-1} \ln \frac{C_o}{C}\right) = \frac{-\Delta E_A}{RT} + \ln k_o \tag{3}$$

where C_o = input concentration,
C = exhaust concentration,
t = reaction time,
E_A = apparent activation energy,
T = gas temperature,
k = absolute reaction rate,
k_o = frequency factor.

From the data in Figure 6, where between 20 and 80% SiH_4 reacted, the reaction rate of $\ln(t^{-1} \ln C_o/C)$ was calculated and plotted against

[6] A. A. Forst and R. G. Pearson, *Kinetics and Mechanism*, 2nd ed., John Wiley and Sons, Inc., New York (1961).

reciprocal temperature. The resulting curves, Figures 7 and 8, are straight-line functions, indicating that the oxidation of SiH_4 at the stated concentration levels can be considered a monomolecular reaction. The apparent activation energies calculated from the slopes of these curves are

SiH_4–O_2 reaction = 8 kcal
SiH_4–N_2O reaction = 32 kcal

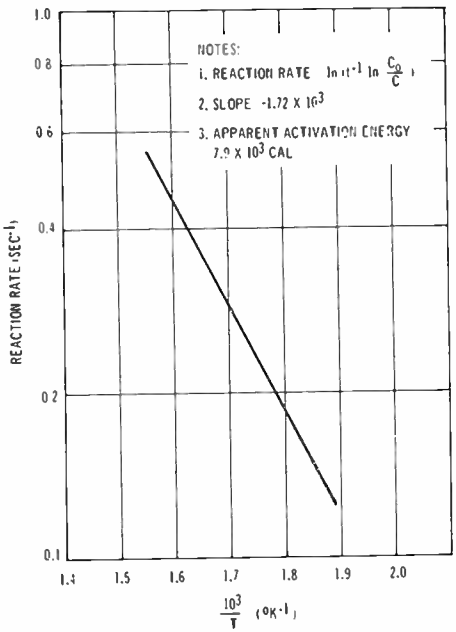


Fig. 7—Temperature dependence of the SiH_4–O_2 reaction.

This indicates that the SiH_4–N_2O combination is considerably more stable than the SiH_4–O_2 mixture.

To determine the range of conditions over which the apparent activation energies were applicable, the effect of varying oxidant/SiH_4 ratio was investigated. To date only preliminary results have been obtained. However, these data indicate that O_2 has an anomalous effect on the oxidation of SiH_4 (see Table II). Contrary to expectation, increased oxygen seems to increase the stability of the SiH_4–N_2–O_2 mixture. Conversely, the stability of SiH_4–N_2–N_2O mixtures is not affected by increased N_2O.

Table II—Initiation Temperatures for Oxidant-SiH_4 Ratios

Oxidant/SiH_4 (Calculated volume ratio based on flow-meter settings)	Initiation Temperature (°C)	
	O_2	N_2O
2	139	540
5	197	525
20	257-270	532

In this series of tests, the input SiH_4 concentration was held at 0.4%. The oxidant concentration in all cases was above the stoichiometric concentration. It is most likely that the oxidant was thoroughly mixed with the SiH_4–N_2 mixture before entering the reactor. Since total flow was held constant (1000 cm^3/min), no change in reaction temperature was anticipated.

Reaction Products

Further information on the SiH_4 oxidation mechanism was obtained from a materials balance of a partially completed SiH_4–O_2 reac-

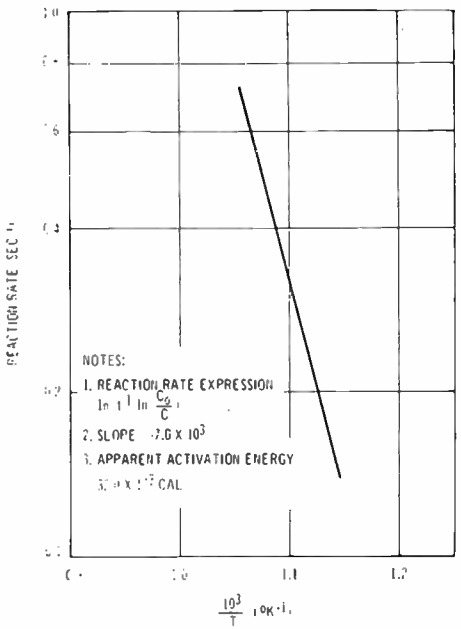


Fig. 8—Temperature dependence of the SiH_4-N_2O reaction.

tion. A typical mass spectrographic analysis of a SiH_4–O_2–N_2 mixture before and after reaction is shown in Table III. Analysis of gas mixtures from SiH_4–O_2 reactions up to 450°C similarly indicate that the only gaseous product formed is H_2.

These test results indicate that the best overall equation that would describe the SiH_4–O_2 reaction at 240-450°C for the dilutions employed is

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

The analytical data for H_2 in the exhaust stream and H_2 calculated from the SiH_4 reaction are in reasonable agreement. On this basis, the absence of H_2O from the exhaust stream can be explained.

Table III—Material Balance (% Concentration by Volume)
Reaction Temperature—241°C

Gases	Reactor Input	Reactor Exhaust	Reacted	Calculated H_2, Based on SiH_4 Reacted
SiH_4	0.365	0.124	0.241	—
O_2	0.80 est.	0.575	0.225	—
H_2	—	0.492	—	0.482
H_2O	—	—	—	—

Conclusions

The room-temperature stability of SiH_4–N_2–O_2 mixtures up to 0.8% SiH_4 indicates that these gases can be premixed well before the deposition reactor. As a result, flow controls at the reactor could be greatly simplified. The use of a single feed stream into a deposition reactor could also simplify the gas-flow pattern within a reactor. This could result in more reproducible deposition results. Further, the sensitivity to leaks in SiH_4 delivery lines would be reduced by transporting a stable gas mixture from a gas storage area to the reactor.

This study also indicates that N_2O can be used as an oxidant for SiH_4. Mixtures of SiH_4–N_2–N_2O are considerably more stable and less temperature sensitive than SiH_4–N_2–O_2 mixtures. Thus, the use of N_2O as an oxidant in combination with improved reactor design could lead to a process in which SiO_2 deposition is essentially confined to wafer surfaces, and phosphorus and boron dopant levels are still accurate and reproducibly controlled.

Another factor of some significance in the study of the SiH_4–O_2 reaction is that H_2 rather than H_2O vapor is formed.

ACKNOWLEDGMENTS

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The author wishes to thank William Stever and Robert Vibronek for helping to construct the reactor system and to obtain the experimental data. David Puotinen was most helpful in aiding the author to formulate a kinetic model for the reaction, and Alfred Mayer gave many valuable suggestions on experimental procedure.

DEVELOPMENT OF P-CHANNEL ENHANCEMENT MOS TRIODES

By

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Summary—A p-n channel MOS triode was designed and fabricated by use of a doped-stepped-oxide technique. The diffusion of p-type impurities from the oxide extends the drain electrode that defines a narrow channel length not easily accomplished with normal photoresist techniques. The resultant device has a feedback capacitance of 0.2 picofarad, and retains the advantages of a full-gate structure.

Introduction

In MOST charge-controlled devices, the voltage gain or amplification factor is defined as the ratio μ_a of the input capacitance C_{in} to the internal feedback capacitance C_{fb};

$$\mu_a = \frac{C_{in}}{C_{fb}}.$$

The development of techniques for reducing feedback capacitance received primary emphasis in development of a p-channel MOS triode for linear applications. The design variables that were evaluated included increased gate-to-drain distance by use of increased oxide thickness, abrupt source and drain junctions, minimum metal gate-to-drain overlap, and substrate doping effects. This paper compares the p-channel enhancement MOS device with a conventional structure (see Figures 1(a) and (b), respectively) and reviews some experimental results that were obtained from the new model.

Experimental Approach

The development of a p-channel enhancement MOS device required the proper choice of substrate material. As a result, silicon having a resistivity range of 12 to 18 ohm-centimeters and cut along the (100) plane was selected. This choice permits maximum drain-to-source voltage (V_{DS}) and minimum threshold voltages (V_{TH}) consistent with

the use of clean oxide technology. Moreover, the selected resistivity range facilitates the control of p-type concentration during the solid-to-solid diffusion. The source–drain diffusion is achieved with p+ regions formed at 1150°C from an oxidized boron nitride source that yields V_{DS} ratings of −60 volts, as shown in Figure 2.

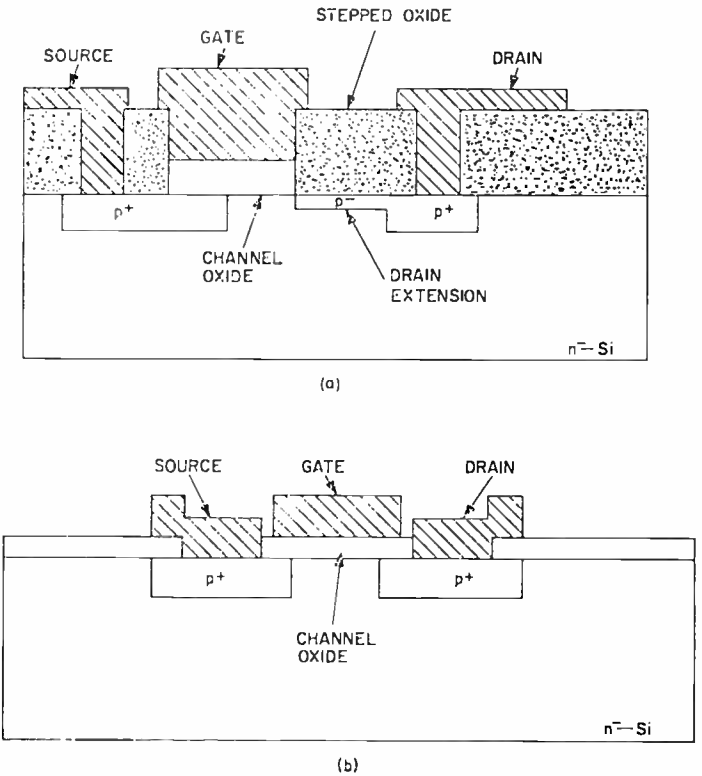

Fig. 1—P-Channel enhancement MOS device (top) and conventional structure (bottom). Note the increased distance between the gate drain and electrodes accomplished by the stepped oxide of the developed p-MOS leading toward a marked decrease in feedback capacitance.

Deposition of oxide is performed at 400°C by use of the familiar hooded hot-plate rotated-disk apparatus. Diborane is introduced into the gas stream with the silane to produce a doped oxide approximately 2000 Å thick. Additional SiO_2 is deposited in a separate, clean, undoped gas system to produce the desired stepped oxide, as shown in Figures 3(a) and (b). This removal from one system to the other is a prerequisite to consistent photoresist results. Figure 3(a) is a photo-

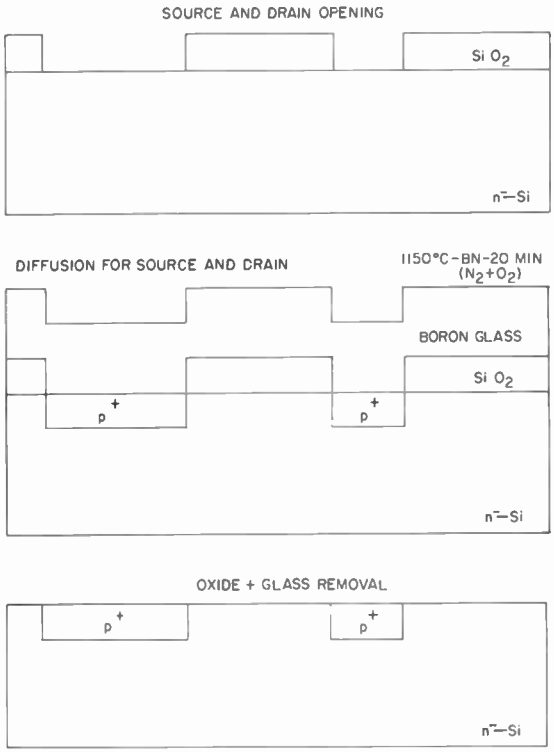

Fig. 2—Processing steps required for isolation of drain and source regions.

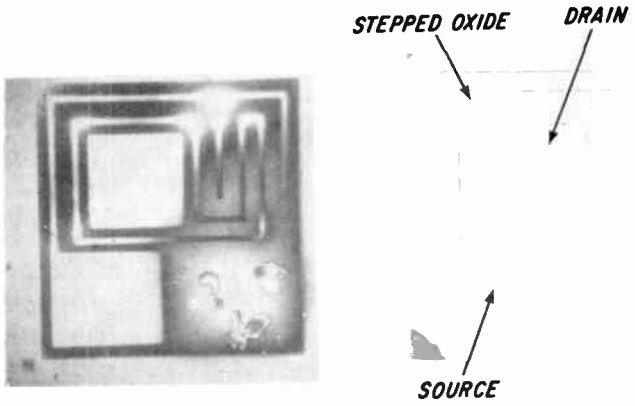

Fig. 3—Photomicrographs of stepped oxides: Left, uncontrolled boron-doped SiO_2 (subsequent undercutting), and, right, with a 5000 Å cap of undoped SiO_2 over the doped oxide (subsequently well defined).

micrograph of drastic photoresist lifting that resulted when an attempt was made to exhaust all the diborane in the system prior to deposition of the pure SiO_2 cap. From this work, it was determined that rapid dissolution of the glassy layer is a prime factor in the control of channel length.

Silane densification proved to be the most critical factor in this development. Earlier attempts to diffuse boron from the oxide in a 950°C nitrogen furnace resulted in almost complete degradation of the existing p-n junction. During this procedure, densification produced strains along the surface of the silicon, as shown in Figure 4. Cracks

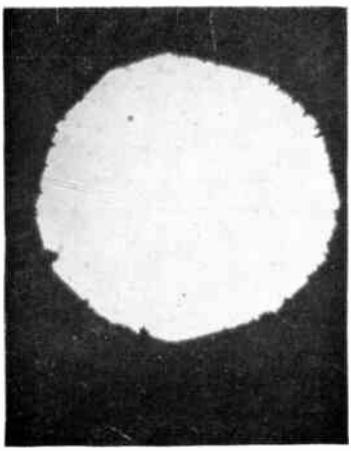

Fig. 4—Boron microstrains on a silicon surface as the result of diffusing into silicon of the boron-doped oxide in the presence of oxygen without a buffered SiO_2 layer.

that failed to follow a crystal lattice orientation occurred only in the presence of oxygen. Apparently, in an oxygen atmosphere, the boron outdiffuses or segregates into the region of the silicon dissolved by the diffusing oxygen. During cooling, the boron redistributes along the propagated cracks formed by the mismatch between the glassy layer and silicon. This effect produces extended accumulation regions that join the source and drain and cause degradation of the p-n junction. To avoid this problem, densification is performed at a lower temperature (800°C) in the presence of oxygen. In this method, the buffered zone of SiO_2 (100 to 150 Å), as shown in Figure 5(c), is thermally grown at the doped oxide p-n junction interface. With subsequent drive in at 950°C, the drain region is extended, as shown in Figure 6, with no junction degradation. Subsequent analysis of the

sample indicates a concentration level on a 12-18 ohm-cm control chip at 2000 ohms per square.

In previous attempts to fabricate the device, the boron diffusion was delineated with a 10% HF solution. This procedure was performed for ease in alignment during definition of the stepped-oxide

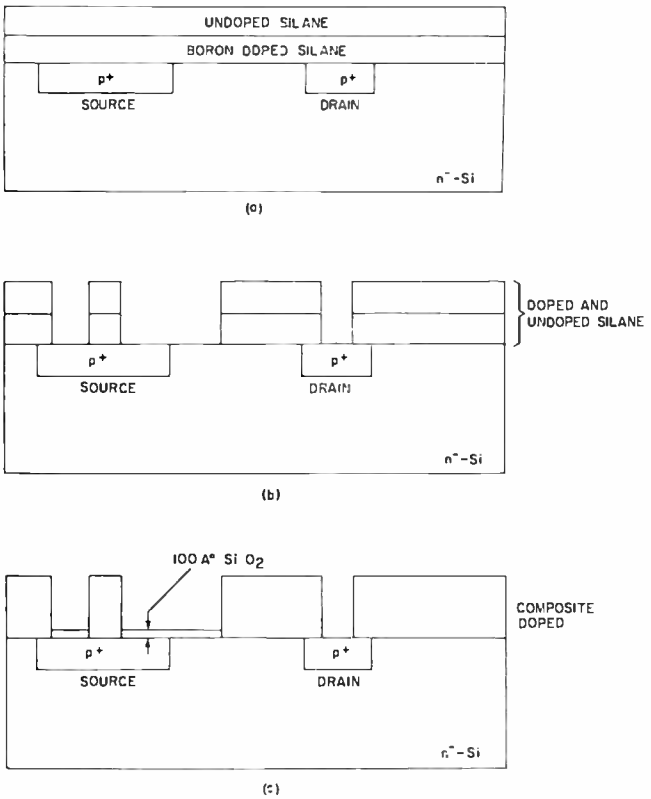

Fig. 5—Processing steps defining the doped stepped-oxide regions and the buffered SiO_2 layer.

regions. Thus, during the subsequent solid-to-solid diffusion, blistering of the silane occurred only in the stained area shown in Figure 7.

The subsequent processing steps, shown in Figures 6(a), 6(c), and 1(b), were performed under "clean" conditions. MOS devices exhibiting maximum stability and the lowest threshold voltages were achieved. Subsequently, the process cleanliness was verified from curves of capacitance as a function of voltage.

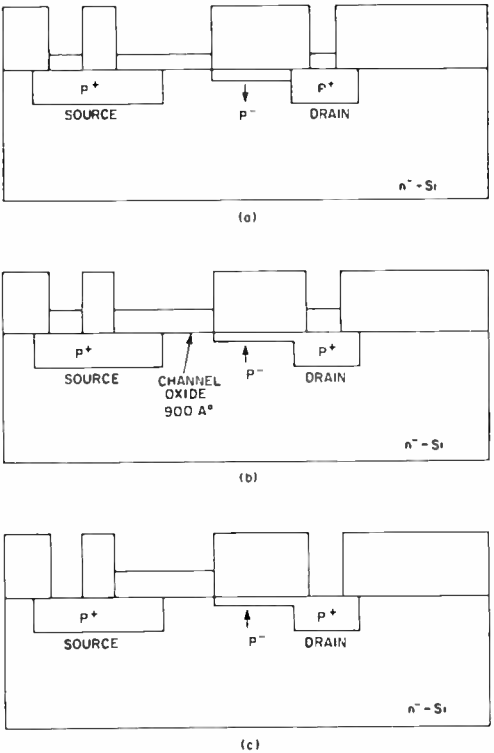

Fig. 6—Processing steps required to (a) introduce the drain extension, (b) to form the channel oxide, and (c) to define the contact regions.

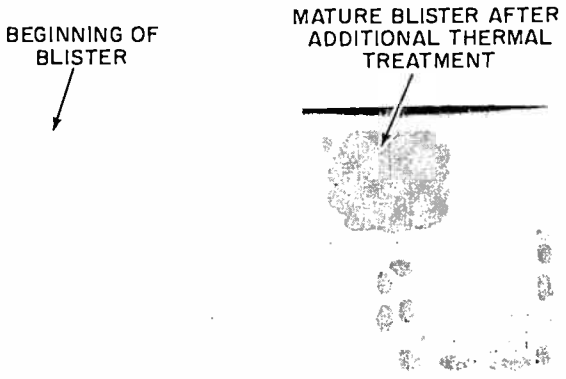

Fig. 7—Photomicrographs showing (left) beginning of blister as a result of the eruption of impurities from boro-silicate glass source underlying the oxide and (right) mature blister after thermal treatment (950°C in N_2).

Table I

Parameters	Value Range	Test Conditions
I_{gss}	0.0 − 100 pA	$V_{gs} = +20$ V
$I_{D\ (off)}$	0.01 − 1 nA	$V_{DS} = -15$ V, $V_{gs} = 0$ V
$I_{D\ (on)}$	32-40 mA	$V_{DS} = -15$ V, $V_{gs} = -15$ V
R_{ds}	200-250 ohms	$V_{DS} = 0.1$ V, $V_{gs} = -15$ V
g_{fs}	3800-4200 μmho	$V_{DS} = -15$ V, $I_D = 7.5$ mA
g_{fs}	4300-4600 μmho	$V_{DS} = -15$ V, $I_D = 15$ mA
$-V_{TH}$	2.2 − 2.5 V	$I_D = 10$ μA
$-V_{DS}$	35 − 40 V	$I_D = 10$ μA

Performance

The electrical results for the stepped-oxide device are shown in Table I. The range of these results is similar to those of a conventional n-channel structure.

Figure 8 shows the dramatic difference in feedback capacitance at various voltage levels. Measurements were taken on a direct capacitance bridge at 1 MHz. A comparison of the change in feedback capacitance with voltage, shown in Figure 9, revealed a more abrupt drop with the stepped-oxide device than with the conventional structure. This drop is produced by widening of the depletion layer, because the drain extension is a more linearly graded junction than the more heavily concentrated p+ drain region of a conventional MOS device. When more heavily doped substrate material is examined, however, fringing or parallel-plate force lines from the drain terminating at the channel region appear to play a major role and cause a rise in feedback capacitance, as shown in Figure 10. Further proof of this mechanism was demonstrated with n-channel depletion devices of the

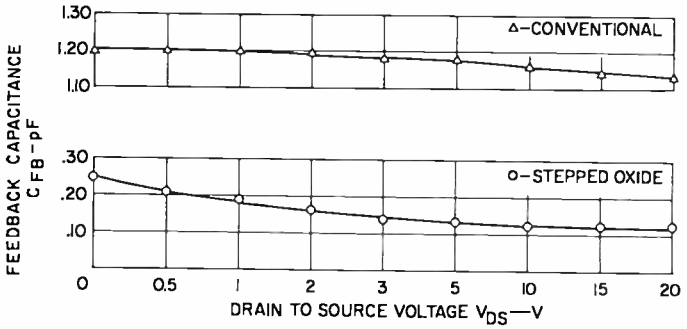

Fig. 8—Comparison of feedback capacitance for conventional and stepped-oxide devices.

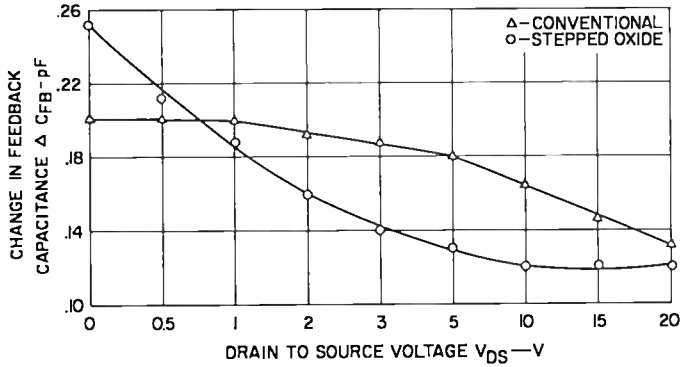

Fig. 9—Comparison of change in feedback capacitance with voltage for conventional and stepped-oxide devices.

same geometric relationship, as shown in Figure 11. When sufficient bias voltage $-V_G$ is applied to the gate of the n-channel units to simulate enhancement conditions ($I_D = 0$), the C_{fb} drops on any applied $+V_{DS}$ above zero; however, with the introduction of current ($I_D > 0$), a slight rise in C_{fb} is experienced before the incremental drop, with V_{DS} equal to 0. Thus, the fringing mechanism, shown in Figure 12, predominates over a small voltage range before the depletion or space-charge capacitance from the extension diode affects the C_{fb}.

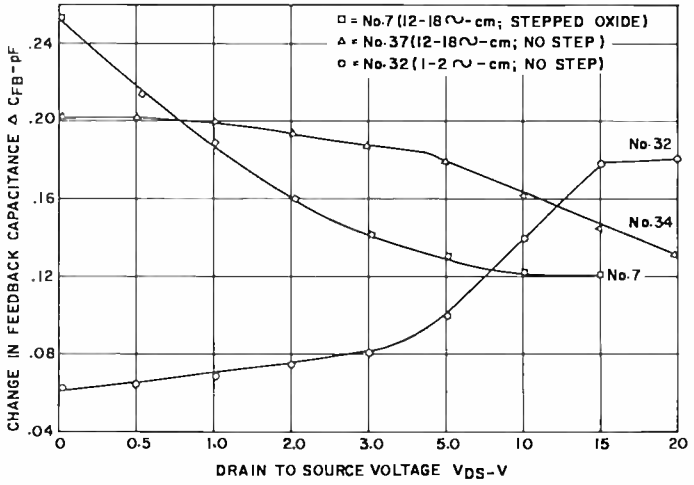

Fig. 10—Effect of use of heavily doped substrate material on ΔC_{fb} versus V_{DS}.

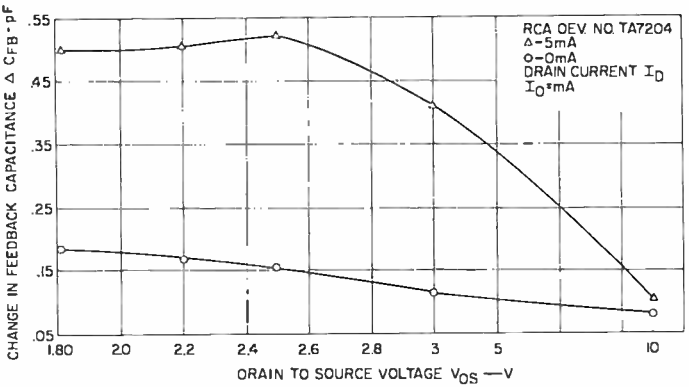

Fig. 11—ΔC_{fb} versus V_{ds} for n-channel depletion devices.

A general summation (C_{fb}) formula can now be written that takes into account all the influencing mechanisms shown in Figure 12:

$$C_{fb} \propto \frac{N[C(fl)_c] + C_{gox}}{\frac{1}{C_{cm}} + \frac{1}{C_j} + \frac{1}{C_{cx}}}$$

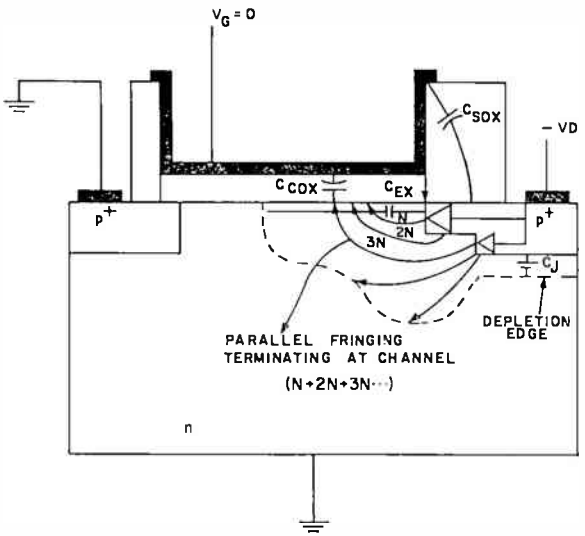

Fig. 12—Effect of fringing or parallel-plate force lines.

where $N|C(fl)_{ss}|$ is the capacitance of the fringing parallel lines, N is the number of lines terminating at the channel, C_{sox} is the stepped-oxide capacitance, C_{cox} is the channel-oxide capacitance, C_j is the space-charge capacitance of a normal junction (applicable with devices having no extension diode), and C_{j_e} is the space-charge capacitance of the extension diode.

Discussion

Results of this development show that reversal of the polarities of the p-channel device shown in Figure 1(b) will result in the structure of a depletion device such as the RCA-3N138. Comparison of the depletion and enhancement devices reveals similarity only in feedback capacitance (0.2 picofarad) resulting from the use of identical stepped-oxide structures. Other electrical parameters are different because of inherent differences in electron and hole mobilities. This difference is demonstrated most clearly by the transconductance measurements. The transconductance g_{fs} for the 3N138 is approximately 5600 micromhos at 5 milliamperes; under the same conditions, the p-channel device has a typical g_{fs} of 3600 micromhos. Other differences are as follows:

(a) The charges in the oxide channel of the depletion device result in a drain current of 16 to 20 milliamperes at zero gate voltage V_G, while the enhancement device exhibits nanoampere current under the same condition.

(b) Different interface state densities of the two devices are the result of different metalizations, background materials, and levels of process cleanliness. These factors have a marked effect on the cutoff and drain voltages.

Because of these differences, the merits of the two devices cannot be compared in a competitive manner. Each device should be considered as a distinct unit.

Conclusion

A p-channel full-gate triode MOS stepped-oxide device has been developed. In this device feedback capacitance has been substantially reduced, as compared to conventional MOS transistors, without affecting other electrical parameters. Control of the p-type extension appears to be critical, not only for limiting spurious capacitance but also for obtaining proper junction-breakdown levels.

Acknowledgment

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