RCA Engineer

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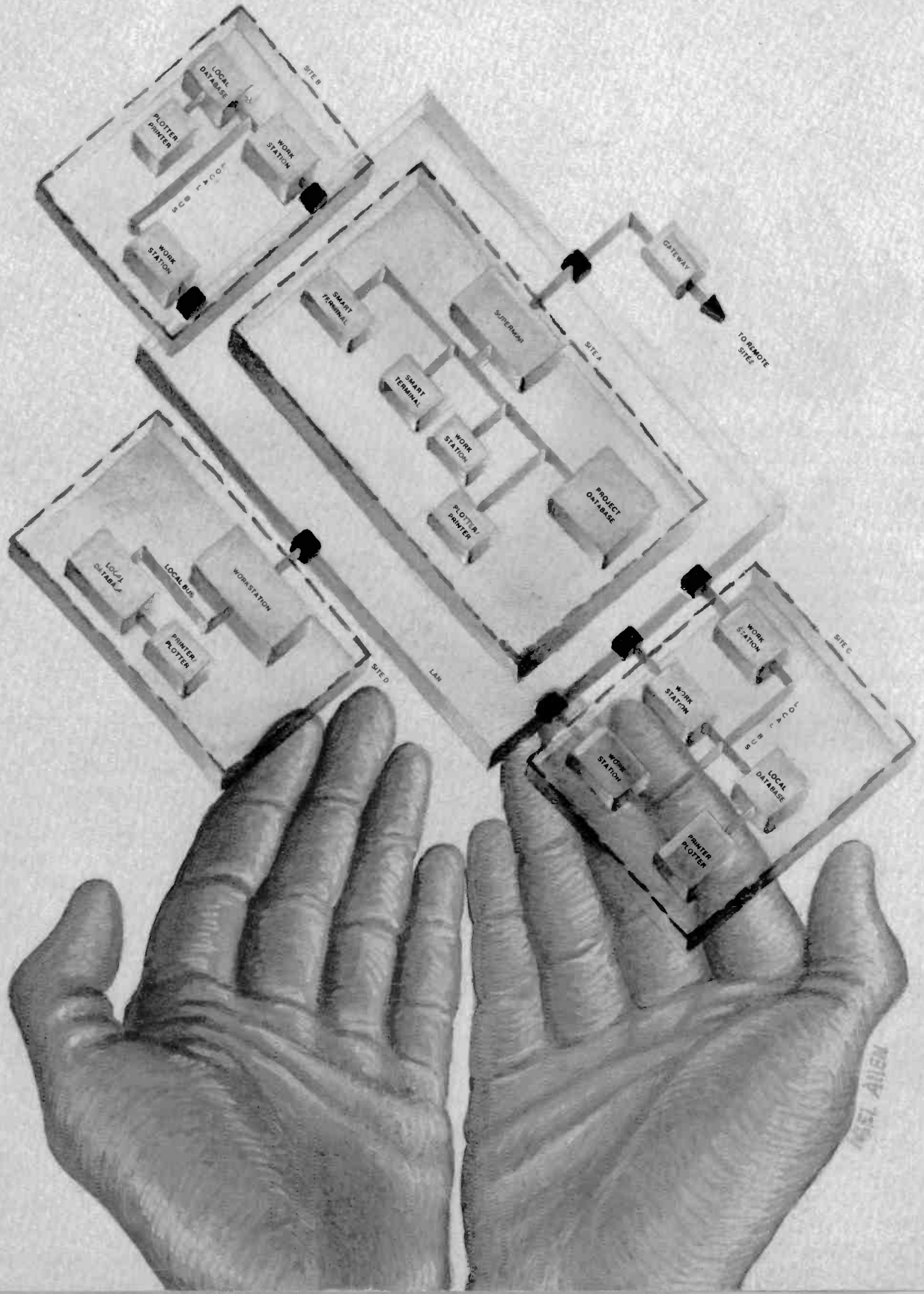
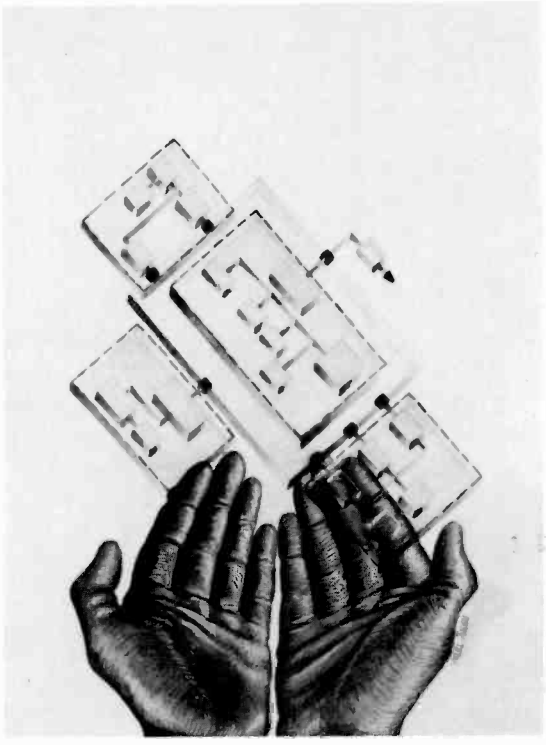


Cover illustration by Mel Allen



Putting computer power at the engineers' fingertips.
Our cover depicts the possible shape of future systems that could allow engineers at different sites to have system-wide access to tools on other stations and on a superminicomputer. In this issue, RCA authors describe today's realities—the ongoing and successful efforts to automate the engineering workplace.

—MRS

Illustrations on pages 7 and 12 by Mel Allen; page 13 by Diane Farkas; page 20 by Helen Mary; page 28 by Denise Miller; and page 61 Joseph McGarrity.

RCA Engineer

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

C.A. Quinn

Bringing computer power to the engineer

The strength and vitality of our engineering community sets the pace for RCA's future. Increasing pressures for shorter design cycles, better quality designs, and faster response to changing market needs, all focus on the effectiveness of the engineering staff. The growing complexity of the engineering task reaches beyond the design cycle into vital areas of the manufacturing process. This demands better coordination and control.

Sheer numbers of engineers will not suffice in the solutions to these types of problems. We must ensure that each engineer is operating at maximum potential—increasingly, this means engineers must have direct access to computer tools that improve individual productivity. Personal computers, graphic work stations, electronic communications, retail software, and so on, offer new options that complement and extend the conventional mainframe solution. At the same time, the multitude of choices can lead to chaos if a broad plan is lacking.

RCA management is addressing these issues by investing heavily in programs that bring computer power directly to the engineers. The productivity and performance gains that will ensure our future are dependent on meeting this challenge.

Many exciting steps are underway across the Corporation. This issue of the *RCA Engineer* reports on some of the leadership efforts.

Charles A. Quinn
Division Vice-President and General Manager,
Video Component and Display Division

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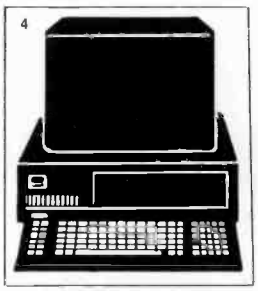
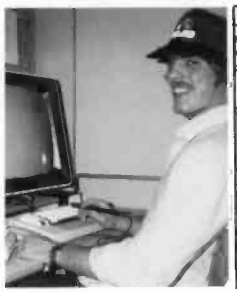
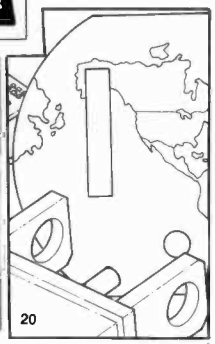
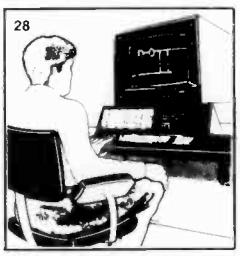
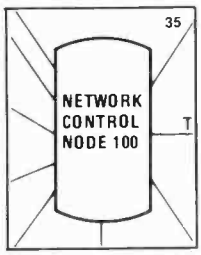
in this issue ...
automating the engineer's workplace

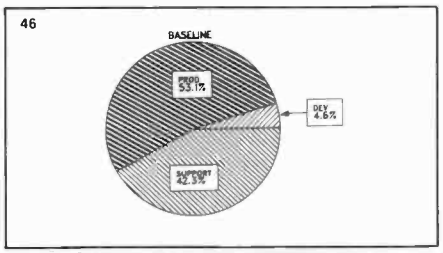


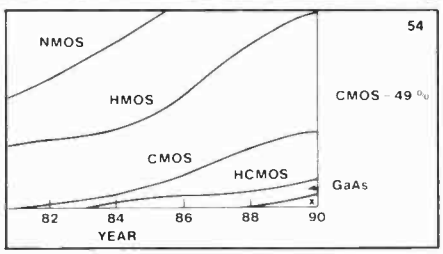












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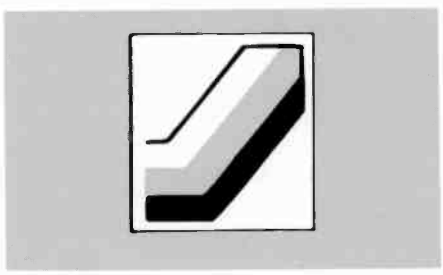
materials science applications,
imaging technology,
communications.



J.C. Miller

VCAD, an engineering productivity strategy

VCAD is an aggressive computer-based engineering productivity strategy. Video—Computer-Aided Design tools are already dramatically changing the work style of engineers, technicians, secretaries, and managers at RCA Video Component and Display Division.

Abstract: *VCAD is an aggressive computer-based engineering productivity strategy; the initials stand for the Division's name as well as "Video—Computer-Aided Design." This paper describes the VCAD system from concept through implementation and covers the purpose, architecture, major subsystems, training, and early results. VCAD has been a successful program. Even at this early stage the best testimonial is the strong desire from the engineering managers for more VCAD tools. Although VCAD is technically a computer system, from a managerial perspective it is a productivity multiplier. Companion papers in this issue contain expanded treatment of two VCAD subsystems: the CADAM graphics design system and the use of personal computers.*

Final manuscript received March 22, 1984.
Reprint RE-29-3-1

The Video Component and Display Division (VCD) had made modest use of computer technology in previous years; critical design needs had been programmed, but most of the ancillary tasks were fragmented across departmentally based systems. Limited use was made of the Corporate Computing Center due to its cost, features, and remoteness. Lacking a coherent plan, the Division had acquired a number of small computers, each different and incompatible. There were few economies of scale. Many tasks suitable for a computer remained in a manual mode. The dilemma was how to change to a modern system without destroying the existing base of applications.

Video—Computer-Aided Design (VCAD) began in early 1983 as a multi-year proposal to increase the productivity of the Engineering Department through a carefully designed and well-integrated computer system. By the end of 1983, Phase I of the VCAD program was complete; a broadly conceived system had been installed and was in productive use.

Approach

The VCAD effort began with a recognition of the primary needs of the Engineering Department. We sought increased productivity and concluded that a massive infusion of computer technology was needed, but we lacked the resources to write large amounts of code or to tackle major technological risks in the computer approach. We recognized that our community required assistance in administrative (non-technical) computing, electronic sharing of information, coupling of discrete systems, increased local computer "horsepower," and graphical design aids. Significantly, VCD senior management was willing to back the VCAD project based upon intuitive productivity arguments as opposed to conventional cost/benefit analyses.

The VCAD design philosophy has been to provide a locally-based distributed system in a standard environment with a logical and comprehensive communication framework (see sidebar, facing page). Fortunately, the evolution of the computer art had resulted in technology that was not available in earlier years. An approach was defined based upon several elements.

- Use of the IBM 4341 computer with VM/CMS as the core of the system. This is a low- to mid-range machine with very reliable hardware and a stable operating system. The host can be upgraded as the system load demands. The IBM 4341 runs in an unattended mode 24 hours a day, 7 days a week. All non-IBM computers and terminals link to the host via the communication nework.
- Construction of a local area network (LAN) to serve as the communication bus joining the host and the many terminals and computers already in place. A LAN is a multi-port communication switch that allows one to logically and simultaneously connect pairs of terminals; it uses translation tables and a network controller to link devices with different protocols, transmission speeds, parity conventions, and so on. Within rather wide limits any two devices can be coupled. The LAN provides the technical means to accommodate the variety of existing terminals and eliminates the need for an additional investment.
- Recognition of the personal computer as the key to putting computer power directly on the desk of the professional. The IBM personal computer (PC and XT) was chosen as our standard. Each PC was attached to the LAN and can operate in either a stand-alone or 3278-terminal mode. The PC provides adequate dis-

Video—Computer-Aided Design overview

The goal of VCAD is increased productivity. The VCAD approach is to saturate the entire engineering department with common hardware and software under a comprehensive integrated system design.

Central host computer. A common hub to the overall system, this is currently an IBM 4341 running VM/CMS. It services CADAM, PROFS electronic mail, VSFORTRAN/VSPASCAL programming languages, interactive and batch work. It also holds common databases and core software, and is easy to expand as requirements dictate. The IBM host supports various IBM, and non-IBM terminals via a 3274 controller and local area network. The computer is highly stable and flexible; it runs unattended 24 hours a day, non-stop.

Local area network. The LAN is an "electronic highway" that links various terminals and computers in a standard framework. As a solution to our problem of equipment from many vendors, the LAN handles devices with different protocols, baud rates, parity conventions, and so on. It supports the PC as a 9600-baud full-screen device, and can transfer files between dissimilar terminals or computers. The LAN is linked to the host via a Hydra protocol converter.

Personal computers. These off-load work to a locally-controlled environment. Powerful PC software lets users solve their own problems where possible. PCs support word processing, spreadsheets, planning, databases, analysis, and so on. They can act as 327X-class terminals to the VCAD host when desired. Personal computers are used by all levels of the organization as the basic computer terminal.

CADAM graphics design. CADAM offers a 0.3-second response time to user requests, supports a large number of users sharing a divisional database, and will eventually grow to 50-plus CADAM terminals. CADAM's friendly design environment is based upon well-known drafting methodology. Using this system, it's easy to train new users and get rapid productivity gains. It generates high-quality output drawings on the Versatec plotter in 30 to 60 seconds. CADAM comes in modules that extend the system to many application areas. The system drives CAEDS and ANSYS to generate 3D designs and finite-element analysis, and couples to a numerical controlled machining module.

tributed computing power on a local (and immediate) basis while retaining the ability to link to the IBM 4341. Each PC has a common configuration and software complement (see companion paper, by Miller and Kelley, for details).

- Selection of a turnkey graphics design package CADAM (CADAM Inc.) as the vehicle for converting the core of the manual design process into an integrated system. Centralizing all of the graphics information into a common database eliminates many duplicate manual steps and enhances productivity. A scaled-down variant of CADAM, IBM's FASTDRAFT, was selected for our remote plants in Marion and Scranton (see companion paper, by Miller and Kunz, for details).

Configuration

The initial phase of VCAD hardware (Fig. 1) consisted of a fully implemented LAN covering the entire Engineering Department, an IBM 4341 with four megabytes of memory, three 800-megabyte disks, a tape drive, a 3274 controller for the 3270-class terminals (provision for 32), two 16-port Hydra (JDS Microprocessing) protocol converters, three Displaywriters and seventy-

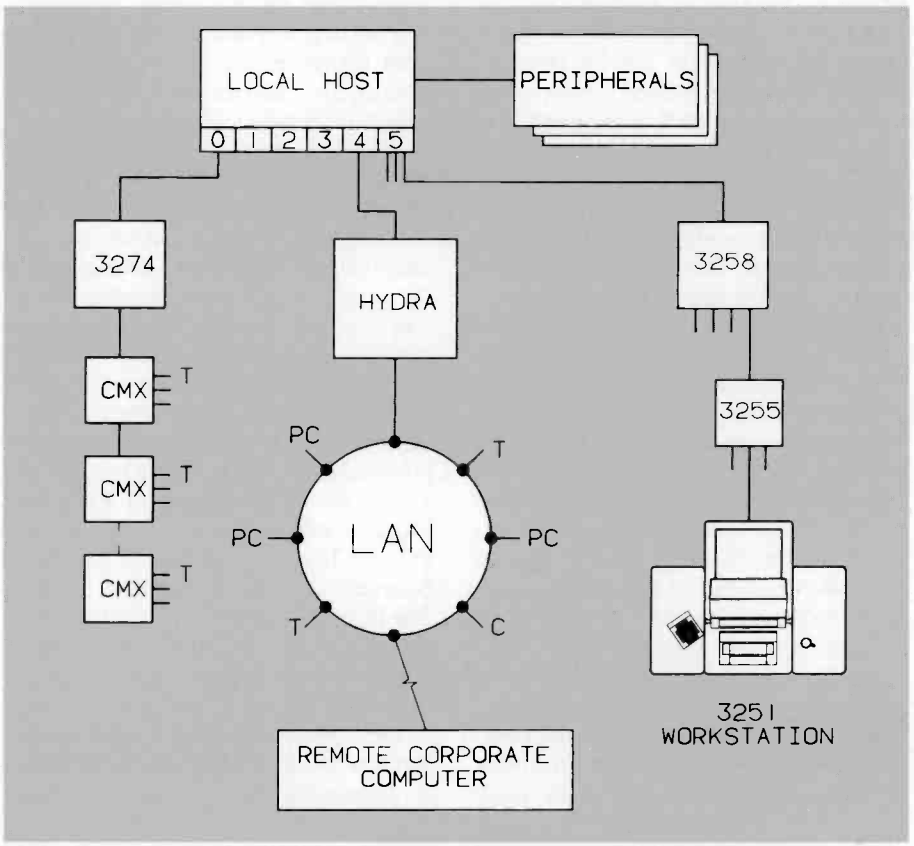
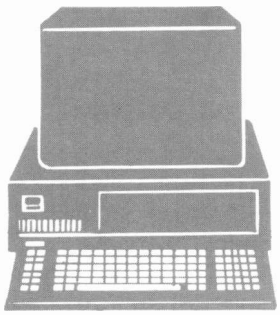


Fig. 1. *VCAD architecture. An overview of the communication arrangement, showing 3274 controller path, the Hydra link, the local area network, and the CADAM terminal arrangement. The local host serves as the gateway for communications. The LAN connects various terminals, PCs, and non-IBM computers as required.*



three IBM PC/XTs—all linked to the LAN, six 3251 graphic design terminals and associated controllers, five printers, and a 36-inch Versatec electrostatic plotter. There are now 168 devices (computers, PCs, terminals) attached to the LAN. The 3251s are 19-inch video graphic design terminals used exclusively with the CADAM design software. We chose the NET/1 LAN hardware from Ungermann-Bass and linked it to the IBM host via the Hydra converter. IBM full-screen terminals (3178/3279) were supported by a 3274 driving Ungermann-Bass's CMX multiplexors.

The communication arrangement is nonconventional. From the outset we were faced with the need to support the existing terminals (from many vendors), and the new IBM terminals. The LAN provided a vehicle for linking the existing terminals but the question remained, "How could we best attach the LAN to the host?" The usual solution would have been an IBM 3705 front-end processor. The Hydra offered most of the necessary features at a lower cost, and with a somewhat simpler system interface. The Hydra is a protocol converter that presents asynchronous screen-oriented devices to the host as 3278 terminals with cursor control. As a side benefit, the Hydra-supplied PC-3278 terminal emulator (ACOM, Computer Vectors) was found to be superior to the IBM 3101 emulator. We have been very pleased with the full-screen terminal mode of operation for the PC. A suitable emulator was also found for the (existing) Hewlett-Packard terminals, which enables them to communicate with the host via the LAN.

It was desirable to avoid the star architecture associated with the conventional 3274 cabling for the IBM-class terminals. The CMX multiplexor operates in a daisy-chain mode that makes it possible to greatly reduce the total cable length of the installation. The communication arrangement offers considerable flexibility in installing new devices. On the other hand, the Hydra decision splits the functional responsibility between two vendors in a critical area. Both Hydra and IBM have been responsive in solving communication problems and offering support. On balance, we have been pleased with the design choice.

Most of the engineering managers use a personal computer as their terminal, and the majority of the engineers have reasonable access to some kind of terminal. Our plan is to have an appropriate terminal available for every user.

Software

It was our goal from the outset to stay with "plain vanilla" software as provided by the vendor and resist the temptation to modify it. This made it possible to minimize the support effort required and improve the overall system stability. All new application software was purchased and applied to the system without change. Many of the programs developed in the past already ran on the same operating system as the corporate computer at Cherry Hill, N.J., thus eliminating the need for a conversion—but this did require the installation of twelve VM/CMS system patches from Cherry Hill to retain compatibility. Overall, the "plain vanilla" and "buy, don't write" combination were good decisions.

For example, the host software complement includes VM/CMS, VSFORTRAN, VSPASCAL, PROFS, CADAM, CAEDS (SDRC Inc.), and ANSYS (Swanson Analysis). By retaining total control of the project, it has been possible to fine-tune the operating system to achieve the desired response times and performance for the various user groups—this would have been difficult to do under shared circumstances. All engineering applications previously run at Cherry Hill (except for a very large design program) have been brought back to the VCAD system. The PCs run Lotus123, MultiMate (SoftWord Systems), and other purchased software. The PC 3278 emulator (ACOM) is a full-screen package obtained from Computer Vectors. It also supports file transfer between host-PC and PC-PC.

The Lockheed-developed CADAM system was acquired as the basis for all graphic engineering design. This is a proven modular product capable of running a large number of graphic design terminals on the same system, all sharing a common database. CADAM offers extensive design features coupled with subsecond response to operator inputs. The fast response time is the key to productivity. CADAM is viewed as the most important application on the host. CAEDS and ANSYS support finite-element modelling.

IBM's PROFS was adopted as the core electronic mail system, but is not the primary tool for word processing. This decision was approached with mixed emotions due to the rather negative observations formed in the RCA Laboratories' experiment. The reasons for the relatively successful installation to date include: VCAD's broad base of installed PROFS users (you have to span the people you normally communicate with), cautious start-up, careful training, follow-up support, but primarily, our nondependence upon the PROFS limited word processing features.

Word processing is supported by a mix between standard PROFS features and MultiMate on the PC. MultiMate relieves the pressure on DCF document preparation, the weakest part of PROFS. Except for three Displaywriters, all Engineering secretaries use MultiMate on their IBM personal computer for their daily work. The ACOM emulator makes it possible to transfer files between MultiMate and PROFS in a straightforward fashion, making it a user decision as to where each task is done.

The PC not only supports useful applications locally, it also off-loads substantial work that would otherwise have "cluttered" the host. In our environment, this reduces the interaction between CADAM and other host-based programs while offering better support to the user. The low cost and wide variety of PC software make it easier to pursue new applications.

Training

The VCAD program had high management visibility within the Division. Extensive training was provided for each facet of VCAD. Locally available talent was mobilized to present a wide variety of training courses, lectures, demonstrations, visits, and so on. Much of the success of VCAD may be attributed to the careful planning of the training effort.

A simple but effective "PC College" was established to indoctrinate users into the use of their new tool and the standard software. Participation in the PC College was a prerequisite to receiving the comput-

er. Extensive and highly personalized CADAM/CAEDS/ANSYS training programs were developed ranging from introductory level material to advanced topics. Training was provided for each software package and for all levels and skills. Training is a demanding, expensive, but vital task. Failure to train leads to frustration, inefficiency, and ultimately to lack of results.

The VCAD training program used a top-down philosophy wherever possible. This simple management concept has proven itself to be a powerful one and has removed much of the mystery from the computer. Mr. C.A. Quinn, VCD Vice-President and General Manager, was the first CADAM student, one week after delivery of the VCAD system; the Division Controller and MIS manager also received early training.

Before an individual user could be trained to use a CADAM terminal, every manager in the chain of command up to the Divisional General Manager was required to have CADAM training. This technique required management commitment and paid substantial dividends in the following months. The managers' intimate knowledge of CADAM has greatly facilitated their constructive use of the system. Similarly, in the PC area, the initial terminals were preferentially assigned to managers who took training as a condition for receiving a PC. Their hands-on understanding made it easier to extend the process to their subordinates. Reminiscent of the famous Western Electric Hawthorne study, this active management involvement contributed to the success of the program.

Measurement

Since the major purpose of the VCAD investment was to enhance engineering productivity, significant effort was devoted to measurement. Engineering productivity is a particularly elusive quarry. Prior to the delivery of the system, detailed measurements were made of the number of hours required to develop each type of engineering drawing in the various departments. This data was used as a benchmark to measure the progress of the CADAM system. We have used results from General Motors (who has reported a 3.81 productivity improvement with CADAM) as our nominal goal. After only one month of CADAM experience, all operators were exceeding their manual rates and were pleased with the CADAM system. Monthly and daily data is being gathered and published to track our progress in detail. A CADAM user group was quickly established to reinforce good practices and provide a feedback forum.

The impact of personal computers on productivity had been sampled by a survey of the users shortly after delivery of the machines and will be repeated after a six-month interval. PC user groups have also been established, sponsored by the MIS Information Center.

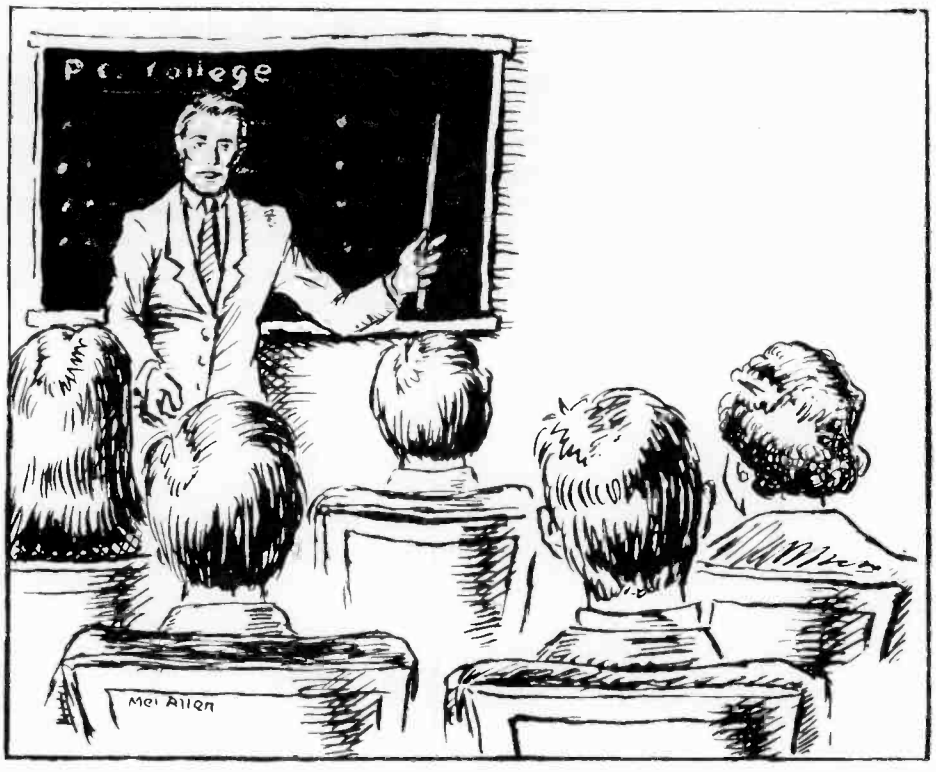
Implementation

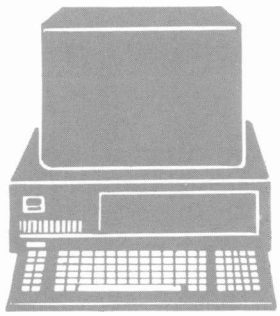
A conceptual plan for the VCAD project was submitted in April 1983, approvals were obtained by midyear, and the equipment was installed and made fully operational by December 7, 1983. All project dates and goals were met. Corporate CISS Staff was helpful at all points and cooperated in allowing a flexible approach to the myriad of hardware/software changes that occurred during execution of the plan.

The plan was implemented by two task-force teams: one interfacing with the vendor (IBM) and another (VCAD) with the user community. Each task force met on a biweekly basis for two hours and represented a collateral duty for its members rather than a full-time assignment. The VCAD task force consisted of a representative from each user department and was particularly useful in hammering out the necessary system-design compromises and communicating with the user community. The smaller IBM task force met with the vendor to deal with the technical details of the project. Excellent support was provided by the vendor. Two full-time professionals were added to the engineering staff to support VCAD.

Expansion

At the outset of the VCAD program a Phase II expansion was envisioned for 1984; in fact, this process is well underway and will more than double the system resources by midyear. Phase II will result in additional PCs, 3178 and 3179 terminals, and triple the number of CADAM stations (using the new 5080 color terminals). Moreover, this phase will lead to an upgraded host, doubled disk storage, an A-size Versatec plotter, and new software





modules (CADVUE, TRANSGRAPH, PRANCE/CBDS, SQL, and so on).

The expansion will broaden the CADAM applications beyond the initial mechanical area into electrical designs (schematics, printed circuit board routing and placement, simulations). PROFS usage will go beyond routine electronic mail into mechanizing a number of paper-based subsystems. We intend to merge Engineering Standards into the CADAM database. A new task force has been formed to begin the process of extending CADAM into the numerical controlled machine area. As with Phase I, the expansion will be coupled with an active training program. The project is being planned using the Harvard Project Manager (Harvard Software Inc.) on an IBM XT. MIS has adopted the VCAD architecture as the basis for the new divisional efforts.

Acknowledgments

My sincere thanks to M.B. Fisher and C.A. Quinn who authorized VCAD on faith; J. Balling (CISS) who ran interference; T. Hart (MIS) who became an enthusiast; P. Kunz (CADAM), W.T. Kelley (PCs), B. Mangolds (Communication), and K. Walker (System) for their key contributions; and to the remaining members of the VCAD Task Force—M. Renfro, H. Hillegass, R. Miller, R. Marsland, C. Lausman, and G. Gadbois—who represented the user community in a professional manner and whose cooperation was essential.

James C. Miller is the Manager of Technical Projects and Engineering Administration at VCD in Lancaster, Pa. He earned a BSEE from Rensselaer Polytechnic Institute and an MEng and PhD from Yale University. He received the Honeywell Award from Yale, three RCA Laboratories Achievement Awards, and shared the David Sarnoff Award for Outstanding Technical Achievement. Dr. Miller holds 23 U.S. patents and has published extensively. His current interest is in the application of computer technology to improving organizational productivity.

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Resource guide:

VCAD system hardware and software

This set of articles on the VCD Engineering organization's progress toward a network of automated workstations includes numerous references to equipment and software. To help you sort out the options, we have culled this briefly annotated listing complete with company addresses from our own site-specific experiences. If you have any questions, why not call the authors? Or write the manufacturers.

The asterisked items (*) denote PC hardware and software that are considered "standard" for the VCD Engineering organization; individual machines vary in software/hardware configuration. The double asterisk (**) indicates "under study." We do not necessarily purchase from the source indicated. All of the items have been found to be useful in VCD applications, but this does not constitute a blanket endorsement. All software mentioned will work on our standard hardware configuration.

Personal Computer Hardware

Computer: IBM PC with Dual Floppy* or XT System Unit*, with a memory of 256 Kb (minimum)*.

Adapter boards: Monochrome/Printer Adapter* [IBM]; Asynchronous* [IBM]; Color Graphics [IBM]; Printer Adapter [IBM].
Alternates: STB Graphix Plus**. Monochrome graphics. [STB Systems Inc., 601 N. Glenville Avenue, Suite 125, Richardson, TX 75081].
Hercules. Supports monochrome graphics. [Hercules Computer Technology, 160 Beechnut Drive, Hercules, CA 94547].

Display/monitor: Monochrome* [IBM]; Color [IBM].

Keyboard: IBM* [IBM].
Alternate: Keytronic KB5151**. Separate numeric and cursor-key clusters. [Key Tronic, P.O. Box 14687, Spokane, WA 99214].

Printer: Okidata ML93 with IBM Plug'n Play Kit*. Our standard PC printer [Okidata Corp., 111 Gaither Drive, Mount Laurel, NJ 08054].
Alternate: NEC 3550 with Dual Bin sheet feeder. Letter-quality printer for secretaries. [NEC Home Electronics (U.S.A.), Inc., Personal Computer Division, 1401 Estes Avenue, Elk Grove Village, IL 60007].

Personal Computer Software

Operating system: DOS 2.0* [IBM] or DOS 2.1 [IBM]

Database/file managers:

Pfs File/Report. Easy for the novice to use. Suitable for simple filing, reporting, and retrieval applications. [Software Publishing Corp., 1901 Landings Drive, Mountain View, CA 94043].

TIM IV. A relational base with good report-writing features, and allows linked files. Rigid input protocol and limited number of fields/record. [Innovative Software, Inc., 9300 West 110th Street, Suite 380, Overland Park, KS 66210].

Data Base Manager II—The Integrator. Convenient means to move information between different application packages. Simple database, easy to use. [Alpha Software Corp., 30 B Street, Burlington, MA 01803].

R:Base4000. Powerful relational database system suitable for more complex applications. Good features. Not for the beginner. [Microrim, 1750 112th Avenue, N.E., Bellevue, WA 98004].

ThinkTank—The Idea Processor. Unique system for handling outlines, text, concepts, "todo" lists, and so on. Billed as an idea organizer. Very handy for managers. [Living Video Text, Inc., 1000 Elwell Court, Suite 232, Palo Alto, CA 94303].

Plotting: Graphwriter**. A powerful, yet easy to use, package for presentation—quality technical graphs. [Graphic Communications, Inc., 200 Fifth Avenue, Waltham, MA 02254].

Statistics: Statgraphics. A sophisticated and powerful statistical package; many features. [Statgraphics Inc., P.O. Box 1558, Princeton, NJ 08540].

Project Management: Harvard Project Manager. An excellent CPM planning tool for the PC. Works with monochrome graphics. Practical features. Easy to use. [Harvard Software Inc., 512 Great Road, Littleton, MA 01460].

Spreadsheet: Lotus123*. Justly called "king of the mountain." Excellent spreadsheet, simple but useful database, fine graphics, very limited word processing. Outstanding features. [Lotus Development Corp., 161 First Street, Cambridge, MA 02142).

Word Processing: MultiMate*. An excellent "Wang-clone" product with features usually found only in dedicated word processors. Well-received by secretaries and engineers. [MultiMate International Inc., 52 Oakland Avenue North, East Hartford, CT 06108]. Volkswriter and Volkswriter Deluxe. Not used by VCD. Simple to learn and use. Just what the name implies. [Lifetree Software, Inc., 411 Pacific Street, Suite 315, Monterey, CA 93940].

Communications

Local Area Network (LAN): Net/1. Links terminals, and so on, to common electronic data path. Couples to host via Hydra. [Ungermann-Bass, 2560 Mission College Boulevard, Santa Clara, CA 95050].

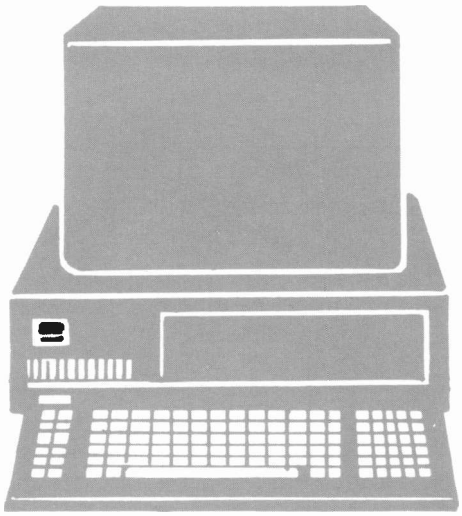
Hydra: Channel-attached protocol converter. Permits PC to look like 327X-class device to host. Supports other devices as well. [JDS Micro-Processing, 25 Mitchell Boulevard, Suite 7, San Rafael, CA 94903].

Terminal Emulators: ACOM*. Used with Hydra. Full-screen 327X emulator with file-transfer capability. [Computer Vectors, Inc., 24871 Pylos Way, Mission Viejo, CA 92691].

CMX: Couples to 3274 terminal controller and allows daisy-chain cabling to various IBM devices. This saves cable length. [Ungermann-Bass, 2560 Mission College Boulevard, Santa Clara, CA 95050].

J.C. Miller | W.T. Kelley

Personal computers, an engineering productivity tool



The personal computer is a powerful productivity multiplier. As one manager said: "I never really wanted the PC, but now if anyone tries to take it away, I'll break their arm."

When the first personal computer (PC) was brought into the Video Component and Display Division (VCD) only a few years ago, it was a struggle; the authorization system was geared toward remote time sharing and centralized computing. The PC was a somewhat heretical approach to computing, deemed suitable for hobby applications but not for "real" computing. The PC allowed users to do their own computing directly—in an uncontrolled fashion. Where would it all lead if everyone could use a computer? Who would direct it? Wouldn't users just play games? Where is the economy of scale? These were just a few of the objections.

In a short time, personal computers have gone from "persona non grata" to the "engineer's best friend." What caused the transition and why has it occurred with such speed? The PC surge reflects the democratization of computing. Plummeting PC costs and explosive varieties of PC software have made it irresistible. Daily ads in the local papers and on TV have extolled the virtues of the PC. Amidst the "hoopla" one can find a large kernel of truth: computers can be used by non-experts.

Well-thought-out software is the key to PC usage. Unlike historical computer users, the PC user views the computer merely as an optional tool to do his real job more effectively. If it is easy, well and good; if not, it won't be used. In fact, the marketplace has generated an amazing range of software directly aimed at the nonprofessional user—these are tools to solve problems. A dynamic cottage industry has been spawned. No longer does the user require the time and skill to craft his own tools. Just as the do-it-yourself carpenter does tasks formerly done by the professional, so now the PC user picks off-the-shelf software to do his work.

The Apple personal computer, with its cost, features, and software, was the trigger to this market avalanche. The now-famous VisiCalc (VisiCorp) spreadsheet was the professional's eye-opener—it provided a generic solution to a wide class of important problems and attracted users exponentially. VisiCalc on the Apple was chic. IBM's later entry into the market put the seal of approval on PCs and, through a strong marketing strategy, rapidly rose to a dominant position. Writers of PC software adopted the IBM PC with its open architecture as the machine of preference and gave it the position of a de facto standard.

On the average, the professional spends the bulk of his time communicating, documenting, and planning—as opposed to designing or testing—yet these "administrative" tasks traditionally have the weakest level of support (Fig. 1). In the VCAD approach, we targeted the PC usage directly at the administrative functions (including minor calculations) as opposed to the computer-intensive tasks.

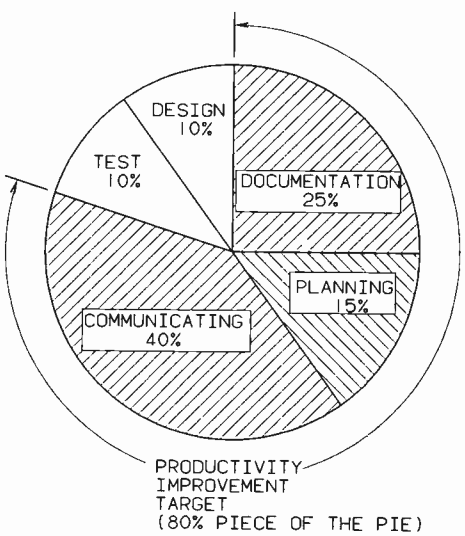


Fig. 1. *Pie chart breaking out the typical engineer's time profile, based upon data from Hewlett-Packard. Traditional computer support focuses on the test/design segment. The bulk of the engineer's time is spent upon tasks that can benefit from computer assistance, but this is not widely provided. VCAD seeks to service the entire pie through a rounded set of tools.*

Abstract: *The personal computer (PC) is a powerful tool for bringing computer power directly to the user. The Video Component and Display Division has made extensive use of the IBM PC as part of an overall engineering productivity strategy (see companion paper, by Miller, on VCAD). This paper describes the approach taken, some of the thinking behind the hardware/software choices (risks and mistakes), system integration, training, and results of an early productivity measurement.*

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Approach

The VCAD project recognized the PC as a key part of its overall productivity strategy. It provided a means to distribute useful computing power directly to the engineering community, flexibility in selecting software, and the potential to be used in a dual mode—local or terminal. It was clear from the outset that the PC was the means to reach a broad class of users and change their work habits. The PC was not viewed as some sort of super-design workstation for the elite engineer.

The next decision was which vendor and what product? From a hardware perspective, there were many suitable choices and complex tradeoffs to consider. But from the software side, the answer was clear: we chose the IBM PC/XT (the XT is a PC with a Winchester disk) as the standard. While remaining alert to the turmoil in the operating system area, PC-DOS was adopted as the standard operating system. We wanted to avoid the problems that accompany multivendor installations and resisted the temptation to select several PC vendors, each offering some purported advantage. In the VCD engineer ing environment, standardization offered significant advantages over specialization and proliferation.

Standardization is a risky tactic in a volatile market environment; it is easy to pick an Edsel. The VCAD design concept does not depend upon the PC being an IBM one. So far, the choice has stood the test of time although we are constantly on the alert for other trends. There are over one hundred manufacturers of PCs and literally thousands of software offerings. The risk of making a mistake is high. We also learned that there are many subtle errors one can make in meshing PC software to specific hardware configurations. Because the field is relatively new and highly fragmented, it is much more difficult to make good decisions about PCs than about the nominally more complex mainframe options.

Within this conceptual framework, a standard configuration was devised for the PC and the XT. The engineering standard PC/XT was a 256K machine with a monochrome monitor and Okidata 93 printer. A variant configuration was adopted for the secretarial user (different printer). For purposes of investigation, some machines were acquired with minor variations: color monitors, Hercules Graphics cards, more memory, math co-processor, pen plotters, and so on, but these represented variations on a theme rather than radical changes. Each PC/XT was also configured to be attached to the local area network (LAN) so that it could communicate with other devices and computers.

An intuitive judgment was made on the ratio of PCs to XTs, balancing the following factors: cost, ease of use, number of users of the machine, and user sophistication. The XT was felt to be suitable for the more experienced user, the person who could make intelligent use of the larger hard-disk capacity, or the person who had an identified application requiring the disk. The XT user also tended to be someone who would not be sharing the machine with other users. Limited disk-security features made it too easy for someone to inadvertently ruin the disk's contents in a shared environment. The PC was a good entry-level machine. We bought 73 machines in 1983, with PCs to XTs in a 4:1 ratio. All secretarial machines were PCs.

Although there is considerable enthusiasm for the PC as an engineering tool, it is not a cure-all. Many other kinds of PCs and workstations on the market offer more computing power, specialized analytic software, and so on. As the need for higher "horsepower" arises, these terminals can be attached to the LAN without change to the system. For example, experiments with the PC as a laboratory instrumentation computer have shown it to be insufficient for some of the more computation-intensive tasks. In such applications, a 16-bit machine with a faster processor is required. Also, we would characterize the standard configuration as having a weak graphics capability; this can be improved by several relatively minor changes or by use of the host.

The broad dilemma was whether to wait for things to settle down and make a safer choice, or to proceed in the face of certain change. We have opted for the latter in the belief that the overall system architecture is sufficiently robust. Downstream, we will acquire PC-type machines with increasing capabilities.

Software

Adopting reasonable hardware standards early in the project made it possible to investigate software from a more systematic viewpoint. It was assumed that the primary application for the PC was in simple applications with a high administrative flavor as opposed to computer-intensive or graphics tasks. Early in the process, word processing and spreadsheets were identified as the basic software areas, in addition

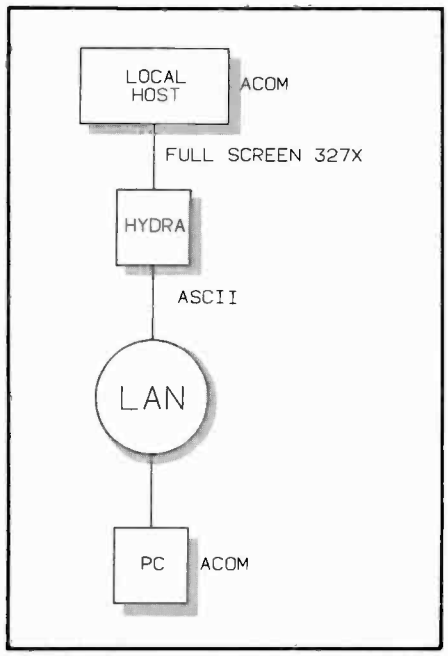
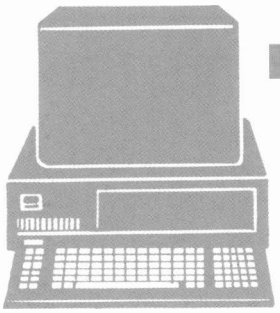


Fig. 2. *The PC connection. The personal computer is attached to the local area network, which in turn is coupled to the host via the Hydra protocol converter. ACOM software in the PC and host cause the PC to be presented to the IBM 4341 as a full-screen 327X-class device with full-function key support. ACOM also supports two-way file transfer. When in the terminal mode, the PC is driven at 9600 baud. Upon request, the PC can be linked to other devices on the LAN, or of course operate in a stand-alone mode.*

to ancillary areas such as database managers, statistics, graphics, project planning, and so on. At all times we tried to balance the tradeoff between doing tasks on the VCAD host versus the PC. This is indeed a delicate balance—on the one hand, putting too little on the PC emasculates the original purpose, on the other, each PC tends to become a miniature computer center.

Word processing (WP)

Perhaps no area has as many choices and different user opinions as word processing. No one seems to agree on the ideal set of features. In fact there is no one best WP, but a surprising array of specialized offerings, each with strong and weak features. Volkswriter (Lifetree) was selected at the beginning of the VCAD effort (based upon simplicity and ease of learning). Before purchasing it we learned of MultiMate (SoftWord Systems Inc.) and made a decision to change direction. MultiMate, a WP based upon the popular Wang dedicated-

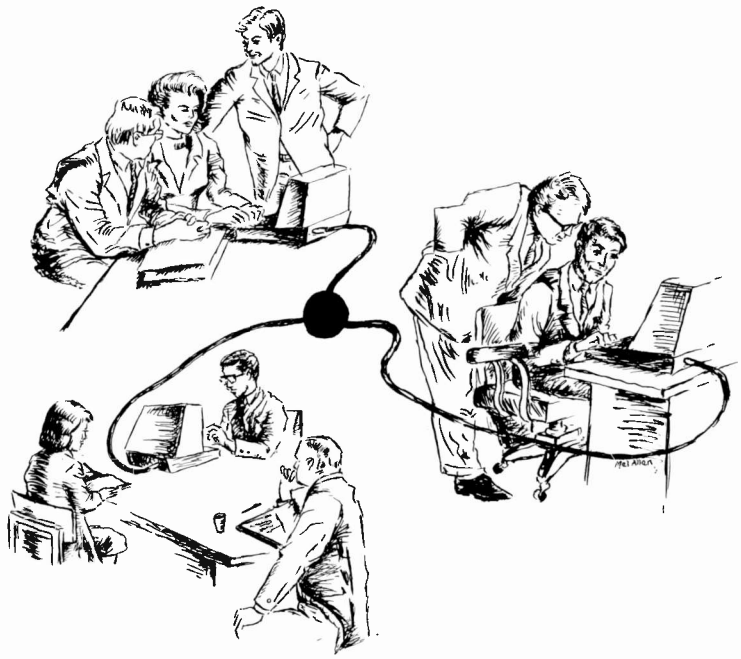


WP system, has an extensive set of features, is well supported by the vendor, and approximates the features of a dedicated WP. From a psychological point of view, it was attractive because there were several Wang WPs already in use in the Division; MIS was asked to concur in the recommendation and they did so. Engineering secretaries who had been trained on the Wang, now prefer the PC with MultiMate.

Spreadsheet

Here the decision was easy—Lotus123 (Lotus Development Corp.), perhaps the finest software written. Lotus123 builds on the excellent VisiCalc concept and adds extremely useful capabilities. Lotus123 offers excellent spreadsheet features, useful interactive graphics, modest database capabilities, and very limited word processing. Standard output interfaces make it possible to transfer information between MultiMate and Lotus123 (as well as other packages).

Fig. 3. *Secretary using the PC and MultiMate for word processing. The general reaction of the secretaries has been highly favorable. Some secretaries are also using packages such as Lotus123 for spreadsheet work. A turnkey Lotus123 template was created to fully automate the business expense report from input to final form ready for signature. Such techniques are improving efficiency.*



Communications

We made a mistake in this area, initially selecting the IBM 3101 emulator to link the PC to the LAN. After acquiring it, certain deficiencies were found in the software that caused us to look for another solution. Fortunately, the ACOM emulator (Computer Vectors) was found; it supports file transfer as well as PC-3278 emulation.

MultiMate, ACOM, and Lotus123 were installed on virtually all of the PCs acquired. They became the basic software building blocks. It has been a gratifying process to watch users develop their own applications with these tools. Many tasks that would never have reached the level of approval on an MIS Data Processing Request were now being solved quickly and imaginatively, following only a few hours of instruction, often by users with no computer background.

PROFS

Although the IBM Professional Office System (PROFS) is not a PC application, each PC owner is coupled to PROFS via the LAN. From a software point of view, it is a package directly available to each user. PROFS serves as the electronic mail link between VCAD users. Using the ACOM emulator, files can be transferred between host and PC; this allows a letter to be composed in MultiMate, sent to another user via PROFS, and so on. Of course the full spectrum of PROFS features are available to each PC user.

A number of packages (database managers, project planning, graphics plotting, statistics) have been reviewed. This is an ongoing effort of the VCAD task force; new software is periodically acquired and studied to determine its utility. Formal reports are generated to document the review. In general, these offerings are specialized and of interest to only a portion of the PC community. Perhaps a dozen different packages are in use within the VCAD community. Authority to purchase PC hardware and software is focussed within engineering to minimize proliferation and encourage synergy among users.

Training

Several decisions were key to the PC installation process. Every person assigned to PC had to agree to take training prior to receiving the machine. Secondly, a "PC College" was established as a forum for training. The PC college was not a highly structured school. Students were asked to devote adequate hours to learning DOS, typing skills, and Lotus123 using programmed tutors and selected problems. This combined self-study with hands-on use of a PC and short lectures. MultiMate was

Typical comments on the PC investment

"... Having had little previous exposure to computers, I was slow getting started but I see more and more applications as time goes on. I was not anxious to get the unit, but will now break the arm of anyone who tries to take it away! Every phase of my work has been improved by the use of my PC. Clearer memos, better project planning, and more in-depth analysis and documentation of experimental results ...

... The PC is an amazing and powerful tool. The ability to revise documents in MultiMate and have new copy within minutes has been a tremendous time saver ... The system provides an easy access file so that all of the information I need is at my fingertips without going through a lot of paper work ...

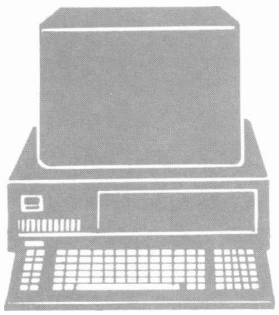
...It is easier and less intimidating to write reports using the word processor than using pencil and paper ... The most important application is large-scale data manipulation for factory test ... I look forward to retiring my typewriter, supplementing my calculator for engineering calculations, and dispensing with hand tabulation of data and hand plotting on graph paper ...

... A returned Development Tube (DT) sample had a poor focus gun. By looking at a data comparison of all DTs shipped, three other "bad" tubes were found that were not previously known. The ability to find interesting and important facts in large data fields has been too cumbersome to do in the past. This PC ability will improve this situation ...

... Lotus123 allows "after thoughts" to be quickly and easily inserted and rapid comparisons made with alternate input variables ...I am now able to keep abreast of time schedules on all important jobs ...The quality of work is improved particularly on design analysis. In cases where formerly features were calculated at a limited number of locations, those same features can be analyzed at an unlimited number of locations. ...

... We're now able to set up project tracking system for each engineer and designer. The PC will allow each individual to update their project as progress is made ... Project outlining, planning and manpower resources are now possible through worksheet analysis by sorting against projects, group leaders, and so on ...

... We're now able to combine 'Things-to-do' inputs for MUSCLE, DT list, Marketing, Technical aid contracts, engineering meetings, Customer Contract Reports, Test Requests, and so on. This was impossible to do manually and has never really been done ..."



taught to secretaries in a 4-hour session; others learned it by themselves. Some of the training was devoted to housekeeping tasks such as care of floppy disks, how to run the printer, and so on. Although the time required to train was insignificant, and it varied with the background of the student, it saved many mistakes in actual usage of the machines.

PC user groups have been established to provide a means to share results, tips, problems, and solutions. These user groups are now sustained by the newly-formed MIS Information Center and service the Division rather than just engineering. PROFS training was conducted on a more formal basis in March, using the standard IBM reference material supplemented by an introduction to CMS. During this training, the students also were introduced to ACOM, the means to link to the host and transfer files.

Measurement

In February, 1984, a productivity study was undertaken to measure the results of the PC investment. A detailed survey was taken of each PC user querying them about the utility of the machine (see sidebar). Some of the highlights of the study are:

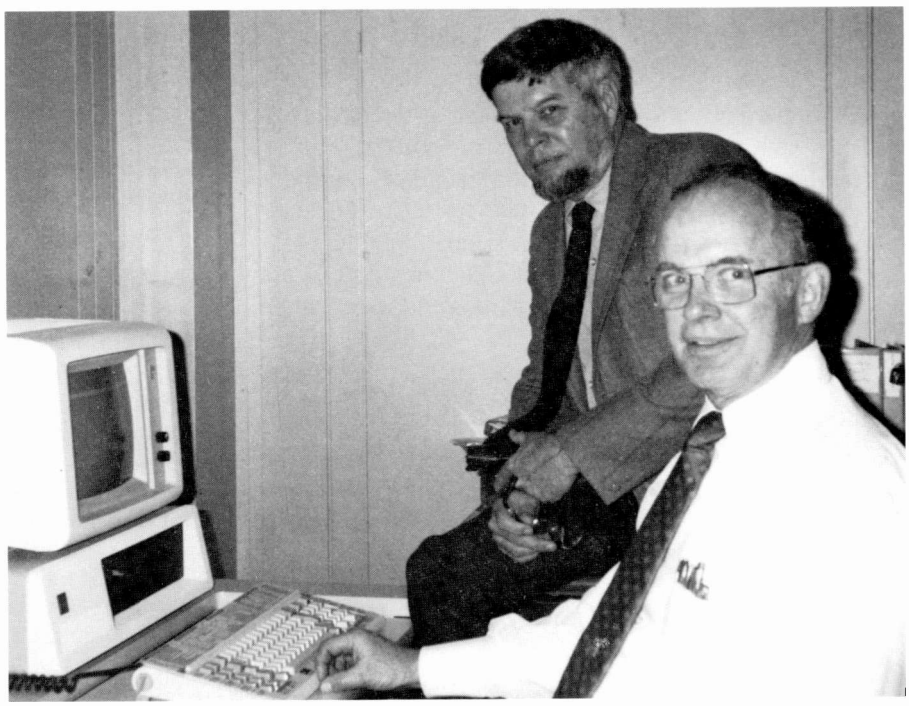
- Almost uniform enthusiasm, good response to the standard software, and a significant increase in computer literacy.
- 73 machines installed. Productivity gains of 25 percent per machine hour after only 1.8 months, and average machine use of 4 hours per day, with 2.6 users/machine. Faster problem solving. Lotus123 productivity gain 2.6:1, and MultiMate productivity gain 1.5:1.
- Better planning, communications, project tracking. Creation of simple but useful databases in all areas. A myriad of useful analyses reduced to routine.

Expansion

Based upon the favorable initial user reactions, we are in the process of defining the Phase II VCAD expansion in the PC area. The current plan is "to reward the rich," that is, to add additional resources preferentially to the groups that have made the best use of the first PCs. Our problem is slightly more complex the second time around as there are additional PC offerings to consider (XT/370, XT/3270, . . .), each of which has certain desirable features. In the laboratory measurement area, we are reviewing the IBM 9000 where higher performance is a requirement.

Acknowledgment

Special thanks are due to the enthusiastic engineering community who adopted the new approach while in the midst of major project responsibilities; M. Renfro and H. Hillegass who taught in the "PC College"; B. Mangolds for communications support; and T. Hart who formed the Information Center.



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CADAM, an engineering productivity tool

We are using CADAM, a computer-graphics system, as the key to upgrading our manual design methods into an integrated modern approach. CADAM is already increasing productivity and design quality at VCD, and changing the way engineers work.

Abstract: *CADAM (CADAM Inc.) is the key part of a graphic design system used in the VCAD program. It is an assemblage of powerful computer hardware and software tools. These tools, although internally complex, allow managers, engineers, designers, and drafters to easily perform their normal design functions with greater speed and accuracy. This paper documents the CADAM system from concept to implementation. The rapid success of CADAM is seen by its early use in a broad range of design problems, its easy assimilation into the existing work environment, and the demand for more terminals. Our motivation with CADAM is single-minded: increased engineering productivity. With 2 weeks of training and 8 weeks of production usage, productivity has already reached 2:1 versus manual methods—our goal is 4:1 over the full span of user activity. The CADAM system will eventually be expanded to support approximately 50 terminals.*

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The Video Component and Display Division had made modest use of graphical computer-aided-design tools. Several years ago, an Applicon design system had been acquired and installed in one engineering department. Though a good decision at the time, when viewed in hindsight, certain limitations may be discerned: deficiencies in reliability, number of terminals, ease of training, access, and response time made it inappropriate to extend the system to a broader base. The system was primarily dedicated to specific aspects of electrical design. Eventually it evolved into a closed-shop service in which dedicated operators did a mix of design, plotter operation, trouble shooting, backup, and programming. The operators were physically and organizationally separated from their parent design groups. As with any service center, work scheduling became an issue. Productivity gains were asserted but difficult to monitor routinely. The formal training program was weak, consisting of either do-it-yourself work or a short course at the vendor.

Approach

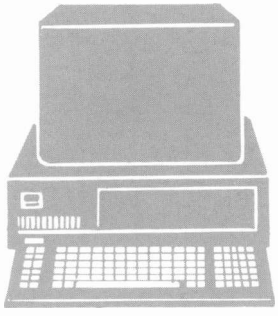
As the VCAD program was planned, we sought a turnkey graphics design system approach that addressed these concerns and that led to an integrated solution. We envisioned a need for a large number of terminals, fast system-response time, a tight focus on productivity, a common database across all users, and a desire to access a wide set of software tools. A balance was sought between speed and advanced design abilities: it is all too easy to incorporate a feature that, while elegant, consumes exorbitant system resource and slows all other users. Because of the need for many terminals, the incremental cost-per-terminal was an important factor.

It was important to integrate the new approach into the existing organizational fabric; therefore, the new system had to be easy to learn, and not require its users to become computer specialists. The graphics system had to assist our communication flow; properly designed and integrated via a good database, it would reduce paper and eliminate duplicate manual steps. Of course, it had to help shorten the overall program design cycle. Different users need to operate the system appropriately; let designers draw and engineers think—not operate a CAD system. Reducing the number of times a part or product is drawn, easy access to current designs, increased quality level, and so on, were other concerns.

Overall, we concluded that a successful and productive solution required a solid host operating system, stable graphics software, and a formal training program. The system was to be imbedded in the existing work culture and organization, yet formed and guided by a standard overall outlook.

The Lockheed-developed Computer-Aided Design and Manufacturing (CADAM) software was selected as the heart of our graphic design approach. This is a comprehensive and stable set of programs that drives a graphics database. The system was augmented by acquiring CAEDS (SDRC Inc.) and ANSYS (Swanson Analysis) to support finite-element modeling as an adjunct to CADAM. These products offer a broad base of engineering tools to use in design from concept and analysis to the final machined part. One man was assigned to implement the system and assumed software, system, and training responsibilities. This is the first CADAM installation within RCA.

CADAM is a widely-used system ca-



pable of supporting large numbers of terminals (one installation has 600+). CADAM provides design and manufacturing advantages such as increased productivity, shorter design cycle, lower costs, better designs, greater accuracy, flexibility to make changes, and the opportunity to have more standardization of design. General Motors has reported 3.81:1 productivity gains via CADAM. Even higher ratios are achieved in specialized tasks. The CADAM system provides a high performance, broad function, design/drafting package together with a number of aids for analysis. It then moves onto completing the job by providing numerical control parts programming abilities. The central database is the system "glue," enhancing communications and reducing manual drawing-retrieval efforts.

Configuration

All CADAM hardware is attached to an IBM 4341 (Model 9) computer with 4 megabytes of memory and 2.4 billion bytes of disk storage. The current CADAM workstation consists of the IBM 3251 graphics terminal, which uses a program function keyboard, standard typewriter keyboard, and light pen, to control the program and enter data. Three of the 3251 workstations are attached to a single 3255 terminal controller stationed up to fifty feet away. The 3255 is attached via coaxial cable to a 3258 controller in the computer room; up to four 3255s can be attached to one 3258. The Phase I installation supports six 3251 terminals. The CADAM terminals are placed directly in the user work area rather than in segregated computer spaces. In a very real sense this configuration is a "starter-kit" to prove the concept.

The designer sits at the terminal (Fig. 1) accessing work stored on the large disk in a special CADAM database. He can recall previous work and make changes, start afresh, initiate an analysis, compare drawings, and so on. Each user can access his own reserved portion of the database or, with system authorization, view and copy designs stored in other work areas. All of the normal graphical commands are supported. The terminal works in a menu-driven mode that makes it easier to learn and that always coaches the user as to the next set of steps available. For practical purposes, the size of the database is limitless—all active work is kept on-line. Data is stored in a so-called "2½D" CADAM database. Every ten interactions the full working drawing is backed up by the system, preventing loss in the event of a crash. Each user designs with a 5K-size working model to instill good practices and avoid waste of resource. Files are protected by a multilevel password scheme and are grouped into sets based upon organizational requirements.

The workhorse of the hardcopy facility is a 36-inch-wide Versatec plotter. The plotter uses an electrostatic process to place elements on the paper or film with a resolution of 200 dots/inch. Through a channel-attached controller, it can produce typical E-size plots in ninety seconds or less. Generally, a plot is completely finished by the time the requester has walked to the plotter. This process saves time formerly lost while searching for a drawing in the manual files. The Versatec Random Element controller and software are used to produce plots with radii that look truly round. Plot quality generally exceeds that of manually drawn tracings.

The CADAM database structure is shown in a simplified form in Fig. 2. In our implementation, we have opened the base to most of the CADAM user community to facilitate sharing of work. Elaborate security provisions may be appended as desired.

For tactical reasons an interim approach was chosen for remote graphics in Phase I of VCAD; IBM FASTDRAFT systems were installed in Marion and Scranton. FASTDRAFT is an interactive, two-dimensional, isometric system for computer-aided drafting. It uses the IBM 3251 terminal with a light pen and typewriter keyboard. The program runs on a stand-alone 7361 graphics processing unit. Output is produced on an E-size drum plotter with up to eight colors. Unfortunately, FASTDRAFT is not directly compatible with CADAM; this complicates efforts to link Lancaster with the manufacturing sites. In

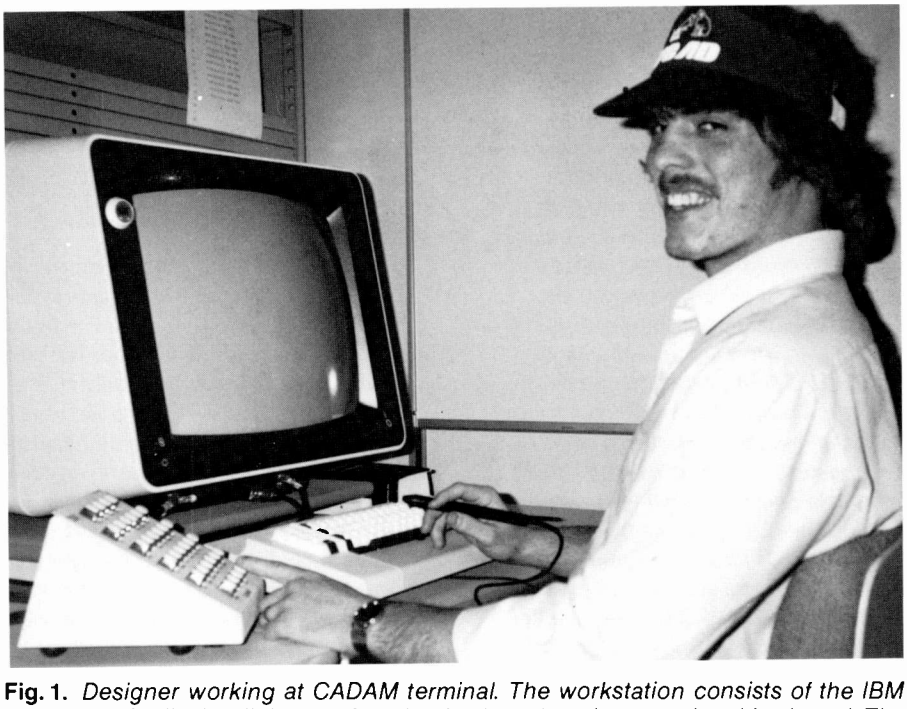


Fig. 1. *Designer working at CADAM terminal. The workstation consists of the IBM 3251 graphic display, light pen, function keyboard, and conventional keyboard. The system provides a 0.3-second response to most requests. The 3251 operates in a mode that shows the menu at the bottom of the screen and the required response options for a selection at the top. The VCAD visor is part of the VCAD training publicity effort.*

the short run, software links between CADAM and FASTDRAFT via IGES (a graphics interchange facility) are being investigated, but a longer-range solution may be satellite CADAM stations.

Software

The turnkey CADAM software has the ability to set various performance parameters and options that are installation dependent. The primary workhorse is the graphics design package CADAM (release 19.1). CADAM is an interactive graphics system for computer-aided design, developed by Lockheed Corporation for over 15 years. CADAM is divided into modules and we are currently running the following: CAD/CAM, Data Management, Hardcopy, Statistical Data, Accounting, 3-D Surface, Geometry Interface, CADGRAM, CADEX, and 3-D Mesh Geometry. CADAM was installed without incident and has proven to be very stable.

CADAM is a complex piece of software that can be tuned in a myriad of ways internally and with respect to the VM/CMS host operating system. This is a complex process and must be done carefully to properly balance the system resources. The users are not involved in tuning, database management, or backup—they concentrate on their work. In our view, system tuning in an engineering environment is sufficiently subtle and dynamic as to require local skills. In the VCAD system, priorities have been arranged such that CADAM is the most important task on the system. Each CADAM user normally sees system response to a light pen "hit" within 0.3 seconds. This extremely rapid response time—even with a large number of terminals and considerable background work—is the key to productivity. A skilled operator can stack up commands even at this fast rate. The machine does not normally limit the thinking process.

CAEDS and ANSYS are used in combination for finite-element modeling. CAEDS is an integrated program that addresses the functions and applications of mechanical product development. CAEDS emphasizes the use of analytical modeling and analysis of a design in the conceptual phase. It interfaces with the CADAM database and will extract 3-D data from a model for mesh generation. Our configuration uses the modules FRAME and GRAPHICS and then interfaces to the nonlinear solver of ANSYS to analyze the model. ANSYS is a large-scale, general-purpose program for the solution of engineering analyses. Figure 3 shows a typical ANSYS output generated on the Versatec plotter.

The combination of the two products, along with CADAM, provides a powerful tool to build analytic models interactively and solve them for any conditions that we presently encounter.

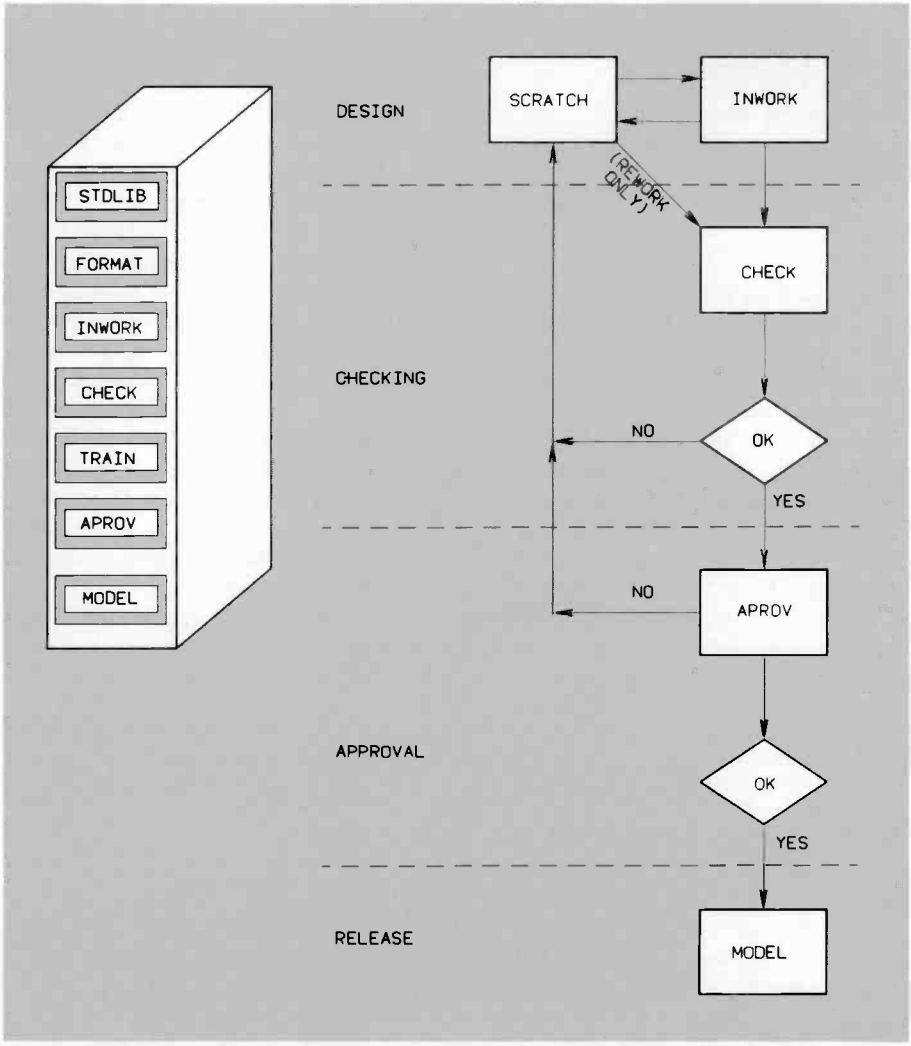
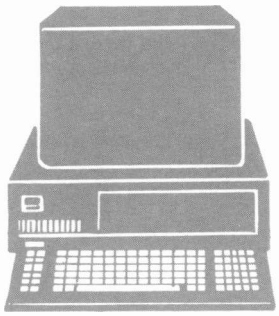


Fig. 2. *CADAM database structure. A design is initiated and stored in the user's work space. When complete, it is advanced through several levels for checking and approval. The user work space is deliberately kept small to force passing work on for approval and release. Each level in the hierarchy blocks the subordinate users from making changes. Final released drawings cannot be altered by any of the users; but they can be copied and used as the basis for starting a new design. While signed file copies are maintained for archival and legal purposes, the "real" design rests in the CADAM database. All drawings are maintained on-line and can be accessed in a matter of seconds by any authorized CADAM user. This facilitates sharing and reduces redundant effort.*

Training

Training is an extremely important aspect of the entire operation. It is an investment in future results yielding return as increased output at a higher quality level. Extensive training is needed to fully use the options available—this not only applies to the everyday users but most importantly to the managers who will have control over the jobs on the terminal.

We have followed a top-down training philosophy in order to imbed CADAM



into the working culture as quickly as possible. The first CADAM trainee was Mr. C.A. Quinn, the Division Vice-President and General Manager. All managers in the command chain between him and the ultimate user were trained prior to training the user. The benefits of this approach cannot be overestimated. Excellent standardized training is available at the vendor but we opted for a local approach. One of the authors (P.J.K.) took specialized training at the vendor's site prior to installation of the equipment; he then served as the local trainer. This technique allows the training to be conducted in a fashion that best matches the norms and work system of the location with minimum disruption to the normal job assignments, and has proven to be extremely effective.

A broad range of courses are presented: CADAM BASIC, On-the-Job Training, BASIC II, BASIC NC, Advanced NC, FEM, ANSYS, 3-D Surface. The basic course includes 40 hours of terminal time and a second 40 hours of on-the-job training doing productive work. Thirty-two people have been trained in 2.5 months, representing over 2000 hours of class time. All have finished the courses and are at least 1:1 with manual techniques at the end of training. Refresher courses are held to maintain skill levels or review new system features. Demonstrations are given to acquaint untrained persons with the CADAM potential. Close follow-up is maintained with each user to review performance and skill level. All graduates of training receive certificates; buttons, hats, and so on, are issued to gain attention.

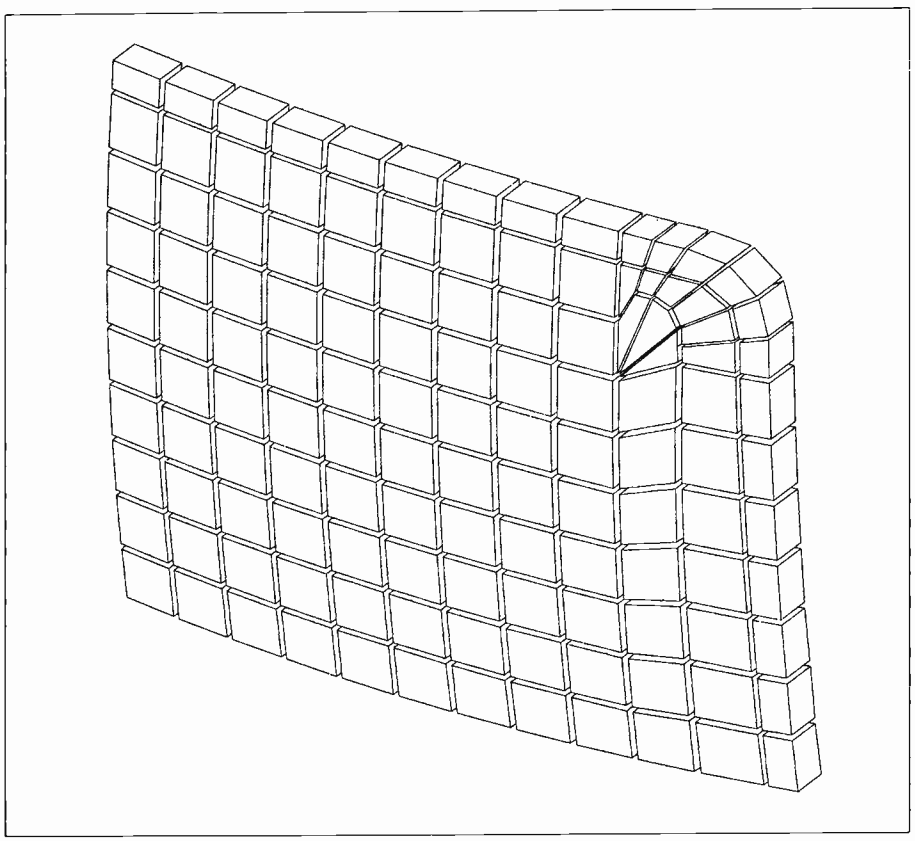


Fig. 3. *Typical ANSYS plot. Finite-element models can be created directly through ANSYS procedures (the slowest method) or through the CAEDS/CADAM techniques starting with a CADAM drawing. VCAD offers good turnaround and excellent plotting through the Versatec graphic plotter. A drawing takes 45 seconds to generate from the ANSYS output run.*

Measurement

A major effort was invested to establish an effective productivity measurement scheme. At a very early date, benchmark data and work statements were received from the managers of the groups that were targeted to receive CADAM. Benchmark data was also received from the Scranton and Marion plants before using FASTDRAFT. It was not simple to obtain meaningful data and a certain element of subjectivity was involved. Each group is being monitored against their individual measurement standards.

The CADAM system has been well received and is meeting our expectations. Evidence of this is seen in the progression of events. Prior to receiving the system, the managers did not believe 1:1 productivity would be reached for eight to twelve months. After they were trained, their figure was revised to six months, and currently, after 8 weeks of production use, the same managers will affirm that the operators are at a level of 2:1 productivity or better. A further sign of acceptance appeared in February, when terminal utilization jumped to better than 90 percent during normal working hours. By March, we were experiencing 90 percent usage over a 12-hour day plus some weekend time. One engineer, after only 3 weeks of production experience, solved a knotty design problem with CADAM and avoided an estimated $100K loss that would otherwise have occurred with a manual design. That single effort "paid" for the CPU.

Our goal is to move up the productivity curve to a level of 4:1 or better. Managerial attention is focused on this factor. Over the period ahead, the productivity monitoring effort will be automated in order to highlight performance and possible retraining needs.

We have reached a point where new training has essentially stopped because each person cannot schedule adequate terminal time. New designs and some rework are being done on the system, which is currently being used primarily for mechanical, as opposed to electrical, design. Users have embraced the new technique and voiced no desire to return to the older ways. It is too early to determine the number of draw-

ing boards replaced by a terminal.

The system has been available for use around the clock since December 7, 1983. The host 4341 runs unattended and has been solid (one unscheduled IPL since November) since installation. This type of performance is crucial to a centralized system. During the first 45 days of operation (6 terminals, 10-hour CADAM day), we logged 1688 production terminal hours from an available 2700 hours (62 percent usage), and lost 21 terminal hours to an in-plant power failure.

Regular CADAM Users Group meetings have resulted in excellent feedback. All trained personnel have agreed that the system is stable, fast, and easy to learn. They are beginning to develop their own techniques to improve their new-found skill. Several user areas have developed new ways to perform their design problems including applications where they had previously been unable to get satisfactory answers. The Drafting Standards Committee has started to integrate CADAM into the work standards.

Expansion

The enthusiastic reaction to CADAM and its auxiliary tools has justified an early expansion of the system. By midyear, the host computer will have been upgraded and a dozen additional CADAM terminals will be arriving. The present projection calls for an ultimate need for more than fifty CADAM terminals and will require further expansion.

The new CADAM terminals will be of the IBM 5080 family, featuring color, raster refresh, and tablet input. The 5080 architecture has one controller per terminal, allowing them to be sited individually as desired. In future CADAM releases, more function will be downloaded to the 5080 terminal, thus allowing more terminals per unit of CPU resource.

At the same time, we are broadening our scope to consider the extension of CADAM into numerical controlled machining. A numerical control task force has been established to do the preliminary planning, and experiments are being conducted with the existing CADAM numerical control modules to determine its viability. Links have been established between VCAD and the existing NC equipment at Lancaster. We had acquired CADGRAM and CADEX, two electrical-design-oriented CADAM modules as a part of Phase I. As the new terminals arrive, these will allow us to extend the scope of CADAM into the electrical design area. CADAM is also being studied as a mechanism to put our Engineering Standards on-line for the technical community; it would be accessed by relatively inexpensive 3179 color terminals using CADVUE. The list of potential improvements is greater than our capacity to address them.

Acknowledgment

Sincere thanks to K. Walker for his contributions in the system area.

James C. Miller is the Manager of Technical Projects and Engineering Administration at VCD in Lancaster, Pa. (see biography, page 8).

Peter Kunz received the BSME with a minor in Materials Science from the University of Connecticut in 1979. He joined RCA in 1979 and his initial work centered on machine design of production equipment for the electron gun, including cathode problems and the quick-heat bimetal cathode process. He received his first patent in 1983 and has several patents pending. In 1983, Mr. Kunz was promoted to Member Technical Staff and joined the VCAD project. In his current capacity, he is responsible for implementation and support of the CADAM computer-aided design system including training, database management, finite-element modeling, productivity measurement, and systems support.

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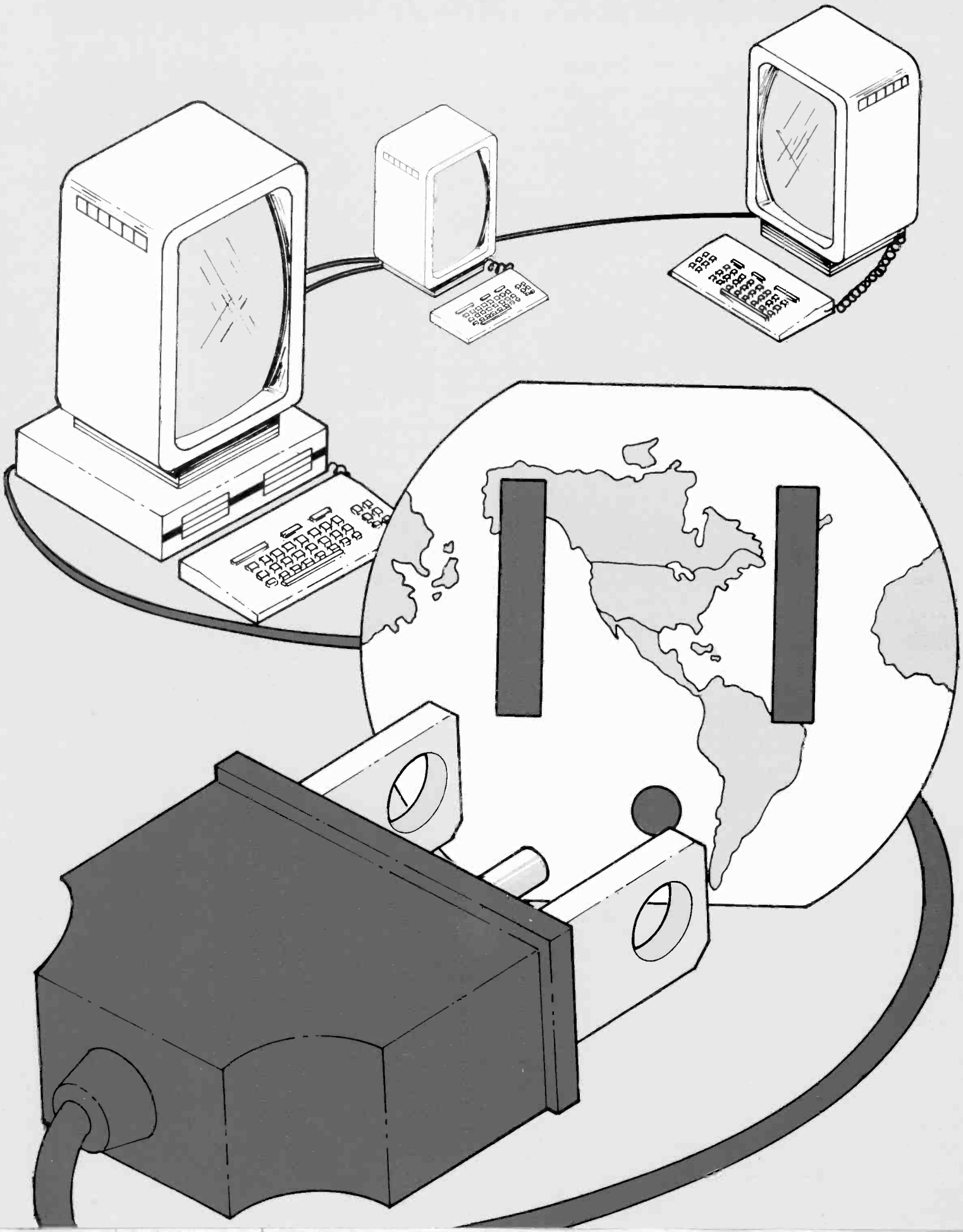
Authors Miller (left) and Kunz.



E.M. Melendez

Emerging engineering design tools

Future workstations will allow flexibility, integration, ease of use, and prospects for creating proprietary sets of design tools. The tools will paradoxically and powerfully integrate broad individual design freedom within highly organized and synergistic group efforts.

During this decade and into the 1990s the design of embedded microcomputer systems will require a new set of design tools. The design environment for the logic and system (hardware and software) engineers will consist of highly intelligent design/development workstations containing highly integrated automated software tools on one hand and an automated software-support environment residing on a superminicomputer on the other. Both these subsystems will be linked together onto a network and will share an adaptive design database management system that will behave as the central data-monitoring and control facility for the multi-engineer team. This design system will increase productivity, shorten the design cycle, and will allow management to better monitor and control the design cycle. Creativity and innovative use of these automated design tools by the design team will ensure a competitive edge in the marketplace.

In pursuing research on what type of tools an engineer will need and use in the future, an interesting cause-effect relationship was discovered. Today, most engineers are team players, relying on each other to perform project-related tasks in taking a product from concept to completion. The size of most engineering-related undertakings dictates that an engineer interface and work in cooperation with an integrated design team. However, in past years engineering as a profession was thought of as an individual pursuit that demanded creativity and a working knowledge of most all of the engineering disciplines. If the recent and continuing evolution to low-cost memory becomes married to the emerging revolution on artificial intelligence, the engineer may move from a team player environment back to an individual, less specialized way of working.

It is important for the reader to realize that the projections of what future engineering tools for the engineering profession will be is an opinion of the author and not a stated policy of RCA. In Burlington, Massachusetts, RCA Automated Systems has been and continues to pursue many of the areas discussed in this article. For example, Automated Systems has under development an artificial intelligence program for microprocessor-based test systems, a plant-wide local area network (LAN) for development activities that is married to today's most advanced engineering tools. Many of the projections made in this article reflect the baseline Automated Systems has established in its drive to provide engineers with the best available engineering tools that will meet not only today's but tomorrow's technical challenges.

Abstract: *This article addresses today's engineering design problems and how they may be solved using technology together with recent and future software applications. Aspects of managing design projects in present and future environments will be covered, including system tools, IC design tools, PC-board design tools and hardware/software integration tools. The distributed database environment is a key to achieving teamwork within a highly individualized working environment. Other aspects of future systems will be artificial intelligence, rigorous project management tools, superminicomputers, and powerful user interfaces.*

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Managing design projects

Use of IC technologies such as gate arrays, programmable array logic, standard cells, custom VLSI, and the ever-increasing amount of software that needs to be developed on most design projects has placed new demands on the designer and the related environment. Today, an embedded microcomputer system requires strict packaging considerations and, as a result, PC-board designers depend more than ever on the assistance of computers. In fact, microprocessor technology has outstripped the ability of engineers to program them without automated assistance.

Today, software maintenance can be as high as 70 percent of the total software costs. For example, a software maintenance plan must include provisions not only for finding and fixing bugs but also for enhancing system capability. These tasks are especially difficult if design data and documentation is not well

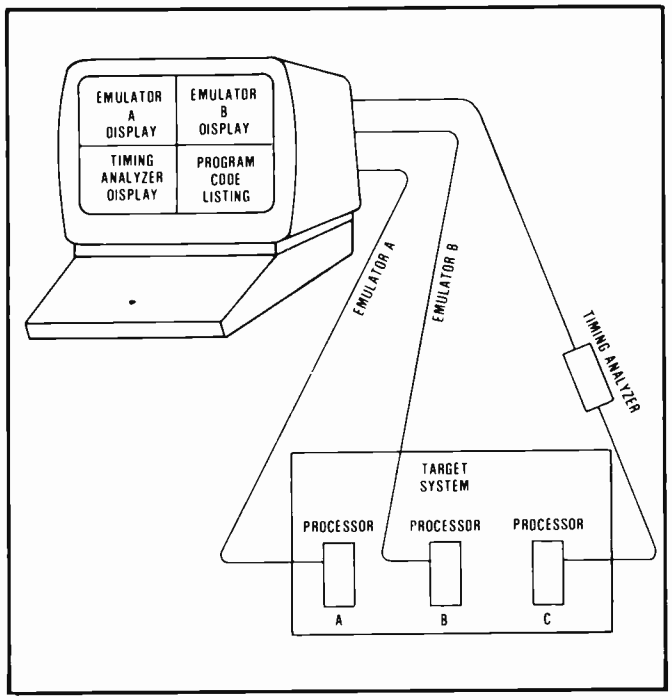


Fig. 1. *Hardware/software integrated configuration allows the engineer's workstation to emulate two processors and perform timing analysis on a separate processor. The window capabilities allow the user to view all pertinent data on one screen.*

maintained. A design team must know the full impact of any code changes it proposes. As a result, it is apparent that the role of managing today's and tomorrow's design projects will not be easy.

Only a well conceived, tightly integrated design environment can support the management, documentation and efficient use of today's large databases. When a design team becomes large, successful system integration relies on project-management tools that support partitioning of the many design tasks. But, effective system and design-task partitioning requires engineering tools that can analyze circuit behavior, packaging, testing, and integration attributes with respect to IC- and PC-board design. Also new tools will be needed that can assist with the design of computer systems and software requirements.

Presently, most IC vendors have access to automated design tools, while PC-board tools are limited to only draftsmen and not engineers. The main problem even with hardware and software integration tools is that they work as separate tools and they only address a subset of the integration phase. As a result, there is an inherent underuse of narrowly focused expensive capital equipment and longer design cycles. In the future, in order to alleviate this situation there will be a highly integrated design system that is network based. It will provide most of the design tools that will be needed for the entire design cycle. It will consist of computer-assisted engineering (CAE) workstations with computer-aided design (CAD) capabilities linked on a local area network (LAN) to a superminicomputer. The design system will contain a highly flexible architecture that will allow users to configure the network according to application. Each workstation will possess multiple microprocessors working in parallel, local database storage, a high-resolution color-graphic display with windowing capabilities, and a highly interactive, easy-to-use, user interface. The workstation will host a wide range of automated design tools that will allow the user to configure it as an IC-design station, as a PC-board design station, or as a hardware/-software integration development system as depicted in Fig. 1.

The design system will behave as a virtually linked system. This will allow users at any station to access tools and design data anywhere on the network without having to know its location. The superminicomputer will host the automated software support environment and the central project database (Fig. 2).

The workstations will typically include 4 megabytes of real memory, 200 megabytes of disk memory, a plotter, and a printer (plotter and printer are optional; they can be shared). As personal computers gain more processing power and obtain virtual memory operations, they will be used as low-cost workstations. Presently, even though the applications are general, personal computers work with CAE design tools provided by second- and third-party vendors that allow them to currently assist the design engineer.

System tools

Most of the IC- and PC-board tools intended for the workstation will be highly portable in that they can also be hosted on the superminicomputer. Yet for the most part they will operate in a workstation environment. These tools are discussed according to their application.

IC design tools

Although most IC automated design tools have existed for years, they have remained largely inaccessible to the circuit and systems engineer. Conventional batch processed tools provide unduly slow response time and therefore can't significantly increase engineering productivity. To increase engineering productivity, engineers must be able to interact with fast and capable analysis tools, to rapidly assess new ideas and efficiently investigate the operation of designs in progress. By providing local, easy-to-learn, graphics-intensive CAE systems that support the interactivity needed, the designers can benefit from the capabilities of the computers they design.

The IC design tools will support most IC technologies especially for fully custom and semi-custom applications. Presently the major sources for IC design tools are silicon vendors since they are best able to keep up with changing technologies and provide simulation tools that accurately predict device behavior. But this will change as more CAE vendors enter the picture, due to their nurturing of software expertise.

The IC design tools that will be available on a workstation are:

- Functional libraries for different IC technologies (for example, standard cells, gate arrays)
- VLSI mask design and verification routines
- Logic and circuit simulators
- Interactive waveform display routines for logic simulation results
- Automatic and interactive function cell placement and routing software
- Schematic and logic capture packages
- Cell compiler libraries and real chip libraries
- Design analysis tools
- Net-list extractors (for physical design) and net-list comparators (for logical design)

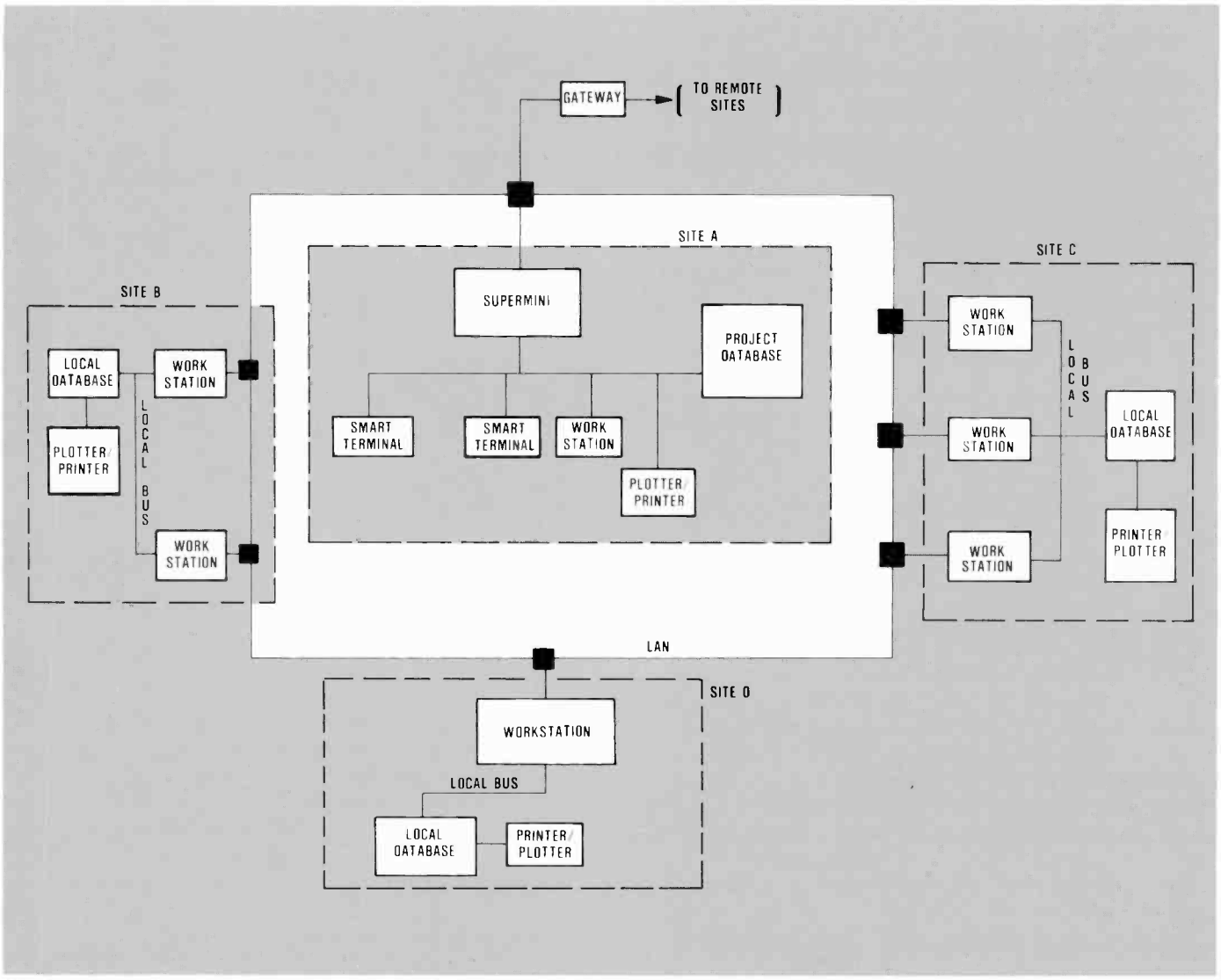


Fig. 2. *This system diagram illustrates the inherent flexibility of this architecture. Engineers at different sites will have system-wide access to tools on other stations and on the superminicomputer.*

- Testability analysis tools
- On-line design and electrical rule checkers
- Physical layout verification routines
- Schematic and layout plotters
- PLA generators and optimizers
- Text editors and graphics editors for generating design specifications
- Format interchange (for putting output tape into proper data format for the intended silicon foundry) software.

Together these tools will support the system design from the writing of specifications, through the logic design and simulation, to mask design and verification. The output will be a silicon-foundry input tape. The physical design tool will offer flexibility for full-custom as well as standard-cell and gate-array design. The logic design tools will support all IC design styles and may be used as a design capture-and-analysis system for printed circuit design.

PC-board design tools

Presently, IC-layout systems aren't the only CAE products moving from drafting to system-design environments. PC-board design systems will also be acquiring automated design capabilities. As a result, we will see that these tools will also be available on an engineer's local workstation. They will play an increasingly important role in front-end circuit-creation and analysis tasks. Future PC-board design tools will address automated data-entry needs. Typically, PC-board designers enter schematics from predrawn pages and thus require a data-entry package that accommodates package-oriented flat designs. However, engineers require more flexible schematic capture programs that support less restrictive data-entry forms. Below is a list of tools that will be supported by the workstation for PC-board design.

- Symbol creation routine
- Schematic entry routine
- Interconnection routing software for multilayer board design
- Schematic and component libraries

APSE—solution for software development portability

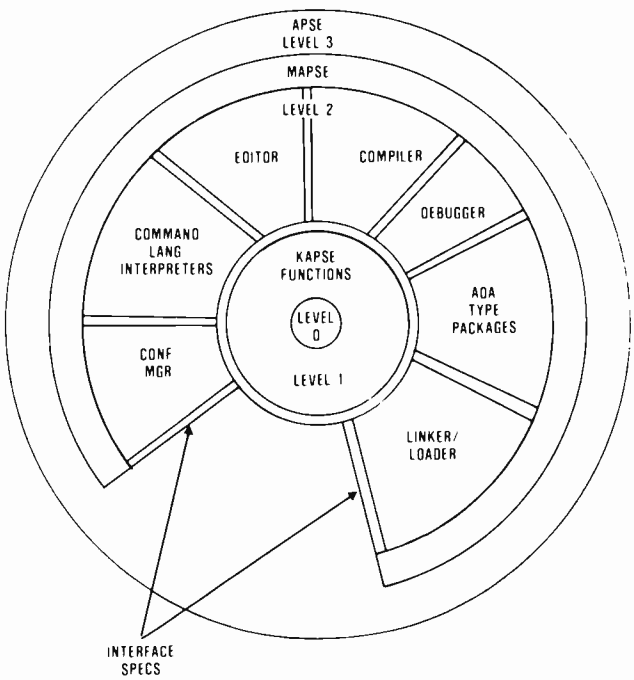
The overall objective of the APSE is to offer cost-effective support to all functions a project team engages in during the development, maintenance and management of Ada application software, throughout the lifetime of the software project, particularly in the embedded computer system field.

To promote portability in this software support environment, the APSE will contain two lower levels: the kernel APSE (KAPSE), and the minimal APSE (MAPSE). This figure depicts the APSE structure.

Level 0—Hardware and host software as appropriate.

Level 1—KAPSE; provides database, communication, and run-time support functions to enable the execution of an Ada program (including a MAPSE tool) and which present a machine independent portability interface. That is, it behaves as a virtual support environment for Ada programs, including tools written in Ada.

Level 2—MAPSE; provides a minimal set of tools, written in Ada and supported by the KAPSE, that are both necessary and sufficient for the development and continuing support of Ada programs.



Level 3—APSE; are constructed by extensions of the MAPSE to provide fuller support of particular applications or methodologies.

- Gate allocation routine
- Fine-line routing and variable grid
- Drawing duplication software
- Automatic component-placement software
- Logic capture and simulation software

Hardware/software integration tools

The major future requirement for hardware and software integration tools is real-time interaction of all the various test support units (such as analyzers, emulation, stimulation, and so on). Today, this is a serious problem since most development system vendors don't offer complete integrated support. Future workstations must allow test instrumentation to interact in a cohesive, real-time manner. The stations will support a variety of processors.

Today, in-circuit emulators are severely pressed to behave exactly like the microprocessors in a target system when the ROM code is tested. These instruments must faultlessly duplicate the nanosecond propagation delay that the CPU exhibits within its internal registers. Future emulators will allow users to emulate two or more target units at once. The emulator provides a window into the inner operation of a microprocessor and simulates its activity, giving the designer the feedback and control necessary for development work. A logic analyzer, alternatively, will evaluate logic timing and states on dozens of input channels simultaneously, and then present results in an easily recognizable format, determining whether the problems are hardware- or software-related.

The station will contain a software-performance-analysis package that will, in addition to symbolic debugging, supply an overview of system operation, printing out the relative activity among various software modules, including I/O routines, system interrupts, memory allocation instructions, or actual program execution states. These activities will be visually presented as time distributions or histograms; as lists of average time spent on each software task; as percentages of the program's total execution time. The station will allow users to detect redundant DO loops, spot excessive time spent on processing interrupts, and pinpoint execution-mode access times. Another tool that will be available is a real-time debugger intended for multitasking of software environments.

These tools intended for the hardware and software integration phase will provide the workstation with a powerful stimulus-response interactive measurement system that can be applied to the integration problem of multiprocessor or embedded systems.

Distributed database environment

In this design system, it is imperative that users have the ability to create and format their own local database without violating the overall structure imposed by the central project data-management programs (hosted on the superminicomputer). A local database in the workstation will serve the individual designers on a temporary basis, holding working copies of portions to the complete base that is stored on the superminicomputer. All tools

on the network will have a common interface to the system-wide database structure via a standard object-oriented interface. Likewise, all tools will have a standard interface to the user (Fig. 3). The database structure will support intertool communications.

The central project database will support not only the automated support environment for the software development effort but also the managing and controlling of all design activities on the design system network. The database will consist of raw data in relational tables, and object-mapping capabilities that transform the data from a relational format into user objects (such as gates, wires, networks, pages, specifications, design documentation, program source text, program documentation, test data, and so on). The database manager, residing on the superminicomputer, inserts and retrieves data from these tables. When requested, the manager extracts data from the project database and transmits it to the local processor in the workstation that made the request. There the local data manager enters it on a disk. Application programs then obtain the data through the data-access manager, a program responsible for translating between user objects and the database formats. In this way, the user can reference and alter a database portion in local memory indefinitely, needing no interaction with the project database. At the end of a session, the local data manager sends the edited portion back to the project database, updating the relational tables to reflect all the changes. The local database and its associated software thus act as a high-speed buffer between the user and the slow, centralized project database.

As a result, the individual designers benefit while performing individual tasks; however, they are subtly required to ensure that their designs' external characteristics conform to the overall structure.

Both local and project databases will have characteristics of a design database management system that elects how to structure the design data within the database system. Although the database system does not interpret the data it manages, a design-database management system "understands" how the structure of the data describes a project. The major components of the design-database management system include: the storage component (reliably storing design data on disk); the recovery subsystem (saving incremental changes and ensuring resiliency to "crashes" either at the workstations or at the superminicomputer); the design librarian (supporting check-in/check-out of design parts from the database); the validation component (checking that design constraints remain in force after a change); the design transaction component, using the recovery subsystem, the design librarian, and the validation component to control the creation of new versions of data objects and the browser (providing an interactive front-end for creating and viewing the data structure). The database system combines design tools, project management tools, and recalls pieces of design and validates correctness. The project management tools assist in planning the implementation effort. The design database management system is responsible for structuring the design and exploiting the structure to keep the total design consistent.

Artificial Intelligence (AI)

Artificial Intelligence will be extended to databases in future design systems. For example, a self-adaptive simulation database would learn from characterization of presimulated circuits. As investigations of physical circuit implementations feed actual performance data back into the design system, the AI database

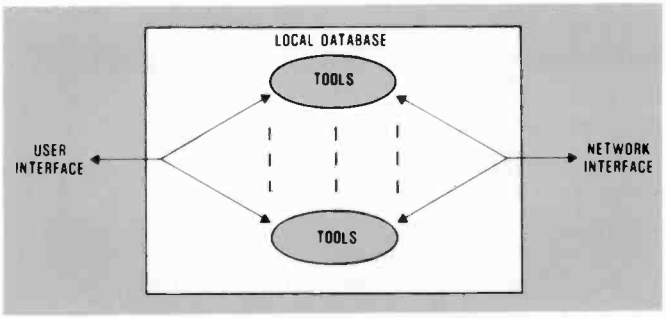


Fig. 3. *Workstation-standardized interfaces will allow intertool communication and allow tools to be accessed either by the network or by the user interface.*

manager would compare actual and predicted behavior. Then, the design system will automatically correct simulation models to minimize future discrepancies. Adaptive databases will also configure specific tools for specific designers. Presently, many design automation programs support a range of menu and setup options, requiring users to spend considerable time and effort configuring tools before they can do valuable work. Adaptive databases will also learn the user's preference and store setup parameters within specific design files.

Project management tools

The present problem facing the manager of large team efforts involves partitioning a design and assigning individual tasks, cross-checking and integrating separately developed pieces, controlling access to the project database and managing its content, enforcing design standards and methodologies amongst team members, and monitoring the overall progress of the design. It is the responsibility of managers to establish clearly defined forms for project documentation. At the outset of design projects, managers can delineate those issues that must be addressed in design documents; automated design tools can then monitor the completion of documentation forms, preventing design storage until all forms contain at least some text.

The recordkeeping will be made transparent to the design system users. Documentation can be added to drawings, component-library elements, and software modules as an attribute. Thus, recordkeeping becomes an integral part of the design database and users add new designs as they specify components or new software modules depending on the application. By providing on-line documentation aids, automated tools can subtly force designers to record their activities and explain their design without interfering with the productivity and creativity that future design automation tools promise.

Below is a list of some of the automated management tools that will be incorporated into the design system:

- Automatic separation of information according to type, version and variant
- Controlled access of the information
- A guaranteed audit trail for software for all information (what changes were made, by whom, why, when)
- Document grouping to form libraries
- Version and release control routines
- Automated PERT, CPM, and GERT modeling routine
- Report generation

- Transparent recording of design and analysis transactions
- Electronic mail utility
- Capability of obtaining printout or plot of all relevant management and design documentation

Aside from the mentioned tools, there will exist management tools that will automate the tracking of product status and associated warning tools that will continuously compare activity status in real-time against present activity parameters, alerting the project manager when activity levels (such as time to complete) exceed the parameters.

Superminicomputers and the automated software support environment

The superminicomputer will primarily be used for software design and development purposes via an automated support environment (aside from hosting secondary storage, the project control database system, and project monitoring and control program).

The Department of Defense's Ada® program is a common programming language that can serve as the basis for a common environment. The Ada program has adopted the concept of a common automated support environment into which automated tools may be conveniently installed. Through a community-wide interactive process, the STONEMAN requirements definition for a system supporting work in the Ada language was evolved, which defines an Ada programming support environment (APSE) built upon common interfaces and data representations for automated tools.

Due to the DoD's commitment for Ada, I believe the STONEMAN requirements presently offer the baseline concepts for tommorrow's future host software development environment (see sidebar on APSE). The purpose of the APSE is to support the development and maintenance of Ada application software through its lifecycle. It will also promote portability of both user programs and of the software tools within the APSE. The APSE adapts a host/target approach to software construction. That is, a program which will execute in an embedded target computer will be developed on the superminicomputer (host) which offers extensive support facilities. The APSE will provide a well-coordinated set of useful tools, like the workstation tools, with uniform tool interfaces and with communication through the central project database, which acts as the information source and product repository for all designers on the network.

The APSE contains certain characteristics of the design network itself, that is it will be an open-ended system. This will facilitate the development and integration of new tools and it will permit improvements, updates, and replacement of tools. The APSE will support at a minimum:

- Text manipulation
- Requirement specification
- Overall system design
- Program design
- Program verification
- Project management
- Cross development for target system
- Documentation system
- Project control system
- Configuration control system
- Measurement tools
- Fault report system
- Libraries
- Object importers (to support other languages, like PASCAL, FORTRAN)

User interface

The design system will contain an easy-to-learn, easy-to-use, powerful, consistent user interface with rapid and complete data access capabilities. The user interface will support a wide range of design styles via the use of artificial intelligence. These interfaces will "learn" user's needs and habits. The design system could then track designers progress along learning curves and provide custom-tailored command-entry formats as individual users become accustomed to tool characteristics. Such intelligent interfaces will also learn user's habits, recording and providing menu items only for most frequently used and forgotten commands. Moreover, the design system would calculate a time-dependent regression factor for each user, automatically compensating for the effects of time spent away from specific tools. The system will also keep track of what project was last worked on, and when, and will automatically return to the last-referenced design step.

A graphics screen and keyboard will be the primary user interface, with a touch-screen mode as an option for some operations. Multiple windows may be opened on a single screen, moved about, and enlarged or shrunk as needed. The system workstations will contain context-oriented *help* functions that will provide guidance and explain errors.

Benefits of reconfigurable architecture

One of the major characteristics of future engineering design systems will be inherent flexibility due to a standardized reconfigurable modular architecture. Major benefits can be obtained: technologically independent tools, technology insertion, and the ability to configure the design system according to the design application and phase.

With the present effort of standardizing microcomputer buses, the hardware architecture of most workstations will allow them to add on new tools and capabilities via the use of plug-in modules in an expansion chassis. Also due to the present acceptance of a de-facto operating system standard, UNIX, device drivers that will be needed in order to add new tools to a workstation would be readily available. An operating system standard will promote design tool portability.

Aside from the standards mentioned above, most importantly there will exist design tool standards that define the means for transmitting data from one tool to another. Such standards will allow tools to be highly integrated and free designers to investigate alternative tool sources.

Presently these types of design tool standards are not available but, through cooperation between workstation vendors, instrumentation vendors and silicon foundries, standardization at the design description level will materialize. With these types of standards, a workstation can be easily configured to behave either as an IC-design station, PC-board design station, or a hardware/software development system.

The tools supported by the APSE, will be portable to other host computers due to the KAPSE. The distributed processing afforded by an LAN will also provide a measure of obsolescence. Presently, LANs are gaining wider industry acceptance and through the efforts of the IEEE-802 committee and the International Standard Organization, LANs will be the standard information bus of future automated design systems. Newer workstations or superminicomputers can be added to replace older ones as required with minimum hardware and software impact. The other benefit of a LAN is that, with the use of

Enrique Melendez joined RCA in 1977 as an engineering co-op student while attending Northeastern University. He earned a BSEE degree (*magna cum laude*) from Northeastern University in 1981. Enrique enrolled in RCA's Corporate Graduate Study program and received his MSEM from Northeastern University in 1982. He will be awarded his MSCS from Northeastern University in June 1984. Since joining RCA, he has worked on microprocessor hardware, software designs, and IR&D projects in the ATE field. Presently, he is working on LAN communications software for the next generation of ATE.
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gateways, the design system can be tied to other automated design systems that may exist at remote sites.

Conclusion

As new automated design tools become available, it is important that design engineers study their respective applications to see what tools they may require. Likewise, after examining the complete design cycle requirements, design managers should decide on tools that will not only fulfill the design and development requirements but also the project management requirements. In this context, the future design tools must be easy to use, configurable, and must have standardized (network, user, database) interfaces. By incorporating this flexibility, the design team will be able to explore and create a class of proprietary tools. This is an important factor if, as predicted, CAE tools saturate the market. Unless a company has developed its own proprietary tools, they will be forced to compete with the same tools that its competitors have. As a result, the creativity and innovative use of these tools by design teams will play in the future an even more important role.

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C.A. Burton

Choosing a CAD system

RCA Government Communications Systems realized that before they could use a CAD system effectively they had to make the right buying decision. Here's a look at that process.

Combine the wide variety and increased complexity of work being done at RCA with the intense competition in the electronics industry. The result is that RCA must use every advantage available to stay in the mainstream. One of the more important recent developments in the area of new technical design tools has been the computer graphics design terminal. To stay competitive, RCA must implement the use of computer-aided design (CAD) terminals in the areas of engineering design, analysis, and drafting. But the first question to be answered is: "Which system to buy?"

RCA Government Communications Systems (GCS) recently went through an extensive benchmarking procedure for the selection of a mechanical design turnkey CAD system. Outlined below are some of the major areas we investigated with each CAD company under consideration. This information should help increase awareness of the important issues during the selection of a computer graphics design system. Although these techniques were used in the selection of a CAD system, these same investigation techniques could also be applied to other tradeoff studies in advance of a major equipment purchase.

Abstract: *RCA Government Communications Systems, in an effort to strengthen and upgrade their computer-aided design capabilities for mechanical engineering, recently completed a benchmarking project for the evaluation of five vendors' systems. The techniques used are described here in general terms because they could apply to other engineering equipment evaluations. Sidebars throughout the article give specific details on the actual work evaluation and equipment at GCS, leading to the selection of Auto-Trol CAD equipment.*

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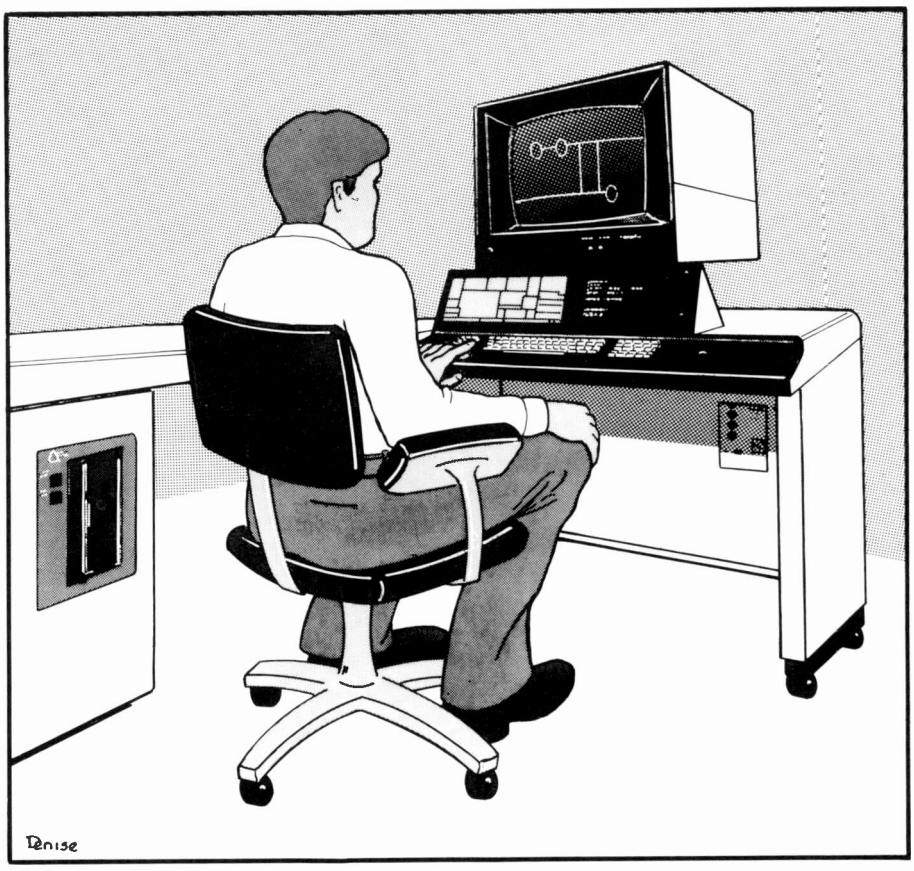

Beginning

The first task undertaken was to outline in detail the long-term and short-term requirements of the system to be acquired. The variety of turnkey systems available today is astounding, but few are suitable for every application. Each product will usually show a specialization or concentration in one or several areas of expertise (that is, PCB

GCS's mechanical CAD choice

A benchmark of mechanical CAD systems was performed from September 1982 through February 1983. Originally, two vendors were to be investigated, but before the benchmarking procedure got into full swing, the view was expanded to include five additional companies. The company chosen to supply mechanical CAD systems to GCS was the Auto-Trol Technology Corporation.

The first Auto-Trol equipment for GCS was delivered in mid-September of 1983. RCA's system consists of three Advanced Graphics Workstations (AGW), a magtape unit, a TI line printer, and an HP7580B plotter. Three engineers and four draftsmen/designers have been trained to date on the system. Training has included two weeks of basic operator's training, three days of finite-element modelling, and three days of Fortran interface use.

Currently, two terminals are operated on a two-shift basis for drafting production work. Production work on the terminals was started in November of 1983. The third terminal is for engineering analysis, development, and system management.

A variety of projects have been handled including two-dimensional detail drawings, three-dimensional modelling, flex cable development, finite-element analysis, mass properties analysis, and clearance analysis. Further development work is planned in finite-element modelling and analysis, three-dimensional modelling, and mass properties calculations. In addition, factory automation and MIS interfaces are planned for development. The emphasis will be on integrating all areas of design, analysis, and production through the use of the Auto-Trol workstations.

design, IC design, two-dimensional drafting, technical illustration, and so on).

In addition, different companies are at different levels of development in these areas of expertise. For example, an extension of mechanical CAD is the development of numerical control interfaces. Some companies have expanded into this area, while others have limited their commitment to strictly drafting and documentation functions. If factory automation interfaces are unimportant to you, or if you intend to develop them in-house, this will affect your selection of CAD vendors to be considered.

Other applications that should be considered before initiating an investigation are finite-element modelling packages, flat-pattern development, solids modelling, pattern nesting, and so on. All possible applications that may be required of the system, short-term and long-term, need to be addressed prior to focusing on several vendors for the investigation.

Some systems will be good at accepting user-developed automated routines that can customize the system. Others may have hardware that allows the use of many third-party-developed software packages to enhance the system. Therefore, the amount of in-house development to be committed to the CAD area is an issue that must be decided in order to focus the benchmark investigation properly.

If there is more than one type of application for CAD in an area, there are two options for filling those needs with CAD terminals. One is to choose a system that can satisfy both needs. By doing this, training needs are simplified, a working knowledge of the system can be shared, and direct interfaces for transmitting information are readily available. The result of such a decision is that one vendor will probably not be the best for both applications. Therefore, capabilities in one package may be sacrificed in an effort to gain these advantages in system commonality. In such situations, more commitment to system customizing, whereby automated routines are developed specifically for in-house use, may be required.

The other school of thought seeks to choose the best system for each application and, if necessary, develop interface links in-house or use translation languages such as IGES, an all-purpose graphics language, to allow the two systems to interface. GCS has chosen to purchase the system we believe is the best for a particular application and to handle interface operations separately. GCS decided that contending with the added complexity of training needs was worthwhile, in order to have the best package in an application area. The decision became whether or not to devote effort to developing interface capabilities or to customizing the system.

The benchmark

One of the most important aspects of the data collecting/decision-making process is the execution of a typical application by all competing vendors. The best test of a system is a significant exercise as close as possible to the customer's actual work.

This benchmark project was a requirement for considering a company as a possible supplier of CAD terminals to GCS. Although a lot of companies do not want to spend the time and effort a true benchmark effort takes, the response to GCS's invitations to compete in the benchmark competition was very good. As soon as one company agreed to do the benchmark project, others joined suit and made the commitment to show their capabilities by executing a controlled, timed benchmark project. The CAD industry is very competitive and with a big name like RCA, the implications are enough to really intensify the competition.

In choosing a benchmark project, it was important to consider the type of work, the time involved for the vendors to complete it, and the availability of data for comparison to manual effort. Much of the mechanical work at GCS involves the design of sheet-metal housings and drawers for electronic equipment. Therefore, this type of design was chosen for the benchmark (Fig. 1). Care was taken to include as many typical aspects of the work done at GCS as possible. The mounting of electrical components is a common occurrence in designs, and therefore was included in the requested benchmark design. How each vendor handles the creation and implementation of standard components in a design was watched carefully for its contribution to better efficiency through the use of CAD.

The benchmark project used by GCS to test mechanical design systems was one that had been done previously by a designer on a drafting board and, therefore, the times required to complete the design on the drafting board were known. These times, along with the CAD vendors' estimates of productivity enhancement ratios, allowed an estimate of the time that was required by each vendor to complete the design on their company's system.

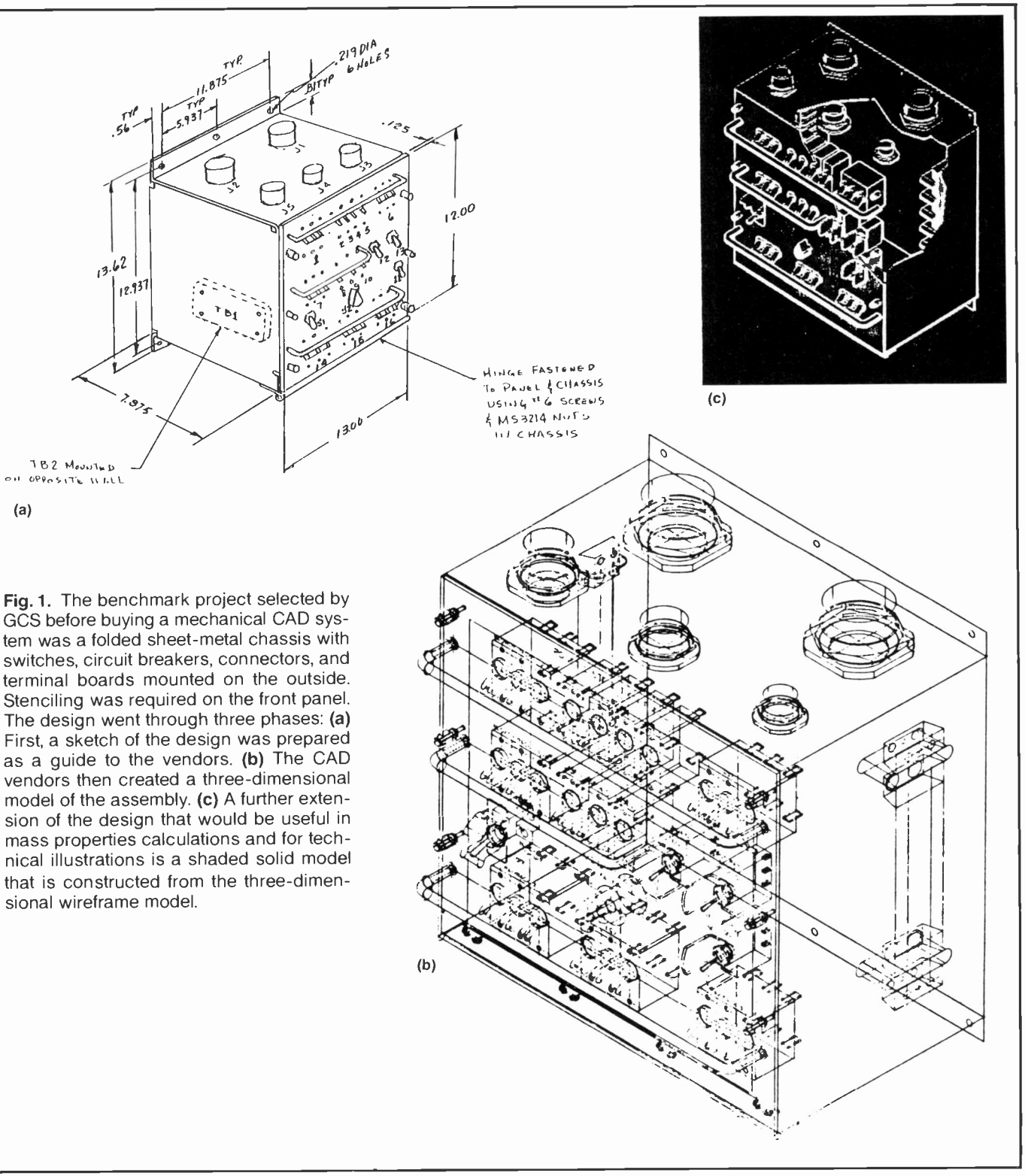

Fig. 1. The benchmark project selected by GCS before buying a mechanical CAD system was a folded sheet-metal chassis with switches, circuit breakers, connectors, and terminal boards mounted on the outside. Stenciling was required on the front panel. The design went through three phases: **(a)** First, a sketch of the design was prepared as a guide to the vendors. **(b)** The CAD vendors then created a three-dimensional model of the assembly. **(c)** A further extension of the design that would be useful in mass properties calculations and for technical illustrations is a shaded solid model that is constructed from the three-dimensional wireframe model.

For each competing vendor to have an equal chance in completing the benchmark project, all the pertinent data (general guidelines and requirements, a parts list, a sketch, and component specification sheets) were accumulated into one package and thoroughly reviewed for completeness. This same package of information was given to all vendors involved. Every effort was made to make available information comparable to that which is available to a designer at GCS.

One specific contact from GCS was assigned to follow the benchmark project and to field any questions that arose concerning the design. This simulated the engineer/designer relationship that normally exists on a project and allowed a better view of how projects would actually proceed on a normal basis using the system.

As much of the actual work was observed as was deemed practical. Each vendor usually did some preliminary work ahead of time, such as creating patterns

Geometric construction capabilities

The following is a list of features that contribute to the construction capabilities of a system. A brief explanation is given of each for those unfamiliar with the language of CAD.

Separate Drawing/Model Modes—This allows separation of the three-dimensional model from drawing entities such as notes and dimensions.

Independent Construction Plane—Also referred to as working coordinate system, this allows entities to be added using more than one coordinate system.

Number of User-Defined Views—A system will usually define a certain number of standard views, but will allow the user to define additional ones, hence, user-defined.

Number of Working Views—This is the number of views that may be displayed at one time.

Limit on Model Size—Most systems allow the file size to be limited only by system disk space, but some have smaller limits.

Use of Grid—The use of a grid causes entities to "snap" to grid points and therefore adds a guide for locating entities quickly, yet accurately.

Number of Levels—Levels can be likened to sheets of Mylar, containing entities, which can be viewed in any combination.

Color Definition—Color usually is defined by levels, component type, or entity number, or a combination of these.

Offset Capability—This provides a quick method of copying geometry that needs to be duplicated a specified distance from the original entities.

Surface Generation—Surfaces are an extended application of three-dimensional modelling. It is particularly useful in checking interferences.

Cross-sectioning—If a particular piece of geometry is surfaced, a spline can be generated automatically to represent its cross-section at a certain depth.

Automatic Hidden-line Removal—Used in three-dimensional modelling to make views of objects that look like the solid object would look.

Dynamic Capabilities—Dynamics allows the user to move objects interactively on the screen.

Edit Versus Reference Levels—A method of identifying a set of entities on specified levels, which can either be tagged as changeable or not.

and storing them, and practicing the techniques to be used in the design. Most of the actual design work in each case was observed live.

To compare the vendors on a common scale, all the circumstances that could affect the completion times and quality of the design work were documented. Such circumstances included the experience of the application engineer executing the design, his (or her) background, the type of terminal used in completing the design (versus the type of terminal that would be purchased), the load on the system during the benchmark work, and the amount of actual work completed. Some of the vendors did not complete all of the requested work, but were able to complete enough to allow a realistic determination of the actual time it would have taken. Others did more than the required design, such as adding extra notes or providing an isometric view of the design. All these factors were noted and taken into account. An effort was made to adjust the completion times to reflect the effects of these factors. Although this gives a somewhat subjective result, it is more realistic than ignoring the unequal circumstances altogether.

Demos

Another method of seeing what a particular system can do, one which is a favorite of most CAD vendors, is that of demonstrations, or demos. Most likely the companies will have certain "canned" demos ready to show. These are usually impressive, but they sometimes will give a false impression of the ease of accomplishing certain tasks with the system. Companies rarely show any demo that would reveal system limitations or awkwardness. To see a more realistic view of the particular system, a method was employed to force the vendor into demonstrating the system live.

Several small, typical design tasks, which normally could be done in an hour or two on the drafting board, were outlined. Times were arranged to have these demonstrated, but the outlines were not given to the vendors ahead of time. This prevented any advance preparation and forced a live, realistic demonstration of the system. Some software bugs, which were conveniently avoided in a canned demo, surfaced in a live demo such as this. All CAD software packages have some bugs, but it is important to make sure they are limited, are ones that can be worked around, and that the vendor, when made aware of them, will respond to correct them. When such bugs surfaced, the vendor was asked to check them out and tell us whether they were bugs they were aware of and what their action concerning them would be. This allowed a first-hand view of the vendor's customer response.

Talking to users

We talked to users of the different systems—this proved to be an interesting and surprising part of the system investigtion. First contacts can be made through the vendors, but by virtue of what they are trying to accomplish, they are only going to supply the names of contented customers. The best source of vendor users is a complete list of the user's group members from either the vendor or the user the vendor referred. Then, by a random selection of users, a more honest impression of the vendor can be obtained. A lot of times the users will be divided into groups categorized according to industry. This allows identification and contact with users with similar applications.

Questions posed to the users included:

Drawing/dimensioning capabilities

An important aspect of any CAD system is the ease with which drawings can be made. Listed below are features that contribute to that ease.

Automatic Dimensioning—Entities can be identified for dimensioning and the system automatically measures the distance and inserts it in the dimension.

Automatic Update of Dimensions—If the entities that are dimensioned to are moved or changed, the dimension will automatically be updated.

English-to-Metric Conversion—This is the ability to change a drawing that was dimensioned in one system of units to the other.

Geometric Tolerancing—The capability to dimension using geometric tolerancing methods is becoming increasingly important.

Calculation of Tolerance Buildup—Automated routines can be developed to calculate the tolerance buildup in a certain area.

Exploded Views—A certain area oftentimes will need to be blown up in an exploded view to show detail. Automatic capability helps greatly.

Text Fonts—The kinds and number available help to enhance the appearance of a drawing.

Number of Line Weights—Different thicknesses of lines often need to be shown. It is a convenience to be able to assign them automatically.

Enhanced productivity features

Features that add to the speed and efficiency of the system are the ones which allow the system to pay for itself. The features that GCS noted as enhancing design work with CAD were the following.

Menu-driven—Menu-driven systems allow the user to make choices from a displayed menu and therefore are very easy to use.

Display Tolerance—Even though curves and surfaces may be defined exactly, rough approximations can be used for display to speed up repaint of the screen.

Interruption of Commands—If a command takes a long time to execute, and is initiated by mistake, it is beneficial to be able to interrupt it.

Measuring Capability—This is the ability to have the system measure distances as would be done on a drawing.

Calculator Mode—Most systems will allow the user to calculate values as on a calculator.

Sketch Mode—Control of the cursor to sketch freely on the screen adds flexibility to the system.

Command Log—A record of all operations executed are stored in a file and can be "replayed" as with a tape recorder.

Programming—The ability to interface to the graphics capabilities through programs adds to automating certain routine procedures.

On-line Documentation—Time is saved when command usage information is provided on the system as well as in manuals.

Plot Queue—A plot queue stores plot files so that a graphics terminal is not tied up when plotting is being done.

Tablet Symbol Recognition—This is a type of command execution where the system will recognize symbols drawn with the cursor and execute the corresponding command.

Why did you select this particular vendor?

What is the response of the vendor to service calls?

Have a significant number of bugs been encountered in the software?

How big a system do you have?

How long have you had the system?

What types of applications do you run with the system?

Most users that were contacted were willing to discuss any issues concerning their system. A few questions were all that were necessary to start the flow of information. CAD/CAM is such a new field that those involved are usually excited and proud of what they are doing. Much insight was gained by talking to users of the competing vendors' systems.

Some of the best sources of CAD users are within RCA itself. Different divisions of RCA are using systems supplied by Applicon, Auto-Trol, Medusa, Computervision, and Calma among others. The work done by one division in an area, such as CAD, can and should be used by other divisions for the advancement of the company. Some of the other CAD users of RCA are Astro-Electronics Division, Missile and Surface Radar, Broadcast Systems Division, and the Laboratories. Useful information was obtained from the other CAD users in the company, resulting in a significantly less difficult decision-making process.

Hardware features

Most of the features readily looked at on a CAD system are software-related. To ensure the best implementation of the software, good hardware is also a must.

Screen Resolution—This parameter dictates how accurately lines, arcs, and splines will look on the screen.

Number of Colors—Most systems can only display a certain number of colors at once.

Size of Buffer—The buffer stores commands if the operator types faster than the system can execute and executes them in the order entered.

Number of User-defined Menus—Menus are sets of user-defined macros (sequences of commands). Usually a menu is created for each type of application.

Remote Diagnostics—Some systems provide diagnosis of system problems via a phone modem, saving the number of service calls.

Intelligence of Terminal—Some terminals have computation power that offloads the CPU and enhances performance.

Type of Cursor Control—Cursor control is usually accomplished with a joystick, thumbwheels, a digitizing pen, a light pen, a mouse, or a touchpad.

Separate Numeric Keyboard—A separate numeric keyboard provides for easy entry of numeric values.

Screen Adjustment—To provide a comfortable working environment, a screen that swivels or adjusts in height is a nice feature.

Separate Alphanumeric Screen—To display the commands executed, some systems provide a separate alphanumeric screen, whereas some combine it with graphics.

Turnkey—A total system package—hardware, software, and support—is called a turnkey system.

Stand-alone—A stand-alone system is self-sufficient. It has its own CPU and does not affect the work of any other terminal.

Analyzing features

Once the actual data collection began, objectivity was the most important quality for the investigator to have. Many times the opinions of management or the views of the company on specific concerns will change in the course of the investigation. Collecting the information as objectively as possible allowed more flexibility when the decision process actually began.

The procedure used by GCS in accumulating decision-making data on all the vendors was to make note of every feature each system had. This entailed time-consuming visits to each vendor, to watch work in process, or to work on the system personally. The benchmark project itself provided an excellent mechanism for gaining knowledge about a system. During the GCS benchmark, approximately two working days were spent with each vendor observing the benchmark design in progress. Extensive notes were taken on everything imaginable—design approach, hardware features, line-font capabilities, cursor-control mechanism, number of colors for display, dynamic capabilities, and so on. After visiting all the vendors the first time, an accumulative list of features was developed. The major features were divided into four categories: geometric construction capabilities, drawing creation/dimensioning capabilities, enhanced productivity features, and hardware features. Some of the features noted about one vendor may not have been investigated with another. Therefore, by accumulating the list of features, second contacts with each vendor were made in order to clear up all issues with all vendors.

After all the information had been collected and tabulated, it was condensed to a number of issues considered important. GCS had ten major issues that it felt were important in choosing a CAD system. The three most important issues were speed of the system, geometric construction capabilities, and reliability of the system. The next two areas of concern were dimensioning capabilities, and the ability to customize

Cindy Burton is a Mechanical Engineer who has been with RCA almost two years. She began her work at RCA in the Applicon printed wiring board design facility, working as a printed circuit board design consultant and as a computer graphics development engineer. As a result of her benchmarking effort and the acquisition of three Auto-Trol mechanical design terminals, she has taken on the role of Lead Development Engineer in the Mechanical CAD area.

Ms. Burton received her BS in Mechanical Engineering from Ohio Northern University in 1980. Prior to coming to RCA, she held a position of Mechanical Design Engineer with Westinghouse Corporation in Lima, Ohio, where she worked on the design and analysis of generator and motor housings for aircraft electrical systems and related applications.

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the system. Of next importance were surfacing capabilities, the ease of use of the system for casual operators, and hardware features. The final group of issues involved available training and the aesthetics of the terminal layout. Each group of issues were given a different weight between one and four according to their importance to GCS management in deciding on a CAD vendor.

Each vendor was given a rating from one to ten for each issue (such as geometric construction capabilities, hardware features, and so on). According to how they were judged in each compared to the other vendors. These ratings were based on the list of features accumulated and tabulated during the benchmark and demos. Then the vendors were each given a weighted score for each issue, which was obtained by multiplying the one-to-ten ratings by the weight of importance (a number between one and four) for each issue. Total weighted scores were then calculated for each vendor and used as a major indication in determining the best system for GCS's use.

By analyzing the systems in this manner, the information that was collected can be used, even if views or intentions change, merely by choosing different major issues or assigning different ratings for them. It may also be desirable to look at the data under several different priority arrangements for the issues in order to get a broader picture of how the systems compare.

Conclusion

One of the key factors in being satisfied with a decision or a purchase is assurance that the investigation was thorough, so that the buyer does not see a better system two months down the line. The whole benchmark and investigation procedure was an eye-opening experience. GCS obtained a broad picture of what is available from the turnkey CAD industry market. Although the technology itself is changing rapidly, GCS is satisfied that the system chosen was the best available, at the time, to fit their specific needs.

W. Carey

The MSR local area network

A local area network of computers, terminals, and peripherals now in place at Moorestown has greatly amplified the service of the Missile and Surface Radar Development Facility and the skills of its users.

This article describes the origins of the present computer network system associated with the Missile and Surface Radar (MSR) Software Development Facility at Moorestown, N.J. The present configuration of that facility was described in a recent article by Liggett.[1] A systematic, integrated combination of hardware, software, and firmware provides a cohesive, reliable, data-communication network that meets engineering communications requirements. This network is based on three principles: network transparency, virtual-circuit switching, and centralized network control.

Background

In 1980, RCA Moorestown established a software development facility (SDF) designed to house all the processors involved in software development (Fig. 1). The computing power represented by the machines in the SDF was at that time sufficient to meet all MSR requirements.

A terminal room that could house as many as 20 terminals was set up adjacent to the SDF. The number was chosen to minimize both the expense involved in setting up the linkages and the waiting time required for access to any particular system. Although the number 20 still holds, unanticipated requirements soon created doubt as to the advisability of having a single terminal room servicing all programmers.

First of all, as the number and variety of projects increased, locating all involved people within reasonable walking distance of the terminal room became impossible. MSR is a widely dispersed organization, and programmers and engineers who use the system for development work are stationed in all parts of the complex. Some users would find themselves walking as much as a quarter mile through inclement weather to get to a point from where they could access the computers.

Furthermore, many in-house projects require operations to be performed on different systems. A user might need one terminal for part of a particular application, and then a different, and frequently

Abstract: *A growing organization with an increasing number of buildings in the Moorestown area, RCA Missile and Surface Radar faced the problem of making its computer facilities available to the greatest number of users with the least amount of access effort. The local area network precludes the need for acquiring additional computers by making more efficient use of existing systems.*

Terminals operating at 2400 baud are connected via lines and trunks from the network processor and network control console to the VAX 11/78s, PDP 11s, Eclipse, and Novas in the Software Development Facility.

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Fig. 1. *MSR's Software Development Facility is dedicated to supporting the development and test of software systems.*

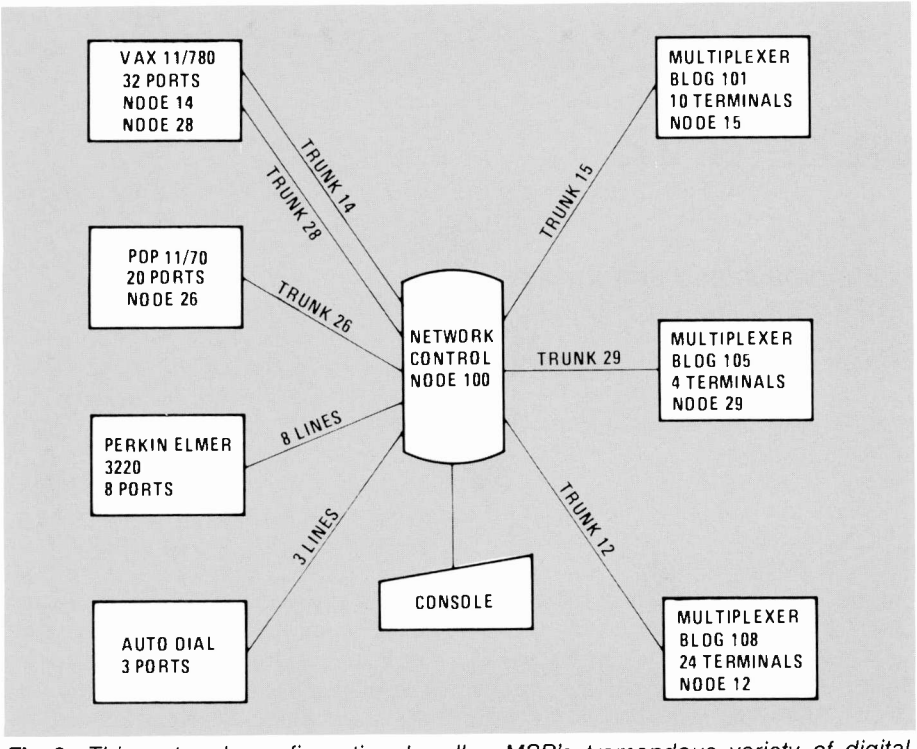


Fig. 2. *This network configuration handles MSR's tremendous variety of digital processing tasks.*

busy, terminal to complete his task. The frustration factor could be excessive.

In some cases a program must be entered and compiled on one host, then transferred to a different host for debugging and/or execution. Transferring of the programs between hosts was done by magnetic tape or floppy discs, and necessarily involved going into the SDF room and physically handling the hardware, sometimes with catastrophic results when attempted by personnel unfamiliar with the system. The growth of the number of personal computers and home terminals had also spurred requests for access to the mainframes over phone lines. With the dedicated terminal approach, such access had to be denied.

By 1983, the use of digital processing on various Missile and Surface Radar projects had multiplied. Not only had the number and variety of computing systems—micro, mini, and midi—expanded dramatically, but hardware and software documentation was now being included on the discs and tapes associated with the systems. Thus, in addition to the conventional users, secretaries and stenographers were extending use of the system for word and text processing. MSR faced the choice of either greatly expanding the number of processing systems, or making far more efficient use of the existing systems. Networking was an attempt to implement the latter approach.

Selection criteria

MSR issued a request for proposal describing our problem and a general approach to the solution to a dozen potential suppliers. Our hardest task was to decide which of a number of technically excellent replies was the best. To that end, MSR established a set of selection criteria that each proposal had to meet to qualify for further consideration.

Basically the proposed arrangement had to provide

- A means for accessing computers in the SDF from anywhere in the MSR complex.
- A means whereby a single terminal could access any of the resources in the SDF.
- These capabilities in a manner that made the network transparent. The fact that the switch was between the terminal and the computer should be undetectable.
- These capabilities without the use of mechanical switches. The network *must* establish "virtual" circuits; that is, circuits which have no physical existence, but which exist only in the memory of the network.
- Control over the network from one central location, which could permit or deny access of specific terminals to selected resources.
- The ability for data to be interchanged between computers without the use of external media, and at the command of the user (this capability might be limited to ASCII data with no penalty).
- The capability of dumping data to remote printers.
- Some communications capability via common carrier, as opposed to leased telephone lines.
- The ability to dial out from a terminal or a computer and to treat incoming calls as coming from terminals.

Selected system

Although none of the proposals fulfilled every requirement in every detail, the system made by Digital Communications Associates, Inc. of Atlanta was selected. The original configuration of the system is shown in Fig. 2.

The network processor and the network control console are physically located in the SDF, near the computing systems with which they interface. The role of the network processor is to accept traffic from lines and trunks and, by examining destination tags on the incoming information, send it to the correct line or trunk.

In the current context, a trunk is a communications link that can carry information destined for two or more ports. Hence, the link between the network processor and the PDP-11/70 is a trunk, since it can carry information for up to 16 ports on the PDP-11/70. The links between the Perkin-Elmer and the network processor are not trunks, since each is dedicated to a specific port on the Perkin-Elmer.

Installed in the VAX and the PDP-11/70 are boards, built and supplied by DCA, which create 16 ports on the host computer. That board communicates with the network controller via a single 9.6 kbps trunk. Two such boards are installed in the VAX and one in the PDP-11/70.

Three pairs of modems were included in the system for long distance (up to a quarter mile, in this early system) communication with remote multiplexers. These modems supply full-duplex communication links over distances that digital signaling could not handle. Each one accepts digital input at one port, converts it to phase-encoded information, and ships it to the trunk. It also accepts phase-encoded information from the trunk, converts it to digital levels, and sends it to its local host, which is either the network processor or a statistical multiplexer.

The statistical multiplexer is a purely digital device which interfaces with up to

32 terminals, and allots each one a portion of the multiplexer's total bandwidth, as determined by that terminal's immediate needs relative to the rest of the terminals. Through modems, the network processor drives remote statistical multiplexers, each of which interfaces with terminals that are relatively local. The network processor also interfaces with the RACAL-VADIC telephone line interface unit which (1) accepts incoming calls and routes them to the network processor, and (2) provides an out-dialing capability so that a terminal of a computing system may dial out to a remote location.

Installing the system

Installation of the computer network system was performed by a team of both RCA and DCA personnel. The system was installed in two steps—the first step consisting of testing each interface without actually "switching to traffic," and the second step consisting of the final installations and a night-time switchover so that users were relatively unaffected by the change.

As expected, most of the problems arose in the first step. The majority of these problems came about because of MSR's unfamiliarity with switching systems of this nature. We found for instance that, in every case, the operating systems that were intended to work with the switch were improperly generated and had to be redone. These problems and their solutions occupied the better part of a week but, all in all, the testing went rather smoothly. The problems associated with running all the necessary cables occupied most of the next week, and these problems were of course strictly internal to RCA. DCA had no part in them.

Operational experience

The very first user reaction to the terminals on the switch was one of resistance and grumbling because these terminals, in order to increase their total number, were being operated at 2400 baud rather than at 9600 baud.

However, the engineers rapidly discovered that the convenience of a terminal a few steps from their desk was far greater than the (mostly illusory) value of the four times greater data rate, which could only be used in one direction and at infrequent intervals. The switched terminals were soon used far more heavily than those in the terminal room.

Whether productivity has measurably increased is a debatable point, since we have never had an adequate measure of programmer or engineer productivity. But there can be no doubt that morale has increased, simply because use of the system is more convenient, and because frustrating delays in gaining access to a terminal are far less frequent.

Capabilities and expectations in a product development

Environment

The initial concept of the Software Development Facility was as a tool for the creation and maintenance of deliverable software. An ancillary application was for the development and support of a limited number of utility programs to be used primarily by software engineers for the purpose of expediting the development of software. Such programs as special-purpose editors, disc and tape utilities, and indexes of existing software fall into this category. The initial concept expanded rapidly and almost from the first day of operation, additional computing loads have been placed upon the facility. The number and type of additional tasks are listed below.

Computer-aided design

With the use of microcomputers in all facets of MSR products, we find ourselves frequently tailoring a microcomputer instruction set to a specific application. The hardware configuration designed to implement the instruction set is fed into a software-implemented logic breadboard via a special algorithmic language, and the program tests the configuration against a standard. Any errors in the design are flagged, giving the engineer an opportunity to correct them before the hardware is built.

Cross-assemblers, compilers, and linkers

A variety of these have been made available. In general, they implement their assigned function while running on one of the larger machines and create output to be used by a small minicomputer that is not a part of the SDF, or by a microcomputer that is a part of deliverable equipment.

Simulation

An array of simulators has been incorporated into the available software of the SDF, ranging from simple, but nontrivial digital filter simulators to an expanded version of the General Purpose Simulation System.

Documentation

MSR is moving toward the preparation of all documents on word or text processors. This includes proposals, reports, specifications, and even this paper. Since dedicated word processors are scarce, the tendency has been to obtain software which runs on one or more of the SDF machines, and create and edit the documents from a terminal. It is becoming more and more common to see a secretary or a stenographer sitting at a computer terminal and using it as a typewriter. By the summer of 1984, most secretaries will have desktop terminals that will be used far more often than their typewriters.

Education

Not the least of the SDF applications is educating both MSR personnel and others in the use of computers. In-house courses on programming are provided for MSR personnel, and the SDF computers are also used for educating special groups such as the Boy Scouts.

Each application has its own peculiar software and user requirements. Secretaries do not use complex operating procedures, simulation users do not need the detailed operations involved in a compile and link task, and we certainly cannot expect Boy Scouts to be sophisticated users. Hence, support effort directed toward the SDF and its machines has increased along with the work load on the system itself.

A measure of the success of the SDF and its underlying philosophy is the fact that as of now, software users of the SDF almost always outnumber software developers. The application of computers to the design of MSR products is still growing, but is already greater than the effort required to design the software under use. With all the capability we now have, we are just beginning to comprehend that we have made only one small step in the direction of realizing the needs that will become apparent in a very few years. The application of computers and digital logic is still increasing. If MSR is to maintain its position in its chosen field, we must continue to expand our capabilities in digital processing, both as it pertains to deliverable products and to supporting our engineers in all of their manifold specialties.

One thing we are striving for, and prob-

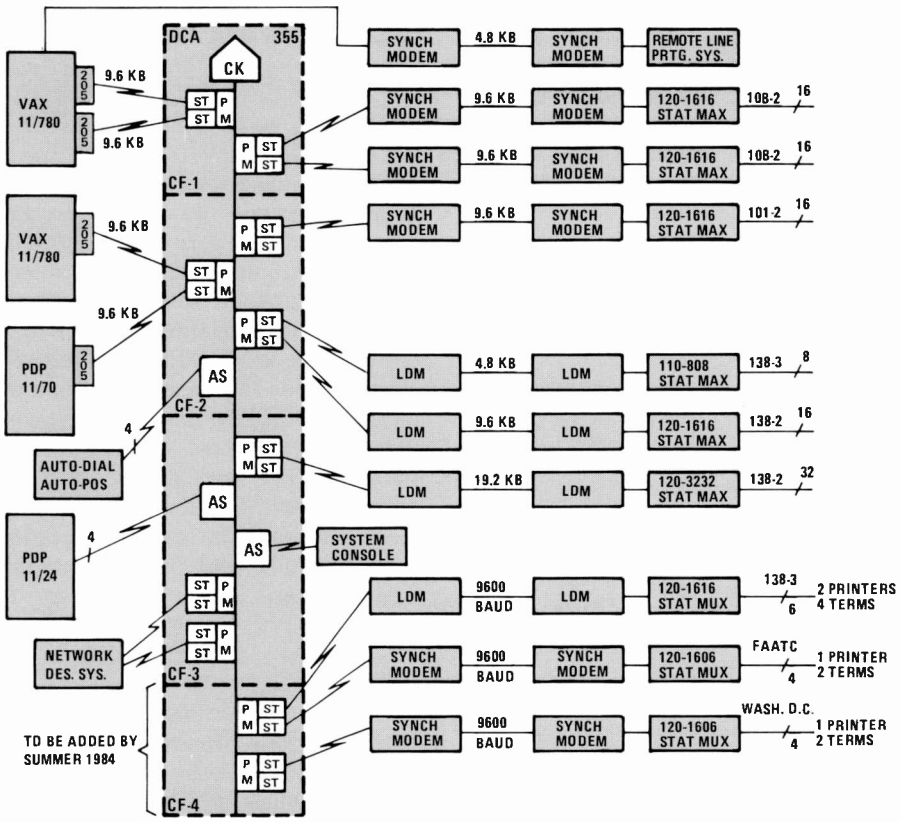
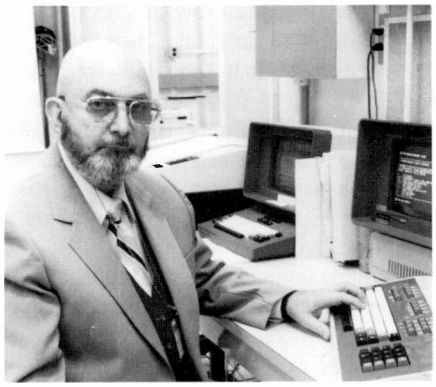


Fig. 3. *MSR Software Development Facility Local Area Network, Buildings 101, 108, 138.*



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ably the most important thing for the near future, is a single operating system language that will be common to all our computers. The two prime candidates at present are UNIX and Ada. Given a single operating system language, the next desideratum is a unified set of programming languages, compilers, assemblers, linkers, translators, and so on. Given that many features of these languages are strongly hardware dependent, we have a great deal of work before us to even define the requirements, let alone implement them.

At present we have, to a small extent, unified and centralized our hardware resources. We would like, some time in the future, to also unify and centralize the human resources required to make SDF a truly general purpose tool. It would be desirable to have a pool of specialists available for the purpose of entering large data bases, of monitoring complex compilations and linkages that require human supervision, and of generally relieving the software engineers of most of their current time-consuming tasks.

A wide variety of currently nonexistent tools will be required to implement our plans. More user-friendly software, especially for the non-expert who currently makes up the majority of the users, is a first requirement. In addition, general-purpose report generators, forms generators, code-to-flowchart translators, documentation aids, indexes to tools, syntax checking software, parsers, and many other items have already been requested and are under consideration.

Of prime importance in this category is a set of configuration management utilities, so-called programmer's workbench programs. These will help us to maintain a complete historical audit trail of all development of, and modifications to, software as it evolves. In a world where software available at a user's terminal can be measured in millions of lines of code, such a service will be indispensable.

Other and more exotic requirements that we hope to realize in the fairly near future include electronic mail service and connection to a broadband net that will allow us to interconnect with other computer systems in geographically remote areas, including probably ARPA (Advanced Research Projects Agency in Washington, D.C.) and several RCA dedicated networks.

Conclusion

The network has proved its flexibility and reliability through four expansions and a major relocation, which involved moving the entire SDF to a building three miles from its original location. In this latter case, the network was taken down, moved, reinstalled, reconfigured, and brought back up in less than twenty-four hours

The Summer 1984 configuration of the network is as shown in Fig. 3. The FAA Pomona, New Jersey and Washington, D.C. nodes are, respectively, 50 and 250 miles from the network processor itself. The traffic is about four times that of the original system, and still the network shows no sign of overloading. We are successfully operating remote printers, and handling dial-in traffic on an almost continuous basis.

The only disappointment so far is the discovery of a fundamental incompatibility between the out-dial hardware and the network as currently engineered. We have not been able to successfully implement the out-dial feature. Fortunately, this is a feature of very limited application.

Reference

1. C.K. Liggett, Jr., "MSR Centralizes Software Development Activities in New Computer Center," *RCA Engineer*, Vol. 29, No. 1, pp. 37-39 (January/February 1984).

S.G. Handman

An attached processor provides calculation speed and accuracy

This powerful new addition to the Corporate computer service will speed the calculation of complex and mammoth mathematical problems.

Engineering and scientific computations may impose special requirements on a computer system—a high rate of throughput for repetitive calculations, manipulations of large arrays of data, precision in cascaded calculations, accommodation of numbers over a large dynamic range, and reasonable ease of programming. These classes of calculations have been limited by the traditional, general-purpose computer architecture. Calculations on arrays of 1024 data points are routinely required and fast-Fourier transforms on 16,000 data points are not uncommon. To a large extent, algorithms for scientific calculations consist of long sequences of additions, multiplications, and multiplication-additions involving real and complex numbers.

Abstract: *Corporate Information Systems and Services (CISS), Cherry Hill, N.J., has acquired a Floating Point Systems 164 attached processor to be integrated with the host IBM system running VM. The FPS 164 was specifically acquired to provide cost-effective processing of large-scale scientific and engineering applications, specifically CPU-intensive vectorizable problems. Working as an attached processor, it can operate in both batch and interactive modes. Topics covered by the author include computer accuracy and speed. Two methods for using the attached processor—Single Job Entry (STE) and Array Processor Executive (APEX)—are described, with examples of pertinent applications.*

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Reprint RE-29-3-7

A computer must be able to manipulate these calculations quickly and accurately to satisfy the needs of the RCA scientists and engineers. In addition to speed and accuracy, these calculations must be performed cost effectively. These calculation requirements have led to the evolution of supercomputers, such as the Cray, and of programmable array processors that can be combined with a general-purpose host to optimize throughput, precision, and dynamic range. To address these needs, CISS (Corporate Information Systems and Services) in Cherry Hill, N.J., has acquired a Floating Point System 164 (FPS 164) attached processor to supplement its IBM general-purpose computing facility.

Accuracy

Scientific computers are measured in both accuracy and speed. In scientific computers, the speed is measured in megaflops (millions of floating-point operations per second). Floating point refers to the binary version of scientific notation. In scientific notation, a number is represented as the product of the mantissa, with a magnitude between 0.1 and 1, and the characteristic, an exact power of 10. Thus, 5068 is represented as 0.5068×10^4. This method is necessary in scientific calculations where the range of magnitudes may be very large. Computers represent this scheme with a binary version of floating-point notation in which the characteristic is an exact power of 2, and the mantissa and exponent of the characteristic are expressed in strings of 0s and 1s (binary notation).

A single floating-point operation can be the addition, subtraction, multiplication, or division of two floating-point numbers to get a floating-point result. Computers, such as the FPS 164 or Cray, are designed for 64-bit (binary digits) processing, thus providing up to 15-decimal-digit accuracy. Such accuracy may be necessary to offset the inevitable small rounding errors that can occur during thousands of iterative calculations.

Speed

The speed of some of the scientific computers is increased where the hardware or software can take advantage of vector processing. In conventional sequential processors, only a limited number of instructions can be performed in a single time slice. Each instruction depends on the completion of a previous step—whether the two processes are interrelated or not. Vectorization is used to increase the speed with which a large number of arithmetic processes are handled, thus allowing for the simultaneous execution of a large number of calculations. One method for such a speed-up is computational pipelining.

Pipelining is analogous to industrial assembly-line processing where the manufactured product moves through a series of stations. Each station executes one step in the manufacturing process and all stations work simultaneously on different units in different stages of completion. Floating-point addition, for example, calls for several steps that must be carried out in sequence. A pipelined floating-point adder is divided into segments, each of which does a portion of the work that takes one clock period. At the end of the clock period, each segment passes the result of its work

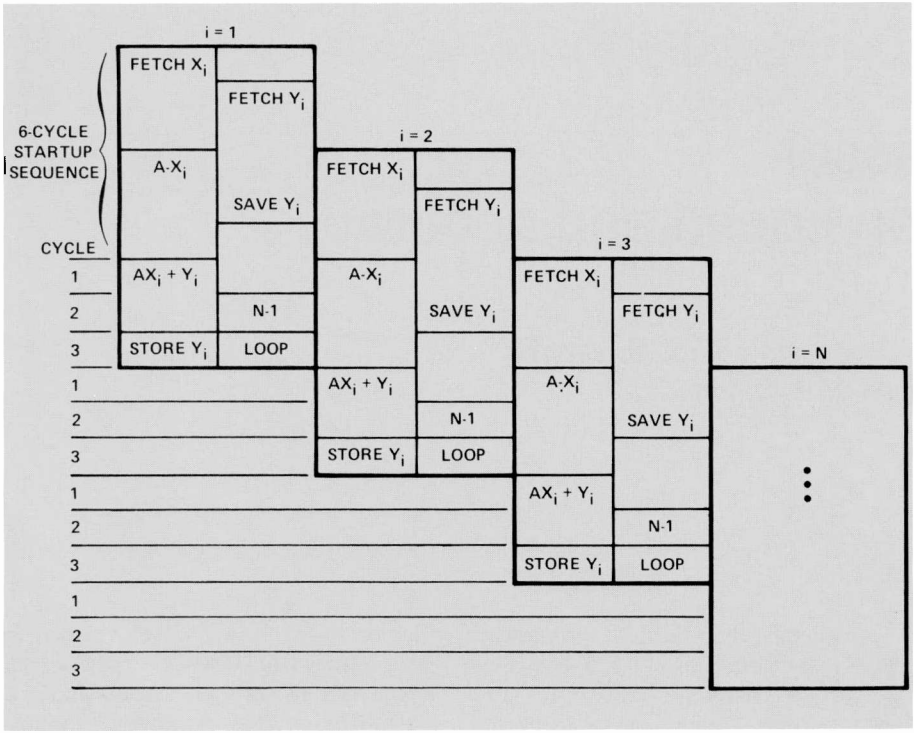

Fig. 1. *By performing more than one task in a single cycle, pipelining reduces the number of steps required to perform long, repetitive processes such as matrix multiplications.*

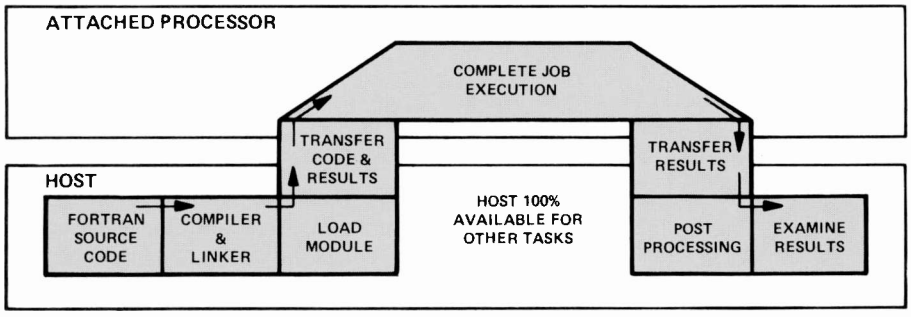

Fig. 2. *SJE (Single Job Executive) allows a computer user to submit the job, complete with data, to the FPS 164. This will allow the host IBM to process other tasks.*

to the next segment and accepts the partial results from the preceding segment. Hence, after a start-up time equal in clock periods to the number of segments in the pipeline, the adder can produce one floating-point sum per clock period as long as a new pair of operands is supplied to the first segment every clock period.

The application of pipelining to largely iterative scientific calculations is a major factor in increasing the speed of their solutions (Fig. 1). Some of the applications where engineers can take advantage of pipelining include the solution of simultaneous equations, image processing, Fast Fourier Transforms, and digital filtering, to name a few. At RCA, the engineering community can take advantage of pipelined calculations in such diverse applications as circuit analysis and structural analysis (see sidebar section).

Attached processors

There are several solutions to the need for high-speed, high-accuracy calculations. These solutions range from supercomputers (ranging in price up to $12 million) to attaching array processors to existing general-purpose computers. Here are several features of an "attached" processor:

1. It is a peripheral for a conventional host computer and is intended to enhance the performance of the host in "number-crunching" applications.
2. It achieves high performance through parallelism or pipelining.
3. It can be programmed by the user to accommodate a variety of arithmetic problems.

How they work

The remaining part of the discussion on attached array processors will be devoted to the FPS 164 currently running attached to the IBM 3081 in Cherry Hill. The FPS attached processor is nominally rated at 12 megaflops and has a dynamic range from 10^{-308} to 10^{+307}. It is connected to the 3081 through an Input/Output (I/O) channel. Using the I/O channel, the host sends and receives information to and from the FPS 164. The FPS 164 in Cherry Hill currently runs any job that can be compiled and executed in ANSII Standard Fortran 77. It has its own compiler with several levels of optimization that reside on the host machine. Advice in conversion of existing code to Fortran 77 can be obtained from Computer Services in Cherry Hill. Help can also be provided in the definition of jobs that would be candidates for vectorization. The FPS 164 also has a myriad of its own subroutines and functions, which were designed and written to take advantage of its pipelining capabilities.

There are two ways to use the attached processor—to process an entire job, or to process a subsection of the calculations as a subroutine box. The first method described is termed SJE or Single Job Entry, while subroutine processing is accomplished using APEX (Array Processor Executive).

Single job entry (SJE)

The SJE Operating System accepts commands input into the 3081 via VM/CMS. The SJE job flow is straightforward.

1. Prepare source Fortran code using the CMS editor.
2. Include references to the FPS Math Library for additional performance improvement (at user's option).
3. Compile the source using the FPS Fortran-77 compiler on the 3081.
4. Link the compiled code using the host-resident link editor to produce a load module. At this stage all external references to Fortran functions and the FPS Math Library are resolved.
5. Run the job.
6. Transfer the results of the job back to the host for output or analysis.

Using this approach, the host computer performs processing for which it is best

Math libraries and more . . .

The FPS basic libraries include Fortran-callable routines to perform:

Basic Math Routines

- Vector addition, subtraction, multiplication, and division
- Logarithms, trigonometric functions, random-number generation
- Vector-to-scalar routines, such as the SVE (sum of the elements)
- Vector comparisons
- Complex vector arithmetic
- Matrix routines, such as multiplication, transposition, and inversion
- Fast Fourier Transforms (FFTs) on real and complex vectors

Advanced Math Routines

- Eigenvalue and eigenvector solutions
- Transformation of complex Hermitian matrices
- Revised simplex routine for the solution of linear programming problems

Image Processing Routines

- Two-dimensional Fast Fourier transforms
- Two-dimensional convolution and correlation
- Spacious filtering
- Contrast enhancement

Simulation Routines

- Single and multistep solutions for ordinary differential equations
- Runge-Kutta fourth-order integrator

In addition to these routines, other software, written especially for the FPS architecture, can be obtained.

- BSCLIB—a collection of subroutines developed by Boeing Computer Services
- FMSLIB—Fast Matrix Solution Library
- MSC NASTRAN—McNeal Schwendler Nastran
- ANSYS—Swanson, Inc., finite element package
- QSPICE—circuit analysis by Quantitative Technology, Inc.

suited, while the FPS-164 processes computationally-intensive jobs in parallel with the host (Fig. 2).

Array processor executive (APEX)

A user can take advantage of the attached processor's capabilities for only a subset of his tasks. Under this method the host 3081 is called upon to perform scaler operations while the FPS 164 performs those calculations best suited to pipelining. The APEX job flow can lead to extremely efficient results.

The host Fortran program calls an APEX routine to transfer instructions and data to the array processor and then continues executing its portion of the task. Later, it calls another APEX routine to verify completion of the transfer, and then instructs the array processor to start execution of the task. The host program once again resumes work on its portion of the task.

After that, the host program calls APEX routines to verify completion of the array processor task, to return results to the host, and to ascertain that the results have been returned. At that point the host program can perform any processing that depends on those results.

Using APEX calls, the host program can also transfer data for a second task to the array processor while the array processor is completing the first task. The APEX library thus gives the host/AP system a multitasking capability that results in extremely efficient use of the system's hardware resources (Fig. 3).

The decision to use either the SJE or APEX mode will depend on the nature of the problem to be solved. Many problems will clearly be more advantageously solved by the use of APEX, because of their limited need for intensive calculations. They may depend heavily on interaction by an end user before performing calculations, returning intermediate results, and anticipating further interaction before continu-

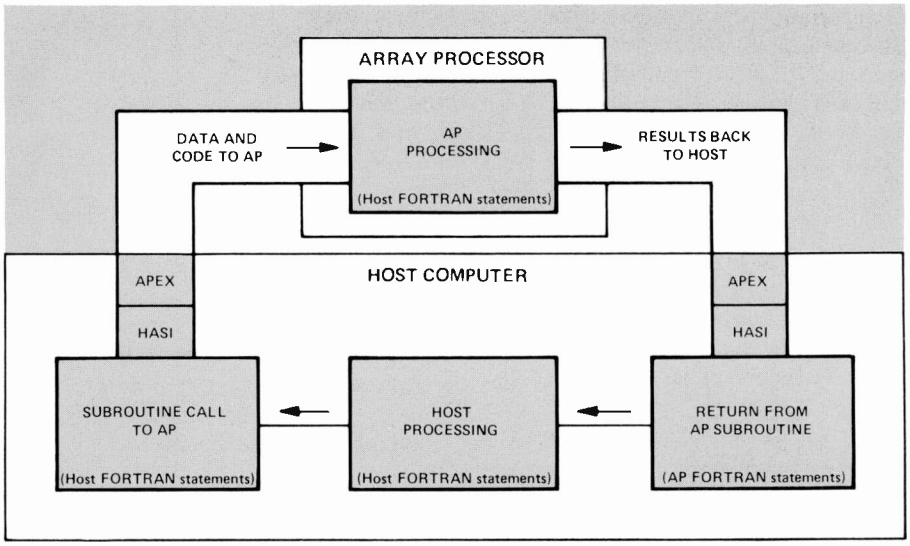

Fig. 3. *APEX (Array Processor Executive) mode will allow the computer user to take advantage of the capabilities of the FPS 164 when vectorizable code is appropriate. The user can run routines on the host IBM for other tasks, thus utilizing the FPS 164 as a subroutine box.*

ing to calculate. Such application areas may use inquiries to set up a problem, and may query the user for tolerance limits while calculating. In such a scenario, the APEX mode is a good choice. Because there is no clear-cut definition of where each is optimal, the user must consider the unique nature of his problem.

The inclusion of the FPS 164 into the general-purpose environment at the shared data center in Cherry Hill will provide increased capabilities to the RCA computer user at substantially reduced costs. The 64-bit capability of the FPS 164 will provide the accompanying necessary accuracy. If you would like further information on attached processing, please contact the author.

Susan Handman is currently Account Manager at RCA Corporate Information Systems and Services (CISS) in Cherry Hill, N.J. She is primarily responsible for engineering-related accounts. She received a B.S. in Mathematics from the University of Pittsburgh. After joining RCA in 1980, she provided technical support on math and statistical packages, and also worked in customer services on engineering and scientific implementation. Ms. Handman is the new CISS Editorial Representative for the *RCA Engineer*. Contact her at:

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Correction note:

March/April *RCA Engineer*

"Image sampling and analysis technique for high-resolution measurement of micrometer-sized features," an article by M.T. Gale and R.L. Covey published in the March/April 1984 *RCA Engineer* contains an error. Figure 10, p. 64, was printed incorrectly and should appear instead as shown here. You can obtain corrected copies of the entire article from Robert Covey, RCA Laboratories, TACNET: 226-3044.

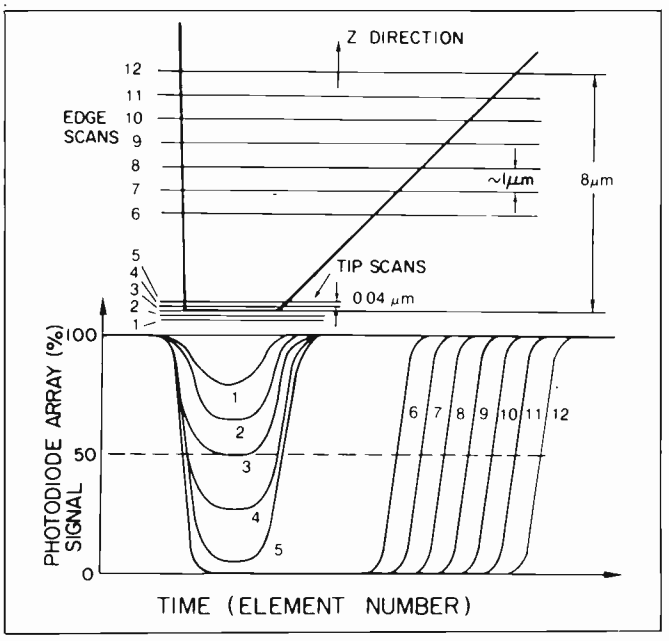


Fig. 10. *The tip and edge scan measurement operations showing both an image plane schematic and the corresponding analog signals. All dimensions are referred back to the stylus object plane. Only the photodiode array is moved during these operations.*

D. Zarodnansky

Adapting CMS for a varied user community

RCA Laboratories encourages scientists and engineers to begin and continue using CMS by providing site-specific help for them.

The VM/CMS timesharing system, which is used not only in the RCA Cherry Hill computer installation, but also in many other computing centers worldwide, is perhaps more suited for computer users with moderate to extensive experience than for someone who is just learning to interact with a computer for the very first time. Although RCA's Corporate Information Systems and Services (CISS) staff in Cherry Hill has made extensive modification to the product in an attempt to make it more easily used, most of their modifications have, of course, been in response to the needs of general users of the system, regardless of their location, as opposed to site-specific modifications.

Over the past several months, a number of steps have been taken at the RCA Laboratories in Princeton, N.J., to address user needs that are specific to that site, and to enhance access to CMS for new users. These efforts have included a set of utility programs developed at the Labs to perform common functions such as formatting and printing documents on a high-quality laser printer, and doing file management. Wherever possible, the utilities are menu driven, so that users need not memorize commands. In addition, the installation at the Laboratories of data-stream protocol convertors has allowed our terminal users (mostly on ASCII terminals) to access CMS in a full-screen mode, as opposed to the line mode, which was the only access to CMS available to most Labs users in the past.

A set of EXEC procedures, some of which provide site-specific utilities, and some of which provide alternatives to system commands, were written and tested at the Labs, and were released to the general user population as a utility package called LABSUTIL. The LABSUTIL package is fully documented, and supported by the Laboratories Computer Services activity.

In addition, another set of EXEC procedures that were designed to enhance CMS error recovery and avoidance, were written and tested on a small subset of novice users at the Laboratories, to determine if CMS usage could be made more pleasant for that group.

Access to this set of EXEC procedures is supplied to CMS users only upon request. We felt that it might cause a problem for the more experienced users to have the system respond in ways other than what they were used to and what was documented in the manuals supplied by IBM and Cherry Hill.

Abstract: *A large fraction of the personnel at RCA's David Sarnoff Research Center in Princeton use the CMS timesharing computer system provided by the RCA Corporate Information Systems and Services activity in Cherry Hill, N.J. This paper describes some of the techniques employed at RCA Laboratories to make the CMS system easier for the "novice" to use, and also describes some of the site-specific utilities developed to make the system more useful to the "veteran."*

Final manuscript received March 29, 1984.
Reprint RE-29-3-8

Preparing documents on the CMS system

One of the first requests that users made was for easier access to the IBM 6670 laser printer in the Labs Remote Job Entry facility. The 6670 is a correspondence-quality printer for documents such as reports, letters, and internal memos. Since the 6670 provides copy quality comparable to that available from an IBM Selectric typewriter, it was hoped that this facility would allow an increase in productivity by permitting users to use their terminals to view and edit documents, and to reprint the edited version, rather than having to retype an entire document each time a revision was to be made.

The facility used for formatting documents within CMS is the IBM Document Composition Facility (DCF), sometimes also known as SCRIPT. It is available to all CMS system users. The 6670 laser printer was already in place as a result of its purchase as part of an office automation pilot test of an IBM application program running under CMS.

IBM 6670 preprocessor software was installed on the system by CISS, to handle conversion of the DCF output into a form that could take advantage of the capabilities of the 6670, such as font switching, special symbols, and rotated printing. The standard means of invoking the preprocessor is to make a call to an EXEC procedure. Any options that the user wishes to use must be supplied as part of the command that calls the EXEC. To make this process more user friendly, a driver EXEC was developed that presents all of the options in a menu format, and allows the user to select the desired ones. This driver EXEC then constructs the command that invokes the preprocessor, and executes this command.

Once the capability for processing documents for printing on the 6670 laser printer was developed, it soon became apparent that additional software for formatting equations on the 6670 would be required as an adjunct to DCF. This took the form of

a DCF Application Programming Function (APF), called DSRCPROF. Ultimately, this APF was expanded to provide the capability for automatic numbering and cross referencing of the equations within the body of the document, direct control over font changes, and standard skeleton-outline formatter. This software has been tested, and is considered acceptable for clerical users. Further development to provide additional flexibility and ease of use, and to provide additional functions, is underway.

Another user request was that the documents be printable on special forms, specifically Internal Correspondence stationery. A system was developed whereby the application presents a series of questions to be answered by the user, and the answers are entered into the proper places in a formatting framework. This system has been expanded to cover forms such as External Correspondence stationery, legal-size paper, and special stationery that the user may provide.

File management utility programs

The CMS user is aware that the CMS Virtual Machine contains a disk that is used to store files. The purpose of the files and the mechanics of managing the disk space are concepts that the casual CMS user may not understand, yet file management is an important part of computer use. Users may tend to ignore the need to occasionally clean off files that are no longer needed, in part because they do not understand the reasons for, or means of, doing so. To make file management easier for the user, LABSUTIL includes a number of file management utility programs. Some of these utilities are:

- SCRUB, which presents the filenames to the user one at a time, along with a number of choices for the disposition of the file. The user may KEEP, DELETE, TYPE, PRINT, or XEDIT the file, or QUIT.
- FIND, which works like the LISTFILE command, except that it then prompts the user for a disposition for the files found. This is useful for performing the same operation on a number of related files, as well as for locating files on disks other than one's own.
- XCHECK, which cross-checks two disk areas looking for files with identical filenames and, upon finding a matching pair of names, matches the contents of the files and allows the user to dispose of one or both of the files.This reduces redundancy and wasted disk space.

Documentation for the CMS user

All of the effort put into the utility programs described above would be useless if the users were unaware of the existence of the programs, or did not know how to use them. User support and documentation comprise a major portion of the effort involved in making this system more user friendly. This support takes on a number of forms.

Written documentation

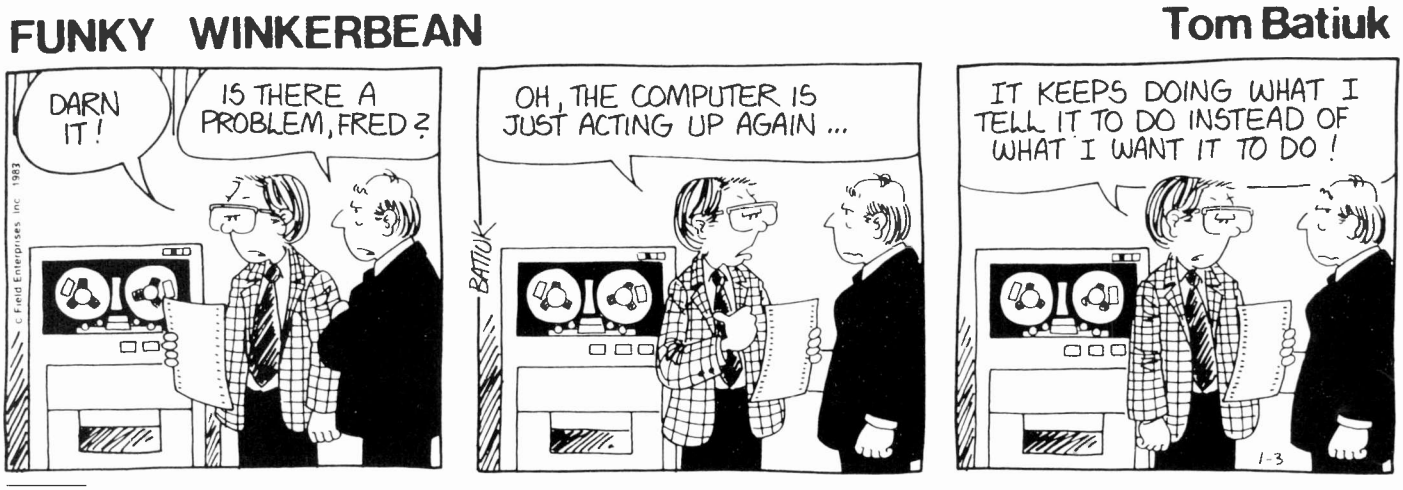
We have written manuals describing how to use these functions, which are distributed to users upon request. In addition, those manuals that we feel are of sufficiently general interest are distributed to all CMS users at the Labs. These manuals are intended as an adjunct to, and not a replacement for, the CMS User Guide, and other manuals supplied by the corporate CISS activity. The manuals document the utilities as they apply to the Laboratories site, and also point up differences, where they exist, between system standard products, and those modified to be specific for the Labs site. These manuals presently include a user manual for LABSUTIL, one describing procedures for preparing documents using DCF and the 6670 laser printer, and one describing the use of CMS in the full-screen mode through the datastream protocol convertors available on the Labs' local area network.

Internal documentation within programs

Everything on the LABSUTIL disk is written such that, if invoked with a question mark as the only argument, a brief HELP display of no more than one screen is shown. This display explains the syntax of the command and the valid options. This facility will be extended to the other Labs Computer Services-generated software as time and manpower permit.

HELP files

Utilities on the LABSUTIL disk are all documented in standard CMS HELP formatted files. Thus, those who are familiar with



"Funky Winkerbean" by Tom Batiuk reprinted by permission from Field Newspaper Syndicate, Irvine, California. Copyright © 1983 Field Newspaper Syndicate.

```
                                        (FOR26670 V 9.1.0 03/01/84)

Settings in effect for the FORMAT67 processor are:

1) Bind = 12 , 12

2) Duplex = NO

3) Fonts are: ELITE 163 ELITE 193

4) Lines Per Inch is: 6.0 , Spacing is 1

5) Number of copies is: 1

6) Paper drawer selection is:

7) Forms type is PLAIN paper

Please enter the NUMBER of any options that you wish to change or
examine the settings of, or a carriage return to accept these settings. If you
wish to change more than one setting, separate the numbers with a
SPACE:
```

The local printer utility main menu.

```
Please do not print output over 10 pages long on local Dot-Matrix
Printer . . . . . .Thank You

Please select a printer from the following:

     1          Printer in E-014          (Dot Matrix)
     2          Printer in S-209          (Dot Matrix)
     3          Printer in W-117C         (Dot Matrix)
     4          Printer in SW-122         (Dot Matrix)
     RMT21      1403 Line Printer in Labs RJE room
     LOCAL      3800 Line Printer at Cherry Hill

Enter Printer number, or remote number, or "LOCAL"

To ABORT the print operation, enter only a CARRIAGE RETURN.


To print output on the 6670 LASER PRINTER in the RJE room, use the
FOR26670 EXEC on the LABSUTIL disk.
```

The FOR26670 main menu. This utility allows use of the 6670 laser printer.

this facility may receive help with these utilities in the same manner that they get help with standard CMS commands.

The CMS HELP desk

Experience has shown that if users can get immediate on-site assistance with a problem, they are more likely to continue to make use of the products provided on the system, and to ask for assistance when they need it. With this in mind, the Labs Computer Services group has a program to provide users with immediate assistance, including a helpline, which is staffed by a person who primarily provides intensive user assistance, and one-on-one instruction when needed. Feedback from the users indicates that they are more comfortable asking questions in this setting than if they are required to call off-site for assistance. In addition, the on-site personnel are trained in the site-specific software and hardware found at the Labs, and are thus able to provide assistance with them.

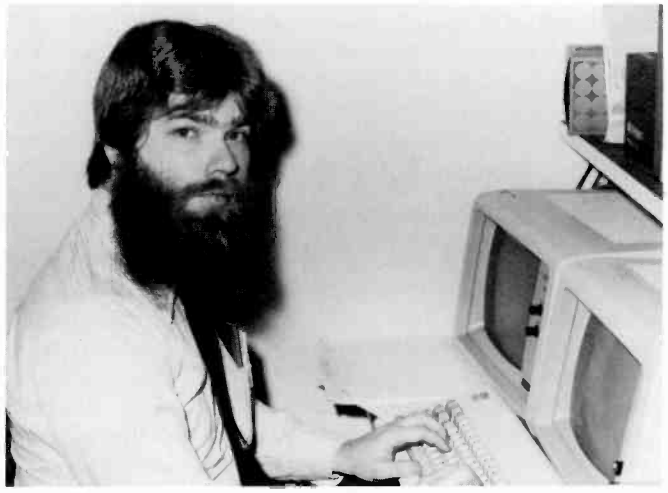
This also gives the the person providing assistance the opportunity to follow up on the original request if more help is needed. A telephone-answering device monitors the helpline and takes messages when the CMS help person is working with other users. For problems requiring immediate attention, the recorded message on the answering machine provides a number that users may call to have key members of the Labs Computer Services staff paged to handle urgent problems. Initial user response to this service has been very positive.

Further attempts at user friendliness

We have found that some of the nontechnical users of CMS require additional assistance with the system. Along this line, a number of EXEC procedures have been developed to enhance error avoidance and recovery when executing some simple CMS commands. For example, a user attempting to type or edit a document might forget to enter the filetype when naming the document. The standard CMS response to this omission would be an error message saying, "INCOMPLETE FILEID SPECIFIED." The EXEC procedure that these users now invoke in place of the system command puts a different error message on the screen, which tells the user exactly what is missing from the command. Because immediate feedback is provided as to the nature of the mistake, the user is much less likely to make the same mistake in the future.

As another example, the default condition for the LISTFILE command, which normally lists only the filename, filetype, and filemode, has been changed to show all of the information associated with the DATE option of that command, and assumes a "wildcard" for the filetype if not otherwise specified. The EXEC procedures that implement these changes are contained on a disk that is accessed by the users only if they wish to use the modified procedures.

Feedback from the users indicates that novice users find the modified procedures much more comfortable to use than standard CMS. One might argue that the users will never learn "real" CMS this way but, on the other hand, some users feel that they have no more need to learn "real" CMS than they have to learn assembly language, as long as the system does the job they need. The entire attempt to make CMS more "friendly" is founded on this approach—the system exists as a tool for the users. The system should be adapted to them; they should not be forced to adapt to the system.



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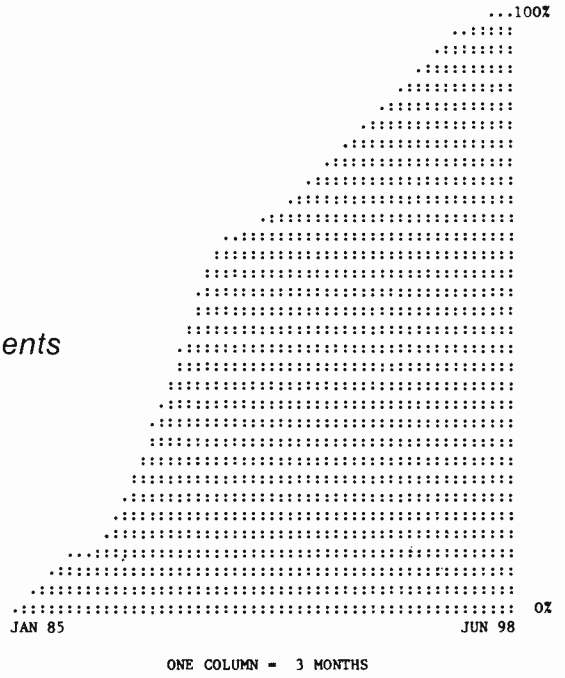
A. DeMarco

Analyzing design alternatives with the PRICE models

Complex engineering projects demand simplified assessments of cost tradeoffs, before the job begins.



Have you ever wondered how a conceptual design change would affect the life-cycle cost of a system for years to come? Conventional methods of evaluating the cost impacts of such a change would consist of days and weeks of reviewing bills of material, labor tables, reliability records, inflation forecasts, and . . . what a mess! Faced with all of that effort you might be persuaded to dismiss the cost considerations entirely unless, of course, there were an automated, streamlined procedure for reviewing the cost impacts of your concept. This procedure is the PRICE system.

Abstract: *The primary responsibility of the systems engineer is that he keeps the task within bounds. Time, people, and money are limited resources. Conventional methods of estimating a program's consumption of these resources are difficult and tedious. Parametric resource modeling can assist the systems engineer to balance design margins against resource limitations by rapidly displaying the far-reaching impacts of design alternatives. By comparing the program cost and schedule to the modeled cost and schedule through the execution and integration phases, engineering managers can help troubleshoot unexpected problems that may result in overruns in these areas.*

The PRICE cost- and schedule-estimating models have been used in many disciplines to progressively automate the compilation of estimates of program-resource consumption. These conversational computer models, which were developed at RCA, are easy to use and provide many features that allow quick evaluation of trade-off studies. An increasingly important measurement of system performance is its acquisition/life-cycle cost, and parametric cost modeling can help to automate the complicated measuring process.

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The PRICE system

PRICE is a system of computerized cost-estimating models and supporting programs. The PRICE Hardware model was first developed in 1962 as an internal RCA procedure to help automate the cost-estimating process. It was made commercially available for general use outside of RCA in 1975. Since that time, the PRICE family of models has multiplied to the numbers shown in Table I.

The PRICE models use the parametric approach to estimating. Therefore, the cost of a system is not estimated from parts lists and labor tables, but from the general impacts that certain descriptive measures of that system have on its cost. This method allows an analyst to describe a system concept that can be used in the models, without the analyst having to know the details of its "nuts and bolts."

A similar technique can be applied when considering the construction and mainte-

Table I. *The PRICE family.*

PRICE Systems creates and maintains a family of parametric models available to each customer via network computer services. Briefly, the models are:

PRICE H—Cost estimates for hardware development and production. Addresses assemblies, whole systems and systems integration.

PRICE HL—Cost estimates for equipment/system use-maintenance, repair, and other support functions to yield life cycle costs.

PRICE M—Specific cost estimates for microcircuit (chip) development and production.

PRICE S—Costs, schedules and manpower for design, implementation, test, and integration of new computer software.

PRICE SL—Costs of maintaining a software system throughout its projected operational life.

PRICE PM—Prepares master schedules for interdependent development and production activities—a project planning and management tool (a new model).

nance costs for a home. The number of rooms in the house, and the type of home are general indicators of the amount and quality of the required materials, and indicate the overall effort required for construction and maintenance. Pertinent labor rates depend upon time and geographic location. Therefore, the zip code of the home and the year of the required tasks can be used to indicate the level of the labor rates. Such a four-parameter model (Fig. 1) may appear simple at first glance, but consider the diverse ramifications of the addition of a single room. Not only would one aspect—such as carpentry cost—be affected, but masonry cost, roofing cost, wiring cost, schedules, and the ensuing maintenance costs would all be affected in varying degrees. One can see that such a model must be internally complex.

The PRICE models contain thousands of integrated equations relating descriptive parameters to costs and schedules. They have played many roles and have been used in numerous types of applications, including:

- Evaluations of bids and proposals
- Design-to-Unit-Production-Cost analysis
- Estimates of cost to complete
- Bid preparation and submittal
- Estimates of cost to modify
- "Should" cost analysis
- Bid, no-bid decisions
- Long-range planning
- Procurement planning
- Cross-checking of design concepts
- Microelectronic cost estimating
- Application to life-cycle cost analysis
- Design cost trade-offs analysis

The key to flexible use of the PRICE system is model calibration. Each of the PRICE models operates in "reverse." In this mode, historical costs and schedules of completed projects are entered as inputs to the models. Indices are then generated, which fingerprint the peculiarities of a particular product and a particular organization. These indices calibrate the generalized PRICE system to a model of a specific application. The indices serve as the foundation for use in the "forward" mode to estimate the costs and schedules of future projects. It has been found that the PRICE system provides a universal method of generating accurate cost and schedule estimates in the space, defense, and commercial business environments.

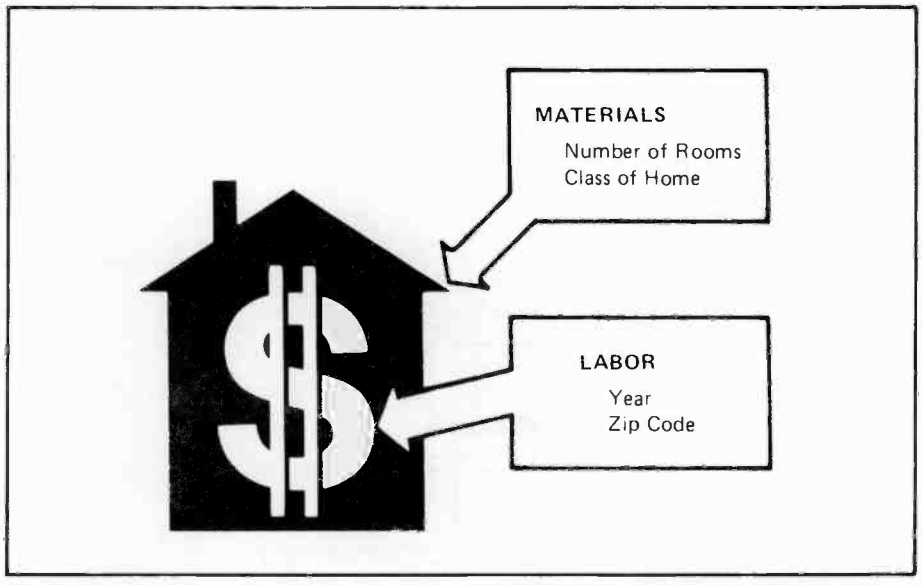


Fig. 1. *The construction and maintenance costs for a house can be estimated with a simple parametric model using four inputs.*

PRICE and the systems engineer

Resources available to any particular project are limited. Time, people, and money are all usually scarce. It is important that the design tradeoffs made during the concept phase of a program be balanced against its resource limitations. The primary responsibility of the systems engineer is to bound the task and to keep specifications within bounds throughout program evolution.

The scenario

The following example, based on an actual case study, illustrates the role of the PRICE system in assisting the systems engineer with his complex job. The scenario involves the insertion of advanced electronic technology into a United States weapons system. The particular device in question is generally known as a Programmable Signal Processor (PSP). The baseline configuration of the PSP, which is currently in full-scale development, contains large-scale integrated (LSI) circuitry. It is suspected that the insertion of very large scale integrated (VLSI) circuitry into the PSP would improve reliability, enhance performance, and reduce supply and maintenance costs. The reduction in the supply and maintenance costs would be a result of reduced number of part types, reduced circuit-board space, and longer times between PSP repair.

Two alternatives are proposed by the customer for the design and insertion of the VLSI technology: Concept A and Concept B, described in Table II. Concept A keeps the PSP's overall architecture intact. The total PSP design is translated to its VLSI equivalent and repartitioned for minimal size and integrated circuit types. In Concept B, enhancements are permitted in the redesign to optimally use the VLSI architecture. Built-in-test functions are implemented, and operational throughput is increased. It is claimed that Concept B will reap the benefits of Concept A while enhancing the PSP's overall capability. However, a high price will have to be paid during development.

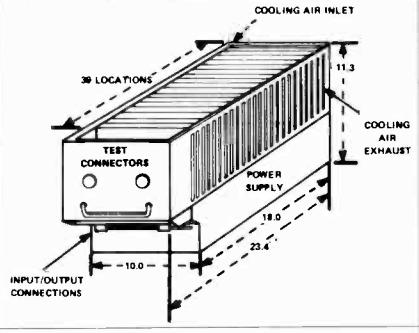
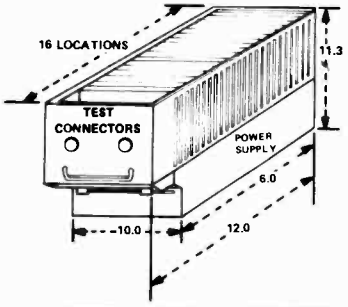
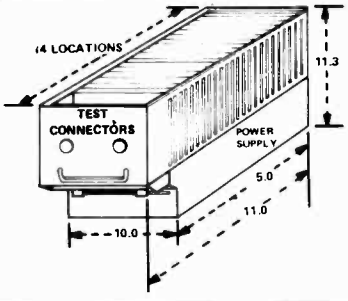
It is the job of the systems engineer to explore these concepts and determine which is most appropriate to meet the customer's specifications. The validity of the seemingly attractive improvement claims must be carefully studied before embarking on the long and costly process of developing the VLSI technology.

The analysis

An analysis to further specify each alternative concept and determine which will prove more cost effective can be performed with the PRICE system. The analysis covers all program phases from design through a ten-year deployment, and accounts for operation and support.

The method used to estimate the various costs and schedules is shown in Fig. 2. Initially, data on each concept must be collected and scrutinized. The projects are compared to similar projects that preceded them. The customer expresses uncertainty in the deployment quantities of the device. Thus, the analysis must cover both a 500-unit and a 2,000-unit deployment scheme. PRICE inputs are formulated that will accu-

Table II. *Two design concepts for the insertion of VLSI circuitry into the PSP's baseline configuration are proposed.*

Description	*Picture of unit*	*Weight (lbs)*	*Capability (millions of complex operations per second)*	*Integrated circuits*	*Number of board pairs*	*Number of software instructions*
Baseline configuration. Currently in full-scale production.		100	16	5950	31	120,000
Concept A. The total baseline design is translated to its VLSI equivalent and repartitioned for minimal size and IC types.		49	16	950	13	120,000
Concept B. The total baseline architecture is redesigned and enhanced to fully use VLSI capability.		43	25	850	11	130,000

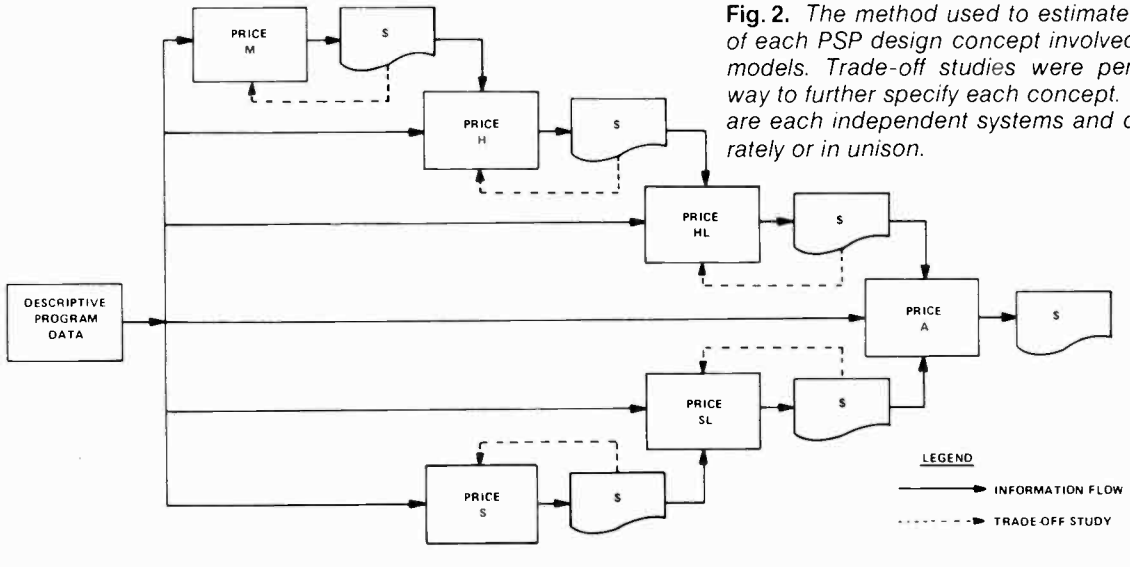


Fig. 2. *The method used to estimate the life cycle cost of each PSP design concept involved five of the PRICE models. Trade-off studies were performed along the way to further specify each concept. The PRICE models are each independent systems and can be used separately or in unison.*

Computer Graphics: A design, feedback, and display aid for the PRICE engineer . . .

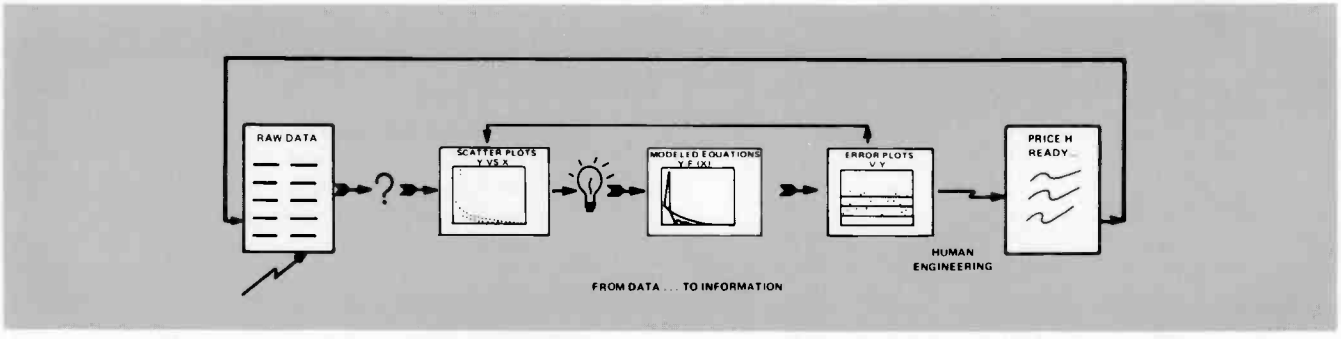
The PRICE modeling process involves systematic data gathering, analysis, model formulation, and a very active feedback mechanism. Statistical techniques supported by graphical plots of data fits and trends automatically transform raw data into information. Graphical illustrations identify data patterns that are fitted to produce the PRICE parametric formulas.

Key input and output factors of the PRICE methodology, such as cost and schedule data, are easily converted into scatter diagrams and trend plots that are the basis of correlated algorithms. At this model design stage, computer graphics saves the engineer time and effort. Erroneous data points and obvious trends are spontaneously discovered.

As shown by the illustration below, a typical modeling cycle involves constant data consolidation and analysis. A number of graphics devices are currently available to the PRICE engineer. A quick preview of the data points on a Tektronix 4105 terminal using Tellagraf provides a general idea of data patterns and identifies clusters and outliers. Similarly, an IBM PC can act as the graphics monitor once equipped with the proper interface. A hardcopy can also be obtained by a screen dump of the plot to a Tektronix 4695 ink-jet plotter. For a plot requiring excellent quality, a Zeta 8 desktop pen plotter is used.

User-friendly graphics software and smart devices automate the data-to-information transition effectively. More time is available for critical questioning of assumptions and procedures. This results in faster turn-around of hypothesis formulation and testing. As more data is fed from the PRICE Models' user, and as the scope of the models' technological applications is broadened, the regular use of computer graphics as a design and display aid increases in value.

—*Carmen Rueda,*
PRICE Systems



rately describe the concepts to the models.

It becomes apparent that each of the proposed concepts would entail the acquisition of thousands of custom and semicustom integrated circuits (ICs). However, the specific design approach to employ in the development of these devices is not clear. Three options face the systems engineer in this case: The full-custom handcrafted approach, the standard-cell approach, and the universal-array appraoch.

The handcrafted approach involves a detailed design of the IC at the transistor level. Design lead times are long and difficult to predict. In many cases the cost and schedule risks entirely prohibit the handcrafted approach.

The standard-cell approach abbreviates the handcrafted approach. The foundation of this approach is an extensive, well-documented library of circuit building blocks, called cells. Each cell is a group of circuit elements combined to perform a certain function. The cells are very adaptable to computer-aided design because of their generality. The designer now can construct the IC in terms of these cells, obviating the manipulation of tens of thousands of individual transistors and circuit elements. Development costs are much lower than that of the handcrafted approach, yet the resulting ICs are more costly to manufacture.

Universal arrays take this standardization a step further. In this approach, chips are preprocessed to yield regular arrays of uncommitted circuit elements. The designer constructs the circuit in terms of cells that can easily be created by interconnections of these circuit elements. Thus, when the design is complete, the circuit elements on the chip are merely linked together to form the IC. The development effort is similar to that of the standard-cell approach. The turnaround times for fabricated units are much shorter than that of each of the other approaches, but the manufacturing cost per unit is higher.

The question before the systems engineer is: When does it become cost effective to forgo the popular universal array approach and opt for either the standard

cell or the handcrafted approach? A tradeoff analysis using PRICE M, which estimates the development and production costs for ICs, can help to rescue him from his dilemma. The particular device chosen for illustration is a MilSpec, 2500-gate VLSI chip required for Concept A. The IC has 64 pins and is fabricated using a CMOS process. The critical factors to be considered for each approach are shown in Table III.

These, along with other descriptive parameters, are entered into PRICE M and a sensitivity analysis on production quantity is performed. The results are shown in Fig. 3. The intersecting curves reveal the point where each approach becomes more cost effective.

Although the handcrafted approach may seem appealing, money is not the only resource to be balanced. Time is also a consideration. Development schedules estimated by PRICE M and presented by PRICE PM showed that a large amount of time would be required to develop the handcrafted approach as opposed to other approaches.

Table III. *Some PRICE M descriptive parameters for each IC design approach.*

Parameter	*Hand-crafted*	*Std. cell*	*ULA*	*Explanation*
SIZE (mils²)	176²	225²	305²	Surface area of chip
ECMPLX	1.1	1	0.3	Scope of work versus engineer's experience
NEWCEL	0.8	0.2	0.05	Percent of newly designed cells
DESRPT	0.2	0.25	0.5	Percent of design repeat
CADFAC	0.8	1	1.2	Degree of computer-aided design
ITERAT	2	1	0	Design/proto/test iterations

The decision becomes clear. It is estimated that either 30,000 or 100,000 of these devices will be needed, dependent upon the final production quantity of the PSP. Also, the maximum development time for this project is 18 months. Therefore, the standard cell approach is chosen for the IC.

The information produced by PRICE M on the custom and semicustom integrated circuits assists in describing each system concept to the PRICE H model. PRICE H will estimate the PSP development and production costs as well as vital reliability information. These data, along with an equipment deployment scheme, are entered into PRICE HL. The deployment scheme defines equipment disburse-

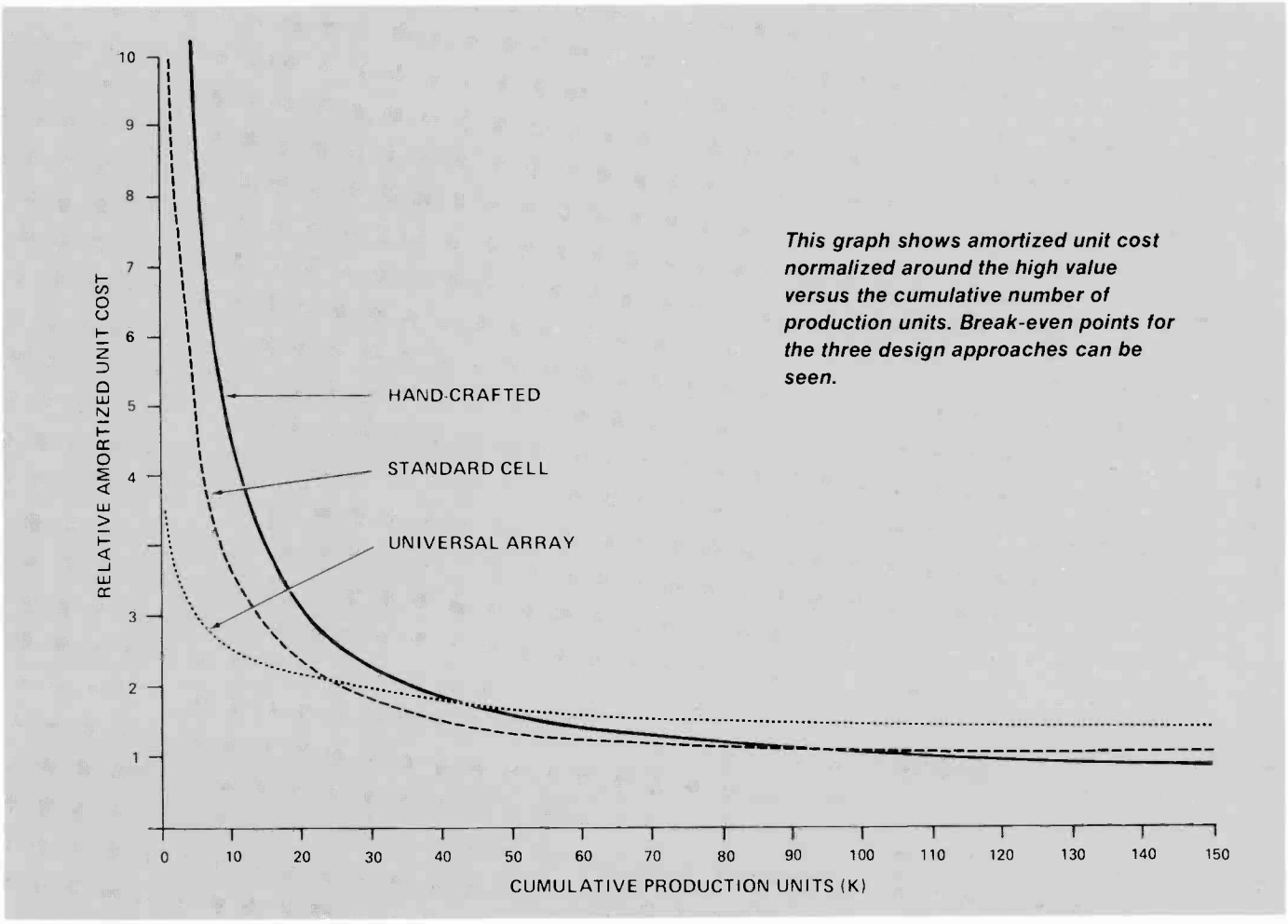


Fig. 3. *The results of a PRICE M analysis can be used to decide which IC design approach to implement.*

ment, maintenance and supply locations, equipment operating hours, and the life of the program. Here, the benefits of the built-in-test functions in Concept B are realized. It is determined that the units' own ability to determine which circuit board is malfunctioning in the field will allow a two-level maintenance concept to be implemented.

The two-level concept involves the replacement of the boards at the equipment level, with their repair at the depot. The more traditional three-level maintenance concept must be used for both the baseline configuration and Concept A. In the three-level concept, the entire PSP must be replaced at the equipment level. The defective PSP must then be tested with special test equipment at an intermediate level to determine the defective board. The board is then sent to the depot for repair. This factor will easily be analyzed since the above are but 2 of 28 maintenance concepts PRICE HL considers with every run. PRICE HL then estimates the PSP support costs and operational availability. A consolidated report displays the hardware development, production, and support costs.

A similar procedure is used to estimate the cost of software development, support, and maintenance. PRICE S and PRICE SL are used for this process. For each design concept, care must be taken when evaluating the number of instructions, a critical system descriptor used by both models. The baseline configuration consists of 120,000 lines of developed microcode. Concept A requires that 10 percent of the software be redesigned. Concept B requires 10,000 lines of new software to implement the built-in test equipment, plus a redesign of 25 percent of the baseline system's software. This complex scheme is modeled with the PRICE input parameters.

PRICE S produces a report showing costs and schedules for the various stages of software development. It becomes apparent that the software development effort required for Concept B looms large. A penalty must be paid if such a big job is to be done in the proposed time. Inevitably, more people than normal will have to be brought onto the job. PRICE S output displays the cost penalty to be expected when the accelerated schedule dictated is imposed on the project. The software data from PRICE S is then entered into PRICE SL to generate software costs for the 10-year support period.

Next, the hardware and software cost information for each concept is consolidated and described to PRICE A. PRICE

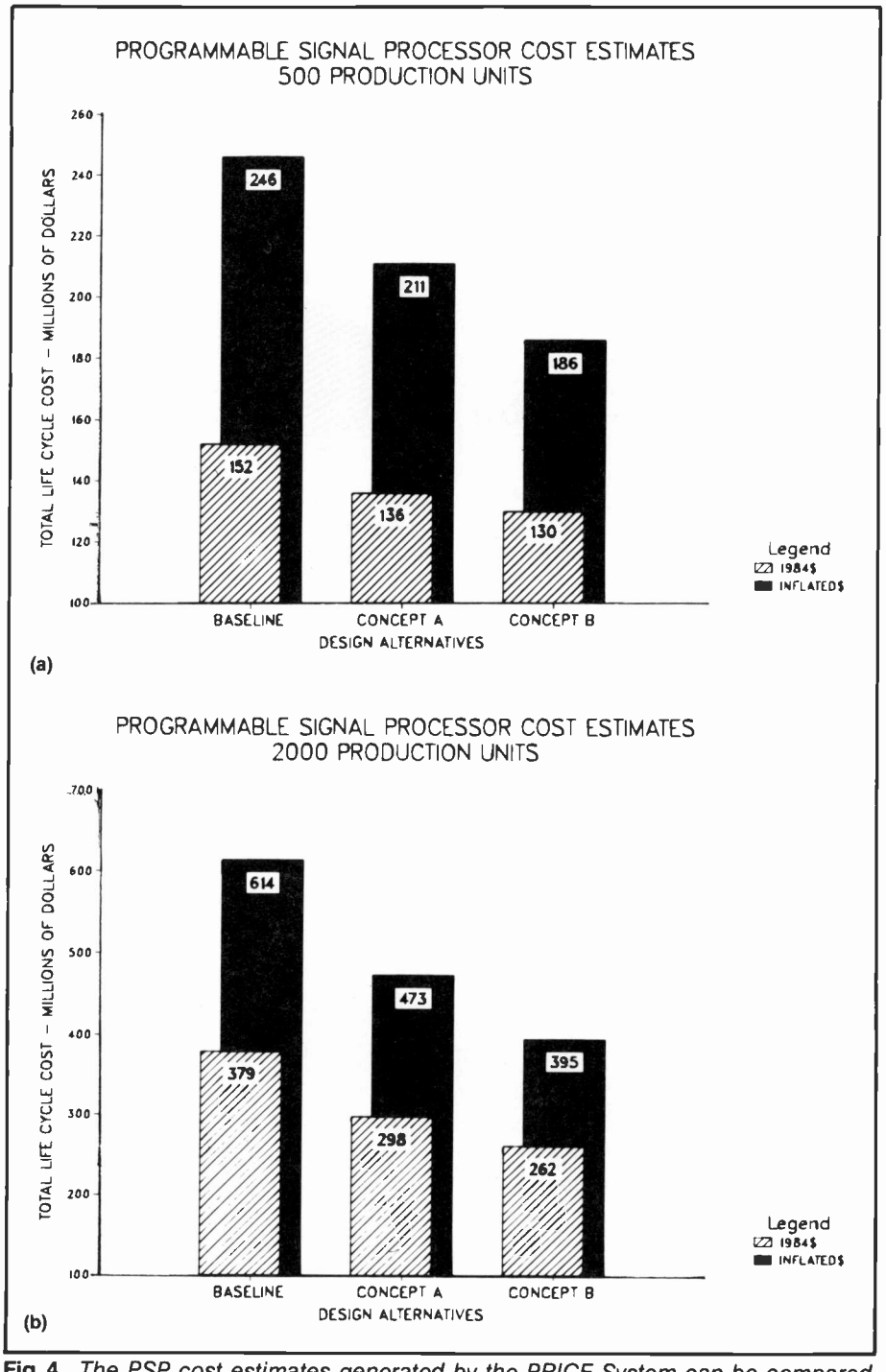


Fig. 4. *The PSP cost estimates generated by the PRICE System can be compared to determine the most cost-effective design alternative. The impact of inflation magnifies the benefits of Concept B.*

A applies economic escalation to the costs based on specified spending profiles. The model combines results and presents a unified picture of each concept.

The results of the cost analysis are shown in Figs. 4 (a) and (b) and 5. Both redesign concepts show a reduction in total life-cycle cost, as was suspected. Examining the quantity tradeoffs, it appears that the case for a redesign of the baseline configuration is stronger in the 2000-unit case than the 500-unit case.

Concept B proves to be the cost winner of the two design approaches in the out-years. The additional initial investment demanded by Concept B to further develop the VLSI technology greatly increases system reliability and maintainability, thus, decreasing support costs. This is due to the built-in test functions and the resulting stream-

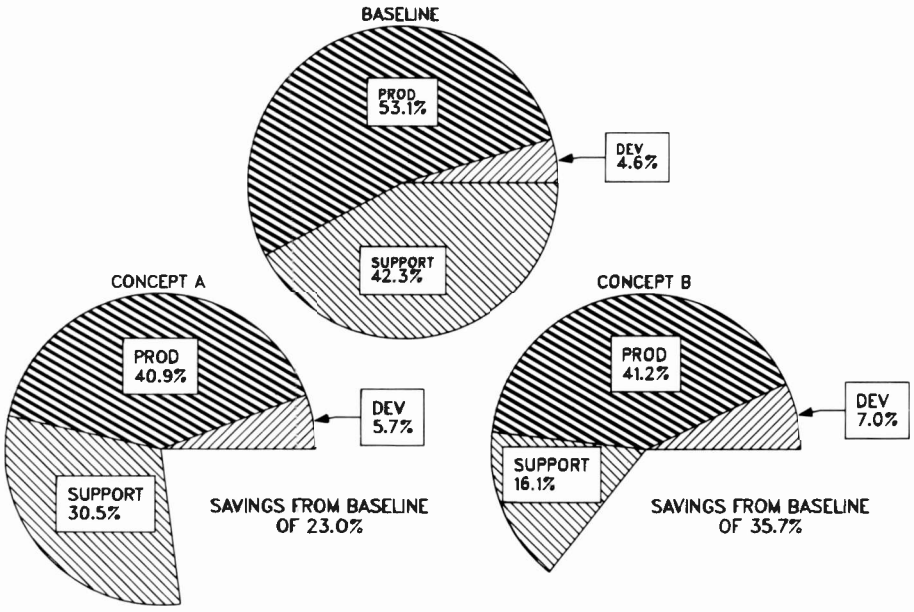


Fig. 5. *The breakdown of the PSP cost estimates shows the expected beneficial effects additional development spending has on support costs.*

Table IV. *The evolution of the PSP as it progresses through various program phases.*

Phase	*Concept exploration*	*Full-scale development*	*Production and deployment*
Weight	100, 49, 43	43, 40, 39	39
Number of prototypes	2, 5, 20	5	N/A
Production quantity	500, 2000	500, 2000	2094
Capability (MCOPS)	16, 15	25	25
Number of ICs	5950, 950, 850	850, 825	825
Number of circuit board pairs	31, 13, 11	11, 10	10
Number of software instructions	120K, 130K	130K, 131K	131K

Table V. *A comparison of the typical resources required to perform the PSP cost analysis shows the large time savings provided by the PRICE System.*

Cost analysis function	***Resources required***	
	With conventional methods	*With the PRICE Systems*
Secure descriptive information on the scope of work.	80 man-hours	12 man-hours
Select and analyze comparative cost experiences for estimating purposes.	20 man-hours	5 man-hours
Adjust historic cost data for differences in scope of work, technology, economics, resources, scheduling, tooling, and so on.	40 man-hours	Included in second category by automated models
Develop the estimate including potential engineering changes, schedule factors, inflation, and so on, through a ten-year support period.	150 man-hours	8 man-hours
Total for basic estimate above.	290 man-hours	25 man-hours
Perform sensitivity analysis and technology trade-offs.	100-200 man-hours (but time seldom permits)	4 man-hours
Continue with design-to-cost tracking, throughout full-scale development	60 man-months	6 man-months

lined two-level maintenance concept. The benefits of Concept B are magnified when PRICE A inflates the dollars as they are expected to be spent throughout the schedule. Though the case appears strong for Concept B, the size of the additional investment in development is a factor that must be presented to the customer.

The systems engineer has now accumulated a wealth of information from a relatively small amount of data. Armed with this information, he can address the alternatives confident that the design/cost/schedule tradeoffs have been thoroughly synthesized for each task. The systems engineer was also able to uncover potential problem areas, such as software development, that would result in cost and schedule overruns, if not addressed. Concept B was chosen in the scenario. The development funds and manpower will be provided to accomplish the design, because the customer wishes to realize the huge support savings predicted in the out-years of the program.

Tracking design-to-cost

The applicability of the PRICE system does not stop at the concept exploration phase of a program. The systems engineer must orchestrate a program through detailed design, execution, integration, test, and operation and support. He must also ensure that the program stays within its proposed bounds throughout its life. This is a very formidable task, since it is inevitable that a system will change in size, shape, and function as the program progresses from phase to phase. The particular evolution of the PSP is shown in Table IV.

Once the PRICE descriptive parameters of, in this case, the processor, are established, it is a simple matter to update them monthly, or even weekly, as the system evolves. Parameters that were estimates during the concept phase can now be updated to reflect internal and subcontractor actualities. Other physical parameters become measurable as prototypes are built. The PRICE system becomes a tracking machine with this type of periodic parametric maintenance. Such a machine produces monthly cost-allocation reports that can detect potential overruns before they propagate. Also, the far-reaching life-cycle cost impacts of proposed engineering changes can be immediately viewed and presented to the designers. This tracking procedure ensures that the cost and schedule consequences of each design change are thoroughly analyzed. Pe-

riodic analysis is critical to keeping the task within its bounds.

Time savings due to automation

The conceptual analysis and design-to-cost tracking of the PSP were accomplished in far less time than conventional bottom-up estimating methods. Table V shows the estimated man-hours that were saved by using the PRICE system. This savings was realized due to the high degree of automation the PRICE system provides.

The "PRICE" of success

The results and the time savings presented in this scenario are impressive. However, the road to the level of automation that can be achieved with the PRICE system must be initially cleared. Model calibration is the key. Organizations that have calibrated the PRICE products typically achieve savings by reducing estimating cycles to 8 to 12 times less than that of conventional methods. To realize this savings requires a significant commitment by the PRICE user. Special training is required, and there is the preliminary model validation and acceptance phase that all organizations must experience. Model calibration never really ends. There is always the need to substantiate the PRICE performance, as there is with the performance of other estimating methods, including conventional ones. The most prominent characteristic of an organization that successfully uses the PRICE system is an energetic commitment toward making the PRICE system work for them.

Access to the PRICE system

The PRICE system is available to all PRICE-trained RCA personnel. Over 100 RCA personnel have been trained in the PRICE system. Anyone desiring training must attend one- to two-week courses in Mt. Laurel, New Jersey. Each attendee receives a computer-based work area and a complete set of reference material. Trainees learn the theory of the models, techniques to develop parametric data, and methods of analyzing their results. Contact with PRICE personnel does not stop when the courses are over. Trained PRICE users are supported by a fully staffed Operations group as well as periodic newsletters and technical bulletins which keep them abreast of current methods and events. For details on PRICE training enrollment, contact Ms. Geri Devlin, (609) 338-5215.

Conclusion

The PRICE parametric system of estimating saves time. The potential use of the PRICE system throughout the life of a program was illustrated by the Programmable Signal Processor study. This and other cases prove that the PRICE system is a valuable tool for systems engineering, as well as many other disciplines.

As an organization matures, management identifies opportunities to mechanize certain tasks and reduce costs. This phenomenon creates a steady rate of technological improvement within the industry. However, dramatic productivity increases come about not by mechanizing existing tasks, but rather by using new methods that stimulate changes in an organization and in the way information is handled.

The PRICE system offers a means to truly automate the estimating process. A strong commitment to the PRICE methodology will enhance the flow of information within an organization and facilitate faster and more informed decisions.

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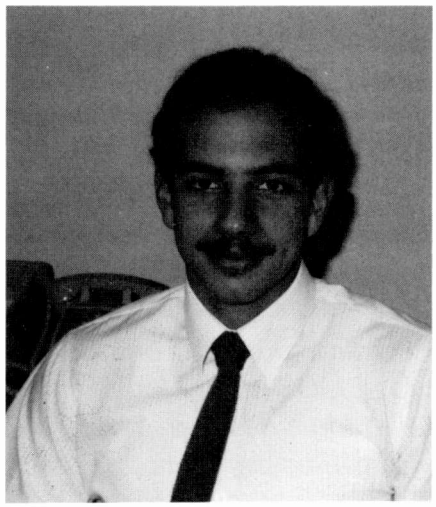

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H.G. Patterson | J.L. Magos

CMOS technology moves towards IC leadership

Semiconductor processing advances are opening new vistas for CMOS technology. In microprocessor applications, memory, and logic devices, CMOS appears ready to displace two of its long-time competitors, NMOS and TTL.

Ever since their development at RCA's David Sarnoff Research Laboratories in Princeton, N.J., in the early 1960s, Complementary-Symmetry Metal-Oxide Semiconductor (CMOS) devices have moved steadily to the forefront of the digital and linear integrated-circuit technologies. Originally conceived as a logic-device family, CMOS technology now spans the full range of digital circuitry from microprocessors and memory chips to gate array and standard-cell semicustom devices. CMOS use is growing in linear circuits such as operational amplifiers and analog-to-digital converters, and it is fast becoming a key technology for the emerging telecommunications and data-communications markets.

Abstract: *This tutorial on CMOS technology reviews the fast-moving history of metal-oxide semiconductors and shows how CMOS in particular holds the most promise for devices in the 1980s and 1990s. The low power, the high noise immunity, and the wide operating-temperature range, all benefits of CMOS, are becoming increasingly important to circuit designers. Enhancements, such as QMOS for higher speeds, and HCT for TTL logic functions, promise to broaden CMOS popularity. The authors conclude with a look at the other CMOS devices, such as static RAMs and peripheral chips.*

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In view of its wide acceptability, most knowledgeable observers expect CMOS to become the dominant semiconductor technology of the 1980s and beyond.

MOS and bipolar types

CMOS is one of three types of semiconductor circuit techniques that use MOSFETs (Metal-Oxide Field-Effect Transistors). The other two are PMOS (*p*-channel MOS) and NMOS (*n*-channel MOS). CMOS technology is unique in that it combines both PMOS and NMOS transistors on a single silicon chip. The principal advantage of this arrangement—but by no means the only one—is that a CMOS device consumes substantially less power than any other major form of integrated-circuit semiconductor.

In both semiconductor structure and performance, all MOS devices differ dramatically from the transistors of the other major type of integrated-circuit technology, that is, bipolar. The use of bipolar technology is exemplified by the well-known digital IC family known as Transistor-Transistor Logic or TTL. Although individual bipolar and MOS transistors can be described ideally as switches, their operating characteristics are exactly opposite.

A bipolar transistor is a current-controlled switch having a low input impedance, while an MOS transistor is a voltage-controlled switch with a high input impedance. An MOS switch is much like the old-fashioned vacuum tube switch, because it is voltage-controlled with high input impedance. Bipolar technology is uniquely built for high current and high speed—and it has high power consumption. CMOS technology is characterized, in general, by lower current and speed—and it consumes very little power. It is also perfectly suited for basic logic devices up through the dense circuitry required by the coming generation of Very Large Scale Integrated Circuits (VLSI).

On the other hand, bipolar logic circuitry consumes too much power to be used for VLSI—and the high power is usually a handicap in its use in even the smallest scale integration. This fundamental difference accounts for the diverse roles played by each in the world of digital and linear ICs. To understand how basic CMOS devices operate and are constructed, refer to the box, "CMOS devices, top to bottom."

Four user benefits of CMOS

Low power

The ultra-low power consumption of CMOS translates into a number of advantages for users as listed in Table I. For example, if an IC technology is power conserving, designers need less expensive and sophisticated power supplies, which naturally reduces system costs. Moreover, such supplies can operate without special cooling equipment—fans, blowers, and so on—providing a savings in both the cost and physical size of the equipment. Low-

power consumption also permits the design of battery-powered, portable products. In fact, CMOS is the only technology considered by designers for products of this type.

Wide voltage range

A close second to the low-power advantage of CMOS is the advantage of the wide operating voltage range of CMOS ICs. There are CMOS IC types that operate at as high as 20 V. The widely used CD4000B logic family operates from 3 V to 18 V. Regulation is rarely needed and battery life is extended due to this characteristic. In contrast, most TTL logic must operate at 5 V ±0.25 V; this means that expensive, high-current, and well-regulated supplies are a must with TTL, but not with CMOS logic.

Switching-level stability

Another parameter favoring CMOS circuits over TTL IC circuits is switching-level stability over wide temperature ranges. As the table shows, plastic-packaged CMOS ICs are specified to operate over a −40 to +85°C range. Plastic packages are the most common and inexpensive types, filling most industrial and consumer applications. Ceramic-packaged CMOS devices are rated for operation over the full military temperature range of −55 to +125°C.

Plastic-packaged devices in other IC technologies—NMOS, PMOS and bipolar—are usually rated for operation only over a 0 to +70°C range. Because of this restriction, such technologies are a definite handicap in certain extended-temperature-range applications. One of these, automobile-engine controls, is increasingly moving towards the CMOS camp. If an engine controller is intended for under-the-hood service, CMOS becomes the favored technology because its stable temperature characteristics can withstand the wide fluctuations experienced in the automotive environment. There are many other "wide-temperature-range" applications of this type in space, military, consumer, and industrial systems that rely on very stable operation over extended temperatures.

Noise immunity

A fourth characteristic that sets CMOS atop all other IC technologies is its high immunity to electrical disturbances (noise) generated within a system or arising from external sources. In digital IC specifications, two parameters are defined—noise-immunity voltage and noise margin. Noise-immunity voltage—either a logic high or logic low—is that noise voltage at any one input to a logic device that does not cause a false signal to propagate through the system. Noise margin is the difference between the specified input voltage of a device and its specified output voltage. Figure 1 illustrates the concepts involved in noise definitions.

Table I. *CMOS characteristics and benefits.*

Key characteristics	*Benefits*
• Very low power consumption: Typical values at 1 MHz/5V Gate 1 mW Counter 3 mW 8-bit micro 5 mW 4 K RAM 20 mW	• Low power supply costs • No cooling fans (lower cost/small size) • Battery operation/standby/portable
• Very low standby current e.g. 16K CMOS RAM 15 μA/3 V/70°C	• Allows backup storage with small/low-cost battery
• High noise immunity e.g. 1.5 Volts at V_{DD} 5 Volts	• Operation reliably in noise environments without special filtering e.g. process controllers
• Wide temperature range: Plastic −40 to +85°C Ceramic −55 to +125°C	• Reliable operation in hostile conditions e.g. automotive, engine control and military

Noise margins are defined in terms of inputs and outputs to gate elements, the basic building blocks of all digital circuits. In Fig. 1, the input voltage to the load gate is the output voltage of the driver gate. Both gates in this example operate from a supply voltage of +5 V. For CMOS gates operating at a 5-V supply level, the maximum logic 0 input-voltage ($V_{IL\ max}$) to a gate can be 1.5 V. This means that the driver gate's logic-0 voltage can be as high as 1.5 V and still be recognized by the load gate as a logic-0 voltage. Thus, the "logic-0 input region" in Fig. 1 extends from 0 to 1.5 V. Similarly, the minimum logic-1 input voltage ($V_{IH\ min}$) can be 3.5 V. That is, if the driver gate's output is as low as 3.5 V, the load gate will still recognize this level as a logic-1 voltage. The "logic-1 input region" in Fig. 1 extends

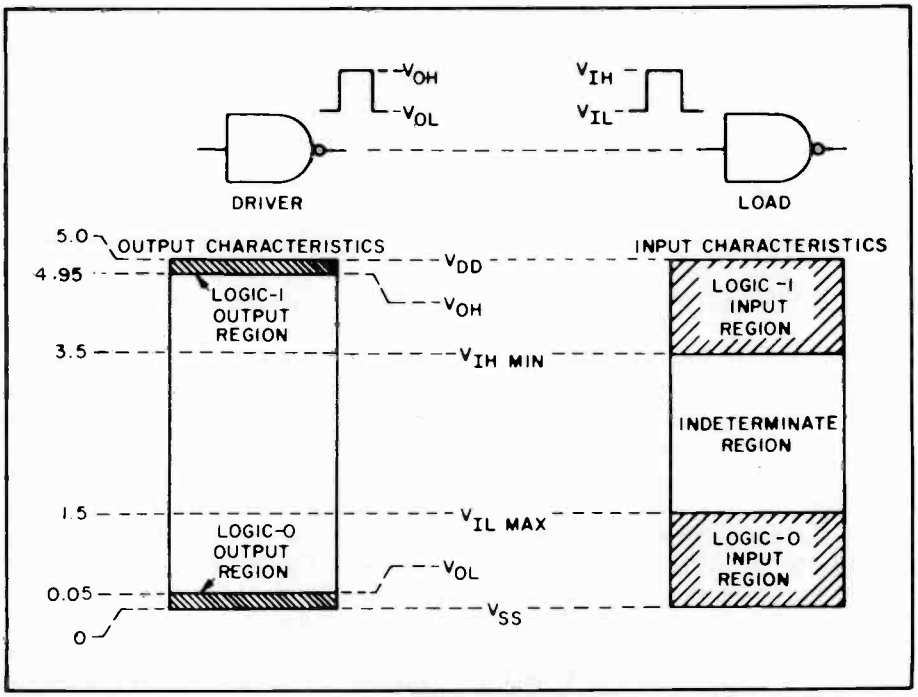


Fig. 1. *The noise margins of the CMOS CD4000B family are wider than those of any other semiconductor technology. Because the logic-1 and logic-0 input regions shown above are 1.5 V wide, CMOS devices are more immune to noise than other logic forms. In TTL logic, for example, the same input regions are just 0.4 V wide.*

CMOS devices, top to bottom

From the most complex microprocessor circuits to the simplest gates, deep within all CMOS devices is a basic circuit element called an inverter. As shown in Fig. A, a CMOS inverter is composed of a *p*-channel MOS transistor at the top and an *n*-channel transistor at the bottom. Because *n*-channel and *p*-channel transistors have diffusions of opposite polarity dopings, they operate with voltages of different polarity. Thus, a positive input voltage turns on an *n*-channel device but turns off a *p*-channel. Conversely, a zero voltage (ground as shown in Fig. A) at the input to the inverter turns on the top (*p*-channel) transistor and turns off the bottom (*n*-channel) transistor. Note at the bottom of Fig. A that both transistors can be represented as switches to simplify the explanation.

This simple CMOS circuit performs the most basic of logic operations in a digital system, namely, that of inversion. If the voltage applied to the input (In) terminal is positive, the *p*-channel switch turns off, disconnecting the output (Out) terminal from the supply voltage (+). The Out terminal is therefore at ground potential because the *n*-channel switch is turned on and connected to ground. Now if the voltage at the In terminal is zero, the *p*-channel switch turns on, connecting the Out terminal to the positive supply voltage. This time the *n*-channel switch turns off. This sequence describes the basic logical operation of inversion; the output logic (voltage) level is always opposite that of the input.

In an actual CMOS IC, *p*-channel and *n*-channel transistors are fabricated on a silicon metal substrate, as shown in Fig. B. The contact terminal of either transistor is the gate. In the original CMOS technology, the gate was made of metal, which formed one plate of a capacitor. The other plate was the substrate of the device, and the two plates were separated by silicon dioxide (SiO_2), an insulating

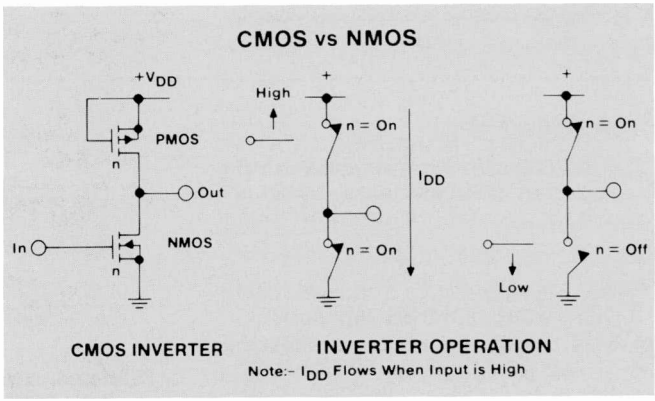


Fig. A. *The basic CMOS inverter.*

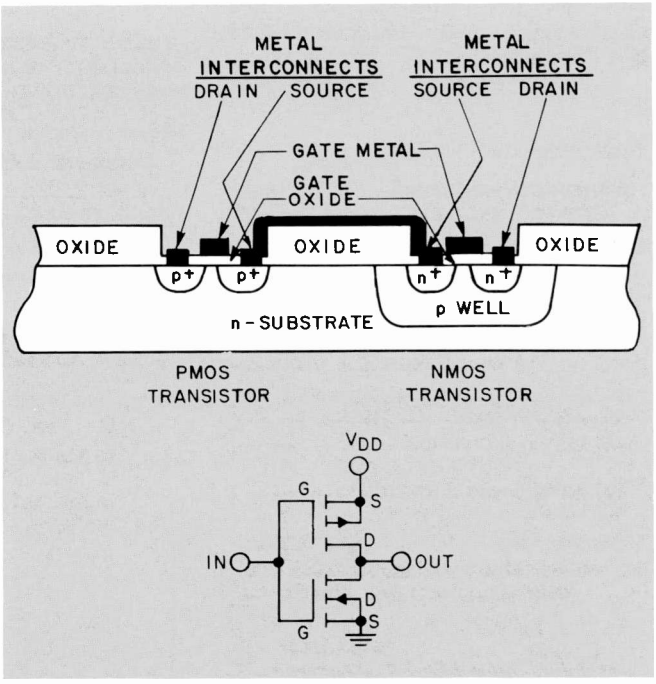


Fig. B. *CMOS construction on a single chip.*

from 3.5 V to the power-supply rail (+5 V).

Note that both input regions are 1.5 V wide, that is, they have noise margins of 1.5 V. Assume, for example, that the driver gate output (voltage) is a logic-0 voltage, that is, a nominal V_{OL} level of 0.05 V. Therefore, V_{OL} can have 1.45 V of overriding spurious noise and yet the load gate will be able to recognize the signal as a logic-0 level. In effect, there is a margin of error of 1.45 V against the effects of noise. The same holds true for the driver gate output logic-1 voltage of 4.95 V, that is, V_{OH}. Noise can pull this level down to 3.5 V, while the load gate continues to recognize a logic-1 signal. Obviously, the larger the noise margin, the greater the device's immunity to error from unwanted noise.

CMOS provides the highest specified noise immunity (or noise margin) of any logic family. TTL logic, by contrast, offers a logic "0" ($V_{IL\ max}$) of 0.8 V and an out voltage of 0.4 V ($V_{OL\ max}$). Thus, the noise margin is only 0.4 V compared with 1.45 for CMOS! Therefore, spurious noise is more likely to introduce errors than is the case with CMOS. Furthermore, CMOS logic operating at 15 V is specified to provide 5 V of noise immunity at both "high"- and "low"-logic levels. The foregoing data illustrate the fact that CMOS can serve in applications in which comparatively high levels of electrical noise can be encountered. Two notable examples are factories that use heavy machinery and automobiles; in the latter, solenoids, ignition, horn, and so on, generate lots of high-energy noise.

CMOS in perspective

With its multiplicity of technical advantages over other semiconductors, CMOS is already becoming the leading IC technology, especially for digital circuits.

First, Fig. 2 illustrates the expected use of MOS technologies—PMOS, NMOS, CMOS, HCMOS—through the end of this decade. The projections indicate that CMOS will experience the most dramatic growth of any technology. By 1990, according to *Integrated Circuit Engineering,* CMOS will command about 50 percent of the IC market, up from about 20 per-

material. Because the gate input is a capacitor, the input current is extremely low (for descriptive purposes, it can be assumed to be zero).

When the output of one CMOS inverter drives the capacitive input of another, no IR (resistive) voltage drop occurs in the drain circuit as a result of the input current (assumed to be zero). Therefore, the output voltages can rise or fall to their full positive (power supply voltage) or negative (ground) levels. Moreover, since one transistor is on and the other is off, the net current in the drain circuit—called quiescent current—is extremely low, typically in the nanoampere (10^{-9}amps) range. For this reason, CMOS devices consume the least power of any semiconductor technology.

Another observation from Fig. A and the operating description given above is that this operation occurs over a 3 V to 18 V supply voltage (CD4000B logic). Also, the ideal switching voltage is 50 percent of the positive supply voltage (a 1.5 V switching level for a V_{DD} of 3 V and a 9-V switching level for a V_{DD} of 18 V). Over a temperature range of −55°C to +125°C, this switching voltage varies less than ±1 percent of the supply voltage.

Some years ago, a significant processing breakthrough occurred in MOS technology. This was the development of the silicon gate as a replacement for the metal gate. In silicon-gate technology, a conducting form of silicon serves as the gate material instead of metal. Not only does the silicon gate improve the performance of CMOS devices, it allows the gate to be formed before the drain and source are diffused (see Fig. C). In this process, a patterned polysilicon material is used to define the gate area so that the following source and drain diffusions are self-aligned to the gate. The process, called self-aligned silicon gate, is now standard in all CMOS digital devices.

Among the advantages of the self-aligned silicon-gate process compared to metal gate are lower operating power consumption, higher speed, higher density, and lower operating voltages. Silicon-gate CMOS devices are characterized by low-power consumption and high density (many devices in a given amount of chip area). By contrast, bipolar (TTL) devices are characterized by low density and high power. Obviously, however, each technology has an appropriate role in digital system design.

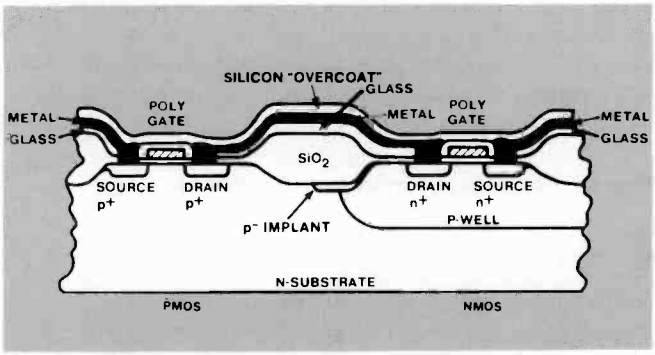


Fig. C. *CMOS self-aligned silicon-gate technology.*

Not content to stand still, RCA for example, forged ahead in processing technology with the development of self-aligned silicon gate CMOS on a sapphire substrate. Called CMOS/SOS (CMOS/Silicon-on-Sapphire), the process produces the highest frequency MOS integrated circuits. In the fabrication technique, a thin film of heteroepitaxial silicon is deposited on a sapphire substrate. High-speed devices are possible because the process eliminates many of the parasitic capacitances of conventional structures. Distributed parasitic capacitance imposes frequency limitations on a circuit. In addition to high speed, CMOS/SOS ICs have the highest resistance to nuclear radiation. This makes them the preferred technology for ICs used in aerospace and certain military systems.

cent at present. HCMOS is a new high-speed version of CMOS considered primarily for logic devices and is included in the total of 50 percent. Over the same period, the use of NMOS will remain about the same as at present, while PMOS will be on the decline as a digital technology.

Historically, PMOS is the oldest of the MOS semiconductor processes and was used in the early memory devices of the early 1970s. PMOS was comparatively easy to build, but it had some major drawbacks, including: it requires two power-supply voltages for operation rather than the single supply voltage of all other technologies, it's slow, it's very temperature limited, and it consumes appreciable power when compared to CMOS. NMOS, which is more difficult to fabricate, appeared on the scene in the early 1970s, just in time to catch the phenomenal growth of microprocessor and memory devices. The big advantage of NMOS over PMOS is that its current carriers are electrons rather than holes. The greater mobility of electrons means that the same size NMOS transistor is two to three times faster than its PMOS counterpart. Looking at it another way, for a particular speed a transistor in NMOS is smaller than the PMOS version and hence, NMOS chips are much smaller. NMOS also runs at lower threshold (turn-on) voltages and can operate from a single +5 V supply, making it compatible with other logic technologies.

As a result of these features NMOS became, and still is, the leading technology for the fabrication of microprocessor, memory chips, and VLSI circuits in general. Interestingly, however, neither NMOS nor PMOS was much of a factor in logic-family ICs—inverters, gates, flip flops, counters, and other such devices classified as small-scale integration or SSI. This vast arena is dominated by bipolar (TTL) technologies. The only competition here came from CMOS, but the two logic technologies split off into different application areas (TTL for high-speed computers and CMOS for most other uses).

As is well known, computers will continue to be not only the fastest-growing market in the electronics industry, but the

major consumer of ICs as well. Of course, CMOS logic serves in computer systems also, but primarily in peripheral circuits that can tolerate its slower speed constraints. Nevertheless, the CD4000B series of CMOS logic, manufactured by semiconductor giants such as RCA, Motorola, and National Semiconductor, has grown into one of the most widely used SSI families in the electronics industry. As described previously, CD4000B logic offers users significant advantagaes over TTL—lower power, wider voltage range, wider temperature range, higher noise-margins—with the only limitation being a lower speed. Also, when compared with the higher-powered TTL at 5 V operation, CMOS is very reliable due to its lower IC chip-power dissipation.

Table II. *CMOS logic versus two competitors.*

	LS TTL	*NMOS*	*CMOS*	*CMOS advantage*
Gate delay	8 nS	8 nS	8 nS	
Power (f/flop at 1 MHz)	20 mW	8 mW	2 mW	x
Noise immunity	0.4 V	0.4 V	1.5 V	x
Temp. range (commercial)	-40° +85°C	-40° +85°C	-55° +125°C	x
Supply tolerance	±0.25 V	±0.25 V	2 V -18V	x

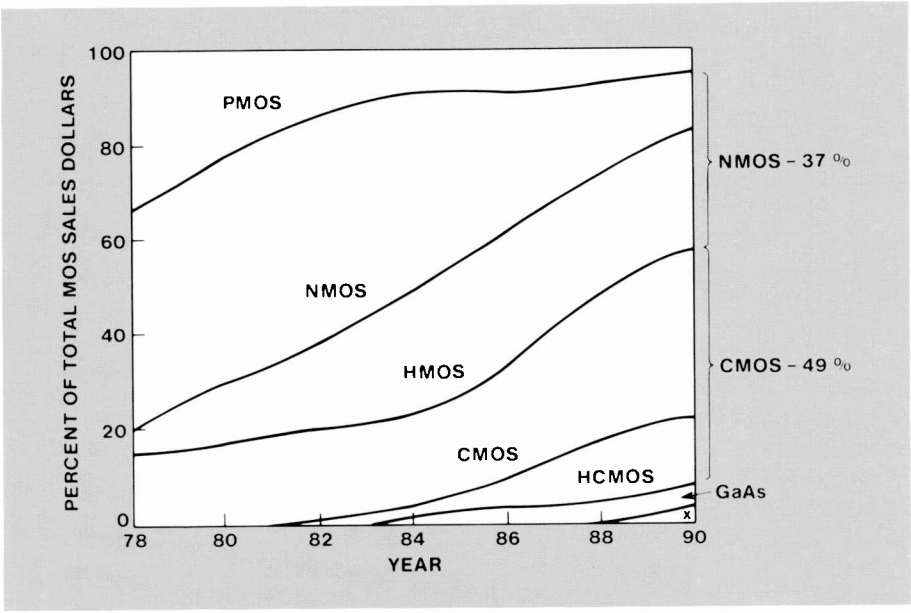


Fig. 2. *CMOS is emerging as the leading semiconductor technology of the decade. If the projections shown here are on target, CMOS technology will capture 50 percent of the total digital chip market by 1990. Other technologies, by comparison, are either declining or remaining static.*

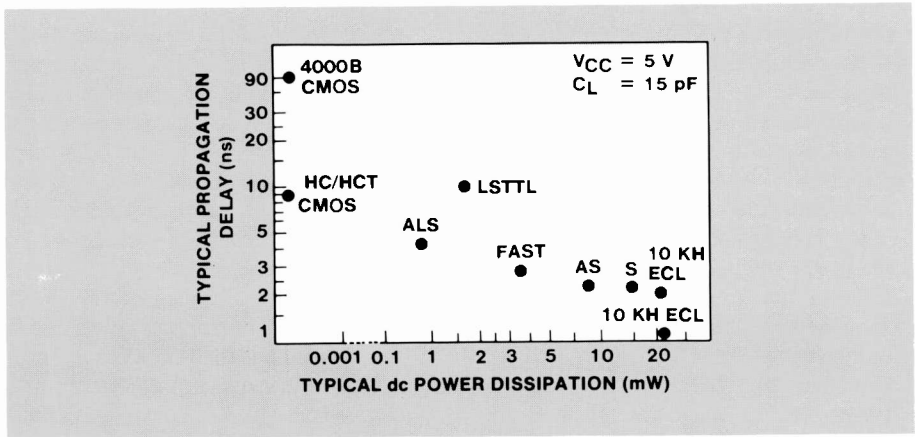


Fig. 3. *A dramatic increase in its speed capability has pushed CMOS into the same speed range as bipolar (LSTTL) technology. But CMOS logic consumes far less power than bipolar, giving it a significant edge in all but the highest-speed applications.*

Dramatic changes are occurring in the semiconductor industry of the 1980s, including the reversal of the traditional roles of digital technologies. One of the most far-reaching is the emergence of a new class of CMOS logic, which runs at the same speed as one of the most widely used TTL families, LSTTL, for low-power Schottky TTL. QMOS (Quick CMOS) by RCA offers the best of both worlds—the speed of LSTTL and the low power consumption of CMOS.

Figure 3 shows the speed versus power characteristics of the major semiconductor technologies used in logic devices. Note the position of the HC/HCT CMOS family. It is about ten times faster than its older brother, 4000B CMOS, and just as fast as its principal TTL competitor, low-power Schottky TTL (LSTTL). Although HC CMOS and LSTTL operate at the same speed—about 9-ns average propagation-delay time—the difference in power dissipation overwhelmingly favors CMOS. Its dissipation is barely measurable (several orders of magnitude less) on the power scale in Fig. 3, but that of LSTTL is about 1.5 mW. Generally, a CMOS system dissipates about one-hundreth of the power of LSTTL logic when the operating, or dynamic, power is considered along with dc power.

The implications of fast CMOS have significant importance to designers. For the first time, they can obtain bipolar performance along with all the power, voltage-range, temperature and noise-margin enhancements of CMOS. In fact, a special CMOS family called HCT has been created to provide pin-for-pin and specification-for-specification replacements for all of the TTL logic functions. The basic family, HC, is intended primarily for new all-CMOS designs. Therefore, in all but the highest-speed applications, the HC/HCT family of CMOS logic will be the successor to the TTL family. Since the majority of data-processor digital circuits operate in the speed range of fast HC/HCT CMOS, the family is well positioned to replace TTL as the leader in digital IC logic technology.

Table II summarizes the key parameters of CMOS, NMOS, and LSTTL. The speed enhancement made possible by QMOS-type processing advancements gives CMOS

a substantial advantage over the other devices.

CMOS—a complete family of devices

While CMOS logic gradually overtakes TTL, the advantages of the technology are continuing to make an impact on microprocessor and memory ICs. In microprocessors, RCA introduced the first CMOS 8-bit chip, the CDP1802, in 1976. It has become the most popular CMOS microprocessor. Moreover, the same technological advantages responsible for producing fast CMOS logic—processing, lithography—have spawned a variety of improved versions of the CDP1802.

The family tree of Fig. 4 shows the evolution of RCA's CDP1800 series of microprocessors. Two trends are evident. First, the speed of CMOS microprocessors is increasing. The latest versions run at clock frequencies of 5 MHz compared to the 3.2 MHz of the CDP1802A. Second, improved semiconductor processing allows a larger number of system functions to be incorporated on-chip. The CDP1804A, for example, contains 2 kbytes of read-only memory (ROM), 64 bytes of random-access memory (RAM) and a timer/counter circuit in addition to the basic microprocessor. In addition, users obtain all of the power, temperature, and noise-margin benefits associated with CMOS technology. Thus, CMOS microprocessors can be applied in

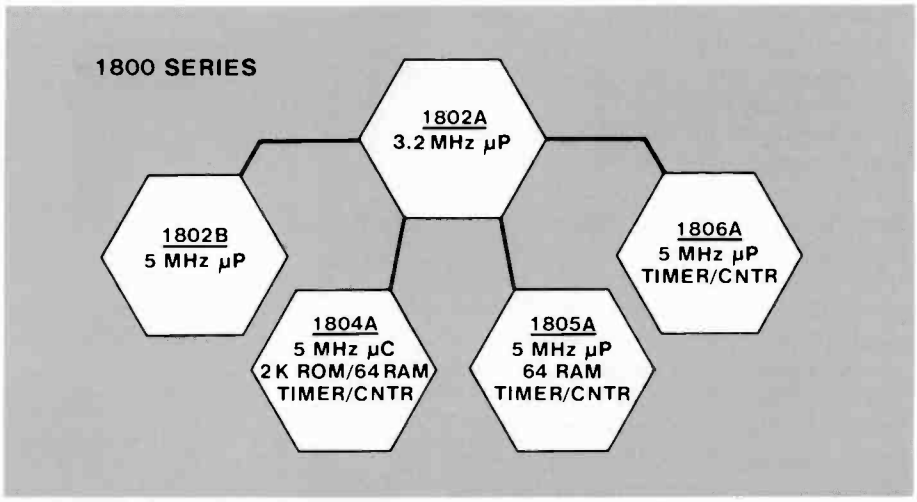


Fig. 4. *Beginning with the 8-bit CDP1802A microprocessor, RCA's family has steadily increased in both speed and functionality. Together with the power savings, wider temperature range and noise-margin advantages of CMOS, these processors are on the verge of industry leadership.*

equipment in which it is virtually impossible to use either a bipolar or NMOS microprocessor.

As microprocessor-based systems become more memory-intensive, the need for high-density, low-power memory devices increases. CMOS technology's forte is in static RAMs (rather than dynamic RAMs) and large ROMs. These two types of memory chips are projected to experience the largest growth increases of any memory devices during the period to 1990. One reason—applicable to RAMs—is that a static RAM requires far less control circuitry (called overhead) than a dynamic RAM.

Because the basic storage cell of a RAM is more complex than that of a ROM, the total storage capacity of RAMs is much smaller than that of ROMs. At present, static RAMs are commonly available in 16-kbit sizes with 64-kbit chips expected shortly. By contrast, ROMs can be as large as 256 kbits, four times the storage capacity of RAMs.

Users can look forward to two trends in memory technology. The first is that densities—the number of bits/chip—will continue to grow larger. Just as important, the

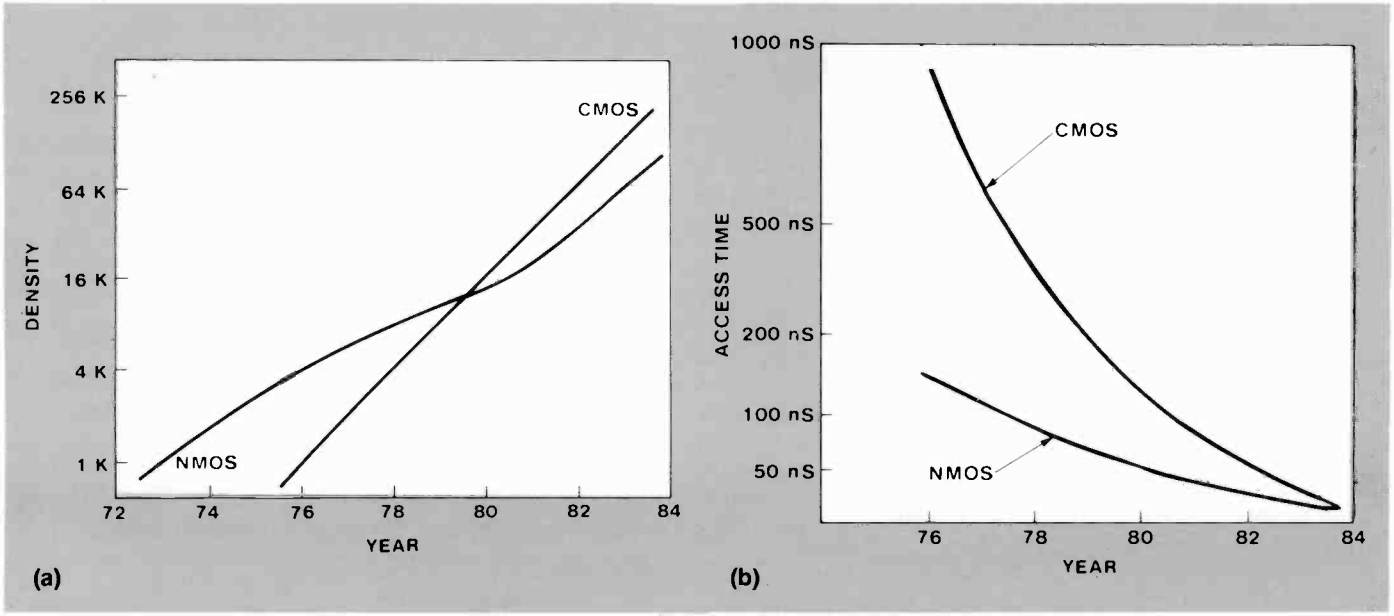
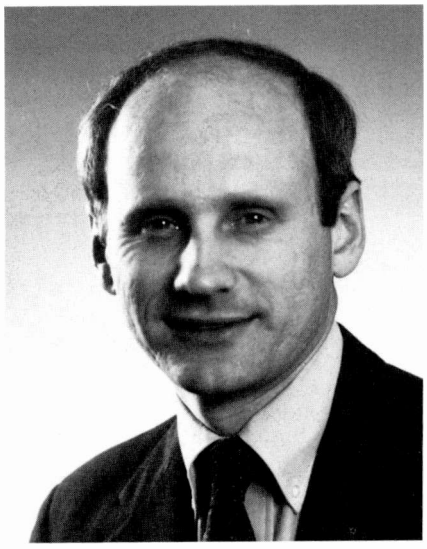


Fig. 5. *Two reasons why CMOS static RAMs are ousting their NMOS competition are* ***(a)*** *increased density and* ***(b)*** *faster access times. With their high speed and low-power dissipation, CMOS RAMs are expected to be one of the leading memory technologies by the end of the 1980s.*

speed of memory devices continues in an advancing trend. Figure 5 shows these two developments compared to NMOS technology for static RAMs.

As most users are aware, a complete system requires support devices to transfer data between the processor and memory, handle input/output (I/O) functions, perform timing functions, and other such so-called housekeeping chores. A wide range of peripheral chips is available in CMOS technology to support the microprocessors and memories. In the arsenals of RCA and other manufacturers are chips such as keyboard interface devices, interrupt controllers, real-time clocks, UARTs (Universal Asynchronous Receivers/Transmitters) and video controllers. These and other devices permit users to construct systems by assembling building blocks of completely compatible components.

The decades of the 1980s and beyond hold great promise for CMOS technology. Because of its inherent characteristics, it stands on the doorstep of technology leadership across the broad range of all integrated circuits.



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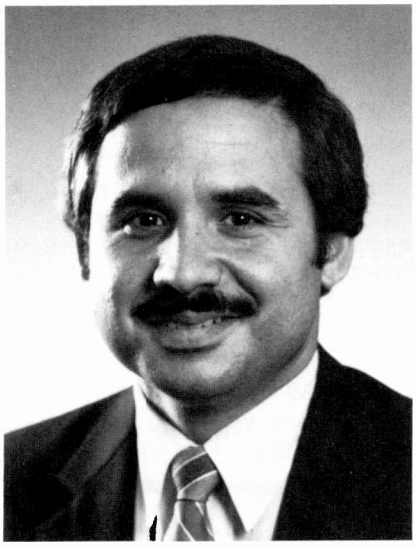

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A day in the life of an information-efficient scientist

Paul Schnitzler
RCA Laboratories
Princeton, N.J.

My name is Thursday, Annie Thursday. I'm a scientist.

6:58 A.M. *I just rolled out of bed; looked in the mirror; didn't like what I saw. Got moving anyway.*

8:00 A.M. *After the usual things, I found myself in my laboratory. Punched the ON button on the terminal and went to hang up my coat. Coffee smelled good; somebody left some for me.*

Logged on; checked mail. Three notes from the boss: "Need to see you, Thursday," "Need to see you, Thursday," and one flashing, "Where the hell are you?" The next three items are memos, two on video processing, the third on the new PAX machine. I see this last one is written by Joe Friday.

Key in message to boss: "I'm back—when's a good time?"

Call up CALENDAR. I see it's my son's birthday tomorrow and my anniversary is coming up in two weeks. I have a meeting tomorrow morning. Today is clear.

8:07 A.M. *Now to work. Turn on the main power to the bench and drink some coffee. Jack Kraft, the technician I work with, tells me that everything has been running okay for the last three days. He wants to know why I came in this morning. I throw an eraser at him.*

Started measurements on the new video modulator/up converter. It's the old story, set a frequency, check the level, record the amplitudes, do it again. Key each value into the terminal, one at a time. Called up PLOT. Well, that helps; at least the curve is smooth, but something's wrong near point nine megahertz. I'll take more points.

Enter points, PLOT. That's better; save this stuff. I tell Kraft to continue the run; it looks like it's going well.

Message-waiting signal. The boss again: "Forget it." Fine.

Courtesy *IEEE Communications Magazine.* Adapted from Vol. 20, No. 3, pp. 24-25 (May 1982).

8:48 A.M. *Let's see what Friday's latest report has to say.*

Spend the next hour reading reports on the tube. Take some notes; I want copies of a couple of pages here and there. Send a particularly interesting figure to the color printer.

9:51 A.M. *Jack says the data is done. I call up the graphs on the terminal one after another. Seven look interesting and I request copies.*

Jack will pick up the figures and the graphs while I check the shop schedule, on the tube again, for the status of the new modulator/up converter assembly.

The model shop schedule shows a delay. No reason entered.

10:14 A.M. *It appears some personal reconnaissance is called for. I key in a note to Jack that I'm going down to the shop.*

I meet Sam Waterford in the hall. He is working on fiber optics these days. He suggests a cup of coffee and I say fine. Sam tells me he has new data on some low-loss crystal material. I must remember to look it up. I step into the next office and find a free terminal; I key in a quick note to myself to check out Waterford's work.

10:38 A.M. *The shop. After nosing around a few minutes, I find my job has been delayed because of a new high-visibility program that got in ahead of me. I talk to the administrator and with a little sweet talk I get a new, firm date. Well, that cashed in one favor.*

11:00 A.M. *I'm back at the lab. I find Jack has been going strong. The graphs are on my desk and they need some study. They don't make much sense; there is some inconsistency between them. I can't tell whether there's noise in the measurements or real artifacts are present. Perhaps some additional data is required. But Jack is busy right now.*

11:58 A.M. *Len Awsom looks in. Suggests lunch. The salad and yogurt are okay. The argument about the price of butter in the Third World countries makes no sense at all and lasts 45 minutes. Not okay.*

1:01 P.M. *I see Jack; he tells me his other experiment is performing strangely and he wants me to check it out. I agree. We call up the statistical-analysis package to check the significance of the data. The difference of the means shows the confidence is just over 50%, not nearly good enough. We agree more data is necessary and, on the terminal, I enter changes in the experimental plan to reflect these new requirements. The tube responds with suggested revised milestone dates for the project. The new dates look acceptable and I okay them.*

2:13 P.M. *I have been thinking about that technical report I'm writing and I have some new ideas. I call up my current version and type in some new text. In a few minutes, I have placed it in the correct location in the body of the report. I realize that a figure would be helpful at this point. I check my project experimental data file and I find just the figure I want. I notice the address in memory and "send" a copy of it to the report.*

I read the whole report at this point; it reads well. I'll let it stew in my mind overnight just to be certain and I'll release it for distribution tomorrow.

2:39 P.M. *I call Ellen Strong, the hot-shot division program manager. The recent manufacturing changes are going well, but she tells me of a new problem. The schematics are in file and I look them up on the tube. After some discussion, we agree on the problems and some changes that might help. I propose some tests to check out the changes and, with some modifications, she agrees. The data will be recorded at the division and will be accessible through my file.*

3:29 P.M. *More coffee. Jack talks of a date he had last night. I listen; I guess I'm a voyeur at heart.*

3:41 P.M. *Back to those graphs. I still don't know what to do with them. Awsom had provided an analysis of the problem and I applied his techniques to the data. There are some serious discrepancies.*

The only way I'll resolve this is if I meet with Len and Joe. I use the CALENDAR routine to find some open times on all our schedules. 11:00 A.M. tomorrow looks good. I send a message to each of them for their approval of that meeting time.

4:16 P.M. *I finally have some time to see Waterford's crystal-loss data. There is a lot of data and it takes me some time to look it over. There are a number of interesting facets. I need to talk to him more about it.*

4:50 P.M. *Uh, oh, late again. Before leaving, I key up the TV listings. Looks like the only thing on tonight is a new film, "Through the Kinescope." I guess I just can't get away from it.*

Better type in a note to my husband that I'm going to be late. He'll get it when he gets home.

6:12 P.M. *Dinner. Same old stuff, but tasty. My eight-year-old Jill comes in. She shows me some white material in her hand and wants to know what it is. I tell her it's paper and she asks what the funny marks are. I tell her that's writing. I explain that that's the way we used to send each other messages. I also tell her that I did all my homework on that stuff when I was her age. She looks at me like I'm an escapee from a looney bin.*

Kids!

Contact: ***P. Schnitzler*** **TACNET: 226-2199**

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint.

Advanced Technology Laboratories

G. Ammon
Performance of an Optical Disk Jukebox—Presented at the Topical Meeting on Optical Data Storage, Monterey, Calif., and published in the *Proceedings* (4/18-20/84)

M. Beacken
Efficient Implementation of Highly Variable Bandwidth Filter Banks with Highly Decimated Output Channels—Presented at IEEE 1984 Int'l Conf. on Acoustics, Speech, and Signal Processing, San Diego, Calif., and published in the *Proceedings* (3/19-21/84)

M. Crouthamel
Spacecraft Thermal Design Using Interactive Graphics—Presented at the AIAA 22nd Aerospace Sciences Meeting, Reno, Nev. (1/9-12/84)

A. Feller
Custom LSI Devices Using the Standard Cell Approach—CAD/CAM Series of Texts to be published by Auerbach Publishers

J. Gaev | P. Kleinosky | J. McAdams
Test Programs That Teach—Presented at the IEEE Workshop on Automated Test Program Generation, Crystal City, Md., and published in the *Proceedings* (2/8-9/84)

R. Hackenberg
Computer Processing of Phase Structure Rules—Presented at CALICO (Computer Associated Language and Learning Consortium) Symposium, Baltimore, Md., and published in the *Proceedings* (1/14/84)

W.A. Helbig
Hardware Descriptive Languages—Presented at the 17th Hawaii International Conference on System Sciences, Honolulu, Hawaii, and published in the *Proceedings* (1/4-6/84)

R.A. McClain | W.B. Schaming
The RCA Multifeature Statistical Tracker—Presented at ARO Workshop on Analytic Methods for Target Acquisition and Tracking, Ft. Belvoir, Va. (2/13/84)

Astro-Electronics

G. Beck
The ACTS Flight Segment: Cost-Effective Advanced Communications Technology—Presented at the 10th Annual AIAA Commun. Sat. System Conf., Orlando, Fla. (3/18-22/84)

D. Chu
Harmonic Responses Reanalysis of Modified Structures—Presented at the AIAA 25th SDM Conference, Palm Springs, Calif. (5/14/84)

S. Dhillon | H. Goldberg | P. Goldgeier
R. Sudarsanam
17/12 GHz Communication Receiver for DBS—Presented at the Int'l Microwave Symposium, San Francisco, Calif. 1984 IEEE MTT-S (5/30/84)

J. Engel
Production of the SOOS Cradle Structure—Presented at the Fifth Strategic Systems Project Office Mgf. Tech. Mtg., Ontario Canada (3/28/84)

R. Gounder
Chaired two sessions on Spacecraft Structures and Materials—29th National SAMPE Symposium and Exhibition, Reno, Nev. (4/3-5/84)

R. Gounder
Structures and Material Technology Interfaces in Satellite Systems—Presented at New York Chapter of SAMPE, Woodbury, Long Island (3/20/84)

S. Moochalla | D. Aubert
20-GHz Lumped Element GaAs FET Driver Amplifier—Presented at the 84 IEEE MTT-S Conference, San Francisco, Calif. (3/84)

S. Moochalla | E. Kohut | D. Aubert
S. Dhillon | H. Zelen
Dual Mode Driver Automatic Level Control APM for Direct Broadcast Satellite Transponder—Presented at the AIAA 10th Comm. Sat. Systems Conf., Orlando, Fla. (3/84)

C. Profera | H. Soule | J. Rosen
J. Dumas | J. MacGahan
Shaped Beam Antenna DBS—Presented at the AIAA Comm. Sat. Systems Conf., Orlando, Fla. (3/18/84)

A. Weinrich | M. Freeling
RCA Advanced Satcom - The First All Solid State Communications Satellite—Presented at the AIAA 10th Comm. Sat. Conf., Orlando, Fla. (3/19-22/84)

Automated Systems

J.W. Betz
Performance of the Deskewed Short-Time Correlator—Presented at the IEEE Conference on Acoustics, Speech, and Signal Processing, San Diego, Calif. (3/84)

M.J. Cantella | D.F. Dion
A Real-Time Histogram Equalization Processor for Dynamic Range Compression of IR Video Images—Presented at the National Aerospace and Electronics Conference, Dayton, Ohio (5/84)

M.J. Cantella | F.F. Martin
Performance and Application of a 160 × 244 Element Schottky Barrier IR Focal Plane Array—Presented at the 32nd National Infra Red Information Symposium, San Francisco, Calif. (5/84)

G.R. Edgar
Location of Multiple Faults by Diagnostic Expert Systems—Presented at SPIE's Technical Symposium East '84, Washington, D.C. (4/84)

H.W. Grunbaum
Learning Curves: The Theory and Implementation—Presented at the NCMA Workshop 1984, Cambridge, Mass. (3/84)

J.D. McCready
Graphic Design Industry—Presented at the Regional Career Fair '84, University of Lowell North Campus (3/84)

E.M. Melendez
Chapter Motivation Workshop Talk—Tau Beta Pi, Northeast Regional Convention, Northeastern University, Boston, Mass. (4/84)

S.B. Mesnick
Post Award Audit—Presented at the NCMA Workshop 1984, Cambridge, Mass. (3/84)

E.H. Miller
Military Applications of Commercial Computer Technology—Presented at the Command, Control, and Communications TMSA Conference, San Francisco, Calif. (3/84)

K.I. Pressman
Comparison of FAR (Federal Acquisition Regulations) with DAR (Defense Acquisition Regulations)—Presented at the NCMA Seminar, Buffalo, N.Y. (3/84)

Government Communications Systems

D.E. Britton
Formal Verification of a Secure Network with End-to-End Encryption—Presented at the 1984 Symposium on Security and Privacy, Oakland, Calif., and published in the *Proceedings* (4/30/84)

J.H. Hoover
A 10^{13}-Bit Optical Disk Jukebox System—Presented at the Tape Head Interface Comm. Colony 7, Maryland (3/84)

Laboratories

D.E. Ackley | D. Botez | B. Bogner
Phase-Locked Injection Laser Arrays with Integrated Phase Shifters—Published *RCA Review*, Vol. 44 (12/83)

R.C. Alig
Picture Tubes for Color Television—Presented at the Virginia Polytechnic Institute, Blacksburg, Va. (5/8/84)

R.E. Askew
A Cooled Low-Noise GaAs FET Amplifier—Published *RCA Review*, Vol. 44 (12/84)

I. Balberg | N. Binenbaum | C.H. Anderson
Critical Behavior of the Two-Dimensional Sticks System—Published *Physical Review Letters*, Vol. 51, No. 18 (10/31/83)

R.R. Barton
Defect Location Clustering Schemes—Published *North-Holland European Journal of Operational Research*, Vol. 15, pp. 203-211 (1983)

D. Botez | J.C. Connolly
M. Ettenberg | D.B. Gilbert
Very High CW Output Power and Power Conversion Efficiency from Current-Confined CDH-LOC Diode Lasers—Reprinted from *Electronics Letters*, Vol. 19, No. 21, pp. 882-883 (10/13/83)

D. Botez | J.C. Connolly
High-Power Phase-Locked Arrays of Index-Guided Diode Lasers—Published *Appl. Phys. Lett.*, Vol. 43, No. 12 (12/15/83)

M. Ettenberg | G.H. Olson | I. Ladany
P. Webb | N.J. DiGiuseppe | T.J. Zamerowski
J. Appert
On the Reliability of 1.3-μm Lasers and 1.0- 1.7-μm Detectors Grown by Vapor Phase Epitaxy—Presented at the Int'l Semiconductor Laser Conf., Rio de Janeiro, Brazil (8/7-10/84)

T.J. Faith | C.P. Wu
Elimination of Hillocks on AlSi Metallization by Fast-Heat-Pulse Alloying—Published in *Appl. Phys. Lett.*

P.J. Gale | B.L. Bentz | W.L. Harrington
C.W. Magee | H.A. Weakliem
Analysis of Silanes for Hydrogenated Amorphous Silicon (α-Si:H) Production by Gas Chromatography/Mass Spectrometry (GC/MS)—Presented at the 32nd Annual Conf. on Mass Spectrometry and Allied Topics, San Antonio, Tex. (5/27/84)

J. Gibson
Effects of Transmission Impairments on the Quality and Coverage of Multi-Channel Sound for Television—Presented at the NAB Convention, Las Vegas, Nev. (4/30/84)

A.M. Goodman | J.P. Russell
L.A. Goodman | C.J. Neuse | J.M. Neilson
Improved COMFETs with Fast Switching Speed and High-Current Capability—Reprinted from *Proceedings* of the IEEE International Electron Devices Meeting (12/83)

J.M. Hammer | C.C. Neil
Adjustable Modules for High-Power (Over 7.5-mW CW) Coupling of Diode Lasers to Single-Mode Fibers—*Journal of Lightwave Technology*, Vol. LT-1, No. 3 (9/83)

E.F. Hockings | S. Bloom | D.J. Tamutus
A High-Transmission Focus Mask for Color Picture Tubes—Published in *RCA Review*, Vol. 44 (9/83)

S.T. Hsu
A Simple Method to Determine Series Resistance and k Factor of an MOS Field Effect Transistor—Printed in *RCA Review*, Vol. 44 (9/83)

G. Kaganowicz | J.W. Robinson
Room Temperature Glow Discharge Deposition of Silicon Nitrides from SiH_4 and NH_3—Presented at a Session of Plasma Technology, 34th Canadian Engineering Conf., Quebec, Canada

M. Kaplan
X-Ray Photochemistry: w-Chloro Olefin Sulfones—Reprinted from *Polymer Engineering and Science*, Vol. 23, No. 17 (Mid-December 83)

H. Keiss | V. Augelli | R. Murri
Carrier Lifetime from Transient Photoconductivity Measurements on Silicon Films—Presented at Int'l Conf. on Physics of Semicond., San Francisco, Calif. (8/6-10/83)

H. Keiss | G. Wieners | R. Keller
Photoconductivity in trans-$(CH)_x$—Presented at Int'l Conf. Physics and Chemistry of Low-Dimensional Synthetic Metals, Abano, Italy (6/17-22/84)

M. Keith | R. Siracusa
A Complete Software Implementation of NABTS Teletext Decoder—Presented at Conf. Digest of Int'l Conf. on Consumer Electronics

H.P. Kleinknecht | H. Meier
Optical Profilometer for Monitoring Surface Contours of Si Power Devices—Reprinted from *SPIE Vol. 398–Industrial Applications of Laser Technology* (1983)

W.F. Kosonocky
Visible and Infrared Solid-State Image Sensors—Published in the *Proceedings of IEDM 83*, - 1 (1983)

M.E. Labib | R. Williams
The Use of Zeta-Potential Measurements in Organic Solvents to Determine the Donor-Acceptor Properties of Solid Surfaces—Published in the *Journal of Colloid and Interface Science*, Vol. 97, No. 2 (2/84)

H.W. Lehmann | R. Widmer | M. Ebnoether
A. Wokaun | M. Meier | S.K. Miller
Fabrication of Submicron Crossed Square Wave Gratings by Dry Etching and Thermoplastic Replication Techniques—Published in the *J. Vac. Sci. Technol.*, B 1(4) (10/83-12/83)

H.W. Lehmann
Dry Etching for High Resolution Microfabrication—Published in *Microcircuit Engineering* 83

B.J. Lechner
High-Definition Television—Presented at the EE Department Seminar, Columbia University, New York, N.Y. (4/6/84)

S.G. Liu | S.Y. Narayan
Rapid Capless Annealing of ^{28}Si, ^{64}Zn, and ^{9}Be Implants in GaAs—Published in *Journal of Electronic Materials*

P.A. Longeway | R.D. Estes | H.A. Weakliem
Decomposition Kinetics of a Static Direct Current Silane Glow Discharge—Published in *Journal of Phys. Chem.* (1984)

J.R. Matey
User-Defined Functions for SAS—Published in *SAS Communications*

D.D. Mawhinney
Microwave Tag Identification Systems—Published in *RCA Review*, Vol. 44 (12/83)

D. Meyerhofer | L.K. White
Image Formation in the Sublayer of a Multilayer Resist Structure—Presented at the SPIE Advances in Resist Technology Conf., Santa Clara, Calif. (3/12-13/84)

R.W. Paglione
Miniature Microwave Antennas for Inducing Localized Hyperthermia in Human Malignancies—Published in *RCA Review*, Vol. 44 (12/83)

J.I. Pankove | D.E. Carlson
J.E. Berkeyheiser | R.O. Wance
Neutralization of Shallow Acceptor Levels in Silicon by Atomic Hydrogen—Published in *Physical Review Letters*, Vol. 51, No. 24 (12/12/83)

F. Sechi | R. Paglione | B. Perlman | J. Brown
A Computer-Controlled Microwave Tuner for Automated Load Pull—Published in *RCA Review*, Vol. 44 (12/83)

S.A. Siegel | D.J. Channin
PIN-FET Receiver for Fiber Optics—Published in *RCA Review*

R.K. Smeltzer | C.W. Benyon, Jr.
Dielectric Integrity of Gate Oxides in SOS Devices—Published in *RCA Review*

H.S. Sommers, Jr.
Experimental Study of the Lasing P/N Junction as an Electro-Optical Transducer—Published in the *J. Appl. Phys.*, Vol. 55, No. 5 (3/1/84)

P.J. Stabile | A. Rosen
W.M. Janton | A. Gombar
Millimeter Wave Silicon Device and Integrated Circuit Technology—Presented at the IEEE MTTS Symposium, San Francisco, Calif., and published in *Symposium Digest* (5/29-6/1/84)

P. Stein
Applying Statistics to Real-Life Problems—Presented at Antioch University Colloquium, Yellow Springs, Ohio (4/27/84)

F. Sterzer | R. Paglione
A. Winter | J. Laing | E. Friedenthal
J. Mendecki | C. Botstein
Enhancing the Efficacy of Localized Thermotherapy by Monitoring Changes in Tumor Blood Flow—Published in the *International Journal of Radiation Oncology/Biology/Physics*

F. Sterzer | R. Paglione | J. Mendecki
E. Friedenthal | C. Botstein
Heating Patterns During Cancer Heat Therapy as a Function of Blood Flow—Presented at the 4th Annual Meeting of the North American Hyperthermia Group, Orlando, Fla. (3/24-29/84)

J.H. Thomas, III | R.V. D'Aiello
P.H. Robinson
A Scanning Auger Electron Spectroscopic Study of Particulate Defects in Metallurgical-Grade Silicon—Reprinted from *Journal of the Electrochemical Society*, Vol. 131, No. 1 (1/84)

J.H. Thomas, III
Improved Sensitivity of Backscattered Electron Detection Using Beam Brightness Modulation with Phase Sensitive Detection in Scanning Auger Instruments—Published in the *J. Vac. Sci. Technol.*, A2 (1) (1/84-3/84)

S. Tosima
Surface Acoustic Wave Stylus: Part 2 - Relationship Between Rectangular and Fan-Shaped Interdigital Transducers—Published in the *RCA Review*, Vol. 44 (9/83)

S. Tosima | M. Nishikawa
Surface Acoustic Wave Stylus: Part 3 - Optimum Tip Shape for Pickup Devices—Published in *RCA Review*, Vol. 44 (9/83)

S. Tosima | M. Nishikawa
T. Isawa | E.O. Johnson
Surface Acoustic Wave Stylus: Part 1 - Pickup and Recording Devices—Published in *RCA Review*, Vol. 44 (9/83)

S. Tosima | M. Nishikawa
Surface Acoustic Wave Stylus: Part 4 - Pyramid-Shaped Surface Acoustic Wave Transducer for Signal Recording Cutterheads—Published in *RCA Review*, Vol. 44 (9/83)

J.L. Vossen
Thin Film Technology—Presented in the Frontiers in Chemistry Lecture Series, New Paltz, N.Y. (5/3/84)

C.C. Wang
Heteroepitaxial Growth and Characterization of Compound Semiconductors—Presented at Chemistry Colloquium, State University of New York, Stony Brook, N.Y. (5/4/84)

L.K. White
Advanced Optical Lithography for IC Fabrication—Published in *RCA TREND*

L.K. White
Planarization Phenomena in Multilayer Resist Processing—Published in the *J. Vac. Sci. Technol.*, B1 (4) 1235 (1983)

C.A. Whybark
The Making of a VideoDisc—Presented at the Northeastern Christian Jr. College Science Fair, Villanova, Pa. (4/7/84)

O.M. Woodward
Broadband Balun—Published in *RCA Review*, Vol. 44 (12/83)

C.P. Wu | G.L. Schnable
B.W. Lee | R. Stricker
Improved Conductivity in Polysilicon Films by Pre-annealing—Reprinted from *Journal of the Electrochemical Society*, Vol. 131, No. 1 (1/84)

B.S. Yarman
A Dynamic CAD Technique for Designing Broadband Microwave Amplifiers—Published in *RCA Review*, Vol. 44 (12/84)

Missile and Surface Radar

K. Abend
Seminar Coordinator and Editor of Seminar Lecture Notes—Presented at IEEE Philadelphia Section Educational Seminar: Techniques of Modern Spectral Estimation, University of Pennsylvania, Phila., Pa. (4/7/84)

A. Afrashteh | V. Stachejko
L-Band Phased Array T/R Module—Presented at IEEE AP/MTT-S, Phila., Pa. (3/22/84)

J.A. Bauer | P.N. Bronecke
F.R. Kolc | R.L. Schelhorn
Overview and Application of Surface Mounting Technology - Parts 1 and 2—Part 1, March 1984; Part 2, April 1984. *Electri • Onics*

R.M. Blasewitz
Ada As A Program Design Language—Presented at the Second Annual Conference on Ada Technology, Hampton, Va., and published in *Proceedings* (3/27-28/84)

D.F. Bowman
Impedance Matching and Broadbanding, Chapter 43—Published in *Antenna Engineering Handbook*, Second Edition, McGraw Hill

F.J. Buckley
A Guide to Standards Development for the Software Engineering Standards Subcommittee—Published in *Computers and Standards*, Vol. 2, No. 4 (1983)

F.J. Buckley
IEEE Standard 830-1984—IEEE Guide for Software Requirement Specifications—Printed February 1984

F.J. Buckley
Software Quality Assurance—Published in the *IEEE Transactions on Software Engineering* (1/84)

M.W. Buckley, Jr. | W.C. Grubb, Jr.
Electro-Optics, Fiber Optics, and Lasers for Non-Electrical Engineers—Presented at George Washington University, Washington, D.C. (4/23-25/84)

C. DiMaria
The Robot That Does Windows—Published in *RCA TREND* (2/84)

J.R. Fogleboch
A High-Performance Multiple Algorithm Programmable Processor—Presented at the IEEE National Radar Conference, Atlanta, Ga. (3/14/84)

W.C. Grubb, Jr. | M.JW. Buckley, Jr.
Minicomputers, Microcomputers, and Microprocessors for Non-Electrical Engineers—Presented at George Washington University, Washington, D.C. (2/6-7/84)

D.R. Higgs
Software Documentation—Presented at East Stroudsburg University Computer Science Seminar, East Stroudsburg, Pa. (3/13/84)

M. Niemeyer
Estimation of Coordinate Misalignments—Presented at Modeling and Simulation Conf., University of Pittsburgh, Pittsburgh, Pa. (4/19/84)

F.E. Oliveto
Fault Tolerant Design—Presented at the Fifteenth Annual Reliability Symposium, Phila., Pa. (4/25/84)

W.J. Paterson | C.T. Jorgensen
Problems in Designing a VLSI Based Computer to Meet a Specified Concurrent Fault Detection Capability—Presented at the IEEE Built-In Self Test Workshop, Kiawah Island, S.C. (2/28-3/1/84)

W.T. Patton | J.T. Nessmith
Antenna Engineering Handbook, Second Edition, McGraw Hill

M.D. Rauchwerk
A Microprocessor-Based Floating Point Library—Presented at IEEE Southeastcon '84, Louisville, Ky., and published in the *Proceedings* (4/11/84)

S.M. Sherman
Monopulse Principles and Techniques—Published by Artech House, Inc., Dedham, Mass.

M. Weiss
Modal Testing in the Performance Verification Process of Shipboard Equipment—Presented at the 2nd International Modal Analysis Conf., Orlando, Fla., and published in *Proceedings* (2/5-10/84)

F.E. Wuebker
Design Experiences from the Multilevel Secure MCF Operating System—Presented at IEEE Symposium on Computer Security, Oakland, Calif. (4/23-24-25/84)

F.E. Wuebker
Military Computer Family Operating System: An Ada Application—Presented at Second Annual Conf. on Ada Technology, Hampton, Va., and published in *Proceedings* (3/27-28/84)

F.E. Wuebker | J.O. Neilson
Design Experiences from the Multi-Level Secure MCFOS—Presented at IEEE 1984 Symposium on Security and Privacy, Oakland, Calif., and published in *Proceedings* (4/84)

NBC

J. Gibbings
Stereo Audio Production for Television—National Association of Broadcasters Annual Convention and International Exposition, Las Vegas, Nev. (4/28-5/3/84)

P. Smith
The Status of Teletext in North America—Special session of the North American National Broadcasters Association (NANBA) Technical Committee, Las Vegas and Los Angeles (5/2-5/84)

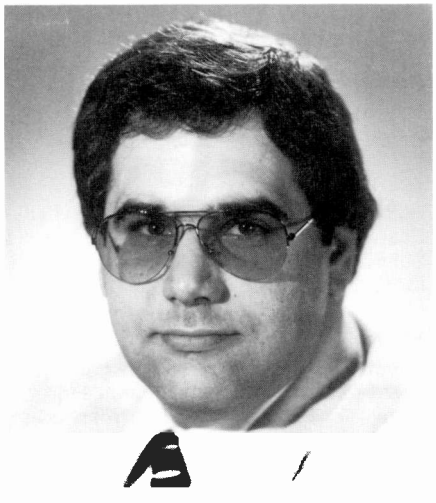
Solid State Division

G. Dolney
Using the SPICE Computer Program as a Circuit Design Aid—A twelve-week course presented at Wilkes College

H.R. Ronan, Jr. | C.F. Wheatley, Jr.
Power MOSFET Switching Waveforms: A New Insight—Presented at Eleventh Annual International Power Electronics Conf., Dallas Tex., and published in *Proceedings* (4/10/84)

Engineering News and Highlights

Steven Bonica becomes Vice-President, Engineering, NBC



Steven Bonica has been named Vice-President, Engineering, it was announced by **Michael J. Sherlock,** Executive Vice-President, Operations and Technical Services, NBC. Bonica will report to Sherlock. In his new position, Bonica will act as Chief Engineer for the NBC Television Network. His areas of responsibility will include systems engineering, technical development, video imaging systems, and frequency coordination of allocations.

Most recently, he had been Director, Broadcast Systems, Engineering, NBC, since July, 1982. In that post he was responsible for the design and implementation of all television broadcast facilities for the National Broadcasting Company in New York. Before that he was Director, Videotape Operations, Network News.

Bonica began his professional career at NBC in January 1969, in the News Film Department as an Editing Room Assistant. He later became an Assistant Film Editor, then Film Editor. During his seven years in News Film, his editing assignments took him to Europe, South America, Russia, Africa, and Southeast Asia.

In 1976, he became a Videotape Engineer in the Operations Department. Later that year, he moved to the Electronic Journalism Department as an editor of videotape. He was a supervisor when he left EJ in 1980 to rejoin the News Department as a Technical Planning Manager. His responsibilities in that position included the planning and development of future news-editing systems and the organization and supervision of videotape operations for coverage of the Republican and Democratic National Conventions.

In 1981, he became Manager, Videotape Operations, Network News, and subsequently, Director. Born and raised in New Jersey, Bonica studied electronic engineering at Fairleigh Dickinson University.

Herman Heads Solid State Technology Center

John M. Herman, III has been appointed Division Vice-President in charge of the Solid State Technology Center in Somerville, N.J. The technology center is part of RCA Government Systems Division and primarily designs and manufactures major systems for the Department of Defense and other federal agencies. Dr. Herman reports to **James B. Feller,** Division Vice-President of Engineering for GSD.

Dr. Herman's operation engages in the development of technology and the fabrication of integrated circuits for the business units in the Government Systems and the Solid State Divisions.

Herman will also oversee SSTC's other operations, which include custom and semicustom design, program management, package/assembly, test, computer-aided design, design automation, and photomask development.

Prior to his appointment, Dr. Herman was SSTC's Director of VLSI Manufacturing Technology. Dr. Herman joined RCA in 1982 as the Director of Integrated Circuit Design and Process Development. Before joining RCA, Dr. Herman held several engineering and management positions with Texas Instruments, Inc. He was elected a senior member of that company's technical staff in 1980. Dr. Herman holds two patents for fabrication methods on high-performance, bipolar logic circuits using Schottky diodes. Dr. Herman received his bachelor and master of science degrees from Southern Methodist University, and his doctorate degree from the University of Illinois.

Miller named Chief Engineer at RCA Government Communications Systems

The appointment of **Donald D. Miller** as Chief Engineer was announced by **Lawrence J. Schipper,** Division Vice-President and General Manager at RCA Government Communications Systems. Mr. Miller came to RCA from the ITT Defense Communications Division in Nutley, N.J., where he was Vice-President and Director, Strategic Communications Systems, and had been employed since 1975.

Previously, Mr. Miller worked for six years at General Electric, Pittsfield, Mass., as a group leader in mechanical engineering. Born in Los Angeles, Mr. Miller received a bachelor's degree in mechanical engineering from the California State Polytechnic Institute at San Luis Obispo, and master's degrees in mechanical engineering and management from Rensselaer Polytechnic Institute.

Elliot heads new Americom marketing group for business networks

RCA American Communications, Inc., announced the formation of a new group for the development and marketing of business networks via its Satcom satellite system. The new group will be headed by **Dennis W. Elliott,** Vice-President, Business Networks. His organization will include sales, technical and business personnel responsible for marketing, design, installation and service of specialized networks for business.

Mr. Elliott brings to the new service offering an extensive background in engineering, business analysis, marketing, and finance. According to **Dr. James J. Tietjen,** President of RCA Americom, Business Networks will focus primarily on digital network offerings ideally suited for satellite transmission, and falling within transmission rates from 9.6 kilobits per second to 1.544 megabits per second. The offering will also focus on and expand RCA Americom's 56 Plus Service (56 kbps), which has been transferred to the new group from Commercial Communications Services.

Staff announcements

Executive Vice-President Staff

Roy H. Pollack, Executive Vice-President, announces the appointment of **Jay J. Brandinger** as Staff Vice-President, Systems Engineering. In this capacity Dr. Brandinger will report to Roy H. Pollack organizationally and to **Dr. William M. Webster,** Vice-President, RCA Laboratories, on a functional basis.

Roy H. Pollack, Executive Vice-President, announces the following appointments on his staff: **Carl R. Turner,** Division Vice-President and General Manager, Solid State Division; **Robert S. Pepper,** Vice-President, Business Development; and **Gordon W. Bricker,** Staff Vice-President, Planning.

Americom

James J. Tietjen, President and Chief Operating Officer, RCA American Communications, Inc., announces his organization as follows: **John Christopher,** Vice-President, Technical Operations; **Dennis W. Elliot,** Vice-President, Business Networks; **Harold W. Rice,** Vice-President, Video and Audio Services; **Robert E. Smylie,** Vice-President, Government Communications Services; **James J. Tietjen,** Acting, Employee Relations;

James J. Tietjen, Acting, Finance; and **Jack F. Underwood,** Vice-President, Commercial Communications Services.

Astro-Electronics

H. Soule has been appointed Manager, Antenna Design.

Consumer Electronics

Larry A. Olson, Manager, Manufacturing Technology Center, announces the appointment of **Allen L. Collier** as Manager, Automated Process Development.

James R. Arvin, Manager, Quality Control, announces the appointment of **Robert A. Straub** as Manager, Production Quality Control.

Globcom

William A. Klatt, Director, Network Operations, announces the organization of Network Operations as follows: **Joseph D. Ciaccia,** Manager, KCC TOCC and Trouble Reporting Center; **John A. Kruk,** Manager, Gateway Operations; **Eugene B. Stanley,** Manager, KCC Plant Services; and **John P. McIntyre,** Administrator, Data Management Projects.

John P. Shields, Director, Network Engineering, announces that the Engineering Systems Development function has been transferred from Leased Facilities and Systems Operations to the staff of the Director, Network Engineering.

RCA Service Company

Donald M. Cook, President, RCA Service Company, announces the following appointments in his organization: **Earle A. Malm, II,** is appointed Division Vice-President, Automated Business Communications Services. In this capacity, Mr. Malm will be responsible for planning, developing, evaluating, and test marketing all new voice and/or data communication systems and will continue to be responsible for the Data Services business. **Raymond J. Sokolowski** continues as Division Vice-President, Consumer and Commercial Services, and will also assume responsibility for the Telephone Systems business.

Donald M. Cook, President, RCA Service Company, announces the appointment of **Michael F. Camardo** as Division Vice-President, Government Services.

Solid State Division

Jon A. Shroyer, Division Vice-President, LSI and Technology Development, announces the appointment of **Martin A. Blumenfeld** as Principal Member of the Technical Staff. Mr. Blumenfeld will report to **Ian Arnott,** Manager, Wafer Fab Operations.

Stephen C. Ahrens, Director, Engineering—Standard Integrated Circuit Products Engineering, announces his organization as follows: **Sushil K. Chawla,** Manager, Telecommunications System Design; **Charles Engelberg,** Manager, Test Engineering; **Merle V. Hoover,** Manager, Engineering—Computer, Telecommunications and Industrial Products; **Lewis A. Jacobus,** Manager, Engineering—Logic Products; **Sterling H. Middings,** Section Manager—Layout Services; and **Bruno J. Walmsley,** Manager, Engineering—Automotive and Consumer Products.

VideoDisc Division

Arnold T. Valencia, Division Vice-President and General Manager, VideoDisc Division, announces the appointment of **Harry Anderson** as Division Vice-President, Disc Operations.

Professional activities

RCA Laboratories achievement awards given

Dr. William M. Webster, Vice-President, RCA Laboratories, Princeton, N.J., announced that the following engineers and scientists have been given RCA Laboratories Outstanding Achievement Awards for contributions to electronics research and engineering during 1983. Recipients of individual awards are:

Robert A. Duschl, for outstanding performance in conception, development, and implementation of a manufacturing inspection system for in-process automated evaluation of color picture tubes.

Lorenzo Faraone, for contributions to the understanding and control of tunneling current through thin thermally grown silicon dioxide layers of silicon devices.

Krishnamurthy Jonnalagadda, for analysis work to accurately predict the performance of voice and voice-band data circuits in the RCA single-sideband system.

John H. Thomas, III, for contributions in the areas of Auger electron spectroscopy and x-ray photoelectron spectroscopy and their use in wide areas of materials characterization research.

Edward H. Adelson, Charles H. Anderson, James R. Bergen, Curtis R. Carlson, and **Albert P. Pica,** for contributions to the development of advanced signal-processing concepts that match properties of the human visual system.

Victor Auerbach, Thomas Y. Chen, Walter G. Gibson, Thomas F. Lenihan, and **Charles M. Wine,** for contributions to the development of the first CED random-access interactive VideoDisc player.

William E. Babcock, William E. Rodda, Walter Truskalo, and **Werner F. Wedam,** for contributions to the development of a 13-inch-diagonal high-resolution computer monitor prototype with switchable scan rates.

William J. Bachman, Robert R. Demers, Nitin V. Desai, Robert W. Jebens, Frank R. Reed, and **Gerard Samuels,** for contributions to the development of concepts that have led to an innovative VideoDisc player designed for automated manufacturing at a lower cost.

Donald F. Battson, Walter F. Kosonocky, Peter A. Levine, and **Frank V. Shallcross,** for contributions to the design and development of a high-sensitivity, low-noise CCD imager.

Rodney P. Borchardt, Glenn A. Reitmeier, Terrence R. Smith,and **Christopher H. Strolle,** for contributions to the design and implementation of an advanced computer-based television simulation facility.

Richard Brown, Henry C. Johnson, Adolph Presser,and **Franco N. Sechi,** for contributions to the development and application of a new batch-fabrication process of miniature microwave circuits.

Michael T. Duffy, Michael F. Leahy, and **Jer-Shen Maa,** for contributions in developing methods for the reactive sputter etching and plasma etching of insulating, semiconducting, and conducting elements of integrated circuits.

John R. Fields, Ronald Śverdlove, and **Norman D. Winarsky,** for contributions to the development of a computer program that fully models the electron beam in a picture tube.

Joseph H. McCusker, Sidney S. Seffren, Alan Sussman, Barry J. Thaler, and **Thomas J. Ward,** for contributions leading to innovations in the manufacturability, reliability, and design of high-voltage transformers for TV receivers.

RCA publications sweep competition

The New York Chapter of the Society for Technical Communication honored several 1983 RCA technical and news publications in several categories for their excellence in competition with those from, for example, AT&T, IBM, Western Electric, Ford Foundation, Springer-Verlag, American Physical Society, and more. These awards are continuing signs of the high professionalism of all RCA engineers who write for publication.

- **Periodicals**—*RCA Engineer* magazine (Distinguished Technical Communications Award)
- **Training Manuals**—"Guide for *RCA Engineer* Authors" (Distinguished Technical Communications Award)
- **House Organ**—MSR's *RCA Family* (Award of Excellence)
- **Newsletter**—AEGIS Excellence Newsletter (Award of Merit)
- **Reports**—AEGIS EDM4 Development Award Fee Progress Report (Award of Excellence)
- **Reports**—AEGIS Production Programs Status Report No. 63 (Award of Merit)
- **Publication Graphics-Illustrative**—MSR's "47/51 Parallel Course" (Award of Merit)
- **Single Sheet Designs**—MSR's "Chemical Safety" (Award of Achievement)

Astro professionals serve AIAA

The following members of RCA Astro-Electronics held appointments to American Institute of Aeronautics and Aerospace Technical Committees:

J.N. LaPrade—Associate Member of Committee on Communications Systems

P. Pierce, Principal Member Technical Staff—Aerospace Power Systems Committee

R. Joshi, Senior Member Technical Staff—Astrodynamics Committee

P.G. Goodwin, Manager, Electronic Subsystems Engineering—Computer Systems Committee

R.A. Amadio, Manager, Financial Control—Economics Committee

S.J. Arkuszewski, Member Technical Staff—Ground Testing Committee

R.D. Scott, Staff Engineer—Interactive Computer Graphics Committee

L. Gomberg, Director, Satellite Programs—Management Committee

R.T. Feconda, Member Technical Staff—Solid Rockets Committee

Technical excellence

Indianapolis Consumer Electronics annual awards


Nortrup


Dasgupta


Becker


Benson


Shah

The 1983 Indianapolis Technical Excellence Committee banquet was held on February, 1984. The keynote speaker was **Mr. R.H. Pollack,** Executive Vice-President of RCA. The banquet was attended by over three hundred members of the CED technical community. **Dr. J. Donahue,** CED Vice-President and General Manager, presented the annual awards. **Dr. J.E. Carnes,** Division Vice-President, Engineering, was an after-dinner speaker. The recipients are:

Kevin Nortrup—for the definition and design of a menu-based customer interface to the CTC 141 digital receiver. Specifically, in recognition of outstanding engineering contributions made toward the completion of the engineering prototype system in time for use in a marketing study and for engineering evaluation.

Basab Dasgupta—for the development of a better theoretical understanding of yoke parameters. He has developed a mathematical basis to describe yoke phenomena that has advanced the state-of-the-art of CE yoke design.

Hollis Becker—for the development of a graphics printing process combining inks and a topcoat that produces a highly reliable product. It is used on the unified remote transmitter for J-Line television and VideoDisc products. The wear performance of this process is presently considered superior to CE competition.

Walt Benson and **Kashyap Shah**—for outstanding effort in the design, development, and implementation of CE's first fully automated robotic spray-painting system. This robot is used on portable television cabinets.

RCA Somerville 1983 third- and fourth-quarter award recipients

Larry Rosenberg, *Manager, Design Automation, Solid State Technology Center (left) with (from left to right)* ***Mike Gianfagna, Rich Gopstein,*** *and* ***Joe Mastroianni.***

Bob Geshner, *Manager, Mask Tooling Operations, Solid State Technology Center (left) with (from left to right)* ***Ronnie Toland, Al Shoemaker, Jon Butcher,*** *and* ***George Durante.***

Bob Geshner, *with (from left to right)* ***Steve Preston, Bernie Ostrowski, Mary Evancho, Marie Wendt,*** *and* ***Joe Mitchell.***

Steve Ahrens, *Director, Standard IC Products Engineering, (second from left) with (from left to right)* ***Bob Dawson, Tom Freeman,*** *and* ***Tom Deegan.***

Nick Kucharewski, *Manager, Design Engineering, Solid State Division, (left) with (from left to right)* ***Bob Pollachek, Debbie Petryna,*** *and* ***Dale Barker.***

D. Barker, R. Pollachek, and **D. Petryna,** for outstanding team effort in achieving, on schedule, the design of a family of 64K/128K/256K ROMs. This family far excels competitive product in die size and performance.

I. Wacyk and **D. Alessandrini,** for the design, layout, and testing of a radiation-hard (≥200 Rad Si) 16K SOS RAM, which includes fuse switching of redundant columns for increased yield capability. The RAM was designed to be tolerant of degraded operational parameters so that full functionality can be maintained as long as possible in destructive radiation environments.

M. Gianfagna, T. Deegan, T. Freeman, R. Gopstein, and **J. Mastroianni,** for interdepartmental team work, over a two-year period, that resulted in the specification and development of a symbolic layout system to layout and verify bipolar integrated circuits. The intent of this work was to reduce the number of silicon cuts required to obtain a working bipolar IC. Key elements of this system include the following: symbolic layout and layout compaction computer aids, a parameterized cell library that has been characterized, automatic detection of shorts or opens in a layout, and generation of a circuit description for the layout that includes parasitic devices and is suitable for simulation.

M. Evancho, J. Butcher,S. Shoemaker, R. Hilton, S. Preston, R. Toland, A Frattali, B. Ostrowski, M. Wendt, G. Durante, and **J. Mitchell,** for consistent pursuit of major manufacturing goals of high yield and effective cycle times. Throughout the first and second quarters of 1983, this group exceeded all goals set for it, allowing production of high-quality masks for the factories and pilot lines that has allowed RCA to respond to customer demands and allowed the Engineering design community to test designs and complete difficult reiterative mask sets to prove designs such as AT/MAC, Jelly Bean, "ROM – Express." In June, they produced a global line yield of 99 percent against an aggressive plan of 77 percent, with cycle times of 1.3 to 1.7 days against a commitment of 2.0. On some ROM jobs, cycle times of as little as 12 hours were realized.

GCS announces team technical excellence award

The Technical Excellence Award has been made to the Computer Controlled Equipment Engineering team responsible for the design and development of a 1-MHz Digital Acquisition System under the Unit's Independent Research and Development program. The team members are: **Thomas J. Fritsch; Joseph F. Hoey; Edward A. Timar;** and **Stanley A. Tomkiel.**

This equipment can digitally channelize a 1-MHz bandwidth signal into 160, 8-kHz wide channels (on 6-kHz centers), recognize signals at a 4-dB S/N ratio in an 8-kHz bandwidth, and provide cross-correlation of a multi-pattern signal at a 10-Megabit rate. The project included the development of a special mass storage, interactive controller capable of sustaining a 2.4-Mbit read/write rate in association with a Winchester disc drive.

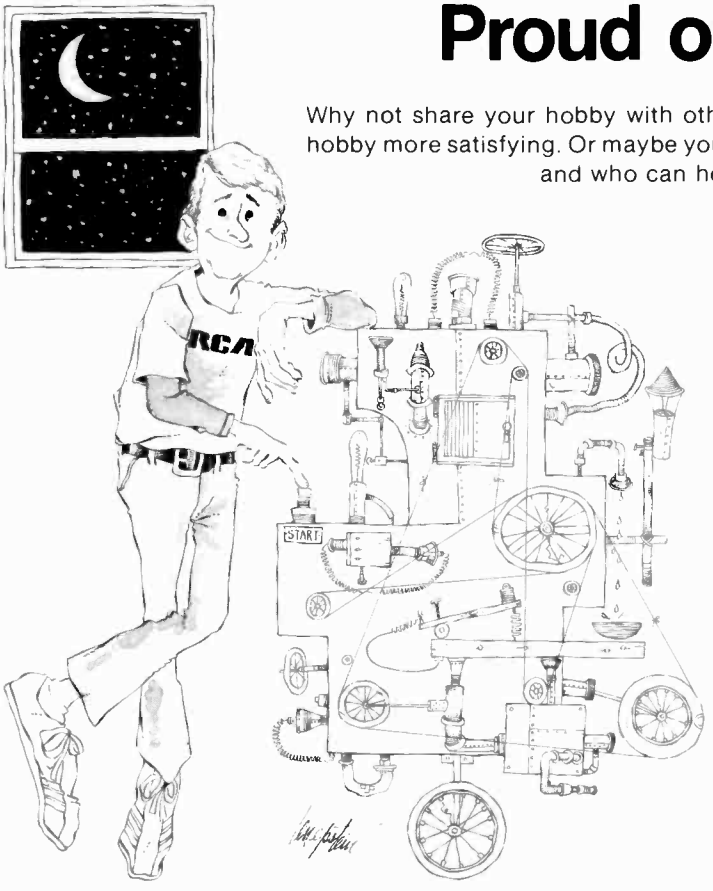
The team's performance in conceiving a two-stage coarse and fine-grain processing architecture to handle a wide range of signal characteristics, and developing an overlap seek and read/write of data in order to record 16 channels and read 2 channels of 125 Kbps real-time data simultaneously was an outstanding example of engineering creativity.

This effort has led to an in-house resource for sophisticated signal-processing equipment, digital filtering and correlation. RCA Government Communications Systems has submitted a sole-source proposal for classified applications of the system that is now included in the customer's 1984 budget and is expected to lead to substantial Navy business in the future.

GCS Chief Engineer, ***D.D. Miller*** *(far left), with Technical Excellence Award winners (from left to right):* ***Joseph F. Hoey, Thomas J. Fritsch, Stanley A. Tomkiel,*** *and* ***Edward A. Timar.***

Proud of your hobby?

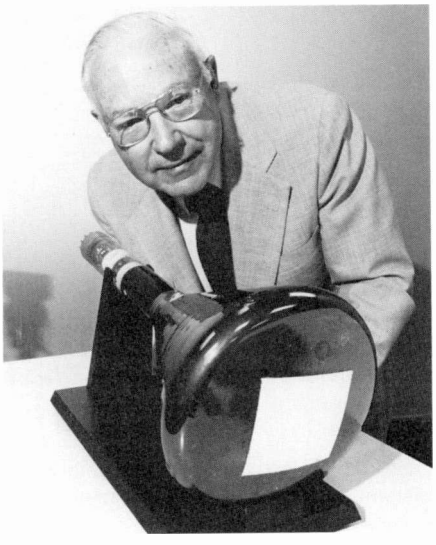
Why not share your hobby with others? Perhaps their interest will make your hobby more satisfying. Or maybe you'll find others who already share your hobby and who can help make your own efforts more rewarding.



The *RCA Engineer* likes to give credit to engineers who use their technical knowledge away from the job. We've published articles about subjects as diverse as a satellite weather station, model aircraft and railroading, solar heating, and an electronic fish finder.

For more information on how you can participate in this feature of the *RCA Engineer*, call your local EdRep (listed on the inside back cover of the *Engineer*) or contact Frank Strobl.

Dr. Harold B. Law, RCA color television pioneer



Dr. Harold B. Law died on April 6, 1984, in Princeton Medical Center. Dr. Law was 72 years old. He was recognized throughout the electronics industry for developing fabrication techniques that led to the first practical shadow-mask color picture tube demonstrated by RCA in 1950. Among his key contributions were the "lighthouse" to simulate the shadowing of electron beams on the tube's faceplate and the corresponding photodeposition of a mosiac of tiny phosphor dots to produce the color picture. Still used today, Law's techniques made possible the hundreds of millions of color TV receivers produced in the last 30 years.

Dr. Law received many honors for his work, both from RCA and from outside professional groups. In 1979, he was elected to membership in the National Academy of Engineering of the United States of America, the highest professional distinction that can be conferred on an engineer.

Born in Douds, Iowa, but raised in Kent, Ohio, Dr. Law received B.S. degrees in Liberal Arts and in Education, both in 1934, from Kent State University. He earned M.S. and Ph.D. degrees in Physics from Ohio State University in 1936 and 1941, respectively. In 1959, Dr. Law received a citation from Kent State as an outstanding graduate. He was to receive an Honorary Doctorate from Kent State at the 1984 graduation ceremonies.

Dr. Law joined the RCA Corporation in Camden, N.J., in 1941, working on television camera tubes. He transferred to the newly established RCA Laboratories in Princeton in 1942, and was one of three RCA researchers honored by the Television Broadcasters Association in 1946 for the development of the image orthicon camera tube, the "technical accomplishment of the year."

He was named a Fellow of the Technical Staff of RCA Laboratories in 1960 and two years later, was appointed Director of the RCA Electronic Components Materials and Display Device Laboratory. He retired in 1976.

In 1955, the Institute of Electrical and Electronics Engineers (IEEE) awarded Dr. Law the Vladimir K. Zworykin Television Prize and in 1975, the Institute presented him the Lamme Medal "for outstanding contributions in developing color picture tubes, including the fabrication techniques which made color television practical." Dr. Law was a Fellow of the Society for Information Display (SID) and in 1975, received the SID Frances Rice Darne Memorial Award for his work in color picture tube development.

Harold B. Law: Inventor/Engineer/Manager: 1911–1984

The sudden and unexpected death of **Dr. Harold B. Law** was a great blow to all of his many friends and former colleagues at RCA. Although he was formally retired since 1976, he was a frequent visitor at RCA Laboratories and active in social and community affairs up to the time of his death.

Few engineers have done work that has been seen directly and regularly by more than a billion people; Harold is among them. How many know what's inside a color television set, or how the programs are generated and transmitted? But every color television viewer looks directly at Harold Law's creation, the shadow-mask picture tube screen, and every viewer is affected by those beautiful colors that are displayed on it.

Several publications tell the story of the color picture tube, but the best is the one Harold wrote himself.[1] He tells there how he made the two key inventions—the method of photodepositing a pattern of color phosphors, and the invention of a "lighthouse" for producing the correct light and shadow areas so that these phosphors are positioned in exactly the right place. To Harold, and to all of us who were involved, it has always been an amazing story. First, the early success took place in less than 6 months between 1949 and 1950, and since then the shadow-mask principle and Law's basic techniques have remained dominant for all these 34 years. It's likely that more than 200 million color tubes have been made, with a total economic value far greater than any other single electron device.

Dr. Law's career was well under way at the time of his color tube work. A graduate of Kent State University, with a Ph.D. from Ohio State University, Harold joined RCA in 1941. His early work was on television camera tubes, and he was a member of the team that developed the image orthicon during the war. From the start, Harold showed the characteristics that led to his achievements. He lived by the motto "if at first you don't succeed . . . . ," and he was one of the most dedicated workers in the electron device field. At RCA, he was promoted from the technical staff to Fellow and then to Laboratory Director.

Law received many honors but he was a modest man, not at all changed by this imposing array of accolades. There is, however, one more award, which Harold was told about, but had not yet received. Kent State was to bestow an honorary doctorate on him at their 1984 graduation ceremonies. Of all his honors, this one pleased him most; Ruth, his devoted wife and helpmate for 42 years, will accept the award for him.

Those of us who saw Harold after retirement know that his activities on a small farm were exactly what he wanted to do. He worked tirelessly on garden, fruit, and vegetable plots; he used his technical expertise to solve problems at home, at his church, in the community, and among neighbors. His last years were happy and contented ones.

—Edward W. Herold

1. Harold B. Law, "The Shadow-Mask Color Picture Tube: How It Began," *IEEE Trans. on Electron Devices*, Vol. ED-23, pp. 752-759 (July 1976). Also in *RCA Engineer*, Vol. 22, No. 1, pp. 88-94 (June/July 1976).

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