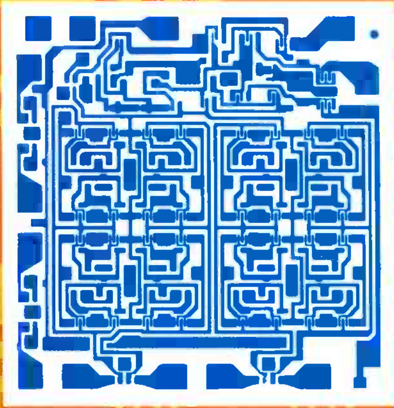
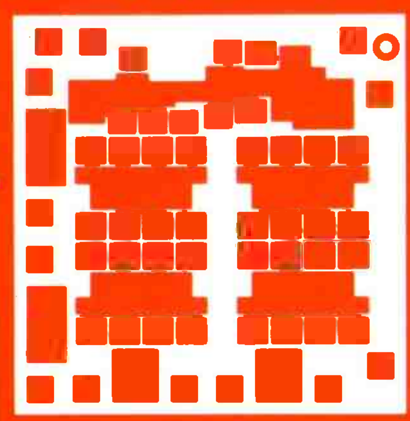
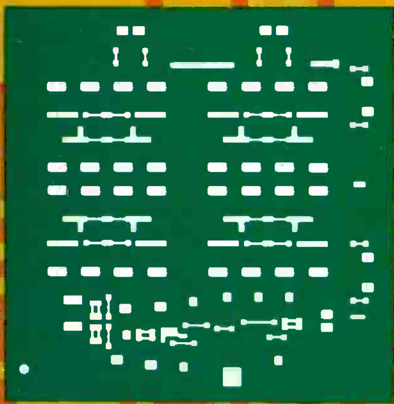
RCA ENGINEER







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OUR COVER

The photomasks that provide a colorful background for this cover typify masks used in fabricating the integrated circuit arrays described in this issue. The engineer-authors standing beside a test set used for automatic probing of integrated circuit arrays are Mike D'Agostino (front) and Borys Zuk of the Array Design Group, Electronic Components and Devices, Somerville, N. J.

Integrated Circuits— A Fascinating Challenge

Integrated circuits—one of the fastest growing technologies that the electronics industry has encountered—will affect every facet of our business. Traditional methods of interface between the component engineer and the circuit engineer are changing. Circuit engineers must become more familiar with what can and cannot be accomplished with integrated circuits. Likewise, the integrated-circuit component engineer must become more knowledgeable of circuit requirements and trade-offs permitted by this new technique. Undoubtedly, whole new circuit concepts will evolve which can be achieved only with integrated circuits.

Engineers and management alike are trying to find the best interface between systems and integrated circuits, and it is doubtful that any one method will prove to be the best. However, the systems-circuit engineer who becomes skilled in creating circuit layouts that can be used directly to make masks for chip processing will have an advantage over the engineer who does not understand this approach. The integrated-circuit component engineer who understands the requirements of circuits and systems will be better able to evolve optimum integrated-circuit components to help meet these needs.

In brief, the dialogue and interface between component and circuit engineers must become very close for the best solutions to their respective problems. Fortunately, electronic engineers are accustomed to change, and they will surely meet the fascinating challenge of integrated circuits and will create even more outstanding accomplishments.

C. E. Burnett, Vice President and General Manager, Solid State and Receiving Tube Division, Electronic Components and Devices

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A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA**, PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

• To disseminate to RCA engineers technical information of professional value. • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer. • To serve as a medium of interchange of technical information between various groups at RCA. • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions. • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field. • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management. • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

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IN 1966, RCA's sale of manufactured products, accounted for $1.69 billion of the Corporation's total income of $2.56 billion—a lot of dollars and a lot of products. And it took a lot of materials and manufacturing to produce that many products from the designs created by RCA's engineering departments. In all, RCA offers more than 11,000 different products ranging in size from miniature integrated circuits to 175-ton radars.

These 11,000 products are produced by RCA's line divisions. That point should not be forgotten throughout this article, which deals with a corporate staff organization, RCA Manufacturing Services and Materials. If the line divisions manufacture the products, what then is the function of the Staff?

The Engineer and the Corporation

RCA MANUFACTURING SERVICES AND MATERIALS

A. L. MALCARNEY
Executive Vice President
Manufacturing Services and Materials

Stated simply, the Staff provides a number of specialists (about 50)—skilled and knowledgeable in manufacturing, purchasing, and facilities—who are always ready to assist their counterparts in the product divisions on jobs or projects that are different than what the division normally handles. Whether the assistance takes the form of problem solving or passing on to one division some beneficial knowledge acquired by another division or by industry in general, the job is to work with the line divisions to help them achieve their goal—the profitable sale of RCA products manufactured from the designs of RCA engineers. As readers of the RCA ENGINEER should know, the best engineered product in the world can have little value to the Corporation unless is can be manufactured and sold at a competitive price. Thus, anything we can achieve in concert with the divisions that will make our products cost less and be more desirable to the customer and more profitable to the Corporation strengthens all of RCA.

ORGANIZATION

There are three major functions in the Manufacturing Services and Materials organization (Fig. 1): Materials, Facilities, and Manufacturing. The first is headed by George A. Fadler, Staff Vice President, Materials, the second by Frank Sleeter, Vice President, Facilities, and the third by Robert A. Schieber, Staff Vice President, Manufacturing.

Basically, the function of Mr. Fadler's activity is to assist the divisions in obtaining the best materials for the job at reasonable prices. His men are also concerned with the transportation and warehousing.

Mr. Sleeter's group is concerned with RCA's world-wide physical facilities (such as, buildings, grounds, telephones, and food services) and construction programs.

Final manuscript received July 21, 1967.

Mr. Schieber's activity assists the divisions in applying the modern manufacturing processes, machinery, and controls needed for efficient, low-cost production. All of these activities very directly affect our ability to compete successfully and profitably. The work is quite specialized and often quite complex. In the following paragraphs we will try to give you some idea of the nature and scope of the work involved.

MATERIALS

The Staff Materials organization under Mr. Fadler has a number of subdivisions:

- Purchasing;
- Transportation, Warehousing, Packaging, and Physical Distribution;
- Value Analysis and Purchasing Research;
- Production Planning and Materials Control; and
- Critical Materials Support.

Purchasing

Purchases last year by the product divisions totaled more than $800 million. If you check *Fortune* magazine's 1966 list of the 500 biggest businesses in the United States, you'll find that 316 of them had total sales less than $800 million. In other words, RCA's purchasing effort is big business, and the effectiveness of our purchasing is easily translated into profit dollars.

Most of RCA's purchasing is done by divisional purchasing men. The function of the Staff Purchasing directors is to establish RCA purchasing policy and practices, and to provide overall guidance and assistance to the divisional purchasing men to make certain that RCA receives maximum value for our purchasing dollars.

A prime example of Staff Purchasing's work is the negotiating of corporate or volume purchasing agreements. Many RCA divisions need to buy such things as resistors, connectors, capacitors, fuel oil, industrial gases, stationery, etc. It makes sense, and saves money, for us to take advantage, where possible, of our large buying power for such items by dealing with the vendors as a Corporation rather than as individual divisions.

We purchase about 18 million gallons of fuel oil annually for RCA plants in New Jersey and Pennsylvania under a volume purchasing agreement—the price per gallon decreases as the total consumption increases. Incidentally, the total corporate consumption of fuel oil is about 25 million gallons a year.

Similarly, we purchase 690 million cubic feet of industrial gases annually. These are mainly argon, hydrogen, oxygen, and nitrogen. And just one more impressive statistic is RCA's annual utilization of approximately 350 million feet of hookup wire and cable and nearly 10 million pounds of magnet wire.

Allied with this volume buying there is also market and commodity research. For example, if research indicates that a particular item will, for any of a number of reasons, become scarce and expensive, Staff Purchasing attempts to find a substitute material or a guaranteed supply.

For instance, there is one man who keeps abreast of developments in the integrated circuit market, so that RCA purchases of IC's will represent maximum value. IC's may be miniature, but RCA's purchases of them (including IC's bought from RCA activities) is not. The total industry IC sales in 1966 have been estimated at $148 million, with RCA buying approximately 12% ($18 million) including IC's bought from EC&D.

Another illustration is that last year, despite a worldwide copper shortage, through the combined effort of divisional and staff purchasing men we were able to work with the

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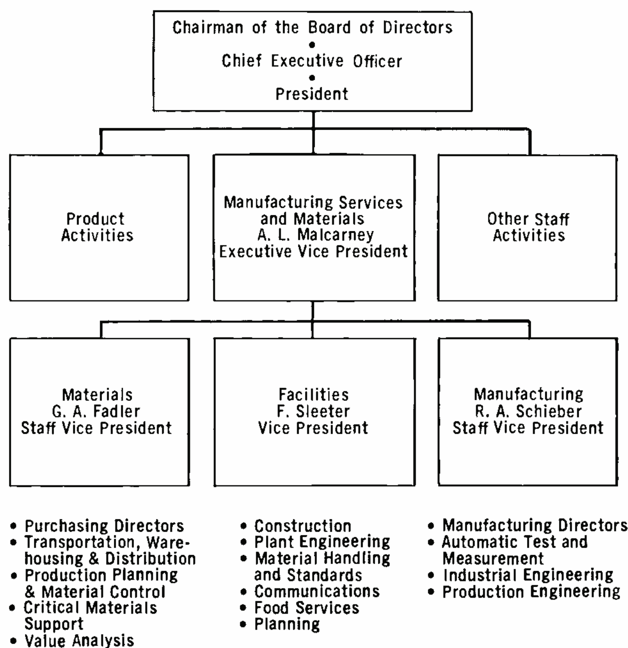

Fig. 1—Manufacturing services and materials organization.

ARTHUR L. MALCARNEY was appointed Executive Vice President of the newly established Manufacturing Services and Materials organization of the Radio Corporation of America on January 1, 1967. He has been a member of the RCA Board of Directors since December 1, 1961. Mr. Malcarney had previously been Group Executive Vice President since May 15, 1962, with over-all responsibility for the Defense Electronic Products, Electronic Data Processing, Graphic Systems Division, and Manufacturing Services activities of the Corporation. Mr. Malcarney joined RCA in 1933 as an inspector in the Camden, New Jersey, plant. Between 1936 and 1940, he was successively assistant foreman, foreman, and superintendent in various component manufacturing activities. He became Manager of the Parts Fabrication Department in 1942, and was named Manager of Production two years later. In 1946, Mr. Malcarney was appointed Parts Plant Manager and was advanced to General Plant Manager of the former Engineering Products Division in the following year. He remained in this position until 1953 when he was made Manager of Production for the Division. He became Manager of Commercial Electronic Products in October, 1955; Vice President, Commercial Products, in June, 1956; and Vice President, Defense Electronic Products, in June, 1957.

vendors so successfully that no RCA production line was stopped at any time because of that copper shortage.

Speaking of vendors, this is a good point to state RCA's purchasing policy as it applies to them. In essence we try to establish a mutually beneficial relationship. While we expect them to make a profit in their dealings with us, we feel they must remain competitive in cost, quality, and delivery of their products. When this is the case, it is obviously in our interest to have continuing associations with them, thus avoiding the problem of having to secure a new vendor for each procurement.

Transportation, Warehousing, and Physical Distribution

With RCA's overall transportation costs exceeding $30 million a year, a major function of the Transportation, Warehousing, and Physical Distribution activity is to assist our divisions in having their raw materials and finished products transported as inexpensively, quickly, and safely as possible. As in other staff areas, the basic responsibility in transportation falls on the product divisions. But RCA Staff Transportation works with the divisions and coordinates their efforts for the best interests of the Corporation.

One way this has been done is in the establishment of freight consolidation centers in major RCA purchasing areas. There is a center in New Market, New Jersey, for the North Jersey-New York area; one in Chicago for that area; and one in Camden for the Philadelphia area. Incoming materials from vendors in these areas are shipped to the consolidation centers rather than directly to the plants. Solid loads are then hauled by RCA's own trucking fleet to the respective plants. RCA's manufactured products are then hauled from the plants back to customers located in the consolidation areas providing the balanced two-way loading required for economical operations.

By far the greatest part of our shipments are carried by railroads and independent motor carriers, with some use of air and ocean freight services. In addition, however, RCA's total vehicle count approaches 4000. Most of these are the vehicles used by the RCA Service Company branches throughout the country, however we also have about 100 tractors and 250 trailers leased for over-the-road operations. Staff Transportation is involved in the negotiations leading to corporate-wide lease arrangements for these vehicles.

Packaging

We can do the best job in the world of engineering and manufacturing a product, sell it competitively, and ship it quickly, but if it arrives damaged, we've lost the ballgame, or at least the profit on that particular item. That's why Staff Transportation, Warehousing, and Physical Distribution has a special activity that deals with packaging our products. A measure of RCA's packaging activities is that last year about $10 million was spent for more than 200 million square feet of corrugated paper board.

Because of the diversity of RCA products ranging from memory cores (30 mils in diameter) to TV sets, computers, and BMEWS sites (which require 60,000 containers to make one shipment)—packaging is a real challenge. There are 35 men throughout the divisions who specialize in the design of protective packaging for our products. To assist these men, RCA Staff maintains a central package testing laboratory in Camden. Here the packaging and the product it protects can be subjected to simulated shipping and storage hazards. In addition, new packaging materials are evaluated and standard packing materials are tested to make certain we are getting what we specify and pay for.

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Value Analysis and Purchasing Research

Value Analysis is a tool for making RCA products more competitive by increasing the worth of the product to the user, relative to its cost. It depends on getting the right people together at the right point in time.

Cost reduction alone can increase value by keeping the worth of a product constant while lowering its cost. Similarly, product improvement alone can increase value by increasing the product's worth. Simultaneous achievement of product improvement and lower cost are what the value analyst tries to accomplish.

As practiced at RCA, value analysis does not pretend to do or to correct the work of designers, buyers, or production men. These specialists apply their skills to their usual tasks. But in a value task group, they apply them jointly and often concurrently, thus achieving substantial gains because, being together, they can appreciate the impact of each of their specialized decisions on the product.

Production Planning and Material Control

Another function of RCA Staff Materials is Production Planning and Material Control. This is a relatively new function directed at assisting the divisional production activities to provide better customer service, with less inventory, and with the most efficient plant operation possible. These three objectives work against one another unless they are properly balanced through a practical system of planning and control.

Production Planning develops production schedules in support of sales and inventory objectives as well as plant capabilities. It tracks production performance and identifies problems that impede accomplishment of production and cost goals. Material Control provides services for the handling, storage, protection, and accountability of material acquired to support production plans.

FACILITIES

Before we can manufacture anything, we must have a place to do it in. And that's what RCA Staff Facilities is all about. The activity is made up of engineers and specialized personnel who serve the Corporation, providing consulting services and administrative guidance in seven areas—construction, plant engineering, communications, material handling, facility planning, food services and standards.

Construction

Table I shows that in the last five years RCA added 4.9 million square feet. This includes 2.6 million square feet added through the expansion of existing facilities and 2.3 million square feet in new construction. The most recent new plant additions are the EC&D color kinescope plant at Scranton and the Home Instruments plants in Indianapolis and Memphis.

RCA now has 36 manufacturing plants in 32 cities in 12 states. New Jersey with nine plants and Indiana with five are the heaviest populated with RCA production facilities.

The 36 RCA plants with their associated warehouses occupy a total of nearly 18 million square feet of floor space—enough room to play 1000 football games at the same time. (The total for the entire Corporation is about 22 million square feet.) The 36 plants are located on approximately 3000 acres of ground or about five square miles.

Selecting the best site for a new RCA plant has become an exacting science, with hundreds of factors being considered before the community or specific location is finally picked. Complete studies are made of many sites in a carefully selected group of states and communities. Teams of experts subject each site to searching examinations, scoring them on pre-determined factors such as schools, climate, highways,

TABLE I—Expansion of Facilities—1962 through 1967 (Square Feet of Floor Space)

Location & Product Division	*Expansion of Existing Facilities*
Lancaster, Pa. (TV Picture Tube)	481,000
Bloomington, Ind. (Home Instruments)	750,000
Indianapolis, Ind. (Home Instruments)	290,000
Indianapolis, Ind. (Records)	241,000
Indianapolis, Ind. (Magnetic Tape)	60,000
Marion, Ind. (TV Picture Tube)	352,000
Mountaintop, Pa. (Solid State & Rec. Tube)	86,000
Findlay, Ohio (Solid State & Rec. Tube)	65,000
Somerville, N. J. (Solid State & Rec. Tube)	126,000
Palm Beach Gardens, Fla. (E.D.P.)	130,000
Monticello, Ind. (Home Instruments)	26,000
Needham, Mass. (Memory Products)	35,000
Subtotal	2,642,000
	New Construction
Palm Beach Gardens, Fla. (Solid State & Rec. Tube)	25,000
Lewiston, Maine (Solid State & Rec. Tube)	116,000
Scranton, Pa. (TV Picture Tube)	300,000
Princeton, N. J. (Graphic Systems)	25,000
Memphis, Tenn. (Home Instruments)	1,200,000
Indianapolis, Ind. (Home Instruments)	620,000
Subtotal	2,286,000
Total	4,928,000

local government, taxes, availability of workers, housing, community services, etc.

Once a site is selected, and funds approved by the Board of Directors, Facilities engineers and specialists sit down with the division involved and work out the layouts, construction schedules, and the many other details involved in getting the project underway, including awarding of contracts for architectural and construction work.

Each of the other activities in RCA Staff Facilities are called upon to contribute their part to the planning of the new plant, including the telephone and telegraph system, food services, material handling, and plant engineering services.

Considerable attention is given to the plant's architectural features—the outside appearance of the building. RCA's policy is to build facilities that are an asset to the community and to maintain our reputation of being a good neighbor.

Working with the various divisions and subsidiaries in new building projects constitutes only a part of the day's work for Facilities personnel.

On a day-to-day basis, the men are busy assisting the divisions in many projects ranging from tests of a new type of paint or floor cleaner to installation of a new conveyor or warehousing systems to the expansion of the dial telephone facilities or to rearrangement of the cafeteria to accommodate a few hundred more employes.

Food Services and Phones

Two services which probably touch the lives and affect most individual employes are those of food services and telephones. Under the guidance of the Staff Food Services activity, 19 of our plants operate RCA-owned cafeterias. Others have contracts with professional food concessionaires or are serviced through automatic vending machines. About 70,000 meals are served each day in RCA cafeterias, dining rooms, and other food areas.

In the area of communications, RCA operates one of the most extensive private telephone-teletype systems of any company in the world. General supervision and direction of the

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system, which reaches into every state and into Canada, is the responsibility of Staff Communications.

RCA's Interlocation Dial Network (IDN) enables an operator at any of the 49 RCA plants or offices on the network to dial directly to another telephone anywhere in the United States or Canada without intervention by another RCA or commercial telephone operator. More than 2.4 million calls were made on the IDN last year, and the phone bill exceeded $15 million, exclusive of the expenses involved in a vast network of commercial lines required by NBC and RCA Communications, Inc.

Materials Handling

Materials Handling is another activity of RCA Staff Facilities which provides specialized assistance to all of our plants, warehouses, and distribution centers. Assistance is given divisions in designing new plants and warehouses so that they will have an efficient, low-cost system for handling raw materials, parts, work in process, and finished goods. Working with material handling people in all RCA locations, Materials Handling spearheads a company-wide program of cost reduction which last year saved the company more than $3 million.

Plant Engineering

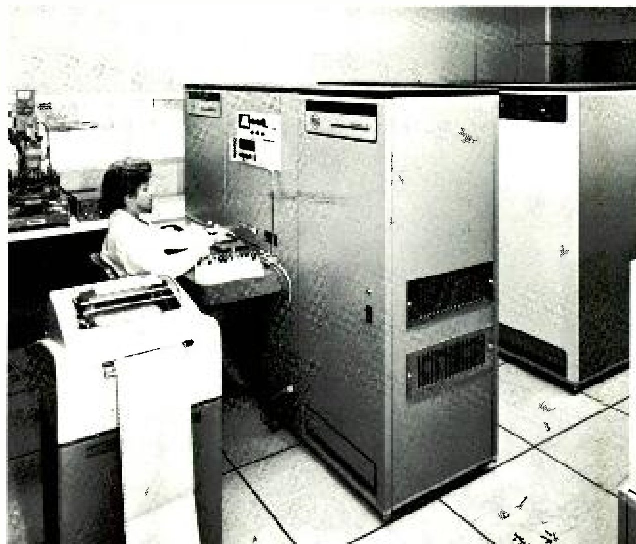
Staff Plant Engineering works with the various plant engineers on problems related to plant maintenance, safety, and pollution control.

In 1962, the Facilities Staff assisted the product divisions in a long range, comprehensive Maintenance and Repair Program. Designed to provide modern and effective methods for the repair and maintenance of RCA buildings, machinery and equipment, this program had by 1966 reduced the overall maintenance and expense by 13 cents per square foot. Thirteen cents a square foot doesn't sound like much until you multiply it by the 18 million square feet occupied by the product divisions and then it exceeds $2 million a year. These savings were accomplished despite rising material costs and a 58-percent increase in labor costs.

Standards

The establishment of corporate standards for many items of furniture and equipment used in administrative, engineering and production areas is the responsibility of the Facilities Standards activity.

All types of items ranging from typewriters and desks to shelving, work benches, and lift trucks are constantly being evaluated and established as standards for use throughout the Corporation. At present there are more than 150 approved items on the list.



Computer controlled integrated circuit tester in Somerville.

MANUFACTURING

Manufacturing at RCA covers a broad spectrum. At one extreme the finished product is built up from an engineering design by assembling and testing discrete components. The other extreme is where the product is made by chemically and mechanically processing materials in order to give it special properties. In one case you can make a repair by replacing a component; in the other, you have to throw it away. An integrated circuit is an example of the latter—a TV tuner of the former.

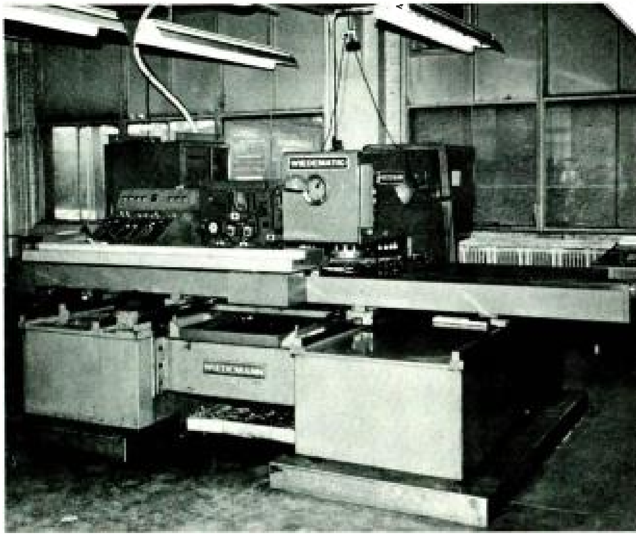
This full range of manufacturing falls under the purview of Staff Manufacturing headed by Mr. Schieber. The staff functions reporting to him are: Production Engineering, Industrial Engineering, and Automatic Test and Measurement Systems.

Production Engineering

As a new product progresses from research through advanced development and then into production, the division faces the question of how manufacturable it is. Are the mechanical parts designed so that they can be machined by straightforward methods? Will there be much raw material scrapped? What kind of tooling is required for the specified raw material and can the tolerances be met?

Machining and parts fabrication is just part of the picture

Color kinescope plant in Scranton.



Wiedematic N/C turret punch press in Camden. This 15-ton press punches 60 holes/minute in ⅜-inch steel material and has a table travel of 600 inches/minute.

you also have to look at assembly. Are the parts designed so automatic assembly machines can be used? Will the volume warrant the design of special equipment, and if so, what is the best way of getting it and how many will be needed?

Staff Production Engineering helps the divisions answer these questions. The activity makes it possible for a division to take advantage of the knowledge and experience gained in production engineering work throughout the Corporation and even in other companies and industries.

For example, high impact extrusion techniques used in the auto industry to make valve lifters have been recommended to an RCA division for forming a certain copper part. Making the part with regular screw machine techniques would require a great deal of machining and result in a lot of raw material scrap. High impact extrusion on the other hand will reduce material costs by 40 percent.

Industrial Engineering

While walking through a plant a manufacturing man invariably asks: "How efficient is it?" In other words, for every 100 items you set out to produce—whether they're transistors, radar equipments, or TV sets—how many are shipped? In RCA, where we make so many different products ranging from some "never previously produced" to others "in volume production for several years," obviously some of our plants are relatively more efficient than others, and none is perfect. The job of Staff Industrial Engineering is to assist all RCA plants in becoming more efficient producers.

At the request of the divisions, manufacturing studies are performed to get at the root of problems. If the symptom is high costs, it could be because there is high personnel turnover; or the flow of materials to the assembly line might be uneven, causing expensive waiting time; or the line might be out of balance, causing overloads for some operators.

Another function of Staff Industrial Engineering is to assist with labor and overhead controls; this involves the development, installation, application, and monitoring of measurement programs for direct and indirect labor. It is possible to set scientifically based standards for manual motion times and even mental process times for every manually controlled motion likely to be encountered in a work situation. Efficiency can then be measured by checking performance against the standard. In 1966, time standards courses were attended by more than 200 employees at fifteen different RCA plants.

A continuous educational effort has also been conducted on Work Simplification—an organized way of using teamwork and common sense to find and apply better ways of doing things. Over 5200 employees have received this training that contributes to lowering the costs of RCA products.

Automatic Test and Measurement Systems

During the last decade, the demand for automatic test equipment has accelerated greatly. The complexity of present products and their subassemblies make testing by yesterday's methods too slow and too costly. The test specialist, even though better trained than his counterpart a decade ago, cannot check out complex systems in a reasonable time with standard multimeters, oscilloscopes, and bridges. This has created a demand for automatic equipments with capabilities ranging from component to systems testing.

At present, depending upon the product, the cost of testing is 10 to 45 percent of the total labor cost of the product. Reducing this cost and also that of rework and scrap is the objective of the Automatic Test and Measurement systems activity.

The Test activity is working to accomplish its objective by helping the divisions identify opportunities and assisting them in the selection, design, and use of necessary equipment. It sponsors development of conceptually new test equipments and techniques which look like they might benefit more than one division.

RCA is already profiting through the use of automatic test and measurement systems in product testing, and many more benefits can be expected. For example:

The accuracy, precision, and reliability of testing will be increased by eliminating human intervention in establishing test conditions, conducting the tests, and interpreting the results.

Test-station throughout is increased and direct labor costs reduced.

Changeover from one test routine to another is facilitated by use of computer programs with consequent savings in direct labor cost and elimination of operator errors in establishing test conditions and parameters.

MANUFACTURING TRAINING PROGRAM

The importance of manufacturing and the need for topflight personnel in all levels of manufacturing management has led to the start of a corporate-wide training program to develop potential manufacturing managers. New college graduates will undergo a 30-week formal training program of actual working assignments in RCA plants before being assigned to an operating unit.

After a few days of orientation, to be given by RCA Staff College Relations at Cherry Hill, New Jersey, each trainee will be given six 5-week assignments in different RCA divisions. All product divisions are participating.

CONCLUSIONS

RCA's manufacturing plants are the output stages of most of the engineering and research that is done in the company. The products we now make are better than they ever have been before. The reality is that they have to be—customers demand quality at competitive prices, and stockholders deserve profits. The proof is seen in the dynamic, profitable growth of RCA.

As we continue to grow and prosper, there's a need for experienced guidance and exchange of information across the company in the fields of materials, manufacturing techniques, facilities, and other aspects of plant management and operations. The job of Manufacturing Services and Materials is to be always ready to provide this necessary help and guidance to the divisions—just as it is up to the divisions to know what help is available and when to ask for it.

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THE IMPACT OF INTEGRATED CIRCUITS ON ENGINEERING

With the introduction of integrated circuits, the electronics industry started into its third major era—an era which is changing, and will continue to change, the range of knowledge and skills required of device, circuit, and systems engineers. This paper discusses the nature of these changes in engineering, and points out some of the effects of integrated circuitry on the structure of the electronics industry. Also described is the interesting interplay between integrated-circuit technology and another major technological achievement of this decade—the computer.

H. KIHN

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THE ADVENT of integrated circuits has already brought many changes in the methods of design and fabrication of electronic devices and equipment, even though these circuits are at the very early stage of their development and growth cycle. This new technology has had a marked impact both on the engineer and on the devices and equipment he designs. It is important to understand the implications of the integrated-circuit era because, in retrospect, we can assess the profound technical and economic effects of two previous eras in the electronics industry: the vacuum tube and the transistor. The integrated-circuit era represents a truly major trend—not a transitory technological dead end (see the growth curve shown in Fig. 1). There is an increasing transition of discrete-device to integrated-circuit equipment resulting from superior reliability, cost, and performance as well as the advantages accruing from miniaturization. Many defense programs specify integrated circuitry exclusively where such circuit functions are available. The manufacturer of devices, the designer of equipment, and the industrial and defense systems planner are indeed aware of the technical revolution in the electronics industry. This new technology will have a great impact on the device engineer, the circuit engineer, and the systems engineer.

DEVICE ENGINEERING

The device engineer must learn new technologies and refine his present technologies to a degree of precision heretofore deemed impractical. For example, the transistor device engineer, embarking on monolithic integrated circuit activity, must develop sophisticated processes involving precision photolithography and application of computer-controlled mask-making techniques, as well as computer-controlled probing of circuits. He is obliged to encroach on the province of the circuit engineer and learn how to synthesize active devices, such as transistors and diodes, integral with resistors and capacitors, on a common silicon wafer. He must understand new circuit and performance considerations such as fan-in, fan-out, flip-flop, rise time, and pair delay, and must understand the significance of resistance *ratios* rather than absolute values to attain optimum tolerances in his circuits. He must broaden his spectrum of engineering interest.

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CIRCUIT ENGINEERING

The circuit engineer in turn must become familiar with the characteristics and limitations of semiconductor device processing so that his circuit designs will be feasible to manufacture at good cost/performance ratios. He must become familiar with N- and P-type semiconductors and understand the significance of N+ and P+ layers for high conductivity tunnels and interconnections. He must be concerned with the resistance and capacitance behavior of doped silicon and gallium arsenide semiconductors and with the crucial effect of large area circuitry on device yield. He must learn to overcome the presence of parasitics inherent in the monolithic circuit approach and to avoid the use of inductance as a circuit element because it defies microminiaturization. He must also broaden his knowledge of the basic physical sciences in a fashion similar to the device engineer's reaching for competence in circuit design. The circuit engineer must think about possible system modification to take advantage of the improved packing density. Because of the high cost of making changes in integrated circuitry, the circuit engineer must use simulation and employ computer techniques to optimize his designs before production.

SYSTEMS ENGINEERING

We can divide the integrated circuit era into several phases, or periods of development of increasingly complex devices. Phase I, in which we are presently involved, deals with the development of single and multiple gates (up to four) on a silicon chip; small functional chips such as flip-flops and amplifiers; and integration of two or three functions of a receiver or similar electronic equipment on a single chip. Since its beginning in 1960, this phase has grown to a $250-million industry involving computers, space and defense microelectronics, radio and television, aviation, industrial electronics, and many other applications.

The systems engineer is less affected by Phase I, than the device or circuit engineer. He designs his computer logic organization, or radio receiver, or servo amplifier using integrated circuitry in much the same way as he did for transistors and discrete components, although he does take advantage of its improved packing density, high reliability, and lower cost. For example, to the computer systems engineer, Phase I means smaller higher-speed plug-in devices performing the same function as his previous discrete circuit design, but with the above mentioned improvements.

Phase II, Large Scale Integration (LSI), involving hundreds of circuits on a single silicon chip, is now in the early developmental stages, but this phase may well have as revolutionary an impact on the technology and fabrication of electronic equipment and on the spec-

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trum of the engineer's specialization as did Phase I. This technology involves not only devices and circuits that come under the purview of the device engineer, but subsystems as well. The systems engineer, who up to this time was content to draw black boxes and logic diagrams with the knowledge that somehow his system would be implemented by the device and circuit engineer, is now forced by the characteristics and economics of LSI to re-examine the organization and architecture of his equipment. For example, he may regularize the logic of a computer to take advantage of LSI characteristics. To judge the extent of the necessary system reorganization, the systems engineer must now become aware of the province of the device engineer as well as the circuit engineer. Furthermore, because of the new dimensions of performance, low cost, and packing density, he can now think of greater system complexity being feasible —tending toward *supersystems.*

Fig. 2a illustrates the growth of the required skills and professional interests of engineers for discrete circuit technology and Phase I, integrated circuits.

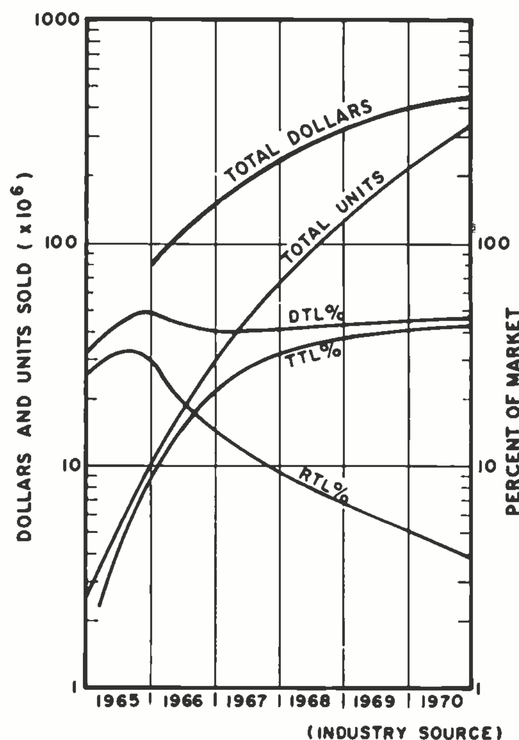

Fig. 1—Industrial growth of monolithic integrated circuits (abstracted from a recent industry survey).

HARRY KIHN received the BSEE from the Cooper Union Institute of Technology in 1934 and the MS from the University of Pennsylvania in 1952. Mr. Kihn joined RCA in 1939 as a research engineer associated with television receiver, and circuitry development. During World War II, as a member of the technical staff of RCA Laboratories at Princeton, he performed research relating to radar for automatic bombing and altimeters. With the advent of color television development in the postwar period, he played a prominent part in the development of receiver circuitry. Subsequently he was engaged in further radar research and directed research in pulse code and digital communication and computer systems. Since early 1960, he has been a staff Engineer on the RCA Research and Engineering Staff, in charge of coordinating RCA technical activities in data processing, semiconductor devices, and other fields, including both defense and commercial applications. Mr. Kihn is a member of Materials Advisory Panel on Electronics, National Academy of Science, Sigma Xi, and is a Fellow of the IEEE. He has issued over 20 patents and has authored several articles on radar theory, amplifiers, digital decoders, data communications, and integrated electronics.

Phases I and II are compared in Fig. 2b. These spectra of skills are qualitative and vary with the specific fields of electronics involved—particularly the cross-overs between the various disciplines—but, in general, represent the expanding knowledge required of the engineering professionals in this developing world of integrated circuitry. This trend is apparent by the great emphasis on the solid-state sciences and on the computer applications of design, both in the colleges and in retraining courses in industry.

A COUNTER-TREND

There is an interesting counter-trend to this expansion of knowledge in the engineering community. A circuit engineer of the past would design a flip-flop by calculating transistor parameters, resistances, capacitances, and voltages; then he would acquire the components and finally build and test the circuit. With integrated circuits, a large selection of *functional units* (e.g., shift registers, amplifiers, counters, waveform generators) having the desired characteristics can now be purchased. The average engineer may find that these "packaged functions" will reduce the need for many design skills in much the same manner as the availability of *packaged components* eliminated the need to design them several decades ago. Because of the availability of these electronic functions, the circuit engineer can now be more concerned about *systems.* He can quickly synthesize and test a subsystem with the assurance that large quantities of these devices will be available from several vendors, thus insuring that the production cycle will be feasible and successful.

IMPACT ON INDUSTRY

In our discussion of the effect of integrated circuitry on the engineer, we have touched on the products of his designs and the environment in which these are carried on—engineering. It is interesting to note the impact of the integrated circuit era on the electronics industry before discussing the technical aspects of the subject. The size of the integrated circuit market, the directives of the Defense Department to emphasize IC's in equipments, the proliferation of manufacturers and products involving IC's, the place IC's occupy in the industry press, the professional societies' symposia—all these attest to its growing importance.

Since the integrated circuit and the emerging LSI technology combine device, circuit, and subsystem functions, there is a good deal of soul searching in the electronics industry as to when the systems-oriented companies should broaden their product lines to include semiconductor device development and fabrication to maintain a high percentage of contributed value to their product. On the other hand, the semiconductor device organizations having developed "subsystems on a chip" are questioning themselves as to why they should not combine these devices into a system and go into the electronic equipment business. Both of these trends are presently being implemented to some degree, but the necessity for decision will become increasingly

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acute as time goes on. Here, then, is an important example of the impact on the engineering and corporate organization of the electronics and associated industries.

Within RCA, the early development of the high speed ECCSL integrated circuit that constitutes the heart of the logic structure of the Spectra 70 computers was performed jointly by EC&D, EDP and DME engineers. Interestingly, the last named group was organized by DEP, a systems-oriented division, to be located, and jointly develop IC's with, the Somerville Integrated Circuit facility. This had an impact both on the engineering organization of a major division and on the inclusion of highly skilled circuit and systems engineers within a device-oriented facility. As a result of this coordinated effort there has been a great out-pouring of IC developments, particularly in the linear circuit field where a great shortage of adequate circuits existed which were required by the systems divisions, and a great opportunity has been presented to RCA to take industry leadership in this important category.

An important lead was also taken by Consumer Products Division, which organized an affiliated facility at Somerville. As a result, RCA television receivers were the first in the industry to include the integrated-circuit devices that replaced whole functional assemblies of discrete circuits. This occurred several years before the most optimistic predictions indicated the transition would occur.

Integrated Circuits and the Computer Industry

It is interesting to note that two of the major innovations in this decade—*integrated circuits* and *computer systems*—complement each other: one to make the complex high-speed computer feasible, the other to provide the environment for low-cost, high-yield, large-volume production of complex devices.

One of the major differences between integrated circuit and discrete circuit functional assemblies is the effect of making changes both on a time and cost basis. Discrete circuits are readily altered; however, integrated circuits require costly mask and sometimes semiconductor processing changes. In the overall systems project costs, these differences may not appear significant. However, in the *development* phase of a project, particularly where time is a factor, these are extremely important. To minimize changes, the digital computer has been brought into active use, both in the original modeling of the circuit and subsystem and in the rapid evaluation of parametric factors. The computer has thus become an indispensable tool to integrated circuits for several reasons:

1) To optimize the circuit and systems concepts described earlier in the paper;
2) To increase the yield of circuits that meet the specifications by device probing; and
3) To anticipate topological conflicts in the interconnection masks.

The engineering operation is therefore forced to become familiar with, and use, computer-controlled processes in addition to using the computer for circuit design.

Although it may not always be evident in this early developmental phase of functional assemblies, more complex systems can be designed and built by a relatively small engineering organization and with a shorter turn-around time from proposal to fabrication. Thus, complex electronic equipment costs will become less as increasing use is made of integrated circuit assemblies; or for the same cost, more complex modular systems will materialize. This is becoming increasingly true in the computer industry where specifications of the next generation computers have a projected performance/cost improvement of severalfold, much of which is due to the use of circuit integration. The use of prepackaged, type-tested integrated circuit assemblies will help reduce the design-manufacturing time cycle of electronic systems and will therefore have a material effect on the profitable operation of a company.

The LIMAC computer, now under development at the RCA Laboratories. was fabricated using LSI techniques. The range of circuit performances from the RCA-501 transistorized computer to LIMAC are shown in Fig. 3. It is apparent that for speeds predicted for the 1970's, only LSI will meet the specifications. The considerable decrease in physical size of circuit assemblies, despite the increased numbers of circuits per package, is shown in Fig. 4 where the early BIZMAC plug-in is shown with an RCA-301, and a Spectra 70/45; the LSI module incorporating a high-speed scratch-pad computer memory is shown in Fig. 5.

Impact on the Semiconductor Industry

An important effect of the rapid growth of integrated circuit technology is on the semiconductor manufacturing industry itself. The successful development of high performance IC's is obsoleting many lines of small-signal transistors, particularly the germanium units although silicon units are affected as well. This obsolescence requires costly reorientation of design and production facilities to meet the competition, since there is little that can be done to stop the trend.

TECHNICAL ASPECTS OF IC'S

There are a number of competing technologies vying for the integrated-circuit market with varying degrees of success, but the monolithic silicon approach is far in the lead at present. Fig. 6 lists leading types of integrated circuits and arrays and some of their important characteristics. The bipolar silicon devices have by far the major share of the market, both in digital and analog circuit configurations.

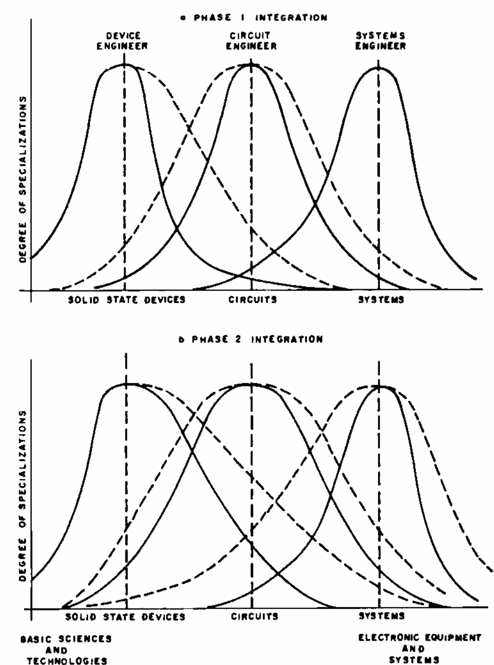
Field-Effect Devices

The field-effect family—which includes MOS, MNS, and SOS—both P- and N-channel types as well as combinations of P and N in complementary pairs are becoming increasingly important, particularly in large arrays for lower power applications such as scratch-pad memories for computers. The complementary pair is particularly useful for this application requiring extremely low power.

Flip-Chip Hybrids

Flip-chip hybrids utilize ceramic or other insulating substrates upon which passive components and conductive interconnections have been deposited. Active devices in the form of discrete transistors or

Fig. 2—The effects that Phase I and Phase II of integrated circuitry are having on the specializations of the engineering professions.



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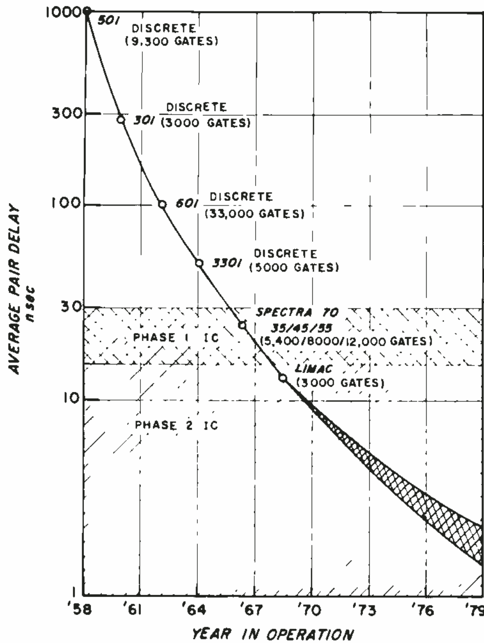


Fig. 3—Average circuit pair-delays for RCA computers.

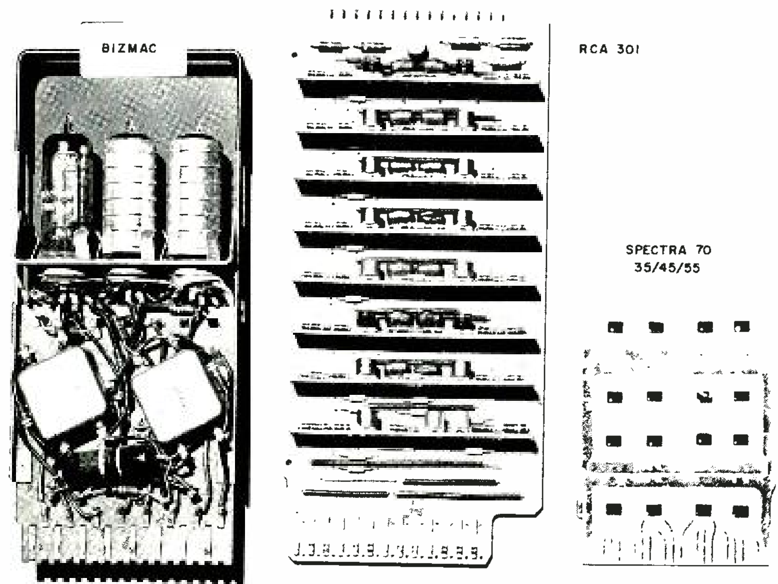


Fig. 4—Plug-in cards for the Bizmac, 301, and 70/45 computers. The 70/45 plug-in contains 16 IC's or approximately 32 logic gates.

simple integrated circuits are soldered to "lands" on the substrate to complete the circuit. This hybrid approach is an old technique that had been obsoleted by the monolithic silicon integrated circuit, but is now returning to act as a support and interconnection matrix for these very silicon monolithic circuits to form an array. The main virtue of the flip-chip-hybrid approach is that *existing* active devices can be interconnected to produce arrays without expensive design and fabrication cycles. Whether this hybrid approach will be as economical as monolithic bipolar or MOS arrays has by no means been established, but it does have advantages in small quantity production and higher power circuitry.

Custom Monolithic Circuits

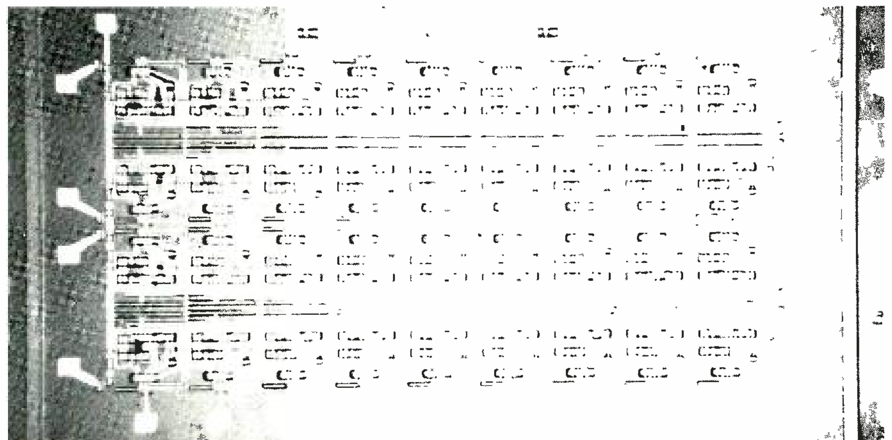
For specialized or "custom" monolithic circuits, a new technology may be imposed on systems-oriented engineering organizations. For economy, the *universal wafer*, which is a silicon wafer with hundreds of identical integrated circuits and two layers of metalization, will come into prominence. The "underlayer" will provide *intra-circuit* connections, and the upper layer will be solid aluminum thick film connected to appropriate points on each circuit. The *inter-circuit* connections can be etched by the customer as dictated by his circuit design. If this practice should prove economical, there will be a major change indeed in the mode of operation of circuit and equipment engineering. Fig. 7 shows projected costs of discrete circuits, simple (Phase I) integrated circuits, and LSI (Phase II) circuits. The locus of the minimized cost/gate is seen to de-gration.

Multilayer Printed Circuits

Although printed-circuit boards have crease markedly with Large Scale Inte- been extensively used with discrete circuits, these circuit boards in turn have been largely interconnected with *discrete wiring* although the latter may have been automated by wiring machines. The microminiaturization resulting from integrated circuits has encouraged the use of printed-circuit *multilayer platters* that provide complex interconnections at controlled impedance transmission characteristics, supplying of multilevel voltages, and filtering and bypassing of high-frequency currents.

The use of platters results in very compact and duplicable equipment. Due to

Fig. 5—A complementary MOS memory array of four words with nine bits each. This chip, 75 mils x 135 mils in active area (about the size of a match head) contains 432 transistors.



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the early state of the technology of platter fabrication, problems have arisen in interconnection between layers, but these problems are gradually being eliminated as evidenced by the successful use of interconnection platters in the Spectra computers. The application of the computer-controlled coordinatograph provides rapid generation of photomasters for these platters, thus allowing changes in the interconnection pattern to optimize performance.

Integrated interconnection platters are lifting the present limitation to higher speed computers, that is, the time of travel of signals along conventional long-wire paths due to the finite velocity of electromagnetic waves (1 foot of wire produces 1 nanosecond delay or more depending on the dielectric constant of the insulation). This continual effort to realize higher-speed computers is a major factor in dictating the use of arrays for the high-speed (2 nanosecond delay) logic functions contemplated in the next generation of computers.

All these factors demonstrate the feasibility of developing more sophisticated and higher performance systems with a shorter design cycle and at lower cost than could have been accomplished with discrete circuitry. Furthermore, as more complex systems are developed for use in physically smaller spaces, the difficulty of servicing and maintaining the equipment brings into play the concept of "throw-away" packages and the automatic self-diagnosis of system problems, both largely new in engineering design.

Fig. 6—Categories of integrated circuits and arrays.

Category		*Circuit*	*Typical Uses*	*Speed or Stage Delay*	*Characteristics*
Bipolar	Digital	Diode Transistor Logic (DTL)	Logic Circuits	Medium to high (20 ns)	High voltage swing, low cost, maximum availability
	Digital	Current Mode Logic (CML or ECCSL)	Logic Circuits	Super high (2 ns)	Highest speed circuit, balanced to external currents, low voltage swing, medium cost
	Digital	Transistor-Transistor Logic (T^2L)	Logic Circuits	High (10 ns)	High speed, medium voltage swing, low cost
	Digital	Large Scale Integrated Arrays (LSI)	Computer Subsystems Fast Memories	Medium to super high	High speed, ultimately low cost, complex computer subsystem capability, presently low yield
	Analog	Amplifiers, Oscillators, Discriminators, Detectors, Filters, etc.	Communications Consumers Space & Defense Computers	D.C. to U.H.F.	Wide selection of functions that are penetrating a wide range of markets
Field Effect Transistor Integration		Metal Oxide Silicon Arrays (MOS) P Channel N Channel Complementary Silicon on Sapphire (SOS) Metal Nitride Silicon Arrays (MNS)	Logic and Memories	Slow to medium Medium Medium to high High Same as MOS	Fabrication simpler than bipolar and are capable of higher packing density Inherently lower stand-by power and operable under wide tolerances
Hybrid Integrated Circuits		Flip Chip on Ceramic Substrate	Digital and Analog	Medium to super high D.C. to U.H.F.	This is an alternative method of interconnecting active and passive components to form a complex array

CONCLUSIONS

Integrated circuit technology will require the careful attention of engineers in the planning of future equipment. This technology has important economic implications that may seem to be out of the province of this discussion, but it really is only a matter of semantics, because, in a sense "engineering is economics applied to science". Much of the impact on electronics engineering has already been made by the transistor and solid state device revolution, whose results are apparent to us in present engineering. Integrated circuitry and particularly functional arrays are logical next steps in this process. The tremendous penetration that electronics has made into many fields—industry, defense, space, aviation, consumer, finance, medicine, and several others—will be accelerated by microelectronics and circuit integration. These technologies can bring into reality the full potential of high reliability, low cost, personal communication, information processing, and consumer products, as well as automatic control of many of the appliances presently used in the home. They can insure the emergence of supersystems that would otherwise be impractical as regards physical size, power requirements, reliability, and cost.

One need only compare the past three generations of computers to realize that technological innovations are increasing the system performance of equivalent computers at the rate of an order of magnitude every eight years. To sense the pace of development, one must realize that arrays of integrated circuits whether on monolithic silicon wafers or flip chips on ceramic substrates, whether MOS or bipolar in configuration, coupled with computer-aided design and system optimization, will radically alter both the techniques of electronics engineering and the skills required for its implementation. If properly implemented, these changes will assure the growth of our industry and opportunities for our engineers.

ACKNOWLEDGEMENT

Information for Figs. 3, 4, 5, and 7 was supplied by H. Miller and M. Lewin of RCA Laboratories and P. Gardner of EC&D.

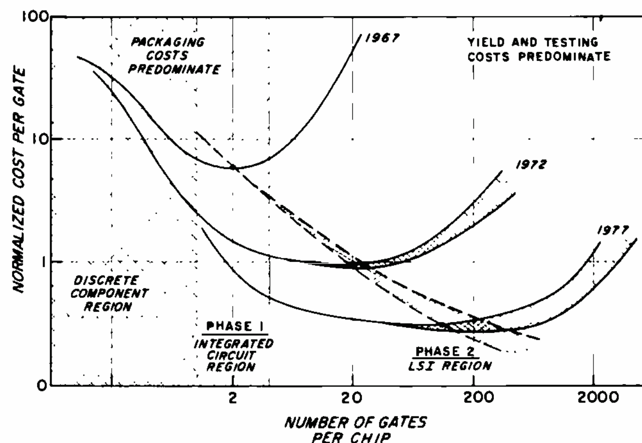

Fig. 7—Projected costs for Phase I and Phase II integrated digital circuits.

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INTRODUCTION TO LARGE-SCALE INTEGRATION

The development of thin-film and semiconductor techniques for the fabrication and interconnection of microminiature components and circuits has stimulated investigations into the problems of fabricating and packaging much larger electronic complexes. This article is concerned with the design concepts, processing techniques, fabrication problems, and potential of large-scale integrated circuits. The problems of yield, crossover requirements, power dissipation, and testing complexity are considered; LSI fabrication problems are compared and contrasted with the problems of single-circuit fabrication. Finally, some of the techniques currently being used in large-scale integration (LSI) are described and their advantages and disadvantages considered.

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LARGE-SCALE INTEGRATION is concerned with the fabrication of multistage electronic functions in a single package. In digital equipment, this approach can be applied to the fabrication of registers, sections of memory, counters, etc. The use of LSI in linear small-signal equipment is the first step toward such accomplishments as the enclosure of the circuitry for a complete radio receiver or transmitter in a single package. Just as normal integrated circuit production involves more than merely putting many individual components in a single package, LSI involves more than multiple-circuit packaging. The elements of an LSI array lose their identity as individual circuit stages. The only external interconnections used are those required to attain the desired electronic function. Performance is measured in terms of the total function rather than in terms of sub-circuit performance.

Fig. 1 illustrates how an electronic system is built up through the application of technologies involving basic properties of materials, component design and fabrication, component interconnection, circuit design and interconnection, and finally subsystem design and interconnection. The integrated circuit manufacturer was involved, before the advent of LSI, in only the first three areas of Fig. 1. However, LSI now requires an extension of manufacturing activity into the subsystem level. This extension requires not only more sophistication and refinement in fabrication technology but major improvements in testing and evaluation procedures.

LSI ARRAY ADVANTAGES

Performance

Including many circuit stages in one small package can reduce the size and improve the performance of electronic equipment. Improved performance is realized mainly through the shorter lead lengths inherent in small packages: lead inductance and capacitance that ordinarily limit the speed of digital integrated circuits is minimized. The close spacing also helps to keep all circuit elements at the same temperature, facilitating stable operation. In addition, the enclosure of many stages in a single package makes possible operation of all circuit stages under identical power supply conditions. Operation of all circuit stages under the same electrical and environmental conditions improves the noise immunity of the system.

Cost

Although fabricating an array of circuit stages is a great deal more complex than fabricating a single stage, a high-cost processing system is not required. It is more economical to produce a digital system in array form than as a combination of single stages, even if the cost of an array is high, as long as the cost per gate is the same or less than it was for individual stages. Fig. 2 illustrates how the relative cost per gate varies with increasing circuit complexity. The values in the Figure are based on the cost of a semiconductor or thin-film integrated circuit assembled in a multilead package. The package and assembly costs are major elements in the total cost of an integrated circuit. Because these costs are fundamentally independent of circuit complexity, it is reasonable to expect a decrease in the cost per gate as circuit complexity is increased. However, as chip contents become more complex, it is also reasonable to expect that yield will decrease. In fact, yield losses do become more severe and more than compensate for the package and assembly savings; the result is increased cost per gate. The broken curve in Fig. 2 indicates the effects of improved device technology on large-scale array feasibility. The yield for a single-circuit stage in an array is higher than for the same single circuit individually packaged because the individually packaged stage must exhibit satisfactory performance in a wide variety of applications under worst-case conditions while the array stage has only to satisfy one specific set of better defined power supply and input-output conditions. The yield and testing problems involved in making a ten-gate array are much less severe than those involved in testing and packaging ten individual gates in a single package.

The costs described above are the incremental costs incurred in making devices after design engineering is complete: the engineering costs for complex circuits are much greater than for simple functions. The greater initial costs may be justified by the monetary savings realized in final system-interconnection and yield and by the time savings real-

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I. H. KALISH received the BSEE degree from the Cooper Union School of Engineering in 1953 and the MS degree in Electrical Engineering from Columbia University in 1956. He has completed additional graduate work at the Polytechnic Institute of Brooklyn. He joined RCA in 1953 as a semiconductor-device engineer. He is presently a Manager in the Electronic Components and Devices, Integrated Circuits Division and has been responsible for the design of devices and processes used for the fabrication of semiconductor integrated circuits. Mr. Kalish is currently manager of the Small-Signal-Device Model Shop and is responsible for providing support to semiconductor programs involving both discrete and integrated semiconductor devices. Mr. Kalish is the author of several papers on semiconductor devices and a book, Microminiature Electronics. Since 1954 Mr. Kalish has taught Physics and Electrical Engineering at the Cooper Union School of Engineering and Science and is currently an Adjunct Professor of Electrical Engineering there.

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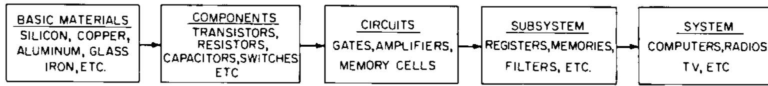

Fig. 1—Diagram of electronic system development.

ized because of the existence of fewer testing problems.

PROBLEMS IN LARGE SCALE INTEGRATION

The relationship between large arrays and single-stage circuits is very similar to that between integrated circuits and discrete components. It did not make technical or economic sense to integrate a circuit function by replacing the elements of its discrete version on a component-by-component basis. Instead, the circuit function as a whole was reviewed and a circuit design chosen so that the desired function was achieved while exploiting the advantages and minimizing the disadvantages of the technology available. Similarly, the design of arrays requires much more engineering attention than merely devising means for reproducing the combinations of integrated circuits found on computer circuit boards on a single chip. The circuits on computer circuit boards were designed to minimize the number of gates required rather than to minimize the number of different board configurations needed. In addition, each computer circuit board may have from 20 to 100 terminals. The most effective array designs are those which combine a number of computer circuit-board functions yet minimize the external circuit connections required through the use of complex circuitry within the component package.

Fig. 3 illustrates some of the areas in which engineering decisions are required before a commitment can be made to a particular array function or type. The electronic configuration of the entire system must be reviewed to determine how many arrays of the same type can be used. If the answer is only a few per system, the high engineering cost associated with that array may be prohibitive. If standard packages can and are to be used, the electronic functions of the system must be partitioned in terms of fourteen-, twenty-eight-, or forty-lead package types. The power dissipation capabilities of each package must also be reviewed in terms of maximum thermal dissipation.

The particular choice of array must take into account the capabilities and limitations of existing fabrication methods. If the performance requirements are such that monolithic silicon or thin-film methods cannot produce acceptable yields, a hybrid approach may be required. The preparation of test specifications and procedures for use with integrated arrays is a difficult task. The increased number and functional interdependence of the leads on an array package compared to a single-circuit package results in an exponential increase in the number of test conditions that are required to guarantee circuit performance over a wide range of input conditions. Circuit-board test procedures are only partially applicable to arrays because of the lack of directly accessible internal check points on the array. It is probable that a small specially-programmed computer will eventually be used for testing complex multi-lead circuits.

FABRICATION PROBLEMS

Yield

The major problem in fabricating an array comprising many circuit stages is achieving a processing yield high enough to keep the cost of fabrication reasonable. Because the function of an individual stage in an array is very specialized, and its input and output requirements uniquely defined, the stage can be designed to operate satisfactorily despite relatively large variations in the values of the components in that stage. Thus the yield per array stage is higher than the yield for a single-circuit stage which must meet specifications for a variety of possible applications. The circuits in an array will be acceptable unless they contain some catastrophic type of defect such as an open or a short circuit. If it is assumed that the major yield loss is due to the random occurrence of catastrophic defects in an array, the expected fabrication yield of an array having a given number of circuit stages, n, will be the yield for a single stage raised to the nth power. For example, if a single-stage circuit can be made with a yield of seventy percent then the yield that could be anticipated for an array containing ten such stages would be 0.7^{10} or approximately three percent. Fig. 4 illustrates the relationship between array yield and circuit complexity as a function of the yield per stage. If it is assumed that it is not economically or theoretically feasible to produce arrays at yields of less than one percent, it becomes clear that a very high yield per stage is necessary to make the fabrication of even moderately complex arrays worthwhile. The relationships shown in Fig. 4 indicate that a yield per stage of ninety-five percent would be necessary to make feasible fabrication of a ninety-stage array, while a stage yield lower than eighty percent would make the fabrication of arrays with greater than twenty stages impractical.

The discussion above refers to the problems involved in fabricating the many stages of an array simultaneously as in the case of thin-film or monolithic-silicon processing. Other approaches that do not require simultaneous fabrication of elements will be discussed later.

Fig. 2—Variation of cost per gate with increasing circuit complexity.

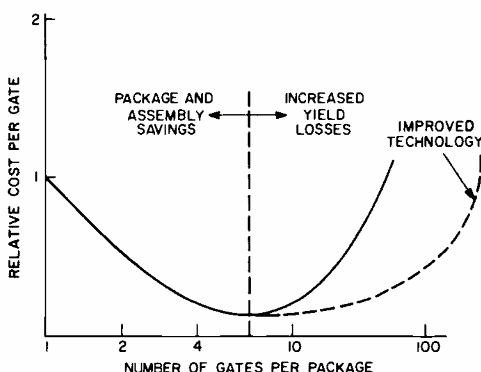

Fig. 3—Engineering decisions required before LSI array production.

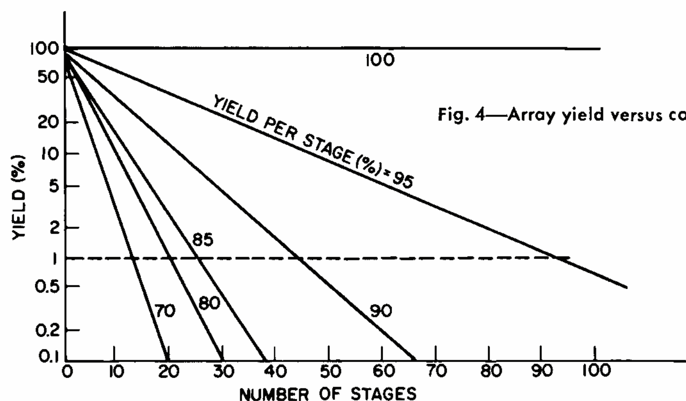

Fig. 4—Array yield versus complexity.

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Causes of Defects

Catastrophic defects can occur in many areas of monolithic-silicon processing and in the substrate material used. If there are bumps and polycrystalline structures on the surface of the starting material, oxides grown on it will contain defects ("pinhole" defects) and will not serve as effective diffusion masks. Photographic-mask defects in the form of scratches or surface dirt may cause the oxide to be opened at undesirable points and may cause the obstruction of some desired windows. Because from six to ten masking operations may be required for array fabrication, the quality of the masks is crucial. Another major source of catastrophic damage to monolithic-silicon circuits results from defects in the metal interconnection pattern. These defects can be caused by mask defects, improper mechanical handling, or the presence of conductive foreign particles on the circuit surface. For these reasons monolithic-silicon array fabrication requires a much higher level of processing technology than is necessary for the economical fabrication of single stages.

Crossovers

Occasionally, in two-dimensional circuit fabrication, it becomes necessary for two conductors to pass over the same point in the circuit plane. This point is called a crossover point; its occurrence is a significant problem in the fabrication of monolithic-silicon circuits. Fig. 5 illustrates two methods commonly used to permit crossovers. The best method requires that the circuit be arranged so that the crossing of current carrying paths occurs over a resistor. This permits the resistors to be used as one conductor and the metallization pattern, separated from the resistor by an insulating oxide, as the other. Fig. 5 shows the interconnection of the emitters of two transistors through the use of a resistor lying between them. Where the resistor crossover technique is not practical, "tunnels" may be required. For example, in Fig. 5 assume that a current path between A and B that does not intersect conductor C is desired. The isolation mask is designed to leave an N region between A and B. During the transistor emitter diffusion, an N+ region is diffused between A and B. This diffusion reduces the sheet resistance in this area to approximately three ohms per square and creates a conductive "tunnel" that can be used to connect A and B. The resistance of a tunnel is typically only a few ohms; it can be used in those parts of the circuit where the additional resistance and capacitance will not significantly affect circuit performance.

Because the flexibility of layout required to make the best use of the resistor-crossover method is difficult to achieve without wasting area and because the large scale use of tunnels is practical only in low-current low-speed applications, a third method of crossover construction—multilayer metallization—is usually required. This method is illustrated in Fig. 6. One set of interconnections, usually those required within the cells, are formed conventionally. A second layer of insulation: sputtered glass, an oxide formed at low temperature, or some organic insulator is then deposited. The second metallization interconnecting the cells can then be fabricated atop the second insulating layer. Because of the high wiring density of array patterns, extreme care is taken to reduce pinhole defects in the insulation so that a reasonable yield can be obtained.

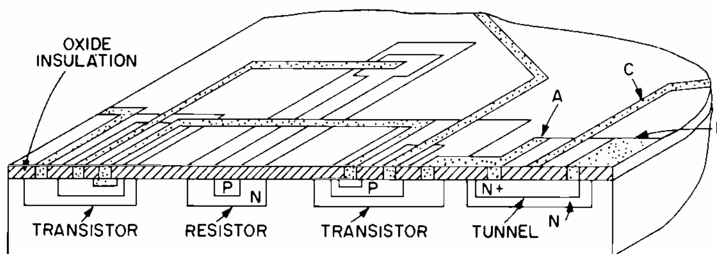

Fig. 5—Resistor and tunnel-type crossovers in monolithic circuits.

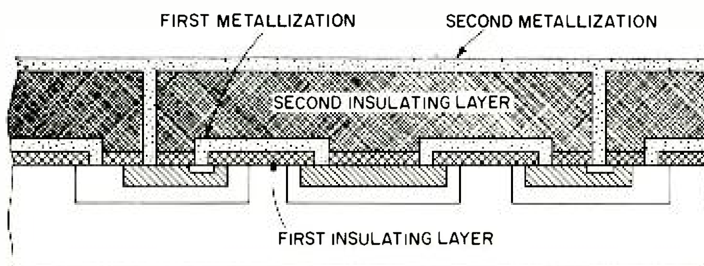

Fig. 6—Multilayer metallization.

APPROACHES TO LSI

Hundred Percent Yield

The most direct, but at the same time the most difficult, approach to the fabrication of a complex electronic function involves the refinement of the available technology to the extent that perfect results can be achieved over a large enough portion of a silicon wafer to permit the desired function to be produced with an acceptable yield. This approach yields the greatest packing density with a minimum of processing and testing operations. Small memory-cell arrays and complex arithmetic elements for computers have been successfully fabricated through the use of bipolar technology and the one-hundred-percent-yield approach. Continuing improvements in bipolar technology will result in an evolutionary increase in the complexity of bipolar-type arrays.

The one-hundred-percent-yield approach may be implemented by choosing a very simple high-yield method which does not demand superior performance from devices made under that method. The application of arrays of P-channel MOS devices to low-speed digital applications represents such an approach. The relatively simple processing required to fabricate MOS devices is illustrated in Fig. 7. After initial oxidation, windows are opened for the source and drain diffusion. A second oxide is then grown and windows opened for the contact metallization. Metallized contacts are made to the source and drain regions, while, simultaneously, a layer of metal is evaporated over the oxide in the region between the source and drain; this metal acts as the gate electrode. Fabrication by this method requires only one diffusion and three photographic masking operations. Only the masking operation that defines the contact openings must be performed to a very high degree of perfection; pinholes generated by this operation can cause catastrophic failures in the form of gate-to-substrate shorts. Masking defects that occur in the source and drain diffusion operation or during metallization are not as serious and will not cause catastrophic device failure unless the defect is so severe that it causes a short between source and drain or an open- or short-circuit in the metallization path. Thus, the MOS fabrication technique requires only a minimum number of critical processing operations, making it an attractive solution to the problem of obtaining one hundred percent yield. In addition, the high impedance

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Fig. 8—Discretionary-wiring array-fabrication procedures.

of MOS circuit structures permits the use of crossover tunnels without affecting circuit performance. Therefore, crossover problems are easier to solve with the MOS approach. MOS arrays having hundreds of stages have been successfully fabricated.

Discretionary Wiring

Between twenty and seventy percent of the circuits on a typical monolithic integrated-circuit wafer function properly. The precise yield is dependent on circuit complexity and severity of performance specifications. Nevertheless, on a wafer containing 500 circuit patterns it is not unreasonable to expect to find 100 operable circuits. Under the discretionary wiring approach to LSI, attempts would be made (by provision of a suitable interconnect mask) to form the desired complex electronic array by interconnecting only the good stages on the wafer. An array so formed could, in this case, contain up to 100 stages.

Fig. 8 illustrates the procedures used in the discretionary wiring approach. A wafer containing several hundred circuit cells is processed through metallization in conventional fashion. Each cell is provided with test points so that it can be functionally tested through the use of a multipoint circuit probe and a computer-controlled test set. The location of all good circuit cells is fed into a computer. This location information is combined in the computer with system requirements regarding external pin configurations. The combined data is then used to determine the interconnection pattern required to form the final desired array. Provision is made for the generation of this final pattern by the computer. With suitable facilities and a sufficient engineering development effort, the time required to fabricate a specialized interconnection pattern for each wafer can be reduced to several hours. The cells of the array can then be interconnected, packaged, and prepared for final electrical evaluation.

The mechanics of this system are easy to describe but difficult to implement. The number of ways in which 100 good circuits may be selected out of 500 on a wafer is immense—approximately 10^{100}. Even a high-speed computer system could evaluate but a negligible fraction of these possibilities in a reasonable time; hence, all of the possible combinations of 100 good cells will not normally be known. The cells are, in addition, still vulnerable to normal yield losses during the packaging operations. Therefore, the major disadvantage of this approach is the enormously high engineering and equipment cost per array. Nevertheless, if the system requires a 100-cell array (using conventional bipolar technology), the probability that an array of this complexity can be fabricated successfully on a single silicon wafer is highest with the discretionary-wiring approach.

Hybrid Approach

The hybrid or multichip approach to array fabrication makes use of a combination of semiconductor and film techniques to generate complex electronic functions in a minimum volume. Briefly, this approach uses monolithic silicon technology in the fabrication of the circuit cells of an array, but makes use of either thick- or thin-film techniques to interconnect the cells on an insulating substrate.

Fig. 9 illustrates the basic operations in the hybrid approach. The semiconductor circuits are prepared, tested, and separated in the usual manner. An insulating substrate is prepared by using either thick- or thin-film wiring for interconnections to the cell sites. The circuit chips may be mounted on the substrate surface with the circuit itself facing up or down. If the circuit is mounted face up, conventional bonding may be used to connect the circuit pads to the substrate wiring; if the circuit is mounted face down, the "beam lead" or some other "flip-chip" approach is used for interconnection of circuit pads with substrate wiring. If a few large resistors or capacitors are needed to implement the array function they can be fabricated as part of the substrate. After assembly the arrays are tested and the causes of any malfunctions localized. The major advantage of the hybrid approach is that after faults are localized they can usually be repaired by replacing the appropriate circuit cell. This means that even if the yield is not one hundred percent at the completion of initial processing, an operable array can still be obtained with a certain amount of rework. The hybrid approach is particularly applicable to situations in which only a few of many different kinds of arrays are needed; the approach is flexible enough to permit variety without major expenditures for new or additional engineering or equipment.

To some extent, the hybrid approach may be viewed as the use of a miniature printed circuit board; it permits miniaturization of practical equipment to an extent not yet feasible with other approaches to LSI. The major defects of the hybrid method are that it does not permit the degree of miniaturization offered by the other approaches and that its potential for low cost is poor. Although present hybrid-method costs look favorable when compared to other LSI approaches because of the higher yields obtainable, the hybrid approach offers little advantage over conventional integrated circuit use except miniaturization. In addition, the reliability potential of the hybrid system is poorer than that of other LSI approaches because the circuit connections are made individually rather than as part of a single controllable processing operation.

Fig. 7—Fabrication of P-channel MOS devices.

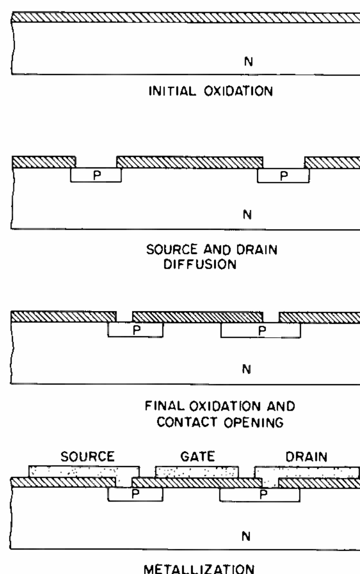
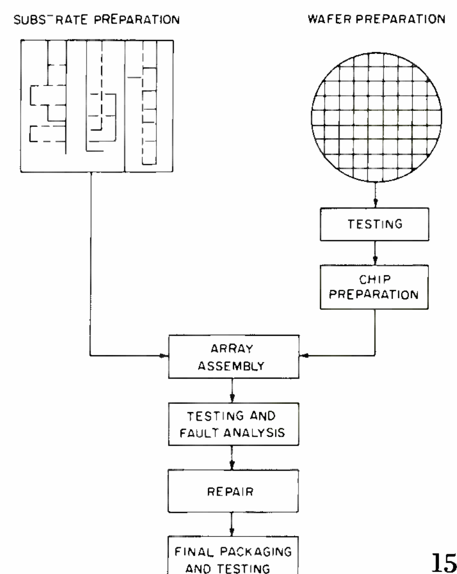


Fig. 9—Hybrid-array fabrication procedures.



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CURRENT-MODE-LOGIC ARRAYS

The next generation of large high-speed computers will most likely use non-saturating emitter-coupled logic circuits because of their superior speed and system performance. Also, these large systems will require some use of integrated circuit arrays, because, in an array environment, the switching rate of high-speed circuitry is not masked by interconnect-wire capacity and transmission-line propagation delay. In addition, higher packaging density can be achieved, thereby reducing the number and size of printed circuit boards required in the system. This paper describes current work on the solution of problems associated with the achievement of high-volume production of monolithic integrated-circuit current-mode-logic arrays.

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PHYSICALLY reducing the size of a system improves its performance; reducing printed-circuit-board size and number helps reduce cost. If, by the introduction of arrays, the system speed is predominantly limited by gate speed, a higher performance system can be realized simply by replacing the old arrays with new ones which have higher performance due to improved device fabrication techniques. As the state of the art advances, diagnostic circuitry could be added to the array chip greatly enhancing machine maintainability. Fortunately, it can be shown that many of the above mentioned advantages can be accomplished with a rather modest level of array technology (10 to 30 gates). In addition, since current-mode-logic (CML) circuits are non-saturating, process and parameter control (storage time, saturation voltage, breakdown voltages) are much easier.

Final manuscript received August 8, 1967.

FABRICATION

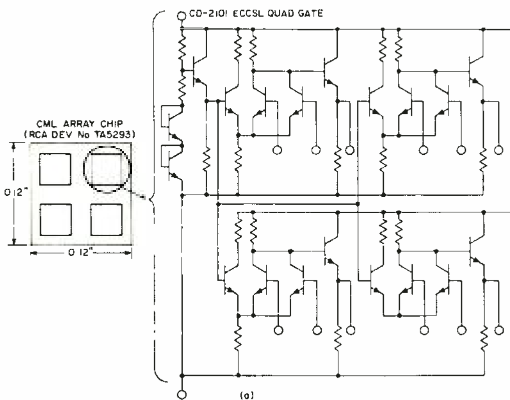
There are many array approaches which can be adapted by an integrated circuit manufacturer. The three most commonly described are:

1) *The functional array*—an array designed for a particular application thereby making optimum use of available chip area;
2) *The master-chip array*—a wafer composed of "cells" (a simple circuit or group of undesignated components) which can be interconnected by different metalization patterns to create different logic functions; and
3) *The discretionary array*—a master-chip array in which the cells on the wafer have been pretested. For any one junction, different metalization patterns are used to connect together only those cells which are known to be operational.

Each of these array fabrication schemes is being evaluated. Often the type of array function desired will dictate which approach is most feasible. However, all these approaches have the same fundamental considerations:

1) Multilevel metalization,
2) Yield versus area,
3) Testing,
4) Power dissipation, and
5) Packaging.

Fig. 1 shows the logic diagram and schematic of a CML array vehicle containing 16 CML gates and four temperature-track-



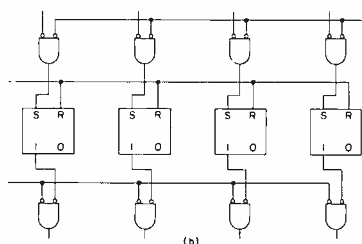


Fig. 1—A 16-gate CML array: a) array chip contents and configuration; b) logic diagram.

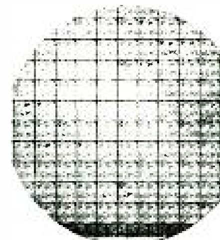


Fig. 2—Wafer containing CML array of Fig. 1.

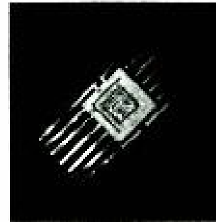


Fig. 3—Array chip mounted in a 14-lead and 28-lead flatpack.

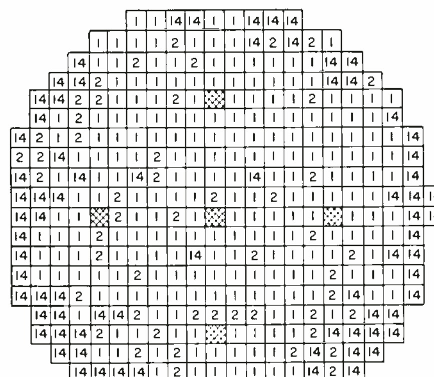


Fig. 4—Yield map for first-level circuitry.

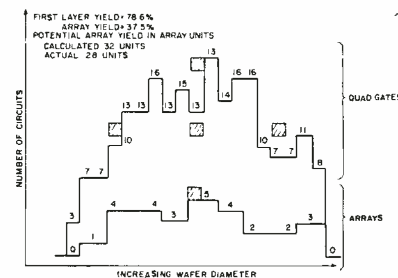


Fig. 5—First-level circuitry yield and potential array yield.

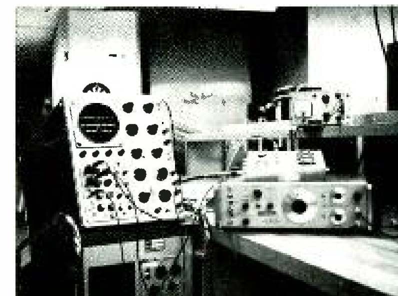


Fig. 6—Dynamic type array tester.

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ing reference-voltage circuits. The register function represented by this array is found quite frequently in the data-flow paths of high-speed computers. A second-layer metalization pattern has been created which ties together four standard RCA-CD2101 ECCSL quad two-input integrated circuits and facilitates the fabrication of this array on a chip. Each cell (each CD2101) of the array is a pellet 0.06-inch square. The four cells, combined with the second-layer metalization pattern in a master-chip fashion create a CML array 0.12-inch square. The insulation between the aluminum metalization layers is SiO_2 glass; the array dissipates approximately 520 milliwatts.

Fig. 2 shows a photograph of a wafer containing the arrays just described; Fig. 3 shows the array chip mounted in 14-lead and 28-lead flat packs. Although the component density on the array chip is not as high as can be achieved with present array technology (76 transistors, 76 resistors) the chip serves as an adequate vehicle for evaluating the following factors:

1) Multilevel metalization, including process yield, process repeatability, and reliability;
2) Dynamic performance of a circuit in a conventional wiring environment and in an array environment;
3) The effect of power dissipation on performance as a function of package configuration;
4) Testing procedures; and
5) Yield.

TESTING

Arrays are tested at three stages of development:

1) First-layer metalization wafer probe,
2) Array wafer probe, and
3) Dynamic performance of the array in a package.

Probe Testing

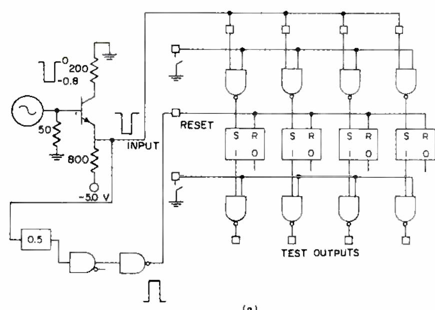
Both wafer-probe tests are performed by an automatic test set in which the main component is an RCA Spectra-70 computer. A typical yield map for the first-level circuitry is shown in Fig. 4. The squares represent circuit locations; the numbers appearing in the squares represent circuit test results. The number 1 indicates that the circuit at that location has passed all electrical tests; other numbers indicate the type of failure experienced by the cell at that location. The yield map indicates graphically the number and location of potentially good arrays on a particular wafer and permits experimentation with interconnect mask shifting to increase array yield. Fig. 5 shows a yield plot of the first-level circuitry, and a corresponding potential array-yield plot. The dips in the array-yield plot reflect the statistical problems caused by the requirement that a number of adjacent circuits be good so that a good array can be produced from a combination of them. Yield is plotted at each manufacturing step through packaging and dynamic testing so that the effectiveness of array fabrication procedures can be studied.

DYNAMIC PERFORMANCE

Arrays are tested dynamically with the simple tester shown in Fig. 6; the tester logic diagram and timing waveform are shown in Fig. 7. Dynamic testing, while not exhaustive, exercises each input of each gate in the array. Fig. 8 shows speed as a function of temperature for the same array in two different type of packages. The performance of the array in a 28-lead flatpack is superior due to its lower thermal resistance.

CONCLUSIONS

The ECCSL arrays have been successfully fabricated using two levels of metalization on 120- by 120-mil chips. The yield, fabrication, and performance studies of these arrays, while not yet complete, indicate that CML arrays of 10 to 30 gates are entirely feasible. This is especially true if the size of the chips are reduced as much as possible (preferably below 0.10 by 0.10-inch). Indications are that arrays with relatively low gate counts (10 to 30 gates) greatly reduce the testing problems usually associated with array technology.



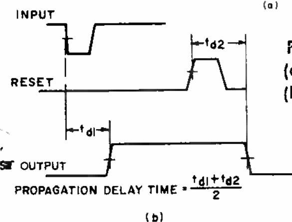


Fig. 7—Logic diagram (a) and timing waveform (b) for the array tester.

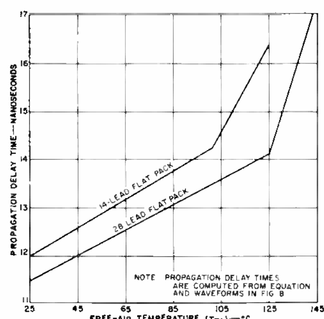


Fig. 8—Speed as a function of temperature for a typical CML array in a 14-lead and a 28-lead flatpack.

M. D'AGOSTINO received the BSEE from Villanova University in 1960 and the MSEE from Drexel Institute of Technology in 1963. At RCA, Mr. D'Agostino has worked on the Micropac memory, ferrite cores, and memory planes, and has designed the temperature control and sensing circuitry for memories. Mr. D'Agostino was also responsible for the design of the selection circuitry used on a thin-metal-sheet multiaperture-element memory. In 1963, with the Defense Microelectronics Group, Mr. D'Agostino contributed to the evaluation of integrated component characteristics and was responsible for the circuit design, analysis, and evaluation of high-speed monolithic logic circuits. In September 1966, Mr. D'Agostino was promoted to Leader in the Special Electronic Components Division of EC&D, where his present responsibilities include the design and development of bipolar and complementary MOS arrays. Mr. D'Agostino is the author of seven technical papers, has been granted two patents, and has three other patent applications filed. He is a member of the IEEE and Eta Kappa Nu.

LUCIO VOLLARO received the degree of **Dottore in Ingegneria Elettronica** in 1965 from the University of Rome, Italy. He is currently working for the PhD at Polytechnic Institute of Brooklyn. After one year at Olivetti, Milano, where he was engaged in research and development in the field of digital computers, he joined RCA where he is responsible for the design and the test of arrays.

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HIGH-YIELD PROCESSING OF LARGE-SCALE INTEGRATED ARRAYS

Presently, sophisticated fabrication techniques are being used in the integrated circuit industry to permit fabrication of low-cost complex devices. For large scale integrated arrays, additional fabrication controls must be applied to ensure consistent quality in these more complex devices. This paper reviews some new approaches to improving large-scale integrated array fabrication, including two-layer metalization, high-yield processing, close-spaced photolithography, redundant processing, and special-care processing.

DR. ANDREW G. F. DINGWALL

Array Development

Electronic Components and Devices, Somerville, N.J.

LARGE-SCALE integration (LSI) represents an exciting development in advanced bipolar integrated-circuit technology. By fabricating very large logic functions on a single silicon chip in arrays of hundreds of gates, it is possible to design compact circuits of higher reliability and superior performance. Performance improvements result mainly from switching speeds in the low nanosecond region. Faster switching is possible because of the low capacitance and very short interconnections naturally occurring within integrated arrays.

Programs now active at RCA are scheduled to produce LSI arrays of at least 100 gates by early 1968. Each array will contain a minimum of 700 transistors and a like number of resistors per chip. The LSI programs, supported by both RCA funds and Air Force Contract No. AF33(615)-3491 are based on 100-percent-yield techniques[1] in which arrays are fabricated directly through the use of fixed masks and non-discretionary wiring. Because a single defective component or a shorted interconnect can result in an inoperative array, it is clear that high-yield techniques are of the utmost importance.

When reviewing processing steps that can be taken to ensure high yield, it must be recognized that very sophisticated fabrication procedures are already employed in the integrated circuit industry; current techniques have been successful in permitting the fabrication of low-cost devices of a complexity which could scarcely have been projected a decade ago. Among these techniques are:

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1) Extensive use of laminar flow rooms (Fig. 1) to permit all operations to be carried out in ultra-low-dust ambients; and
2) Minute attention to all phases of wafer processing and handling to reduce sources of wafer contamination and damage.

Because of the care already exercised in normal manufacture, a simple "tidying up" of conventional processes and conventional circuit layouts is not considered the major avenue of approach to 100-percent-yield array fabrication. Rather, the programs aimed at improving yield have been based on approaches designed to eliminate sources of defects.

APPROACHES TO LSI FABRICATION

Two major methods of LSI fabrication are now in general use:

1) The "fixed wiring" or "100-percent-yield" method[2] in which high yield techniques are employed to ensure that 100-percent of the gates on a given chip are operative. Fixed interconnect masks are used to interconnect the components on the chips into the desired circuit configurations. Just as with present integrated circuits, true 100-percent yield is not required to make this approach economically feasible; it is only necessary that a moderate fraction of the 20 to 100 potential arrays on a wafer be perfect.
2) The "tailored-interconnect" or "discretionary-wiring" method[3] in which each gate on a wafer is first tested electrically and identified as operable or inoperable. A computer is then employed to calculate interconnect patterns and generate the necessary artwork and photomasks so that only perfect gates are incorporated in the circuit. Because of the need to allow space for probing pads (required in electrical testing) and for potential wiring paths, high levels of compactness are not as readily obtained with this method as with the fixed wiring or 100-percent yield method. Normally, only one potential array per wafer is possible with the tailored-interconnect method.

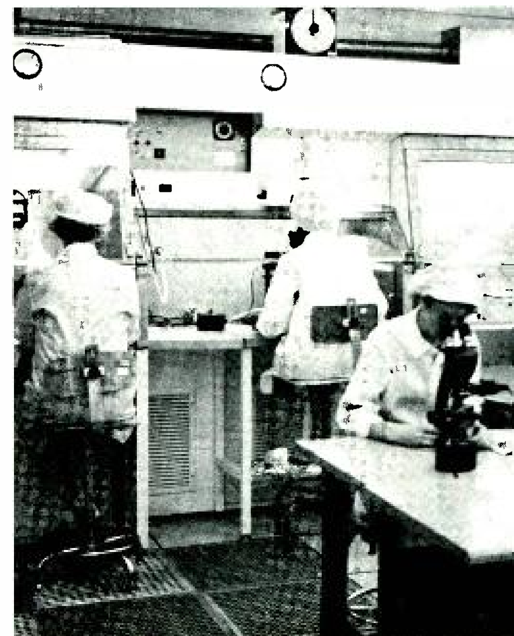
RCA has approached LSI through the 100-percent-yield method. This method was adopted because it represents the more conventional and simpler approach to LSI; and because it permits normal integrated-circuit fabrication sequences. Low-cost devices can be produced with 100-percent-yield techniques because of the routine fabrication procedure and greater number of potential circuits per wafer. A further direct benefit arises in that any techniques that improve array yield also benefit the IC industry.

Which of the two approaches to LSI fabrication will ultimately be preferred for any application will depend on array complexity, high-yield statistics and the outcome of present programs. RCA's present projections indicate that high-yield processing sequences now under development will permit the economical fabrication of arrays of 100 to 200 gates.

Two-Layer Metallization

One feature of all LSI approaches that differs from conventional IC technology is concerned with the topological problem of interconnecting large numbers of gates on a chip. To date, by carefully laying out components, designers of conventional integrated circuits have been successful in providing electrical interconnections with only a single layer of metallization and, where crossing of leads was unavoidable, a limited number

Fig. 1—Laminar flow facilities used in IC fabrication



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of diffused "crossunders." The large number of low-resistance interconnects required on arrays, however, has made a second layer of metal crossovers mandatory.

After the first interconnect patterns have been formed, a silicon dioxide insulating film is deposited on the wafer; windows are etched through this film where contacts are required. A second level of metal is then evaporated and etched. Fig. 2 is a photograph of the two-layer metallization crossovers on an experimental RCA array and illustrates the application of this technique.

Fabrication of the multilevel metallization interconnect is one of the most critical operations in the manufacture of arrays because shorts through pinholes in the dielectric or damaged interconnects can impair array operation even if all components are good.

The two photomasking steps required in two-layer metallization represent one quarter of the total photoresist operation. This means that the use of high-yield techniques is unavoidable especially in the discretionary approach. An important advantage of the RCA fixed-wiring approach is that, because of smaller chip size and fixed wiring, the numbers and locations of the second-level metal crossovers can be carefully optimized in advance to minimize lead lengths and the possibility of shorts; these factors result in definite yield advantages in this critical fabrication stage.

High-Yield Processing Techniques

Because LSI arrays are much more complex than present typical commercial IC's, it is anticipated that special processing techniques will be required to achieve consistently high yields. Fortunately, there appears to be no theoretical reason why any defective components need occur on silicon wafers processed through typical integrated-circuit fabrication sequences. From time to time, wafers of exceptional perfection are observed among the regular commercial product, supporting projections that with sufficient care and environmental control, high-yield wafers can be fabricated reiteratively on a production basis.

Four basic approaches to high-yield processing are now being studied:

1) Use of minimum-area devices;
2) Close-spaced photolithographic methods to improve the perfection of the photoresist operation;
3) Extensive use of redundant processing sequences; and
4) Use of special-care handling and environmental controls to ensure a continuous quality product.

Minimum Area Devices

Most of the defects occurring during IC fabrication occur randomly over the silicon wafers. These defects include imperfect areas on the silicon wafer itself, defects caused by dust, and defects caused by random photomask flaws. Small-area arrays, on the average, contain fewer such random defects than large-area arrays, and, all other factors being equal, show a higher percentage of yield. An added benefit of the smaller size array is that the number of chips per wafer increases rapidly as array size is reduced. Based on such area considerations alone, yield per wafer (which determines cost) will vary approximately with the inverse square of array area. Thus, significant improvements in yield can result through area conservation.

DR. ANDREW G. F. DINGWALL received the BSME from Princeton University in 1949 and the MS from Columbia University in 1950. He was a Fulbright Exchange Scholar at the University of Sheffield, England, where he received the PhD in glass and ceramic technology in 1953. He received the MS in mathematics from the Polytechnic Institute of Brooklyn in 1956, where he recently completed the course requirements for the PhD degree in mathematics. Dr. Dingwall joined the Electron Tube Division in 1953 as a member of the Electron Physics Group of the Chemical and Physical Laboratory, where he made significant contributions to the high-temperature operation of electron tubes. He joined the Thermoelectric Device Development activity in 1961, where he was active in the development of both chemical processes and devices, utilizing high-temperature silicon-germanium semiconducting alloys for direct energy conversion. He received an ECD engineering achievement award in 1963. Dr. Dingwall joined the RCA Integrated Circuit Department in 1966 and has been active in high yield processing of bipolar arrays. Dr. Dingwall is a member of the American Ceramic Society, a member of the American Physical Society, and a member of the American Mathematical Society. He has authored numerous technical papers and has fourteen patents pending.

Fortunately, through careful circuit design and component layout, the basic cells in an array can be made more compact. The use of special-care photoresist techniques to ensure accurate pattern registration and edge definition can also permit area savings through tignter dimensional tolerances.

Fig. 3 summarizes calculations of yield versus array area assuming a model in which various levels of defects are presumed to be distributed randomly over a wafer and where Poisson statistics are applicable. Advantages of a high-yield process capability are illustrated by the family of curves which show the fall-off of yield with processing technique. The estimated benefits of compactness are illustrated by comparing the area-yield relationship of a 100-gate array constructed of "conventional" components with a 100-gate array of "compact" components. Finally, comparison is made in Fig. 3 of the area-yield relation of typical commercial IC's with that of arrays scheduled for fabrication in these studies. Note that arrays of greater area than planned have been successfully constructed with conventional components, suggesting that random defects alone will not limit present program objectives.

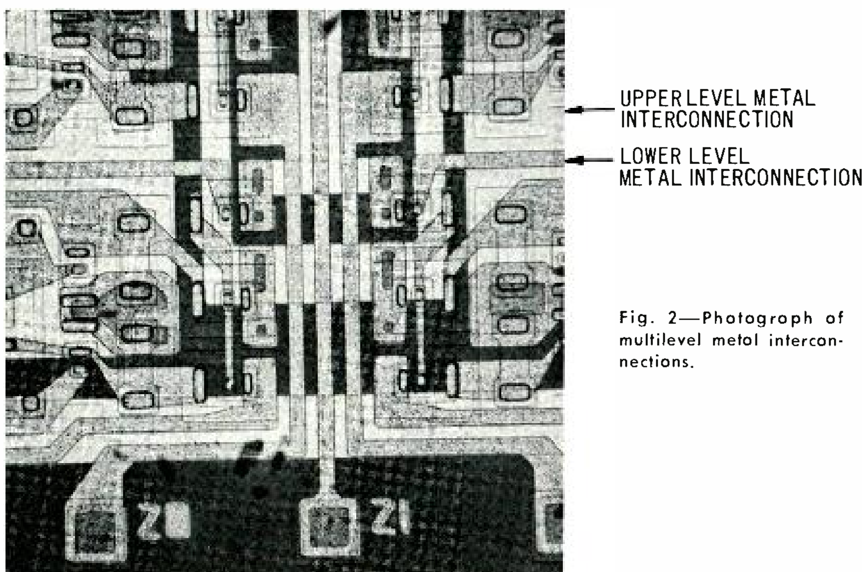

Fig. 2—Photograph of multilevel metol interconnections.

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Close-Spaced Photolithography

Imperfect photoresist-generated patterns represent the largest single source of defects occurring in the conventional integrated-circuit process. Because of the high component density employed in arrays, all dimensional tolerances must be maintained closely to ensure proper circuit functioning. Even relatively small deviations from ideal component dimensions due to photoresist defects can lead to imperfect arrays due to shorted components or open circuits, and in the case of resistors, to incorrect resistance values. Among the most common sources of defective photoresist patterns are:

1) Scratches and tears in the photoresist resulting from contact between photomasks and photoresist-coated wafers during the photographic contact printing step.
2) Scratches, tears, and lumps of photoresist on the photomask resulting from contact with the photoresist on the silicon wafer during the photographic contact printing step.
3) Imperfections in the photomasks as received.
4) Pinholes in the photoresist caused by a print image of opaque dust particles, or imperfect films.

The importance of virtually perfect photoresist techniques is best illustrated by noting that a minimum of eight distinct photoresist steps are required in LSI fabrication. These steps are summarized in Table I. A single defective pattern in any of the eight photomask stages, among any of the 1500 to 3000 transistor and resistor patterns in a 100-gate array, may cause the entire array to be inoperative. It is, therefore, necessary to form 10,000 to 20,000 "perfect" patterns to ensure proper array functioning.

Fig. 4 compares the close-spaced photolithographic techniques being used experimentally for LSI fabrication with conventional contact printing. As shown in Fig. 4(a), mask and wafer are brought into intimate contact under pressure for exposure and conventional contact printing. The unavoidable mechanical abrasion present in this process results in damage to both photomask and photoresist coating. All such damaged or scratched areas on the photomask are faithfully reproduced on all subsequent wafers on which the mask is used. Because damage occurs even on the first contact printing, there is little incentive to obtain "perfect" photomasks because the perfection is lost with the first use.

With close-spaced photolithography as shown in Fig. 4(b), however, generation of photographic images on the wafer is achieved without physical contact; mask and wafer are separated by a small distance and the image is formed on the wafer by shadows cast by the opaque regions on the photomask under parallel illumination. Absence of physical contact during the photographic step prevents mechanical damage to the photoresist and mask during exposure and permits many high-quality images to be generated from the same mask. Under these revised procedures there is great incentive to obtain highest quality photomasks; this task has become an important segment of the LSI high-yield program.

While close-spaced photolithographic techniques have been useful in improving the perfection of photoresist patterns, the use of this technique requires a tradeoff with optical resolution due to Fresnel diffraction effects, manifested as fringes about the periphery of the photoresist images. Analytical and experimental analyses of this problem are in good agreement and indicate that fringing and resolution losses can be controlled with suitable component design provided mask-to-wafer spacings do not exceed 1 mil.

Redundant Processing

Redundancy provides yet another powerful approach to high-yield processing; an approach which is especially useful in reducing pinhole defects. The basic purpose of redundant processing is to provide a second line of defense against potential sources of defects. For failure to occur in the composite system, it is necessary that defects coincide exactly in both lines of defense. However, since additional processing is normally required to achieve the benefits of redundancy, it is necessary that more defects be removed than reintroduced during the extra processing for this approach to be effective.

Fig. 5 presents calculations of improvements in yield which may be obtained when redundant processing is used. To simplify this example, it has been assumed that both the original and redundant process have the same fraction defective and that failure occurs in the composite system only when defective areas coincide exactly. It will be noted from Fig. 5 that relatively little improvement in yield is possible when almost all areas are defective. However, very substantial improvements in yield result when defective areas are rare. This latter case, fortunately, is generally applicable to pinhole defects.

Fig. 6 shows how redundancy can provide added protection against pinhole defects in thermally-grown oxide masking layers. The two independently deposited oxide layers provide improved protection against pinholes because of the unlikelihood that two pinholes will be exactly superimposed. Similarly, multiple processing may be useful for repairing tears and pinholes in photoresist images. By applying a second photoresist coating and aligning an independent mask over the original pattern, a second independent redundant photoresist image is provided in which the probability is low that the defects will align exactly. Although multiple photoresist processing reduces pinhole defects, it also tends to double the number of defects due to "reverse pinholes" or undesired "oxide spots"; some of these defects are tolerable in certain of the fabrication steps, but a careful analysis is required to ensure optimized yields.

A basis for optimizing the use of redundant processing sequences is provided by an analysis of the sensitivity to pinhole defects of each stage of the array fabrication process. Table I summarizes the effect on yield of a pinhole defect

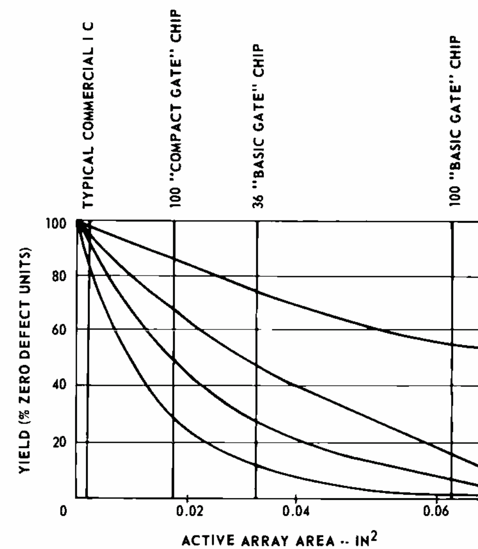

Fig. 3—Calculated yield versus array area.

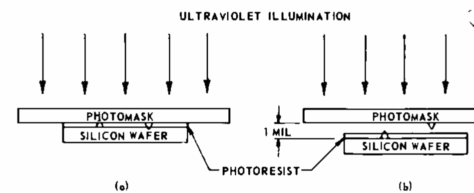

Fig. 4—Comparison of conventional and closed-space photolithographic techniques: a) Contact printing, b) Close-spaced photolithography.

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for each fabrication step of a typical array and the probability that a pinhole will fall on a critical area and cause a defective array. In computing Table I, it was assumed that oxide pinholes averaged 3 microns[4] in size and occurred randomly. Clearly, the isolation and first- and second-level contact stages are most susceptible to pinhole defects, and redundant processing sequences are most desirable at these points.

Special-Care Processing

Although extra care is the rule in the manufacture of integrated circuits, it is nonetheless possible to make yield improvements through the exercise of additional special care. Improvements have resulted from

1) Stringent inspection criteria on incoming materials, photomasks, and wafers in process;
2) Use of specially trained, experienced, and highly motivated personnel for high-yield work; and
3) Conduction of ultra-clean operations for contamination control.

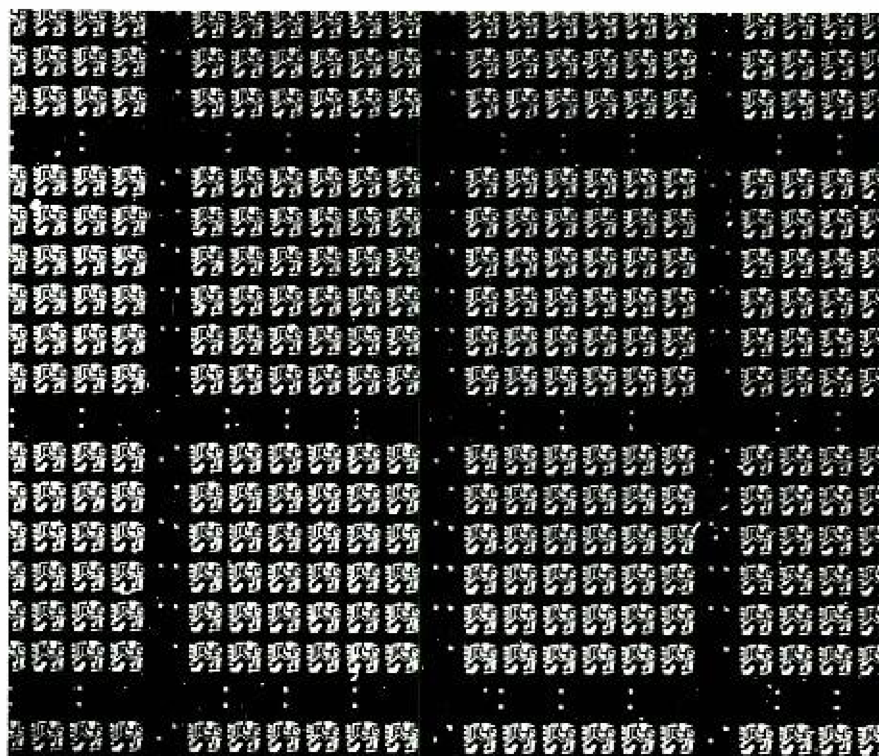

Fig. 7—Experimental 300-transistor array.

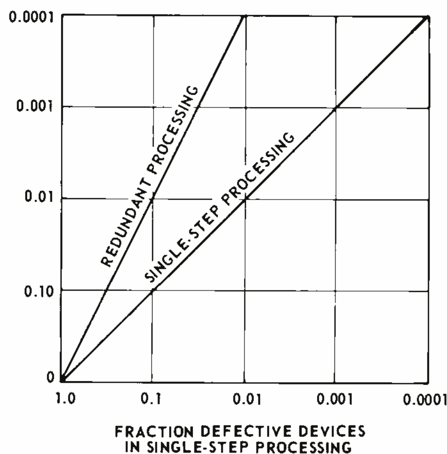

Fig. 5—Calculated improvements in yield for ideal redundant processing sequences.

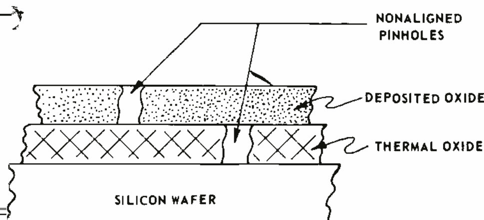

Fig. 6—Use of two independent oxide layers for redundant protection against pinhole defects.

Particle control is a special-care processing area which is being actively studied in RCA array programs. Dust is a major contaminant because particles can "print through" in the critical photographic steps and cause imperfect photoresist patterns. Similarly, particles adhering to the wafers during a wafer diffusion will cause localized contamination of array components. To combat dust, integrated circuits are normally fabricated in laminar-flow clean rooms or boxes where high-efficiency filters reduce typical atmospheric particle counts of 500,000 per cubic foot by a factor of 5,000 to 10,000. As part of the program to control dust, critical array fabrication stages are completed under the doubly-high-efficiency filtration conditions offered by laminar flow boxes within laminar flow rooms. Further, only highly filtered solutions are permitted to contact the wafers. Such ultraclean ambients will aid in the realization of maximum cleanliness attainable under laboratory conditions.

FABRICATION OF EXPERIMENTAL ARRAYS

Present program plans call for the fabrication of 100-gate arrays containing 700 to 1500 transistors during early 1968. To gain experience in the high-yield techniques of handling and testing such arrays, programs in 1967 were directed toward the fabrication of a number of increasingly complex multigate circuits. As noted previously in Fig. 3, chips currently fabricated are as large in area (although not in component density) as the ultimate goals of this high yield program.

Fig. 7 shows details of a 36-gate full-adder array constructed under the high-yield program. Each array contains approximately 300 transistors, and 250 resistors at a moderate packing density. The components are combined on a chip 0.175-inch square; this chip represents an active chip equal to or as large as, that of maximum current program plans.

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TABLE I—Photoresist steps required in LSI Fabrication and the effect of pinholes on yield for a typical array.

Photoresist Step (Mask)	*Defect*	*Probability that pinhole is not harmful*
N+ pocket	10-volt breakdown	0.96
Isolation	shorts to ground	0.71
Base & resist.	—	1.00
Emitters	6-volt breakdown	0.90
Contacts	shorts	0.68
First metal	—	1.00
Second contacts	shorts to first metal layer	0.79
Second metal	—	1.00

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PHOTOMASKS FOR LARGE-SCALE INTEGRATION

Photomask generating capability has kept pace with requirements by the continued introduction of better equipment and procedures into the Photomask Operation. As demands for more precise and complex imagery increase with the LSI approach, photomask technology will expand to encompass them. The Photomask Operation is staffed and structured to provide the design engineer with the best photomask for his application. Questions about a specific problem or creative approach to a new LSI design receive serious attention and frequently result in another advance in capability and technology.

E. W. CONLEY

Photomask Operation

Electronic Components and Devices, Somerville, N. J.

PHOTOMASKS—basic tools for semiconductor engineering development and manufacturing—are glass plates containing arrays of microscopic semiconductor-device images. Photomasks of various types in chrome and emulsion are shown in Fig. 1. This paper describes the basic steps in the production of a photomask and discusses photomask parameters and limiting conditions, especially for large-scale integration (LSI).

PHOTOMASK PRODUCTION

Artwork

Artwork is an enlarged representation on film of the finished device, typically 200 times final size. The two types of artwork in general use are 1) photographically produced on a computer-controlled light-trace table and 2) scribed and stripped two-layer film. The scribing film is a layer of clear plastic coated with a thin layer of opaque gelatin which is cut and stripped on a coordinatograph (Fig. 2). The pattern is made clear by peeling away the areas of gelatin that describe the semiconductor image. The films are inspected on a light table as shown in Fig. 3.

Final manuscript received August 8, 1967.

First Reduction

The second step in photomask production involves the reduction of the film images. For the first of two reductions, a large camera such as that shown in Fig. 4 is used. The camera is a specially-designed micro-photographic instrument in which the prime feature is the capability to produce predetermined, repetitive reductions to a high degree of accuracy. The reduction process is a highly specialized procedure in that the system of copyboard, lens, and photosensitive plate must yield true distortionless images of every detail in the original artwork.

Reticle Alignment

After the artwork has been reduced onto high-resolution glass photographic plates and developed, it is inspected again and mounted on metal frames. The images are carefully aligned in the frames by a reticle aligner as shown in Fig. 5. The reticle aligner is equipped with a master reference gauge that operates in conjunction with a cross hair in the microscope mounted on the equipment. The

Fig. 1—Some typical photomasks.

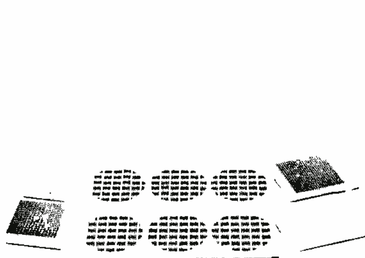
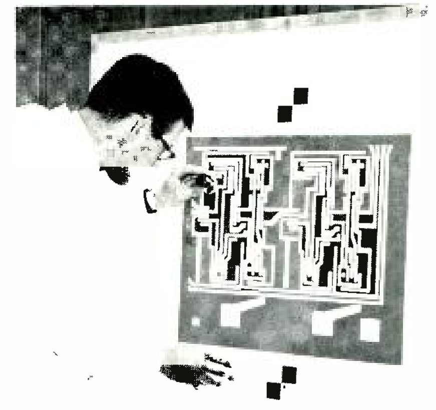


Fig. 2—A coordinatograph.

Fig. 3—Light table.



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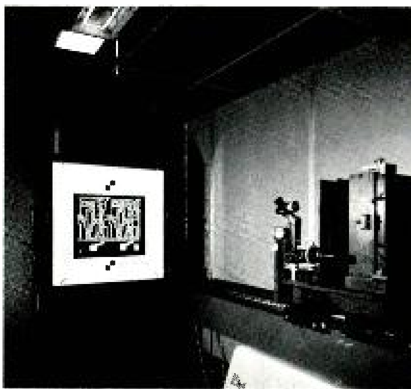
Fig. 4—Camera used for first reduction of artwork.

Fig. 5—Reticle aligner.

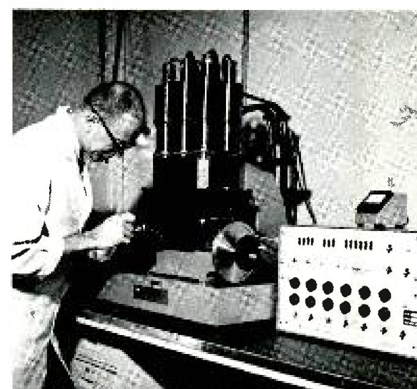
Fig. 6—Photorepeater.

operator manipulates the vacuum-held photographic plate until its reference marks are coincident with the crosshair. The plate is then permanently attached to the frame. Alignment is necessary to insure that the image is on the optical axis of the photorepeater, the next instrument used in the photomask production process.

Photorepeater Master Plates

The mounted images are placed in a highly specialized machine called a photorepeater. The photorepeater, (Fig. 6) is a mechanical device that optically reduces the intermediate image and transfers it to a photographic plate by flashing a xenon lamp as the plate is traversed. The photorepeater generates images in rows on an ultra-flat photographic plate by successive exposure of a single image; the location of an image relative to others is determined by the paper-tape-controlled digital encoding and counting circuit that triggers the flash. The development and inspection of the photorepeater master plates complete the most important phases in the photomask production process. The master plates contain all of the device geometries in finished one-to-one precision; they are the source of all contact prints used in making solid-state components.

Contact Printing of the Photomasks

The final step in photomask production is the making of a contact print, a reverse tone reproduction of the photorepeater master plate. Contact printing is performed in a laminar-flow work station and consists of placing a master plate, with its emulsion surface away from the light source, against the emulsion side of high-resolution glass plate in a printing fixture. Air is evacuated from between the plates and, after a sufficient vacuum has been attained, a xenon lamp is pulsed to expose the photoplate through the master. Absolute contact of the two emulsions is necessary to eliminate the possibility of diffraction of light at an image edge. Diffraction could cause loss of definition and affect the size of image elements during the transfer process. After exposure in the contact printing fixture, the plates are chemically developed to establish the images. The resulting prints are the photomasks.

E. W. CONLEY received the BS degree in Electrical Engineering from West Virginia University in 1953. He then joined the General Electric Company Engineering Training Program. In 1954, he was admitted to the Advanced Technical Course and in 1955, to the Creative Engineering Program. Training assignments at several plant locations preceded his joining the Advanced Equipment Development Group in Schenectady where he developed various high speed grid winding equipments for planar and frame grids. Mr. Conley joined RCA at Somerville, N. J. in 1959 as a member of the Advanced Mechanical Design Department and contributed extensively to the design of work stations on the Automatic Device Assembly Machine. In 1960, he joined the Equipment Development Operation where he designed and developed solid state processing equipment such as a photomask-wafer aligner, nail-head thermo-compression bonder, pellet sorter, and techniques for grinding and polishing bulk crystal into confocal laser rods. Mr. Conley joined the Photomask Operation in 1964 where he has been responsible for the advanced development of new equipment, processes, and techniques for making photomasks. Mr. Conley is a member of IEEE and Eta Kappa Nu. He holds a patent on micro-manipulators and has one pending on photomask contact printing.

Photomasks are typically two inches square and contain an array one-and-one-half inches square. There are several sizes of photomask plates available in both chrome and emulsion; however, chrome is preferred because of its natural resistance to abrasion.

Photoplates

High resolution plates are available in various grades of flatness: plates flat to 0.001 inch per inch are used for contact prints; plates flat to 0.0005 inch per inch are used as photorepeater masters. The flattest plates, 0.00002 inch per inch, are used for experimental purposes.

Processing

Photoplate images are fixed by chemical processing in a laminar-flow ultrasonic developing device with temperature controlled baths and recirculated refiltered solutions. These conditions are necessary to prevent particulate matter from adhering to the emulsion and obstructing wetting action. Such obstructions could cause pinhole effects in the images on the photoplate. Developing-cycle timing and the concentration of the solutions used determines the edge quality of the elemental parts of the photomask. The edges of a printed element may be made to extend or retract from the master dimension by 0.000030 inch through adjustments in the developing process.

SYSTEM CONSIDERATIONS FOR LSI PHOTOMASKS

The above procedures and equipment are designed to provide a system whereby general photomask requirements are met and exceeded. The advent of LSI has subjected the system to a reappraisal because of the new requirements for ten-fold increases in area simultaneously with sub-micron accuracy.

These increased demands on the photomechanical equipment for large-scale integration are being met by using the best characteristics of the system with some modifications and new equipment.

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As the areas of LSI are increased, the "single image" limit of the system is first encountered at the photorepeater equipment.

Photorepeater Lenses

The principal concerns in a photorepeater are the maximum image size and accuracy. The image-field size of the photorepeater lens system is governed by the tolerable limits of distortion and resolution; a lens has the least distortion and best resolution at its center. By limiting the image size, these lens properties are used to maximum advantage. An image field diameter of one-tenth the focal length is commonly used. This limit yields field diameters in the photorepeater of 0.064 inch for 16 millimeter objective lenses and 0.140 inch for 35 millimeter lenses. These areas would encompass square pellet areas of 0.045 and 0.100 square inches respectively. Recently developed photorepeater lenses are expected to yield 0.375-inch field diameters. Because some LSI's are larger than the above maximum sizes, a means of bypassing these limits must be utilized to make large-area images.

Piecing

An image assembly technique is used to bypass the lens-field limits. The essential characteristic of this piecing method is the dissection of an oversize device in the early stage of photomask production and precision reassembly after passing through the limiting lens. An example of this technique is noted in Fig. 3, which shows one quadrant of a device at the artwork stage and its assembly with three other pieces in Fig. 7 after final reduction in the photorepeater. This technique rests heavily on the optical and mechanical accuracies of all the equipment, since the reassembled area must have no element or line mismatch with other parts of the same image or other photomasks in the series.

Piecing Methods

Photocomposition can be performed at various levels of complexity. The most fundamental approach is by using a single small element to build lines, rectangles, etc. This approach is considered as a means of computerized pattern generation both at the final and intermediate sizes. This technique of piecing elements and/or sections of devices can be extended indefinitely for large-scale integration. For example, a sub-division of the pattern as previously described is used when the device has a complex non-repetitive geometry. Another method of piecing is performed by joining a number of repetitive device sections into larger areas.

Image Accuracy

Image fidelity at piecing is assured by the lens reduction and mechanical accuracy of the photorepeater. The Y-axis placement accuracy of any image element is within ±0.000050 inch image-to-image non-cumulative. This is a manually set position for row location on the photorepeater master. The accuracy of image placement on the X-axis is more precise because it is regulated automatically as the plate is passed under the optical system by means of a motor-driven screw. The screw is attached to an encoding and digital-signaling circuit that flashes the xenon lamp to expose the images.

Continued development of encoding equipment has increased X-axis placement precision to ± 0.000020 inch. This figure is expected to be improved to ± 0.000010 inch in both axes.

The capability of the equipment to generate master plates to this high degree of precision in conjunction with piecing elements and parts gives the LSI designer freedom to extend his devices far beyond the lens field limits of photorepeaters.

Reduction Camera Lenses

The above methods of bypassing the lens field limits by photocomposition in the photorepeater presents the first reduction camera as the next possible limiting facility for LSI photomasks. The series of lenses used at the camera provide a wide range of available artwork reductions; Fig. 8 shows some typical lenses. The relationship between lens reduction and recommended maximum field diagonals is shown in Fig. 9. This maximum can be determined by matching a lens dot to a point on the lens-range scale with a straight-edge. Note that as the desired field coverage increases, the reduction ratios decrease.

Artwork

As the artwork size increases for larger LSI and the available reductions decrease, the effect is reflected into the artwork preparation equipment as a demand for higher precision. Any deviation in the artwork is a proportion of the final image so the accuracy must be such as to reduce the effects of any inherent mechanical inaccuracy. The scribing accuracy of the coordinatograph is generally held to ± 0.001 inch but can be held to ± 0.0001 inch in special cases. Since the system total reduction through the camera and photorepeater may be from 60 to 1000 times, the ± 0.001 inch error is about 16 micro-inches, or less, on the final image. Artwork generated on the computer-controlled light table has approximately twice the error of scribed artwork. The advantages of computer-controlled artwork over scribed artwork for LSI are a marked decrease in artwork preparation labor and the relatively short turn-around time for alterations.

Fig. 7—Photo repeater-assembled circuit.

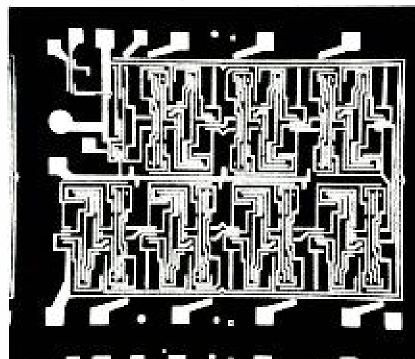
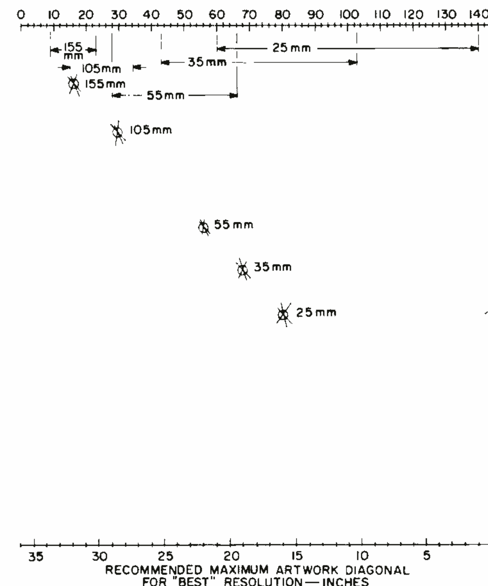


Fig. 8—Camera lenses.

Fig. 9—Camera Lens Chart.



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INTEGRATED-CIRCUIT RELIABILITY

The ever-increasing use of integrated circuits is the result of several factors, among them the promise of high reliability. This high reliability is a function of the inherent reliability of the integrated-circuit chip, derived from the fact that all components are produced simultaneously on a single silicon chip, and the care, quality control, and testing programs that are utilized in manufacturing the circuits. This paper describes some of the work done at RCA, Somerville to ensure reliable IC production through quality control and testing.

T. SPITZ

Integrated Circuit Design

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THE current fiscal situation in the commercial integrated-circuit field precludes a high-reliability screening program; reliability must be built into the circuits. For this reason, a great deal of effort is being expended in the development of highly sophisticated techniques, such as fabrication in laminar flow rooms, ultrasonic bonding, and the use of computer-controlled test sets for both circuit characteristic analysis and diagnostic analysis of failures.

CONSTRUCTION FOR RELIABILITY

Integrated circuits are produced by a complex process consisting of more than 100 basic steps including 4 to 6 diffusions, 4 to 6 etchings, 4 to 6 photomaskings, 2 to 4 thermal oxidations, 2 to 3 evaporations, and 6 to 10 cleaning operations. Thus, a large number of potential failure modes exist. Each can effect production-line yield. However, there is little correlation between low yield and reliability, because very few devices that demonstrate correct electrical characteristics contain potential failure mechanisms. Most process errors result in chips that are catastrophic failures electrically. The circuits containing flaws are located and removed at the first electrical test, while the device is still in wafer form.

To assure control of the production processes, the Quality Control Department performs as many as 103 inspections along the fabrication line. The inspections include checks on such essentials as resistivity, layer thickness, photoresist thickness, and bake temperature.

The sealing of an integrated circuit in its package is accomplished in a dry-nitrogen atmosphere. Dry nitrogen is used to insure the elimination of all moisture which would, over a period of time, attack any exposed metalization in the device and increase leakage between terminals in the circuit.

Very few reliability problems are associated with the chip proper. Most problems arise from the deposition of the interconnect metalization, and the interconnecting of the circuit chips into usable packages.

As one of the final steps in the processing of a wafer, a layer of silane glass is now being grown over the metalization in an effort to protect it during handling prior to sealing.

All circuits produced by RCA are now bonded by ultrasonic welding and utilize 1.5-mil aluminum bonding wire for an aluminum to aluminum junction on the chip. Furthermore, a visual inspection is made of all bonds before the package is sealed. ICs produced by RCA are presently supplied in one of six packages: an 8, 10, or 12 terminal modified TO-5 can; a ceramic 14-lead flat pack or 14-lead dual-in-line ceramic package; or a plastic 14-lead dual-in-line package. All of these package types are shown in Fig. 1. All but the plastic package are hermetically sealed in welding.

TESTING FOR RELIABILITY

A complete electrical test is performed on an IC while the device is still a single chip on a wafer of several hundred chips. A multiple-point probe and high-speed automatic test set such as that shown in Fig. 2 sorts out acceptable units from failures.

After the devices are sealed, they undergo a series of preconditioning processes which are intended to pinpoint those units that might be potential failures. The preconditioning processes are aimed at detecting nonhermeticity and temperature-dependent failure modes, such as weak bonds and poor mounting; these processes are:

1) Temperature cycling: $-65°C$ to $+150°C$
2) Helium leak test: 1×10^{-8} cc/sec at 1 atmosphere
3) Gross leak test: 5×10^{-4} cc/sec Hologen

After preconditioning, the units are electrically tested to insure conformance with circuit specifications. Testing at this stage usually involves a great number of static tests, performed on high-speed test equipment of the type shown in Fig. 2, and several functional or switching tests.

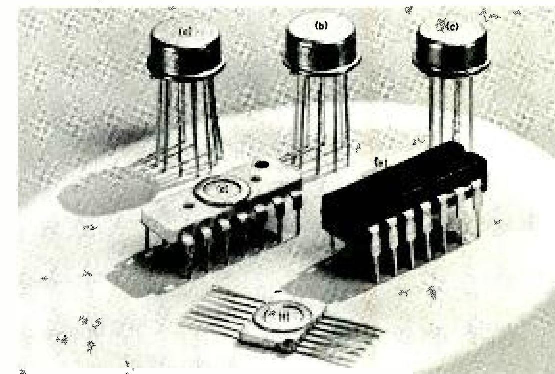
The Quality Control Department audits all tests and selects a sample on a lot-tolerance percent-defective basis to be submitted for mechanical and environmental testing.

ENGINEERING RELIABILITY STUDIES

The Engineering Reliability Group is responsible for evaluating finished circuits and for determining the tolerance of each to all types of environment. One portion of this task is accomplished by subjecting the circuits to the tests listed in Table I. The Engineering Reliability Group must also develop tests that will stress the circuits far beyond the standard military requirements so that the appearance of any potential failure mechanism will be accelerated. Failures resulting from the tests are analyzed and weaknesses pinpointed so that Design Engineering can take steps to improve materials, processes, or packaging.

In determining the weakest point in an integrated circuit, some units are

Fig. 1—Package types: a) 12-terminal TO-5 can. b) 10-terminal TO-5 can. c) 8-terminal TO-5 can. d) 14-lead dual-in-line ceramic package. e) 14-lead dual-in-line plastic package. f) 14-lead flat pack.



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stressed to destruction so that the safety margin between the unit's actual capability and its specified capability can be determined and so that those failure mechanisms most likely to become reliability problems can be identified.

The testing program for any new circuit or package is designed specifically for that device and usually includes some special as well as some standard tests.

Some of the standard tests shown in Table I have been increased in severity for the purpose of engineering evaluation. Mechanical shock, for example, is performed at 3000 g's—the limit of the equipment presently available. Constant acceleration is currently performed at 40,000 g's; however, new equipment is being ordered which will raise this figure to 100,000 g's. Operating life tests are normally run for many thousands of hours in excess of the required 1000 hours.

TABLE I—IC Reliability Tests

Test	*MIL STD*	*Method*	*Condition*	*Special Conditions*
Physical Dimensions	750	2036	—	None
Thermal Shock	750	1056	B	−65°C to +125°C
Hermetic Seal	202	112	IIIa	1×10^{-8} cc/sec
Gross Leak	—	—	—	1×10^{-4} cc/sec freon
Moisture Resistance	750	1021	—	10 days, at 98% relative humidity
Mechanical Shock	750	2016	—	3000 g's, 0.5 ms, 5 blows in 6 directions
Vibration Fatigue, Variable Freq.	750	2056	—	100 to 2000 Hz
Constant Acceleration	750	2006	—	40,000 g's
Terminal Strength	750	2036	A	2 lbs for 3 seconds
			E	0.5 lb., 5 bends
			F	2 lbs for 3 seconds
Solderability	750	2026	—	All leads
Salt Atmosphere	750	1041	—	None
Storage Life Tests	—	—	—	Temperature: 200°C ±3°C; test time: 1000 hours
Operating Life Tests	—	—	—	Temperature: 125°C ±3°C; test time: 1000 hours minimum

Fig. 2—High-speed automatic test equipment and multiple probe used in electrical testing.

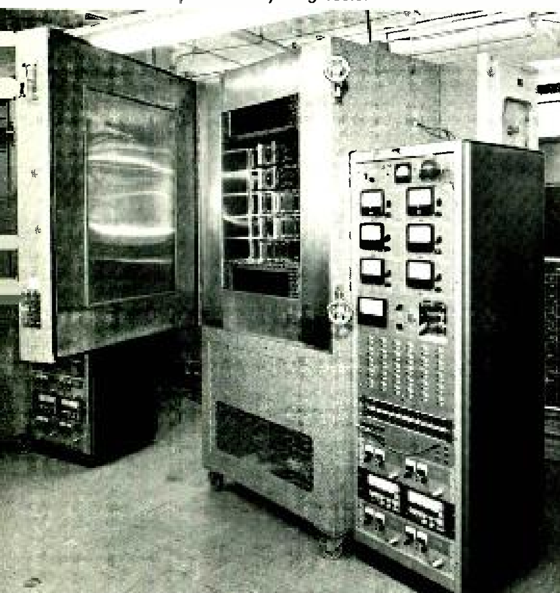

Fig. 3—Cycling chamber used in long-duration temperature cycling tests.

The following are typical of the special tests included in new programs:

1) *Long-duration temperature cycling test:* a sample of units is operated dynamically, in the cycling chamber shown in Fig. 3 and subjected to varying temperatures over a 6-hour period: one hour at −65°C, two hours of increasing temperature to +125°C, one hour at +125°C, and a two-hour period of decreasing temperature to −65°C. In 1000 hours, this cycle is repeated 166 times. Another sample of units undergoes dynamic life testing in the same test circuits at +125°C and in the same test circuits. Dynamic life testing is performed concurrently with the temperature cycling test. In dynamic life testing, units are operated at rated voltage and all digital devices are tested in ring oscillators with 50-percent duty cycles. The cycling test described has proven to be 8 to 10 times more effective in accelerating failures than those tests performed at a constant +125°C (based on equal numbers of test hours).
2) *Wide excursion storage cycling test:* devices are cycled between exposures in a container of liquid nitrogen at −195.5°C and an oven set to +200°C. The total cycle of 1 minute at the low temperature and 10 minutes at the high temperature plus the time required to periodically replenish the supply of liquid nitrogen results in a rate of approximately 20 cycles/day. Devices are normally exposed to 50 cycles of this environment. This has proven to be the equivalent of many times more cycles at a lesser temperature difference and has proven highly successful in uncovering potential failures.
3) *Multiple thermal-shock test:* where the number of temperature cycles is thought to be important, cycling is performed between two chambers, one set at −65°C and the other at +150°C. Many new package developments have undergone 250 or more such cycles at rates of about 3/hour or 25/day for 10 days. Temperature exposures of 10 minutes are more than sufficient to allow the pellet to come to the ambient temperature. Devices are electrically tested at regular intervals throughout multiple thermal-shock testing.
4) *Step-stress-to-destruction test:* the temperature of a unit is raised in steps of 25°C until it fails. The unit is then analyzed to determine the cause of failure. The limiting factor during these tests has been found to be in chip-to-package mounting, chiefly because the gold used in most mounting operations melts at approximately 375°C. Chips mounted with epoxy adhesives are rated at even lower temperatures.

The advent of the plastic package has necessitated the addition of tests aimed at determining the capability of non-hermetic devices to withstand moisture. A common kitchen pressure cooker has proven of great value in determining this capability in that it subjects units to a temperature of over 120°C at 100-percent humidity and a pressure 15 pounds above atmosphere. These conditions tend to force moisture into the package along the leads and toward the pellet.

Units are tested immediately after removal from the cooker, before any moisture can escape. Leakage tests are usually stressed due to their sensitivity to moisture. In another type of moisture test, devices are cycled between the pressure cooker and a −65°C chamber. Moisture remaining in the unit freezes and tends to break or chip the plastic.

VALIDITY OF PRESENT TESTING

More than 200 units have been subjected to a storage life test at +200°C for 1000 hours each according to standard storage life-test procedures; not one unit failed. This test, therefore, is not considered severe enough or as effective as the dynamic life test.

Standard dynamic life tests are performed throughout the industry at

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+125°C; a standard temperature originated by the military specification MIL-STD-202, Method 107. This test, though quite severe, is not severe enough for engineering reliability studies. Therefore, for each group of new units that is tested at +125°C, another group is subjected to the dynamic temperature cycling previously described.

Fig. 4 shows the failure rates for two groups of units life tested over the past two years. As explained above, the cycling environment is several times more severe than the constant-temperature life-test environment. With far fewer units under test, nearly four times as many failures were caused by the cycling tests.

Another interesting deduction may be made from the curves in Fig. 4: a prestressing (or "burning in") of as much as 1000 hours would not effectively change the failure rate for the succeeding 1000-hour periods because the failure rate remains relatively constant up to at least 7000 hours.

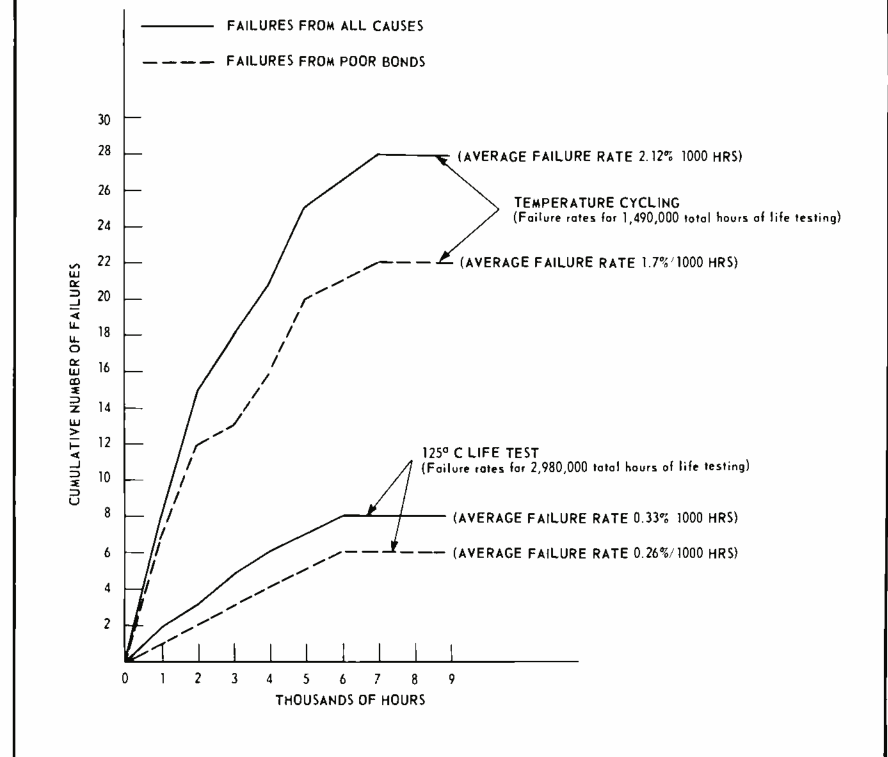

Fig. 4—Failure distribution resulting from standard life tests at 125°C and cycling between —65°C and +125°C.

FAILURE ANALYSIS

All of the testing previously described would be valueless were it not for the ability to locate and eliminate, through analysis, the causes of circuit failure. Complete electrical data for a circuit is analyzed by both the Reliability Engineering Group and the cognizant circuit design engineer. As an aid in the electrical diagnosis, a computer controlled test set such as that shown in Fig. 5 is used to test and analyze the cause of the failure.[1] The package is then opened and a visual examination made to verify the electrical analysis. If necessary, the device is probed and readings taken of the characteristics of the components in the unit. After probing has identified the general area of the failure, the circuit is examined by the semiconductor-device engineer whose responsibility it is to determine the exact mechanism in the semiconductor material, metalization, bonding, or package that caused the failure. Many facilities are available at Somerville for detailed analysis. These facilities include X-ray and spectroscopic equipment, as well as complete chemical laboratories in which the nature of any contamination on a circuit can be determined.

FUTURE IC RELIABILITY

The main causes of integrated-circuit failure are being pinpointed, and changes in processing or materials made to eliminate them. For example, new methods of sputtering and evaporating glass over the wafers have been developed that will protect the metalization against nearly all possible abuse. Methods of interconnecting chips to package leads are being tested which should greatly improve the reliability of circuits by eliminating bonding and bond wires. The continual improvement in reliability of RCA integrated circuits has been due to the test and modfication procedures described in this article; there will undoubtedly be still greater improvement in the near future.

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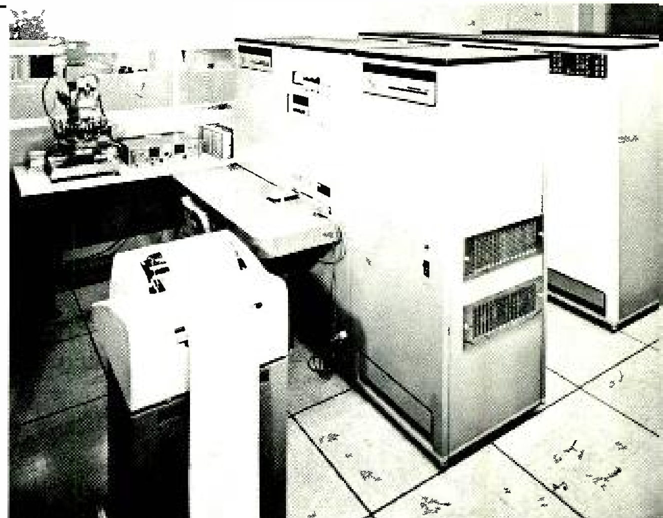
Fig. 5—Computer-controlled test set.



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EPITAXY—A VERSATILE TECHNOLOGY FOR INTEGRATED CIRCUITS

Epitaxy, a technique for vapor deposition of thin single-crystal silicon films, has made possible semiconductor structures heretofore unattainable and has been an important tool in the production of high performance integrated circuits. This relatively new and useful technique is perhaps revealed to its best advantage in integrated circuit manufacture where the increased freedom in design and fabrication are best utilized and where critical crystal and electrical properties must be precisely controlled. The epitaxial film constitutes the electrically active portion of the solid-state device or integrated circuit and to that extent its reproducibility and electronic perfection are essential to the performance and quality of the final circuit. This article highlights some of the more important aspects of epitaxy and shows its application to present and potential solid-state circuits.

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Many methods of epitaxial film production have been investigated and developed. These include vacuum evaporation, crystallization from solvents, and methods involving gas-phase chemical reactions.[1-5] The gas-phase chemical reactions have been particularly successful in that they have resulted in superior crystal formation, high film purity and fine control of film doping and thickness. The gas-phase epitaxial growth process in most widespread use in the U.S.A. involves the hydrogen reduction of silicon tetrachloride in the presence of appropriate doping agents. The popularity of this process stems from its simplicity, reliability, flexibility, and ease of adaptation to production demands.

The utility of the epitaxial process in the production of monolithic integrated circuits lies in its ability to produce reproducible thin semiconductor films with desired electrical properties and to enable formation of structures which lower the "saturation resistance" of diodes and transistors. In addition, the structures produced can, by solid-state diffusion, be easily isolated electrically, techniques into individual areas, each representing an active or passive circuit component. These isolated components in the surface of the silicon wafer can later be interconnected by metallization to form the complete circuit. The original approach to the fabrication of integrated circuits by diffusion technology was lacking in two respects: the ability to precisely control the thickness of high-resistivity active regions and the ability to reduce the "saturation resistance" of the active devices. Both of these capabilities are essential for present-day high-speed circuits.

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STRUCTURES

There are two nearly equivalent types of epitaxial integrated circuit structure in commercial production: the double layer structure, historically the first, and the pocket structure. These structures are shown after epitaxial deposition and isolation diffusion in Fig. 1.

The important features of the two-epitaxial-layered structure are the N^+ region (heavily doped and highly conducting) and the high-resistivity N region (usually 6 to 12 microns thick). Isolation is achieved with the help of local P^+ regions, formed by diffusion, which effectively surround the N and N^+ regions in a "bathtub" of P-type silicon. The P-N junction formed at the interface between the bathtub and the N/N^+ region, when properly biased electrically, becomes a reasonably good insulator. In the N region, active devices will be formed; the N^+ region facilitates current flow to the individual active devices.

In the pocket structure the important features are the localized N^+ (highly conducting) regions. These regions are formed by diffusing a high concentration of electrically active impurity (usually antimony or arsenic) onto the substrate through a silicon dioxide mask. The masking oxide is etched from the substrate and, after cleaning, the wafer is ready for epitaxial deposition.

Two disadvantages exist in the pocket structure:

1) There is additional need for oxidation and photolithographic and diffusion processing on the wafer before epitaxial film deposition.

2) Crystal structure in the epitaxial layer is relatively poor because it is difficult to clean the substrate adequately before epitaxial deposition.

These disadvantages are outweighed, however, by several advantages of the pocket structure over the layer structure:

1) Breakdown in the layer structure will occur between regions (3) and (2), shown in Fig. 1, and begins at 10 to 20 volts; breakdown in the pocket structure occurs between regions (3) and (1) and usually requires 50 to 100 volts. The higher breakdown voltage in the pocket structure results from the reduced impurity density in region (1) relative to region (2). As a result, larger voltages can be applied to these devices, and greater outputs can be realized.

2) In the layer structure, there is an electrical capacitance associated with

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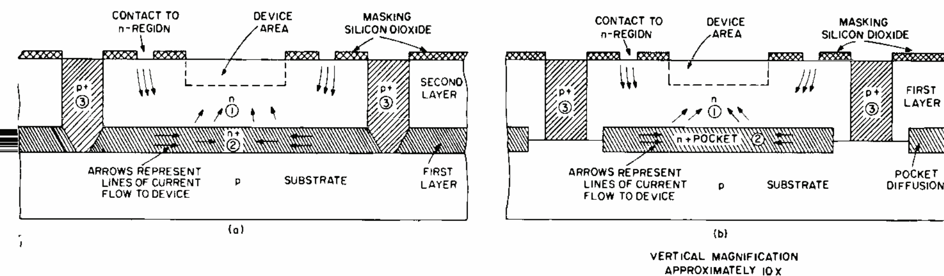


Fig. 1—Two common epitaxial structures used in monolithic integrated circuits: (a) layered structure and (b) pocket structure.

each P-N junction that increases with doping level on both sides of the junction. These distributed capacitances are parasitic and impair the performance of the circuit at high frequencies. In the pocket or buried layer structure, however, there is no significant capacitance between regions (3) and (2).

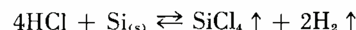
3) To achieve isolation in the layer structure, isolation diffusion must be carried on over an extremely long period of time so that the high background impurity density in region (2) can be overcome. Isolation diffusion times for the pocket structure are 3 or 4 times less than those required for the layer structure.

DEPOSITION SYSTEMS

An epitaxial deposition system consists basically of sources of gases or other volatile compounds which can be metered into a deposition chamber where environmental and process conditions can be precisely controlled. Control means the ability to vary environmental and process conditions with time so as to perform the desired etching and/or deposition reactions. A schematic of the gas-source portion of a typical epitaxial system is shown in Fig. 2. The chemical substances required in the deposition processes are delivered to the deposition chamber from this source area. Exact gaseous compositions are controlled through accurate needle valves and gas-flow meters; non-gaseous compounds, such as the $SiCl_4$, are delivered as volatile vapors borne by a hydrogen gas which serves as a carrier. When liquid or solid sources are used, thermostatic control of the evaporator may be required to maintain constant vapor pressure and permit fine control of the deposition process. Inasmuch as deposition consists of the introduction of various gases to the reaction chamber at different times and for various periods of time, the process lends itself rather well to relatively simple automation. Through the use of suitable sensing devices (such as two-color optical pyrometers for monitoring deposition temperature and a sequence of interval timers which can be preset to operate solenoid gas valves (not shown in Fig. 2) the entire cycle can be made completely automatic. The solenoid valves introduce or shut down gas flows at appropriate points in the cycle.

Deposition is normally performed at temperatures varying from 1200°C to 1250°C at rates from 0.5 to 2.0 microns/min. These conditions are such that for most structures a minimum amount of interdiffusion between layers or regions occurs and abrupt transitions in doping concentrations are achieved without significantly affecting the crystalline perfection of the growing layer. High gas velocities in the chambers insure product uniformity and also permit changes from one doping concentration to another in a matter of seconds. The flexibility of the epitaxial process is due mainly to these high gas velocities. Changes in resistivity and conductivity can be made at will during the course of the deposition process. Fig. 3 shows the commonly used doping impurity sources and the levels of doping available. It should be noted that resistivities, over a range of six orders of magnitude of both conductivity types can be achieved.

A very important feature of the epitaxial system is its ability to permit high-temperature etch cleaning of the silicon substrate before growth of the epitaxial layer.[6] This cleaning, which typically removes 0.5 to 5 microns of substrate, assures a substrate free of contamination and mechanical damage and produces a film of the highest purity. It also significantly improves the degree of crystalline perfection of the film and reduces the electrical leakage between the N region and the substrate. High-temperature etch cleaning is accomplished with 0.5 to 5-percent anhydrous HCl and may be defined chemically as the reverse of the deposition process:

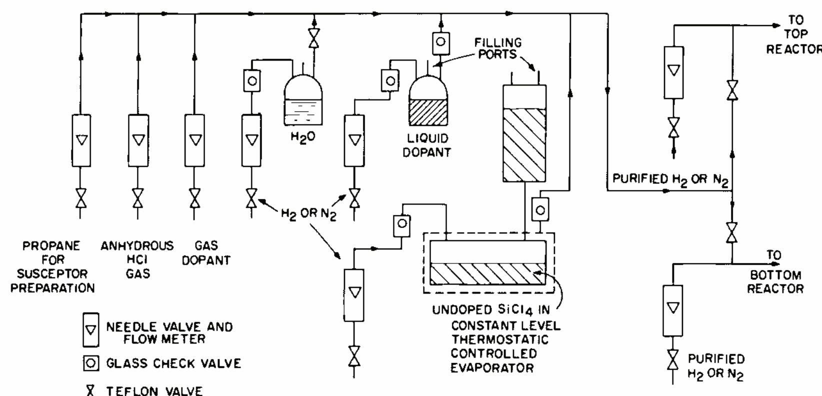


$$4HCl + Si_{(s)} \rightleftarrows SiCl_4 \uparrow + 2H_2 \uparrow$$

The water-vapor source shown schematically in Fig. 2 lends further versatility to the epitaxial process. This source is used in combination with $SiCl_4$, to vapor deposit SiO_2 films.[7] At elevated temperatures, a heterogenous hydrolysis occurs on the wafer surface producing a dense pinhole-free SiO_2 film. This film can be used as a substitute for the thermal SiO_2 layer normally used as a mask prior to isolation or pocket diffusion. The film in addition to permitting improved oxide integrity, decreases the possibility of contamination between the steps of epitaxial growth and thermal oxidation.

Within RCA, the horizontal epitaxial deposition system is in most widespread use although the rotating vertical system shows great potential from the viewpoints of increased capacities, cost reduction, and improved system uniformity and reliability. Fig. 4 shows the horizontal epitaxial deposition system; Fig. 5 shows the vertical system. Table I presents typical operating conditions and performance characteristics for typical horizontal and vertical epitaxial systems. The horizontal system requires a power source that operates at RF frequencies of 450 kHz because of external

Fig. 2—Gas-source portion of an epitaxial deposition system.



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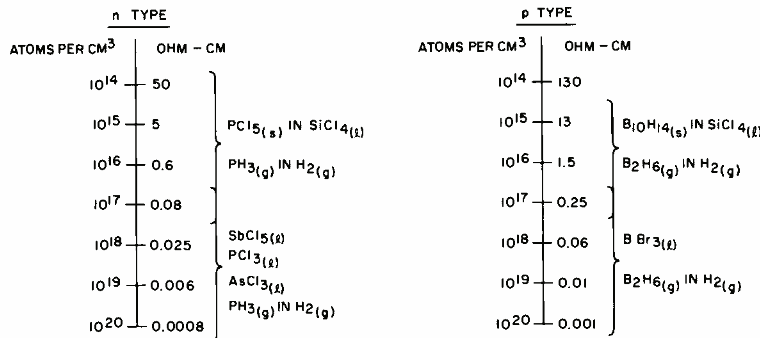


Fig. 3—Doping sources and levels for epitaxial films.

coupling demands. Individual units capable of processing fifty 1.25-inch wafers simultaneously require power sources with as much as 40 kilowatts output. The vertical system, because of improved coupling, can operate at lower frequencies, and 10-kHz motor-generator power sources are common. Induction heating is used in both systems because it is simple and provides clean localized heating. In addition, induction heating allows cold-chamber-wall operation which eliminates wall deposition and reduces stream depletion effects and chamber-wall spalling problems. In both systems, the susceptors are made of graphite coated with vapor-deposited silicon carbide. The processes involved in the preparation and treatment of a susceptor are extremely important in keeping contamination at a minimum, in obtaining high crystallographic perfection, and in maintaining the reliability of the epitaxial deposition process. A photograph of a production-type automatic horizontal system capable of handling twenty-six 1.25-inch diameter wafers simultaneously is shown in Fig. 6. Noteworthy features are the dust-free laminar-flow loading area, the dual-chamber front-loading arrangement and the automatic control console.

FILM EVALUATION

In large-array integrated circuits in which the individual circuit covers a large fraction of the wafer surface, it is important (particularly from the standpoint of high-yield production) that the film be uniform and homogeneous in critical properties over its entire surface, from wafer to wafer within a run, and from run to run. The ultimate objective of film evaluation[8] is to measure certain characteristics of the film directly and nondestructively for the purpose of quality control. Film properties most subject to fluctuation are layer resistivity, thickness, and crystallographic perfection. The procedures used at RCA for measuring these properties are described below.

Resistivity

The sheet resistivity (P_{si}) of the film in structures where it is isolated from the substrate, as in the two-layer epitaxial structure, can be measured by means of a simple in-line four-point probe in which the probe points are spaced 50 mils apart.[9-11] The sheet resistance of a single film is related to the bulk resistivity (P_{Bi}) as follows: $P_{Bi} = P_{si} t_i$, where t_i is film thickness. If more than one film of the same conductivity is involved, as is the case in the two-epitaxial-layered structure, the total sheet resistance (P_{s_T}) is given by:

$$P_{s_T} = \frac{1}{P_{s1}} + \frac{1}{P_{s2}}$$

If an isolating barrier is not part of the structure, an opposite-conductivity control wafer may be inserted into the system during deposition to provide a means for measurement of sheet resistivity on a suitable layer grown with the unknown. However, this method of measurement is indirect and interruption of the deposition process often causes defects in the crystalline structure of the film. The precision of this method of determining resistivity is usually limited by the precision with which film thickness (t_i) can be measured.

Resistivity can also be measured by means of a three-point probe.[12-14] With this type of probe, the reverse break-

TABLE I—Typical System Characteristics of Horizontal and Vertical Epitaxial Systems

Characteristic System	*Standard Horizontal System Value*	*Prototype Vertical System Value*
Deposition temperature (°C)	1100 to 1300	1100 to 1300
Growth rate (microns/min.)	0.5 to 3	0.5 to 3
HCl etch rates (microns/min.)	0.5 to 1.0	0.5 to 1.0
Mole ratio (H_2/Halide)	50 to 250	50 to 150
Hydrogen flow velocity (cm/min.)	1500 to 3000	500 to 2000
Capacity (number of 1¼" diameter wafers per run)	26	50 (approx.)
Total Cycle time, minutes (10-micron layer on pocket type)	45	60
RF input requirement (kW)	35	55
Reactor quartz requirement	Rectangular 4" x 1.5"	Cylindrical 6.5" dia.
Control capability in production (±%)		
Thickness	15	10
Resistivity	25	20

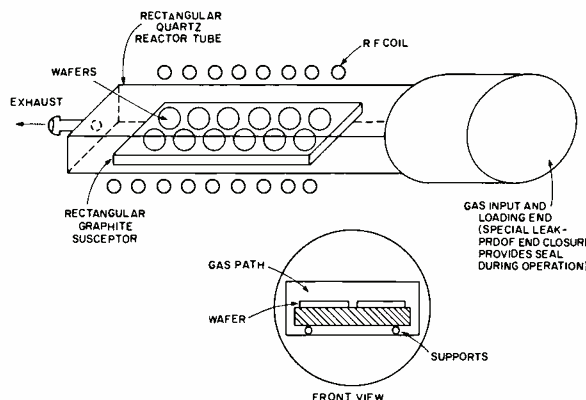
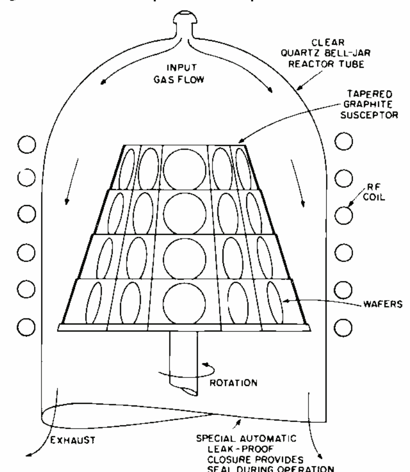


Fig. 4 — Horizontal epitaxial deposition chamber.

Fig. 5—Vertical epitaxial deposition chamber.



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down voltage of a pressure metal-to-semiconductor contact is measured and empirically related to the impurity density (resistivity) of the semiconductor. To reduce heating effects at near breakdown conditions, the duty cycle of the power supply is reduced by pulsing. A schematic diagram of a three-point probe and a chart relating resistivity to reverse breakdown voltage is shown in Fig. 7. The three-point-probe film-measuring method is direct and nondestructive and has a precision of ±15 percent in the 2.0 to 0.2 ohm-centimeter range. The method is limited however in that only top-layer resistivity can be measured. It should also be noted that the resistivity of the top layer is limited by film thickness. The resistivity of films thinner than the depletion width of the space charge at breakdown in the metal-semiconductor diode cannot be accurately determined.

Thickness

The thickness of an epitaxial film can be measured by polishing an edge of the deposit at an angle of 1 to 5 degrees to the film surface; this process is called "angle lapping."[15] Under high illumination and at high magnification, and after suitable chemical treatment, the epitaxial layers are revealed, and regions in the deposit that differ in conductivity type or resistivity can be detected. This method relies on the difference in chemical plating potentials existing in different layers. Although the precision attainable with this type of test is largely dependent on the skill of the operator, regions differing in conductivity level by an order of magnitude and/or changes in conductivity type can usually be measured to a precision of ±15 percent. This method, in addition to being destructive, requires control wafers, and is therefore indirect.

A technique that gives perhaps the most accurate measurement of layer thickness can be used whenever a high resistivity film (resistivity greater than 0.1 ohm-centimeter) exists over a heavily doped degenerate region (resistivity less than 0.02 ohm-centimeter). Inasmuch as lightly doped silicon is transparent to infrared radiation and heavily doped material is reflecting, interference patterns can be obtained by scanning the sample with infrared radiation; this is usually done in the 3- to 30-micron range. The effective difference in the abilities of these two regions to transmit infrared combined with the application of interference techniques, provides sufficient data to permit computation of the high-resistivity-layer thickness.[16-18] Epitaxial layer thickness, T, is determined from

$$T = \left(p - \tfrac{1}{2} + \frac{\phi}{2\pi}\right) \frac{\lambda}{2(n^2 - \sin^2\theta)^{1/2}}$$

where p is the order of reflectance; ϕ is the phase shift at the N/N^+ boundary; and n is the refractive index of silicon.

This precise phase-shift correction due to the partially transmitting and complex behavior of the substrate region as a function of wavelength results in a measurement precision of ±3 percent by this method. This method is used in both the two-layer epitaxial structure and the pocket structure. A schematic diagram illustrating how this measurement is made is shown in Fig. 8.

Crystal Perfection

Perfection of the epitaxial deposit is of prime importance to the successful fabrication of large-area arrays. Small localized disturbances in the epitaxial layer[19] can often result in the complete failure of a large circuit array. These disturbances or imperfections are illustrated in Fig. 9 and described below:

1) *Macroscopic*—Bumps, pyramids, and other protrusions visible to the unaided eye or at low magnifications. This type of disturbance is high enough to damage a contact photoresist mask. Successive use of the same photoresist mask on a number of different wafers each having macroscopic imperfections in different locations of the wafer could damage the mask severely and significantly reduce yield.
2) *Microscopic*—Defects visible under moderate magnification (50 to 500X); usually described as spots.
3) *Atomic*—Defects revealed by x-ray, electron diffraction techniques, or by destructive preferential-etch methods. Diffraction techniques are seldom used because they are too sophisticated and time consuming to be of practical value in process control. Instead, the Sirtl etch[b] is used on either the epitaxial film or the single-crystal substrate to reveal edge dislocations, stacking faults, and other types of atomic imperfections in the crystal. By etching, the dislocation and stacking faults are revealed where they intersect the surface on either the (111) or (100) planes; densities are recorded as intersections per square centimeter. The etch method is destructive; usually 0.5 to 5 microns of the crystal or film surface must be removed to provide good resolution. Besides being useful for examining the substrate and epitaxial film, the etch method can be used for studying the propagation of defects from work damage and/or contamination on the substrate into the epitaxial film.

Elimination of imperfections formed during deposition has proven to be the most difficult task in the growth of epitaxial films. Because nearly all the imperfections originate at the interface between the epitaxial film and the substrate, damage-free atomically-clean substrates are vital to good film growth. To assure substrate cleanliness, final wafer preparation is performed in a laminar-flow dust-free chamber built onto the loading end of the epitaxial chamber. As an additional precaution, the substrates are etched *in situ* in HCl at temperatures ranging from 1200°C to 1250°. The HCl chemically attacks many foreign materials and converts them to volatile chlorides which are vaporized from the substrate; in addition, the HCl etches away shallow damage resulting from handling or polishing. The effect on spots, dislocations

Fig. 6—Production-type epitaxial deposition system.

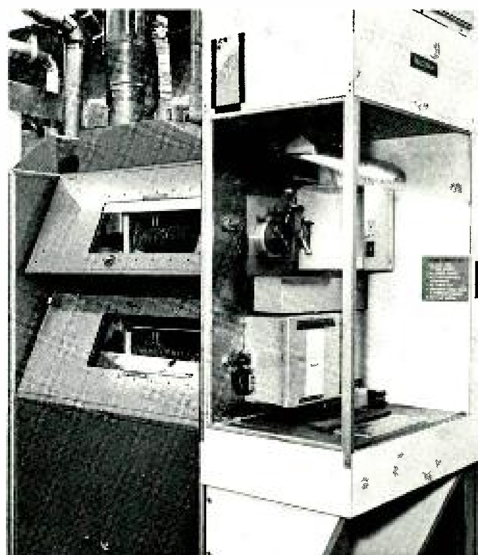
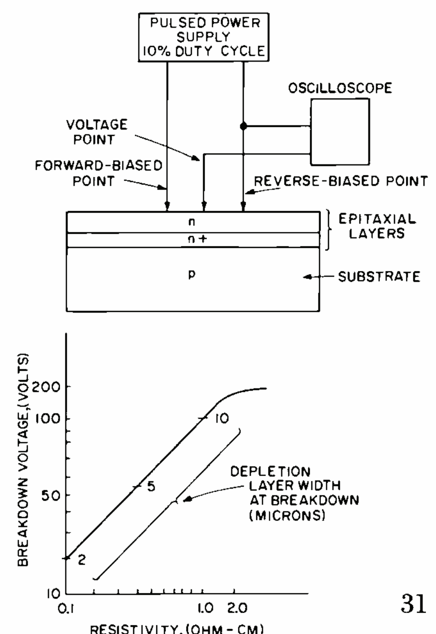


Fig. 7—Diagram of a three-point probe for film resistivity measurement and chart relating resistivity to reverse breakdown voltage.



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and stacking faults are particularly dramatic. Densities are reduced by 2 to 4 orders of magnitude. In addition, the improvement in breakdown voltages of the isolated N regions is markedly improved. In the pocket structure, the depth of removal by the etch must be carefully controlled so that the high surface-conductance layers of the diffused pockets are not etched away, a condition that would raise the sheet resistance of these regions above tolerable levels. When contamination or surface damage calls for deep etching, the depth of pocket diffusions must be increased so that the required amount of surface can be removed. Table II shows the effectiveness of the HCl cleaning treatments.

TABLE II—Effectiveness of High-Temperature Gaseous-HCl Etch Cleaning (Typical Values)

CRYSTAL PERFECTION

Wafer Type	*Edge Dislocation/* cm²	*Stacking Faults/* cm²	*Spots*/cm²	*Bumps*/wafer
(111) Substrate 1.5" diameter	10^3	0	0	0
N layer over ZrO_2 polished substrate; NoHCl	10^4 to 10^5	10^5	—	—
N layer over SiO_2 polished substrate; NoHCl	10^2 to 10^3	10^2 to 10^3	—	—
N layer over 1-micron diamond polished substrate; NoHCl	massive damage	>10^6 parts	—	—
N layer over any of above; finished with HCl etching to remove 5 microns of substrate	10^3	0 to 10^2	0	5
N layer over pocket diffused wafer; ZrO_2 polished substrate; NoHCl	10^3	10^4 to 10^6	10^2 to 10^3	10
N layer over pocket diffused wafer; ZrO_2 polished substrate; HCl etched to remove 0.5 to 1 micron	10^3	10^3	10 to 10^2	5

BREAKDOWN VOLTAGES OF ISOLATED N—REGIONS (AT 10 MICROAMPERES)

Wafer Type	*Median Breakdown Voltage*	*Range*	*Scatter*
Standard N pocket wafer, 1-ohm-cm epitaxial layer; No HCl etching	24 volts	0.6 to 80 volts	poor
Same as above with deeper pocket diffusion and HCl etch	78 volts	74 to 96 volts	excellent

CONCLUSION

Epitaxial film technology has progressed to the point where it is a sophisticated and precise science. It is of significant importance to present day integrated circuit production because of its versatility and will probably receive further attention in such new areas as higher voltage, higher power, and complementary integrated circuits.

ACKNOWLEDGMENT

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Fig. 8—Infrared technique for measuring film thickness.

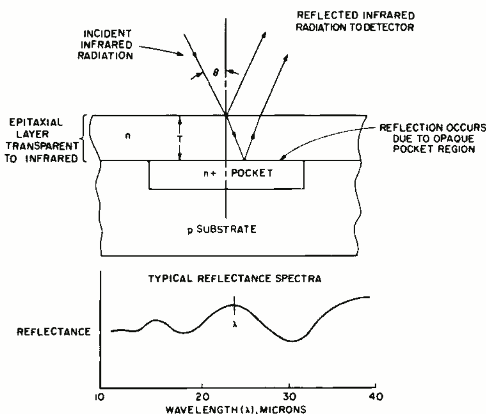
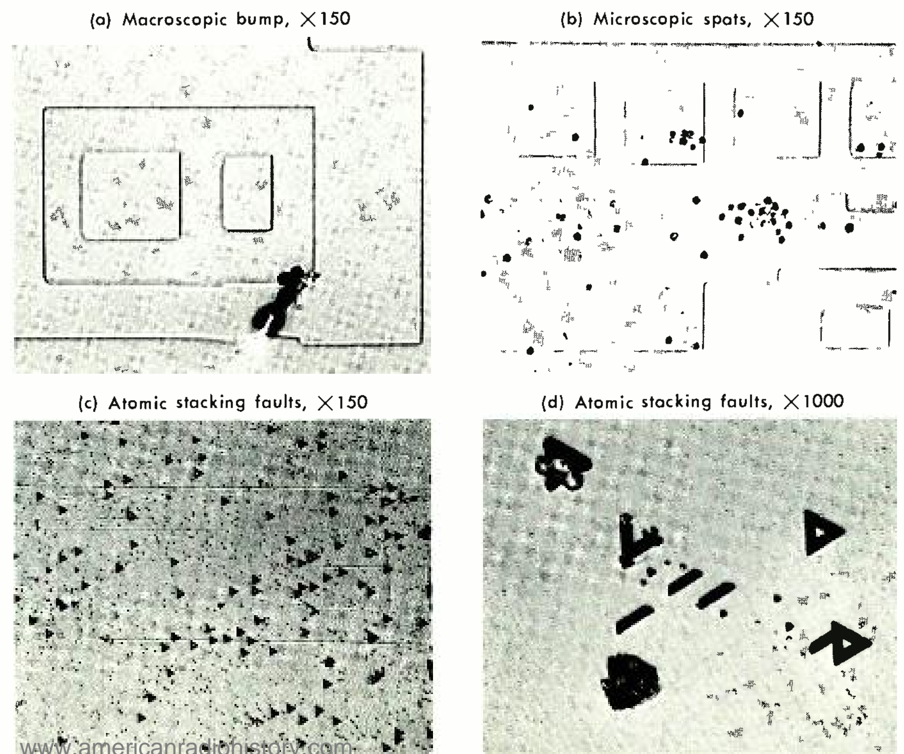


Fig. 9—Imperfections in epitaxial films.



(a) Macroscopic bump, ×150
(b) Microscopic spots, ×150
(c) Atomic stacking faults, ×150
(d) Atomic stacking faults, ×1000

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DIAGNOSTIC TESTING OF INTEGRATED CIRCUITS

The manufacture of integrated circuits is presently a batch-type process, but the more it changes and becomes a flow-type process with automatic feed-back of corrected information, the higher will be the yield and the lower the cost of the final product. Because the processing is extremely complex and the end product is extremely small, it is difficult to make the electrical measurements required at all stages of processing. However, at the completed wafer stage the product can be tested electrically and its characteristics determined. At this point the product consists of a silicon wafer 1.5 inches in diameter with 500 to 1000 integrated circuits formed within it and suitable metallizing on its surface to allow it to be connected to external contacts. The cost per circuit at this stage is not too high and, if the yield is reasonable, it is economically advantageous to test each chip and to eliminate bad circuits, thus saving the subsequent processing and packaging costs. For low-yield wafers, it becomes essential to collect data on failing units. This article explains how data is collected and formulated.

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Test Engineering and Reliability

Electronic Components and Devices, Somerville, N. J.

In the circuit-probe testing technique, the completed IC wafer is connected to an automatic test set by probes which make contact with the metallized regions of the wafer. The probing machine is designed so that the wafer is indexed automatically, with the probes contacting the chips sequentially. Once the wafer is set up, it can be completely tested automatically.

The test set used at this stage must be an automatic DC test set with the requisite pin capacity, power supply ranges, and comparator capability. Because speed of testing is very important, the test set should be capable of being multiplexed to two or more probing machines so that it can be used to its maximum capacity. Testing speed is restricted somewhat by current methods of data acquisition. Typical test rates for present-day automatic GO/NO-GO testing are 60 to 100 tests/second with the ultimate being about 200 tests/second. These figures will remain firm at least as long as reed relays are used for making connections. Data logging considerably reduces the testing rate, the degree of reduction depending on the type of data logging used. A typical rate for punched card data logging is two tests/second; for typed-out data the rate is similar. The fastest form of data logging presently available with standard IC test sets is magnetic tape. The best rate achievable by this method is about 10 tests/second, because of the time required by a digital voltmeter to digitize the data. (Integrating digital voltmeters normally take 20 to 50 milliseconds to integrate and digitize one parameter of four digits.)

Final manuscript received August 8, 1967.

All data provided by current data logging methods requires further analysis. A wafer containing 800 pellets might produce 30,000 parameter readings, all of which must be condensed into a comprehensible summary if the wafer is to be characterized. The data would probably be analyzed on a remote computer, causing some additional delay between the acquisition of the data and the presentation of the final results.

A computer analysis normally provides statistical information on all parameters and yield information by wafer and parameter; it does not necessarily provide the type of information required by the process engineer nor does it necessarily pinpoint the causes of low yield on a wafer. To perform these latter tasks it is necessary that the test set be controlled by a computer and that the data produced by the test set be analyzed by the computer immediately after it is taken (in real time). A computer-controlled test set with these capabilities is now in operation. This article extends the use of that computer-controlled test set into the diagnosis of failure modes in integrated circuits for the purpose of process control.

DIAGNOSTIC TESTING

The diagnosis of faults in an integrated circuit may proceed by several paths:

1) Perform as many tests as can be devised, and by a process of logical deduction from the results, determine the failure mode. This is the method normally used in analysing data from a series of sequential tests.
2) Perform complex tests which initially include many variables and gradually narrow the area down until the fault is determined. This procedure can lead to erroneous conclusions when several interacting faults occur in the same circuit.
3) Perform simple two-terminal tests first and gradually build up a case history of the circuit being analysed. This procedure has been found to be most appropriate in analysing the circuits presently being manufactured.

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TABLE I — Diagnostic Statements

	ARITHMETIC
Addition:	TA = TB + TC
Subtraction:	TA = TB − TC
Multiplication:	TA = TB * TC
Division:	TA = TB/TC
Absolute Value:	TA = | TB + TC − TD * TE |

LIMIT

LIMI = 2.76E+1, T2, HR4, T1

DYNAMIC POWER SUPPLY

T10 $ T10 = +1.0 (A constant is put in the memory location corresponding to T10.)

T11 $ PS4 = T10 (Test 11 is performed with PS4 programmed to the value in T10.)

T12 $ T10 = T10+1 (A constant in T10 is incremented by 1. If the program is now directed back to T11, that test will be repeated with the incremented value of PS4 voltage.

REQUIREMENTS OF A DIAGNOSTIC TESTING SYSTEM

The following components must be present in a diagnostic testing system for integrated circuits:

1) A computer-controlled test system such as that currently in use at RCA:[1] The system consists of a DC Test Set with five power supplies and current and voltage measurement instrumentation capable of testing units with up to 40 terminals. The Test Set is digitally programmed from a Spectra 70/15 processor through a specially designed 320-bit register known as a Special Equipment Controller. Tests are run under computer control; digitized data is collected from the Test Set by the processor which performs limit comparisons and some statistical analysis.

2) Computer Programs: These include an Executive Program for INPUT/OUTPUT control, a Diagnostic Program Generator for transforming the Diagnostic Program Language into machine language, and a Diagnostic Program Controller for setting up the tests and performing the arithmetic and logic.

3) A Diagnostic Test Program: This is a program specifically designed for each circuit to be analysed. It is written by a circuit engineer in the Diagnostic Program Language; its capabilities are discussed in the next section.

DIAGNOSTIC TEST PROGRAM

The Integrated Circuit Diagnostic Test Program is designed to be used with a properly formulated series of diagnostic tests to provide information about the faults in a device in the form of simple messages. The program has the capability:

1) To set up any test condition within the range of the test equipment;

2) To compare measured parameters to specified limits and to branch in one of several directions as a result of the comparison;

3) To perform arithmetical operations on measured values and to compare the results to limits;

4) To set a power-supply value to the result of an arithmetical operation;

5) To adjust the range of current and voltage measuring instrumentation as required; and

6) To use the above capabilities to perform searches to locate a particular point on a characteristic.

The diagnostic program consists of a series of *tests* defined by *T* numbers. The tests may be parameter tests to be performed on the circuit under test, arithmetical operations, or combinations of both. The final result of each test is stored in a table in the processor memory so that it will be available later in the program.

The statements used in the diagnostic program for setting up the test conditions are almost identical with those used in the RCA Computer Controlled Test System.[1] One notable difference is the ability of the Diagnostic Test Program to set a power supply to the result of a previous measurement or calculation. This capability allows the test engineers to increment a power supply in specified steps and thus to plot a characteristic curve or search for a point on a characteristic curve.

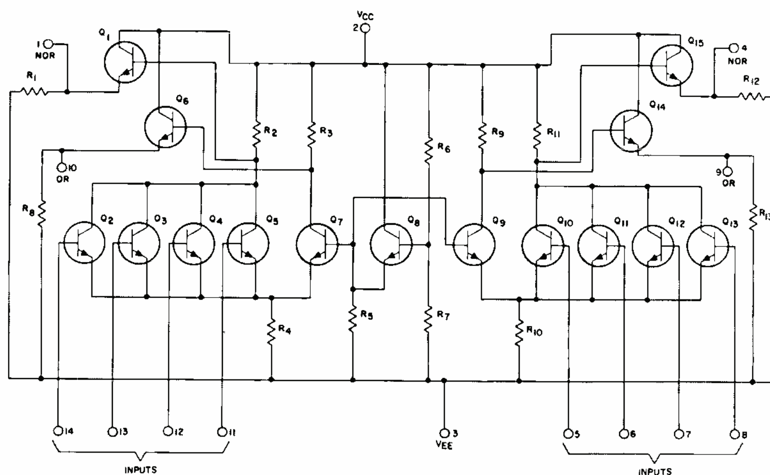
The arithmetical and limit statements are shown in Table I. The result of the calculations performed on the right-hand side of the arithmetical statement is stored in the space in memory allocated to the *T* number indicated on the left-hand side.

The explanation of the LIMIT statement is as follows:

	Value	*Action*	*Message*	*DVM Readings*
LIMI =	d.dddE+n,	HALT, *Tn*	LOWR4,	TB, TC

Value:	This may vary from 10^{-9} to 10^{+9}.
Action:	This specifies the action to be taken if the value being compared is less than or equal to the limit value. Two actions are possible, HALT or go to another specified test which need not be the next sequential test. If the value being compared is greater than the limit, the program proceeds to the next statement whether it be the next limit, an arithmetical operation, or the next test.
Message:	This may be any desired message up to 15 characters. The message indicates the cause of failure based on the previous logical sequence of tests culminating in this particular limit comparison.
DVM Readings:	Optionally specified parameter readings may be typed out as part of the message by inserting test numbers in this part of the limit statement. These parameter values may be useful in interpreting the messages.

Fig. 1—Schematic of a dual 4-input ECCSL gate.



DESIGN OF A DIAGNOSTIC TEST PROGRAM

Fig. 1 shows the dual 4-input ECCSL gate used in preparing the sample diagnostic program described below. Upon assuming control the program first measures resistors *R*1, *R*8, *R*12, and *R*13 and compares the measurements to limits. The values of resistors *R*2, *R*4, *R*10 and *R*11 are then determined by calculating the slopes of the input characteristics to terminals 2 and 3. These initial tests also determine open circuit terminals and shorted inputs or outputs. The resistor values are stored and may be used to determine resistor ratios. The ratio of *R*2 to *R*4 is important because it determines the zero levels on the NOR side of the gate. Power is then applied to terminals 2 and 3. This is done gradually

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in 1-volt steps as the rate of rise of current with voltage is checked to determine if the rate is normal. Rapid current rise may indicate a short circuit between the isolated N regions and the substrate, a condition under which the program may be halted.

After the program has determined that it is safe to apply power to the circuit, such parameters as input leakage, input current, input saturation voltage, output levels, and output impedance are measured. Output levels are temperature sensitive; therefore, to obtain precise values, the unit is heated in the test socket and the variation of output level with time is measured. If the difference between successive readings is within a prescribed range, the unit is thermally stable and testing can proceed.

The crossover voltage of the output characteristic is shown in Fig. 2. This circuit parameter is important because it closely approximates the reference voltage which appears at the emitter of Q8, but which cannot be measured on a finished unit. The crossover voltage may be determined by a search technique such as that shown in the flow chart (Fig. 3). The input voltage is increased or decreased until the difference between the output voltages is less than about 50 millivolts. The input voltage for this condition is the crossover voltage. The gain of the differential amplifier at the crossover point may be measured by changing V_{IN} and measuring the slope of the transfer characteristic.

A total of 80 tests were devised for this circuit. A single average diagnostic test requires 50 to 60 bytes of memory in addition to the requirements of the Diagnostic Test Program Controller. The messages produced by the test program are limited to a maximum of 15 characters and do not always tell the exact reason for failure. For example, if a constant negative current of 16 milliamperes is applied between terminals 1 and 2 the voltage at terminal 1 should be −0.8 volt. If it is more negative than about −0.85 volt the reason may be:

1) Low current gain of Q1,
2) Saturation of Q1 due to resistance in collector contact,
3) High value of R2, which can be checked, or
4) High emitter contact resistance.

The printed message might be simply LNOR11 (low "1" level at NOR output, terminal 1). This message can be expanded by referring to a table or legend —a normal part of the diagnostic program which usually helps the production engineer to interpret the abbreviated output messages in physical terms. The legend contains information similar to that shown in the numbered statements above. Table II shows the typical output of a diagnostic test program.

USE OF DIAGNOSTIC TEST PROGRAMS

Several Diagnostic Test Programs have been written and are in use at Somerville, N. J. Their usefulness is limited only by the skill of the designer of the program, the computer memory capacity, and the availability of test points within the circuit. Once the program and its associated legend has been written, it is always immediately available. Thus, a time-consuming task (and one very much dependent on the ability of the engineer doing the analysis to remember his previous methods of analysis and his findings) is eliminated.

In future computer-controlled test systems used in production activities, the diagnostic programs might be called in automatically as soon as a low-yield wafer was detected. The program tests would be run on a representative sample of the pellets and an immediate analysis of failure modes would be available for rapid feedback to the processing stages.

REFERENCE

1. Walmsley, B. J., *et al*, "The RCA Computer-Controlled Integrated-Circuit Test System," RCA reprint no. 361.

TABLE II — Typical Output of Diagnostic Program.

Actual Output	*Interpretation*
DG5147003 LOT ID006 TO33 P11OC	Unit No. 6 Terminal 11: open circuit
TO43 HR4 TO43 1.0200E-1	High R4: 1.02 kilohms
TO45 HALT READY!	
DG5147003 LOT ID007	Unit No. 7
TO05 LR12 TO05 .0254	Low R12: 254 ohms
TO13 HRATR1:R12 TO13 2.003OE+O	High ratio R1 to R12 :2.003
TO45 HALT READY!	
DG5147003 LOT ID008	Unit 8
TO15 HRATR1:R6R7 TO15 2.423OE-1	High Ratio R1 to R6+R7:0.2423
TO21 LBQ10 TO21. 1568E+O	Low Beta Q10: I_B=156.μA
TO40 LBQ2 TO40 .1918E+O	Low Beta Q10:' I_B=191.8μA
TO45 HALT READY!	

Fig. 2—ECCSL gate output characteristic.

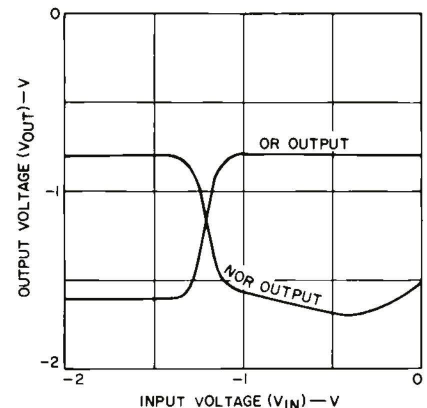
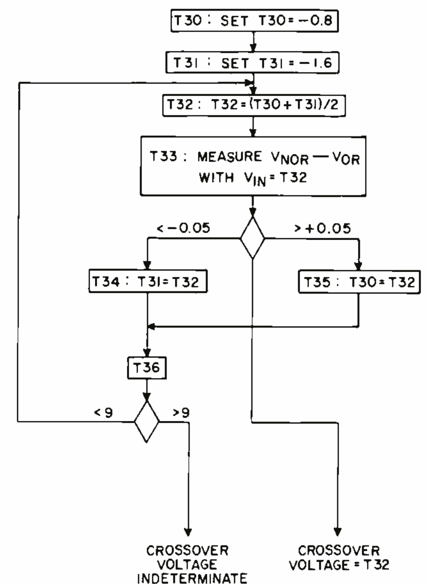


Fig. 3—Flow chart showing method of crossover voltage determination.



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FABRICATION OF COMPLEMENTARY MOS CIRCUITS

Complementary MOS integrated circuits are well suited to large-scale integration because of their minimal area requirements and their low power dissipation and high yield. This article describes the sequence of processing steps required to produce a complementary MOS integrated circuit.

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THE first step in the fabrication process is shown in Fig. 1(a). In this step a low concentration "well" is diffused into the homogeneous N-type silicon which is typically material with a resistivity of 1 to 2 ohm-centimeter. Next, the high concentration P regions which form the source and drain of the P-channel devices are diffused as shown in Fig. 1(b). In a similar manner, high-concentration N-regions are diffused within the P well to form the source and drain for the N-channel devices as shown in Fig. 1(c). The separation between these diffused regions determines the channel length and directly affects device characteristics.

Up to this point, the fabrication of complementary MOS devices is very similar to the fabrication of conventional bipolar planar devices (i.e., processing steps for both types of device include silicon-dioxide growth, photoresist application, oxide etch, high-temperature deposition and diffusion of impurities, and masking operations). At this point, however, MOS fabrication takes a different turn, mainly because in MOS construction the purity of the silicon dioxide directly over the channel and beneath the metal gate is far more critical than in bipolar devices. Any mobile charges in this oxide due to sodium or calcium impurities move under the influence of the high field between the gate and substrate and can induce uncontrolled leakage currents between the source and drain. These leakage currents were a major obstacle in the development of early MOS enhancement devices.

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To ensure that a pure channel oxide will exist in the critical region, the existing oxide is etched back to the surface in the source-channel-drain area as shown in Fig. 1(d). The wafer is then thoroughly cleaned, and a thermal oxide grown in a specially prepared and maintained "clean" furnace. A small amount of phosphorous-doped oxide is usually added as a "getter" during this process to immobilize any stray ions that may intrude on the surface. This step is illustrated in Fig. 1(e).

Precautions are also taken during the metal evaporation phase to ensure that no contaminants reach the surface of the channel oxide beneath the gate metallization. These special precautions require the use of ultra-pure aluminum wire, and a scrupulously clean vacuum chamber. The contact opening and metal etch steps are shown in Fig. 1(f).

A technique that has proved of great value in the development of the clean-oxide clean-metal process is the capacitance-voltage measurement technique. Briefly, this technique involves the measurement of the capacitance due to the oxide dielectric in series with the capacitance of the surface space-charge layer. The induced junction voltage is ideally due to the field between the metallized electrode (or channel if this were a gate) and the substrate. However, as explained previously, mobile charges (in impure oxide) can induce an inversion layer, thus changing the bias voltage at which the series capacitance appears. Fig. 2 shows capacitance-voltage curves for clean and impure oxides after one minute at 300°C with 10-volts positive bias.

Fig. 1(g) demonstrates the use of guard bands in the fabrication of complementary MOS devices. These bands are heavily doped N+ or P+ regions at the borders of the N substrate and P well, respectively. Since the ability to invert a surface (cause conduction between oppositely doped regions) is inversely proportional to the concentration, the heavily-doped guard bands effectively restrict leakage currents.

Fig. 3 shows a protective diode located at each gate input and spaced as far as possible from the bond pad. The diode, a P+ diffusion in the N substrate, prevents breakdown of the gate-channel oxide by such electrical phenomena as transients and static charge. Because the substrate of the MOS is normally connected to $+V_{DD}$, the diode is back biased for normal signals; its only effect on circuit characteristics is a small increase in input capacitance: about 0.5 picofarad. Should the input exceed $+V_{DD} = +0.7$ volts, the diode conducts, diverting the charge away from the gate oxide. The diode also protects the gate (which can normally sustain 70 volts) from negative transients; the diode is designed so that a negative transient greater than −30 volts will cause it to break down.

No extra processing steps are required for the fabrication of the protective diodes and the guard bands because they are diffused simultaneously with the sources and drains.

LAYOUT OF COMPLEMENTARY MOS CIRCUITS

Translating a complementary MOS circuit into a mask layout is a fairly straight-forward task, and most design engineers find little difficulty in following the rules and restrictions dictated by the process technology. These design rules are explained in the following paragraphs; however, it is recommended that any proposed design be discussed with the MOS Integrated Circuit Group at Somerville before a layout is begun.

A. H. MEDWIN received the BSEE from the College of the City of New York in 1949. After graduation, he designed oscilloscopes, vacuum-tube voltmeters, and signal generators. In 1957, he entered the computer field, working at the Monrobot Division of Litton Industries as Project Engineer. In June 1959, Mr. Medwin joined the Micromodules Department of the RCA Semiconductor and Materials Division as a Senior Engineer. In this capacity he was responsible for the design of Micropac digital computer micromodules and the development of microcircuit techniques for ultra-high-speed computers. This work included tunnel-diode memory arrays and nanosecond switching circuits. In 1962, Mr. Medwin developed RCA's Digital Microcircuit line, making substantial contributions to the hybrid-chip technology and thin-film resistive components used in this program. Further responsibilities included new developments in isolation processes, thin-film components, and advanced amplifier techniques for bipolar and MOS integrated circuits. Later, as Project Manager for the bipolar portion of the Wright Field Large Array Pogram, he directed efforts in 100% yield techniques and multilevel metallization. In December 1966, Mr. Medwin was appointed Manager of MOS Integrated Circuit Technology, with responsibility for the development and production of complementary MOS circuits and arrays. He holds two patents and is the author of a number of technical papers. Mr. Medwin is a member of Eta Kappa Nu, IEEE, and the American Vacuum Society.

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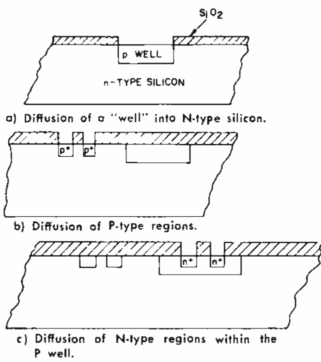

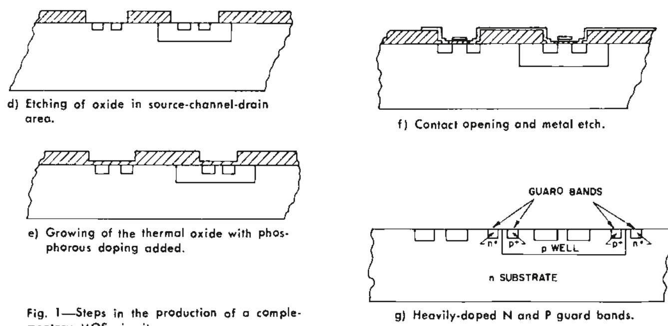

Fig. 1—Steps in the production of a complementary MOS circuit.

The first consideration is the expected size of the various MOS devices in the circuit. The sizes are determined by load and speed requirements and are usually firm by the time the breadboard phase of the circuit design is complete. Fig. 4 shows the relationship of MOS channel width to transconductance g_m for P- and N-type devices. (N-type devices always have higher values of g_m than P-type devices because electron mobility is higher than hole mobility.) The curves of Figs. 4 and 5, which show the relationships of g_m to speed, establish the required channel width. The channel length is, in all cases, 0.3 mil.

Fortunately for the designer, all MOS devices are electrically isolated from each other by the normally reverse-biased N substrate ($+V_{DD}$) and the P-well ground. Therefore, if feasible, all N-type devices should be placed in a single-well area because the side diffusion allowances for the well and its guard bands require a considerable lineal spacing; any additional wells would only increase the total area with no functional benefit.

Crossovers can conveniently be made on the MOS structure merely by extending one of the heavily-doped source or drain regions. Because these are covered by an insulating oxide, a metal interconnect can cross directly above. Separate "tunnels" (common in bipolar integrated circuits) are seldom required. Sheet resistivities of N+ diffusions are three ohms/square; of P+ diffusions, 50 ohms/square.

The total active area of an MOS device comprises the channel plus the leading edge of the source and drain. The remaining area of each source or drain is determined by the contact opening and allowances for metal overlap and metal separation; Table I lists important dimensions; Fig. 6 illustrates these.

TABLE I—Important MOS Device Dimensions

Characteristic	*Dimension*
Channel length	0.3 mil
Channel width	As required (1.5 mil minimum)
Gate metallization	0.5 mil (0.1-mil overlap each side)
Contact opening	0.3 by 0.5 mils (The minimum dimension from the edge of diffusion is 0.3 mil.)
Contact metallization	0.5 mil (0.1-mil overlap each side)
Interconnect metallization	0.3 mil
Separation between metal conductors	0.3 mil
Guard bands (n+ or p+)	0.5-mil minimum (Expansion to fill non-active area preferred.)
Bond pads	4 by 4 mils (The minimum distance from metal, diffused area, or dicing line is 2 mils. Center-to-center bond-pad spacing is 8 mils.)
Dicing allowance	4 mils

The determination of a source width is made by summing the contact opening (0.3 mil); the metal overlap on each side of the contact (0.1 mil plus 0.1 mil); the overlap of the gate metallization, one side (0.1 mil); the separation between metal strips (0.3 mil); and an allowance for space between the contact opening and the edge of the diffusion (0.3 mil minus the 0.1 mil already allowed for metal overlap). This totals 1.1 mils.

LARGE-ARRAY INTEGRATION

Because of their small size, low power dissipation, and high yield, MOS devices are well suited to large-array integration. For example, the TA5342 seven-stage counter incorporates 114 devices on a 0.085-x0.075-inch pellet (Fig. 7). This sharply reduced area required per unit cell is also shown in Fig. 8. The improved efficiency of the large array is due to two factors:

1) The peripheral requirements (for bond pads, dicing allowance, etc.) are relatively constant regardless of the number of devices; and
2) The function and load of each of the individual devices within the array is fixed; therefore, the geometry of each device can be tailored for minimum size and capacitance.

Arrays of more than a 1000 MOS devices are foreseeable in the very near future.

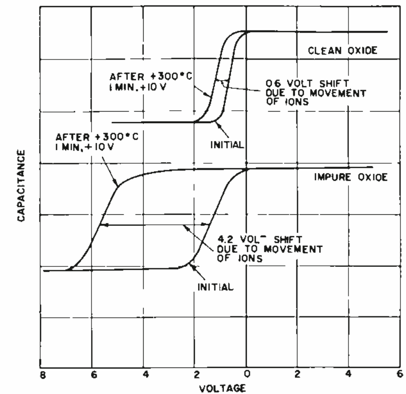

Fig. 2—Capacitance-voltage curves for clean and impure oxides.

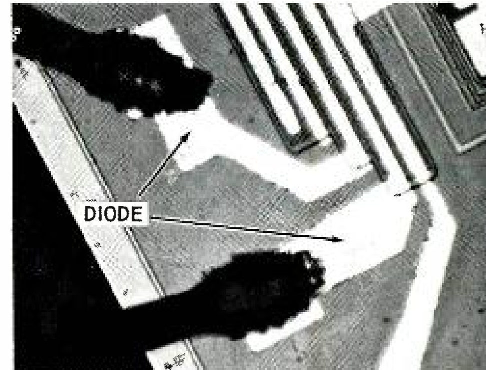

Fig. 3—Protective diode at each gate input.

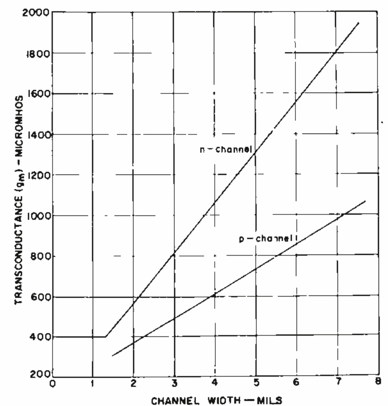

Fig. 4—Relationship of channel width to transconductance for P- and N-type MOS devices

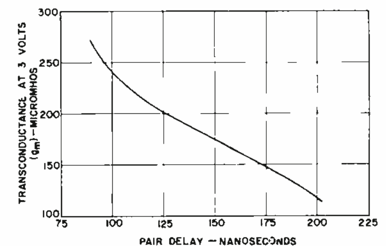

Fig. 5—Relationship of transconductance and speed in MOS devices.

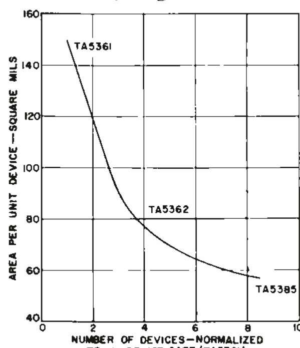

Fig. 8—Graph showing trend toward less area per unit cell.

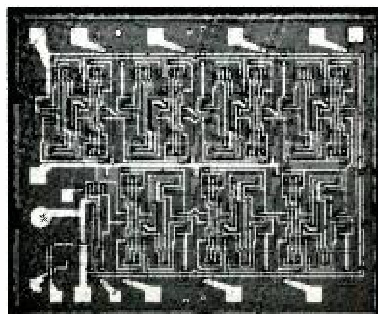

Fig. 7—A seven-stage counter (RCA Dev. Type TA5342).

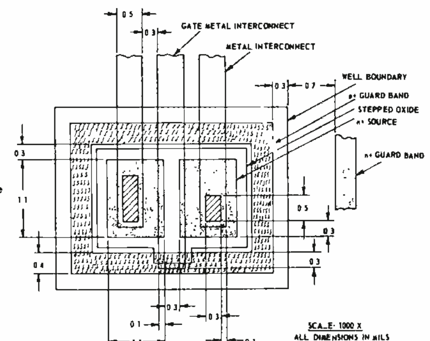

Fig. 6—Illustration of complementary MOS design rules.

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A LARGE-SCALE INTEGRATED SCRATCH-PAD MEMORY

Production versions of a 16-bit scratch-pad memory circuit, which were produced using large scale integrated techniques, are currently being evaluated at Somerville, N.J., and successful initial results have been obtained. This paper describes the organization of this random-access x- and y-select memory and briefly describes the circuit operation.

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A 16-bit random-access x- and y-select memory has been designed for fabrication on a single/semiconductor pellet through the use of integrated—circuit processes. The memory consists of sixteen nonsaturating flip-flops with x- and y-select drivers, and is capable of nondestructive readout. The read and write times are of the order of 10 nanoseconds; power dissipation is 15-milliwatts/bit. The scratch-pad memory is compatible with RCA ECCSL circuits and includes a "phantom OR" output capability.

MEMORY ORGANIZATION

Fig. 1 shows the random-access scratch-pad memory organization, a number of memory cells (or flip-flops) arranged in an x-y matrix. The matrix is flexible in that rows or columns may be added; each row and column is driven by an internal driver. Readout is accomplished through sense-"0" and sense-"1" lines which couple each cell in the array with sense amplifiers and output gates. Only one cell is readout at a time by applying a high ("1") level input voltage to desired x- and y-select inputs while maintaining the remaining inputs at the low ("0") level; readout is nondestructive. The sense-"0" and sense-"1" lines are also used to write information into a selected cell. For this reason, the sense lines are also connected to the write drivers.

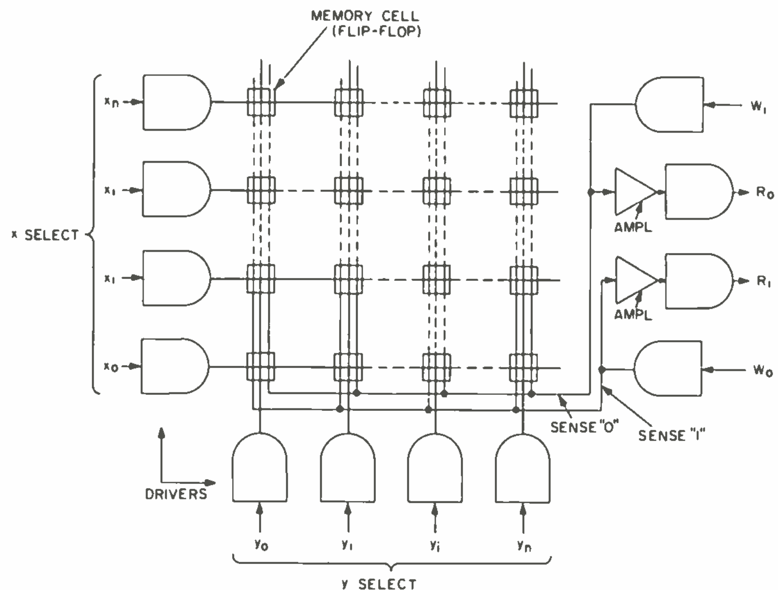

Fig. 1—Scratch-pad memory organization.

MEMORY CELL AND DRIVERS

Memory Circuit Description

Fig. 2 shows a basic memory cell with x- and y-select drivers. The cell circuit is a flip-flop consisting of two transistors, Q1 and Q2; two collector resistors, R2 and R3; and a bias resistor. R1. Transistors Q1 and Q2 have three emitters each for selection purposes.

The two transistors, Q1 and Q2, with their respective collector resistors, R2

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BORYS ZUK received the BSEE from the University of Pennsylvania in 1957. His post-graduate education in the digital computer field is extensive and includes programming, switching circuits, logic, and computer engineering. In 1957, Mr. Zuk joined the RCA Semiconductor Division in Somerville, N.J., as an applications engineer. His duties involved design and development of semiconductor computer devices and the application of these devices to switching circuits. In 1963, Mr. Zuk moved into the RCA Integrated Circuit Activity, where he designed computer circuits specifically for the integrated circuit process. Presently he is working on Large Scale Integrations (complex arrays on a single semiconductor chip) which are used to perform specific logic functions. Mr. Zuk is the author of four technical papers. He has been granted three patents and has several others pending.

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and R3, are cross-coupled to form the flip-flop. In this arrangement, only one side of the flip-flop (or one transistor) conducts at any given time. To insure that the conducting transistor is not in a saturated state, a common resistor, R1, provides negative feedback and limits conduction.

Both x- and y-select drivers are emitter-follower types; each consists of one transistor, one base resistor to prevent oscillations, and one emitter resistor. In the 16-bit memory array, each x- and y-select driver drives four memory cells.

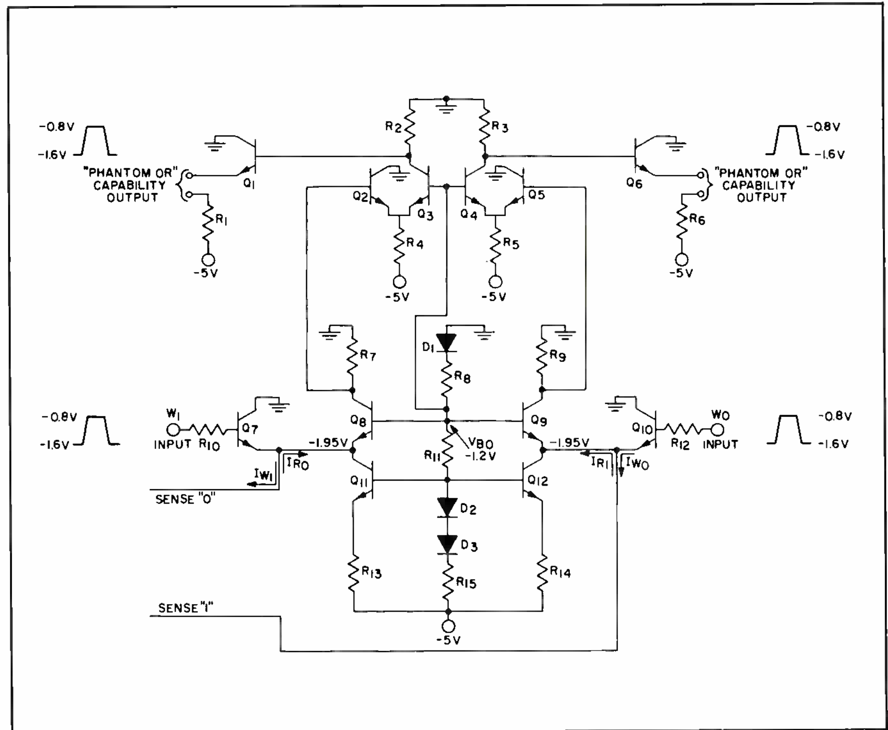

Fig. 3—A sense amplifier and its associated readout gates and write controls.

Biasing

Normally, if there is no selection, the input to the x and y drivers is low level, −1.6 volts, and the output from the drivers is $-1.6\text{-}V_{BE}$ or −2.35 volts: the sense lines are biased at approximately −1.95 volts. Because the output voltage of the drivers is lower than the sense-line voltage, the cells are provided with current by the drivers. At the same time, there is no appreciable current in the sense lines.

To better understand cell biasing, assume that Q1 is conducting and Q2 is nonconducting (Fig. 2). When Q1 conducts, current flows through its collector, R2, and R1 to ground. This current flow induces a voltage across R1 which, through R3, acts as a negative feedback to limit the amount of current through Q1. This limitation restricts the voltage drop across R2 to only 0.4 volt, which, in turn, results in a net forward bias of 0.35 volt on Q2, a voltage not sufficient to turn Q2 on. The opposite state of flip-flop conduction is similar—the cell is bi-stable. The 0.4-volt drop across the collector resistor is not sufficient to forward bias the collector-to-base junction. Therefore, the conducting transistor is in a nonsaturated state, permitting high-frequency operation.

Cell Readout

If the selected x- and y-driver inputs are switched to the high ("1") level, −0.8 volt, the output of the emitter-follower drivers will also switch, from −2.35 volts to −1.55 volts. However, because the sense lines are biased at −1.95 volts, the selected cell latches onto the sense lines. The nonconducting transistor is still off, but the conducting transistor draws current from the sense line. This sense-line current is detected by the sense amplifier and readout occurs.

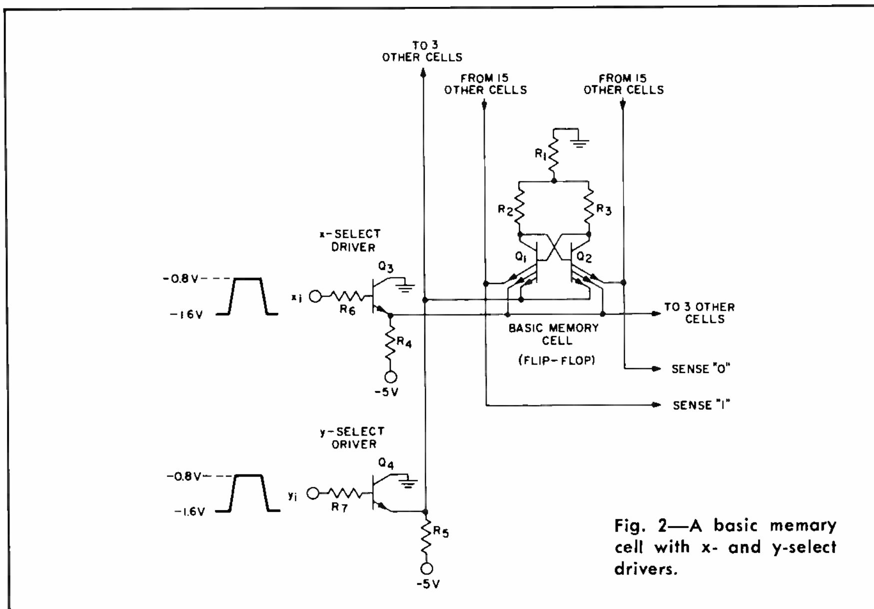

Fig. 2—A basic memory cell with x- and y-select drivers.

THE SENSE AMPLIFIER

Circuit Description

Fig. 3 shows the sense amplifier and its associated readout gates and write controls. The sense amplifier consists of two sections: one for sense-"0" line readout and another for sense-"1" line readout. The section associated with the sense-"0" line consists of amplifying transistor Q8, collector-resistor R7, and a constant-current-source driver, Q11, with its emitter resistor, R13. The section associated with the sense-"1" line consists of Q9, R9, Q12, and R14.

Biasing

Amplifier bias is obtained through three diodes: D1, D2, and D3; and three resistors: R8, R11, and R15. There are two bias points to be considered: the bias for the compensated current sources (at the bases of Q11 and Q12); and the bias for the amplifying sections (at the bases of Q8 and Q9).

Diodes D2 and D3 track current variation with temperature; resistor R15 compensates the current source as the power supply voltage V_{EE} varies. This bias arrangement, combined with Q11 and R13, provides a wholly-compensated current source for the sense-"0" side of the amplifier; Q12 and R14 perform the same function for the sense-"1" side.

The amplifying-section bias point involves diode D1 and resistors R8 and R11. This point is set at $V_{BB} = -1.2$

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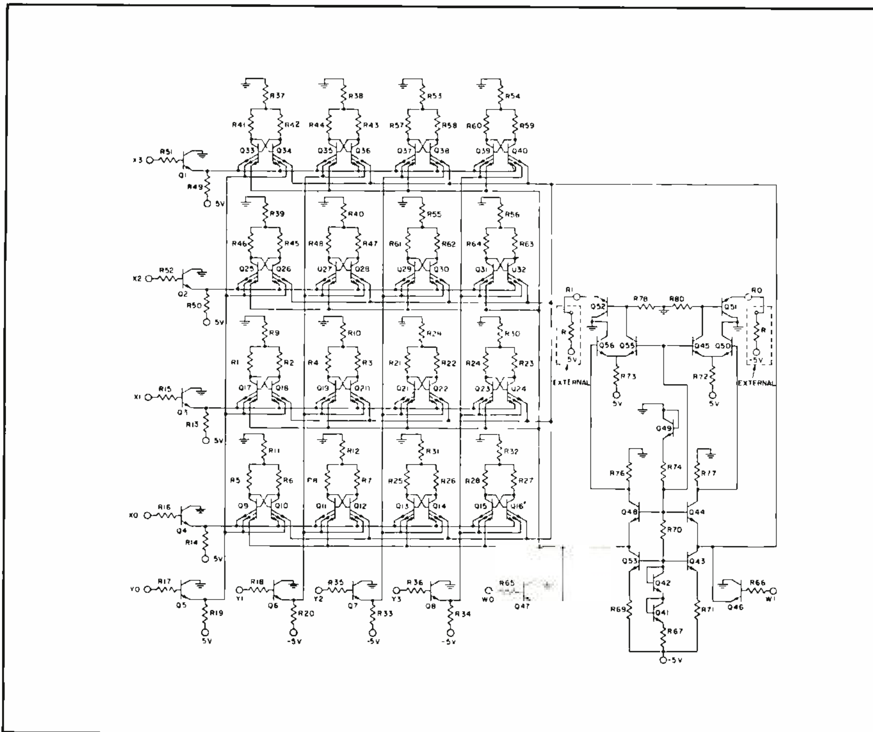

Fig. 4—Scratch-pad memory schematic.

volts at 25°C and V_{EE} = −5 volts so that it will be compatible with the ECL line and provide fifty percent noise immunity for input signals.

Readout

When a cell is selected for readout, either the sense-"0" or sense-"1" line supplies current to the selected cell; that current must come from the sense amplifier. If it is assumed that the sense-"0" line is drawing current, the net current into the emitter of Q8 is reduced. The decrease in current poduces an increase in voltage at the collector of Q8. This voltage increase is amplified and clipped by the gate consisting of Q1, Q2, and Q3, and produces an output voltage change from −.16 volt to −0.8 volt or a standard "1" for ECCSL.

If the sense-"1" line were to draw current, the voltage at the collector of Q9 would increase, producing a "1" output at the emitter of Q6 in a manner similar to that described in the preceding paragraph.

The output resistors in the upper gates in Fig. 3 have been purposely left out to provide "Phantom OR" capabilities. The "Phantom OR" capability permits several scratch-pad memory pellets to be wired in parallel (at the output) to produce a common output.

Writing

Writing of information is accomplished through write drivers consisting of transistor Q7 with base resistor R10 for the sense-"0" line, and Q10 and R12 for the sense-"1" line. Inputs to the write drivers are normally low ("0") level inputs, −1.6 volts. To write a "1" into a cell, the cell is first selected by a means similar to that used in readout. A high-level pulse (−0.8 volt) is then applied to input W1 of Q7 which raises the sense-"0" line voltage to −1.55 volts. However, because the sense-"1" line is at 1.95 volts, the selected cell is forced to assume a "1" state. A "0" is written similarly but requires that the initial high-level pulse be applied to W0 rather than W1.

There are no timing problems; the select input and the writing pulses may appear simultaneously or one may precede the other by any amount of time. Coincidence of the levels, however, determines the state of the cell.

COMPLETED CIRCUIT

Fig. 4 is a complete schematic of the 16-bit scratch-pad memory circuit. The total component count is 196 if the three-emitter transistor is counted as three components. The circuit is designed to dissipate 240 milliwatts or 15 milliwatts/bit.

CIRCUIT TEST RESULTS

A complete model of the 16-bit scratch-pad memory circuit has been built and tested. The test was conducted over the entire military specification temperature range of −55°C to 125°C at a supply voltage of −5V ±20 percent. Successful results were obtained under all temperature and voltage conditions within the ranges specified. At 25°C, the readout time delay and write-pulse width are approximately 10 nanoseconds each with very little variation resulting from small fluctuations in temperature and supply voltage.

INTEGRATION PROGRESS

The scratch-pad memory matrix was fabricated on a 60- by 60-mil silicon chip and included two levels of metalization. Fig. 5 shows the pellet at the completion of first-level metallization; Fig. 6 shows the finished pellet.

Processed units are currently being received for evaluation and are undergoing extensive testing. Initial findings show that integrated units compare favorably with the breadboard model.

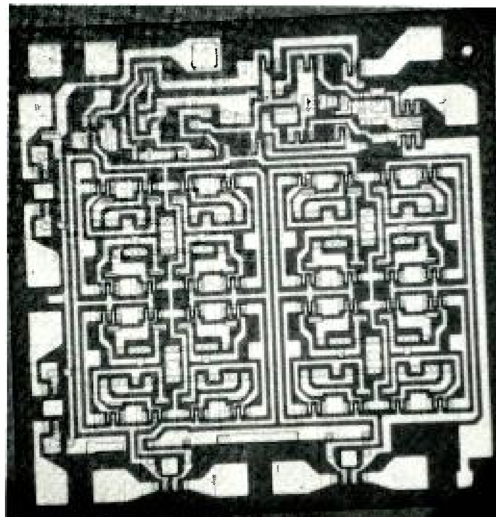

Fig. 5—The scratch-pad memory chip at the completion of first-level metalization.

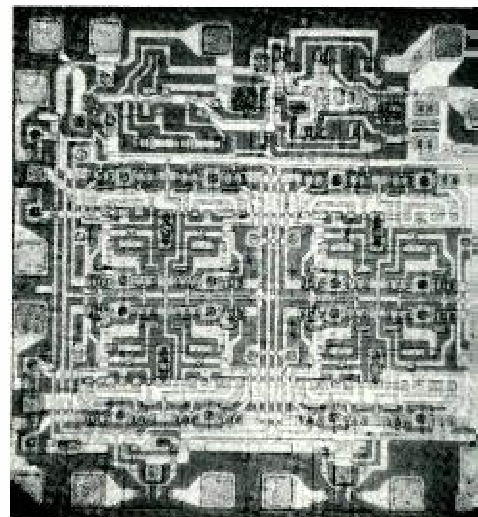

Fig. 6—The finished scratch-pad memory chip.

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INTEGRATED CIRCUITS IN RCA HOME INSTRUMENTS

The use of integrated circuits provides higher performance and reliability in addition to the lower costs resulting from the elimination of many discrete components and their interconnections. This paper describes three new applications of integrated circuits to RCA home instruments, and briefly discusses the operation of each circuit.

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In 1965 RCA successfully pioneered an integrated circuit to perform the intercarrier sound function in TV receivers. Recently three new integrated circuits were introduced into Home Instruments products: an integrated circuit providing automatic fine tuning of TV receivers, a high-gain amplifier integrated circuit used in TV remote control systems, and a low-noise stereo pre-amplifier integrated circuit mounted in the phonograph pick-up head. The four circuits operate in different frequency ranges from DC to 50 MHz and perform diverse functions, demonstrating the wide applicability of integrated circuitry in home instruments. In these applications, the integrated circuits provide higher performance and reliability, and lower costs resulting from the elimination of many discrete components and their interconnections.

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AUTOMATIC FINE TUNING

Precise tuning is important in color television receivers because the presence of the color subcarrier and its sidebands makes the picture quality critically dependent upon accurate tuning of the receiver. Many of the RCA color television receivers in the current line are equipped with the RCA CA3034—an integrated circuit which essentially eliminates the need for manual fine tuning of the receiver.

Fig. 1 is a block diagram of the Automatic Fine Tuning (AFT) system. The frequency of the local oscillator is voltage-controlled. A sample of the picture IF output is applied to the AFT system through a 1.5 pF capacitor located in the plate circuit of the third video IF amplifier (Fig. 2). This incoming picture IF energy is applied to a tuned input circuit consisting of L1301 and C1301. These components act both as an adjacent channel sound trap and an IF frequency peaking circuit—the correct trap frequency is automatically attained when the input tuned circuit is peaked at 46.1 MHz.

The IF beat signal then reaching the IC is still sufficiently large to drive the input amplifier stage on the chip into limiting. The limited IF beat signal is applied to a discriminator where a DC error signal, proportional to the degree of local oscillator mistuning, is developed. The amplified error signal controls the local oscillators of both the VHF and UHF tuners so as to reduce the error resulting from the mistuning of these oscillators.

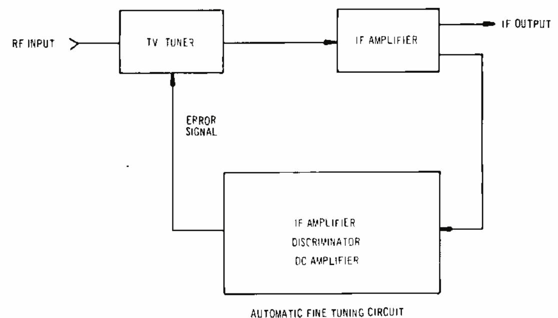

Fig. 1—Automatic fine tuning system.

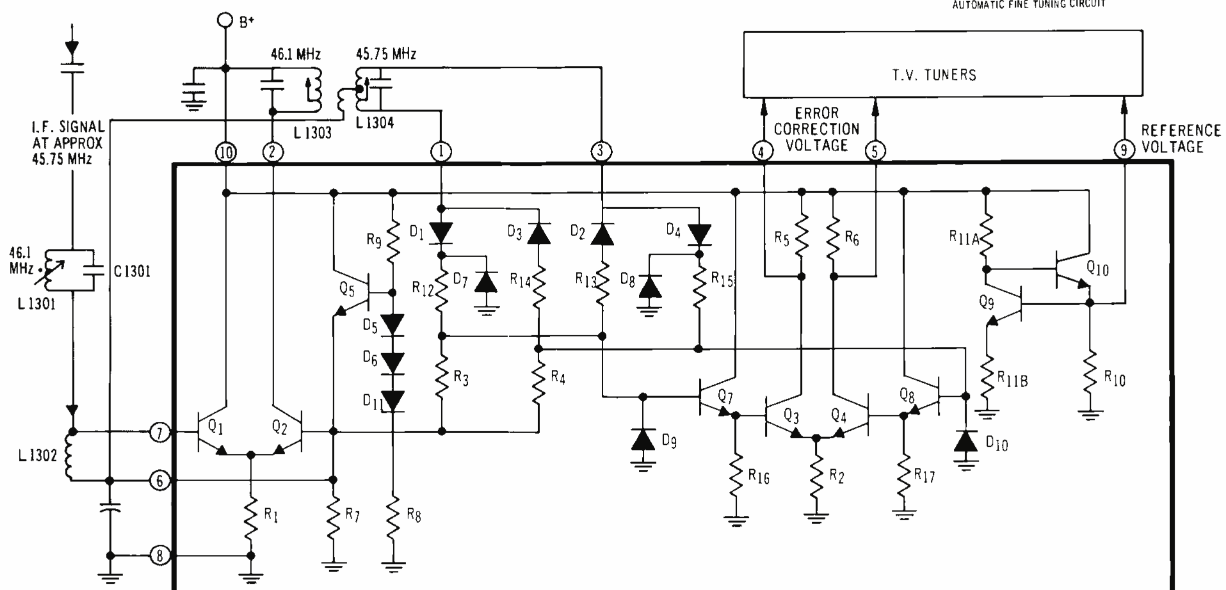

Fig. 2—Automatic fine tuning circuit.

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The high frequency amplifier consists of transistors Q1 and Q2 connected in a differential amplifier configuration. This configuration provides symmetrical limiting and eliminates the need for neutralization. The amplifier load is a phase-shift transformer with the primary tuned to 46.1 MHz for additional high frequency error correction range and the secondary is tuned to 45.75 MHz—the proper picture-carrier IF frequency.

The doubly balanced detectors (diodes D1, D3 and D2, D4) provide symmetrical loading of the discriminator transformer. Diodes D7 and D8 compensate for substrate capacitance, and the reverse-biased diodes D9 and D10 are used for RF filtering.

The DC amplifier is formed by the transistors Q3, Q4, Q7 and Q8 together with the resistors R5 and R6. This stage has a voltage gain of 150, and a large voltage swing at the output terminals (4, 5) is required; therefore the bias stability of this stage is important. In the absence of input signal a temperature-compensated bias network maintains the collector potentials of both output transistors, Q3 and Q4, equal to one-half of the supply voltage. Resistors R5 and R6 are of equal resistance value and large; equal-amplitude, opposite-polarity voltage changes are developed across these resistors if the hetrodyned RF carrier is mistuned creating an IF picture carrier different from 45.75 MHz. The differential DC amplifier allows push-pull or single-ended control of the voltage sensitive elements in the tuner. The temperature-compensating network consists of diodes D5, D6 and D11 combined with resistors R8 and R9. The diodes compensate the V_{be} drops in transistors Q3, Q4, Q5, Q7 and Q8; the voltage drop across the resistor R8 tracks the voltage across R2.

The push-pull control voltages at terminals 4 and 5 are used for VHF, while a single-ended control voltage is used for UHF operation. To defeat the AFT, the two output terminals are shorted to an internal reference voltage provided by the feedback amplifier Q9, Q10. Terminal 9 is the low-impedance output of this amplifier which provides a reference voltage equal to approximately one-half the supply voltage as determined by the ratio of R11A and R11B.

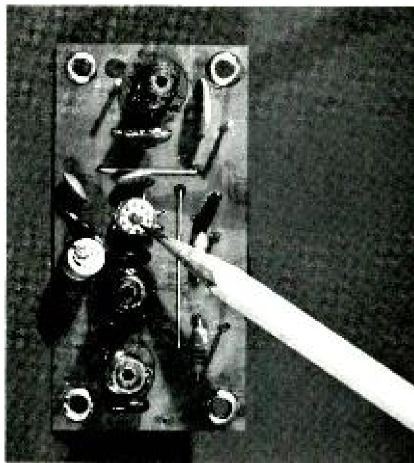


Fig. 3—Chassis layout of the automatic fine tuning.

The RCA CA3034 eliminates approximately 20 discrete components. The circuit exhibits excellent performance: a 1-MHz detuning of the local oscillator is reduced to less than 20 kHz. A photograph of the printed board (Fig. 3) shows the application in a color TV chassis.

REMOTE CONTROL RECEIVERS

A remote control system for TV receivers is shown in Fig. 4. An acoustic signal generated by a small, portable transmitter is detected in the receiver by a condenser microphone. After amplification and filtering, the rectified DC component activates a relay corresponding to the selected function. The signal stength will vary, depending on the position of the transmitter with respect to the receiver; therefore the receiver must be operational over an input signal range of from a few μV to 1 volt.

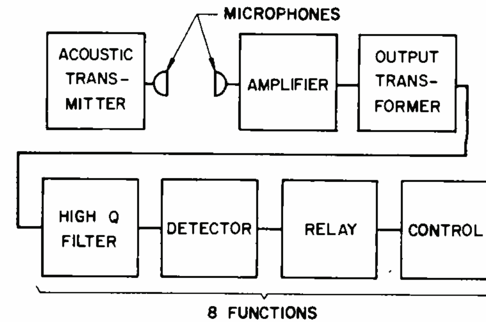


Fig. 4—Remote control system for TV receivers.

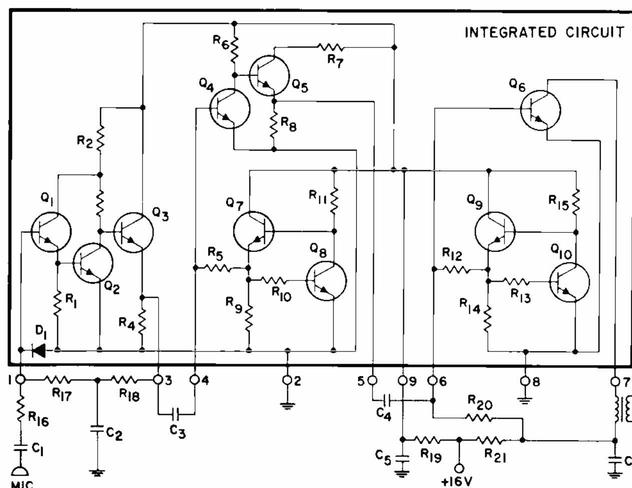
Fig. 5 is the schematic of the RCA CA3035, the IC developed for this application. It operates over a 34 to 45 kHz frequency range, amplifying the signal derived from a condenser microphone by 120 dB.

The three individual stages are coupled by means of off-the-chip capacitors, and the output is developed across a tuned transformer. Each stage provides approximately 40 dB of amplification. The first stage is a low noise amplifier with a feedback network for DC stabilization. The feedback network also establishes the high-pass characteristic of this stage. The noise figure of the amplifier is dependent upon that of the first two transistors, so they are made with a special geometry. The second stage consists of a grounded-emitter amplifier followed by an emitter follower. An internal reference supply provides the bias voltage for this stage. The last stage, also biased by an internal bias supply, consists of a grounded-emitter transistor terminated in a tuned transformer. The output stage is designed to produce pulses of constant amplitude at a repetition rate equal to the frequency of the received signal. Therefore, the amplitude of the output signal remains constant over most of the range of usable input signals.

The physical layout of this integrated circuit required careful attention. The chip is only 55 mils square, and since the gain is 120 dB, the components on the chip must be arranged so as to avoid interaction of signals. The input and output terminals are located on opposite ends of the chip. Also, separate ground terminals are provided for the input and output stages.

The integrated circuit amplifier, which replaced 19 discrete components, improved the performance of the remote

Fig. 5—IC amplifier for the remote control receiver.



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control receiver. The amplifier has excellent sensitivity and limiting characteristics, is very stable, and maintains reliable operation over large ranges of temperature and supply voltage.

STEREOPHONIC PHONOGRAPH PREAMPLIFIER

The RCA CA3036 is an integrated stereophonic phonograph preamplifier in a 10-lead TO-5 package, small enough to be mounted with a ceramic pick-up in the phonograph tone arm. Each channel of the CA3036 consists of a two-transistor Darlington emitter-follower. Fig. 6 is a schematic showing the equivalent circuit of the ceramic pick-up, the internal circuitry of the CA3036 integrated circuit, and the equalization network the integrated circuit drives.

The ceramic pick-up equivalent circuit is a voltage generator in series with a small capacitance. The low-frequency response of the circuit is dependent upon the resistive load with which the pick-up is presented. For good low-frequency response, this resistance must be very high. For 3-dB response down to 50 Hz, a 700 pF ceramic element must have a resistive load in excess of 5 megohms.

If this impedance level were maintained across the signal leads threaded down the tone arm, great care would have to be taken to shield the leads from electrostatic hum and noise pick-up. Further, this shielding would have to introduce very little shunt capacity from the signal leads to ground. This is commercially impractical.

The Darlington emitter-follower is an impedance transformer, presenting the ceramic pick-up with very light resistive loading so that low-frequency response is maintained and at the same time providing low drive impedance to the leads down the tone arm. The low-impedance leads have little tendency towards picking up electrostatic hum and noise. Since the Darlington emitter-follower is a power amplifier as well as an impedance-transformation device, the signal voltage level to subsequent amplifiers is preserved. The power gain available makes possible a significant reduction in the mechanical impedance of the pick-up.

The RCA CA3036 was required to introduce no discernible AF noise into the phonograph amplifier chain. New transistor design techniques were developed to obtain bipolar transistors with very low flicker noise. The speakers of an RCA phonograph using the CA3036 are silent when the phonograph pick-up is lifted from the record, and no hum and noise is present to degrade even the lowest-level passages on a phonograph record.

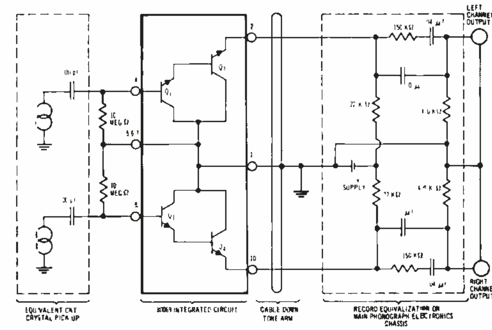


Fig. 6—Stereophonic phonograph preamplifier.

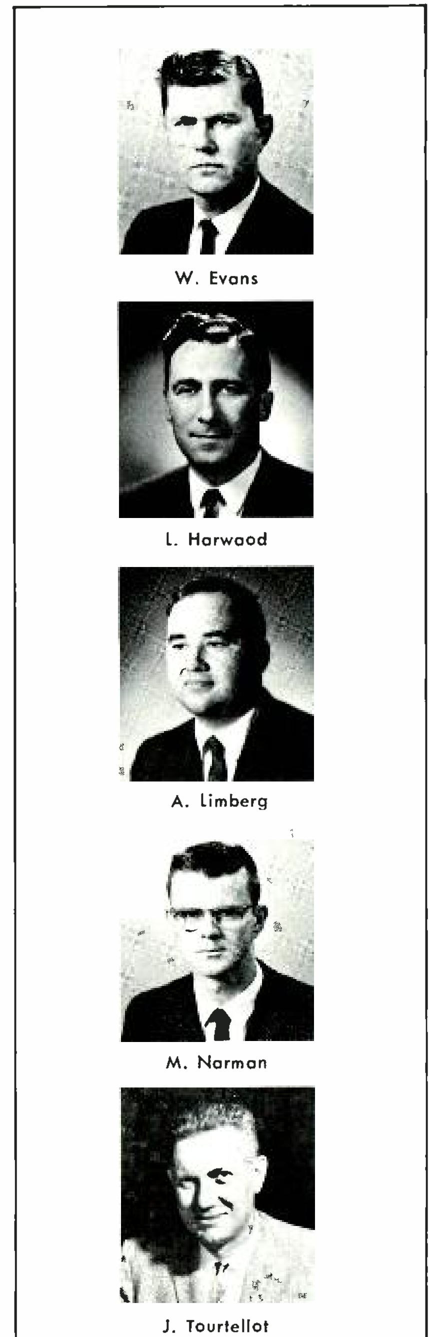
W. W. EVANS received the BSEE from Purdue University. In 1955, he was part of the staff responsible for the installation and operation of an NNC affiliate—WNDU-TV. He then joined DuKane Electronics Corporation and was responsible for the design on an adjusted harbor defense system for the Naval Ordinance Laboratory. From 1957 to 1959 he was in the U.S. Army where he studied, and later taught, microelectronics. In 1959, Mr. Evans was a Remote Site Engineer for Federal Electric Corp. and was responsible for the operation and maintainance of an isolated Tropospheric Scatter Communications installation. In 1964 he joined the RCA Home Instruments color television design group where he developed a totally electronic means of simultaneously adjusting and evaluating both the static and dynamic purities associated with the color television picture tubes. He is the co-inventor of the industry's first solid-state automatic fine tuning system used on commercial color television receivers as introduced by RCA in 1966. Mr. Evans was also responsible for the industry's first integrated circuit automatic fine tuning system used in RCA's current line of color TV receivers. Mr. Evans is a member of IEEE, Tau Beta Phi, Phi Etta Sigma, and Etta Kappa Nu. In addition, he is a member of the Indiana Society of Professional Engineer.

L. A. HARWOOD graduated from Munich Institute of Technology in 1949 with a BSEE. He received his MSEE in 1959 from the University of Pennsylvania. Following engineering experience at Pilot Radio Corp. and Picattiny Arsenal, Mr. Harwood joined RCA in 1952 as an engineer in the Home Instruments Division; his experience in television receivers includes work in development and design of UHF and VHF tuners, development of parametric and tunnel diode converters, and development of a transistorized UHF tuner for TV receivers. Now located with the Home Instruments Division in Somerville, he had most recently been a member of the Home Instruments Affiliated Research Labs., Princeton, N. J. He has been granted several patents in his field of work; he is a member of the IEEE.

A. L. LIMBERG received the BEE degree from Union College in 1958, the MSEE from the University of Pennsylvania in 1966. In 1958 he came to RCA as a design engineering trainee; later in the year he joined the Research Applications Laboratory at the David Sarnoff Research Center, where he engaged in research and development of television receivers and stereophonic radio systems. In 1962, this laboratory merged with the Systems Research Laboratory, where Mr. Limberg did research on communications and display systems. In 1965 he transferred to the Home Instruments Division to work on integrated electronics. Mr. Limberg is a member of Sigma Xi and serves on the FM Receivers Standard Committee of the IEEE.

M. NORMAN received the BSEE degree from the University of Illinois in 1964, and later did Graduate work at Purdue University. In 1964, Mr. Norman joined the RCA Home Instruments Division where he was assigned to the Remote Control Group. He designed a low-cost remote control TV transmitter; he also worked on the remote-control TV receiver preamplifier containing integrated circuits.

J. A. **TOURTELLOT** studied at Columbia University and graduated in 1937 with an AB degree in Physics. From 1937 to 1939 he was engaged in his own private business and joined RCA in 1940. From 1940 to 1945, he was engaged in UHF, electromechanical modulators and "butterfly" circuits work for military applications. From 1945 to 1953 he was with the Philco Corporation, and upon his return to RCA in 1954 joined the Radio & "Victrola" Record Changer Design group. Since then he has been engaged in development and design work on the automobile "Victrola", stereo phonograph pickups and amplifiers, the "Studiomatic" record changer, and tape recorders for the RCA Victor Home Instruments Division.



W. Evans

L. Harwood

A. Limberg

M. Norman

J. Tourtellot

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MICROELECTRONICS IN THE ESSA 2 SATELLITE

The application of microelectronics in the ESSA 2 satellite is described in this paper by briefly discussing the satellite and its mission, the function of the command and control subsystem, and the factors leading to the selection of integrated circuits. Then, the integrated circuit characteristics and typical usage are presented, followed by descriptions of related packaging and manufacturing techniques, special environmental considerations, and the test philosophy and test program. In conclusion, a summary of the operational flight history of the subsystem and the impact of this circuit development on the future of microelectronics in space are presented.

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At 0858 Eastern Standard Time on the morning of February 28, 1966, the ESSA 2 satellite was launched from Cape Kennedy, Florida, into a near-polar sun-synchronous circular orbit some 750 nautical miles above the earth. This event marked the successful initiation of the first fully operational, global weather satellite system. The ESSA 2 satellite, together with its companion ESSA 1 satellite, launched earlier on February 3, 1966, provides complete pictorial coverage of the earth and its cloud cover on a daily basis without interruption. The satellite was among the first to use microelectronic devices extensively. Approximately 420 integrated circuits were used in the command and control subsystem.

SATELLITE DESCRIPTION

The ESSA 2 satellite was built for the Environmental Science Services Administration (ESSA) of which the U.S. Weather Bureau is a division. This satellite is the evolutionary product of the highly successful series of TIROS satellites[1] launched since 1960.

The satellite (Fig. 1) is a cylindrical 18-sided polygon, 22 inches high and 42 inches in diameter, weighing 290 pounds. Approximately 10,000 N-on-P silicon solar cells, mounted on the top and side surfaces, convert solar radiation into electrical energy, which directly powers the satellite. Under normal satellite load conditions, excess electrical energy from the sun is stored in nickel-cadmium batteries; during peak loads, the batteries discharge. Most of the satellite components are mounted on a circular baseplate which is covered by the cylindrical "hat" section. A crossed-dipole antenna, for command reception and for telemetry transmission, projects from the baseplate. A whip or single dipole antenna, for television transmission, projects from the center of the satellite hat. In orbit, the satellite is controlled to spin about its cylindrical axis with a period between 5.475 and 5.525 seconds with a spin axis perpendicular to the orbit plane. Thus, the satellite resembles a wheel, rolling about the earth in a circular orbit, stabilized in attitude by its spin momentum.[2]

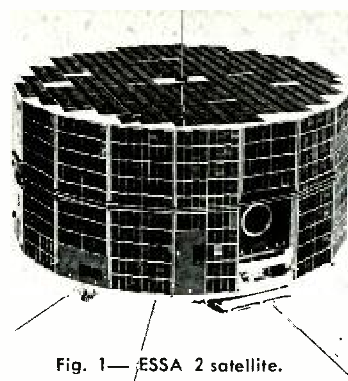
Fig. 1—ESSA 2 satellite.

Two redundant television cameras, to ensure a longer operational lifetime for the system, are mounted perpendicular to the spin axis and point through the side of the hat. Either TV camera subsystem can independently provide complete, global picture coverage on a daily basis. As the satellite rotates about its spin axis, the cameras alternately view the earth's surface and the sky. Pictures are taken automatically when the camera in use is pointing along the nadir or local vertical every 64 spins (352 seconds). The local vertical is determined by infrared horizon-crossing sensors which are displaced a particular distance along the rim of the satellite from each camera. Each picture covers an area of the earth about 2000 statute miles on a side; they can be resolved to approximately 2 statute miles at the center. Overlap is provided between successive pictures and between adjacent orbits.

The Automatic Picture Transmission (APT) television cameras use special vidicon tubes which can be exposed rapidly and yet store the picture information without degradation for 200 seconds, while it is subsequently being read out. The images recorded on the camera are scanned in an 800-line raster and transmitted to APT ground stations. Because of the long readout time available, the baseband of the video signals is quite small (on the order of 1.6 kHz), and these signals are transmitted to the earth using a narrow bandwidth FM transmitter. This, in turn, permits the

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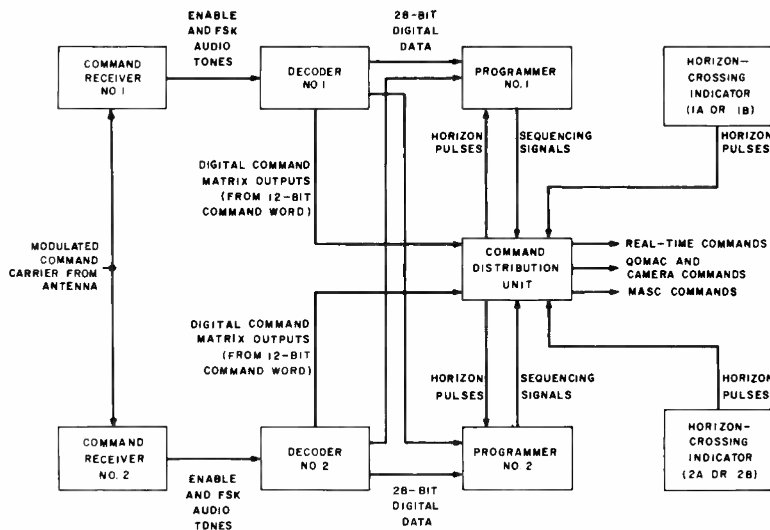


Fig. 2—Functional block diagram of command and control subsystem.

use of simple, inexpensive receiving stations at any convenient location.

The APT ground stations require only a single operator and record the pictures on facsimile equipment. Line-of-sight radio contact with the satellite, and hence picture reception, can be obtained at any ground station from one to three times a day. During a given contact, one to three pictures can be received. There are 50 such APT ground stations located in the United States and 100 others located throughout the world.

COMMAND AND CONTROL SUBSYSTEM

The command and control subsystem functions as a central nervous system for the satellite. It receives, demodulates, and decodes the commands transmitted to the satellite from either of the two Command and Data Acquisition (CDA) ground stations located in the USA; and it actuates the various onboard systems and devices in a preprogrammed sequence. Among the subsystems controlled in this manner are the TV camera subsystem, the attitude spin-rate control subsystems, the beacon and telemetry subsystem, the power supply subsystem, and the antennas. As can be seen from Fig. 2, the command and control subsystem is completely redundant, as are all the other major subsystems and components in the satellite. Thus, in general, two identical units must fail before a major mission function can be disabled.

The command and control subsystem contains a common command distribution unit (CDU) which processes and distributes the commands and programming sequences developed by the decoder/programmer. It also selects, by direct commands, the particular units to be used from among the redundant units aboard the satellite. Thus, individual elements of one subsystem can be cross-coupled to operate with elements of the other subsystem. This enhances the overall reliability and provides greater operational flexibility. Integrated circuits are used extensively to perform a variety of digital logic and control functions in the decoding and programming portions of the command and control subsystem.

MICROELECTRONICS IN THE COMMAND AND CONTROL SUBSYSTEM

While earlier versions of the subsystems had been tested on previous meteorological satellites such as NIMBUS and TIROS, the command and control subsystem (with the exception of the command receiver) had to be uniquely designed to fulfill the mission requirements. The available volume, weight, and power were marginal in view of the anticipated number of modules required. Improvements in reliability were also necessary because of the increased component count, logical complexity, and the operational nature of the mission. In view of these difficulties, consideration was given to the use of integrated circuits to obtain the necessary improvements.

Studies conducted in 1963[3] and earlier to explore the use of integrated circuits for spacecraft had been cautiously optimistic. Therefore, to obtain additional data and to gain greater confidence in these devices, an existing attitude clock, of the type used on early TIROS satellites, was redesigned using commercially available integrated circuits. The results are shown in Fig. 3. The integrated-circuit clock successfully passed all the environmental tests normally performed on TIROS units, while substantially increasing confidence in the use of microelectronics for space and for ESSA 2.

As a result of this study and other studies, it was decided in 1964 that integrated circuits would be used, wherever possible, in the decoder/programmer units for the TOS satellites. These units largely required low-power low-speed digital circuitry which were ideal for integrated-circuit application.

A family of RCTL (Resistor-Capacitor-Transistor Logic) integrated circuits were selected after careful study of all available devices. The choice was based on the comparatively long history of use at the time (approximately 2 years) and the high reliability data supporting this usage. In addition, the low power consumption (2 milliwatts per flip-flop) and the logical versatility of the basic mod-

Fig. 3—Attitude clock.

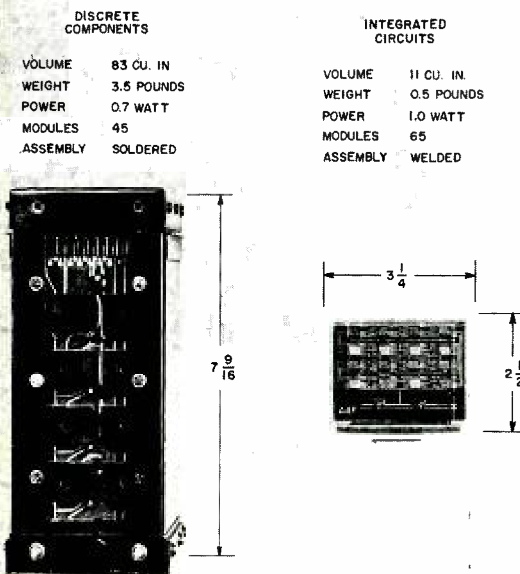


Fig. 4—RCTL flip-flop, schematic diagram.

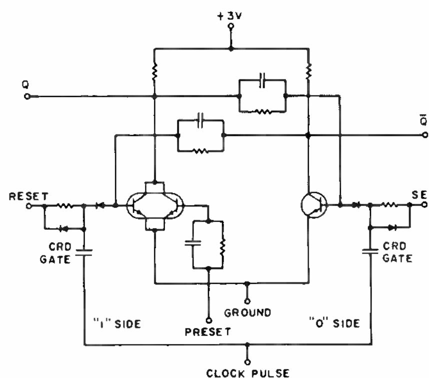
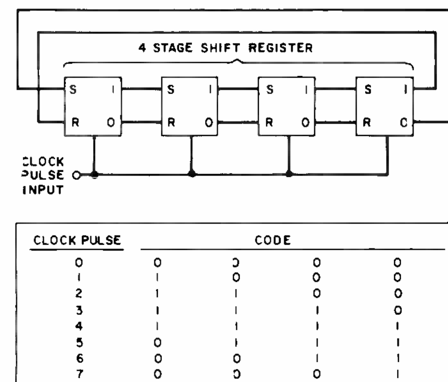


Fig. 5—Divide-by-eight synchronous counter.



CLOCK PULSE	CODE			
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

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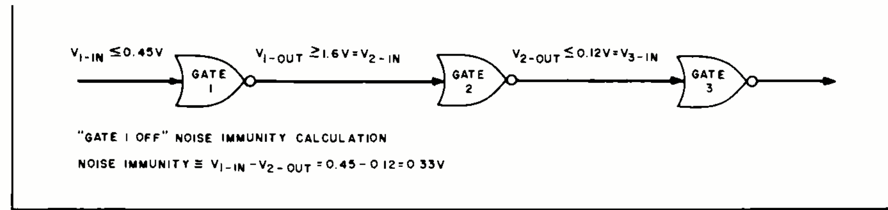

Fig. 6—Noise immunity calculation.

ules were very desirable. Implementation of the logic was accomplished using three logic elements: the flip-flop, the NOR gate, and the clock driver. As can be seen from a typical schematic diagram shown in Fig. 4, the logic was basically DC coupled, with the exception of the clock-pulse input to the flip-flop. The low power dissipation in the logic resulted from a combination of low voltage level (3.0 volts) and relatively high resistance (collector resistors were approximately 5000 ohms, base resistors were of the order of 20,000 ohms). Positive NOR logic was used throughout the circuits.

The flip-flop is a conventional bistable configuration. Initial conditions, for use with DC control signals, may be established with the preset input which drives a transistor in parallel with the Q (or logical "1") transistor of the flip-flop. A positive voltage at this input sets the flip-flop. When not used, the preset input is grounded. Set or reset is accomplished by symmetrical capacitor-resistor-diode (CRD) networks at each input. A positive clock pulse at the clock input charges each capacitor of the CRD gating network. When the clock pulse terminates rapidly, the negative-going transient voltage cannot instantly change the charge on the CRD capacitors; instead, it draws stored charge and base-drive current from the conducting transistor (providing the appropriate set or reset voltage is low) and causes the transistor to be biased to the "off" condition, thus changing the state of the flip-flop. The CRD gating network permits the use of the flip-flop either as a counter or as a shift register by appropriate interconnections.

To enhance the reliability of operation, and to guard against spurious counts, conventional ripple-thru counting was not employed. In its place, various versions of synchronous counting were employed, an example of which is shown in Fig. 5. The upper limit of counting or repetition rate for this flip-flop was approximately 500 kHz. This was well above the maximum operational rate of 150 kHz. The maximum number of "fan outs" per logic element was selected to be five, based on available drive current and noise immunity.

The noise environment of the command and control subsystem was of concern because of the close proximity of radio-frequency transmitting units as well as high-current relays and switches. For this reason, considerable effort was devoted to reduction of noise within the decoder/programmer unit and to the establishment of noise-immunity criteria and specifications for the integrated circuits. A simple but effective approach was evolved, in a joint effort with the manufacturer, using the transfer characteristics of the gate which were calculated at the extremes of the component tolerances. These worst-case analyses were made at temperatures of −55°C, 25°C, and 125°C; the extremes were far in excess of the anticipated space operational temperatures. (Telemetry data from the ESSA 2 satellite in orbit indicated baseplate temperatures ranging from approximately 10°C to 25°C.)

Typical input-output gate transfer characteristics at 25°C are given as follows to illustrate the noise-immunity calculation: the minimum gate output for the "gate-off" condition was +1.60 volts, provided the maximum gate input voltage was no greater than +0.45 volts. Conversely, the maximum gate output for the "gate-on" condition was +0.12 volts for an input voltage no less than +1.2 volts. Two noise-immunity values corresponding to the "gate-on" and "gate-off" conditions are derived from this data. The "gate-off" noise immunity calculation is illustrated in Fig. 6. Noise immunity is defined as the level of additive noise voltage which can be tolerated in cascaded gating before a logic error is produced by an interchange of the logic "1" and "0" voltage levels. This is conservatively calculated to be the difference between the maximum allowable "gate-off" input voltage to gate 1 and the maximum "gate-on" output voltage from gate 2.

Noise immunity peaks between zero and −25°C. At lower temperatures, the noise immunity decreases due to increases in the saturation voltage of the gate transistors; at higher temperatures, increases in the leakage current cause decreases in the "off" level and a corresponding reduction in the noise immunity. Changes in the transistor *beta* and in the base-to-emitter voltage characteristics also contribute to noise immunity decreases in both directions.

In addition to establishing the noise-immunity criteria and corresponding acceptance specifications for the integrated circuits, noise was minimized in the design of the power supplies and the power distribution and grounding systems. The decoder/programmer has separate DC-to-DC converters to permit independent operation (these were located within the enclosure to minimize noise pickup).

The integrated circuits were mounted in planar fashion on multilayer glass-epoxy printed-circuit boards. Radio-frequency decoupling capacitors were used for power supply decoupling on each board. Power distribution and grounding were accomplished using separate internal conductive layers of the multilayer boards. The integrated circuit flatpacks, which were housed in 0.25-inch by 0.125-inch metallic cans, were mounted on the top side of the board. Circuit interconnection wiring ran along the top and bottom sides of the board. A thin insulating shim was cemented to the bottom of each integrated circuit to permit it to be placed over wiring runs without interference. The power and ground planes were connected to the top and bottom wiring by plated-thru holes which made contact to the intervening layers. The ground and power planes served as low-impedance paths for current flow, and they acted as shields against board-to-board or external-noise coupling.

The method of connection was another concern in the design and manufacture of the integrated circuits. After an evaluation of welding and other methods, an impulse-soldering technique was selected. In this method, two previously tinned surfaces are joined by causing the solder to reflow under a controlled application of heat. An improved version of this technique was developed, in which a resistive element bridges the electrode gap; this method produces an excellent joint with high strength.

The complete decoder/programmer unit is shown in Fig. 7. The unit weighs 9.6 pounds and measures approximately 9.2 inches high by 7.3 inches wide by 5.6 inches deep. The enclosure is of 1/16 inch aluminum. Interconnections to other subsystems in the satellite are made through the connectors.

ENVIRONMENTAL CONSIDERATIONS

The satellite system must cope with a hostile environment throughout its lifetime. Previous spacecraft designs had successfully solved many of the problems associated with operation in the near vacuum of outer space, the temperature excursions encountered in space, and the shock, vibration, and acceleration forces present during the launch into orbit. Much less design data and operational experience were available, with respect to effects of the specific energetic particles known to be present (trapped by the earth's magnetic field) at the intended 750-nautical-mile altitude. Previous TIROS satellites had operated at approximately 400-nautical-mile altitudes where the radiation intensity was about 50 times less.

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The sources of potential damage were electrons in the range 0.5 to 8 MeV and a substantially smaller number of protons with energies extending to 1000 MeV. In addition, a third hazard was caused by x-rays or bremsstrahlung produced by the deceleration of energetic electrons striking the external surface of the satellite. Although the actual intensity of radiation incident on the satellite is a function of the orbital altitude, the damage effects depend solely on the total integrated dose over the 6-month assumed mission life. This value was conservatively calculated to be about 10^5 rads. for a typical subsystem.

Information obtained from the integrated circuit supplier, based on tests with a nuclear reactor, indicated that the units were relatively insensitive to radiation. But, because of fundamental differences in the nature of this test radiation and the space environment, a closer simulation was achieved by exposure to 1-MeV electrons and gamma radiation. The 1-MeV electron bombardment was made for dose levels up to 10^{15} electrons per square centimeter; gamma radiation dosage was up to 3×10^7 rads. Sample circuits were subjected to this radiation. Except for two unexplained failures, all the samples survived with relatively minor changes in spite of dose levels 100 times greater than the Tos mission level. In the case of the failures, the evidence pointed to sudden catastrophic failures which are not characteristic of radiation damage. A typical test result[4] is shown in Fig. 8, which depicts the effects of varying levels of radiation on the transfer characteristic of a gate.

ENVIRONMENTAL TEST PROGRAM

In addition to the radiation tests, a number of other environmental tests were conducted under a formal test program that ensures successful operation of the system in orbit. Tests were made at unit, subsystem, and overall satellite levels. Components which failed were painstakingly analyzed to determine the failure mechanism, be it a design inadequacy, a misapplication or overstressing of the part, or a random failure. Even random failures have causes, albeit obscure, and every effort was made to establish detailed specifications and tests to minimize this source of malfunction.

Testing progressively eliminated the sources of predictable failures and hopefully weeded out the remaining random failures, without fatiguing or overstressing the good or well-behaved parts. This technique has been remarkly effective in ensuring successful operation.

The integrated circuits were subjected to a test program both at the component manufacturer's plant and at the satellite manufacturer's facility. A summary of the environmental test levels follows:

Test	*Level*
Shock	1500 g (0.5 millisecond)
Acceleration	20,000 g (1 minute)
Vibration	20 g, peak (5 through 2000 Hz)
Temperature	
a) Storage	125°C (1000 hours)
b) Shock	0°C to 100°C (10 cycles)
c) Cycling	−55°C to 125°C (10 cycles)
Vacuum	7.5×10^{-10} mmHg (48 hours)
Humidity	95 percent (during temperature cycling)
Operating Life	10,000 hours, minimum required

Each integrated circuit was subjected to a preconditioning program which included a nonoperating 48-hour bake at 150°C and a 300-hour dynamic operating test at 125°C. The units were also temperature cycled between 125°C and −55°C in a separate test. Lot acceptance criteria were established on the basis of successful completion of these and other tests.

The electrical design was verified by construction and test of a laboratory model or breadboard of the command and control subsystem. Following this, a prototype decoder/programmer unit was built from final drawings and specifications, using production methods and tooling. This unit was then successfully tested under simulated environmental conditions, both as a separate unit, and subsequently as part of the prototype Essa 2 spacecraft.

OPERATIONAL PERFORMANCE AND CONCLUSION

On August 28, 1967, the Essa 2 satellite successfully completed an orbital life of 18 months, providing continuous daily global picture coverage without interruption. All command functions were successfully performed repeatedly without difficulty. However, after approximately 4 months in orbit, due to an as yet unexplained anomaly, the satellite failed to execute a series of commands. Telemetry data revealed the difficulty to be in one of the two redundant decoders. The second decoder was substituted and successfully performed all the command functions; no loss of operational data or mission function was suffered.

The success of the Essa 2 mission established a noteworthy precedent for the extensive use of microelectronic components in a fully operational system. The use of integrated circuits permitted the design of a relatively sophisticated command and control subsystem which performed more functions with greater reliability than was previously possible. It has been estimated that the command and control subsystem was reduced in size by a factor of 3 and in weight by a factor of 2.5 compared to a system performing the same functions but using discrete components. The power consumption of the microelectronics modules was one-eighth that of discrete modules used previously. In addition, the savings in size, weight, and power consumption made possible the use of completely redundant microelectronic units which further enhanced the reliability. Successful prolonged operation in a high radiation environment was another salient advance. Based on the Essa 2 satellite (and, since its launch, Essa 3, 4, and 5) the application of microelectronics in space is not only practical but is bound to play an ever-increasing role in the drive to improve the reliability of spacecraft components while significantly reducing size and weight.

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Fig. 7—Decoder/Programmer.

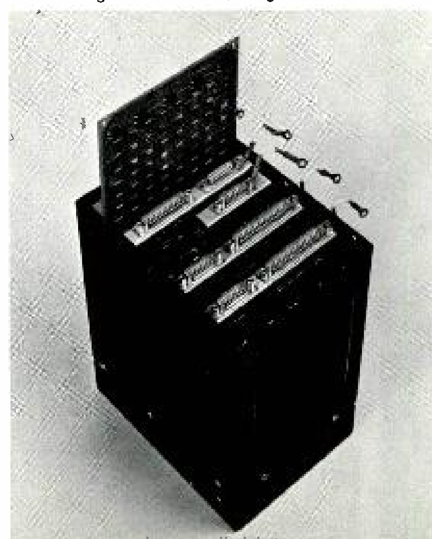
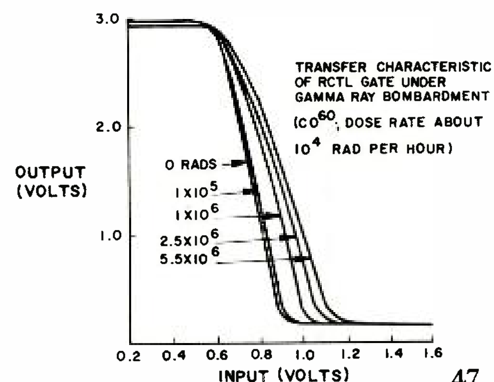


Fig. 8—Typical radiation results.



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GREEN CHIP: HYBRID INTEGRATION TECHNIQUES FOR HF/VHF/UHF CIRCUITS

For many military requirements (e.g. HF/VHF/UHF transceivers) the need for small quantities of special circuit types has prompted the development of Hybrid Integration Techniques. These techniques combine the best attributes of microelectronic technologies to achieve high performance characteristics. The philosophy behind the techniques is relatively simple: choose a method to suit the application. These hybrid integrated circuits must not only be small in size and weight, but their performance characteristics must be equal to, or better than, the same circuit using conventional discrete components. This paper describes the techniques used in fabricating a 300-MHz RF amplifier, a 60-MHz IF amplifier, an 18-MHz IF amplifier, and a phase comparator. The performance of the circuits described will be compared with the corresponding circuit using conventional discrete components. All the circuits developed are part of the CSD ADCOM-75 program.

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To MEET the need for UHF microcircuits for military usage, the Hybrid Integration Techniques Program (Green Chip) for HF/VHF/UHF circuits was initiated. This program centered on the development of a two-stage UHF amplifier using multichip hybrid techniques. The excellent results obtained from the UHF amplifier have since given way to a broader spectrum of hybrid microcircuits.

For most applications, the use of ceramic and cermet passive component chips on gold plated ceramic substrates gives optimum results in terms of ease of fabrication and maintaining circuit tolerances. For other purposes, vacuum evaporation of thin-film components is more desirable. This flexibility of design is one of the advantages of the hybrid technique. Design changes can often be made without added expense and with little loss of time. Size and weight vary with the techniques used and circuit complexity, but a considerable reduction is still achieved. In many instances, repairs can be made on the microcircuit without unusual difficulty. The cost of the circuit does not reflect high tooling, masking or other preliminary costs, and a savings is thereby achieved.

FABRICATION TECHNIQUES

Multichip Hybrid IC

The fabrication of a multichip hybrid begins with the substrate, a ceramic slab 0.025 inch thick, gold plated on both sides, and usually 0.72 inch square. An interconnection pattern is photoetched on the substrate by conventional methods. The masks are cut on Rubylith-type mylar films and exposed on a 10:1 reduction camera. The substrates are exposed one at a time, since the quantities required are small.

Once the substrate is prepared, the passive and active components are soldered using solder preforms and a hot gas jet as a soldering tool. Where only one end of a passive component can be attached directly to the interconnection pattern, the other end is connected by soldering on a small-diameter copper wire. This makes a stronger connection than gold wire. Where silicon active devices are available only as bare chips, wire bonds are made to the devices by ultrasonically bonding aluminum wire.

The chip components are obtained from several vendors, and because of increasing interest in hybrids, new sources of components are continually appearing. The resistors used are "Ceradot" cermet cylinders 0.050 inch in diameter and 0.030 inch high, rated at 1/10 watt dissipation, and are made by CTS Corporation. The capacitors are multilayer ceramic chips made by Electro Materials Corporation. Chip size varies with capacitance and dielectric, but the size typically used is 0.095 x 0.050 x 0.050 inch.

Wherever possible, transistors, monolithic integrated circuits, and diodes are obtained in a small package of a size compatible with hybrid techniques. While it is true that these packages take up more real estate than bare chips, easier handling and a high reliability is assured. Typical of these is the "pill" package long used for microwave diodes, nominally 0.05 to 0.06 inch in diameter and 0.05 to 0.075 inch high. Transistors are being marketed by at least two manufacturers in a "LID" (Leadless Inverted Device) ceramic package 0.075 x 0.045 x 0.032 inch in size. This package has gold plated pads which may be soldered directly to the interconnection pattern. The transistor is sealed in the package with an epoxy.

Inductance in microcircuits has always been a square peg in a round hole. Inductors with acceptable Q's for most application require volume, which is usually at a premium. However, inductance cannot always be designed out of the circuit. Therefore, we have to learn to live with the problem of inductance, until new techniques currently being developed become available. For some applications, inductors of a compatible size are commercially available. Fixed and tunable inductors nominally 0.080 inch in diameter and 0.170 inch long are marketed by Piconics, Inc. Fixed toroidal inductors are available from Delevan Electronics Corporation in a package 0.1 x 0.1 x 0.065 inch in size. However, the

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SHUI YUAN received the BSEE from the University of California in 1952 and the MSEE from Columbia University in 1956. From 1953 to 1955 he was a Member Technical Staff at RCA, where he designed and developed television broadcasting components. His main responsibility was the design and development of a high-power UHF slotted TV transmitting antenna. From 1957 to 1958, he was employed as a Senior Engineer with the Electronics Division of Curtiss-Wright Corp. From 1958 to 1963, he was associated with the Electronics Research Laboratory of Columbia University as a Senior Research Engineer. During that period he made some basic contributions to the theory and design of highly-efficient frequency multipliers, wideband parametric amplifiers for FM communications systems, and threshold extension of FM systems. In 1963 he rejoined RCA, as a Senior Member Technical Staff in the Solid-State RF Techniques Group; he is now a Leader of the Advanced Microelectronics Techniques Group. With the Solid-State RF Techniques Group, his responsibilities were the Interference Reduction, Frequency Multiplier, and Signal Detection in the Presence of Noise programs. He is the co-inventor of a balanced mixer circuit which can alleviate high-order intermodulation and cross-modulation distortion. He is currently involved in the fabrication of thin-film circuits and the design and development of the microelectronic microwave circuits for X-band transmitters and receivers. Mr. Yuan is a member of Tau Beta Pi, Eta Kappa Nu and Phi Tau Phi, has published about ten papers, and has a pending patent.

THOMAS PICUNKO received the BEE degree from the City College of New York in 1962. Following graduation, he joined RCA specialized training program and was eventually assigned to the New York Systems Laboratory where he became engaged in the development of thin-film parametrons. In 1963, he was called to active duty with the U.S. Army Corps of Engineers. During his tour of duty he was assigned to the Army Engineer School at Fort Belvoir, Va., where he supervised instruction in electrical subjects. Returning to RCA in 1965, he became involved in the development of thin-film integrated circuits. His current assignment is the development of hybrid integration techniques for microminiaturizing circuits operating into the UHF range. Mr. Picunko is a member of Eta Kappa Nu, Tau Beta Pi, and the IEEE.

unloaded Q's of both of these types are typically 40 or less. Where a higher Q inductor is required, as in an RF circuit, hand-wound air-core inductors of a comparable size having a Q of 80 or more are used. While this cannot be considered a high Q, it has proved adequate for most applications. Tuning is accomplished by spreading the turns of the coil. An adhesive or epoxy can then be used to fix the coil in place.

Thin-Film Hybrid IC

Circuits made of thin evaporated films are usually deposited on a substrate of glass. Metal evaporation masks are used, although photoetching is done occasionally. The interconnection pattern consists of a thin layer of chromium for good adhesion, followed by a thick layer of gold or gold-palladium. Gold-palladium is used when it is desired to avoid scavenging by hot solder. Resistors are evaporated next. These can be nichrome (100 to 500 ohms/square) or a high resistance alloy (2100 ohms/square at 0°C). The resistors are then coated with silicon monoxide. Where necessary, resistors can be trimmed upward to closer tolerances by current pumping. The capacitor dielectric is then evaporated on the bottom electrodes, which are part of the interconnection pattern. Silicon monoxide is used for the dielectric, followed by an upper electrode of aluminum. Capacitance per unit area can vary depending on the desired breakdown voltage. For example, a thickness of 6000 Angstroms (0.05 pF/square mil) has a breakdown voltage of about 100 volts.

Once the evaporation processes are completed, active devices are attached with solder or conductive epoxy. If necessary, wire bonds are then made as described previously. The problem of inductance and tuning is treated as above, except that additional precautions must be taken to avoid stressing the glass substrate.

Packaging

At the beginning of this program, the type of package to be used for the circuits developed was not established, and it was convenient to use a one-inch-square substrate as shown in some of the Figures. Recently, however, an American Lava 60-lead one-inch-square flat-pack has been used. This requires a substrate of not more than 0.72-inch square. The availability of smaller chip components permits a higher packing density to fit the smaller substrate. Naturally, not all 60 leads are used for a given circuit, but the large number permits flexibility in deciding the configuration of input-output connections. Other packages are also being evaluated.

All the circuits developed to date have been feasibility models or one-of-a-kind circuits. Consequently, problems of encapsulation, stability and reliability were not a major consideration. Eventually data on these factors will be required, and a program of encapsulation studies and environmental testing is being planned which will lead to a hybrid circuit package meeting military specifications.

HYBRID ICs VERSUS CONVENTIONAL CIRCUITS

UHF Amplifier

Fig. 1 shows a UHF chip hybrid amplifier of the type developed under the Green

Fig. 1—UHF amplifier on one inch square substrate.

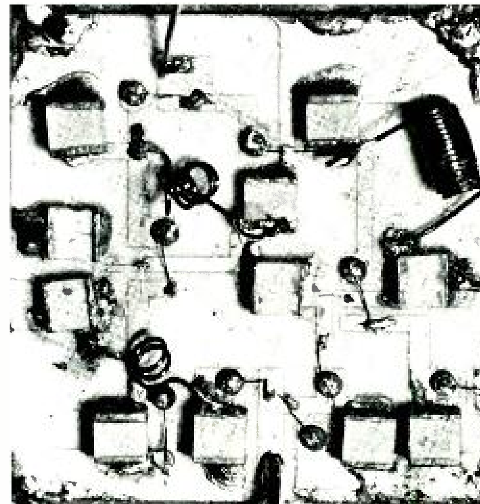
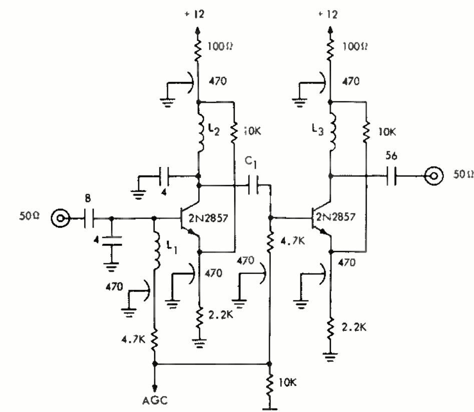


Fig. 2—Schematic diagram of UHF amplifier.



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Chip program. The substrate is one inch square and has larger capacitors than those currently being used. A circuit schematic is shown in Fig. 2. The amplifier consists of a tuned-base tuned-collector stage followed by a wide-band stage. Typical data is tabulated below comparing the hybrid with a conventional circuit. The higher gain of the hybrid is due in part to hand picking 2N2857 transistor chips with good DC characteristics in an attempt to keep the noise figure low. Measurement of the noise figure of a chip transistor has not been accomplished at RCA.

UHF Amplifier

	Conventional	*Hybrid*
Supply voltage (volts)	+12	+12
AGC voltage (volts)	+5.0	+5.0
Gain at center frequency (dB)	20	25
Center frequency (MHz)	290	285
3-dB bandwidth (MHz)	30	28
1-dB bandwidth (MHz)	20	14
Noise figure (dB)	5	5

60-MHz IF Amplifiier

The next circuit which was developed is shown in Fig. 3. This is a 60-MHz IF amplifier consisting of two tuned stages using 2N916 transistors. The substrate used here is also one inch square and also has the larger variety of chip capacitor. Comparative performance data is listed below for a 50-ohm source and load.

60-MHz IF Amplifier

	Conventional	*Hybrid*
Supply voltage (volts)	12	12
AGC voltage (volts)	5.0	5.0
Gain at center frequency (dB)	17	22.5
Center frequency (MHz)	60.0	60.8
3-dB bandwidth (MHz)	2.3	2.5

18-MHz IF Amplifier Detector

One of the most difficult circuits to develop in hybrid form was the 18-MHz IF amplifier-detector shown in Fig. 4. The substrate used is 0.720 inch square for mounting in a one inch square flatpack; smaller chip capacitors are used. The circuit consisted of three high-gain wide-band stages followed by a detector and AGC amplifier. Due to the high gain and circuit layout, enough regeneration was present to cause severe bandwidth narrowing. Eventually this problem was reduced to the point where the circuit was useable. Comparative performance data is tabulated below. The inductors used are Delevan "micro-I" inductors and appear as black squares in Fig. 4.

18-MHz IF Amplifier-Detector

	Conventional	*Hybrid*
Supply voltage (volts)	+6.8	+6.8
Center frequency (MHz)	18	19.3
3-dB bandwidth (MHz)	6	3
AGC trip point at center frequency (μv)	100	105
Audio output for 100 microvolt input at center frequency (mv)	165	160

Phase Comparator

A phase-comparator circuit, part of a frequency synthesizer, is shown in Fig. 5. This circuit is on a 0.720 inch square substrate and is mounted in a one-inch-square flatpack. The transistors are in "LID" packages and the diodes are in glass cylinders instead of the bare chips shown in other Figures. The maximum capacitance in this circuit is 22,000 pF. This unit is currently being evaluated and no data is available.

Circuits Under Development

Hybrid circuits now in preparation include a thin-film 330-MHz RF amplifier using the circuit shown in Fig. 2, a series of voltage-controlled oscillators (VCO) covering the range of 220 to 400 MHz, and a buffer amplifier to follow the VCO stages. These and the previous circuits are all part of CSD's ADCOM-75 program. Another circuit being developed is the GOTHAM program common module, including a 200-MHz amplifier and mixer using dual-gate FET's, and a crystal-controlled oscillator-doubler to drive the mixer.

CONCLUSIONS

The hybrid integration technique has proven to be useful in circuits where special performance characteristics must be met and the quantity of circuits of the same type is small. Hybrid integrated circuits take advantage of the best characteristics of diffused silicon, thin-film, and ceramic technologies. It not only offers flexibility, quick fabrication, and good reliability, but also the capability of small quantity production at a relatively low cost. It makes possible the integration of a large family of unique circuits tailored to the needs of the circuit designer.

ACKNOWLEDGMENTS

Contributors to the development and fabrication of the circuits described in this paper include J. Kurtz and A. Usowski. Circuit designs and assistance in circuit evaluation were provided by members of D. Westwood's group of CSD in Camden.

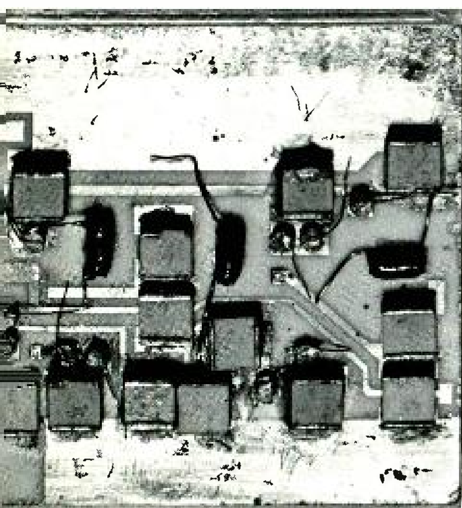

Fig. 3—60-MHz IF amplifier on one-inch-square substrate.

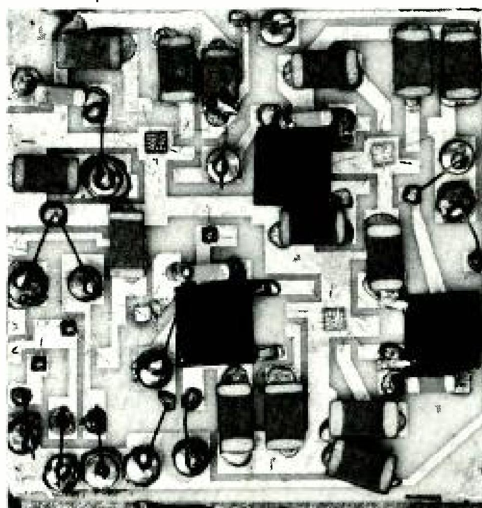

Fig. 4—18-MHz IF amplifier-detector on 0.720-inch-square substrate.

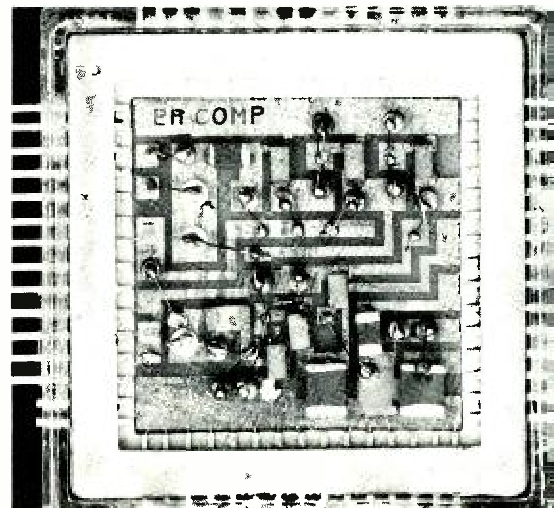

Fig. 5—Phase comparator in one-inch flatpack.

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A MONOLITHIC INTEGRATED CIRCUIT APPROACH

A variety of circuits can be provided on a single monolithic die, thereby reducing costs for lower volume production applications. The two final steps in production of a monolithic circuit—contact etch and metalization—determine the circuit type desired. In this paper, six circuits, which were designed and fabricated to verify this approach, are described along with one application of each.

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Integrated Analog Subsystems

Defense Microelectronics, Somerville, N. J.

THE MONOLITHIC CIRCUIT approach requires rather high capital investment for masks and layout for a single circuit design; therefore, the circuit must have a variety of uses to insure a large volume production. Large volume needs must be evident for a circuit designed for a specific application. An approach which reduces cost for lower volume production applications is to layout a chip for a variety of circuits. Up to the final two steps—contact etch and metalization—the processing and masking are identical. A further advantage of this approach is that up to the final two processing steps the wafers are coated with SiO_2 and can be stored; thus, the final processing can depend on customer request.

To evaluate this approach, six circuits were submitted for fabrication with sufficient layout and circuit evaluation to insure feasibility. The six circuits chosen were two simple circuits (a four-transistor array and a six-diode array) and four complex circuits (a multiplex modulator, a balance modulator, a double differential amplifier, and double cascode amplifier).

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It was found in final layout that the chip area could be reduced by 35% for the transistor and diode array over the other four circuits. This reduction in area has an advantage that offsets the initial mask investment due to the larger number of circuits obtainable per chip; therefore, the decision was made to divide the approach into two-circuit families.

TWO-CIRCUIT FAMILY

The transistor and diode array is made up of six active devices on a circuit die of 40 x 40 mils which was found an adequate area for devices, metalization interconnects, and bonding pads. The

G. THERIAULT received the BS degree in Engineering Physics from the University of Maine in 1950. He joined RCA in the fall of 1950. After a training program, he joined the Advanced Development Section of the Home Instruments Division where he worked on semiconductor applications to radio and television. In 1963, he joined the Defense Microelectronics Group of Defense Engineering Products Division where he has since worked on analog circuit design and application of monolithic integrated circuits. In 1966, he was made Engineering Leader of the Integrated Analog Subsystem Group. Mr. Theriault holds fourteen U.S. Patents.

Fig. 1—Circuit diagram and TO-5 terminal connections for CA 3018.

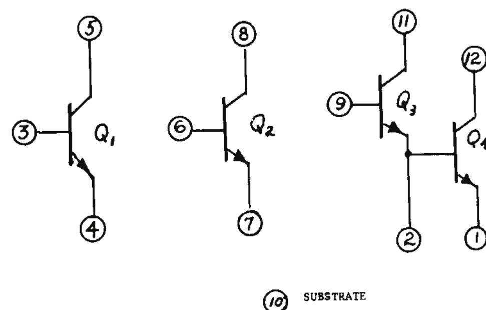
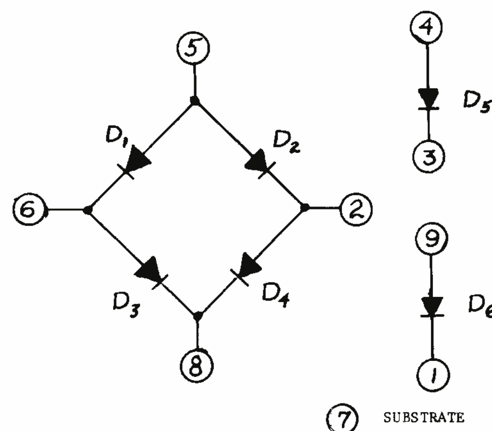


Fig. 2—Circuit diagram and terminal connections for the CA 3019.



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circuit diagrams with the terminal numbers are shown in Figs. 1 and 2. for the CA3018 four-transistor array and the CA3019 diode array, respectively.

Four-Transistor Array (CA3018)

For the CA3018, a common connection is required for two of the devices (Q3 and Q4) to allow the array to be bonded in a TO-5 12-terminal package and still allow a separate connection for the P-substrate (terminal 10). The bonding pads and, therefore, the terminal connections are so chosen as to minimize stray lead compacitance between collector and base by interspacing the emitter lead between the base and collector. The monolithic approach in fabricating four devices has the advantage of producing four nearly identical devices on a single chip.

The applications for the monolithic transistor array CA3018 are nearly as extensive as the applications of an individual transistor and is particularly useful where a large number of active devices are needed in a small space, and component values and circuit needs limit the use of other available integrated circuits. Only a broadband video amplifier application will be discussed and the circuit diagram is shown in Fig. 3. This amplifier consists of essentially two amplifier stages, each made up of a combination of common emitter and common collector configurations (Q1, Q3, and Q4, Q2). DC feedback is applied between terminals 2 and 3 and equal AC and DC feedback is applied between terminals 12 and 5. The output from the common collector Q2 is a low impedance source which is convenient for cascading two of these amplifiers.

The performance characteristics of this amplifier are:

Midfrequency gain	49dB
High frequency bandwidth	32 MHz
Low frequency bandwidth	800 Hz
Tangential sensitivity	20μV
Dynamic range	20 to 11,200μV
Output capability	1V RMS

This circuit configuration only demonstrates a circuit approach using the transistor array and may be altered to suit particular applications.

Six Diode Array (CA3019)

The CA3019 utilizes the six active devices on the chip. Diodes are formed from transistors by connecting the collector to the base which yields the shortest storage time for any of the interconnections for obtaining a diode from a transistor. Four of the diodes are interconnected to form a diode quad and the two remaining diodes have separate connections. This circuit can be mounted in a 10-terminal TO-5 package. The P-substrate is made available separately on terminal 7. The advantage of this circuit configuration is that equal devices are obtained due to the simultaneous fabrication.

A single application — series-shunt gate (Fig. 4)—using the monolithic diode array CA3019 will be discussed, but the circuit can be used for other applications such as balanced modulators, series gates, mixers and ring modulators. All six diodes are utilized and the circuit has the advantages of good off-to-on ratio and low pedestal at the output. Good off-to-on ratio is achieved by providing a low impedance between points A and B by diodes D4 and D6 when quad diodes (D1, D2, D3, D4) are switched off and diodes D5 and D6 are off when the diode quad is on. Successful operation was achieved by floating the substrate (terminal 7) which allowed the circuit to operate without a power supply, but terminal 7 should be connected to a negative supply if a supply is available that is greater than the switching voltage peaks at A and B. If sufficient impedance is available from transformer T1 for the signal frequency V_S then the series resistors R1 and R2 may be omitted.

Fig. 3—Circuit diagram for broadband video amplifier.

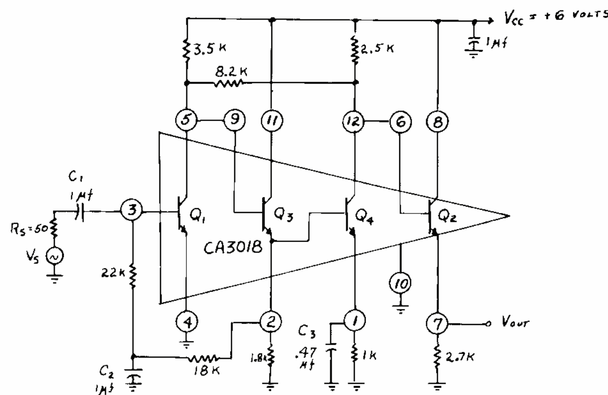


Fig. 4—Series-shunt gate using CA 3019.

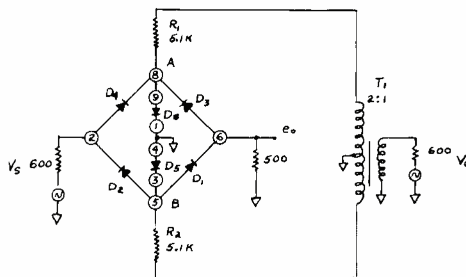


Fig. 5—TA 5227 Double cascode.

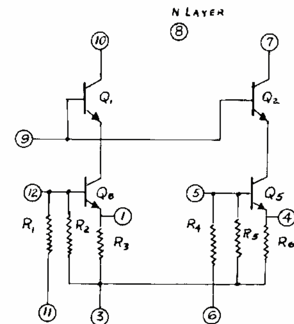
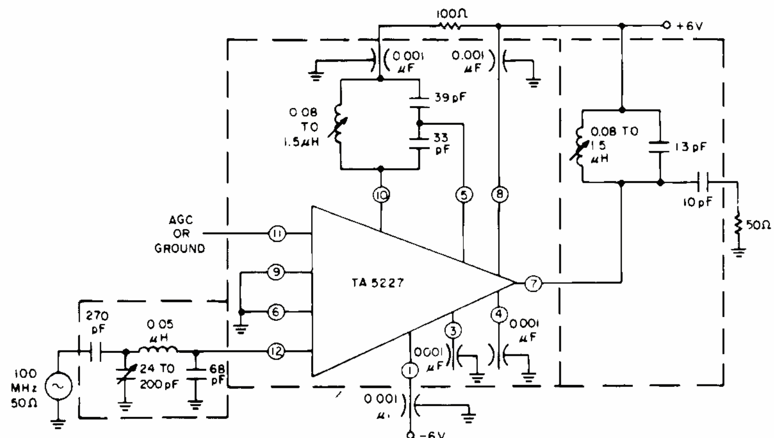


Fig. 6—Circuit diagram of a 100-MHz tuned amplifier using the TA 5227.



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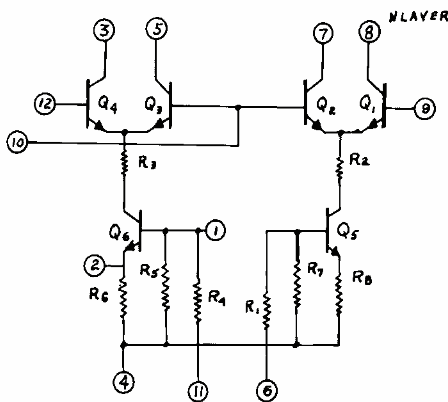


Fig. 7—TA 5226 Multiple differential amplifier.

FOUR-CIRCUIT FAMILY

The four-circuit portion of this family has six active devices and 13 resistors included on a 50x50 mil die. Four of the resistors are of small value and are included for metalization crossovers for the realization of some of the circuits. The transistors are the same as those used in the two circuit family. Each of the four circuits possibilities with this die will be discussed and an application for each will be included. These circuits are all referred to by their development numbers since the decision to make them commercial units is still pending.

Double Cascode Amplifier TA5227

The circuit (Fig. 5) utilizes four active devices and six resistors of the common die. By combining the base electrodes of Q1 and Q2 to common terminal 9 the use of a 12-lead TO-5 package is possible and a separate connection can be maintained for the N-boat isolation are (terminal 8) and for the AGC controls (terminals 11 and 6). Terminals are so chosen to provide interspaced AC ground terminals between signal terminals, thereby, improving isolation.

This circuit is designed for tuned amplifier applications for frequencies up to 100 MHz and the circuit configuration takes advantage of the good isolation obtainable in both the monolithic process and the cascode configuration to obtain relatively high gain on a single die. An application chosen to be discussed for the TA5227 is a narrowband tuned amplifier at a frequency of 100 MHz (Fig. 6). A two supply system was used, but this circuit can be operated from a single supply with the addition of a resistor divider and a bypass capacitor.

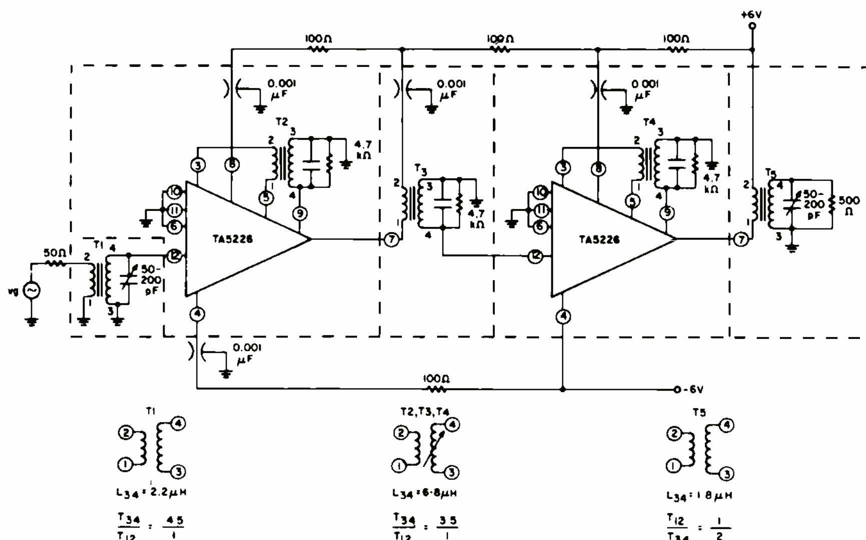
The performance characteristics of this circuit are:

Power dissipation	85mW
Power gain	38dB
3dB bandwidth	400 kHz
AGC range	53dB
Noise figure	8dB

Double Differential Amplifier TA5226

The double differential amplifier, TA5226, utilizes six active devices and eight resistors of the master die. To maintain flexibility and still allow the use of a 12-terminal TO-5 package, internal connections are made and brought out to common terminal 10, and the N+ isolation region and the collector of Q1 are brought out to terminal 8. This permits separating the terminals to which AGC can be applied (terminals 11 and 8) and allows bringing out the base and emitter of transistor Q6 to terminals 1 and 2, respectively. These terminal connections add versatility as the circuit can be used as an oscillator-mixer as well as an amplifier.

Fig. 8—10.7-MHz limiting amplifier with TA 5226 integrated circuits.



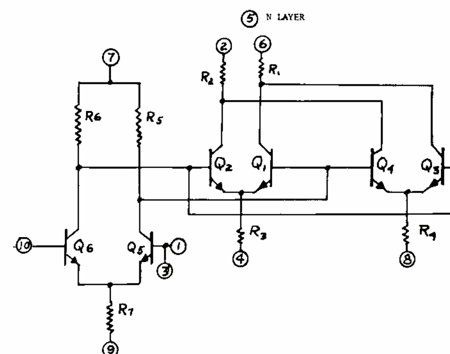


Fig. 9—Circuit diagram and terminal connections for the TA 5224.

An application for the TA5226 is as a 10.7-MHz IF amplifier for limiting use (Fig. 7). The amplifier was designed to give approximately 20DB power gain for each differential amplifier, for a ±6 volts supply. For this application, metal shielding was incorporated as shown in the dotted line in Fig. 8, but it is probable that a conventional shielded-transformer design would operate satisfactorily. The operating characteristics of this circuit for both ±6 and ±4.5-volt supplies are:

	±6 volt	±4.5 volt
Power dissipation (mW)	136	64
Voltage gain (dB)	88	77
Power gain (dB)	77	67
Limiting level (μV RMS)	5.1	7.5
Bandwidth, theoretical (kHz)	600	500
Noise at output (mV RMS)	18	4

Multiplex Modulator TA5224

The multiplex modulator TA5224 utilizes the six active devices and seven of the resistors on the die and can be bonded into a 10-terminal TO-5 package (Fig. 9). Resistors R1, R2, R3, and R4 are included for metalization crossovers. The circuit is interconnected to form three differential pairs. The differential amplifier, transistors Q5 and Q6, processes the carrier drive. A carrier input drive greater than 0.2 volt RMS will provide a square-wave drive to the other pair of differential amplifiers. The emitters of the two differential amplifier pairs made up of transistors Q1, Q2 and Q3, Q4 are transformer driven by the signal frequency and the collectors and interconnected such that the carrier and signal voltage is cancelled at each output (terminals 2 and 6).

A typical application for the TA5224 is as a double-balanced modulator in multiplex equipment (Fig. 10). The carrier is injected at terminal 10 and can be either a square wave or a sine wave. Better performance is obtained with a square wave drive as drive sym-

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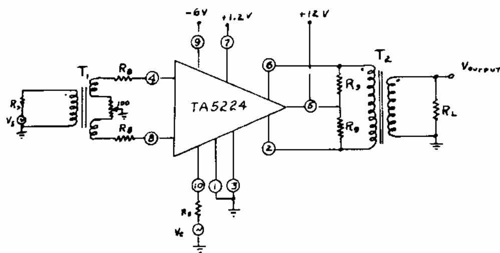

Fig. 10—Typical application for TA 5224.

metry is not affected by slight offsets that can occur in differential pairs made up of transistors Q5 and Q6. The signal is transformer driven (T1) through equal resistors (R8). These resistors must be large enough to provide constant current drive to the emitter of transistors Q1, Q2, Q3, and Q4. A balance potentiometer can be included to reduce carrier leak. The output is transformer coupled to terminals 6 and 2, and the power supply connected to terminal 5 to provide positive bias to the circuit. Some typical performance characteristics with respect to unwanted signals are given below (the 100-ohm balance potentiometer is adjusted for minimum carrier leak).

Frequency (kHz)		dB down from sidebands
C	23	−71
C + V	25	0
C − V	21	0
C + 2V	27	−60
C − 2V	19	−60
2C ± V	48 + 44	−22
2C	46	−54
V	2	−22

Carrier (C): 23 KHz squarewave.
Voice (V): 2 KHz sinewave.

Synthesizer Mixer TA5223

The synthesizer mixer TA5223 utilizes six active devices and ten resistors of the common die and is bonded in a 12-terminal TO-5 package. The circuit interconnection is that of two differential amplifiers and their constant current transistors (Fig. 11). The collector output for the differential pair Q1, Q2 and Q3, Q4 are connected so the balanced push-pull drive on their emitters and bases cancel at each output. Normally, RF signals are applied to the bases of transistors Q1, Q2, Q3, and Q4, and the oscillator is applied to the bases of the constant current transistors Q5 and Q6. If not overdriven, a single differential amplifier is a product mixer, thereby reducing the generation of spurious signals. The linearizing effects of the resistors R8 and R9 insure a current drive to the emitters of each differential pair that is the same as the voltage wave form at terminals 4 and 12. Therefore, for proper drive amplitudes the outputs at terminals 5 and 9 are the desired sum and difference frequencies of the RF and oscillator, with low spurious responses and RF and oscillator frequencies suppressed. Applications for this circuit included mixers, balanced modulators, and product detectors.

The application chosen for the TA5223 is that of a mixer (Fig. 12) with a frequency of 1.0 MHz and an oscillator frequency of 1.7 MHz, with the resulting IF frequency at 0.7 MHz. To evaluate RF and oscillator feedthrough for the circuit alone, transformer T3 could be tuned, in turn, to the oscillator and RF frequencies as well as the IF frequency. The oscillator and RF feedthrough was checked with a fixed RF drive of 6 millivolts from a 50-ohm source and 2 volts RMS of oscillator drive between terminals 4 and 12. The oscillator feedthrough was 9 dB and the RF feedthrough was 13.5 dB below the desired IF. The conversion power gain for this circuit under these conditions was 16 dB and the total power dissipation for a ±6 volt supply was 84 milliwatts. The spurious responses close to the desired RF frequency were measured; the results are shown below:

f_{RF}	f_x (MHz)	dB down with input tuned to f_x
	1.0	0
$2f_o - 3f_x$	.9	−70
$2f_x - f_o$	1.2	−69
$5f_o - 6f_x$	1.3	−70+
$3f_x - 2f_o$	1.366+	−64

Oscillator f_o = 1.7 MHz, 2 volts RMS between terminals 4 and 12
f_{RF} = 1 MHz, 10 millivolts RMS as input reference.

CONCLUSIONS

The approach of providing many circuit possibilities on a common die provides a cost advantage for the monolithic process and a method of coupling high and low volume production circuits types together.

ACKNOWLEDGEMENTS

Acknowledgements go to M. E. Malchow, A. J. Leidich, T. H. Campbell, and R. G. Tipping of DME for their contributions and evaluations, to the Ground Communications Equipment Engineering group of CSD for the circuit design for the TA5224, and to the Integrated Circuit group of SECD for fabrication.

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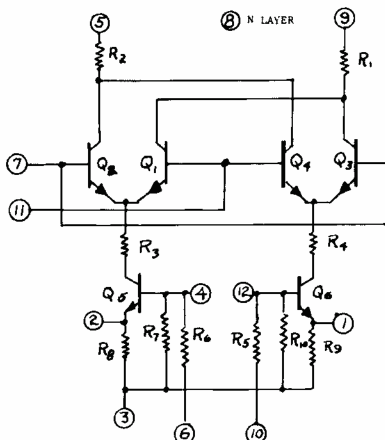

Fig. 11—TA 5223 synthesizer mixer.

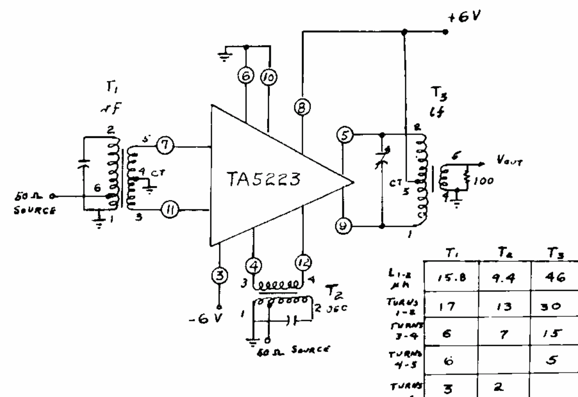

Fig. 12—Mixer using the TA 5223.

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A SURVEY OF HYBRID FILM TECHNIQUES

This paper reviews hybrid film technology, which can be divided into two main areas: thin films and thick films. Both techniques have advantages, and both will find application. The choice of approach should be dictated by the requirements of the specific application. The paper will point out the advantages and disadvantages of both approaches.

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ALTHOUGH great progress has been made in recent years in monolithic integrated circuits, there are many requirements for microelectronic circuits where integrated circuits have not been developed or the complexity required is beyond the state-of-the-art of monolithic circuits. In these areas (e.g., complex digital arrays and linear integrated circuits) hybrid techniques have been used quite successfully. It should be further pointed out that monolithic circuits become most useful and economically feasible when they are used in high volume applications. In cases where small to moderate quantities will be needed (a few thousand circuits), a hybrid technique is a more economical approach with a much quicker turnabout time.

A hybrid circuit contains two or more semiconductor chips on a substrate with either thick- or thin-film resistors; capacitors, and conductors. It is not plagued by the parasitics that may mar the performance of monolithic circuits and requires fewer masks and far less time to make the first unit. Moreover, it is a lot less bulky and more reliable than circuits that are made with discrete components.

THICK VERSUS THIN FILMS

Table I shows some of the advantages and characteristics of each of the two approaches. As can be seen, thin-film techniques offer finer line widths and tighter tolerance components. If the user is going to build a few prototype samples, either technique can be used successfully. When there is a need to produce a few hundred to many thousands of circuits, thick film techniques offer the advantage of substantially lower costs.

THICK-FILM TECHNOLOGY

Thick films are layers of resistive, dielectric, and conductive inks that are deposited on a substrate. The deposition process, similar to graphic silk-screening, employs a fine mesh screen to hold the pattern for the components that are to be deposited. The pattern is produced by photographic means, and wherever the inks are not to be deposited, the holes in the mesh are blocked by an emulsion.

Substrates, usually ceramic, are cleaned and then screened with conductive inks to provide the first pattern, providing the conductor pattern, terminal points, bonding pads, and the bottom plates of capacitors, if necessary. A second screening provides the resistor elements. If capacitors are included in the circuit, a third and fourth screening must be performed: one for the dielectric material, the other for the second capacitor plate.

After each screening, the substrate is first air-dried. The substrates are then fired in a high temperature kiln. Afterwards, the components can be measured and trimmed by an abrasive technique to bring them into tolerance. The substrate can then be dip soldered and finally discrete components or integrated circuits can be attached. After final circuit testing, the units are ready for encapsulation or other packaging. This essentially covers the various fabrication steps in a thick-film process.

Conductors

Various materials are available for screened conductors. The most common are gold-platinum, gold-palladium and silver-palladium. These materials are readily available and can be screened to yield a resistance of 0.01 ohms per square. At present, most conductors are screened to a line width of 0.010 inches on 0.010 spacing, but 0.005 inch line widths have been achieved in the laboratory using routine methods. Recently developed inks that are becoming available were designed specifically for fine-line printing have resulted in 0.002 line widths on 0.005 spacing.

Resistors

Various resistor materials are available which have a resistance range from 500 ohms per square to 20,000 ohms per square. These inks are manufactured and sold with minimal electrical specifi-

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M. L. TOPFER received the BS in Physics from Brooklyn College in 1959. Since that time he has completed the graduate course work toward the PhD in Physics at the Polytechnic Institute of Brooklyn. In addition, he has taken courses in Industrial Management. From 1959 to 1961, Mr. Topfer was engaged in the design and development of germanium alloy junction transistors, for both low frequency and high frequency application. In 1961, he joined the research division of Kollsman Instrument Corporation as a research physicist. At Kollsman he led a group working on the development of silicon planar photovoltaic diodes. In 1962, Mr. Topfer joined RCA Research Laboratories at Princeton, New Jersey, as a member of the Technical Staff. Since that time he has been investigating thin-film approaches to microelectronics in the areas of thin-film organic diodes and thin-film transistors. In particular, he has been responsible for the development of tellurium thin-film transistors in RCA, in which he made many fundamental improvements and innovations. In 1965, he was given the added responsibility for thin-film transistors reliability and performance at the RCA Research Laboratories. In March, 1966, Mr. Topfer joined the Defense Microelectronics Thin-Film Laboratory as a Leader in charge of thin-film active device research. He is responsible for programs in thin-film components, thin-film transistors and photosensitive devices, thin-film circuits, and packaging techniques. In September, 1966, Mr. Topfer was given the added responsibility of establishing a thick-film techniques group. This group will work on techniques to advance the state-of-art of thick film circuits. Mr. Topfer has presented many papers on various phases of microelectronics and has submitted several patent applications pertaining to thin-film devices. He is a member of the American Physical Society, American Vacuum Society, the Electro-chemical Society, the Institute of Electrical and Electronic Engineers, and the Thin-Film Division of the American Vacuum Society.

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cations. When these resistor inks are received, they must be blended to the desired value. The conduction mechanism of the palladium-silver frit-fired composition, most commonly used, is not fully understood. It is complicated by the many constituents (palladium, silver, boron, lead, silicon, platinum, sodium, cadmium, gold) and possible intermetallic compounds and doping effects formed during the firing process. Within a specified range of sheet resistivities and firing temperatures, there is evidence that the formation of palladium oxide controls the conductive process: Pd + Ag + glass frit $\xrightarrow[780^\circ C]{}$ PdAg + PdO + Pd + glass frit. By varying the glass concentration in the resistive composition and/or firing process, a resistor having varied conductive mechanisms can be obtained with the processed materials so that widely varying, yet closely controlled, electrical properties can result. After screening, the resistors can be trimmed to ±0.5%. The characteristics of these resistor materials are given in Table II.

Insulators

Only recently have insulator inks become available. These inks are experimental and little or no information is available about them. Some of the characteristics of these materials that have been reported are listed in Table III.

THIN-FILM TECHNOLOGY

In place of the thick-film techniques described above, many people are using thin-film techniques. This technique offers finer line width and passive components of tighter tolerance without trimming. In this technique, the materials are deposited by either vapor deposition in high vacuum or by the use of sputtering techniques. The films can be deposited through metal masks, or photoresist and etching techniques can be used to define the patterns. The disadvantages of thin-film techniques are the necessity of precise control of the deposition of the films, the need for heating the substrate to achieve good adhesion, and the difficulties in masking techniques.

Conductors

The most commonly used material is aluminum. This material can be deposited to a thickness of 3000 to 4000 Angstroms which will result in a resistance of 0.1 ohms per square. Many of the materials, such as molybdenum, gold, and palladium have been investigated yielding similar results. Conductors as fine as 0.0005 inch line widths on 0.0005 inch spacing can be deposited using photoresist techniques.

Resistors

Precision thin-film resistors can be deposited using the techniques described above yielding initial tolerances of ±5%. The most common materials used are nichrome, cermets, and the valve metals such as tantalum and hafnium.[1] The valve metals have found useful application in precision RC networks. The characteristics of the materials are given in Table II.

Insulators

Thin-film capacitors can also be made to reasonable tolerance using materials such as silicon monoxide and the oxides of the valve metals. The characteristics of these materials are given in Table III. While large capacitors are theoretically practical using these materials, the values of a capacitor that is reasonable is up to about 150,000 picofarads. Larger capacitors will lead to serious problems of pinholes in the film. This value is for the valve metals. For the other capacitor materials, the value is substantially lower.

PACKAGING TECHNIQUES

After the passive components and interconnections have been formed using either thick or thin films, active elements must be added. Most hybrid manufacturers are attaching micropackaged active elements to the circuits. A great deal of research is being carried out to improve these packaging techniques.

Many companies are mounting DC probed chips to the circuits and then using wire bonding techniques to interconnect them. But this does not work too well when fabricating analog circuits. In this case, more detailed measurements must be made on the active elements. The use of ceramic carriers is finding wide use for providing the ability to do more detailed testing of the active chip before attaching to the circuit.

The area receiving most attention is techniques for flip-chip mounting active elements to the circuits. In this case, bumps are formed on the active device, or circuit. These bumps are used to mount the chip to the circuit in an inverted fashion. This eliminates the wire bonding step and acts as the chip-mounting vehicle.

CONCLUSION

The characteristics of the various materials used in both thin- and thick-film hybrid circuits are outlined in this paper. In addition to the investigations being carried out into new materials, a great deal of research is being done on techniques for attaching active elements and fine-line screening of thick-film inks. Many companies are investigating techniques for flip-chip mounting of both transistors and integrated circuits to thin- and thick-film circuits. As pointed out in the introduction, both thin- and thick-film techniques will find application. The choice of approach should be dictated by the requirements of the specific application.

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TABLE I — Comparison of Thick and Thin Films

Circuit Requirements	*Thick Film*	*Thin Film*
Mass Producible	Lower Cost	Higher Cost
Initial Tolerance	± 10%	± 5%
Matching	± 1%	± 0.1%
Trimming Tolerance	± 1% (easily)	± .1% (valve metals)
Temperature Coefficient	± 200 ppm/°C	<50 ppm/°C
Power Handling	50 W/in²	15 W/in²
Line Width	10 mils ± 2 mils	0.5 mils ± 0.02 mils
Resistivities	.05 ohm/sq to 20k ohm/sq	0.1 ohm/sq to 1k ohm/sq

TABLE II — Resistor Characteristics

Characteristic	*Thick Film*	*Cermet*	*Nichrome*	*Tantalum*	*Hafnium*	*Silicon Diffused*
Resistivity	1 to 20k	10 to 10k	25 to 300	25 to 300	100 to 3k	100 to 300
Initial Tolerance	± 10%	± 5%	± 5%	± 5%	± 5%	± 20%
Trimming Tolerance	± 1%	± 1%	± 1%	± 0.2%	± 0.05%	—
TCR (ppm/°C)	± 400	± 300	± 50	+ 100 — 200	+ 100 — 300	+ 2000
Power (W/in²) Rating	50	15	15	15	15	15

TABLE III — Capacitor Characteristics

Characteristic	*Thick Film*	*SiO*	10 to 1,000,000	*Tantalum*
Cap/Area (pf/in²)	10 to 70,000	10 to 25,000	>100	10 to 3,000,000
Rated Voltage	>100	>10	250 ppm	>100
Temperature Coefficient	300 ppm	100 ppm	1%	*Hafnium*
Dissipation Factor	<1%	1%	± 10%	125 ppm
Initial Tolerance	± 15%	± 5-10%	± 5-10%	<1%

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THIN-FILM HAFNIUM COMPONENTS FOR PRECISION NETWORKS

Thin-film hafnium and hafnium dioxide have been investigated for the fabrication of thin-film precision resistors and capacitors to be used in microminiaturized precision filter networks. The metallic hafnium film is deposited by cathodic sputtering. Photolithographic etching techniques are used to create the component and circuit pattern. Anodic oxidation allows the formation of dielectric films of hafnium dioxide for thin-film capacitors and the adjustment of thin-film resistors to precision values (±0.01%). Thin-film capacitors and resistors have a stability between 0.1% and 0.01% after annealing. Thin-film twin-T filters have been built in the audio frequency range.

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Special Fabrication Techniques Group
Defense Microelectronics, Somerville, N. J.

METALLIC films of hafnium and anodic oxide films of hafnium can be used in two major areas of microminiaturization.[1] The high precision and stability of thin-film resistors and capacitors (attainable with hafnium-hafnium dioxide films) are specifically of interest in the fabrication of precision networks, such as twin-T[2] and active RC filter networks. A second area of using films of hafnium is gate insulators in MOS transistors[1] in silicon integrated technology.

In the first area, a passive substrate, such as glass or glazed ceramic, is most frequently used. Size of the final circuit is of secondary importance in this application to the precision, stability, and ability to tune the filter network.[2] A number of properties make the hafnium-hafnium dioxide technology more attractive for this application than other technologies, such as the thin-film tantalum technology.[3,4,5]

First, hafnium films offer the advantage that the circuit pattern can easily be formed by etching the hafnium film with diluted hydrofluoric acid (1% to 2% concentration) without attacking the substrate (glass, glazed ceramic, or silicon-silicon dioxide) or the KPR masking material. In addition, the same starting material (hafnium) is used for the fabrication of thin-film resistors as well as thin-film capacitors in the hafnium-hafnium dioxide technology; while in the thin-film tantalum technology, tantalum films are used for capacitors and tantalum nitride films are used for resistors.

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When initial films of proper thickness are selected, the hafnium films are thick enough to form the bottom electrode and the dielectric layer of the capacitor after anodization. In experiments on twin-T filters, a forming voltage of 40 volts was selected for the formation of the dielectric hafnium dioxide film. The resistive elements are formed by anodizing at higher voltages, thus reducing the thickness of the hafnium metal films to such a degree that the hafnium-hafnium dioxide film represents a resistive film of several hundred ohms per square. It is feasible that the thickness of these resistive films can be adjusted in such a way that compensation of the positive temperature coefficient of the capacitors (+125 ppm/°C)[6] can be accomplished by an equally large negative TCR.

In addition, thin-film hafnium-hafnium dioxide capacitors are practically nonpolar and exhibit high breakdown strength of the oxide film in both forward and backward directions. The high temperature stability of the hafnium dioxide represents another advantage. The significance of the large sputtering rate which is obtainable with hafnium has not yet been fully examined with respect to the performance characteristics of the various devices. It is believed, however, that films with a higher purity can be obtained, a fact which will most likely improve the physical properties of the components.

These advantages are true not only for passive networks but also for hafnium-hafnium dioxide films utilized in silicon integrated circuits. The large dielectric constant (compared to silicon dioxide) and the high breakdown strength of anodically formed oxide films are the main advantages of gate insulators in MOS transistors[1] of hafnium dioxide.

EXPERIMENTAL RESULTS

Cathodic Sputtering of Hafnium

The deposition of the hafnium films is performed in a sputtering system with vertical arrangement of the electrodes. In the original system, the electrodes

Fig. 1—Cathodic sputtering arrangement with hexagonally shaped substrate holder.

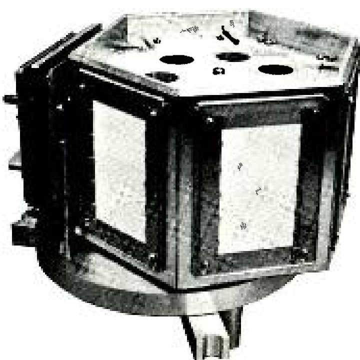


Fig. 2—Rate of cathodic sputtering of hafnium films.

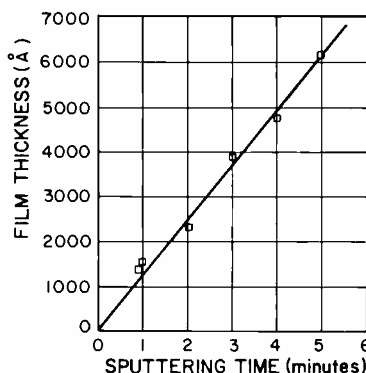
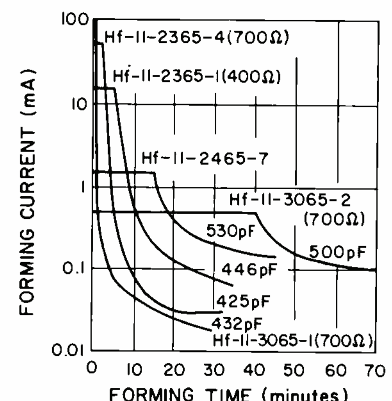


Fig. 3—Decrease of forming current for different initial current densities (forming voltage 200 V_f).



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were placed in horizontal position[6] with the hafnium cathode representing the upper electrode. Dust particles settling on the substrates created pinholes in the metal film.

The horizontal arrangement of the new sputtering system (Fig. 1) offers a number of additional advantages. The anode or substrate holder is hexagonal and has six planes equipped to carry substrates. Rotating this substrate holder around its vertical axis allows a large number of substrates to be coated in one pump-down without breaking the vacuum. This is significant because the cathode is cleaned for 60 minutes by presputtering at the beginning of each pump-down of the vacuum system. The sputtering rate of the hafnium can be greatly increased using this extended cleaning cycle.

Both the sputtering rate and the uniformity of film thickness are determined by measuring the film thickness using the Tolansky multiple-beam interference method.[7] A deposition rate of 1200 Angstroms/min is obtained on a number of films (Fig. 2). The sputtering is performed at a bias of 2800 volts, at a measured pressure of 50 microns of Hg, and a cathode-to-anode distance of about one inch. Argon gas is introduced at a slow rate into the vacuum system. The sputtering rate depends strongly on the cleanliness of the vacuum system and the hafnium cathode. For example, the deposition rate is only 330 Angstroms/min[6] with a cleaning cycle of 15 minutes. The uniformity of film thickness obtained with the new sputtering system is ±2% or better over the 3x5-inch substrate area with a cathode of 6x6-inch size, and ±1% over a 1x1-inch substrate area.

Pattern Generation

The pattern generation of thin-film hafnium devices and circuits can easily be accomplished by photolithographic techniques. Diluted hydrofluoric acid (1% to 2%) etches hafnium without difficulty and doesn't attack the KPR masking material or the substrates. This fact is important when fabricating gate insulators of hafnium dioxide in MOS transistors. These insulators are only a few tenths of a mil wide and cover the channel whose width is only 0.0003 inch. It is important also that the etching solution does not attack the passivating silicon dioxide layer deposited over the silicon substrate.

Other masking techniques, such as using mechanical masks during the sputtering process, have been studied, but have not been found to be as reliable and simple as the KPR etching technique.

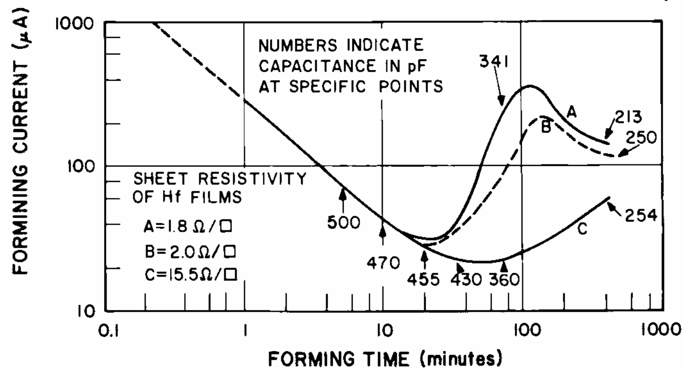
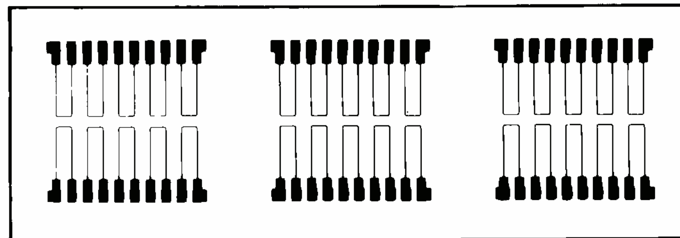


Fig. 4—Anodization of hafnium films as a function of sheet resistivity.

Fig. 5—Thin-film hafnium-hafnium dioxide test resistors.



Mechanical masks, either of metal or glass, limit the resolution and linewidth of the hafnium pattern and adversely affect the uniformity of the sputtering rate and film thickness. In addition, this mechanical masking technique reduces the flexibility of creating patterns of different configurations; it would be extremely difficult to create patterns such as the gate insulators in MOS transistors. The heating of substrate and mask during the sputtering process would have the minimum effect of a misalignment of the pattern.

Anodic Oxidation of Hafnium

Most of the hafnium films have been anodized by wet anodization in an electrolyte consisting of equal parts per volume of ethylene glycol and a saturated aqueous solution of oxalic acid. However, some of the films have been anodized by plasma anodization in a vacuum system, so that both anodization techniques could be compared.

One part of the investigation was concerned with the influence of forming conditions on the electrical properties of thin-film hafnium-hafnium dioxide capacitors. In the first series of experiments, different current densities were used for the wet anodization. A current density of 0.5 mA/cm^2 required 40 minutes to reach the desired forming voltage of 200 volts. In the following 30 minutes, the leakage current decreased to only 100 μA/cm.^{2} Fig. 3 shows the forming characteristics for different initial forming currents. Generally, after 30 minutes, the leakage curent is smaller for a larger initial forming current density. In the extreme case, where the full forming voltage was applied directly to the hafnium film, a strong decrease in the forming current was observed. Current densities of a few μA/cm^2 were obtained in a few minutes.

In another series of experiments, thin films of hafnium with different sheet resistivities were used for the fabrication of thin-film test capacitors. The sheet resistivities were 1.8, 2.0, and 15.5 ohms per square. During the first 20 minutes, the forming current decreased uniformly as shown in Fig. 4. After 20 to 30 minutes, the leakage current started to increase again for hafnium films with a sheet resistivity of 1.8 or 2.0 ohms per square; the maximum leakage current was reached after about 120 minutes. Thereafter, the leakage current decreased again to about 100 μA/cm.^{2}

The hafnium film with a sheet resistivity of 15.5 ohms per square anodized in a somewhat different manner. The minimum leakage current was obtained after about 60 minutes of anodization; the forming current increased during the next 340 minutes without reaching a maximum during the test period of 400 minutes.

Plasmionic anodization is somewhat analogous to the wet-anodization process. An oxygen glow discharge maintained in

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DR. FRANZ HUBER received the M.S. in physics and Ph.D. in physical chemistry from the University of Munich in 1955 and 1957, respectively. Until 1960 Dr. Huber was in the Research Division of Philco as Project Scientist involved in studies on the deposition of dielectric films for passive components, such as anodic oxidation and flash evaporation. From 1960 to 1964 he was responsible for the research activities in thin film microminiaturization at the Research Division of Republic Aviation Corporation. At this time he introduced anodic oxide films in the fabrication of thin film field effect devices and studied the rectification phenomena in anodic oxide films. In 1964 Dr. Huber joined RCA's Defense Microelectronics Activity in Somerville as Staff Scientist and initiated the thin film hafnium technology to be used for precision RC filter networks and hybrid circuits. In 1965 he was promoted to Leader to assume the additional responsibilities of the Solid State Laboratory of CSD in New York. At the present time Dr. Huber is leading a group on Special Fabrication Techniques for Microelectronics involved in work on precision filter networks, thick film field effect transistors, photosensitive arrays and precision silk screening techniques. Dr. Huber has been awarded several patents and is author of some 40 scientific publications, presentations, and lectures. He is known for his original work on anodic oxide films and has received the best paper award from the Electronic Components Conference for his paper on "Thin Film Hafnium-Hafnium Dioxide Capacitors."

a vacuum system provides oxygen ions for the anodization of the valve metal which is positively biased. The anodization, however, is usually limited to small forming voltages[8] and is very time consuming. It was found that the thickness of the oxide film, or at least the measured capacitance value, is not as voltage dependent (forming voltage) as in the case of wet-anodized oxide films. At low forming voltages (up to 60 volts), there is relatively good agreement with wet-anodized hafnium dioxide capacitors. Qualitative agreement was also found in wet- and plasmionically-formed titanium dioxide films for low forming voltages.[9] Both oxide films show pronounced rectification of the electrical current when the counter electrode evaporated over the oxide film consisted of platinum or palladium.[10,11]

In addition to adjusting the resistors to precision values, the anodization creates a protective coating over the remaining metal film, thus contributing to the stability of the thin-film resistors.

THIN-FILM RESISTORS

Fabrication

The pattern of thin-film test resistors (Fig. 5) has been etched by photolithographic techniques using the method described previously. A test slide (1x3 inches) contains three groups with ten test resistors each. Nichrome-seeded gold films are evaporated at the end of the contact areas to establish reliable, good ohmic contact every time. The pattern of one test group is 0.7x0.7 inch. When substrates of the same size are used. the test resistors can be packaged in 1x1-inch flat packages for extensive life testing.

Temperature Coefficient of Resistance

For a number of test resistors with various sheet resistivities, the temperature coefficient of resistance (TCR) has been measured; Fig. 6 shows the measurements for resistors with a sheet resistivity of 15 ohms per square. Up to 400°C, the temperature coefficient is usually small. At higher temperatures, larger changes of the resistance values take place.

Fig. 7 shows the temperature coefficient of resistance as a function of sheet resistivity. Thick films (low sheet resistivity) exhibit a positive temperature coefficient of resistance (up to about +100 ppm/°C). With increasing sheet resistivity, the TCR becomes smaller and then becomes negative. Thin-film hafnium-hafnium dioxide resistors with a sheet resistivity of 2000 ohms per square have a negative TCR of about −300 ppm/°C.

Stability

The fabrication and stability of thin-film hafnium-hafnium dioxide resistors was most extensively investigated on resistors with a sheet resistivity between 100 ohms per square and 500 ohms per square. Thin-film resistors with a negative temperature coefficient of resistance of about −125 ppm/°C are of specific interest for the compensation of a positive temperature coefficient of capacitance of about +125 ppm/°C in RC networks such as twin-T filters.

Fig. 8 shows a typical measurement on the stability of a resistor of 80 ohms per square which has been heat cycled between room temperature and approximately +300°C. Starting value of this resistor was 8994 ohms. After exposure to 300°C, the room temperature value of this resistor was 8995 ohms (stability 0.01%).

A number of test resistors were exposed to life tests at +125°C and their stability was investigated over 600 hours. These resistors were annealed at 250°C for 30 minutes before the anodization for a sheet resistivity of 200 ohms per square. Table I shows the experimental results on resistors exposed to +125°C and measured at room temperature.

Fig. 6—Temperature coefficient of resistance of thin-film hafnium-hafnium dioxide resistors (15 ohms/square).

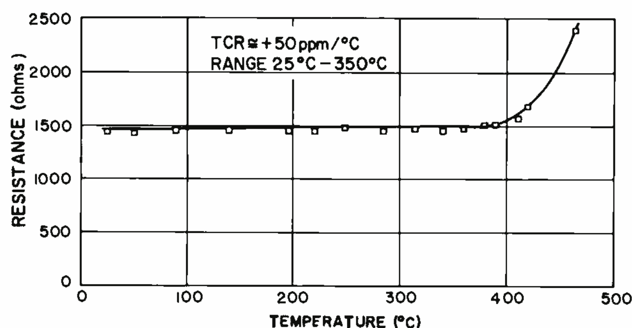
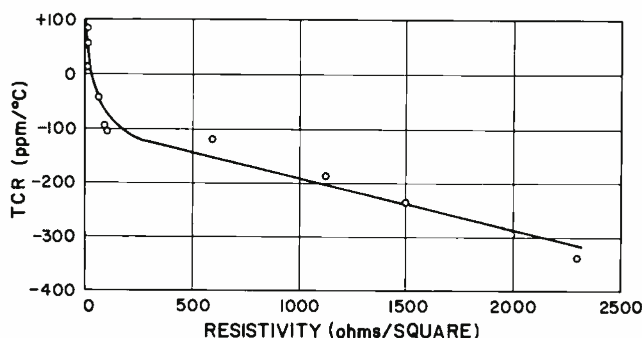


Fig. 7—Temperature coefficient of resistance of thin-film hafnium-hafnium dioxide resistors as a function of sheet resistivity.



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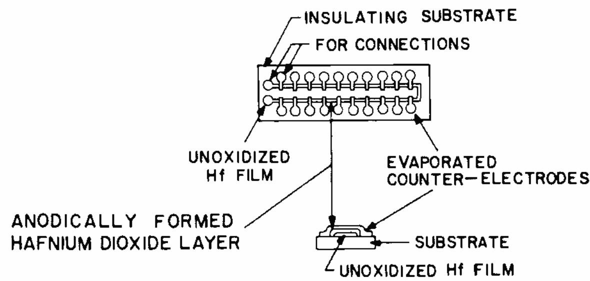


Fig. 9—Thin-film hafnium-hafnium dioxide test capacitors.

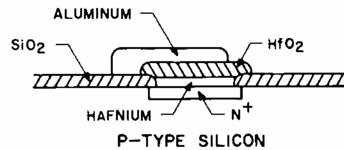


Fig. 10—Schematic of thin film hafnium-hafnium dioxide capacitor on solicon substrate.

TABLE I — No Load Life Test Data of Hafnium-Hafnium Dioxide Resistors at +125°C

Initial Resistance (Ω)	After 600 Hours of Test R (Ω)	ΔR (Ω)	ΔR (%)
20,001	20,004	+ 3	0.015
20,003	20,013	+10	0.050
20,004	20,006	+ 2	0.010
20,003	20,009	+ 6	0.030
20,002	20,009	+ 7	0.035
20,004	20,008	+ 4	0.020

THIN-FILM CAPACITORS

Fabrication

Thin-film hafnium-hafnium dioxide capacitors have been deposited on a number of different substrates. The passive substrates consist of glass (Corning 7059) and glazed ceramic. These substrates, 1x1-inch, contain 20 test capacitors (Fig. 9). Each capacitor is 0.01 cm^2 (1600 mil^2). A number of different structures can be fabricated with silicon as substrate specifically for the determination of the high frequency properties of hafnium-hafnium dioxide capacitors (Fig. 10). The simplest case is the utilization of a silicon substrate coated with a thick passivating layer of silicon dioxide which can be grown by any standard technique. In this approach, the silicon acts as a passive substrate, and the experimental results are analogous to those obtained with glass or glazed ceramic substrates. The pattern of the hafnium film is generated by photolithographic methods and the hafnium is etched with diluted HF acid.

The hafnium films have been anodized both in an electrolyte as mentioned previously and by the application of the full forming voltage at the beginning of the anodization process. After a 30-minute anodization, hafnium-hafnium dioxide capacitors with good reproducibility can be obtained if the anodization temperature and other processing parameters are maintained constant. Fig. 4 shows the effect of forming time on the final capacitance values for different hafnium films.

Forming Voltage

As mentioned previously, hafnium oxide films have also been formed by plasmionic anodization, and thin-film capacitors have been fabricated (Fig. 11). Table II shows the capacitance values as a function of forming voltage for wet and plasmionically anodized hafnium-hafnium dioxide capacitors. The range of forming voltage is limited for the plasmionic anodization process compared to the wet anodization process. Using the latter process, thin-film capacitors with forming voltages up to 300 volts have been fabricated successfully.

TABLE II—Capacitance as a Function of Forming Voltage

Forming Voltage (V_f)	Capacitance: Wet Anodization ($\mu F/inch^2$)	Capacitance: Plasma Anodization ($\mu F/inch^2$)
10	3.48	3.50
20	2.06	1.67
30	1.49	1.35
40	1.03	1.220
60	0.775	0.775
70	0.650	—
85	—	0.615
90	0.535	—
100	0.470	0.775
130	0.400	0.710
150	0.360	—
200	0.280	—
300	0.167	—

The capacitance values obtained with these thin-film hafnium-hafnium dioxide capacitors on silicon substrates agree practically with those obtained on passive substrates when the same anodization procedures are applied.

Leakage Current

The leakage current of some of these capacitors is shown in Fig. 12. These I-V characteristics demonstrate that these thin-film hafnium-hafnium dioxide capacitors are non-polar for practical purposes. The values of the insulation resistance agree well with data from equivalent thin-film hafnium-hafnium dioxide capacitors deposited on glass or ceramic substrates, although the counter-electrodes were not applied by evaporation of aluminum through mechanical masks, but were etched from a continuous layer of aluminum evaporated over the entire silicon wafer and then formed by means of KPR masking and etching techniques.

It seems that forming the counter-electrode by etching from a continuous film does not reduce the breakdown strength of the anodic oxide film. These capacitors exhibit about the same breakdown voltage as equivalently made hafnium-hafnium dioxide capacitors on glass substrates.

Fig. 11—Capacitance as a function of forming voltage (wet and plasma anodization of hafnium).

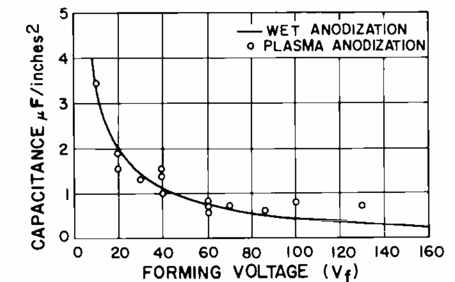


Fig. 12—I-V characteristics of thin-film hafnium-hafnium dioxide capacitor (silicon substrate).

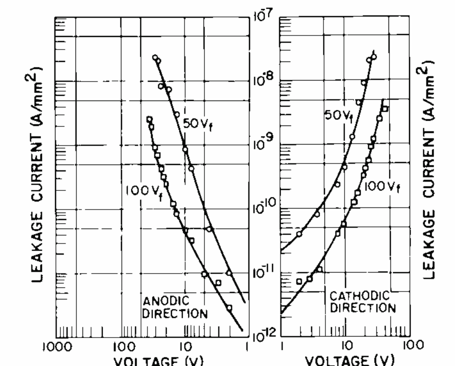
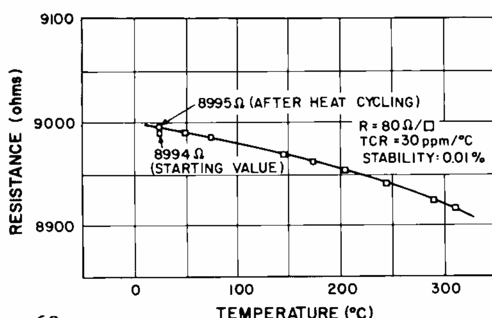


Fig. 8—Stability test of thin-film hafnium-hafnium dioxide resistor.



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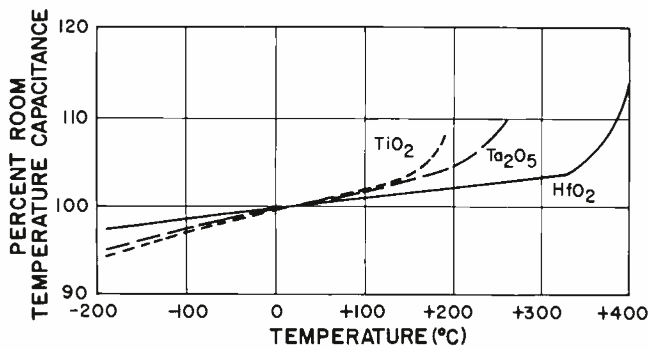

Fig. 13—Temperature dependence of capacitance of thin-film hafnium-hafnium dioxide capacitor.

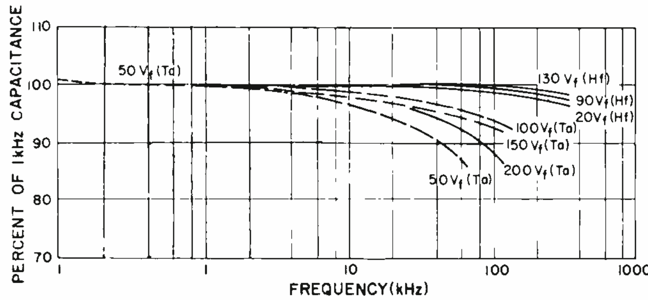

Fig. 14—Capacitance-frequency relationship of thin-film hafnium and tantalum capacitors.

TABLE III—Breakdown Voltages of Thin-Film Hafnium-Hafnium Dioxide Capacitors

Forming Voltage (V_f)	Breakdown Voltage (V_B)	
	Aluminum	Gold
40	30	35
	45	35
	25	
70	60	90
	55	80
	60	80
	65	90
		60
		80
		70
		80
90	110	150
	105	125
	110	125
	108	120
	120	90
	110	
	70	
130	150	180
	180	180
	160	160
	140	155
150	110	100
	130	200

Breakdown Voltage

A number of thin-film hafnium-hafnium dioxide capacitors were tested with respect to their breakdown characteristics. Two types of counter-electrodes (aluminum and gold) were applied to the hafnium dioxide layer by evaporation through mechanical masks. Capacitors were tested with forming voltages ranging from 40 to 150 volts. The test results showed that the breakdown strength exceeded the forming voltage by almost 50%, and breakdown voltages up to 200 volts were measured on hafnium films formed to 150 volts. The breakdown voltages were measured with a Tektronix Transistor Curve Tracer, Model 575, with the hafnium film at the positive bias (anodic direction). These measurements are listed in Table III.

Temperature Coefficient of Capacitance

Thin-film hafnium-hafnium dioxide capacitors exhibit a low temperature coefficient of capacitance over a large temperature range. Fig. 13 shows the capacitance as a function of temperature from liquid nitrogen temperature (−196°C) to over +400°C. Up to about 350°C, the TCC is about +125 ppm/°C. Over a smaller temperature range (−55°C to +125°C), the TCC is approximately +100 ppm/°C. The temperature dependence of thin-film tantalum and titanium capacitors[12] are shown for comparison. It is noted that, at about 250°C, the capacitance of tantalum capacitors starts to increase with temperature in a more pronounced way.

Frequency Dependence

The frequency dependence of a number of thin-film hafnium-hafnium dioxide capacitors has been measured up to 300 kHz. The forming voltages varied from 20 to 130 volts. According to present results, it appears that the thin-film hafnium capacitors produced with a larger forming voltage are less affected by the frequency than those made with lower forming voltages. Fig. 14 shows the capacitance-frequency relationship of thin-film hafnium-hafnium dioxide capacitors for various forming voltages. Corresponding results for thin-film tantalum capacitors are shown for comparison, as reported in the literature. There is a noted difference in the frequency dependence btween the two materials. Fig. 15 shows the measurements of Q as a function of frequency up to 200 MHz of a hafnium-hafnium dioxide capacitor with low-resistive silicon as substrate. These capacitors were mounted in TO-5 cans after the silicon wafer had been diced to form individual capacitors.

The dissipation factor is somewhat more affected at higher frequencies. At 1 kHz the dissipation factor is frequently 1% or smaller, but increases to several percent at 100 kHz.

Fig. 15—The Q of thin-film hafnium-hafnium dioxide capacitors as a function of frequency.

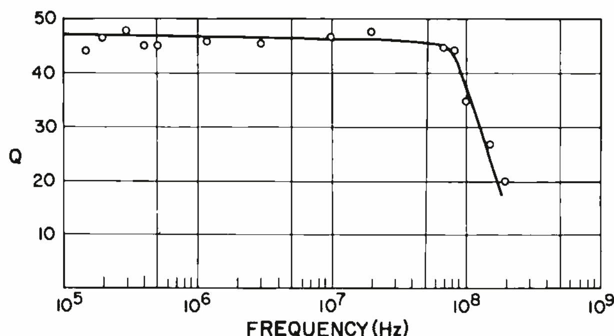

Fig. 16—Thin-film twin-T notch filter circuit.

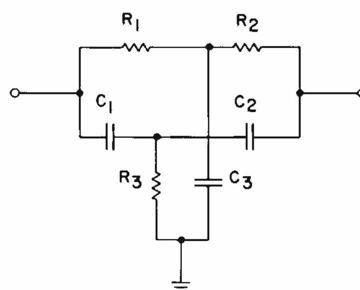

Fig. 17—Hafnium pattern after etching.

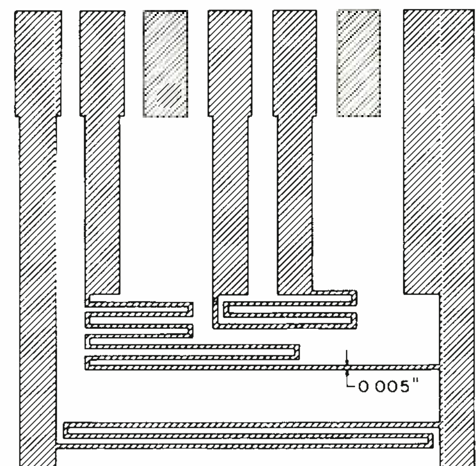

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TABLE IV—Life Test Data of Hafnium-Hafnium Dioxide* Capacitors at +125°C

Test Voltage	+25°C		+125°C								
			Initial Value		312 Hours			650 Hours			
(Vdc)	C (pF)	DF	C (pF)	DF	C (pF)	ΔC (%)	DF	C (pF)	ΔC (%)	DF	TCC (ppm/°C)
40	501	0.015	506	0.009	507	+0.2	0.008	509	+0.6	0.008	+100
40	526	0.007	530	0.009	532	+0.4	0.007	535	+1.0	0.008	+ 80
40	532	0.007	534	0.014	536	+0.4	0.007	537	+0.6	0.008	+ 37
0	526	0.007	530	0.009	531	+0.2	0.009	534	+0.8	0.008	+ 80
0	522	0.007	528	0.008	530	+0.4	0.008	533	+1.0	0.008	+115
0	533	0.007	537	0.010	540	+0.5	0.009	543	+1.1	0.008	+ 80

*Hafnium dioxide prepared by wet anodization at 200 volts.

Life Tests and Stability

Some of the thin-film hafnium-hafnium dioxide capacitors anodized to 200 volts in the electrolyte described previously have been subjected to life tests at elevated temperatures. The life tests were performed at +125°C with 40 volts and without voltage applied to the capacitors. Table IV lists the results of some of the capacitors tested.

The last column gives the temperature coefficient of the capacitors over the temperature range from +25°C to +125°C. The temperature coefficient varies from +37 ppm/°C to +115 ppm/°C. At the present time, the tests have been performed over a period of 650 hours.

THIN-FILM TWIN-T NOTCH FILTER

For the fabrication of the thin-film twin-T notch filter (Fig. 16), thin-film components of hafnium and hafnium dioxide were employed. Ceramic substrates (0.7x0.7-inch) were coated with a continuous hafnium film by sputtering for four minutes. The pattern of the circuit (Fig. 17) was arranged in such a way that, by partial immersion of the substrate into the electrolyte, the various sections of the oxide could be formed. After contacts consisting of chromium-seeded gold had been deposited, the entire hafnium pattern was anodized to a forming voltage of 40 volts to create the dielectric layer for the thin-film capacitors. When only the lower section of the wafer is immersed into the electrolyte, the various resistors (R_1, R_2, and R_3) can be adjusted to the desired resistance values by selecting the proper contacts and forming voltages. The forming voltage for the adjustment of these resistors is larger than 40 volts (100 to 200 volts depending on desired resistance values) so that, for the formation of the thin-film capacitors, the total hafnium film can be anodized to 40 volts without adverse effects. Finally, counter-electrodes of aluminum or gold are evaporated over the indicated areas to complete the thin-film capacitors and thin-film twin-T notch filter (Fig. 18).

The no-load frequency response curve of such a thin-film hafnium-hafnium dioxide twin-T filter is shown in Fig. 18. The resistors had been originally adjusted to 1535.9 ohms, 1534.8 ohms and 788.0 ohms, respectively, and the capacitors had values of 4000 pF and 8000 pF, respectively. Without special tuning of this filter, a notch depth of about 50 dB has been obtained at a frequency of 31,230 Hz. By using hafnium-hafnium dioxide resistors of equal and opposite temperature coefficient to the TCC of the thin-film hafnium-hafnium dioxide capacitors, one can obtain extremely low temperature coefficients of the notch frequency, and filters with temperature coefficients smaller than 50 ppm/°C have been obtained.

Fig. 18—Twin-T filter circuit.

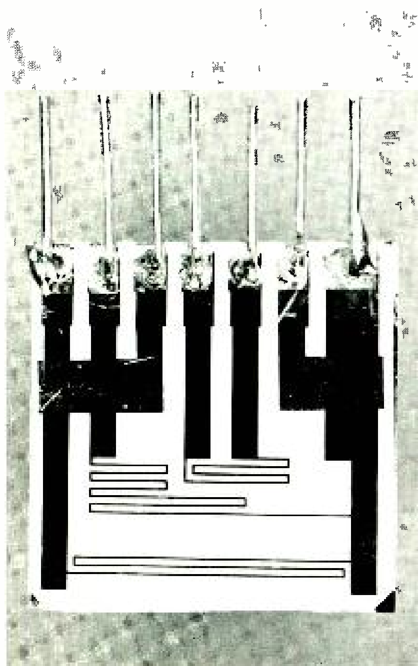
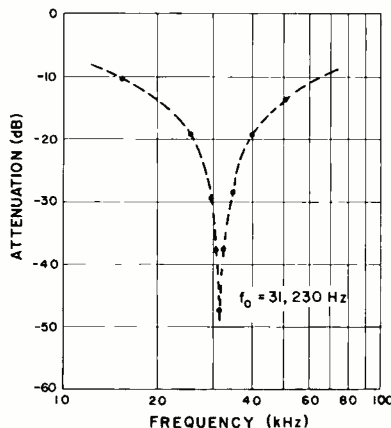


Fig. 19—No-load frequency response curve of thin-film hafnium-hafnium dioxide twin-T filter (f_o = 31, 230 Hz).



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A HIGH PERFORMANCE INTEGRATED OPERATIONAL AMPLIFIER

The design criteria for an operational amplifier configuration are discussed. Considerations and circuit trade-offs required to make a design suitable for monolithic silicon fabrication are explored. Finally, the operation of a new amplifier is discussed, and its performance characteristics are predicted.

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The growth of integrated circuits, both monolithic and hybrid, has precipitated the acceptance of the operational amplifier as a common tool of the circuit designer — far in excess of its limited field of acceptance just a few short years ago. Although much has been written about the application procedures for these devices,[1,2] there is relatively little material on designing the operational amplifier itself. Some of the more salient requirements for an integrated operational amplifier and indeed any operational amplifier are:

1) Equal input and output DC levels;
2) High gain with a reasonable frequency response;
3) Low input bias requirements;
4) Good common-mode characteristics;
5) Adequate power supply stability; and
6) A reasonable and efficient output drive capablility.

Of primary concern here is how these requirements can be fulfilled using circuitry that is compatible with the monolithic silicon fabrication process.

INPUT AND OUTPUT DC LEVELS

One design criterion that pertains to operational amplifiers in general is that the input and output DC bias levels should be equal. This is so that resistive feedback can be connected between the input and output without upsetting either the differential or common mode DC bias. Furthermore, for applications where two power supplies are used, the operational amplifier should be designed so that there is a set of standard supply values for which the equal input and output bias levels are at zero potential with respect to ground. This latter condition is especially important in direct-coupled cascade and comparator applications.

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GAIN AND FREQUENCY RESPONSE

The numerical values of the open-loop gain and 3-dB bandwidth of an operational amplifier are of relatively little importance as such. The important requirement for the open-loop gain is that it must be much greater than the closed loop gain of the transfer response over the frequency range of interest, if an accurate transfer function is to be maintained. As an example, consider a configuration with 50-dB gain, first using a 70-dB amplifier and then using a 90-dB amplifier. If in each instance the open-loop gain decreases 50%, the closed-loop gain will vary 9% using the 70-dB (nominal) amplifier, but only 1% using the 90-dB (nominal) amplifier.[2]

The frequency roll-off characteristics are the prime features of the frequency response of an operational amplifier. The greater the rate of roll-off occurring before the feedback ratio frequency characteristic intersects the open-loop response (the active region), the more difficult the amplifier is to phase compensate. An 18 dB/octane roll-off is generally considered the maximum slope that can occur in the active region before an excessive amount of bandwidth must be traded for stability.[2] Further, since operational amplifiers have useful applications down to and including unity gain, the active region of the amplifier may be considered as the entire portion of the frequency characteristic above its 0 dB bandwidth. Therefore, a well designed amplifier should roll-off at no greater than 18 dB/octave until well below unity gain.

INPUT BIAS REQUIREMENTS

A low DC input current is desirable when an operational amplifier must be operated using high impedance levels because of the nature of the drive source. It is not sufficient to have a high intrinsic AC input impedance, since this does not guarantee a low bias current.

Since transistors that exhibit ultra-high β (consistently over 100) at extremely low collector currents (under 10 μA) are not considered compatible with the monolithic process from a yield standpoint, the alternative of using resistor-less emitter-follower-type inputs is more attractive. The addition of these resistor-less emitter followers to the inputs can degrade the input offset voltage by as much as a factor of two.

COMMON-MODE CHARACTERISTICS

The common-mode-rejection and input-range characteristics are generally not appreciated unless the operational amplifier is used in either comparator or very low gain non-inverting feedback applications.

Under normal differential drive conditions, the common-mode rejection (the ratio of differential to common mode gain) has no drastic effects unless it is extremely low.[3] However, in a comparator type of application high common-mode rejection is imperative. Consider a 90-dB amplifier with a 70-dB common-mode rejection being used to compare a signal against a 1 volt reference. When the signal is also 1 volt, the output will be 3.2 volts when it should be zero. This, at the least, places a threshold restriction upon the succeeding circuitry that could be disasterous. The common-mode input voltage range is defined as the maximum positive and negative voltage excursions applied to both inputs simultaneously without a limiting condition occurring anywhere in the amplifier. As mentioned earlier this feature is of great importance in large-signal comparator-type applications, and in large-signal low-gain non inverting feedback configurations. A high

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positive common-mode-input capability can be attained by raising the collector voltages of the input differential stage to a level that allows Class-A operation under the highest expected common-mode-input voltage. The negative common-mode input range is inherently quite high in a two supply differential amplifier configuration.[3] The limiting factor here is the DC drop across the emitter resistor and the V_{CE} (sat) of the coupled-emitter DC constant-current-sink transistor.

POWER SUPPLY STABILITY

The power supply stability is a measure of the sensitivity of the offset voltage to power supply variations. Since its value at the output is feedback dependent it is normally referred to the input (as are all the other offset parameters) and expressed in microvolts per volt. In a fixed installation application using heavily regulated power supplies this parameter is of little importance. However, in an application where the amplifier is battery operated, it is of the utmost importance. In a single supply system, the amplifier's sensitivity to supply variations should be an absolute minimum; in a two supply system, the difference in the sensitivities to each supply should be minimized, since the supplies in many dual systems tend to track. This results in a cancellation, or at least a partial cancellation, of the two sensitivities.

OUTPUT DRIVE CHARACTERISTICS

As might be expected, the output power requirements for an operational amplifier depend almost entirely on the application. However, a few general conclusions can be drawn about the output-stage design. It should be able to swing essentially the full value of the power supplies and should be versatile enough to adapt to, or to be able to be adapted to, a wide range of loads efficiently. A high output swing capability has a two-fold requirement in that it sets a lower limit on the voltage gain of the output stage as well as demanding a configuration that is capable of swinging the full supply values. The demand for both load versatility and efficiency are incompatible except at low frequencies. Class-B output stages may suffer from cross-over distortion at all frequencies and phase distortion at high frequency due to slight differences between the positive and negative signal channels. Cross-over distortion can be minimized by providing a bias or idle current for the output devices (Class-AB operation) resulting in a slight degradation in efficiency. High frequency phase distortion can be alleviated somewhat by feedback. However, the applicability of even a carefully matched complementary stage is severely limited by phase distortion at frequencies much above 1 MHz. Push-pull stages not using complementary devices (i.e., using only devices of the same polarity) can suffer more acutely from inter-channel phase differences. Nevertheless, it became apparent that there was sufficient interest at the lower frequencies so that the investigation of efficient push-pull output stages suitable for integration would be practical. A complementary output stage was dismissed immediately since a reasonable fabrication process still does not exist to make identical opposite polarity devices. The use of dissimilar opposite polarity devices, while feasible, invariably result in one polarity type being considerably inferior to the other in performance. A stage using all like polarity transistors was finally decided upon because it was the most compatible with present diffusion techniques.

ADDITIONAL MONOLITHIC CIRCUIT DESIGN RULES

In addition to the restrictions already mentioned—transistors of single polarity, and moderate β at the extremely low collector current levels—the monolithic circuit designer must also consider his resistors. Because the absolute value of a diffused resistor cannot be controlled to within ±35%, a suitable circuit design must rely instead on resistor ratios which can be held to ±3%. Another consideration is that diffused resistor ratios can be held much better the closer they are to unity. Chip area is an important consideration as it is one of the factors contributing to yield.

CIRCUIT DESCRIPTION

A consideration of the above operational amplifier characteristics and the monolithic fabrication circuit design rules resulted in the configuration shown in Fig. 1. The circuit is basically a cascade of two differential amplifiers[2] and a direct-coupled all-NPN transistor push-pull output stage. In addition, input and interstage isolation are provided as well as strong common-mode feedback. Phase lag and lead compensation points[2] are between the collectors of the first stage and across $R13$ and $R14$ in the output stage, respectively.

The first differential stage is comprised of differential pair transistors $Q3$ and $Q4$, current sink transistor $Q8$ and input isolation transistors $Q1$ and $Q2$ which can be bypassed when low offset characteristics are desirable. The second stage which is driven push-pull by the first stage consists of differential pair transistors $Q6$ and $Q7$, current sink transistor $Q10$ and inter-stage isolation transistors $Q19$ and $Q20$. Common mode feedback paths are provided by both the collector and the emitter circuitry of transistor $Q5$. The output stage is comprised of DC level shift circuitry which includes transistors $Q11$ and $Q12$, diode cascade transistors $Q13A$ and $Q13$, impedance transforming transistor $Q14$, common emitter stage transistor $Q15$, isolation transistor $Q16$ and drive transistors $Q17$ and $Q18$.

The primary purpose of the first stage is to provide all of the desirable features and characteristics of a differential amplifier[2] as well as moderate gain. The second stage is basically a high-gain stage. As will be seen shortly it also actuates the common-mode feedback circuitry.

Diode configuration transistor, $Q9$ provides thermal compensation for current-sink transistors $Q8$, $Q10$, and $Q12$ in the first, second, and third stages, respectively. It also provides a degree of power supply versatility by causing the bias currents in the three stages to change less dramatically and more uniformly over the range of power supply values.

The functions of the isolating input transistors, $Q1$ and $Q2$ in the first stage

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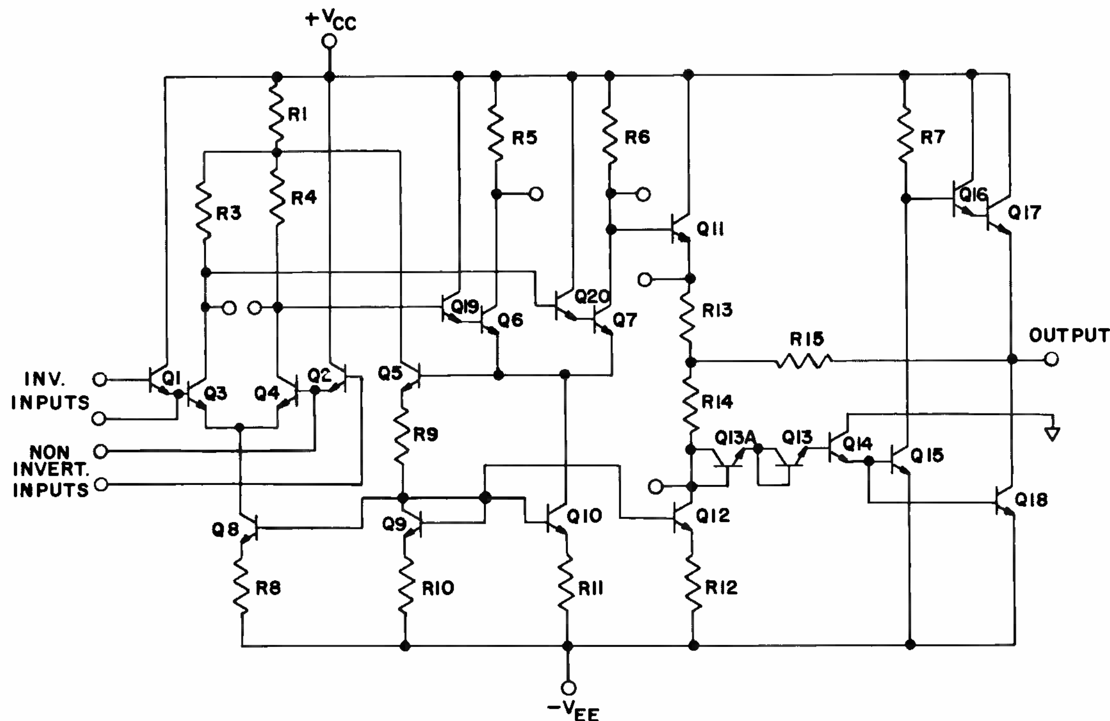

Fig. 1—Schematic diagram of the integrated operational amplifier.

and $Q19$ and $Q20$ in the second stage are to provide buffering and improved frequency response. The buffering is afforded by the very high AC input impedance characteristic and the very low base bias current requirements characteristic of these configurations. The improved frequency response occurs because the effective source impedance of the preceding circuitry is divided by the $(1 + h_{fe})$ term of the isolating transistors. This latter effect is partially masked however by the frequency characteristic of the h_{fe} term at low collector current levels.

The primary purpose of the common-mode feedback circuitry is to achieve a high degree of power supply variation insensitivity in the offset voltage. While the feedback circuitry does favorably affect the common mode gain, the primary contributor to the common-mode input characteristics is the balance and matching in the first stage. In addition, the common-mode feedback circuitry tends to make the amplifier more linear.

All of the common-mode feedback in the design shown in Fig. 1 is provided by transistor $Q5$. A common-mode signal due to either a variation in the power supplies or to a common-mode input appearing at the collectors of the first stage is reflected to the coupled emitters of the second stage (transistors $Q6$ and $Q7$) where it is detected by transistor $Q5$. Its collector circuitry reflects an inverted portion of this error signal back to the collectors of the first stage across common-collector resistor $R1$, thus reducing the actuating error signal. In addition, the emitter circuitry of $Q5$ transmits part of the error to the base of the first stage constant-current sink, $Q8$. Transistor. $Q8$ then causes a common-mode change in the current of the first stage such that the actuating common-mode error signal is further attenuated. This two-fold action by transistor $Q5$ on the first stage is beneficial to both the common-mode gain and the power supply stability characteristics. While the action of the emitter circuitry of $Q5$ on the second and third stages can be somewhat deleterious to the common-mode gain characteristic, it is required for good overall power supply stability. Considering a change in one of the power supplies and accepting the error reduction in the first stage, an in-phase portion of the variation is transmitted by the emitter circuitry of $Q5$ to the bases of current sink transistors $Q10$ and $Q12$ of the second and third stages. If the variation is in the negative supplies, the bases of $Q10$ and $Q12$ tend to follow the negative supply and thereby reduce any change in their base-to-emitter voltage and thus their bias currents. This effect is also present at transistors $Q15$ and $Q18$ in the output stage because the change is transmitted 1) indirectly through $Q10$ with the proper phase relationship to the collectors of the second stage and hence to the collector of $Q12$ and 2) directly through $Q12$ itself. The collector voltage of $Q12$ determines the base bias on transistors $Q15$ and $Q18$. A more or less dual effect occurs with a change in the positive supply: the supply variation causes a primary change in the collector voltages of the various stages instead of their bias currents. The reaction of transistor $Q5$ to a variation in the positive supply can be readily traced to show that it reduces the changes in the pertinent collector voltages of the various stages.

The linearizing effects of common-mode feedback transistors $Q5$ can be appreciated by first considering the nature of any signal appearing at the coupled emitters of $Q6$ and $Q7$ in the second stage. Since the second stage is driven push-pull, this voltage is equal to any common-mode input but is ideally zero when the drive is differential. Under the differential condition the only causes of a deviation from zero signal at this point are non-linearities occurring in the first stage and in the inputs of the second stage. If this non-linearity signal is traced through the amplifier it will be found that the feedback paths produced by the transistor $Q5$ circuitry act in concert to degenerate it.

The third or output stage provides 1) signal gain, 2) DC level shift from the second stage quiescent voltage to zero or

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ground reference, and 3) an efficient high-power-output drive capability.

Neglecting the feedback due to resistor $R15$ for the present, the signal from the second stage is injected into the base of common collector transistor $Q11$ whose emitter circuitry DC level shifts the signal, with very little attenuation, to a DC level which is appropriate for driving the succeeding circuitry. The DC level shift is provided by constant current sink transistor $Q12$. Signal attenuation is minimized by the high input impedance of the succeeding circuitry and by the high output impedance of $Q12$.

The signal appears at the base of isolating transistor $Q14$ through forward-biased diode transistors, $Q13A$ and $Q13$. Transistor $Q14$ drives inversion transistor $Q15$ and output transistor $Q18$ in parallel. The effect of $Q14$ is to provide impedance transformation, multiplying the parallel combination of the input impedances of $Q15$ and $Q18$ by $(1 + h_{fe})$. Its prime function therefore is to provide the high input impedance required by the level shift circuitry for minimum AC attenuation. It also increases the frequency response somewhat by offering a low impedance source to transistors $Q15$ and $Q18$.

Transistor $Q18$ is the output transistor for the negative signal excursions. It has a gain associated with it which is its transconductance (g_m) multiplied by whatever the load impedance might be at the time.

Transistor $Q15$ provides inversion and gain for the positive signal channel. It also presents the negative portion of the signal to the input of the positive output transistors to insure that they are at cut-off while the negative channel is conducting.

Perhaps the most dramatic function of transistor $Q15$ is to provide idle current bias for the output transistors. It accomplishes this by virtue of its V_{BE} voltage drop shunting that of transistor $Q18$. If transistors $Q15$ and $Q18$ are ideally matched, then their collector currents will be equal. Hence, the collector current of transistor $Q15$ determines the output transistor idle current.

This matching requirement between transistors $Q15$ and $Q18$ necessitates the use of parallel transistors for $Q17$ and $Q18$, each identical to $Q15$, to increase the current handling capability of the output stage.

Transistor $Q16$ provides impedance transformation of resistor $R7$ so that it does not limit the positive output swing capability under high load-current conditions. The impedance that effectively appears in series with the load is divided by the $1 + h_{fe}$ of two transistors instead of just the $1 + h_{fe}$ of the output transistor.

Transistor $Q17$ is the positive-channel output transistor. It is a common-collector configuration and therefore has no voltage gain of its own.

Thermal stabilization of the output stage is accomplished by a proper choice of resistor values to offset the thermal variations in the input bias voltages appearing at the bases of transistors $Q11$ and $Q12$ as well as its own inherent variations.

The use of a negative feedback resistor in the output stage aids in thermal stabilization, sets the voltage gain, and enables the use of a wide range of power supply values. The feedback resistor $R15$ is placed between the output and the virtual ground in the level shift circuitry (junction of $R13$ and $R14$). The voltage gain with $R15$ in place is essentially $R15/R13$ regardless of which channel is conducting provided the pos-neg. channel gains without $R15$ are much greater. The voltage gains in each channel without feedback are the same only when the load equals $R7$.

The output stage will work properly over a wide range of power supply values because the collector voltage of $Q12$ is essentially clamped to the negative supply through the diode action of transistors $Q13$, $Q13A$, $Q14$, and $Q15$ and $Q18$. It takes only a few millivolts at the collector of $Q12$ to cover the entire range of $Q15$ and $Q18$, from cut-off to saturation. The feedback can effect this change of a few millivolts, forcing a balance between output transistors $Q17$ and $Q18$.

The use of diodes $Q13$ and $Q13A$ increases the collector voltage on transistor $Q12$ which enables resistor $R12$ to be a larger value. The more voltage dropped across $R12$ the less dependent the circuit is on the thermal characteristics of the base-to-emitter diodes of transistors $Q8$, $Q10$, and $Q12$. In addition, there is an enhancement of the feasibility of integration, since the resistor ratio's ($R8/R3/R4$; $R11/R5/R6$; and $R12/R14/R13$) are closer to unity than they would be if $Q13$ and $Q13A$ were not used.

PERFORMANCE

Table I shows the data that the design equations predict when 12v DC power supplies are used on the circuit shown in Fig. 1. Notice that each predicted value has been placed in one of three columns: minimum, typical, or maximum. The column selections were based upon the dominant parameters used in predicting each value and whether they were minimum values such as α and β, universal values such as g_m and r_e, or typical values such as resistance and V_{BE}.

CONCLUDING REMARKS

It is the skill of the silicon device engineers that will determine the ultimate performance of this circuit. Their ingenuity is challenged in several areas:

1) The component layout on the chips should be such that the circuit is AC stable (this is a very real problem with gain in the 90dB class);
2) Resistor ratios as high as 30 to 1 demanding a close tolerance; and
3) A total of 196 Kohm on a single chip in an economical area demands narrow resistors which are more difficult to produce with a close ratio tolerance.

It is certainly to the credit of the ECD device engineers and fabrication personnel under the able leadership of Heshmat Khajezadah, that engineering samples of this operational amplifier have already been made with good yield and conforming very closely to the predicted specifications.

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TABLE I — Predicted Characteristics for ± 12 V DC Supplies

Characteristic	*Minimum*	*Typical*	*Maximum*
Differential voltage gain	....	92dB	....
−55°C	....	88dB	....
+125°C	....	90dB	....
Differential input impedance	246KΩ	....	....
Input Offset voltage	....	−9.9μV	....
−55°C	....	−414μV	....
+125°C	....	+281μV	....
Input bias current	....	....	318nA
Positive power supply stability	....	+10.5μV/V	....
Negative power supply stability	....	+23.9μV/V	....
Common-mode rejection	....	113dB	....
Common-mode input impedance	865MΩ	....	....
Common-mode input range	....	+6.2V/−10V	....
−55°C	....	+7.1V/−10V	....
+125°C	....	+5.5V/−10V	....
Power Dissipation	....	109mW	....

All data is for a 25°C ambient unless otherwise specified.

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COMPLEMENTARY MOS MEMORIES

For complex computer memories, MOS transistors in a complementary arrangement offer the advantages of fast switching operation and low power dissipation. This paper describes some of the basic circuit arrangements and characteristics of these complementary MOS devices. The operation of these devices in random access memories and associative memories and their relationship to the faster bipolar logic circuits are also covered.

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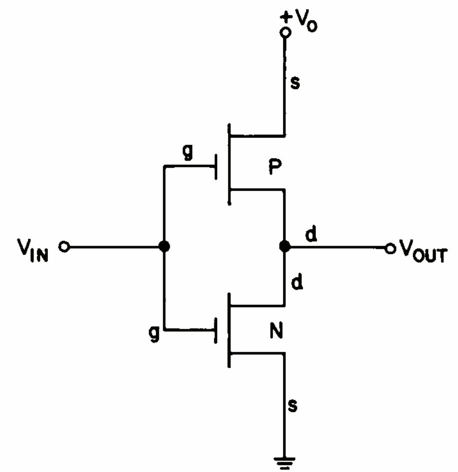

Fig. 1—Complementary MOS Inverter.

The advent of integrated circuit technology, along with the associated reduction in cost of complex systems, has generated considerable interest in computer memories consisting of large arrays of bistable circuits. In addition, such "active" memories offer very high speed operation and enable the fabrication of an entire system including the address decoder and word drivers with the same processing as the storage array. The particular approach most often suggested has been the use of bipolar transistors and is an extension of present silicon monolithic integrated circuit technology to larger arrays. However, since the smallest of memories requires several hundred to a thousand storage cells, the power dissipation per cell must be minimized, otherwise localized high temperatures on the silicon wafer will cause device failures. At the same time, high switching rates are essential if the overall system speed is to compare favorably with the high speed magnetic memories currently under development. This represents a design compromise which is at present not easily met with bipolar logic circuits.

The use of the MOS transistor in a complementary arrangement,[1] however, circumvents this problem as the quiescent power is only of the order of microwatts and yet offers fast switching operation. There is the added advantage that all digital systems, regardless of complexity, can be constructed exclusively with complementary MOS transistors without the need for passive components, thus improving yield and reliability of an integrated system by reducing the required substrate area. The following discussion presents the basic features of complementary MOS circuits after which the operation and performance of memory systems will be outlined.

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BASIC CIRCUIT IDEAS

The complementary MOS inverter (Fig. 1) is used as the basic building block of this approach and has the unique property of dissipating only microwatts of power in either binary state. When the input is at ground "0," the N transistor is cut off while the P transistor is conducting ($V_{gs} = V_0$) and consequently the output is $+V_0$ volts. Similarly, when the input is at $+V_0$, the N transistor is conducting and the P transistor is cut off, which gives zero at the output. In either case, the impedance from the positive supply to ground is that of a nonconducting transistor. Typical standby currents are of the order of 0.1 microamp which for $V_0 = 10$ volts gives a net dissipation of only 1 microwatt.

More complex logic functions can be generated from the same circuit by series-parallel arrangements of the transistors as in the NAND and NOR circuits of Fig. 2 while a bistable circuit is obtained by cross coupling two complementary inverters as in Fig. 3. Thus, by the appropriate use of N and P-type MOS transistors, any combinational or sequential logic function can be realized with only microwatts of quiescent power dissipation.

Switching Response

The switching response of the complementary circuit has been analyzed previously[2] in some detail by a computer analysis and formulas have been obtained for the pair delay, and the rise and fall times, as a function of the device parameters. However, the switching mechanism can be seen qualitatively as being determined by the amount of current available from the conducting transistor for the charging (or discharging) of the load capacitance when the input changes abruptly from $+V_0$ to 0 (or 0 to $+V_0$). Note that in both charging and discharging, the switching current is that of a heavily conducting transistor which is the reason for the superior transient response of this circuit as opposed to other MOS circuits (resistive load or MOS diode load).

Quantitatively, it can be shown that the pair delay time is related to the device parameters by the following expression:

$$T_D = \frac{2L^2}{V_0} f(N,M) \left[\frac{1}{\mu_n \left(1 - \frac{V_{Tn}}{V_0}\right)^2} + \frac{1}{\mu_p \left(1 - \frac{V_{Tp}}{V_0}\right)^2} \right] \qquad (1)$$

where L is channel length;
- V_0 is the supply voltage (typically 10 volts);
- μ_N is the effective mobility of electrons in the N transistors
- μ_P is the effective mobility of holes in the P transistors
- V_{TN} is the threshold voltage of the N transistor
- V_{TP} is the threshold voltage of the P transistor; and
- $f(N, M)$ depends on stray capacitances, parasitic substrate capacitances and is an increasing function of N and M, the fan-in and fan-out of the circuit.

A typical pair delay time with present complementary transistors and $N = M = 1$ is of the order of 5 to 15 nanoseconds, depending on the method of device fabrication. This is comparable to the speeds obtained with bipolar transistor circuits.

Power Dissipation

Although the quiescent power is extremely low, the fact that current flows

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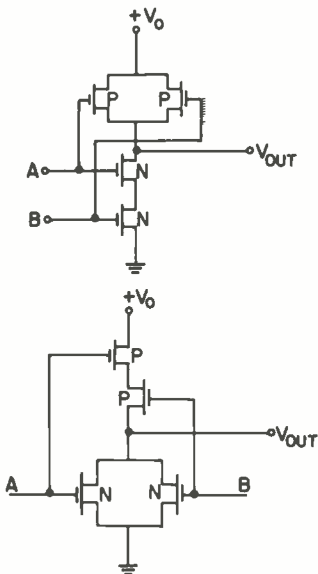

Fig. 2—NAND and NOR circuits.

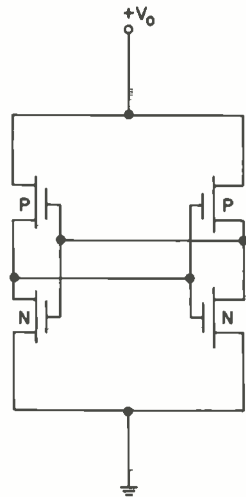

Fig. 3—Complementary flip flop.

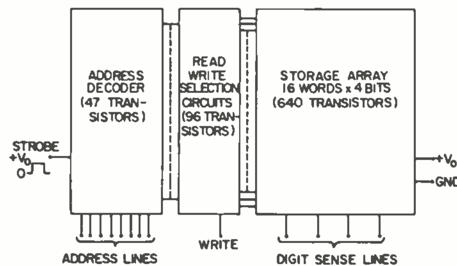

Fig. 4—Block diagram of memory module.

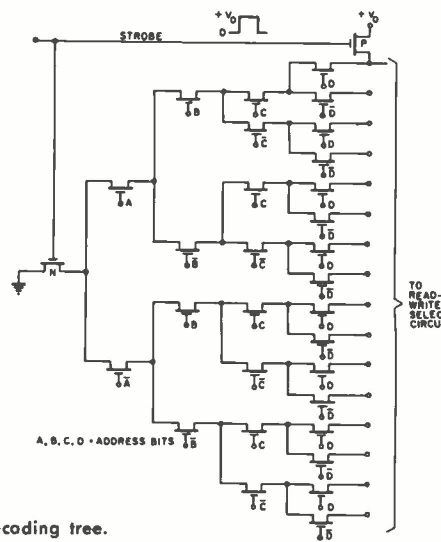

Fig. 5—Binary address decoding tree.

during switching to charge and discharge the load capacitance gives an additional contribution to the circuit power dissipation.

It is well known that in discharging a capacitance, C_L, the energy dissipated is equal to the energy ($\frac{1}{2} C_L V_o^2$) initially stored. In recharging the capacitance, the same energy is again lost.[2] Consequently, the switching power dissipated in the transistors of a complementary MOS circuit operating at switching frequency f is

$$P_{AC} = C_L V_o^2 f \qquad (2)$$

It may appear that the power dissipation is large at high repetition rates (10 mW for C_L = 10 pF; V_o = 10 volts; f = 10 MHz). However, in a large system only a small fraction of all circuits switch each cycle, so that the total power consumption of the system is still very small. This is particularly true for memories, since only one word out of many is selected each cycle. Thus, the use of complementary MOS transistors in "active" memories enables high speed operation at considerably lower power levels than other approaches. In addition the very low standby power consumption of complementary circuits enables the construction of large memories capable of retaining the stored information with a flashlight battery in case of a power failure.

Noise and Drift

A further feature of complementary MOS circuits is that they are very insensitive to noise and drift in device parameters. One reason for this is the fact that the circuits always present a low output impedance. The noise immunity is increased with the threshold voltages of the devices, V_{TN} and V_{TP}. However, as can be seen from Eq. 1, the pair delay is significantly increased as the threshold voltages are increased beyond 20% of the supply voltage V_o. As a compromise, the threshold is usually chosen to be 10% to 20% of V_o.

RANDOM ACCESS MEMORIES

Fig. 4 shows a block diagram of a random access memory module, complete with address decoder and the necessary word drivers for a 16-word 4-bit memory array.[4,5] It should be noted that although the module contains a total of 783 transistors, only 16 output leads are required. Operation of the memory is best described by an explanation of the individual circuits.

The address decoder (Fig. 5) basically consists of a binary decision tree which can be activated by an applied STROBE signal. When the STROBE is present, one of the 16 outputs is switched to 0 volts corresponding to a selected word. The output of the decoder controls the READ and WRITE

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drivers shown in Fig. 6. The WRITE driver is activated only upon a command common for the entire memory. An additional signal, the inverse of the WRITE command, is also generated to insure high speed operation of the storage cell. These lines are then connected to appropriate points of the basic cell, shown in Fig. 7. The cell employs 10 MOS transistors and can be written into by means of two MOS transmission gates—one for opening the feedback loop from *B* to *C*, the other for entering the desired information into the cell at *C* from the digit line. After one pair delay time, the potentials at *B* and *C* are identical and the feedback loop may be closed by bringing the WRITE line down to ground potential, thereby leaving the information stored in the flip-flop. Readout from the memory is accomplished non-destructively by controlling the conductance of an N-type MOS with the output voltage of the cell. Subsequent application of a READ command will result in the presence or absence of a current in the low impedance sense (DIGIT) line, indicating a stored "1" or "0." Current sensing with a low impedance device, such as a grounded-base bipolar transistor shown in Fig. 8, is a very fast operation (<5ns), even if the capacitance of the digit line is large as it would be in a large memory. The sense current, which is typically 1 to 2 ma, is sufficiently large to produce a typical bipolar logic signal (0.8 volt) at the collector. The circuit in Fig. 8 also operates as a complementary emitter follower driving a digit line under the WRITE operation.

The capacity of the memory is expandable in modules of 16 words, 4 bits by the appropriate connection of the individual STROBE lines of each module. More words can be obtained by the addition of external address decoding to select the desired STROBE line and more bits per word by connecting STROBE lines in parallel.

The memory module described above has been constructed using semi-integrated packages (4 transistors per package). In this form, the access time was 50 ns, most of which was spent in the address decoder and the MOS word drivers. Thus, for very high speed scratch-pad memories (cycle times <50ns) it is advantageous to make the drivers as well as most of the decoding with bipolar circuits.

A particular integrated circuit, intended for a high speed scratch pad memory, consisting of one word of 9 bits, has been fabricated using thin film silicon on sapphire technology.[6,7,8,9] This circuit (Fig. 9) occupies an area of 0.08 x 0.08 inches and is designed to be packaged in a standard 14-lead flat-pack. The standby power of this entire 90-transistor circuit is 90 microwatt. Fig. 10 shows the delay between the application of the WRITE command and the output response of the cell as measured on the sense line.[10] The minimum duration of the WRITE command pulse is less than 10 nanoseconds. Temperature tests conducted on these circuits showed an increase in standby current from 1 μA to 20 μA and an increased switching time of less than 25%. These effects were reversible indicating that the stability is comparable to bulk silicon MOS transistors.[11]

The excellent performance of these circuits is largely a result of the circuits being on the insulating sapphire substrate, whereby the usual parasitic substrate capacitances and the harmful substrate gating effects are eliminated. This is of particular importance in low fan-out, high speed circuits, such as storage cells.

A system of interconnected modules of the type shown in Fig. 4 can provide the basic ingredients of a word-organized memory: the storage cells, the word drivers, and all decoding except the strobe selection of 16-word groups. However, in addition to the modules, other "external" circuits are required such as: address-line drivers, digit-line drivers, strobe drivers, digit-current sensors, strobe decoders, timing circuits as well as data and address-registers with associated gates. This is a fairly complex system which is preferably not made with MOS circuits but with the faster bipolar logic circuits used in other parts of the computer system. These bipolar circuits operate at a different logic level than the MOS circuits, which may have 0 volts and + 10 volts levels for logic "0" and "1" respectively. For high speed emitter-coupled logic circuits (ECCSL) the corresponding levels are −1.6 volts and −0.8 volts. The fact that signal conversions are required between bipolar and MOS circuits is not a trivial problem. Such "interface" circuits (e.g. the circuits shown in Figs. 8 and 11) consume time and power and require special hardware. The interface circuit shown in Fig. 11 must, in general, be followed by a high current driver of the type shown in Fig. 8, if a large capacitance, such as an address line or a digit line, is to be driven with a logic swing of 10 volts in a short time. In the system design, the number of interface circuits must be kept to a minimum, which is difficult to realize in a word-organized system. A compromise design is that of using coincident voltage or *XY*-memory cells in a so-called bit organized system. In these memory cells one level of decoding, i.e. the coincidence of a "1" in the *X* and *Y* lines, is performed in the cell, while the rest of the decoding is left to be done with external circuits. In a system with N^2 words, which would require at least N^2 word drivers in a word organized memory, the number of drivers in a bit organized memory can theoretically be reduced to $2N$.

ASSOCIATIVE MEMORIES

The fact that storage cells and logic circuits can be integrated together using the same technology enables the fabrication of more sophisticated storage systems, such as associative memories. These memories, also referred to as content addressable, are accessed, just as the information in a telephone directory, by the content of the stored word rather than by a specifically assigned address as in a random access memory. An important application of associative memories is in the translation of addresses in large, time-shared, data processors.

Fig. 11 is a block diagram of a content addressable memory (CAM) made exclusively of complementary-MOS circuits. The CAM cell shown in Fig. 12 contains the logic required for generating a mis-

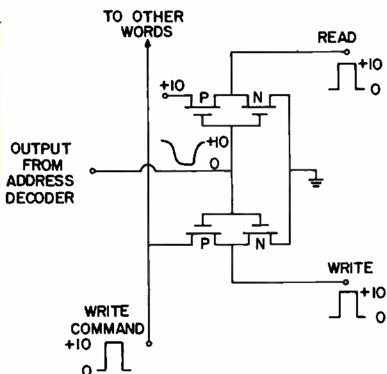

Fig. 6—MOS read-write drivers.

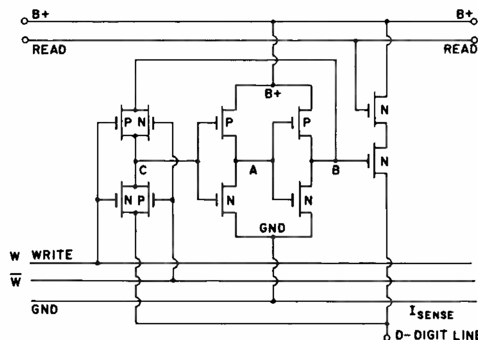

Fig. 7—MOS memory cell with nondestructive read-out.

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match signal when one or more of the stored bits in the word does not match the search criterion set up on the interrogation lines. These lines are also used for writing into the cell. The "don't care" criterion ($D_1 = D_2 =$ "0") will leave the cell undisturbed during writing, and will also yield an unconditional match during a search. The flip-flops of the match register (Fig. 11) are all set to a match at the beginning of a cycle and upon a search command, those flip-flops corresponding to a mismatched word are reset. The content of the match register is fed into a multiple match resolving logic tree,[4,12,13,14] which selects one of the matched words (referred to as the lowest match). This particular word can then be operated on, after which the associated match flip-flop is reset. The tree automatically selects the next matched word, etc. This system with four words of four bits each has been tested with MOS transistors.

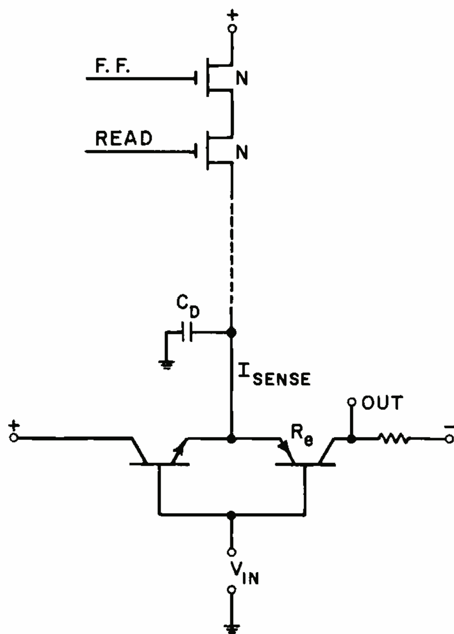

Fig. 8—Complementary bipolar drive-sense circuit.

CONCLUSION

The important question, which only the future may answer, is how well MOS scratch pad memories, which require special interface circuits are going to compete with all bipolar scratch-pad memories. This is going to depend on packing density, size, yield, speed, noise immunity, and power consumption of the arrays, as well as the overall systems aspects, such as packaging, need for special purpose circuits, maintenance, etc. It is also going to depend on future developments in integrated circuit technology.

ACKNOWLEDGMENT

This paper surveys the results of the research efforts of a large number of people at RCA Laboratories whose contributions are gratefully acknowledged.

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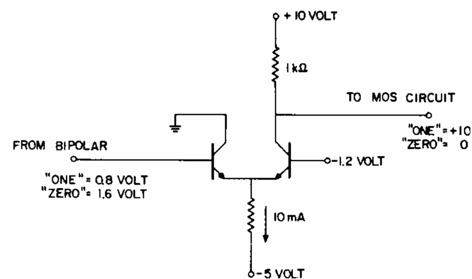

Fig. 11—Bipolar to MOS interface circuit.

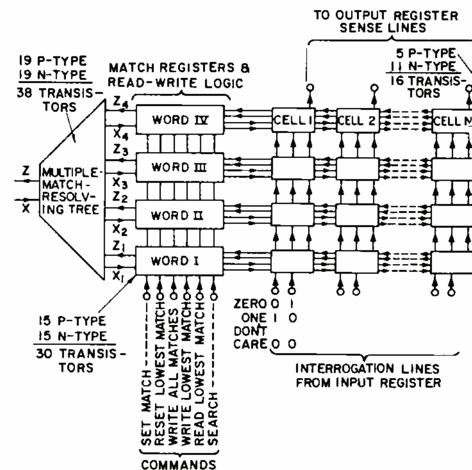

Fig. 12—Block diagram of associative memory module.

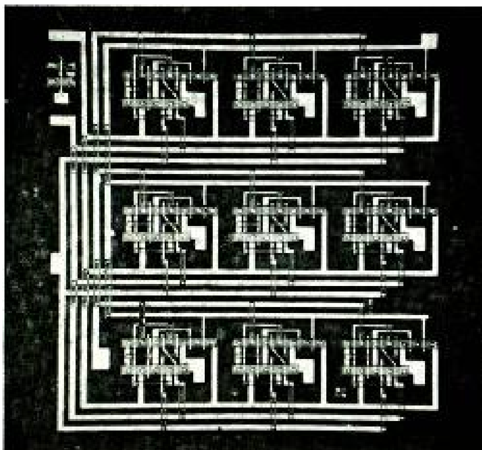

Fig. 9—9-bit memory array.

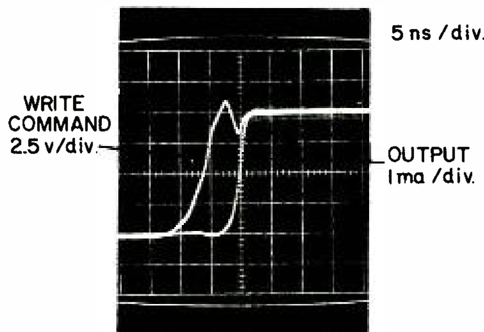

Fig. 10—Response of memory cell.

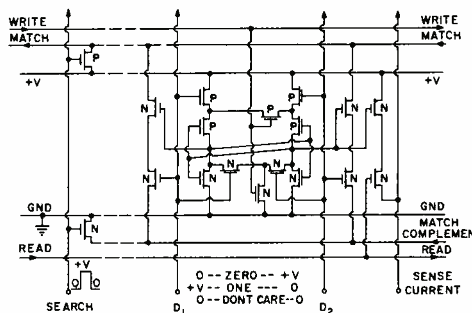

Fig. 13—MOS associative memory cell.

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SEMICONDUCTOR STRAIN GAGES—RESISTORS VERSUS TRANSISTORS

Within the last decade the dominant position of the metal strain gage for applications in the electromechanical transducer field has been increasingly challenged by several new semiconducor devices. These new devices are divided into two general classes—resistors and transistors—based on the nature of their output characteristics. This paper compares these two types of semiconductor strain gages so that their potential importance for transducer applications can be properly appreciated. The comparisons are based upon evaluations of the devices and their immediately associated circuitry, such as power supplies and output detectors. On this basis, the thin-film transistor gage gives promise of having a system sensitivity two orders of magnitude higher than the resistor-gage system, while requiring a supply regulation three orders of magnitude lower. These numerical estimates are based on contemporary typical values.

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THE applications of the metal strain gage span the spectrum of electromechanical transducers. In addition to its original use for strain measurement, this device is commonly incorporated in sensors which measure displacement, acceleration, pressure, and force. Within the last decade, the dominant position of the metal gage has been increasingly threatened by the development of semiconductor devices based on newly discovered or previously unexploited electromechanical effects.

Probably the best known of the new devices is the resistive semiconductor gage based on the piezoresistive effect in germanium or silicon. These units have gage factors which exceed those of ordinary metal gages by one to two orders of magnitude.[1,2,3,4] Because of their great promise, an extensive research and development effort has been devoted to the technical improvement of these devices, and the success of this effort is demonstrated by the appearance within the last few years of a variety of commercial transducers based on this effect.

However, the piezoresistive gage does not represent the sole challenge to the metal gage in transducer applications. A number of potentially competitive devices utilizing transistor-type structures have been demonstrated or proposed,[5,6,7] and at least one of these, the stress sensitive junction transistor,[5] has been the subject of a significant research effort. Thus far, none of these devices has reached a sufficient level of technical perfection to be considered a practical alternative to the resistive gages, but their promise of unique properties continues to spur additional effort.

One portion of the current research program at the David Sarnoff Research Center is an evaluation and investigation of the properties of electromechanical transducers, with particular reference to their possible applications in commercially important areas. Over the past year, a substantial percentage of this effort has been devoted to establishing the potential of the transistor-based strain gages.

Initially, many of the arguments for the potential superiority of this class of devices were based on largely intuitive grounds. These usually hinged on a statement to the effect that the device "includes the amplifier with the sensor". At first glance this appears as a quite persuasive point, but the prospect of basing the entire justification of a research project on such grounds is not particularly attractive.

As an alternative, the decision was made to develop a more quantitative evaluation of the potential properties of these devices—in direct comparison to those of the piezoresistive strain gage. It is the result of this effort which forms the subject of this paper.

The fundamental difference between the two general classes of resistor gage (RG) and transistor gage (TG) can be illustrated quite clearly in terms of their typical electrical output characteristics, as shown in Figs. 1 and 2. The former is simply a variable linear resistor, while the transistor gage has the character (in the current saturation range) of a con-

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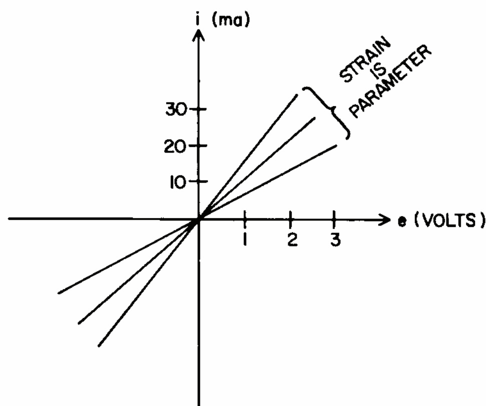

Fig. 1—Output characteristics of piezoresistive gage.

stant current source in parallel with a large resistance.

In keeping with the very general objective of this investigation, the detailed mechanisms which underlie the electromechanical interaction in these gages are not discussed, but instead the two general classes are evaluated entirely on the basis of their basic output characteristics. More specifically, they are primarily evaluated in terms of the power supply and output detector requirements for their operation as transducers. In addition, a relative evaluation is made on the basis of sensitivity when this can be done in a valid manner.

Thus the investigation really consists of a systems type characterization of each transducer class and its associated circuitry, followed by various comparisons of the merits of the alternative systems. The basic nature of the overall systems which are considered is represented in Fig. 3, and includes power supply as well as output detector.

BASIC RESISTIVE GAGE SYSTEM

Traditionally, metal strain gages have been incorporated in bridge circuits to convert the resistance change of the gage into a usable output voltage. When used in this fashion, the figure of merit is the gage factor, G, of the strain gage which is defined as

$$G = \frac{\Delta R/R}{S} \qquad (1)$$

where ΔR is change in resistance, R is nominal resistance, and S is applied strain.

However, with the advent of the semiconductor resistor gage (RG), the use of bridge circuits for single gage applications was no longer practical because of the sensitivity and hence large resistance changes of these devices. This effect leads to unacceptable nonlinearities of the bridge output which are due entirely to the nature of the bridge unbalance equations, i.e., this is an effect in addition to any inherent gage nonlinearity.[1] For example, a strain of 10^{-3} will produce a $\Delta R/R$ of about 13% (i.e., G = 130), and a bridge output nonlinearity of over 6%.[2] By comparison, this problem is not at all critical for wire strain gages, where $\Delta R/R$ rarely exceeds 0.5% for the same strain levels.[2]

To exploit the large available resistance variation in the RG, and still obtain an output voltage which is linearly related to ΔR, it is necessary to use a constant current system of the type illustrated in Fig. 4.[3] As a first approximation, for an ideal current supply and voltage detector, the voltage change ΔE due to the resistance variation ΔR is

$$\Delta E = I\Delta R = IGR \qquad (2)$$

It is apparent from Eq. 2 that this circuit allows the full resistance variation of the device to be used and still maintains linearity of output.

At first glance, it would appear that ΔE could be made as large as desired by the apparently simple expedient of increasing I. However, this possibility is limited by several practical considerations. The most important is that a large gage current leads to excessive ohmic heating—hence resistance changes due to temperature rise and thermally induced strains, as well as possible burn out of the gage. For example, RG units typically have a power dissipation limit of about 0.1 watt,[4] and for a nominal gage resistance of 350 ohms this limits the gage current to approximately 17 mA.

Now that the basic constant-current system has been introduced, the supply and detector will be discussed individually in more detail. It should be emphasized that the constant-current circuit is absolutely necessary when a single gage application is considered, but that for certain special two and four gage applications, a bridge circuit can still be used.[1] However, for the present purpose of comparison with the analogous single-transistor-gage system, the constant current circuit is the logical choice.

SUPPLY REQUIREMENTS AND LOADING CONSIDERATIONS

A more realistic representation of the system shown in Fig. 4 is given by the equivalent circuit of Fig. 5. This circuit can be used to evaluate loading and supply regulation effects. The voltage change, ΔE, for this circuit is

$$\Delta E = I\Delta R \left[\left(\frac{R_p}{R_p + R} \right)^2 \left(\frac{1}{1 + \Delta R/(R_p + R)} \right) \right] \qquad (3)$$

where

$$R_p = \frac{R_s R_o}{R_s + R_o}$$

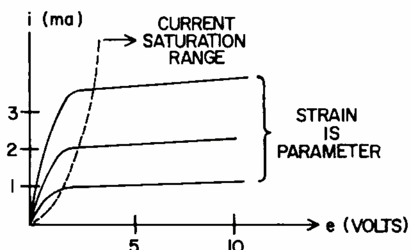

Fig. 2—Output characteristics of transistor gage.

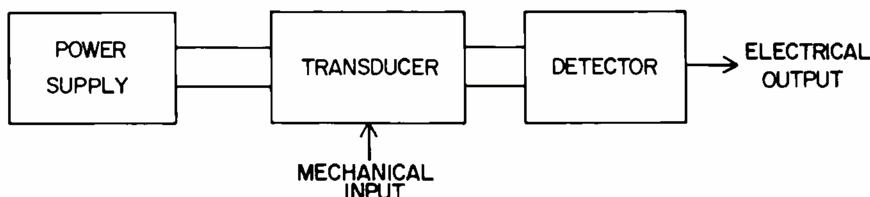

Fig. 3—Transducer system under evaluation.

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It can be seen from this expression that the loading due to R_s and R_o has a twofold effect. The first factor involving R_p tends to reduce the voltage change, and the second leads to a nonlinearity of the voltage change with ΔR. In a transducer application, the nonlinearity is the more critical consideration, and to reduce this effect to negligible magnitude the requirement is

$$R_p + R >> \Delta R \qquad (4a)$$

or, since ΔR can be an appreciable fraction (10% or more) of R, this can be written as

$$R_p >> R \qquad (4b)$$

Using this condition, Eq. 3 reduces to

$$\Delta E \cong I\Delta R = IGR$$

Thus, the approximate expression given in Eq. 2 is valid provided that the parallel combination of R_s and R_o is much greater than R. It should be stressed again that this requirement is necessary both for reasons of output linearity as well as maximization of the output voltage change.

The effect of poor current regulation can be developed in the following manner. Suppose I changes by amount ΔI with no change in gage resistance. Then the spurious voltage change will be

$$\Delta E' = \Delta IR$$

provided that the loading effect is negligible. Thus the resolution of the constant current system is limited to the detection of gage resistance changes such that $\Delta E = \Delta E'$, or

$$I\Delta R = \Delta IR$$

and the smallest ΔR which could be detected would be

$$\Delta R_{min} = R\Delta I/I \qquad (5a)$$

Alternatively, this can be expressed in the form

$$\Delta R/R = \Delta I/I \qquad (5b)$$

or, using Eq. 1, this reduces to

$$S_{min} = \Delta I/GI \qquad (6)$$

where S_{min} is the minimum detectable strain. Hence the regulation of the current supply directly determines the resolution of the RG transducer system.

To give a quantitative estimate of the required stabilization of the current supply, suppose that an arbitrary resolution standard of 1×10^{-6} strain (i.e., one microstrain in engineering usage) is chosen for evaluation purposes. Then, for a typical gage factor of 100,[1] Eq. 6 yields

$$\Delta I/I = 10^{-4} = 0.01\% \qquad (7)$$

as the required supply regulation. That is, for example, the current supply must not have variations larger than 1 μA if it supplies 10 mA to the gage. It should be kept in mind that this regulation must hold when the resistive load (i.e., the strain gage) is varying by as much as 10% in either direction at a frequency of possibly several kHz.

VOLTAGE DETECTOR CONSIDERATIONS

As seen from Eq. 4b, the voltage detector circuit must have a high input impedance relative to the nominal resistance of the RG (typically in the range of a hundred to a thousand ohms). A simple amplifier stage is sufficient to supply this type of input impedance. If a junction transistor stage is used, an emitter follower (or similar device) would be required, and would yield a voltage gain of approximately unity.

If a field effect transistor (FET) were used, a grounded source configuration would suffice. In this case the output would basically be a change in the drain current Δi_D, i.e.

$$\Delta i_D = g_m \Delta E \qquad (8)$$

where g_m is the transconductance of the FET. Eq. 8 will be used later for comparing the RG and TG systems for typical values of the critical parameters.

THE BASIC TRANSISTOR GAGE SYSTEM

Several types of transistor gage (TG) have been demonstrated, or proposed, using junction and field effect transistors. The physical mechanisms utilized include: anisotropic stress effect in P-N junction of junction transistor;[5] piezoresistive effect in junction and field effect transistors;[6] and piezoelectric effect in thin-film field effect transistors.[7] All of these devices have the general type of output characteristics represented in Fig. 2, although they differ in terms of scale factors for the current and voltage axes. The development which follows is based upon these typical output characteristics and hence is applicable to all of these types of transistor gages. However, when numerical estimates are made the appropriate values for the thin-film piezoelectric device will be utilized.[7]

The circuits proposed for the utilization of the TG current variation have usually taken the form of standard amplifier configurations, where the change in current develops an output voltage across a load resistor. However, such a circuit is not suitable for all of the applications of possible interest, and hence the more general system represented in Fig. 6 will be used in this paper. By making simple variations in the properties of the current detector it will be possible to accommodate the various system requirements of major interest.

The basic figure of merit for the TG is the current-strain sensitivity, K, defined as

$$K = \Delta i/S \qquad (9)$$

where Δi is the change in TG output current for constant TG output voltage, and S is the applied strain.

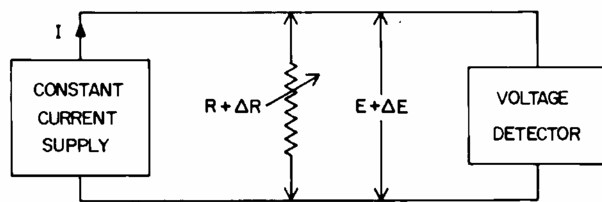

Fig. 4—Constant current system for piezoresistive gage.

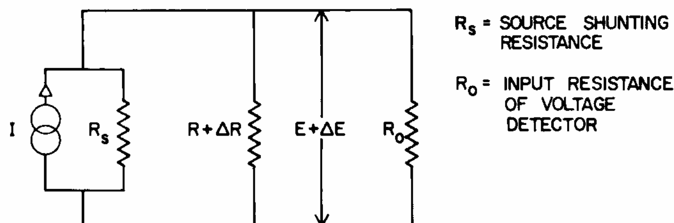

Fig. 5—Equivalent circuit for constant current RG system.

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As a first approximation, for an ideal voltage supply and current detector, the change in current seen by the current detector (i.e., Δi_o) is equal to the change in gage current, or

$$\Delta i_o = \Delta i = KS \qquad (10)$$

Thus it is apparent, from Eq. 10, that the system represented in Fig. 6 allows the full current variation of the device to be utilized.

It should be noted that the supply voltage, E, does not appear in Eq. 10, whereas the analogous expression for the RG system, i.e., Eq. 2 contains the supply current I. This is the first indication of a fundamental, and useful, difference between the two types of gages—its implications will be developed in the following section.

Now that the basic constant voltage system has been introduced, the supply and detector will be discussed individually in more detail, and comparisons made with the RG system.

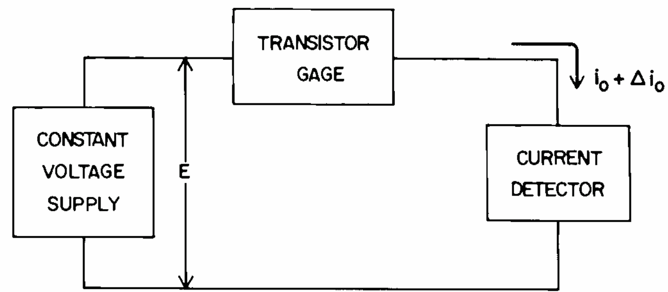

Fig. 6—Constant voltage system for transistor gage.

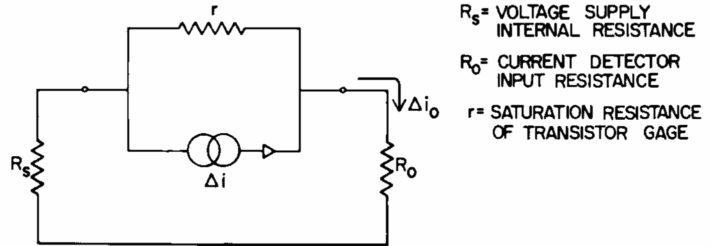

Fig. 7—Incremental equivalent circuit for constant voltage TG system.

SUPPLY REQUIREMENTS AND LOADING CONSIDERATIONS

To analyze the properties of the TG constant voltage system it is necessary to replace Fig. 6 by a more realistic representation. If the transistor gage is operated around a quiescent point in the current saturation region, then the incremental equivalent circuit takes the form shown in Fig. 7. Again it should be noted that the supply voltage, E, does not appear in this circuit, in contrast to the analogous RG circuit given in Fig. 5. This is under the assumption, of course, that E is absolutely constant. The effect of a variation in E will be examined separately.

Using Fig. 7, the current change, Δi_o, is given by

$$\Delta i_o = \Delta i \frac{r}{r + R_s + R_o} \qquad (11)$$

This expression has important similarities and differences in comparison with the analogous expression, Eq. 3, for the RG system.

First, the factor involving $R_s + R_o$ tends to reduce the actual output current variation, Δi_o, below the maximum available from the TG, i.e., Δi. This effect is exactly similar to the reduction of the RG output voltage produced by the first modifying term in Eq. 3. However, in contrast, no nonlinear terms appear in Eq. 11 due to the loading by $R_s + R_o$. Thus if, for a particular application, it is found advantageous to use a value of R_o which is not negligible in comparison with r, then there will be no degradation of the system linearity due to this loading of the TG. This is, of course, in sharp contrast to the distinct output nonlinearity which occurs for the RG system under equivalent loading conditions. In summary, the properties of the TG are such as to provide an inherent isolation effect which prevents any finite loading from degrading the linearity of the output. (This result corresponds to the intuitive statement that the device inherently combines the functions of sensing and amplification.) The flexibility which results from this property of the TG unit will be examined in detail in the following section on current detector considerations.

The effect of poor voltage regulation can be evaluated from the equivalent circuit shown in Fig. 8. This circuit is similar to that of Fig. 7, but it includes a voltage generator of magnitude ΔE (i.e., the voltage supply variation) and does not include a current generator in parallel with r. The latter situation arises because it is desired to compute the change in output current which occurs in the absence of a strain induced variation—viz., the change due only to the voltage supply fluctuations.

Using this circuit, the spurious current change is

$$\Delta i_o' = \frac{\Delta E}{r + R_s + R_o} \qquad (12)$$

and the resolution of the system is limited to the detection of strain-induced current variations such that $\Delta i_o = \Delta i_o'$, or, using Eqs. 11 and 12, this becomes

$$\Delta i \frac{r}{r + R_s + R_o} = \frac{\Delta E}{r + R_s + R_o}$$

Hence

$$\Delta i_{min} = \Delta E / r \qquad (13)$$

is the smallest strain-induced current change which can be resolved.

Alternatively, this can be expressed, using Eq. 10, as

$$S_{min} = \frac{1}{K} \frac{\Delta E}{r} = \frac{1}{K} \frac{E}{r} \frac{\Delta E}{E} \qquad (14)$$

where S_{min} is the minimum detectable strain. It can be seen that the minimum detectable strain is dependent on the supply regulation, but that the effect is modified by the factor (E/r). Such a modification does not occur in the analogous expression for the RG circuit, i.e., Eq. 6. This result follows directly as a result of the form of Eq. 12, as previously discussed in connection with that equation.

To obtain a numerical estimate of the required voltage supply regulation, the arbitrary resolution desired will again be chosen to be 1×10^{-6} strain. Typical values for the thin-film field-effect TG are[7,8]

$$K = 2.4 \text{ amps/unit strain}$$
$$E = 2.5 \text{ volts}$$
$$r = 10^5 \text{ ohms}$$

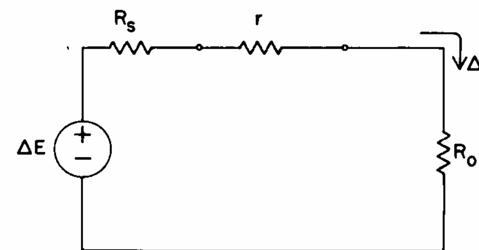

Fig. 8—Incremental equivalent circuit for evaluation of voltage regulation effects.

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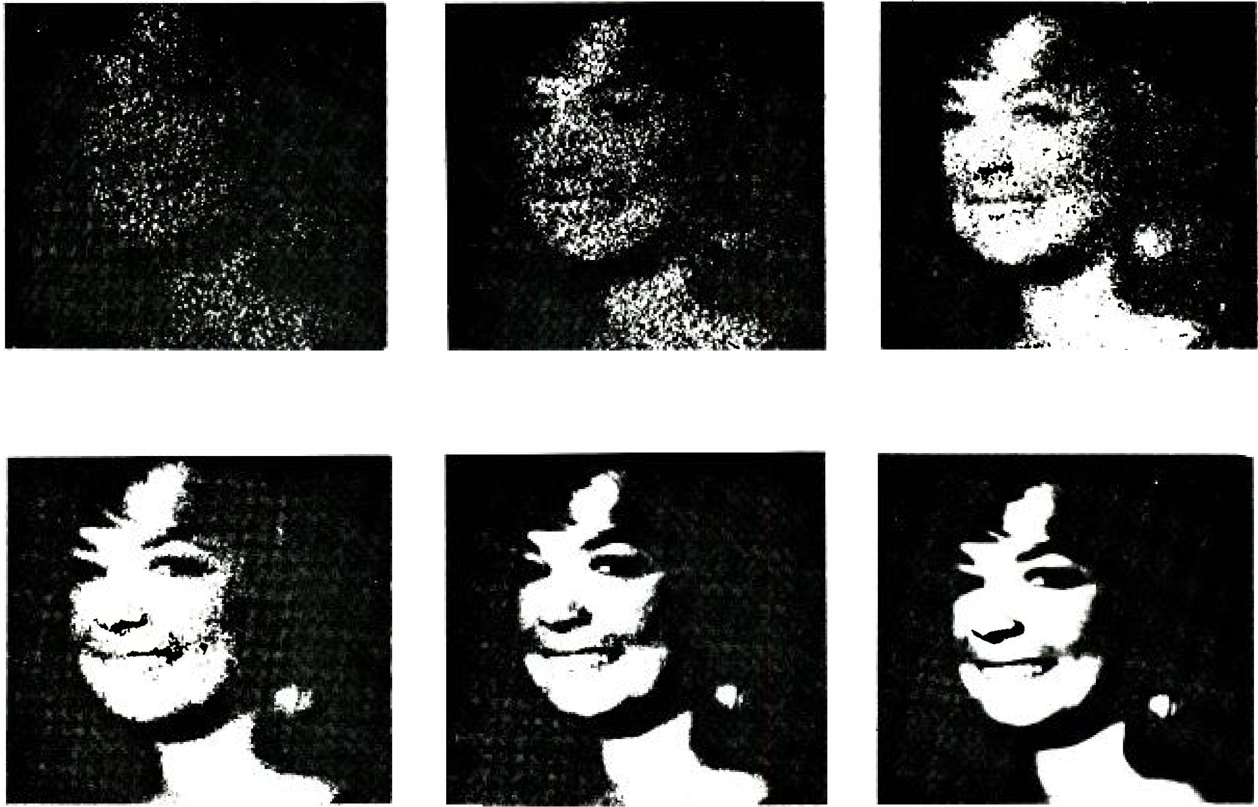

Fig. 2—Electronically produced images illustrating the statistics of image production.

PHYSICS OF LOW-LIGHT-LEVEL VIEWING

Light is composed of small packets of energy called photons. These photons provide scene information according to the number which arrive at the eye in a given time (corresponding to brightness) and the energy of each photon (corresponding to color). The first part of this paper discusses only the number of photons, or brightness, because present low-light-level viewing devices do not reproduce scenes in color. Uses of different wavelengths or colors for night viewing systems are discussed later.

Under normal room brightness, tens of billions of photons per second are emitted from an area the size of one typed letter. On a dark night (without any stars or moon), the number of photons per second from the same area may be less than 100. This decrease in brightness directly affects ability to "see" a scene.

In a scene made up of squares as shown in Fig. 1, for example, N_a photon events occur in the white square and N_b events in the gray square. (A photon event may be arrival of a photon or, in the case of a camera tube, emission of a photoelectron.) The difference in brightness between the white area and the gray area is determined as shown by the equations in Fig. 1.

First, it should be noted that the light level on any scene is not constant, but changes in a random manner. A measure of this variation is given by the square root of the number of events. If there are N_a events, therefore, a variation of as much as $\sqrt{N_a}$ can be expected. For instance, if the average number of events in a second is 100, the number in any particular second may be $100 \pm \sqrt{100}$, or from 90 to 110 events (a 10-percent variation). As a result, the difference in brightness between the white and gray squares in Fig. 1 can not be distinguished unless the difference between N_a and N_b is some factor k times greater than the random variation in N_a,[1] as shown by the third equation in the left-hand column.

Although these random variations are not apparent at normal light levels, they become a factor in operation at very low light levels. As mentioned previously, at normal room illumination there are 10 billion photon events per second from a small typed letter; the square root of 10 billion is 100 thousand, and thus the variation is only one one-thousandth of one percent, as compared to the 10 percent variation at low light levels. It can be seen, therefore, that the signal-to-noise ratio of a scene in even a poorly lighted room is much better than that of the same scene under nighttime illumination.

The difference between N_a and N_b can also be considered a contrast difference, as defined in the fourth equation in the left-hand column of Fig. 1. The number of photon events per second n_a is then equal to the square of the certainty factor k divided by the square of the contrast ratio C, the square of the dimension of a resolution element d, and the integration time t, as shown in the top equation in the right-hand column. The physical significance of this equation is that the size of the smallest element which can be resolved increases as the light level is reduced. The pictures of Fig. 2 show how resolution improves with increasing light level.

The limitations on resolution imposed by low light level can be overcome in three ways: 1) by use of a larger-diameter lens to obtain more light for the detector, 2) by use of the most sensitive and efficient detector available, and 3) by integration over a longer period of time.

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A. L. MOREHEAD received the BSEE degree from the University of Minnesota where he graduated with distinction in 1958. From 1958 to 1960 he investigated noise in electron tubes under a research assistantship granted by the EE Department. He received the MS in Electrical Engineering from the University of Minnesota in 1960. The subject of his thesis was "Noise in Field Emission Tubes." In 1960, he was employed by RCA and assigned to the Advanced Development Group of the black and white kinescope section. While in this group, he developed a new electron gun for low power kinescopes. Mr. Morehead was assigned to the Image Tube Design Group in 1961. In 1963, he was promoted to Manager, Image Tube Product Engineering. He assumed his present position as Leader of Low-Light-Level Camera Tube Advanced Development Engineering in 1965. Mr. Morehead is a member of Tau Beta Pi, Eta Kappa Nu, and the IEEE.

Use of a larger-diameter lens is the oldest and easiest of the three possibilities. The diameter of the lens in the eye is approximately 7 millimeters at night. The diameter of the lens of a 7 x 50 binoculars is 50 millimeters. Fig. 3 shows the improved acuity obtained when an observer uses binoculars, as compared to that of the unaided eye.[2] If the field of view of the binoculars is sufficient, this technique is a very good method of improving night-viewing capabilities.

When it is necessary to obtain wider fields of view than binoculars can provide, or when larger lenses are desired, an image tube or a camera tube must be used. The bottom curve in Fig. 3 shows the acuity attained when a 150-millimeter lens is used with a very sensitive imaging tube or camera tube. The improved performance as compared to binoculars results from use of a larger lens to collect more light, and of a more sensitive detector (a photocathode that has an S-20 response rather than the eye).

The use of a more efficient detector makes a significant contribution to better "seeing" at night. The multialkali photosurface, which has an S-20 response, provides two advantages as compared to the human eye. It is more efficient (ranging from 15 to 25 percent at its peak, compared to 5 percent for the eye), and it is sensitive to a wider range of wavelengths (from 3000 to 8500 angstroms). This broader sensitivity allows the use of more of the available radiation and thus provides better statistical averaging. Another advantage is that the efficiency of the photocathode is constant at all light levels.

The use of longer integration time to improve resolution has limited usefulness. This method is equivalent to taking a time exposure with film. Although long-term changes in the scene can be observed, any fast movement of the scene is lost. Astronomers make great use of long integration times for improving the resolution of their pictures. However, it is probably not practical for a nighttime surveillance system in which movement may occur.

CAMERA AND IMAGE TUBES FOR PASSIVE LOW-LIGHT-LEVEL VIEWING

It has been shown that when nighttime surveillance is required and artificial illumination is prohibitive, useful results can be obtained by use of image tubes and camera tubes built to operate at very low light levels. At this point it may be constructive to consider the characteristics of some of these devices.

Most image tubes operate in basically the same manner. A light image from a lens system is projected on the tube. This image is changed to a corresponding electron image inside the tube. The electron image is then amplified and converted back to a visible image, either directly or through a television chain; Fig. 4 shows this operation in more detail. The image intensifier tube shown at the top of Fig. 4 consists of a photocathode, an electron lens, and a phosphor screen. The photocathode converts the light image to an electron image which is focused onto the phosphor screen by the electron lens. The focusing system also accelerates the electrons, increasing their energy from about 1 electron-volt to 10,000 to 15,000 electron-volts depending on the applied voltage. This action provides the gain in the tube. The phosphor screen glows when it is struck, and produces a visible image which is 40 times brighter than the original visible image.

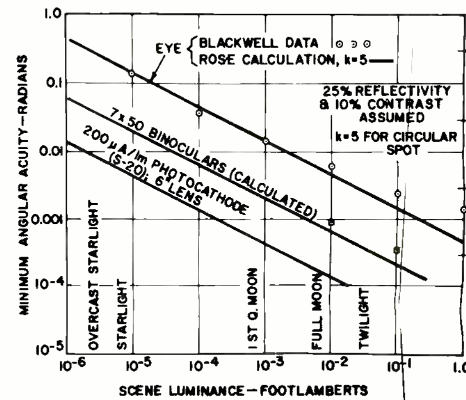

Fig. 3—Resolving capabilities of the eye compared to those of a photocathode detector.

An image intensifier has several useful features. Because there is an electron image between the original image and the image seen by the viewer, electronic processing may be used to alter the output image. The electron beam can be biased off to achieve a shuttering effect. This shuttering can be accomplished in five nanoseconds, a time much shorter than that obtained with mechanical shutters. In addition, the electron beam can be deflected to change the position of the image on the phosphor screen. With appropriate electronic circuits, for example, the image on the phosphor screen can be made to appear stationary, even though the image on the photocathode may be moving. Finally, the wavelength or color of the output image can be made to vary from that of the input; therefore, the tube can be used as a wavelength converter. These features can be useful in several problem areas; the third feature is discused later.

The lower schematic diagram in Fig. 4 shows the operation of an image orthicon. The operation of this type of tube has been described by Rose et al.[3] The light image is projected on the photocathode, which emits electrons in proportion to the brightness of the light. These electrons are focused onto a storage target, which is a thin sheet of glass or a thin semiconductor film. The electrons strike

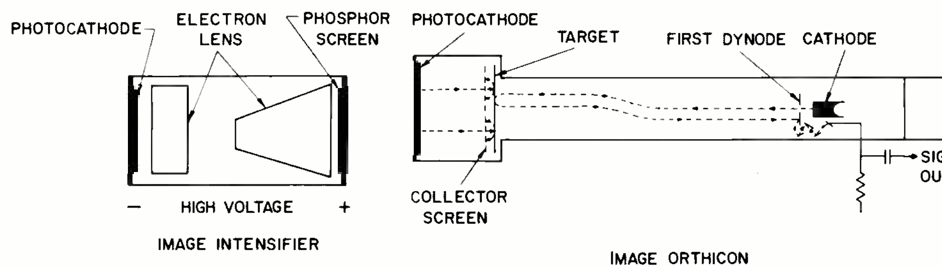

Fig. 4—Schematic representation of image-tube operation.

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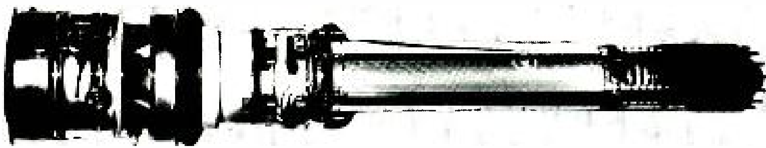

Fig. 5—RCA-4470 intensifier image orthicon.

the storage surface with enough energy to liberate several secondary electrons per primary electron. These secondary electrons are collected by the mesh collector screen; thus a net positive charge accumulates on the storage target. The image section of the image orthicon, therefore, transforms the light image on the photocathode to a charge pattern on the storage target, and provides the gain of secondary emission in the process.

In the reading section of the tube, the electron beam which is scanned across the target detects the charge pattern on the target. In areas where the charge is more positive, a portion of the electron beam lands on the target and neutralizes the charge, while the remainder of the beam returns to the first dynode. In areas where the charge is more negative, fewer electrons land on the target, and more electrons return to the first dynode. The return beam, therefore, provides a video signal corresponding to the charge on the target. This signal is amplified within the tube in the return-beam multiplier, and the output is connected to a television video amplifier for display on a television receiver.

The operation of the vidicon tube is simpler than that of the image orthicon. The vidicon has no image section; instead, the charge image is created directly on a photoconductive storage target by the incident light image. In addition, there is no return-beam multiplier; the video signal is obtained from the target current rather than from the current rejected from the target.

Besides having some of the features of the direct-view tube described previously, the image orthicon and the vidicon provide a video signal which can be used for remote viewing of the scene.

In the RCA-4470 intensifier image orthicon (Fig. 5), an intensifier is coupled to the front of an image orthicon to provide enough gain for operation at the lowest light levels at which a useful signal may be obtained. This coupling is accomplished by placing the phosphor screen of the intensifier on one side of a very thin mica membrane and the photocathode of the image orthicon on the other side; the two tubes are built as one unit. This low-light-level detector, which was described by Morton,[4] was the first of the very-low-light-level camera tubes, and is still the most sensitive camera tube built today. It can be operated in a slightly modified studio television camera; the scanning section of the tube is the same as that of a standard 3-inch image orthicon. The tube is 22 inches long and has a 4-inch diameter at its larger end.

Another common method of coupling tubes for increased gain is to use a fiber-optic plate. Such a plate consists of many light pipes fused together into a large-diameter plate. A typical light pipe, as shown schematically in Fig. 6, consists of a core glass, a clear cladding glass, and an absorbing layer of glass. The indices of refraction of the core and the cladding are selected so that total reflection occurs for a light ray which strikes the boundary between the two. Therefore, any light which enters the core of one pipe remains within that pipe until it reaches the opposite end.

An image tube that uses a fiber-optic faceplate at its screen end can be directly coupled to a camera tube that uses a fiber-optic faceplate, without the need for a lens. Such coupling is very efficient, and resolution loss can be controlled by the size of the light pipes which make up the faceplate. The developmental type RCA Dev. No. C23001 shown in Fig. 7 uses this type of coupling. Although this tube is not as sensitive as the intensifier image orthicon, it is easier to operate, smaller, and more suitable for rugged environments and unattended operation. This tube is 10 inches long and 2.6 inches in diameter. The sensitivity of the intensifier vidicon can be improved by the addition of more intensifier stages.

In addition to the camera tubes described thus far, which provide a television picture of a scene, cascaded image intensifier tubes are very useful for direct viewing of a scene. The direct-view tubes are simpler to operate because there are no scanning circuits or video processing circuits. In addition, because the one tube provides an output image directly, there is no need for a TV monitor, and the power required to operate the tubes is very low. A system using a direct-view tube consists of an objective lens, the tube, a magnifier, and a power supply. The whole system may be hand-held or mounted on a tripod. The developmental type RCA Dev. No. C700-21A three-stage intensifier is 9 inches long and 4.5 inches in diameter. This tube consists of three intensifier stages ... coupled by mica membranes (as ... described for the 4470), and is capable of reproducing scenes at the lowest usable illumination levels.

One measure of the efficiency of low-light-level viewing devices is the resolution obtainable at various illumination

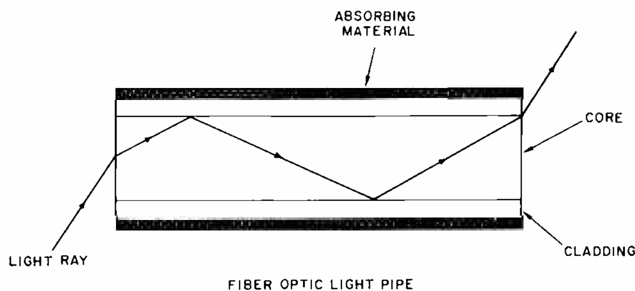

Fig. 6—Schematic representation of a fiber-optic pipe.

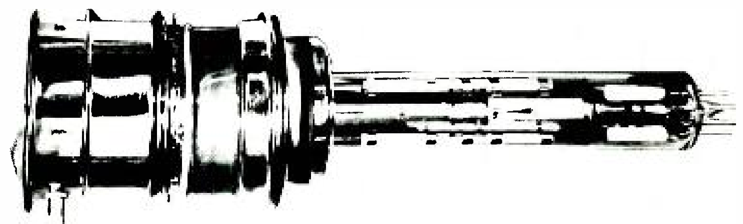

Fig. 7—RCA Dev. No. C23001 intensifier vidicon.

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levels. A chart of resolution as a function of light level on the photocathode is shown in Fig. 8 for the three devices described previously. The nighttime illumination conditions corresponding to the photocathode illumination for a typical lens and contrast ratio are shown at the top of the graph. The resolution is given in line pairs per millimeter. This information can be used to calculate the range at which an object (e.g., a man) can be detected. If a 20-degree field of view is assumed, the curves show that the intensifier image orthicon, an intensifier vidicon with an intensifier gain of 10^5, and the direct-view intensifier can detect a man at 200 yards on a moonless overcast night. The intensifier vidicon, which was shown in Fig. 7 requires quarter-moon illumination to do the same job.

Although viewing systems that use low-light-level tubes are much more sensitive than the human eye, they suffer from many of the same problems. A bright light within the field of view of the system tends to obscure the scene around the light. This effect is much the same as that observed around an oncoming car using bright lights on the highway at night. The tubes are capable of handling brightness differences of about 50 to 1 in the same scene without loss of scene information; above this ratio, some information is lost.

Scene motion can also cause degradation of resolution, especially at the lower light levels. Direct-view tubes are less susceptible to this problem than camera tubes because their speed of response is faster. Camera tubes show the effect more as light level is reduced because of the method in which the target charge image is converted to a visible image. For many surveillance problems, this effect may not be troublesome. For example, some movement such as people walking does not degrade the image beyond usefulness. However, a running person may not be identifiable, even though the viewer would know that someone is there. In addition, the system would probably not be useful for identifying people traveling past the camera in cars.

NON-VISIBLE-RADIATION-SENSITIVE TUBES

Although passive low-light-level systems do a remarkable job within their capibilities, there may be times when the resolution of a low-light-level system is not adequate. The problems of "seeing" inside a totally dark building, of detecting small objects at great distances, and of identifying swiftly moving objects are examples of applications which require illumination. Again, however, the particular problem may require that visible illumination be avoided.

One method of solving this type of problem is to use illumination which is outside the band of wavelengths that are visible to the eye. Fig. 9 shows the wavelength interval over which the eye is sensitive. Therefore, if radiation at wavelengths shorter than 4000 angstroms

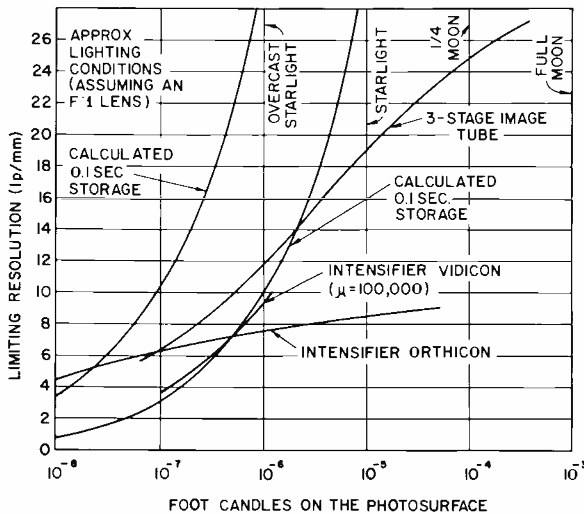

Fig. 8—Resolution of low-light-level image and camera tubes as a function of illumination level.

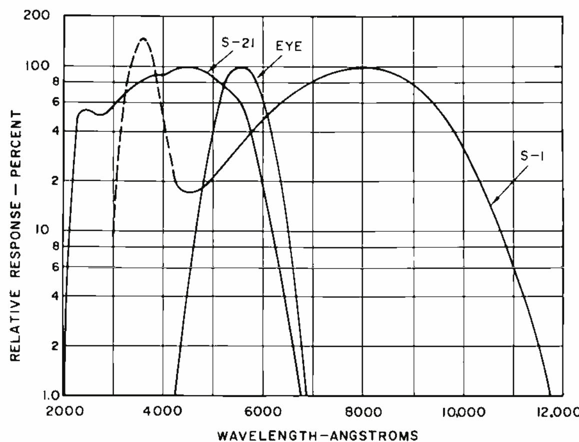

Fig. 9—Spectral response of the eye and photocathodes.

Fig. 10—RCA-6914 and RCA-7404 image converter tubes.

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or longer than 7500 angstroms is used, the "light" is invisible to an observer and the intensity can be quite high.

When such illumination is used, it is necessary to use a suitable detector, such as an image tube, which is sensitive to the invisible radiation and which provides a visible output. Relative spectral sensitivities of such tubes are also shown in Fig. 9. Tubes that have an S-21 response are sensitive to ultraviolet radiation, and those that have an S-1 response are sensitive to infrared radiation.

Two image tubes which have sensitivities in the invisible regions of the spectrum are shown in Fig. 10. The larger of the two tubes shown is an RCA-6914, which has infrared response; the smaller tube is an RCA-7404, which has ultraviolet response. Both tubes are suitable for use in direct-view systems. If the tubes were modified to incorporate fiber-optic output faceplates, they could also be used in conjunction with camera tubes for remote-view applications.

The infrared region is usually more attractive for surveillance work because infrared illuminators are easier to manufacture and more readily available, and because infrared radiation does not cause objects to fluoresce, and thus to reveal that invisible radiation is in use. An additional factor is that ultraviolet radiation is more readily absorbed in the atmosphere and in lenses; as a result, illuminating efficiency is reduced and more power is required.

The main design goals for an active system of this type are high resolution and light weight. The light weight is possible because very large lenses are no longer required to gather enough light. As a result, smaller image formats can be used, and thus the size of the image tube can be decreased. High resolution is possible because illumination no longer limits the resolution to low values; resolving power is determined by the viewing system rather than the light level.

In addition to being useful for surveillance problems, tubes sensitive to invisible radiation can be used in the laboratory. The reflectance of a material is usually dependent on the wavelength of the light being reflected. If two materials have the same reflectance characteristics in the visible spectrum, it is difficult to separate one from the other by eye (this principle is the basis for camouflaging). However, the two materials may not have the same reflectance characteristics in the infrared or the ultraviolet region. One can then be distinguished from the other by use of infrared illumination and an RCA-6914 viewer. Although the use of such a system in the laboratory requires some knowledge of materials and their optical properties; the system is very useful when such information is available.

SUMMARY

The quality of an image obtained at very low illumination levels depends on the quality of the viewing system and on the amount of light collected. For high-quality, high-gain systems, the major limitation to resolving power is the amount of light available. Once this limit is reached, further amplification of the available light does no good because the limitation is in the random fluctuations of the light itself and amplification does not improve the statistical average of these fluctuations. However, the limitation can be overcome by use of a longer averaging time, or a more sensitive detector, or by collection of more light with a larger-diameter lens to improve the statistical averages. At illumination levels below 10^{-4} footcandle, the distance at which an object can be detected is reduced. Low contrast also reduces the working distance of a system.

The intensifier image orthicon can be used with very low levels of illumination. In conjunction with a suitable lens and camera system, this tube can detect a man up to 200 yards away on a moonless night.

A tube which is easier to operate, but less sensitive, is the intensifier vidicon. When this tube is used with a high-quality preamplifier, it can detect a man at 200 yards with illumination of a one-quarter moon.

These devices are suitable for remote surveillance of an area when the purpose is detection of unwanted objects or people without the use of additional illumination. However, they are less suited to following fast-moving objects because they do not respond to movement as quickly at low light levels as at high levels; as a result, the scene becomes blurred. The tubes work best when the brightness range in the scene is less than 50 to 1. Larger ranges (such as that produced by a bright light in a black background) tend to overload the portion of the tube which is brightly illuminated and wash out the picture from other portions of the tube.

Direct-view devices are also available for use at very low light levels. These devices are much simpler in operation, but must be viewed directly. They are useful for direct nighttime surveillance when it is not desirable to illuminate the area.

The major advantages of a viewing system suitable for use at night, as compared to the unaided eye, are a wider field of view and a larger light-gathering capability. Binoculars can provide larger light-gathering ability at the expense of field of view, but a suitable electron-tube system can provide both. Therefore, the low-light-level electron-tube system should be used when these requirements cannot be compromised. (When a wide field of view is not necessary, binoculars may be sufficient.)

In applications where low-light-level illumination does not provide adequate performances, but visible illumination is not desired, infrared or ultraviolet systems may be used. These systems use a tube that has infrared or ultraviolet sensitivity, and need not be extremely sensitive because the invisible radiation can be made adequate. Tubes suitable for use in such systems are the 6914 image tube, which is sensitive in the near-infrared region, and the 7404 image tube, which is sensitive in the ultraviolet region. Both tubes are suitable for use in direct-view systems, or for use in remote-view systems in conjunction with a camera tube. When additional illumination is used, the image tube or the camera-tube system can be smaller; as a result, weight and power requirements can be reduced as compared to systems without additional illumination.

Infrared and ultraviolet-sensitive image tubes can also be used in the laboratory to find traces of certain materials. A material which cannot be seen under visible light may be visible when viewed with infrared or ultraviolet radiation. The reflection factor for infrared or ultraviolet radiation may be different than that for visible light, so that the contrast is enhanced.

Although these viewing devices can be used to provide many unique services to law-enforcement agencies, they must be considered in conjunction with specific applications. Unless a system is tailored to the application, it may be cast aside as a waste and nuisance. To be really useful, a system must be used in an application that requires its particular features. In some applications, for example, additional visible light must be avoided, detection of the observer must be avoided, or electronic "tricks" may be needed to gain useful information.

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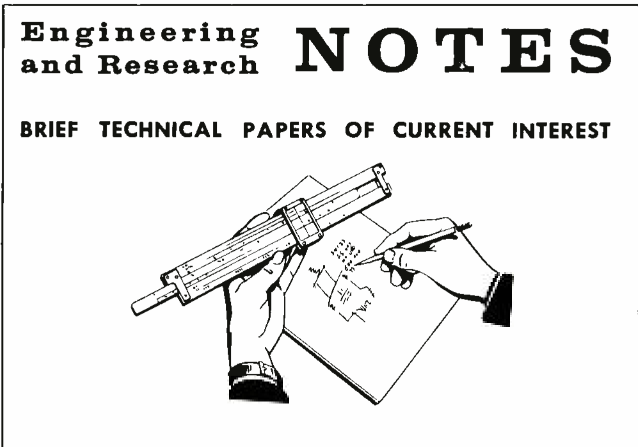

Multivibrator Can Be Remotely Programmed for Various Functions

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With a conventional multivibrator, the remote location of the frequency controls is a problem. The amount of frequency change per control resistor is usually no more than 15:1, the period does not have a linear relationship to the control resistor, and only a square wave output is normally available. With the circuit shown in Fig. 1, controls can be remotely located (Fig. 2A). The amount of frequency change can be as high as 100:1, by changing R_p from 0 to 500 kilohms. (The coarse selection is done via miniature relays, as shown in Figs. 2A and B). The period has a linear relationship to the control resistor (Fig. 3), and the circuit has two available outputs—a square wave and a sawtooth. The sawtooth amplitude varies somewhat with frequency, if Ca and Cb ($C1$ and $C2$ of Figs. 1 and 2 in parallel) are less than 300 pF. The sawtooth output at $Q5$ should be terminated into an impedance > 1 megohm.

The best frequency tracking is obtained with $F_{max} \leq 8$ MHz. When using 51pF for $C1a$ and $C1b$, a small trimmer capacitor (2 to 7 pF) across each should be used to balance both sides of the multivibrator. The output from $Q4$ is terminated into a 3-kilohm resistor to develop voltage levels of equal amplitude above and below ground. (The minimum value for this resistor is 500 ohms.)

Theory of Operation (Fig. 1):

Assume $Q2$ *on* (0 volt) and $Q3$ *off* (+4.5 volts). $C1a$ will discharge through $D6$ and the collector of $Q5$. $Q5$ supplies a constant current source, so $C1a$ can discharge in a linear manner. The current through $Q5$ is adjusted by R_p. Since this is basically a DC adjustment, it can be done remotely (Fig. 2).

With $Q3$ *off*, $Q4$ is *on*. The output (1) is at approximately $-4.2V$, and the anode side of $D9$ is at $-3.6V$. The capacitor $C1a$ cannot discharge through, $D9$, only through $D6$ and $Q5$.

As $C1a$ reaches the turn *on* V_{BF} for $Q3$, $Q4$ begins to turn *off*. The $Q4$ collector goes to $+4.3V$ as $Q3$ turns completely *on*. The anode side of $D9$ goes to $+1.5V$. The base current for $Q3$ is now supplied through $D9$ and the 11 kilohm resistor to $+6V$. In this manner the discharge path for $C1a$ becomes independent of the hold-on current (I_b) path for $Q3$. This makes possible a 50/1 frequency ratio by adjusting R_p.

$Q2$ is now *off*, and $Q3$ *on*. $C1b$ now discharges through $D4$ and $Q5$. The action for the $Q1$, $Q2$ side is the same as described for the $Q3$, $Q4$ side. $D4$ and $D6$ isolate each side of the flip-flop from each other.

Summary:

The capability of a basic multivibrator can be expanded to the following: 1) Its frequency can be adjusted a minimum of 50/1 by one resistor with a frequency accuracy of within 2% at room temperature. 2) The program resistor can be remotely located. 3) The multivibrator can be programmed over a range of 10MHz to 1Hz. (t_R and $t_F \leq 20$ ns). Selection of the proper miniature relay acts as the coarse control.

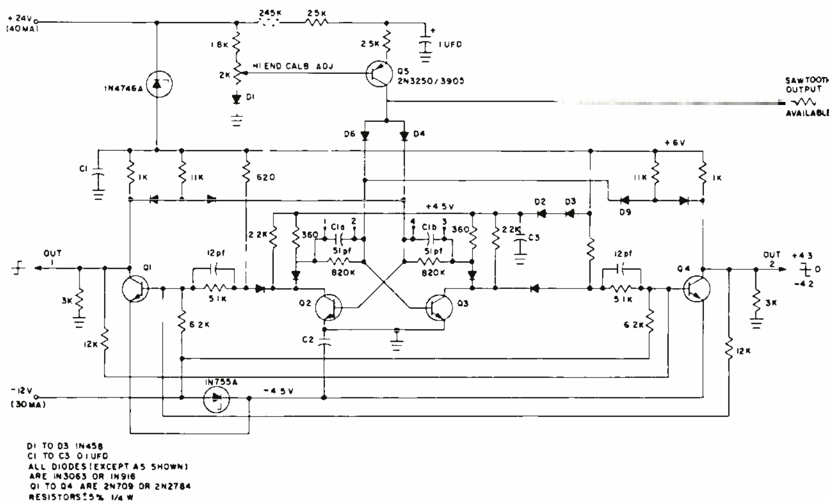

Fig. 1—Schematic diagrams of the multivibrator.

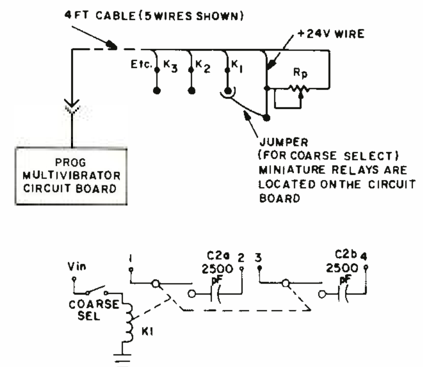

Fig. 2—Remote connections.

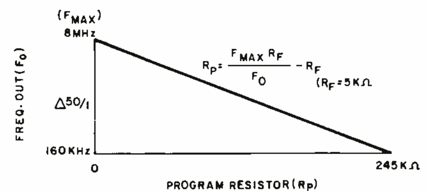

Fig. 3—Frequency versus program resistance.

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What Is Industrial Tube Standardizing?

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Industrial Tube Standardizing is the coordinating activity between design engineering and manufacturing that ensures consistent high quality in RCA's industrial-tube product line. This activity is responsible for organizing engineering data in the form of standardized notices, using language and nomenclature that is universally understood by the supplier of the raw material, Incoming Inspection, the Factory, and the Warehouse. Proper utilization of these notices guarantees a uniform, high-quality product that reaches the customer ready to serve its purpose at a competitive price and yield a profit.

A complete tube-type specification begins with a meeting of representatives from each participating activity, each detailing his department's requirements to meet the engineering design of a new tube. Additional information is obtained from RCA engineers, the PC system, Government Standards, and standards of associations such as the ASTM, CDA, and AISI. After the design meeting, the specification may be changed only by an approved PC (Proposal for Change) as refinements in design are realized. The Standardizing Notice represents the state-of-the-art for industrial tubes made by RCA and constitutes a legal document.

The Industrial Tube Standardizing activity maintains a complete Master Set of the notices issued by the standardizing activities within EC&D. In addition, this department transfers all superseded and recalled notices pertaining to the industrial-tube product to its Permanent File. With these records available, the department can advise engineering what is being done now, and can readily determine what was done at any particular time period during the production of the tube. It should be emphasized that the Standardizing Notice tells only the "what" and "how" of tube manufacture. Supporting data dealing with the "why" of tube building are recorded on the PC. For reference purposes, a file of PC's is maintained on a yearly basis for a ten-year period.

Standardizing maintains an Extra-Copy File of all the active notices pertaining to industrial-tube products. This file consists of 32 four-drawer cabinets containing extra copies of approximately 22,000 notices. These files are used by Standardizing to compile new sets of notices as requested by department managers. The files are also used to supply extra copies of notices to requesting activities for surveys, meetings, preparation of changes, or posting at production stations, as well as submitted to suppliers with orders for materials and parts. Occasionally, during development of a tube, Standardizing is requested to aid engineering in formalizing the product for manufacture by compiling booklets for tubes of a complex design.

Standardizing services 81 sets of notices in the Lancaster complex plus 45 sets of notices in other activities within EC&D. Each department or function receives a set of notices that are specific for that activity. For example, the Phototube Factory receives complete specifications pertaining to phototube information only. Specifications common to two or more products are distributed to the respective departments. When it is realized that Industrial Tube Standardizing services supplies information on ambient-air-cooled power tubes, forced-air-cooled and water-cooled power tubes, vacuum components, image tubes, pickup tubes, vidicons, storage tubes, oscillograph tubes, phototubes, vacuum gauges, super power tubes, and color picture tubes, the distribution system alone must be highly sophisticated.

Standardizing also maintains a "where-used" card file on all parts and assemblies, processes, and tube and parts packing materials. These files enable Standardizing to identify what tubes are involved when a parts change is requested. When the item is used in more than one product line, this file system guarantees that all respective departments are notified of the change. For example, should Power Tube Engineering desire to make a change on a part common also to phototubes, Phototube Design and Manufacture would be made aware of the proposed change for their evaluation. In this manner over-all cost and inventory size are controlled. Standardizing also has a personal interest in the card files. When an item becomes obsolete, the system enables the department to withdraw the standardizing notice from the sets.

How to Use the Standardizing Notice System

Basically, the Standardizing Notice System is a catalog containing 45 sections and grouped generally into 10 classes of information as follows:

Section 1: General Information relative to the system itself. This section consists of a general outline of the system, along with numerical and alphabetical indexes of the Standardizing Notice System, and general explanatory information.
Section 3: Tube Construction Data subdivided by tube classification.
Sections 8 thru 24: Parts and Assembly Drawings (grids, plates, machined parts, bulbs, bases, etc.) *(Except Section 23)*
Section 23: Electrical Ratings and Test Specifications for finished tubes.
Section 25: Shrinkage Symbols, Inspection Procedures, Sampling Tables.
Section 26: General Life-Testing Procedures and Circuit Diagrams.
Section 27: Tube Marking and Branding.
Section 29: Parts and Tube Packing.
Section 33: Material Purchasing, Handling, and Manufacturing Specifications.
Section 34 thru 45: General Detailed Process and Equipment Specifications.

The remaining sections not shown are not being used at present and are left available for future use.

Regardless of what information an engineer wishes to know about a given tube, he should start with Section 3—the Construction Data. It is divided according to product [that is, Phototube (3-1L-(Type), Power Tube (3-1P-(Type), etc.] The pages in this section are filed basically by tube type number, example: 3-1L-926 (P. 2, 3, 3a, 4, 5, 5a, 5b, 6, 7), 3-1L-927 (P. 2, 3, 3a, 4, 4a, 4b, 5, 5a, 5b, 6, 7). The page numbers for a tube also have specific functions, as follows: Page 2 contains special instructions for the manufacture of the specific tube, Page 3 the outline drawing of the tube and tube dimensions, Page 4 the mount drawing, Page 5 contains the sealing instructions, Page 6 the aging specifications and Page 7 the Bill of Materials. (List of the component parts and assemblies required to build the tube).

Example Problems

Suppose an engineer is interested in obtaining processing information on the cathode for tube type 927. Starting with Section 3, Page 7 of 3-1L-927, he scans the left-hand column until he comes to the word—*cathode.*

Reading across from this heading, he sees the part number as well as some pertinent data on the composition of the cathode and various treatment involved in the processing.

If the engineer is interested in specific information on a certain component of the 927 tube (e.g., item 16—the cathode, part number: KS 619), he refers to the nomenclature index (Section 1-1-1) to find the specific section for parts with a KS prefix. The numeric portion of the cathode part number (619) corresponds to the page number in the cathode section of the notices. On this page he finds all of the criteria involved in processing the cathode for the 927 tube type. This method is direct and should take no more than a few minutes to obtain any standardizing information desired on a specific tube.

Industrial Tube Standardizing is a service-oriented function. Its procedures have been developed through the years by people who have been, and are, devoted and dedicated to the work. The system is for you. Please use it to the fullest advantage.

Determination of Modulation Index from Carrier-to-Sideband Ratio

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In phase modulated systems, it is often desirable to determine the modulation index without the aid of a coherent CW signal. A popular method is to observe the carrier-to-first-sideband ratio (R) on a spectrum analyzer where R (dB) $= 20 \log [J_0(X)/J_1(X)]$, where X is the modulation index in radians. The curve shown in Fig. 1 allows direct conversion without the need of tables. For example, a difference of 14.9 dB would indicate a modulation index of 20°, or 40°, peak to peak.

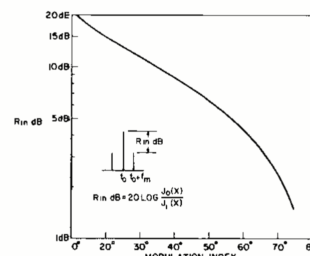

Fig. 1—Carrier-to-sideband ratio versus modulation index in phase-modulated systems.

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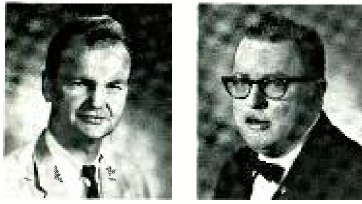
A New Type of Latching Switchable Ferrite-Junction Circulator



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and W. A. SCHILLING

The Microwave Applied Research Laboratory has recently demonstrated a new type of extremely compact, latching, microwave ferrite junction circulator that can be switched in approximately two microseconds and requires only tens of microjoules of switching energy.

The circulator, illustrated schematically in Fig. 1, employs magnetically closed ferrite assemblies that are put into operation by a pulse of direct current through a wire loop that surrounds a portion of the magnetic circuit. Each assembly provides a closed magnetic path through the ferrite cylinder and ring, and two ferrite or high-remanence metal discs. As a result of magnetic closure, the ferrite operates at remanence after termination of the current pulse. The internal DC magnetization required for circulation is provided by the remanent magnetization without need for an external permanent magnet. Switching (i.e., reversal of isolated and transmitting ports) is achieved by reversing the polarity of the current pulse.

The ferrite materials used in the circulator must have high (greater than 0.7) squareness (remanence-to-saturation) ratios, as in other types of latching devices, such as phase shifters.[1]

The significant difference between the new type of circulator and previous latching configurations[2-6] is the placement of the entire DC magnetic circuit within the region of circulation, and achievement of circulation by use of ferrite assemblies having opposite directions of DC magnetization. These features result in very small size and switching energy for this new type of circulator. Fig. 2 is a photograph of an experimental latched circulator that operates at frequencies of about 7.3 GHz.

To verify the principle of operation, the initial experiments were performed by use of high-remanence metal discs for the transport of flux between the ferrite cylinder and ring. Such a design is best suited for applications requiring only occasional switching because switching time is limited to tens of microseconds by eddy currents in the metal discs. The 20-dB isolation bandwidth for the ferrite-metal-disc assemblies was approximately 4%, the center frequency was 7.325 GHz, and the insertion loss was 0.25 dB. This isolation bandwidth was increased to 8.2% by use of a triple-stub tuner in the transmitting arm.

For applications requiring fast, low-energy switching, it is necessary to employ ferrite discs for flux transport between the cylinder and the ring (Fig. 1).

The 20-dB isolation bandwidth for a circulator similar to that shown in Fig. 2, but employing all-ferrite assemblies and stub tuners for RF impedance matches, was 4.1%. The switching time and energy for this circulator were 2 microseconds and 25 microjoules, respectively.

On another assembly, which used all-ferrite components and quarterwavelength transformers, a 20-dB isolation bandwidth from 5.345 to 5.455 GHz (2%) and an insertion loss of 0.4 dB were measured. The linear dimensions of this circulator were approximately 25% larger than those shown in Fig. 2. The switching time and energy for the circulator were respectively 2 microseconds and 9 microjoules. This switching energy was lower than that given for the circulator described previously because the coercive force of the ferrite and, therefore, the area of the B-H loop were significantly smaller.

Operation of the latched circulator that used high-remanence metal discs was also demonstrated in a tunnel-diode amplifier. This amplifier had a maximum gain of 18 dB and a 3-dB bandwidth from 7.210 to 7.460 GHz. Switching of the circulator was also demonstrated with this amplifier.

Acknowledgement: The authors thank H. K. Jenny and Dr. F. Sterzer for guidance in the course of the project, and F. E. Vaccaro for performing the experiments with the tunnel-diode amplifier.

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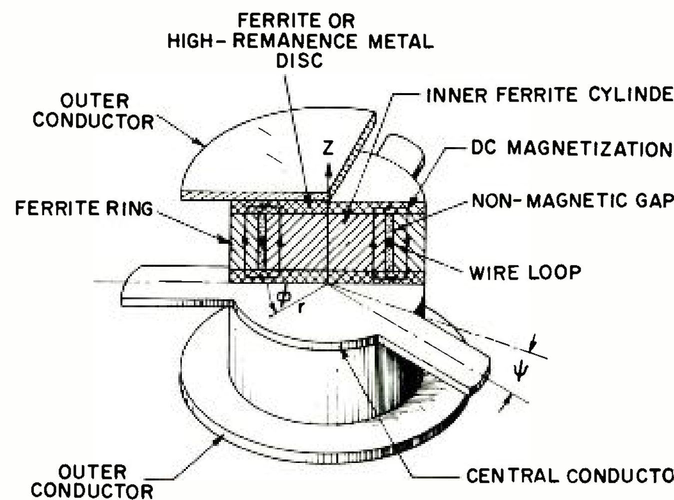

Fig. 1—Schematic representation of the latched circulator.

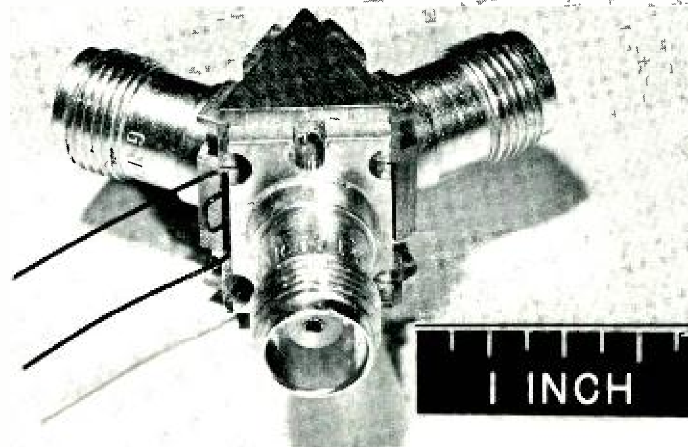

Fig. 2—Latched circulator.

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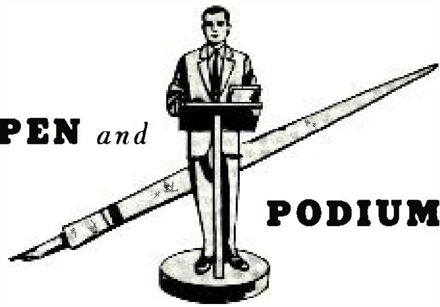

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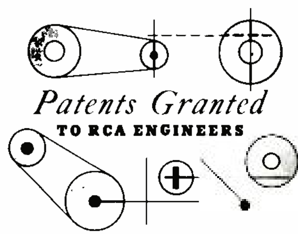

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Stabilizing Coatings for Semiconductor Device—N. H. Ditrick (ECD, Som) U.S. Pat. 3,334.281, August 1, 1967

Method of Isolating Chips of a Wafer of Semiconductor Material—D. N. Kenney (ECD, Som) U.S. Pat. 3.332,137, July 25, 1967

Shadow Mask Frame with Curved Supporting Flange Paralleling Screen Surface—R. C. Demmy (ECD, Lanc) U.S. Pat. 3,333,134, July 25, 1967

BROADCAST COMMUNICATIONS PRODUCTS DIVISION

Transistorized Preamplifier for Television Cameras—B. S. Vilkomerson (BCD. Cam) U.S. Pat. 3.341,655, Sept. 12, 1967

Pulse Counter—R. N. Hurst (BCD, Cam) U.S. Pat. 3,341,693, Sept. 12, 1967

Coaxial Resonator Apparatus—R. N. Clark (BCD, Gibbs) U.S. Pat. 3,325,746, June 13, 1967 (assigned to U.S. Gov't)

Frequency Multiplier—F. A. Barton, C. B. Leuthauser (BCD, M.L.) U.S. Pat. 3,337,791, August 22, 1967

Line Blanking Apparatus for Color Bar Generating Equipment—R. R. Brooks (BCD, Cam) U.S. Pat. 3,334,178, August 1, 1967

RCA LABORATORIES

Adaptive Semiconductor Device—J. O. Kessler (Labs, Pr) U.S. Pat. 3,341,821, Sept. 12, 1967

Pick Up Tube with Infra-Red Sensitive Thermionic Cathode with Cooling Means Spaced from the Thermionic Cathode—G. A. Morton, G. L. Krieger (Labs. Pr) U.S. Pat. 3,333,133, July 25, 1967 (assigned to U.S. Gov't)

Memory Circuits Employing Negative Resistance Elements—J. C. Miller (Labs, Pr) U.S. Pat. 3,339,185, August 29, 1967

Serial Memory of Anisotropic Magnetostrictive Material Accessed by Stress Wave—H. Weinstein (Labs, Pr) U.S. Pat. 3,339,188, August 29, 1967

Imbedded Loop Conductor Magnetic Memory—M. M. Kaufman (Labs, Pr) U.S. Pat. 3,339,190, August 29, 1967

Method of Making Magnetic Material with Pattern of Embedded Non-Magnetic Material—R. L. Noack (Labs, Pr) U.S. Pat. 3,333,333. August 1, 1967

Method of Making Magnetic Body with Pattern of Embedded Non-Magnetic Material—J. A. Kuliczkowski, C. Wentworth (Labs, Pr) U.S. Pat. 3.333,334, August 1, 1967

Electrostatic Printing—R. G. Olden (Labs, Pr) U.S. Pat. 3,333,572, August 1, 1967

Electrophotographic Developing—E. C. Giaimo, Jr. (Labs, Pr) U.S. Pat. 3,333,958, August 1, 1967

Unipolar Transistor Having Plurality of Insulated Gate-Electrodes on Same Side—S. R. Hofstein (Labs, Pr) U.S. Pat. 3,333,168, July 25. 1967

COMMUNICATIONS SYSTEMS DIVISION

Register Position in a Multi-State Switching Network—J. A. Ceonzo, L. Stambler, A. Weiss (CSD, N.Y.) U.S. Pat. 3,290.446, December 6, 1966 (assigned to U.S. Gov't)

Multi-Stage Switching Network—J. A. Ceonzo, L. Stambler, A. Weiss (CSD, N.Y.) U.S. Pat. 3,317,897, May 2, 1967 (assigned to U.S. Gov't)

Signal Distortion Detection by Sampling Digital Diphase Signals at Twice the Bit Repetition Rate—G. J. Meslener, C. R. Atzenbeck (CSD, N.Y.) U.S. Pat. 3,335,224, August 8, 1967

Multilayer Circuit Board Structures—R. A. Mandeville (CSD, Camb.) U.S. Pat. 3,334,275, August 1, 1967

Harmonic Generator with Non-Linear Devices Operating in the Same Mode at a Fundamental Frequency and a Harmonically Related Frequency—B. Polin, O. J. Hanas (CSD, Cam) U.S. Pat. 3,334,295, August 1, 1967

WEST COAST DIVISION

Rotating Random Access Card Selection System—L. W. Bleiman (WCD, VanNuys) U.S. Pat. 3,343,149, Sept. 19, 1967

HOME INSTRUMENTS DIVISION

Electric Motor—J. A. Tourtellot (HI, Indpls) U.S. Pat. 3,341,723, Sept. 12, 1967

Adjustable Voltage Supply—B. E. Denton (HI, Indpls) U.S. Pat. 3,339,103, August 29, 1967

Semiconductor Filter Circuit—J. B. Beck (HI, Indpls) U.S. Pat. 3,335.355, August 8, 1967

MISSILE & SURFACE RADAR DIVISION

Reciprocal Latched Ferrite Phase Shifter—W. W. Siekanowicz, W. A. Schilling, I. Bardash (MSR, Mrstn) U.S. Pat. 3,340,484, Sept. 5, 1967

ADVANCED TECHNOLOGY

Electrical Circuit—R. H. Bergman (AT, Cam) U.S. Pat. 3,339,089, August 29, 1967

Electronically Variable Delay Line—J. F. Schanne (AT, Cam) U.S. Pat. 3,333,110, July 25, 1967

RECORD DIVISION

Endless Tape Cartridge—H. E. Roys (Rec, Indpls) U.S. Pat. 3,337,150, August 22, 1967

ELECTRONIC DATA PROCESSING

Document Stacker—T. J. Misbin, D. M. Fisher (EDP, Cam) U.S. Pat. 3,333,843, August 1, 1967

AEROSPACE SYSTEMS DIVISION

Pulse Discriminator Employing Delay Lines and Threshold-Circuit for Selecting Pulses of Certain Widths and Amplitudes—M. J. Cantella (ASD, Burl) U.S. Pat. 3,315,168, April 18, 1967 (assigned to U.S. Gov't)

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Meetings

NOV. 1-3, 1967: **Northeast Research & Engrg. Meeting (NEREM)**, New England Sections, Boston-Sheraton Hotel, Boston, Mass. **Prog. Info.:** W. E. Morrow, Jr., MIT Lincoln Lab., Lexington, Mass. 02173.

NOV. 2-5, 1967: **Fall Product Assurance Conf.**, Met. N.Y. Sections, et al., Waldorf Astoria, N.Y.C. **Prog. Info.:** Richard Jacobs, Westinghouse Elevator Div., Jersey City, N.J.

NOV. 6-8, 1967: **Conference on Speech Communication and Processing**, G-AE, AFCRL, Kresge Aud., Cambridge, Mass. **Prog. Info.:** B. Gold; C. P. Smith, AFCRI (CRBS), L. G. Hanscom Field, Bedford, Mass. 01730.

NOV. 6-8, 1967: **Basic Telecommunications—Evaluating and Improving the Voice and Message Services**, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 6-8, 1967: **Reliability Physics Symposium**, G-ED, G-R Statler Hilton Hotel, Los Angeles, Calif. **Prog. Info.:** George Jacobi, Illinois Inst. of Tech. Res. Inst., 10 W. 35th Street, Chicago, Illinois 60616.

NOV. 8-10, 1967: **Computer Applications —Management of Computer Programming Projects**, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 9-10, 1967: **Western Conference on Broadcasting**, G-B, Ambassador Hotel, Los Angeles, Calif. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y. 10017.

NOV. 13-15, 1967: **Organizing & Managing Engineering Projects**, Lord Simcoe Hotel, Toronto, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 13-16, 1967: **Engineering in Medicine & Biology Conf.**, G-EMB, JCEMB, Statler Hilton Hotel, Boston, Mass. **Prog. Info.:** David Geselowitz, Moore Sch. of E.E., Univ. of Penna., Phila., Pa.

NOV. 14-16, 1967: **Fall Joint Computer Conf.**, G-C, AFIPS, Anaheim Convention Center, Anaheim, Calif. **Prog. Info.:** H. T. Larson, Philco-Ford Corp., Ford Rd., Newport Beach, Calif.

NOV. 15-17, 1967: **Utilizing the Techno-Economic Appraisal**, New York, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 20-22, 1967: **Data Automation**, New York, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **Configuration Management**, Business Information Systems, Los Angeles, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **EDP/Scheduling, Computer Applications & Management**, Los Angeles, American Management Association, 135 W. 50th Street, New York City, N.Y.

PROFESSIONAL MEETINGS

DATES AND DEADLINES

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

NOV. 29-DEC. 1, 1967: **Effective Supervision of the Engineering Project**, Research and Development, New York, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **Evaluation & Measurement of the Research & Development Program**, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **Creating & Evaluating Research Projects**, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **Finding, Screening & Appraising New Products**, American Management Association, 135 W. 50th Street, New York City, N.Y.

NOV. 29-DEC. 1, 1967: **Fundamentals of R & D Management for Newly Appointed First-Line Supervisors**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 4-6, 1967: **Microfilm—Microfilm Information Retrieval Systems**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 4-6, 1967: **Documentation—Development Effective Standards and Documentation for EDP Applications**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 4-6, 1967: **Managing the Product Development Department**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 5-7, 1967: **Vehicular Conference**, G-V, New York Hilton, New York. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

DEC. 11-13, 1967: **Managing the Product Development Department**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 11-13, 1967: **Research Project Management**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 20-22, 1967: **Management Information Systems—Planning and Implementing Computer-Based Management Information Systems**, American Management Association, 135 W. 50th Street, New York City, N.Y.

DEC. 20-22, 1967: **Finding, Screening & Appraising New Products**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 8-10, 1968: **Computer Applications—Management of Computer Programming Projects**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 8-10, 1968: **Data Automation—Source Data Automation and Input Systems for Data Processing**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 8-10, 1968: **EDP/Inventory & Production Control—Designing EDP and Management Information Systems for Production and Inventory Control**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 8-10, 1968: **EDP/Maintenance—EDP Applications for Managing Maintenance Systems**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 8-10, 1968: **Managing & Measuring Engineering Effort**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 10-12, 1968: **Information Retrieval —Indexing and Search Techniques**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 15-17, 1968: **Effective Technical Service—Improving Coordination and Communication between the Technical Service and Marketing Efforts**, American Management Association, 135 W. 50th Street, New York City, N.Y.

JAN. 16-18, 1968: **Symposium on Reliability**, G-R, ASQC et al., Sheraton Boston Hotel, Boston, Mass. **Prog. Info.:** V. R. Monshaw, Astro-Electronics Div., RCA, P.O. Box 800, Princeton, N.J.

JAN. 31-FEB. 2, 1968: **The R&D Manager's Responsibilities for Technical Recruiting & Staffing**, American Management Association, 135 W. 50th Street, New York City, N.Y.

FEB. 13-15, 1968: **Aerospace & Electronic Systems Winter Conv. (WINCON)**, G-AES, L.A. Council, International Hotel, Los Angeles, Calif. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

FEB. 14-16, 1968: **Int'l Solid State Circuits Conf.**, SSC Council Phila. Section, Univ. of Penna., Univ. of Penna. & Sheraton Hotel, Phila., Pa. **Prog. Info.:** R. L. Petritz, Texas Inst. Inc., P.O. Box 5012, Dallas, Texas 75222.

FEB. 28-MAR. 1, 1968: **Scintillation & Semiconductor Counter Symp.**, G-NS, U.S. Atomic Energy Commission, NBS, Shoreham Hotel, Washington, D.C. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

MAR. 18-21, 1968: **IEEE Int'l Convention & Exhibition**, IEEE, Coliseum & N.Y. Hilton Hotel, New York, N.Y. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

APR. 3-5, 1968: **Int'l Magnetics Conference (INTERMAG)**, G-MAG, Sheraton Park Hotel, Washington, D.C. **Prog. Info.:** Philip Cohen, Magnetics Inc., Butler, Penna. 16001.

APR. 9-11, 1968: **Nat'l Telemetering Conf.**, G-AES, G-COM Tech, Shamrock Hilton Hotel, Houston, Texas. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

APR. 23-26, 1968: **Cybernetics Conference**, German Sec. of IEEE, DGK, NTG, Munich, F.R. Germany. **Prog. Info.:** H. H. Burghoff, 6 Frankfurt/Main 70, F.R. Germany, Stresemann Allee 21, VDE-Haus.

APR. 30-MAY 2, 1968: **Spring Joint Computer Conference**, G-C, AFIPS, Atlantic City, New Jersey. **Prog. Info.:** AFIPS Hdqs., 345 E. 47th Street, New York, N.Y.

MAY 6-7, 1968: **Human Factors in Electronics Symposium**, G-HFE, Marriott Twin Bridges Motor Hotel, Washington, D.C. **Prog. Info.:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

MAY 6-8, 1968: **Aerospace Electronics Conference (NAECON)**, G-AES, Dayton Section. **Prog. Info.:** IEEE Dayton Office, 124 E. Monument Ave., Dayton, Ohio 45402.

Calls For Papers

JAN. 26-FEB. 2, 1968: **Winter Power Meeting**, G-P, Statler Hilton Hotel, New York, N.Y. **Deadline Info.: 10/30/67 (papers) to:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

SPRING 1968: **14th National ISA Analysis Instrumentation Symposium**, Philadelphia, Pa. **Deadline Info.: (abstract) 4 months prior to meeting to:** Dr. Lewis Fowler, Division Director, Monsanto Co., 1700 S. 2nd Street, St. Louis, Mo.

APR. 17-19, 1968: **Southwestern IEEE Conference & Exhibition (SWIEEECO)**, Region 5, Houston Convention & Exh. Ctr., Sheraton-Lincoln Hotel, Houston, Texas. **Deadline Info.: 11/1/67 (abstract) to:** J. V. Leeds, Jr., Rice Univ., P.O. Box 1892, Houston, Texas 77001.

APR. 30-MAY 2, 1968: **Spring Joint Computer Conference**, AFIPS, Atlantic City, N.J. **Deadline Info.: 5 copies of preliminary by 10/30/67 to:** Prof. T. R. Bashkow, Techn. Prog. Committee Chairman, 1968 SJCC, Department of Electrical Engineering, 1312 S.W. Mudd, Columbia University, New York, N.Y. 10027.

JUNE 23-28, 1968: **Summer Power Meeting**, G-P, Sherman House, Chicago, Ill. **Deadline Info.: 2/9/68 (papers) to:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y. 10017.

JAN. 26-31, 1969: **Winter Power Meeting**, G-P, Statler-Hilton Hotel, New York, N.Y. **Deadline Info.: 9/13/68 (papers) to:** IEEE Headquarters, 345 E. 47th Street, New York, N.Y.

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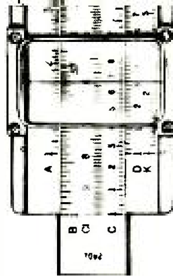
Engineering  NEWS *and* HIGHLIGHTS

WENDELL C. MORRISON APPOINTED STAFF VICE PRESIDENT OF PRODUCT ENGINEERING

Wendell C. Morrison has been appointed Staff Vice President, Product Engineering, by **Dr. G. H. Brown,** Executive Vice President, Research and Engineering. Mr. Morrison, previously Director, Product Engineering, assumes the post vacated when D. F. Schmit retired (see pp. 48 and 49, Vol. 13, No. 2 of the RCA ENGINEER).

Reporting to Mr. Morrison are the following Product Engineering Staff Activities: **S. H. Watson,** Mgr., Standardizing; **J. P. Veatch,** Director RCA Frequency Bureau; **H. E. Schock, Jr.,** Administrator, General Product Assurance; **W. O. Hadlock,** Mgr., RCA Staff Technical Publications; **G. A. Keissling,** Mgr., Product Engineering Professional Development; and **J. W. Wentworth,** Mgr., Engineering Educational Programs.

Mr. Morrison joined RCA in 1940 after receiving his BSEE and MSEE from the State University of Iowa. He was a member of the Technical Staff of RCA Laboratories, Princeton, N.J., for 15 years, engaged in development work in such fields as UHF-TV transmitters, antenna pattern calculators, and color TV terminal and test equipment. In 1957, he became a Staff Engineer for the former RCA Industrial Electronic Products organization, and, in 1959, was promoted to Manager, Engineering Plans and Services. Two years later, Mr. Morrison was designated Assistant to the Chief Defense Engineer of RCA Defense Electronic Products. In 1963, he was appointed Chief Engineer for the Broadcast and Communications Products Division. In 1966, he was appointed Director of Product Engineering. The Institute of Electrical and Electronics Engineers named Mr. Morrison a Fellow in 1963 for "significant contributions to the fields of VHF, UHF and color television." He is also a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi.

W. C. Morrison

SERVICE COMPANY ACTIVE IN UNDERSEA TECHNOLOGY

In the "tongue of the ocean" area of the Bahamas, where the waters are 4800 to 6000 feet deep, the U. S. Navy is conducting the Atlantic undersea test and evaluation (AUTEC) program under a 20-year agreement with the United Kingdom.

The main base of the Project is on Andros Island, largest of the Bahamas, about 33 air miles from Nassau. Five self-sufficient downrange sites—Salvador Point, Big Wood Cay, Golding Cay, Deep Creek, High Point Cay—are accessible by helicopter or boat.

This 130-million-dollar complex is maintained and operated by RCA Service Company's Government Services organization. Under a 3-year contract to the U. S. Navy, the RCA Service Company has assumed responsibility for all technical support of the systems on the three ranges. In addition, they provide data gathering support for weapons tests—including computer programming and operation, communications equipment installation and maintenance, and the operation of repair and modification shops. The group also operates public works functions and furnishes local dining, medical services and supply support.

The AUTEC contract is viewed as especially significant to RCA Service Company because of the wide spectrum of technical disciplines and specialists involved and the special management challenge inherent in operating instrumentation in a tropical environment.

The contract is also significant because it represents an additional commitment to the Government's programs in underseas technology. This is a field in which the RCA Service Company has already gained considerable reputation by participating in the underwater communications studies and assisting the Navy at the Atlantic Fleet Weapons Range and the Naval Ordnance Test Station.

PROFESSIONAL EXCELLENCE AWARD TO R. NOTO

Richard Noto of DEP Advanced Technology, received an individual award in the Professional Excellence Program, sponsored by the Engineering Department of the West Coast Division, Van Nuys, California. The presentation was made by **R. H. Aires,** Chief Engineer of WCD. Mr. Noto was cited for his outstanding performance on the 4101C integrated circuit computer project, where his responsibilities were the coordination of the design automation, artwork generation, platter fabrication, discrete wiring and quality control of the six backplane platters. Six RCA divisions were involved in this task. Through the outstanding personal efforts of Mr. Noto, the extremely tight program schedule was met within the cost estimate. Key personnel who contributed to the successful completion of the project were: **A. J. Carusi, L. J. Cohen, F. Devenny,** EDP; **J. G. Eife, D. P. Schnorr,** CE; and **D. J. Green, L. Pryzwara,** CSD.

THE 1968-1969 DAVID SARNOFF FELLOWSHIP PROGRAM

Applications for the 1968-1969 David Sarnoff Fellowship Program for RCA employees are now open, according to **Dr. Douglas H. Ewing,** Chairman of the RCA Education Committee.

The Fellowships were established in 1956 in honor of the Chairman of the Board of RCA and to commemorate his 50 years in the radio-television-electronics business. These are the top educational awards available to RCA employees and are awarded each year to outstanding employees selected to work toward post-graduate degrees at approved universities.

Fellowships are awarded in the field of Science and Engineering, in Business Administration, and in Dramatic Arts or Journalism. The Fellowship in Dramatic Arts or Journalism is designed for award to an employee of NBC. The other Fellowships are open for application by all employees of RCA and subsidiaries.

The Fellowship is granted for one academic year, but application may be made for renewal for one additional year. Employees awarded these Fellowships are given leaves of absence without pay for the duration of the award.

The stipend granted to a recipient of a David Sarnoff Fellowship is \$3100 to \$5000, depending on marital status, in addition to RCA payment of full tuition and allowance toward purchase of textbooks. The unmarried employee is granted \$3100 for the academic year, a married employee without a child \$3750, and a married employee with children will receive \$5000. An undesignated gift of \$1000 also is made to the university where the recipient studies.

Recipients are selected by the RCA Education Committee on the basis of academic aptitude, promise of professional achievement, and character. Employees who apply for these Fellowships must have demonstrated ability in Science, Engineering, Business Administration, Dramatic Arts, or Journalism and must qualify for graduate study in a graduate school acceptable to the RCA Education Committee. Preference will be given to Science and Engineering applicants who have indicated, by successful completion of courses at graduate level, their ability to proceed on a doctoral program. In the case of Business Administration and Dramatic Arts or Journalism applicants, the end degree need not necessarily be the doctorate.

The head of the employee's division or subsidiary will nominate outstanding candidates to the RCA Education Committee. Awards will be announced in February, 1968.

ABOUT THIS ISSUE

Our thanks go to **I. Kalish, C. A. Meyer,** and **C. Dunaieff** for their efforts in the early planning, expediting, and coordinating of this issue of the RCA ENGINEER. Thanks also go to **E. W. Conley** and **J. Flannery** who provided the photomask artwork used on the cover.

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STAFF ANNOUNCEMENTS

W. W. Watts, Group Executive Vice President, appointed **B. Kreuzer** Division Vice President and General Manager, Broadcast and Communications Products Division.

A. K. Weber, Vice President, Defense Electronic Products, appointed **C. S. Constantino** General Manager, Astro-Electronics Division.

G. H. Brown, Executive Vice President, Research and Engineering, appointed **W. C. Morrison** Staff Vice President, Product Engineering.

W. G. Hartzell, Manager, announced the organization of Microwave Devices Operations Department, Industrial Tube Division, RCA Electronic Components and Devices, as follows: **W. E. Breen,** Manager, Pencil Tube Operation; **L. J. Caprarola,** Manager, Special Components Operations; **R. C. Fortin,** Manager, Microwave Quality and Reliability Assurance; **N. S. Freedman,** Administrator, Special Engineering Projects; **H. K. Jenny,** Manager, Microwave Solid State Devices Operation; **H. M. Learner,** Manager, Traveling-Wave Tube Operation; **R. H. Myers,** Manager, Microwave Plant Accounting; and **A. Rau,** Manager, Microwave Operations Services.

L. W. Grove, Manager, announced the organization of Development Services and Display Tube Operation, Conversion Tube Operations Department, Industrial Tube Division, RCA Electronic Components and Devices, as follows: **C. P. Hadley,** Engineering Leader, Chemical Electronics and Materials; **M. D. Harsh,** Engineering Leader, Product Engineering Display Tubes; **J. G. Kindbom,** Manager, Production Engineering—Display Tubes; **J. L. King,** Manager, Development Services Fabrication; **R. L. Youngquist,** Superintendent, Display Tube Manufacturing; and **J. A. Zollman,** Engineering Leader, Tube Structures and Fabrication Shop Engineering.

T. E. Yingst, Manager, Power Devices Engineering, Industrial Tube Division, RCA Electronic Components and Devices, appointed **G. Y. Eastman** Manager, Heat Transfer Engineering.

J. V. Regan, Director, Patent Operations, Research and Engineering, announced the organization of Patent Operations as follows: **G. H. Bruestle,** Manager, Patents—Electronic Components and Devices; **H. Christoffersen,** Manager, Patents—Electronic Data Processing; **P. G. Cooper,** Manager, Management Information Systems—Patents; **M. J. Ellman,** Staff Patent Counsel—International; **E. J. Norton,** Manager, Patents—Engineering Products; **A. Russinoff,** Staff Patent Counsel—Domestic; **E. M. Whitacre,** Manager, Patents—Home Instruments; and **M. S. Winters,** Manager, Patent Plans and Services.

G. H. Bruestle, Manager, Patents—Electronic Components and Devices, appointed **L. Greenspan** Resident Senior Patent Counsel—Lancaster.

J. Hillier, Vice President, RCA Laboratories, announced the appointment of **A. N. Curtiss** Staff Vice President, Administration, and **J. A. Rajchman** Staff Vice President, Data Processing Research.

B. G. Curry, Director, Management Information Systems Programs, appointed **J. F. Griffin** Manager, Information Systems Projects. **F. F. Tetz** continues Administrator, Information Systems Projects and reports to the Manager, Information Systems Projects.

F. L. McClure, Staff Vice President, Organization Development, appointed **J. J. League** Administrator, Professional Employment and Organization Development.

... PROMOTIONS ...
to Engineering Leader & Manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parentheses.

RCA Service Company

- **R. W. Dunivant:** from Ldr., Engrs.—BMEWS to *Mgr., System Maintenance Analysis* (D. L. Lyndon, Greenland)
- **K. W. Hargus:** from Engr. to *Ldr., Engrs.* (O. E. Cole, Kwajalein)
- **B. A. Barnwell:** from Engr. to *Ldr., Engrs.* (G. M. Powers, Andros Island)
- **T. J. O'Brien:** from System Service Engr. to *Ldr., System Service Engrs.* (W. Hayford, Camden)
- **J. E. Reeder:** from Ldr., Engrs. to *Mgr., Elec. Systems* (T. J. Barry, Springfield, Va.)
- **D. Kennedy:** from Engr. to *Ldr., Engrs.* (J. Haik, Greenbelt, Md.)
- **J. S. Warren:** from Ldr., Mass Services to *Mgr., Satellite Orbit Analysis* (A. S. Porter, Florida)
- **J. B. Vilmerding:** from Sr. Systems Analyist to *Mgr., Signature Processing* (Dr. J. R. Garrett, Florida)

Electronic Data Processing

- **S. J. Pelish:** from Class "A" Engr. to *Ldr., Des. & Dev. Engs.* (B. I. Kessler, Camden)
- **D. Q. Harper:** from Sr. Mbr., D&D Engrg. to *Ldr., Tech. Staff* (H. N. Morris, Florida)

Broadcast and Communications Division

- **J. W. Coleman:** from "AA" Engr. to *Ldr., Des. & Dev. Eng.* (N. Vander Dussen, Camden)

Electronic Components and Devices

- **W. Caton:** from Engr., Product Dev. to *Ldr., Product Dev.* (H. J. Wolkstein, Harrison)

Communications Systems Division

- **J. V. Fayer:** from "A" Engr. to *Ldr., Des. & Dev.* (T. L. Genetta, Camden)

West Coast Division

- **J. Rester:** from Sr. Mbr., D&D Engrg. Staff to *Ldr., D&D Engrg. Staff* (J. Parsons, Van Nuys)
- **R. Egermeier:** from Staff Engrg. Scientist to *Mgr., Elec. D&D* (J. Parsons, Van Nuys)
- **R. Morris:** from Sr. Mbr., D&D Engrg. Staff to *Ldr., D&D Engrg. Staff* (J. Parsons, Van Nuys)

Advanced Technology

- **G. T. Burton:** from Engr., D&D Anal. or Res. A to *Ldr., D&D Engr.* (D. J. Parker, Camden)

Aerospace Systems Division

- **T. E. Nolan:** from Sr. Proj. Mbr., T.S. to *Ldr., T.S.* (J. H. Woodward, Burl.)
- **K. H. Pomeroy:** from Sr. Proj. Mbr., T.S. to *Ldr., T.S.* (P. Bokros, Burl.)
- **R. C. Kley:** from Sr. Proj. Mbr., T.S. to *Ldr., T.S.* (H. Schlegelmilch, Burl.)
- **W. L. Ary:** from Ldr., T.S. to *Mgr., Electro-Optics Test Systems* (S. Kolodkin, Burl.)

PROFESSIONAL ACTIVITIES

Central Engineering, Camden, N.J.: **D. Roger Crosby,** Parts Applications, Central Engineering, Camden, recently conducted two four-session workshops on ECAP (electronic circuit analysis program) for engineers at Moorestown and Camden. The first session consisted of a general survey of computer-aided circuit design and program familiarization. The remaining session covered AC, DC, and transient analysis using the IBM-7090 computer. ECAP is also now available for operation in Camden on the Spectra 70/45 computer located in building 10-7.

Frank Morris is RCA representative on the Institute of Printed Circuits (IPC) subcommittee entitled "Inspection Processes for Chemical Resistance of Epoxy-Glass Laminates" that is currently sponsoring an industry-wide round-robin testing program based on a procedure developed by the group. RCA is one of six user companies selected to perform testing of printed-circuit board materials provided by seven selected copper-clad laminate suppliers. Testing is in progress and results will be presented at the IPC national meeting in Los Angeles, California, September 18-20, 1967. Besides being active on the above subcommittee, Mr. Morris is also a member of three other IPC subcommittees: prepreg, raw materials and flexible cable.

J. W. Fulmer, Electromechanical Parts activity, has been appointed liaison engineering representative to the Underwriters Laboratories, Inc. (UL). Mr. Fulmer's consulting duties include interpretation and implementation of UL requirements and developing and assisting in test programs with a view toward obtaining UL approvals and listings of equipments presently being designed or manufactured by RCA's new Medical Electronics Division and Graphic Systems Division.

H. S. Ingraham, Jr., Leader, Measurements Laboratory, was a route supervisor in a nation-wide measurement comparison survey of standard resistors, standard cells, zener references, voltboxes, capacitor pairs, and platinum resistance thermometers sponsored by the National Conference of Standards Laboratories (NCSL). The results of Mr. Ingraham's work are published in the *Proceedings of the 1966 Standards Laboratory Conference* U.S. Department of Commerce, National Bureau of Standards, miscellaneous publication No. 291, pp. 23-30, July 13, 1967.—*John Hendrickson, Sr.*

Astro-Electronic Division, Princeton, N.J.: **F. J. Bingley,** Leader, TV cameras has been named a Fellow of the SMPTE.

S. Krevsky, Systems Engineering and Advanced Programs activity, has been nominated chairman of the New Jersey Coast Chapter of the Aerospace and Electronics Systems Group of the IEEE.—*S. Weisberger*

Aerospace Systems Division, Burlington, Mass.: **A. DiMarzio** has been appointed to the 1968 IEEE convention technical program committee, to aid in coordination of the session on electromagnetic compatibility.

L. T. Lee has been appointed to the Society of Automotive Engineers committee AE-4, electromagnetic compatibility.—*D. B. Dobson.*

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Missile and Surface Radar Division, Moorestown, N.J.: **J. H. Sidebottom,** Division Vice President and General Manager, has been reappointed to the council of the greater Philadelphia section of the American Institute of Aeronautics and Astronautics. **T. G. Greene** was elected secretary of the same AIAA section for the fiscal year 1967 to 1968.

Receiving Tube Engineering, Somerville, N.J.: **T. E. Deegan, A. A. Jalajas,** and **C. M. Morris** received certificates of satisfactory completion of a course in "Advanced Semiconductor Physics" (instructor, **Dr. F. P. Heiman**).

T. N. Matthews, J. E. Hill, J. A. Arico, and **R. K. Reusch** received certificates of satisfactory completion of a course in "Transistor Physics and Circuit Analysis" (instructor, **Dr. R. B. Schilling**).

RCA Missile Test Project: **Robert P. Murkshe,** engineer was re-elected president of the Society of Photo-Optical Instrumentation Engineers.—*W. R. Mack*

LICENSED ENGINEERS

H. Dendunnen, DEP-ASD, PE-21437, Mass.
P. T. Frawley, DEP-ASD, PE-21429, Mass.
S. Aron, DEP-MSR, PE-15447, New Jersey
S. G. Miller, DEP-SEER, PE-15407, New Jersey

SIX DAVID SARNOFF FELLOWS ATTEND SEMINAR

Six RCA employees, who have been awarded David Sarnoff Fellowships for graduate study, recently attended a seminar to familiarize them with the benefits and details of the Fellowships. The fellowships are awarded annually to RCA employees who are working toward their graduate degrees in such fields as science, business administration, and dramatic arts or journalism.

Participating in the seminar were **Dr. Douglas H. Ewing,** Staff Vice President and Chairman, RCA Education Committee; **G. P. Wixted,** Administrator, Management Referral and Placement, and **James C. Blair,** one of last year's fellows and a renewal for this year.

David Sarnoff Fellows at the session included: **Thomas J. Holleran,** of Electronic Components and Devices, who will attend the Carnegie Institute of Technology; **Stephen L. Goldman,** of the Aerospace Systems Division, who will attend the University of Pennsylvania; **Richard W. Nosker,** of RCA Laboratories, who will study at Princeton University; **Gerald P. Quinn,** of NBC, who will study at the University of Southern California, and **Lawrence B. Schein,** of RCA Laboratories, who will attend the University of Illinois.

NEW DOCUMENTS RELEASED BY EIA

The Electronic Industries Association (EIA) has issued four EIA recommended standards and a new publication of the Joint Electron Device Engineering Council (JEDEC). The documents are:

RS-218-A: "Metal Encased Fixed Paper Dielectric Capacitors for DC Application" (revision of RS-218). This document covers the general requirements for paper dielectric fixed capacitors, hermetically sealed in metallic cases (intended primarily for filter, bypass and blocking where the AC component is small with respect to the DC voltage). It also covers removable mounting brackets for use with capacitors. Portions of RS-186 and the latest revision of MIL-STD-202, "Standard Test Methods for Electronic Component Parts" form a part of RS-218-A. *Price $5.50.*

RS-267-A: "Axis and Motion Nomenclature for Numerically Controlled Machines" (revision of RS-267). This document presents improved axis definitions and several new schematic drawings which interpret the standard axis and motion nomenclature for typical machines. The original document, RS-267, extends application of the standard to numerically controlled machines instead of limiting it to machine tools. *Price $4.*

RS-318-1: "Characterization of a Reverse Recovery Test Fixture" (supplement No. 1 to RS-318). This document establishes a method to characterize the test fixture used in the reverse recovery test outlined in RS-318, "Measurement of Reverse Recovery Time for Semiconductor Diodes." *Price $1.*

RS-337: "General Specification for Glass-Coated Thermistor Beads and Thermistor Beads in Glass Probes and Glass Rods (Negative Temperature Coefficient)." This document covers glass-coated thermistor beads in glass probes and glass rods. It includes a type-designation system which codes the style, zero-power resistance, and resistance ratio of the units. Also included are definitions and test methods and performance characteristics. *Price $2.*

JEDEC Publication 63: "Preferred Lead Configuration for Triode or Triode-Connected Field-Effect Transistors." In view of the increased interest in field-effect devices, the preferred lead arrangement was formulated to enhance orderly development of that class of transistor. *Price 25 cents.*

The publications can be ordered from the EIA Engineering Department, 2001 Eye Street, N.W., Washington, D.C. 20006. Minimum order $1.

45 YEARS OF SERVICE

Samuel H. Watson, Manager, Standardizing, Product Engineering, recently completed forty-five years of service with RCA. Mr. Watson's unusual length of service was recognized recently at a luncheon given by some of his friends and associates.

Mr. Watson entered the General Electric Company, Schenectady, N. Y., in 1922 where he specialized in calculating weight, stress, and strain. He entered the GE Engineering School in 1923 and graduated in 1927. In 1929, Mr. Watson transferred to RCA in Camden, N. J., and was engaged in design and field engineering on automotive and aircraft receivers until the spring of 1941. From 1941 until 1944, he was a mechanical project engineer on armed forces communications equipment. He was appointed manager of Corporate Standardizing in 1944.

Mr. Watson currently represents RCA on the American Standards Association Company Member Conference. He was chairman of the conference in 1949 and again in 1952. He is a senior member of the IRE and a charter member of the Standards Engineers Society.

CENTRAL ENGINEERING EXPANDS FACILITIES

Central Engineering's test capability is being significantly improved as the result of acquisitions of the following new test and converter equipments: 1) Automatic RFI test equipment (available for use during the last quarter of 1967); 2) Model-card to tape unit that will convert (80-column Hollerith code) punched card data to 8-channel punched paper tape data (available for use in January 1968); 3) Punched-paper-tape to magnetic-tape unit that will convert 8-channel punched-paper-tape data to ½-inch IBM, industry-compatible, 7-channel magnetic tape (available for use in January 1968); 4) Perkin-Elmer model 820 gas-liquid chromatograph which, when used with the infrared spectrometer, is capable of separating and identifying all the components in an unknown complex organic mixture (now ready to use); 5) Perkin-Elmer model 303 atomic absorption spectrophotometer which is capable of revealing trace concentrations of metals. A single analysis takes just a few seconds compared to old time-consuming wet-chemical analytical methods; 6) Instron model TTC automatic tensile and compressive strength measuring machine for cyclic testing of plastics and elastomers within the temperature range from −100°F to 600°F; 7) Hygrodynamic's electric hygrometer, model 15-3001C, that measures moisture-vapor transmission rate (permeability) through thin films of plastics and elastomers; 8) Pasadena hydraulic transfer press, model EQ 233 C, with a rain pressure of 35 tons for measuring the gel time in laminate boards and for fabrication of multilayer panels; and 9) A dust-free clean room with Zicon spray gun, Binks spray booth, and Liberty dry box for depositing plastic and elastomeric coatings with thicknesses as small as 0.1 mil.—*J. R. Hendrickson*

DEGREES GRANTED

F. Micheletti, Pr. Labs. .... PhD., Electrical Engineering, Princeton Univ., 1/68
T. Nelson, Pr. Labs. .... PhD., Electrical Engineering, Princeton Univ., 12/67
P. Schnitzler, Pr. Labs. ... PhD., Electrical Engineering, Polytechnic Inst. of Brooklyn, 12/67
A. H. Teger, Pr. Labs. .... PhD., Electrical Engineering, Univ. of Penna., 12/67
D. Walters, Pr. Labs. .... PhD., Electrical Engineering, Univ. of Penna., 12/67
H. Heinemann, CSD, N.Y. .... MEE, City College of City Univ. of N.Y., 6/67
R. Gill, AED .... MS, Physics, Stevens Inst. of Tech., 6/67

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W. A. CHISHOLM ASSUMES TPA DUTIES AT RCA VICTOR, LTD.

The editorial staff of the RCA ENGINEER welcomes **William A. Chisholm** as Editorial Representative and Technical Publications Administrator for RCA Victor Co., Ltd. Mr. Chisholm replaces **H. J. Russell** who retired recently. Mr. Chisholm has already made a significant contribution to the RCA ENGINEER by following up on the recent Vol. 13, No. 2 issue, devoted to communications satellites and ground stations, featuring the accomplishments of RCA Victor engineers.

William A. Chisholm graduated in 1954 from the Royal Technical College (Strathclyde University) Glasgow, Scotland, with a Higher National Certificate in Mechanical Engineering. Upon arrival in Canada, he joined the engineering department of A. E. Watts Ltd., Montreal, and was involved in the design of marine heating equipment for the RCN hydrographic survey vessels. Following this, Mr. Chisholm joined Canadair Ltd. as a mechanical design engineer where he carried out design and analysis of aircraft flying controls and equipment. In 1959 he became Assistant Secretary of the Canadian Aeronautics and Space Institute and, as Editor of the *Journal*, was responsible for all publications. In 1961, he returned to Scotland to assume the position of Project Design Engineer with Pressed Steel Co., Ltd. Paisley, where he was responsible for the redesign of the Volvo P1800 sports car. In 1963, he rejoined Canadair Ltd., Montreal, where he designed the landing gear on both the CL-84 V/STOL tilt-wing aircraft and the CL-215 water bomber, an amphibious aircraft specifically designed to combat forest fires. In 1965, he was appointed Assistant to the Director of Research and Development. In this capacity he administered the Research and Development group at Canadair Ltd. He joined RCA Victor Company, Ltd., in March 1967, as Manager—Research Administration. Mr. Chisholm is a Member of the Society of Automotive Engineers.

CONTENTS OF THE SEPTEMBER 1967 RCA REVIEW

High-Frequency Characteristics of the Insulated-Gate Field-Effect Transistor .... J. R. Burns

Standard Test-Lamp Temperature for Photosensitive Devices-Relationship of Absolute and Luminous Sensitivites .... R. W. Engstrom and A. L. Morehead

Gigahertz Tunnel-Diode Logic—M. Cooperman

The Resolving-Power Functions and Quantum Processes of Television Cameras .... O. H. Schade, Sr.

The RCA REVIEW is published quarterly. Copies are available in all RCA libraries. Subscription rates are as follows (rates are discounted 20% for RCA employees):

	DOMESTIC	FOREIGN
1-year	$2.00	$2.40
2-year	3.50	4.30
3-year	4.50	5.70

NEW TPAs FOR DEP

Defense Electronic Products has recently appointed Technical Publication Administrators for each division in an arrangement whereby the division chief engineer will assume greater responsibility to insure that all corporate safeguards (such as security, law, patent, commercial standards, and policy (are taken in 1) review and approval of papers, 2) referral and liaison with other divisions, and 3) approval and implementation of proper distribution of reports. Thus, each of the new division TPAs will operate, in cooperation with the RCA Staff Technical Publications Manager, just as the DEP Technical Publications Administrator formerly did for all of Defense Electronic Products. The newly appointed TPAs who will serve for DEP are **H. Gurin,** Astro-Electronics Division; **D. Dobson,** Aerospace Systems Division; **F. D. Whitmore,** Communications Systems Division; **T. G. Greene,** Missile & Surface Radar Division; **R. J. Ellis,** West Coast Division; **M. G. Pietz,** Defense Engineering—which includes Advanced Technology (Camden), Central Engineering (Camden), Defense Microelectronics (Somerville), and Systems Engineering, Evaluation and Research (Moorestown).

The Technical Publications Administrators are the engineer's primary contact for approval and placement of technical papers, questions on technical reports and engineering memoranda, and reprints of RCA ENGINEER articles. A complete list of Technical Publications Administrators and their locations is given below:

Administrator	*Division*	*Location*
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M. L. Hutchins 212-363-4071	RCA Communications, Inc.	66 Broad Street New York, N. Y.
M. G. Gander 609-963-8000 (PY 5687)	RCA Service Company	Bldg. 203-3 Cherry Hill, N. J.
W. A. Howard 212-247-8300 (4385)	NBC & RCA Institutes, Inc.	30 Rockefeller Plaza New York, N. Y.
A. M. Max 317-635-9000 (VT 502)	RCA Victor Record Div.	6500 E. 30th St. Indianapolis, Ind.
C. A. Meyer 201-485-3900 (TH 2216)	RCA Electronic Component and Devices	415 So. 5th St. Harrison, N. J.
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W. A. Chisholm 514-Wellington 3-7551 (452)	RCA Victor Co., Ltd. Research Labs.	1001 Lenoir St. Montreal, Canada
C. W. Sall 609-452-2700 (2321)	RCA Laboratories	Princeton, N. J.
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D. B. Dobson 272-4000 (2272) (Papers & TRs & EMs)	Aerospace Systems Division	Box 588 Burlington, Mass.
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J. Hendrickson 609-963-8000 (PC 4854) (Papers & TRs & EMs)	Central Engineering	Bldg. 1-6 Camden, N. J.
H. Epstein 609-963-8000 (PM 4942) (Papers & TRs & EMs)	Systems Eng. Evaluation and Research Activity	Bldg. 127-310 Moorestown, N. J.
W. O. Hadlock, Manager 609-963-8000 (PC 2040)	RCA Staff Technical Publications	Bldg. 2-8 Camden, N. J.
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FUTURE ISSUES

The next issue of the RCA ENGINEER emphasizes Advanced Computer Technology. Some of the topics to be covered are:

System Aspects of Large Scale Integration
Satellite Controls
Time Sharing
Programming
Emulation
Languages
Number Systems
IC Technology and the Computer
Advanced Packaging Concepts

Discussions of the following themes are planned for future issues:

Broadcast and TV Communications
Graphic Systems and Devices
Automatic Testing
Man-Machine Alliances in Engineering
Electron Tubes: Conversion, Power, Color TV
Interdisciplinary Aspects of Modern Engineering

* Technical Publication Administrators.

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