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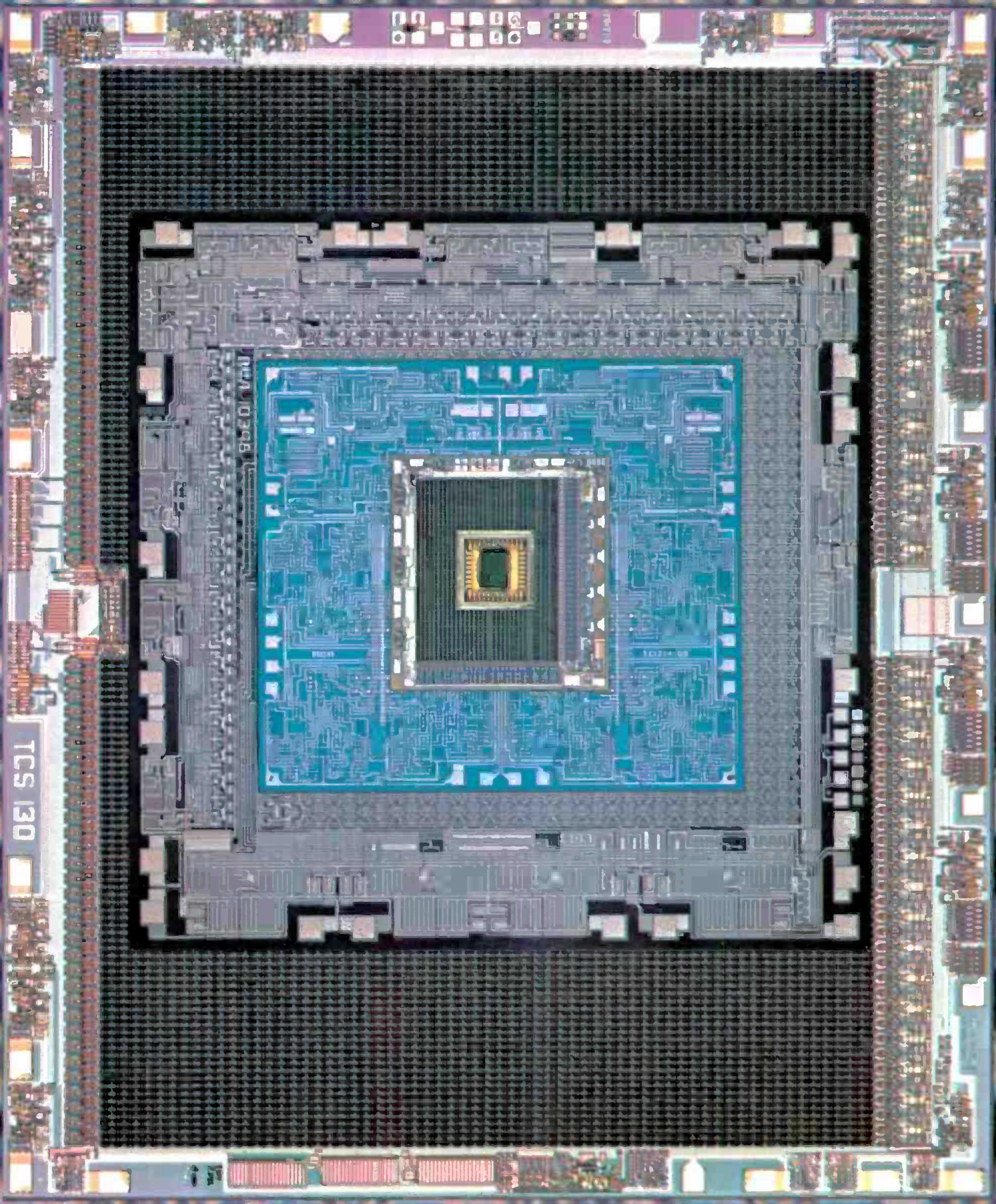

Microelectronics

RCA Engineer

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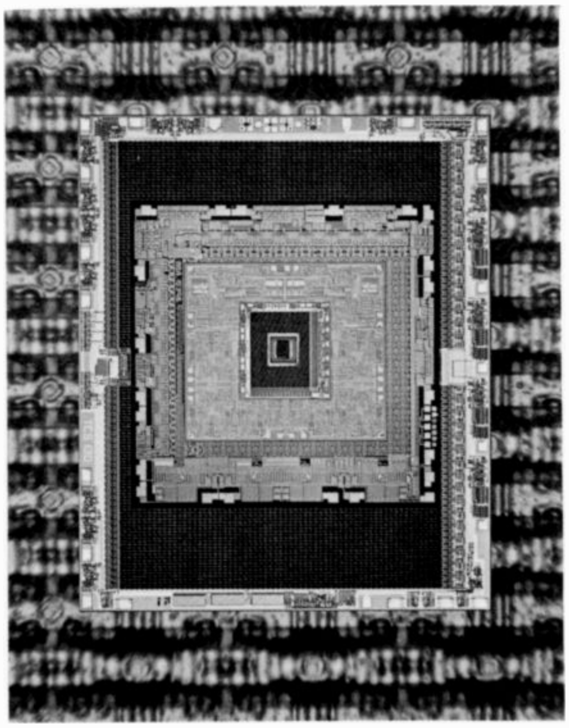


The trend in integrated circuit design toward increasing complexity is illustrated by this issue's cover. Beginning at the outside of the page, the six photographs are described below. The TCS 151 and TCS 130 are under development; the rest are currently in production.

Close up of memory cells in TCS 151 high performance 4K CMOS/SOS static RAM. Magnification: ~1167X.

High performance 16K CMOS/SOS static RAM, TCS 130, contains 87,000 transistors.

SSD's commercial 1K static RAM, CDP 1822.

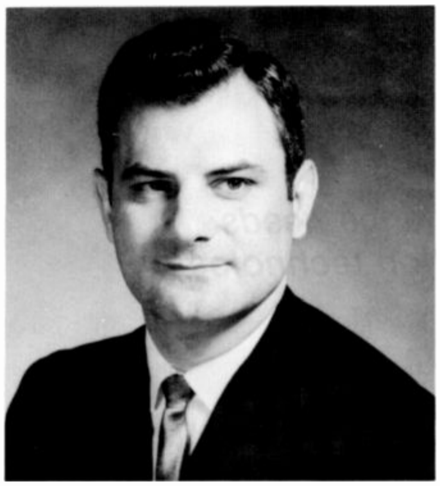
Dual waveform controller, the TC 1214, is a custom circuit designed for the TK-47 microprocessor-controlled TV camera.

Another view of the TCS 151 static RAM.

At the center of the page, the CDP 1802, COSMAC 8-bit microprocessor, uses standard silicon-gate CMOS. (This is shown actual size.)

- To disseminate to RCA engineers technical information of professional value
- To publish in an appropriate manner important technical developments at RCA, and the role of the engineer
- To serve as a medium of interchange of technical information between various groups at RCA
- To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions
- To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field
- To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management
- To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Winning the microelectronics race



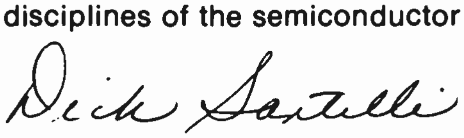
Richard A. Santilli

Semiconductor technology has had a profound effect on the growth of the electronics industry. The performance and flexibility of electronics equipment have increased dramatically in parallel with, and as a result of, equally dramatic improvements in the complexity, efficiency and reliability of semiconductor components. Over the last ten years the equipment-design engineer has witnessed a major evolution in semiconductor technology—particularly in integrated circuits. The trend in both linear and digital ICs has been toward increasing complexity: SSI, MSI, and now LSI and VLSI (very-large-scale integration). This trend, which will continue into the foreseeable future, has provided the equipment designer with vastly improved tools to achieve his equipment-design goals—tools that, to a great extent, determine design philosophy even though the semiconductors used might represent only a small percentage of the finished-equipment cost.

To the IC manufacturer, the challenge lies in minimizing die size while maximizing test and manufacturing yields. In the LSI and VLSI world, the IC designer must be intimately involved in the photomask and wafer-processing operations, as well as in device design, since equipment resolution, environmental conditions, and materials and processing constraints can be limiting factors to the successful manufacture of the product. Die layouts have become so complex (particularly with digital technology) that computer-aided design is required to optimize device design, eliminate human design errors and check out the final results before processing. Complete testing of the finished device, in a reasonable time, can be a formidable challenge requiring very sophisticated test equipment and handling methods, along with complex test programs and debugging techniques. The manufacturers of the micro-precision equipment used to implement these latest IC designs are meeting the challenge by producing process and test equipment that has substantially improved the resolution limits and tolerances required to meet our processing needs.

The semiconductor business is worldwide. So, in addition to the technological parameters, all of the complexities of international trade (currency fluctuations, trade regulations, government policies, etc.) must be taken into consideration. I believe that the United States has, and will continue to hold, a lead in these high-technology semiconductor areas—both technologically and commercially.

The articles on microelectronics manufacturing in this issue of the *Engineer* are of great importance as reports on new techniques, philosophies, and controls in this specialized field. Moreover, they are of great value as background information for the equipment designer who needs to understand the interplay within the various disciplines of the semiconductor industry.



Richard A. Santilli
Division Vice President
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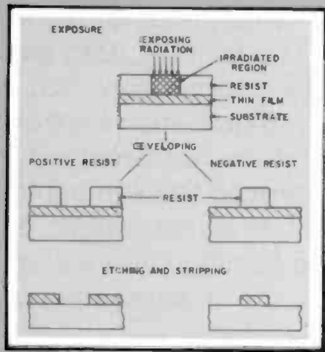
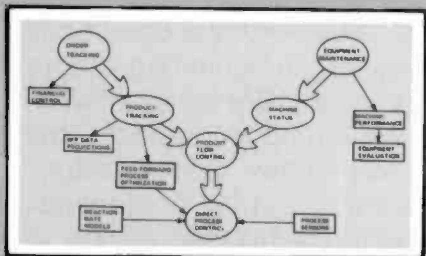
Somerville, N.J.

Highlights



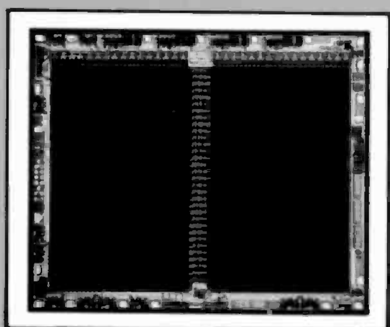
Ever increasing performance needs challenge microfabrication technology.

pages 4, 15, 21



Only computer-aided manufacturing can keep under control the enormous number of devices, processes, tests, and inventory in the production cycle.

pages 26, 31, 34, 37



Monolithic and hybrid applications are required to fill the diverse user needs.

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Data television — the next service to capture the U.S. consumer?

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Upcoming issues

Anniversary Issue: contributions from many activities

Later: color television, microprocessors, quality and reliability

RCA Engineer

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C.A. Deckert | D.L. Ross

Microlithography—the key to solid-state device fabrication

Photographic processes, descended from the graphic arts, are used to define the extremely fine patterns characteristic of modern integrated circuits.

Over the past twenty years or so, expressions such as "solid-state circuitry" and "electronics revolution" have become increasingly familiar to the American consumer. The birth and growth of the solid-state industry has been responsible for increased reliability, availability, miniaturization, complexity, and cost reduction of consumer electronics items.[1]

The solid-state device, or chip, consists of patterned thin films of one or more metals, dielectrics, and semiconductors on a monolithic substrate, usually a silicon or sapphire wafer as large as 100 mm in diameter. An individual chip varies from about 4 to 15 mm on a side, and may contain as many as 250,000 discrete components which are usually transistors.

The fabrication of these devices depends on controlled deposition and removal of the various thin film and substrate materials.[2] In order to produce the desired patterns in the solid-state device, a process called microlithography is employed. At various stages in the fabrication process, whenever a new pattern must be defined in the device, a temporary, stencil-like pattern in a thin film covering the surface is defined by techniques related to photography; and selective etching (or, in some cases, deposition) takes place in the unprotected areas. The temporary film, known as a "resist" material, is then removed and processing continues.[3] This image-forming process is clearly the key to producing complex, patterned, multilayer solid-state devices.

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Final manuscript received January 10, 1979.

Resists: Chemical principles[3,6]

All resist materials used for microelectronics depend on radiation-induced changes in the solubility of a synthetic organic polymer in some selected developer solvent. Resist materials are classified as either positive-working or negative-working, depending on whether solubility in the developer increases (positive) or decreases (negative) upon exposure to irradiation (Fig. 1). Polymers are universally used for preparing resists because of their excellent film-forming and coating properties and the ease with which such properties can be influenced by synthetic techniques. The polymers usually employed are linear and have molecular weights ranging from a few thousand to several hundred thousand. When dissolved in easily-evaporated solvents, the viscosity of their solutions are such that films of useful thickness can be obtained by spin-coating. The molecular structures of the polymers are chosen to permit good spreading and wetting behavior on metal and oxide surfaces. Polymers used to prepare positive resists, where the "stencil" is comprised of *unexposed* (and, therefore, chemically unchanged) material, must possess the physical and chemical robustness and adhesion to the substrate necessary to withstand subsequent processing steps (or be capable of having these properties imparted to it by a simple post-development step, such as baking).

To act as a resist, the polymer must be capable of absorbing the radiation used to expose it, and it must contain, either as components of its molecular composition, or as a second constituent mixed with it, species that will chemically react in carefully selected ways when excited by the absorbed radiant energy. These chemical reactions bring about the desired changes in solubility.

Photoresists must absorb light in order to react. It usually is necessary for the light to be absorbed directly by the molecular species that are to undergo the desired chemical reactions. This is accomplished by choosing conjugated unsaturated systems as the reactive species so as to provide molecular energy levels capable of undergoing electronic transitions corresponding to optical wavelengths in the near ultraviolet (350-450nm).

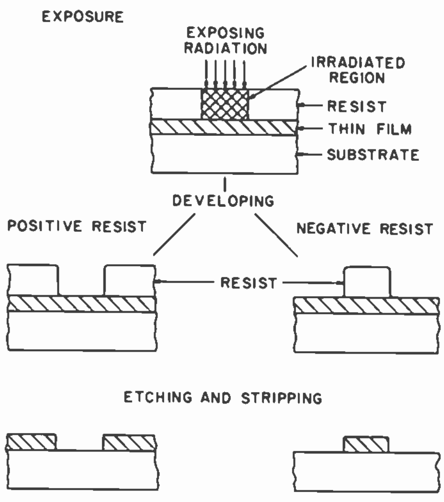
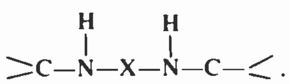


Fig. 1
Schematic diagram of the microlithographic process

The applications of these principles to modern resist technology are outlined below.

Photoresists

Negative-working. There is only one general type of negative photoresist presently of significance to microelectronics fabrication. Exposure to light causes cross-linking of the polymer molecules. This cross-linking produces an increase in molecular weight, reducing the solubility. Eventually, a three-dimensional network of interconnected polymer molecules (a gel) forms that is totally insoluble. The resist is prepared by mixing with a suitable polymer a polyfunctional, light-sensitive additive that, when excited by the absorption of light, can attach itself to at least two sites on the polymer molecule. Modern negative resists of this class use difunctional azides, N_3-X-N_3, in which X contains aromatic groups as part of a conjugated system so as to place the optical absorption band in a useful region of the spectrum. On excitation, these compounds lose two molecules of nitrogen and form species known as nitrenes :N-S-N:. These highly-reactive, short-lived intermediates can react with the C-H bonds (Fig. 2) of a polymer to form the desired cross-links:



The polymers used for azide-based resists are usually aliphatic, rubber-like materials based on poly(isoprene). Some closely-related resists have been described in which monofunctional aromatic azides are attached to the polymer chains. The patent literature suggests that certain organic compounds act as photochemical sensitizers for azide systems. These compounds absorb some of the incident light and are raised to electronically excited states from which energy can be transferred to the azide molecules which then react as though they had been directly excited. By this means, the sensitivity of these systems can be extended to wavelengths beyond those at which the reactive sites themselves absorb.

While their solutions, and coatings made from them, have considerably better stability and life than dichromated colloids, and their processing is relatively insensitive to environmental factors, all of the negative photoresists currently used for microelectronics suffer from several shortcomings. Two shortcomings worthy of mention are inherent to all conventional negative resists: (1) Because adhesion of the image areas to the substrate depends on the photocrosslinking reaction, the exposure required must be adequate to penetrate to, and produce some minimum amount of, cross-linking at the substrate-resist interface. This sometimes makes it difficult to achieve adequate adhesion without overexposure of the resist (line broadening); (2) Although the cross-linking reactions render the polymer insoluble in the developer, they cannot completely prevent the exposed resist from solvent-induced swelling. This causes very fine ($\sim < 2\ \mu m$) patterns to distort in size and shape and, in extreme cases, to lift from the substrate. Defects known as "stringers" and bridging can be produced by such processes.

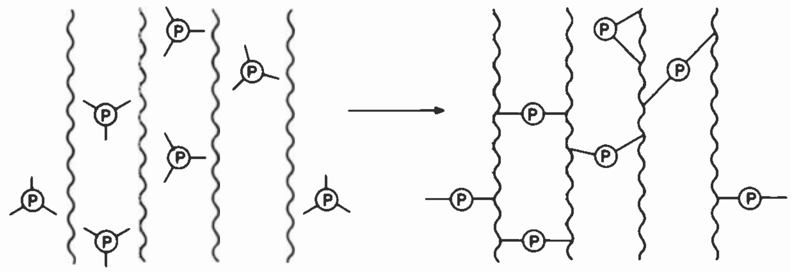


Fig. 2
A typical negative-working photoresist is a mixture of polymer molecules (represented by the wavy lines) and molecules of a light-sensitive, polyfunctional additive (symbolized by the P's). When excited by the absorption of light, the additive reacts with several sites on the polymer chains, causing the polymer to cross-link and, thus, to decrease in solubility in the developer solvent.

In addition, the azide-based resists are sensitive to oxygen which can compete with the desired photocross-linking reaction by reacting with the nitrene intermediates. This can lead to "reciprocity law failure": the amount of insolubilization produced by a given total exposure is dependent on the rate at which the exposure is delivered, since the kinetics of the oxygen-based reactions depend on the rate with which oxygen molecules can diffuse in the resist film. When exposure and pattern definition are very critical, films of these resists are generally purged of oxygen prior to exposure by flooding with an inert gas (nitrogen, CO_2).

Positive-working. All positive photoresists in current use are based on the photochemical conversion of an ortho-diazoketone to a carboxylic acid (Fig. 3). This reaction converts a neutral, organic-soluble molecule to one that is readily soluble in weakly alkaline aqueous developer solvents. These resists are usually formulated from a mixture of relatively low-molecular weight, hydrophobic, phenolic polymer (which, itself, has some alkali solubility) and a diazoketone (about 15% by weight) derived from an amino-naphthol sulfonic acid, such as is illustrated in Fig. 3. In other closely-related systems, the diazoketone is attached directly to the polymer molecules. As a result of association between the polymer and the diazoketone, the solubility of the mixture in the alkaline developer is inhibited. The hydrophobic nature of the polymer further inhibits attack by the developer. On exposure to light, the diazoketone liberates a molecule of nitrogen and undergoes a molecular rearrangement to the alkali-soluble acid. The formation of the polar carboxyl groups in the exposed areas also renders the film less hydrophobic and, thus, more easily attacked by the aqueous developer.[7]

One of the most signficant advantages of this family of resists is the fact that, instead of swelling the film and leaching out the solubilized materials, the developer removes the exposed areas by an etching process. As a result, no swelling-induced pattern deformation occurs, and images of extremely high resolution ($< 0.25\ \mu m$) can be formed. Because the adhesion to the

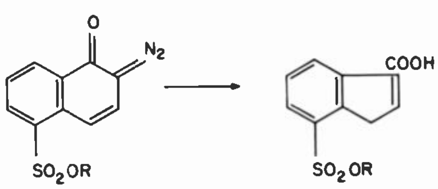


Fig. 3
The molecular structure of a 2-diazo-1-naphthol-5-sulfonic acid ester. Compounds of this type are mixed with phenolic polymers to prepare positive-working resists. When excited by the absorption of light, the normally alkali-insoluble compound loses a molecule of nitrogen and is converted to a carboxylic acid. This causes an increase of the solubility of the mixture in the aqueous alkaline developer.

Historical development of modern microfabrication techniques[4,5]

Techniques directly related to microlithography have been widely used in the graphic arts industry for over 100 years. The term "lithography" (literally, writing on stone) is actually a misnomer as applied to the process described here. Lithography is a printing method that utilizes a flat-surfaced, normally water-receptive, plate or stone, on which the image areas have been made water-repellant and ink-receptive by photochemical or other means. The surface is wet with water and a greasy ink is applied that adheres only to the image areas. The ink is transferred from the surface to the paper (sometimes *via* an intermediate rubber surface) by pressure. The procedures developed by the printing trade that are the true antecedents for today's electronics microfabrication industry relate to the manufacture of printing plates, usually of metal, on which a surface relief pattern is produced by removal of material through chemical etching.* In the process called gravure printing, ink is transferred to paper from small "wells" that have been etched into the surface of a plate. Photogravure processes are well established in graphic arts. *Thus, "microgravure" might be a more accurate term to apply to the subject of this article.*

The development of photoetching techniques represents an example of the impact of the industrial revolution on fields that had traditionally been the province of artisans. Chemical technology was substituted for the meticulous hand labor involved in the cutting away of portions of the surfaces of plates (woodcuts, engravings) used to print pictorial images. The invention of lithography in the last decade of the 18th century by the Bavarian, Alois Senefelder, was perhaps the first step in this process. The key events leading to the discovery of an integrated process for chemically etching a relief printing plate with the use of a *photoresist* have been well documented.

* In the graphics arts, a distinction is made between *relief plates*, from which the ink is transferred to the paper from the raised portions of the surface (examples: letterpress, woodcuts), and *intaglio plates*, from which the ink is transferred from those portions cut below the surface (engravings, etchings, gravure plates).

1782: Jean Senebier, a Swiss, studied the influence of light on a variety of materials (including silver compounds) and found that certain naturally occurring resins change color on exposure to sunlight.

ca. 1814: Joseph Nicéphore Niépce (French) wished to capture the images produced by the *camera obscura* without the labor involved in tracing them on paper. He began experiments on light-sensitive materials. By about 1824, he had found that a natural asphalt, "bitumen of Judea," when exposed to light, became less soluble in certain organic solvents. Niépce made the first photograph by coating a polished pewter plate with a thin layer of the asphalt, exposing it (for 8 hours!) in a camera, and developing the image. Within the next several years (ca. 1826), he had used the insolubilized asphalt pattern as a *resist* and etched the metal (pewter, copper) with acid to produce a relief plate. [Niépce went on to collaborate with Louis Jacques Mandé Daguerre who discovered (ca. 1837) how to make permanent images on the sur-

substrate is not influenced by the photochemistry, the exposure and development conditions can be adjusted strictly in terms of the relief pattern geometry desired.

The diazoketone resists do not respond to photochemical sensitizers and are not affected by the presence of oxygen.

"Deep-UV" Resists. The pattern resolution achievable by photoresists is ultimately limited by the wavelengths of the light used to expose them. During the last several years, in attempts to define patterns 1.0 − 1.5 μm in size, work has been carried out with new light sources and special (quartz) optics to permit exposure systems to utilize wavelengths in the 200-250 nm region. While some conventional photoresists respond adequately to these wavelengths, many do not because the polymers from which they are derived absorb strongly enough to block the transmission of the exciting radiation. The use of these shorter wavelengths makes the task of designing the reactive sites somewhat easier because simpler systems can be used (long conjugated systems are unnecessary). Because of the limitations of negative resists that were previously discussed, most of the new resists being developed for deep-UV applications are positive-working and are based on polymers that will undergo a reduction in molecular weight (and, thus, an increase in solubility) as a result of photo-induced main-chain scission. Work in this field is in its infancy. The degree to which it flourishes will depend on systems evaluations comparing this approach to higher resolution with those involving electron-beam and X-ray exposure schemes.

Electron-beam and X-ray resists

With the ability to focus electron beams to very small diameters (below 1000Å), and the very short wavelengths of soft X-rays (5-50Å), the pattern resolution obtainable when resists are exposed to this kind of radiation is no longer primarily dependent on the exposure means. The fundamental limitations are now a function of the scattering of electrons (or, in the case of X-rays, the range of the photoelectrons produced on absorption of the radiation) in the resist material, or the scattering of electrons reflected from the substrate. During the last 10-15 years, electron-beam exposure schemes for the defining of sub-μm patterns in resist materials have been examined at several electronics companies.[8] At RCA, the impetus was the mastering of the VideoDisc for which it was desired to record relief patterns having wavelengths of about 0.5μm.[9] At Bell Laboratories and IBM, the application was the fabrication of chrome master masks and direct exposure of IC wafers. More recently, research done at MIT Lincoln Laboratories demonstrated that soft X-rays could also be used to expose appropriate resist materials. The electron-beam techniques employ a scanned, faces of silvered copper plates which had been sensitized with iodine vapors (the daguerreotype).]

1832: Gustav Suckow (German) published his observations that mixtures of organic substances with potassium dichromate change color on exposure to light.

1839: Alfred Donné (French) etched daguerreotypes with acid, producing relief printing plates.

1839: Mungo Ponton, a Scot, found that paper soaked in potassium dichromate was light-sensitive. When the paper was washed in water following exposure, the unexposed regions washed clean while the exposed pattern remained orange-brown.

1840: Edmund Becquerel (French) investigated Ponton's findings and determined that the starch sizing in the paper played an important role in the image formation.

1841: Joseph Dixon (American) employed the fact that a mixture of dichromate and natural gum, on exposure to light, changed its surface properties (the exposed areas become ink-receptive while the unexposed areas remain water-receptive) to produce lithographic printing plates. He used such plates to counterfeit bank notes.

1852: W.H. Fox Talbot (English) discovered that exposing films of dichromated natural colloids (e.g., gelatin) to light produced sufficient solubility reduction to permit the unexposed regions to be selectively washed away with water. He patented the use of these materials in photoengraving. This was the first use of a synthetic (man-made) photoresist.

Thus, by the mid-1800's, the groundwork had been laid for today's sophisticated microelectronics fabrication techniques.† It is interesting to note that, with the exception of two university professors, Suckow and Becquerel, all of the investigators were amateur inventors.

† In fact, by about 1870, optical equipment had been developed that permitted photoreduction of images by a factor of 1/300 to produce pellicles in silver halide emulsions. These precursors of microfilm and photoreticles were used by the French with the help of pigeons, to communicate with the outside world during the siege of Paris.

Dichromated colloid resists suffer from a number of practical shortcomings including a relatively short "pot life," "dark-hardening" (the unexposed coating gradually loses its solubility on storage), excessive dependence of solubility (developability) properties on environmental factors such as ambient humidity, and poor resistance against the strong etchants used for microelectronics materials. In spite of this, dichromated colloids remained the workhorse photoresists of the printing industry until after World War II. Even today, RCA uses substantial quantities of these materials for the printing of phosphor screens in kinescopes and for the etching of shadow masks for color picture tubes.

Photoengraving techniques were first employed by the electronics industry in the fabrication of copper printed circuits shortly after the war. The application of this technology to transistor fabrication in the early 1950's depended on the development of new classes of entirely synthetic photoresists.

sharply-focused beam as a "pencil" to delineate the desired patterns while the X-ray scheme uses a flood exposure through a patterned mask. In both cases, the interaction of energetic electrons with the resist material brings about the solubility-altering chemical reactions.

The principal difference between these materials and photoresists lies in the fact that, here, the incident energy is absorbed more or less indiscriminately by all functional groups in organic polymer molecules rather than being selectively absorbed at specific reactive sites. The primary chemical event induced by exposure is the breaking of covalent bonds to produce free radicals or ions. As a consequence, the chemical changes brought about are more analogous to those produced by heat than by light. The fate of the ions or radicals determines whether the resist is negative- or positive-working: if these species react with one another to form new covalent bonds, the polymer can increase in molecular weight and/or cross-link; while, if the fragmentation leads to backbone scission, the molecular weight will decrease.

The major emphasis in the search for negative resists is the identification of materials that have the highest practical sensitivity and the best edge definition in the face of the usual swelling problems. Of course, the usual requirements, outlined above, of good adhesion, etch resistance, etc., must be met. Currently, the most widely-used negative electron beam resist is a copolymer of ethyl acrylate and glycidyl methacrylate ("COP") developed at Bell Laboratories. The epoxy groups provide a highly-sensitive route for cross-linking. It is interesting to note that the cross-linking reactions in this material proceed for a time following the electron exposure. Thus, exposed substrates must be kept in the vacuum chamber of the exposure apparatus for some 20-40 minutes after exposure is completed to obtain uniform results.

The most useful classes of polymers for positive resists are those known to degrade in molecular weight by thermal processes. The first, and still widely used, positive electron-beam resist is poly(methyl methacrylate), long known to be capable of "cracking" back to monomer, by destructive distillation. Although a factor of $10-50$ lower in sensitivity than is required by today's electron-beam exposure systems, it has very high resolution and good etch resistance. Another class of polymers known to undergo efficient thermal degradation is the poly(olefin sulfones).[10] These materials are synthesized by the copolymerization of SO_2 and unsaturated monomers:

$$SO_2 + \mathrm{C{=}C} \rightarrow [-SO_2-\mathrm{C}-\mathrm{C}-]_n$$

A wide variety of these has been examined at RCA and Bell Laboratories. One, the copolymer of butene (polybutene sulfone, "PBS"), is currently used in the production of chrome masters in MEBES.[11] With these polymers, cleavage of the backbone can lead to a chain depolymerization reaction from which the comonomers are regenerated. This introduces considerable "gain" into the exposure process and can produce excellent separation of molecular weight (and, thus, good differential solubility in developers) between exposed and unexposed regions of the resist film. In some materials, the depolymerization process is so efficient that relief patterns are produced directly by evaporation of the reaction products in the vacuum chamber of the exposure apparatus without the need for a separate development step. PBS suffers from several shortcomings: its development characteristics are very dependent on the effects of moisture and ambient humidity; it cannot be used in coatings that are as thick as are needed for step coverage in wafer fabrication; and it has poor resistance against the "dry etching" proceedings to be discussed below.

Because the phenolic polymers have low sensitivity to electron-beam-induced cross-linking and because the diazoketones can also undergo heat-induced molecular rearrangement, certain formulations related to typical positive photoresists can function usefully as electron-beam resists. Over a thousand VideoDisc masters were fabricated by electron-beam recording using RCA Mark II resist, a material of this type.

While the field of X-ray resists is quite new, it can be predicted that most of the findings relevant to electron-beam-sensitive materials will apply here. Many of the materials that function well as electron beam resists show similar behavior on X-ray exposure. Considerable emphasis is placed on the incorporation of high Z-value elements in the polymer structure so as to increase the absorption of incident soft X-ray energy.

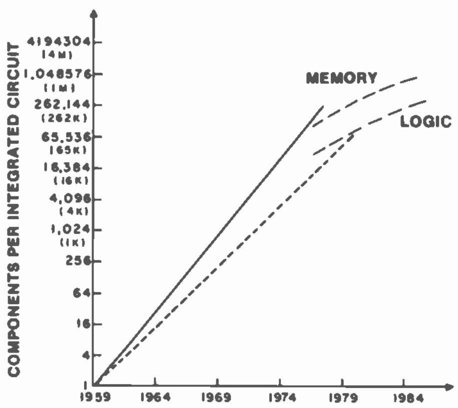


Fig. 4
Number of components per chip has been increasing at a geometric rate since 1959, when the planar transistor was developed. Solid line—Ref. 1; short dashes—Ref. 12; long dashes—Ref. 13 (prediction).

Microlithographic processing — overview

In the fabrication of solid-state devices, the photolithographic process is constantly pushing the limits of the state of the art. Many of the requirements for producing today's complex chips would have been considered impossible just a few years ago, and this trend appears to be continuing unabated,[1, 12, 13] as shown in Fig. 4.

The most important resist properties required for producing a microlithographic pattern are resolution, contrast, freedom from defects, uniformity, high sensitivity to the exposing radiation, ease of processing, adhesion to the substrate, resistance to degradation by the etchant, and subsequent ease of removal.[3]

The resolution requirement in particular has increased rapidly over recent years. It is important to distinguish between best possible resolution achievable over a small-area unpatterned substrate under carefully controlled laboratory conditions, and best resolution achievable at reasonable yields over large areas in a production environment when various levels must be accurately aligned and precise dimensions maintained. In this article, unless otherwise stated, the term "resolution" will be taken to mean the smallest feature on a chip that can be imaged economically on 3-inch wafers under production conditions. For example, RCA's 16K RAM SOS device requires 4-μm resolution. This chip is illustrated in Fig. 5. It is thought that the current practical limit for production using conventional photolithographic methods is no better than 3 μm.[14] On the other hand, surface structures as small as 80Å have reportedly been defined in the laboratory.[15] Some examples of the recording of high resolution on resists, not from the solid state industry, include RCA's VideoDisc masters,[9] which were formerly fabricated using electron-beam recording, and Holotape®,[16] relief-phase holograms which were recorded using a He-Ne laser. In both these cases, illustrated in Figs. 6 and 7, resolution of 0.25 μm was routinely achieved over a large area substrate.

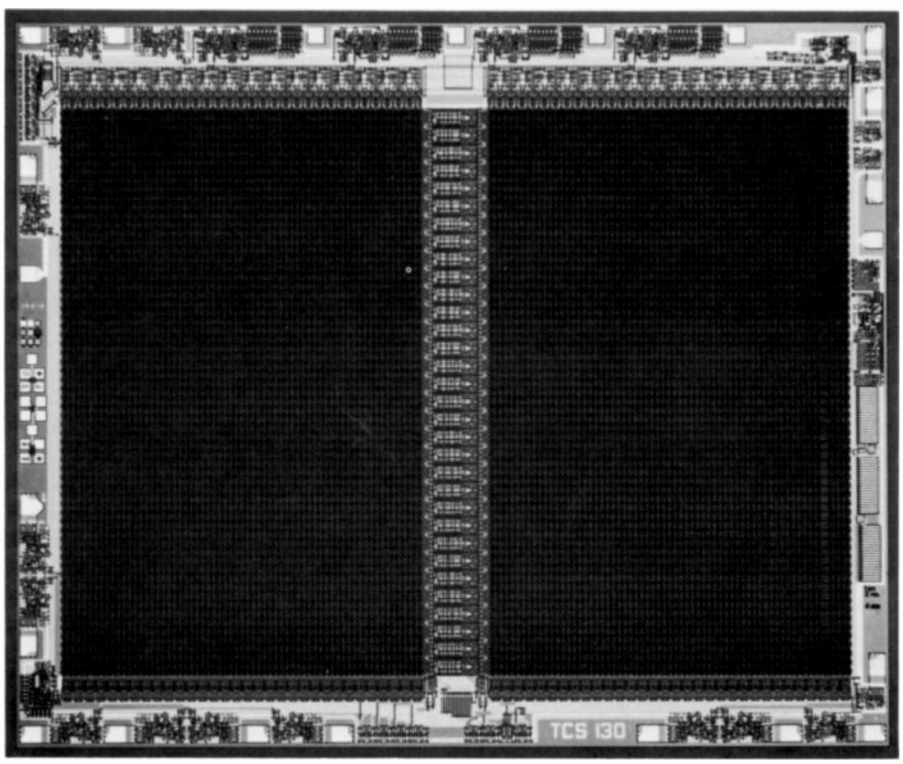


Fig. 5
RCA's most complex chip, the 16K RAM SOS device illustrated here, requires four μm resolution. Even finer dimensions will be required on next-generation circuits.

In order to fulfill the requirements of microlithography, some steps of the process have become more or less standardized,[3] while at most steps, a compromise between high performance and cost is reached. Control of the environment and the choice of resist material itself are other factors where choice is dependent on process requirements.

"Microlithography," as used in electronic device fabrication, designates the successive steps of: preparing the substrate, (e.g., a silicon wafer); applying a thin (usually less than 5 μm) film of radiation-sensitive polymeric composition (the "resist) to the surface of the substrate; prebaking the resist coating; exposing the film to a pattern of electromagnetic radiation (light, electron beams, X-rays) so that chemical reactions take place in the film that change its solubility in certain solvents ("developers"); bathing the film in a developer solvent that selectively removes either the exposed ("positive-working") or unexposed ("negative-working") areas thereby creating a patterned stencil in the resist film; postbaking the resist; selectively removing material from, or depositing material on, those areas of the substrate which have been uncovered by the development step; and finally removing the remaining resist pattern ("stripping").

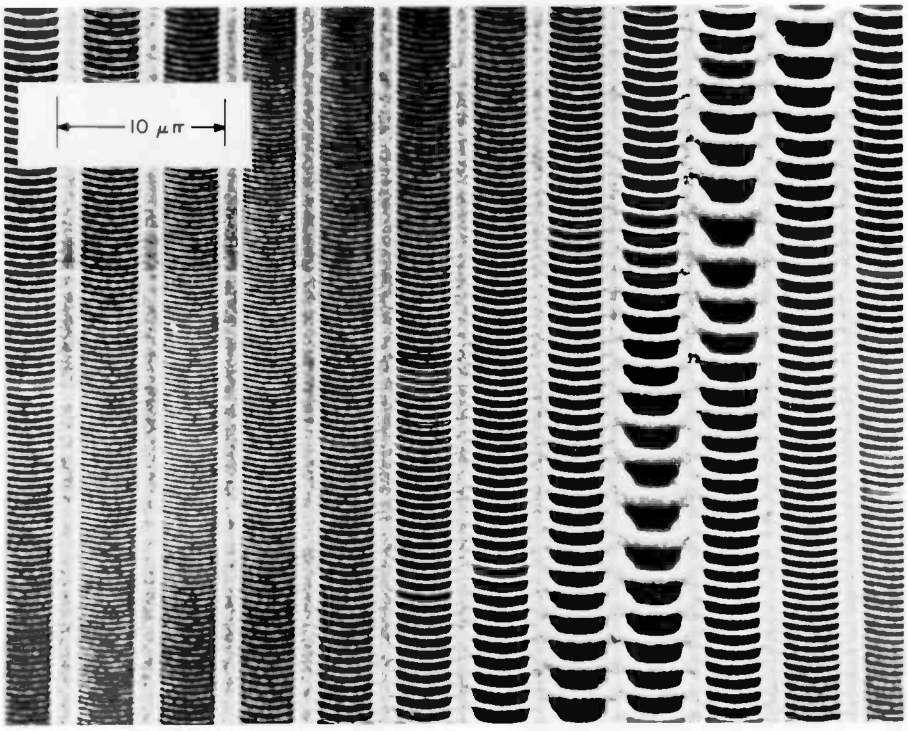


Fig. 6
The masters for RCA's VideoDisc were formerly recorded in a resist material using electron beam exposure.

Substrate preparation

Preparation of the substrate may involve film growth or deposition, diffusion or implantation of impurities, or cleaning procedures. If the wafers have been exposed to the ambient for more than a few minutes, contamination is probable,[3] and a high temperature bake (~200°C) and/or an application of an adhesion promoter are employed. In many wafer processing areas, these steps are routinely used regardless of the time lapse. The importance of cleanliness in solid state processing cannot be overemphasized. Surfaces must be scrupulously cleaned and kept clean. Contamination, in some form or another, is probably the principal cause of day-to-day processing problems in fabrication areas. For this reason, environmental control (particle count, air flow and quality, clothing, humidity level) is a major factor in determining yields of good chips. A defect which can be traced to surface contamination is shown in Fig. 8.

Coating and prebaking

Microlithographic processes usually employ liquid resist materials rather than dry film resists* because of the higher resolving power of the former. The method of application is nearly always a spin-on technique, which offers very good uniformity at a low processing cost. Resist solutions are formulated so that during the application and spinning process, the solvent(s) evaporate at a rate optimum for producing a non-"skinned" coating of uniform thickness.[17] In order to remove the last traces of solvent from the resist film and to promote adhesion to the substrate, a prebake step is next carried out, usually at a moderate temperature (70-90°C).

Exposure

Exposure is probably the single most important step in the microlithographic process. Resolution and pattern uniformity are determined at this step, and the exposure equipment and operation must be maintained at the precise optimum level to ensure good image production.

The most common type of exposure system involves near-UV exposure of the resist-coated wafer through a patterned (photographic emulsion, chrome, iron oxide) glass mask with which it is in contact; however, several other types of exposure systems are now available or under development. These various systems, as well as their respective advantages and disadvantages, will be discussed below.

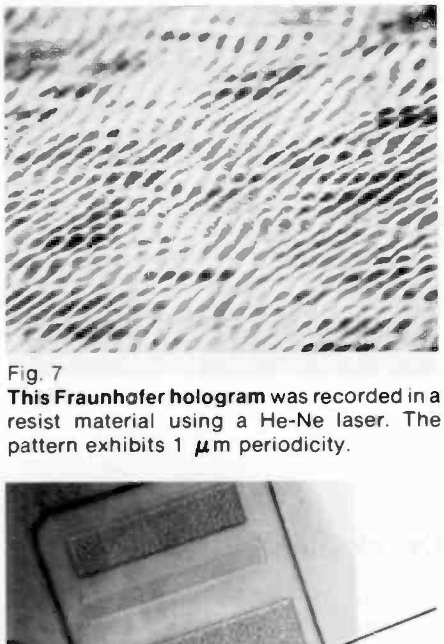


Fig. 7
This Fraunhofer hologram was recorded in a resist material using a He-Ne laser. The pattern exhibits 1 μm periodicity.

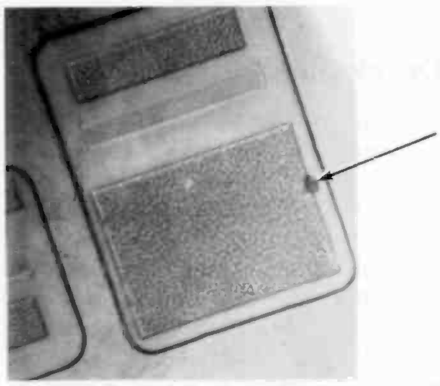


Fig. 8
A foreign particle, either on the surface or in the resist, produced the defect seen in this photoresist pattern. (Light gray areas bear resist material.)

* Dry film resists are non-solvent-containing photoresist films, as thin as 25 μm (one mil), supplied in a laminated form, and used primarily in the printed circuit board industry.

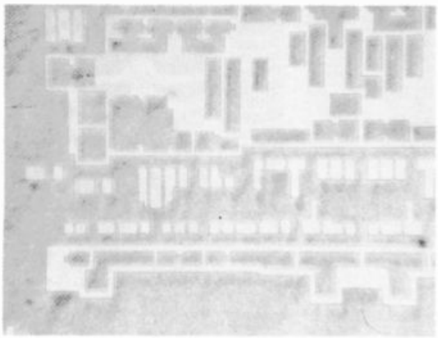


Fig. 9a

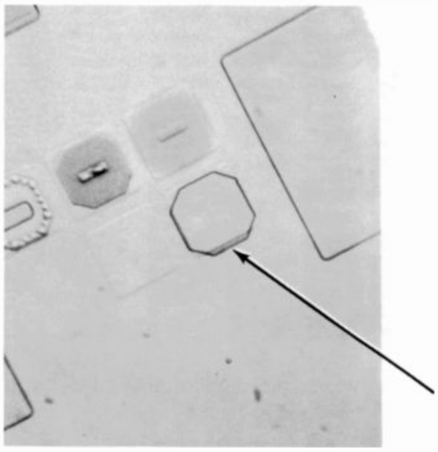


Fig. 9b

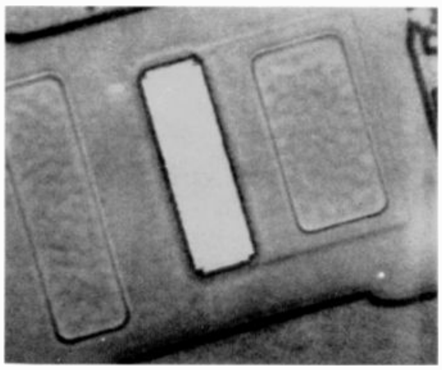


Fig. 9c

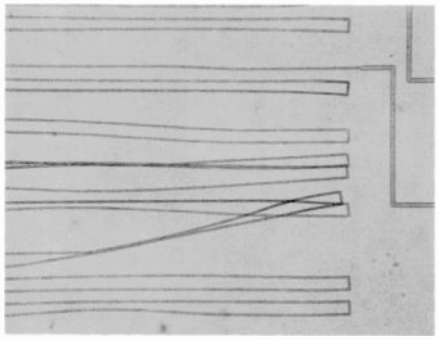


Fig. 9d

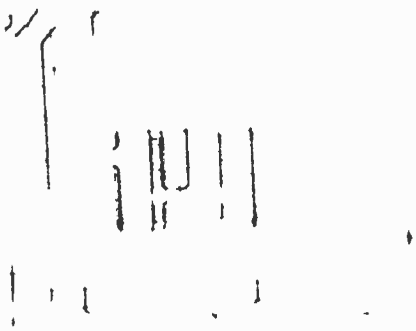


Fig. 9e

Fig. 9
Various types of photoresist pattern defects observed after development. (a) "Orange peel" is a common occurrence when negative resists are underexposed. (b) The photoresist pattern is slightly misaligned in this pattern test key, since the octagon-shaped resist image does not coincide perfectly with the underlying substrate image. (c) Imperfect contact between mask and wafer caused the inward notching at the corners of this photoresist pattern (gray areas are covered with resist). (d) Poor adhesion of the photoresist to the substrate can lead to lifting of the resist image during development. (e) Bridging of the resist across open areas can be due to either substrate contamination, poor contact during exposure, or underdevelopment.

Development

Following exposure, the resist film is developed, i.e., treated by a solvent in which either the unexposed (negative resist) or exposed (positive resist) areas are soluble. Development is carried out either by a spray or immersion technique. As discussed previously, certain types of resists are subject to swelling during development. After development, the wafers are treated in a rinse solvent to remove residual developer and to reduce any swelling. Some types of resist pattern defects can be detected by inspection at this point, as illustrated in Fig. 9.

Postbake

After developing, the patterned resist films are postbaked to drive off any remaining developer or rinse solutions and to maximize the film/substrate adhesion. Typical postbake temperatures are 120-135°C. It is thought that best adhesion is obtained by baking at as high a temperature as possible just below the softening point of the resist.

Etching

In most cases, the photolithographic process is subtractive, and the next step involves etching the unprotected areas of the wafer. Either wet or dry etching processes may be used. Wet, or chemical, etching is the traditionally used method, in which the wafers are immersed in liquid etchant (gas phase etching is also included in this category).[18] Wet etching is simple and inexpensive, and this method was used almost exclusively until the past few years, when it became evident that the sloped edges inherent in isotropic wet-etching processes would limit control of the feature size. In addition, the lack of perfect adhesion of the photoresist film to the substrate during wet etching leads to "undercutting," a failure mechanism in which very highly sloped edges occur[18, 19] (Fig. 10). In certain instances, a sloped edge is preferred so that the material to be subsequently deposited will cover the edge uniformly and completely. In order to achieve controlled undercutting, a very thin layer of material which dissolves in the etchant more rapidly than does the substrate film may be deposited prior to resist application. Equipment is now available for "dry etching" (plasma etching)[20] of wafers reproducibly, at high resolution, and in production volumes. Photoresist adhesion is much less critical in dry etching processes, and very high aspect ratios can be achieved in planar systems[21] as illustrated in Fig. 11.

Deposition

In those cases where an additive photolithographic process is employed, the substrate is not etched, but rather, an evaporation, ion implantation, or plating step is carried out at this point. In the trimetal (Ti-Pt-Au or Ti-Pd-Au) process,[22] for example, the gold layer is electroplated through openings in the photoresist onto the Pt or Pd layer on the substrate. In this case, poor resist adhesion leads to "underplating," an example of which is shown in Fig. 12.

Resist removal

Finally, the resist material must be stripped before the next level of the device can be defined. A variety of acids, bases, and solvents are used for stripping, as is a plasma stripping procedure. Removal of the last traces of resist residue, however, can be rather difficult to achieve.[23] An example of incomplete resist removal is shown in Fig. 13.

Quite relevant to a discussion of processing is the procedure of inspecting wafers and masks. Operator inspection using an optical microscope is the traditional inspection method, but for masks, in particular, several types of highly sensitive and accurate, automatic inspection instruments have recently been developed.[24, 25] Some very simple mask inspection techniques, such as optical examination using a collimated light beam, either at a glancing angle or from behind the substrate, can also be very sensitive to defects.

Exposure techniques are crucial to the microlithographic process

As discussed above, exposure is often considered the most crucial step in the photolithographic process. It is at this point that the resolution, uniformity, and image fidelity of the device are determined. Because of the interaction of the mask, the exposure equipment, and the resist material, the choice of an exposure system must consider all these elements. Tradeoffs in terms of resolution, cost, and throughput will determine which system is chosen.

Masks

Masks that are in current use, or will be used in developmental systems, include photomasks, electron-beam masks, photoreticles, and electron-beam reticles. [Photomasks and electron-beam masks bear an array of patterns whose magnification is the same as the pattern to be defined on the device wafer; a reticle, on the other hand, bears a single pattern whose magnification is larger (usually 5 or 10x) than that to be defined on the wafer.] In addition, applications not requiring a mask, for example the use of direct electron-beam writing on a wafer, are under consideration. Masks are typically fabricated of silver halide emulsions, chromium (reflective or nonreflective), or iron oxide patterned onto a glass substrate. Emulsion masks are lowest in cost, but resolution and durability are limited. Iron oxide masks offer the advantage that the operator can see through them for easy pattern alignment. However, most high-quality masks are now fabricated of chromium with a thin surface layer of oxide which makes the metal film nonreflective. Exceedingly complex and/or

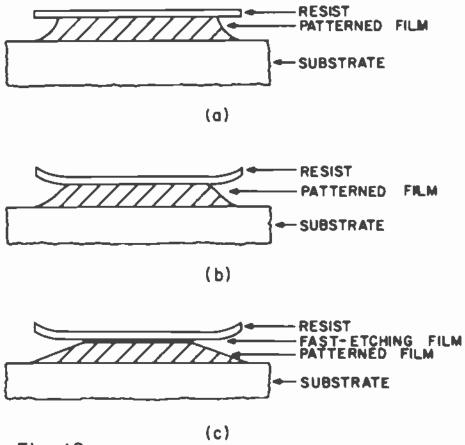


Fig. 10
Different edge profiles produced from various degrees of undercutting: (a) good resist-to-film adhesion produces this type of edge; (b) undercutting has occurred at resist-film interface; (c) use of a fast-etching film to achieve controlled undercutting.

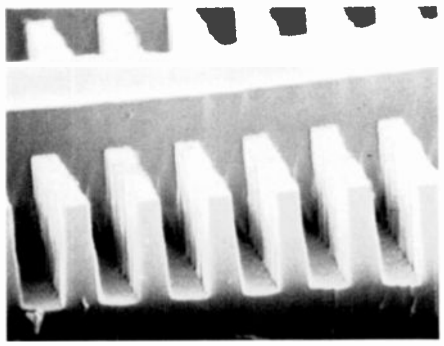


Fig. 11
Photoresist pattern over grating in fused quartz. Thickness of resist layer from top of lines = 1 μm. Periodicity of grating in SiO_2 is equal to 1.4 μm; periodicity of grating in photoresist is 10 μm (5 μm line width). A reactive sputter etching procedure in a fluorocarbon gas was used to etch the SiO_2.

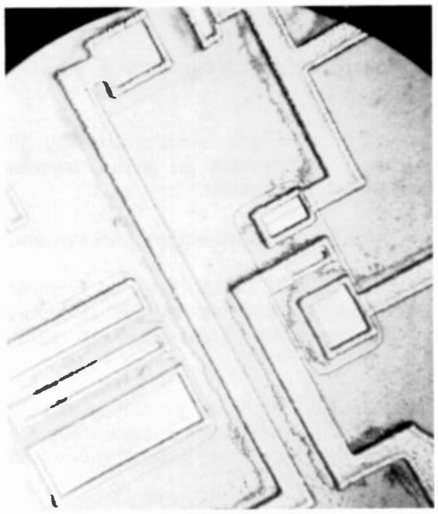
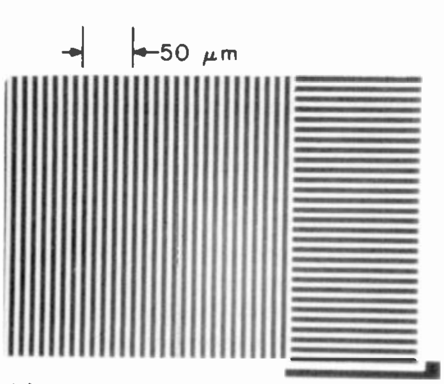
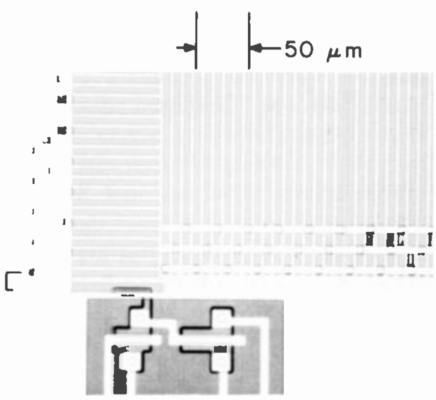


Fig. 12
Gold has been electroplated into the open (interconnect) areas of the photoresist pattern. Poor photoresist adhesion has led to plating under the resist film pattern edges.

Fig. 13
An extreme case of incomplete photoresist removal.

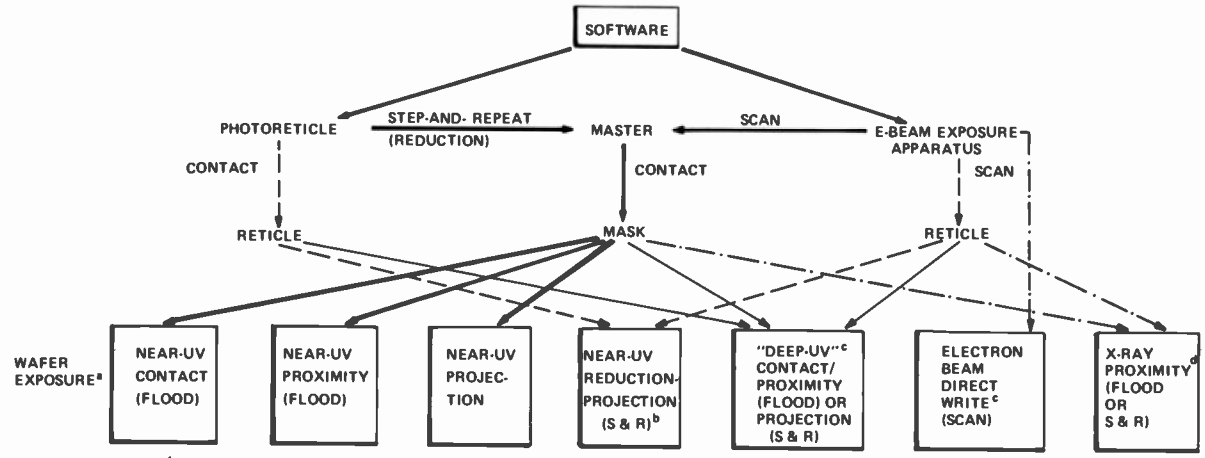


(a)



(b)

Fig. 14
RCA's CCD requires essentially perfect photolithographic patterning over a large area (10mm x 15mm). A small portion of the pattern is shown here. (a) Electron-beam generated master polysilicon gate level. (b) Completed CCD.



	NEAR-UV CONTACT (FLOOD)	NEAR-UV PROXIMITY (FLOOD)	NEAR-UV PROJECTION	NEAR-UV REDUCTION-PROJECTION (S & R)[b]	"DEEP-UV"[c] CONTACT/PROXIMITY (FLOOD) OR PROJECTION (S & R)	ELECTRON BEAM DIRECT WRITE[c] (SCAN)	X-RAY PROXIMITY[d] (FLOOD OR S & R)
RESOLUTION, μm[e]	3[f]	3[g]	2.5	1.25	1.0[h]	0.5-1.0[i]	2-3[j]
MASK LIFE[k]	SHORT	MODERATE	LONG	LONG	LONG (S & R)	–	LONG
THROUGHPUT[l]	HIGH	HIGH	MODERATE	MODERATE	MODERATE?	LOW[m]	LOW?[n]
COST PER[o] WAFER, $	LOW	LOW	LOW	MODERATE	MODERATE?	HIGH?	MODERATE?

STATUS AT RCA
——— PRESENT
— · — IN RESEARCH AT RCA LABORATORIES
— — — UNDER ACTIVE STUDY FOR INTRODUCTION TO PRODUCTION
——— NOT UNDER STUDY AT PRESENT

Fig. 15
Wafer exposure processes and parameters.

Notes:

(a) Much of the data in this chart were updated from a report prepared by Central Engineering, RCA Somerville, in mid-1978.

(b) Using 10x reticle.

(c) Only a few prototype systems available.

(d) First commercial system prototype (Cobilt) using proximity flood exposure now being tested. S&R systems not commercially available.

(e) Factory conditions, 3-in. wafers assumed. For near-UV exposure, resolution quoted is for positive photoresist. Near-UV exposed negative resist resolution about 30% larger.

(f) One μm resolution possible on small flat substrates.

(g) At 20 μm mask-to-wafer spacing, the minimum acceptable to avoid frequent mask-to-wafer contact.

(h) Estimate for a projection S&R system.

(i) Using MEBES (Manufacturing Electron-Beam Exposure System, ETEC Corporation) raster scan. Vector scan can resolve 0.1 μm.

(j) Resolution limit on prototype system, limited by manual alignment accuracy. Bell Labs proprietary resist and equipment can resolve 0.5 μm.

(k) Short, 100-150 exposures; moderate, 150-1500; long, 1500-5000 or more.

(l) Low, < 25 3-in. wafers per hour; moderate, 25-50; high, 50-100.

(m) MEBES could print less than two 3-in. wafers per hour. IBM EL-1 can do twenty-two 2¼-in. (or twelve 3-in.) wafers per hour.

(n) Bell Labs resist and equipment can do 15 3-in. wafers per hour. Information not available for Cobilt system.

(o) Based on ratio of capital equipment cost to wafer throughput only.

large masks, such as a CCD mask (Fig. 14a), and masks to be used in noncontact exposure systems may be generated by contact printing from an electron-beam master,[11] or an optically generated step-and-repeat (S&R) master may be used directly. Very fine geometry (<2 μm) masks can be fabricated directly by electron-beam recording. Masks which are to be used with deep-UV exposure systems require quartz substrates, and X-ray exposure systems utilize a heavy metal (e.g., gold) pattern on a thin substrate such as beryllium, silicon, silicon carbide, or an organic polymer.[26]

Systems and equipment

Various types of wafer exposure systems may be used. These include UV flood exposure (contact or proximity), UV exposure (projection), UV S&R reduction exposure (projection), X-ray flood exposure (proximity), or electron-beam scan exposure (direct writing). The various combinations of mask types and wafer exposure systems which are in use or are being developed are shown in Fig. 15, along with a summary of some features of each type.

Near-UV flood exposure (contact mode) is the traditional method of photolithographic exposure. This method affords very good resolution; in production, about 3 μm can be achieved on the newest instruments,[14] and throughput is usually high. On a laboratory scale, square wave gratings with micron and submicron periodicities and etch depths up to 3 μm have been achieved[20] (Figs. 11 and 16). Hard contact (thousands of grams force between mask and wafer) causes short mask life; however, as a result, very expensive masks, such as electron-beam generated masters, or very complex masks where very low defect levels are required, cannot be used economically.

Near-UV flood exposure using soft contact (only a few grams force between mask and wafer) or proximity (wafer separated from mask by tens of micrometers) is another exposure scheme. The resolution capability is somewhat lower than for hard contact, but improved mask life can make this a feasible process in certain cases. Power transistors, for example, use relatively coarse geometries and often have mask-damaging "bumps" on the wafer surface.

Projection near-UV exposure has become quite popular in the microelectronics industry over the past 3 to 4 years because of the advent of accurate, relatively high-resolution 1:1 projection alignment instruments (Perkin-Elmer Corp.). These

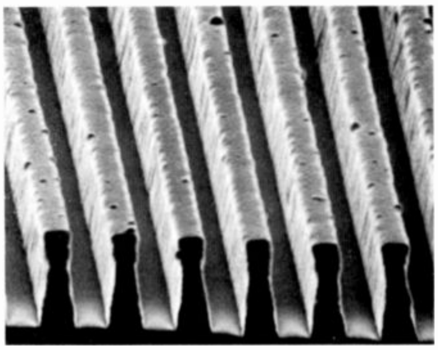


Fig. 16
Photoresist pattern on (111)-Si; thickness of resist layer, 1.5 μm; 1.4 μm periodicity grating.

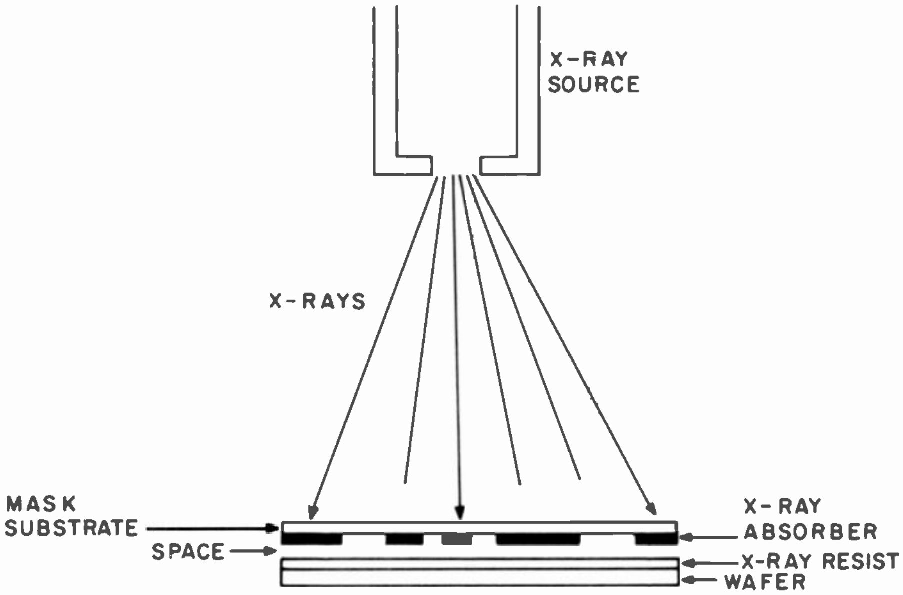


Fig. 17
Schematic diagram of X-ray proximity flood exposure system.

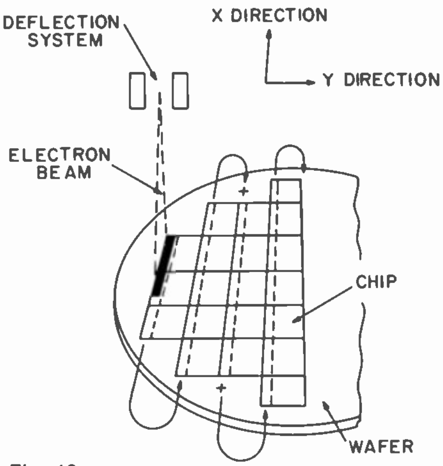


Fig. 18
A raster scan technique may be used for wafer fabrication by direct electron beam exposure.

instruments are highly cost-effective because they afford essentially infinite mask life and can achieve resolution down to about 2.5 μm. Because of the long mask life, expensive masks, such as electron-beam-generated masters, can be used.

Under typical factory conditions, existing near-UV exposure systems are limited in resolution by factors such as photomask accuracy and dimensional stability, runout, and wafer flatness.[27] The advent of commercial S&R reduction UV exposure systems,[14, 28] using a single 5x or 10x photo- or electron-beam-generated reticle as the photomask, is of considerable interest at present (GCA Mann, Electromask Corp.). Some features of these systems are high resolution (1.25 μm), virtually no runout over the wafer, automatic focusing at each step, long mask life, and relative insensitivity to dust on the mask (because of the reduced image size).

The eventual use of deep UV exposure may extend the useful wavelength range of conventional photolithography and thus allow somewhat higher resolution.[29] A few domestic commercial deep-UV systems are now reportedly being tested.

No X-ray exposure systems are commercially available as yet, but an experimental model (Cobilt), offering 2- to 3-μm resolution capability, is reportedly now being tested. This method, using flood exposure in a proximity mode (Fig. 17), appears quite promising in terms of resolution (limited by alignment, by dimensional stability of mask and wafer, by the resolving power of the resist, and by accuracy of defining the mask pattern) and anticipated moderate cost per wafer.[14, 26, 28]

Use of an electron beam for wafer fabrication appears to be limited to direct writing by a computer-controlled scanning method[28, 30] (Fig. 18). At present, this procedure is not commercially feasible because of low throughput, but improved system design and the advent of very large scale integrated (VLSI) circuits may bring the method into use in the 1980s.[14]

An alternative method for fabricating devices by electron exposure is electron-beam projection[28, 31] whereby a special thin-film photomask is bombarded with electrons, and resultant emission of electrons from the mask projects the mask image onto the wafer. However, because of problems, this approach has been virtually eliminated from consideration.

Resist material

The type of resist material chosen depends on the type of exposure system used. In general, photoresists cannot be used in electron-beam or X-ray exposure systems, but there are exceptions. For example, certain of the diazoquinone-type positive resist materials can be used in either deep-UV or electron-beam systems as well. In all areas of microlithography, more sensitive resist materials are constantly being sought, particularly in X-ray lithography, where low source intensity is a particular problem.

As mentioned previously, liquid resists are used almost exclusively, even in relatively low-resolution applications. Conventional UV/contact exposure processes have traditionally used negative photoresists, both for historical reasons and because of their greater process latitude[32] and lower costs relative to positive photoresists. However, the finer resolution capability of positive photoresist materials has led to a widespread shift throughout the microelectronics industry over the past several years, as more and more highly complex chips are designed.

Conclusion and a look ahead

The field of microlithographic processing for producing integrated circuit devices has evolved so far from classical lithographic procedures that a comparison is hardly possible. Requirements for producing the next generations of devices, such as 1M RAMs, will surely bring about more

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Daniel Ross joined the Technical Staff at RCA Laboratories in January 1964, where he worked on organic laser materials and investigations of the chemistry of organic derivatives of the rare-earth metals. He has directed and coordinated work on the interaction of laser radiation with organic materials for the RCA Graphic Systems Applied Research Laboratory.

Dr. Ross is currently Head, Organic Materials and Devices Research. In this position he has been responsible for investigations of novel materials and processes for electron beam recording, liquid-crystal display research, and photoresist materials and processes for kinescope fabrication. More recently, this work has focused on the development of improved resists for electron beam, "deep UV," and X-ray microlithography. During 1976 and 1977, Dr. Ross led a task force involved in the development and implementation of the complex set of coatings required for the RCA SelectaVision VideoDisc. He is the author of over 18 technical publications, has been granted 18 U.S. Patents, is a member of the Chemical Society (London), The Society of the Sigma Xi, and The American Association for the Advancement of Science, and is listed in American Men and Women of Science.

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developments of high sophistication and capability. Minimum geometries of 2 μm by 1980 and 1.3 to 1.5 μm by 1982 are estimated,[14, 33] and thus future trends in the solid-state industry will include such processes as X-ray and electron-beam exposure of wafers, and increased use of dry etching processes. However, the wide range of device requirements will certainly ensure continued use of conventional photolithographic processes in many areas as well.

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Photomask manufacturing—requirements, capabilities and trends

Major improvements in mask making technology during the 1970s have resulted in finer line structure, increased quality and reduced delivery times. Expectations are for increased requirements to obtain nearly perfect photomasks.

Photomask manufacturing is a key element in the continuing technological development of the solid-state business. The photomask, a glass substrate coated with chrome or a photosensitive emulsion, is the basic tool used in wafer fabrication to generate integrated-circuit or power-transistor devices. A typical IC wafer process requires 8 to 10 photolithographic steps, each of which involves the defining of an image on the wafer in an epitaxially grown silicon layer, an insulating or protective layer such as silicon dioxide or silicon nitride, or a conducting layer such as polysilicon or aluminum.

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The images to be transferred at the various steps of the wafer process are initially defined on the photomask. The procedures required to produce these defined images involve a number of critical interfaces between the designer, design automation personnel, the mask-operation and the wafer-fabrication facilities. The Photomask Technology and Operations Department (PTO) located in Somerville, N.J., is responsible for providing all photomasks necessary to support the Solid State Division's manufacturing operations. In addition, this department supplies photomasks to the Government Systems Division, the Solid State Technology Center, and the David Sarnoff Research Center. PTO is also responsible for the development of new mask technology.

Major improvements in mask-making technology have taken place in PTO during the 1970s. These improvements are related to changes in the nature of the interface between the design and photomask activities which process the more complex integrated-circuit designs and to the improved electromechanical-optical and chemical processing equipment used to make the photomasks. As a result of these changes, the ability to make higher quality masks has been considerably enhanced. The finer line structure of the masks makes possible larger circuit (die) sizes and larger arrays. This high quality has been achieved while mask and new tooling delivery cycle times have been reduced by 60 percent (since 1976). In 1979, production masks for integrated circuits will have line widths as narrow as 3 microns, die sizes as large as 7 mm, as well as 4-inch arrays on 5 x 5-inch masks. The largest die mask set useable for production, a 0.8 x 0.6-inch charge-coupled device (CCD), was generated for Electro-Optics and Devices, Lancaster, on RCA's electron-beam mask-generation system (MEBES), which was introduced into production during 1978.

Trends in mask parametric requirements

As the state of the art in wafer exposure technology advances, designers are able to create circuits that employ smaller circuit elements; the result is circuits of higher "packing density" or complexity. As a result of this general trend (Fig. 1), the mask maker is being required to tighten parametric requirements on the photomasks in the following areas:

Die Size: Die size is increasing rapidly (Fig. 2) especially the size of memory circuits. The combined requirements of wide field and high resolution will eventually approach the limits of the refractive optics now used in conventional mask making. However, the recently introduced electron-beam mask-making equipment (discussed below) will essentially eliminate this problem.

Circuit Element Size and Tolerance: As circuit design rules dictate smaller line widths, the control of line width necessarily becomes more critical, and more accurate measurement techniques are required. Current semi-automatic electronic measuring equipment has improved measurement capability to the extent that lines as small as 2 microns can be measured with a precision of ±0.05 microns and an accuracy of ±10 percent. A measurement system developed and under construction at the RCA Zurich Laboratories utilizes diffraction gratings on the mask and wafer and a helium-neon laser to measure line widths down to 0.5 microns with ±7 percent accuracy.[1]

Layer-to-Layer Registration: In addition to control of line widths, tighter design rules also require better control of layer-to-layer registration. Figure 3 shows the trend in this parameter. Commercially available optical comparators similar to the one shown in Fig. 4 provide precision down to approximately 0.125 microns, which is adequate to check layer-to-layer registration to within ±0.5 microns. (The requirement for registration tolerances tighter than 0.5 microns will coincide with the requirement for line widths narrower than 2 microns. Present indications are that this requirement will be met using direct imaging on the wafer, a technique discussed further below.)

Defect Density: The concept of defect density (defects per unit area) has been widely used as a measure of process performance in mask making and in wafer fabrication over the last five years. The relationship between defect density and die area* is used to predict circuit-probe yields in semiconductor manufacturing operations. As circuit packing density increases, however, the yield is influenced more by the number of defects on a mask and the size of defects, since a given defect will be more likely to affect a critical circuit element on a densely packed die. In addition, a given number of randomly distributed defects on a mask will affect a larger percentage of the dice on a wafer. Therefore, the increase in die sizes also requires a reduction in defect density if acceptable wafer-fabrication yields are to be achieved.

PTO has been utilizing the defect-density concept for the last five years as a means of tracking photomask quality. Substantial reductions in defect density have been achieved and continue to be made (Fig. 5) through improvements in the following areas: control of incoming materials; automatic processing and in-process controls; and master cleaning.

*Defined by the Poisson equation: $y = 1/(1 + D_oA)^N$, where y is yield; D_o is the killer defect density/critical layer; A is the die area; and N is the number of critical layers.

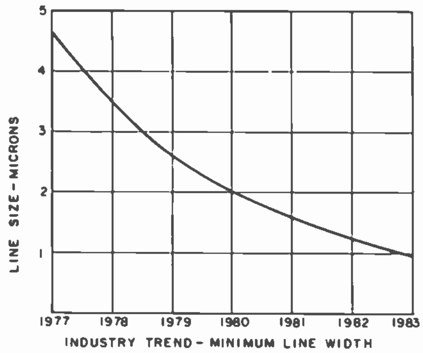


Fig. 1
Industry trend in line width. As the width decreases, the "packing density" or complexity of the circuit increases.

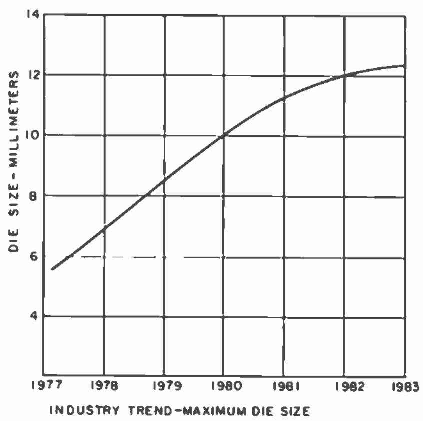


Fig. 2
Industry trend in maximum die size. Die size is increasing rapidly, especially the size of memory circuits.

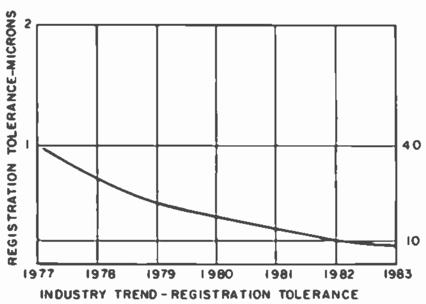


Fig. 3
In addition to control of line widths, tighter design rules also require better control of layer-to-layer registration. This figure shows the trend in the registration parameter.

Fig. 4
The latest versions of equipment, such as this registration analyzer, assure precision of registration down to approximately 0.125 microns.

Chronology of photomask processing sequences

Major improvements in mask-making technology have taken place over the years (Fig. 6); the result is significant improvement in mask quality.

Yesterday

Prior to the introduction of computer-controlled pattern-generator equipment in the early 1970s, the mask-making process started with a hand drawn 200X or 500X layout for each layer of the device. From this layout the mask shop would manually create a piece of "artwork" at the same scale as the layout. The artwork medium was a mylar sheet with a red film coating (Rubylith) which could be cut and stripped away from the mylar so as to leave the desired pattern. The artwork was then reduced to 10X size on an emulsion plate by means of a large reduction camera. The 10X emulsion plate, called a "reticle," was then placed in a step-and-repeat machine which reduced the size to 1X and created an array of identical patterns on a third emulsion plate. This third plate then became the "master." A chrome submaster was contact printed from this master. The submaster was then used to contact print (by means of the equipment shown in Fig. 7) emulsion or chrome "working masks, which were then shipped to the wafer fabrication lines.

As die sizes and complexity increased and element sizes decreased, more stringent requirements were imposed on mask parameters. The mask-making process outlined above became inadequate for the following reasons:

- Die size and complexity increased to the point where hand cutting of artwork became unfeasible.
- Problems were encountered at the camera in the first reduction from 500X to 10X because of wide-field lens distortion and poor resolution.
- Tightened requirements for defect density, critical-dimension control, and registration could not be achieved using the three-step process (emulsion master, chrome submaster, print).

A major advance in mask making was achieved in the early 1970s with the introduction of computer-controlled pattern generation equipment. The pattern generator produces a 10X emulsion reticle from a magnetic tape input. With this equipment, more complex reticles could be generated with a high degree of accuracy, and the problems previously encountered with the artwork-cutting operation and the first-reduction camera were eliminated.

The next major advance in mask making occurred when step-and-repeat equipment that was capable of exposing photoresist-coated chrome plates instead of emulsion was introduced. RCA acquired this equipment and, by 1974, had converted from a three-step master-to-print process to a two-step process (master, print). This change enabled PTO to produce a higher quality master for the following reasons:

- The inherent defect level of photoresist-coated chrome blanks was significantly lower than that of emulsion plates.

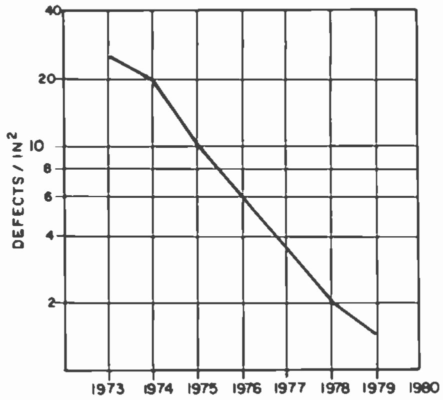


Fig. 5
Chrome-mask defect-density chronology. The curve is based on average defect density obtained by visual inspection of a 0.5 square-inch template area using an optical microscope at 100X magnification.

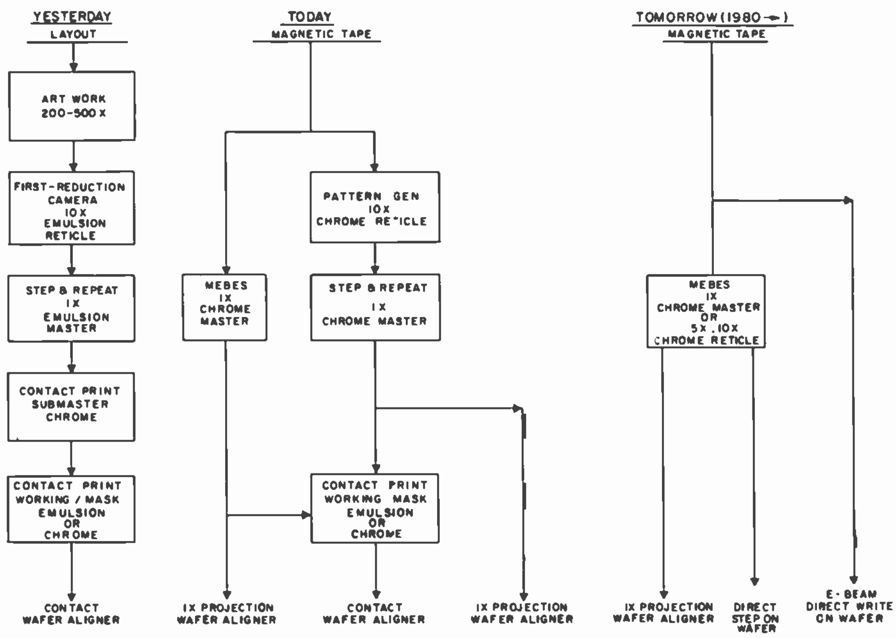


Fig. 6
Changes in photomask generation from the design to the wafer-lithography stage.

Fig. 7
A Tamarack printer used to contact-print emulsion or chrome "working" masks from a master. The working masks are used on the wafer fabrication lines.

- The flatness of chrome blanks was better than that of emulsion plates by a factor of 3X to 5X. A ground and polished glass substrate is used for the chrome blank while emulsion plate substrates are "as-drawn" glass. The improved flatness provided better control of registration and critical dimensions, since the step-and-repeat equipment used at this time employed fixed-focus systems.
- Resolution and critical dimension control was increased with the use of the chrome blank because: (1) the thickness of the imaging layer is 0.5 μm compared to 4 to 5 μm for emulsion; (2) the operating wavelength of the exposure light is lower: 436 nm for photoresist versus 546 nm for emulsion; (3) edge acuity of the pattern elements is significantly better for chrome than for emulsion.

The change from a three-step to a two-step process enabled PTO to reduce the defect density on chrome working masks by a factor of 2. Subsequent improvements have reduced this level further (Fig. 5). Registration was also improved by a factor of 2 by the elimination of the intermediate printing step.

Today

The two-step process described above is still used at RCA, although advancements in manufacturing equipment, incoming material quality, processing techniques, and inspection methods have improved the overall quality of the masks and the reliability of inspection results.

Incoming inspection provides control of defect levels, flatness, and speed of chrome plates. Automatic equipment is used for chrome-plate processing, providing an "all wet" process. This procedure generates fewer defects than the previous method, which involved a post-bake step, and provides better control of critical dimensions. The traditional method of defect inspection is the tedious and error-prone procedure in which an operator counts defects by means of a microscope. Automatic defect-inspection equipment, which increases the accuracy of this inspection, and the throughput, has recently been introduced, Fig. 8. The area inspected on each mask has been increased by a factor of 10 so that, currently, 5 square inches are covered; and the inspection is completed in two-thirds the time. Electronic measurement systems (Fig. 9) in use for approximately one year, provide significantly improved accuracy in the measurement of mask-pattern elements. With this equipment, line widths can be accurately measured to 2 millionths of an inch (0.05 micron). The present method of measuring mask-to-mask registration involves the optical comparison of a new mask with an existing one of the same type and measurement of the differences.

The equipment systems currently used for pattern generation and step-and-repeat procedures have also been greatly improved. These systems, computer-controlled laser interferometer machines, have increased the speed and accuracy of reticle and master generation. Air bearings are used to eliminate wear and increase speed; automatic focusing compensates for deviations in plate flatness. With the acquisition of the Electromask 2500 combination pattern generator and image repeater in 1977 (Fig. 10), PTO gained the capability to produce a chrome reticle directly on the pattern generator, thereby eliminating the contact printing step previously required. The Electromask 2500 can also be used in the step-and-repeat mode to generate chrome masters.

RCA purchased an electron-beam generation system called MEBES (Manufacturing Electron Beam Exposure System) (Fig. 11) in 1977, and is currently using the system to generate most of its very-large-scale-integration (VLSI) master requirements. This equipment is capable of generating a master directly from magnetic tape, eliminating the need for the creation of a 10X reticle. Since the reticle generation time for complex devices using optical pattern generators can be as much as 20 hours for one layer, significant cycle-time reductions have been achieved with MEBES. Total generation time for a master on the MEBES equipment is less than 1 hour, and is virtually independent of device complexity. Mask-to-mask registration on a MEBES mask set of ±0.125 μm is expected.

Electron-beam exposure systems represent a relatively new technology in the semiconductor industry. As we progress on the learning curve, improvements will be made in processing techniques and material quality so that the full potential of the MEBES equipment can be realized. The result will be production masters with micron geometries and very low defect densities.

Fig. 8
The accuracy of defect-inspection procedures has increased through the use of equipment like this KLA automatic mask-inspection system.

Fig. 9
This ITP electronic measurement system provides significantly improved accuracy in the measurement of mask-pattern elements.

Over the past several years there has been a major trend in wafer fabrication away from contact printing to 1:1 projection printing. Since masks for the projection aligners are used to expose thousands of wafers, the mask maker must supply masks of the highest possible quality. These masks are made on the step-and-repeat or MEBES equipment, with no contact-printing steps. The masks are inspected 100 percent by means of the automatic inspection equipment, and repairable defects such as chrome spots are removed by the use of a laser, so that a "near perfect" mask is delivered to the factory. Additional equipment to be purchased in the near future will make use of the output of the automatic inspection equipment to drive a laser to the location of the defect, permitting the operator to observe and classify the defects and remove those that are chrome spots. Other mask-quality parameters, such as registration and critical dimension control, are also improved by elimination of the contact-printing step.

Tomorrow

The use of projection-printing equipment in wafer exposure will increase during the three years beginning in 1980. The photomask operation will continue to supply masters generated on either MEBES or optical step-and-repeat equipment. Less critical, small-die medium-scale-integration (MSI) will continue to be made by means of conventional contact aligners. Contact prints will be supplied to the wafer-fabrication lines for these types. Improvements in material processing and automatic inspection techniques, including the introduction of the semi-automatic laser to remove excess chrome defects, will result in higher quality masks for the wafer-fabrication lines.

With the introduction of more VLSI devices with tighter design rules, however, new methods of wafer exposure will be required. Equipment has recently been introduced that allows the step-and-repeat process to be performed directly on the wafers; these "direct-step" systems, which expose the wafer through a 5X or 10X reticle, are modifications of existing mask-making step-and-repeat equipment and are capable of improving defect density and registration. Critical-dimension control will be improved by the use of automatic focusing, which compensates for wafer distortion. Vendors of this equipment are also developing automatic-alignment features that will compensate for lateral wafer distortion resulting from high-temperature wafer processes.

There is currently a great deal of interest in the direct-step systems described above; some of this equipment will be in use at RCA in 1979. The mask maker will supply this system with 5X or 10X reticles generated from optical pattern generators or from MEBES. Direct-step systems should be capable of producing devices with line widths of 1.5 microns in production.

The production of devices having micron or submicron line widths will require new wafer-exposure techniques. Electron-beam (E-beam) systems currently available commercially have the necessary resolution capabilities, but writing times are too long for the systems to be economically feasible in production. The next generation of E-beam equipment, expected to be introduced in 1980-81, will have acceptable throughput rates. X-ray exposure technology is currently in the developmental stage, and may become a factor in wafer exposure by the mid-1980s. This technology has the potential to produce wafers with fine lines and low defect densities, but an entirely new method of producing masks or reticles for these systems will be required.

PTO quality control

To ensure that photomask quality parameters meet specifications, a significant amount of effort is applied to the inspection of reticles, masters and working plates (Fig. 12). All reticles and masters are submitted by the manufacturing activity to a quality control (QC) tooling inspection group, and all must be certified as acceptable by QC before being used for subsequent manufacturing steps. After working plates are printed, production lots are submitted to a manufacturing inspection group where they are sample inspected.

Reticles are inspected for visual, dimensional, and pattern-integrity defects. Masters are inspected for verity of registration and critical dimensions and for defect density. Working masks are subjected to lot-sampling procedures by the manufac-

Fig. 10
The Electromask 2500, combination pattern generator and image repeater, makes possible the generation of a chrome reticle directly on the pattern generator and eliminates the contact-printing step previously required.

Fig. 11
The MEBES system is capable of generating a master directly from a magnetic tape, eliminating the need for the creation of a 10X reticle.

turing inspection group; parameters checked are the same as those for masters. Accepted lots of working masks are then submitted to a quality audit group which performs another sample inspection. Lots rejected at audit are returned to the manufacturing inspection group to be 100 percent inspected and resubmitted to audit. Lots accepted at audit are shipped to the wafer-fabrication lines.

Production and material control (logistics control)

The production and material control group in PTO plays a major role in the ability of PTO to meet commitments with regard to timely completion of new design master sets and delivery of working masks to the wafer-fabrication facilities. The functions of this group include the following:

1. Determining mask and master load based on customer inputs and historical data;
2. Scheduling the mask and tooling manufacturing areas;
3. Ordering sufficient raw material (chrome plates and emulsion plates) to support manufacturing needs;
4. Assisting in the preparation of daily production reports;
5. Tracking the progress of jobs and issuing computer summaries; and
6. Maintaining adequate control of work-in-process to keep cycle time within commitments.

The success of this group is reflected in the actual cycle time trends.

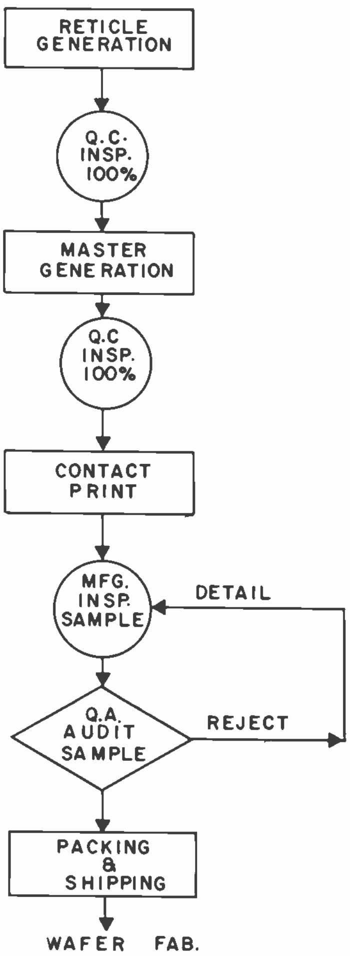


Fig. 12
In-process quality control and quality audit flowchart.

Cycle time trends

In addition to developing the capability to deliver high-quality photomasks that are cost competitive with those supplied by outside vendors, PTO was faced with the need to make drastic improvements in cycle time to meet the designers needs for quick turn-around on new designs. A typical complex integrated-circuit design will require at least one, and typically three or four, iterations of the initial design. In order to remain competitive in the rapidly changing solid-state business, these iterations must be converted from the designer's mind to a finished wafer in very short order.

By applying improved logistics control, shorter process sequences, and improved process controls, PTO has been able to reduce the average cycle time from tape input to finished mask from approximately 20 days in December 1976 to approximately eight days by June 1978. At the same time, the handling of a limited number of high-priority jobs on a last-in-first-out (LIFO) basis has resulted in average cycle times of four days. Single level ROM variations are frequently handled in two to three days. Utilization of MEBES, which promises to further shorten the process sequence, permits a more typical turn-around of three days, even without LIFO handling.

Conclusions

As indicated in the section on photomask processing sequences, the trend over the past few years has been towards a reduction of the path length between the designer's input (artwork or pattern-generator tape) and the photolithographic processing of the wafer. This trend undoubtedly will continue during the next few years with direct step-and-repeat on the wafer becoming a feasible production process in 1979-80, and direct write on the wafer (with newer E-beam equipment) becoming feasible for production use in 1981-83. The higher initial costs of these equipments and the lower throughput, however, will limit their use to state-of-the-art LSI and VLSI designs for the next few years. Consequently, the need for photomasks to satisfy the bulk of wafer production needs will not disappear. In view of the strong current trend towards projection printing to minimize the defects inherent in contact printing and to increase mask life, a significant portion of the photomask load will shift from contact prints to master photomasks. The requirements for initial inspection and repair of these masters to obtain nearly perfect photomasks will increase. The higher cost of the master photomasks relative to contact-print photomasks will also increase the attractiveness of automatic mask-inspection equipment at the wafer-fabrication facilities. Finally, one requirement that will become more important as these trends become established is the need for an increasingly close integration of the photomask operation with design engineering, design automation and the wafer fabrication facilities.

Acknowledgment

A technology survey completed by Photomask Technology and Operations in 1978, which resulted in a three-year photomask technology projection, served as the basis for some of the projections on future mask parametric needs and equipment trends. This survey included data obtained by R. Rhodes (no longer with RCA), R.L. Van Asselt, and the author during visits to various photomask houses, equipment manufacturers, and competitors. Inputs from the Solid State Division, also factored into these projections, were obtained from a questionnaire survey of the key people in the various product lines.

Reference

1. Geshner,R.A., Kleinknecht,H.P., Meier,H., and Mitchell,J., "Linewidth Measurements on Masks for Integrated Circuits," PRRL-78-TR-017, 9/28/78.

M.J. Meehan

Defect densities in integrated circuits

A mathematical model sets some guidelines to help maximize integrated-circuit yields.

Defect density is an expression commonly used to describe the density of defective sites on an integrated circuit as a result of wafer processing. Defect density (D_0) is expressed as defects per square inch.

The electrical yield of integrated circuit wafers depends partly upon circuit size and the defect density incurred during processing of the wafers. It is generally agreed that a wafer-fabrication process which is sufficiently controlled to yield good dimensional and parametric values produces wafers whose circuit-probe (electrical test) yield is limited primarily by random defects. The most prevalent of these defects, the so-called "photo-induced defects," are those generated in the photoresist-etching process. As a consequence of this dependency, various defect-density models have been developed and are in use throughout the semiconductor industry to aid in yield prediction.

Fabrication area model

One of the simpler defect-density models (based on Bose-Einstein statistics) was chosen for use in the CMOS fabrication area at Findlay, Ohio. The model assumes the defects are random; the calculated yield predictions are close approximations of actual results.

The equation is as follows:

$$Y = \frac{1}{(1+D_oA)^n} \qquad (1)$$

where:

Y = yield
D_o = defect density in defects/in^2/level
A = die area in sq. in.
n = critical photo levels

Solving for D_o, the equation becomes:

$$D_o = \frac{(1/Y)^{1/n} - 1}{A} \qquad (2)$$

In the model used at Findlay, all the photo levels are considered critical with the exception of the bond-pad photo level. This photo level uses a proximity mode alignment system and, as a result, both the number of defects generated and their impact on yield are so small as not to be considered critical. Empirical results have supported that assumption. In other levels, as a worse-case assumption, defects have been considered to be "killer defects," that is, defects capable of causing a circuit to be rejected at current probe (C.P.).

Sample calculations of D_o can be made by this typical use of the model equation (2):

*Type CD*4011A Chip size .056 x .053 in.
(Area = .002968 sq. in.)
C.P. Yield = 80%
n = 6 Therefore, D_o = 12.7 def/in^2/level

*Type CD*4008A Chip size .083 x .086 in.
C.P. Yield = 60%
n = 7 Therefore, D_o = 10.5 def/in^2

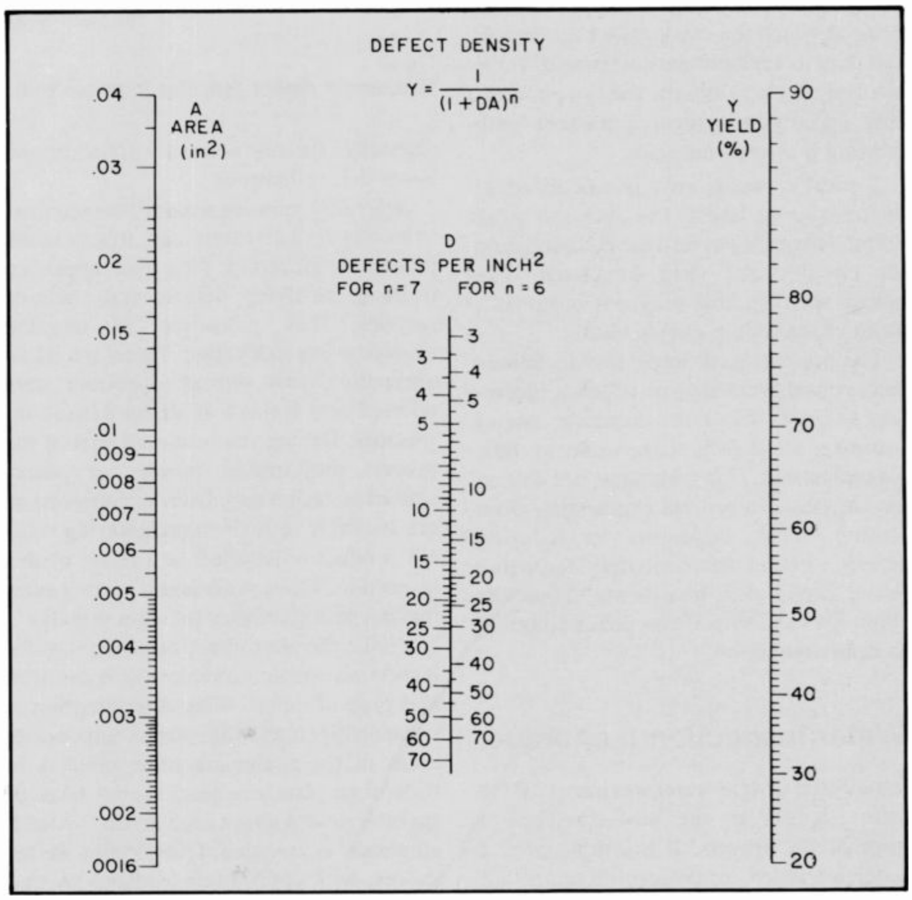


Fig. 1
Nomograph for estimating defect density of CMOS six and seven photo-level products.

Establishing base line defect density

The model was tested on bipolar types run in the CMOS fabrication area, and involved Process #2 with six critical levels and Process #4 with seven critical levels. The majority of CMOS types have either an A or B suffix. Types with A suffixes have six critical photo levels, and those with B suffixes have seven.

A nomograph (Fig. 1) is shown for the two main processes having six and seven critical levels. Using the nomograph or a calculator, one can readily assess the correct defect density for any CMOS product.

Photomask inspection

The photomasks used in the manufacture of integrated circuits are a prime source of defect generation in the wafers. Thus, inspection of new and used masks before and during use is the key to controlling defect density at each photo level. Mask life is finite since defects accumulate during use.

A typical graph showing the increase in defect density with usage is shown in Fig. 2. Empirical data is required to determine the point at which the mask causes more yield loss than its replacement cost is worth. One can only seek to obtain the lowest mask cost (maximum usage) consistent with meeting projected die costs.

Typically, wafer cost is calculated at different usage levels. The observed mask defect density is put into the equation, and the circuit-probe yield calculated. The lowest net chip cost may not occur at a point of maximum circuit yield.

The present mask-inspection technique has evolved from that of training inspectors to count only killer defects to one of counting all defects observable at 80X magnification. This technique has shifted the emphasis in process engineering from training mask inspectors to reducing defects, whether the defects definitely cause circuit probe yield loss or not. Thus, the emphasis has shifted from defect counting to defect reduction.

Wafer inspection technique

Initially the CMOS wafer was inspected for defect density at the post-development stage of the process. If a sample from a wafer lot failed inspection, the entire lot was reprocessed. A lot that failed was then traced through its recycle procedure; generally, the reprocessed wafers showed lower defect densities.

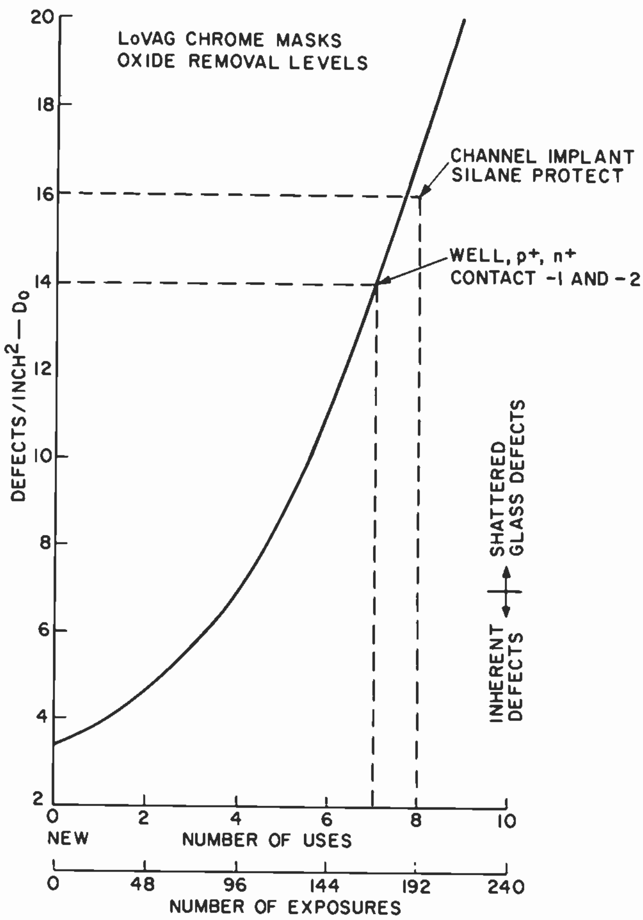


Fig. 2
Photomask defect densities increase with use.

Originally, nine inspectors were required to handle the wafer start load. But, so much process engineering time was spent on training, verifying defects and tracking recycles, that correction of ongoing problems was ineffective. Therefore, as an alternative, two veteran operators were selected and trained as defect-density inspectors. During the post-etch part of the process, they inspect samples for control and information only from as many lots as are available in their manufacturing shift. No product is recycled as a result of this inspection. Then, process engineering summarizes and publishes the data weekly.

Unlike the photomask inspection, wafer inspection sets limitations on size, location and type of defect. This determination is more readily made with wafers since active areas of the circuit are more obvious in wafer form. The inspectors are not asked to make decisions about each defect. Instead, emphasis is on identifying major defect modes, with appropriate feedback to, and correction by, process engineering.

It should be noted that the defect-density inspection is performed subsequent to both post-develop and post-etch inspection procedures. This inspection removes from the population some of the nonrandom defects, such as misalignment and poor definition. Typically, six percent of the product wafers require reprocessing as a result of nonrandom defects. Although handled separately from the defect-density data, routine photoreprocessing must be kept under control. Excessive reprocessing can lead to increasing defect densities.

Practical uses of the model

Process monitoring and control

Defect densities calculated from circuit-probe yields are plotted by a technician; the plots show daily and month-to-date defect-density values for CMOS A and B series processes. Mean die sizes are used in the calculations.

As an example of the application of this information, the data taken during two weeks of a typical month (May 1978) have been selected and used below and in Tables I and II to demonstrate the effects of

Table I
Defect densities and major failure modes for a one-week period ending May 19, B series.

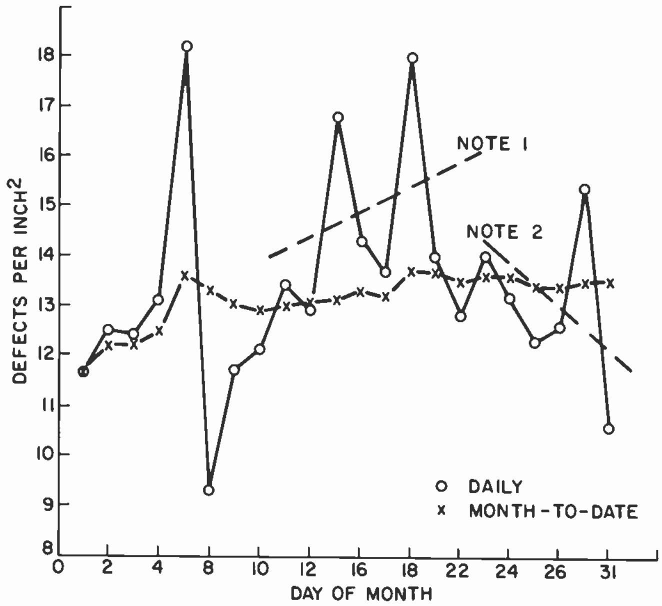
Level		*# Pellet Insp*	*# Pellet Defect*	*% Pellet Defect*	*Total Defects*	D_i	*Major Failure Mode*
Well	Daily	-	-	-	-	-	
	MTD	160	11	6.9	11	6.3	Islands
N−	Daily	120	4	3.3	4	3.0	
	MTD	200	8	4.0	8	3.6	Distorted & damaged
P+	Daily	40	2	5.0	2	4.5	
	MTD	120	9	7.5	11	8.3	Hole, dirt
N+	Daily	160	11	6.9	11	6.3	
	MTD	440	37	8.4	38	7.9	Holes, islands
S.O.	Daily	30	6	20.0	7	21.2	
	MTD	190	35	18.4	41	19.6	Distorted & damaged
Contact	Daily	80	5	6.3	13	14.8	
	MTD	310	12	3.9	22	6.5	
Metal	Daily	160	28	17.5	38	21.6	
	MTD	510	98	19.2	122	21.7	
MTD Avg. D_i Level					10.6 def/in^2		

Table II
Improvement in defect densities for one-week period ending May 26, B series.

Level		*# Pellet Insp*	*# Pellet Defect*	*% Pellet Defect*	*Total Defects*	D_i	*Major Failure Mode*
Well	Daily	80	2	2.5	2	2.3	
	MTD	240	13	5.4	13	4.9	Islands
N−	Daily	30	4	13.3	5	15.2	
	MTD	230	12	5.2	13	5.1	Islands
P+	Daily	40	2	5.0	2	4.5	
	MTD	160	11	6.9	13	7.4	Scratches, distorted & damaged
N+	Daily	110	9	8.2	10	8.3	
	MTD	550	46	8.4	48	7.9	Islands, (distorted & damaged, torn)
S.O.	Daily	120	6	5.0	6	4.5	
	MTD	310	41	13.2	47	13.8	(Distorted & damaged, holes, torn)
Contact	Daily	80	4	5.0	5	4.5	
	MTD	390	16	4.1	27	6.3	
Metal	Daily	90	12	13.3	12	12.1	
	MTD	600	110	18.3	134	20.3	
MTD Avg D_i Level					9.4 def/in^2		

actions taken in wafer processing on inspected defect density (D_i) and the relationship between inspected defect density and circuit-probe defect density (D_o).

Defect densities (D_i) for the metal level in the week ending May 19 are compared with those of the following week, May 26. The inspection data show the reduction (21.6 def/in^2 to 12.1 def/in^2) accomplished by the introduction of a release coating on the metal masks. This improvement is clearly visible in its effect on the circuit probe defect density plotted in Fig. 3. Results as dramatic as these are the exception rather than the rule, but careful examination of circuit-probe defect-density trends will usually signal existing or impending problems.



NOTES
1-PERIOD OF HIGH DEFECT DENSITY AT METAL INSPECT; D_I = 21.7 DEF/IN^2
2-DEFECT MODE CORRECTED; D_I = 12.1 DEF/IN^2

Fig. 3
Plot of defect density vs. day of month, May 1978.

Identification of design problems

The general yield and defect-density data are also analyzed periodically to determine whether certain types meet the defect-density model. A few examples of CMOS design-related yield problems are as follows:

1. *Type* 10256

Process: B-Series (n = 7)
Chip size: .053 x .054 in.
Circuit yield: typical 48%
D_o = 37 def/in^2/level (Eq. 2)
B-Series types of similar chip size performed as follows during the same processing time-frame.

Type	*C.P. Yield* (%)	D_o
4051B	57	11.2 def/in^2
4520B	56	10.8
4050B	66	15.5

Redesigned Version of 10256

Chip size: .064 x .045 in.
Yield: 81.1%
D_o = 10.5 def/in^2/level

The redesigned type now fits the model.

2. *Type CD*4027B

Process: B Series (n =7)
Chip size: .082 x .063 in.
Circuit yield: 49%
D_o = 20.8 def/in^2/level
The performance of B-series types of similar chip size is the same as that shown under example 1, above, for the type 10256.

The problem in this case was not one of design. Through an exhaustive analysis of the circuit-probe test data by engineering, a *random* missing element of a particular transistor was found on the photomask step-and-repeat master, and on the production contact prints. The anomaly occurred in the transfer of the design from the reticle to the step-and-repeat master.

Wafers were manufactured using prints from a new step-and-repeat master. Results were as follows:

C.P. Yield = 64.7%
D_o = 12.4 Defects/in^2/level

This type now fits the defect density model.

3. *Type* 3123 (*Bipolar*)

Process: #2 (n = 6)
Chip size: .053 x .045 in.
Circuit yield: 65% typical
D_o = 31 def/in^2

Other Process #2 runs in the same time frame had defect densities of approximately 15 def/in^2. Analysis of the circuit-probe data showed a high parametric loss for a specific resistor. The resistor was redesigned and the process adjusted to recenter the resistor value. Initial circuit-probe yields ran at 80 percent or 15 def/in^2. However, subsequent tightening of the parameter limits at circuit probe has degraded the yield to 67 percent or 30 defects/in^2. Another redesign is now required to enable this circuit yield to be photo-defect limited.

New product and process critiquing

- New products in the CMOS Model Shop in Findlay are evaluated for their ability to fit the model. If defect-density variations for the new product are within ±10 percent of the current, accepted value, the new product qualifies for manufacture.
- The effect of new design rules can be evaluated in a manner similar to that used for new products, but with more initial emphasis placed on device parameters such as source to drain breakdown voltages, threshold voltages, etc., *prior* to circuit probe testing.
- Standard cost yields can be properly established using the model and direct costs calculated for each type. Marketing then has accurate data to use in setting an average selling price (ASP) consistent with the profit-margin goals of the division. Engineering effort can then be focused on the problem types when direct cost and ASP mismatches occur.

Justifying capital-equipment purchases

State-of-the-art wafer-processing equipment is required to reduce and control defect density in wafer fabrication. The extent of defect reduction is evaluated using various means that depend on the equipment under study. Some of the sources are as follows:

- Vendor specifications and/or supporting data generated in the field or at the vendor's plant.
- Rental of equipment and empirical data generated in manufacturing.
- Wafers sent to a vendor with analysis of results at the vendor or in manufacturing.
- Industry trends, seminars, technical papers.
- Identification of a defect cause which a new piece of equipment eliminates, e.g., auto loading of mask aligner eliminates tweezer loading (a known cause of defect generation).

Once the potential for defect-density reduction is substantiated, it is used in the defect-density equation. The cost reduction associated with the projected circuit-probe yield improvement is calculated. If there is not an appropriate return on investment, the capital request will be rejected and an alternative method sought to reduce the defect density. Facility improvements can be justified using the same technique.

Summary

The foregoing discussion is a simplistic presentation of a rather complex manufacturing discipline. Enormous effort is directed daily at maintaining and upgrading our control of defect density. However, the utility of the tool more than justifies this expenditure. The further refinement and application of the technique will help to establish the controls necessary for cost-effective production of integrated circuits.

Acknowledgments

D.G. Cox contributed Figs. 1 and 3 of this article, and D.P. Hagerty, Fig. 2; J. Huffman supplied the information for Tables I and II. J. Arico assisted in the preparation of the paper through technical discussions with the author and provided support in all phases of publication.

M.J. Meehan joined the Solid State Division in Findlay in 1973 as Leader, Technical Staff, MOS Wafers. In that capacity he was responsible for the engineering effort directed toward improving wafer fabrication yield and quality. At the time of the writing of this article he had assumed the responsibility of Manager, MOS Wafer Fabrication. He has since left RCA.

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Computer-aided manufacturing for the semiconductor industry

A CAM system is basically set up to collect factory-generated data from people or equipment, analyze it, reduce it, and feed back control information to people or to equipment.

CAM's task

Computer aided manufacturing, or CAM, has different meanings to people in different manufacturing environments. That is to say, industry uses computers to aid manufacturing in a variety of ways. For example, a manufacturer who moves his product through the factory in "lot" form has fundamentally different data requirements than one with product that moves through the factory continuously, such as in a process type industry.

Another anomaly in industry is the relationship between CAM and CAD (Computer Aided Design). Sometimes there is close alignment between the two, such as in the automotive industry where the CAD group generates many of the control programs required by CAM. In the electronics business, however, the relationship between CAD and CAM is not as well defined.

The Solid State Division (SSD) has used computers to aid the manufacturing of semiconductors for well over ten years. The two major applications have been:

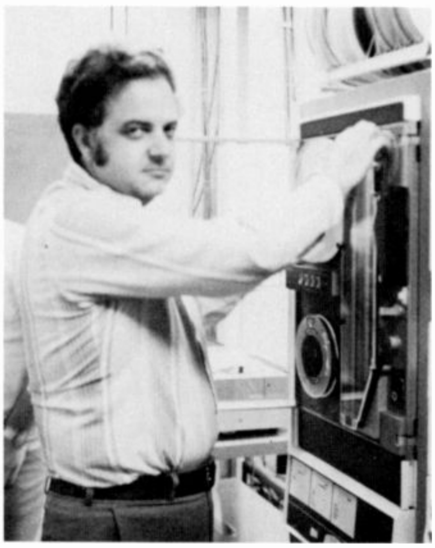
1. Minicomputers for controlling test sets.
2. Large and small computers for developing daily production reports.

Test set control was an early application of the first minicomputers. Over the years computer control in this area has become more and more prevalent and sophisticated.

The daily production report was a pioneering effort when first placed on the local site business computers and operated in batch, using punched cards. In 1974 an IBM System 7 was placed on line to accomplish real-time data collection. Although some production data reports were available directly from System 7, the daily production report was still generated from the IBM 370 by data received from System 7.

Three years ago use of computers for control of process equipment emerged when computer-controlled furnace tubes became available. Now, computerization of semiconductor process equipment is further accelerating with the advent of the low-cost microprocessor. The bulk of future semiconductor process equipment will certainly be controlled by microcomputers.

In anticipation, SSD has set up a CAM



Jim Rudolph joined the Small Signal Transistor Design activity at RCA, Somerville, in 1964. He transferred to Findlay in 1968 and began work in wafer fabrication of silicon transistors and bipolar integrated circuits, and circuit probe and final testing of bipolar integrated circuits. He is currently Leader, Computer Aided Manufacturing, Integrated Circuits.

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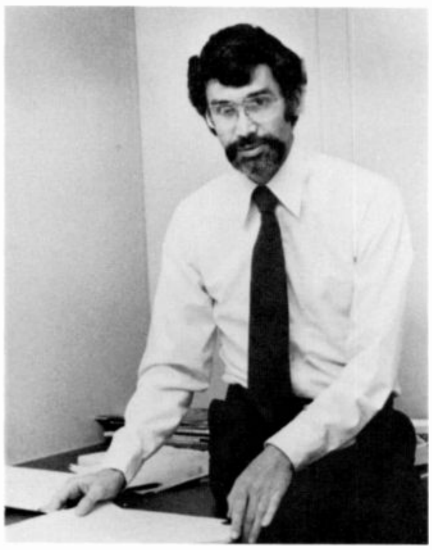

Stuart Levy joined RCA in 1959 as a Project Engineer for the Ballistic Missile Early Warning System (BMEWS) and helped in its installation in Thule, Greenland. He later transferred to the Corporate Staff Manufacturing Technology group. He joined the Solid State Division in 1974 in Findlay, Ohio, and later transferred to Somerville, N.J. as Manager, Computer Aided Manufacturing. He is presently Manager, MOS Test Technology.

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group whose mission is to employ various real-time computers in meaningful, integrated systems to aid the division in semiconductor manufacturing.

A CAM system is basically set up to collect factory-generated data from people or equipment, analyze it, reduce it, and feed back control information to people or to equipment. Figure 1 shows a sample system.

The functions of CAM are in three major areas:

1. Logistics management
2. Test data collection and analysis
3. Process equipment monitoring and control

Goals of CAM in manufacturing

As a first step in determining what CAM can do for industry, consider the three objectives of manufacturing: build a product of good *quality*, at a low *cost*, to meet a *delivery* date.

To keep tight controls on these three goals, a substantial amount of data must be continually collected and examined. This is especially true in semiconductor production because of two special characteristcs of the business. The first is the number of distinct steps in manufacture, which is upwards of 300. The second is the number of variations in the product types produced. This is of the order of several hundred, and many of these types require different process sequences. One need only multiply the hundreds of steps, by as many different product types, and the volume of data required to monitor semiconductor manufacturing performance can be seen as overwhelming.

1. Logistics management

This is the handling of production flow data. There is a sequence of process steps for each type of device. Certain process steps are designated inventory control steps which are mandatory reporting stations. Lot movement data of the following type must be entered into the system at these steps:

Lot Number	Scrap Units
Process Step	Recycle Units
Net Good Units	

Logistics management systems are designed to operate under lot control, that is, product movement in the factory is by lot, where each lot has a unique lot number. The size of a lot is arbitrary and may vary from one unit to several thousand, based on handling and processing considerations. In a typical wafer fabrication area, storage and processing occurs in carriers which hold 24 wafers each.

Lot integrity

During processing, lot size decreases as units are rejected or recycled. As a result, the production area soon has a large number of lots, each with very few units. To minimize this problem, CAM allows two or more lots to be combined into one. On the other hand, where necessary, "sublotting" will form a new lot from a portion of an existing one. This freedom to break apart and combine lots involves the concept of lot integrity.

Lot integrity implies that once a lot is formed, no additional units may be added. Lot combination is not allowed with full lot integrity. The history of each unit in the lot is the same as the history of the lot itself. It is very important to understand the distinction between lot control and lot integrity. Whereas lot integrity is impossible without lot control, lot control neither implies nor requires lot integrity. While a minimum level of lot integrity is necessary to provide definitive cause/effect data relating processing parameters to test yield, too high a level of lot integrity will result in production delays due to the large number of lots either created or being held as a result of recycling. Any level of lot integrity, from zero to 100 percent, is possible with CAM systems.

One advantage of lot control and the reporting of lot movement into the CAM system is that CAM *adds time of entry* to all data entered. This allows the system to calculate the time it takes the lot to move from one reporting station to the next. This is called cycle time. The CAM system can report cycle time for individual lots, or calculate an average cycle time between any two reporting points for all lots.

The advantages of the lot control, therefore, are:

- Better control of product on the floor;
- Improved data in CAM since more validation is possible;
- Cycle time available; and
- Lot status available;

while the advantages of lot integrity are:

- Lot traceability;
- Lot history; and
- Correlation of test data for a lot.

The benefits of a logistics management system are primarily improved visibility of yields, cycle times and inventory control, allowing supervision and management to improve performance.

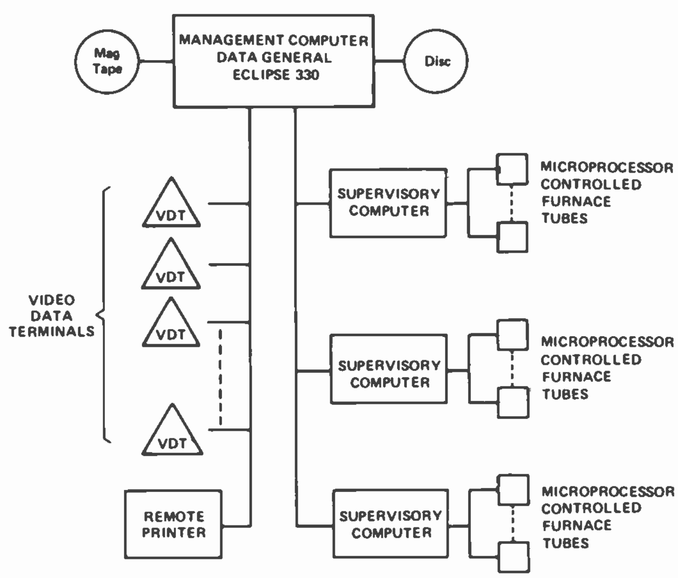

Fig. 1
Typical production line CAM system, where, through video terminals, all lot data is collected. Direct interface with diffusion furnace tubes provides monitoring of performance and downloading of control recipes.

2. Test data collection and analysis

This operation is concerned with product-oriented data and the interfacing with test sets and test systems. Inputs describe such characteristics of the product as:

- Resistivity
- Thickness
- Wafer acceptance/electrical test (test key data)
- Circuit probe test data
- Final test data

The outputs of the CAM systems consist of summary (and trend) reports, histograms, and customer reports. Another output of the CAM system is the capability of downloading test programs. This is the storage of test programs in the CAM computer and, upon request, transferring the programs directly to the test set.

Test data collection and analysis systems are in operation at the present time. One such system collects resistivity and thickness data, and after analyzing the data, generates proposed recipes.

Another system develops histograms from wafer test key data; while still another system digests test data and generates complete customer reports for the High Reliability activity.

One of the key benefits of analyzing test data is to give engineering the summaries they need to make proper judgments in their task of improving yield. Downloading test programs improve test set productivity and reduce operator error.

3. Process equipment monitoring and control

This function concerns data relating to temperature, pressure, gas/flow, alarms, equipment sensors, and other such variables collected from process equipment. In addition to the summary report output of the CAM system, the system has the capability to interface the process equipment and control it. Also, recipes can be downloaded to the equipment to reduce operator error, such as in the operation of diffusion furnace tubes. Prior to entering the wafer lots in the tube, the operator makes an entry into the CAM system. The system confirms that the lots are the same type, that they are ready for a diffusion step and that the furnace tube is the right one. The CAM system then downloads the correct recipe and starts the process. It is generally agreed that present manual operation results in operator errors and reduced yields.

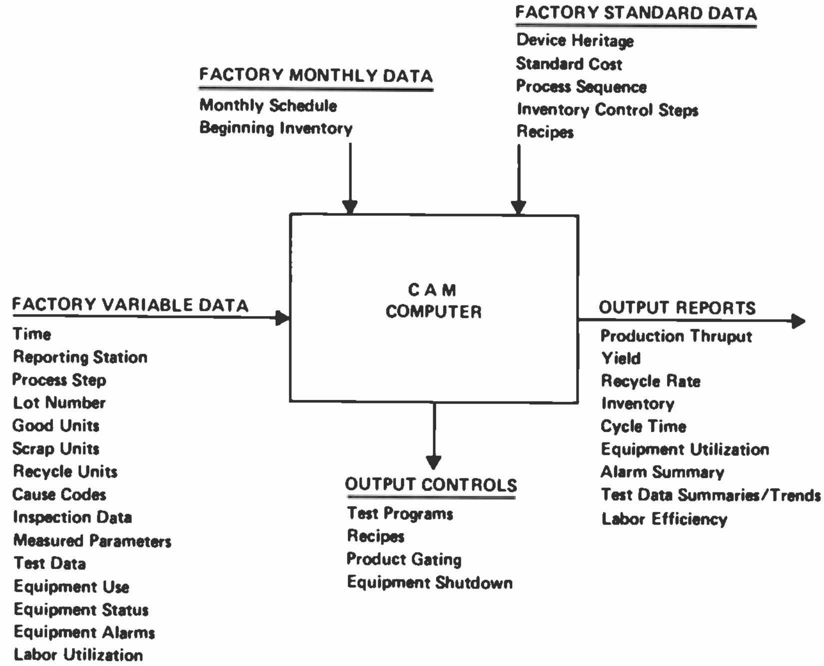

Fig. 2
Data inputs and outputs of the CAM computer.

CAM system data

Fig. 2 depicts the data flowing into and out of the CAM system. Input data is divided into three categories. First is the factory variable data. This includes all the dynamic data of factory logistics, test, and process equipment. The second category is called factory monthly data. This is production-related data such as scheduling and inventory that, in a typical factory environment, changes monthly. The third category is factory standard data, which describes the manufacturing operation. Some change daily, some yearly, but the data is required in the CAM system so that CAM can validate incoming data, and develop analysis and reports that include device heritage, standard cost, process sequences, inventory control steps, and recipes.

Device heritage refers to a "father-son" relationship of a device as it moves through the factory. Device heritage must be available in the system so that appropriate validity checks can be performed on the input data and historical trends can be developed.

Standard Cost data is required so that production data can be used to generate financial reports such as costing inventory or material variance. *Process sequence* by type is required so that incoming data can be validated. It will also insure that lots go through the process sequence and errors are not made. *Recipe* data can be used to control production equipment. For example, on diffusion furnaces, where setup conditions often vary from run to run, direct computer control of the operation, using recipe downloading, will minimize yield loss due to operator error.

The output data of Fig. 2 is in two categories. The first contains reports which are used by supervisors, engineers, and managers in controlling the factory. In the second category of outputs are direct controls to process equipment. The reports give the factory the tools necessary to improve their operation; and the direct controls eliminate operator errors.

CAM implementation

How then are the CAM functions shown in Fig. 2 physically structured? There are four requirements: (1) a technique for inputting data must be determined; (2) methods for handling the large amounts of data in the CAM system must be developed; (3) distribution of computer power must be considered; and (4) the system must have operating characteristics that are satisfactory to the user.

Many considerations including previous systems, non-CAM systems, and experiences of a variety of people come into the structuring of a computer system. Some of the more important decisions made relative to the system were:

1. Use video data terminals (VDT) with full alpha/numeric keyboards for inputting data.

2. Use the Data General Eclipse computer with a 96 megabyte disc as the mainstay of the system.
3. Use microprocessors or minicomputers in a distributed mode to reduce the load on the main computer.
4. Use a data base management system as the core of the software.
5. Use standard software as much as possible.

TYPE______LOT NO._____CLOCK NO.____ACTION ______OPERATION CODE_____

ACTION LINE

Fig. 4
Action line screen on VDT to be filled in by operator.

TYPE 3134G   LOT NO. 1   CLOCK NO. 601   ACTION MOVE   OPERATION CODE 610

MOVE OF PRODUCT FROM STEP 340 (FINAL POK INS)
TO STEP 610 (EPI)

NET	SCRAP	CODE	LOST	FOUND	RECY
- - -	- - -	- - -	- - -	- - -	- - -
48 - -	- - -	- - -	- - -	- - -	- - -
	- - -	- - -			
	- - -	- - -			
	- - -	- - -			

Fig. 5
Screen of VDT which is used to move product through reporting stations.

Computer configurations

There are a variety of ways to systematize computers. A multitude of small, independent processors can be made to do individual jobs; at the other extreme, one large processor does the entire job. The several independent processors offer the advantage that if one fails, only a small part of the system is down; but to integrate all the data from the independent computers requires a host computer communicating to all the smaller ones. The advantage of the large single computer is that the data for a large activity is centralized in one computer; of course, if that one computer should fail, the entire system is down. Between these two extremes there is a variety of options which mix small computers with large computers either in loops or in hierarchical structures.

Figure 3 depicts the computer configuration chosen. It basically separates the computers by function.

Manual inputting and outputting

The primary device for inputting data from the factory floor is the video data terminal with a full alpha/numeric keyboard. SSD has previously used VDT's in real time production reporting systems. They are fast, accurate, and extremely flexible. The input data can be alpha/numeric.

The procedure starts with an action line screen shown in Fig. 4. The operator keys in the appropriate data and another screen will come on for a specific application. Fig. 5 shows the "move" screen which is used to move product through a reporting station. While the operator is filling in the screen, the VDT is off line. When the screen is filled in, the operator presses the send key, transmitting the whole screen to the computer. The screen is cleared and an action line screen appears waiting for the next entry.

A variety of input screens are available to serve different applications. Some screens will allow or require the inputting of test data such as resistivity. Also, a variety of retrievals are available so that production personnel can review the status of the operation.

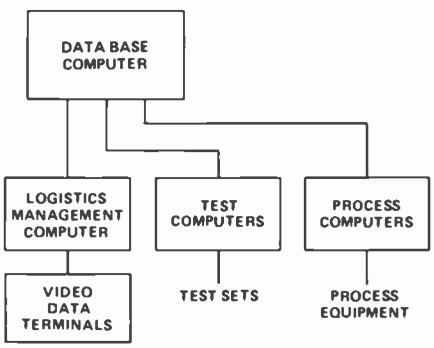

Fig. 3
CAM computer capable of handling test data and process equipment.

Automatic inputting and outputting of data

An intermediary computer is used to transmit data between the CAM computer and the process equipment. The purpose of this computer is to satisfy the protocol of the process equipment, digest the data wherever possible, and control the process equipment if required.

Several different types of intermediary computers have been used, such as:

1. COSMAC 1802 microprocessor;
2. Hewlett Packard 9825 computer/calculator; and
3. Computer Automation computer as a part of a delivered Thermco furnace tube system.

Software

Not all CAM systems use the same software. For the basic logistics management task, the Solid State Technology Center (SSTC) has developed a software package which they call PMC — *P*rocess *M*onitoring and *C*ontrol software.

PMC is a general purpose system for logistics management, and is expandable to process equipment monitoring and control.

The PMC software includes a sophisticated data base management system and other program modules tailored to semiconductor manufacturing tasks.

Operating SSD systems

Following are some highlights of the real time CAM systems described in Table I and presently operating in SSD.

1. *OPEN*
   Though solely a logistics management system, this first-time use of data terminals for real time data gathering proved that VDT's can successfully collect production data.
2. *RTE*
   A supervisory computer for up to six multiple computer-controlled test sets is now being interfaced with circuit probe test sets.
3. *WAT*
   For over a year, WAT has been successfully contributing to early detection of wafer fabrication problems.
4. *HiRel*
   Since September of 1977, this system has completely automated the once tedious

Fig. 6
The impact of microprocessors on computer-aided manufacturing system.

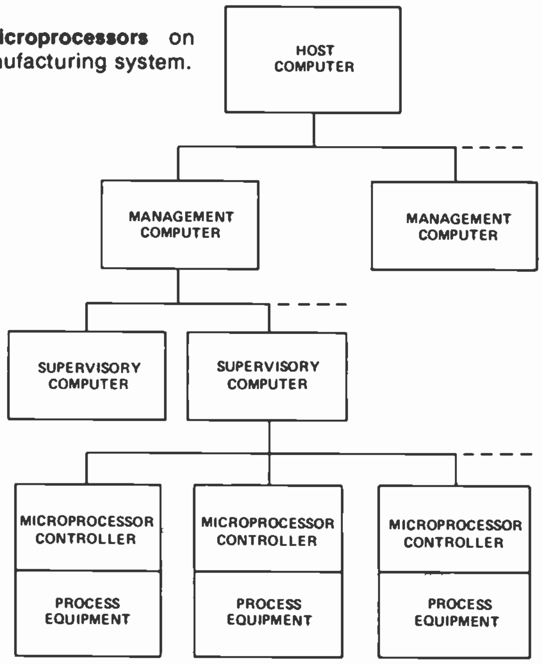

Table I
The seven CAM systems of SSD.

Name	*Description*	*Location*	*Date on-line*	*Computer*
OPEN *O*n *L*ine *P*roduction *E*ntry *N*etwork	Real-time logistic management system for MOS & bipolar. Did not use lot control.	Findlay, Ohio	1974	IBM Sys. 7
OPEN	A logistics management system for HiRel using lot control.	Findlay, Ohio	1974	IBM Sys. 7
RTE *R*eal *T*ime *E*xecutive	Data collection and analysis by a host computer from computer-controlled test sets.	Mountaintop, Pa.	1975	HP 2100
WAT System *W*afer *A*cceptance *T*est	Test data collection in real time from a WAT system and circuit probe testers.	Findlay, Ohio	1977	Data General Eclipse 330
HiRel Test Data System	Collection of test data into a data base, generation of HiRel customer reports.	Findlay, Ohio	1977	Data General Eclipse 330 Eclipse 130
Bipolar Wafer Fab.	A second generation logistics management system.	Findlay, Ohio	1979	Data General Eclipse 330
ERIC *E*pitaxial *R*eal *T*ime and *I*nformation *C*ontrol *S*ystem	A logistics management system capable of determining new recipes based on test history.	Mountaintop, Pa.	1979	Data General Eclipse 330

and time consuming manual preparation of customer reports.

5. *Bipolar Wafer Fabrication*
This, the first system to use the SSTC PMC software, first went on line in 1979.
6. *ERIC*
This system includes Hewlett Packard 9825 computer/calculators for inputting data.

CAM benefits

A coordinated CAM program produces immediate results which lead to several important benefits:

- *Reports and summaries*: higher yields, better inventory control.
- *Lot tracking, reporting and control*: reduced cycle time, reduced inventory.
- *Downloading of test programs and process equipment recipes*: reduced operator errors, operation de-skilling.
- *Validation of input data*: improved data quality, correct lot movement, improved productivity.
- *Equipment monitoring and reporting*: reduced capital investment.
- *Test data collection and analysis*: detection of product performance trends.

The CAM of the future

The microprocessor is sparking a major evolutionary step in the kind of process equipment available for semiconductor manufacture by making it economically feasible to build-in new control and monitoring sophistication. Such equipment will provide "stand alone" capabilities permitting the user to program, in simple language, the process sequence and control he requires.

Microprocessor systems, as shown in Fig. 6, will also have a communication port to the outside world, i.e., to mini or small supervisory computers which in turn will communicate with a larger management computer. Thus, data "up and down" the factory floor will be available to all people of the management team. These machines, coupled with further complexities in manufacturing, will require a central CAM base system for overall management.

J.W. Gaylord

Process monitoring and control—a computer-based system for manufacturing

If you are in manufacturing and your product goes through the usual design, materials selection, processing, assembly, quality control and finishing steps, this documented paper on PMC may be what your are looking for.

An economically sound general purpose computer based system has been developed for the monitoring and control of the manufacturing process. This system can be programmed to track and control product flow, monitor and optimize processes, enforce the maintenance of manufacturing equipment, assist production scheduling, and report production problems and status.

It is a significant contribution to RCA's manufacturing capability because it is relatively easy to install and adapt to a variety of manufacturing operations.

The birth of process monitoring and control

In 1974, the RCA Laboratories, with the support of the Solid State Division, initiated the process monitoring and control (PMC) project to assist with this manufacturing task. A general computer based process control system for large scale integrated (LSI) circuit manufacturing was the goal. Emphasis was on process control to assure competitive manufacturing yields as the size and complexity of integrated circuits increased. It turned out that a prerequisite to process control was the knowledge of product location and its status. This led to the initial development of a logistical PMC system for tracking product.

In 1976 The Solid State Division formed a computer aided manufacturing (CAM) organization to pool SSD resources to more efficiently implement and maintain real time computer systems used in manufacturing. The CAM organization is essential to realizing the benefits of PMC. CAM takes basic systems developed by the PMC group, installs and maintains them at the manufacturing sites, and develops the unique application programs necessary for their use. An article in the *RCA Engineer* by J. Rudolph/S. Levy on the "Computer Aided Manufacturing" organization describes two applications of PMC in the Solid State Division.

Process control received greater Solid State Technology Center (SSTC) emphasis in 1978, with the completion of the logistics system and its transfer to SSD. Programs covering photolithographic processes and yield improvement are currently being executed with the objective of making LSI production in SSTC an extremely efficient, high yield operation. System standardization permits the transfer of this technology to SSD when its utility is proven.

What is PMC?

PMC is a real time minicomputer system, with appropriate communication peripherals, which gathers and stores, in a data base, event information usually associated with physically identifiable product. Computer programs are then invoked to use this data or results derived from it to help direct the manufacturing operation. A typical system configuration is shown in Fig. 1.

The video terminals used for information input are operated directly by the same personnel who do the production processing, assembly, or testing (Fig. 2). This provides the most accurate timely input to the system. Conversely communications to the operators doing their work is directly achieved through the same video terminals. This reduces communication time to those who ultimately control the process. The central computer (Fig. 3) has an overview of the entire manufacturing system and maintains storage of all data that is required to produce reports, maintain a

John Gaylord usually doesn't make pizzas using electron beam evaporated metals as pictured. He is more often found behind a cluttered desk managing the Process Monitoring and Control group of the Solid State Technology Center and the Computer Aided Manufacturing groups of the Solid State Division. Experience in power tube and solid state device design, manufacturing systems, a smattering of newly acquired computer systems technology, and a real interest in people and how they work together brings him his present assignment.

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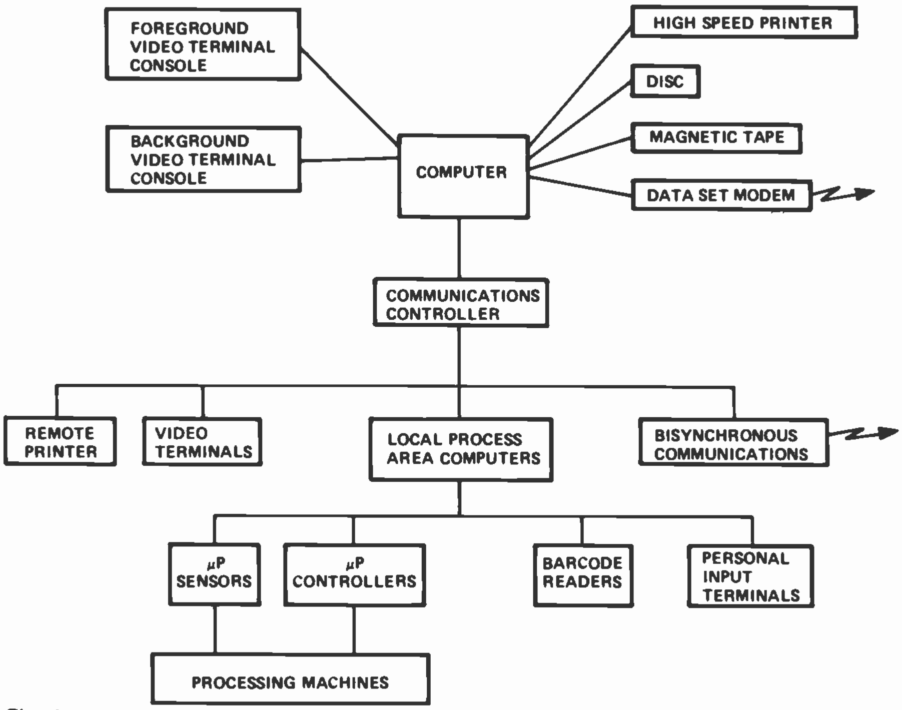

Fig. 1
The typical PMC system shows the many types of equipment used in gathering data from many different types of sources, communicating between locations, computing and analyzing data and producing reports in various ways.

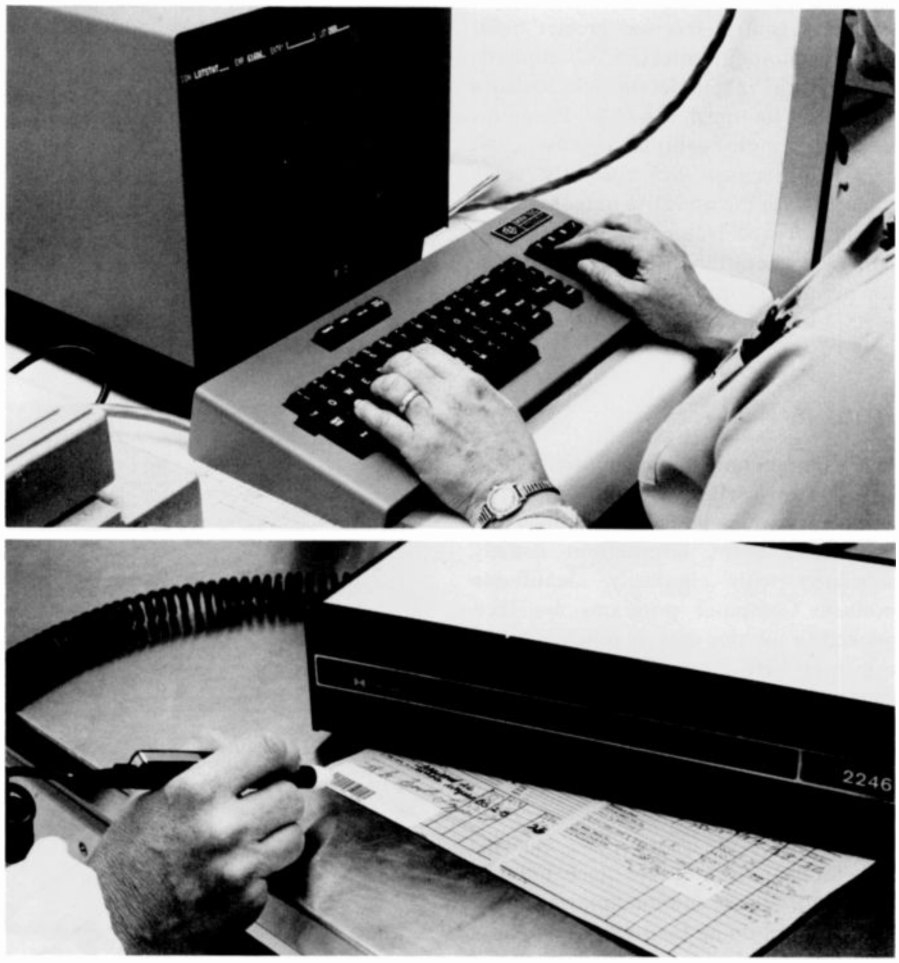

Fig. 2
The keyboard and barcode reader shown represent typical equipment used to enter logistical and measurement data in the PMC system.

history and optimize the interaction between process steps. This central computer communicates to an array of data input terminals, bar code readers, sensors, and controllers. These, in combination, form subsystems that can operate independently from the central computer to sense, measure, test against limits and store for analysis process related data. These subsystems also stop or start processes and detect alarm conditions. They are generally controlled by microprocessors grouped by logical process steps and dedicated to specific machines. In this configuration, local as well as global process control and optimization is achieved.

How does PMC work?

Imagine a production line composed of many serial process steps. As product moves from step to step, its position, as it enters and leaves each step, is known by PMC. Product flow can be controlled prior to each step and the results of processing can be measured after each step. PMC collects this information and, through application programs that are unique to each system site, uses the data to provide the functions shown in Fig. 4.

Results

Three PMC systems have been installed. The initial system used for continuing development is in the Solid State Technology Centers large scale integrated circuit production facility at Somerville, NJ. This system has monitored product logistics, and process parameters for over a year. Real time analysis by this system has provided insight into the relative magnitude and changing trends of process yields, processing time, and product deliveries.

A second system is located in the Solid State Division manufacturing plant at Findlay, OH. This Bipolar Integrated Circuit installation monitors product logistics, highlights the source of low yields, converts process measurements to physical parameters meaningful to production engineering personnel, maintains floor inventory, generates production reports, and provides the Divisional MIS community with direct data for monthly financial control.

The third system is in the epitaxial wafer production area at Mountain Top, PA. This system monitors measurements on wafers produced, calculates changes in the process used to make subsequent wafers to optimize yield, and maintains a status and history of the wafer production operation.

These systems are continually evolving and additional systems are planned for installation at these and other Solid State Division sites.

How much does a PMC system cost?

A minimum system for continuous on-line service is composed of an Eclipse computer with 128K words of memory, a 96 megabyte disc, line printer, magnetic tape station, two control consoles, and a communications chassis. The capital cost is approximately 100 thousand dollars plus 10 percent annually for maintenance. In addition, video terminals are required for communication with the production floor at a cost of about two thousand dollars each.

A second system is essential for backup and the inevitable continued development of application programs to enhance system usefulness.

The software for this system is furnished by SSTC. The user must provide or contract for personnel who can write application programs using the high level Fortran PMC language that tailors the basic PMC system to each specific site requirement. The PMC group provides training in this area but the application programmer should be experienced in Fortran programming.

Fig. 3
The PMC computer room contains the minicomputer used to control the system.

What is the return on this investment?

The PMC system provides real time tracking of orders and product. It will produce statistics related to product flow, cycle time, yields, reprocessing, scrap location and the reasons for scrap or reprocessing. It monitors process parameters, analyzes trends in control parameters, warns when processes and equipment are going out of control, and can adjust processes to optimize yield.

What this equates to in savings to offset the investment depends on the specific needs of each site. Generally savings have resulted from reduced human error, increased yield, and a reduction in labor required to report and control the operation. In the Solid State Division these savings are between 100 and 200 thousand dollars per year-system permitting capital write off at the end of one to two years of operation.

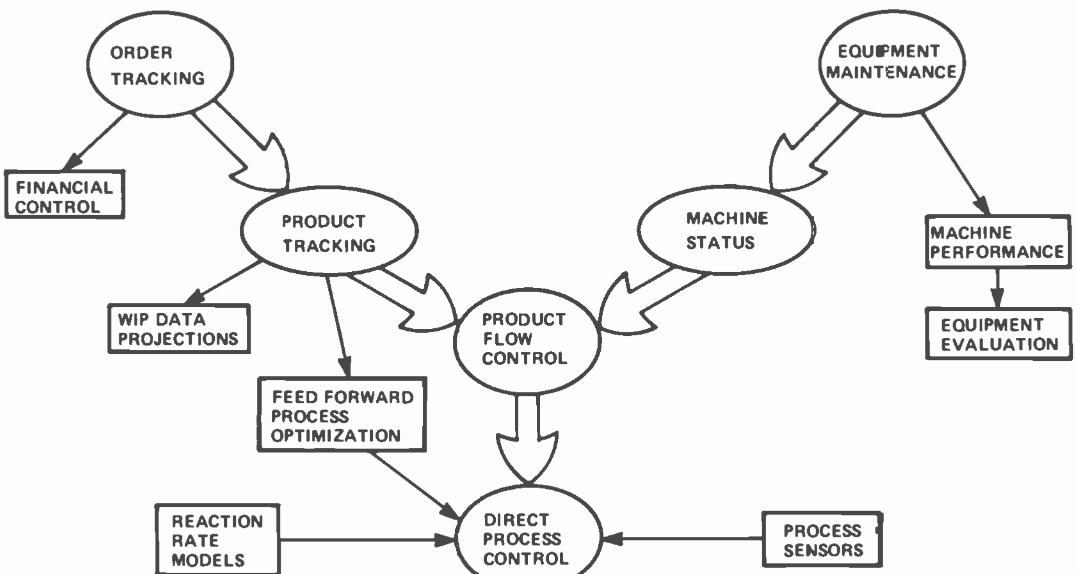

Fig. 4
The chronology of process control. The status of product being manufactured is known through functions depicted in the left arm of this Y. This leads to better management through timely informed decisions and fast accurate communications. The status of the production facility is known through functions depicted in the right arm of the Y. These two bodies of knowledge combine to permit the control of product flow and the processes used.

P.T. Valentine

Cycle time—a key measure of productivity

A product turnaround that is too fast can be just as bad as one that is too slow. Engineers must find the optimal time to cycle a product through its manufacturing steps and not stray far from it in either direction.

In manufacturing, cycle time is the number of working days a product takes to move through a series of processing steps to partial or full completion. Cycle time is a key factor in production and, because it affects a company's ability to deliver goods, is an important factor in marketing and sales.

Cycle time can be measured as follows:

Theoretical cycle time is measured through step-by-step process analysis and assumes a FIFO (first-in, first-out) product flow, no "banks" of product, and no queuing of work-in-process. Theoretically, as a unit or lot of units completes one process step, it immediately proceeds to the next step for further processing.

Actual cycle time is defined as the quotient of the month-end work-in-process inventory divided by the quotient of one-half the sum of product starts plus completions divided by the number of scheduled workdays.

Goal or target cycle time falls within a range of two to five times theoretical cycle time within the solid-state industry. The actual factor applied will depend upon the nature of the specific operation, operational experience, and more importantly on the priority and emphasis that management places on cycle time.

A summary of these measures is shown in Table I.

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How does cycle time affect cost and sales?

Organized management of cycle time can significantly affect product cost performance and a company's response to its customers. Any given manufacturing process has a desired or target range of cycle time within which both costs and customer responsiveness can be optimized. Beyond the limits of this range, either an increase or decrease in cycle time will increase product costs; shorter cycle time continues to improve response time to customer needs somewhat, but at increasing cost tradeoffs that are both unrealistic and noncompetitive. This phenomenon of cost versus cycle time can be illustrated as a somewhat "parabolic" curve, as shown in Fig. 1, whose dimensions are meant only to be descriptive and not to be measured literally.

Table I
Cycle time can be measured theoretically and actually. Optimal value is neither of these, but is in the range of 2-5 times theoretical value.

Three measures of cycle time

Theoretical
- FIFO
- No Banks
- No Queuing

Actual

$$\frac{\text{Ending Inventory}}{\left(\frac{1/2\,(\text{Starts} + \text{Sales})}{\text{Work Days}}\right)}$$

Industry Practice

2-5 x Theoretical

During 1977 a Solid State Division team* selected a group of factors key to the conduct of business and empirically and subjectively examined what effects cycle-time changes would have upon each of them. Cycle times were varied about the previously described optimal standard of performance employed within the solid-state industry. This effort was undertaken chiefly to provide increased and improved understanding of the cost/cycle-time phenomenon described earlier and to serve as a basis for further and more objective investigation.

The factors selected were:

- Customer response time
- Learning experience
- Yield
- Fixed-asset investment
- Direct-labor utilization
- Work-in-process inventory

What happens when cycle time is too high?

Figure 2 describes the effect that cycle time has on these selected factors, assuming the actual cycle time of production is greater than the optimal time and is cycling between "excess" and "optimal."

* Members of the team were B.A. Jacoby, J.J. Kollmar, M.H. Lewis, and the author.

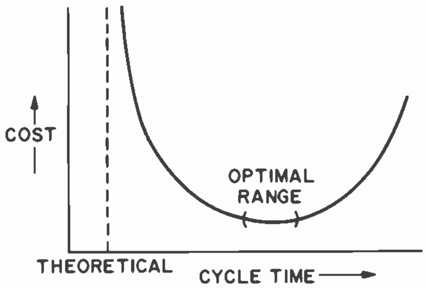


Fig. 1
Cycle-time/cost curve is "parabolic" in shape; desired range of operation is at bottom of curve. Decreasing cycle time too far to the left past optimal point will produce very fast customer response time, but at an unrealistic cost. (Curve is not quantitative.)

The rationale employed to support the effects shown in Fig. 2 follows:

Customer response time improves as cycle time decreases, since the line of communications between customers' orders and product manufacture is shortened, simplified, and more ordered. The noise level is low! As cycle time increases, customer response time worsens as the line becomes lengthened, more complex, and less ordered. The noise level is high!

The total-process learning experience frequency (encompassing labor, materials, and overhead) increases as cycle time decreases, providing a greater number of opportunities within a given period of time to complete, critique, and take corrective action to improve the total process, i.e., product performance and cost. As cycle time increases, the learning experiences per period decrease, thus slowing the rate at which product improvement and cost reduction occur.

Product yield is the percentage of parts that survives and meets the output standards of a process compared to the number of parts submitted to the process. As the opportunities for corrective action increase, as cycle time shortens, product yield should improve. As cycle time increases, such opportunities become less frequent and the percentage of scrap decreases more slowly.

Fixed-asset investment will tend to increase as cycle time moves from excess to optimal. This is desirable, since the focus is on keeping all units under active process. As cycle time moves from optimal to excess, it becomes less complicated to keep machinery or equipment loaded, since the pressure for continuous product movement is lessened and inventory grows, providing banks of product to keep equipment working at processing capacity.

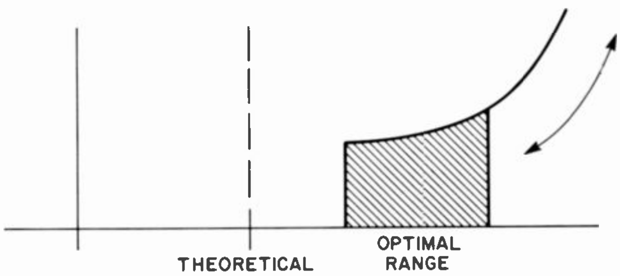
Direct-labor utilization or efficiency of performance will decrease as cycle time decreases from excess to optimal, since inventories in the process are reduced. Cross-training and improved operator mobility are required to offset this trend to increased waiting time for product. The backlog syndrome,[1] or subtle efforts on the part of the manufacturing labor force to maintain work-in-process inventories at a level of "employee security," also plays a role as output per man-hour tends to drop to prevent inventory reduction (a by-product of cycle-time reduction). Output per man-hour tends to rise as cycle time increases and "comfortable" levels of banked inventories are reached. At some point of further increased cycle time, labor efficiency drops rapidly to conform to the unbusinesslike atmosphere that has been generated.

Work-in-process inventories vary directly with cycle-time changes; the added expense of increasing inventories with increasing cycle time and the savings associated with decreased inventories as cycle time decreases directly affect financial performance. The backlog syndrome described earlier must also be considered as a factor in this area.

What happens when cycle time is too low?

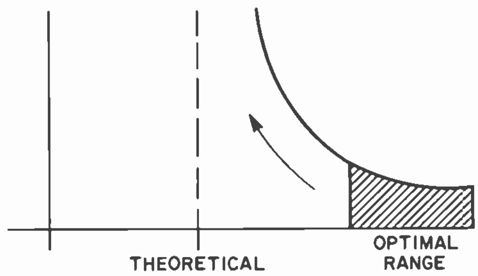
Figure 3 illustrates the effect cycle time has on the selected business factors as it moves from the optimal zone towards theoretical cycle time. The rationale to support Fig. 3 follows:

Responsiveness to the needs of the customer continues to improve as cycle time decreases beyond the optimal range, but at a slower rate. The level of responsiveness achieved eventually is faster



Factors	*As Cycle time decreases*	*As Cycle time increases*
Customer response time	Improves	Worsens
Learning experience	Increases	Decreases
Yield	Improves	*Worsens*
Fixed-asset investment	Increases	Decreases
Direct-labor utilization	Decreases	Increases/ decreases
Work-in-process inventory	Decreases	Increases

Fig. 2
Decreasing cycle time toward optimal value has these effects on business factors.



Factor	*As cycle time decreases*
Customer response	Improves at slower rate
Learning experience	Increases
Yield	Improves up to a point
Fixed-asset investment	Increases rapidly
Direct-labor utilization	Decreases
Work-in-process inventory	Decreases

Fig. 3
Decreasing cycle time ***past*** **optimal** value has these effects on business factors.

than the requirements of competition within the marketplace.

Learning experiences continue to increase, but as the number of opportunities to learn approaches the theoretical, meaningful reaction can not be managed. This is also true of *product yield* performance.

Fixed-asset investment increases rapidly, since decreasing cycle time means that no part in the process must wait for its next processing step. This situation can become economically impracticable and unmanageable, requiring excess floor space, energy, and equipment.

Direct-labor utilization, or operator efficiency, falls off rapidly, since, as in the case of fixed assets, the decreased cycle time begins to require that an operator be always available for processing parts. Since line momentum can not be balanced or matched easily to the constant movement of personnel required by very rapid cycle time, it is economically undesirable to permit the operation to reach this point.

Work-in-process inventory continues to decrease in direct relationship with cycle-time decreases, but at some point the unavailability of inventory begins to affect operational soundness.

Parker T. Valentine joined the Solid State Division 23 years ago. He has been Minuteman Project Manager, Plant Manager at Mountaintop, and Manager of Power Product Marketing. In his present assignment, Manager, Operations Support, he is responsible for Divisional Plant, Industrial, and Facilities engineering. He is chairman of the SSD Manufacturing Council.

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Conclusion

Cycle-time theory had been employed in varying degrees within the Solid State Division prior to its analysis in 1977; the management of cycle time is now recognized as a prime factor in the conduct of the business of the division. Consequently, management now reviews cycle-time performance versus goal for processes throughout the division, domestic and offshore, as a key measure of productivity on a monthly basis.

Reference

1. Earl R. Gomersall, "The backlog syndrome" (No. 64505), *Harvard Business Review*, (Sep-Oct 1964).

J. Kollmar

Labor analysis and productivity

A report on SSD's worldwide program to provide tools through which manufacturing supervision can optimize productivity.

Lord Kelvin once said, "When you can measure what you are speaking about and express it in numbers, you know something about it; but if you cannot, your knowledge is of a meager and unsatisfactory kind."

This thought applies to the approximately 7500 direct labor operators employed by the RCA Solid State Division (SSD) throughout the world. Their annual payroll, including associated expense, is approximately $39 million. With any payroll of this magnitude, a mere 1% shift in productivity causes a $400,000 shift in division profitability. It is, therefore, essential that manufacturing management obtain data to evaluate direct labor productivity, so that corrective action can be taken whenever performance is found to be unsatisfactory.

Establishing norms

Direct labor productivity can be measured in two ways. First, it is necessary to know how efficient each individual is while working toward an established goal or quota. Second, we must know how many hours each operator works on a prescribed process during the shift, and how many hours are lost due to downtime or time spent on nonstandard assignments. So-called "norms" are developed by the industrial engineers who establish production rates through procedures such as stopwatch time studies or work factor analyses. The production rates represent a mean, or the capability of an average operator, around which the performance of a group should cluster.

Absolute efficiency

The actual output of each individual operator is measured against the applicable norm in order to establish his or her productivity. The second step is accomplished by measuring all occurrences that keep an operator from actually performing the assigned operation. For example, if an operator is 100 percent productive during the first four hours of a work shift, but did not work during the second four hours, the overall productivity is 50 percent for that shift. This measure, known as Absolute Efficiency, is most important because it relates labor hours paid to labor hours earned as measured by units processed. Most people are motivated by the performance goals that have been established for their assignments and require only occasional follow up by supervision, but occurrences of downtime and other nonproductive job interruptions require constant attention by management.

Computer-based system

Because of the importance of knowing the status of the performance measures discussed above, it was determined that a computer-based Labor Analysis system would be installed in all the SSD locations. This system, which had been developed and used in the Mountaintop plant, has replaced the various manual and semi-automatic systems that had been used by individual plants. The computer based labor analysis systems have the division-wide capability to uniformly and rapidly provide each level of management with the information that is required to properly utilize the direct labor work force.

The input document for the system is a labor analysis card (Fig. 1) which is filled out by each operator, then reviewed and approved by the supervisor. The data includes the operation code, amount of work produced, time spent on the job, applicable downtime, or nonproductive time, code, and the time for each occurrence. The program compares and evaluates the inputted data with the production rates and other parameters of acceptable performance which are resident on tape or discs and provides a number of reports for management.

Jim Kollmar, Manager of Division Industrial Engineering, is responsible for setting, and giving direction on, policies and procedures for the location Industrial Engineering Departments, as well as for providing uniform controls in such areas as Direct Labor Productivity and Cycle Time construction. He has also worked as Manager of IC Administration as well as in various industrial engineering positions in Somerville since joining RCA in 1962.

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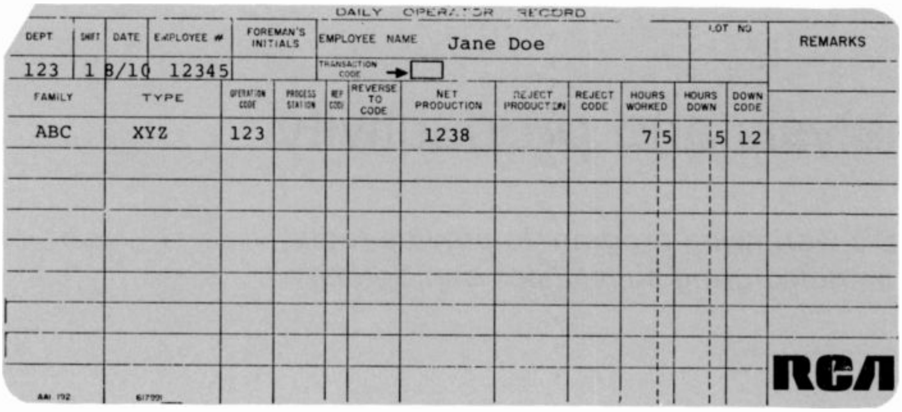

Fig. 1
The labor analysis card is filled in by the operator and indicates product family and type worked on, amount of production, hours worked, and hours down. This is the input data for the Labor Analysis system.

Table I
Supervisor's report gives each operator's output and downtime, also summarizes the shift for the foreman. The data is flexible, in that downtime information is categorized according to the needs of the location.

DAILY OPERATOR EFFICIENCY AND SUMMARY REPORT SAMPLE DATE 07/06/78

DEPT 123.4 SHIFT 3 %EFFICIENCY MIN 75 MAX 150

EMPLOYEE CLOCK	NAME	OPER CODE	GROSS PRODUCT	WORKED TIME	DOWN/TIME HRS	CODE	TOTAL HOURS	STD OPR RATE/HR	% EFF	NOTICES		
03327	C. Brown	662E	65	1.0			1.0	70.00	93			
	ie. (operator CB)	664E	97	5.5			5.5	17.20	103			
			162	6.5			6.5		100			
03674	B. Green				1.3	01	1.3					
		300E	2173	4.8			4.8	454.00	100			
		345E	21	.3			.3	65.00	108			
			2194	5.1	1.3		6.4		100			
03899	D. Gold	870E	66	1.0			1.0	66.00	100			
		871E	270	4.5			4.5	60.00	100			
		872E	45	1.0			1.0	45.00	100			
			381	6.5			6.5		100			
04159	N. Whyte	269E	1060	5.5	1.0	01	6.5	194.00	99			
	•		1060	5.5	1.0		6.5		100			
	•		•	•	•		•	•	•			
	•		•	•	•		•	•	•			
	•		•	•	•		•	•	•			
	•		•	•	•		•	•	•	EARNED HOURS	ABS EFF	MEAS TIME
EMPLOYEE COUNT 28												
TOTALS:			23753	162.0	18.6		180.		94	119.6	66	126.9

DOWN TIME CODE	DESCRIPTION	COUNT	HOURS
001	LACK OF MATERIALS	12	17.0
002	MACHINE DOWNTIME	5	1.4
004	INSTRUCTION	1	.2
	TOTALS	18	18.6

NON-STANDARD CODE	DESCRIPTION		COUNT	HOURS
023	INVENTORY	923	4	2.0
024	TRAINING	924	2	11.0
027	STAGING	927	1	1.0
032	CLERICAL	932	2	.5
033	DL OPEN SYS IN	933	1	.5
038	NOT YET RATED	938	1	2.8
053	START UP CLN UP	953	1	.3
	TOTALS		12	18.1

1. The First Line Supervisor (Table I)

This report compares the performance of each operator with the established production rate for his or her job assignment and displays the resultant labor efficiency. The report also 1) develops the composite labor efficiency for each cost center and shift, 2) summarizes all categories of nonproductive time by shift, and 3) establishes the absolute efficiency by combining the two previous items.

2. The Superintendent Level (Table II)

This report presents 1) the composite labor efficiency for all shifts of a cost center, 2) a summation of all nonproductive time for the same shifts, and 3) the resultant absolute efficiency for the cost center. The superintendent will periodically review the details shown on the report designed for the first line supervisor.

3. The Plant Manager Level (Table III)

The report summarizes performance data for the cost center reporting to each superintendent and product line manager. It identifies the labor efficiency for the reporting period and the average efficiencies for the reporting period and for the last four weeks. It also shows the percentage of several types of nonproductive time and the absolute efficiency for each of the cost centers.

> **Editor's note:** Tables I-V are taken from actual computer printouts, but have been shortened for readability. In some cases, names and sensitive information have been changed.

Table II
Superintendent-level report presents the composite labor efficiency, nonproductive time, and absolute efficiency for all shifts of a cost center.

DEPT 345.6 — DAILY OPERATOR EFFICIENCY AND SUMMARY REPORT — SAMPLE DATE 07/06/78

	GROSS PRODUCT	WORKED TIME	DOWN TIME HRS/CODE	TOTAL HOURS	% EFF	EARNED HOURS	ABS EFF	MEAS TIME
EMPLOYEE COUNT 25	53143	187.1	1.1	188.2	91	144.1	77	159.1

DOWN TIME CODE DESCRIPTION		COUNT	HOURS
002 MACHINE DOWNTIME		1	1.1
TOTALS		1	1.1

NON-STANDARD CODE DESCRIPTION		COUNT	HOURS
017 N-S MONITOR 1	917	1	4.3
024 TRAINING	924	1	8.0
033 DL OPEN SYS IN	933	1	1.2
053 START UP CLN OP	953	6	2.0
054 CHANGEOVER	954	1	.3
055 NON STANDARD	955	4	7.3
056 LOAD & UNLD FCE	956	4	3.7
TOTALS		18	26.8

Table III
Plant manager's report has information from cost centers reporting to each superintendent. It includes plant totals for labor efficiency, downtime, absolute efficiency, and four-week running averages.

100 % SAMPLE WEEKLY LABOR ANALYSIS—SUMMARY BY MANAGER — WEEK ENDING 07/06/78 PAGE 1

PRODUCT LINES	DL COVERED	%	HOURS REPORTED	PROD HOURS	EARNED HOURS	% EFF	LAST 4 WEEK %	TOTAL % EFF	NON STD%	NON MEAS%	MTL HDLG%	DOWN TIME%	ABS EFF
J. Doe CM PRO	26	91	180.5	170.5	70.0	41	46	41				1	41
J. Deer FIN TS	2	100	16.0	13.0	11.0	85	80	85	19				69
	28	92	196.5	183.5	81.0	44	48	44	2			1	43
J. Brown	53	98	415.1	267.0	221.0	83	81	83	23	2		1	62
J. Cork PHOTO	18	74	106.1	56.2	72.0	128	121	128	47				68
J. Cork DIFF	71	92	521.2	323.2	293.0	91	88	91	28	2			63
O. Fawn PHOTO	108	97	784.9	496.9	483.5	97	94	97	14	2		15	67
P. Buck DIFF	58	53	229.0	168.1	149.0	89	89	89	10	2		15	65
	166	81	1013.9	665.0	632.5	95	92	95	13	2		15	67
F. Deer HR TEST	28	88	188.2	159.1	144.1	91	105	91	14	1		1	77
F. Deer CM BRN	8	38	24.0	8.0	6.0	75	37	75	67				25
F. Deer HR BRN	14	113	126.2	40.0	38.5	96	98	96	67				32
F. Deer MECH SN	7	57	32.0	28.9	28.9	100	93	100	10				90
F. Deer LIN BRN	9												
Y. Doe ASY A	14						83						
Y. Doe ASY B	14						84						
B. Amy LIN A+B	4						91						
B. Amy PLT INSP	17	88	120.3	113.7	69.4	61	59	61	3	2			58
B. Amy BOND PBI	57	92	420.2	323.8	274.9	85	83	85	17			2	69
	172	67	910.9	673.5	561.8	83	80	83	22			1	64
H. Frank	437	78	2642.5	1845.2	1568.3	85	83	85	18	1		6	63

Table IV
This report is a summary of those areas serviced by a particular industrial engineer and is an indication of areas that may need work.

M26304 100 % SAMPLE WEEKLY LABOR ANALYSIS — I E SUMMARY WEEK ENDING 07/06/78 Page 1

PRODUCT LINES	DL COVERED		%	HOURS REPORTED	PROD HOURS	EARNED HOURS	% EFF	LAST 4 WEEK %	TOTAL % EFF	NON STD%	NON MEAS%	MTL HDLG%	DOWN TIME%	ABS EFF
A. Brown	RWA	53	98	415.1	267.0	221.0	83	31	63	23	2		1	62
B. Craft	RWB	18	74	106.1	56.2	72.0	128	121	128	47				68
D. Drew	RWC	28	88	188.2	159.1	144.1	91	105	91	14	1		1	77
L. Green	RWD	7	57	32.0	28.9	28.9	100	93	100	10				90
A. Jones	RWE	14	113	126.2	40.0	38.5	96	96	96	67				32
M. Long	RWF	14						83						
M. Moore	RWG	14						84						
J. Peters	PWH	4						91						
R. Ross	RWI	17	88	120.3	113.7	69.4	61	59	61	3	2			58
J. Stewart	RWJ	57	92	420.2	323.8	274.9	85	83	85	17			2	69
L. Thomas	RWK	9												
J. Victor	RWL	8	38	24.0	8.0	6.0	75	37	75	67				25
A. Wills	RWM	26	91	180.5	170.5	70.6	41	45	41				1	41
S. Young	RWN	2	100	16.0	13.0	11.0	85	80	85	19				69
J. Forrest	RWO	108	97	784.9	496.9	483.5	97	94	97	14	2		15	67
H. Hill	RWP	58	53	229.0	168.1	149.0	89	89	89	10	2		15	65
		437	78	2642.5	1845.2	1568.3	85	83	85	18	1		6	63

Table V
This report gives a summary of efficiencies and nonproductive time by code. It points out areas where attention may be needed.

M26305 100 % SAMPLE WEEKLY LABOR ANALYSIS—SUMMARY BY CODE SAMPLE DATE 07/06/78 Page 65

PLANT TOTALS

NON MEASURED

CODE	DESCRIPTION		THIS WEEK COUNT	THIS WEEK HOURS	LAST 4 WEEKS COUNT	LAST 4 WEEKS HOURS
OTH	NON MEAS IN MSTR					
999	NON MEAS BY EMP					
	TOTALS					

OTHER

CODE	DESCRIPTION	THIS WEEK COUNT	THIS WEEK HOURS	LAST 4 WEEKS COUNT	LAST 4 WEEKS HOURS
	TOTALS				

ABSENTEEISM

CODE	DESCRIPTION		THIS WEEK COUNT	THIS WEEK HOURS	LAST 4 WEEKS COUNT	LAST 4 WEEKS HOURS
012	LATE	967	2	3.0	2	3.3
013	ABSENT	968	9	62.3	13	90.2
014	VACATION	969	10	80.0	2	22.0
015	LOA	970	5	16.0	7	58.8
	TOTALS		26	161.3	26	174.4

NOTICES

CODE	DESCRIPTION	THIS WEEK COUNT	THIS WEEK HOURS	LAST 4 WEEKS COUNT	LAST 4 WEEKS HOURS
002	SHIFT NO INVALID	1	8.0	8	27.2
003	NO NAME AVAILABLE	10	43.9	11	47.0
005	OPER CODE OMITTED	7	12.1	3	3.6
007	DT CODE IMPROPER	10	13.4	7	9.4
010	NOT IN RATE FILE	12	28.1	16	38.4
011	GROSS COUNT OMITTED	7	20.5	4	7.7
012	HOURS OMITTED	6		4	
019	EXCESSIVE EFF	4	26.0	11	23.1
	TOTALS	57	152.0	67	156.7

HRS & ABSOLUTE EFF

CODE	DESCRIPTION	THIS WEEK COUNT	THIS WEEK HOURS	LAST 4 WEEKS COUNT	LAST 4 WEEKS HOURS
	EARNED HOURS		1568.3		1782.7
	TOTAL HOURS		2521.8		2919.5
	MEASURED TIME		1845.2		2154.1
	ABSOLUTE EFF		62.0		61.0

4. Miscellaneous

The system has the capability for generating a number of other reports, such as the industrial engineering report, Table IV, and the summary by code, Table V. The former is similar to the plant manager's report but lists the areas by their responsible industrial engineers; the latter shows the efficiencies being achieved on each productive operation and the non-productive occurrences for the present period and the last four weeks.

Summary

A review of the reports shows that much data that could otherwise be overlooked or ignored can be summarized, analyzed, and interpreted to determine the correct action that should be undertaken by manufacturing management. Although other factors of productivity must be addressed in manufacturing, the control and intelligent maximization of the output of the Solid State Division's direct labor workforce is of prime importance.

W.J. Greig | P.J. Moneika | R.A. Brown

Multichip packaging for high density and high reliability

New packaging approach increases hybrid circuit yields and densities.

In the manufacture of multichip packages and the subsequent assembly of high-density hybrid microcircuits, the substrate or package manufacturing process combines conventional electroplating with new thin film technology to produce bi-level multichip circuitry. The process is well established, readily monitored and controlled, and adaptable to high volume manufacture.

A high density, multi-level wiring capability on the substrate is attained by employing a "microbridge crossover" technique developed by Bell Laboratories.[1]

The first level conductor is a tri-metal system consisting of titanium, palladium and gold. The second level—the microbridge crossover—is electroformed gold. Addition of an organic layer directly over the first level metallization functions as an insulator and offers mechanical protection while contributing significantly to both yield and reliability.[2] Furthermore, the use of beam lead devices in conjunction with this thin film interconnect technology enhances the reliability and practicability of this high density multichip packaging approach.

Advantages to be realized with the beam leads are as follows:

- *Improved reliability because of immediate reduction by one half in the number of bonding interfaces.*
- *Optimum metallurgical integrity at all bond interfaces.* All bonds are gold to gold.
- *Decreased bond area requirement enhancing high density component capability.* Beam lead chips require an area only 10 x 10 mils larger than the chip size. Additionally, the "bugging" feature of the chip is compatible with designs in which conductor stripes pass under the chip.
- *Repairability.* Beam leads are completely

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amenable to chip removal, site repair and chip replacement.

- *Non-hermetic packaging.* The combination of beam lead sealed junction devices and an equally thin film interconnect permits the use of a non-hermetic packaging scheme that not only reduces size and weight, but also allows for hybrid repair all the way through the next level of interconnect.

Microbridge substrate manufacturing

The fabrication of microbridge substrates employs procedures commonly used in the manufacture of more complex integrated circuits. Large ceramic cards (3¾inches x 4½ inches) are processed permitting multiple substrates to be generated per card. The cards, typically 12 to a lot, are batch processed through all operations. Upon completion individual substrates are separated by laser scribing.

Four mask levels are required for fabrication. The masks are 5 inches x 7 inches, iron oxide type. Iron oxide is used to minimize damage and for the "see-through" capability. Since the large size ceramic cards present a relatively rough surface as well as camber problems, patterns are exposed with the mask raised above the photoresist coated cards by approximately 2 - 3 mils. All photoresist is applied by spraying. A negative resist is used for the first layer, while positive resist is used for the remaining three layers.

The basic steps in the process are as follows:

1. Titanium and palladium are sputtered onto the ceramic card.
2. Photoresist is applied and the desired conductor pattern is defined in the resist.
3. Using the resist as a plating mask, gold is selectively plated to define the conductor pattern.
4. The resist is stripped and the palladium and titanium are etched using the gold as the etch mask (Fig. 1). For single level substrates, the ceramic cards are now laser scribed and separated. However, for multi-level packages, fabrication of the microbridge substrates begins at this point.
5. Following base conductor fabrication, the insulating material, polyimide, is applied, defined, and cured over the base metallization. This is done in all areas except where contact with the base conductor is required, such as in pillar areas, chip bonding sites, and lead attach terminations (Fig. 2).
6. The entire circuit card is covered by an applied copper "spacer" about 0.001 inch thick. This layer serves as a conductor for electroplating the microbridges.
7. Photoresist is applied and the pillars defined.
8. Using the resist as an etch mask the copper is etched in the pillar area to expose the base conductor.
9. The microbridge crossover pattern is defined in photoresist and, using the resist as a mask, gold is electroplated to form the microbridge crossover. The thickness is typically 0.001 inch. (See Fig. 3)
10. Following stripping of the resist, the copper is etched away leaving a void beneath the crossover and insulator-protected base conductor. An SEM (scanning electron microscope) image of a microbridge crossover is presented in Fig. 4.

Processing is complete at this point and individual circuits are separated using laser scribing.

Following separation a rigid final visual inspection is performed. Each substrate, and in particular the microbridge crossovers, are subjected to a "tape-test" to verify mechanical strength and continuity. This, combined with an electrical test of each substrate (wherein a sample of the microbridge/conductor isolation points is tested), provides assurance of the microbridge crossover integrity.

The substrates proceed from this point into the substrate assembly area for lead attachment. A substrate with a lead attached is shown in Fig. 5. The leads, which are nickel and gold-plated copper, are thermocompression bonded to the thin film metallization, providing a monometallic interface. Should a hermetic package be desired, attachment of the lead frame would be omitted.

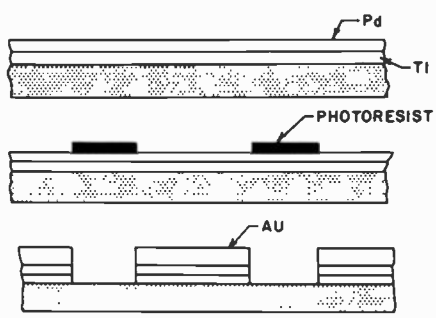

Fig. 1
Cross section showing stripping of the resist and the etching of the palladium and titanium using the gold as the etch mask.

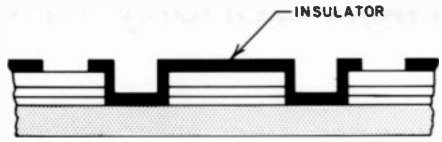

Fig. 2
Insulating material, polyimide, defined and cured over the base metallization in all areas except where contact with the base conductor is required.

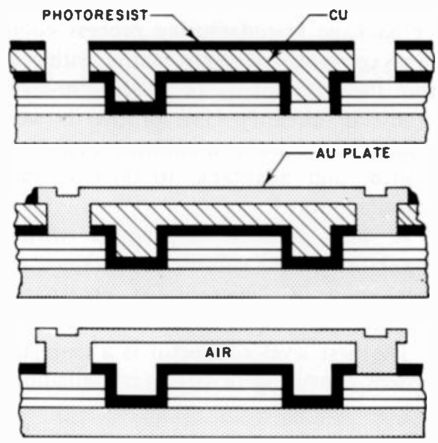

Fig. 3
Microbridge crossover pattern defined in photoresist, electroplating of gold to form microbridge crossover, and etching away of the copper to leave a void beneath the microbridge.

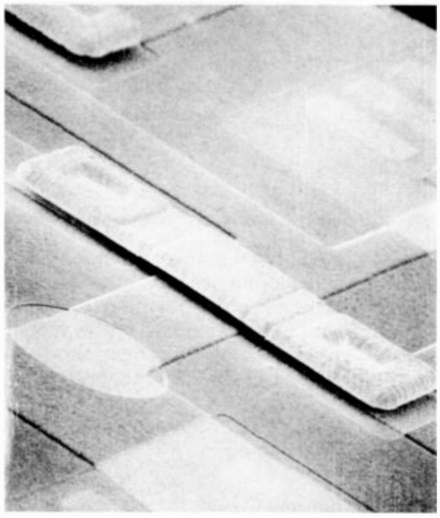

Fig. 4
A scanning electron microscope photograph of a microbridge crossover.

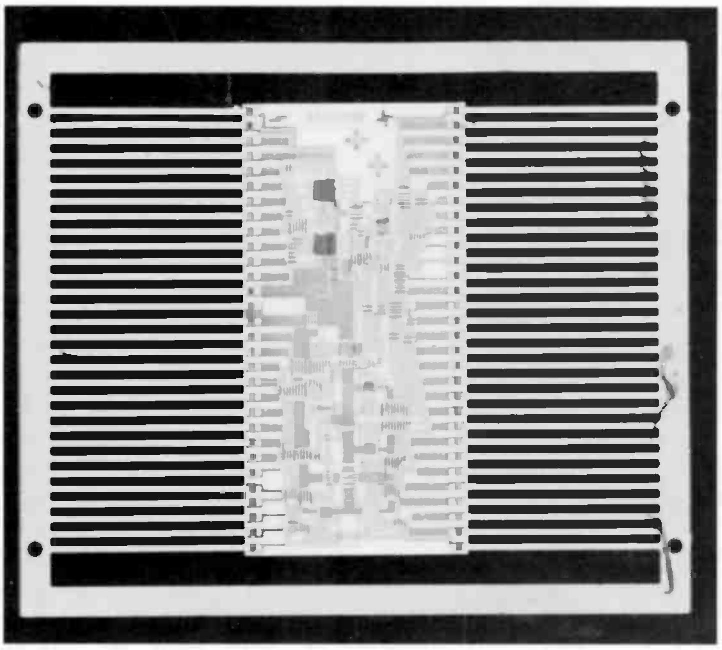

Fig. 5
Lead-frame bonded microbridge substrate.

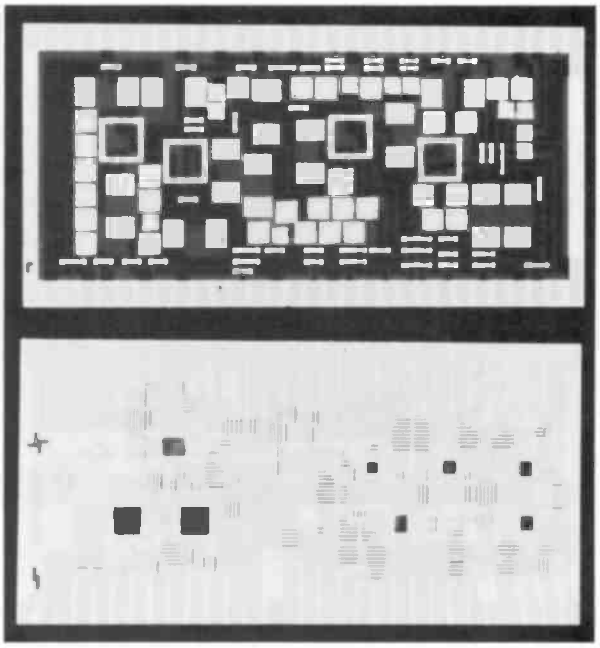

Fig. 6
Location of the polyimide layer is optional. It may be applied over all areas except where bonds are to be made or only under the bridges.

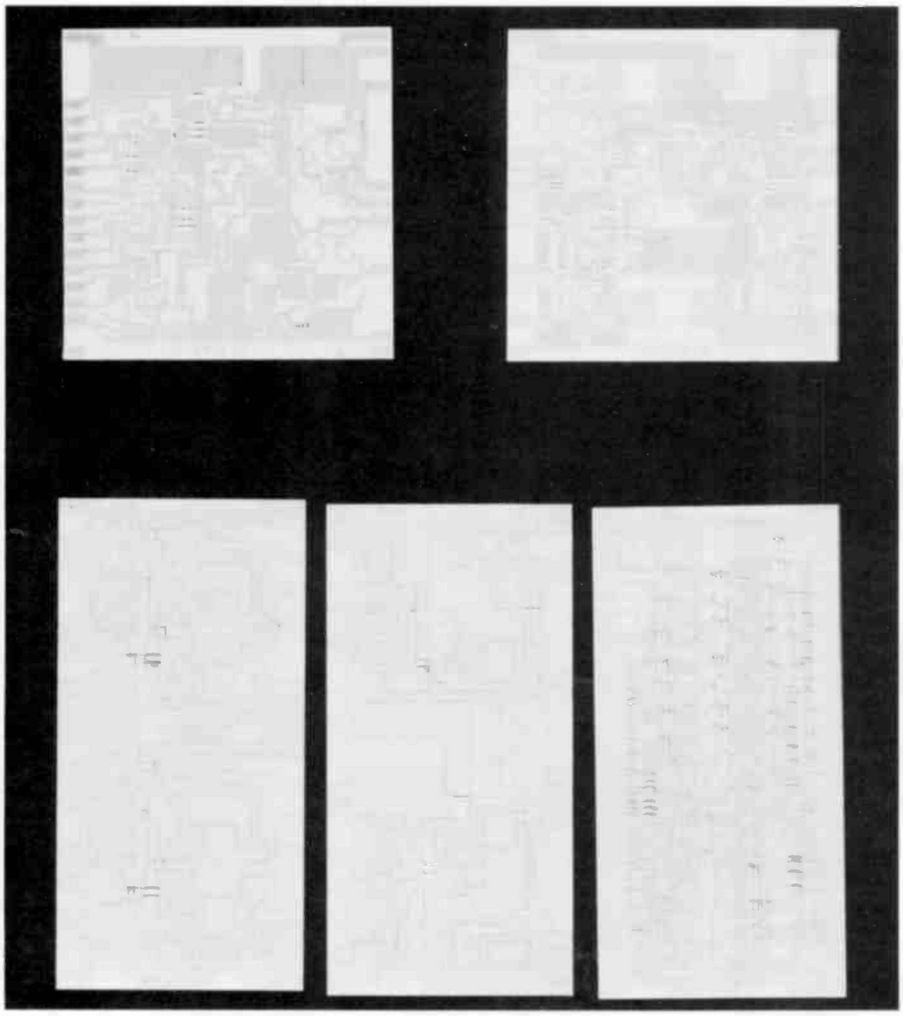

Fig. 7
Several substrates with the polyimide removed.

Polyimide contributions to yield

The use of polyimide which was originally intended to function only as an insulator has been found to contribute significantly to substrate yield. Prior to its use, processing anomalies were experienced which affected yield. However, with the polyimide in place the critical areas on the base conductor patterns, such as under the bridges, are now protected and no longer contribute to such yield variations.

The actual location of the polyimide layer is optional. The decision for the most part will usually be determined by the circuit layout designer and/or the method used for artwork generation. The polyimide can either be applied over all areas except where bonds are to be made, or only under the bridges (see Fig. 6).

The polyimide can be removed, if necessary, while the substrates are still in card form, prior to hybrid assembly, or upon completion of hybrid assembly before encapsulation or sealing. Figure 7 shows several substrates with the polyimide removed. The figure also illustrates the various complexities of the circuits fabricated. Figure 8 is a closeup view of a complex circuit with a high density of wiring and microbridges. Note that the density of microbridges results from either a desire for redundancy or to build up conductivity.

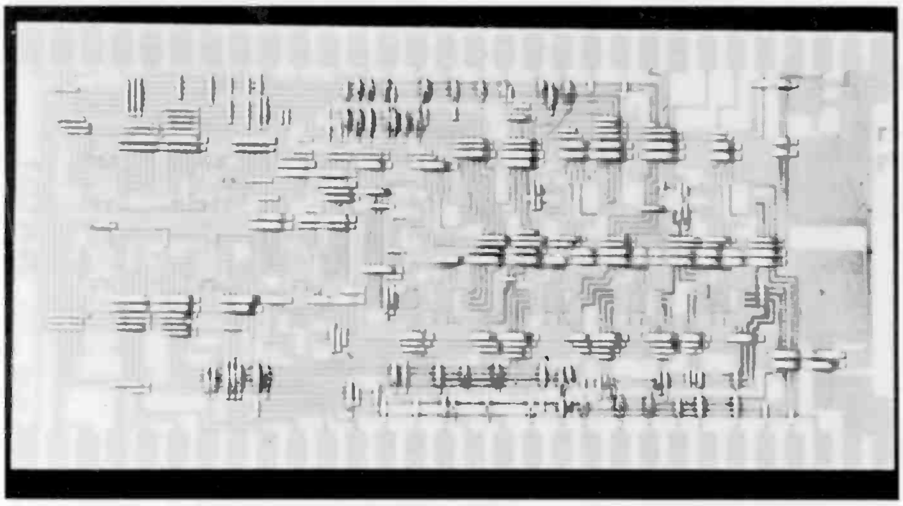

Fig. 8
A complex circuit with a high density of wiring and microbridges.

Table I
Hybrid circuit component density
(Substrate size ¾-inch x 1½-inch).

Number of hybrid circuit types	25
Average number of components	40
Minimum/maximum	12/81
Average number of actives	17
Average number of resistors	23
Average number of capacitors	4

Multichip hybrid assembly

In this particular case, all components were beam leaded and consisted of integrated circuits (up to 36 beams), transistors and diodes, tantalum nitride resistors on silicon (16 beams), and brick capacitors with gold plated copper tabs. All components were thermocompression bonded producing highly reliable gold-to-gold bonds. During assembly, a sequence was established to minimize the thermal exposure time of those components which are temperature sensitive. The components were bonded in the following sequence:

Transistors and Diodes
Integrated Circuits
Resistors
Capacitors

Minor variations in this order are possible as long as the most temperature-sensitive components are assembled last.

After all components are attached the hybrid is subjected to a rigorous visual inspection at typically 30 - 60 X magnification. Each component is carefully checked for proper bonding, chip "bugging", misalignment, or damage to the substrate as a result of assembly. A hybrid circuit carrier, as shown in Fig. 9, is used to facilitate subsequent electrical testing and to function as a handling device for encapsulation, temperature cycling, and retesting. Figure 10 shows both the carrier and the contactor used in electrical testing.

The organic coating, which has been in place throughout both the microbridge process and the component assembly, may now be removed, if desired. The method will depend upon the type of devices on the hybrid, but several different procedures are available. After stripping, the hybrid is subjected to cleaning, followed by encapsulation and final test. The hybrid is now complete. Figures 11 and 12 show typical hybrid circuits of varying component density. In both cases the organic protective layer is still in place.

Table I describes average component densities for a group of 25 different hybrids using this technology.

Repairability

In this hybrid approach, involving large numbers of chips per package, it is essential that a repair capability exist which is practical and can be accomplished without compromising reliability. Such is the case in this instance. Because of the nature of the bond between gold beam and gold conductor the chip can be easily removed. The chip bonding site can be repaired by scraping the bond pads to provide a more

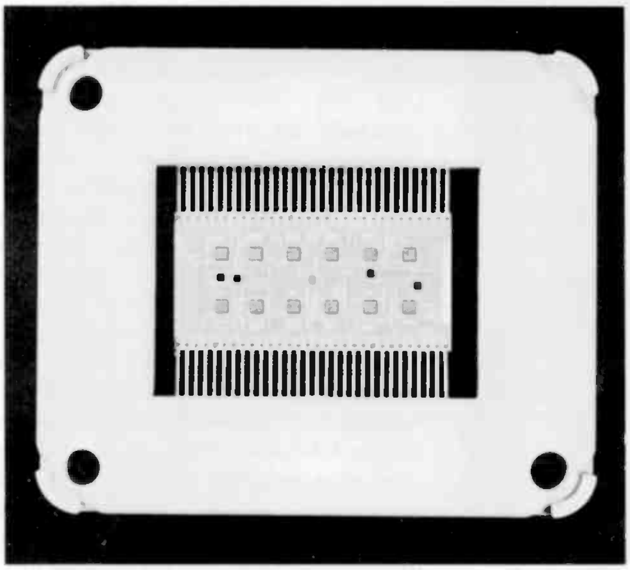

Fig. 9
A hybrid circuit carrier.

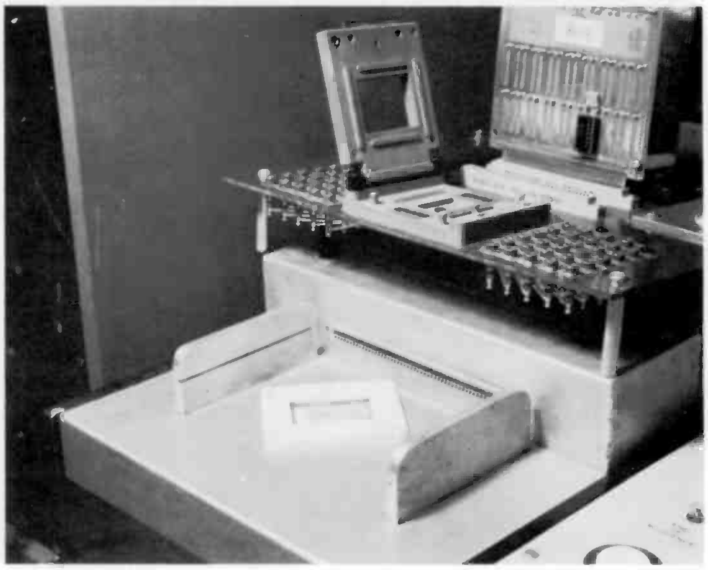

Fig. 10
Carrier and contactor used in electrical testing.

uniform rebonding site. The entire procedure is readily accomplished because gold is the only metal present.

Hybrid assembly/test yields

The value of this repair capability is best demonstrated by the following yield experienced on a production run of 175 hybrids consisting of 15 different hybrid types involving approximately 4000 beam lead devices. The actual mix of devices was as follows:

Transistors and diodes	897
Resistors	1211
Integrated circuits	1862

Visual inspection of each hybrid resulted in a 0.8% chip replacement for bonding defects. After electrical test, it was necessary to replace approximately 4% of the 4000 chips. Since all hybrids were of the non-hermetic type, units were subjected to a rigorous cleaning prior to the application of a flow coatable RTV (room temperature vulcanization) encapsulant. After encapsulation the hybrids were subjected to temperature tests and final electrical testing, where further failures resulted in the replacement of 0.15% of the chips. Nevertheless all following repaired hybrids survived without a single hybrid being scrapped.

Analysis of chip/hybrid failures

Although there was no loss of hybrids, the amount of re-work was considered to be excessive. Analysis of all the data highlights the difficulties and solutions.

The chip replacement rates were:

Pre-test visual	0.8%
Pre-cap electrical	4.0%
Final electrical	0.15%

The corresponding hybrid yields were:

Pre-cap electrical	67.0%
Final electrical	97.5%

The analysis indicated that in some cases improvement could be realized simply by changing procedures or modifying specifications. Some of the problems were supplier oriented. Others were the result of operator errors.

In order to analyze the electrical failures it was necessary to segregate the rejects by device type. Segregation of IC's by type further highlighted the problems. However, whatever the cause for the failures, it was readily apparent that a pre-assembly chip electrical test would be desirable and could have a dramatic effect on hybrid circuit yields. Further, if it was possible to subject the chips to electrical "burn-in", additional problem chips could be removed from the system.

Beam lead pre-testing by chip carriers

Pre-testing of beam lead chips using a chip carrier has been reported previously.[3] A carrier presently in use follows a flatpack carrier form factor. The carrier is shown in

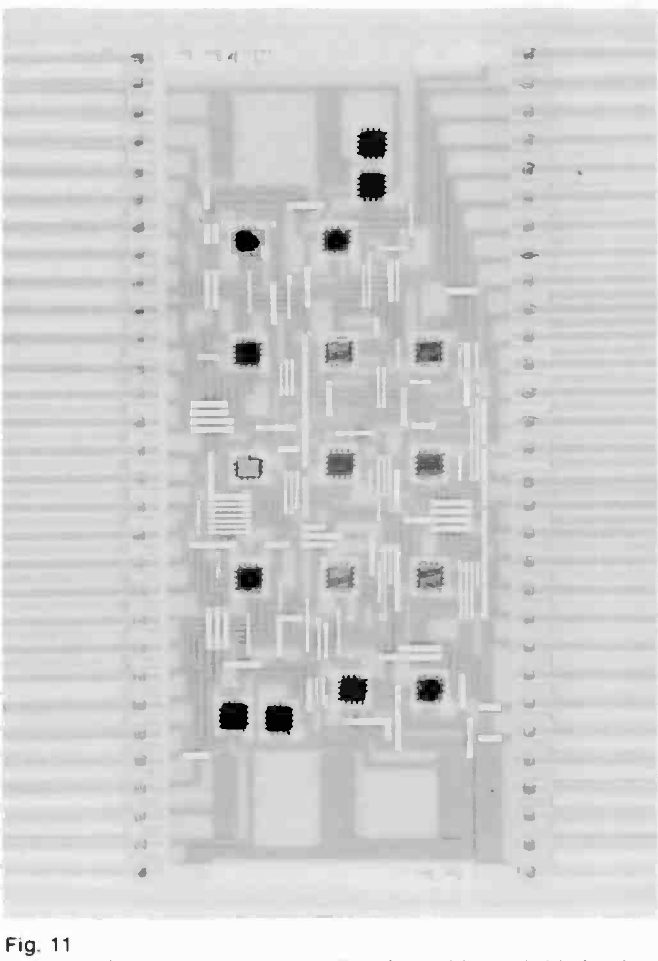

Fig. 11
Assembled low-component-density microbridge hybrid circuit.

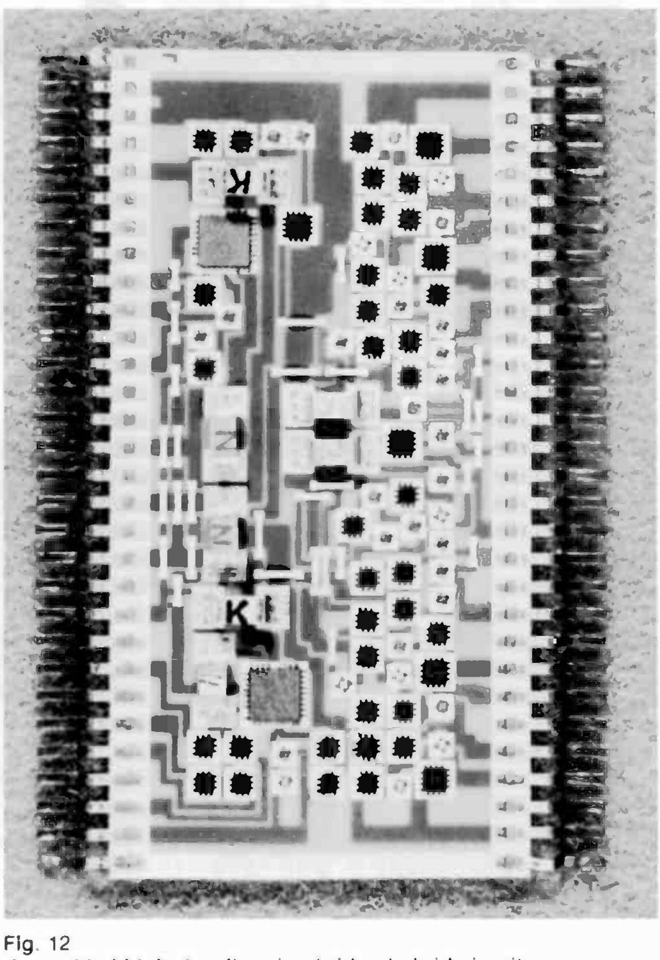

Fig. 12
Assembled high-density microbridge hybrid circuit.

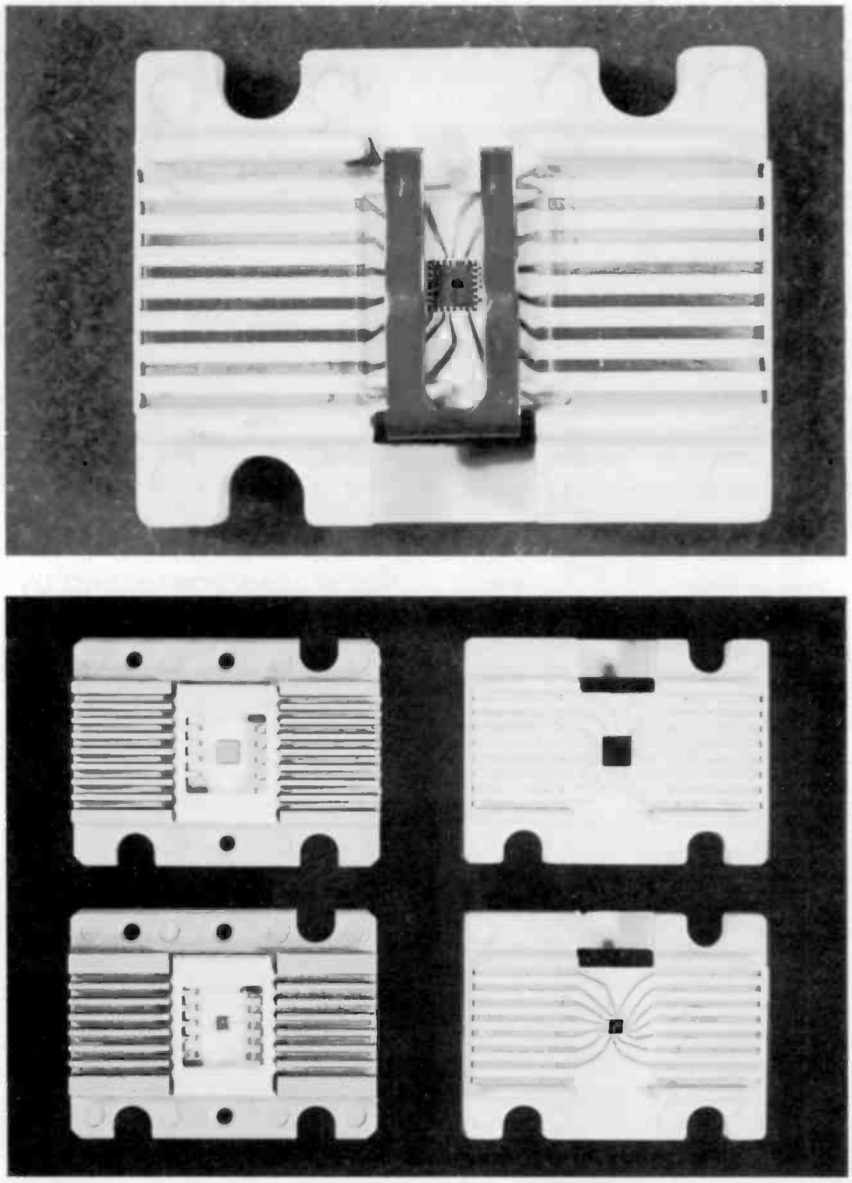

Fig. 13. This carrier permits beam lead chips to be electrically tested and put through a "burn-in" cycle. This capability must therefore be considered a dominant factor if any high density multichip packaging approach is to be successful. Hybrid circuits similar to the types discussed have been assembled with chips pretested in carriers. The increase in yield has been significant.

Fig. 13
Beam-lead chip and flatpack carriers.

A solution for beam lead deficiencies

While beam leads contribute significantly to this high reliability, high density packaging approach, they do have some disadvantages. For example, beam lead devices must be bonded face down, which presents problems in heat sinking. Power devices, therefore, must be attached and/or interconnected by some other means. With regard to resistor chips, the fact that they are bonded face down prevents them from being laser trimmed.

The solution to these difficulties may lie with the beam tape approach,[4] which allows for face up bonding so that power chips can be heat sinked and resistor chips laser trimmed. Also, the beam tape has its own built-in test carrier permitting pretesting with minimum handling. A multichip package with beam tape bonded chips is shown in Fig. 14. The thin film conductors once again provide an ideal surface for thermocompression bonding of the beam tape. The increased bond area required for attachment can be offset to some degree by utilizing the thin film microbridge technology more fully, that is, using both sides of the ceramic, and finer lines and spaces.

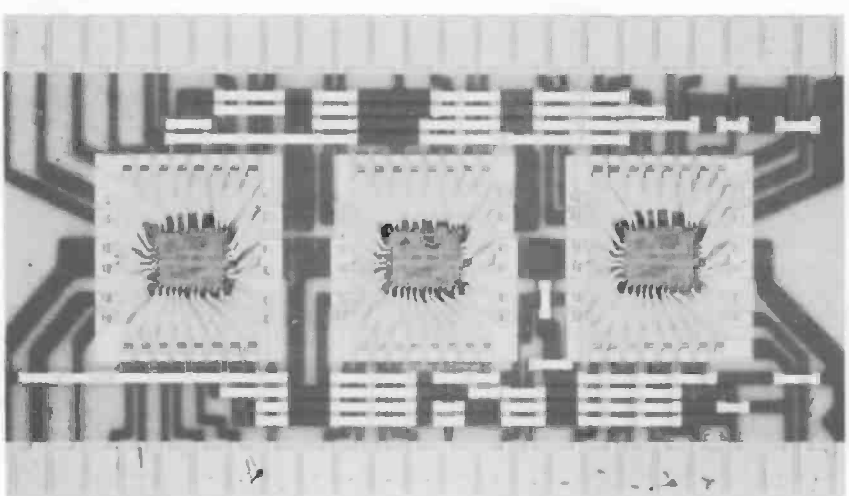

Fig. 14
Beam-tape-bonded microcircuits on microbridge substrates.

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SOS technology for real-time signal processing

Silicon on sapphire technology has definitely come of age. In large scale integrated circuitry, it is easy and economical to use, and it has proven performance in a wide range of real-time signal processing applications.

The principal features of SOS LSI, as far as the designer of real-time systems is concerned, are high speed and low power requirement. Often of equal importance is high device density. These and other advantages, are listed in Table I along with characteristics that make them possible. Several comparative disadvantages of using SOS have been cited in the past. Most of them have been alleviated, as indicated by the up-to-date evaluations in Table II.

One can argue for or against any technology. The systems designer cognizant of the pros and cons has to extend his viewpoint to implementation and economics. He wants to design and partition systems in a cost-effective manner. Beyond the SOS combination of power, speed and density advantage are two major implementation assets—the ready availability of powerful CMOS/SOS microprocessors and memories, and design methods utilizing an array of computer-aided design tools that quickly make concepts realizable in LSI and VLSI arrays.

Handcrafted custom design

When using the handcrafted method, the designer first partitions the system into functional logic units. The functions are verified by simulation, and then the units are laid out. Interconnections and placements are determined by manual drafting, or by using an interactive graphic terminal.

Once the artwork is generated, the array is completed by mask making, fabrication, packaging, and testing. The last steps are common to all three design approaches. Though the highest density is achieved by handcrafting, it is the most time consuming and the designer has to be very familiar with the basic technology, design rules, and the effect of layout on performance.

Standard cell design

The standard cell approach to designing LSI arrays is quite similar to the handcrafted method in the initial phases, where system partitioning is accomplished. However, once a system is partitioned into logic functions that can be implemented on an LSI array, the similarity ends. Standard cells with defined logic functions and

Table I
What SOS offers the system designer.

Advantage	*Contributing Factor*
Low Dynamic Power	Small geometry devices with minimum device capacitance.
High Density	Elimination of guard bands.
Wide Range of Operating Voltages	Complementary structure.
Radiation Resistance	Elimination of latch-up and high peak photocurrent.
Simplified Design	Exotic clocking systems not needed for high-speed static logic.
Easy to Model	Device performance can be reliably simulated using known dimensions and standard material constants.

Table II
An update on historical disadvantages of SOS.

Disadvantages (Or Lack of Advantage)	*Current Evaluation*
High Cost of Material	Cost reduced to competitive level by 3-inch wafers and and ribbon sapphire.
High Densities in Other Technologies	Bipolar circuits, dynamic NMOS memories, and I^2L are more dense—but the power requirement is 4 to 10 times higher than for SOS.
Low Power Can be Achieved for I^2L	At a trade-off for performance.
High Speed Can be Achieved with Other Technologies	True, with the large choice of components in bulk MOS and bipolar.

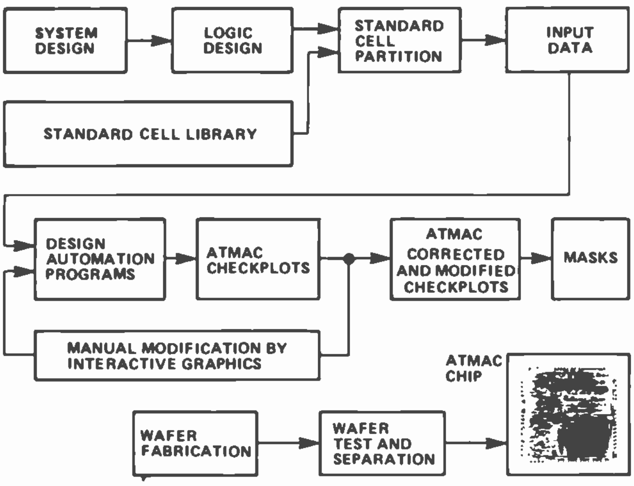

Fig. 1
Design methodology for standard cell approach.

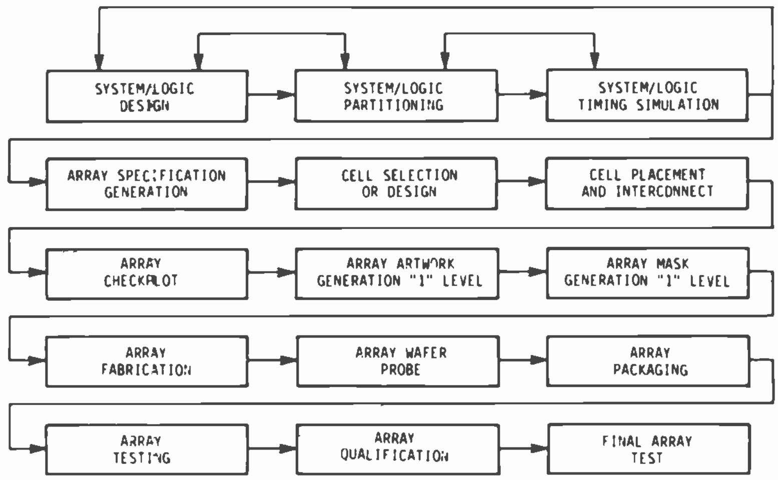

Fig. 2
Design methodology for universal gate array approach.

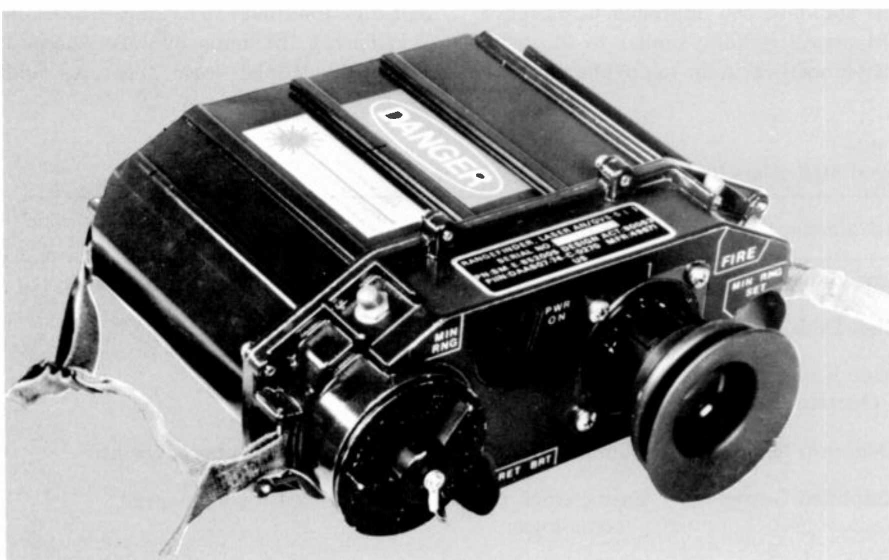

Fig. 3
AN/GVS-5 handheld laser rangefinder.

predetermined configurations and dimensions are selected from a computer stored library to perform the partitioned functions. The flow of the standard cell approach is shown in Fig. 1. Simulation is done by using timing and logic information from a catalog of logic cells. Once the simulation has verified that the logic is correct and will execute in the time required, cell interconnect information is fed to a computer program that automatically lays out the array.

RCA has been working with this approach to LSI for over 10 years and has developed several families of standard cells. The standard cell approach offers the system designer the opportunity to closely interact with the array design without an exhaustive understanding of the basic technology.

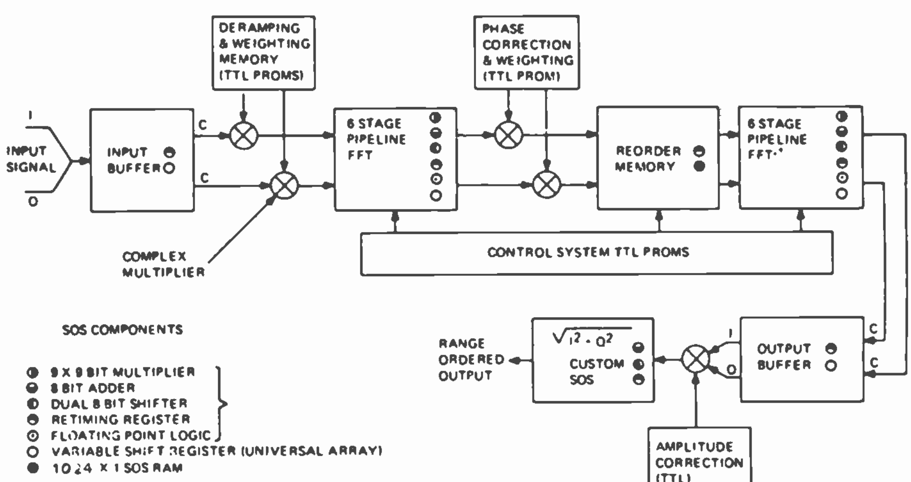

Fig. 4
Programmable waveform generator system.

Universal gate arrays

The universal gate array (UGA) approach to designing LSI arrays has also been successfully used by RCA for over 10 years. The logic is partitioned onto available UGAs and then simulated. A typical flow of design steps is shown in Fig. 2. The UGA approach uses logic cells similar to the standard cells, but interconnection and placement are done manually. RCA is now working on an automatic UGA placement and routing program.

The major advantages of the UGA approach are minimum cost and minimum turnaround time from design to fabricated array. The disadvantages are minimum density and a limitation on the number of input/output pins.

System applications of SOS circuits

The performance of SOS LSI circuits has been proven in a variety of equipment, extending in complexity from a handheld rangefinder to a radar signal processor, and in physical and environmental constraints from large ground-based systems to RPV-borne miniaturized units. The following descriptions indicate the equipment requirements and constraints, and show how SOS circuits were used to meet them.

AN/GVS-5 handheld laser rangefinder

The AN/GVS-5 resembles a pair of ordinary binoculars (Fig. 3), but contains a light-weight, inexpensive device that observers can use to determine the precise range of a distant object within one second. The user simply aims at the target and depresses a button that triggers an invisible laser beam. The beam hits the target and returns through a receiver telescope. Elapsed time between transmission and reception is automatically converted to a range-to-target reading, which appears as a display in the eyepiece. Typical characteristics of this rangefinder are given in Table III. Many units are now in use by the U.S. Army and Marine Corps.

Two CMOS/SOS UGAs, a crystal oscillator and a display subassembly comprise the essential part of the range counter/display module. Here the use of SOS arrays permits the stringent high speed, low power and high reliability requirements to be met.

The UGA approach was selected for this application because early in the development there was a need to show feasibility in the shortest possible time. UGAs are commonly considered for applications where schedule is the most critical requirement.

Programmable waveform generator

The programmable waveform generator (PWG) was designed for use in an advanced linear FM radar and synthetic aperture processing application.[1] Processor goals included time bandwidth products programmable in the range of 100 to 1000, sidelobe levels less than −35 dB, and clock rates up to 10 MHz.

A functional diagram of the PWG system is shown in Fig. 4, which indicates the major functional subsystems and the CMOS/SOS circuits used in them. Pipeline architecture employed permits input data to be processed in real time.

All elements of the functional pipeline were implemented in CMOS/SOS, while the control system employed transistor to transistor logic (TTL). The use of SOS technology permitted a 10-MHz operating speed with a system power consumption of about 460 watts. Five handcrafted custom SOS LSI designs were used in the PWG arithmetic operations. A sixth SOS circuit

Table III
AN/GVS-5 characteristics.

Technology	CMOS/SOS (Universal Gate Arrays)
Emission Wavelength	1.06 microns (neodymium YAG)
Time to Range	One Second
Energy Output	>15 millijoules
Reliability	>30,000 mean rangings between failures (MRBF)
Operating Temperature	−50 °F to +160 °F
Ranges per Battery Charge	>700

Table IV
Programmable waveform generator system.

9 x 9 Multiplier (TCS-057)	8 Bits Plus Sign; Sign-Magnitude Multiplier with Optional 8-Bit Rounded Product
9 Bit Adder (TCS-065)	9-Bit Ones or Twos Complement Adder with Overflow Detection and Compensation
Dual 8-Bit Scaler (TCS-016)	Dual 8-Bit Position Scaler for Floating Point Applications and Other Binary Division
Retimer Register (TCS-015)	18-Bit Reclocking Register with Complement Select
Floating Point Logic Control (TCS-017)	Floating Point Control for FFT Arithmetic Unit of Arbitrary Radix (Parallelism)
Programmable Shift Register (TCS-060-400B)	Highly Flexible Shift Register with Variable Length, Complementing Functions and Switched Delays. Total Registers = 38 Bits

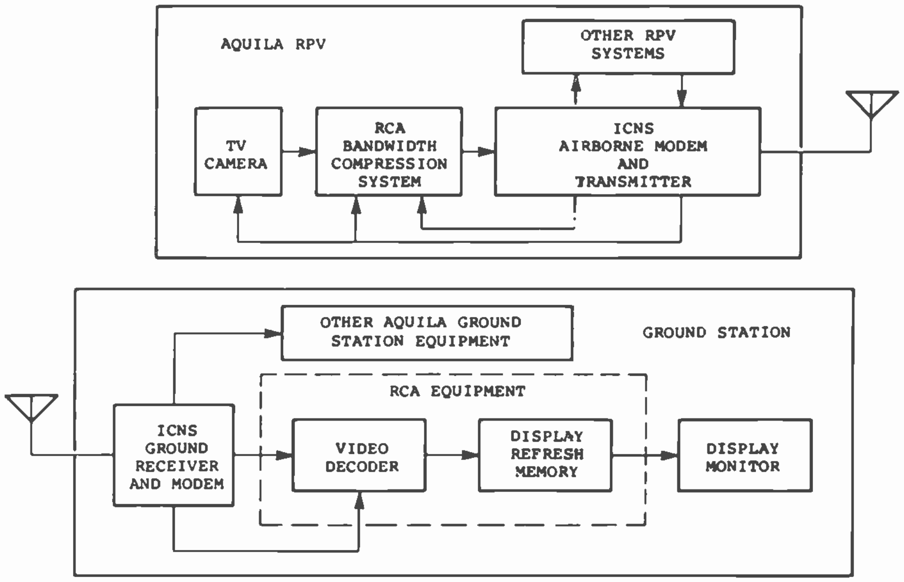

Fig. 5
Aquila system diagram.

utilized the universal gate array approach to obtain a programmable shift register memory. The functions of these circuits are described in Table IV. The bulk memory requirements were met with an SOS random access memory. These arrays were partitioned in six basic functional hybrid module types which house about 70 percent of the circuits employed in the PWG.

As in many advanced digital signal processors, the hardware is sophisticated. Another typical characteristic of a real-time digital signal processor is that many of the basic arithmetic functions are either repeated many times or are very similar throughout the system. Thus, the overall hardware complexity and cost can be minimized if this functional redundancy can be exploited by partitioning the system into a limited number of functional blocks. The design of the CMOS/SOS LSI circuits and modules in the PWG achieved this end.

Image bandwidth compression system

The most challenging physical constraints for a real time signal processing system were met by SOS technology in the design and fabrication of an image bandwidth compression equipment for the U.S. Army's Aquila RPV.[2] Figure 5 shows how the RCA airborne system fits into the Aquila electronics. The airborne unit accepts the output of a TV camera mounted in the nose of the aircraft, reduces the frame rate, digitizes the video, performs the bandwidth compression, and delivers a serial data stream to the Integrated Communication and Navigation System (ICNS) modem. The ICNS modem multiplexes the video signal into its communication link with the ground. On the ground, the modem delivers the demultiplexed encoded signal to the video bandwidth-compression decoder, which restores the video to an analog signal suitable for driving a TV monitor.

The processing techniques to achieve bandwidth compression are: 1) the transformation, in the horizontal direction, of the video to its spatial frequency components by a discrete cosine transform (DCT); 2) the encoding of the transform coefficients in the vertical direction by a differential pulse code modulation (DPCM); and 3) selective quantization of the DPCM words. As a result of this processing, the bit rates for the transmission of the digitized TV are reduced to 3.2, 1.6, 0.8, and 0.4 bits per pixel (selectable). With the associated reduction in resolution to 256 by 256 pixels, and frame rate reduction to 7.5 frames/second, the overall data transmission rates are 1600, 800, 400, and 200 kb/s, corresponding to the four selectable data bit rates.

A particularly challenging aspect of the design was the required degree of miniaturization. It was achieved by a combination of SOS LSI and advanced hybrid circuit packaging. The resulting airborne encoder, embodying more than 112,000 equivalent transistors in four hybrid

Table V
Airborne bandwidth compression components.

Components	*Input*	*DCT*	*DPCM*	*Output*	*Total*
Analog	7	-	-	-	7
TTL	16	26	8	7	57
CMOS	10	2	4	12	28
CMOS/SOS	1	9	10	6	26
PMOS	-	-	2	-	2
IC Chips	27	37	24	25	113
Resistors	18	35	26	8	87
Capacitors	12	15	9	3	39

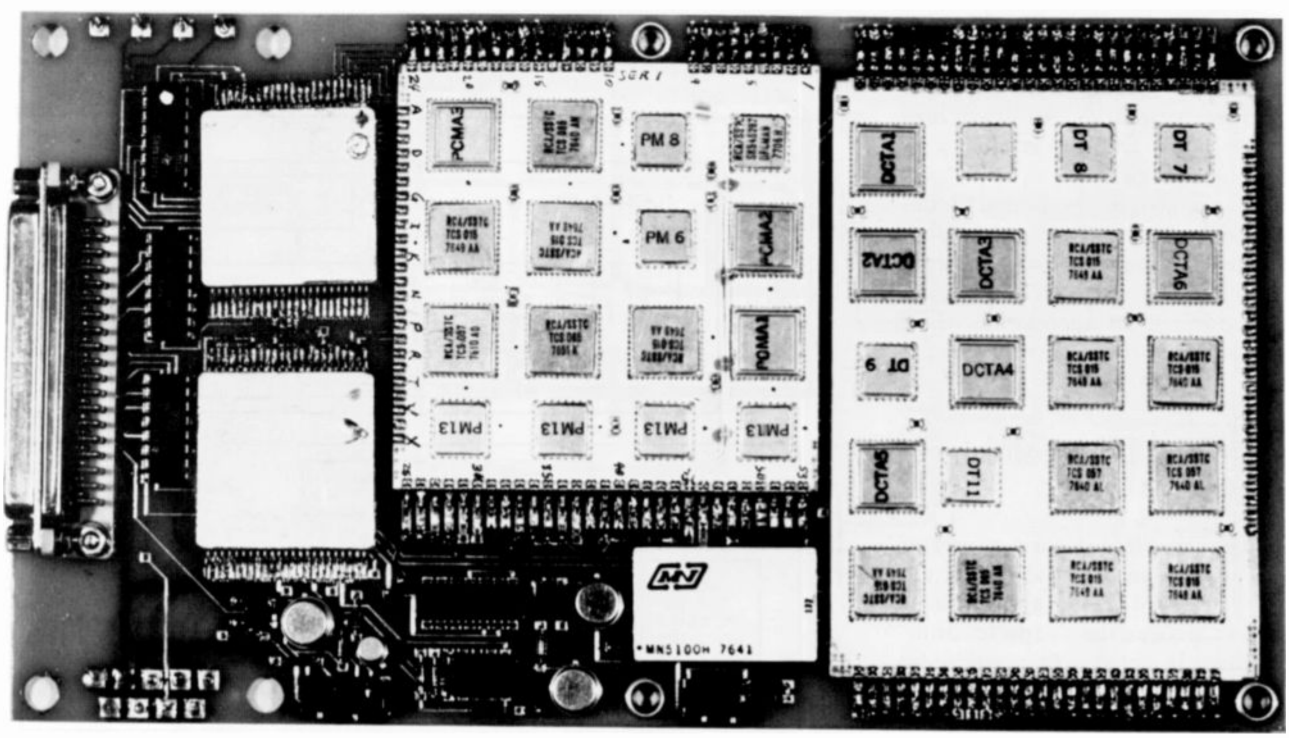

Fig. 6
Bandwidth compression encoder.

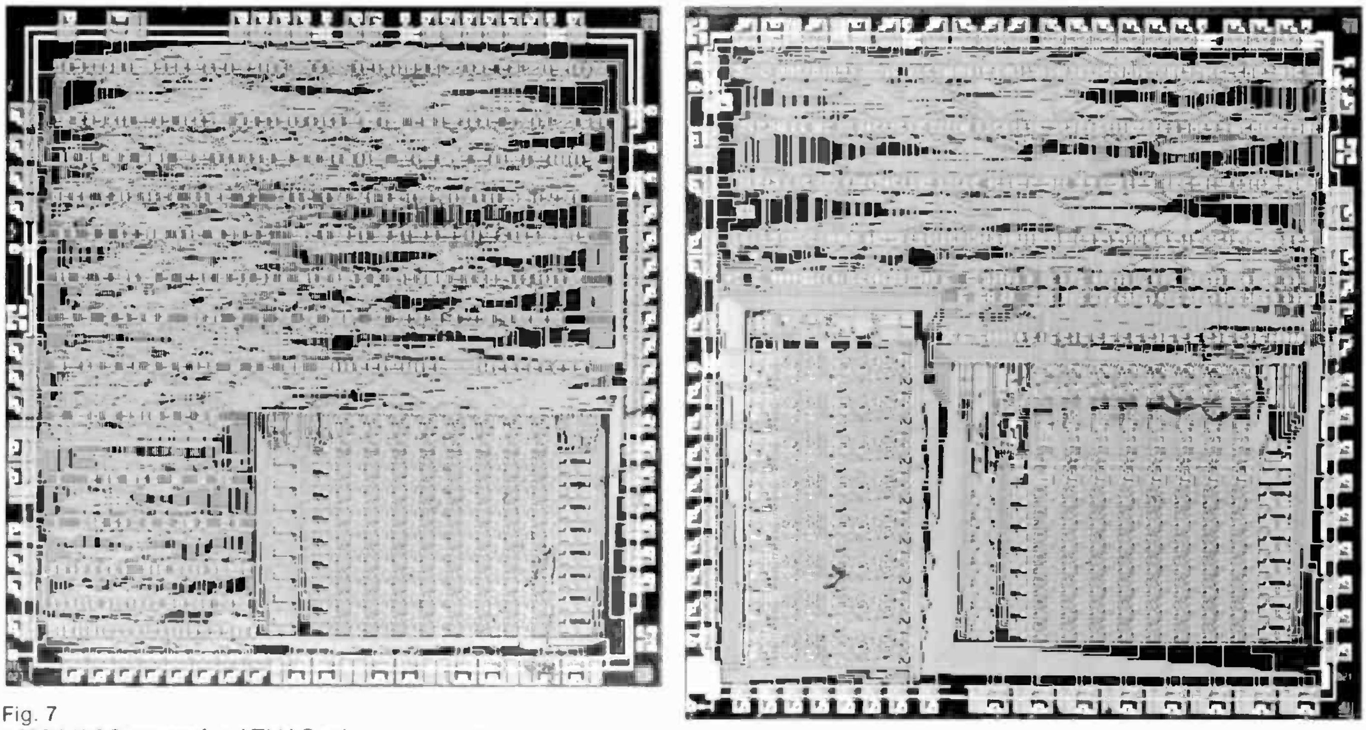

Fig. 7
CMOS/SOS arrays for ATMAC microprocessor.

assemblies, was built on a board 5 by 9 inches, which weighed 0.78 lb, and consumed 13.5 W of power.

The quantities of components used for the various functions are listed in Table V, and the airborne operational system is shown in Fig. 6. The bandwidth compression system used building block arrays from the PWG program and was successfully designed and fabricated in 10 months.

Application of CMOS/SOS microprocessors

Two standard cell CMOS/SOS arrays (Fig. 7) were designed to contain all of the circuitry required for a bit-slice processor expandable in 8-bit increments. Two arrays of each type have been configured into 16-bit microprocessors (named ATMAC) and used for high-speed, complex signal processing.

Sonar signal processing

RCA has assembled, programmed, tested and demonstrated a microprocessor based system that performs adaptive spatial beam forming, complex translation, and digital filtering for processing sonar signals in real time.[4] The demonstration of this system proved the practicality of developing equipment to perform this type of

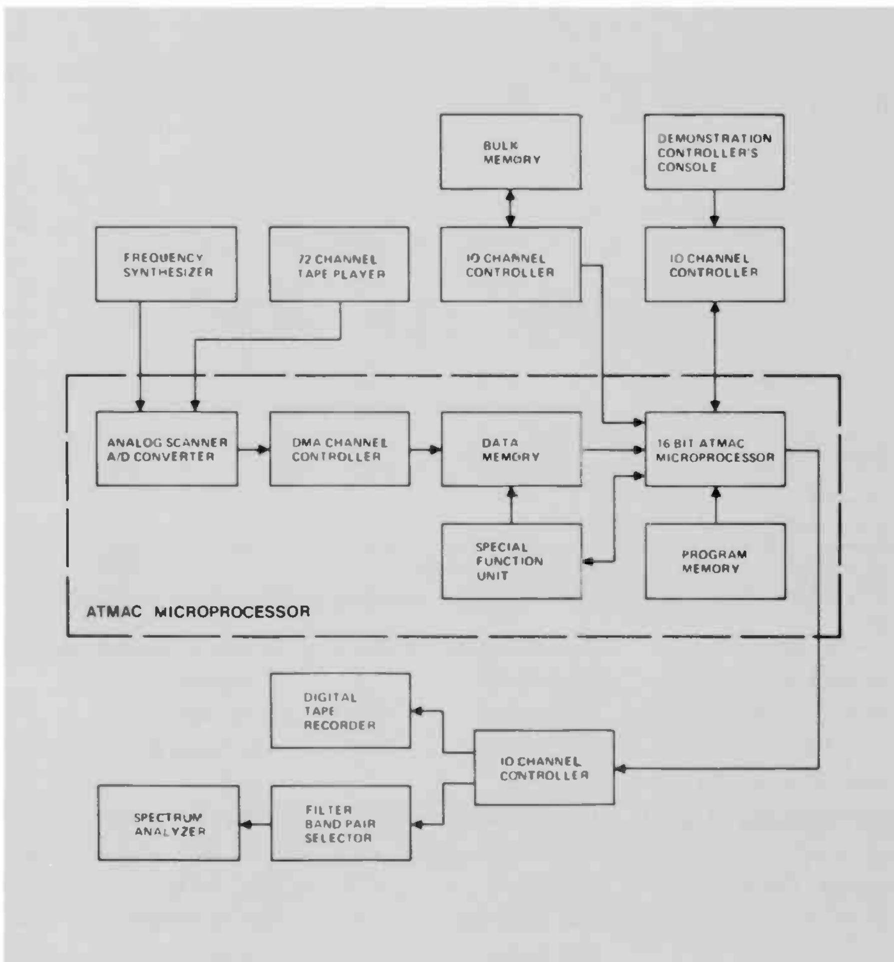

Fig. 8
Sonar signal processing demonstration system.

Table VI
Future developments in two LSI technologies.

Characteristic	*NMOS* 1978	*NMOS* 1980	*SOS* 1978	*SOS* 1980
Density (Gates/(mm)^2)	140	200	110	200
Gate Delay (ns)	1	0.5	2	1
Power Dissipation (mW/Gate)	1	0.4	0.1	0.05
Speed/Power (pJ)	1	0.2	0.2	0.05
Mask Levels	6	6	7	8
Critical Dimensions (Microns)	4	2	5	3.5
Static Memory Cell (Sq. Microns)	2400	1100	3300	1000

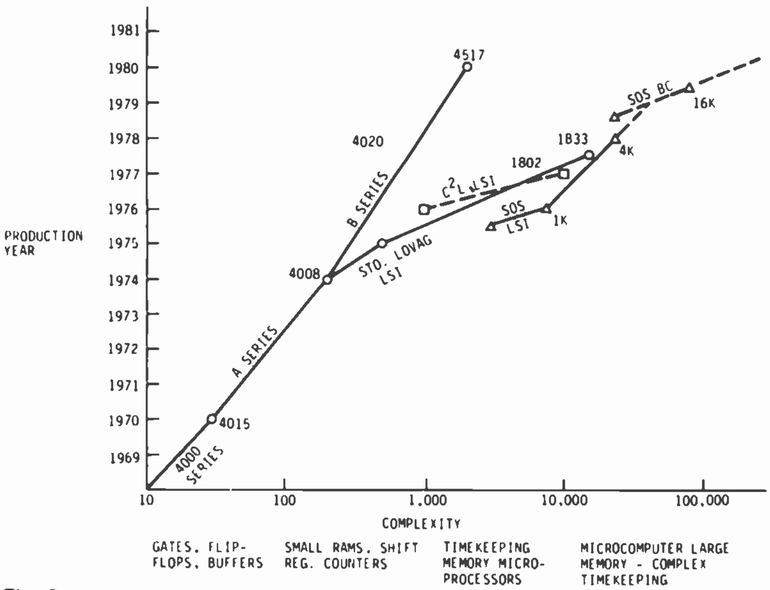

Fig. 9
RCA CMOS/SOS evolution.

Table VII
Future SOS product direction.

	1980	1982
Process Innovations	Buried Contact Double Poly	E-Beam Photolithography
Design Rules	3½ Micron	2 Micron
Die Sizes (Typical)	5 Sq. mm	6 Sq. mm
Wafer Sizes	4 in Squares	5 in Squares
Defect Density (Per Level)	1/sq. cm	½/sq. cm
Die Complexity (Typical)	80K Transistors	150K Transistors
Potential Products	16K RAM	64K RAM
	8K EAROM	28K EAROM
	64K ROM	126 ROM
	16-Bit Microprocessor	32-Bit Microprocessor

processing in an unattended buoy. In this environment, the equipment is required to form multiple beams simultaneously and to filter the data computed through a large number of complex digital filters simultaneously. The microprocessor system, including all of its peripheral controllers, is to consume less than 5 watts.

In the demonstration system, (block diagram, Fig. 8), the signal inputs come from either a frequency synthesizer or the playback of a tape with signals previously recorded from an array of sensors in the ocean. This unit uses CMOS/SOS throughout most of its construction. The same parts are directly applicable to the final system design.

The 16-bit ATMAC microprocessor is also used for this application. In the demonstration system, it is supported by a special function unit consisting of a CMOS/SOS 16-bit multiplier with its accumulator controller, and a special Modulo Arithmetic Address Generator Unit. The microprocessor includes 2048 words of 24-bit program memory and a data memory consisting of 14,336 words of 8 bits each and 6144 words of 16 bits each. The data and program memories are constructed using the RCA CD5041D 1K-by-1 CMOS/SOS RAM.

In the buoy deployed system there are two microprocessors. Both have a 16-bit by 16-bit multiplier and accumulator-controllers. One of the two microprocessors has a Modulo Arithmetic Address Generator Unit.

The memories in the deployed system have capacities of 2000 24-bit program memory words for each microprocessor, and data memories as follows:

a. For one microprocessor, 13,312 words of 8 bits each and 2048 words of 16 bits each; and
b. For the other microprocessor, 6144 words of 16 bits each.

These memories are constructed using the newly developed 1K-by-4 CMOS/SOS RAM, the RCA TCS051.

Two low power consumption sea-trial units will be completed by 1980. In each system, 123 CMOS/SOS LSI arrays will be employed.

Radiation-hardened CMOS/SOS circuits

At this point, we would like to give some attention to a different but very important requirement for LSI circuits—their ability to remain operable in a heavy radiation environment.

Many of the factors that make CMOS/SOS attractive for LSI/VLSI applications also make the technology well suited for radiation-hardened applications. The fabrication of CMOS devices in epitaxial silicon grown on sapphire allows the devices to be isolated, eliminating the interaction with the substrate normally experienced in CMOS devices fabricated in bulk silicon. This isolation from the substrate allows normally designed devices to operate successfully in transient radiation environments up to 10^9 rads per second or greater. Another aspect of CMOS devices attractive for radiation environments is that they are majority carrier devices and, therefore, not affected by neutron radiation until very high levels are reached—approximately 10^{14} neutrons per square centimeter or greater.

The type of radiation that causes the most degradation in CMOS/SOS devices is continuous dose radiation. This kind of radiation causes charges to be trapped in silicon dioxide/silicon interfaces, which causes the threshold voltage and mobility to change. The effects of ionizing radiation can be reduced by using processing techniques that hold the threshold voltage shift to a minimum. Another technique used is circuit design oriented. This circuit technique consists of tying the substrate of the P devices to a fixed potential. These helped hold the P-device threshold shifts in the 1- to 3-volt range.

RCA recently designed and produced a high-speed code generator using the hardening process and circuit technique just described. The code generator performed at a rate greater than 10 MHz after exposure to over 10^6 rads (Si). This work is described in reference 5. The availability of CMOS/SOS circuits that will continue to perform in hostile radiation environments has made it possible to design space systems that operate for long periods. An example of a system that will use RCA's radiation hardened technology is the SAMSO sponsored Fault Tolerant Spaceborne Computer.

Future CMOS/SOS technology

The previous material has discussed CMOS/SOS technology as it stands today, and its application in several recent systems. Now we would like to review where the technology is going in the next

Jim Saultz has been selected just recently to coordinate GSD's response to the Government's need for Very High Speed Integrated (VHSI) circuits. He will be concerned with all aspects, including systems applications, device architecture, technology, automated design, processing and testing. Before assuming this responsibility, he was manager of ATL's Digital Systems Laboratory, directing the development of LSI circuits custom designed for signal processing. He was responsible, also, for enhancement and application of microprocessors, including the ATMAC, and for expansion of the Computer Aided Design and Design Automation System for standard cell circuits and universal gate arrays.

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Stan Ozga, Unit Manager of the Processor Design Group of ATL, is responsible for development of advanced LSI computer architectures implemented with CMOS/SOS technology and computer aided design. His expertise was beneficial in the development of the ATMAC microcomputer, the SUMC/DV computer, and many other custom-designed systems.

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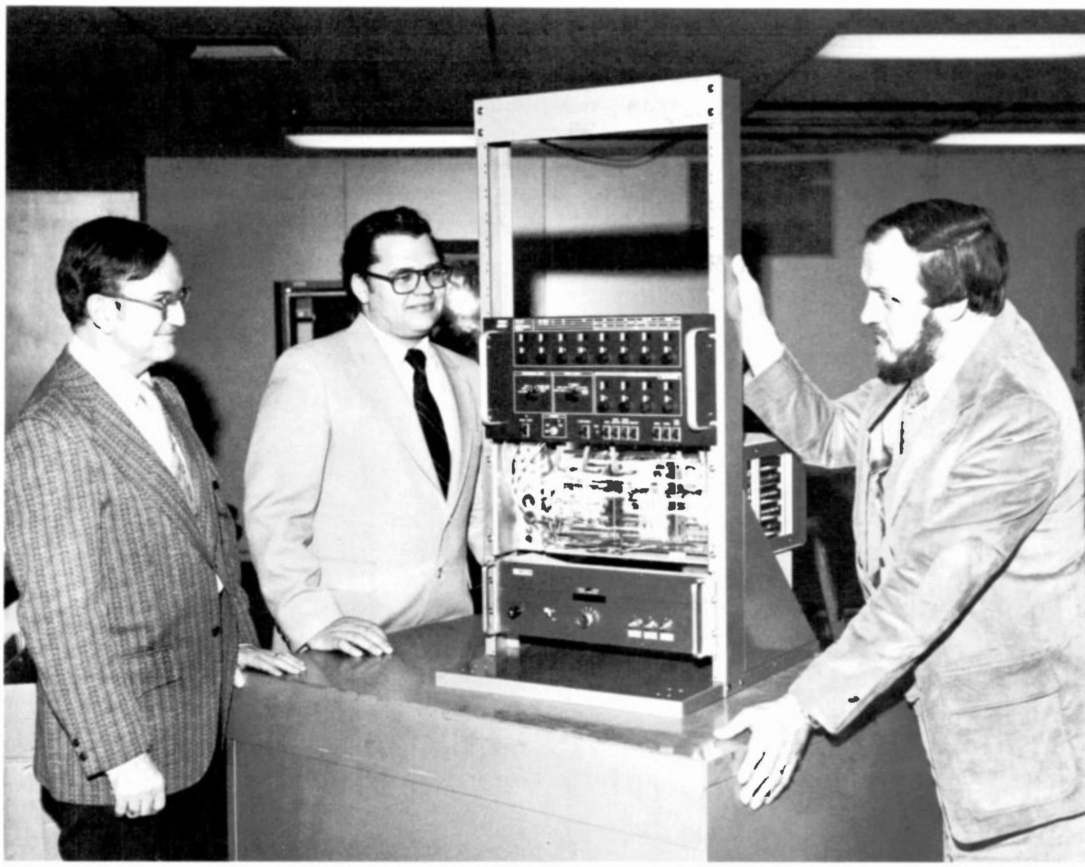
Ext. 3094

Walt Helbig, Unit Manager of the Systems Application Group of ATL, is the prime mover behind the ATMAC microprocessor, several portions of which are illustrated in this paper. Walt's experience encompasses many aspects of signal processing, lately including digital time-domain beamforming of acoustic data, subsequent complex translation, and digital filtering, as well as the development of ATMAC programs for demodulating bauded signals. He holds 13 patents in the fields of circuit and logic design.

Contact him at:
Advanced Technology Laboratories, Government Systems Division, Camden, NJ
Ext. 2838



Authors **Helbig** (left), **Ozga** (center) and **Saultz** with the ATMAC Program Development Center.

few years. During the past ten years, the implementation of CMOS technology has progressed from a few gates per chip to the present day capability of 4K RAMs on one chip. This increasing capability comes from improved processing methods and advances in photolithography, which make it possible for fine line geometries to be produced on large chips. A more recent innovation is E-Beam (electronic beam) mask making, which will provide even finer line geometries, with resultant increases in circuit speed and device density.

Current MOS production in industry is based on design rules of 4 to 7 microns. The near-term future will see the technology progressing to design rules at the 1- to 2-micron level, and later to less than 1 micron. RCA is heavily committed to these advances and is conducting development programs that will enable production of SOS static RAM devices with 4-micron technology. A summary of CMOS development from 1978 through 1980 is indicated in Table VI, and in Fig. 9. The generation of 150,000 transistors on one chip, chip fabrication using electron beam techniques and 2-micron design rules are a straightforward extrapolation of present efforts. Products that will be available as a result of this development are shown in Table VII.

It is reasonable to expect a 16-bit processor, like the one used in the speech processor and ocean surveillance applications, to be contained on one chip. The data (RAM) memory will be contained on 4 to 16 chips and the 16-by-16 multiplier with accumulator would be on one chip. The program memory (ROM) would require from 1 to 4 chips. Therefore, a very sophisticated system can be envisioned to consist of 10 to 20 VLSI arrays. In addition to the small parts count, the speed of 16-bit processors will increase to the point where 50-nanosecond instruction times will be possible. If 50-nanosecond processors are tied together in arrays or in distributed systems, processing speeds of one hundred million instructions per second can be achieved.

Conclusion

CMOS/SOS technology has proven its capability and viability for real-time signal processing applications. The material presented in this paper shows how CMOS/SOS technology can be applied to all types of real-time signal processing applications, ranging from low frequency to high frequency, and all with low power requirements. The flexibility of the technology allows system designers to configure processor architectures as simple as arithmetic processors, and as complex as distributed processor networks. In addition to being able to build real-time signal processing systems that have high speed and low power, the technology provides designers with the capability to produce equipment that will withstand the high radiation environment encountered in satellites and missiles.

Near-term developments will provide capability to build 16-bit microprocessors, 16K RAMs, and 64K ROMs on one chip. Future advances will provide the capability of building 32-bit microprocessors, 64K RAMs, and 128K ROMs on one chip. Speeds will double by 1980, and the 1980 speeds will quadruple by 1985. Power dissipation will continue to decrease.

Acknowledgments

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H. Borkan, J. Scott, I. Kalish, J. Fabula, for CMOS/SOS technology support.

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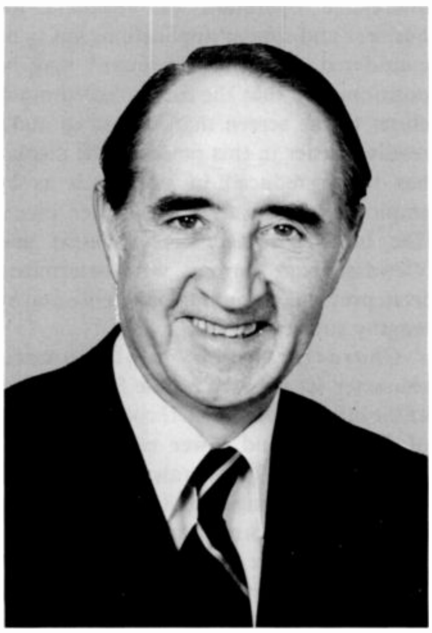
K.M. McKee

Data television—a bright star on the color TV horizon

New Viewdata systems for home and business provide on-line access to a database of useful information via an adapted domestic TV receiver and a telephone line. Teletext systems insert data in the vertical blanking lines of television signals.



Ken McKee is Manager, European Technical Relations and has been with RCA in London since 1959. For 28 years he has been concerned with advances in television. Initially, he was engaged in broadcast systems research, and subsequently in international marketing, manufacturing and licensing.

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Digital data television was promoted in the United Kingdom during the early 1970s. Its purpose was to provide a new, continuously updated information service for the home and office displayed by words and simple graphics on a color TV receiver. Two features vital to viewer acceptance were simplicity of use and low cost. Other important factors were good legibility at normal viewing distance and sufficient flexibility within the display format to offer a varied and attractive presentation. Hard copy output from a printer was considered to be a feasible option. More recently, computer technology combined with the application of LSI digital processors to TV receivers has opened up a whole new range of possibilities involving "interactive participation" by the user. It is becoming apparent that a powerful new information medium with a marketing capability is in the initial phase of growth.

Early data television

The basis of the present data television system was the "Homefax" system[1] developed by RCA Laboratories in the 1960s, and successfully tested in New York and New Jersey.

Following this in February 1972, the British Broadcasting Corporation[2] developed a digital system now known as CEEFAX. In April 1973, the Independent Broadcasting Authority demonstrated another data broadcast system later named ORACLE. A milestone was passed when unified standards were agreed upon by BBC, IBA and the TV receiver industry, enabling the first joint specification to be published during 1974. A final data broadcast version[3] with additional features appeared two years later. Experimental transmissions by both broadcasters had by that time been replaced by the CEEFAX and ORACLE daily services broadcast nationally in the UHF band over the two BBC and IBA color TV networks.

Modern broadcast and wireline systems

Today, data television systems can be divided into two broad categories: broadcast and public telephone; or to use the new generic terms: Teletext and Viewdata. Teletext is broadcast over a normal television picture channel by inserting the digital data signals during unused lines in the field (vertical) blanking interval (Fig. 1).

Viewdata links the user to a network of computer databases via the public telephone system. The service is interactive, with the user interrogating a remote computer by means of a hand-held keypad controlling an adapted color TV receiver. The receiver has the role of an on-line visual display unit in a conventional computer system. For extended use in business, a keyboard can replace the keypad, and a specially designed low-cost printer can be connected up to the receiver terminal to provide hard copy output.

To reduce the costs of the LSI digital processors, character generators and

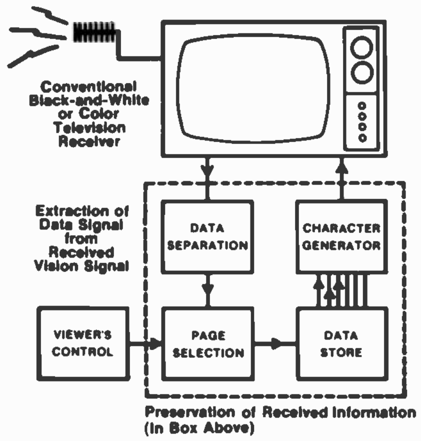


Fig. 1
Schematic diagram of a Teletext data TV system. In Teletext, the digital data is inserted into the vertical blanking interval of a normal broadcast television signal.

stores, Viewdata and Teletext systems normally employ the same color display format. The British Post Office which initiated the Viewdata concept has had a pilot scheme in operation for over two years. The trial system has since been followed by a public test service involving 1,500 TV receivers in three cities. The Post Office has decided to use the name "Prestel" for all of its Viewdata services.

Display hardware is not the only area common to both Teletext and Viewdata: some of the software is also shared. For instance, news items of every description — weather and travel information, what's on where, TV and radio guides, leisure magazines — all are suitable material for either service. But there are important differences arising from each system's limitations. During and after major sporting events hundreds of thousands of people want to know the latest scores. Access to a Viewdata database is confined to the availability of telephone circuits between users and the computer ports (first-generation Viewdata computers, for example, have 208 ports). As lines rapidly become busy, access for the vast majority is denied and any form of electronic queuing is certain to exasperate eager fans. The same situation occurs when news of any kind breaks which immediately affects a large number of users. Provision of additional circuits and ports to meet such peaks in demand is clearly impractical.

Broadcast Teletext does not suffer this handicap, but if Teletext is transmitted on only two lines in the field blanking interval, as is the case at present, the Teletext database is confined at any one time to 800 "pages" of information — the technical reasons for this will be explained later. Teletext and Viewdata are thus to a certain extent complementary, Teletext being a medium with unrestricted access for mass dissemination of a limited database, while Viewdata, with finite access, has the capability of retrieving information in depth from a database of virtually unlimited capacity.

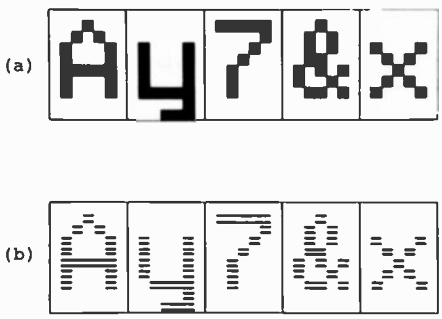


Fig. 2
The dot matrix characters (a) are based on the ISO-7 subset of the ASCII code. The effect of scanning 9x5 dot matrix characters is shown (b).

Standardization of systems

The potential of data television has attracted interest in many countries and a number of broadcasters and telephone authorities apart from those in the United Kingdom have set up experimental systems under a variety of names (Table I). The Teletext specification was primarily based on the English alphabet and numerals. An extension has since been proposed introducing a supplementary set of 85 accented characters which will permit the languages of 88 percent of Europe's 500 million population to be displayed. It has been pointed out that this extension will probably also cover all the broadcast languages of North and South America, South Africa, Australia and New Zealand, i.e., English, French, Spanish, German, Dutch and derived languages. A different supplementary set of 91 accented characters would cater to the languages of the remaining 12 percent of the population living in Eastern Europe.

Another problem to be faced is incompatibility between the technical standards that have been proposed for several of the new systems, each claiming special advantages. If internationally switched telephone networks are to be used for Viewdata, compatibility becomes essential. The position is at present under review by the International Telegraph and Telephone Committee (CCITT) of the ITU with the object of harmonizing standards to avoid proliferation of incompatible systems. In the absence of agreed international standards, the descriptions which follow refer to Teletext and Viewdata systems developed to comply with the 1976 Teletext specification[3] published in the UK. The Teletext systems have been successfully transmitted over the three national TV networks for more than three years as regular broadcast services.

The display format

The basic requirement of a data TV display is that the screen be easily legible at normal viewing distances. This favors large size characters, but of course the larger the characters, the fewer can be accommodated per page of data. Then again, the interactive operation of Viewdata for business and similar applications has to be considered where the keyboard may be positioned so that the user is seated much closer to the screen than usual. To make reading easier in this position, the display has to be reduced in size, such as by employing a receiver with a smaller screen. The basic parameters of Teletext and Viewdata page formats were determined from previous computer experience and by lengthy subjective testing.

Characters The alphanumeric character set is based on the ISO-7 subset of the international ASCII code, consisting of 52 upper and lower case alphabetic characters, "ten" numerals, and 34 special characters, making a total of 96 characters. Characters are formed on the screen using 9x5 dot matrix where the upper case characters are on a 7x5 matrix with the extra lines below for lower case "tails", for example, y and g (Fig. 2).

Rounding Interlaced scanning the diagonal portions of dot matrix characters produces a double-line stepped structure and reduces the average brightness of these to $1/\sqrt{2}$ of the vertical and horizontal portions. An optional rounding technique on alternate fields (Fig. 3) considerably improves the outline and brightness of diagonals with only a small addition to character generator cost.

Capacity Each data line carries codes for a row of 40 characters and there are 24 rows/page, making a total of 960 characters/page. The term row is used rather than line to avoid any confusion with TV lines. Teletext has 100 pages per

Table I
Early growth of data television. The potential of data television has attracted interest in many countries.

System	*Affiliation*	*Location*	*Status*
TELETEXT			
CEEFAX	BBC	United Kingdom	National service since 1974
ORACLE	IBA	United Kingdom	National service since 1975
ANTIOPE/DIDON	ORTF, CCETT,TDF	France	Paris Bourse service since 1977
TEXT-TV	Swedish TV	Sweden	Test Transmissions since 1975
VIDEOTEXT	ARD,ZDF, BDZ	W. Germany	Test Transmissions since 1977
TELETEXT	Danish TV	Dènmark	Test Transmissions since 1977
CIBS	NHK	Japan	Test Transmissions since 1978
TELEDATA	KSL TV	Saltlake City, USA	Test Transmissions since 1978
INFO-TEXT	Micro TV	Philadelphia, USA	Local business service 1979
LINE-21	PBS	Washington, USA	Service for the deaf 1979
VIEWDATA			
PRESTEL	Post Office	United Kingdom	Public test service 1979
BILDSCHIRMTEXT	PTT	W. Germany	Public test service 1980
TITAN	PTT	France	Public test service 1980
CAPTAINS	Post Office, NEC, etc.	Japan	Pilot test service 1978
TELSET	PTT, Sanoma, Nokia	Finland	Pilot test service 1978
VIDEOTEX	Bell	Canada	Pilot test service 1979
VIEWDATA	Hong Kong Telephone	Hong Kong	Business service 1979
VIEWDATA	PTA	Netherlands	Pilot test service 1979

Several major US companies are actively engaged in developing other Teletext and Viewdata systems in collaboration with broadcast, common carrier and CATV operations.

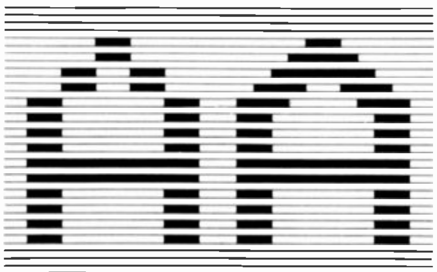


Fig. 3
Rounding improves the outline and brightness of character diagonals.

magazine with a maximum capacity of eight magazines for transmission on two television data lines. The top row of a page is reserved for the identification header, i.e., service, page number, clock time, etc., and the bottom row for control messages. Approximately three percent of the page is required for control characters appearing as blank spaces on the screen known as "black holes." This means that the effective page capacity amounts to some 750 characters or about 150 words, which in practice is often further reduced to 100 words per page to allow for more liberal spacing.

Modes Thirty-two control characters, usually positioned in the spaces before words, initiate a range of display modes (Fig. 4) at the start or within a row. Control characters determine alphanumeric or graphics mode, color, background and other modes that will be described separately. The art in composing a data page is the skilled manipulation by editorial staff of the various modes singly or in combination to produce a clear and effective presentation.

Graphics The 64 graphics characters are based on a small 2 x 3 dot matrix (Fig. 5). Each bit in a graphics character digital code can illuminate one dot cell, permitting the construction of simple maps, diagrams, and extra large letters. The dot cells can be either contiguous or separated, again determined by control characters.

Color By off-on control of the color tube guns, text and graphics can be white, yellow, cyan, magenta, red, green or blue. A special "hold" character in the graphics mode enables itself and any following control characters to be displayed as repeats of the previous graphics character thus allowing adjacent areas to be colored differently without intervening black holes.

Double Height To emphasize certain words, a control character can initiate a double height mode where following

	b_7	0	0	0		0		1		1		1		1	
	b_6	0	0	1		1		0		0		1		1	
	b_5	0	1	0		1		0		1		0		1	
Bits b_7 b_6 b_5 b_4 b_3 b_2 b_1	Row \ Col	0	1	2	2a	3	3a	4	4a	5	5a	6	6a	7	7a
0 0 0 0	0	NUL				0				P		—		p	
0 0 0 1	1		Cursor DC1 On	!		1		A	Alpha* Red	Q	Graphics Red	a		q	
0 0 1 0	2			"		2		B	Alpha* Green	R	Graphics Green	b		r	
0 0 1 1	3			£		3		C	Alpha* Yellow	S	Graphics Yellow	c		s	
0 1 0 0	4		Cursor DC4 Off	$		4		D	Alpha* Blue	T	Graphics Blue	d		t	
0 1 0 1	5	ENQ		%		5		E	Alpha* Magenta	U	Graphics Magenta	e		u	
0 1 1 0	6			&		6		F	Alpha* Cyan	V	Graphics Cyan	f		v	
0 1 1 1	7					7		G	Alpha* White	W	Graphics White	g		w	
1 0 0 0	8	Cursor ← BS	CAN	(		8		H	Flash	X	Conceal Display	h		x	
1 0 0 1	9	Cursor → HT		)		9		I	Steady	Y	Contig Graphics	i		y	
1 0 1 0	10	Cursor ↓ LF		*				J		Z	Separated Graphics	j		z	
1 0 1 1	11	Cursor ↑ VT	ESC	+		.		K		←		k		¼	
1 1 0 0	12	Cursor Home & Clear FF		,		.		L	Normal Height	½	Black Background	l		‖	
1 1 0 1	13	Cursor ← CR		–		=		M	Double Height	→	New Background	m		¾	
1 1 1 0	14		Cursor RS Home	.		>		N		↑	Hold Graphics	n		÷	
1 1 1 1	15			/		?		O		⁝	Release Graphics	o		▮	

Fig. 4
Viewdata transmission codes. Control characters determine alphanumeric or graphics mode, color, background, and other modes.

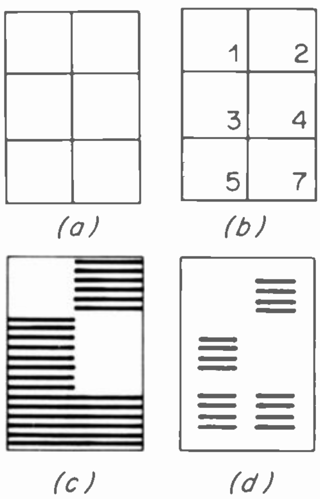


Fig. 5
Graphics character dot matrix (a); each dot controlled by one bit (b); contiguous graphics mode (c); separated graphics mode (d).

characters or graphics are displayed twice the normal height but with the former width.

Boxing Control characters are provided to instruct a Teletext receiver to blank out a "box" in a TV picture or page of data and insert a Teletext message. The facility enables a news flash, subtitles or captions to appear superimposed on the display framed against a black background. Teletext subtitles superimposed on the TV picture is the basis of a new service to aid the deaf in viewing television.

Flashing To draw the attention of the viewer to a message of particular significance within a page or superimposed on a TV picture, words can be made to flash continuously on and off at a rate of about one flash per second.

Conceal The conceal mode causes part of the display stored in memory to be suppressed. By pressing a "reveal" key on the remote control unit, the missing portion of the display appears. The feature enables answers in quiz and education programs to remain concealed until disclosed by the viewer.

Hard Copy A number of low-cost compact printers will soon be available for permanent recording of data TV text and graphics in monochrome. Most of these are adaptions of 7x5 dot matrix printers intended for data processing, communications and instrumentation printout on a 4 to 5-in. roll of paper. One type under development by the BBC (Fig. 6) uses impact printing on plain paper taking 35 seconds to print a page. The printhead scans the page in a manner similar to facsimile, printing any text or graphics. Other types print a fixed set of characters on electro-sensitive aluminized paper at speeds of less than one second per page; however, metallized paper costs more than plain paper and is not as easy to read. After a volume market develops, manufacturers are confident that the printer price including interface logic could be in the region of $200.

An even simpler and cheaper way of recording data TV is to read the receiver page store into a modified audio cassette recorder, since the data rate need be no higher than 1,200 bits per second. An average page will occupy up to 5 seconds of standard audio tape, so a one-hour C60 cassette could store up to 700 pages. Audio cassettes obviously offer an inexpensive means of recording data TV information for later display and perusal at leisure.

Teletext system

Teletext data lines can be transmitted on any two of 25 lines in the field blanking interval, but were found to be least noticeable above the top edge of a 625-line TV picture on lines 17 and 18, 330 and 331. The digital data stream will not be visible on a correctly adjusted receiver having normal flyback timing and suppression. During each line period, data is transmitted at 6.9375 Mbps using a two-level NRZ (Non-Return-to-Zero) signal[2] with binary "0" at black level and binary "1" at 66 percent white level. All address and page control instructions are protected by Hamming codes which enable single errors to be corrected and double errors to be detected at the receiver; while character codes have an added odd-parity bit allowing single errors to be detected. The presence of a data line is indicated and bit timing established by a clock-run-in sequence. Figure 7 shows the general structure of each page transmission and how each row is separately addressed to ensure correct positioning within the page display.

Fig. 6
Impact printer under development by BBC, prints any text or graphics page on paper within 35 seconds.

Two data lines per field transmit one page every 12 fields or 0.14 second; blank rows however can be omitted. The page address identifies the data and enables the receiver decoder to select the magazine and page keyed-in by the viewer. The page header then displays the number keyed alongside the transmitted page numbers which rotate in sequence until the keyed number is reached; whereupon the complete page appears on the screen. If the viewer is unfortunate enough to key a page immediately after it has been transmitted, he will have to wait until all other pages in the cycle are run through before it is re-

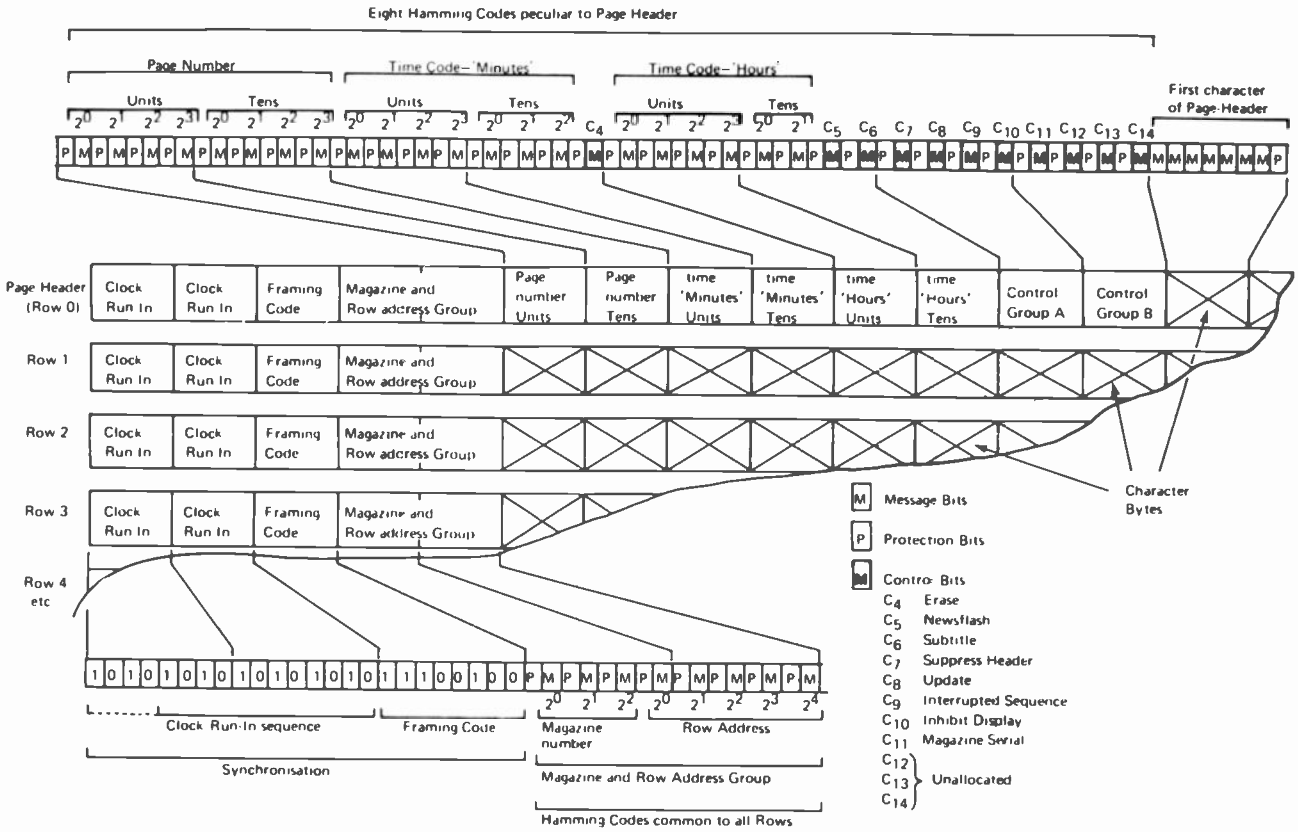


Fig. 7
Page structure showing header, row control and other codes. Each row is addressed separately to ensure its correct positioning within the page.

transmitted. This maximum access time is usually kept down to about 30 seconds by limiting the pages per cycle. Access time for priority pages, such as indexes listing the contents of the magazines, can be reduced by inserting these pages more than once per cycle.

Where information on an item exceeds the capacity of a single page, a group of self-changing pages can be inserted and displayed in sequence one per cycle. Alternatively, a summarized version on one page can quote the number of a "sub page" where more information can be found. Teletext capacity can be considerably extended without increasing access time by employing the transmitted clock time in hours and minutes as an address, and changing the data on some pages if necessary as often as once a minute. Any page may be pre-selected for a particular time and, when received, held in the page store for subsequent viewing. By employing a programmed time switch, a large number of pages could be recorded on an audio cassette and later retrieved at random for display using the time code as an address.

Teletext data insertion terminals and editorial facilities are usually located at a TV studio center, and comprise a data processing system with tape and disc files, keyboards for data entry, and video display units. Staffing requirements are modest, only an editor assisted by one or two journalists are needed at any one time to maintain a service. A skilled journalist can key and enter a page directly, complete with graphics, in two minutes. News items, sports reports, financial data and other items of topical interest are in most cases already on hand at the broadcast center, making the additional costs of a Teletext service minimal.

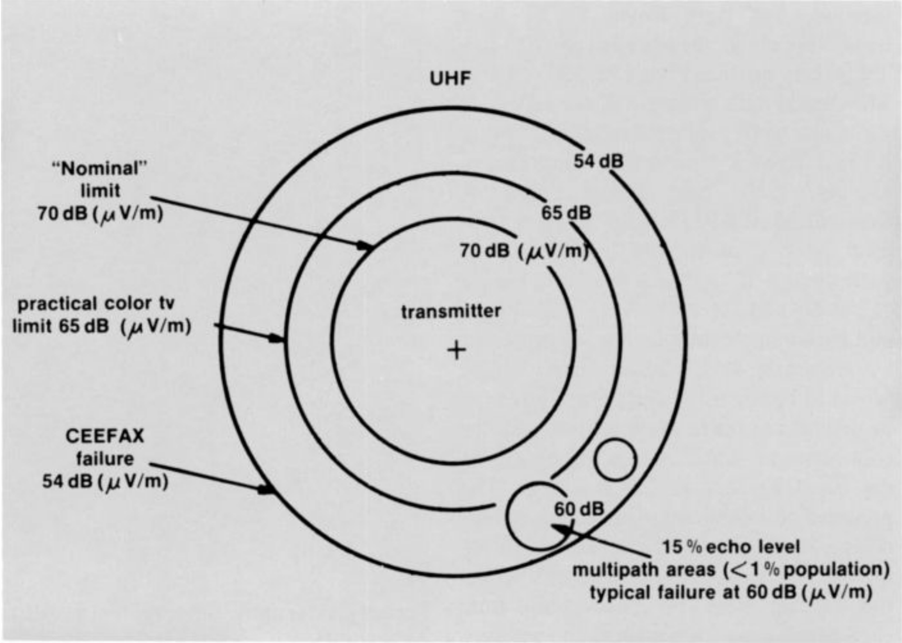
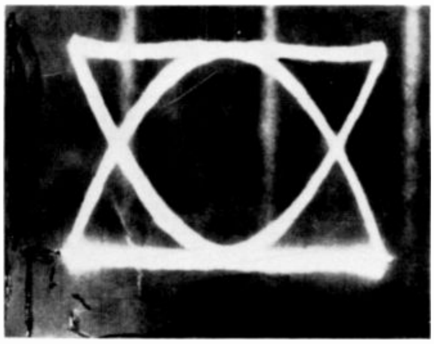


Fig. 8
Results of UHF field tests to evaluate propagation and reception of digital Teletext (CEEFAX field trails results).

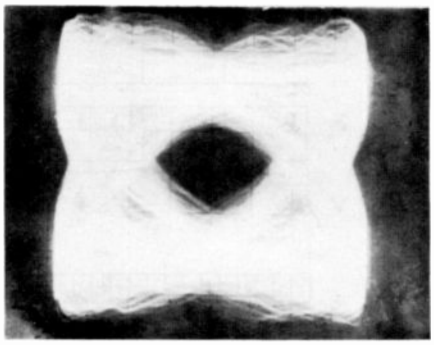
Teletext field tests

Both IBA and BBC have carried out extensive and successful UHF field trials[4] to evaluate the propagation of digital teletext, and to compare reception with the video picture component of the transmitted signal (Fig. 8). Subsequent VHF trials[2] in Germany and Sweden have yielded equally satisfactory results. The quality of the digital waveform after transmission is measured by a parameter known as eye-height[5] (Fig. 9) and represents the percentage voltage difference between the lowest level of logic "0" and the highest level on logic "1" at the center of the bit waveform. The X-axis of an eye display represents one bit period obtained from the data clock frequency, and the Y-axis the digital waveform amplitude. In a recent study, measurement of eye-height directly from the transmitter gave an average figure of 72 percent and at the receiver antenna terminal 56 percent. Degradation is due mainly to interference between adjacent samples in the bit stream caused by multipath distortion and receiver antenna mismatch. Abrupt failure of the decoders may take place below 25 percent eye-height, and usually occurs beyond the outer fringe of the transmitter service area, where the picture signal would in any event be lost in noise.

Data television is likely to influence the future design and performance of picture tubes and TV receivers. Any fall-off in focus at the corners of the screen will make characters in that area difficult to recognize, while poor vertical and horizontal linearity will be even more apparent with data than picture. The frequency response of TV IF circuits has to be sufficient to maintain an eye-height of at least 25 percent into the decoder. In this connection the recent introduction of IF filters represents a major advance, and in addition, enhances picture resolution. RCA's Zurich Laboratories are engaged on an active program studying these and other problems associated with Teletext, Viewdata and microprocessor terminals.



(a)



(b)

Fig. 9
A parameter known as "eye-height" measures the quality of transmitted digital waveform; transmitted eye height (a), and 40 percent eye-height at decoder (b).

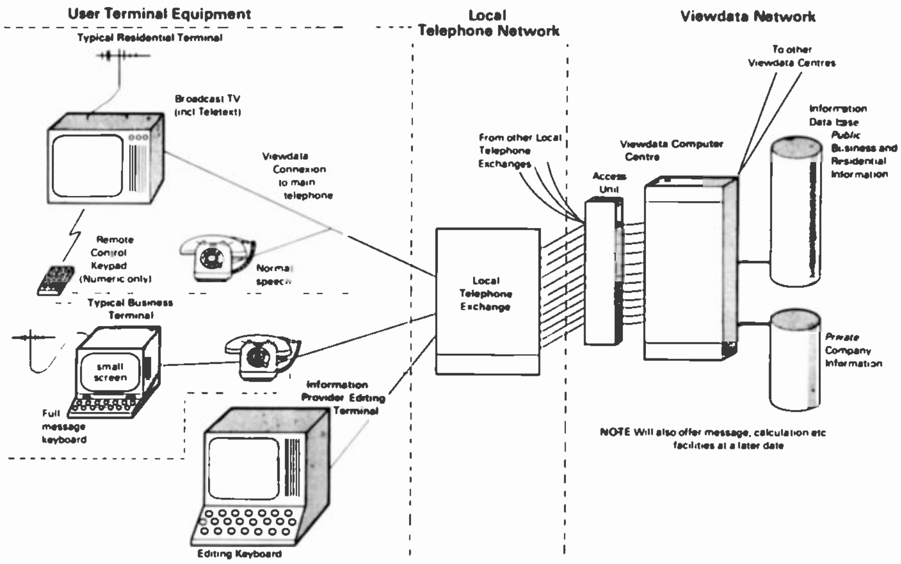


Fig. 10

The Viewdata system offers a simplified interactive terminal for the nonspecialist and more sophisticated terminals for business use. The terminals are connected via the local telephone network to a Viewdata Center.

Viewdata system

Remote interrogation of a computer by an on-line keyboard and visual display terminal is common practice in the data communications world. Technically, Viewdata offers a similar but simplified facility at a fraction of the cost and primarily designed for the non-specialist without any training or expertise in data processing. The database is stored at Viewdata computer centers linked to form a national and eventually an international network to facilitate inter-center transfer of data. The user terminal consists of a remote control keypad or a keyboard connected to a color TV receiver with decoder and modem, which in turn is connected via a local telephone exchange line to the Viewdata center (Fig. 10).

Transmission Digital data is transmitted from computer to terminal at 1200 bps, and from terminal to computer at the lower 75 bps rate. An 8-bit character asynchronous code[6] (10 bits with start and stop bits) is employed, which includes a parity bit to detect single transmission errors. The duplex transmission system enables the user to key while the computer simultaneously "echoes back" keyed characters for display on the screen, thus providing additional error protection. 1200/75 duplex fsk modems are standard, transmitting at 1300 Hz downstream for binary "1" and 450 Hz for "0". Viewdata and Teletext alphanumeric and graphics character codes are identical, and it is only the transmission coding and functions of a number of the control characters that differ. As a result, the design of terminals combining Viewdata and Teletext is greatly simplified.

Calling Sequence A call initiation key is pressed and dial tone is returned from the exchange. Following a second operation of the key, dialing digits are automatically transmitted to call the Viewdata system and a ring tone is then heard from the TV terminal loudspeaker. In replying, the Viewdata number of the terminal is automatically entered at the center for charge purposes. When a "welcome to Viewdata" page appears displaying the user's name as a check, the terminal is ready for an information search to commence. The user may start the dialogue by accessing page zero for the general index, or key known page numbers obtained from a printed directory.

Data Selection Information is divided into two categories: Public, which can be accessed by anyone; and Private, accessible only to a Closed User Group (CUG) by a special password, usually a four-digit number. The pages are organized in tree structure, each branch dealing with a narrower area of the subject in more detail. From page to page, the user is guided in his selection of subsequent pages by being shown up to ten different choices on each page. As he progresses down the tree, the page number is built up, e.g., if he selects item 5 on page 487, the known page number will be 4875. Where appropriate, cross references are quoted to enable a jump to be made from one branch to another. As an aid to access, two special keys * and # together with 0 instruct the computer as follows:

* 0#	Return to index page zero—fresh enquiry
* N#	Jump to known page—number N
* #	Recall previous page—wish to check
* 00	Retransmit page—corruptions on page
**	Erase—keying error

Future Facilities The cursor in Viewdata (Fig. 4) is a symbol which appears on the screen as a bright rectangle the size of an upper case character. It may be switched on or off and moved about the display by special keys on the keypad, or remotely by the computer. Used as a pointer, its position indicates where the next character is to appear, so avoiding the insertion of rows of blank spaces. Additionally, the cursor is useful for editing and overwriting without resorting to page erasure.

A further Viewdata facility will be transmission of messages such as greetings displays between terminals via the Viewdata center. When a user next accesses the center, the user will be informed that there is a message waiting, which will then be displayed. An extension of this facility currently being explored will set up a conversational mode between two terminals. While the dialogue is in progress, the screen is split in half to display simultaneously the transmitted message on top with the received message underneath.

Information Providers (IPs) supply and update the database information and also decide the price the user pays for it. The Viewdata organization rents database storage to the IPs and recovers the cost of the information, Viewdata service and telephone charges, from the user. Information revenue is returned to the IPs after storage rental has been deducted.

As mentioned previously, editorial skills and experience are required to compose an effective Viewdata page. Experienced editors are offering IPs their services as Viewdata agents in the same way as advertising agents service advertisers, editors have in fact been recruited by advertising agencies. Editing systems allow an IP to update his section of the database on-line using the full alphanumeric keyboard complete with graphics and other Viewdata facilities. In operation, the systems enable new pages to be composed and entered, existing data deleted and amended often by overwriting, all without interference to the Viewdata service. If desired, the Viewdata computer can also be programmed to undertake packaged calculations of a higher standard than can be performed on a pocket calculator, but not as sophisticated as the computation services available from established computer bureaus.

At the time of writing, the UK Post Office has had to close the list of IP applicants for the public test service when the number reached 160. The 160 IPs have reserved 190,000 Viewdata pages covering some 600 subjects—a short summary is shown in Table II. When a full national Viewdata service is established, the database will be considerably enlarged allowing the number of IPs to be further increased.

Cost to users

Since inception, no charge or increase in license fee has been made to users of Teletext services in the United Kingdom. Due to the relatively modest cost of providing the service, broadcasters have decided for the time being to absorb the extra costs. On the other hand, the price of a color receiver complete with Teletext decoder is currently approximately 120 pounds ($240) or 35 percent more than a set without decoder. Set-top adaptors connected between the antenna and antenna socket are priced at 400 pounds ($800), though due to the additional demodulation/modulation the display quality is somewhat degraded. When decoder IC modules reach production levels of thousands per month, the increment on the set price is expected to be halved, and in time reduced further with increases in volume. The same situation prevails with Viewdata and combined Teletext/Viewdata terminals, except that there is an additional increment of about 15 percent on the set price to cover the cost of the Viewdata modem, but this too will fall with volume production as with the other IC modules. Business terminals with smaller monochrome display tubes are correspondingly cheaper although a full-size keyboard rather than a keypad is generally required.

In the case of the Prestel public trial service, the British Post Office makes the standard unit charge of 3p (6 ¢) for a local call which buys 2-12 minutes according to the time of day. Longer distance calls to other Viewdata centers have proportionately shorter periods per unit charge. Prestel users will have added to this a frame charge which normally varies from nothing to 2p (4 ¢) per single page but can be as much as 50p ($1) depending on the charge made by the IP for the content. Private CUGs usually operate on a subscription basis which incorporates Prestel service levies.

A future need will certainly arise for public terminals at selected sites under surveillance within shopping centers, post offices, libraries, and airports. Pay terminals are under development for this purpose which will either be coin-operated or accept credit cards. At a later date there is likely to be a requirement for free terminals able only to access a restricted section of the database, as well as advertising and ordering. Free terminals could be used for a wide variety of reservation services, e.g., flight, hotel, theatre and restaurant bookings.

On the horizon—telesoftware

Early in 1977 W.J.G. Overington[7] proposed telesoftware, literally "software at a distance", and as the name implies one computer transmits programs to one or more remotely located computers. Overington considered telesoftware in the context of Teletext, but the close relationship between the Teletext and Viewdata systems makes telesoftware also applicable to Viewdata, although the benefits are less apparent. Teletext and Viewdata decoders have a page store which can be utilized as a memory, the TV display constitutes a VDU, and the keypads a data entry device. If a suitable microprocessor with extra memory is now added at a cost of approximately $100, all basic units of a minicomputer are present and contained within a standard TV receiver cabinet. Microprocessors are nothing new to advanced TV receiver design and are already being used to control program selection,

Table II
Some "Prestel" database subjects. The 160 Information Providers have currently supplied 190,000 Viewdata pages, covering some 600 subjects.

Accommodation	Dining Out	Hotels	Professional Recruitment
Advertising	DIY	Housing	Property
Air Travel	Education	Industrial Development	Public Transport
Audio & TV	Electrical Goods	Insurance	Rail Travel
Baby & Baby Care	Employment	Investment	Recipes
Books	Encyclopedia	Law	Scientific Information
Careers	Entertainment	Leisure	Sport
Children's Stories	Finance	Mortgages	Taxation
Clothing & Footwear	Games & Quizzes	Motoring	Tourism
Communications	Gardens & Gardening	Museums	Travel & Transport
Community Services	Guides & Extracts	News	Weather
Consumer Guides	Going Out	Office Equipment	
Credit Cards	Hobbies	Pension Advice	
Currency	Holidays	Places to Visit	

video game operation and other functions.

The Teletext receiver adapted for telesoftware immediately has an interactive capability being able to perform as a local two-way programmed system. Telesoftware bits are presented to the terminal as pairs of standard Teletext characters from a transmitted Teletext page, or if the capacity of a single page is inadequate, from a group of sequential pages. More extensive software could alternatively be built up on audio tape by recording a page changing each Teletext cycle and using the time codes referred to previously as addresses. Later, the recorded telesoftware may be entered into the terminal minicomputer as required. Proprietary telesoftware can be even more rapidly transmitted from a Viewdata center and similarly stored at a terminal. Leisurely interrogation of a terminal would cost almost nothing compared with mounting telephone charges incurred by prolonged dialogue with a Viewdata center.

The applications of telesoftware for information transmission and processing may be said to be limited only by the imagination and the boundaries of practical reality. One constraint that tends to be overlooked is the relatively few words that can be displayed on a data TV page. A hundred or so words is the equivalent to two to three short paragraphs of a newspaper column. While eminently suitable for concise statements, reading anything of length consisting of such brief pages soon becomes tedious. Although computer VDUs display up to 80 characters/row, i.e., double the page capacity of data TV, the words can only be easily read at less than normal TV viewing distance.

The following telesoftware applications have been cited as being suitable for Teletext:

1. *Video games*[8] of a wide variety and varying standards, including animation which will depend more on the complexity of accessories to provide the analog inputs at the terminal than on the software.

2. *Automated education*, especially multiple choice type of question and answer learning, with provision for regular checks on progress.

3. *Small advertisements*, e.g., for used cars and houses, perhaps broadcast at night. Using time code addressing, the terminal would be programmed by the user to switch on, select and store items of interest for review the following morning.

4. *Public information and guidance* on personal problems, e.g., claims, health and tax. On introducing tax changes, a government or local authority would be able to broadcast an updated program. The user, within the hour, could enter his own data and have an immediate assessment of his liabilities. Unlike other computer systems, telesoftware offers a completely confidential dialogue with the terminal.

Viewdata telesoftware techniques are likely to have far-reaching implications for business. Low cost and ease of operation together with telephone network interconnection means that every level of an organization can be equipped with an interactive and intelligent terminal. Within CUGs, daily or even hourly updates of telesoftware from central computer files can be transmitted and stored in terminals at branch offices or even shops to answer clients and customer queries with the latest data. In the other direction, stock and sales data, etc., could be entered at the terminal, accumulated, and automatically transmitted back to central files periodically at maximum data rate, again reducing telephone charges. Above are but a few of the possibilities presented by the telesoftware concept. If data television offers a new dimension for color TV, telesoftware may be said to add a further dimension to data television.

On the outside back cover of this issue are CEEFAX and ORACLE "pages" photographed from the TV screen showing various Teletext features and services. (The pages have been reproduced from 35mm color slides.)

Today and tomorrow

The technical feasibility of Teletext and Viewdata has unquestionably been established, although it must be recognized that many marketing unknowns and other uncertainties remain. Are people prepared to pay the cost of a decoder in a color TV receiver? And then later pay more money for the interactive facilities of telesoftware? Will the purchase price plus the prospect of heavier telephone bills deter the public from Viewdata? Answers to these questions will be determined to some extent by the level of disposable income consumers have available in coming years, always bearing in mind the counter-attractions of new home products such as the video tape and videodisc players. If in due course data television wins the support of mass market, the predominant LSI costs of the hardware are certain to fall dramatically and so enhance demand.

For this reason, Viewdata penetration of the business market appears likely to occur before the widespread acceptance of either Teletext or Viewdata by consumers. Many medium to small enterprises have found purchase or leasing of conventional on-line computer systems beyond their resources. The Viewdata CUG service should meet this need, with aid from software specialists. Larger organizations are beginning to appreciate the advantages of changing to Viewdata compatible formats for in-house computer systems operating from private databases. Direct access will then become possible to the public Viewdata service, in the same way as private telephone exchanges have access to the public switched network.

Well-sited public terminals, analogous to present day phone booths, may turn out to be the most effective way of introducing data TV services to the man in the street. Around the world the growth of data television seems destined at first to be unspectacular, but gaining in momentum as prices fall and people begin to realize that a new visual information medium is entering everyday life offering surprising benefits in convenience and speed over a wide range of novel and useful services.

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R. Mausler

From graphic artist to composite scene—the digital way

How graphics and digital techniques are being combined in a network television news operation to achieve greater flexibility and lower operating costs.

Digital technology is rapidly gaining acceptance as a new tool in the preparation of television programs.

This paper highlights several new uses at NBC, in particular:

1. how it allows the graphic artist to compose more artwork in the short span between news receipt and air time;
2. how combination of character generation and still store equipment speeds up availability and access of titled graphics material;
3. how an almost unlimited slide store library can be maintained at network stations;
4. how many special effects previously obtained by optical and film means can now be obtained instantaneously by electronic means.

Graphics for newscasts

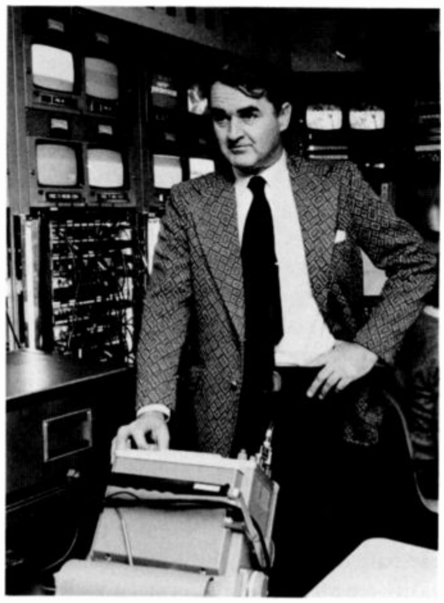
The local, two-hour television news program enlists the creative efforts of an entire graphic arts department of 14 people: a video character generator equipment operator, at least one film transparency equipment (Vizmo) operator, telecine crew, and one or more VTR machine operators, in addition to the normal studio camera and control room personnel. All this is geared up for a brand new program each day. News show people must have few restrictions on thier creative ability to organize, edit, and produce the daily NEWS scene (Fig. 1).

Creation of NBC's two-hour "News Center 4," begins early in the day with an editorial meeting between management and the graphics art director, outlining the possible stories and features for that night's show. So begins the process of researching the files for graphics material, and preparation of the artwork and film slides which are to be integrated into the show as visuals. Preparation time limits the use of these techniques if materials are to be ready before air time.

Typically 40 pieces of artwork converted into 5 x 7 film transparencies with perhaps a half dozen 35 mm slides may be required in a single airing. There may also be an unexpected demand for maps, photos, and other information for late breaking happenings. Titles and other nomenclature must also be added to visual presentations. Titling is done using electronic character generator equipment. For each show about 100 character generator items are prepared and stored on floppy discs awaiting recall for on-air integration with appropriate visuals by the technical director. There may also be as many as 200 or 300 additional titles available as part of an immediate access back-up library. The mixing of film, video tape and studio camera images with titling is done by an insert mode in the studio switcher, based on oral cues between the assistant director and character generator operator.

The graphic artist's new tools

A new approach to integrating the graphic artist's work into the production of a news show may be seen in Fig. 2. This graphics/color camera equipment system is unique. The equipment consists of an Oxberry graphics stand, an RCA TK76



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portable color camera, an ADDA still store remote control panel, camera monitor, studio monitor and still store monitor. The equipment is located within the graphics artist area, not in the studio, a significant factor in the integrated system.

Note, that the still store remote control panel (Fig. 3), in conjunction with the Oxberry stand and color camera with electronic zoom lens, allows the graphic artist complete freedom. The camera may be lowered or raised, or electrically zoomed, and the art material may be closely positioned using the graphics table. The TK76 camera and its mounting on the Oxberry stand are shown in Fig. 4. Transparencies may also be used with an additional attachment to the stand. When the graphic artist has created what he wants, as previewed on the camera monitor, he then stores the material as a video frame in the ADDA still store unit, located elsewhere. At the artist's discretion, several variations in the material may be stored, including semi-animation sequences, by simply using the remote control panel to store each visual frame. Any number of graphics may thus be created and stored on the disc file for the show. The only limitation is in the size of the still store system. For this, a 200-frame capacity was selected. Interestingly, the combining of electronic store control with art creation turns out to be highly motivational for the graphics people.

Titled graphics more available

The News Center 4 program makes heavy use of a video character generator. As noted, about 100 titles are set-up for each show, with another two or three hundred accessible by transfer from a floppy disc. Fig. 5 shows the character generator room. The equipment includes a standard character generator keyboard; an auxiliary control panel used for color graphics, a control panel for computer interfacing and multiple disc drive control; and an ADDS terminal interface for computer operation; edit and generator output monitors, studio monitor, still store monitor, ADDA control panel, waveform monitor and communications units. The character generator equipment system is standard in all NBC New York studios. The still store equipment is new.

Placing the still store and character generator together provides an efficient facility for integrating the titling and graphic artist's work into a finished graphic. The still store operator has available, under his keyboard control, access to all of the stored graphic work previously entered into memory storage by the graphic artist. Therefore, the character generator and still store operators simply compose their respective titling and graphics material, storing the combined result at another memory location. The still store operator can also use the sequence mode to assemble a number of frames for sequential release, limited only by a total of 400 frames, for all sequence groups. To order graphics into a show sequence for presentation, the technical director merely uses an existing "Next" button. This feature simplifies the operation by eliminating cueing and response problems which can otherwise occur.

The still store facility located in the main equipment room is shown in Fig. 6. Note the two disc drives as well as the digital and video processor units. The system uses a disk pack providing 100 frame storage, hence, the two drives provide immediate access to 200 stored frames. Larger systems may be configured (up to 3000 frames) but for this initial graphics system, the choice of 200 available stills is believed to be adequate. It should also be realized that additional stored graphics are available, ad infinitum, by simply changing disc packs. Such a procedure could be used wherein a library access is required, even with a small 200 immediate store system. Disc packs can be changed, from system *down* to system *up*, in about two minutes; which means altogether about five or six minutes for a library change. On-line still access is approximately one-half second.

These new developments in digital slide store and graphics application clearly offer new and improved means for news program production.

The slide store library

Another interesting application of digital slide store technology, in conjunction with the use of state-of-the-art one-inch VTR's has been developed for a library function. The on-line, immediately accessible, slide store library is integrated within a studio facility as part of the slide store capability.

Cost effectiveness

Consider first, that the hardware cost for presenting one digitally stored frame can be estimated roughly at $300, for a 200

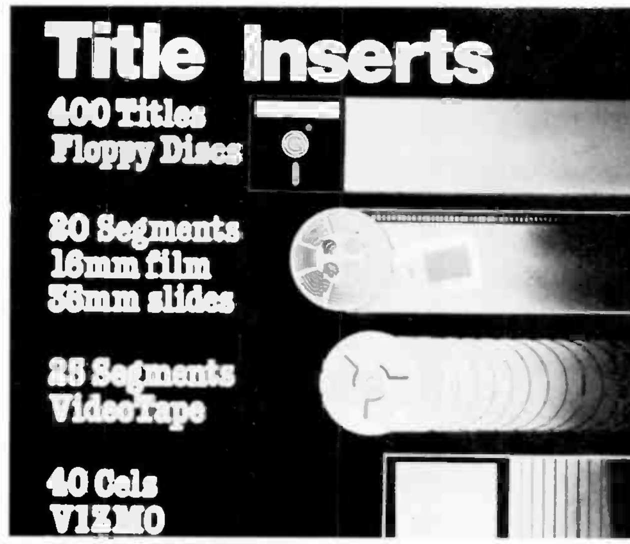

Fig. 1
Tools and techniques in the production of major news show.

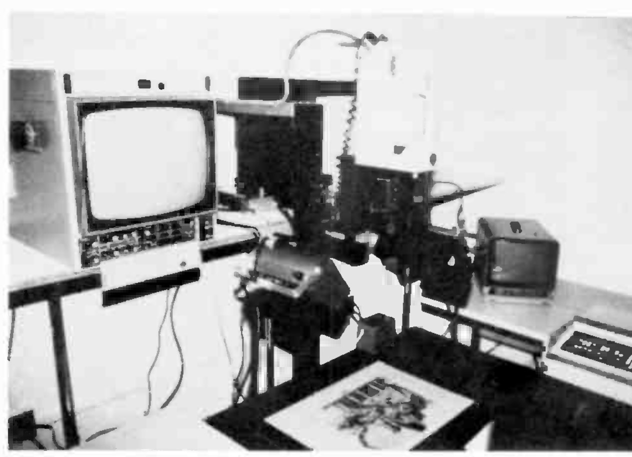

Fig. 2
Unique news show production system. RCA TK76 portable camera (top center); remote control panel (right); graphics stand (bottom).

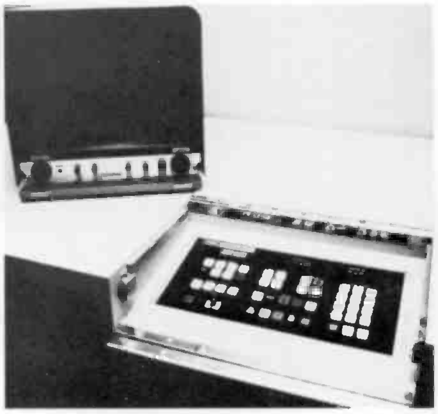

Fig. 3
Still store remote control panel at graphic artist operating position.

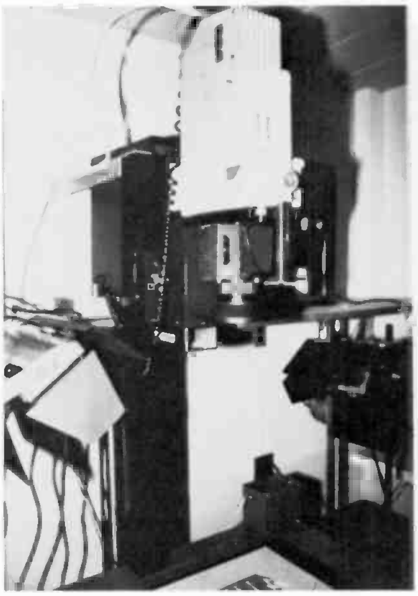

Fig. 4
Mounting of camera on Oxberry stand. Graphic table lights are below stand.

Fig. 5
Character generator room of News Center 4. Character generator keyboard is seen at bottom right; auxiliary control panel (bottom center); still store control panel (bottom left); ADDA terminal interface (top left).

frame store system. Therefore, the incremental cost of one more frame, beyond 200, is substantial. Suppose, however, we could utilize the existing 200-frame store capacity in an almost infinite way, without the problems of using additional disc packs. In that case we should have the best of both worlds, with a virtually unlimited library. How might this be done? Consider the following:

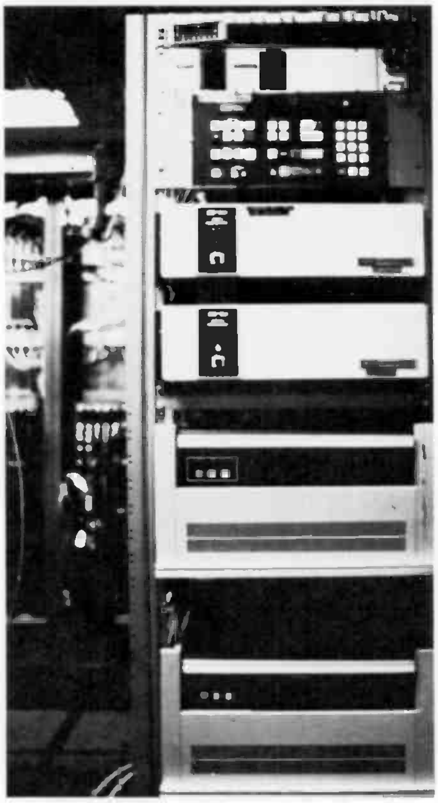

Fig. 6
Still store equipment located in the main control room. Units from top to bottom: ADDA control panel; video processor; digital processor; disc drives.

a. 108,000 frames may be stored at 30 frames/sec on a one hour tape.

b. With a VTR price of about $60k, the cost per frame is about $1.75. (and the frame is first generation)

Therefore, if we wish to organize a practical system, utilizing a one-inch VTR and slide store technology, to provide a cost effective library function, we might organize the system as follows:

a. Record in groups 50 frames each minute.

b. Each frame to occupy one second.

c. Total storage available for a one hour reel: 50 frame-seconds/min x 60 min = 3000 frame-seconds.

(Note: to avoid confusion between frames as defined by SMPTE, and stored frames in this system, a frame-second is defined as that picture recorded on tape from slide store for a period of 1 sec.)

Rapid transfer ability

If we have pre-recorded SMPTE time code on our VTR recording we can then identify each group of 50 frame-seconds by selecting on playback the desired minute

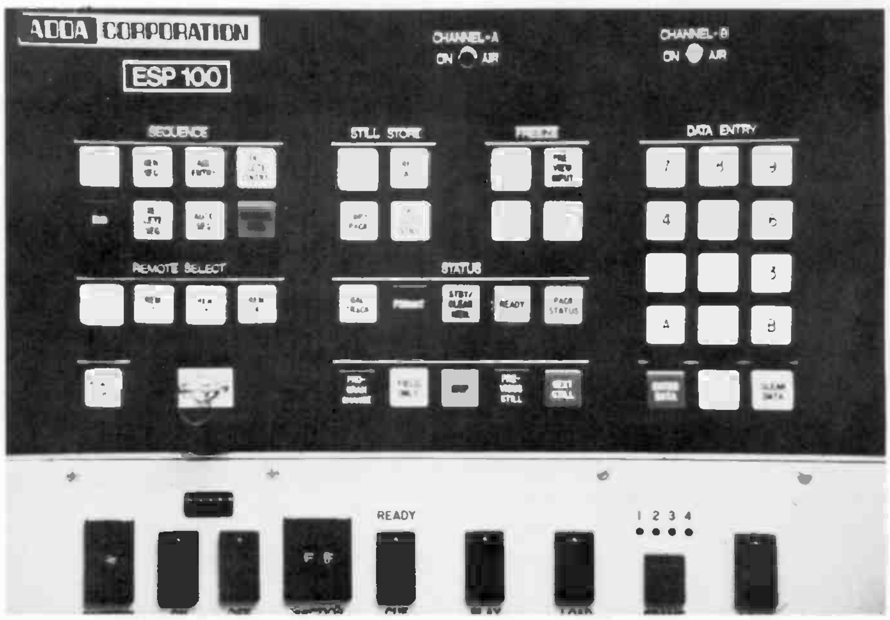

Fig. 7
ADDA remote control panel and library control panel (bottom).

group and playing it back. Thus a playback of the 50 frame-seconds, containing perhaps one or two desired segments, permits an update of the disc memory and a new News sequence for that particular show. Manipulation of the selected frame-seconds (adding and deleting) is done in the ADDA. Completed sequences can, of course, be recorded on the VTR at any time. Just such a system is soon to be incorporated into NBC News operations.

In concept this system conveys another tremendous advantage over past film practice in that an entire library of frame-seconds may be exchanged between network stations by simple VTR playback during periods of network downtime, or between shows. The result of this ability for rapid library transfer means, of course, a virtually unlimited library can be maintained at each station.

We should note that the location of the disc drives and processors may be influenced by space considerations as well as drive noise, library accessibility, and maintenance requirements. We may expect that with a library of 3000 frame-seconds available the disc drives may be remotely located since the need to change disc packs should seldom arise.

Library operation

The library system consists of an ADDA 200 system which can record 200 frames on each disc drive, a remote control panel, and the digital processor for each 200 system. Also included are an RCA TH-100 one-inch VTR, and the special library remote control panel shown with the ADDA remote control panel (Fig. 7), which controls both the ADDA and VTR.

All fundamental components of the system are unmodified and may be used in their normal manner. The one-inch tape requires only a pre-recorded time code and a 1500 Hz tone on two of its audio tracks, together with black burst on the video channel.

The library control panel and ADDA remote control panel are interfaced in such a way that the library facility fully controls all exchanges to and from library tape and disc.

Special effects

The old way

Yet another important area of television production being revolutionized by digital technology is "special effects".

Until the development of digital video effects equipment, scenes consisting of a news personality and perhaps a full size background map have been composed by using Vizmo film projection equipment as shown in Fig. 8. A major show such as News Center 4, may also use a second Vizmo rear projection setup.

Direct lighting of the screen through blue gel filters is used for frequent chroma key inserts of film or video tape into the screen area. Previously, compositing a full frame picture in this mode of chroma key could only be accomplished by use of a separate camera and monitor with its apparent quality limitations. This method of chroma key can be eliminated with a digital video effects system. For the relatively few 35mm film slides required, additional telecine equipment such as shown in Fig. 9 is also required.

The new way

The digital video effects portion of the new system—an electronics system under microcomputer control—is built around a frame synchronizer, and interfaces with the studio switcher. The inclusion of the frame synchronizer makes freeze frame and picture expansion/compression effects possible, in addition to picture push-off/on and

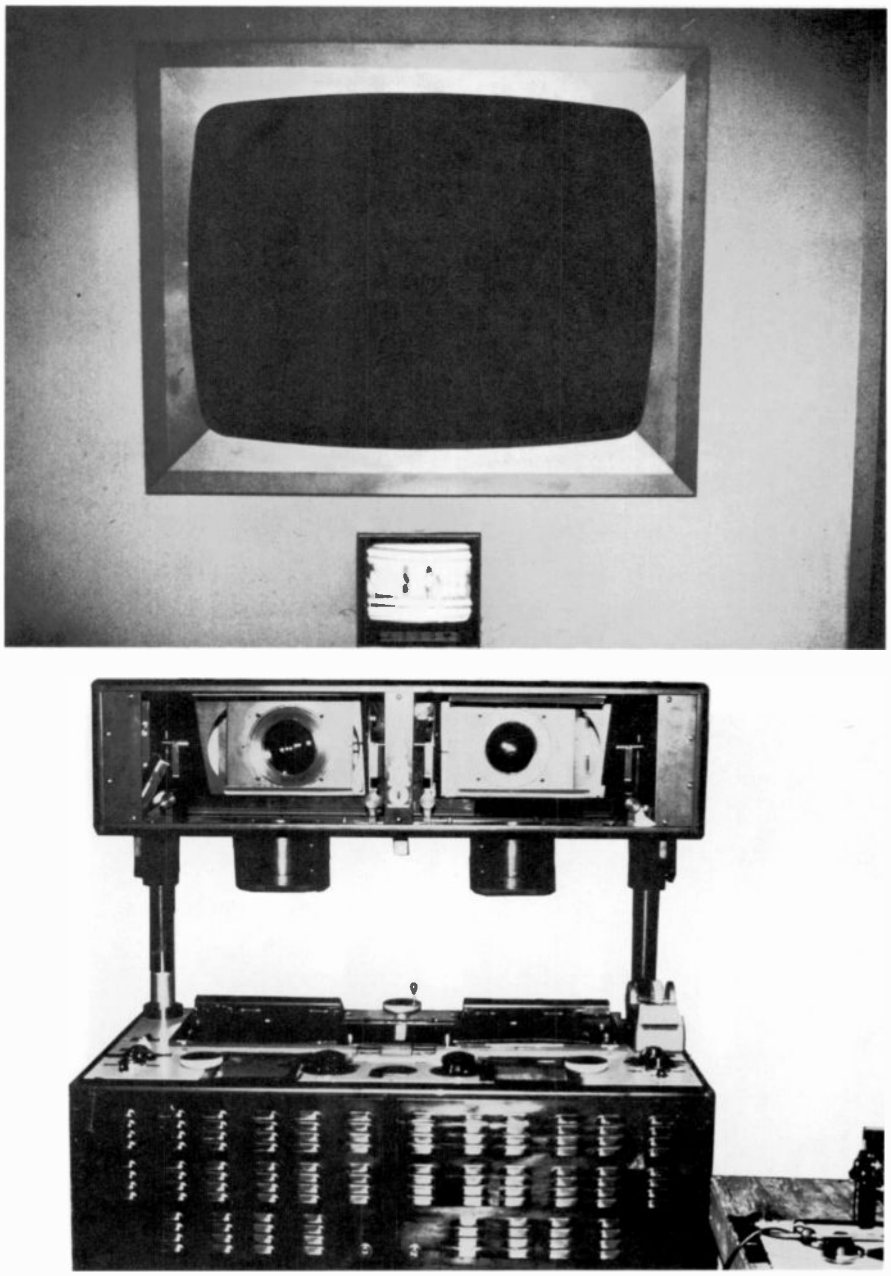

Fig. 8
Film projection equipment commonly used on news shows before digital video effects. Rear projection screen (top); film projector (bottom).

tracking chroma key, as well as many other effects.

While the digital video effects system is effective alone, the production capabilities are substantially enhanced when the digital still store and electronic graphics systems are integrated with it into a complete studio system. Figure 10 shows one example of the graphics-titling on the studio program monitor. The composing was created by using the still store and character generator in the two step process. A close up sequence was also stored so that on a series of closeups the graphic expands to the area of interest which is circled. A view of a compressed insert is shown on two control room program monitors in Fig. 11. The chroma key blue card on its stand may also be noted on the left hand monitor. The digital effects equipment consists of an NEC FS15 frame synchronizer and a Grass Valley DVP15 digital video processor. The equipment is located in the main equipment room where it interfaces with the existing Grass Valley series 1600 studio switcher.

All of the chroma key effects derive from the blue card on the tripod, picked up by the studio camera, as shown in Fig. 12. The inserted effects will follow any positioning of the chroma-key signal, as framed by the pickup camera. Because the frame synchronizer is an integral part of the digital effects system, both synchronous and non-synchronous signals may be freely inserted. The integrated frame synchronizer also permits the creative use of "last story" frame grabbing for effective buffering in News presentations. Tracking chroma key, a major feature of the system, is particularly important on News Center 4. Using this feature, a composite picture with a keyed-in foreground may be zoomed or changed while still maintaining correct picture perspective. Also, many other effects are possible due to the continuous picture compression and microcomputer control of the digital circuits, effects that were possible previously only by optical or optical/film means.

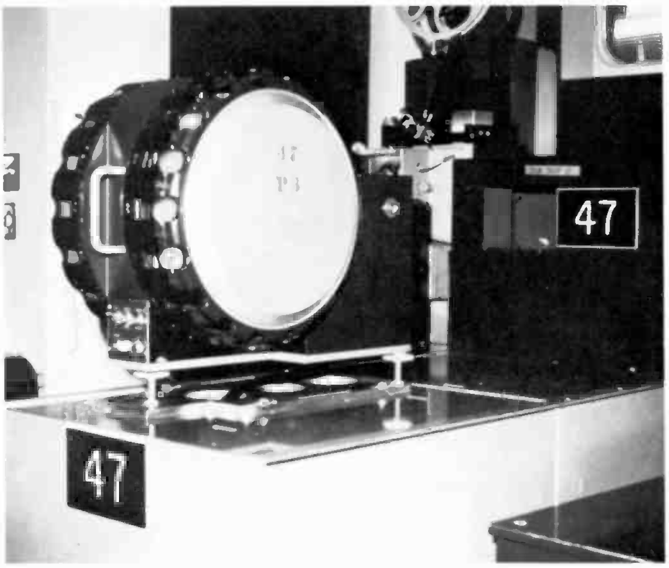

Fig. 9
RCA telecine projector for handling 35 mm slides.

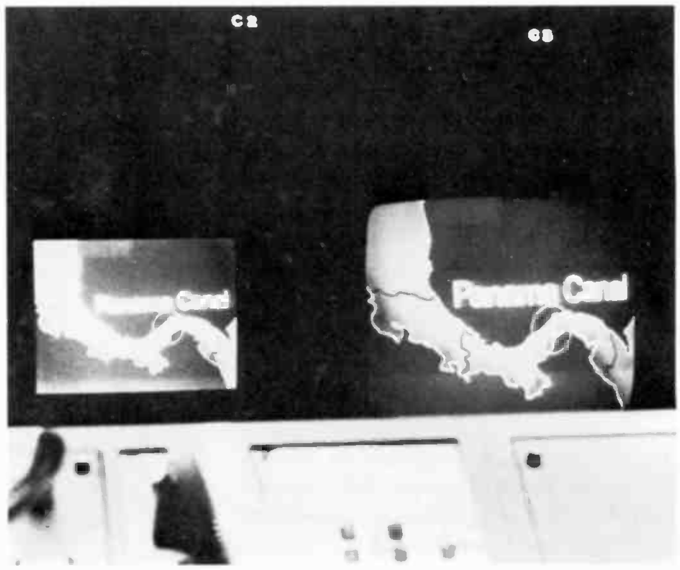

Fig. 10
Titling of graphics on studio control room monitor.

Fig. 11
Compressed picture derived from blue card on tripod (left-hand control room monitor).

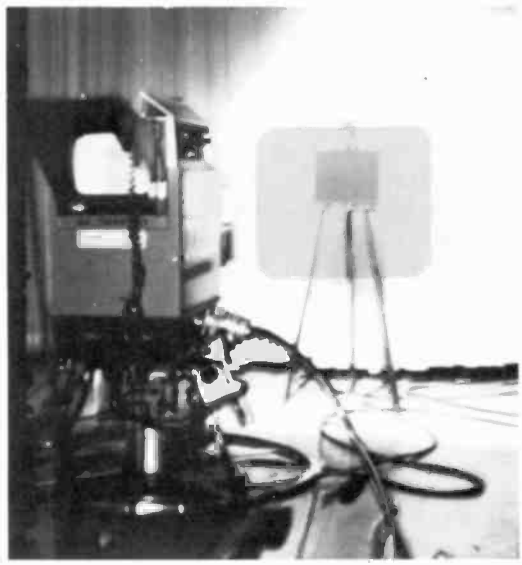

Fig. 12
RCA camera in studio and blue card on tripod for "chroma key".

Dates and Deadlines

Upcoming meetings

Ed. Note: Meetings are listed chronologically. Listed after the meeting title (in bold type) are the sponsor(s), the location, and the person to contact for more information.

JUL 16-28, 1979—**Annual Conf. on Nuclear & Space Radiation Effects** (IEEE-HPS/DNA) Santa Cruz, CA **Prog Info:** J.P. Raymond, Mission Research Corp., P.O. Box 1209, La Jolla, CA 92037

JUL 17-30, 1979—**Joint Intermag and Magnetism & Magnetic Materials** (MAG; AIP) Statler Hilton, New York, NY **Prog Info:** Paul Shumate, Bell Labs, 600 Mountain Ave., Murray Hill, NJ 07974

AUG 5-10, 1979—**Intersociety Energy Conversion Engr** (ED, AES) Sheraton Boston Hotel, Boston, MA **Prog Info:** Dr. J. Plunkett, Montana Energy & MHD Institute, P.O. Box 3709, Butte, MT 59701 (406-494-4569)

SEP 4-7, 1979—**Compcon Fall** (Comp) Washington, DC **Prog Info:** H. Hayman, P.O. Box 639, Silver Springs, MD 20901 (301-439-7007)

SEP 1979—**Instrumentation in Aerospace Simulation Facilities Int'l Congress** (AES) **Prog Info:** Henry Oman, Meetings Coordinator (AES), Boeing Aerospace Co., Box 3999, Seattle, Washington 98124 (206-773-8962)

SEP 10-12, 1979—**Design Engineering Technical Conf.** (ASME) Sheraton-St. Louis Hotel, St. Louis, MO

SEP 16-19, 1979—**Engineering in the Ocean Environment** (IEEE MTS/OEC) Town & Country Hotel, San Diego, CA **Prog Info:** Dr. H. Blood, NOSC, San Diego, CA 92152 (914-225-7275)

SEP 18-21, 1979—**WESCON** (IEEE) San Francisco, CA **Prog Info:** W.C. Weber, 999 N. Sepulveda Blvd., El Segundo, CA (213-772-2965)

SEP 19-21—**AUTOTESTCON** (IEEE, AES) Radisson Hotel, Minneapolis, MN **Prog Info:** A. Thornsjo, Honeywell, Inc., 1625 Zarthan Ave., S, St. Louis Park, MN 55416 (612-542-4811)

SEP 24-26, 1979—**TELECOM 79** (IEEE TAB/COMM) New York, NY **Prog Info:** R. Jerril, IEEE, 345 E. 47th St., New York, NY 10017 (212-644-7861)

SEP 26-27, 1979—**Ultrasonics Symp.** (IEEE SU) Monteleone Hotel, New Orleans, LA **Prog Info:** G.A. Alers, Rockwell International, P.O. Box 1085, 1049 Camino Dos Rios, Thousand Oaks, CA 91360 (805-498-4545 ext. 183)

OCT 1-2, 1979—**First ASSP Workshop on Two-dimensional Signal Processing** (ASSP) Lawrence Hall of Science, Univ. of Calif., Berkeley, CA **Prog. Info:** Dr. Dennis M. Goodman, L 156, Lawrence Livermore Laboratory, P.O. Box 5504, Livermore, CA 94550 (415-422-8186)

OCT 2-4—**Int'l. Electrical & Electronics Conf. & Exposition** (IEEC & E) (Canadian Region) Sheraton Centre, Toronto Canada, Conf. at Automative Bldg. of the Nat'l. Exhibition in Toronto **Prog Info:** IEEE Canada Office, 7061 Yonge St., Thornhill, Ont., Canada L3T 2A6 (416-881-1930)

OCT 2-5, 1979—**First International Conf. on Distributed Computing Systems** (C) Huntsville, AL **Prog Info:** B.D. Carroll, Electrical Engineering, Auburn University, 207 Dunston Hall, Auburn, AL 36830 (205-826-4330)

OCT 3-5, 1979—**5th Int'l Conf. on Very Large Data Bases** (C) National Hotel, Rio de Janeiro, Brazil **Prog Info:** Prof. Stanley Y.W. Su, 500 A Weil Hall, Univ. of Florida, Gainesville, FL 32611 (904-392-2371)

OCT 6-7, 1979—**Frontiers of Engineering in Health Care** (EMB) Denver Hilton Hotel, Denver, CO **Prog Info:** Morton D. Schwartz, Ph.D., California State Univ., Long Beach, CA 90840 (213-498-5102)

OCT 7-11, 1979—**1979 Joint Power Generation Conf.** (ASME/ASCE/PES IEEE) Radisson Plaza Hotel, Charlotte, NC **Prog Info:** Harold K. Couch, Brown & Morrison, P.O. Box 4307, Charlotte, NC 28204 (704-333-0774)

OCT 8-9, 1979—**Symposium on Hardware Descriptive Languages** (C) Palo Alto, CA **Prog Info:** Waldo Magnuson, Lawrence Livermore Labs, P.O. Box L-156, Livermore, CA 94550 (415-422-9550)

OCT 8-10, 1979—**Engineering in Medicine and Biology** (EMB, AEMB) Denver Hilton, Denver, CO **Prog Info:** Eli Fromm, Drexel Univ., Phila., PA 19104 (215-895-2217)

OCT 8-10, 1979—**1979 International Conf. on Cybernetics and Society** (SMC) Denver Hilton Hotel, Denver, CO **Prog. Info:** Dr. James D. Palmer, Adm., Research & Special Programs, Dept. of Transportation, 400 7th Street, Washington, DC 20590 (202-426-4461)

OCT 8-11, 1979—**Electrical/Electronics Insulation Conf.** (EI, NEMA) Sheraton Boston Hynes Auditorium, Boston MA **Prog Info:** J.D. Deacon, Gen'l. Conf. Chairman, P.O. Box 4305, E. Providence, RI 02914 (401-434-2340)

OCT 9-11, 1979—**Electronic and Aerospace Systems Convention** (EASCON) (AES, Wash. Section) Sheraton Nat'l. Hotel, Arlington, VA **Prog. Info:** Herbert D. Benington, V.P. & Gen'l. Mgr. of Metrek Division, Mitre Corp., 1820 Dolly Madison Blvd., McLean, VA 22101

OCT 9-11, 1979—**Electromagnetic Compatibility Conf.** (EMC) Town & Country Hotel, San Diego, CA **Prog Info:** F.J. Nichols, Lectro Magnetics, Inc., 6056 W. Jefferson Blvd., Los Angeles, CA 90016 (213-870-9383)

OCT 17-19, 1979—**Design Automation Workshop** (C) Michigan State University, East Lansing, MI **Prog Info:** Mr. Harry Hayman, P.O. Box 639, Silver Spring, MD 20901 (301-439-7007)

OCT 21-25, 1979—**Electrical Insulation & Dielectric Phenomena** (NRC/NAS & EI) Pocono Hershey Resort, White Haven, PA **Prog Info:** Dr. P.K. Watson, Xerox Corporation, Webster Research Center, 800 Phillips Rd., Webster, NY 14580

OCT 22-23, 1979—**4th Conf. on Local Computer Networking** (C, Local Chapter, TCCC) Marquette Inn, Minneapolis, MN **Prog Info:** Kenneth Thurber, Sperry Univac, P.O. Box 3525, St. Paul, MN 55165 (612-456-3806)

OCT 22-24, 1979—**Second Computers in Aerospace Conf.** (C, AIAA, ACM, & NASA) Hyatt House Hotel, Los Angeles, CA **Prog Info:** Richard Erkeneff, McDonnell Douglas Astronautics Co., Dept. 236, Bldg. 13-3, 5301 Bolsa Ave., Huntingdon Beach, CA 92644 (714-896-4975)

OCT 23-25, 1979—**1979 Test Conf. on Semi-Conductors** (C, IEEE Phila. Section) Hyatt House, Cherry Hill, NJ **Prog Info:** Raymon Oberly, Prog. Chairman, IBM Corp., P.O. Box 100-53X 057, Kingston, NY 12401

Calls for papers

Ed. Note: Calls are listed chronologically by meeting date. Listed after the meeting (in bold type) are the sponsor(s), the location, and deadline information for submittals.

SEP 16-19, 1979—**1979 Fall Meeting—Electronics Div.** (American Ceramics Soc.) "Electronic Ceramics & Energy Conversion," Williamsburg, VA **Deadline Info:** David Hill, TI, Inc., 34 Forest St., MS-10-13, Attleboro, MA 02703 (617-222-2800 ext. 7338)

JAN 7-10, 1980—**14th IEEE Photovoltaic Specialists Conf.,** San Diego, CA **Deadline Info:** 7/15/79 300-word abstract to: Charles E. Backus, College of Engineering and Applied Sciences, Arizona State University, Tempe, AZ 85281

FEB 26-28, 1980—**CLEOS/ICF 80** (IEEE) San Diego, CA **Deadline Info:** 10/1/79 35 word abstract/2-500 word summary to CLEOS, c/o Optical Society of America, Suite 620, 2000 L Street, N.W., Washington, DC 20036

Pen and Podium

Recent RCA technical papers and presentations

To obtain copies of papers, check your library or contact the author or his divisional Technical Publications Administrator (listed on back cover) for a reprint. For additional assistance in locating RCA technical literature, contact RCA Technical Communications, Bldg. 204-2, Cherry Hill, N.J., extension 4256.

Advanced Technology Laboratories

K.R. Andersen
LSI testing—a tutorial—reliability section—IEEE Computer Society LSI Tutorial, Los Angeles, CA (1/22/79)

E.P. Herrmann|D.A. Gandolfo
Programmable CCD tapped delay line—*IEEE Transactions—Electron Devices*, Vol. ED-26, No. 2, pp. 117-122

D.P. Schnorr
Chapter 13: assembly repair—*Printed Circuits Handbook*—Second Edition by C.F. Coombs, McGraw Hill Co. (1979)

W.W. Thomas
Industry views of government specifications and standards—Army Logistics Management Center, Ft. Lee, VA (Defense Specifications Management Course) (1/10/79)

W.W. Thomas
Reliability specification tailoring—'79 Annual Reliability and Maintainability Symposium, Shoreham Americana, Washington, DC (1/23/79)

Automated Systems

R.E. Hartwell
ATE technology applied to the testing of non-electronic devices—University of Lowell Seminar, Lowell, MA (3/15/79)

F.P. McGurk
Design to unit production cost—Cost/Price Analysis Seminar, Waltham, MA (3/21/79)

K.I. Pressman
Financial management of engineering effort—Western New England College, Hanscom AFB, MA (2/6/79)

D.M. Priestley
Automatic test support—Army Aviation Electronics Symposium, Freehold, NJ (3/22/79)

Broadcast Systems

J.J. Clarke|N.P. Kellaway
Operational features of a microprocessor-controlled TV camera—NAB, Dallas, TX (3/25/79)

N.L. Hobson|L.J. Thorpe
A microprocessor-controlled TV camera—SMPTE, San Francisco, CA (2/2/79)

A.C. Luther
Rèmarks on digital recording—SMPTE, San Francisco, CA (2/2/79)

Laboratories

V.S. Ban
Novel reactor for high volume low-cost silicon epitaxy—*J. of Crystal Growth*, Vol 45, (1978), pp. 97-107

A.E. Bell|R.A. Bartolini
High performance Te trilayer for optical recording—*Applied Physics Letters*, Vol. 34, No. 4 (2/15/79)

D. Botez
Near and far-field analytical approximations for the fundamental mode in symmetric waveguide DH lasers—*RCA Review*, Vol 39 (12/78)

G.J. Brucker|A. Rosen|A Schwarzmann
Neutron damage in pin diode phase shifters for radar arrays—*IEEE Transactions on Nuclear Science*, Vol. NS-25, No. 6 (12/78)

C.A. Catanese|J.G. Endriz
The multiplier-assisted discharge: a new type of cold cathode—*J. Appl. Phys.*, Vol. 50, p. 2 (2/79)

R.E. Enstrom|R.S. Stepleman|J.R. Appert
Application of finite element methods to the analysis of stresses in television picture tubes—*RCA Review*, Vol. 39 (12/78)

M. Ettenberg|H.F. Lockwood
Low-threshold-current CW injection lasers—*Fiber and Integrated Optics*, Vol. 2, No. 1 (1979)

M.T. Gale|J. Kane|K. Knop
ZOD images: embossable surface-relief structures for color and black-and-white reproduction—*J. of Appl. Photographic Engineering*, Vol. 4, No. 2 (Spring 1978)

A.M. Goodman|G. Harbeke|E.F. Steigmeier
Optical properties of amorphous and recrystallized SiO_x layers—*Inst. Phys. Conf. Ser.*, No. 43 (1979): Chapter 23

D.M. Hoffman
Operation and maintenance of a diffusion-pumped vacuum system—*J. Vac. Sci. Technology*, Vol. 16, No. 1 (Jan/Feb 1979)

K.M. Kim
Morphological instability under constitutional supercooling during the crystal growth of InSb from the melt under stabilizing thermal gradient—*J. of Crystal Growth*, Vol. 44, No. 4 (11/78)

K.M. Kim
Microdefects in small-diameter silicon crystals grown by the pedestal technique—*J. Appl. Phys.*, Vol. 50, No. 2 (2/79)

C.S. Kim|W.E. Ham
Yield-area analysis: Part II effects of photomask alignment errors on zero yield loci—*RCA Review*, Vol. 39 (12/78)

K. Knop
Diffraction gratings for color filtering in the zero diffraction order—*Applied Optics*, Vol. 17, No. 22 (11/15/78)

J.J. Mezrich
Structure visibility change with contrast reversal—*Vision Research*, Vol. 19, No. 3, pp. 327-333 (1979)

C.J. Nuese
Advances in heterojunction lasers for fiber optics applications—*Optical Engineering*, Vol. 18, No. 1, p. 20 (Jan/Feb 1979)

J I. Pankove|M.L. Tarng
Amorphous silicon as a passivant for crystalline silicon—*Applied Physics Letters*, Vol. 34, No. 2 (1/15/79)

W. Rehwald|A. Vonlanthen
Ultrasonic studies of the structural phase transition in squaric acid—*Physica Status Solidi (b)*, Vol. 90, No. 61 (1978)

C.W. Struck|W.H. Fonger
Transition rates in single-$\hbar\omega$ models—*J. of Luminescence*, Vol. 18, No. 19 (1979) pp. 101-104

J.L. Vossen
Glow discharge phenomena in plasma etching and plasma deposition—*J. of the Electrochemical Society*, Vol. 126, No. 2 (2/79)

Missile and Surface Radar

M.W. Buckley
Project management—IEEE Central Indiana Section, CMO of the Naval Weapons Support Center, Crane, IN (3/79)

S.L. Hazen
Structural mode control in large aircraft (Vu-graph presentation)—IEEE Control Systems Section, University of Pennsylvania (3/79)

W.T. Patton
Microwave design for reliability/availability—the AN/SPY-1A radar—*Microwave Journal* (3/79)

R.J. Rader
Real-time software development—NY Academy of Sciences, New York City, (2/13/79)

S.M. Sherman
Plot your own range-height-angle charts—*Microwave Journal* (3/78)

H. Urkowitz
Reducing straddling losses in detection and estimation by digital interpolation—Electrical Engineering and Science Colloquium, Moore School of Electrical Engineering, University of Pennsylvania (2/1/79)

Mobile Communications Systems

J. Soblak
Impulse noise elimination techniques for mobile communications—*ENTELEC*, New Orleans, LA (3/21/79)

Patents

Astro Electronics

C.A. Berard, Jr.,|J.S. Kinsley
Bilateral energy transfer apparatus—4143282

L.R. West
Ground station data storage system—4139900

Automated Systems

W.J. Hannan
Color image storage and display utilizing holography—4142204

Commercial Communications Systems

J.R. Barkwith
Idle-busy signalling between telephone system and radiophone system—4138595

R.A. Dischert|R.E. Flory
Video signal amplitude registration system—4141040

L.V. Hedlund|A.C. Luther, Jr.
Disc eccentricity compensating system—4138741

L.V. Hedlund|R.P. Fink|D.I. Wright
Disc track servo system—4142209

E.J. Nossen|E.R. Starner
Arithmetic synthesizer frequency generation with reduced phase jitter—4144579

B.M. Pradal
Crystal overtone oscillator using cascade connected transistors—4139826

Consumer Electronics

R.E. Fernsler
Television horizontal oscillator frequency control arrangement for use with tape recorder—4144544

R.E. Fernsler|M.L. Henley
Television horizontal oscillator frequency control arrangement for use with a tape recorder—4144545

L.A. Harwood|E.J. Wittmann
Automatic brightness control circuit employing a closed control loop stabilized against disruption by large amplitude video signals—4143398

J.L. Smith
Magnetizing method for use with a cathode ray tube—4138628

F.R. Stave|L.A. Torrington
Video disc package—4138703

D.H. Willis
Television receiver protection circuit—4145639

Coronet Industries

D.B. Nichols, Jr.
Multi-dye textile dyeing process—4146362

Electronic Component Division

M.R. Freeling|H.J. Wolkstein
RF burst signal recirculation memory system having a diplexed feedback loop—4145691

Government Communications Systems

R.W. Allen|A. Jackson, 3rd
Frequency activated circuit—4145660

M. Packer
Extrudable, non-flowing and non-aqueous solvent soluble hold compound for printed wiring board assembly—4143005

E.R. Starner|E.J. Nossen
Accurate phase-measuring system using arithmetic synthesis—4144572

Laboratories

F. Aschwanden
SECAM modulator—4145711

W.H. Barkow
Deflection yoke with permanent magnet raster correction—4143345

A. Bloom
Electro-optic device—4141627

D.E. Carlson|A.R. Triano, Jr.
C.R. Wronski
Schottky barrier semiconductor device and method of making same—4142195

S.H. Cohen|J.J. Fabula
Process for manufacturing a radiation hardened oxide—4139658

A.R. Dholakia|J. Alexander
Video disc pickup with preplay stylus—4145718

J.G. Endriz
Image display device with optical feedback to cathode—4142123

J. Goel
Method of making a short gate field effect transistor—4145459

L.F. Hart
Apparatus and method for aligning wafers—4141456

E.P. Herrmann
Charge transfer output circuits—4140923

D.D. Holmes
Comb filter apparatus—4143397

H.P. Kleinknecht|J. Kane
Optically monitoring the thickness of a depositing layer—4141780

R.J. Klensch
Range rate measurement—4146890

H.G. Lewis, Jr.
Analog-to-digital converter—4143366

M.J. Lurie
Redundant hologram rocording method employing temporal information signal—4142772

R.S. Mezrich
Switchable depth of focus pulse-echo ultrasonic-imaging display system—4138895

M. Nowogrodzki
Indicating temperature within living tissue—4138998

J.I. Pankove
Solar cell with a gallium nitride electrode—4139858

K.D. Peters|C.H. Anderson
Modular guided beam flat display device—4145633

W. Phillips
Surface acoustic wave device with reduced spurious responses—4142163

J.J. Risko
Two level threshold circuit—4139851

A.D. Robbi
Signal sampling circuit—4143329

A. Rose
Photoconductor for imaging devices—4139796

D.J. Sauer
CCD input circuits—4139784

T.O. Stanley
Flat panel display device—4143296

L.C. Upadhyayula
FET-TELD combination with capacitively coupled output electrode means—4145624

C.M. Wine
Memory type tuning system for storing information for a limited number of preferred tuning positions—4138647

Missile and Surface Radar

J.A. Diciurcio
Voltage level generator using digital integration—4145743

W.T. Patton|N.R. Landry
Short radiating horn with an s-shaped radiating element—4138683

Picture Tube Division

A.M. Morrell
Cathode-ray tube with a corrugated mask having a corrugated hinging skirt—4146816

SelectaVision Project

F.X. Conaty
Video record package—4145726

Solid State Division

A.A. Ahmed
Current mirror amplifier—29910

A.A. Ahmed
Signal translation circuits—4140977

H.R. Beelitz
Decoder circuit—4143359

W.F. Dietz
Regulated deflection circuit—4146823

A.G. Dingwall
Drain extensions for closed COS/MOS logic devices—4142197

W. Hulstrunk
Contact clip—4141028

J.E. Wojslawowicz
GTO bi-directional motor control circuit—4146826

Engineering News and Highlights

Kressel named Staff Vice President, Solid State Technology

Appointment of **Dr. Henry Kressel** as Staff Vice President, Solid State Technology, RCA Laboratories, was announced by Dr. William M. Webster, Vice President. In his new position, Dr. Kressel will be responsible for RCA's integrated circuit research at Princeton and for the RCA Solid State Technology Center at Somerville, N.J.

In 1959, Dr. Kressel started work for the RCA Semiconductor Division, and in 1963, was awarded a David Sarnoff Fellowship to pursue his doctoral studies. In 1966, he joined RCA Laboratories, and in 1969, became Head of the Semiconductor Devices Research Group. In 1977, he was appointed Director of the Materials and Processing Research Laboratories, the position he held prior to his present appointment.

Dr. Kressel is the author of more than 100 published scientific articles on semiconductor lasers (in which field he co-authored a textbook), light emitting diodes, solar cells, transistors, and microwave devices. He holds 25 U.S. Patents. In 1974, he received RCA's highest technical honor, the David Sarnoff Outstanding Achievement Award, for "outstanding research and leadership in the development and advancement of semiconductor devices." Previously, he had received two RCA Laboratories Outstanding Achievement Awards plus a similar award from the RCA Semiconductor Division.

He is a Fellow of both the American Physical Society and the Institute of Electrical and Electronics Engineers (IEEE), and served as President of the IEEE Quantum Electronics and Applications Society.

Promotions

Astro-Electronics

D.A. Aievoli from Engineer to Manager, S/C Project Engineering.

D. Balzer from Staff SYSSCI to Manager, Propulsion SYSS.

M.E. Kavka from Engineer to Manager, Systems Engineering.

Broadcast Systems

D.I. Wright from Principal Member, Engineering Staff to Unit Manager, Engineering Staff.

Consumer Electronics

Robert D. Altmanshofer from Senior Member, Engineering Staff to Manager, Project Engineering.

Paul E. Crookshanks from Senior Member, Engineering Staff to Manager, Project Engineering.

Edward W. Curtis from Senior Member, Engineering Staff to Manager, IEMS Product Engineering.

Dal F. Griepentrog from Senior Member, Engineering Staff to Manager, Project Engineering.

Ronald N. Norley from Member, Engineering Staff to Manager, Component and Liaison Engineering.

Richard Sunshine from Principal Member, Engineering Staff to Manager, Computer Aided and Advanced Mechanical Engineering.

Paul C. Wilmarth from Senior Member, Engineering Staff to Manager, Project Engineering.

Picture Tube Division

Frederick L. Armstrong from Manager, Equipment Design Engineering to Manager, Plant Engineering.

Edward Eaton, Jr. from Member, Technical Staff to Manager, Equipment Design Engineering.

Staff announcements

Consumer Electronics Division

D. Joseph Donahue, Division Vice President, Operations, announced the appointments of **J. Paul Belanger,** Director, Product Assurance; and **Leonard J. Schneider,** Division Vice President, Manufacturing.

Eugene Lemke, Chief Engineer, New Products Laboratory and Engineering Development, announced the organization as follows: **James E. Carnes,** Manager, Technology Applications; **Ronald L. Hess,** Manager, Television Systems Development; **Jerrold K. Kratz,** Manager, Magnetics Engineering; **James A. McDonald,** Manager, Display Systems; **Leroy W. Nero,** Manager, Deflection Sub Systems; **Robert M. Rast,** Manager, New Products Development; and **Richard Sunshine,** Manager, Computer Aided and Advanced Mechanical Engineering.

Larry A. Cochran, Manager, Signal Systems and Components, announced the organization as follows: **David J. Carlson,** Manager, Television Systems Engineering; **Jack S. Fuhrer,** Manager, IF and Baseband Signal Processing; and **Ronald N. Norley,** Manager, Component and Liaison Engineering.

Perry C. Olsen, Manager, Product Design Engineering, announced the following organization: **Robert D. Altmanshofer,** Manager, Project Engineering; **Eldon L. Batz,** Manager, Resident Engineering; **Edward W. Curtis,** Manager, IEMS Product Engineering; **David M. Dew,** Manager, Resident Engineering (Juarez); **J. David Elliott,** Manager, Prescott Engineering; **Robert D. Flood,** Administrator, Cost Reduction; **Robert F. Shelton,** Manager, Resident Engineering (Bloomington); **Elmer L. Cosgrove,** Administrator, Engineering Services; **Paul E. Crookshanks,** Manager, Project Engineering; **Dal F. Griepentrog,** Manager, Project Engineering; **Paul C. Wilmarth,** Manager, Project Engineering; **George W. Yost,** Manager, Engineering Services/Reproduction Services; and **Cecil D. McGinnis,** Manager, Engineering Model Shop.

Arthur Kaiman, Manager, Systems Application, announced the organization as follows: **Melvin W. Garlotte,** Manager, Instrument—Mechanical; **Vernon Morton,** Manager, Ferrite Engineering; and **Arthur Kaiman,** Acting Manager, Chassis—Mechanical.

Laboratories

Henry Kressel, Staff Vice President, Solid State Technology, announced the organization as follows: **Phillip K. Baltzer,** Head, LSI Systems and Applications; **Harold Borkan,** Manager, Special Projects and Products

(SSTC); **Harry L. Cooke,** Manager, Administrative and Technical Operations (SSTC); **Larry J. French,** Director LSI Systems and Design Research Laboratory (SSTC); and **Joseph H. Scott,** Director, Integrated Circuit Technology Research Laboratory.

Nathan L. Gordon, Staff Vice President, Systems Research, announced the organization as follows: **David D. Holmes,** Director, Consumer Electronics Research Laboratory; **Marvin A. Leedom,** Director, Manufacturing Systems and Technologies Research Laboratory; and **Alfred H. Teger,** Director, Advanced Systems Research Laboratory.

Kerns H. Powers, Staff Vice President, Communications Research, announced the organization as follows: **Bernard J. Lechner,** Director, Video Systems Research Laboratory; **Fred Sterzer,** Director, Microwave Technology Center; and **Daniel A. Walter,** Director, Communication Systems Research Laboratory.

David Richman has been appointed Director, Materials and Processing Research Laboratory. He will report to **James J. Tietjen,** Staff Vice President, Materials and Components Research. His organization is as follows: **Vladimir S. Ban,** Head, VideoDisc Materials and Diagnostics Research; **Chih C. Wang,** Fellow, Technical Staff; **Glenn W. Cullen,** Head, Materials Synthesis Research; **Leonard P. Fox,** Head, VideoDisc Applied Process Research; and **Daniel L. Ross,** Head, Organic Materials and Devices Research.

Brown F. Williams, Director, Energy Systems Research Laboratory has announced the organization as follows: **David E. Carlson,** Head, Photovoltaic Devices; **Richard Williams,** Fellow, Technical Staff; **Richard Denning,** Manager, Advanced Power Engineering (Somerville); **Arthur H. Firester,** Head, Process and Applications Research; **Bernard Hershenov,** Head, Energy Systems Analysis; **Charles J. Nuese,** Head, Semiconductor Devices Research; **Jacques I. Pankove,** Fellow, Technical Staff; **Henry S. Sommers, Jr.,** Fellow, Technical Staff; **Brown F. Williams,** Acting, Semiconductor and Optical Materials Research; and **Joseph J. Hanak,** Fellow, Technical Staff.

Appointment of **Charles B. Carroll** as Research Group Head was announced by **Marv A. Leedom,** Director, Electromechanical Research Laboratory. Mr. Carroll is in charge of the Electromechanical Systems Research Group.

Frank J. Marlow has been appointed Head, Digital Video Research. Dr. Marlowe reports to **Bernard J. Lechner,** Director, Video Systems Research Laboratory.

Solid State Division

Fred G. Block, Manager, Central Engineering, announced the organization as follows: **Anthony J. Bianculli,** Manager, Publications & Standards; **Robert E. Brown,** Manager, Data Nomenclature; **John W. Gaylord,** Manager, Computer Aided Manufacturing; **George J. Pulsinelli,** Administrator, Technical Services; and **Harold S. Veloric,** Manager, Materials & Process Laboratory.

Mr. Gaylord, while continuing in his present position under the Director, LSI Systems and Design Laboratory, will for this assignment also take direction from the Manager, Central Engineering.

Richard L. Sanquini, Director, Memory, Microprocessor and Timekeeping Operations, announced the appointment of **Nicholas Kucharewski,** Manager, Design Engineering.

Corporate Engineering

Howard Rosenthal, Staff Vice President, Engineering, announced the appointment of **Gerald B. Herzog,** Staff Vice President, Advanced Technology.

"SelectaVision" VideoDisc

Jay J. Brandinger, Division Vice President, "SelectaVision" VideoDisc Operations, announced the organization as follows: **Harry Anderson,** Division Vice President, Player Manufacturing; **Arthur W. Hoeck,** Director, Finance; **J. Patrick Keating,** Manager, Purchasing; **Robert C. McHenry,** Director, Industrial Relations; **Donald S. McCoy,** Division Vice President, Technical Liaison; **James L. Miller,** Director, Systems and Test Engineering; **Edwin S. Shecter,** Director, Product Assurance; **Harry Weisberg,** Division Vice President, Disc Operations; and **Willard M. Workman,** Manager, Player Engineering.

Mr. Keating will report to Charles A. Quinn, Division Vice President, Materials, Consumer Electronics Division, but will receive business guidance from the Division Vice President, "SelectaVision" VideoDisc Operations.

technical excellence

Harwood

Kosonocky

Wittke

Harwood, Kosonocky and Wittke, New Labs Fellows

Dr. William M. Webster, Vice President, RCA Laboratories, recently appointed **Leopold A. Harwood, Walter F. Kosonocky,** and **James P. Wittke** Fellows of the Technical Staff, in recognition of their outstanding contributions. The designation of Fellow, which was established by RCA Laboratories in 1959, is comparable to the same title used by universities and virtually all technical societies, and is given in recognition of a record of sustained technical contribution in the past and of anticipated continued technical contribution in the future.

Presently the Fellows of the Technical Staff at RCA Laboratories are:

Charles H. Anderson
Kern K.N. Chang
Roger L. Crane
Andrew G.F. Dingwall
Robert E. Flory
James J. Gibson
Joseph J. Hanak
Leopold A. Harwood
Karl G. Hernqvist
Ralph W. Klopfenstein
Walter F. Kosonocky
Simon Larach
Jacques I. Pankove
Dalton H. Pritchard
Allen H. Simon
Henry S. Sommers, Jr.
Thomas M. Stiller
Chih Chun Wang
Paul K. Weimer
Richard Williams
Charles M. Wine
James P. Wittke
J. Guy Woodward

GCS technical accomplishment award

Government Communications Systems has selected **Steve Nossen, Henli Tung,** and **Dean Gumacos,** for a Technical Excellence Team Award. The trio was cited "for the design and development of a self-contained microprocessor digital demodulator for off-loading large array processing equipment."

Fifty-seven RCA scientists honored for research achievements in 1978

Fifty-seven scientists have been given RCA Laboratories Outstanding Achievement Awards for contributions to electronics research and engineering during 1978. **Dr. William M. Webster**, Vice President, RCA Laboratories, Princeton, announced that the recipients of individual awards are:

Christopher Davis, for contributions to the development of the RCA integrated-circuit analysis program.

Dr. William E. Ham, for the development of innovative techniques for the characterization of semiconductor devices and circuits.

Dr. Gregory H. Olsen, for the development of advanced vapor-phase growth methods and improved metallurgical understanding for heteroepitaxial structures employed in electro-optic devices.

Dr. Martin Rayl, for the conception and development of innovative programs leading to a better understanding of the safety and reliability of electronic systems.

Joseph O. Sinniger, for contributions leading to significant LSI component sales for automotive engine controls.

Dr. Robert S. Stepleman, for the development and application of a three-dimensional electron-optics computer program.

Recipients of team awards are:**Bernard D. Alexander, Jack Craft, Norman H. Ditrick,** and **Jack R. Harford,** for contributions to a team effort in the development of novel integrated circuits for color television.

Wayne M. Anderson and **Dr. Kenneth W. Hang,** for contributions to a team effort leading to innovations in the development and processing of glass and ceramic materials.

Brian Astle, Robert E. Flory, William E. Barnette, Robert Dischert, Bernard Hurley, and **Dr. Michael Lurie,** for contributions to a team effort in the conception and development of an automatic broadcast camera setup system.

William H. Barkow, Dr. Josef Gross, Dr. Peter J. Wojtowicz, Charles Horak, Jr., John W. Mirsch, John J. Thomas, and **Robert W. Shisler,** for contributions to a team effort in the development of a novel semitoroidal deflection system for color picture tubes.

Carl W. Benyon, Jr., Dr. Robert B. Comizzoli, Robert H. Dawson, A. Wayne Fisher, Roger W. Stricker, and **Roy G. Turner,** for contributions to a team effort leading to the understanding of silicon integrated-circuit failure mechanisms and to the technology to achieve high-reliability plastic-encapsulated integrated circuits.

John C. Bleazey, Anil R. Dholakia, Richard C. Palmer, and **Raymond L. Truesdell,** for contributions to a team effort in the conception and implementation of innovative approaches to improve the tracking performance of VideoDisc pickups.

Robert R. Demers, Karl F. Etzold, Dr. Arthur H. Firester, and **William R. Haldane,** for contributions to a team effort leading to improvement in the technique for sawing silicon boules, resulting in a significant increase in the quality and output of wafers.

Robert M. Evans, and **Gerald E. Theriault,** for contributions to a team effort leading to automatic alignment of television intermediate-frequency circuits.

Dr. Alvin M. Goodman, Herman F. Gossenberger, and **Dr. Ming L. Tarng,** for contributions to a team effort in the preparation and characterization of polycrystalline silicon layers utilized for the passivation of semiconductor devices.

Richard D. Hassell, Peter A. Levine, Dalton H. Pritchard, Walter E. Sepp and **Donald J. Sauer,** for contributions to a team effort in the application of charge coupled devices in color television receivers.

Henry C. Johnson, Ronald W. Kipp, Daniel D. Mawhinney, and **Robert W. Paglione,** for contributions to a team effort in the development of small cw radars.

Susumu Osaka and **Dr. Minoru Toda,** for contributions to a team effort in the conception and development of a novel and simple electromotion transducer.

R. Craig Skevington, and **Joseph A. Zenel,** for contributions to a team effort resulting in the novel application of voice-processing technology to efficient voice transmission by satellite.

Symposium on Multiprocessor and Distributed Data Processing Systems

The Symposium on Multiprocessor and Distributed Data Processing Systems was held at David Sarnoff Research Center, Princeton, N.J., on March 14, 1979. In his introductory remarks, D. Latham, VP Engineering, GSD, pointed out the tremendous growth in the computer industry: 1977 production ($15.5 billion) was doubled from 1972 and production is again expected to double by 1982. Computer manufacturing and services are expected to reach $64 billion by 1981! Rapid technological advances, shortage of qualified personnel, and plenty of challenges make up the current software picture.

About 80 attendees from many locations followed these presentations:

Taxonomies, J.B. Tindall, Adv. Prog. Dev., GSD.

Phased Array Control Using Multiprocessors, W. Patterson, Software Design and Development, MSR.

Distributed Processing Using Dedicated Microprocessors, H. Hurtado, Software Design and Development, MSR.

Software Impact of Distributed Microprocessors, S.A. Steele, Software Design and Development, MSR.

Distributed Computer System Design For the AEGIS Ship Combat System, R.J. Kosich—AEGIS Computer Program Development, MSR.

Automated Test Program Generation, S. Freeman, Systems Analysis Research, DSRC.

Inter-Process Communication in a Multiprocessor Configuration, W.G. Wong, System Architecture Research, DSRC.

Adaptive Workload Distribution Method, C. Ricker, Software Engineering, GCS.

NAGE—TIROS N Aerospace Ground Equipment System, A. Aukstikalnis, Satellite Programs, AE.

Considerations for Distributed Processing Techniques, J. Mergler, Command & Control Engineering, AS.

Command Language for Man/Machine Interface, J. Mergler, Command & Control Engineering, AS.

Simulation of Surface Ship Defense Against Torpedo Attacks, F. Milillo, Data Systems Engineering, AS.

T.A. Martin, Engineering Staff GSD, planned, organized and chaired this symposium.

Reaction by attendees was very positive, 87% stated that the symposium was useful to them and there was an almost unanimous request to continue software symposia.

For additional information:

- ask for the symposium proceedings (from libraries, chief engineers or attendees)
- contact speakers
- call Tom Martin, TACNET 222-5853.

Professional Activities

1979 Edison Medal Recipient

On the occasion of the recent Electro '79 IEEE meeting in New York, **Albert Rose** was awarded the 1979 Edison Medal. His citation read: "For basic inventions in television camera tubes and fundamental contributions to the understanding of photoconductivity, insulators, and human and electronic vision."

Dr. Rose retired from RCA as a Fellow of the Technical Staff of RCA Laboratories, Princeton, in 1975. He started his "retirement" with the appointment as a Fairchild Distinguished Scholar at California Institute of Technology. Since then, Al Rose has been a Visiting Professor at Stanford University, Boston University, University of Delaware, Hebrew University in Jerusalem and the Polytechnic Institute in Mexico City.

During his 40-year career with RCA, Dr. Rose was involved in important discoveries and applications in photoconductivity and photosensitivity, including basic contributions to the orthicon, image orthicon and vidicon TV camera tubes.

In 1942 when RCA Laboratories was established, Dr. Rose transferred to Princeton from Harrison, N.J., bringing with him a completed model of what later became the image orthicon. At RCA Laboratories he was joined by Dr. P.K. Weimer and Dr. H.B. Law, who had developed what was essentially an electrostatic counterpart of Rose's tube. The three combined their efforts to perfect a new pickup tube with increased sensitivity, greater contrast, improved picture quality, and decreased size and weight.

RCA Engineer, Retired, Elected IEEE Fellow

James S. Hill, who retired from the RCA Service Company, Springfield, Va., in January 1978, was elected a Fellow of the IEEE during 1978.

Mr. Hill's citation reads: "for leadership in promoting the international exchange of electromagnetic compatibility technology and for contributions in the field of measurement of the electromagnetic environment."

While with the RCA Service Company, Mr. Hill prepared an Electromagnetic Compatibility Training Manual for Navair and conducted the training program. He also conducted three aerial surveys of the electromagnetic environment for NASA Goddard. The last one of these was the Airborne Science/Spacelab Experiments Systems Simulation (ASSESS II), a detailed simulation of the Space Shuttle/Spacelab operations conducted at the NASA Ames Laboratory, Sunnyvale, Calif. He has been very active in the IEEE, currently as a member of the Administrative Committee of the Electromagnetic Compatibility Society. He is also chairman of the International Affairs Committee and the Book Review Editor of the EMC Society Newsletter.

Dr. Harold B. Law, retired RCA television pioneer, elected to National Academy of Engineering

Dr. Harold B. Law, a retired RCA Laboratories researcher, is one of 99 engineers recently elected to membership in the National Academy of Engineering of the United States of America. Dr. Law is recognized throughout the electronics industry for the development of the techniques that made possible the manufacturing of the shadow-mask color picture tubes employed in the vast majority of color TV receivers.

The academy cited him for "creative use of materials, and methods to make camera tubes and color picture tubes for television."

On display in the DSRC Library is the first color TV picture tube which Dr. Law and his co-workers used to demonstrate the technical feasibility of the shadow mask in 1950.

RCA Camden engineers cited by NASA for scientific contribution

Two RCA Camden engineers have been awarded certificates of recognition from the National Aeronautics and Space Administration (NASA) for their work in velocity measurement techniques for the Space Shuttle orbiter.

Edward J. Nossen, Staff Engineer, and **Eugene R. Starner,** Senior Engineer, in Camden's Government Communications Systems activity were cited "for creative development of a scientific contribution... of significant value in the advancement of the aerospace technology of NASA."

The RCA engineers' contribution involved development of a special system that adds a velocity-measuring function to the Space Shuttle radio. Working with a Space Shuttle-type radio, they designed a system that measures slight changes in the frequency of the radio waves as the spacecraft and ground stations communicate. The result is a unit that provides a steady flow of information about the craft's position and velocity.

Included in the system is a microprocessor, designed and built by the RCA engineers, as well as signal processor, display unit and related equipment.

Licensed engineers

When you receive a professional license, send your name, PE number (and state in which registered), RCA division, location, and telephone number to *RCA Engineer*, Bldg. 204-2, RCA Cherry Hill, N.J. New listings (and corrections or changes to previous listings) will be published in each issue.

Automated systems

J.B. Perry, Burlington; CA-SF002825

Avionic Systems

J.U. Fahning, Van Nuys; CA-QU5285

Globcom

S.M. Solomon, Piscataway; NJ-13053
NY-38663

Books by RCA authors

Two scientists at RCA Laboratories in Princeton, **John L. Vossen** and **Werner Kern,** are the editors of *Thin Film Processes* recently published by Academic Press, New York. The book is concerned with deposition methods and etching of materials, especially those used to make microelectronic devices in the semiconductor industry. Emphasis is placed on the practical use of the various processes to provide working guidelines for their implementation. Other members of the RCA Laboratories scientific staff who contributed to the book are **Dr. Vladimir Ban** and **Dr. Cheryl A. Deckert.**

A book entitled, *How To Buy Solar Heating Without Getting Burnt!*, authored by **Irwin Spetgang** of GCS, Camden, and **Malcolm Wells** was selected by *Library Journal* as one of a hundred outstanding scientific and technical books of 1978. In its March 1 issue, the publication recommended these books for general library collections. Written for the layman, the book includes chapters on the fundamental principles of solar heating, insulation, contracts, building codes, and tax laws. Also included are names of equipment manufacturers and references to books and periodicals in this field.

Mini/Micro Soldering and Wiring by **Murray P. Rosenthal** of Americom, Piscataway, N.J., has received a special Award of Distinction from the Society for Technical Communication in its 1979 Publications Competition Program. The book, published by Hayden Book Co., explains methods of wave soldering and dip soldering for ICs. It also discusses the best methods of standard hand soldering and wire-wrap soldering, both for industrial applications and for the individual technician.

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*Technical Publications Administrator, responsible for review and approval of papers and presentations.

From the article "Data television — a bright star on the color TV horizon," by K.M. McKee, are shown sample pages photographed from the television home receiver.

New Viewdata communications systems for home and business provide on-line access to a database of useful information via an adapted domestic TV receiver and a telephone line. Teletext systems insert data in the vertical blanking line of TV signals.

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