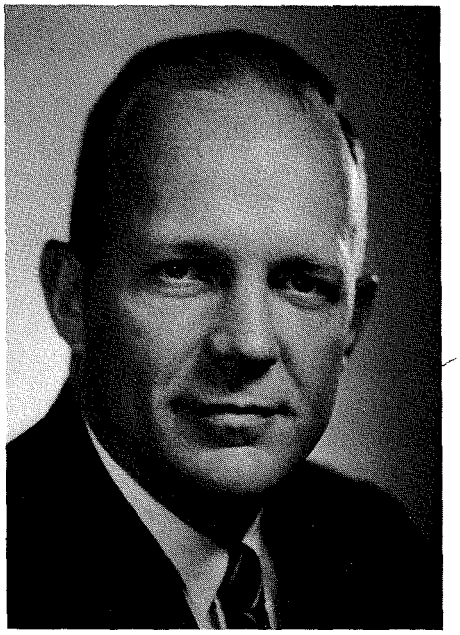
Linear integrated circuits

The decade of the 1960's was a time of remarkable advance in electronics, particularly in information processing systems of great variety. In this period the integrated circuit moved rapidly from an expensive, limited-performance laboratory curiosity to an amazingly capable, inexpensive building block. In the main these integrated circuits were designed to perform digital functions and thus have been used in very large quantities in logic applications. Digital circuits utilize two conduction states, "off" and "on," and are thus relatively simple to design and use compared to circuits in which analog information is being processed. Consequently it has been only recently that integrated circuits capable of operating as linear devices have become available in production quantities.

RCA is an acknowledged leader in the linear integrated circuit field. We have been successful in developing high performance circuits for both consumer and industrial-military applications which are gaining acceptance in many applications where discrete devices had to be used previously. The papers in this issue illustrate the variety of applications now feasible for linear integrated circuits and give an insight into the growth potential in the decade of the 1970's for this rapidly emerging technology.



William C. Hittinger

William C. Hittinger
Vice President and
General Manager
Solid State Division
Somerville, New Jersey

Our cover

. . . shows a wafer of linear integrated circuits manufactured by the Solid State Division in Somerville, New Jersey. The carpenter bee adds color and provides an interesting size comparison; the photo is about two and one-half times larger than life. **Photo credit:** W. Eisenberg, DCSD, Camden, N.J.

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• To disseminate to RCA engineers technical information of professional value • To publish in an appropriate manner important technical developments at RCA, and the role of the engineer • To serve as a medium of interchange of technical information between various groups at RCA • To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions • To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field • To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management • To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

Contents

editorial input

acronyms anonymous

People generally agree that acronyms are bad form—other people's acronyms, that is. When someone gives birth to an acronym that they think is particularly "cute," their parental pride often outweighs their consideration for others as they push their weak-kneed offspring to the forefront at every possible opportunity.

Recently, we received a letter from Irv Seideman of the Astro-Electronics Division which called our attention to a particularly knotty problem in integrated-circuit technology (the theme of this issue):

> "At the moment, I am struggling with CMOS (and PMOS). This I have seen also as COS/MOS, COS-MOS. Next comes SOS (silicon-on-sapphire) which, in combination, could become CMOS SOS, CMOS-SOS, C-MOS-SOS, etc., etc. MOS also is shown combined with Al_2O_3, which could be Al_2O_3 MOS, or also Al_2O_3-MOS. What would a chemist think? And should MOSFET be MOS FET or FET MOS, MOS-FET, or MOS/FET?"

In subsequent discussions, Irv suggested that one solution might be to form an AA (acronyms anonymous) organization. In this way, whenever an engineer feels the uncontrollable urge to coin an acronym, he could make a telephone call and all available members would come over and drink with him until the urge goes away.

As appealing as Irv's solution sounds, we feel that a more formal, organized approach should be followed. Our recommendation is to form a Committee for the Liquidation of Acronyms (CLA), which would be headed up by a Director (CLAD) and several Managers (CLAM's). Each manager would have the support of his own Staff Secretary (CLASS)—naturally.

Probably the first order of business would be to state CLA's Purpose (CLAP), its National Goals (CLANG) and its International Mission (CLAIM). Since defense work appears so prominently in today's technical literature, CLA will also have to establish its own Military Policy (CLAMP).

Looking slightly to the future, a Standardization Policy (CLASP) will be established, and several subcommittees will be formed: there probably will be a Writer's Subcommittee (CLAWS) and—for the first time anywhere—a United Subcommittee of Editors (CLAUSE).

But we should not expect that the entire movement will be without its problems. There will undoubtedly be factions and splinter groups vying for supremacy; one could easily envision a radical group becoming disenchanted with the nonviolent approach to reform, calling themselves the CLA Militant Brotherhood to Abolish Knotty English (CLAMBAKE).

Perhaps, the ultimate simplicity in communication will be achieved only through drastic measures such as the CLA Proposal To Reject and Abolish Prose (CLAPTRAP).

Future issues

The next issue of the *RCA Engineer* features command and control equipment and techniques. Some of the topics to be discussed are:

Airborne Data Automation

New shipboard internal communications systems

Human factors in command and control systems

Minuteman reliability assurance

Command and control equipment

Stepper motors—design and selection

Threshold logic

IC voltage regulator

Minicomputers in manufacturing

Discussions of the following themes are planned for future issues:

RCA engineering in New York

Consumer electronics

Displays, optics, photochromics

Computers: next generation

Mathematics in engineering

Advanced Technology Laboratories

The linear integrated circuit market

D. P. Heacock | J. S. Lempner | D. M. Griswold

In 1970, linear integrated circuits will make a major penetration into a broad variety of new markets. The industrial and military markets will be served by a variety of relatively simple "building-block" circuits which supplement and support more complex operational amplifiers, power control subsystems, and gain-block elements; the flexibility offered by combinations of these elements permits the utilization of linear IC's in both high and low volume applications. The consumer market will experience a trend toward sophisticated and complex IC's which will satisfy user goals of value, performance, and reliability. In each market, RCA has significant strength. This article illustrates the increasing utilization and importance of linear integrated circuits in both areas.

The Engineer and the Corporation

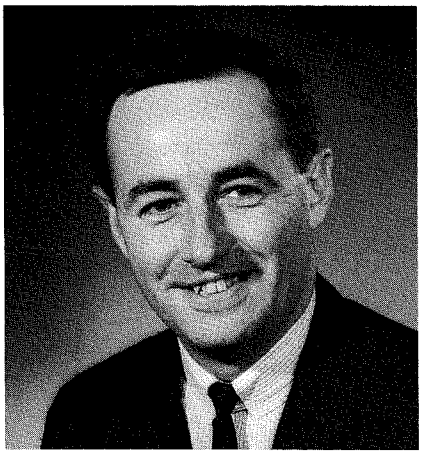
THE DEVELOPMENT OF LINEAR IC'S lagged behind the natural application of integrated circuits to the volume digital market. Large quantity utilization of individual digital circuits were both an excellent vehicle for integrated circuit introduction and a necessity for the growth of the computer industry. Advances in technology and the fast expansion of the integrated circuit industry have resulted in a growing list of unique linear integrated circuits.

The non-consumer market

Industrial and military linear IC's commonly referred to as "non-consumer" can be placed in six basic categories:

1) Differential amplifiers,
2) Operational amplifiers,
3) High-gain wide-band amplifiers,
4) Arrays,
5) Power-control circuits, and
6) Special-function circuits.

Although many non-consumer applications require a relatively low volume of product, techniques had to be found to supply integrated circuits for those applications which would benefit from the reliability and logistic simplicity which IC's had already brought to large-volume markets. The fundamental problem was to provide cost-



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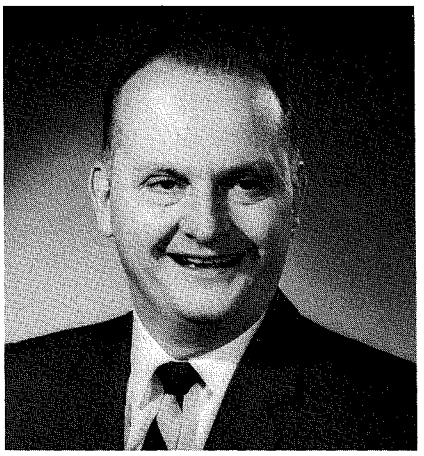
received the BSEE from Ohio State University in 1957. He joined RCA in June 1957 on the Corporate Engineering Training Program. In 1958, he became a field engineer in the Semiconductor Division. He served as a field engineer in Dallas, Chicago, and Indianapolis sales offices until May 1967 at which time he joined the signal marketing department with responsibility for consumer linear integrated circuit marketing.



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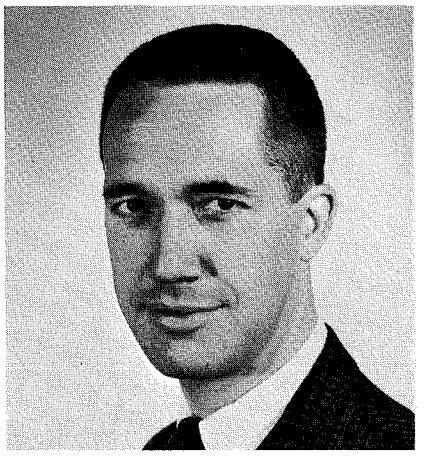
received the BSME from Rutgers University in 1941 and the MSEE from Stevens Institute of Technology in 1946. In 1941 he was employed by RCA as an engineer in the Test Engineering Group of the Electron Tube Division. He later transferred to the Application Laboratory, and in 1953, he became Manager of the Receiving Tube Application Laboratory. He joined the Corporate Engineering Staff in Camden in 1956. In 1969 he became Manager of Product Planning for the Consumer Products Department of the Semiconductor Division at Somerville. He has since been Product Marketing Manager for various solid state products. Mr. Heacock is a member of Tau Beta Pi and Phi Beta Kappa and is a Senior Member of the IEEE.



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graduated from Drew University in 1951 and joined RCA as an engineering trainee. He was assigned a variety of semiconductor engineering assignments in test engineering and industrial applications. In 1958, he became manager of the Semiconductor Rating Laboratory at Somerville. He became Manager of Test and Reliability Engineering in 1961. From 1962 to 1967, he was a Senior Engineer in the Consumer Applications Department with responsibility for evaluation and applications work related to the development of the MOS Field Effect Transistor. In 1967, he transferred to the power transistor applications department. In 1968 he moved into his present job in marketing. Mr. Griswold is a member of IEEE and has served on various semiconductor standardization committees of the IEEE, EIA and IEC.

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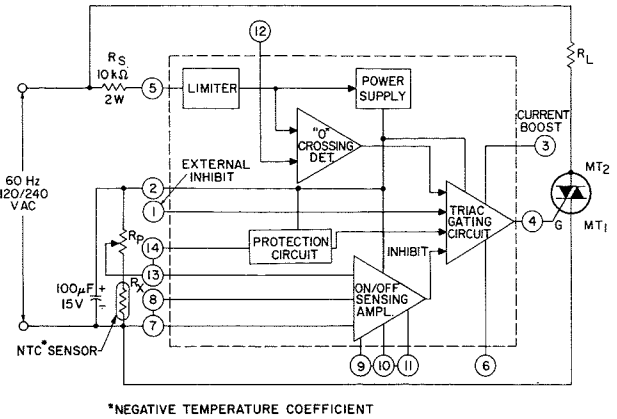


*NEGATIVE TEMPERATURE COEFFICIENT

Fig. 1—Functional block diagram of thyristor control circuit.

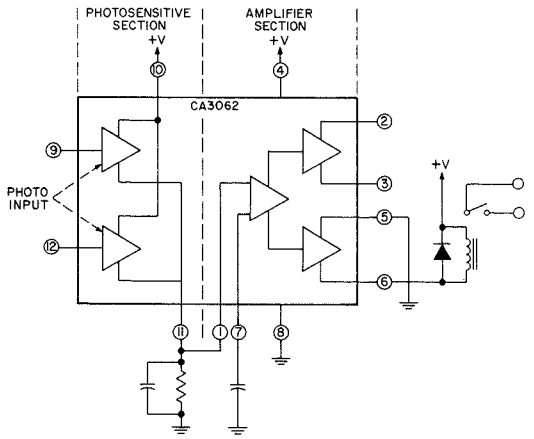


Fig. 2—Light operated relay using CA3062.

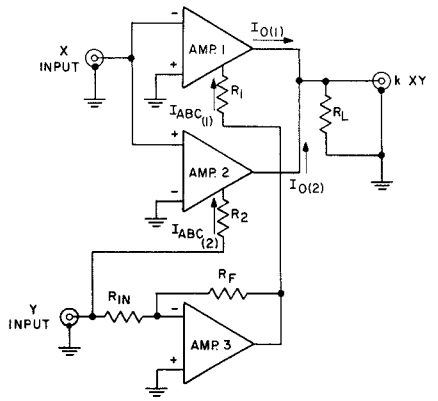


Fig. 3—Four-quadrant multiplier circuit using the CA3060.

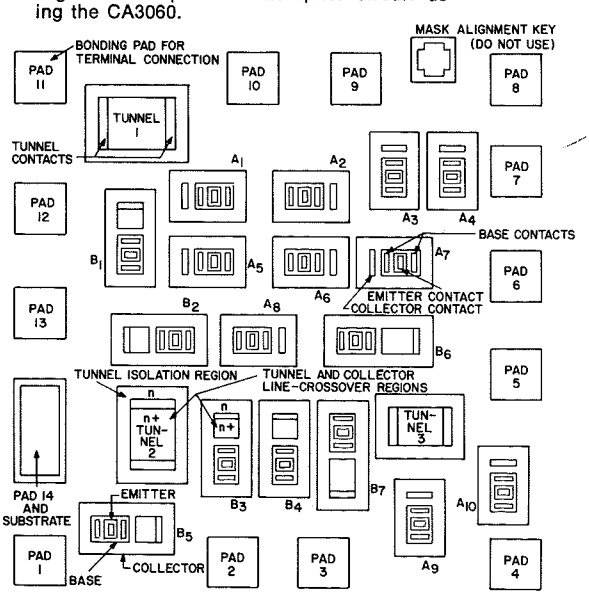


Fig. 4—RCA custom design array.

effective circuits to many different low-volume applications, when none of these applications could individually justify the cost of a special design effort.

Initial solutions to this problem have resulted in the components industry providing to the equipment designer two fundamental kinds of circuits: the *building-block* circuits and the *multiple-application* complex circuits.

The building-block circuits are represented by most of the differential amplifiers and arrays. These are simple circuits which can be combined by the user in a variety of ways to perform a number of different functions. The building blocks may comprise an entire system or may perform the level shifting and peripheral circuitry surrounding the more complex devices. The multiple-application complex circuits are typically more sophisticated than the building-block circuits but perform some function which has common utilization in many equipments. In this category are the high-gain wideband amplifiers, operational amplifiers, and certain special-function circuits such as voltage regulators. Because of the flexibility of the building-block circuits and the improving availability of certain complex circuits, the equipment manufacturer can now utilize an increasing variety of product in his new equipment designs. In turn, the integrated-circuit manufacturer has sufficient production volume by type to permit product pricing which represents true value to the user.

Over the past year, RCA has introduced a number of new monolithic IC's, several of which fall into the multiple application category. Four of these are discussed to illustrate the variety of circuits that are becoming available and the unique characteristics which the linear IC brings to the circuit designer.

CA3059 zero voltage switch

All thyristors (SCR's and triacs) require some type of circuitry to provide the necessary gate trigger pulse to initiate the conducting or ON state. The RCA CA3059 (shown in Fig 1) is a thyristor control circuit which provides the required gate trigger pulse only when the alternating line voltage is passing through zero *and* the external sensor circuit exceeds a threshold value (compared to the built-in reference). This minimizes or eliminates the radio frequency interference normally caused by thyristors when they are triggered into conduction at other than zero line voltage. The CA3059 also has an automatic shutdown circuit which functions in the event of any failure in the external sensor and a built-in circuit (compatible with T^2L logic levels) which can inhibit the normal gate trigger pulses. This latter feature makes the CA3059 ideal for use with logic-controlled incandescent light displays.

CA3062 photosensitive IC switch

The RCA CA3062 illustrated in Fig. 2 combines a photodetector, amplifier, and two high-current switches on a single chip of silicon. One of the 100-mA switches can be used for "normally-OFF" operation while the other switch serves the "normally-ON" function. The photodetector is electrically independent so it can be either directly coupled or capacitively coupled to the amplifier section to suit particular needs. The hermetically sealed package has a flat lens lid.

The CA3062 is characterized for direct relay, lamp, or triac drive in such ON-OFF applications as counting, sorting, cutting, and intrusion detection. With appropriate changes in the operating conditions, it also has interesting possibilities for analog applications.

CA3060 triple operational transconductance amplifier

The operational transconductance amplifier (OTA) represents an entirely new type of operational amplifier. Its output impedance is extremely high so that its output current is primarily a function of its differential input voltage—hence, a transconductance amplifier. The operating transconductance is a linear function of an external bias current over an extremely wide dynamic range.

The RCA CA3060 can be used as a conventional operational amplifier, as a fine four-quadrant multiplier (see Fig. 3), as an active filter element, or as an extremely low-power-consumption amplifier

Custom linear IC planner

Another circuit developed by RCA to assist the alert equipment designer is

the new custom linear IC array. The basic array (shown in Fig. 4) consists of 17 transistors which can be interconnected in many different ways by varying the metallization mask configuration to accommodate special circuit requirements. This IC is available in several popular metal, ceramic, or plastic packages and provides the low-volume user with a new and economical design flexibility. To further aid the designer, a guide booklet defining design and layout rules, basic chip diagrams, packaging alternatives and transistor design data is available. Confining changes solely to the metallization pattern means that a minimum amount of engineering and manufacturing effort is required to provide a custom linear integrated circuit array that meets the design and economic objectives of specialized industrial applications.

The future of industrial linear IC's

The utilization of linear integrated circuits in the industrial and military market is growing daily as component manufacturers introduce a broad variety of cost effective linear IC's. Adding to fundamental cost effectiveness are the benefits of higher reliability, improved manufacturing logistics, unique performance, and weight and volume reductions. For optimum utilization of this powerful IC technology, equipment designers and component designers must work as a team. Typically, unique requirements in each must be modified to arrive at the most economical solution for total performance. Although special low-volume

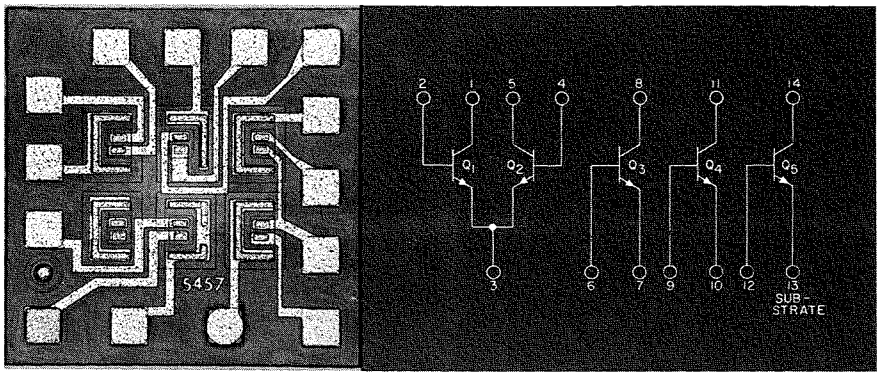


Fig. 5—An example of a minimum-complexity linear IC, the CA3046 transistor array showing the pellet and the circuit diagram.

applications requiring custom design at premium cost will always exist, the more common circumstance will call for cooperative and creative effort by manufacturer and user to establish appropriate economic solutions. This approach is becoming increasingly evident today and is setting the pattern for broad utilization of linear IC's in the 1970's. It will simultaneously provide powerful tools for the equipment designer and a promising business for the IC manufacturer.

The consumer market

Although linear IC's did not penetrate the consumer market as rapidly as was earlier predicted, there is evidence now that usage will accelerate rapidly during the next few years. In the TV segment of this market, for example, only about half of the domestic TV manufacturers used IC's in their 1969 production instruments; whereas, in 1970 nearly all manufacturers can be expected to use at least one or two IC's in a portion of their line. Three major reasons for the anticipated upsurge in TV are:

1) *The current efforts by many of the major manufacturers to either maintain or return the assembly of such equipments to domestic soil.* Integrated circuits, in their current state of technology and cost effectiveness, can be expected to contribute significantly to savings in instrument assembly, alignment and re-work expenses, as well as the many other "intangible" expense savings that also become significant when the majority of small-signal functions of the instrument become integrated.

2) *The current emphasis on ease and simplicity of serviceability.* Most manufacturers feel that modularization, in one form or another, will significantly reduce the problems now facing the radio and TV service trade. And IC's, of course, are ideally suited to modular instrument construction concepts.

3) *Availability of multiple* IC *sources.* Even though different manufacturers' IC's are not always directly interchangeable, a good many are functionally equivalent. Television manufacturers, by utilizing the modular concept, are able to design interchangeable modules, thereby minimizing the risks of a single IC source.

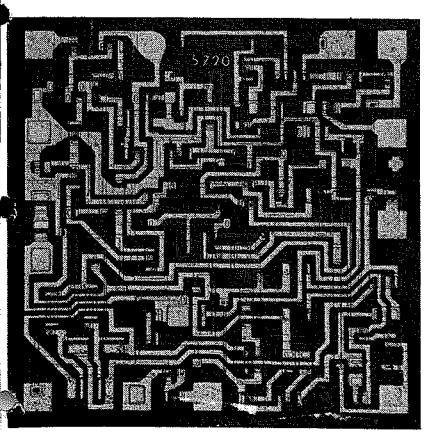
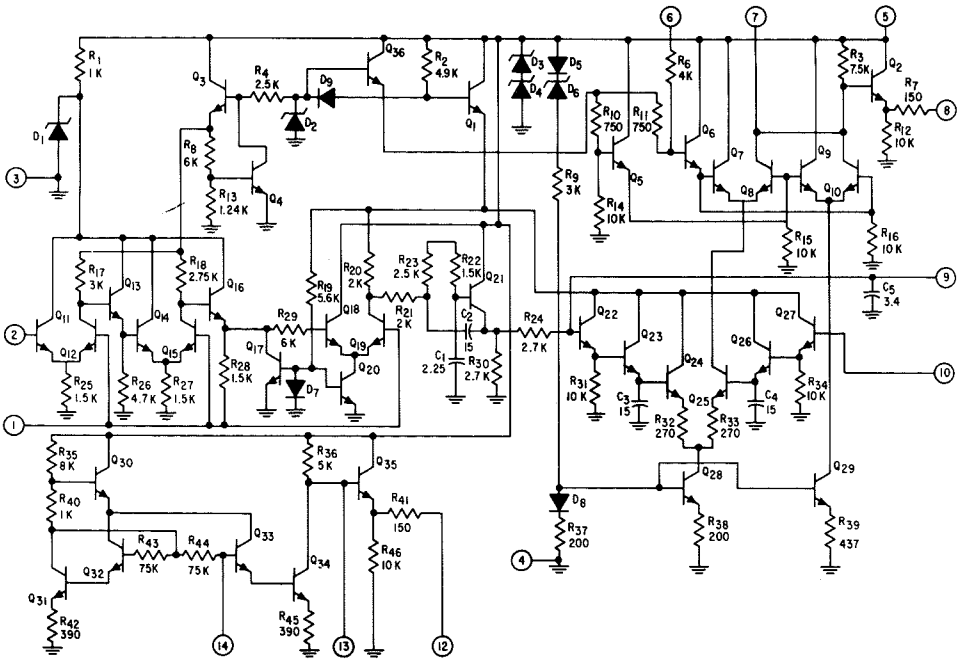


Fig. 6—An example of a high-complexity linear IC, the CA3065 TV sound system showing the pellet and the circuit diagram.



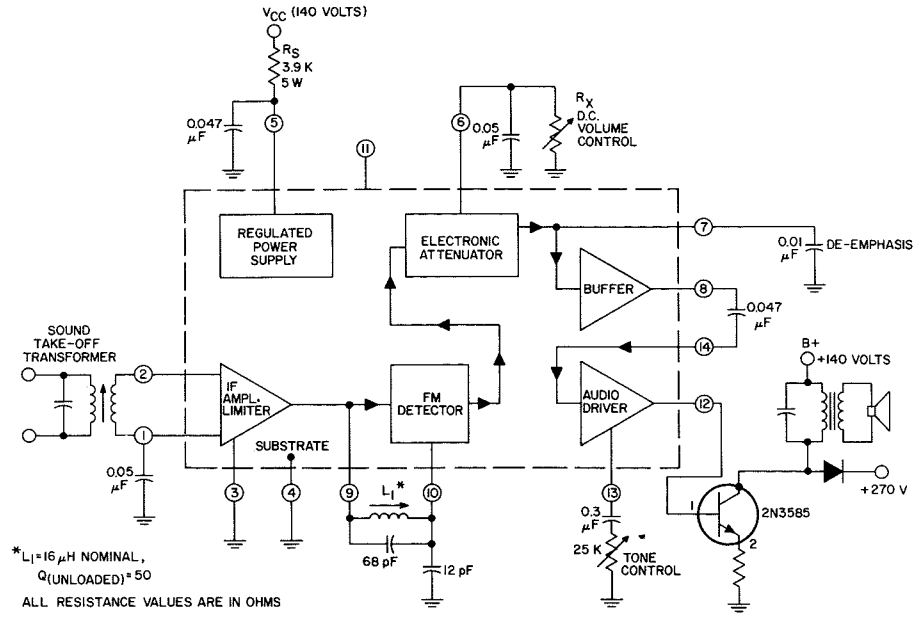


Fig. 7—CA3065 in a typical TV sound system.

All major manufacturers of linear integrated circuits now offer a broad product line capable of providing many functions. And in this breadth of products, circuit complexity can vary from extremely simple pellets containing perhaps only a few active devices (such as the transistor array illustrated in Fig. 5) to an extremely complex subsystem (such as the CA3065 TV sound system shown in Fig. 6). The CA3065 pellet contains 35 transistors, 9 diodes, 46 resistors and 5 capacitors (95 total components), and circuits are currently in development (for consumer market applications) that contain over 300 components per monolithic pellet.

Future of IC's for the consumer market

The IC's greatest promise for the consumer market is in reliability improvement and systems cost reduction. Because the anticipated production volume is large, special-function circuits can be expected to dominate the major portions of this market. The IC can be designed specifically for a particular application or group of functions, whereby the uniqueness of monolithic design can be utilized to its fullest extent to minimize the external components needed to complete the system, particularly those components that require alignment or adjustment for optimum instrument performance. An example of such an IC is the CA3065 TV sound system mentioned previously where, as can be seen by Fig. 7, only 12 components in addition to the IC are required for the entire sound system of a typical TV receiver (excluding the output transformer and speaker). Even the cost of shielded cable (and its associated labor and expense) to and from the volume control has been eliminated. Now the volume control acts merely as a DC-bias adjustment for the active attenuator section of the IC. This electronic attenuator is particularly adapted for, and contributes most significantly in, a remote-control receiver, where the costly geared motor and motor relay are replaced by electronic components such as an MOS-capacitor memory module. In that case, the DC voltage stored by the memory module can be applied directly to the IC.

In the USA alone, the conventional segments of the consumer electronics market (TV, home and auto radio, phonographs, and tape recorder/players) represent ultimate annual IC sales of well over 100 million units. An additional potential of nearly 200 million units exists in those segments of the market that to date have been largely considered to be mechanical or electro-mechanical—e.g., automotive control systems, appliance control systems, clocks and timers. And if one were to speculate even further into the future, applications, such as personal communications systems, home "computers," and control systems might add another 300 million units to the ultimate annual sales potential.

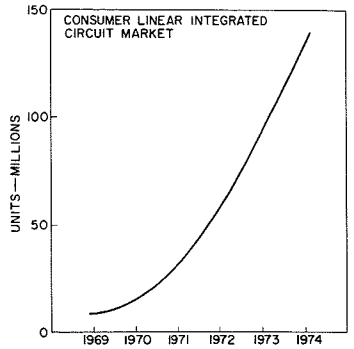


Fig. 8—Anticipated growth rate of linear IC utilization in the USA consumer market over the next four years.

Fig. 8 illustrates the anticipated growth rate of linear IC utilization in the USA consumer market over the next four years. In addition, the international market can be expected to be at least equivalent to domestic usage.

The current trend has been toward more complex IC designs, and that trend can be expected to continue in the future. Because greater complexity is generally associated with more contributed IC value, and because improvements in technology continually reduce the cost penalty for the additional pellet area required, IC complexity in the next few years will probably be restricted mainly by package limitations. Ultimately, with the rapid advance in sealed-junction beam-lead technology that is now taking place, one can envision a compatible combination of monolithic and hybrid techniques wherein a ceramic substrate is utilized as the interconnect mechanism for several silicon IC pellets. Thus the need for the conventional IC package is eliminated and the monolithic pellet complexity becomes primarily a function of pellet cost.

Integrated circuits represent an exciting challenge to the consumer electronic system designer. Unique utilization of monolithic techniques opens the door, for example, to improved system performance or additional system features which may not be economically or technically practical using discrete components. Totally new and novel mechanical and styling concepts can emerge as a result of innovations in the electronics portion of the equipment. But most important to the consumer market is the reduction in cost and the enhancement in reliability made possible by total system integration.

Transistor circuits: discrete and integrated

Dr. R. B. Schilling

Editor's note: The Continuing Engineering Education (CEE) program was developed to meet the specific needs of practicing engineers in RCA divisions. This special industry-centered program provides courses that are necessarily different from the conventional graduate-level courses that are theoretically oriented toward the needs of young men working toward engineering degrees.

This article presents an in-depth look at the scope, structure, teaching philosophy, and content typical of most CEE courses. This first paper of a series is based on a course entitled Transistor Circuits: Discrete and Integrated by Dr. Ronald B. Schilling; it is particularly relevant to the present issue on linear integrated circuits because Dr. Schilling presents a nine-transistor IC operational amplifier as an example of the analysis technique used in the course.

An earlier article [Dr. J. M. Biedenbach, RCA ENGINEER, Vol. 15, No. 3, Oct.-Nov. 1969] described the general objectives, format, and curriculum of the CEE courses. More than 35 practical engineering courses are presently offered, and several more will be available in the near future. For more information on CEE courses, write to Engineering Educational Programs, Corporate Engineering Services, RCA Building 2-8, Front and Cooper Sts., Camden, N.J. 08102.

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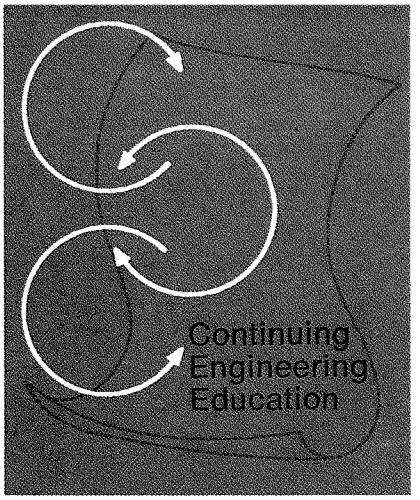
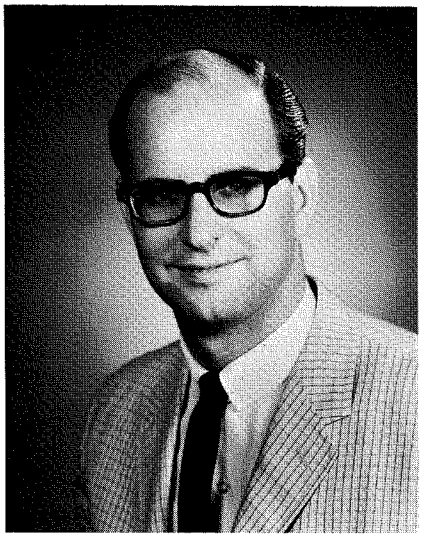
THE PRIME OBJECTIVE of this course is to provide insight into the analysis and design of discrete and integrated electronic circuits. The course starts with a review of basic circuit techniques followed by a discussion of diode and transistor circuits. Included are Thevenin's theorem, superposition, voltage and current division, and impedance reflection. The concepts of DC and AC load lines along with large-signal and small-signal analyses are introduced in connection with diode circuits. When the transistor is then studied, all the techniques are firmly established.

Bias stability and biasing arrangements employed in integrated circuits are introduced in addition to the standard techniques. Low frequency power amplifiers are then discussed followed by small-signal low-frequency amplifiers. The concept of impedance reflection, established early in the course, is used throughout as a shortcut in the analysis of complicated circuits. Multiple transistor circuits are then examined with emphasis on those circuit configurations (such as the difference amplifiers and other DC amplifiers) which lend themselves naturally to integrated circuit fabrication techniques. The principles and advantages of feedback are brought out by a study of gain, sensitivity, and impedances from both the analysis and design points of view.

Examples of feedback amplifiers stress those which use linear integrated circuits. The fabrication and design techniques of integrated circuits are presented followed by a detailed analysis of an IC operational amplifier containing nine transistors (outlined below). The operation of junction and MOS field-effect transistors is studied next. The remaining topics are devoted to frequency response covering low and high-frequency response of RC-coupled amplifiers, the transistor as a switch, tuned narrowband amplifiers, methods for extending the bandwidth of wideband amplifiers, frequency response of feedback amplifiers, stability





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received the BSEE from the City College of New York in 1961. The same year, he joined RCA Laboratories to work in the areas of semiconductor-device theory and fabrication. He attended Princeton University under the RCA Laboratories Graduate Study Program and received the MSEE in 1963. Under the RCA Laboratories Doctoral Study Award, he attended the Polytechnic Institute of Brooklyn and received the PhD in Electrical Engineering in 1966. In December of 1966, he transferred to the Technical Programs Laboratory of Electronic Components in Somerville as a Project Engineer involved in computer-aided transistor design and semiconductor-device design and fabrication. He assumed his present position in July 1968 where he is responsible for the development of microwave integrated systems. Dr. Schilling has lectured at Brooklyn Polytechnic Institute, the City College of New York, RCA Somerville, and in the CCSE and CEE programs. He is author or co-author of 10 published papers and of a chapter, with M.A. Lampert, on "Injection in Solids" in Vol. 6 of *Semiconductors and Semimetals;* he is also co-editor of a McGraw Hill book on modeling and computer-aided design. He has served on a panel on "Computer-Aided Bipolar Design," (1968 IEDM) and on a panel on microwave integrated circuits (1969 G-MTT). He is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, and IEEE, and is active in the Basic Sciences Committee of the New York IEEE section having served as 1969-1970 chairman. Dr. Schilling has been awarded two patents.

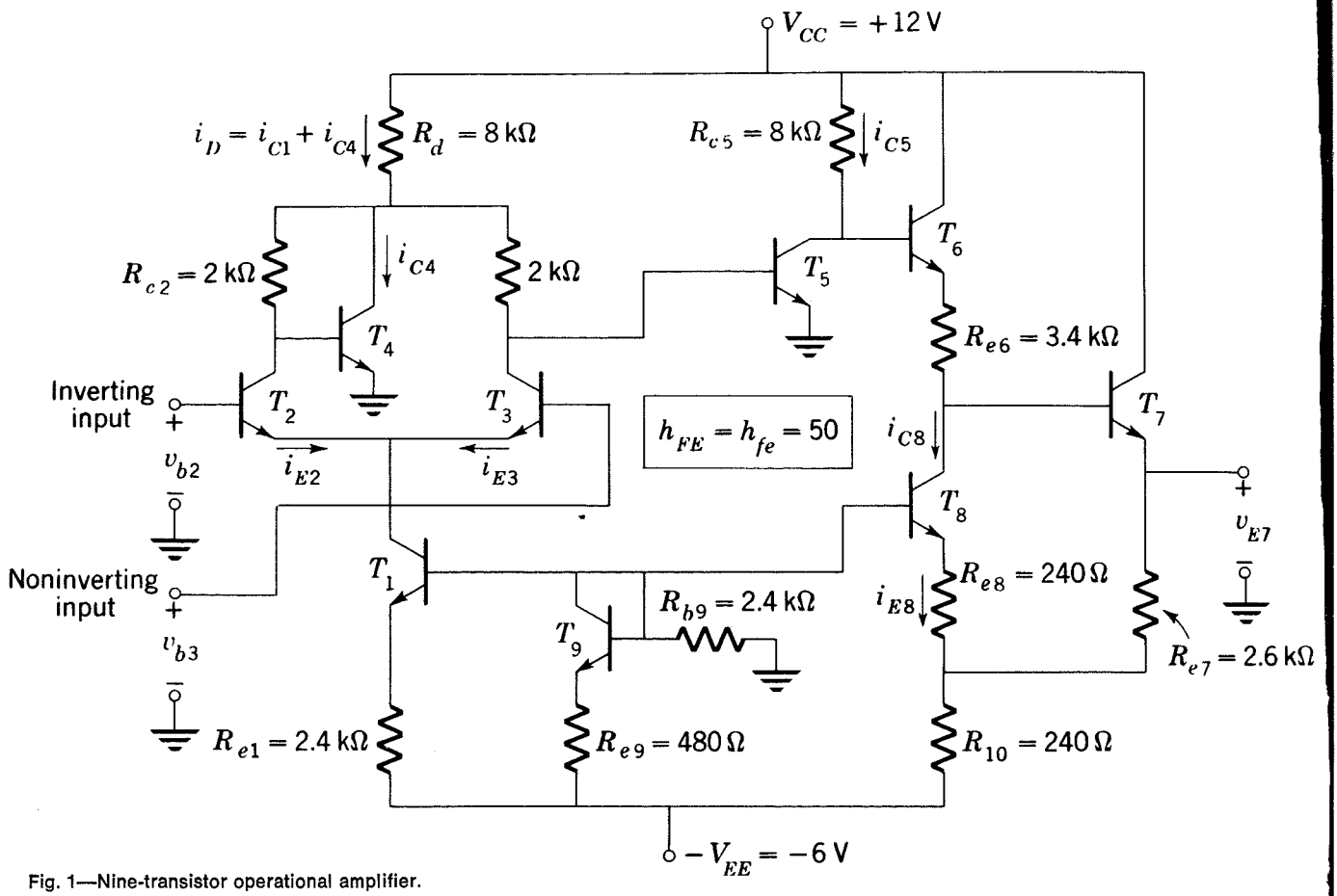

Fig. 1—Nine-transistor operational amplifier.

problems, and frequency compensation techniques.

Course structure

The course closely follows the text *Electronic Circuits; Discrete and Integrated* by D. L. Schilling and C. Belove.[1] The topics described above are covered in three twelve-session courses—each session consisting of two approximately forty-five minute tapes. The tapes combine lectures covering new material with review material and short quizzes which aid in both review and learning. A typical sequence is as follows: a 15-minute lecture—a 5-minute quiz—5 minutes for solution—15-minute lecture—5 minute quiz. The solution for the last quiz would then be on the start of the second tape for that session. No rigid sequence is followed; it would detract from effective teaching. The lecture/quiz procedure is very effective. It keeps the student constantly aware of his progress.

Course philosophy

Major emphasis has been placed on the "building-block" approach. After the basic techniques are presented, circuit analysis proceeds as a normal outgrowth. Complicated circuits are then built from the simpler circuits studied previously.

Another important technique that has been used successfully in this course is that of "discovery". For example, when studying impedance reflection, which is developed from the basic tools, it is found that the impedance looking into the base of a transistor with an emitter resistor is given by the product of (beta +1) and the emitter resistance. When the topic of the emitter follower is presented a few sessions later, the student realizes that he discovered this principle earlier. He then feels fully confident to tackle the emitter follower.

Over the years, I've found the discovery game to be a most powerful teaching technique. Often the worst thing the instructor can do is to "name" the topic. A more impressive example is that of the Laplace transform. The first time I taught a course in circuit theory, the title Laplace Transform scared them away. The next time, I multiplied a simple differential equation by e^{st} and carried out a simple integration. The students were extremely proud to have discovered the Laplace transform by applying existing tools.

To demonstrate the level of this course and the method of presentation, a portion of one lecture has been taken directly from the video tape and is given below.

Sample lecture—the operational amplifier

We now consider the analysis of the nine-transistor IC operational amplifier shown in Fig. 1. Transistors T_1, T_2, and T_3 form a difference amplifier with a constant-current supply. The bases of T_1 and T_8 are tied to the base and collector of T_9, which is connected as a diode, forming a diode bias circuit for temperature compensation. Transistor T_5 serves to amplify the output signal of the difference amplifier. The cascode amplifier, consisting of T_6 and T_8, shifts the DC level from a high level at the collector of T_5 to approximately ground level at the emitter of T_7—the output. This is done with negligible loss in gain. Since T_7 is an emitter follower, it provides the circuit with a low output impedance. Transistor T_4

serves a dual role: it balances the currents in T_2 and T_3 and, as shown later, it provides a gain of 2. Note the 2.6-kilohm resistor (R_{e7}) which is tied between the emitter of T_7 and the emitter branch of T_8.

We will now show that R_{e7} provides positive feedback. Consider that V_{E7} (output) increases. Therefore V_{E8} will increase forcing V_{BE8} to decrease since V_{B8} is held fixed. A decrease in V_{BE8} results in a decrease in I_{C8} forcing an increase in V_{B7} and therefore V_{E7}. The result is that an increase in V_{E7} results in further increase of V_{E7} and therefore positive feedback.

Portions of this circuit are very familiar to you. The difference amplifier, the temperature compensation circuit, the emitter follower, and the positive feedback circuit were all studied in detail in previous sessions.

Exercise

Since most of the circuit is familiar to you, let's start the analysis with an exercise:

Find $I_{C1} \simeq I_{E1}$ in terms of V_{EE}, V_{BE9}, and V_{BE1};
Assume impedances seen looking into the base of T_1 and base of T_8 are "very large";
Time allotted $\simeq$ 5 minutes.

(At this time, the tape is shut off and the class proceeds. If more time is required the Associate Instructor can leave the tape off for longer than the allotted time. The tape is then put on).

Solution

We will first find V_{B1} and then use it to find $I_{E1} \simeq I_{C1}$. Since we assumed the base impedances are high, we can neglect the base currents of T_1 and T_8 resulting in the equivalent circuit shown in Fig. 2 from which V_{B1} is determined.

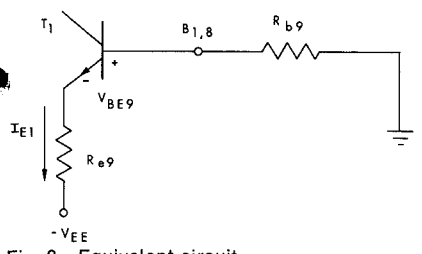

Fig. 2—Equivalent circuit.

From Fig. 2, using voltage division,

$$V_{B1} = V_{B8} = [R_{b9}/(R_{b9} + R_{e9})](-V_{EE} + V_{BE9})$$

From Fig. 1,

$$I_{C1} \simeq I_{E1} = (V_{B1} - V_{BE1} + V_{EE})/R_{e1}$$

1. Overall evaluation of session — Excellent | Good | Fair | Poor
2. Material presented is useful to your work — Immediately | Foreseeable Future | Of Little Value | No Value
3. Academic level of material presented — Too High | About Right | Too Low
4. Overall TV Instructor presentation — Excellent | Good | Fair | Poor
5. Study Guide Material — Excellent | Good | Fair | Poor
6. Any TV projection problems? — None | Did not affect Learning | Had some effect on Learning | Lecture Ineffectual
7. Time allotted for doing in-class exercises — Too Much | Satisfactory | Not Enough
8. Depth and detail coverage — Tried to cover too much | About Right | Covered too Little
9. Any additional comments

Fig. 3—Coure rating form.

Hence,

$$I_{C1} = \{(V_{BE5} - V_{EE})[R_{b9}/(R_{b9} + R_{e9})] - V_{BE1} + V_{EE}\}/R_{e1}$$

Having determined I_{C1}, we can find $I_{C2} = I_{C3}$. We know that for a balanced difference amplifier

$$I_{C2} = I_{C3} = I_{C1}/2$$

We next determine $I_{C4} = I_{C5}$. Consider the loop in Fig. 1, consisting of $V_{CC} - R_d - R_{C2} - V_{BE4}$. Writing the loop voltage equation, we have

$$V_{CC} = R_d(I_{C1} + I_{C4}) + R_{C2}(I_{C1}/2) + V_{BE4}$$

from which

$$I_{C4} = I_{C5} = \frac{V_{CC} - R_d I_{C1} - R_{C2}(I_{C1}/2) - V_{BE4}}{R_d}$$

We proceed in the above manner to find all the DC currents and voltages in the network. Then the complete small-signal analysis is performed. Roughly half the effort is covered in exercises and the other half in instructor presentation. This allows for an effective interaction between student and instructor.

Evaluation of the tape-teaching technique

From the instructor's point of view there are many advantages with the TV-tape media. The fulfillment associated with teaching others is present; however, there is a delay factor. Several weeks may go by before the "reviews" come in. Each student fills out a rating form (Fig. 3). Doing a good job in CEE consists not only of a fine presentation, but more important, presenting material that is useful.

I am personally satisfied that there are hundreds of RCA engineers doing a better job because of these courses. Another valuable advantage of the tape is that the instructor can have his material simultaneously presented at many different locations.

Teaching to a camera instead of a live audience takes getting used to. Teaching on tape calls for a greater amount of self judgment than live lecture where the students' comments and reactions help to monitor the pace and level of presentation. Teaching via tape in my opinion is easier than a live lecture only in so far as having to get the material across properly only once. When teaching something for the first or second time, an instructor is often more enthusiastic. He also is more concerned with the critical details of understanding associated with teaching and learning the material. If these items are captured on tape, the presentation is significantly more effective.

The student benefits from having a good course on useful material brought directly to his plant location. At many locations, it is difficult to have qualified instructors in the many subject areas that are pertinent to the RCA engineer.

Reference

1. Schilling, D.L. and Belove, C., *Electronic Circuits: Discrete and Integrated* (McGraw-Hill Book Company, New York, 1968).

Monolithic linear IC's for the consumer market

R. A. Santilli

This paper traces the evolution of the linear integrated circuit as a device for use in consumer products. At present, the most viable applications are in home entertainment units, such as radio, television, and audio equipment. However, as the non-entertainments consumer products become more complex and reliability requirements become more stringent, the linear integrated circuit could also become a strong contender for this market.

THE TRANSITION FROM electron-tube technology in consumer products to linear integrated circuits (LIC's) is an evolution in progress. At present, the major inroads have been made in home-entertainment products, specifically color television. The total consumer market, however, is represented by a myriad of products, a partial listing of which is shown in Table I. Because a few of these products are more suitable to integration than the others, it is easier to assess their requirements, timing, benefits, and economics. As an example, it is possible to partition a radio or television receiver, examine a functional block of either tube or discrete solid-state electronics, and fairly accurately estimate its cost and the contributed value that the IC must have to economically serve the application.

The picture is less clear, however, when similar comparisons are attempted with systems of a mechanical or electromechanical nature, such as washers or dryers. In these cases, simple mechanical timers and associated switches provide the needed power switching and timing for relatively low cost. However, as additional features are added, the complexity and cost of the mechanical timer increase, reliability decreases, and a point is reached at which solid-state control becomes economically viable. Although it is realistically certain that IC's will make sizable gains in this market, the timing will vary with the specific application because of the consumer's desires and the need for continual systems development for the best performance/cost ratio.

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The requirements that linear integrated circuits must meet in order to compete in TV, radio, and audio applications are as follows:

1) *Contributed value*—The domestic consumer market is extremely competitive. Fundamentally, unless the IC provides functions not presently included in the system, it is simply replacing a function performed by tubes or discrete transistors and will not be utilized unless it is cost effective. Although a portion of a circuit considered for integration can easily be assessed relative to its cost on the basis of such factors as pellet size, circuit complexity, and package, true cost cannot be ascertained until user specifications are resolved and yields established. Despite the assistance of computer-aided design techniques, this user-specification problem cannot be resolved in many critical circuits until the product is manufactured because there are complex dynamic testing requirements. Component manufacturers and system manufacturers must be alert to each other's needs to assure that the IC will be of an optimum design.

Again, because of the size and the highly competitive nature of the market, consumer IC designs tend to be "custom-circuit" oriented rather than "general-purpose" circuits.

2) *System simplicity and reliability*—The advantage of lower component and interconnect count contributes to system simplicity. Reduced inventory requirements also provide a significant advantage to the component user.

Improved reliability is inherent in the IC system, provided rigid reliability criteria are applied. RCA has established mechanical and environmental requirements for IC's (including operating and storage life) which are at least as severe as those for a single discrete bipolar device intended for the same function.

3) *Circuit advantages*—Monolithic technology provides inherent circuit advantages relative to component matching (active or passive), temperature compensation, and voltage regula-

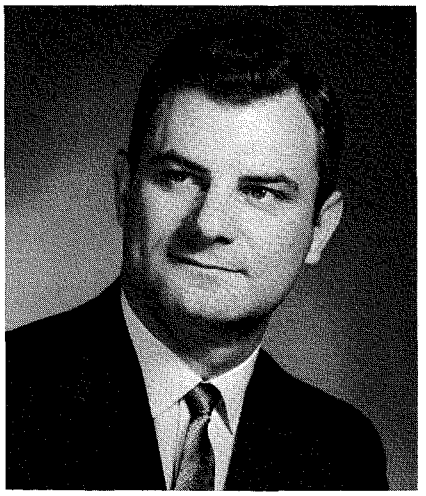

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Table I—Listing of consumer products with LIC potential.

Major category	*Typical applications*
TV	All small-signal processing in color and black-and-white receivers.
Radio	AM, AM/FM in console, table, portable, or automotive receivers.
Audio	Mono, stereo, tape
Household appliances	Washers, dryers, ovens
Musical instruments	Organs
Visual equipment	Projectors, cameras
Automotive	Heating and air-conditioning controls, anti-skid systems.

tion that contribute to excellent system performance.

4) *Serviceability*—Servicing is made easier in some complex systems (such as television) through the use of sockets and/or replaceable boards.

Television

Considerable effort has been devoted to IC's for color TV. Black-and-white TV receivers have benefited from the color TV development work and utilize some of the compatible circuits. Exclusive of the VHF and UHF tuners, present-day monolithic IC technology can provide IC's capable of performing all other small-signal functions in a color television receiver. The task of partitioning the receiver for integration can be accomplished in different ways. One partitioning system cannot suffice for all users. The crosshatched functions shown in Fig. 1 indicate areas in which reasonable industry agreement exists on partitioning. The areas marked "C" indicate the circuitry capable of being integrated today.

Exclusive of the replacement of a discrete stage with a simple integrated circuit (i.e., a differential amplifier), the first LIC for television was introduced in 1966.[1] This circuit, the present RCA CA3014 shown in Fig. 2, consists of a sound-IF amplifier/limiter, an FM discriminator, and an audio emitter-follower output. The CA3014 was started in production in the RCA-CTC25 chassis, and replaced the commonly used tube-type IF amplifier and quadrature detector. Since that time, the sound-IF amplifier has progressed through several IC developments, each providing more contributed value with fewer peripheral components.

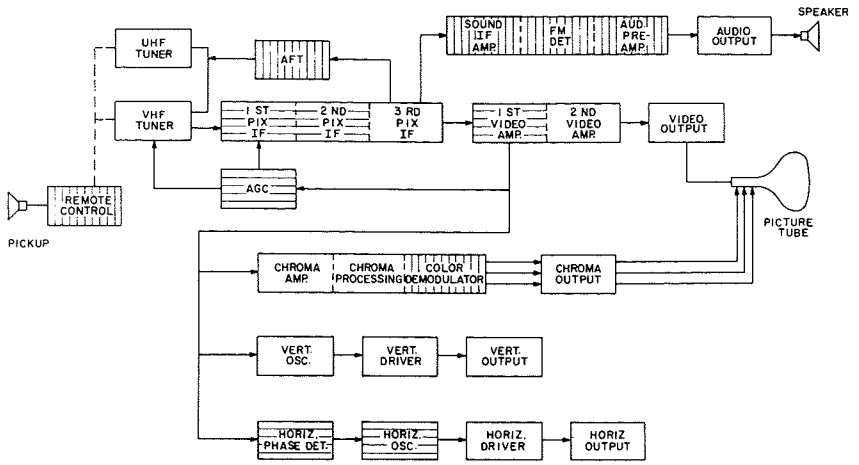


Fig. 1—Color TV receiver block diagram.

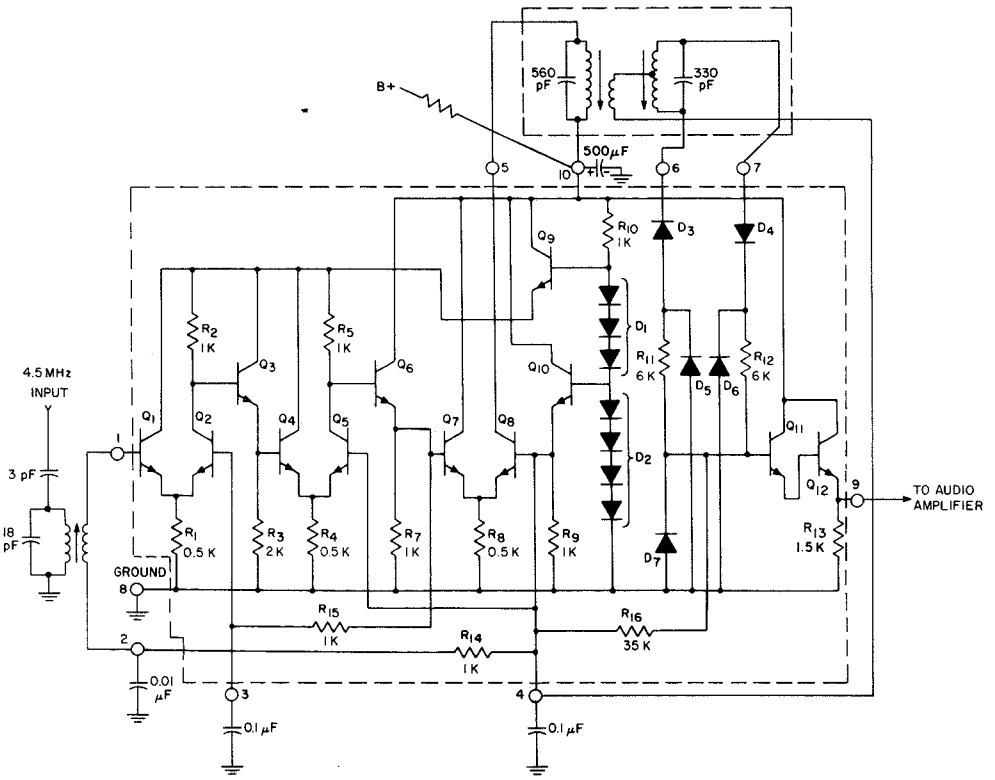


Fig. 2—Schematic diagram of the CA3014 sound-IF amplifier.

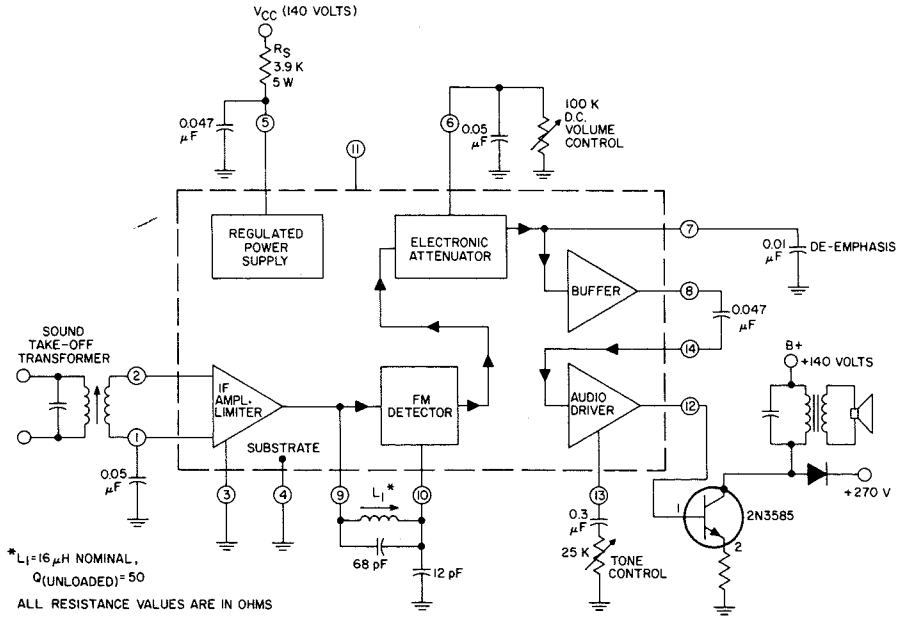


Fig. 3—Schematic diagram of the CA3065 sound-IF amplifier.

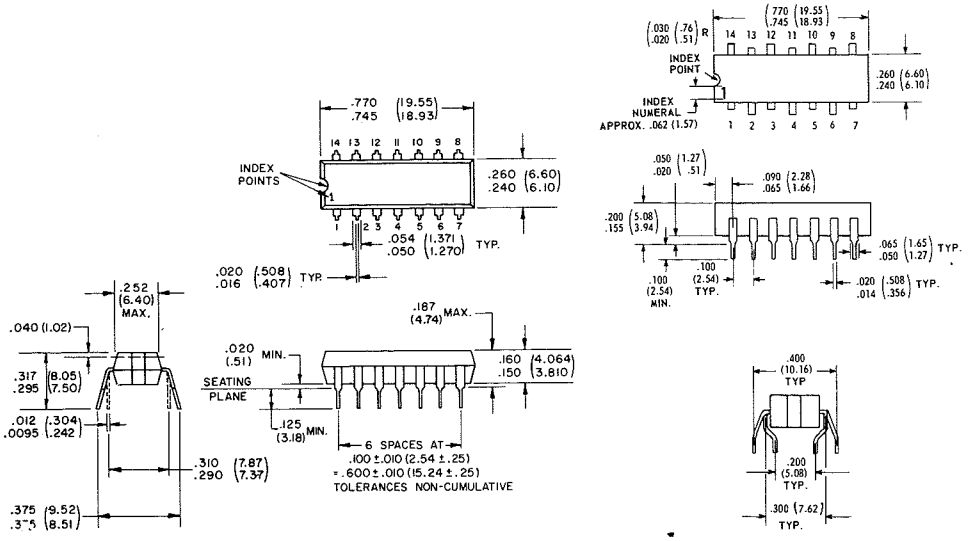


Fig. 4—In-line lead arrangements.

The latest sound-IF amplifier, the CA3065, is shown in Fig. 3. In comparison with the CA3014, the CA3065 has better limiting sensitivity (200 μV maximum as compared to 400 μV maximum at 4.5 MHz), and a zener power supply. This power supply provides stable power for the chip while simplifying the power-supply decoupling network by eliminating an electrolytic capacitor. In addition, the conventional double-tuned discriminator-transformer is replaced with a single-tuned coil; the emitter-follower is replaced by an isolated-biased audio amplifier having 20 dB of gain, and a DC volume control following the detector is incorporated into the design. The DC volume control permits the use of a single, unshielded wire to the volume-control potentiometer which may be bypassed, if necessary, for hum suppression. The CA3065 is available in a 14-lead, dual-in-line plastic package. Although interlead spacing on this package is 0.1 inch, a quad in-line staggered forming of the leads is available which provides a spacing between leads of 0.14 inch, as shown in Fig. 4.

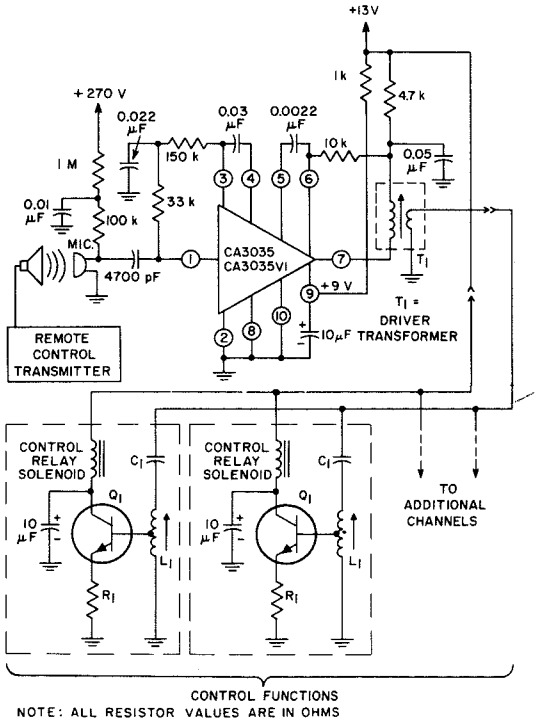


Fig. 5—Block diagram of CA3035 remote-control IC.

Frequently forgotten in the application of these circuits is the fact that the IF gain-block portion of these circuits is subject to stability criteria[2-4] to eliminate regeneration. It is recommended that the source-load conductance product be compatible with the manufacturer's recommended circuit.

A remote-control amplifier and an automatic-fine-tuning circuit followed the sound-IF amplifier in 1967. The block diagram for the RCA CA3035 remote-control system is shown in Fig. 5. The CA3035 is an ultra-high-gain (132 dB at 40 kHz), low-noise device consisting of three separate amplifiers. These single-ended amplifiers are normally capacitively coupled with small-value capacitors to provide the required low-frequency roll-off. Internal bias circuits establish stable operating conditions for amplifiers No. 2 and No. 3 as a function of supply voltage and temperature; amplifier No. 1 is stabilized by DC feedback from terminal 3 to terminal 1. The unit is supplied in a 10-lead, TO-5 package. Because the CA3035 is basically the receiver portion of the remote-control system (up to the relay drivers), it is compatible with electromechanical or all-electronic systems, and thus has not suffered from technical obsolescence.

Automatic-fine-tuning systems have progressed through several generations since their introduction. The functions of the chips have basically remained the same: a biased wideband IF isolation amplifier/limiter (up to 60 MHz), an FM detector network, and an error-voltage amplifier. However, the performance has been improved and the peripheral circuitry has been simplified. Fig. 6 shows the first automatic-fine-tuning circuit introduced, the CA3034, and the recently introduced CA3064. The IF-amplifier gain has been improved by 20 dB (45.75-MHz picture-carrier reference), a zener supply has been incorporated, and bypassing has been simplified in the IF amplifier through the use of a single-ended IF amplifier. The CA3064 is available in a 10-lead TO-5 package.

A good deal of field history has been generated on these functions since 1966. Although 27 million digital monolithic IC's were sold in 1966, no significant field history existed for monolithic linear IC's in these applications; the translation of reliability from one system to another can only be made in general terms because of systems-induced failure modes. Some common failure modes which were uncovered during this period are as follows:

1) In TV receivers in which the sound IC was used directly to drive an audio output tube, warmup tube arcing was transmitted through the grid to the audio preamplifier of the IC and damaged the preamplifier. Inclusion of a series resistor having a minimum value of 0.1 megohm between the preamplifier and the tube grid solved this problem.

2) Instances have been investigated where IC's "mysteriously failed" on receiver life tests. Artificially induced picture-tube arcing duplicated the failure mode, and a simple ground layout or lead dress solved the problem.

Current developments

The prime area of current development in the TV industry is chroma demodulation. A doubly balanced demodulator, balanced for chroma

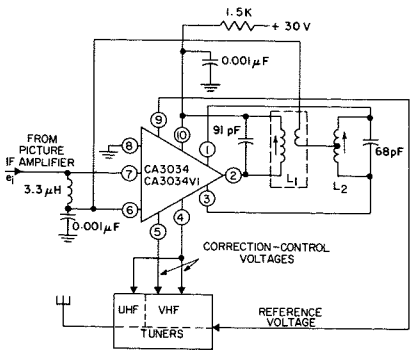
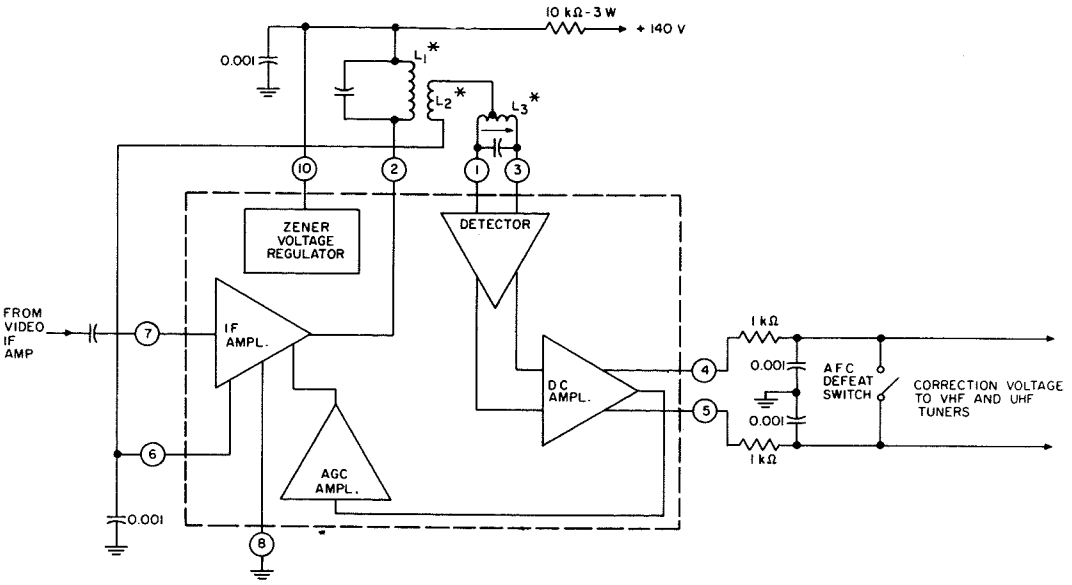


Fig. 6—Block diagrams for CA3034 and CA3064 AFT circuits (L_1 and L_2 are the phase detector transformers).



demodulation as well as the 3.58-MHz reference, is shown in Fig. 7. This circuit operates in a synchronous detection manner in which the chroma signal is fed to the constant-current source in a differential-amplifier circuit, while the reference voltage is applied to the differential amplifier. The doubly balanced configuration provides cancellation of the 3.58-MHz reference and minimizes the need for filtering at the outputs. The outputs of the two decoders are fed to a resistive matrix in which the color-difference signals are developed and then individually delivered to the outputs through emitter-follower isolation amplifiers.

Manufacturers have introduced IC's for other portions of the receiver also. Examples of such IC's are as follows:

1) First and second picture-IF amplifiers, AGC gating amplifier, and IF and RF AGC amplifier.

2) Sync separator, horizontal oscillator, automatic frequency control, automatic phase control, and noise blanking.

3) Video preamplifier, gated AGC detector and amplifier, noise detector and gate, sync separator, automatic horizontal sync circuit, and vertical sync amplifier.

Although the primary penetration has been in color TV, black-and-white receivers can use compatible devices such as IC's in the sound-IF amplifier. Ultimately, it is anticipated that black-and-white TV may justify development of some of its own custom circuits.

Radio

The immediate radio market is for home-entertainment and automobile AM and AM/FM radios. Until recently, the AM radio had few options in the use of an IC for AM, although an array, a differential amplifier, or an audio preamplifier circuit could be used. The new RCA Dev. No. TA5640, however, now provides a flexible and versatile AM "front-end" circuit (up to 30 MHz) compatible with composite IF amplifiers in AM/FM receivers.

The TA5640, shown in Fig. 8, consists of an RF amplifier with an AGC circuit, a mixer oscillator, two IF amplifiers, and a 5.5-volt zener reference supply. The AGC-amplifier portion of the circuit, consisting of Q_1 through Q_4, drives Q_6, which acts as a variable, unbypassed emitter-resistance for the low-noise RF-amplifier stage Q_5. The mixer-oscillator stage is a differential amplifier with a constant-current source. The RF input is fed into the differential amplifier (either push-pull or single-ended). The oscillator is a common-base configuration utilizing Q_7 and Q_8 in parallel as the active element. Single-ended feedback is provided from the common collectors

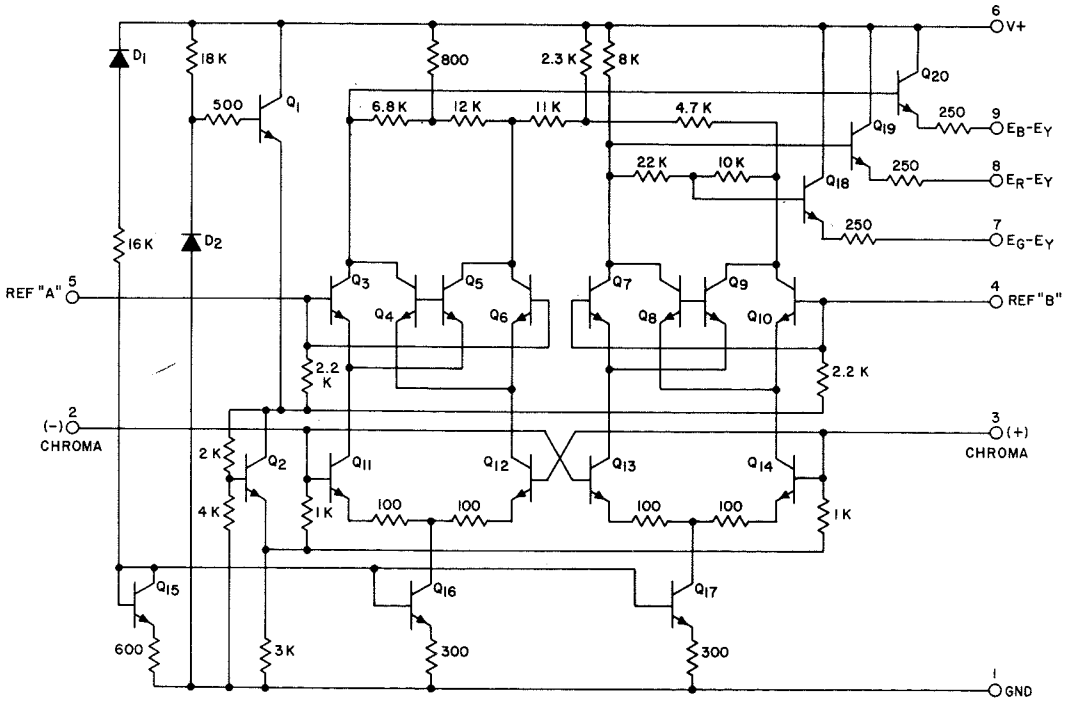


Fig. 7—Schematic diagram of a basic chroma demodulator circuit.

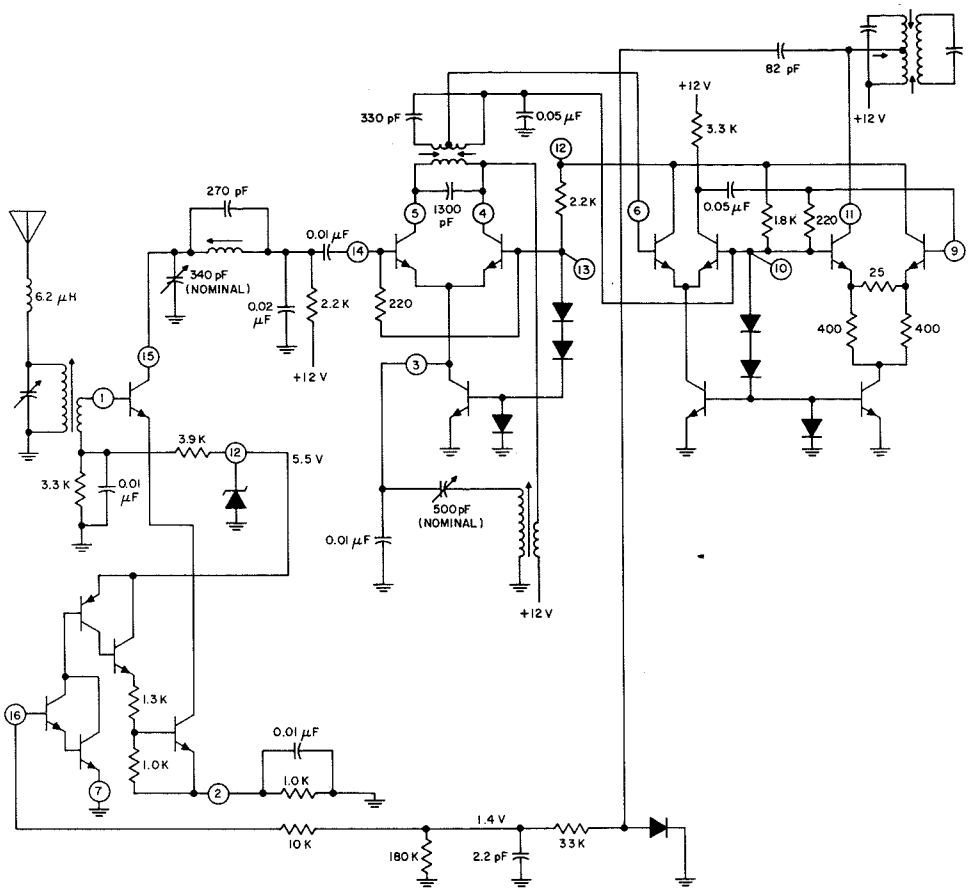


Fig. 8—RCA Dev.No.TA5640 AM "front-end" circuit.

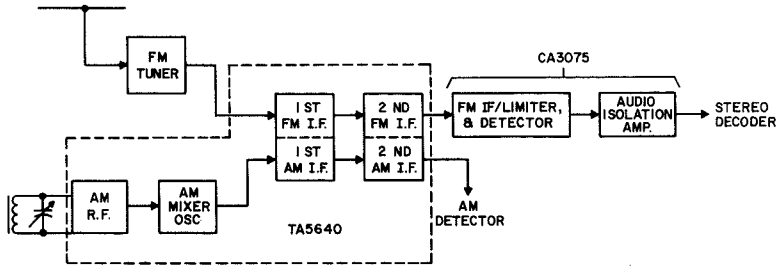


Fig. 9—AM/FM receiver block diagram.

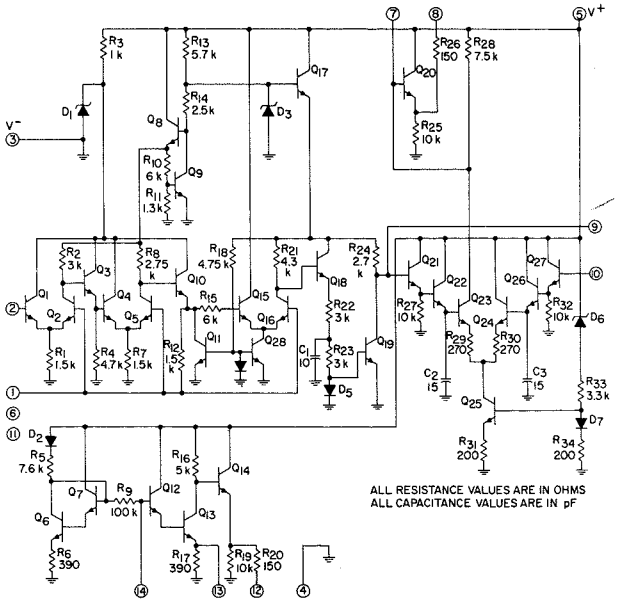


Fig. 10—Schematic diagram of CA3075 amplifier.

through the oscillator-tuned circuit to the common emitters. Because oscillator current can flow in either or both legs of the differential amplifier, and because this current is fixed by the constant-current source, AGC may be applied to the mixer without objectionable oscillator pulling or blocking. Thus, the circuit behaves more as a mixer-oscillator than as a conventional bipolar self-oscillating mixer circuits (i.e., autodyne converters). Two IF-amplifier stages are provided, one with unbypassed emitter resistance for good linearity and dynamic range.

This mixer-oscillator IF configuration provides maximum versatility for composite AM/FM IF-amplifier configurations. A typical block diagram of a high-performance AM/FM receiver is shown in Fig. 9. The first and second

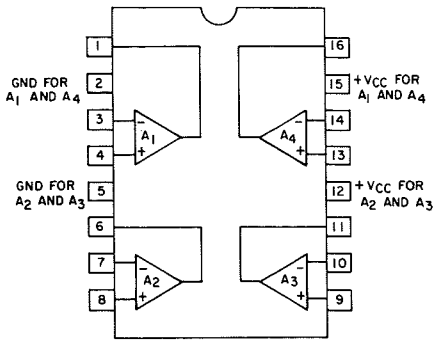


Fig. 11—Schematic diagram of CA3052 stereo preamplifier.

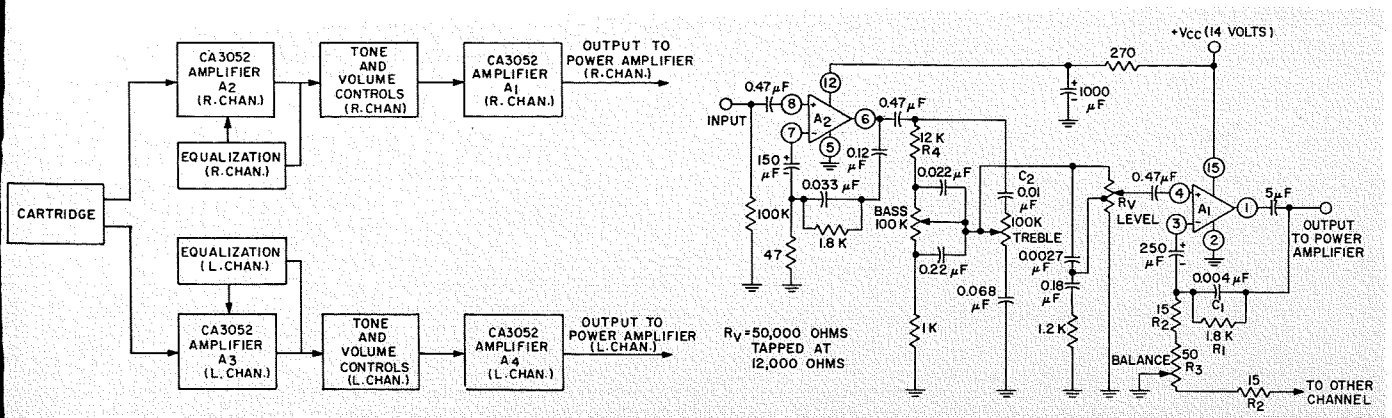
IF-amplifier stages are RC-coupled and composite for AM and FM. The FM-IF output of the second IF amplifier is transformer-coupled to the high-gain amplifier block, which is a portion of another IC, the CA3075. The CA3075, an IC developed and optimized specifically for FM IF applications, consists of a three-stage direct-coupled amplifier/limiter, an FM detector network with an isolated emitter-follower amplifier, and an audio preamplifier, as shown in Fig. 10. The FM detector requires only a single-tuned coil, which simplifies alignment while minimizing cost. The −3-dB limiting sensitivity of the IF gain block (10.7 MHz) is 500 μV maximum, and the recovered audio at the detector output (terminal 8) is 525 mV minimum (400 Hz modulation, 75 kHz deviation).

The audio amplifier is a single-stage amplifier with emitter-follower input (for high input impedance) and emitter-follower output. The amplifier provides an audio gain of 21 dB with terminal 13 unbypassed. No external bias components are required for the audio amplifier.

The TA5640 and the CA3075 allow many AM/FM receiver options for either mobile or home-entertainment applications. Strings of B+ zener diodes (of approximately 12 volts) have been intentionally omitted from both types to accommodate mobile or marine applications. The TA5640 and the CA3075 are available in 16-lead dual-in-line packages.

Audio

In audio equipment, monolithic IC's have started to pervade the stereo-preamplifier and low-power audio-amplifier market. The availability of multiple-amplifier IC's, such as the



Gain at 1-kHz reference	47 dB
Boost at 100 Hz	11.5 dB
Boost at 10 kHz	11.5 dB
Cut at 100 Hz	10 dB
Cut at 10 kHz	9 dB
Noise: At maximum volume (input shorted)	>70 dB below 1 V
At minimum volume *	>80 dB below 1 V
Total harmonic distortion (at 1-kHz reference and an output of 1V)	<0.3%

Fig. 12—Block diagram, schematic diagram, and performance data of typical high-quality stereo phonograph preamplifier.

CA3052 shown in Fig. 11, has permitted stereo circuits with additional degrees of design freedom. The CA3052 consists of four identical, independent, low-noise amplifiers that can be connected to provide all the amplification necessary in a stereo preamplifier. Each of the amplifiers in the CA3052 consists of a differential amplifier (Darlington input) driving a common-emitter amplifier. Internal negative DC and AC feedback is provided from the output of the common-emitter amplifier to the non-inverting side of the differential amplifier. The AC feedback may be adjusted by controlling the AC impedance from the non-inverting side of the differential amplifier to ground (i.e., terminals 3, 7, 10, or 14 to ground). When this point is AC-bypassed, a maximum gain of 58 dB per amplifier is obtained with a bandwidth of 300 kHz. Equalization techniques for phonograph or tape can easily be incorporated with appropriate RC networks between the amplifier output and the non-inverting side of the differential amplifier. The block diagram and schematic (one channel) of a typical high-quality phonograph preamplifier are shown in Fig. 12.

Low-power audio amplifiers (up to 5 watts) have been readily available in the consumer market for the last two years. Basically, the designs are of a driver-output configuration with output circuits of the conventional push-pull (transformer-output), or quasi-complementary-symmetry type. A typical example is the CA3020A shown in Fig. 13. This circuit consists of a differential-amplifier configuration that provides gain as well as phase inversion and drives emitter-follower amplifiers which, in turn, drive the isolated outputs. A temperature-compensated bias circuit is incorporated, together with an optional emitter-follower buffer input stage for increased input impedance. Common applications of the CA3020A include the power-driver function as well as the conventional audio-output stage shown in Fig. 14.

Conclusion

Leading the increased use of linear IC's in consumer products are home entertainment units, in which IC's are already making major inroads. Although many non-entertainment consumer applications are only in the drawing-board stage and require improved systems or a better performance/cost ratio, the trend is clear. For consumer products, the '70's will be a decade of integration.

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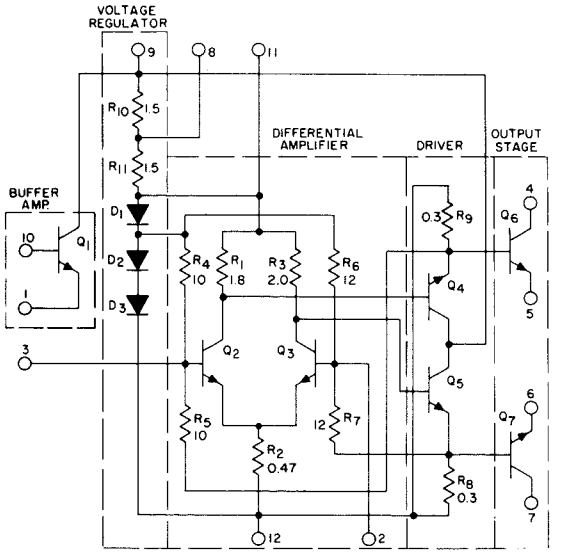

Fig. 13—Schematic diagram of CA3020A audio amplifier.

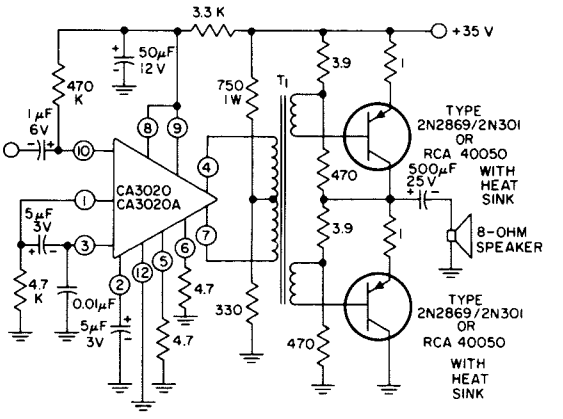

Fig. 14—One-watt audio-output circuit using CA3020A power driver.

Designing practical monolithic integrated circuits

R. L. Sanquini

The design of high-volume monolithic integrated circuits to a prescribed schedule requires a different approach from the conventional research and development used for other subsystem circuit design. It is not enough to innovate a new product, make a few operating samples, and then turn the concept over to another group which spends money and time to engineer the product for factory fabrication. To design new products "against the clock", the IC designer must work with proven production processes. The ground rules are set and, therefore, must be an integral part of the engineer's thinking. To many in the design community, this approach may seem inhibiting, but with IC's the opposite seems to be true. In fact, these constraints foster practical and useful innovations. Many clever circuit design and device "tricks" have been developed to circumvent problem areas.

THE LATERAL P-N-P TRANSISTOR shown in Figs. 1a and 1b is easily fabricated with standard bipolar processing. This transistor has a relatively low output resistance. In fact, in the circuit shown in Fig. 2a which uses this type of transistor, the output resistance could be low enough so that any voltage variations appearing at the V^+ terminal would be reflected in the output. This problem would show up as poor supply-voltage rejection. Two possible solutions are applicable: the development of a P-N-P transistor having a high output resistance by use of a new process development (there are many which are complex or partly understood) or circuit design innovation using existing IC processing. The latter solution is usually the more practical and economic choice, and its application is illustrated in Fig. 2b. In this solution, cascode circuitry was added to improve power-supply rejection. Recently, this solution was successfully applied to the design of the CA3060 now in production.

Fig. 3 shows another example. In this case, the circuit design required "off-line" operation with a power supply and a ground reference. Thus, every time the input voltage became negative with respect to ground, the IC substrate diode would be forward biased and therefore cause a reduction in the device power-supply current (a most undesirable condition). The high-voltage aspect of the "off-line" opera-

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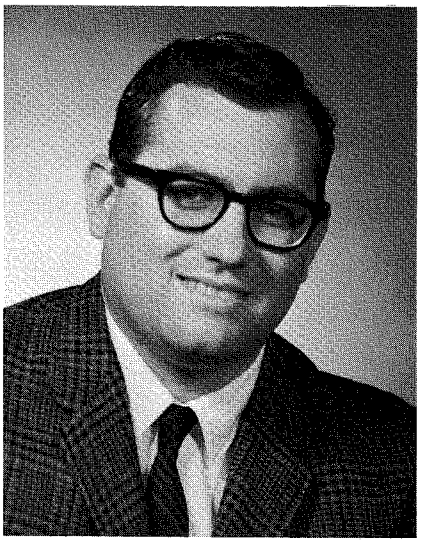

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received the BSEE from the Milwaukee School of Engineering in 1959 and has pursued graduate studies toward the MSEE at Columbia University. In 1959, Mr. Sanquini joined RCA as a Design and Development Engineering Trainee. After concluding the training program, he was engaged in the design and analysis of customer applications using solid state devices. In 1962, he joined the Integrated Circuit Design Group as an application engineer where he was instrumental in the product design of RCA's first silicon monolithic Integrated circuit, the TA5001. From 1962 to 1966, he was engaged in the design, application and testing of both linear and digital IC's. In 1966, he was promoted to Engineering Leader of the Linear IC Design Group. In 1969, Mr. Sanquini was promoted to his present position where he is responsible for both linear and digital integrated circuit development. Mr. Sanquini has published six technical articles concerning integrated circuits and has been active on the microelectronic committees of the EIA.

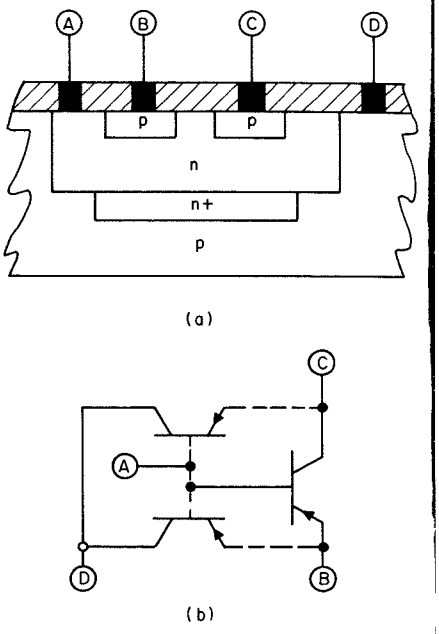

Fig. 1—A P-N-P lateral transistor compatible with standard bipolar IC processing: (a) cross section; (b) equivalent circuit.

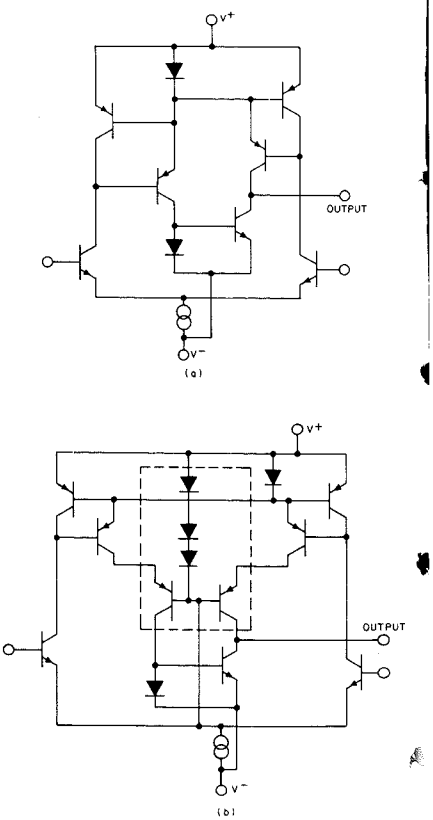

Fig. 2—Improved performance through good circuit design: (a) a poor power-supply voltage rejection as a result of circuit design: (b) an improved power-supply rejection with additional cascode circuitry.

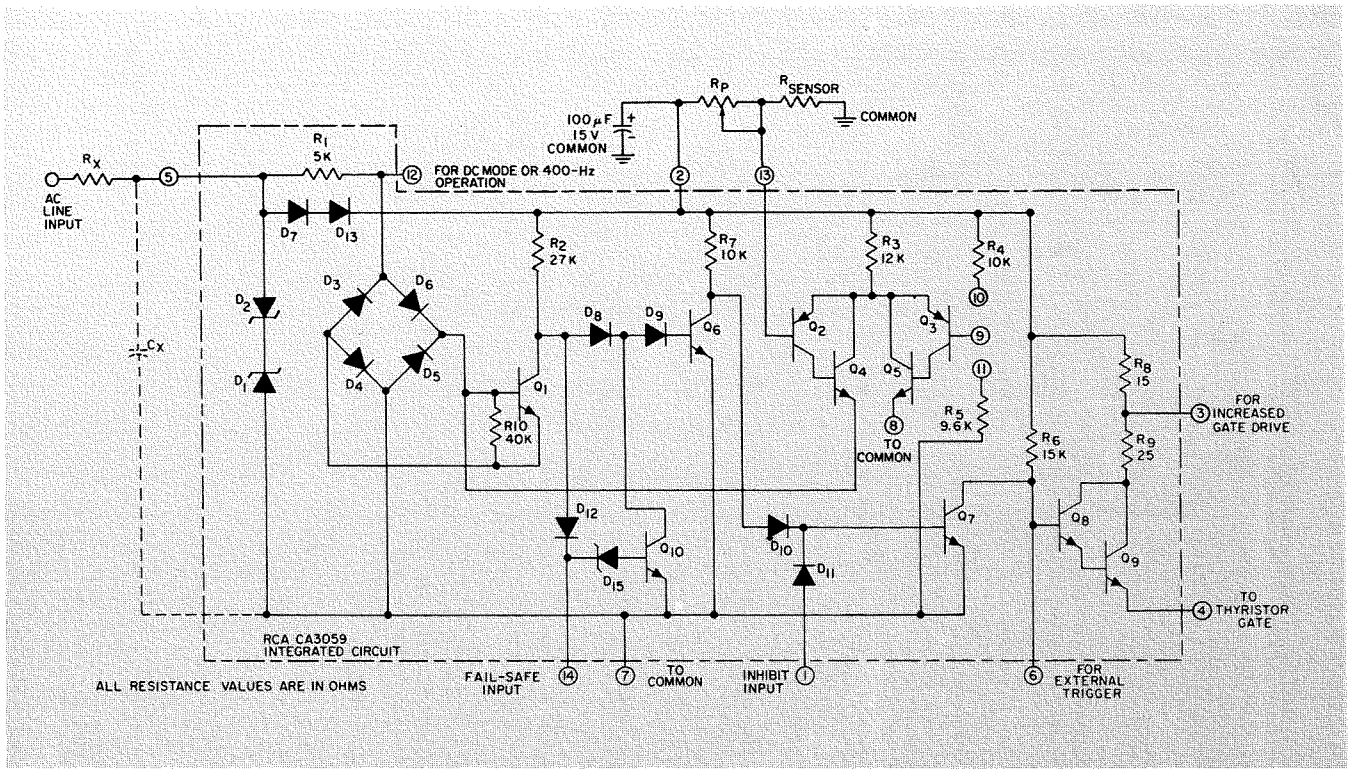

Fig. 3—Circuit diagram for the CA3059 zero voltage switch.

tion was solved by the external addition of a series dropping resistor (R_X) and the incorporation internally of two zener diodes back-to-back across the input to the circuit. The forward-biased substrate required for this design, however, proved formidable. The solution was finally obtained by use of a floating substrate and special N+ diffusions implemented to reduce parasitic P-N-P effects in the circuit. A cross-sectional view of the floating substrate used is shown in Fig. 4. These concepts have been applied to the CA3059 zero-voltage switch that is currently in production.

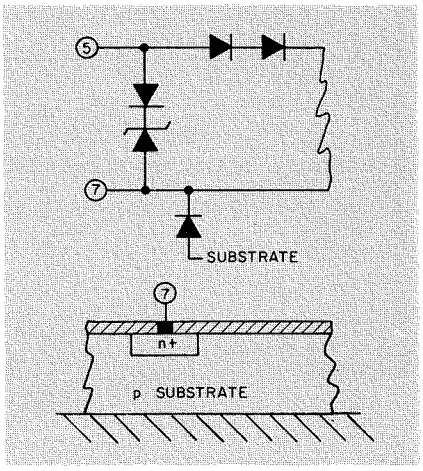

Fig. 4—A cross-section of floating substrate used in the CA3059.

Design cycle

In the RCA Solid State Division, the design engineer is required to design both custom circuits and standard "off the shelf" devices. The engineering design cycle, for either type of new product, is shown in Fig. 5.

Custom circuits

For the custom IC, the "black box" inputs are usually easy to obtain. Often, the final specifications are so fluid that they resemble a moving target. Success in this type of effort requires a very close working relationship between the design engineers of the equipment manufacturer and the IC design engineers. With close cooperation from the outset, the IC designer can synthesize a circuit within the framework of the lowest cost processing and still achieve optimum performance.

Off-the-shelf circuits

The black-box inputs required for off-the-shelf circuits are more difficult to obtain because the IC's are intended for many different end-uses. Combined marketing, application, and design efforts develop these specifications based on customer and field inputs.

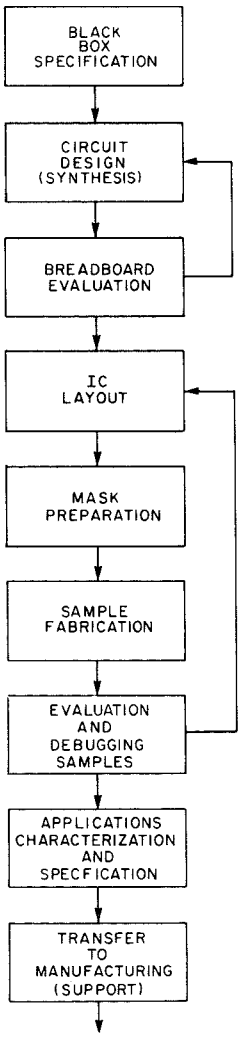

Fig. 5—New-product design cycle.

Initial design

Once the black-box specifications are established, the circuit design is synthesized on paper. The IC engineer understands the cost implications and configures the circuit with this factor in mind. With the circuit synthesized, IC components are used to make a breadboard of the circuit. The circuit is then modified and finalized to achieve the required performance. At this point, rigorous calculations are made to determine reproducibility of the circuit in a factory environment. For this determination, computers can make significant contributions in the prediction of the static and dynamic performance as a function of IC process variables. After the design review of the circuit, the chip layout begins.

Circuit layout

The IC design engineer works with a development layout engineer and draftsman to configure the optimum topology. The layout is either detailed by the draftsman or developed by use of computer-aided artwork-generation techniques. Masks are generated and samples processed and assembled. The first samples are evaluated and, if necessary, debugged. This problem-solving phase is critical in the IC development because chip performance is scrutinized so that both desirable and undesirable characteristics are understood.

Problem solving—a case history

Evaluation of the first CA3059 samples showed lack of sensitivity and low chip power-supply DC voltage as two major problem areas evident on all units. The breadboard did not exhibit these characteristics nor did the calculations. Moreover, the calculations performed on the circuit did not account for all the parasitic interactions that limited circuit performance. Moreover, the calculations are extremely complex, time consuming, and frought with frustration. If these techniques were used, more time would be spent in the anticipatory analysis than for analysis of samples and implementation of solutions (e.g., computer aid is required).

Intensive analysis of the transfer characteristic gave the first clue to the problem. The transfer characteristic from terminal 5 to 7 should have exhibited the characteristic curve shown in Fig. 6 (the curve labeled "GOOD"). The characteristic labeled "REJECT" suggested that the problem was caused by undesirable silicon-controlled rectifier (SCR) action. Further investigation showed that this action took place only when the substrate was forward biased. A circuit model for the defect mechanism was then constructed (Fig. 7).

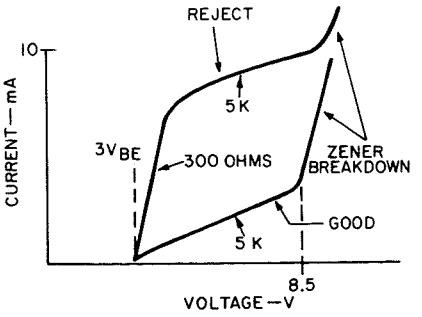

Fig. 6—Transfer characteristic of the CA3059 between terminals 5 and 7.

In this case, transistor Q_1 normally conducts in saturation except when the input traverses through ±2.1 volts. With Q_1 saturated, its parasitic P-N-P will conduct. When node **A** swings negatively (every half cycle), the composite P-N-P and N-P-N transistors from the base of Q_1 to node **A** could "latch", if the composite beta of both transistors is greater than one. Further investigation proved this hypothesis to be true. Layout and processing techniques which reduce the parasitic P-N-P were implemented on this design, and the problem was solved.

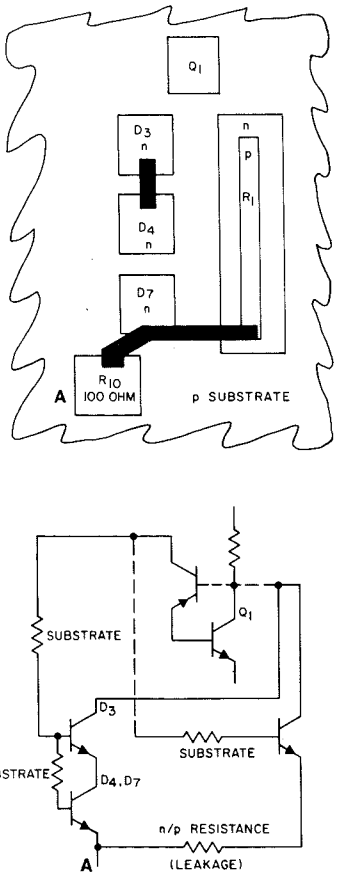

Fig. 7—Model of defect mechanism.

Development cycle

At this point, if debugging of first samples proves to be sufficient, a second cut of samples may be made for another attempt. Usually, the second samples are satisfactory, and the manufacturing start-up date established at the outset of the project is confirmed. At this point, the innovative portion of the design cycle is complete and the major part of the development cycle starts. The development cycle includes the following steps:

1) Many wafers are fabricated, changing process variables;
2) Parameter distributions are acquired;
3) Circuit probe and final test programs are written and debugged;
4) Data sheets are written;
5) Master specification sheets for factory production are established; and
6) Transfer to the factory is accomplished.

As evidenced from the delineated items, this portion of the development cycle is extremely costly. It is, therefore, obvious why problems must be caught in the design cycle.

Conclusions

New processes which may be suitable for high-volume circuits evolve from the low-volume, specialty products of today. In the linear IC category, monolithic MOS bipolar IC's, high-frequency IC's (1.3 GHz) and even high power IC's (15 watts) have been designed. Digital IC's use high-frequency processes, two- and three-level metal, and thin epitaxial layers to achieve speed and high packing density on a chip. As these processes develop along with solid packaging techniques such as beam leads, the high-volume monolithic IC's will slowly change and adapt to the new processes. This trend will extend monolithic IC's into domains unachievable today.

Beam-lead integrated circuits

I. H. Kalish

The beam-lead approach described in this article represents the extension of simultaneous processing to interconnection operations as a means of reducing costs and improving reliability.

DURING THE PAST TEN YEARS, semiconductor technology has been used to produce interconnected circuit components in complex arrays at manufacturing costs matching those of competing technologies. A key factor permitting this achievement has been simultaneity of processing. For example, in bipolar integrated circuits, all components within a circuit and all circuits within a wafer receive the same processing at the same time. Fig. 1 illustrates the basic processes used to determine the components of a bipolar integrated circuit. The number of these components and the manner of their interconnection are determined by the details of the photographic masks.

The economic benefits of simultaneous processing are obvious in that a few processes and limited facilities can produce many circuits. There are more subtle, but crucially vital, aspects of simultaneity that affect yield and reliability. The yields of components fabricated sequentially are multiplicative. For example, if a 90% yield is carried through fifty sequential operations, the result is negligible. However, 90% of fifty simultaneously processed circuits is more than satisfactory. The improved reliability associated with batch processes results from the high degree of process control that can be focused on each operation and from the ability to apply statistical quality control techniques to qualify a given manufacturing lot. In general, however, final assembly operations have depended more on sequential rather than simultaneous operations.

In the past decade, integrated circuits have demonstrated a reliability exceeding that of any previous fabrication approach. Those failures that do occur, however, have been most frequently associated with defective wire-bonding techniques and aluminum metalization. Fig. 2 shows a typical wire-bonded unit; each wire has been placed and welded with two independent operations.

Fig. 3 shows the face of a wafer that has gone through beam-lead processing; the pellets on the wafer are separated by etching. Fig. 4 shows the pellet face-down after separation, and Fig. 5 shows the pellet connected to a package substrate. The beams are made of gold, and they are thermocompression bonded to the substrate in one operation. The substrate uses gold lands in the bond area resulting in a reliable gold-to-gold connection.

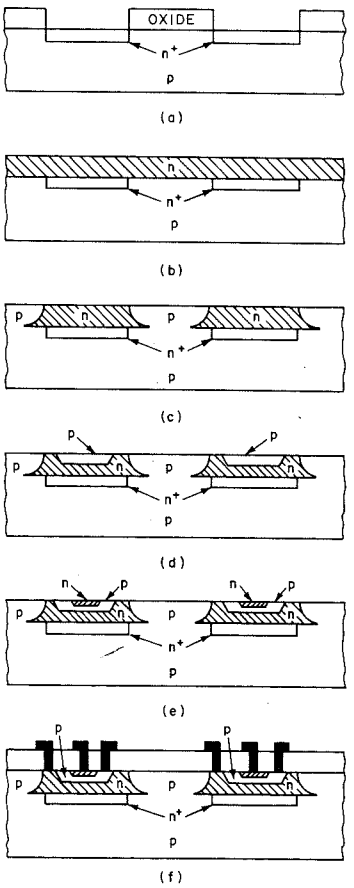

Fig. 1—Basic processing used to determine the components of a bipolar integrated circuit: (a) N+ pocket diffusion, (b) epitaxy, (c) isolation diffusion, (d) base and resistor diffusion, (e) emitter diffusion, and (f) interconnection.

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Process modifications

Several significant processing modifications have been made in the wafer area to take advantage of the beam-lead concept, as outlined in Fig. 6. Although gold is the most desirable metal for reliable bonding, the low eutectic temperature (370°C) of the gold-silicon system makes gold undesirable when used in contact with silicon. Thus, a more complex metallurgical system is required. The silicon wafer receives the standard bipolar processing through emitter diffusion. A silicon nitride layer is then formed over the silicon dioxide on the surface of the wafer. This layer forms a true hermetic seal (i.e., impervious to moisture and ionic contaminants) for the components in the wafer, the implications of which will be discussed later. The contact windows are etched through the nitride and oxide layers and a coating of platinum is applied by sputtering. Subsequent heating forms platinum silicide in the contact areas, which provides a low-resistance electrical contact to the circuit components. The unreacted platinum is re-

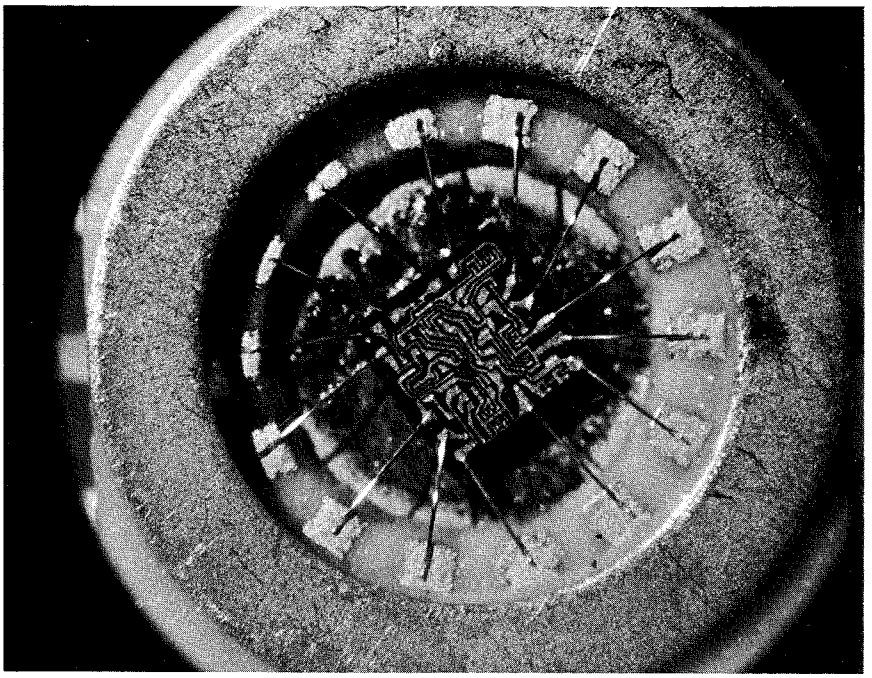

Fig. 2—A typical wire-bonded unit.

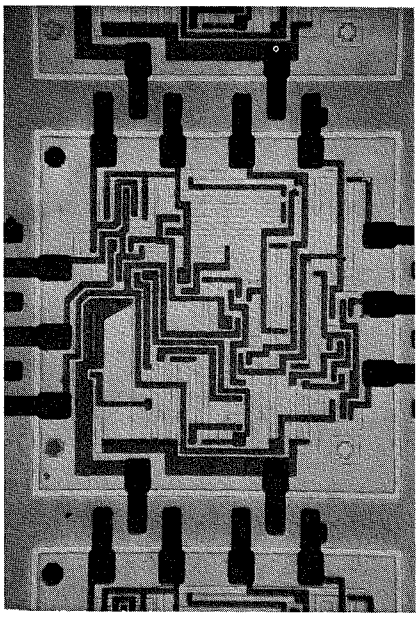

Fig. 3—Face of a wafer after beam-lead processing.

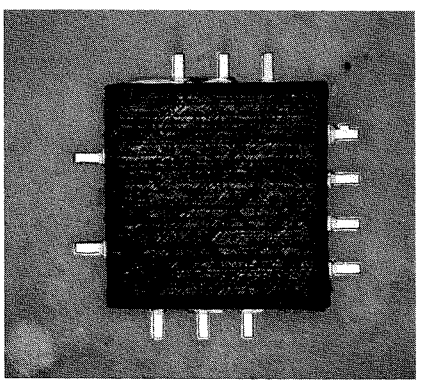

Fig. 4—Beam-lead pellet face-down after separation.

moved from the wafer, and a layer of titanium sputtered on. The titanium provides tenacious adherence to the nitride insulation. Another layer of platinum is sputtered on and then etched to define the component interconnection pattern. A low-resistance interconnection pattern is achieved by plating 20,000 angstroms of gold over the 1,500-angstrom layer of platinum. The layer of platinum is necessary as a diffusion barrier to prevent the gold from diffusing through the titanium into the silicon. Finally, the gold beam pattern is plated to a thickness of one half a mil. The continuous titanium layer which carried the current for the plating operations is now removed in those areas not covered with platinum and gold. Wafers are then mounted on sapphire discs, and lapped to a thickness of a few mils. Individual chips are then separated by etching, as shown in Fig. 7. Electrical probing of the pellets can now be performed after which the devices are ready to be connected to their final package.

It was mentioned earlier that the silicon nitride layer and gold metalization applied to the wafer provide a true hermetic seal; thus, from the standpoint of reliability, the beam-lead pellet is already packaged. On the other hand, a conventional pellet exposed to moisture is subject to catastrophic damage of its aluminum interconnections and is also extremely vulnerable to the instabilities caused by sodium-ion contamination.

Applications

Because of the inherent reliability of the beam-lead pellet, it is particularly suitable as a component for the assembly of hybrid circuits. To achieve maximum-package component-packing densities, many manufacturers are building equipments on ceramic substrates using thick-film resistors, interconnection lines, and semiconductor integrated-circuit chips. When standard wire-bonded chips are used, the absence of a package represents an increased reliability hazard. The beam-lead chip, however, is as reliable as its conventionally packaged counterpart. In addition to the size and reliability advantages, the beam-lead chip is particularly attractive for hybrid-circuit manufacture because it can be removed from the substrate and replaced without reworking the substrate. Thus, if poor performance of a complex circuit function is traced to a defective chip, repair is possible.

RCA has recognized the attractiveness of beam-lead pellets for hybrid applications by designing beam-lead versions of several of its standard linear circuits. Fig. 3 is a photograph of a beam-lead version of the RCA CA3030 operational amplifier; while Fig. 8 is a version of the RCA CA3046 transistor array. In both cases, beam-to-beam spacings of ten mils are standard, because such tolerances are within the capability of generally available thick-film technology. Some complex circuits may require many leads; for example, 72 leads are needed for a current computer-memory element. In such cases, the area of the chip will be determined not by its active area but by the perimeter required to place the beams. The beam-lead wafer technology is capable of providing two-mil-wide beams on three-mil centers. A reasonable compromise with the assembly techniques, however, is the use of five- or six-mil centers. The use of narrow spacing represents a significant reduction in the area of silicon required and justifies the thin-film processing required for substrate preparation.

Problem areas

There are a number of difficulties en-

countered in translation of standard circuits to the beam-lead format. To eliminate unique bonding tools and substrate patterns for every different circuit, some standardization of pellet sizes has been initiated within the industry. This requirement will increase the average size of pellet in most instances.

The beam-lead wafer processing operations are not as mature as the standard and, today, have lower processing yields. Enough data has been obtained, however, to indicate that yield differentials eventually will be small between standard and beam-lead approaches. In addition, as new pellets are designed with the anticipation of a beam-lead format, the area differentials will vanish. Thus, an evolutionary transition to the beam-lead technology is anticipated for all low-power integrated-circuits.

Standard integrated circuits are usually mounted with the pellet back against the package for efficient heat transfer. With the face-down bonded beam-lead pellet, heat must be transferred through the leads. This arrangement limits chip dissipation. Improved mounting (such as mounting face up) and encapsulation techniques should significantly improve this situation.

Conclusion

The application of the silicon-nitride beam-lead technology to the fabrication of semiconductor integrated circuits provides a means for hermeticity at the chip and improved reliability in assembly operations. This technology is immediately applicable to the fabrication of high-performance hybrid circuitry and ultra-reliable packaged devices.

Acknowledgement

The basic beam-lead system described above was invented by Bell Telephone Laboratories. Its application to commercial linear circuits was achieved through the cooperative efforts of S. Husni and J. Mongioi of the Bipolar Engineering Group and W. Greig and J. Banfield of the Advanced Materials and Processes Group. In addition, valuable guidance was obtained by the Safeguard Engineering Organization.

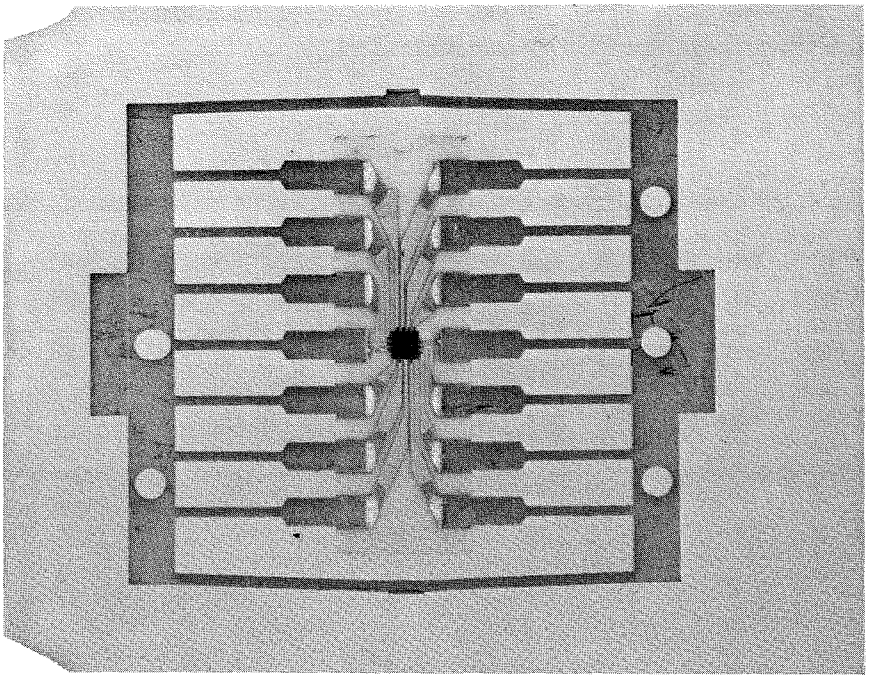

Fig. 5—Mounted pellet connected to a package substrate.

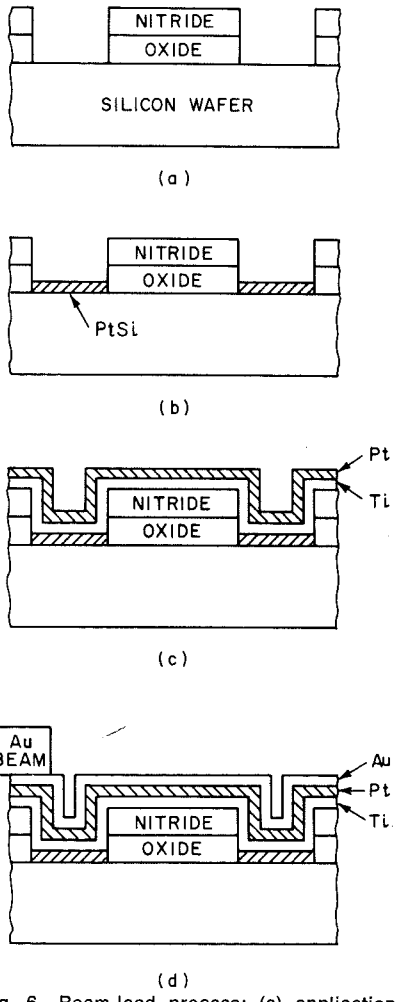

Fig. 6—Beam-lead process: (a) application of nitride and opening of contacts, (b) formation of platinum silicide, (c) sputtering of titanium and platinum, and (d) gold-plate interconnection and addition of beams.

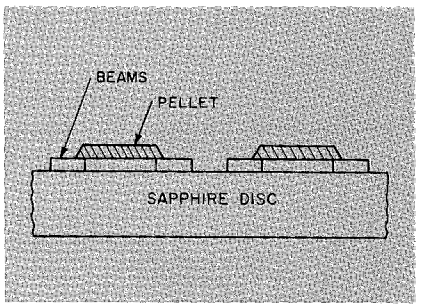

Fig. 7—Wafer mounted on sapphire disc, lapped to thickness of a few mils, and separated by etching.

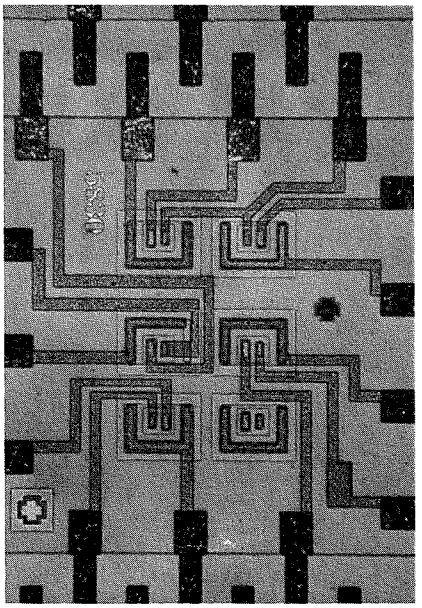

Fig. 8—A beam-lead version of the CA3046 transistor array.

Linear IC engineering

B. V. Vonderschmitt

Effective product engineering dictates that changes in technology be continually included in new products in proper balance to avoid early product obsolescence. Nevertheless, cost effectiveness is the most important measure of product-engineering excellence, and cost effectiveness applies not only to the component but to the total equipment that uses the component. Often, significant component and equipment cost tradeoffs can be made. For example, a more complex component may cost more, but the increase may be compensated by a reduction of equipment-manufacturing cost and maintenance. The objective, therefore, in product engineering of linear integrated circuits is to maintain a balance: to use improved technology and processes, and to increase device complexity to the extent that it is cost effective. Failure to achieve proper balance results in a non-competitive position for newly developed circuits. RCA's Linear Integrated-Circuit Engineering Group is a compartmentalized organization of engineering skills that provides an atmosphere of free interaction to achieve such a technology/cost-effectiveness balance.

THE DEVELOPMENT OF LINEAR INTEGRATED CIRCUITS requires contributions from six engineering groups whose efforts are logically compartmentalized to permit optimum focus of engineering experience in each area (see Fig. 1); at the same time, these groups maintain technical interaction on a constructive basis.

Five engineering groups are directly responsible to the engineering manager; the sixth group (Services and Support) is responsible to Engineering on a project basis. Services and Support Group has four significant areas: Advanced Materials and Processes, Equipment Technology, Packaging, and Standards. Probably the best way to understand the functions, responsibilities, and interactions of these groups is to follow the evolution of an integrated-circuit design from concept through introduction to manufacturing.

Process/technology development

Fig. 2 shows the major steps in the manufacture of an integrated circuit; the Process/Technology activity is centered in areas A and C. This activity develops new and improved components, modifies the process that these components require, and develops the necessary packaging. The objective of these efforts may be lower cost, higher power dissipation, improved reliability, or some combination of these.

After an improved or new component is produced, a specific circuit function, utilizing the component, is developed to test and define process variability. Within the engineering facility, this variability is established over a three to nine month period by distributions determined from completed units. After this period, a new device and the attendant process may be released for use in product design with a manufacturing and product commitment. The acceptance of a new process critically depends on successful life-test history.

In the development of new processes, this group calls on centrally located skills within the Solid State Division staffed by engineers and scientists who are specialists in diffusion techniques, metallurgy, plating, and packaging. Specifications and characteristics of new equipment that may be required in either the wafer processing or assembly area are prepared jointly with Equipment Technology. The actual design of hardware is assigned to this Equipment Technology Group which either develops the equipment or subcontracts to utilize skills in other RCA divisions or outside of RCA. In a normal development of a linear integrated-circuit product, which is committed for commercial announcement or specifically designed for a custom application, processes are always limited to those used on a previous design or those that demonstrate pilot product feasibility.

Circuit development

Fig. 3 illustrates the complete development cycle of a product—from objec-

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received the BSEE from Rose Polytechnical Institute, Terre Haute, Indiana and the MSEE from the University of Pennsylvania. Since joining RCA, Mr. Vonderschmitt was associated with Monochrome and Color Television Design as part of the Electronic Components Division and the Consumer Products Division. In 1959, he joined the Semiconductor Division, Somerville, New Jersey, working in the Microelectronics Department. In 1963 he became manager of Integrated Circuit Applications. In 1967 he became Manager of Linear Signal Device Engineering with responsibility for the development of Discrete Signal Devices and Integrated Circuits. In 1969 he became Manager of Product Engineering for Bipolar Integrated Circuits. He is a member of the IEEE, Tau Beta Pi, and is a registered professional engineer. He has been awarded 13 patents.

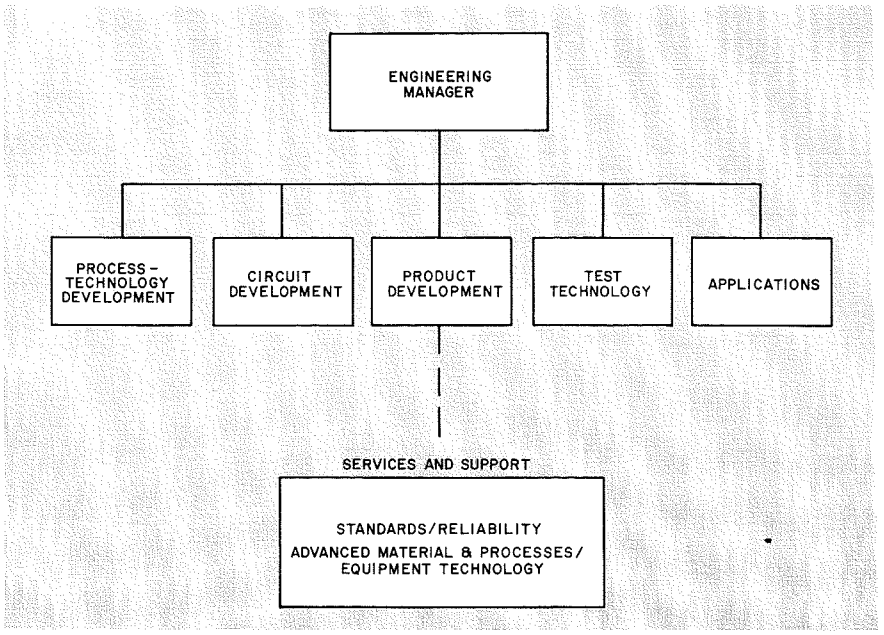

Fig. 1—The six engineering departments responsible for development of linear integrated circuits.

tive specifications to release of the design to manufacturing. Device requirements originate from different sources; some of these sources are as follows:

1) *Marketing development*—inputs may come from sales engineers whose daily contact with customers provides an excellent source of equipment designers' requirements.
2) *Custom requirements*—a specialized equipment manufacturer has a unique requirement best understood by him. During a review with the equipment manufacturer, the circuit development engineer develops preliminary specifications that are the basis for initial circuit work. Compatibility of the functional requirements and the cost constraints normally require three to four weeks of engineering effort to establish a basis to proceed or discontinue the development.
3) *Application engineering* — requirements for a product as developed by the internal Application Group or the Circuit Development Group.

After an initial requirement is defined and black-box specifications are developed, the Circuit Development Group details the component requirements and configures the circuit. Fig. 4 shows typical black-box specifications for a voltage regulator. This approach is normally used as the objective specification during the circuit development phase. In the development of the circuit, the Circuit Development Group is limited to processes and components compatible with the use of circuit elements. The following list of items constitutes the total circuit development cycle:

1) Configuration of a circuit, such as the specific circuit as shown in Fig. 5.
2) Development of a circuit breadboard using integrated components compatible with the selected process for all "active" (diodes and transistors) devices as shown in Fig. 6.
3) Simulation of the circuit and computer-aided analysis techniques are sometimes used to confirm the objective specifications particularly for performance characteristics such as high-frequency performance, coupling, and thermal interaction for which the physical size of breadboarding precludes simulation of the actual integrated device.
4) Generation of an updated specification which highlights deviation from the initial objectives.

At the completion of the circuit design, a design review is held at which the circuit design engineer gives a detailed review of the circuit concepts and any unique requirements which demand attention in circuit layout or which may be sensitive to process variations. Examples of particular requirements include:

Sensitivity of circuit performance as a result of beta variations;
Sensitivity to match between devices, i.e., beta and V_{BE} match between transistors;
Matching between resistors for which ratios are important to circuit performance;
Any portion of the circuit particularly sensitive to leakage; and
Any transistor requiring more than minimum (5 mA) current capability or more than a 10-V breakdown.

After the design is critiqued by the five engineering groups, another cost analysis is made to determine that the mature manufacturing cost and the objective selling price for the application are compatible. The most significant items that contribute to this cost are pellet area, pellet yield, and packaging —with pellet area being the largest contributor. At this point, the investment that will bring the circuit into successful production is between 10 and 20% of the total development cost; therefore, a review is needed to establish the economic feasibility of the product.

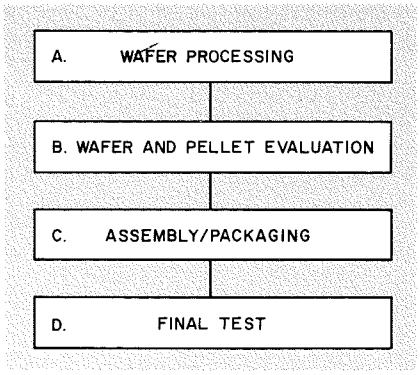

Fig. 2—Gross steps in the manufacture of an integrated circuit.

Product development

After the Circuit Development Group completes the design review and generates a comprehensive report describing the individual device requirements, the Product Development Group becomes the focal point of product development until the device is released to production. The initial layout (placement of critical components and position of bonding pads) is determined and jointly approved by the product development engineer and the circuit development engineer. After approval of the preliminary layout, the product development engineer prepares a specific layout and generates detailed drawings of the six to nine mask levels required to define the total circuit topology. The preparation of detailed drawings is completed through one of the two paths delineated in Fig. 3. By 1971, the automatic Mann generator will be utilized for a significant percentage of the designs. After completion of either the automatically generated artwork or manually prepared rubies, masks are

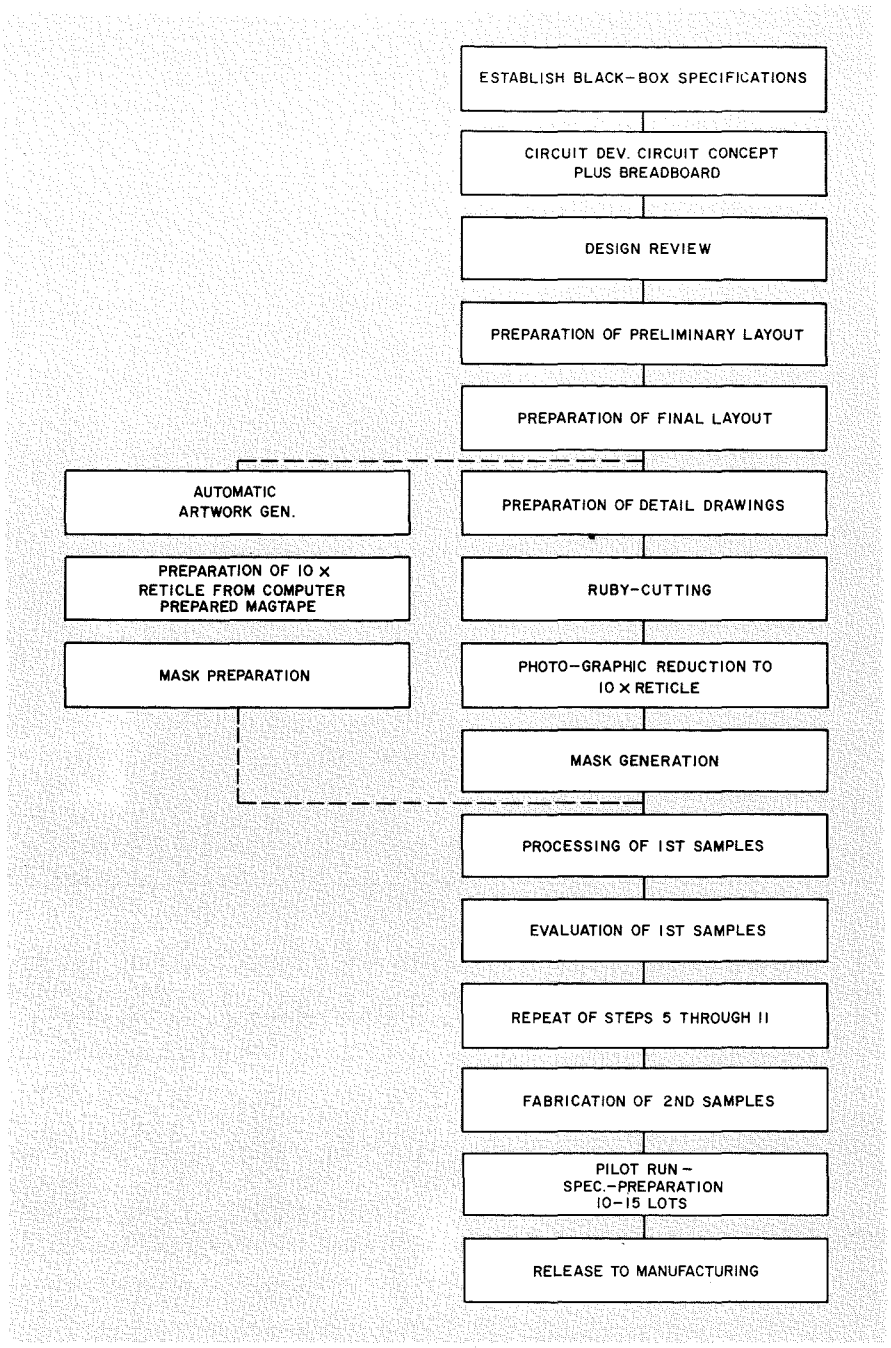

Fig. 3—Steps in the integrated-circuit product development.

Parameter	*Objective specification*	*Final specification*
Line regulation	0.3%	0.56% (min)
Temperature coefficient	0.004%/°C	0.0025%/°C (typical)
Input voltage range	7.5 V (min), 40 V (max)	7.5 V (min), 40 V (max)
Output voltage range	1.6 to 36 V	1.8 to 34 V (max - min and min - max)
Standby current drain	4.5 mA	10 mA (max) 7.5 mA (typical)
Output noise voltage	Not specified	0.45 mV (typical)

Fig. 4—Objective specifications of a voltage regulator.

prepared and devices are processed for initial evaluation. Evaluation of these devices is done jointly by the original circuit development engineer and the product development engineer.

The Product Development Group continues to function as the focal point during the remainder of the product development cycle. The product development engineer is, in essence, the project engineer on each device, from circuit design release through introduction into Manufacturing. The significant contributions that the Product Development Group makes during the remaining development of a product are as follows:

1) In the normal development cycle, first-cut samples have either gross or marginal operational problems resulting from either layout errors, circuit configuration, or parasitic effects which are not properly simulated during the breadboard phase. In concert with the circuit development engineer, the product development engineer diagnoses problems and proposes alternate layout or processing methods.
2) During the checkout of a complete circuit for which test points are available only at nodes connected externally, internal components, particularly resistors, are probed for absolute value as well as ratio to other resistors in the circuit. It is a function of the Product Development engineer to probe all components to insure proper centering and matching of devices.
3) "Test keys" located at five diverse points on the wafer are designed into the wafer for process control purposes. These "test keys" have metallization options differing from the standard circuit. These options permit separate probing of critical transistor and resistor values for such critical process determining items as the beta of the transistors, the voltage breakdown of the transistors, and the absolute values and matching of the resistor values. The pattern selected is such as to permit maximum information to control wafer processing through measurement of individual transistors and resistors. This arrangement simplifies the analysis necessary for control by definition of the basic processing problems as opposed to basic circuit problems.
4) The process to be used for a particular type is defined by the product development engineer. He also determines reliability of the device and provides early interface with Manufacturing on all technical questions associated with manufacturing of the unit. An additional important responsibility after the first successful fabrication of the device during the engineering development cycle is the determination of the circuit probe and final test yield to define the cost of the unit after release to Manufacturing. A significant part of this function relates to the achievement of realistic specifications from the Application Group. These specifications must permit devices to be accepted provided the process is within the normal manufacturing process variations. The validity and practicability of the specifications are corroborated in the engineering-development model shop by a series of five to fifteen processed lots consisting of five to ten wafers per lot. The circuit-probe yields and final-

test yields that use proposed specifications as criteria are determined from a sample of these wafers. During the processing of these samples, process variations are purposefully made that most significantly affect the circuit performance.

Application engineering

The functions which are the prime responsibility of the Application Enneering Group include the following:

1) This group prepares a Master Specification which defines the static and dynamic parameters for Manufacturing. In addition, this group prepares the environmental and life-test conditions and defines the failure criteria and the permitted failure rate.

2) Application Engineering also prepares data sheets which describe to the customer the circuit characteristics. An important consideration is that the data sheet defining the device for a customer must completely agree with the Master Specification sheet which defines the circuit performance from the component manufacturing viewpoint.

3) Finally, Application Engineering assists equipment manufacturers in the integration of the device into an equipment function. This assistance involves printed-board layouts for the device for stabilization considerations, definition of peripheral components required in the normal circuit operation, maximum voltage, current and power ratings, and a check of the specific application to insure that the device is being operated within the rating under all normal equipment operating conditions. On those devices which have general purpose applications, it is customary for the application engineer to prepare an Application Note that describes various functions that the circuit can perform. The more specific the circuit application, the less useful the Application Note, because the equipment user is in a better position to understand the application than the application engineer handling the component.

Test technology

The testing of integrated circuits can be the most expensive part of the total manufacturing process. Testing is defined as circuit probing of the pellet while it is still in wafer form. It also includes performance of the final static and dynamic tests to assure conformance to the Master Specification Sheet. Automatic static (DC) testers are available that permit segregation of product into failed and varying classes of acceptable categories. These commercial equipments, however, have failed to provide sufficient capability for "on-line" data reduction to permit easy data analysis that defines failure modes. Data analysis is necessary to provide process feedback related to circuit failures that are not discernible from the individual components described earlier. In addition, complex linear circuits require as many as twenty-five dynamic tests which cannot be completed with one test insertion. The Test Technology Group has the responsibility to define and design this specialized equipment (with support from the central Equipment Technology Group).

The functions of the Test Technology Group fall into three broad categories.

1) This group prepares test-equipment specifications for major test systems used in both the engineering and manufacturing evaluation of the unit. This equipment includes automatic dc testers and data gathering and data reduction systems used for process control.

2) Test Technology group also prepares dynamic testers which perform normal linear tests of gain, frequency response, linearity of gain, noise figure, distortion, output power, and many other measurements required for custom-designed linear circuits.

3) Finally the group prepares detailed test programs for automatic testing of devices. This function includes not only the details of the program generation but assurance that the device is stable (in the oscillation) in the test environment under all test conditions.

Summary

The development of linear integrated circuits involves the proper application of diverse engineering disciplines. For cost effectiveness the processes and packages must permit design of technologically competitive circuits. Further, with a specific process base, circuit configurations must be optimized in consideration of that process; also, circuit layouts and topology must be prepared for optimum yield under the direction of the product development engineer, and the devices must be characterized for the customer and specified to Manufacturing in accordance with the basic circuit design and the process capability. In addition, the units must be evaluated and tested with equipment that minimizes labor costs and ambiguity in test results. The Linear Integrated Circuit Activity develops specialized knowledge in each of five areas, and is encouraged to have continuing engineering interaction during the total product development period. This interaction results in the proper balance of technological advancement, circuit innovation, cost effectiveness, manufacturability, and customer acceptance.

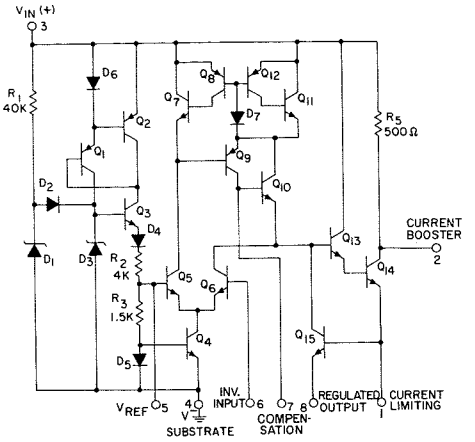

Fig. 5—Circuit diagram of RCA CA3055.

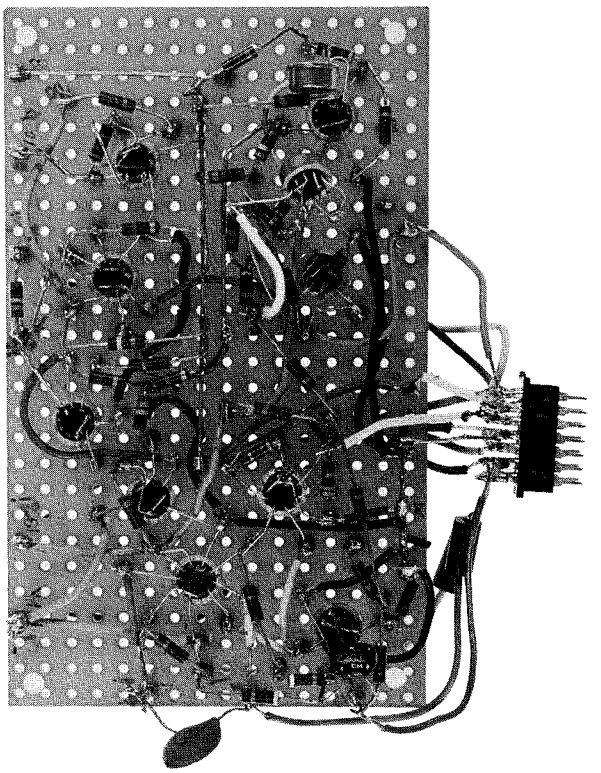
Fig. 6—Circuit breadboard using integrated components compatible with selected process for all "active" (diodes and transistors) devices.

Linear integrated-circuit arrays—building blocks for designers

H. M. Kleinman

This paper describes some design guidelines which should be followed for most effective use of linear IC arrays, discusses some basic configurations that serve as "building blocks" in the design of complex monolithic circuits, and presents some typical circuits that illustrate the application of linear IC arrays.

RCA HAS DEVELOPED a number of linear integrated circuits consisting only of active devices, i.e., transistors and diodes. These arrays (Fig. 1) are extremely useful in circuit design because they provide the close electrical and thermal matching of device characteristics inherent in all monolithic integrated circuits, but are not limited by the restrictions applicaple to passive elements (resistors, capacitors, and inductors) in the monolithic system. Besides making practical many circuits which cannot be constructed economically with descrete devices, these arrays may also be used for the "breadboarding" of complex monolithic circuits.

The simplest of these integrated-circuit arrays are finding wide commercial acceptance in a variety of fields because they provide the circuit designer with economical, easily handled packages of matched semiconductor devices. To date, high volume commercial usage has included audio amplifiers for automobile radios, sense amplifiers for small scale computer memories, balanced amplifiers for AC and DC instruments, relaxation, oscillators, for muscle stimulators, DC-operated audio attenuators, and waveshaping networks for function generators. The key to success is the ability of these IC's to provide matched components for prices very close to the cost of similar unmatched devices. The CA3046, for example, provides five transistors for 98 cents (in quantities of 1000 and up), or less than 20 cents per transistor. [Price based on the time that this article was written.]

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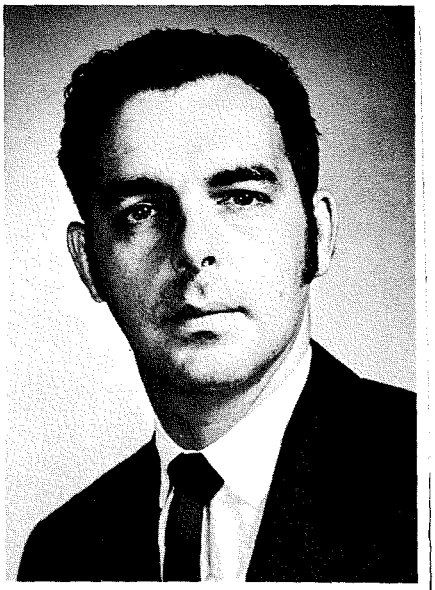
General design guidelines

If linear IC arrays are to be used to best advantage in circuit design, some basic rules must be observed to assure proper device operation and to avoid damage to the IC chip. Perhaps the most important rule is that the collector voltages of all array transistors must be kept positive with respect to the IC substrate. As shown in Fig. 2, the collector region of each N-P-N transistor is isolated from the P-type substrate material by an effective diode (N-P junction) which must always be reverse-biased for normal transistor operation. The emitter and base regions of the transistor may be negative with respect to the substrate, provided the collector-to-emitter and collector-to-base voltage ratings are not exceeded.

It is also important to prevent forward-biasing of the base-to-collector diode of a monolithic transistor to assure normal operation. The base-to-collector voltage should not be permitted to exceed 0.6 volt unless the current in the base lead is limited by a fairly large resistor (1000 ohms or more). As shown in Fig. 3, the fabrication of a monolithic N-P-N transistor in a P-type substrate produces the structure for an associated P-N-P transistor in which the collector is the substrate, the base is the collector of the N-P-N transistor, and the emitter is the base of the N-P-N transistor. If the base-to-collector junction of the N-P-N transistor becomes forward-biased, therefore, high currents can flow into the substrate unless limiting is provided in the base lead. Unwanted currents can also develop if the collector of the N-P-N transistor is left open because the P-N-P transistor then operates in the V_{CEO} mode.



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received the BSEE and MSEE from MIT. He joined RCA in 1957. He is presently responsible for evaluating devices, developing test equipment, establishing test specifications, and preparing technical data for commercial data sheets and application notes for both consumer and non-consumer linear integrated circuits. Mr. Kleinman has been granted three U.S. patents and has published several articles. He has received two RCA Engineering awards. The first was a divisional team award in 1963 for the development of devices and circuits which introduced the era of commercially practical solid-state audio amplifiers. The second was the 1966 David Sarnoff Team Award in Engineering for the development of the first commercial high voltage silicon power transistor.

Another important consideration in the use of linear IC arrays is the maximum dissipation rating for the integrated circuit. This rating is based on the sum of the dissipations of the individual devices in the array. Therefore, total dissipation must be calculated on the basis of all the devices operating in a given application.

A final point to be remembered is that the close electrical and thermal matching mentioned previously applies only to devices fabricated on the same IC chip. When several arrays are to be used in a circuit, the design should employ devices of a single array to provide matched characteristics when they are required.

In addition to these few general rules for proper device operation, some basic configurations should be recognized and used as "building blocks" in the design of complex monolithic circuits. Several of these configurations have been described in another paper.[1]

Design ideas for RCA CA3018, CA3018A, CA3045, and CA3046 transistor arrays

The RCA CA3018, CA3018A, CA3045, and CA3046 transistor arrays

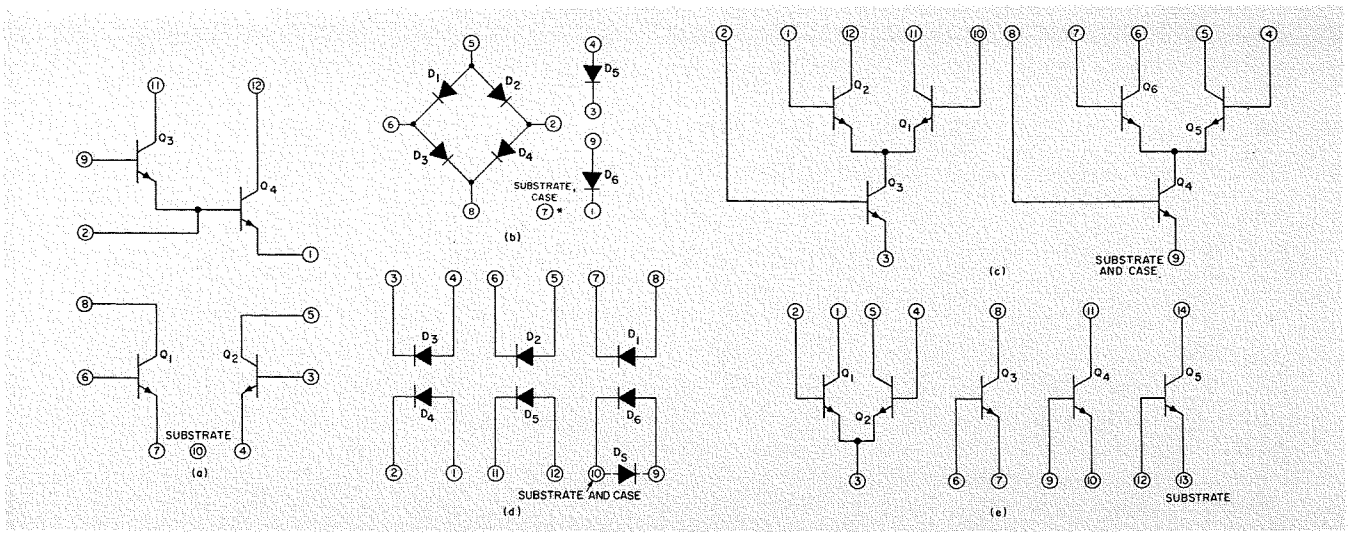

Fig.1—Schematic diagrams of RCA linear IC arrays:
(a) CA3018; (b) CA3019; (c) CA3026, CA3054; (d) CA3039; (e) CA3045, CA3046.

consist of closely matched general-purpose silicon N-P-N transistors on a common monolithic substrate; the schematic diagrams for these arrays are shown in Figs. 1a and 1e. Although the specification limits for the different types vary (as shown on the individual data sheets), the transistors in all these arrays have the following typical characteristics:

Collector-to-base voltage (V_{CBO})	60V
Collector-to-emitter voltage (V_{CEO})	24V
Emitter-to-base voltage (V_{EBO})	7V
Small-signal forward-current transfer ratio (h_{fe} at I_C = 1 mA)	100
Gain-bandwidth product (f_T)	550MHz

The CA3018 and CA3018A (Fig. 1a) consist of four transistors packaged in a 12-lead TO-5 can; the only difference between the two types consists of tighter control of some characteristics for the CA3018A. The CA3045 and CA3046 "handy pack" arrays (Fig. 1e) provide a more flexible arrangement of five transistors in 14-lead dual-in-line packages (ceramic and plastic, respectively).

The general-purpose transistors in these arrays are well suited to a wide variety of applications in low-power systems at frequencies from DC through the VHF range. They may be used as discrete devices in conventionally designed circuits to achieve the advantage of improved packing density. However, their full advantage will be realized only when the circuit design makes use of the close electrical and thermal matching of the devices on each IC chip.

Several possible applications for these arrays are presented in the following paragraphs. For some of these circuits, performance is well documented;[2] others are design ideas which have not been proven out. Many circuits do not make use of all the devices on a chip; others require extra components. In general, these applications are presented to suggest the potential uses of these arrays of matched transistors; they should serve as a beginning to stimulate the thinking of circuit designers.

Differential amplifiers

The CA3018, CA3018A, CA3045, and CA3046 arrays are suitable for use in a wide range of differential-amplifier applications, particularly in tuned-amplifier, mixer, IF amplifier, and limiter service. Because the transistors in these arrays are similar to those used in the CA3004, CA3005, CA3006, CA3028A, and CA3028B RF-amplifier integrated circuits, the performance of the RF-amplifier types gives an excellent indication of the potential operation of the arrays.[3,4,5] Some caution is required when the CA3045 and CA3046 dual-in-line circuits are used in high-frequency applications because capacitive coupling between the leads of these packages is greater than in the TO-5 packages. However, if care is taken to reduce capacitive coupling from input to output, these arrays are suitable for operation from DC to 100 MHz.

Fig. 4 shows the schematic diagram for the RCA-CA3028A and CA3028B integrated circuits. The operating point of the circuit is stabilized by a 500-ohm emitter resistor for transistor Q_3. At the normal operating current of 6 mA, this resistor represents a voltage drop of about 3 V from the power supply.

Fig. 5a shows the CA3028A or CA3028B connected as a differential amplifier and limiter, and Fig. 5b shows an equivalent circuit that uses the transistors in a CA3046 array. It can be seen that fewer external components are required when the array is used. In addition, the CA3046 can provide as much dynamic range when operated from a 6-V supply as the CA3028A or CA3028B operated from a 9-V supply, and more gain and output power can be obtained from the CA3046 when a 9-V supply is used.

One disadvantage of the circuit shown in Fig. 5b is that the current drain is higher because the bias transistors draw the same current as the amplifier. This current can be reduced by use of two transistors in parallel for the constant-current source, as shown in Fig. 6. In this circuit, both Q_3 and Q_4 draw the same current as the bias transistor Q_5; as a result, the bias current may be reduced by 50%. It should be noted, however, that the base of transistor Q_2 must be bypassed

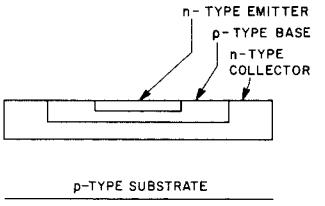

Fig. 2—Structure of an N-P-N monolithic transistor.

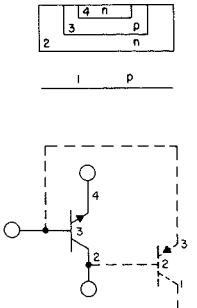

Fig. 3—Associated P-N-P transistor inherent in monolithic fabrication.

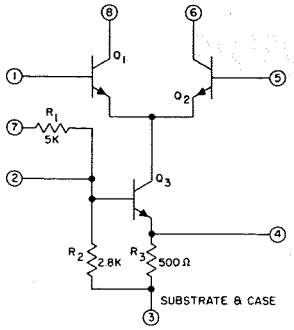

Fig. 4—Schematic diagram of CA3028A or CA3028B RF amplifier.

[no bypassing is required in the circuit of Fig. 5b because of the low-impedance connection through the diode-connected transistors to ground].

Automatic gain control (AGC) may be applied to the differential amplifiers shown in Figs. 5 and 6 by reduction of the current in the biasing device(s). However, the high current in the bias circuit makes it necessary to include DC amplification of the AGC signal. Fig. 7 illustrates the use of the fifth transistor of a CA3046 array as an AGC amplifier. Full AGC capability is realized with a positive-going AGC voltage.

Although the differential amplifiers shown have single-ended input and single-ended output and operate from a single power supply, the arrays shown in Figs. 1a and 1e can also be operated from dual supplies or with balanced inputs. In addition, the arrays provide better control for operation with DC loads than the RF-amplifier integrated circuits mentioned above.

Cascade amplifiers

Operation of the CA3045 or CA3046 array as a cascode amplifier is illustrated in Fig. 8. In this circuit, the diode-connected transistor Q_4 serves as a temperature-compensated base-bias supply for the input transistor Q_5. The secondary winding of the input transformer T_1 is connected between Q_4 and Q_5. The DC resistance of this connection should be less than 20 ohms to assure accurate control of the operating current. The AGC is applied to the circuit by means of a positive-going voltage at the base of Q_1. Fig. 9 shows an adaptation of the cascode amplifier which permits the use of a grounded signal source. In this circuit, the DC resistance of the source must be less than 1 ohm for accurate control of bias. If the DC source impedance is greater than 1 ohm, a matching resistor should be inserted in the emitter circuit of Q_3. Loss of gain can be kept to a minimum provided this resistor is smaller than 5 ohms. The cascode-amplifier techniques discussed can be readily applied to such applications as balanced mixers, product detectors, and other variations.[3]

Wideband video amplifiers

Fig. 10 illustrates the use of the CA3018 (or four transistors of the CA3045 or CA3046) to provide a wideband video amplifier with a gain of 49 dB and a bandwidth of 30 MHz.[2] This amplifier may be considered as a cascode of two direct-coupled stages. Gain of the amplifier is constant within 1 dB over the entire temperature range.

The adaptability of the devices in the CA3045 and CA3046 arrays is best illustrated by the tachometer circuit shown in Fig. 11. This circuit is designed to provide a full-scale current of 1 mA at an engine speed of 5,000 revolutions per minute (r/min) with an eight cylinder automobile engine. In this circuit, Q_5 acts as a switching transistor, Q_4 as a zener diode, Q_1 (used as a diode) and Q_2 form a current transfer circuit, and the collector-to-substrate diode of Q_1 (shown dotted) is used to provide a path to discharge the capacitor C. Calibration of the system may be changed, by changing the value of capacitor C:

$$C = \left(\frac{I}{V}\right)\left(\frac{pulses}{revolution}\right)\left(\frac{revolutions}{minute}\right)\left(\frac{1\ minute}{60\ seconds}\right)$$

where I and the number of revolutions per minute are full-scale values. The number of pulses per revolution is four for an eight cylinder engine and three for a six cylinder engine; V is approximately equal to zener voltage. For high-speed operation, it may be necessary to reduce the one kilohm-resistor in the collector of Q_5 to 470 ohms.

Operational amplifiers

Although integrated-circuit operational amplifiers have become widely used general-purpose devices, many applications require features which are not readily available in fully integrated form. The CA3045 and CA3046 arrays are especially suited to the construction of special-purpose operational amplifiers for battery-operated equipment in which low current drain and good performance at low supply voltage are extremely important.

Fig. 12 shows the schematic diagram of an "op-amp" meter amplifier using two CA3046 arrays. The circuit is designed to drive a 1-mA DC meter to full scale in the positive direction only. The open-loop voltage gain is 80 dB, and the input bias current is less than 20 nA.

The first CA3046 is connected to form a Darlington-connected differential amplifier similar to the first stage of a CA3033. This stage operates at a current level of less than 40 μA. The Darlington-connected pairs have a composite beta in excess of 1000, and therefore provide an input bias current of less than 20 nA. Transistor Q_{4b} of the second CA3046 is used as an impedance-matching level shifter to drive the voltage amplifier Q_{1b} and Q_{2b}. Transistor Q_{3b} is an emitter-follower output. Transistor Q_{5b} is used to keep Q_{3b} from cutting off when the output is at zero volts. Capacitors C_1 and C_2 reduce the high-frequency gain to avoid the possibility of oscillation with feedback. Standby current drains are 500 μA from the positive supply and 200 μA from the negative supply, for a total dissipation of about 2mW. A total meter resistance (R_m) of 1000 ohms is recommended. Various feedback techniques can be used to tailor the amplifier to specific applications.

Other uses

The ability to use the matched device characteristics of IC arrays to replace bulky bypass elements is illustrated in Fig. 13 if R_{C2} is selected for maximum output-voltage swing and R_B is

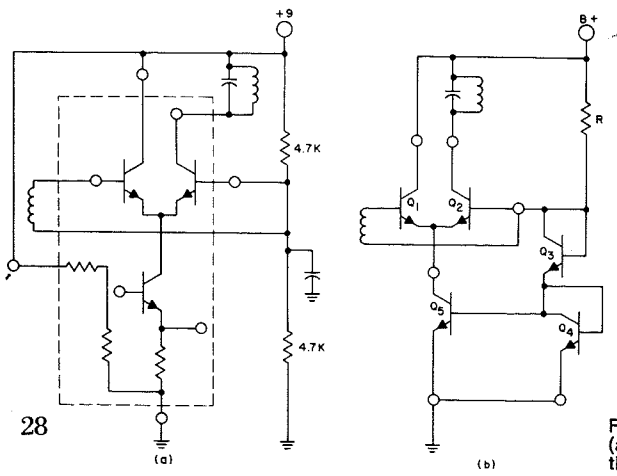

Fig. 5—Differential-amplifier/limiter circuits (a) for the CA3028A or CA3028B and (b) the CA3046.

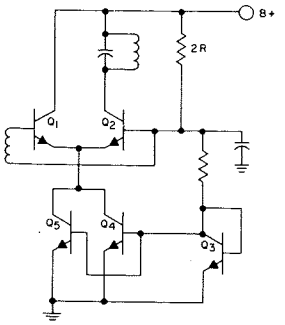

Fig. 6—CA3046 differential-amplifier/limiter circuit with reduced current drain.

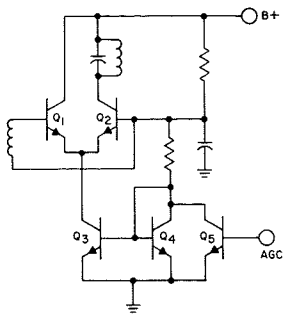

Fig. 7—CA3046 differential amplifier using Q_5 for AGC amplification.

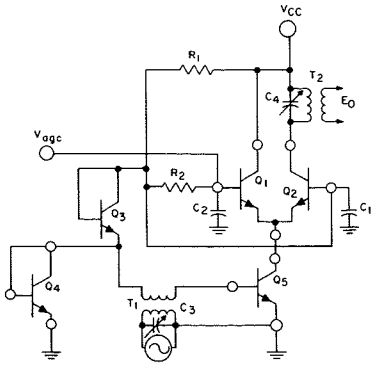

Fig. 8—Cascode-amplifier circuit using CA3045 or CA3046 array.

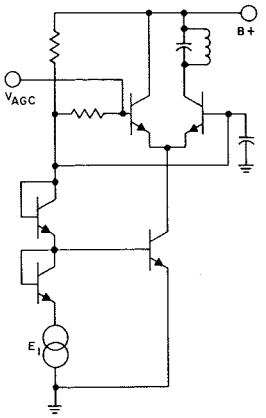

Fig. 9—Cascode amplifier with grounded input.

selected so that I_{C2} does not change more than ±10% from its center value as the beta of Q_1 changes from minimum to maximum, the circuit of Fig. 13a has the characteristics and typical performance shown in Table I. (However, the circuit is easily tailored to different requirements.) If it is desired to maintain the input impedance and gain of the circuit within 3% of the midband values at a low frequency of 20 Hz, C must have a value approaching 3000 μF. Although C is a low-voltage capacitor, for this requirement it becomes a large and expensive component.

The circuit of Fig. 13b shows how the matched characteristics of the CA3046 may be used to eliminate this large capacitor. In this circuit, Q_2 and Q_3 are connected in the same manner as in the circuit of Fig. 13a, except that no AC signals are applied to these transistors. Provided all the resistors are matched within 1 or 2%, the current in Q_1 is the same as that in Q_2. The voltage drop across the diode-connected transistor Q_2 then exactly compensates for the drop across R_E in the circuit of Fig. 13a. The operating points of Q_1 and Q_5 are at the levels desired, and the dynamic performance is the same as that of the discrete-component circuit.

Design ideas for the RCA-CA3026 and CA3054 dual-differential-amplifier array

The CA3026 integrated-circuit transistor array consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six N-P-N transistors which comprise the amplifiers are general-purpose devices similar to those in the arrays and IC's described previously. These transistors exhibit low $1/f$ noise and a value of f_T in excess of 300 MHz; these features make the CA3026 useful from DC to 120 MHz. Bias and load resistors are omitted in the array to provide maximum application flexibility.

The schematic diagram of the CA3026 is shown in Fig. 1c. The most obvious advantage of the array is an improvement in packaging density; the circuit provides two differential amplifiers in one package instead of one differential amplifier per package as in the case of the popular CA3028A and CA3028B. This more compact packaging of differential amplifiers results in simultaneous economic advantages. However, the two matched amplifiers of the CA3026 provide other advantages which transcend anything previously available in either tubes or solid-state devices.

Although doubly balanced circuits are not new, they have not been commonly used because of the difficulties encountered in obtaining components which are truly matched and which maintain their match despite variations in temperature and the passage of time. While the procurement of matched passive components (e.g., center-tapped coils, matched resistors, and the like) has been merely tedious, provision of matched active components (e.g., tubes and transistors) has been both difficult and costly. However, the CA3026 provides matched active components in the proper configuration for the design of customized doubly balanced circuits. Some typical doubly balanced circuit configurations are described in the following paragraphs.

Four quadrant multiplier modulator

The matched differential amplifiers of the CA3054 (Fig. 1c) are ideal elements for the construction of a so called "doubly balanced circuit." This configuration is the basis for many multiplier, modulator, and demodulator circuits. A typical circuit of this type is shown in Fig. 14. The doubly balanced designation is justified because the circuit is balanced for both inputs. When the 100-ohm balancing potentiometers are properly adjusted, neither input signal appears at the output. The waveform photos of Figs. 15a through 15d show the squaring of a 200-Hz sinewave, a 500-Hz triangular wave, a 1-MHz sinewave, and a 5-MHz sinewave, respectively. Note that the response at 5 MHz is about 3 dB below that at low frequency. Fig. 15e illustrates double-sideband suppressed-carrier modulation of a 5-KHz sinewave by a 100 Hz triangular wave with the modulation wave superimposed to indicate the linearity. The phase reversal of the carrier as the modulation changes polarity is easily seen.

A CA3018 is used to complete the circuit. Transistors Q_1 and Q_2 form the constant current source for the multiplier, while Q_3 and Q_4 provide a high impedance load for the modulator and a low output impedance.

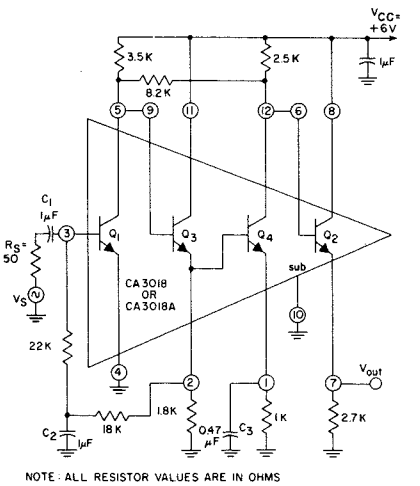

Fig 10—Wide-band video amplifer using the CA3018.

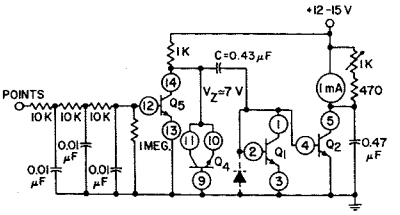

Fig. 11—Tachometer circuit showing a wide variety of uses for the devices, e.g. zener operation, diodes, switches, and substrate diodes.

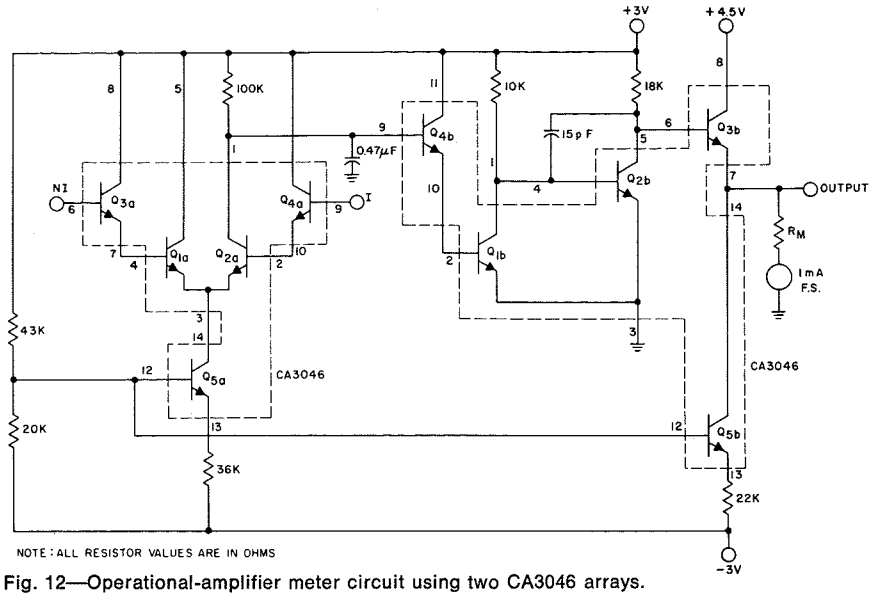

Fig. 12—Operational-amplifier meter circuit using two CA3046 arrays.

Table I—Approximate characteristics for the circuit of Fig. 13.

$$\text{Voltage gain} = \frac{(V^+ - 2V_{BE})^2}{2(0.026)^2}\left[1 + \frac{(V^+ - 2V_{BE})}{0.026\beta_2}\left(\frac{I_{C1}}{I_{C2}}\right)\right]^{-1}$$

$$R_{in}\ (min) = \frac{0.022\beta_1\ (min)}{I_{C2}} \quad ; R_B = \frac{0.140\beta\ (min)}{I_{C1}} \quad ; R_{C1} = \frac{V^+ - 2V_{BE}}{I_{C1}}$$

$$R_{out} = R_{C2}\ ; R_E = \frac{V_{BE}}{I_{C2}} \quad ; R_{C2} = \frac{V^+ - V_{BE}}{2I_{C2}}$$

Example

$V^+ = 12V$	$R_{C1} = 0.1$ megohm
$V_{BE} \cong 700mV$	$R_{C2} = 5600$ ohms
$I_{C2} = 1mA$	$R_B = 42{,}000$ ohms
$\beta_2 = 100$	$R_E = 700$ ohms
$\beta_1\ (min) = 30$	

$$\text{Voltage gain} = 2.12 \times 10^3 \cong 67dB$$
$$R_{in}\ (min) = 6600 \text{ ohms}$$
$$R_{out} = 5600 \text{ ohms}$$

Synchronous detector

A synchronous detector is another example of a doubly balanced circuit. Fig. 16 shows a simplified synchronous detector using the CA3026 which can be used to detect both the phase and the amplitude of a TV chroma signal. In this circuit, the reference signal is fixed in both phase and amplitude at 3.58 MHz. The chroma input signal varies in both phase and amplitude in accordance with the hue and saturation information, respectively. The TV detector must compare the steady reference signal and the varying chroma input signal without causing interaction between the two signals, and must cancel the reference signal without resorting to elaborate filtering systems in the output. A doubly balanced demodulator is an ideal means of accomplishing this objective. Although a rigorous analysis of this circuit is beyond the scope of this paper, a brief description of the circuit configuration is given below.

Transistors Q_3 and Q_4 are connected as a differential amplifier for the chroma signal input, and supply opposite-phase chroma signals to the transistor switches Q_1, Q_2 and Q_5, Q_6. The chroma-signal currents flow from Q_3 and Q_4 into either of the output leads in accordance with the instantaneous state of each transistor switch. The state of the switch is entirely dependent upon the reference signal applied to its base. In essence, the reference signal performs synchronous switching at its frequency of repetition. By the synchronous comparison process, it is possible to produce an output signal which is a function of the instantaneous phase difference between the chroma and reference signals. Because both the chroma and the reference signals enter into balanced-differential networks, the circuit is doubly balanced. It can also be shown that amplitude variation in the chroma input (with fixed-amplitude reference input) produces corresponding amplitude variations in the chroma video output.

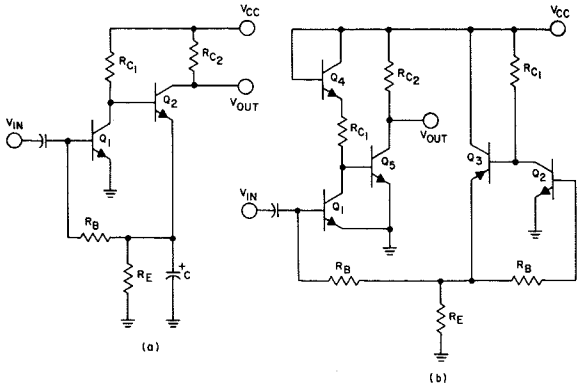

Fig. 13—Circuits illustrating the use of a CA3046 array to eliminate a bulky capacitor.

Although the doubly balanced circuit of Fig. 16 could be built with matched discrete transistors, the need for multiple matched devices would make it expensive. Furthermore, matching would deteriorate as a result of temperature variations and there would be a serious degradation in performance. The circuit could also be built with two single-stage differential amplifiers, such as a pair of CA3028A or CA3028B devices, with Q_1 through Q_3 in one package and Q_4 through Q_6 in another package. Even if selected pairs of CA3028A or CA3028B packages were used, however, serious mismatching could still occur with temperature variations. Because the CA3026 contains the required six transistors on the same chip, it has excellent pair-matching characteristics; in addition, tracking of characteristics is maintained with variations in temperature.

Design ideas for the CA3019 and CA3039 diode arrays

The CA3019 and CA3039 arrays (Figs. 1b and 1d) consist of six ultra-fast, low-capacitance diodes on a common monolithic substrate. Integrated-circuit construction assures excellent static and dynamic matching

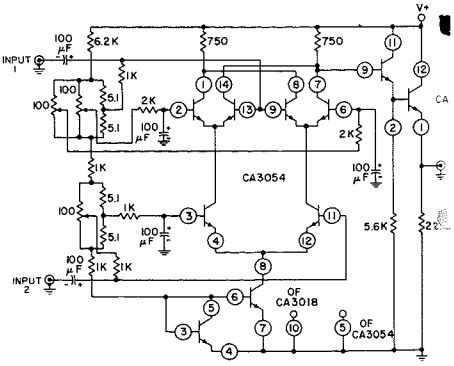

Fig. 14—High-frequency four-quadrant multiplier/modulator with provision for adjustment of all parameters 200Hz to 5MHz.

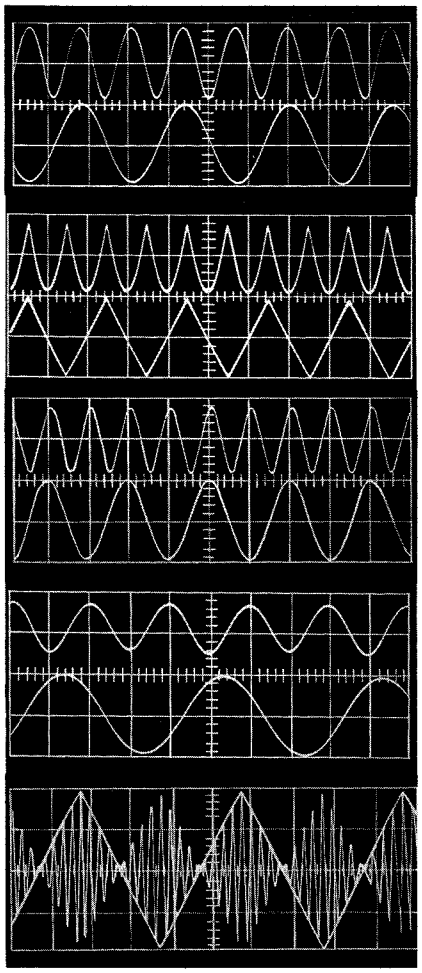

Fig. 15—Input and output waveforms for the multiplier/modulator in Fig. 14 operating from 200Hz to 5MHz.

of the diodes and makes the arrays extremely useful in a wide variety of applications in communications and switching systems. In the CA3019, four diodes are internally connected on a diode-quad arrangement; the other two diodes are independent. In the CA3039, five of the diodes are independently accessible; the sixth shares a common terminal with the substrate.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, these arrays are particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes.

Applications of the CA3019 have been described previously.[5] The six diodes in the CA3039 can be connected in a number of ways for use in voltage-regulator circuits, bias and current-limiting circuits for constant-current sources and SCR triggering circuits, direct-coupled transistor amplifiers, signal limiting and clamping circuits, logic gates, level-shifting circuits in DTL (diode-transistor-logic) circuits, and varistor circuits. The following paragraphs describe a few practical circuits to stimulate the thinking of potential users.

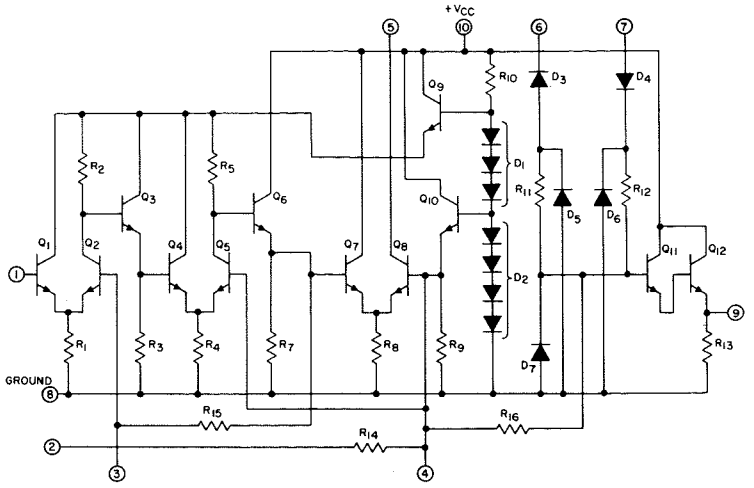

Fig. 18—Schematic diagram of the CA3014 IF amplifier/discriminator/AF amplifier for FM.

Low-voltage regulator circuit

The six diodes in the CA3039 may be connected in series, as shown in Fig. 17, to protect against voltage changes in a voltage source. Thus, the CA3039 is able to provide a regulated voltage output of approximately 4.5 V. Higher voltages may be regulated by connection of an appropriate number of CA3039 arrays in series. The type of regulator shown in Fig. 17, when coupled with the package flexibility offered by the CA3039, can also supply intermediate values of voltage in applications requiring base-biasing. The schematic diagram of the CA3014 FM IF amplifier/discriminator/AF amplifier, shown in Fig. 18 illustrates the manner in which supply potentials for a complex solid-state circuit can be regulated by a diode-connected series-string configuration similar to that of the CA3039. A monolithic series-string regulator can also provide base and collector potentials which track in the face of temperature variations.

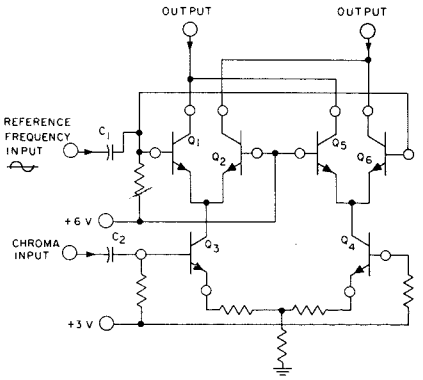

Fig. 16—Synchronous detector using a doubly balanced circuit.

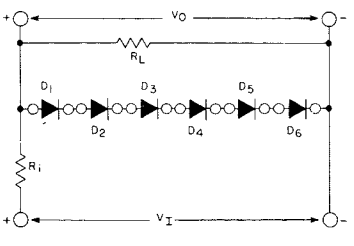

Fig 17—Low-voltage regulator circuit.

Biasing and current limiting for push-pull amplifiers

The amplifier shown in Fig. 19 is a complementary push-pull configuration driven by a class-*A* driver-amplifier device. Resistor R_2 serves as a common path for AC and DC feedback. The diode pair D_1, D_2 biases the output stage in such a way that crossover distortion is minimized while temperature compensation is provided to keep the idling current stable. The other two diode pairs—D_3, D_4 and D_5, D_6—are connected in such a manner that they limit the emitter current in the output transistors and thereby protect them. This emitter-current limiting technique is also applicable to single transistors, as shown in Fig. 20. The maximum emitter current is equal to $(V_{CC}-V_{be})/R_E$, and is relatively independent of load, base drive, and the power supply. This configuration can be used for current-limiting service in amplifiers, switching circuits, and voltage and current regulators.

Signal limiting and clamping circuits

Four diodes of the CA3039 may be connected as shown in Fig. 21 to provide limiting or clamping and a choice of two voltage levels, approximately 3 V or 1.5 V peak to peak.

Logic circuits

The diodes of the CA3039 can be connected to form either passive or active logic gates. Fig. 22 shows five-input OR and NOR gates using five of

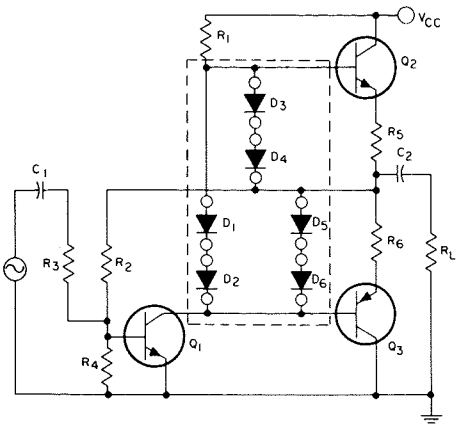

Fig. 19—Complementary push-pull amplifier driven by class-A drive-amplifier device.

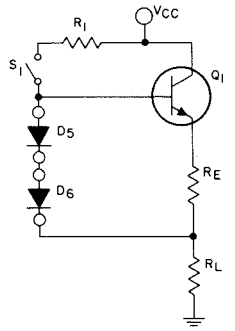

Fig. 20—Emitter-current limiting circuit for single transistors.

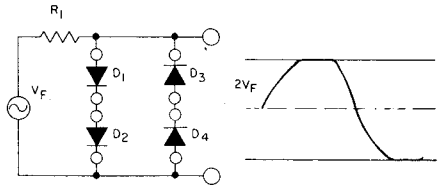

Fig. 21—Use of four diodes of the CA3039 to form a limiting or clamping circuit.

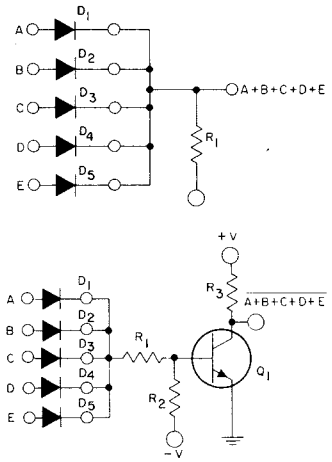

Fig. 22—Five-input "OR" and "NOR" gates.

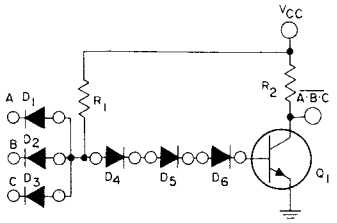

Fig. 23—Use of CA3039 diodes in a NAND gate to provide level shifting.

the CA3039 diodes. The diodes can be connected to provide for level shifting in a NAND gate (Fig. 23) so that only one power supply is required.

Varistor circuits

A varistor is a device consisting of two matched junctions of opposite polarity connected in parallel; it is used primarily for direct conversion of AC and DC information into logarithmic information over several decades. The transfer characteristics of the CA3039 (Fig. 24) illustrate the suitability of this array for such use. Three matched varistors can be provided by proper interconnection of diode pairs in the CA3039, as shown in Fig. 25. Varistors are applicable to fractional voltage regulators, meter protectors, telephone circuits, and negative-temperature-coefficient resistors.

Temperature compensation in SCR triggering circuits

Fig. 26 shows a schematic diagram for a circuit that translates a low-level output signal from a thermistor temperature-sensing element into an on-off control output capable of directly driving high-level loads, such as indicator lamps, resistance heaters, power-control relays, or solenoids. When R_A becomes smaller than R_B, sufficient positive gate current is provided to trigger the SCR ON. When R_A is a thermistor and R_B an adjustable reference resistor, the SCR turns ON when the thermistor temperature rises above the set value. If the thermistor and the reference resistor are interchanged, the SCR operates when the thermistor temperature decreases.

Without the use of the temperature-compensation diodes D_1, D_2 and D_3 the SCR gate trigger voltage would vary as a result of changes in junction temperature. This temperature-sensing error is of the order of 5°C for an ambient temperature change from −55 to 125°C. The use of CA3039 diodes D_1 through D_3 or D_4 through D_6 can reduce this temperature-sensing error to a value in the order of 0.5°C over the same temperature range. When R_A in Fig. 26 is precisely equal to R_B, zero potential exists at a virtual ground point "B" midway between points "A" and "C". With "B" as an imaginary small point, there are effectively 1.5 diodes in the upper leg

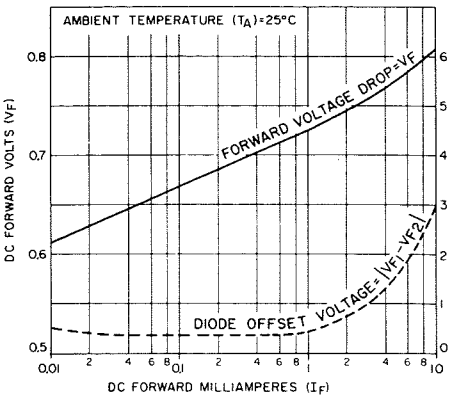

Fig. 24—Transfer characteristics of a CA-3039 diode.

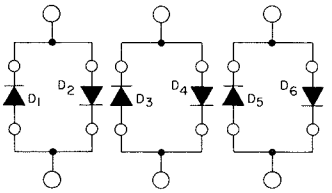

Fig. 25—Three matched varistors composed of CA3039 diodes.

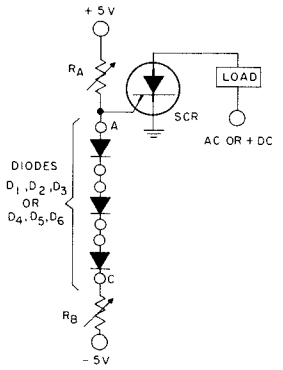

Fig. 26—An SCR triggering circuit with temperature compensation.

of the input circuit and 1.5 diodes in the lower leg; each diode has a temperature coefficient of about −2mV/°C. Thus, if R_A and R_B are kept equal and ambient temperature is changed, the voltage at "A" changes about −3mV/°C (1.5 diodes at −2mV/°C each). Compensation is then achieved because the temperature coefficient of the SCR gate trigger voltage is also of the order of −3mV/°C.

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Fabrication of Al_2O_3 COS/MOS integrated circuits

Dr. F. B. Micheletti | P. E. Norris | Dr. K. H. Zaininger

Operating integrated circuits have been fabricated using Al_2O_3 as the gate insulator. These circuits demonstrate a high degree of radiation hardening and prove the feasibility of Al_2O_3 MOS technology. In this paper, the processing steps are described and the important electrical properties are given.

In Metal-Oxide-Semiconductor (MOS) devices, the dielectric film used as gate insulator is an active, integral part of the device, and device operation and characteristics are very sensitive to its properties. Hence, in MOS technology, emphasis is placed on the fabrication of this oxide rather than on diffusion as in bipolar technology.

For a large number of non-critical applications, the currently commercially available MOS units with SiO_2 gate oxide are adequate. The processing is now well under control and has been reduced to a relatively straightforward procedure. Excellent results have been obtained with increasingly larger and more sophisticated integrated circuits so that low-cost large-scale integration (LSI) of MOS circuits offers considerable promise for the future. However, for certain more critical requirements, two major reliability problems have been encountered:

1) The migration of minute traces of impurities through the films (especially at elevated temperatures and under high field conditions) results in serious drifting and changes in the device characteristics;
2) Radiation also causes drift and/or degradation in device characteristics due to charge generation and trapping in the oxide.

Recently, technological advances were made that allow improved performance of MOS devices in these areas by utilizing aluminum oxide as the gate insulator. Aluminum oxide made by two different techniques has led to significant improvements in resistance to both bias-temperature stress and radiation exposure.[1,3] These techniques are:

1) Plasma anodization of *Al*,[4,5] and
2) Low temperature pyrolytic decomposition[6] of *Al*-alkoxides.

Plasma-grown Al_2O_3 shows, at present, the most promise for COS/MOS applications and will be the subject of this paper. When used as the gate insulator, it can lead to the following advantages:

1) *Low ion drift properties:* This is perhaps the most important gate insulator characteristic. Al_2O_3 resists ion drift perhaps orders of magnitude better than SiO_2. This means that MOS devices made from it exhibit stability to bias-temperature stress, a property that manifests itself in two very practical results: (a) ultraclean technology as required for SiO_2 (state-of-the-art)[7] devices would *not* be necessary (this should reflect itself in the cost, yield, and uniformity of LSI arrays), and (b) Al_2O_3 could act as a junction seal and encapsulant for both MOS and bipolar LSI. A thin film of Al_2O_3 on a junction or over an MOS device would act as a passivation layer giving the equivalent of a hermetic seal.

2) *Radiation resistance:* Measurements made to date on MOS devices on single crystal silicon show good radiation resistance,[1,2,8] better than SiO_2[9] and Si_3N_4 devices.[10] This is important to arrays that will be exposed to the radiation fields of space or nuclear environments. The reason for this improvement is most probably connected with the particular defect structure of Al_2O_3.

Other important properties are summarized in Table I.

Table I—Properties of plasma-grown Al_2O_3

Relative dielectric constant	8.0 to 8.7
Loss tangent (f = 100 kHz)	0.02
Surface-state density	2×10^{10} states/cm^2-eV
Index of refraction	1.67 to 1.70

Plasma-anodization process

The technique of plasma anodization of a metal to form the metal oxide is a relatively new one and, to date, has been primarily used to form oxides of metals for thin-film capacitors. The most prominent materials[4,5] formed have been Al_2O_3 and Ta_2O_5. In general, it has been found that these insulating films are amorphous with a low dissipation factor and a high breakdown strength.

Plasma anodization is carried out in a vacuum system that has been modified as shown in Fig. 1. The aluminized silicon wafer is placed in a closed insulating sample holder which has openings for exposure of the front surface of the wafer and for admission of a contact lead. Electrical contact is made to the back of the wafer with a pressure contact jig. Once the sample is in place, the system is evacuated to 1×10^{-6} Torr and back-filled with dry oxygen. The pressure is set at 0.3 Torr, and a glow discharge is ignited between anode and cathode. The sample, which is in the glow or "positive column" portion of the discharge, is biased positively with respect to the wall potential (defined as the potential which, when applied to a conducting probe in a plasma, reduces the current flow to zero). Because the wall potential may vary considerably during one anodization, depending on the condition of the anode, it must be monitored throughout the anodization. This is accomplished by adding an additional electrode to serve as a plasma probe.

The growth rate of the oxide is greatly dependent on the geometry of the anodization system and is not always linear with voltage. If the film is thick enough so that it is not completely anodized, the growth is self-limiting in a fashion analogous to that of wet anodization. Typically, the oxide is observed to grow at 22Å/volt—although this can vary considerably with the geometry of the anodization system and the mode of operation.[11] For MOS applications, the aluminum film must be completely anodized since any free *Al* at the interface would act as surface states. Hence, a potential sufficient to anodize all the aluminum must be applied. This potential, however, must not be too high or a thin film of SiO_2 can be formed at the silicon interface. The SiO_2 so formed can cause electrical instability (hysteresis in C-V testing) as well as deterioration in the resistance to ionizing radiation. The presence of the SiO_2 layer can be detected by ellipsometry measurements which reveal considerable deviation in the index of refraction and measured film thickness from that expected for Al_2O_3 alone. For the circuits fabricated in this in-

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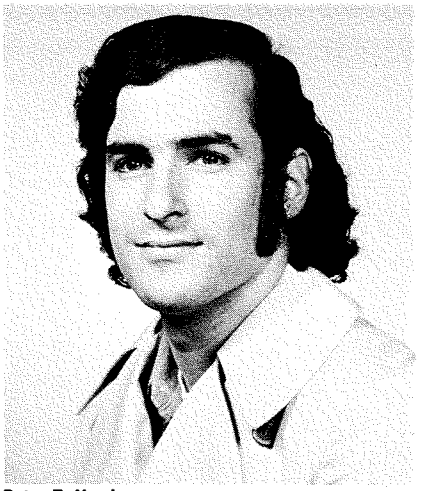

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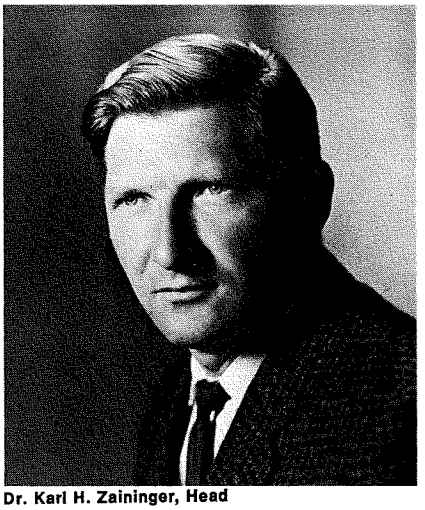
received BSEE from MIT in 1965. From 1965 to 1967 he attended graduate school at MIT receiving both the MS and Engineer's degrees in 1967. During this period he was a member of the Laboratory for Insulation Research working in the area of high resistivity semiconductors. In 1967 he attended the University of Colorado before joining RCA Laboratories in 1968. As a member of the Research Training Program at the Laboratories, he worked on large screen TV displays, photochromics and radiation damage in MOS devices. At present he is engaged in research on improved insulation for IC technology.



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received the BEE (magna cum laude) from City College of New York in 1959; the MSE in 1961, the MA in 1962, and the PhD in Engineering Physics in 1964 from Princeton University. In 1959 Dr. Zaininger joined the staff of RCA Laboratories. He has been working in research on various semiconductor devices, and has been involved in research on silicon based MOS devices since their original inception. He is presently concerned with MIS device physics and technology, with measurement techniques, and with the physics of radiation damage in MIS systems. In August 1968 Dr. Zaininger was appointed to his present position. In 1965 Dr. Zaininger received an RCA Laboratories Achievement Award for team performance for experiments and studies leading to a better understanding of the electrical properties and growth mechanisms of silicon-dioxide films on silicon substrates. In 1968 he received another Achievement Award for team performance in research on aluminum oxide films on TFT and MOS structures leading to stable and radiation-resistant devices. Dr. Zaininger is a Senior Member of the IEEE, and a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the Shevchenko Scientific Society. He is also a co-author of a textbook on field effect transistors.

vestigation, good-quality Al_2O_3 films on *Si* were obtained under conditions listed in Table II. As shown in Fig. 2, a constant current is maintained until the desired voltage, indicative of a certain film thickness, is obtained. This voltage is then held constant, and the current is allowed to decay. The net voltage on the sample is the applied voltage minus the wall potential.

The utilization of the plasma oxide is much more difficult for active device configurations than for simple MOS capacitors because of the peculiar etching characteristics of this oxide. The most straightforward fabrication scheme would be to chemically etch the required geometrical patterns in the oxide after its formation. However, upon exposure to hot phosphoric acid (80°C to 180°C), the plasma-grown oxide softens and eventually peels from the substrate. Similar effects are observed upon exposure to buffered *HF*. Hence, direct chemical etching cannot be utilized at the present. Thus, an alternate technique, namely etching of the aluminum film prior to anodization, was developed and refined to allow device fabrication.

COS/MOS processing

The processing of the wafer proceeds in the same manner as for the conventional SiO_2 unit up through step 6 of Fig. 3. At this point, there are two alternative schemes which can be utilized depending on whether the stepped SiO_2 is to be under or over the Al_2O_3 layer.

In the first version, alternative A of Fig. 4, SiO_2 is removed from the active region only, leaving the stepped oxide on the remainder of the wafer. The wafer is then metallized (420Å of aluminum), contact holes are formed in the aluminum film, and anodization of this film is carried out under the conditions listed in Table II.

In the B version, all oxide is removed from the entire wafer. The wafer is then metallized, contact holes are formed in the aluminum film, and the anodization is carried out in the normal manner. Finally, SiO_2 is deposited and then densified at 800°C to 1000°C before the desired stepped-oxide pattern is formed.

In either version, the unit is completed by first removing the oxide formed in the contact holes during the anodization by a 30-second etch in buffered *HF*, followed by an anneal at 350°C for one hour in hydrogen and finally by forming the contact metallization. The units are then electrically probed, and acceptable units are selected from the diced wafer and bonded into 14-lead flatpacks for testing; see Figs. 5 and 6.

Critical process steps

Wafer preparation—The wafer must be free of both particulate contamination and absorbed moisture prior to aluminum metallization since either can result in oxide defects (bubbles, pinholes, etc.) which would cause failure by electrical conduction. The effects of moisture can be largely eliminated by heating the wafer in an inert ambient prior to metallization. Particulate contamination is minimized by careful cleaning immediately before placing the wafer in the vacuum system for metallization.

Table II—Typical plasma anodization parameters.

Pressure	0.3 Torr (oxygen)
V_p (anode to cathode voltage)	800 to 1100 volts
I_p (plasma current)	40 to 60 mA
Aluminum thickness	420Å
Initial sample current	0.3 mA/cm²
Final applied voltage	60 to 70 volts
Total time of anodization	2 to 3 hours
Al_2O_3 thickness	640Å

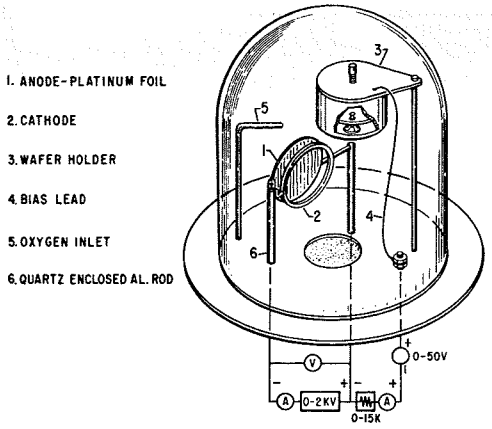

Fig. 1—Plasma anodization chamber.

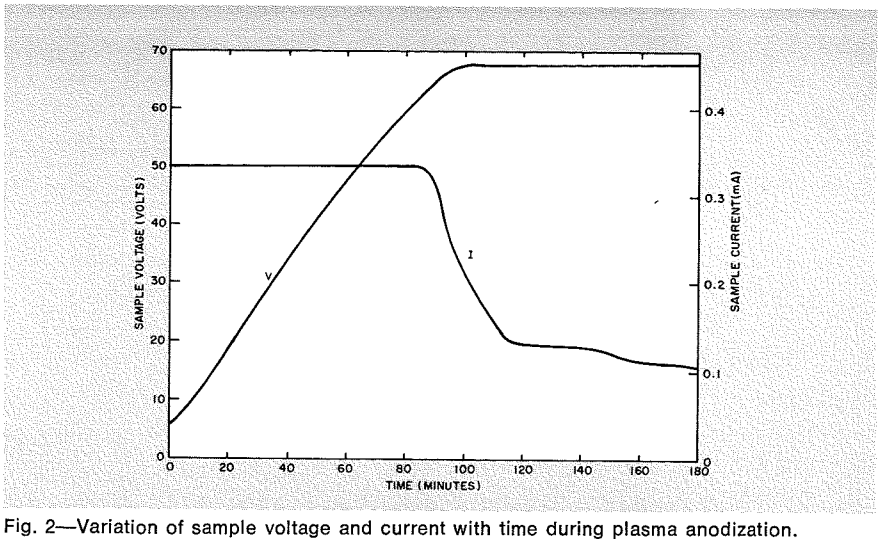

Fig. 2—Variation of sample voltage and current with time during plasma anodization.

Aluminum deposition—Since the oxide thickness is determined by the thickness of the aluminum film, the metallization must be accurately controlled. This can be done quite easily with a quartz crystal monitor. The thickness is normally verified optically by the Tolansky interference technique. This is important since overanodization results in the formation of a thin SiO_2 layer at the silicon interface and in some cases is responsible for the appearance of oxide defects (bubbles or other fine structures).

Measurement of sample voltage—As indicated above, the effective voltage applied to the sample is the supply voltage minus the wall potential. The wall potential is determined not only by the plasma parameters but also by the condition of the anode. During a given anodization, the wall potential increases in magnitude. In some cases, for an anode which has been reused a number of times, the wall potential may vary by as much as 10 volts during an anodization. Hence, the wall potential must be monitored continuously. This is achieved by a plasma probe in conjunction with a high impedance meter such as an electrometer or nulling voltmeter. Errors result if the input impedance of the meter is below 10^9 ohms.

Control of current density—Control of the current density is necessary to obtain high-quality oxide in a reasonable time. If the current density is too high, especially as the growth approaches the silicon interface, oxide defects such as bubbles or fine grainy structure result. On the other hand, if the current density is too low, the anodization proceeds too slowly.

Effects of stepped oxide—When the Al_2O_3 is formed over the stepped oxide (as in version A of Fig. 4), additional care must be taken to ensure that the aluminum is completely anodized over the SiO_2 regions. In version B, the etching of the desired pattern in the SiO_2 overlying the Al_2O_3 must be controlled very accurately since buffered *HF* attacks the Al_2O_3-silicon interface, causing the oxide to peel.

Removal of oxide from contact holes—During the anodization, 50 to 100Å of SiO_2 form in the contact holes. This oxide must be removed by buffered *HF* so that contact can be made to the source and drain regions of the devices. Because the buffered etch attacks the Al_2O_3, photoresist is used to protect the Al_2O_3 during this step.

Electrical properties

Both discrete N-channel units and complementary-symmetry MOS inverters (CD-4007) with plasma grown Al_2O_3 as the gate insulator have been evaluated. In general, a lower yield and a reduction in device quality has been found in comparing the discrete ring-dot units with the individual MOS units on the CD-4007 circuit as summarized in Table III. This is attributed to the greater complexity of the circuit over the discrete ring-dot structure and in particular to difficulties involving the formation of the stepped oxide which was not utilized for the discrete structure.

Typical transfer characteristics for inverter pairs on the CD-4007 chip are shown in Fig. 7 together with the current flowing from the power supply. The schematic for these inverters is shown in the insert to the Figure. The characteristics of the plasma-grown Al_2O_3 units are offset to the right of those of the conventional SiO_2 units due to the large threshold of the N-channel units, and they are somewhat distorted due to contact resis-

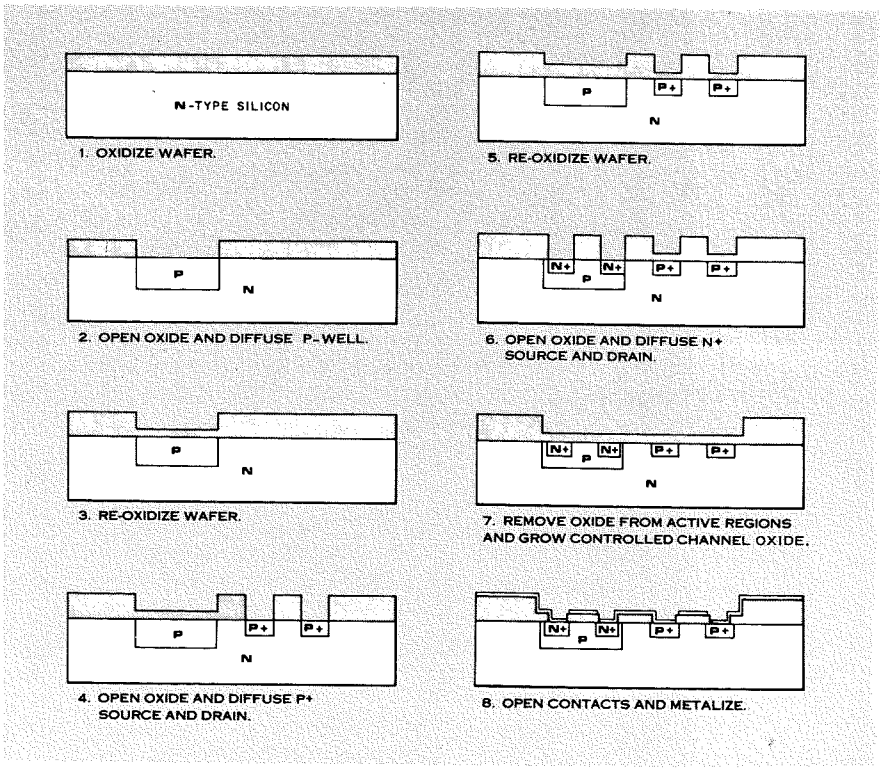

Fig. 3—Major processing steps for complementary MOS integrated circuits with thermally grown SiO_2 channel oxide.

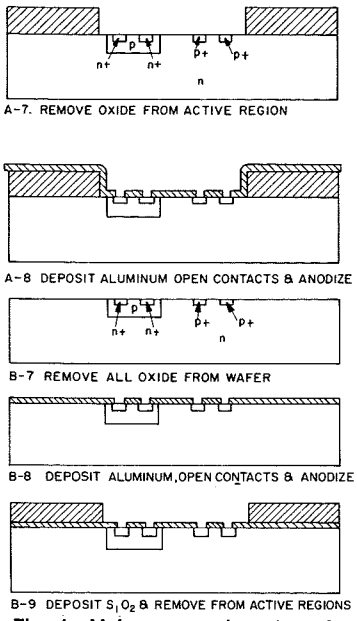

Fig. 4—Major processing steps for utilization of plasma-grown Al_2O_3.

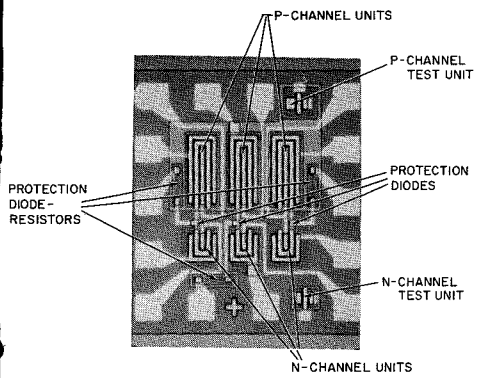

Fig. 5—Topological view of RCA CD-4007 dual complementary pair plus inverter.

tance. On the other hand, there is no appreciable current flow in either steady state condition (V_{in}=0 or +10 volts) as required in most cos/MOS applications. With refinements in the processing, these characteristics should be improved considerably.

Small shifts (~0.5 volts) in these transfer characteristics due to bias temperature stress (150°C, 10 volts, 5 minutes) have been observed. However, these are opposite in direction to shifts caused by positive ion drift and are attributed to interface state effects.

The units with plasma-grown oxide show promise of considerable radiation hardness. All units were bombarded with 1-MeV electrons in the Van de Graaff facility at RCA Laboratories. Fig. 8 shows the net shifts in threshold voltage for the CD-4007 for a +10-volt input, which is the most severe condition for conventional SiO_2 units. These results, together with tests under other biasing conditions, show that plasma-grown Al_2O_3 offers an increase in radiation hardness by a factor of 50 or more over SiO_2.

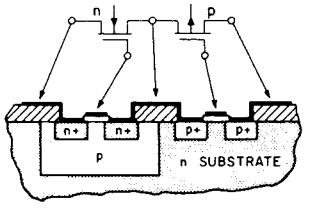

Fig. 6—Cross-section view of COS/MOS inverter showing external connections.

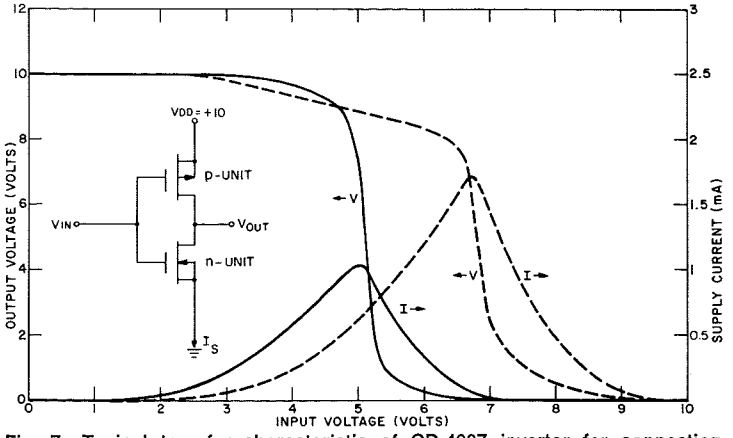

Fig. 7—Typical transfer characteristic of CD-4007 inverter for connection shown in insert: solid curve for conventional SiO_2 unit, dashed curve for unit with plasma-grown Al_2O_3.

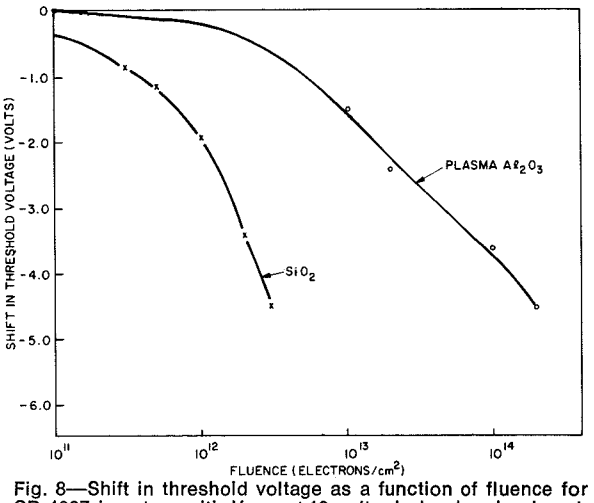

Fig. 8—Shift in threshold voltage as a function of fluence for CD-4007 inverters with V_{in} = +10 volts during bombardment.

Conclusions and recommendations

The results reported in this paper clearly show two major achievements:

1) The first successful fabrication of operating integrated circuits using Al_2O_3 as gate insulator, thus proving the feasibility of an Al_2O_3-MOS technology.
2) The first demonstration that the degree of radiation hardening, expected from MOS-capacitor data, has been achieved in active device structures and integrated circuits.

Considerable work remains to be done, especially in the areas of geometrical pattern definition, optimization of oxide properties and formation techniques, and active device fabrication. Once these difficulties have been eliminated, and statistically significant results have been obtained, there will be enough confidence in the Al_2O_3 technology that it can be transferred into an experimental line for fabrication of integrated circuits. This can then lead to a radiation-resistant technology for integrated-circuit capability.

Acknowledgments

The authors would like to acknowledge the assistance of C. Benyon, J. Groppe, G. Mark, and J. Shaw for fabrication of the devices; D. Flatley and W. French for provision of the CD-4007 substrates with diffusions and F. Kolondra for radiation testing of the completed devices.

Table III—Comparison of discrete MOS characteristics on CD-4007 and ring-dot test units.

Unit		Threshold (volts)	Field-effect mobility (cm^2/V-sec)
CD-4007	plasma Al_2O_3 N-channel unit	+4.0±0.5	23
	640Å P-channel unit	−2.0±0.5	46
CD-4007	SiO_2 N-channel unit	2.0±0.5	102
	1000Å P-channel unit	−1.5±0.5	144
Ring-dot	plasma Al_2O_3 N-channel unit	1.5±0.5	150

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The operational transconductance amplifier — a new circuit dimension

C. Frank Wheatley, Jr.

An operational amplifier has been designed in which the forward gain is best characterized by a transconductance concept. The bias currents and dynamic characteristics are controllable in a linear fashion over a five-decade operating range by means of an externally accessible electrode. An array of these amplifiers has been fabricated upon a monolithic integrated-circuit chip employing 94 bipolar transistors of both conductivity types and no resistors. These arrays permit a wealth of new circuit possibilities. The applications evaluated and discussed include fixed-bias operational amplifiers, gated operational amplifiers, four-quadrant multipliers, variable-gain amplifiers, and multiplexers.

AN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) has all of the characteristics of an operational voltage amplifier except that the output impedance ideally approaches infinity rather than zero. As a result, the forward gain characteristic is best described by transconductance rather than voltage gain. In addition, access is provided to bias the amplifier by means of an externally provided current. As a result, the transconductance, circuit dissipation, and loading may be externally established and varied at the option of the user. This feature provides a new dimension in "op-amp" circuit design.

The integrated operational transconductance amplifier (OTA) described is an outgrowth of an attempt to design a monolithic integrated operational amplifier with extremely low power dissipation. During the early stages of design, it became apparent that bipolar transistors are inherently current output devices, and that a low output impedance could be obtained only by feedback techniques (emitter-follower being the method most commonly used). To obtain a low output impedance at an extremely low power level, it is generally necessary to provide a resistive value in the order of tens of megohms for feedback or for the driver collector load; such a component is most difficult to integrate. If a high output impedance is acceptable, however, the load signal may be delivered from a bipolar collector without feedback, and the need for the very high resistance is circumvented.

Experiments with complementary bipolar transistors yielded circuits requiring a minimum number of resistors. After considerable analysis, it became apparent that the omission of all resistors in an IC design would permit functioning over several decades of operating current, and such a design would be relatively easy to produce.

The high output impedance and the need to provide external bias were considered to be minor disadvantages during the early phases of development when the OTA was considered solely as a means of producing an extremely low-power operational amplifier. However, it soon became apparent that the high output impedance is an asset for applications involving nonlinear loads and in summing and gyrator circuits. It also became evident that the amplifier need not be operated at a fixed bias, but can be operated at a time-varying bias level. As a result, it can be used as a two-quadrant multiplier, a four-quadrant multiplier, and an AGC amplifier. Additional advantages can be obtained by gating off the bias to eliminate power dissipation and circuit loading of the OTA while reducing the transconductance to zero. This property is useful in multiplexers, sample-hold-read circuits, and low-dissipation monostable, astable, and bistable oscillators.

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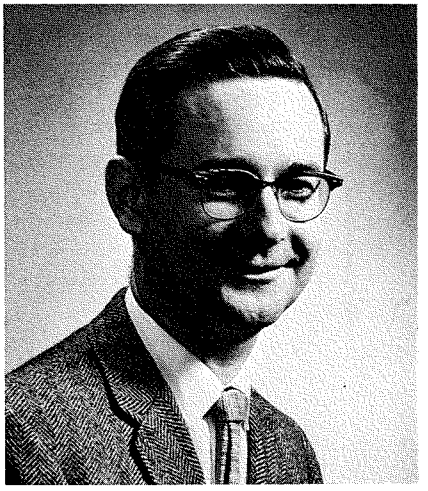

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started work on point contact transistors with RCA immediately after receiving the BSEE from the University of Maryland in 1951. Since then he has worked in the design, production, application, and development of germanium and silicon semiconductor devices. A large portion of this time was directed toward high voltage and high power. Mr. Wheatley was cited by RCA in 1961 for his contributions to industry acceptance of the transistor auto radio, and again in 1963 for his contributions to solid state high fidelity. His later venture into solid state television deflection was culminated by a best paper award bestowed by the Broadcast and Television Receiver Group of the IEEE in 1968. He is currently designing linear integrated circuits. Mr. Wheatley has authored or co-authored twenty technical papers and has fifteen U.S. patents either issued or pending. He is a senior member of the IEEE.

Circuit design features

Basic OTA circuit

The basic circuit developed is shown in Fig. 1. An understanding of this circuit is best obtained by analysis of voltages and currents with almost complete disregard for voltage gain and impedance levels.

Transistors Q_1 through Q_4 in Fig. 1 perform conventional functions, serving as a current mirror, a constant-current source, and a differential pair. An amplifier bias current is externally developed and applied to the current mirror (Q_1, Q_2) to bias Q_3 and Q_4. The differential signal currents of Q_3 and Q_4 are amplified by the beta of the

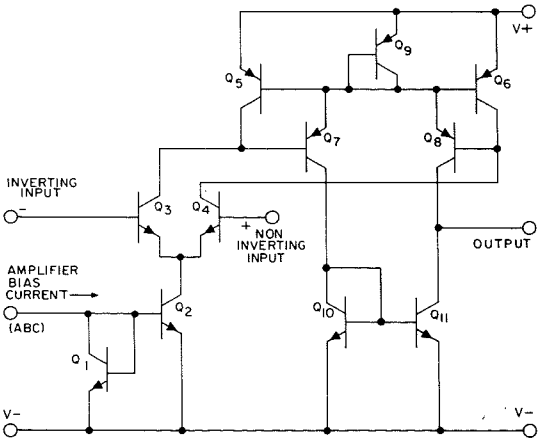


Fig. 1—Basic OTA circuit.

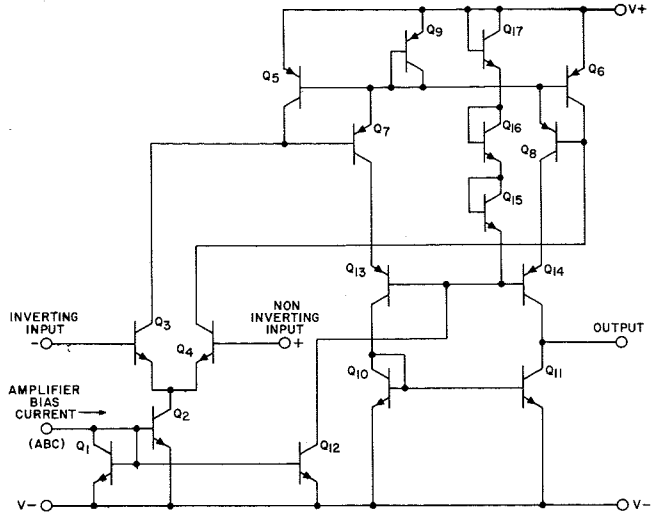


Fig. 2—Improved OTA circuit.

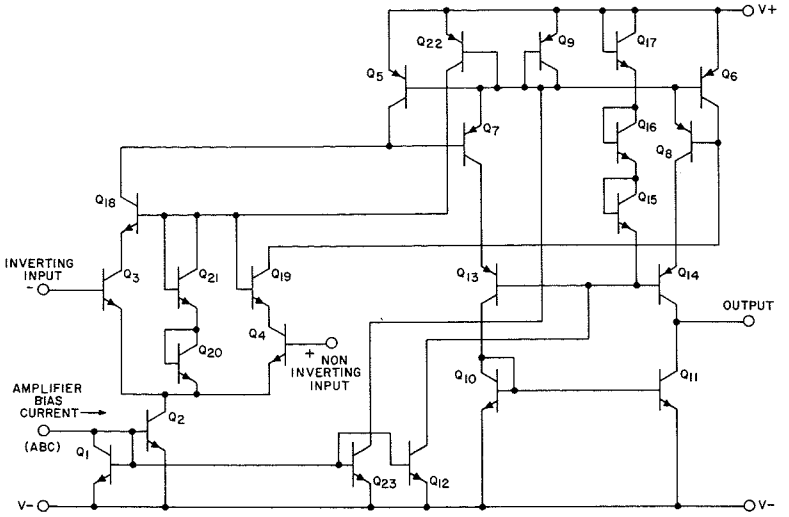


Fig. 3—Final OTA circuit.

differential P-N-P pair Q_7 and Q_8. The current mirror Q_{10} and Q_{11} then transforms the double-ended output of the P-N-P network Q_5 through Q_9 into a single-ended output. The entire circuit functions in a class-A mode.

Ideally, there is no need for a signal ground because the input signal is differential and the output signal is a current. The input and output terminals may operate at most AC and DC potentials within the range of the supply voltages.

The amplifier-bias-current (ABC) level establishes bias for all transistors in the amplifier. Ideally, this circuit would function at ABC bias levels of picoamperes, microamperes, or amperes. In practice, however, the circuit will malfunction if it is biased at a level at which the transistors no longer have desirable characteristics. At high levels, malfunctions may be caused by either beta fall-off or parasitic ohmic effects. Low-current malfunctioning may occur as a result of beta fall-off, channeling, or leakage. Samples of OTA's have exhibited good performance for ABC levels from 10 nA to 1 mA, or over a range of five decades (100 dB). Lack of instrumentation has prevented investigation of lower levels.

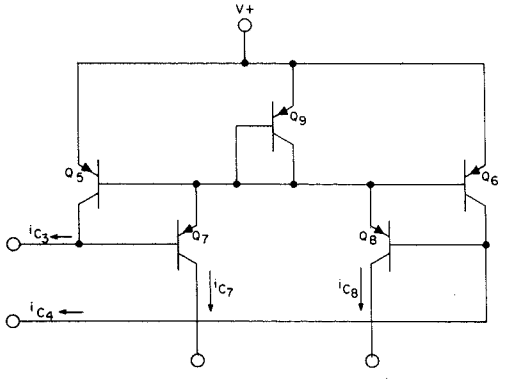


Fig. 4—Network of P-N-P transistors used in OTA.

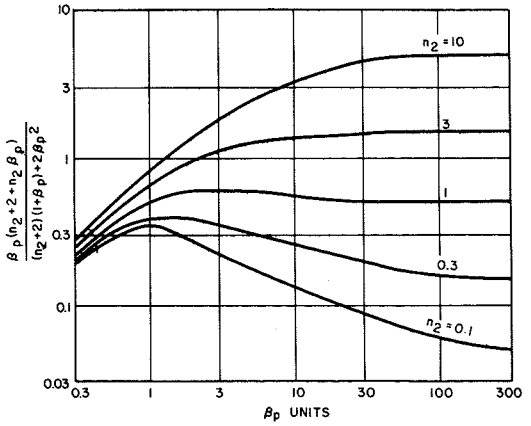


Fig. 5—Current ratios in OTA.

Improved OTA circuit

The common-mode rejection ratio, the supply-rejection ratio, and the output impedance of the OTA are all enhanced by the high output impedances of the transistors Q_2, Q_3, Q_4, Q_7, Q_8, and Q_{11} in Fig. 1. The P-N-P transistors (Q_5 through Q_9) are lateral transistors and exhibit a relatively poor output impedance. Although the common-emitter output impedance R_{out} of a P-N-P lateral transistor is influenced by the chip design, it is approximately given by

$$R_{outP} \approx \left| \frac{500}{\beta_P I_c} \right| \qquad (1)$$

where β is determined at a collector-current level I_c (in amperes). In common-emitter operation, an output impedance of 20 megohms can be expected at a collector-current level of 1 μA if the current gain equals 25. This impedance level is quite low in comparison with that of a conventional N-P-N transistor, which is typically two orders of magnitude higher, as shown below:

$$R_{outN} \approx \left| \frac{2 \times 10^5}{\beta_N I_c} \right| \qquad (2)$$

Eq. 2 yields an output impedance of 2×10^9 ohms at a collector current of 1 μA for a typical beta level of 100.

If a transistor is operated with emitter-current drive, as in cascode operation or common-base operation, the value of β used in Eqs. 1 and 2 is unity. If a transistor is operated as the output of a current mirror (Q_{10} and Q_{11} form a current mirror in Fig. 1), the value of β used in Eqs. 1 and 2 is two (mirror current gain is assumed to be unity).

Examination of Fig. 1 reveals that Q_7 and Q_8 degrade the supply-rejection ratio and the output impedance of the OTA. An obvious improvement can be obtained if these two transistors are operated into cascode stages, as shown in Fig. 2. Transistors Q_{13} and Q_{14} then perform the driving function previously provided by Q_7 and Q_8. Because Q_{13} and Q_{14} are operated in a common-base configuration, the output impedance is improved by a factor equal to β_P, and a similar improvement is obtained in supply rejection and OTA output impedance. Transistors Q_{15}, Q_{16}, Q_{17} provide a bias potential for the bases of Q_{13} and Q_{14}; transistor Q_{12} provides the current that establishes the bias potential.

Provisions for "super-beta" input

Cascode operation of Q_3 and Q_4 enhances the common-mode rejection ratio. In addition, because it assures essentially zero collector-to-base voltage for Q_3 and Q_4, such operation permits a "super beta" option which requires six additional transistors, as shown in Fig. 3. When this "super-beta" arrangement is used, transistors Q_3, Q_4, and Q_{20} may be processed to have very high forward current gain (beta). Because Q_{18} and Q_{19} operate in cascode with Q_3 and Q_4, there is no need for the voltage swing previously required of Q_3 and Q_4. Q_{20} and Q_{21} provide a voltage source for the bases of Q_{18} and Q_{19} which is bootstrapped to the emitters of Q_3 and Q_4. The other source of current necessary to develop

the bootstrapped voltage source is provided by Q_{22}. A bypass transistor, Q_{23}, is incorporated to avoid a bistable circuit condition caused by the addition of Q_{18} to Q_{22}.

OTA characteristics

The characteristics of the final OTA circuit shown in Fig. 3 are established primarily by three factors:

1) The value of the amplifier bias current, I_{ABC};
2) The geometry ratios of the various transistors; and
3) The effect of the beta of the P-N-P lateral transistors.

Amplifier bias current I_{ABC}

The amplifier bias current I_{ABC} is normally provided from the output of another OTA or from a resistive feed. In the case of the latter, the current varies as the voltage across the resistor changes. For suppression of this variable, provisions are made for regulation, as discussed later in more detail in the section on "chip design."

Geometry ratios

If two conventional transistors are identical in everything but size, and if they are biased at identical base-to-emitter potentials, the ratio of collector currents is equal to the ratio of emitter area for the two units. In the case of lateral transistors, the current ratio is equal to the emitter-to-base edge ratio. In the circuit of Fig. 3, all transistors are the same except Q_2, Q_7, Q_8, and Q_9. In relation to the other transistors, Q_2 is four times the standard size, and the other three transistors are three times standard size.

Effect of P-N-P beta

Fig. 4 shows the network of five P-N-P transistors included in the circuit of Fig. 1. The influence of the beta of these transistors on the OTA characteristics is best described by an analysis of this network in which the following assumptions are made:

1) All P-N-P betas are equal;
2) Q_5 and Q_6 are identical;
3) Q_9 is equivalent to n_2 parallel transistors identical to Q_5;
4) All transistors are at the same temperature; and
5) All current gains are independent of collector voltage.

An exact analysis, which is simple but lengthy, produces the following results:

$$(i_{c7}+i_{c8}) = (i_{c3}+i_{c4})\,\frac{\beta_P(n_2+2+n_2\beta_P)}{(n_2+2)(1+\beta_P)+2\beta_P^2} \qquad (3)$$

$$(i_{c7}-i_{c8}) = \beta_P(i_{c3}-i_{c4}) \qquad (4)$$

Eq. 3 implies a DC bias of the network which is independent of the P-N-P beta and the differential signal. Eq. 4 shows that the differential output signal depends only on the P-N-P beta and the differential input-current signal; as a result, common-mode rejection is high. Fig. 5 shows the ratio of $(i_{c7}+i_{c8})$ to $(i_{c3}+i_{c4})$ for various values of n_2.

If the collector of Q_7 is fed to a current mirror which, in turn, is connected to the collector of Q_8, the resulting output current is approximately equal to

$$i_{out} = 2(i_{c8}-i_{c7}) \qquad (5)$$

The peak-to-peak output-current swing then limits at the following value:

$$i_{p-p} = 2(i_{c7}+i_{c8}) \qquad (6)$$

Fig. 5 shows that the DC bias currents are nearly independent of the P-N-P beta; Eqs. 4 and 5 show that the AC current gain of the composite network is directly related to the P-N-P beta. This dependence is reflected in the OTA transconductance.

Bipolar performance

Recent work indicates that operation of transistors in the submicroampere region is less uncertain than previously supposed. Some conventionally processed transistors similar to those used in the OTA were measured for current gain as a function of collector current. Figs. 6 and 7 show the beta characteristics of an N-P-N transistor and of a lateral P-N-P transistor, and Fig. 8 shows the voltage-current characteristic of a zener diode [N^+ into B and R (base and resistor) diffusions]. Although the performance shown may not be achieved by all devices, a great many have such characteristics.

The betas of P-N-P transistors appear to be well matched and quite independent of temperature. Although the output impedance of these lateral transistors is lower than might be desired, this shortcoming has been suppressed in the circuit design.

The noise level of the B and R (base and resistor diffusion) zener diode may be as high as one millivolt peak to peak. As a result, a noise current is supplied to the ABC terminal (as discussed later) which is typically 90 dB below the DC bias current. Because this path of extraneous signal is a common-mode path, considerable added suppression results. Although an N^+-P^+ zener diode would have a lower noise level, the voltage-current characteristic

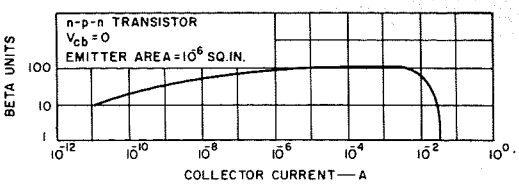


Fig. 6—Beta characteristics of N-P-N transistor.

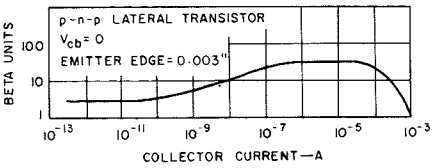


Fig. 7—Beta characteristics of P-N-P transistor.

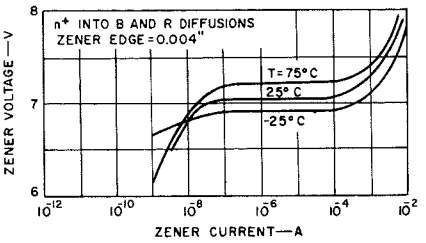


Fig. 8—Voltage-current characteristics of zener diode.

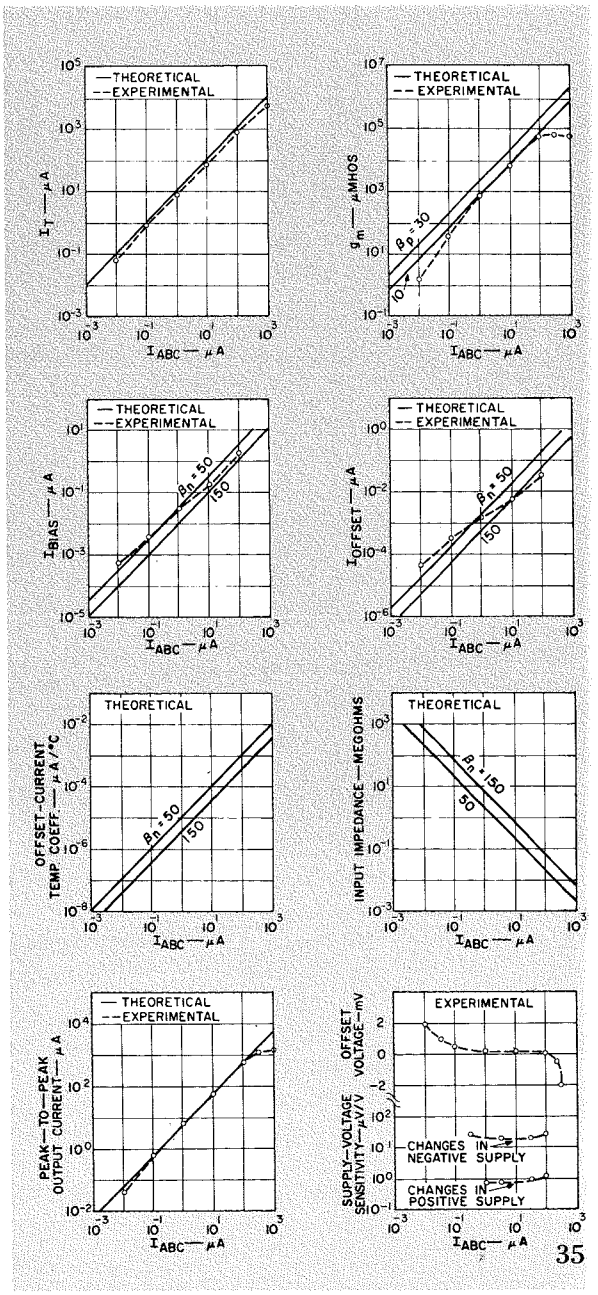


Fig. 9—Performance curves for OTA.

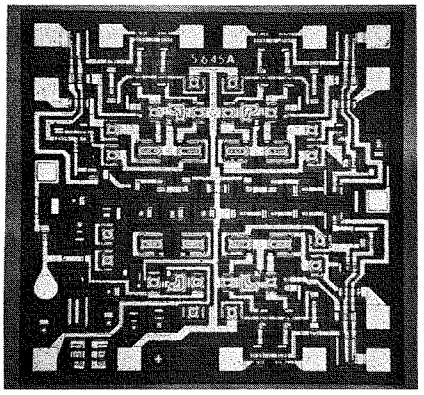


Fig. 10—Photomicrograph of OTA chip.

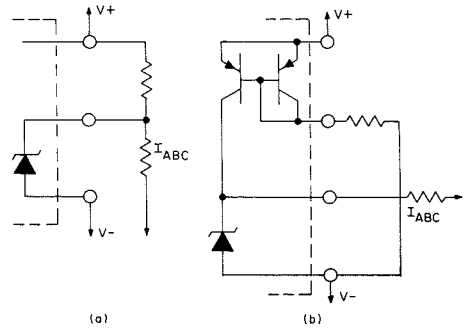


Fig. 11—Voltage-regulator circuits in (a) quad-array, and (b) tri-array.

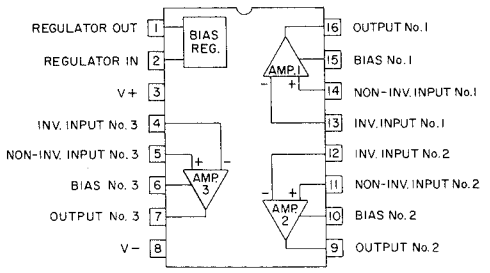


Fig. 12—Functional block diagram of CA3060.

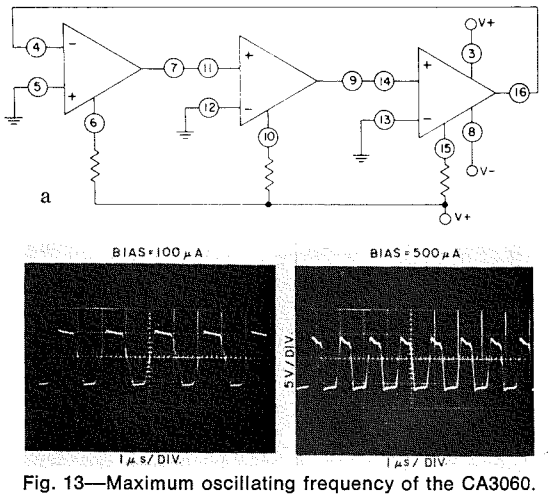
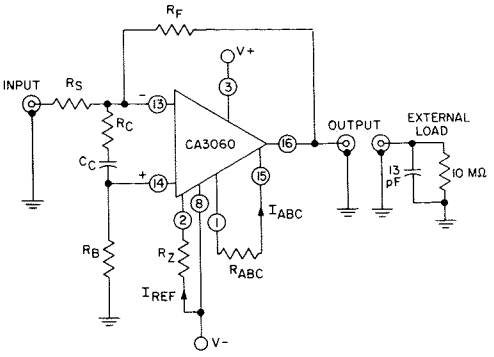


Fig. 13—Maximum oscillating frequency of the CA3060.

would be poorer at low current. In addition, a P+ diffusion step would be required in fabrication. For these reasons, a B+R zener diode was selected for the final chip array.

Total Circuit Performance

The curves in Fig. 9 show both predicted circuit performance and the measured performance of some typical samples of the OTA of Fig. 3.



$$R_Z=\frac{[(V^+)-(V^-)-0.7]}{I_2} \text{ and } R_{ABC}=\frac{V_Z-V_{ABC}}{I_{ABC}}$$

Supply voltage: $V^+=6$, $V^-=6$

Typical slew-rate test-circuit parameters

I_{ABC}	Slew rate	R_Z	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs			ohms				μF
100	8	56k	62k	100k	100k	51k	100	0.02
10	1	56k	620k	1M	1M	510k	1k	0.005
1	0.1	56k	6.2M	10M	10M	5.1M	∞	0

Fig. 14—Slew-rate test circuit and measurements.

Chip design

The final chip design selected features four OTA's and two zener diodes, or a total of 94 transistors, on a 65×65-mil chip fabricated with conventional non-critical processing. A photomicrograph of the chip is shown in Fig. 10. Two metallizing alternatives have been investigated. One features an array of four OTA's with a zener diode, and the other an array of three OTA's, a zener diode, and a P-N-P current mirror. Both designs have been fabricated in 16-terminal dual-in-line ceramic packages.

In the quad-array, the ABC terminals of all OTA's are connected to a common pin because of the limited number of terminals. As a result, all amplifiers of the quad must be biased at the same ABC level. (This requirement does not affect crosstalk between amplifiers.) The remaining terminal of the quad is used for the zener diode, which is referenced to the negative supply. This arrangement permits a simple voltage regulator for the I_{ABC} current (Fig. 11a) and thus maintains the excellent power-supply rejection of the OTA.

The ABC terminals of the tri-array are brought out separately to permit independent biasing. The two remaining terminals are used for a zener diode that regulates the ABC level and a P-N-P current mirror that permits regulation at lower supply voltages than that allowed by the simple zener circuit (Fig. 11b). The P-N-P current mirror in the tri-array configuration is metallized from the unused OTA on the basic chip. The tri-array (without "super-beta") is commercially available at this time as the RCA-CA3060 (Fig. 12).

Speed

The three OTA's of the CA3060 are arranged in cascade (Fig. 13a). The measured output waveforms for two I_{ABC} levels (Fig. 13b) indicate an open-loop slew rate of approximately 50 V/μs for the higher bias current and a propagation time of approximately 150 ns per OTA.

Fig. 14 shows a slew-rate test circuit and the unity-gain slew rate for three bias levels. Values as high as 8 V/μs are obtained at an I_{ABC} level of 100 μA.

Low-frequency noise and short-term stability

Some indication of the low-frequency noise and short-term stability of the OTA was obtained by cascading the three OTA's of the CA3060 in a non-inverting manner. The I_{ABC} levels were adjusted to produce 180 to 190 dB of open-loop voltage gain with feedback adjusted to produce a 120-dB closed-loop non-inverting voltage amplifier. The pen recording of the output in Fig. 15 shows the influence of noise and drift upon the amplified 11-mHz 1 μV peak-to-peak square wave over a period of 8 minutes. Sufficient capacitance was shunted across the input of the final OTA to reduce the system rise-time to 5 seconds.

Applications

Low-power operational amplifier

The power dissipation of the amplifier is determined by I_{ABC}; it is generally below 10 mW, and often below 1 mW. The typical 40-dB inverting amplifier shown in Fig. 16 is operated at an ABC level of 10 μA. The open-loop voltage gain of the amplifier is then equal to $g_m R_L$, or $10\times10^{-3}\times1\times10^6$, or 10^4 (the feedback network and any other loads reflect directly in the open-loop voltage gain). The standard design equations for operational amplifiers may be used to calculate the amplifier closed-loop characteristics, with the load resistance on the amplifier being substituted for the output resistance in the operational amplifier equations. The calculated closed-loop gain is 39.9 dB. The output impedance is 10,000 ohms.

Gyrator applications

The OTA is especially suitable for use in gyrators because the high output im-

pedance satisfies one of the basic requirements for this application. Inductances in excess of 10 kH have been realized by use of only two OTA's. Fig. 17 shows a gyrator circuit that produces such a high synthetic inductance with only a 3-μF capacitor. There is no reference to ground in this circuit; the "inductor" may float within the common-mode restraints of the OTA. Effectively, the inductor is isolated from the supplies by the high-impedance input and output of the amplifier. An attenuation network around the input of both amplifiers extends the differential operating range of each OTA about 100 times. In addition, this network reduces the transconductance by the same factor and thus further increases the gyration resistance. The provision for adjustable bias current to the OTA permits direct control of transconductance and, therefore, varies gyration resistance inversely. Because phase shift restricts the Q of the inductor, operation at frequencies above audio is impaired.

Amplifier with automatic gain control

The variable-transconductance characteristic of the OTA is useful in an AGC amplifier. When the OTA operates in the open-loop condition, the transconductance, and thus the amplifier gain, can be varied directly by adjustment of the ABC level. Therefore, an excellent AGC amplifier is obtained by rectifying and storing the amplifier output and applying this signal to the bias terminal. Fig. 18 shows a functional diagram of such a system. Low-frequency feedback is provided around the gain-controlled stage to balance the amplifier. As the input signal increases, the amplifier bias current decreases and reduces the transconductance and therefore the system gain.

Amplitude modulation

The gain-control characteristic of the OTA can also be used to provide modulation from DC to the upper cutoff frequency of the system with a single OTA. In this application, a carrier signal is applied to the differential input and a modulating signal current is added to the DC level of I_{ABC}. Fig. 19 shows a modulator with carrier and modulating frequency capability greater than 20 kHz. Fig. 20 shows the waveforms obtained when the modulator operates at a carrier frequency of 10 kHz and a modulation frequency of 500 Hz. As a modulator, the circuit should also be able to handle a 500-Hz carrier and a 10-kHz modulating signal; waveforms obtained under these conditions are shown in Fig. 21. The function performed by an AM modulator can be expressed as follows:

$$e_{out}=KX(1+Y) \qquad (7)$$

Multipliers

At times it is desirable to obtain two-quadrant multiplication of the following form:

$$e_{out}=KXY \qquad (8)$$

for all values of X and positive value of Y. For such multiplication, it is desirable that all three variables (e_{out}, X, and Y) be at ground reference for DC as well as AC voltages. This configuration can be obtained with two OTA's, as shown in Fig. 22. If third- and fourth-quadrant multiplication are desired, Fig. 22 may be rearranged so that X and Y signals are fed into the inverting inputs, as shown in Fig. 23. A logical extension of two-quadrant multiplication may be obtained by combining any number of OTA's in the manner shown in Fig. 24 so that the following function is performed for all values of X and positive values of Y and Z:

$$e_{out}=KXYZ \qquad (9)$$

Because the output impedance of an OTA is quite high, current summing is a very simple operation. A four-quadrant multiplier may be realized by combining the circuits shown in Figs. 22 and 23; the resultant circuit is shown in Fig. 25.

An eight-octant multiplier is more complex, but it may be designed by logic similar to that used for the four-quadrant multiplier. Fig. 26 shows the functional diagram. Zero adjustment must be provided for the offset voltage of the eight OTA's. In addition, the multiplying factor must be adjusted for positive values of Z and for negative values of Z; ten adjustments are required.

A four-quadrant multiplier may also be made by summing the outputs of two modulators similar to the one shown in Fig. 19. If one modulator is driven by signals X and Y while the other is driven by signals $-X$ and $-Y$, the output currents are as follows:

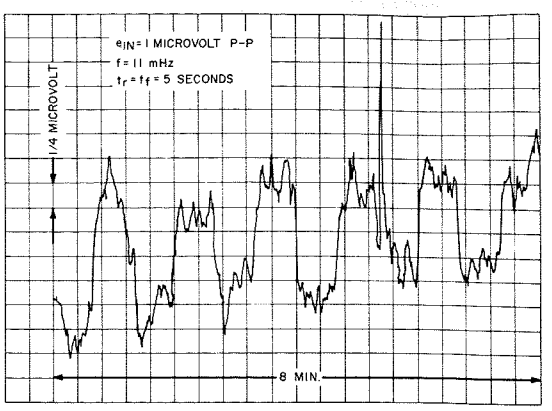


Fig. 15—Noise and drift of CA3060.

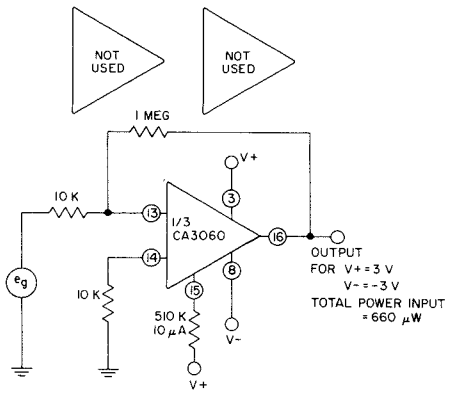


Fig. 16—Typical low-power amplifier.

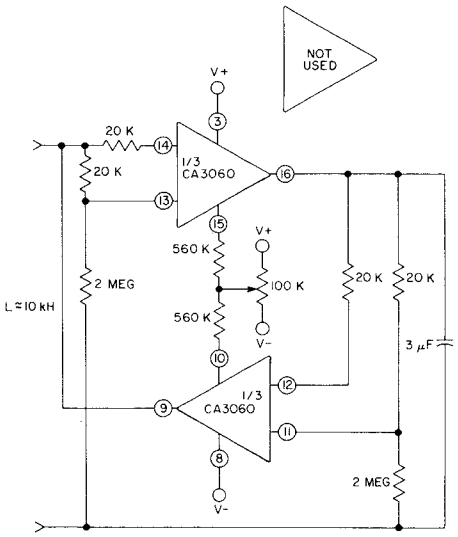


Fig. 17—Gyrator circuit using the CA3060 OTA array.

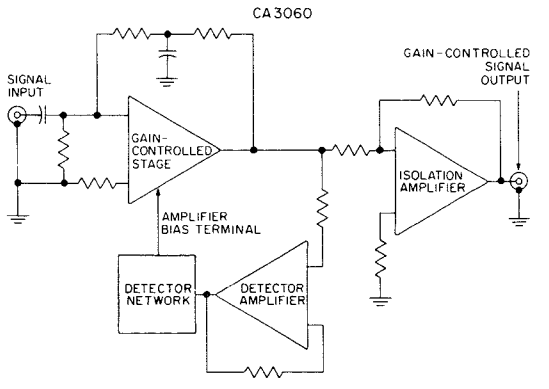


Fig. 18—Gain-controlled amplifier.

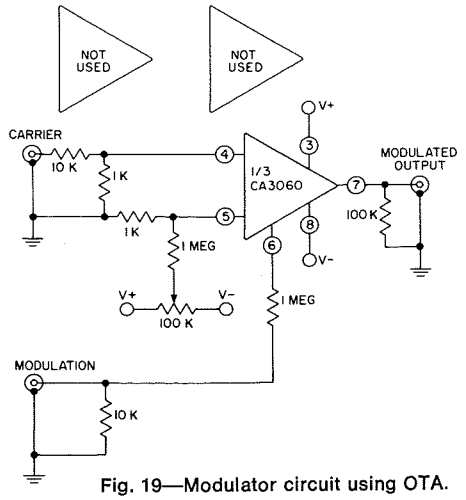


Fig. 19—Modulator circuit using OTA.

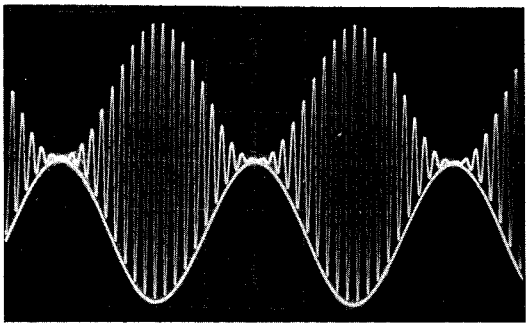


Fig. 20—Waveforms showing modulating signal (lower trace) and modulated carrier (f_c=10 kHz, f_m=500 Hz).

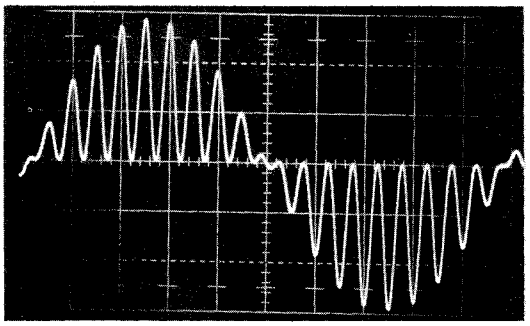


Fig. 21—Waveforms showing modulated carrier with frequencies of Fig. 20 interchanged (f_c=500 Hz, f_m=10kHz).

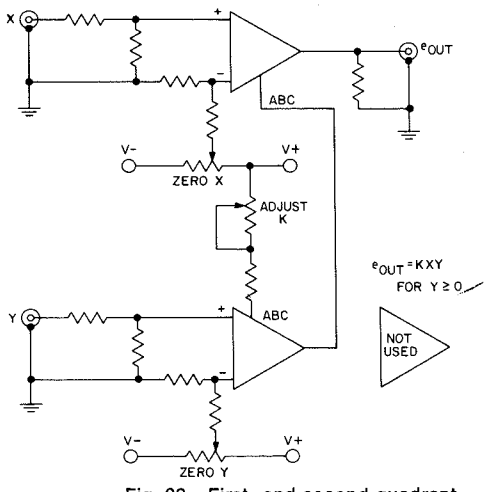


Fig. 22—First- and second-quadrant multiplier.

$$i_{o1} = GX(1+Y) \qquad (10)$$

$$i_{o2} = -HX(1-Y) \qquad (11)$$

where H and G are constant. Summation of Eqs. 10 and 11 provides the total output:

$$i_o = i_{o1} + i_{o2} = (G-H)X + (G+H)XY \qquad (12)$$

If offset adjustments can be made, and if G can be made equal to H, the output voltage is given by

$$e_o = (2HR_L)XY = KXY \qquad (13)$$

where the load impedance R_L is chosen for the particular application.

A circuit which performs this function is shown in Fig. 27. As in all the multiplier circuits discussed previously, all signals are at DC ground potential. Output voltage waveforms of this circuit are shown in Fig. 28. Fig. 28a shows suppressed-carrier modulation of a 1-kHz carrier with a triangular wave. Figs. 28b and 28c show the squaring of a triangular wave and a sinewave, respectively. In both cases, the outputs retain the DC component as well as AC components.

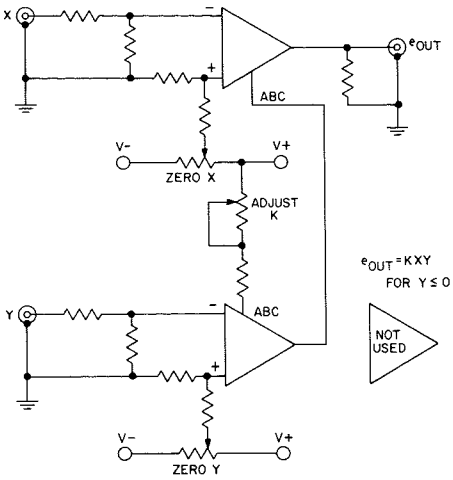


Fig. 23—Third- and fourth-quadrant multiplier.

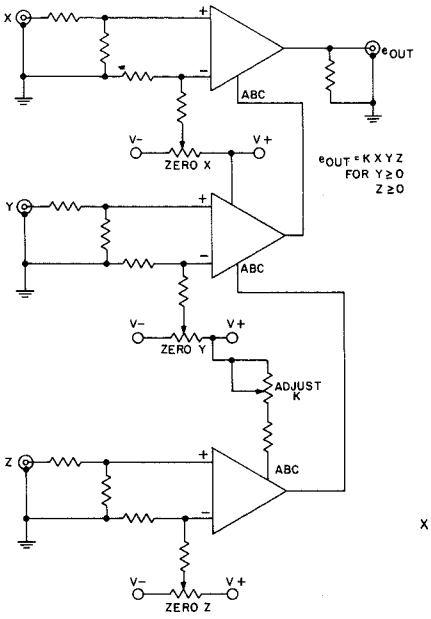


Fig. 24—A two-octant multiplier.

Other analog functions

As is the case for all multiplier circuits, squaring, dividing, and taking the square root can be achieved with OTA's by the simple application of well known methods.

Multiplexing

Fig. 29 shows a three-channel gated amplifier in which each amplifier or channel may be sequentially activated to display its input with gain of about 20dB. Because the input impedance is extremely high when the OTA is biased *off*, common feedback network may be used. Position control of each channel is accomplished with little interaction by applying offset adjustment to the inverting input of each amplifier. Activation of each channel is accomplished by cutting off normally saturated transistors shunting the amplifier-bias-current terminals. Drive to the transistor switches may be applied from a ring-counter-type circuit that is either externally triggered or "free run" to chop the signals.

A bistable/monostable circuit

Fig. 30 shows an OTA circuit that is stable in either of two states. In the lower state, the total circuit dissipation is zero. If the inverting input is made more positive than the non-

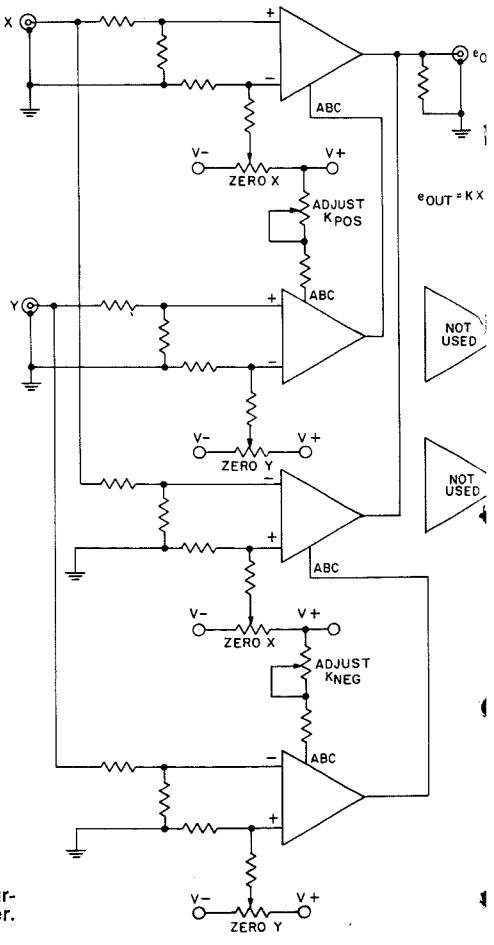


Fig. 25—A four-quadrant multiplier.

inverting input, the circuit becomes monostable in the zero-dissipation state. The inverting input may "float" if bistable operation is desired.

A one-shot circuit with nanowatt dissipation

The OTA shown in Fig. 31 develops a single pulse whenever it is triggered (at a low duty factor only). Circuit current is drawn only during the pulse time. Signal output may be extracted from $V+$, $V-$, or the OUT terminal. If the $V+$ or $V-$ lead is employed for pulse sampling, care must be used to observe the OTA common-mode rejection range. If the $V-$ lead is used, other circuits of the IC may be influenced when the $V-$ terminal and the substrate terminal are common (as is the case for the CA3060). Loading of the output must be light. This one-shot circuit can be biased to ignore trigger pulses if the inverting input is made more positive than the non-inverting input.

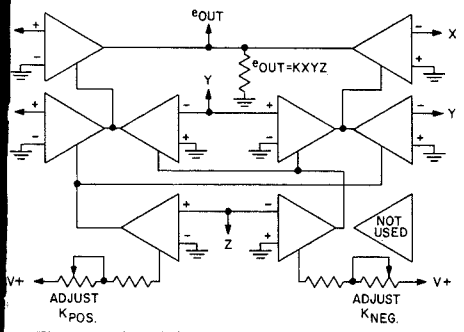


Fig. 26—An eight-octant multiplier.

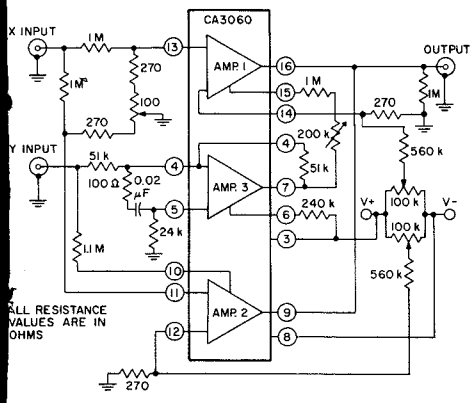


Fig. 27—Four-quadrant multiplication by means of double-balanced modulation.

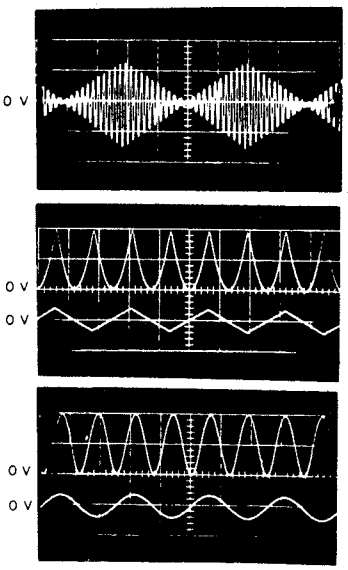


Fig. 28—Voltage waveforms of the four-quadrant multiplier of Fig. 27: (a) suppressed-carrier modulation of 1-kHz carrier with a triangular wave; (b) squaring of a triangular wave; (c) squaring of a sinewave.

A low-dissipation astable circuit

Fig. 32 shows an astable OTA circuit designed for low-duty operation. Power dissipation in the nanowatt level can be achieved with this circuit. Operation is similar to that of the circuits shown in Figs. 30 and 31. The circuit of Fig. 32 may be gated *off* by the inverting input. Pulse width and duty cycle are relatively independent of $V+$.

Sample-hold-read application

Fig. 33 shows a functional circuit in which the storage capacitor is essentially isolated from circuit loading during the *hold* period. Because both the charging OTA and the read OTA are biased off during *hold*, they contribute only leakage currents in this period. Capacitor C_1 is the storage capacitor. C_2 is a small capacitor used to assure stable operation.

Sample-hold-compare application

The OTA circuit shown in Fig. 34 samples a voltage, holds it, and compares it to a reference voltage E. As in the circuit of Fig. 33, loading of C_1 is negligible during the *hold* period.

Conclusions

The OTA concept requires the use of complementary conductive transistors (bipolar and/or unipolar) with no resistors. The CA3060 integrated-circuit OTA array has opened a new dimension to the creative circuit designer. New IC devices employing the OTA concept but with materially different characteristics are certain to follow.

Acknowledgments

The author thanks H. A. Wittlinger, L. Varettoni, and many others in Solid State Division who assist in the work described.

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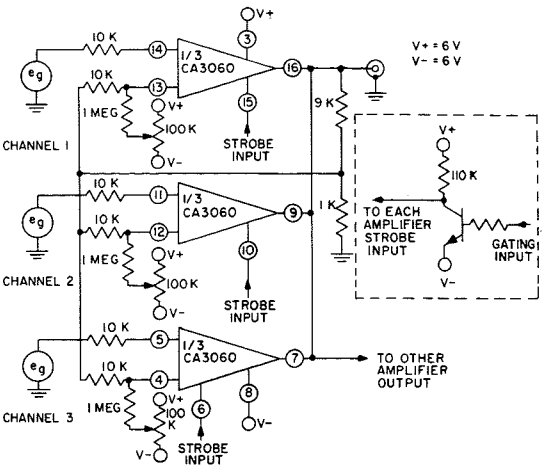


Fig. 29—Three-channel gated amplifier.

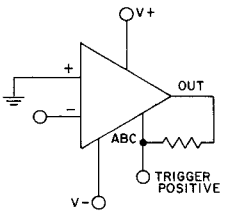


Fig. 30—Bistable/monostable OTA circuit.

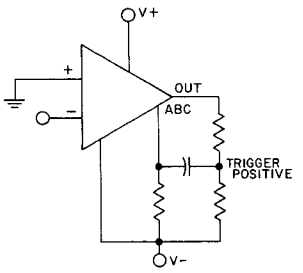


Fig. 31—One-shot circuit.

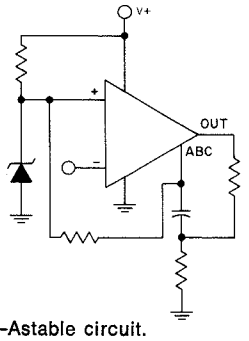


Fig. 32—Astable circuit.

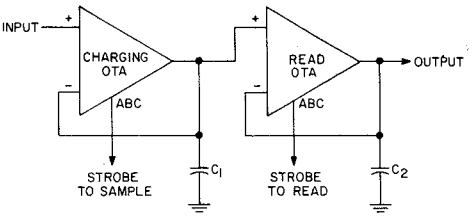


Fig. 33—Sample-hold-read circuit.

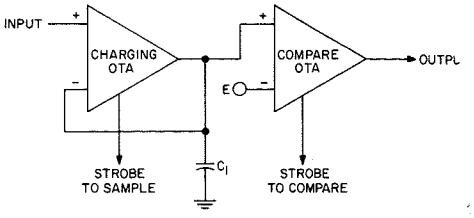
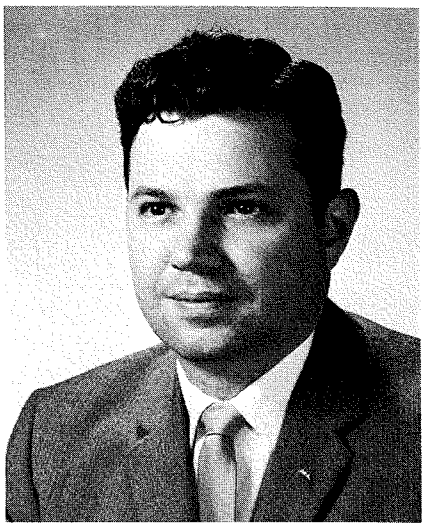


Fig. 34—Sample-hold-compare circuit.

Operational amplifiers . . . yesterday, today, and tomorrow

H. A. Wittlinger

Operational amplifiers are used today in various applications requiring voltage gain with minimum input and output level-shifting problems. Monolithic IC operational amplifiers offer the further advantages of low cost, improved performance, and stability. This paper reviews the development of operational amplifiers, starting with the tube-type units used first in analog computers and concluding with the present day monolithic integrated circuits. Typical design problems are discussed, and some possible future developments are described.



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received the BSEE from Case Institute of Technology in 1965. After graduation, he joined the Tube Division of RCA and was involved with horizontal deflection amplifiers and damper diodes. Before joining the Solid State Division he worked at the Astro Electronics Division. Here he was concerned with the design of television cameras for weather satellites and worked in the areas of video processing and regulating systems variations. In addition, he was responsible for the design of the synchronization system of the portable color TV camera used by NBC in the 1968 presidential conventions. He is presently a linear IC applications engineer, primarily involved with monolithic operational amplifiers. He has authored and co-authored many technical papers and participated in a number of linear IC panel discussions. He is a member of the IEEE.

The use of high-gain DC-amplifier techniques to solve or analyze problems involving differential equations has been in existence for at least 25 years. In 1947, J. R. Ragazzini, R. H. Randall, and F. A. Russell stated that "an amplifier so connected can perform the mathematical operations of arithmetic and calculus on the voltages applied to its input; it is hereafter termed an operational amplifier."[1] This period was the beginning of problem solving by means of the electronic calculators that eventually replaced mechanical differential analyzers. The early electron-tube amplifiers were of the single-ended-input inverting variety and usually employed dual-triode amplifiers with open-loop voltage gain of about 5000.

Probably the most popular early operational amplifiers were manufactured by G. A. Philbrick Researchers, Inc.; Goodyear Aircraft Corp.; and Electronic Associates. These companies are only a few of the many that offered operational amplifiers and full analog-computer systems. Later tube-type operational amplifiers manufactured by these companies employed differential-input amplifiers with input-offset-voltage drifts in the order of 1 to 5 mV over an 8- to 24-hr period. Input grid currents were less than 100pA, and output-voltage swings were in the order of ±100 V. Open-loop voltage gains ranged from about 1000 to more than 100,000, and unity-gain bandwidths were in the order of only 100 kHz. Despite the differential-input configuration of these early amplifiers, the inverting configuration was primarily employed, with the noninverting input used chiefly as a means of balancing the amplifier so that both input and output voltages were at zero.

As digital computers became more reliable and sophisticated, they took over many of the processes previously performed by analog computers. Despite this invasion, much of the peripheral equipment for digital computers still uses operational amplifiers in analog-to-digital converters which digitize computer input information from some type of analog sensor. Computer outputs are then processed by digital-to-analog converters (also using operational amplifiers) which either provide readout or actuate control equipment.

Today, the emphasis on the operational amplifier is outside the computer field in applications such as filters, comparators, multistable circuits, level shifting, buffering, video processing, or functions requiring a voltage-gain block that will minimize input and output level-shifting problems. Some of the reasons for the popularity of the monolithic operational amplifier are the lower cost, improved performance, and stability of the monolithic integrated circuit. Designers can now more easily achieve a performance determined by external feedback components, rather than having the amplifier parameters determine the circuit performance.

What is an operational amplifier?

The basic operational amplifier consists of a differential input stage followed by a gain stage and an output stage. (Table I lists some basic operational-amplifier terms; material in quotation marks shows EIA definitions.) From the standpoint of closed-loop stability, the number of stages beyond the input differential amplifier is usually minimized. This form is essentially the same as that used in later tube-type operational amplifiers.

Although monolithic construction improves the DC-input offset-voltage drifts by at least one to two orders of magnitude, lower drift rates are sometimes required. In these instances, chopper-stabilized amplifiers are usually employed. In this system, the input is alternately disconnected from the source and returned to ground to establish a zero reference for the signal that can then be AC-amplified and detected by similar means to provide synchronous signal detection. Fig. 1 shows a block diagram of the system. Because the upper frequency in the DC portion of this system is limited by the chopping rate, wideband AC amplifiers are

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Table 1—Operational amplifier terminology.

Input offset voltage *(V_{IO}):* "The DC voltage which must be applied between the input terminals to force the quiescent DC output to zero or other specific level."

Input bias current *(I_I):* "The current into the input or the average currents into the inputs for the purpose of establishing the quiescent or balanced state." This current is usually associated with bipolar input transistors. When junction field-effect input transistors are used, this current is more closely allied with input-gate leakage current; in the case of insulated-gate field-effect transistors, it is associated with the gate-protection diodes. A point to remember is that if the field-effect input circuit is not carefully designed and fabricated, the input current of these stages may exceed low bipolar input currents at elevated temperatures.

Input offset current *(I_{IO}):* "The difference between the current into the input terminals of a differential-input amplifier for the purpose of establishing the quiescent or balanced state." This parameter is associated with the beta mismatch of the input transistors and usually is about 10% of I_I.

Common mode rejection *(CMR):* This effect is the quality of a differential amplifier to reject or discriminate against a signal applied to both input terminals of a differential amplifier or operational amplifier.

Common-mode rejection ratio *(CMRR):* "The ratio of the differential voltage amplification to the common-mode amplification." This expression may be given as a ratio of A_{VD}/A_{VC} or, in dB, 20 $\log_{10}A_{VD}/A_{VC}$ where A_{VD} is the differential voltage gain and A_{VC} is the common-mode gain. As an example, an amplifier with a differential voltage amplification of 100,000 and a common-mode amplification of 0.01 has a ratio of $100{,}000/0.01=10^7$, or 140 dB. Alternately, this ratio may be considered in terms of the equivalent differential signal that would appear across the amplifier input as a result of the common-mode signal. In this case, for a 10-V common-mode signal, the apparent differential signal would be 1μV.

Common mode input voltage range *(V_{ICR}):* "The range of common-mode voltages which, if exceeded, will cause the total harmonic distortion to exceed a specified maximum value." When the common-mode input signal is within the common-mode voltage range, the amplifier-output signal is quite low, as explained above. As the input signal approaches the extremes in the common-mode voltage range, either the constant-current source or the differential amplifier saturates and generates a non-sinusoidal output for a sinusoidal input; thus, harmonic distortion may be used as a criterion. Another way of specifying this parameter is in terms of degradation of the common-mode rejection ratio. A 6-dB degradation should yield similar results, because the rise in the amplifier output is extremely rapid once the range is exceeded.

Slew rate *(SR):* "The time rate of change of the closed-loop amplifier output voltage for a step-signal input. Normally, slew rate is measured for the largest input step for which the amplifier performance remains linear with feedback adjusted for unity gain." Because slew rate is a direct function of amplifier phase compensation, the feedback condition requiring the highest compensation is the worst case for slew rate. The unity-gain voltage-follower configuration feeds back the entire output signal and thus requires the largest value of compensation components.

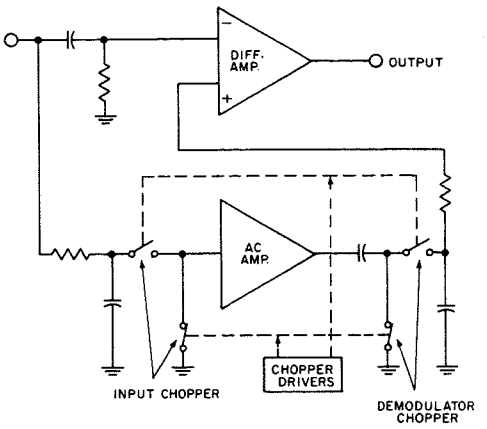

Fig. 1—Chopper-stabilized amplifier.

sometimes used in conjunction with the DC system to provide a stable broadband amplifier.

Methods for signal chopping vary widely from mechanical choppers or switches (used before operational amplifiers) to voltage-variable or light-variable resistors. MOS transistors are used in this application because they exhibit high on-to-off resistance ratios. Most of the operational amplifiers in this category are of the inverting configuration.

Another variation of the chopper-stabilized amplifier is the varactor-bridge configuration, in which the input-signal voltage modifies the capacitance of a balanced pair of varactor diodes. The signal is then AC-amplified and the output is again detected, usually synchronously. Although input offset-voltage drift is comparable to that of standard differential amplifiers, lower input-bias

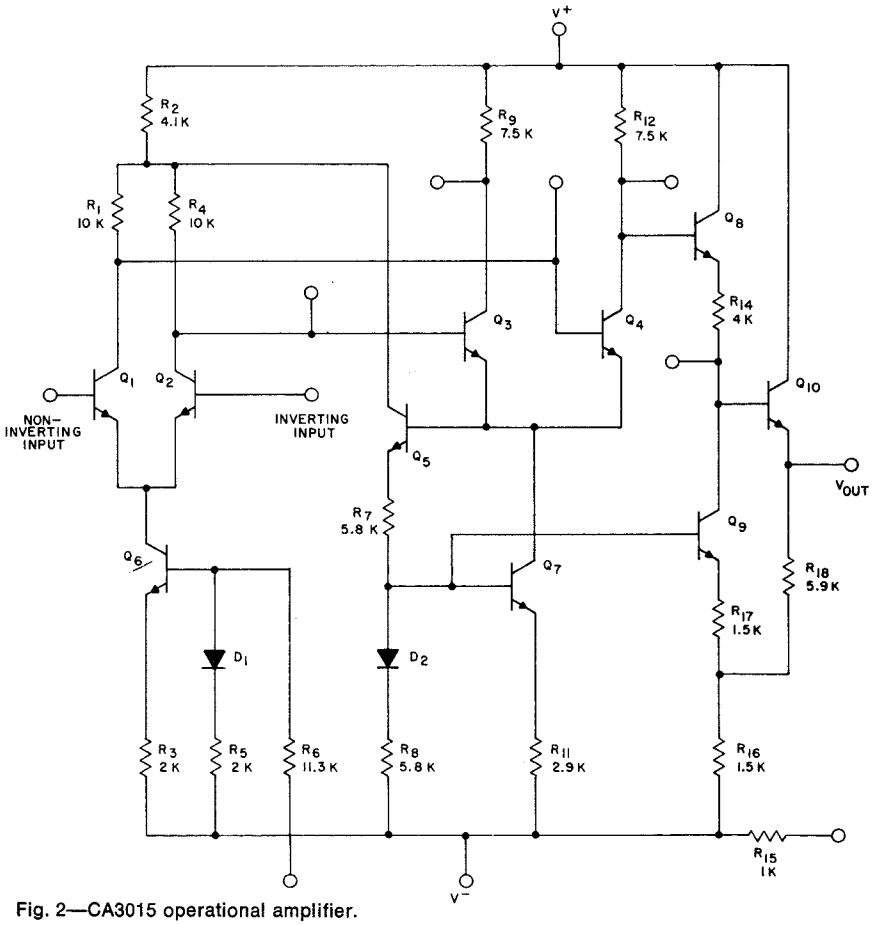

Fig. 2—CA3015 operational amplifier.

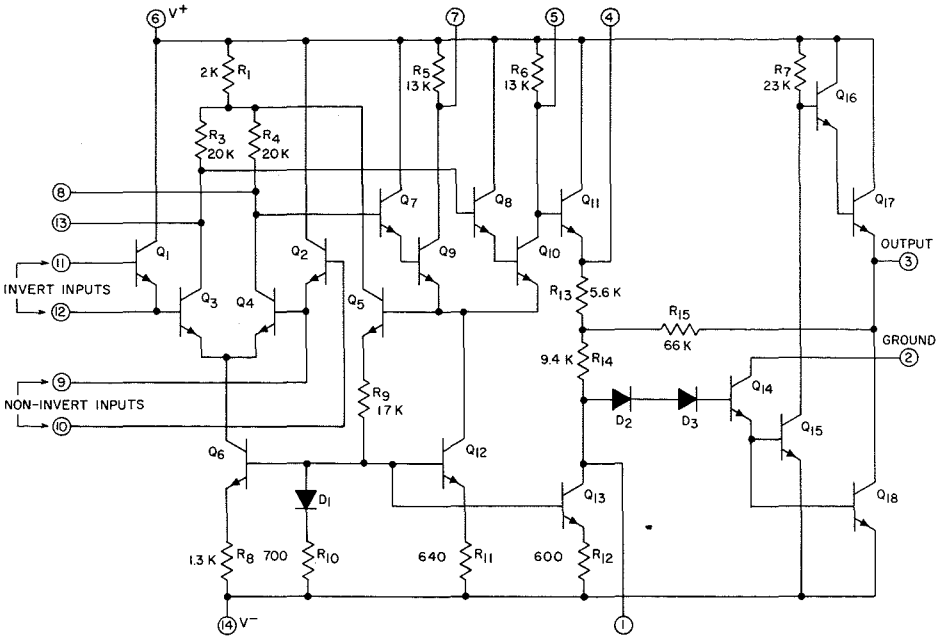

Fig. 3—CA3033 operational amplifier.

current and drifts are the major advantages of this configuration.

Monolithic operational amplifiers

The first operational amplifier introduced by RCA was the CA3010 series. This operational amplifier, shown in Fig. 2, provides a moderate voltage gain of about 60 dB and can be operated with symmetrical power supplies from ±3 V to ±6 V with a fully-compensated unity-gain frequency greater than 12 MHz. The improved performance and lower cost of this circuit made it quite popular. Later, as IC processing improved and the breakdown voltages of IC transistors increased, the CA3015 was generated from this chip. Further processing improvements made it possible to increase transistor beta, reduce input current, offset current, and offset voltage, and further extend the type into "A" versions for the higher-beta devices. From this basic chip, sixteen types have been generated to accommodate various packages, high- and low-voltage types, and high- and low-beta types.

One of the first linear integrated circuits to use P-N-P lateral and substrate transistors was the Fairchild μA709 operational amplifier. This amplifier provided improved performance in terms of level shifting and wider input common-mode voltage range and output swing. Because of the poor gain-bandwidth product of the P-N-P transistors, however, the upper-frequency response of the amplifier deteriorated. The unit operated from symmetrical ±15-V supplies with higher open-loop voltage gain, but a somewhat limited output-current capability.

In December 1967, RCA introduced the CA3033A operational amplifier, shown in Fig. 3, which could be operated from ±15-V supplies. In addition, a CA3033 was introduced for ±12-V operation. The output-current capability of these devices represented a marked improvement over that of the μA709 amplifier and was in excess of 60 mA from the push-pull class-B output stage. In addition, input-bias current reduced to 200 nA. Because of the output-power capability of the CA-3033, the unit has been designed into many control systems in which the extra output power is used to drive small servo motors and other power devices.

All of these operational amplifiers have some disadvantages. First, they are not short-circuit proof. Because of the extreme high power output of the CA3033, no output short-circuit protection is provided. The CA3015 and μA709 operational amplifiers tolerate momentary shorts but cannot limit output-stage dissipation under sustained shorts. In addition, all of these amplifiers will latch in the voltage-follower configuration if the noninverting input is allowed to saturate. The actual mechanism of this latch is straightforward. Once the inverting transistor has saturated, that transistor no longer functions as an inverting stage, and the former negative feedback becomes positive. With the addition of external components, this latch condition may be eliminated.

To overcome some of the problems associated with operational amplifiers, National Semiconductors, Inc. designed the LM101 operational amplifier. This circuit overcomes some of the previous design limitations. With a moderate degree of complexity, the LM101 provides output short-circuit protection by limiting the output current and allows latch-free operation by extending the input common-mode voltage range so that the input differentials cannot become saturated. In addition, the use of an N-P-N/P-N-P combination for the input amplifier provides much higher input breakdown voltages. This circuit provides a two-stage design, with phase compensation accomplished by a single external capacitor. This improved input differential stage served as the basis of a new Fairchild operational amplifier, the μA741, that offers a good compromise between complexity and performance. This device is also manufactured by RCA as the RCA-CA3056 and CA3056A. These devices have the advantages of the LM101 front-end design plus the phase-compensation capacitor built on the chip. For simpler lower-frequency designs, therefore, only the addition of external-feedback components is required for circuit operation. Although this circuit has an advantage in applications that require only a limited lower-frequency response, it has limitations at higher frequencies, where the gain is low because of the internal phase compensation. Fig. 4 shows the gain vs. frequency curves for the compensated CA3056 and the μA741 series of operational amplifiers as compared

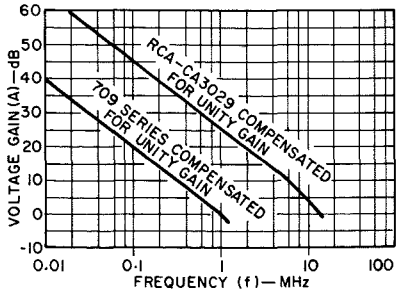

Fig. 4—Gain as a function of frequency of the CA3029 and 709 series operational amplifiers. (Note the increased gain and bandwidth available in the CA3029 amplifier.)

to that for the CA3029 amplifier series also compensated for unity gain. The CA3029 has considerably more gain and thus greater accuracy at the higher frequencies.

In digital-to-analog converters, it is desirable to reproduce the required analog outputs at rates comparable to modern-day digital speeds. In many cases, therefore, the converter must operate at many megahertz to portray the digital output accurately. As a result, efforts have been made to improve the large-signal amplifier-response speed. The term used for this effect is slew rate, or the rate of change of the amplifier output with a step input. Magnitudes for slew rates of present monolithic operational amplifiers with diode isolation (as opposed to dielectric isolation) are in the order of 30 to 50 V/μs. Hybrid designs have slew rates between 1000 and 2000 V/μs.

Although high slew rates are desirable to improve response, settling time must also be considered. Although the amplifier output may move towards the required level quickly, the high-frequency gain determines the time and accuracy in which the output reaches that level. Fig. 5 shows a curve of slew rate for a sinewave signal in terms of frequency and amplitude. These curves actually represent the maximum rate of change of a sine wave going through zero crossing.

Another important aspect of high-slew-rate amplifiers is the driving current capability. Fig. 6 shows a curve of slew rate as a function of available driving current for various load capacitances. From this curve, it is evident that high driving-current capability must be available in high-slew-rate amplifiers if the amplifier is to drive any reasonable capacitive load.

Future

New developments will undoubtedly provide new and improved monolithic operational amplifiers. For example, the use of super-beta transistors will help to raise input impedances by at least two orders of magnitude. In addition, insulated-gate field-effect transistors will be used on the input stages of some of these amplifiers to provide high input impedance without the high-temperature leakage associated with junction field-effect transistors.

Increased supply-voltage ranges will also be available in magnitudes comparable to those of tube-type operational amplifiers. In line with increased voltages, increased dissipation capability will result from advances in both packaging and integrated-circuit design. Higher output currents will also be available.

Higher speeds are also expected, with slew rates in excess of 1000 V/μs at reasonable gains. The limitation in this case involves the external isolation of input and output signals.

Offset-voltage drifts in the single differential-amplifier configuration (no emitter-follower inputs to the differential) are in the order of one to two microvolts per °C. It is not unreasonable to expect one to two orders of magnitude improvement in this characteristic without resort to self-heating and temperature-sensing on the chip. These improvements will result from both processing and design innovations.

One of the most significant advances in the field of operational amplifiers is the operational transconductance amplifier [see "The operational transconductance amplifier—a new circuit dimension" by C. F. Wheatley, Jr., in this issue]. The techniques used to eliminate the level and frequency-restricting resistor in the IC design, coupled with the available gating and switching options, promise entirely new families of both operational voltage amplifiers and operational transconductance amplifiers. This ability to control the amplifier characteristics over many decades of current is exciting and opens new areas of application that were not previously available to designers.

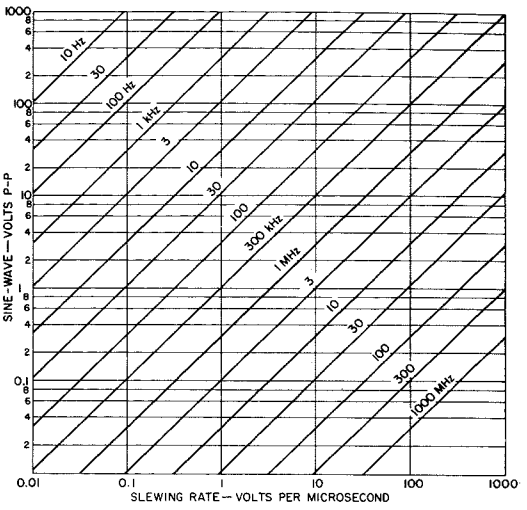

Fig. 5—Slew rate as a function of peak-to-peak sinewave signals for families of frequencies.

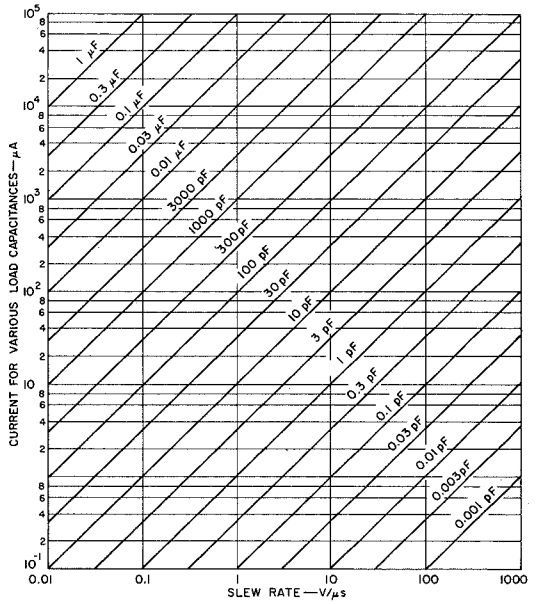

Fig. 6—Slew rate as a function of driving current for various values of capacitance *(dv/dt=I/C)*.

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Design considerations for a monolithic sense amplifier

J. P. Keller

A sense amplifier can be described as an interface circuit that connects the storage elements of a memory to the logic output elements of that memory. By this description, a sense amplifier can have a wide range of input and output requirements, depending on the type of application. There are some characteristics, however, that are important in all memory systems, including the ferrite-core memories discussed in this paper. These characteristics are threshold uncertainty, propagation delay, amplifier-overload recovery, input common-mode characteristics, and supply-voltage insensitivity. This paper discusses design considerations for a monolithic sense amplifier and demonstrates techniques for optimizing all these important performance characteristics.

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THE SIMPLIFIED BLOCK DIAGRAM of a typical ferrite-core memory subsystem shown in Fig. 1 illustrates the location of the sense amplifier in the digital-computer memory organization and indicates the amplifier performance requirements. When a *read* command (to read a core) is sent to the memory-address register, the chosen x and y address lines are selected. Although the selection technique depends on the memory organization, the most common organization uses one core per bit so that the total number of simultaneously sensed cores is determined by the total word length.

As shown in Fig. 2, each core of the memory is threaded by two wires; one wire is common to all cores in a row and another wire is common to all cores in a column. When a particular core is selected, the sense amplifier detects the presence of a *one* or a *zero*. This information is then placed in the memory data register, as shown in Fig. 1. The time required for the information to move from the cores to the memory data register is called the *access time*. If the memory organization is such that destructive readout (DRO) occurs, the information entered in the memory data register must be written back at the same memory location. The time required to write this information back is called the *write time*. The sum of the *read time* and *write time* is defined as the memory *cycle time* and determines the memory speed, i.e.: how fast another bit of information can be retrieved from the memory.

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Both reading and writing are carried out by application of a current through the wires that connect the cores (x and y select lines of Fig. 2). In a coincident-current-type memory, for example, if this current exceeds some value, I_m, the core is reset to a stable magnetic condition that results from its residual flux density (remanence). Any selected core can be reset by application of a current equal to $I_m/2$ through one of the x-address lines and $I_m/2$ current through one of the y-address lines. The core common to both x- and y-address lines is affected by the x and y current sum and is reset. All the other cores located on either the x- or the y-address lines are "half selected" and produce an induced noise voltage. The original magnetic condition of a core may be reestablished by reversal of the current in the two selecting wires.

Reading is accomplished by connection of all the cores with a sense-line winding that is routed to optimize the signal-to-noise ratio. The sense line may be wound through half the cores in one direction and in the opposite direction through the other half. In this manner, stray voltages induced in the sense line partially cancel out. Fig. 3 shows a typical threading of the sense lines.

Any particular core is read by use of a current, applied as described above, to write a *zero* into that core. If the core was in a *one* condition, it switches to a *zero* condition. The switching core then generates a pulse which is picked up by the sense line. If the core is already in a *zero* condition, no pulse is generated.

In addition to the half-select noise and the switching pulse, other signals may be present on the sense line. A large common-mode pulse may exist as a result of the capacitive coupling between the sense line and the selected address line. Noise can also exist as a result of inductive pickup by the sense line itself. If the generated noise amplitude is sufficient, the noise pulse may be recognized as a *one* by the sense amplifier. On the other hand, the amplitude of the *one* pulse may be degraded to such an extent that the sense amplifier detects it as a *zero*. The sense amplifier must, therefore, detect the difference between the *disturbed one* voltage and the *disturbed zero* voltage and reject other noise voltages picked up by the sense line. The threshold voltage of the sense amplifier needs to be adjusted approximately mid-way between the maximum *disturbed zero* voltage and the minimum *disturbed one* voltage, as illustrated in Fig. 4.

The input-voltage range between these two limits is called the uncertainty region. In this region, the amplifier cannot always detect the difference between a *one* and a *zero*. The uncertainty region, therefore, must be minimized as much as possible.

Because of the manner in which the sense line is wound in the memory plane (Fig. 3) a *one* signal of either polarity is produced on the sense line. The sense amplifier must be responsive to bipolar (positive or negative) signals indiscriminately, being sensitive only to their amplitude. In addition, it must be able to withstand large common-mode or differential signals and recover quickly from this overload. During this recovery time, the amplifier may or may not be operative. For example, in a 3D type of memory, a large differential signal appears just before *read* time. This signal normally saturates the input stage of the sense amplifier. Nevertheless, the amplifier must recover rapidly to detect and process the signal generated by the switching of the sensed core that follows the saturating signal. The time at which the amplifier has settled within 1% of its steady-state value is called the *differential-mode recovery time*. This time is an important factor in the determination of the memory-cycle time.

A large common-mode signal may also be present at *read* time. It may have an amplitude sufficient to drive the input out of its linear range. The maximum common-mode range voltage that the amplifier can be subjected to and still detect and process a small differential signal is called the *common-mode range*.

For protection against the amplifier firing of an output outside of *read* time, the output digital gate or the input analog amplifier (or sometimes both) is gated from a strobe line so that the system is enabled only during the time a core is being read.

In the use of a multi-channel sense amplifier featuring independent inputs but a common output for all channels, additional gating is required to switch the chosen input channel to an "enable" condition prior to *read* time, all other channels being kept in their normal inhibited state. An additional advantage of this gating procedure is that the amplifiers will not process signals outside the narrow "read" time and thus will not be saturated by large signals occurring outside the *read* time and will have shorter recovery time.

Monolithic-sense-amplifier design requirements

In accordance with the previous discussion, a multi-channel monolithic sense amplifier should meet the following list of requirements:

1) It should be as versatile as possible;

2) The design should meet a wide variety of speed requirements;

3) The circuit should be suitable for low-cost fabrication;

4) The amplifier should be able to detect bipolar signals;

5) The threshold should be adjustable over a wide range of threshold voltage (to meet the maximum number of requirements with a single amplifier);

6) The threshold voltage should be constant with temperature;

7) The threshold uncertainty region should be as small as possible;

8) The power supplies used should be the type normally used in digital system and the tolerance on these supplies should be as large as possible;

9) The sense amplifier should include provision for a gating signal to enable the chosen amplifier channel and a strobe signal for an eventual *enable* signal to be applied to the output gate;

10) The bandwidth of the amplifier should be sufficiently high to pass the fastest risetime signals with as little degradation as possible;

11) The amplifier should be able to recover rapidly from large differential-mode signals; and

12) The amplifier should be able to handle common-mode signals as large as possible.

TA5654 design philosophy

Fig. 5 shows a block diagram of the RCA Dev. No. TA5654. This circuit consists of an analog amplifier with two differential input stages, a bipolar detector, a DC restorer, a threshold-voltage adjustment, a TTL output gate, an output-strobe circuit, and input gating circuits for channel selection. In this design, only one sensing channel of the amplifier may be in the *enable* condition at any given time. Fig. 6 shows typical signal waveforms of the sensing system. Of particular interest is the fact that the amplifier

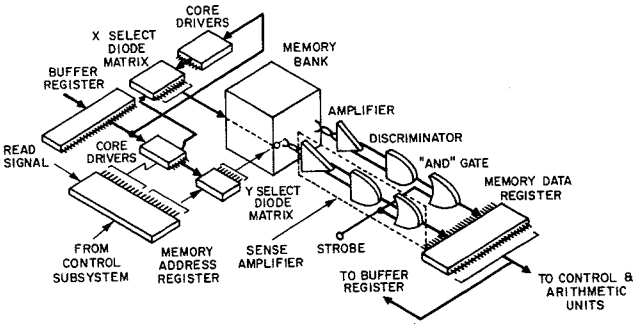

Fig. 1—General-purpose coincident-current-core memory subsystem.

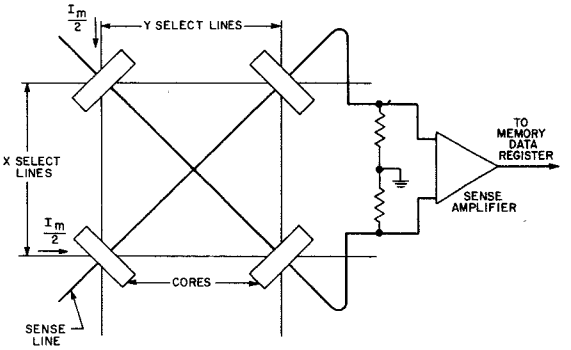

Fig. 2—Half-select wiring showing each core of the memory threaded by two wires.

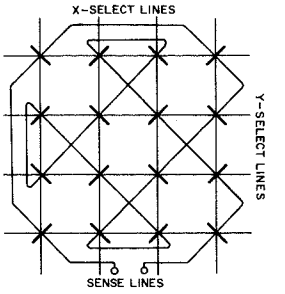

Fig. 3—Core sense-line wiring showing typical threading of the sense lines.

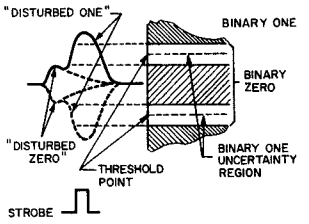

Fig. 4—Typical core output signal.

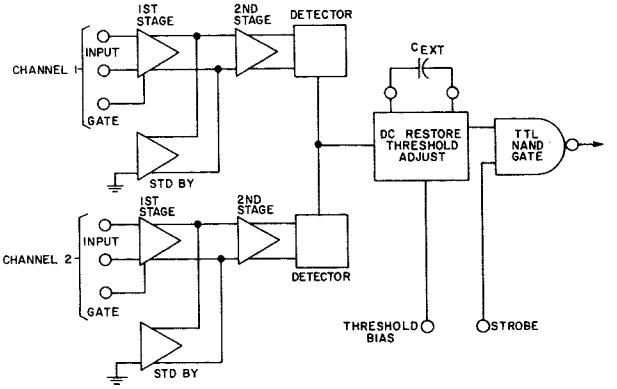

Fig. 5—Block diagram of RCA Dev. No. TA5654.

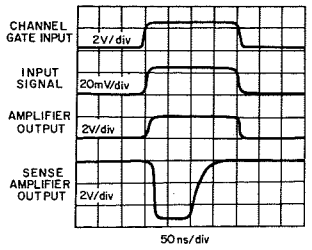

Fig. 6—Typical operation characteristics of RCA Dev. No. TA5654..

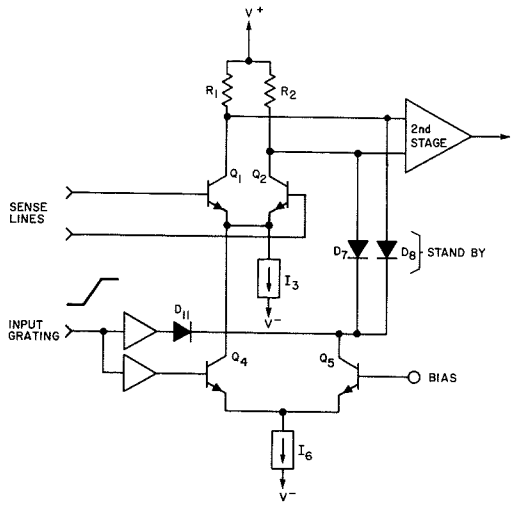

Fig. 7—Functional diagram of the first stage RCA Dev. No. TA5654.

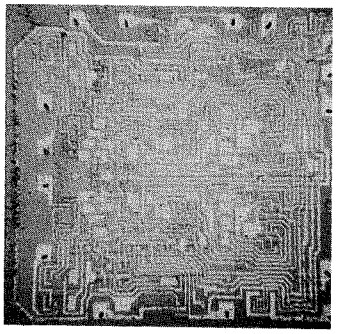

Fig. 8—The chip layout of the RCA Dev. No. TA5654 two-channel sense amplifier.

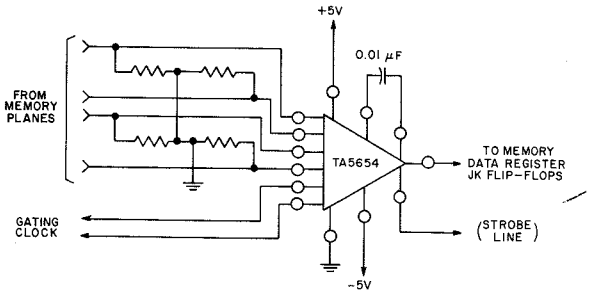

Fig. 9—Typical system interconnection using RCA Dev. No. TA5654.

can be gated ON just prior to signal time and turned OFF after the signal has been received. This procedure prevents processing of the noise signals present during the read-write cycle and significantly decreases the sense-amplifier recovery time because the amplifier is kept out of saturation. This amplifier can operate in systems with memory cycle time less than 500 ns.

Circuit description

A simplified diagram of one channel of the TA5654 circuit is shown in Fig. 7. During standby operation (not gated), each input transistor (Q_1 and Q_2) conducts half of the I_3 current and each diode (D_7 and D_8) conducts half of the I_6 current through transistor Q_5, which is biased at a base voltage of −2.35 V. The base of transistor Q_4 is set at −2.7 V by the channel-gate input when in its logical *zero* (+0.4 V) condition.

The channel gates are designed to operate with DTL or TTL logic levels. The bias on the base of transistor Q_4 keeps it OFF and allows transistor Q_5 to be ON and draw I_6 current, as described above. The current I_6 is adjusted to $1.2I_3$ to reduce the input-stage gain to zero and effectively block out unwanted noise (the diodes D_7 and D_8 present a low-impedance path). When the gate input is raised to a logical *one* level, the base of transistor Q_4 rises to −2.4 V and turns Q_4 ON and Q_5 OFF. The current I_6 is therefore shifted from transistor Q_5 to transistor Q_4, and through Q_4 to transistors Q_1 and Q_2. The input amplifier is then in its high-gain condition and is ready to process the sense-line signals. Because the current through R_1 and R_2 is constant at $\frac{1}{2}(I_3+I_6)$, however, the operating point (and thus the biasing of the following stages) does not change as the input stage is switched from zero to high gain. At the same time diode D_{11} back-biases D_7 and D_8, and thus reduces the capacitance at the collector of Q_1 and Q_2 and allows greater processing speed.

Speed

The above description indicates that the input stage fulfills all the requirements for a sense amplifier and also has high-speed capability. Part of this speed results from the fact that the input stage is already biased at some given value. Because of this biasing, the input stage reaches full collector current in a shorter time than if it had to start from zero current (if it were completely cut off).

Bandwidth

The amplification section of the sense amplifier includes two cascaded differential amplifiers with emitter-follower buffering between them. The number of emitter-follower stages is dictated by DC-level considerations. This buffering between the two amplifier stages significantly increases the bandwidth of the sense amplifier because a low-impedance source is provided to drive the Miller capacitance of the second amplifying stage.

Temperature compensation

Each amplifier stage has emitter-degeneration resistors to reduce and control the voltage-gain variations from channel to channel and unit to unit. The biasing of the amplifier is selected so that essentially constant gain is obtained over the full temperature range usually required for military equipment. In essence, the constant-current biasing point, the constant-current emitter resistor, and the current through the transistor are selected so that essentially constant gain is obtained regardless of temperature.

Small-signal gain

The small-signal gain of the amplifier is set to a typical value of 66, and the gain A is given by the following expression:

$$A=\frac{2(V_1-V_{BE(Q_6)})\left(\frac{R_1}{R_3}+\frac{R_1}{R_6}\right)}{0.104+0.66(V_1-V_{BE(Q_6)})\left(\frac{R_8}{R_3}+\frac{R_8}{R_6}\right)}\cdot\frac{(V_1-V_{BE(Q_{24})})\frac{R_{22}}{R_{24}}}{0.104+0.66(V_1-V_{BE(Q_{24})})\frac{R_{27}}{R_{24}}}$$

where $V_1=V-[R_5/(R_4+R_5)]$ and it is assumed that $V_{BE(Q_5)}=V_{BE(Q_6)}$. This expression is accurate to within a few percent for the first stage of the RCA Dev. No. TA5654; however, it predicts a voltage gain about 10 to 15% higher than obtained for the second stage, primarily as a result of the use of a small-signal analysis for predicting the circuit behavior.

The amplifier proper is terminated by a detector consisting of two emitter-followers (Q_{25} and Q_{26}) that perform an OR operation necessary to present the appropriate signals to the gate that follows. A double detector is required to accommodate the bipolar nature of the input signals.

DC restore and threshold adjust

The DC-restore and threshold-adjust circuit consists of transistors Q_{61} and Q_{62} and the associated diodes and resistors used to establish the DC operating point of Q_{61} and Q_{62}. The threshold of the sense amplifier depends on the DC voltage at terminal 14. Because resistor R_{61} is much larger than R_{65} or R_{66}, changes in DC voltage at terminal 13 are reflected as changes in DC voltage at terminal 14 through the diode chain D_{63} to D_{66} and the transistors Q_{61} and Q_{62}. This change in DC voltage results in an apparent change of gain in the analog amplifier which is reflected to the input as a change in the threshold voltage.

The signal transmission from the detector Q_{25} and Q_{26} to the input of the output gate can be explained as follows. An input to the sense amplifier causes a positive-going signal at terminal 1 which, in turn, causes a change of DC level at terminal 14 through the 0.01-μF capacitor connected between terminals 1 and 14. This signal reverse-biases both Q_{62} and the base-emitter diode of Q_{72}. Simultaneously, the external capacitor charges through resistor R_{63}, and the voltage at pin 14 decreases. When the input signal is removed, Q_{62} is turned ON and the impedance at terminal 14 decreases so that the capacitor is rapidly discharged as a result of the emitter-follower action and the steady-state DC operating voltage is restored at terminal 14. Because the base of transistor Q_{62} is driven from a low-impedance source, the transient produced during the capacitor discharge results in a negligible change of the DC level at the base of Q_{61}.

Output gating

The output gate is similar to a standard TTL gate. Both the amplified signal from the ferrite-core memory and the strobe line must be above the gate threshold level before the output transistor Q_{74} will saturate. This output transistor is capable of handling a current of 10 mA with a saturation voltage less than 400 mV. In terms of temperature changes, the threshold of the output gate changes at a rate of $2V_{BE}$/°C. However, the overall sense-amplifier threshold is maintained at a constant value because the DC voltage at terminal 14 varies as a function of temperature. This effect is achieved through the use of the diode compensation chain D_{63} through D_{66}. The amplifier section, as noted previously, has essentially constant gain with temperature and requires no further compensation.

Threshold uncertainty

Of all the factors affecting the proper function of a sense amplifier, the input thresholds are of paramount importance. For control of these levels, the uncertainty region must not exceed the specified limits of ±3 mV around the ideal threshold value of 17 mV. This threshold uncertainty is caused by the input offset current, the input offset voltage, the gain variation, the differential offset at gating, and the insensitive region of the comparator (the transition region). The contribution of these parameters can be evaluated as follows:

Input offset current (R_s = 150 ohms, $\beta_{m\ in}$ = 50, $\Delta\beta$ = 10%)	±0.5 mV
Input offset voltage ($V_{BE_1} - V_{BE_2}$ = 1 mV)	±0.5 mV
Gain variations	±2.5 mV
Differential offset at gating (change in I_c)	±0.5 mV
Insensitive region of gate	±1.0 mV

Although a worst-case calculation indicates an uncertainty band of ±5 mV rather than the ±3 mV alloted, the parameters causing this threshold uncertainty band are all of a random nature and their contributions would normally be less than maximum and not all in the same direction. It is reasonable to assume a threshold uncertainty with a standard distribution. The threshold uncertainty expected from such an assumption can be evaluated by calculation of the root-mean-square value of the contributors:

$$(0.5^2 + 0.5^2 + 2.5^2 + 0.5^2 + 1.0^2)^{1/2} = \pm 2.84 \text{ mV}$$

This value satisfies the specifications. The RMS value given above assumes that a normal (Gaussian) distribution exists and that the acceptable product will fall within a one-sigma deviation.

In the allocation of uncertainties, the contribution of the insensitive region of the comparator (i.e., the transition of the input-output of the TTL NAND gate) was indicated as +1 mV maximum. Data obtained on the TTL gate indicate that the transition region will not exceed 120 (or ±60) mV. This contribution is then ±60/66 = ±0.92 mV where 66 is the amplifier gain.

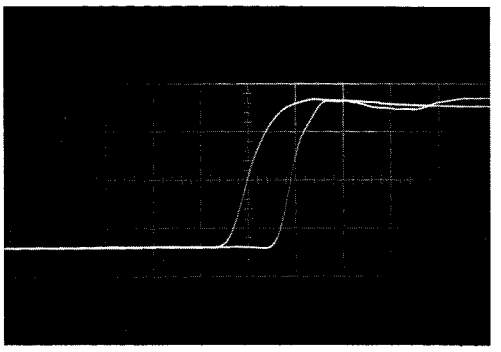

Fig. 10—Typical waveform (gate-to-input propagation time is 10ns/div.).

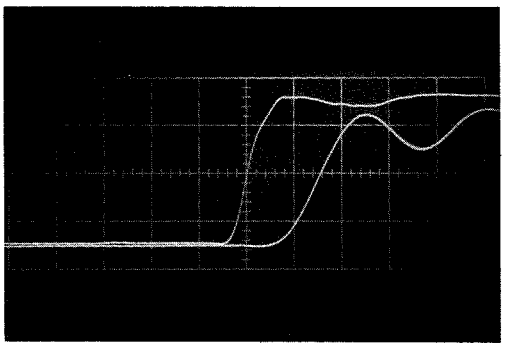

Fig. 11—Typical waveforms (gate-to-input propagation time is 50ns/div.).

The maximum gain variation allowed to meet a specification of ±2.5 mV of uncertainty is (2.5/17) (100) = 14.7%. Thus, the overall amplifier gain should not vary by more than 15%. If it is assumed that resistor ratios can be held to within 6%, the amplifier gain variation should be only 14%.

Experimental results

Fig. 8 shows the chip layout of the RCA Dev. No. TA5654 two-channel sense amplifier. The good layout symmetry of this analog amplifier is immediately apparent. The chip measures 82×82 mils and undergoes a standard analog monolithic IC processing.

Fig. 9 shows typical system interconnections. Measurements show that the typical input-to-amplifier-output propagation time is 15 ns; the gate-to-input turn-on time is 9 ns for a 50% input-voltage overdrive. Figs. 10 and 11 show oscillograms of typical waveforms. The measured threshold voltage centers higher than expected (17 mV). This condition will be corrected on future samples by trimming of some low-value resistors which establish current and gain levels.

Fabrication of Al_2O_3 COS/MOS integrated circuits

Dr. F. B. Micheletti | P. E. Norris | Dr. K. H. Zaininger

Operating integrated circuits have been fabricated using Al_2O_3 as the gate insulator. These circuits demonstrate a high degree of radiation hardening and prove the feasibility of Al_2O_3 MOS technology. In this paper, the processing steps are described and the important electrical properties are given.

In Metal-Oxide-Semiconductor (MOS) devices, the dielectric film used as gate insulator is an active, integral part of the device, and device operation and characteristics are very sensitive to its properties. Hence, in MOS technology, emphasis is placed on the fabrication of this oxide rather than on diffusion as in bipolar technology.

For a large number of non-critical applications, the currently commercially available MOS units with SiO_2 gate oxide are adequate. The processing is now well under control and has been reduced to a relatively straightforward procedure. Excellent results have been obtained with increasingly larger and more sophisticated integrated circuits so that low-cost large-scale integration (LSI) of MOS circuits offers considerable promise for the future. However, for certain more critical requirements, two major reliability problems have been encountered:

1) The migration of minute traces of impurities through the films (especially at elevated temperatures and under high field conditions) results in serious drifting and changes in the device characteristics;
2) Radiation also causes drift and/or degradation in device characteristics due to charge generation and trapping in the oxide.

Recently, technological advances were made that allow improved performance of MOS devices in these areas by utilizing aluminum oxide as the gate insulator. Aluminum oxide made by two different techniques has led to significant improvements in resistance to both bias-temperature stress and radiation exposure.[1,3] These techniques are:

1) Plasma anodization of *Al*,[4,5] and
2) Low temperature pyrolytic decomposition[6] of *Al*-alkoxides.

Plasma-grown Al_2O_3 shows, at present, the most promise for COS/MOS applications and will be the subject of this paper. When used as the gate insulator, it can lead to the following advantages:

1) *Low ion drift properties:* This is perhaps the most important gate insulator characteristic. Al_2O_3 resists ion drift perhaps orders of magnitude better than SiO_2. This means that MOS devices made from it exhibit stability to bias-temperature stress, a property that manifests itself in two very practical results: (a) ultraclean technology as required for SiO_2 (state-of-the-art)[7] devices would *not* be necessary (this should reflect itself in the cost, yield, and uniformity of LSI arrays), and (b) Al_2O_3 could act as a junction seal and encapsulant for both MOS and bipolar LSI. A thin film of Al_2O_3 on a junction or over an MOS device would act as a passivation layer giving the equivalent of a hermetic seal.

2) *Radiation resistance:* Measurements made to date on MOS devices on single crystal silicon show good radiation resistance,[1,2,8] better than SiO_2[9] and Si_3N_4 devices.[10] This is important to arrays that will be exposed to the radiation fields of space or nuclear environments. The reason for this improvement is most probably connected with the particular defect structure of Al_2O_3.

Other important properties are summarized in Table I.

Table I—Properties of plasma-grown Al_2O_3

Relative dielectric constant	8.0 to 8.7
Loss tangent (f = 100 kHz)	0.02
Surface-state density	2×10^{10} states/cm^2-eV
Index of refraction	1.67 to 1.70

Plasma-anodization process

The technique of plasma anodization of a metal to form the metal oxide is a relatively new one and, to date, has been primarily used to form oxides of metals for thin-film capacitors. The most prominent materials[4,5] formed have been Al_2O_3 and Ta_2O_5. In general, it has been found that these insulating films are amorphous with a low dissipation factor and a high breakdown strength.

Plasma anodization is carried out in a vacuum system that has been modified as shown in Fig. 1. The aluminized silicon wafer is placed in a closed insulating sample holder which has openings for exposure of the front surface of the wafer and for admission of a contact lead. Electrical contact is made to the back of the wafer with a pressure contact jig. Once the sample is in place, the system is evacuated to 1×10^{-6} Torr and back-filled with dry oxygen. The pressure is set at 0.3 Torr, and a glow discharge is ignited between anode and cathode. The sample, which is in the glow or "positive column" portion of the discharge, is biased positively with respect to the wall potential (defined as the potential which, when applied to a conducting probe in a plasma, reduces the current flow to zero). Because the wall potential may vary considerably during one anodization, depending on the condition of the anode, it must be monitored throughout the anodization. This is accomplished by adding an additional electrode to serve as a plasma probe.

The growth rate of the oxide is greatly dependent on the geometry of the anodization system and is not always linear with voltage. If the film is thick enough so that it is not completely anodized, the growth is self-limiting in a fashion analogous to that of wet anodization. Typically, the oxide is observed to grow at 22Å/volt—although this can vary considerably with the geometry of the anodization system and the mode of operation.[11] For MOS applications, the aluminum film must be completely anodized since any free *Al* at the interface would act as surface states. Hence, a potential sufficient to anodize all the aluminum must be applied. This potential, however, must not be too high or a thin film of SiO_2 can be formed at the silicon interface. The SiO_2 so formed can cause electrical instability (hysteresis in C-V testing) as well as deterioration in the resistance to ionizing radiation. The presence of the SiO_2 layer can be detected by ellipsometry measurements which reveal considerable deviation in the index of refraction and measured film thickness from that expected for Al_2O_3 alone For the circuits fabricated in this in

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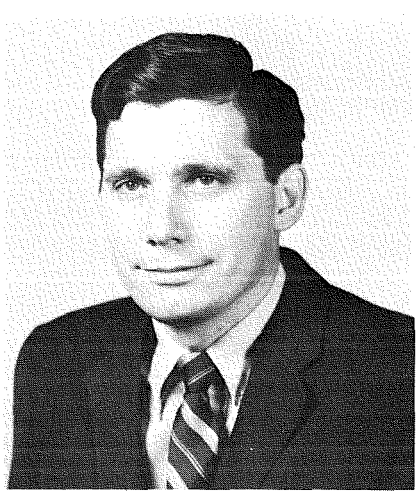

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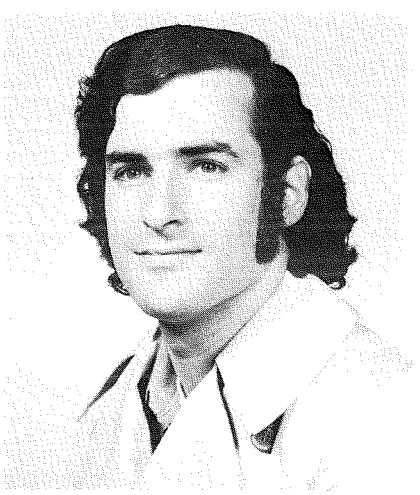
received the BSEE with Highest Distinction, from Purdue University in 1963. From 1963 to 1965 he attended Princeton University, receiving the MS in 1965. During the same period, he was a member of the staff of RCA Laboratories on the Research Training Program working in the area of Magnetic Memories, Epitaxial Deposition of Germanium thin films and chemically-deposited CdS thin films. Following a year of full time study at Princeton on an NSF Fellowship, he returned to RCA. He received the PhD in EE in 1968 from Princeton University. His thesis research was concerned with the effects of chemisorbed oxygen on the photoelectronic properties of polycrystalline CdS films. At present, Dr. Micheletti is engaged in research on silicon-aluminum oxide MIS devices and technology.



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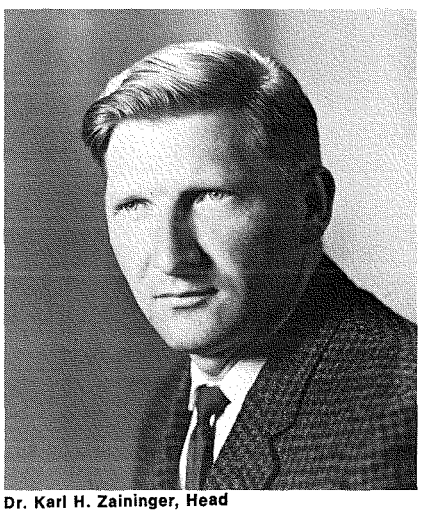
received BSEE from MIT in 1965. From 1965 to 1967 he attended graduate school at MIT receiving both the MS and Engineer's degrees in 1967. During this period he was a member of the Laboratory for Insulation Research working in the area of high resistivity semiconductors. In 1967 he attended the University of Colorado before joining RCA Laboratories in 1968. As a member of the Research Training Program at the Laboratories, he worked on large screen TV displays, photochromics and radiation damage in MOS devices. At present he is engaged in research on improved insulation for IC technology.



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vestigation, good-quality Al_2O_3 films on *Si* were obtained under conditions listed in Table II. As shown in Fig. 2, a constant current is maintained until the desired voltage, indicative of a certain film thickness, is obtained. This voltage is then held constant, and the current is allowed to decay. The net voltage on the sample is the applied voltage minus the wall potential.

The utilization of the plasma oxide is much more difficult for active device configurations than for simple MOS capacitors because of the peculiar etching characteristics of this oxide. The most straightforward fabrication scheme would be to chemically etch the required geometrical patterns in the oxide after its formation. However, upon exposure to hot phosphoric acid (80°C to 180°C), the plasma-grown oxide softens and eventually peels from the substrate. Similar effects are observed upon exposure to buffered *HF*. Hence, direct chemical etching cannot be utilized at the present. Thus, an alternate technique, namely etching of the aluminum film prior to anodization, was developed and refined to allow device fabrication.

COS/MOS processing

The processing of the wafer proceeds in the same manner as for the conventional SiO_2 unit up through step 6 of Fig. 3. At this point, there are two alternative schemes which can be utilized depending on whether the stepped SiO_2 is to be under or over the Al_2O_3 layer.

In the first version, alternative A of Fig. 4, SiO_2 is removed from the active region only, leaving the stepped oxide on the remainder of the wafer. The wafer is then metallized (420Å of aluminum), contact holes are formed in the aluminum film, and anodization of this film is carried out under the conditions listed in Table II.

In the B version, all oxide is removed from the entire wafer. The wafer is then metallized, contact holes are formed in the aluminum film, and the anodization is carried out in the normal manner. Finally, SiO_2 is deposited and then densified at 800°C to 1000°C before the desired stepped-oxide pattern is formed.

In either version, the unit is completed by first removing the oxide formed in the contact holes during the anodization by a 30-second etch in buffered *HF*, followed by an anneal at 350°C for one hour in hydrogen and finally by forming the contact metallization. The units are then electrically probed, and acceptable units are selected from the diced wafer and bonded into 14-lead flatpacks for testing; see Figs. 5 and 6.

Critical process steps

Wafer preparation—The wafer must be free of both particulate contamination and absorbed moisture prior to aluminum metallization since either can result in oxide defects (bubbles, pinholes, etc.) which would cause failure by electrical conduction. The effects of moisture can be largely eliminated by heating the wafer in an inert ambient prior to metallization. Particulate contamination is minimized by careful cleaning immediately before placing the wafer in the vacuum system for metallization.

Table II—Typical plasma anodization parameters.

Pressure	0.3 Torr (oxygen)
V_p (anode to cathode voltage)	800 to 1100 volts
I_p (plasma current)	40 to 60 mA
Aluminum thickness	420Å
Initial sample current	0.3 mA/cm²
Final applied voltage	60 to 70 volts
Total time of anodization	2 to 3 hours
Al_2O_3 thickness	640Å

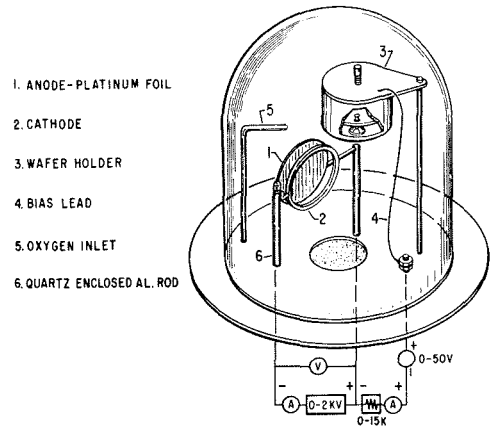

Fig. 1—Plasma anodization chamber.

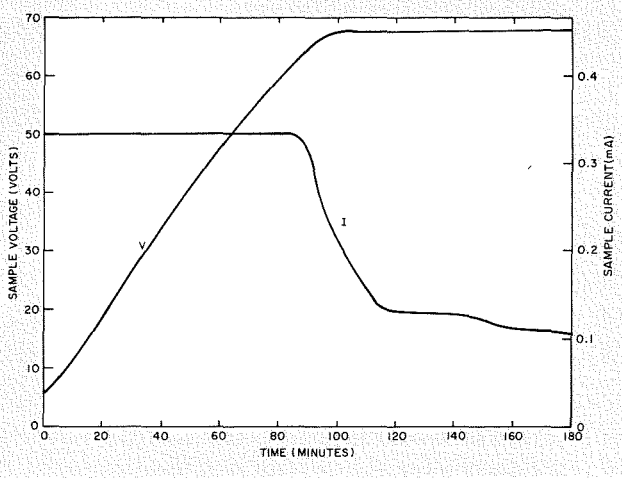

Fig. 2—Variation of sample voltage and current with time during plasma anodization.

Aluminum deposition—Since the oxide thickness is determined by the thickness of the aluminum film, the metallization must be accurately controlled. This can be done quite easily with a quartz crystal monitor. The thickness is normally verified optically by the Tolansky interference technique. This is important since overanodization results in the formation of a thin SiO_2 layer at the silicon interface and in some cases is responsible for the appearance of oxide defects (bubbles or other fine structures).

Measurement of sample voltage—As indicated above, the effective voltage applied to the sample is the supply voltage minus the wall potential. The wall potential is determined not only by the plasma parameters but also by the condition of the anode. During a given anodization, the wall potential increases in magnitude. In some cases, for an anode which has been reused a number of times, the wall potential may vary by as much as 10 volts during an anodization. Hence, the wall potential must be monitored continuously. This is achieved by a plasma probe in conjunction with a high impedance meter such as an electrometer or nulling voltmeter. Errors result if the input impedance of the meter is below 10^9 ohms.

Control of current density—Control of the current density is necessary to obtain high-quality oxide in a reasonable time. If the current density is too high, especially as the growth approaches the silicon interface, oxide defects such as bubbles or fine grainy structure result. On the other hand, if the current density is too low, the anodization proceeds too slowly.

Effects of stepped oxide—When the Al_2O_3 is formed over the stepped oxide (as in version A of Fig. 4), additional care must be taken to ensure that the aluminum is completely anodized over the SiO_2 regions. In version B, the etching of the desired pattern in the SiO_2 overlying the Al_2O_3 must be controlled very accurately since buffered *HF* attacks the Al_2O_3-silicon interface, causing the oxide to peel.

Removal of oxide from contact holes—During the anodization, 50 to 100Å of SiO_2 form in the contact holes. This oxide must be removed by buffered *HF* so that contact can be made to the source and drain regions of the devices. Because the buffered etch attacks the Al_2O_3, photoresist is used to protect the Al_2O_3 during this step.

Electrical properties

Both discrete N-channel units and complementary-symmetry MOS inverters (CD-4007) with plasma grown Al_2O_3 as the gate insulator have been evaluated. In general, a lower yield and a reduction in device quality has been found in comparing the discrete ring-dot units with the individual MOS units on the CD-4007 circuit as summarized in Table III. This is attributed to the greater complexity of the circuit over the discrete ring-dot structure and in particular to difficulties involving the formation of the stepped oxide which was not utilized for the discrete structure.

Typical transfer characteristics for inverter pairs on the CD-4007 chip are shown in Fig. 7 together with the current flowing from the power supply. The schematic for these inverters is shown in the insert to the Figure. The characteristics of the plasma-grown Al_2O_3 units are offset to the right of those of the conventional SiO_2 units due to the large threshold of the N-channel units, and they are somewhat distorted due to contact resis-

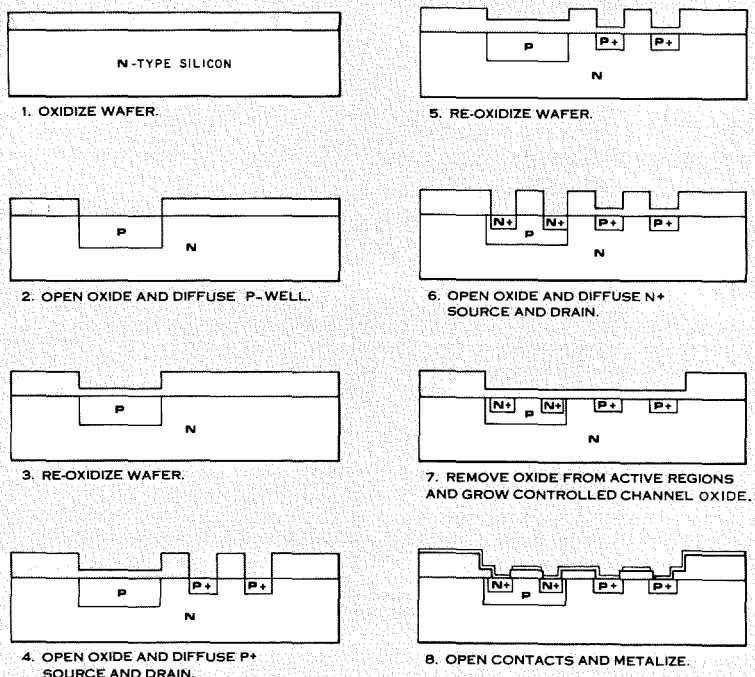

Fig. 3—Major processing steps for complementary MOS integrated circuits with thermally grown SiO_2 channel oxide.

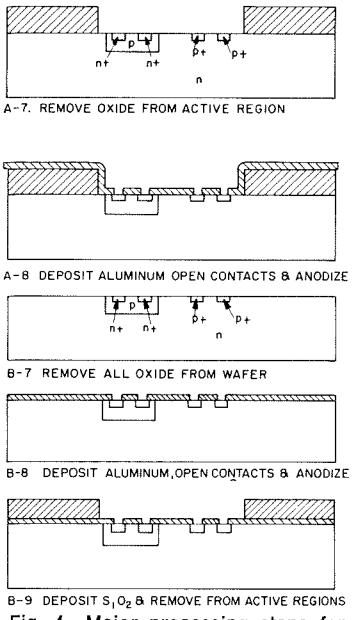

Fig. 4—Major processing steps for utilization of plasma-grown Al_2O_3.

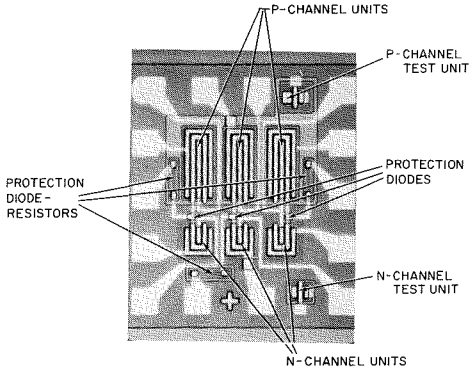

Fig. 5—Topological view of RCA CD-4007 dual complementary pair plus inverter.

tance. On the other hand, there is no appreciable current flow in either steady state condition (V_{in}=0 or +10 volts) as required in most COS/MOS applications. With refinements in the processing, these characteristics should be improved considerably.

Small shifts (~0.5 volts) in these transfer characteristics due to bias temperature stress (150°C, 10 volts, 5 minutes) have been observed. However, these are opposite in direction to shifts caused by positive ion drift and are attributed to interface state effects.

The units with plasma-grown oxide show promise of considerable radiation hardness. All units were bombarded with 1-MeV electrons in the Van de Graaff facility at RCA Laboratories. Fig. 8 shows the net shifts in threshold voltage for the CD-4007 for a +10-volt

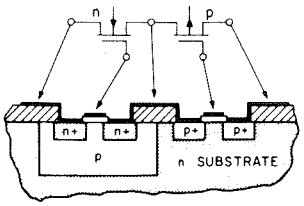

Fig. 6—Cross-section view of COS/MOS inverter showing external connections.

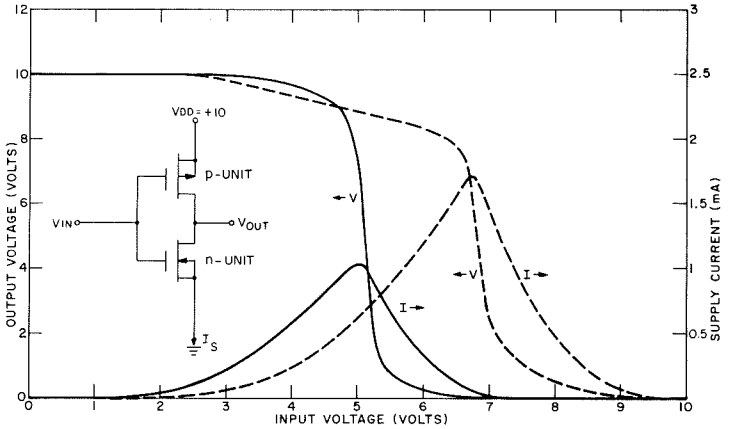

Fig. 7—Typical transfer characteristic of CD-4007 inverter for connection shown in insert: solid curve for conventional SiO_2 unit, dashed curve for unit with plasma-grown Al_2O_3.

input, which is the most severe condition for conventional SiO_2 units. These results, together with tests under other biasing conditions, show that plasma-grown Al_2O_3 offers an increase in radiation hardness by a factor of 50 or more over SiO_2.

Conclusions and recommendations

The results reported in this paper clearly show two major achievements:

1) The first successful fabrication of operating integrated circuits using Al_2O_3 as gate insulator, thus proving the feasibility of an Al_2O_3-MOS technology.
2) The first demonstration that the degree of radiation hardening, expected from MOS-capacitor data, has been achieved in active device structures and integrated circuits.

Considerable work remains to be done, especially in the areas of geometrical pattern definition, optimization of oxide properties and formation techniques, and active device fabrication. Once these difficulties have been eliminated, and statistically significant results have been obtained, there will be enough confidence in the Al_2O_3 technology that it can be transferred into an experimental line for fabrication of integrated circuits. This can then lead to a radiation-resistant technology for integrated-circuit capability.

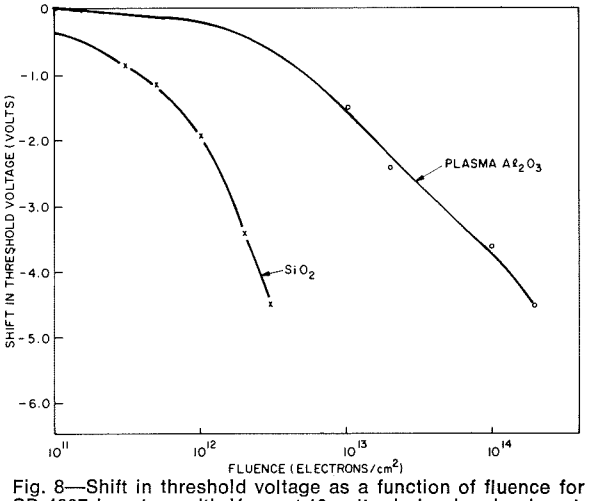

Fig. 8—Shift in threshold voltage as a function of fluence for CD-4007 inverters with V_{in} = +10 volts during bombardment.

Acknowledgments

The authors would like to acknowledge the assistance of C. Benyon, J. Groppe, G. Mark, and J. Shaw for fabrication of the devices; D. Flatley and W. French for provision of the CD-4007 substrates with diffusions and F. Kolondra for radiation testing of the completed devices.

Table III—Comparison of discrete MOS characteristics on CD-4007 and ring-dot test units.

Unit		Threshold (volts)	Field-effect mobility (cm^2/V-sec)
CD-4007	plasma Al_2O_3 N-channel unit	+4.0±0.5	23
	640Å P-channel unit	−2.0±0.5	46
CD-4007	SiO_2 N-channel unit	2.0±0.5	102
	1000Å P-channel unit	−1.5±0.5	144
Ring-dot	plasma Al_2O_3 N-channel unit	1.5±0.5	150

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Vapor deposited tungsten as a metallization and interconnection material for silicon devices

J. M. Shaw | Dr. J. A. Amick

A procedure for metallizing and interconnecting silicon devices and integrated circuits with tungsten is described. For this purpose, a chemical vapor deposition technique involving reduction of tungsten hexafluoride is employed. Advantages of tungsten metallization and high temperature properties of tungsten-to-silicon contacts are discussed.

ALUMINUM is the most widely used material for the metallization of silicon devices. It has the advantages of high conductivity and excellent adhesion to silicon and to silicon dioxide. It also forms low-resistance ohmic contacts to P-type and heavily doped N-type silicon. It is easily deposited by evaporation techniques and can readily be defined into high resolution patterns. However, aluminum has several disadvantages:

1) Because of the low melting point of the aluminum-silicon eutectic (577°C) and because of rapid diffusion of aluminum along grain boundaries, metallized devices cannot be heated safely above about 525°C.
2) Aluminum metallization exhibits certain types of failure under electrical stress, in part because of its low activation energy for self diffusion.[1] For certain power devices, this limitation, and item 1) above, are undesirable.
3) Aluminum metallization is not satisfactory when exposed to air during operation of a device since it corrodes.
4) Successful multilevel metallization of integrated circuits with aluminum requires exceptionally precise control of the processing sequence to avoid high resistance aluminum—aluminum contacts and undercutting of aluminum feed throughs.

To overcome these disadvantages, a number of metallization systems have been suggested. Perhaps the most successful of these is the platinum silicide/titanium/platinum/gold metallization used with beam-lead devices.[2] This metallization system has particular advantages for preparing hermetically sealed chips that must withstand corrosive attack by atmospheric constituents. However, the number of materials involved and the added processing steps required make the metallization system rather expensive. Molybdenum/gold metallization has been suggested,[3] but the processing equipment is again expensive and inconvenient to use. Nickel is employed for a number of large-area power devices where adhesion to oxide layers is not required but it is not generally satisfactory for integrated circuits or for small-geometry devices.

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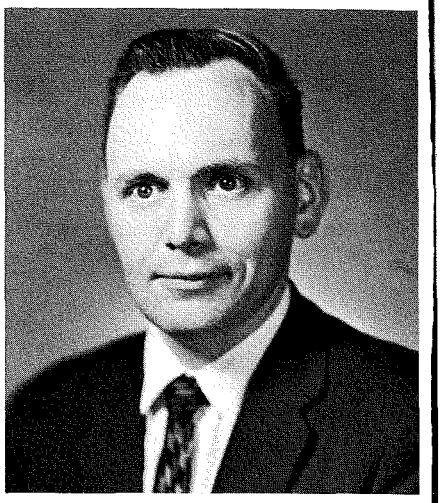
Advantages of tungsten

Tungsten offers a number of advantages as a contact-metallization and intraconnection material for silicon devices and integrated circuits (see Table I). With respect to thermal coefficient of expansion, silicon is more closely matched by tungsten than by any other elemental metal. Tungsten contacts to heavily doped N- and P-type silicon are ohmic, and its resistivity is only about 2½ times that of aluminum. It adheres well to silicon and to silicon dioxide and can readily be defined into high resolution patterns. It is hard, not easily scratched and is not attacked readily by aqueous HF nor by atmospheric constituents. The lowest melting point in the binary system tungsten-silicon is 1410°C. Tungsten does not diffuse readily into silicon, and its activation energy for self diffusion is one of the highest known for metals. For these reasons, it is especially suitable for power devices and for multilevel metallization applications. We have therefore investigated tungsten as a metallization material for silicon devices and integrated circuits.



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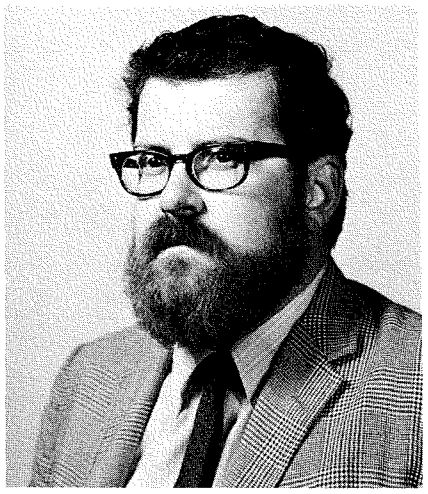
Deposition of tungsten films

Tungsten is readily deposited on silicon device wafers by chemical vapor deposition from tungsten hexafluoride. The adhesion of the films is excellent if a suitable processing sequence is employed. The deposition procedure and devices prepared by this method will be described in this paper.

Tungsten hexafluoride was chosen as the source for tungsten because it is gaseous at room temperature (bp. 17.3°C) making its handling easy. It is readily available in high purity at low cost and in large quantities. Furthermore, no lower-valence fluorides are known.[4] On reduction, the hexafluor-



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ide is reduced smoothly to the metal. Tungsten hexafluoride reacts with silicon, on contact, at temperatures above about 400°C according to the following equation.

$$2WF_6+3Si\rightarrow 3SiF_4\uparrow+2W$$

This reaction has been employed by Crowell, Sarace, and Sze[5] to form Schottky barrier diodes to silicon. If the silicon is sufficiently heavily doped, ohmic contacts can be made to either P- or N-type material. For this purpose, resistivities below about 0.1 ohm-cm P-type, and below about 0.01 ohm-cm N-type have ben found satisfactory—the more heavily doped, the better.

If tungsten hexafluoride is allowed to contact silicon dioxide at this temperature, the surface of the oxide is attacked chemically. If the hexafluoride is sufficiently dilute, the surface becomes almost imperceptibly textured, and tungsten films subsequently deposited on such a surface adhere very strongly. The texture of the surface cannot be seen by the naked eye but is visible if a finely focussed light beam is allowed to impinge on the surface and the surface is viewed at an angle so that the scattered light can be seen. Under these conditions, a very slight haziness can be observed that is not present in the unetched oxide surface.

When a silicon device wafer, opened and ready for metallization, is exposed to dilute tungsten hexafluoride at about 700°C, the silicon regions quickly and selectively become coated with tungsten. In addition, the oxide regions will be slightly etched. This mild vapor etching helps to remove any thin oxide layers over the silicon regions, cleans the oxide surface, and ensures that tungsten films (subsequently deposited on the oxide) will adhere. To minimize undercutting at the edges of openings, a chemically-vapor-deposited silicon-dioxide layer[6] covering the entire wafer can be employed. The surface of this oxide layer is lightly etched with tungsten hexafluoride as the first step in the metallization. The oxide is then patterned with photoresist and contact areas are opened through the oxide. The silicon regions are subsequently metallized with tungsten by contact reduction.

In the presence of hydrogen, tungsten hexafluoride is reduced to metallic tungsten at temperatures in the neighborhood of 700°C according to the following reaction:

$$WF_6+3H_2\rightarrow W+6HF\uparrow$$

By means of this reaction, tungsten films can be deposited uniformly both on oxide and on (tungsten metallized) silicon regions. In our work, these two types of reaction—contact reduction and hydrogen reduction—are used in sequence.

The apparatus employed for this work is shown in Fig. 1 and consists of a simple fused-quartz deposition chamber silimar to that employed for the epitaxial growth of silicon. The substrate is placed on a silicon-carbide-coated carbon susceptor that has a thermocouple inserted through one end. This thermocouple controls the output of an RF generator to give a constant temperature in the block. A wafer is cleaned, then placed on the susceptor, and inserted into the deposition chamber. The thermocouple is inserted, and the reaction chamber is closed. After purging the chamber for a few minutes with argon flowing at about 7 liters/min., the substrates are brought to 700°C. At this point, a few cc/min. of tungsten hexafluoride are introduced for a period of a few seconds. The change in the appearance of the substrate wafer resulting from this step is clearly visible. The silicon regions become more metallic, and the oxide thickness decreases slightly as indicated by a change in the interference color. The tungsten hexafluoride is purged from the system and the argon is replaced by hydrogen flowing at about 10 liters/min. Gaseous tungsten hexafluoride is next introduced into the reactor, a few cc at a time, and deposition takes place on the heated susceptor and the substrate. When the

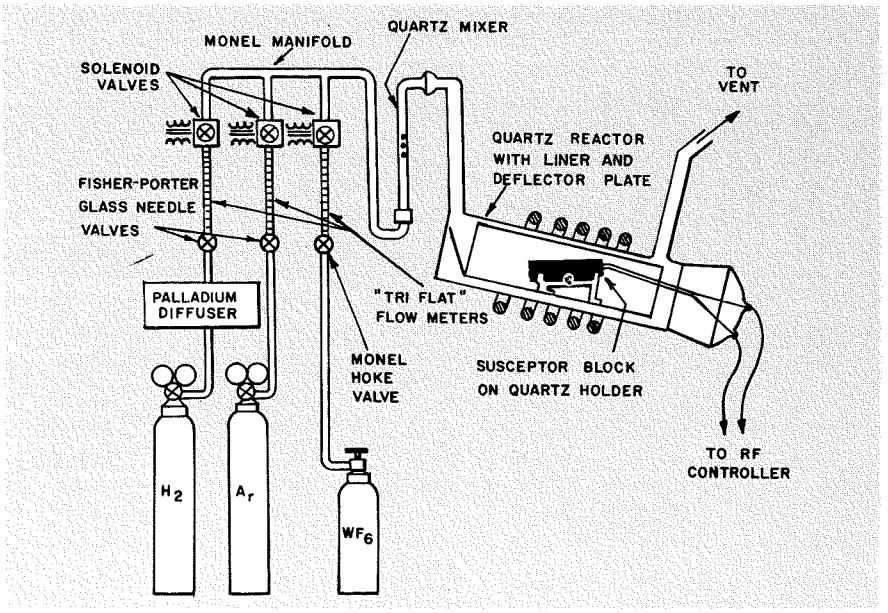

Fig. 1—Apparatus for deposition of tungsten layers from tungsten hexafluoride.

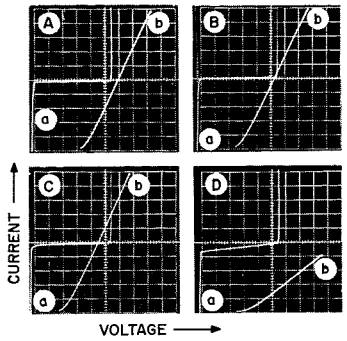

Fig. 2—Forward and reverse bias characteristics of emitter-base junction in an experimental tungsten metallized transistor before and after heat treatment: A) initial characteristics; B) after treatment at 800°C. in *Ar* for 12 min. in closed system; C) after treatment at 900 to 950°C. for 20 min. in *Ar* in closed system; D) after treatment at 850°C. in *Ar* for 20 min. in open tube furnace uncapped at open end. The a) curves are reverse bias: 0.5 A/div and 1.0 V/div; the b) curves are forward bias: 100 mA/div and 0.2 V/div. The emitter junction is about 1.5 microns deep.

desired thickness of tungsten has been deposited, the tungsten hexafluoride flow is terminated and the substrate and susceptor are allowed to cool to room temperature in hydrogen. At this point, the hydrogen is replaced by argon, and a few minutes later, the substrate is removed from the reaction chamber.

Characterization of tungsten layers

For tungsten layers up to about 0.5 μm in thickness, the surface is specular, corresponding to that of the substrate. At thicknesses of about 1 μm or more, the surface becomes slightly matte but is still very smooth. Thicknesses up to 5 μm have been deposited on silicon device wafers with no indication of cracking or separation of the tungsten from the substrate wafer.

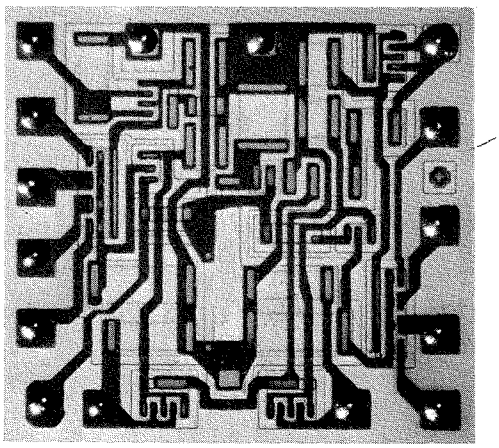

Fig. 3—Tungsten metallized, silicon nitride sealed IC chip with solder bumps.

Table I—Characteristics of various metals used for metallization and interconnection.

Metal	*Temp. Range (°C)*	*Linear coefficient† of thermal expansion* $\left(\frac{\Delta l}{l} \circ C^{-1}\right)$	*Melting point (°C)*	*Bulk resistivity at 20°C (ohm-cm)*	*Melting point of eutectic silicon‡*
Al	0 to 600	28.7 22.5×10^{-6}/°C	600	2.26×10^{-6}	577.2
Pt	−150 to 600	8.8×10^{-6}	1755	10.5×10^{-6}	830°C
Ni	0 to 550	15.7×10^{-6}	1452	6.9×10^{-6}	964
W	25 to 500	4.6 4.46×10^{-6}	3370	5.5×10^{-6}	1400
Mo	25 to 500	5.5	2620	4.8×10^{-6}	~1400
Si	0 to 50 25 to 600	4.15×10^{-6} 3.6×10^{-6}*	1430		

†Source: Research Triangle Inst., Durham, N.C.
Integrated Silicon Device Technology
Volume V Physical-Electrical Properties of Si, (July 1964)
‡Hausen, M. *Constitution of Binary Alloys* (Second Edition, McGraw-Hill, New York, 1968).
*From Wang, C. C., *private communication.*

The deposited tungsten films have a resistivity of 6×10^{-6} ohm-cm ±10%, the same as that of bulk tungsten within the error of measurement. Since this resistivity is about 2.5 times that of bulk aluminum, the thickness of tungsten required for a given device will be somewhat higher than that required with aluminum metallization. In practice, however, the sheet resistivity of evaporated aluminum films rarely equals the bulk value. Tungsten films having a thickness of about 1 μm have been found satisfactory for a variety of experimental devices.

Vapor-deposited tungsten films are hard, brittle, and very adherent. Probe tips can be run across the pattern layers with no gouging out of metal. The only evidence of probing is a slight burnishing of the surface. Patterns can readily be formed in the layers by electro-etching combined with chemical etching in alkaline ferricyanide.

Tungsten contacts to heavily doped silicon are ohmic and unaffected by heat treatment in neutral or reducing atmosphere at temperatures up to 900°C for a few minutes. Typical forward and reverse characteristics for the emitter-base junction of an experimental tungsten metallized transistor are shown in Fig. 2, both prior to, and subsequent to, heat treatment. These devices, having emitter-base junction depths of about 1.5 μm, were heated in argon at temperatures ranging up to 900°C for periods up to 20 minutes with no perceptible increase in the forward resistance, nor any degradation of the reverse characteristics of the junction.

If the hot metallized wafer is exposed to air, the tungsten will oxidize and the forward resistance of a transistor will increase greatly (Fig. 2D). Care must be taken to ensure that the tungsten is cooled to below 300°C before it is exposed to an oxidizing ambient. However, if the tungsten metallization is sealed beneath a layer of silicon nitride or silicon dioxide, oxidation of the metal can be prevented and the metallized units can then be heated in air with no deleterious effects. Because of the high-temperature properties of the tungsten silicon contact, temperatures of 850°C. or higher can be employed for the deposition of silicon nitride. Alternatively, vapor deposited silicon-dioxide layers can be densified in neutral atmosphere at high temperature if desired.

Tungsten itself is not readily bonded and is not wet by solder. A suitable layer of an interface metal is therefore needed to permit interconnections to external circuitry to be made. Metals such as nickel, platinum, copper, gold, aluminum, and other materials can be deposited by a variety of methods at appropriate stages in the processing, depending on the termination desired. An example of a device formed with solder bumps is shown in Fig. 3, while a device having wire bonds is shown in Fig. 4.

The adhesion of the deposited tungsten to the silicon dioxide present on device wafers was evaluated using an Instron. For this purpose, a sputtered platinum layer was first deposited on the tungsten and then selectively desputtered to leave 0.005-inch Pt dots on approximately 0.005-inch-square tungsten pads. Thermocompression (nail head) bonds were formed with 0.002-inch and 0.005-inch *Au* wires. Vertical pull measurements showed bond strengths typically between 8000 and 25,000 lb-f/in^2 (or approx. 60-180g on a 0.005-inch pad). Failure oc-

curred in the gold wire, at the SiO_2-Si interface or in the Si itself.

Extensive temperature cycling tests have not been carried out, but no failures have been observed for glassed, tungsten-metallized integrated-circuit chips cycled five times rapidly from dry-ice acetone slurry (−60°C) to molten lead at 350°C.

Tungsten metallized devices

Both discrete transistors and integrated circuits of the dual 4-input emitter-coupled logic type have been tungsten metallized and DC probed. Following pattern etching of the tungsten, yields comparable to those for aluminum metallized factory products were obtained. The circuits were subsequently coated with a 1500Å silicon nitride layer at 850°C. Next, openings through the nitride—in the contact pad regions only—were formed by conventional silicon dioxide masking[6] and photolithographic processing.[7] Tungsten is attacked only very slowly by hot phosphoric acid and the etching time is not critical. Repeat DC wafer probing at this point showed that no degradation of the electrical characteristics resulted from this processing sequence. A number of these devices, platinum metallized in the contact pad region only, were mounted in flat packs and bonded ultrasonically with aluminum wires. The devices then underwent final testing and yields were found to be comparable to those for aluminum-metallized factory products. Finally, pull measurements were made on the bonded chips. It was observed that the failure mechanism was the pulling apart of the aluminum wire at an applied force of 6 grams, the same as observed for aluminum metallized product.

It has also been observed that, under conditions leading to rapid aluminum "swelling" for conventionally metallized devices, the tungsten-metallized units have not failed even after the conclusion of several hundred hours of testing.

Multilayer metallization with tungsten

Tungsten has a number of advantages for the preparation of multi-level metallization. Crossover test arrays have been constructed using tungsten for the upper and lower metallization with vapor deposited silicon dioxide densified at 800°C for 10 minutes in Ar serving as the insulator. Appropriate contact holes are etched through the oxide layer down to the tungsten surface. Since tungsten is inert to HF containing etchants, this step is noncritical. A second tungsten layer is then vapor deposited and suitably patterned. Examination of these crossovers showed that no high resistance contacts were encountered (Fig. 5). This is probably attributable to the etching action of tungsten hexafluoride on any thin silicon-oxide layer residues, and to the fact that tungsten oxides are reduced to the metal at the deposition temperature employed. Shorting, or low voltage breakdown through the densified insulator, has not been observed. This is perhaps partly because recrystallization of the first tungsten metal layer does not occur at the processing temperatures employed. Consequently, there are no "hillocks" present on the surface to puncture the dielectric layer.

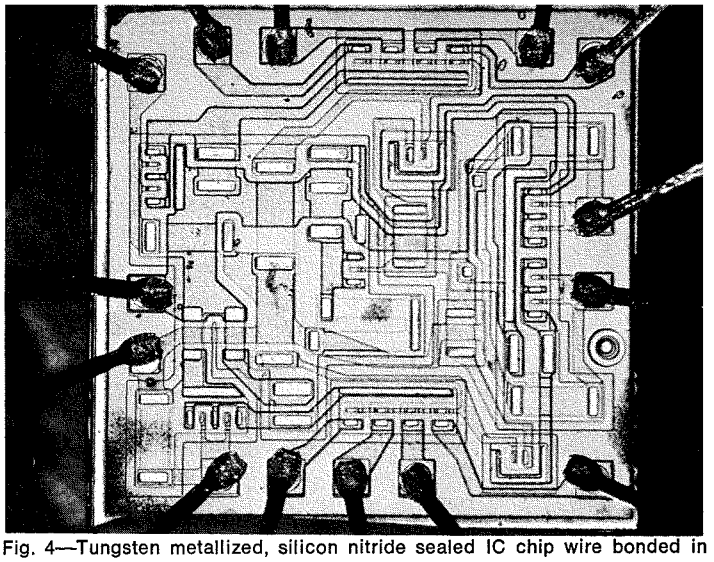

Fig. 4—Tungsten metallized, silicon nitride sealed IC chip wire bonded in ceramic flatpack.

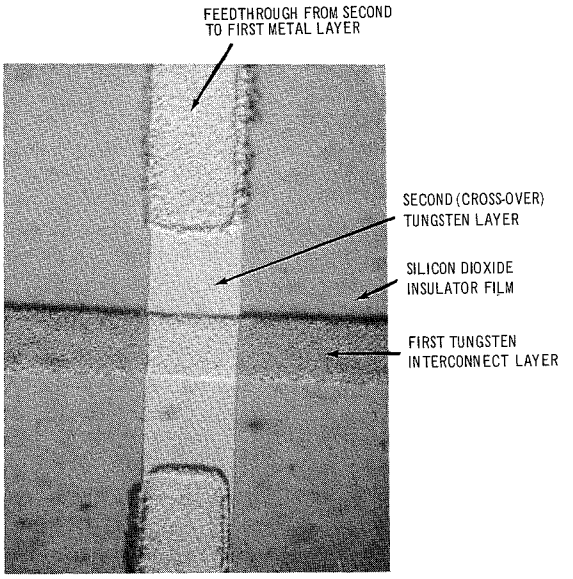

Fig. 5—Element in cross-over pattern prepared using tungsten and vapor deposited SiO_2.

Conclusions

For the metallization of silicon devices, tungsten has a number of advantages. It permits the fabrication of transistors and integrated circuits that can be passivated at high temperature. In such circuits, the passivating layer covers the metallization pattern as well as the active areas of the device or circuit. Openings need then be made only in the contact pad regions, away from sensitive junctions. Tungsten to heavily-doped-silicon contacts are ohmic and they are not degraded by heat treatment.

Acknowledgement

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New technique for etch-thinning silicon wafers

A. I. Stoller | Dr. R. F. Speers | S. Opresko

A novel technique for chemically thinning silicon wafers is described. Gas bubbles, rising from the bottom of the etching vessel, impinge on a float-mounted wafer in a random manner. When wafers are thinned with the apparatus and etch described, wafers having smooth, blemish-free surfaces, and a thickness uniformity of ±0.1 mil, are obtained. A means of observing the light transmission through the wafer without removing it from the etch is also provided. This enables the end-point to be determined simply and accurately when wafers are being thinned to less than 1 mil.

To FABRICATE certain semiconductor arrays, it is necessary that silicon wafers be uniformly thinned from a normal wafer thickness (5 to 10 mils) to 1 mil or less. Examples of such arrays are dielectrically isolated structures[1-4] and image sensor arrays.[5]

Normally, an isotropic acid etch *(HF-HNO_3)* is used for this purpose. However, during the etching, bubbles of gaseous reaction products, such as NO_2, form on, and cling to the surface, leading to nonuniform etching. To dislodge the bubbles, various agitation methods such as a rotating breaker, have been used, but it is difficult to provide agitation while controlling the flow pattern to give a uniform reduction in thickness over the entire wafer.

Described here is an etching apparatus and procedure which overcomes this problem by providing a completely random agitation, resulting in uniformly thinned blemish-free wafers when used with the isotropic etch developed for this purpose.

Apparatus

The apparatus consists of a Teflon cylinder closed at the bottom and having a Teflon screen rigidly mounted just above the bottom. A suitable gas is bubbled up through the etching solution from beneath this screen, providing random agitation of the solution. The wafer to be etched is waxed to the bottom of a Teflon cup, so that it floats just beneath the surface and the rising bubbles impinge upon it. The wafer holder bobs about randomly during etching.

Another feature of this apparatus is a protruding overhang on the etching chamber where the light transmission of the wafer can be observed so that the end point of the etching can be determined without removing the wafer from the etchant. Figs. 1 and 2 show a cross-sectional drawing and a photograph of this apparatus.

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Etchant

Initially, the etching solution used with this apparatus was a mixture of 7% by volume of 48% HF and 93% by volume of 70% HNO_3, with N_2 as the agitating gas. This combination produced wafers that were uniform in thickness, but whose surfaces were often quite rough. Fig. 3a shows a photomicrograph of a typical wafer after etching with the HF-HNO_3-N_2 systems.

At first, the agitating gas was thought to be chemically passive. However, further experimentation with several gases and gas mixtures indicated that certain gases did lead to better surface characteristics for the etched wafer. Specifically CO_2, CO and NO yielded the most blemish-free surfaces, while N_2, O_2, NO_2, and Ar gave varying degrees of surface inhomogeneity, implying that the gas agitant can play a chemical, as well as physical role in the etching process.

With the apparatus described above, an etch solution has been devised that produces smooth, chemically polished surfaces (see Fig. 3b). The composition of the preferred etch solution is:

70% Nitric Acid	90 ml
48% Hydrofluoric Acid	9.5 ml
Glacial Acetic Acid	0.5 ml
Sodium Chlorite, $NaClO_2$	1.4 grams
Carbon Dioxide	bubbled through the solution at 0.5 liter/minute

Although it was found that $NaNO_2$ could be substituted for the $NaClO_2$, the $NaClO_2$ is preferred. The $NaNO_2$ imparts a reddish-brown color to the solution and liberates reddish-brown N_2O_4 gas, making it difficult to observe the light transmission of the wafers. With $NaClO_2$ the solution is a pale greenish yellow that does not obscure the light transmitted by the thinned silicon wafer.

The acetic acid was also found to be necessary in order to obtain blemish-free surfaces. However, if amounts larger than 1.0 ml were used in the preferred etch composition, a passivation layer formed which interfered with the etching. Such passivation layers have been previously reported[6] and identified as a fluorosilicate composition.

Procedure

The three acids are mixed together in the Teflon chamber, and the CO_2 gas is turned on. The solid sodium chlorite is added *slowly and carefully,* since considerable frothing takes place when it is added. When the frothing has subsided, the wafer, mounted on the float, is placed in the etch. The etch rate, about 0.6 mil/minute, has been found to be essentially independent of the wafer orientation and resistivity. The end point of the etching may be determined by timing if the wafer and mounting are not translucent. If, however, the silicon wafer is being thinned to less than 1 mil and the mounting is transparent, the end point may be determined by periodically moving the float into the illuminated,

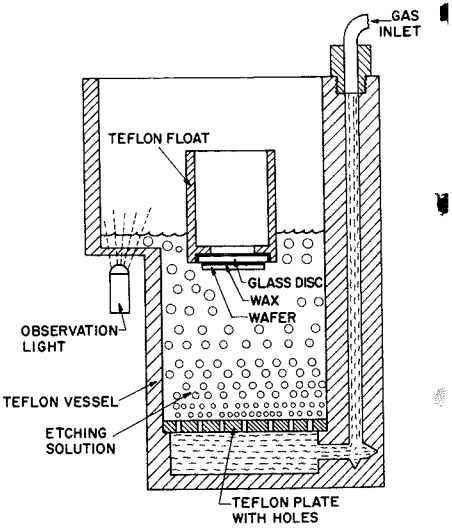

Fig. 1—Cross-section of etching chamber.

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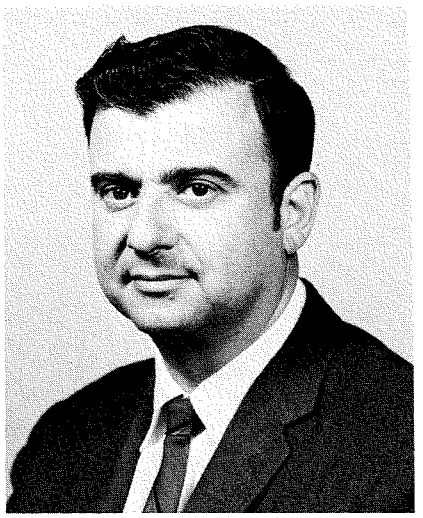

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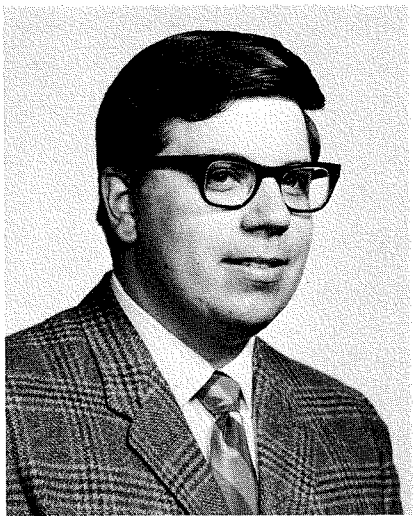

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overhang of the etching chamber and observing the color of the transmitted light. Due to the relatively gradual increase of the absorption coefficient with an increase of the photon energy for silicon[7], the transmitted light changes in hue as the silicon wafer is thinned. With a 28-watt microscope light for illumination, the transmitted color ranges from crimson red for 0.9-1.0 mil-thick wafers, to orange-red for 0.65-mil wafers, to yellow for 0.4-mil (and under) wafers. With some practice, it has been possible to stop the etching reproducibly to a tolerance of ±0.1 mil.

In this way, a thin wafer can be obtained without removing it from the etchant before completion. Such premature removal often leads to "stain films" and poor surface quality. When the etching is completed, the wafer is immediately flushed in distilled water and removed from the float.

It is important that the mounting wax be resistant to attack by the etching solution, otherwise the decomposed wax deposits on the wafer during etching, thereby degrading the surface. A pure paraffin wax (Bareco Be Square 190/195 #1 white wax from the Bareco Division, Petrolite Corp., Ardmore, Pa.) has been found satisfactory.

Evaluation

An evaluation of the uniformity of etching was obtained by measuring silicon wafers with a Proficorder [A product of the Bendix Corp.] along the same path, before and after etching. The wafers were (100) orientation, 20 mils thick, 1.4 inches in diameter, 3 ohm-cm N-type, Czochralski-grown material, one side lapped, the other polished. One wafer was etched on the polished surface, and another on the lapped surface. Etching times of 10 minutes were used to remove approximately 6 mils of silicon. Representative results of the Proficorder recordings before and after etching are shown in Figs. 4a and 4b.

The etched surfaces of the wafers were observed to be flat and specular with a short range nonuniformity of 10 to 20 microinches, independent of the surface finish of the starting wafer. The long range deviation in wafer thickness is typically ±0.1 mil from the original thickness. For the fabrication of a variety of semiconductor arrays, such as dielectrically isolated structures, this is satisfactory.

Conclusions

An apparatus and an etchant have been developed for the uniform chemical thinning of silicon wafers. The approach involves the use of gas bubbles impinging on the surface during etching to ensure a continuous supply

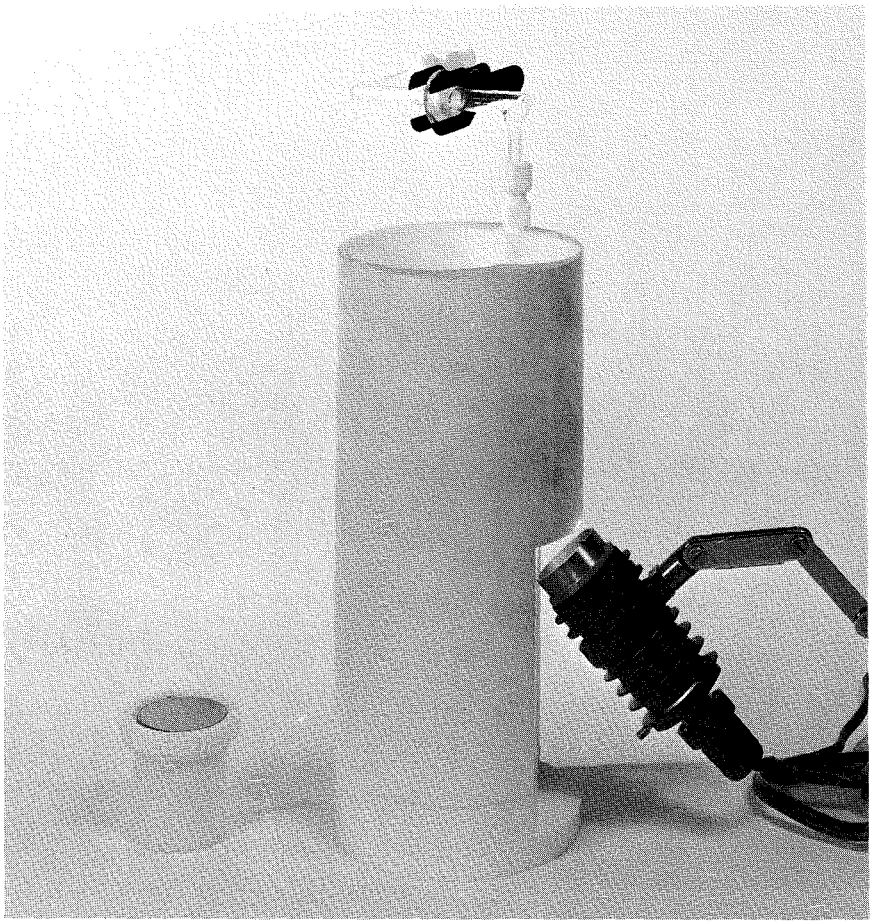
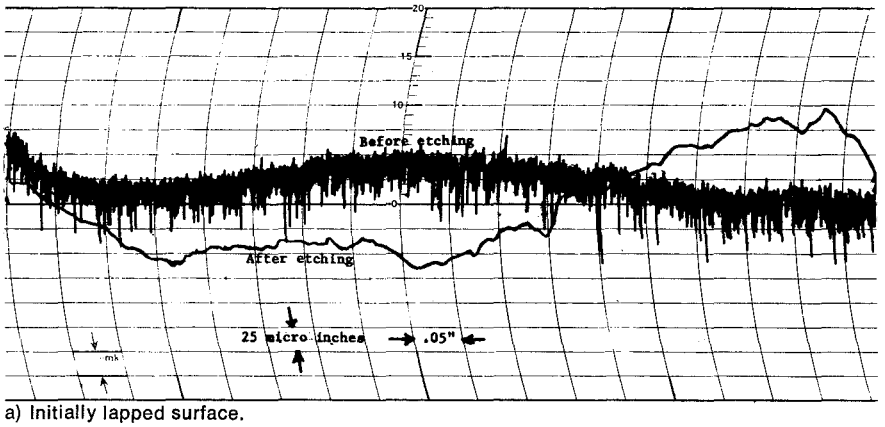
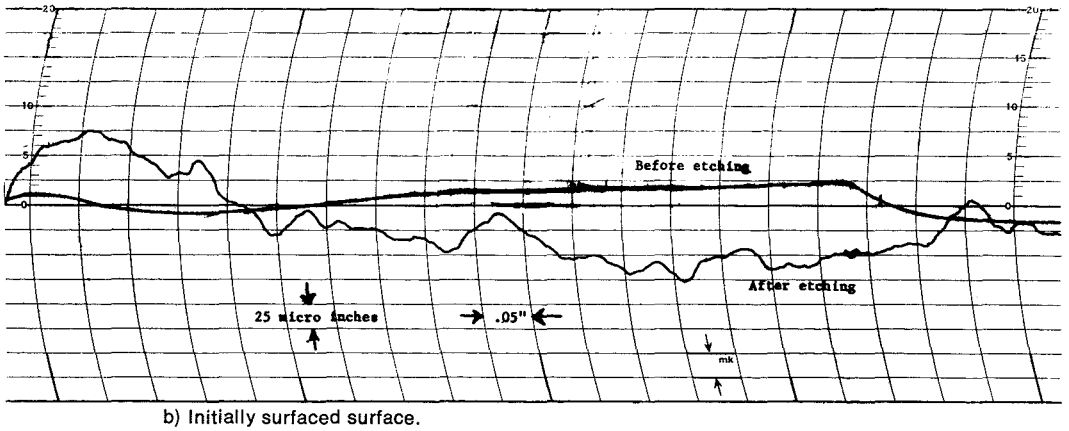


Fig. 2—Etching chamber.



a) Initially lapped surface.



b) Initially surfaced surface.

Fig. 4—Proticorder graphs of surface roughness of a silicon wafer before and after etching.

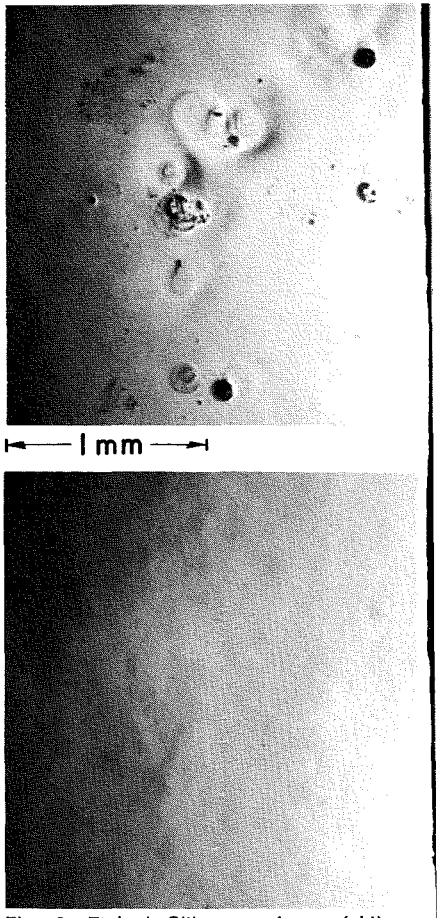


Fig. 3—Etched Silicon surfaces (oblique, lighting): a)—top left—etched with *HF-HNO₃* using *N₂* bubbles; b)—bottom right—etched with preferred etch using *CO₂* bubbles.

of fresh etchant and the continuous removal of reaction products. For silicon, a special etch has been devised to obtain defect-free surfaces. Silicon wafers, 1¼ inches in diameter, can readily be thinned by 6 mils, while introducing less than 0.1 mil nonuniformity. When thinning silicon wafers to less than 1 mil, visual determination of the end point to a tolerance of about 0.1 mil is obtained.

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An IC stereo preamplifier

M. B. Knight

The RCA-CA3052 monolithic integrated-circuit amplifier is an efficient high-gain, low-noise circuit designed specifically for stereo preamplifier use. The complete circuit consists of four amplifier segments, two cascaded in each channel, in a 16-lead dual-in-line plastic package. This paper describes the basic amplifier characteristics of the CA3052, especially as related to the demands of stereo-tape preamplifier applications.

THE DIVISION of each channel of the CA3052 into two amplifier segments permits insertion of gain control, tone control, or equalization at a signal level compatible with good signal-to-noise ratio and wide dynamic range in an amplifier having large overall gain. In a typical system design, the signal from a tape head is inserted directly into an input; the output of that segment is applied through a frequency-response equalizing network of either the passive or the feedback type to the volume control; the resultant attenuated signal is applied to the cascaded output-amplifier segment; and, if tone controls that attenuate the reference signal level are desired, the output-amplifier segment is used for feedback tone control or as the driver of passive tone controls.

Basic amplifier

Fig. 1 is a simplified schematic of one amplifier segment of the CA3052. The differential amplifier, Q_{20} and Q_{21}, has a single-ended output to an emitter-follower, Q_{14}, that drives the base of an output amplifier, Q_{17}. Direct coupled feedback is provided from the output amplifier to the inverting input of the differential amplifier. Alternatively, Q_{20} may be considered as a conventional amplifier that has feedback applied to the emitter circuit through an emitter-follower, Q_{21}. From either viewpoint, the base of Q_{20} is a DC reference point to which the base voltage of Q_{21} is compared and maintained at nearly the same value by the feedback circuit. The feedback circuit also sets the collector voltage of Q_{17} at a desirable value (approximately half the collector supply voltage) by proper choice of the ratio of R_{42} to R_{46}. The design values are selected so that Q_{20} supplies most of the voltage gain; Q_{17} serves as a stable, low-distortion output stage with a voltage gain (about 5) determined by the ratio of the collector and emitter resistors. Because of the internal feedback, however, the overall gain is very low unless the impedance between the base of Q_{21} and ground is reduced. An external bypass capacitor, C_f, and series resistor, R_f, establish the degree of AC feedback desired.

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Contrary to usual differential amplifier design practice, transistors Q_{20} and Q_{21} are operated with unequal currents; balance is not necessary because neither differential input nor differential output is used. With a fixed value of collector current in Q_{20}, the gain is maximum when the current in Q_{21} is made large compared to that in Q_{20}. The collector current of Q_{20} is determined in the operating circuit by the feedback system, which sets the collector voltage of Q_{20}. Therefore, the current in Q_{20} is primarily a function of the value of R_{29}. For minimum noise, the value of collector current should suit the source impedance and the desired frequency equalization in conjunction with the "$1/f$ noise" characteristics of the transistor. The proper current value for typical tape-head impedances and equalization, however, would require a resistance value for R_{29} excessively large for integrated circuits. For this reason, an emitter-follower input is added to increase the input impedance, and to match the source impedance to the differential-amplifier transistors for low noise (Fig. 2). The bleeding of some current through the emitter-follower Q_{19} by way of R_{45} optimizes operating currents for the source impedance and frequency response of a typical tape preamplifier. Although the value of R_{45} is not critical, tests showed that addition of this component improved signal-to-noise ratio by 12 dB. Fig. 2 shows some further refinements of the basic amplifier. The reference bias for Q_{20} is provided by a temperature-compensated bleeder from the collector supply; this allows flexibility in the choice of the collector supply voltage, despite some sensitivity to imperfections in power-supply filtering which would not be a problem with a fixed reference voltage. Transistor Q_{13} is used primarily to shift the DC level at the collector of Q_{20}. The reason for connecting the collectors of Q_{13} and Q_{14} to a tap on the collector resistor of Q_{17} may not be apparent at first glance. If the collectors were connected directly to the Q_{17} collector, the output swing of Q_{17} would be restricted by the sum of the base-to-emitter voltages of Q_{17} and Q_{14}. On the other hand, if the collectors were connected directly to the supply voltage, a large-signal inversion and latching problem would occur. As the instantaneous driving signal to Q_{17}

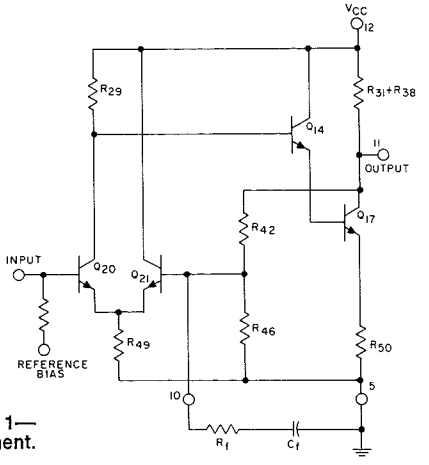
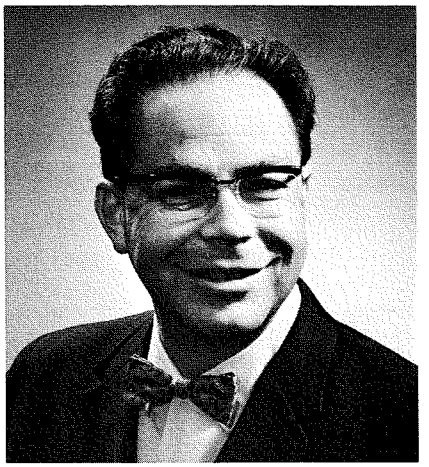


Fig. 1—
One CA3052 amplifier segment.



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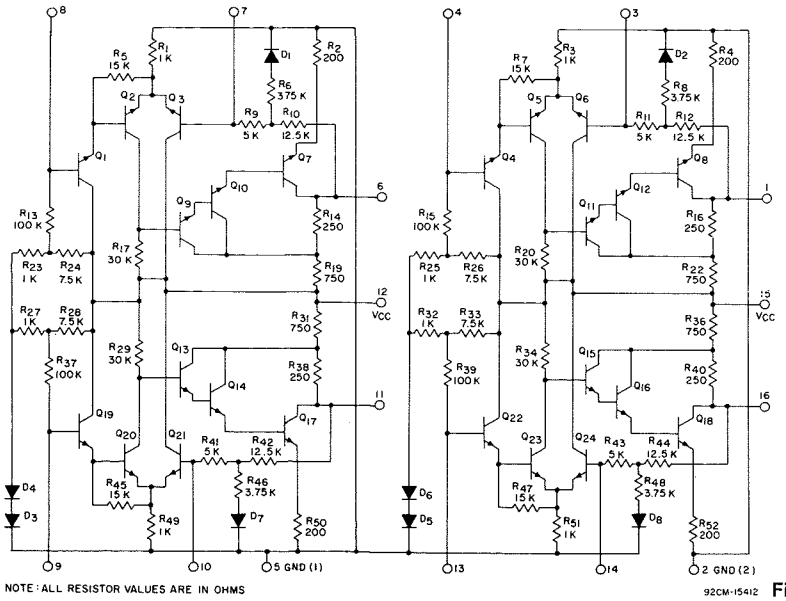

Fig. 2 (left)—Complete schematic diagram of CA3052.

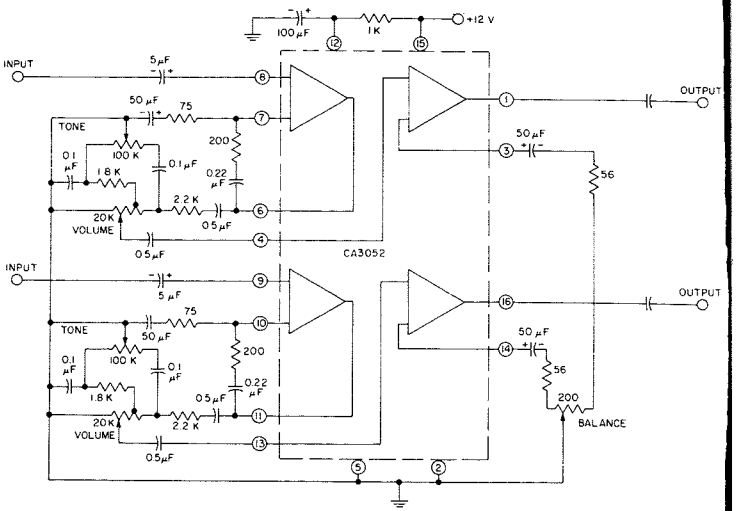

Fig. 3 (above)—Complete preamplifier for 8-track stereo tape player showing discrete components used with CA3052.

swings in the positive direction, the emitter current could be forced to increase even after the Q_{17} collector current became saturated. Because the emitter-to-ground voltage would continue to increase due to excess positive drive, the saturated collector voltage would reverse its normal direction of change, and the feedback circuit would then provide even more drive. Moreover, when the instantaneous collector-to-ground voltage reached the normal DC output voltage, the circuit would latch at this level and the amplifier would be inoperative until the voltage was removed and restored.

The feedback bleeder R_{42} and R_{46} is temperature-compensated by diode D_7, and its high resistance is further increased by R_{41} so that modest values of bypass capacitance (C_f in Fig. 1) are practical. This choice, however, represents some compromise. Because the feedback resistor (R_f in Fig. 1) is a source of noise, an improvement of as much as 3 dB in signal-to-noise ratio can sometimes be obtained by use of external components to reduce the impedance of the feedback network.

In the complete CA3052 stereo preamplifier, the circuit described above is repeated in quadruplicate on a silicon pellet approximately 0.07 inch square. Twelve terminals are provided for input, output, and feedback (inverting input) connections. Two ground and two supply-voltage terminals are provided to permit the isolation and decoupling that may be required for stable operation of the cascaded amplifiers.

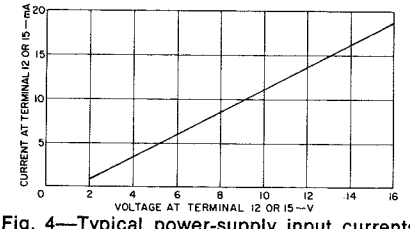

Fig. 4—Typical power-supply input currents as a function of voltages applied.

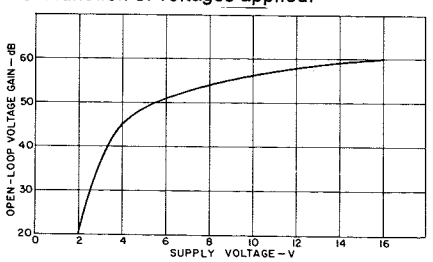

Fig. 5—Typical open-loop voltage gain (feedback resistor R_f = 0) of each segment as a function of DC supply voltage.

Tape preamplifier

Applications for the CA3052 can be demonstrated by discussion of a preamplifier for an automobile 8-track stereo tape player. The external components and connections are shown in Fig. 3. The value of the coupling capacitors from the tape heads to the amplifier inputs may seem large for coupling a signal to a high-input-impedance amplifier, but it is determined by the need for the low circuit noise associated with a low source impedance. The 50-μF capacitors and the 75-ohm resistors correspond to C_f and R_f in Fig. 1. These components restrict the maximum voltage gain of the input-amplifier segments to about 45 dB. The 0.22-μF capacitors and 200-ohm resistors provide a feedback circuit that further attenuates the higher audio frequencies to correspond approximately to the National Association of Broadcasters standard playback frequency response.

Although the preamplifier is stable when a common supply voltage is used for the four segments with the inputs terminated, decoupling is often advisable to ease the requirements on power-supply impedance with regard to filtering, channel separation, and stability. Typical current drain is shown in Fig. 4. In this example, the supply to the input-amplifier segments is dropped to six volts; the decoupling circuit is inexpensive; the power input to the IC is small; yet the dynamic range remains more than adequate. The total current from the 12-volt supply is 20 mA.

The outputs of the low-level segments are DC-isolated from the volume controls to avoid excess resistor noise which can result from direct current. In a test with one type of volume control, excess noise of about 10 dB was produced by a current of 50 μA.

The tone-control of the original tape player is left intact to demonstrate the adaptability of the CA3052 to various amplifier systems. The volume control is coupled to the output amplifier segment through a capacitor that has a relatively large value (as in the case of the tape-head input) to maintain a small source impedance at all frequencies and thus a good signal-to-noise ratio. The maximum gain of either output amplifier is limited to about 50 dB by the 56-ohm resistors in the feedback circuits. Both gain values are about 45 dB at the middle setting of the 200-ohm balance control, and the minimum gain is about 41 dB at the extreme adjustments of the balance control. This control system illustrates departures from conventional circuitry possible with the CA3052.

Amplifier characteristics

The effect of supply voltage on the open-loop voltage gain—i.e., the gain obtained with the feedback (inverting input) terminal bypassed to ground—is shown in Fig. 5 for a typical unit.

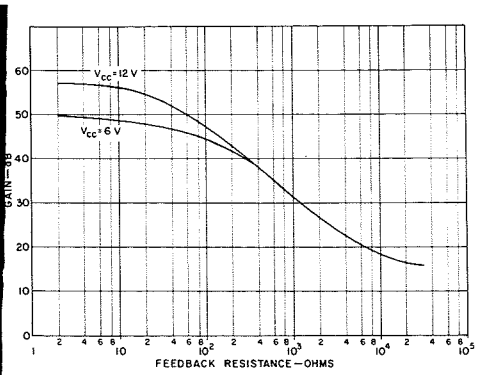

Fig. 6—Typical voltage gain of each amplifier segment as a function of feedback resistance (R_f).

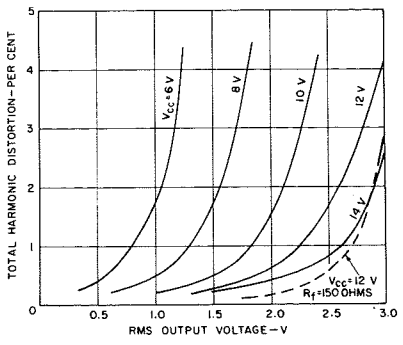

Fig. 7—Typical total harmonic distortion; open-loop (solid) and with 12 dB of feedback (dashed).

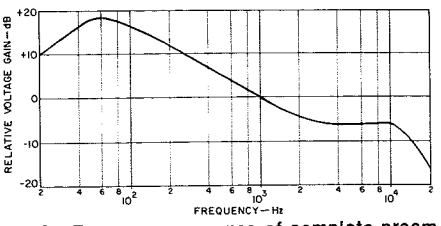

Fig. 8—Frequency response of complete preamplifier equalized for tape playback and passed through "C" filter for noise measurements.

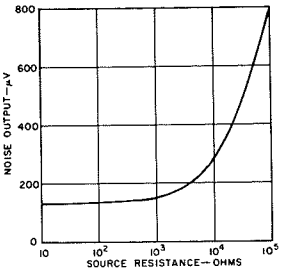

Fig. 9—Typical noise output of one amplifier segment operated at a voltage gain of 40 dB over the audio band (about 13 kHz) as restricted by the "C" noise-weighting filter.

Variations in units or surroundings would have little effect on the closed-loop gain, which is normally reduced by feedback to 45 dB or less. The feedback resistance required for a desired value of gain is shown in Fig. 6.

Output-signal capability and distortion are major considerations in the choice of supply voltage (gain is a secondary consideration provided the supply is greater than about 6 volts). Typical values of total harmonic distortion (THD) as a function of output voltage are shown in Fig. 7. The distortion data are given for open-loop conditions because application of a moderate amount of feedback reduces the THD by the feedback ratio. The dashed curve in Fig. 7 illustrates this reduction for a feedback ratio of 4. (The feedback of 12 dB yields a net gain of 45 dB for the amplifier.)

The frequency-response characteristics of the CA3052 are controlled at the bass end primarily by the feedback bypass capacitor (C_f in Fig. 1) because a relatively large value of input-coupling capacitor is required for reduction of low-frequency noise. The audio spectrum, at least, is easily accommodated. At the high-frequency end, the open-loop response is down 3 dB at about 325 kHz and drops at the rate of slightly more than 6 dB per octave at higher frequencies. This characteristic implies good inherent stability against undesired oscillations. Most cases of high-frequency oscillation are caused by capacitance coupling from output to input. If such capacitance is unavoidable in the circuit layout, a termination impedance to reduce the high-frequency response can be used to stop oscillation.

The noise generated in the tape preamplifier must be weighted in frequency content by the tape equalization and by the response of the ear. The frequency response of a test amplifier segment shown in Fig. 8 includes the tape playback equalization and the standard "C" weighting filters. The use of a "B" filter, which represents a more realistic weighting for the subjective impression of low-frequency noise, would improve the data by about 4 dB. With a source impedance of 1000 ohms, a typical reading of noise output expressed as an equivalent input signal at 1 kHz is about 2.5 μV.

The noise generated in the amplifier segment following the volume control is also of interest because it degrades the signal-to-noise ratio at low volume settings. In this case, the amplifier frequency response is basically flat (unless modified by tone controls) and data are measured for a frequency band limited by a "C" filter (equivalent bandwidth of about 13 kHz). Fig. 9 shows typical noise output voltages of an amplifier segment operating at a gain of 40 dB as a function of input termination resistance. As a point of reference, the theoretical noise voltage generated by a 1000-ohm resistance over this bandwidth is about 0.5 μV (50-μV output).

The input impedance of each amplifier segment is typically about 90,000 ohms. This value is considerably higher than needed for the tape-head application, but is useful for amplifier segments that follow volume or tone controls and adds versatility for other types of signal sources. The output impedance is approximately equal to the collector load of 1000 ohms when the amplifier is in the open-loop condition or when maximum output-swing capabilities are considered. In normal use, the small-signal output impedance is reduced by the feedback: typically about 140 ohms for an amplifier operating at a voltage gain of 40 dB (feedback of 17 dB).

The electrical separation of amplifier segments is expected to be more than adequate for most audio applications. Even in the preamplifier described above, in which segments are cascaded, a 1-kHz signal in one channel induces a signal in the other channel that is lower in amplitude by more than 40 dB at maximum gain (about 65 dB voltage gain); under these conditions, the undesired signal is submerged in noise. The fact that the separation is not detectably worse at 10 kHz indicates that capacitance coupling is no factor at audio frequencies. The capacitances between leads of the package and external wiring are undoubtedly much greater than the internal capacitance couplings, but are significant only at frequencies approaching 1 MHz. Other sources of coupling, however, such as through common ground and positive-supply line resistances, can be high enough to warrant measurement (ratios as low as 20 dB when the overall gain is of the order of 80 dB at low frequencies). Coupling of this degree can be avoided in external wiring of complete amplifiers by avoidance of common ground resistances. The use of two positive-voltage supply points in the CA3052 facilitates isolation of power-supply impedances.

Conclusions

The CA3052 amplifier system described compares favorably with other systems in terms of low noise, low distortion, and high stable gain. Versatility in use of power supplies and amplifier systems arrangements are additional features of interest. The primary purpose of the design, however, is to achieve good performance at lower cost than with other systems.

Acknowledgments

The author thanks H. W. McCord for his contributions to the low-noise design, R. G. Vano for measurements, and the many others who were responsible for layout, fabrication, etc.

Maturation of a chrome-photomasking operation

H. A. Stern

Modernization and expansion of the chrome-photomask area is vital for the continued progress of RCA's solid-state business because the chrome photomask provides many advantages over the conventional emulsion mask, such as improved edge acuity, linewidth resolution, and wafer yield. The facilities initially used for chrome-mask making had been sufficient for development of the technology but were considered limiting in the quantity and quality of chrome photomasks that they could produce. The modernization program described in this paper changed the operation from a laboratory/model-shop state to a technically sound production facility capable of supplying chrome masks for immediate and future needs of RCA's solid-state-device customers.

THE CHROME PHOTOMASK is the most recent and most popularly accepted tool for the translation of micro-imagery onto the silicon wafer in the manufacture of solid-state devices. This significant RCA development has become a standard in the microelectronic industry. In response to the development by RCA of a metal photomask that improved the edge acuity of the micro-imagery on silicon wafers, the RCA Photomask Operation provided laboratory and model-shop facilities for the experimental production of chrome masks. During the ensuing six-year period, the chrome mask was improved to its present state of the art in these facilities.

During 1968, a concentrated engineering effort was expended to establish a technological base for an expanded chrome-masking operation. Much of the work was directed toward the introduction of "good solid-state-device practice"; that is, the institution of known, well-documented, and tested processes capable of performing the required action. Many important non-technical factors had to be taken into consideration—some of which were more important than the basic technology developed. For this reason, this paper discusses both technical and philosophical considerations of chrome-photomask manufacture and the interaction and relative significance of each of these considerations.

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Fundamental chrome-mask process

The basic steps in the production of a chrome mask should be understood as a basis for any in-depth understanding of the need for process improvement. The following list describes the fundamental steps currently followed to produce a chrome photomask:

1) Obtain an acceptable glass substrate.
2) Clean the glass substrate.
3) Apply a 700-angstrom-thick layer of chrome to the glass surface.
4) Apply a photoresist to the chrome surface.
5) Select an acceptable emulsion photorepeater master or an acceptable sub-master generated from the photorepeater.
6) Generate a chrome work master for the purpose of manufacturing chrome prints.
7) Place the photoresist-coated chrome blank in contact with the chrome master to which it is to be exposed.
8) Expose the system to an appropriate light source for a predetermined period of time.
9) Develop the exposed photoresist image in the proper solvents to render a clear image in the photoresist.
10) Harden the photoresist image by an appropriate heating cycle.
11) Etch away the exposed chrome in an etching solution which is compatible with the resist.
12) Remove the polymerized resist in a stripper capable of attacking the resist in question.
13) Thoroughly clean the chrome mask thus generated.
14) Submit the chrome mask for visual, dimensional, and alignment inspection.

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received the ChE from the University of Cincinnati in 1952 and the MS in chemistry from Franklin and Marshall College in 1960. In 1952, Mr. Stern entered the RCA training program. From 1954 to 1956, he served in the U.S. Army Chemical Corps as an engineer. In 1956, Mr. Stern joined the RCA Tube Division in Lancaster, Pa, as an engineer and, in 1962, he was promoted to engineering leader. In 1967, he joined the Solid State Div. in Somerville, N.J. as a senior engineer. Mr. Stern has developed techniques to use radioisotopes and the radiotracer technique in the solution of vacuum tube problems. He did development engineering on picture tube problems caused by chemical factors and was instrumental in adapting "Silverama" processing techniques to mass production. He worked on the development and application of thermonic emitters in relation to power tubes, cathode development for the RF cooking tube, and application of ultra-high-vacuum techniques to the processing of power tubes. Mr. Stern also worked on the development of production processes for the manufacture of emulsion and chrome photomasks and the development of methods to mechanize the bonding and packaging of integrated circuits. He is presently leading an engineering effort to develop fabrication methods for liquid crystal displays. Mr. Stern is a registered Professional Engineer in Ohio and Pennsylvania. He is a member of the American Society of Testing Materials and the Health Physics Society. Mr. Stern has published extensively and has several patents.

The laboratory and its limitations

The chrome-photomask laboratory was established in response to the need for a technical competence in chrome-mask processing. As so often is the case, equipment selected for the laboratory was wafer-processing equipment modified to accommodate glass plates. Several varieties of light sources were employed for exposure of the plates. The photoresist whirler was of in-house construction and had a relatively slow acceleration rate. The general nature of the ambient air was such that particulate contamination was highly probable. Laminar-flow hoods were employed over the photoresist operation only.

Within a relatively short time period, the advantages of the chrome mask were demonstrated, and the laboratory facilities were converted to a model-shop activity whose mission it was to generate chrome masks for production evaluation. Some attempt was made to improve the facilities in the converted laboratory. The printing station was standardized with a 600-watt Sun Gun [Sylvania tradename] positioned at a fixed distance from the exposure frame; the entire apparatus was placed in a laminar-flow hood to improve the air environment. As the demand on the model shop increased, additional facilities were installed. In time, however, the overcrowded conditions at the sinks, the rapid cycling of the chrome-deposition equipment, and the crowded conditions at the printing stations began to take their toll in quality of product and the total production yield.

The technician in the laboratory became the technician in the model shop, and, as time progressed, additional technicians were added to the staff. These technicians can be generally described as well-trained experimentalists; people trained to innovate who, in general, scorn routine. Each technician soon became skilled in his ability to generate chrome masks, but each had his own specific technology for doing so. It became fashionable to speak of one's "bag of tricks" in making chrome masks and, unfortunately, one technician was held in higher esteem than his colleagues because of his superior "bag of tricks."

The lack of standardization, combined with obsolete facilities in an overcrowded work area, appeared to be stifling a promising new technology. It was in response to these conditions that the effort described here was undertaken.

Process improvements

During a year of engineering study of the chrome-photomask area, many individual steps in the process of mask generation were critically reviewed. In some cases, an immediate change in the operation was indicated and was immediately implemented. In other areas where necessary improvement was indicated, the solution to the problem was long in coming. The description of process improvements will be presented according to the logical sequence of steps used in producing a chrome mask rather than in the sequence of chronological events that occurred during the year's study of the chrome-photomask area. The degree of difficulty in achieving these improvements will become apparent in the discussion.

The glass substrate

A new glass substrate has been selected to receive the chrome deposit in the chrome-masking operation. The chrome-mask production was originally started with Corning 7059 barium aluminum borosilicate glass because it provided desirable advantages as a substrate for chrome deposition; it was hard, and the surface was free of physical damage and resistant to abrasion. The surface of 7059 glass was easily cleaned and accepted the chrome deposit readily with excellent adherence. Its only disadvantage was its unacceptable flatness. The glass exhibited a bow and warp that was in excess of 2 mils/in. In addition, the surface exhibited a ripple that could be as great as 0.1 mil in depth. Fig. 1 shows distribution data for the degree of bow and warp of Corning 7059 glass. At first, the excessive bow and warp of the glass did not seem serious because glass substrates with 1-mil/in. bow were of adequate flatness for most applications, and solid-state devices were designed with large tolerances. Because the device designs were large and simple, the problem of alignment of the various parts presented little difficulty. However, as device designs became more critical and dimensional tolerance became

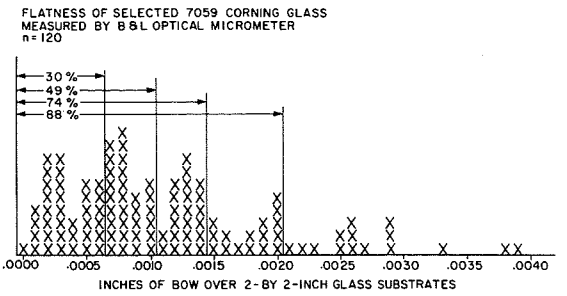

Fig. 1—Distribution data for degree of bow and warp in Corning 7059 glass.

tighter, more and more chrome masks printed on the 7059 glass with the 1-mil/in. flatness specification failed to align. Glass selection or culling served as an interim solution to this problem. The acceptable flatness specification was tightened; first to 0.7 mil/in., then to 0.5 mil/in., and finally to 0.3 mil/in. It is apparent from Fig. 1 that the acceptance level of glass substrates dropped from about 90% to about 30% for 0.3-mil/in. flatness.

The search for a consistently flatter glass substrate started early in chrome-mask technology development with the realization that the Corning 7059 glass was inadequate. Soda-lime glass was immediately recognized as a solution to the flatness problem. This glass could be easily supplied to a specification which would permit a bow or warp no greater than 0.5 mil/in. The surface condition of this glass, however, was totally unacceptable for chrome masking because of scratches, digs, and other surface damage. The decision was made to continue with the use of the Corning 7059 glass in spite of its flatness problem. As a result, considerable difficulty was encountered in mask alignment.

Early in 1968, a concentrated effort

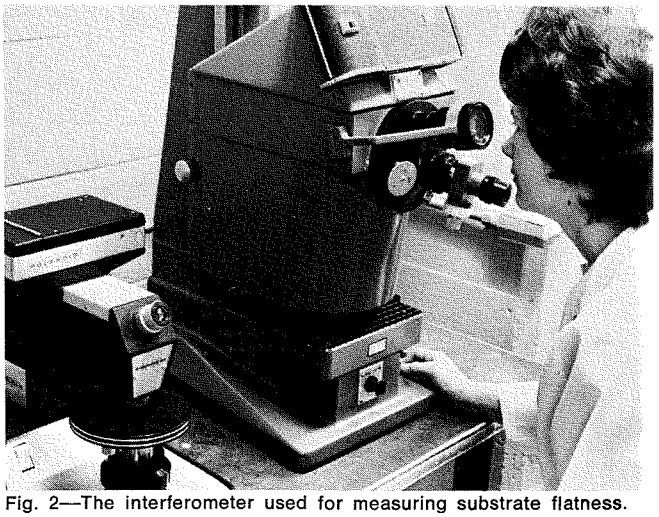

Fig. 2—The interferometer used for measuring substrate flatness.

Fig. 3—The glass-cleaning operation.

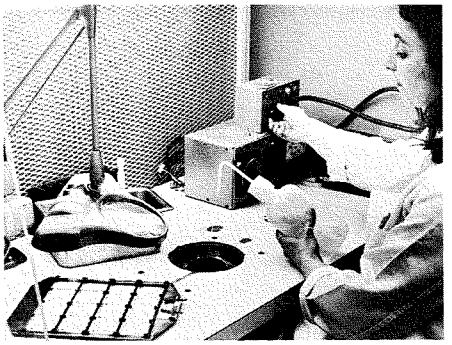

Fig. 4—The final step in the glass-cleaning procedure.

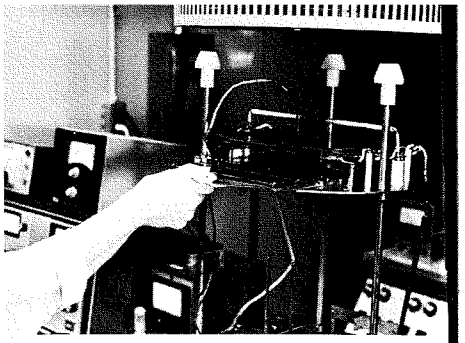

Fig. 6—Mechanical fixturing used with the vacu system.

was made to successfully employ a soda-lime glass as a chrome substrate. The chrome-masking industry was surveyed and was found to be using soda-lime glass substrates exclusively. These substrates were being culled from glass shipments at a 20 to 40% yield level.

When it became known that a major glass supplier was providing glass substrates to members of the photomasking industry, quantities of 1,000 pieces/month were ordered for evaluation. A check on flatness indicated that the bow of the glass was well within the 0.5-mil/in. specification. However, visual inspection of the surface showed a 57% defective level on the first shipment, a 68% defective level on the second shipment, and a 70% defective level on the third shipment. A further reduction in yield was experienced in each shipment after the chrome blanks were quality inspected and additional surface scratches and other imperfections became apparent. This glass supplier was ultimately abandoned as a source of glass substrates for chrome blanks.

Many vendors submitted samples of glass for evaluation but, in almost every instance, the severity of the surface-defect problem was underestimated by the vendor.

A group of vendors did, in fact, supply soda-lime glass that met both the flatness and surface requirement. In every case, however, the glass had been specially treated to provide a defect-free surface. The process of each company was proprietary, but in every case, mechanical and/or thermal polishing was suspected; the cost of these substrates reflected the special treatment. Firms providing these samples included: Laboratory Optical Company, O & S Research, Spectra-Physics, Owens-Illinois Glass Company.

Only the Lustron Division of American St. Gobain Glass Company was able to supply a soda-lime glass substrate which was reported to be a virgin surface that met all flatness and surface requirements. Lustron soda-lime glass is drawn in such a manner as to render its surface less susceptible to mechanical damage during cutting and handling operations. The process includes the deposition of a low coefficient of friction surface by means of a vapor-deposition process. The specific process is considered proprietary by the American St. Gobain Company.

The Lustron soda-lime glass became the standard substrate glass for chrome-blank manufacture in the later months of 1968. The rejection of chrome masks due to alignment runout was virtually eliminated because of the improved flatness. The availability of scratch-free Lustron glass did not totally eliminate visual defects in the completed chrome mask, and because the glass was coated with a protective film, an extraordinary effort was required in the cleaning of the substrate prior to chrome deposition. In addition, each shipment exhibited pits and gouges in the glass to varying degrees; this type of defect is more difficult to detect than are the scratches, and represents a major source of trouble.

Previous mention has been made of the successful use of polished glass substrates in chrome photomasking; a properly polished glass substrate resolves the major problems encountered in drawn or rolled glasses. The polishing process can provide a surface free of mechanical damage; i.e., free of scratches, pits, and the like. In addition, the polishing process can provide a surface flatness that exceeds the best flatness available from virgin glass. Two-inch-square glass plates can be routinely ground and polished to a flatness well within 0.050 mil/in. Polished soda-lime glass plates have been evaluated and found to be quite suitable for a chrome-blank substrate; the polished surface, however, is subject to handling damage as is any soda-lime surface. The increased cost of obtaining polished soda-lime glass was not justified in light of the overall good quality of the Lustron glass source.

The many advantages attributed to the borosilicate "Pyrex type" glasses could become available if only the flatness problem were resolved. [Pyrex is a trademark of the Corning Glass Works.] In this area, grinding and polishing could serve to great advantage. Glass-polishing companies have been contacted and are being asked to provide production quantities of polished "hard" glasses at reasonable prices to serve as chrome-blank substrates. The problem of measuring flatness was resolved with the purchase of an interferometer which allows the measurement to be taken without directly contacting the sample; Fig. 2 shows the instrument.

The cleanliness of the glass substrate prior to chrome deposition establishes the quality of the chrome blank produced. It is, therefore, important to have a technically sound cleaning procedure established that can remove the soils that would inhibit chrome film formation.

The common substrate-cleaning procedure in use early in 1968 was tedious and difficult to justify technically. Where some aspects of it were sound, other aspects were ill-formed and a waste of time. The cleaning procedure was modified to include the use of the well-documented cleaning agent ammonium hydroxide in combination

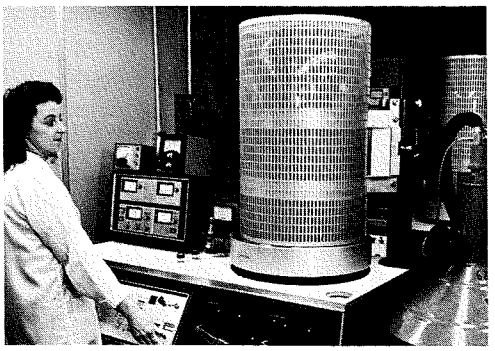

Fig. 5—The high-vacuum system used for chrome deposition.

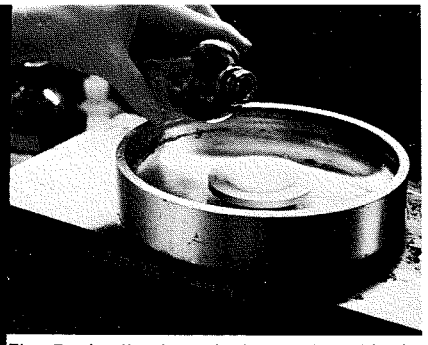

Fig. 7—Application of photoresist with the original whirler.

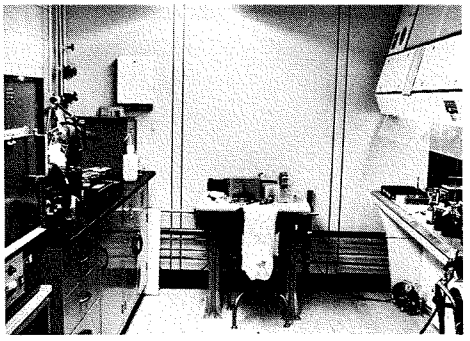

Fig. 9—The positive-resist-application laboratory.

Fig. 10—The original chrome-mask exposure fixture.

with hydrogen peroxide; references dating back to 1958 describe the use of these materials for cleaning glass.[1] Therefore, about mid-year in 1968, a batch, alkaline cleaning procedure employing the cleaning agents described was instituted; Figs. 3 and 4 illustrate steps in the cleaning process.

The alkaline cleaning procedure is adequate where little or no inorganic contamination is present; however, when the glass surface is weathered or otherwise contaminated with an inorganic material, additional cleaning action is required. The introduction of a detergent-paste scrub helps to abrade the surface and free it from inorganic contamination. An increase in the reaction time in the ammonium hydroxide/hydrogen peroxide solution also assists in the removal of inorganic contamination sites. In cases in which the glass is severely weathered, however, as is the case with many soda-lime glasses, an acid cleaning procedure is required to render the glass acceptable for chrome deposition. The essence of this procedure is an acid-detergent solution defined by the following formula:[2] 33% HNO_3—5% HF—2% Suitable Detergent—60% H_2O.

The acid cleaning procedure is severe and difficult to control; considerable evaluation was required before this process was judged useful. In spite of this, the process is considered to be unstable for production use.

The chrome blank

There are two methods of obtaining chrome blanks: by making them in-house or by purchasing them from an outside vendor. The in-house process used to deposit chrome on the cleaned glass substrate was evaluated and found to be technically sound. The process consists of a vacuum deposition of approximately 700 angstroms of chrome on preheated glass substrates located above tungsten source boats containing chrome crystals of high purity; the high-vacuum system is shown in Fig. 5. Chrome deposition is monitored with Sloan thickness apparatus but is manually controlled. Some engineering effort was expended in improving the mechanical fixturing to increase the number of chrome blanks produced during a single pump down; the improved fixturing is shown in Fig. 6. Pump-down cycle duration is in the order of 25 minutes. The chrome blanks are inspected for quality and categorized into three acceptable grades:

Grade A is free of visible defects in the center 1½-inch diameter of a 2- by 2-inch plate.
Grade B may contain 1 to 3 pinholes in the center 1½-inch diameter of a 2- by 2-inch plate.
Grade C may contain 4 to 6 pinholes in the center 1½-inch diameter of a 2- by 2-inch plate.

All plates are visually inspected, without the aid of magnification, over a 600-watt Sun Gun.

The chrome deposition process was formally standardized in a set of operating instructions that included a step-by-step operation of the deposition system, a routine preventive-maintenance downtime procedure, and specific instructions for the inspection and acceptance of a chrome blank.

The manufacture and sale of the chrome blank has become a lucrative business for suppliers of the solid-state device-manufacturing industry. Some masking operations are interested only in the manufacturing of the chrome mask and are satisfied in having the blanks supplied by a vendor. Other masking operations which have chrome-blank facilities still find it necessary to supplement their own production with purchased chrome blanks.

The purchaser of chrome blanks is faced with the evaluation of the several varieties on the market. Some blanks are supplied on polished and others on unpolished substrates of different glass compositions. The chrome can be either evaporated or sputtered in one or several layers that vary in thickness and density. It is not surprising that these factors can induce vastly different results in a standardized chrome-masking process.

The following is a list of some of the problems encountered in evaluating purchased chrome blanks against RCA's own product; these problems could arise with any purchase of chrome blanks:

The vendor's product might not meet the inspection criteria for visible defects.
The glass substrate quality upon which the chrome is deposited might be such that "intrusion" defects would occur after etching.
The etch rate of the chrome could be vastly different from that of the standard in-house chrome blank.
The adherence of the photoresist to the chromed surface might be adversely affected by contamination which, in turn, might cause undercutting of the chrome image during etching. These conditions must be understood, for the blanks purchased.
Vendors might have (indeed, they have had) difficulty in meeting their delivery commitments.

Chrome blanks from the following list of vendors (alphabetically arranged)

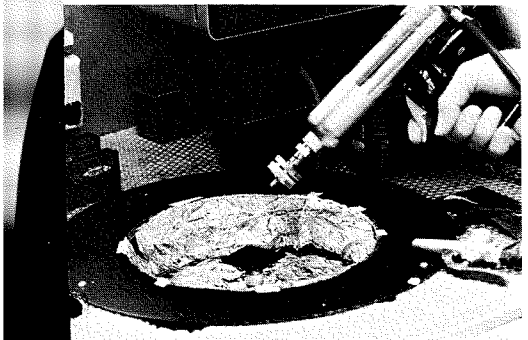

Fig. 8—Application of photoresist with the newer, improved whirler.

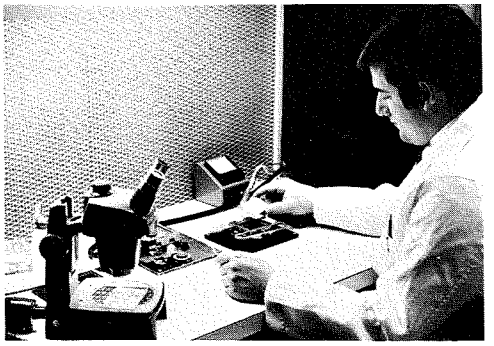

Fig. 11—The newer, improved chrome-mask exposure fixture.

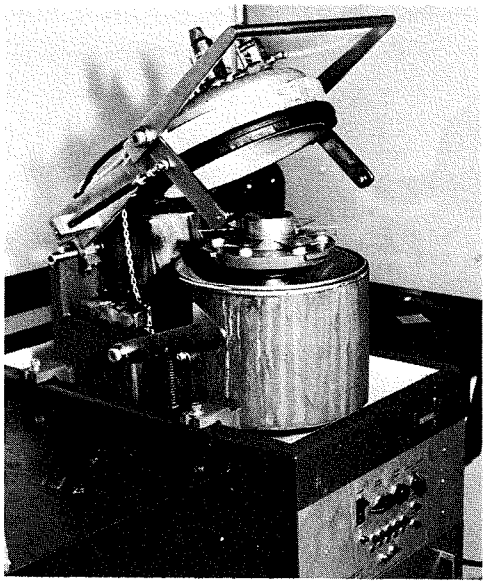

Fig. 12—Spray-development apparatus used on chrome masks.

were evaluated: Bell & Howell Company, Corning Glass Works, Kodak, Spectra-Physics, Towne Labs, Transmask.

Photoresist and photoresist application

The photoresist for chrome masking and its method of application was standardized into a routine production process during the period of this study by introduction of a new whirler, and the selection of one photoresist composition for all but the most unusual cases of chrome masking.

The selection and application of a photoresist in the chrome masking process was the most important item in the technician's "bag of tricks." This fiction was perpetuated and justified with the aid of a whirler, shown in Fig. 7, whose control of speed and acceleration and other adjustments were inaccurate and unreliable. Photoresists in use at the time were Kodak Photoresist (KPR), KPR with 11% Kodak Photoresist Lacquer (KPL), Kodak Thin-Film Resist (KTFR), and Shipley AZ111 Resist.

The KPR solutions were in greatest use, with the KTFR and the positive Shipley AZ111 resist available for special cases. After considerable evaluation, it was decided to standardize the KPR/11% KPL photoresist for production. This standardization became an actuality after the installation of the new whirler shown in Fig. 8. The whirler provided a measureable and reproducible acceleration to operating speed in less than one tenth of a second. These factors permitted a uniform application of the KPR/11% KPL over a wide range of thickness on both 2- by 2-inch and 2½- by 2½-inch chrome blanks. A calibration chart interrelating photoresist thickness and whirler speed was prepared and incorporated in the operating instructions for the process. It must be emphasized that the selection of KPR/11% KPL was a compromise; this negative resist was one which all the technicians were familiar and around which a standardized process could be written, but it was not necessarily the optimum resist for chrome masking.

In conjunction with the above effort, a separate study was made of the various positive resists available on the market. As a result of this study, a complete positive-resist chrome-masking process has been developed for production and has been standardized in a complete set of operating instructions. The process is designed around the Shipley AZ1350 and AZ1350H photoresists. The recently introduced Kodak positive resist KAR3 has been evaluated and can easily replace the Shipley resists with only minor modification of the operating instructions. The positive-resist chrome-masking process has not as yet been evaluated under the rigors of production; it is anticipated that production evaluation will take place when a well-designed commercially-available, mercury-vapor-lamp contact printer is purchased. Fig. 9 shows the laboratory facility in which positive-resist application is being conducted.

Little change has been instituted in the exposure of the photoresist to the 600-watt Sun Gun. Additional process control has been introduced through the monitoring of the light source used for exposure with an IL-600 photometer. It is recognized that the Sun Gun is far from the best ultra-violet light source for fine photoresist imagery, and as mentioned above, engineering effort is being expended to rectify this weakness in the chrome-masking operation. Figs. 10 and 11 show the old and the new exposure fixtures.

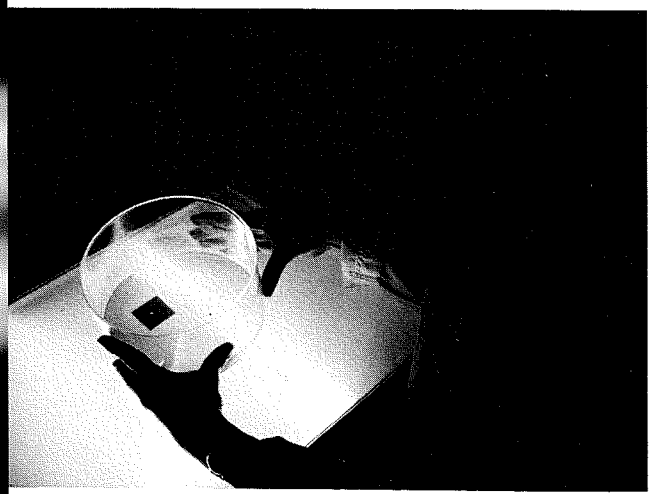

Fig. 13—Single chrome-mask etching.

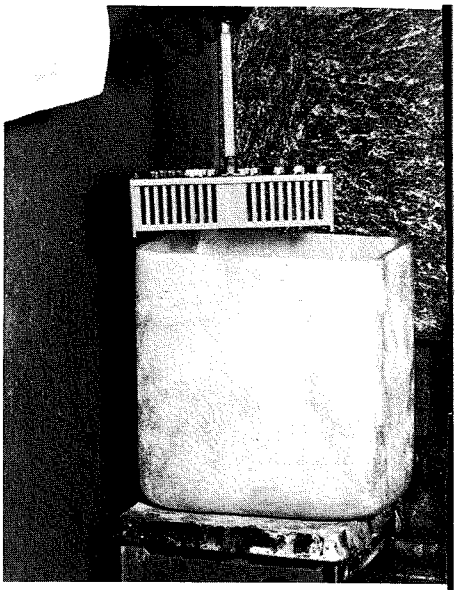

Fig. 14—Batch etching of chrome masks.

The KPR/11% KPL photoresist image is developed in the K & S (Kulicke and Soffa Inc.) spray-developing apparatus shown in Fig. 12. The photoresist image is subjected to the standard RCA developing process for this photoresist.

A new scheme for developing the photoresist has been under investigation and has been found more conducive to the production of chrome masks. The new scheme incorporates a "pot whirler" system which will be included in the new production facilities when constructed. The chemical processing previously described will remain unchanged in the new scheme.

Etching and finishing

The major improvement in chrome etching and chrome-mask finishing

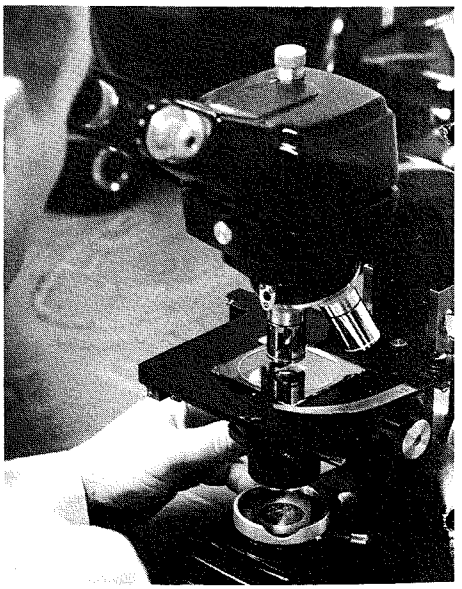

Fig. 15—Microscopic inspection of chrome masks immediately after etching.

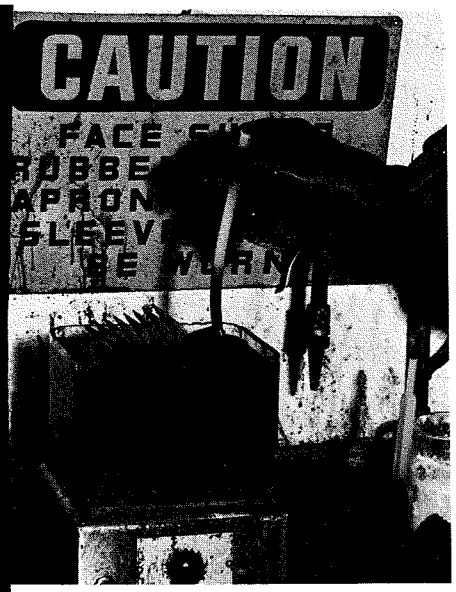

Fig. 16—Batch stripping of photoresist from chrome masks.

was in the optimization of time/temperature conditions to achieve an acceptable, completed chrome mask and in the increase in the number of pieces that could be processed at one time. Fig. 13 shows chrome masks being etched one at a time; Fig. 14 shows the recently instituted batch-etching process. Product inspection was also emphasized at this stage of the process.

The etchant used by RCA is the potassium ferricyanide/sodium hydroxide mixture suggested by Kodak for the etching of their chrome blanks when a negative photoresist is used. An optimum time/temperature cycle was established with this etchant in use. A thorough inspection of the mask upon completion of etching, (Fig. 15) but prior to photoresist removal may reveal areas of unetched chrome that can be removed by additional etching. The operating instructions caution the operator to inspect his product carefully at this stage in the process.

The finishing of the chrome mask comprises the stripping of the photoresist and the final cleaning and drying of the completed product; the stripping operation is shown in Fig. 16. Here again, the process was standardized to limit the exposure of the mask to the photoresist stripping agent. The operating instruction requires the use of a standard stripper. The chrome mask, sans resist, is rinsed in methanol and carefully washed with a detergent solution. It is then water rinsed, methanol rinsed, and dried.

Defects and problem areas

Many of the process improvements instituted to remedy a chrome-mask

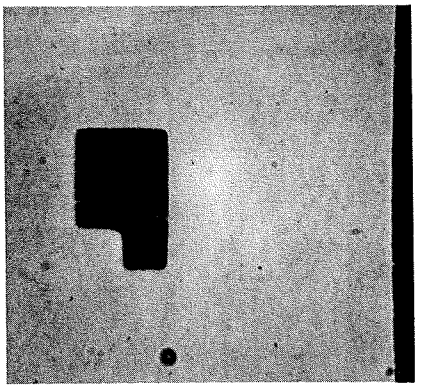

Fig. 17—Photomicrograph of a "finger" intrusion.

defect or a process problem area. These defects and problems are defined below and related to that portion of the process responsible for their cause.

An "intrusion" is defined as a lack of chrome along the edge of an opaque portion of the mask. It appears as either a transparent "finger" reaching into the opaque chrome image, as shown in Fig. 17, or a transparent semicircular notch in the edge of the chrome image, as shown in Fig. 18. The intrusion is characterized as being unrelated to a photoresist failure and results directly from a surface defect existing in the glass substrate, usually in the soft soda-lime glass. An intrusion is formed when a scratch or pit in the glass forms a capillary with the photoresist which permits the etchant to be drawn up over the chrome and to etch it away. Selection of defect-free glass surfaces is necessary to eliminate this defect.

A misalignment between chrome masks in a set made from masters that do align is attributable to the flatness of the chrome-glass substrate. A bow or warp in the glass substrate may be temporarily corrected when the glass is flattened against the master in the vacuum-contact printing fixture during exposure, but when released, the plate will return to its previous curvature. Such a plate, when compared to a truly flat plate, will exhibit a contraction of the image from center to edge. The manifestation is that of

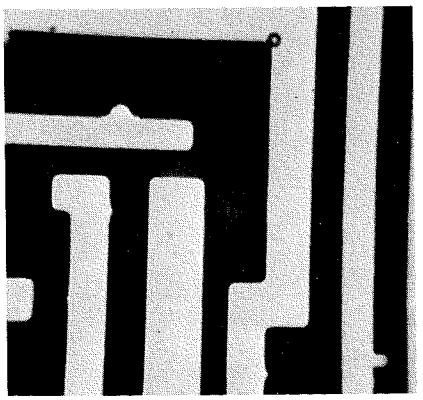

Fig. 18—Photomicrograph of a "notch" intrusion.

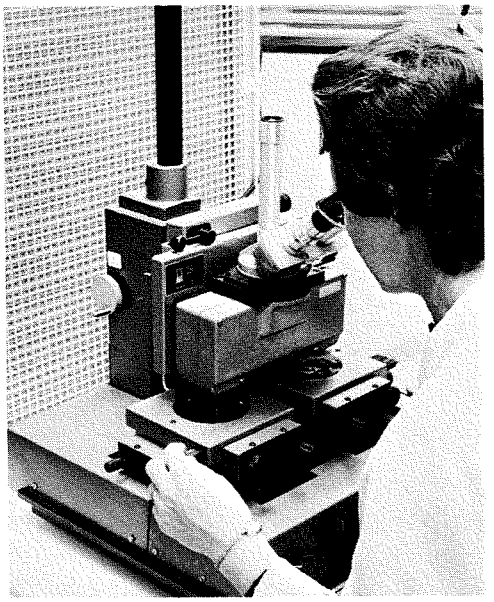

Fig. 19—Mask-alignment equipment.

"run out" of the good plates relative to the bowed plate. Selection of glass with a bow or warp no greater than 0.3 mil per linear inch usually eliminates alignment problems for the average chrome mask. Fig. 19 shows equipment used in the alignment process.

Excessive pinholes in the chrome areas of a mask result from photoresist failure during etching or poorly evaporated chrome blanks. Poor evaporation is caused by poor substrate cleaning or a dirty vacuum system. The former appears to be the dominant cause of pinhole formation. Pinhole formation caused by photoresist failure is usually directly related to photoresist thickness.

Black spots (chrome spots) are formed by residual chrome in transparent areas and usually result from either incomplete development of photoresist, poor rinsing of the photoresist image, or incomplete or insufficient etching of the chrome. The black spot is minimized by adjusting the development process of the resist image to insure adequate removal of unexposed photoresist (by using correct development time) and to avoid the redeposit of particulate matter in developed areas (by using correct rinsing time). Black-spot formation in the etch bath can be traced to microscopic bubble formation during etching. Vigorous agitation of the masks during etching is necessary to eliminate these bubbles.

Loss of photoresist image during development is directly related to excessive spray pressure in the developing apparatus. Underexposure of a nega-

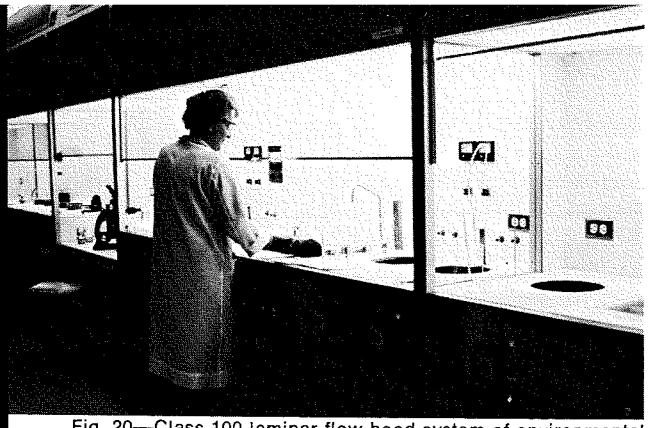

Fig. 20—Class 100 laminar-flow-hood system of environmental control.

tive resist will also show image loss during developing.

Selection and training of personnel

What technical competence must be expected from an operator in a production chrome-photomask operation? Must every operator be a "Nobel Prize Winner"? The second question did not sound as facetious early in 1968 as it does at this writing. Earlier in this paper the innovating, skilled technician with his "bag of tricks" was described; it was obvious that this personality would have a problem adhering to a set of prescribed instructions.

Several types of persons were evaluated as operators in the chrome-masking production area. The most consistent chrome-mask maker was found to be the experienced emulsion-contact printer who was promoted to the chrome operation. His experience in the emulsion mask area had heightened his powers of observation and his understanding of the problems. He had the patience to carefully inspect his work and had already learned to overcome the frustration of having his work rejected by the quality-control activity. The training period for such an individual consists primarily of reviewing the operating instructions for the chrome-masking process, concentrating especially on the problem areas and how to avoid them.

Operating instructions

Many of the procedures in use early in 1968 were basically sound, and variations in approach to these procedures by different technicians were minor. Documentation of the procedure was, however, nonexistent.

One of the most significant steps taken to make the chrome-photomasking operation a routine production facility was the publication of a formal set of operating instructions. The first set of instructions published was far from optimum; in some cases, a process was formalized by taking a consensus among the various technicians and reducing this information to a procedure. However, with time and practice, even these first guesses were revised to workable, formal procedures. As equipment and facilities were purchased and modified, the operating instructions were updated and revised.

The introduction of operating instructions had a tremendous impact on chrome mask production; their inception represented the first real turning point toward the production mode and signaled the end of the model shop approach to chrome-mask making.

Facility expansion approach

The primary objective of the new chrome production facility is to increase production volume and improve the yield at every stage of the process. This primary objective is achieved by implementation of the following secondary objectives: increased production volume and yield, improved production environment, decreased product handling by mechanization, improved work flow, and process control.

The production facility is designed so that during all critical operations the product is subjected to environmental air at least of Class-100 purity. This condition can be achieved in a number of ways, including having all production equipment located in a laminar-flow room, or having a production area composed of interconnected laminar-flow hoods located in an area with one stage of conditioned air (Fig. 20). RCA chose the latter approach for its new chrome-mask facility.

Mechanization is judiciously applied to decrease handling of the product. It is important that the operator have the opportunity to sample and inspect the product as specific points in the process to provide process control. To achieve this control, each "unit operation" is a mechanized module. The development of the photoresist image can serve as an example of a module. The exposed photoresist images on th chrome blanks contained in a tray ar placed in the developing apparatu and exposed to the various solvents i turn. The tray of plates than exit from the developing apparatus in dry state, allowing the operator t sample the tray of plates for the pur pose of inspection. The samples ar then returned to the tray and proceed to the next operation. An apparatu that would automatically proceed from exposure through developing baking, etching, and the like to finish ing would increase quantity of yiel but would be difficult to control. Con siderable process development woul be necessary before such a systen would be feasible.

A production chrome-masking opera tion requires that all materials flow through a production line on which crossovers and bottlenecks are mini mized or totally eliminated. Due consideration has been given to im proving flow of product in the new facility; each step of the process is consecutive and "in-line." Adequate hold stations, inspection stations, and sinks are provided "in-line" to com plete the process without backtrack o crossover.

A production chrome-masking opera tion must incorporate adequate process control at all stages of manu facture. Metering for temperature whirler speed, light intensity, thick ness of deposition, and other factors as well as interprocess inspection must be instituted.

Conclusion

RCA's new chrome-photomasking operation began production during the second half of 1969. Materials and processes incorporated into this operation have been reviewed and in some instances have been improved. Operating instructions for this facility have been published, and factors relating to selection of personnel and facility expansion have been reviewed.

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1. Koontz, D. E., "The Preparation of Ultraclean Electron Tube Components by Chemical Etching," *ASTM Special Technical Publication No. 246.*
2. Naiditch and Wreede, "Cleanness of Glass Surfaces Measured by Evolution of Hydrogen from Sodium-Ammonia Solutions," *Journal of Vacuum Science and Technology,* Vol. 5, No. 2.

Recent technical books by RCA authors

resented here are brief descriptions of technical books which have recently been uthored by RCA scientists and engineers, or to which they have made major contri-utions. Readers interested in any of these texts should contact their RCA Technical ibrary or their usual book supplier. For previous reviews of other books by RCA uthors, see the August-September 1968 and August-September 1969 issues of the CA ENGINEER. RCA authors who have recently published books and who were not ted in these listings should contact the editors, Bldg. 2-8, Camden, Ext. PC-4018.

lectronic Ceramics

. Irwin Gordon
ontributor)
CA Laboratories
rinceton, New Jersey

n compiling this volume, O. J. Witte-ore, Jr. of the University of Washing-n asked six authorities to contribute apers on several specialized areas in the eld of electronic ceramics. Their contri-utions reflect the variety and depth in his highly sophisticated segment of ce-amic technology. As a reference, this ook should be useful both for senior nd graduate courses and also for the ontinuing education of graduate engi-eers. Two papers, on integrated circuits id on microelectronics, ably describe the ecent condensation of electronic cir-uitry. Other subjects covered are pure xide ceramic insulators, ceramic to metal ealing, ferrites, and ferroelectrics.

r. Gordon contributed a chapter on the Relation Between Fundamentals, Prepa-tion Parameters, and Properties of Fer-ites." *(Special Publication No. 3 of the merican Ceramic Society, 4055 N. High treet, Columbus, Ohio 43214).*

DR. IRWIN GORDON received the BS n Ceramics from Rutgers University in 948, the MS in 1951, and the PhD in 952 from the same institution. From 1948 o 1952, he held a research assistantship n the School of Ceramics at Rutgers niversity working on single crystal syn-hesis and studies of various silicates and are earth aluminates. In 1952, Dr. Gor-on joined the technical staff of RCA aboratories where he has worked on the velopment of magnetic materials for arious applications. This has included naterials for permanent magnets, multi-unction composite materials, recording ape pigments, small size HF antennas, nd non-spinel type magnetic materials or use in the VHF and UHF regions. Most recently he has investigated ferrites r use in laminated computer memories, s well as ferrites for microwave use. He s a member of the American Ceramic ociety, the N.J. Ceramic Association, igma Xi, Keramos, and a subcommittee n non-metallic magnetic materials of the .S.T.M.

The New Electronics

Bruce Shore
Corporate Public Affairs
New York, N.Y.

This book is a simple yet highly informative guide to electronics—from the invention of the transistor in 1948 to the very latest advances in holography, lasers, and artificial intelligence. *The New Electronics* offers a literate overview of solid-state electronics and the materials and phenomena associated with it.

The modern solid-state revolution results from the development of quantum mechanical theory, together with a new ability to control the composition and structure of solid materials. From these have come such achievements as field-effect transistors, superconductive magnets, Gunn-effect devices, and even office copying machines. All of this material is treated with a "how it works and where it came from" quality, making even the most highly technical subject easily understandable. The text includes the first popular discussion of hole-electron theory, the roles of bulk, thin film, and surface phenomena in electronic materials, and the current trends of modern electronics away from radio waves and toward light, and toward integrated circuitry and artificial intelligence. *(McGraw-Hill Book Co.; 1970; price $10.00).*

BRUCE H. SHORE received the BA in English from Yale University in 1952. Shortly after graduation, Mr. Shore joined the editorial staff of the *New Haven Register.* In December 1953, he became associated with the Los Angeles Stock Exchange and subsequently worked for Dean Witter & Co. In May 1954, he joined the brokerage firm of Walston & Co., and the following year transferred to the company's New York Headquarters, where he was in charge of the odd lot desk. Two years later, in 1956, he joined the firm of Avery-Knodel, Inc., national spot representative, as Assistant to the Director of Promotion. In March 1958, Mr. Shore joined the NBC Radio Network as a writer in the Sales Presentation and Promotion Department. Among his responsibilities at NBC was the preparation of closed circuit presentations to station affiliates. In 1960, Mr. Shore was appointed Administrator, Press Relations, for the RCA Semiconductor & Materials Division in Somerville, N.J., a position he held until going to RCA Laboratories in 1962 to head its Public Affairs activity. He was named Administrator of Scientific Information for RCA Corporate Public Affairs in April 1967.

Wave Interactions in Solid State Plasmas

Dr. Martin C. Steele
RCA Laboratories
Princeton, New Jersey

and

Dr. Bayram Vural
City College of the
City University of New York

This book presents the properties of solid state plasmas and their wave interactions from a unified point of view. The first part of the text treats wave interactions in terms of quasiparticles and the development of a macroscopic hydrodynamic model from the more fundamental microscopic models. In the remainder of the material, the macroscopic model is used to study the interaction of electrokinetic waves (or carrier waves) with one another and with other collective excitations of the solids such as electromagnetic waves, sound waves, and spin waves. For the most part, the authors use semi-classical approaches since they are considered adequate for all but very high frequencies.

A major feature of the text is its emphasis on the unified nature of the collective behavior of quasiparticles in solids. This permits the reader to see the commonality in such seemingly different phenomena as plasma waves, helicon waves, spin waves, and sound waves and demonstrates the manner in which these waves interact with one another. Each chapter presents both theory and the pertinent experimental information for the wave interaction. One chapter clarifies the role of collisions in instabilities in solids. This is the first book in the literature of solid state plasmas to emphasize the physical origin of collision-induced instabilities.

The interaction of spin waves with electrokinetic waves is developed in much greater detail in this text than in any book published to date. The solid state pinch effect is treated in an up-to-date manner, and there is a presentation of the latest experiments related to the theory. The comprehensive bibliography is compiled with regard to both theory and experiment. *(McGraw-Hill Book Company, New York, 1960, 285 pp.; price $15.50).*

DR. MARTIN C. STEELE received the BChE (cum laude) from Cooper Union Institute of Technology in 1940, and the

MS and PhD in Physics from the University of Maryland in 1949 and 1952 respectively. He worked as an engineer for the Office, Chief of Engineers, before the war, and as a research physicist in the Naval Research Laboratory from 1947 to 1955 where he was head of the Cryomagnetic Research Group in the Solid State Division. Since 1955 he has been with RCA, as head of the Solid State Electronics Research and for three years (1960-1963) as the first Research Director of RCA's research laboratory in Tokyo, Japan. At present he is head of the General Device Research Group of the Semiconductor Device Research Laboratory at RCA Laboratories. His research has covered a wide range of areas in solid state physics. He has published forty-five technical papers in these fields and has refereed many articles for the *Physical Review*, the *Journal of Applied Physics*, and the *Journal of the Physical Society of Japan*. He has thirteen issued patents. Dr. Steele is a Fellow of the American Physical Society, a member of Sigma Xi, and a former member of the Washington Academy of Science.

DR. BAYRAM VURAL had his early education in Turkey and college education in Switzerland. He received an Electrical Engineering degree (M.S.) in 1949 and the Dr. of Technical Sciences degree (Ph.D.) in 1952 from the Swiss Federal Institute of Technology, Zurich, Switzerland. From 1951 to 1953, he was associated with Brown Boveri and Company in Baden, Switzerland. From 1953 to 1959, he was associated with the Electronic Equipment and Tube Department of Canadian General Electric, Toronto, Canada, working mainly on microwave problems in connection with radar and communication. From August 1959 to September 1967, he was a member of technical staff at RCA Laboratories, where he was engaged both in theoretical and experimental research work on electron devices of both vacuum and solid-state types. In September 1967 he joined the Department of Electrical Engineering of the City College, the City University of New York, and is now Professor of Electrical Engineering.

Filter Design and Evaluation

Grant E. Hansell
Astro-Electronics Division
Princeton, New Jersey

This practical volume presents all the material necessary to design and evaluate the most commonly used classes of filters; it will be especially valuable to the inexperienced designer who wishes to achieve filter design comparable to that of the experienced designer, and to the experienced designer who is interested in improving his design methods.

With special emphasis on the evaluation part of filter design, the author presents methods, along with data in tabular and curve form, which permits the designer to evaluate attenuation, phase, phase delay, and envelope delay of lowpass, highpass, and bandpass filters. This makes it possible to evaluate more than one type of filter for a particular application and to select the most suitable design.

The filter parameters are evaluated by making use of normalized data, and the information on attenuation and phase is normalized for a cutoff frequency of one radian. Envelope delay information is normalized in microseconds for a one-kilohertz lowpass filter bandwidth.

Filter Design and Evaluation includes material on the following filters having equal input and output terminations: Butterworth, 2 to 9 stages; Gaussian (Bessel), 2 to 9 stages; Linear Phase with 0.05 degrees phase error; Tchebycheff, 3 to 9 stages, 0.011 to 0.28 dB ripple; Cauer or elliptic function, 3 to 7 stages, 0.011 to 0.177 dB, passband ripple and stopband attenuation $\geq$40, 45, 50, 55 and 60 dB. Much of the data included is not available in any other known source at this time, particularly attenuation, phase, and delay for the Cauer type, which is the most popular filter at the present time.

Material on the use of computers to aid in the calculation of actual element values from the normalized element values, a discussion of phase correctors, and a novel method for phase corrector alignment are also given. *(Van Nostrand Reinhold, N.Y., December 1969, 204 pp., 130 ill., 8½ x 11; price $15.00)*

GRANT E. HANSELL graduated from Purdue University in 1931 with the BSEE. He has been employed in research and development work for RCA since that time. Mr. Hansell's work has been in the communications field. He has had considerable experience in the development of frequency shift receivers and multichannel SSB receivers for telegraph use in the HF range. In more recent years, his work has been in signal processing, chiefly in the multiplexing and demultiplexing of signals for satellites. The requirements for filters and phase correctors for this field led him to pursue information on their design and evaluation. Mr. Hansell has several patents in the communications field. He is presently a senior engineer at the Astro Electronics Division.

Insulator Physics

Dr. Richard Williams
RCA Laboratories
Princeton, New Jersey

This book, written in Portuguese, is based on a course offered to beginning graduate students of the department of physics at the *Escola de Engenharia*, Sao Carlos, Brazil. *Insulator Physics* treats several applications of insulators in current solid state electronics technology. Among the topics covered are photoconductors, schottky barriers, gate insulators, tunneling devices and cold-cathode devices. *(Special publication, Sao Carlos School of Engineering.)*

DR. RICHARD WILLIAMS received the AB from Miami University in 1950 and the PhD in Physical Chemistry from Harvard University in 1954. He served with the U.S. Army from 1954 to 1955 at the Army Chemical Center in Edgewood, Maryland. From 1955 to 1958 he was an instructor in Chemistry at Harvard University where he was engaged in investigations of the luminescence of organic molecules. In August 1958, he joined the Technical Staff of RCA Laboratories where his research has been focused on the studies of the photovoltaic effect, internal photoemission, electrical properties of insulators, and liquid crystals. He spent nine months in the Research Laboratory RCA, Ltd., in Zurich, Switzerland and served as a Fulbright Lecturer at *Escola de Engenharia*, Sao Carlos, Brazil. Dr. Williams has several publications to his credit and is a Fellow of the American Physical Society.

Handbook of Electronic Packaging

Donald P. Schnorr
(contributor)
Missile and Surface Radar Div.
Moorestown, N.J.

This handbook, edited by Charles A. Harper of Western Electric Corp., is the first to provide essential background material and step-by-step guidance on all aspects of modern electronic packaging. Mainly a professional reference for practicing engineers and designers, *Handbook of Electronic Packaging* is also an ideal reference to introduce new people to the field. It can also be used to provide production personnel with a better insight into electronic packaging. Mr. Schnorr contributed Chaper 1 entitled "Design and Application of Rigid and Flexible Printed Wiring." *(McGraw-Hill Book Co.; 948 pp., 929 illus.; price $29.50)*.

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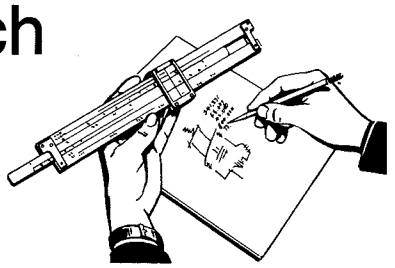
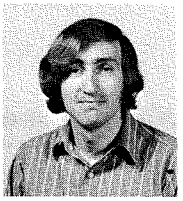
Engineering and Research Notes



Brief Technical Papers
of Current Interest

Solid-state pulse modulator



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Several semiconductor devices (such as transferred-electron devices, laser diodes, and avalanche diodes) require for their pulse applications and performance evaluation power sources of high current capability. Typical pulse currents range from 1 to 10 As, with pulse voltages of 50 to 150 V, and pulse widths from 0.5 to 10 μS. Such requirements have usually been met by large, high-power pulse generators with one or more power tubes in the final output stage. This note describes the design and construction of a compact solid-state pulse generator or modulator which adequately meets the above characteristics for laboratory experimentation and, with some modifications, could also meet specific product applications.

The modulator (Fig. 1) consists of the following stages: 1) a free running multivibrator Q_1 and Q_2; 2) a monostable multivibrator Q_3 and Q_4; 3) a two-stage emitter-follower amplifier Q_5 and Q_6; and 4) a power-amplifier output stage Q_7.

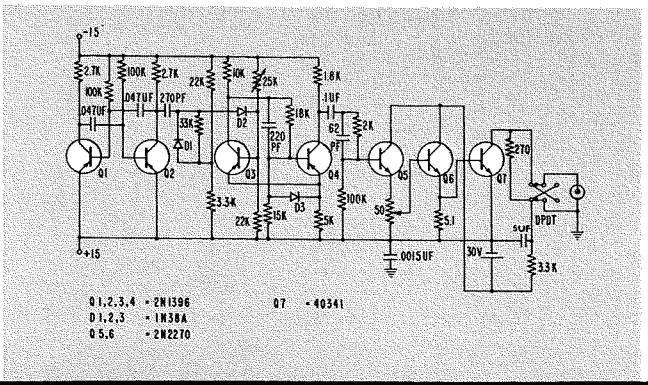
The free running multivibrator (Q_1 and Q_2) determines the pulse repetition rate, which for the prototype model has been set to 200 pulses/second. The RCA transistor 2N1396 has been chosen for Q_1 and Q_2.

The monostable multivibrator (Q_3 and Q_4) determines the pulse width; in the prototype, provisions have been made to vary this pulse width from 0.5 to 10 MS. The 2N1396 is also used for Q_3 and Q_4. This simple pulse train is sufficient for present laboratory investigations. For other applications with more elaborate pulse requirements, such as burst-pulse trains, additional stages can be added.

The emitter-follower amplifier (Q_5 and Q_6) provides the required driving power for the output stage, and because of its high input and low output impedance, also prevents undesirable loading effects on the multivibrator. The RCA transistor 2N2270 serves for Q_5 and Q_6.

The final pulse current and voltage requirements of the load circuit dictate the choice of the power output transistor. In its present form, the modulator is used in research and development work on anomalous avalanche diodes. For this application,

Fig. 1—Modulator schematic.



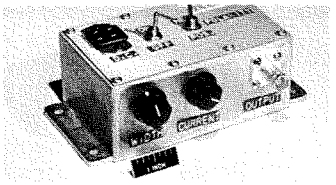


Fig. 2—Packaged modulator.

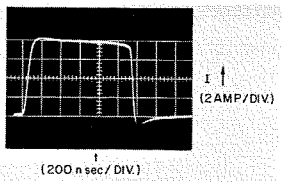


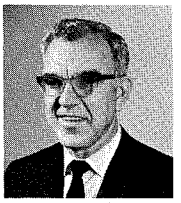
Fig. 3—Modulator wave shapes.

the diode is heavily driven into the avalanche region of the *I-V* characteristic until a pulse current of several amperes flows. The amount of pulse current basically depends on the requirements of the anomalous operating mode, and is controlled by the pulse drive to the output transistor. The RCA transistor 40341 combines the high current (10 A) requirement with adequate voltage ratings (80 V) and good high-frequency response (50 MHz). Fig. 2 is a photograph of the assembled modulator. Fig. 3 shows the current wave shape for a resistive load of 3 ohms. The rise and fall times of the pulse are 70 ns.

If higher power output pulses are needed, other output transistors may be used without further changes in the driving stages. It should also be noted that this modulator acts essentially as a constant current source, with the level of the current pulse controlled by the driving current (I_B) of the output stage.

Acknowledgment: the writer thanks A. S. Clorfeine, R. D. Hughes, and H. J. Prager for helpful discussions, and K. K. N. Chang for his encouragement.

Rotating Mirror Assembly



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Disclosed is a rotating mirror assembly for linearly swinging a beam of light through an angle without longitudinal or lateral translation, using a multiple faced mirror. The principle involved uses secondary reflection of the light beam from a stationary mirror. The device may be used in an ultralinear recorder, or flying-spot scanner with single or multiple channels or as a laser-beam deflector to scan a raster pattern.

An ordinary rotating multiple-faced mirror, which swings a focused beam of light through an angle, has a noncentric focal surface due to the fact that the mirror surface is translated as well as rotated, since the center of rotation is not in the plane of the mirror face. The rotating mirror assembly herein described has multiple faces each of which effectively rotates in the axis of the assembly, using a unique secondary reflection from a stationary mirror to prevent the detrimental effects of mirror face translation.

Assume a horizontal plane mirror, and place a second plane mirror above it, inclined at a 45° angle, as shown in Fig. 1. The reflection of the first in the second is now a vertical (virtual) mirror. If the inclined mirror is rotated about an axis which is normal to the first mirror and in the plane of the reflection of the first in the second (as in the device of Fig. 2) the effect, looking into the pair from any angle, is rotation only of the vertical (virtual) surface.

The number of facets on the rotating mirror may vary from a minimum of three to any practical high number. For three facets, the scan arc approaches 240°.

Fig. 1—Creation of vertical mirror in axis of rotation using secondary reflection.

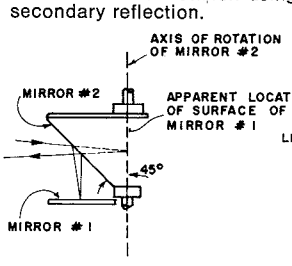
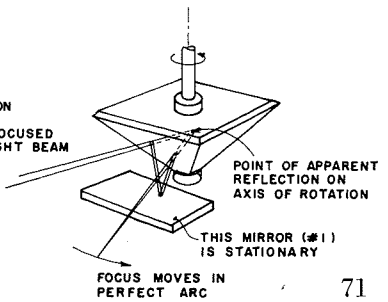


Fig. 2—Rotating assembly.



Zero-voltage-crossover gating sampler

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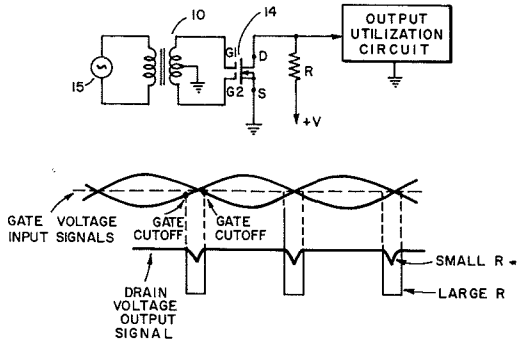

Fig. 1—Zero voltage crossover gating sampler.

An inexpensive circuit for obtaining a pulse output for the zero voltage crossover point of a sinusoidal or other type of repetitive signal is shown in Fig. 1.

A dual-gate metal-oxide semiconductor (MOS) field effect transistor (14) is driven by the secondary winding of a transformer (10).

The primary winding of the transformer is energized by a repetitive signal source, such as the signal from a sinusoidal oscillator (15). The secondary winding of the transformer, which has a grounded center tap, drives the gate electrodes, G1 and G2 of the MOS push-pull transistor (14). The circuit behaves as a cascade gate; and, as shown in the waveform schematics of Fig. 1, it produces an output, by current conduction from source to drain, only during the zero voltage crossover point of the sinewaves. This point is equivalent to zero gate-current bias for the MOS device.

The circuit can be used to synchronize an oscilloscope, trigger an SCR circuit, or, by placing integrating or differentiating circuits in series with the gate electrodes of the MOS device, to produce outputs representative of a plurality of different phases of such repetitive waveforms.

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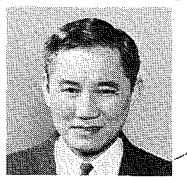
Integrated X-band parametric amplifier


Bura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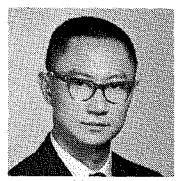
Yuan

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As previously reported[1,2] IC's have been successfully used in parametric amplifier design at *L*, *S* and *C*-band frequencies. Volume reduction of two orders of magnitude was achieved with no sacrifice in the amplifier performance. This paper reports an extension of the integrated parametric amplifier development to cover the *X*-band frequencies. The first phase was to develop the amplifier itself—leaving the circuit integration with a circular and a solid state, Gunn diode pump source for the second stage of the development.

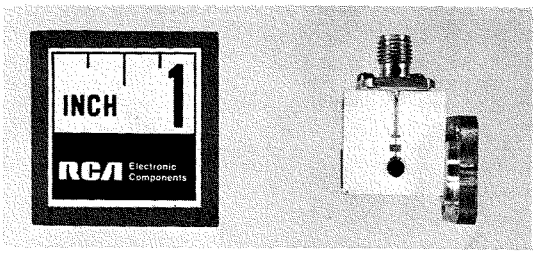

Fig. 1—Integrated X-band parametric amplifier.

The amplifier (Fig. 1) consisted of a shunt mounted, packaged varactor on a gold-alumina microstrip substrate. A *Ka*-band RG-96/u waveguide served both as the pump input and the base plate for the ceramic substrate.

The varactor was probe-coupled to the pump through a hole in the top wall of the waveguide. The waveguide height and width were reduced to facilitate power match to the varactor and to prevent idler frequency propagation by increasing the waveguide cutoff frequency. The pump power match to the varactor was achieved by a fixed waveguide short circuit placed slightly over a quarter of the pump wavelength beyond the varactor.

The signal circuit consisted of an OSM connector co-axial input and a two-section lowpass filter with the cutoff frequency 12 GHz. The varactor, at zero bias, was self-resonant at the signal frequency, so there was no need to provide additional tuning line elements.

The idler circuit consisted of the varactor itself plus a capacitive screw adjustment through the bottom wall of the pump waveguide. The idler frequency was isolated from the signal load by the lowpass filter and from the pump by the waveguide-beyond-cutoff section. Thus, no idler noise component could reach the varactor from those sources and the noise figure was not degraded. A gallium-arsenide diffused junction varactor in a standard pill package was used. Its cutoff frequency and junction capacitance at -6-V bias were 450 GHz and 0.3 pF, respectively. The pump frequency was 35 GHz and pump power for 13 dB gain at the signal frequency of 8 GHz was 80 mW. The 3 dB bandwidth was 90 MHz. The amplifier could be tuned over 300 MHz band either by varying the bias voltage or the pump frequency.

The amplifier noise figure, including 0.4 dB circulator insertion loss, was 2.5 dB. If circuit losses are neglected, the amplifier noise figure is given approximately by

$$F = 1 + \left(1 - \frac{1}{G}\right)\frac{(f_s/f_i)\ \beta + 1}{\beta - 1}$$

where
$\beta = (m_1 f_c)^2/f_s f_i$; m_1 = varactor elastance ratio; f_c = varactor cutoff frequency; G = power gain; f_s = signal frequency; and f_i = idler frequency.

For zero bias, $\beta = 22.9$ and the calculated noise figure becomes $F = 1.32 = 1.21\ dB$

The insertion loss of a lossless five-element lowpass filter is 0.1 dB, so the contribution to the noise figure by the total circuit loss is $\Delta F = 2.1 - 1.3 = 0.8$ dB. This is very similar to the noise figure degradation due to the circuit loss in co-axial and waveguide parametric amplifiers.

The important advantage in the use of the integrated circuitry is in the ease of fabrication, reproducibility and in the large reduction of the amplifier volume. The amplifier volume, without circulator and pump source, was only 0.1 cu. inches. It lends itself to a further system integration by incorporating the circulator and the Gunn diode pump source on the same substrate.

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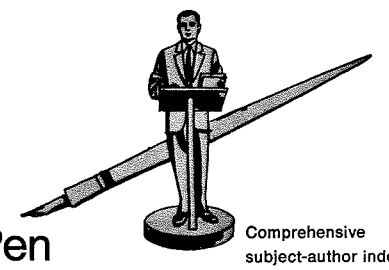

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TRANSMISSION LINES

DIRECTIONAL COUPLERS, Coplanar Waveguide—C. P. Wen (Labs, Pr) G-MTT Int, Microwave Symp.; Newport Beach, Calif.; 5/11-14/70

DUAL-CHANNEL ROTARY JOINT for High Power Operation—O. Woodward (MSR, Mrstn) 1970 IEEE GMTT Int Microwave Symp., Newport, Calif.; 5/11-14/70

TUBES, ELECTRON

POWER GENERATION, Tubes vs Solid-State Devices—L. S. Nergaard (Labs, Pr) Naval Research Laboratories; Washington, D.C.; 6/24/70

SILICON DIOXIDE STORAGE TUBE—R. Silver, E. Luedicke (Labs, Pr) *Proc. of the IEEE,* Vol. 58, No. 2; 2/70

TUBE COMPONENTS

TRAVELING-WAVE-TUBE Ceramic-Metal Seal Problems and Solutions—T. F. Berry (EC, Hr) Presented at American Ceramic Soc. Mtg.; Phila., Pa.; 5/6/70

Author Index

Subject listed opposite each author's name indicates where complete citation to his paper may be found in the subject index. An author may have more than one paper for each subject category.

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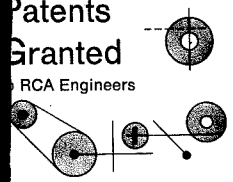
Chew, V. mathematics

Patents Granted

to RCA Engineers



s reported by RCA Domestic Patents, Princeton

DEFENSE COMMUNICATIONS SYSTEMS DIVISION

Digital Demodulator System—L. P. Nahay, B. E. Patrusky (DCSD, Camden) U.S. Pat. 3,514,702; May 26, 1970

Multiple Font Keyboard—T. C. Abrahamsen (DCSD, Camden) U.S. Pat. 3,517,792; June 30, 1970

Head Track Handling—J. Agin (DCSD, Camden) U.S. Pat. 3,518,625; June 30, 1970

ASTRO ELECTRONICS DIVISION

Frequency Shift Keyed Demodulator—S. Feitelbaum, C. Staloff (AED, Hightstown) U.S. Pat. 3,501,704; March 17, 1970; Assigned to U.S. Government

CONSUMER ELECTRONICS

Television Receiver Horizontal Deflection Output Stage Protection Circuit and Direct Voltage Supply—P. C. Wilmarth (GED, Indianapolis) U.S. Pat. 3,518,482; June 30, 1970

Color Killer and Automatic Chroma Control Circuits—D. H. Carpenter (CED, Indianapolis) U.S. Pat. 3,517,114; June 23, 1970

Automatic Chroma Control Circuit—D. H. Willis (CED, Indianapolis) U.S. Pat. 3,517,115; June 23, 1970

Voltage Regulator—W. F. W. Dietz (CED, Indianapolis) U.S. Pat. 3,517,253; June 23, 1970

Resonant Bandpass Filter Having Two Undesired Frequency Cancellation Traps—J. C. Marsh, Jr. (CED, Indianapolis) U.S. Pat. 3,519,737; July 7, 1970

Angle Modulation Discriminator-Detector Circuit—J. Avins (CED, Somerville) U.S. Pat. 3,519,944; July 7, 1970

ELECTRONIC COMPONENTS

Adaptive Diode Having Mobile Doping Impurities—R. B. Schilling (EC, Somerville) U.S. Pat. 3,515,953; June 2, 1970; Assigned to U.S. Government

Field-Effect Transistor Amplifier—D. J. Carlson (EC, Somerville, N.J.) U.S. Pat. 3,513,405; May 9, 1970

Photographic Method for Making Tri-Colored Cathode Ray Screen—D. J. Donahue, A. E. Hardy (EC, Lancaster, Pa.) U.S. Pat. 3,514,287; May 26, 1970

Method of Fabricating Semiconductor Devices—E. T. Casterline, R. Rosenzweig (EC, Somerville) U.S. Pat. 3,513,022; May 19, 1970; Assigned to U.S. Government

RF Power Amplifier—C. B. Leuthauser (EC, Somerville) U.S. Pat. 3,513,406; May 19, 1970

Protective Apparatus for a Super-Conductive Switch—H. C. Schindler, J. J. Drautman (EC, Harrison) U.S. Pat. 3,513,-421; May 19, 1970

Microwave Circuit with Coaxial Package Semiconductor Device—H. C. Lee, G. Hodowanec (EC, Somerville) U.S. Pat. 3,517,272; June 23, 1970

Photomasks for Fabrication of Semiconductor Devices—J. L. McLaughlin (EC, Somerville) U.S. Pat. 3,519,348; July 7, 1970

Regulated High Voltage Power Supply—M. B. Knight (EC, Somerville) U.S. Pat. 3,519,741; July 7, 1970

Photoconductive Pickup Tube Having Opaque Gold Pattern Excapsulated in Tin Oxide Layer—J. R. Leaman (EC, Lancaster) U.S. Pat. 3,519,866; July 7, 1970; Assigned to U.S. Government

Radiation Resistant Silicon Semiconductor Devices—J. J. Wysocki (EC, Lancaster) U.S. Pat. 3,490,965; January 20, 1970; Assigned to U.S. Government

LABORATORIES

Multi-Layer, Light-Emitting Semiconductor Device—W. F. Kosonocky (Labs., Princeton, N.J.) U.S. Pat. 3,514,715; May 26, 1970; Assigned to U.S. Government

Screening Unit for Half-Tone Color Reproduction—S. W. Johnson, M. A. Leedom (Labs., Princeton, N.J.) U.S. Pat. 3,517,596; June 30, 1970

Electrophotographic Apparatus—M. A. Leedom (Labs., Princeton, N.J.) U.S. Pat. 3,517,994; June 30, 1970

Deflection Yoke and Apparatus for its Fabrication Utilizing Magnetic Ramming Technique—J. Gross, W. H. Barkow (Labs., Princeton, N.J.) U.S. Pat. 3,518,-590; June 30, 1970

Coupling System for Elemental Panel Array—J. E. Meyer, Jr. (Labs, Princeton, N.J.) U.S. Pat. 3,518,627; June 30, 1970; Assigned to U.S. Government

Adaptive Diode Having Mobile Doping Impurities—C. Dobin (Labs., Princeton, N.J.) U.S. Pat. 3,515,953; June 2, 1970; Assigned to U.S. Government

Signal Translating Circuit Comprising a Plurality of IGFET Amplifiers Cascaded in Direct Coupled Fashion—J. R. Burns (Labs., Princeton, N.J.) U.S. Pat. 3,516,-004; June 2, 1970

Apparatus for Forming a Beam of Light—W. J. Gorkiewicz, J. Wilder (Labs., Princeton, N. J.) U.S. Pat. 3,512,868; May 19, 1970

Field Effect Transistor with Improved Insulative Layer between Gate and Channel—F. P. Heiman (Labs., Princeton, N.J.) U.S. Pat. 3,513,364; May 19, 1970; Assigned to U.S. Government

Integrated Semiconductor Structure with Frequency Selective Transmission Line Sections—K. K. N. Chang (Labs., Princeton, N.J.) U.S. Pat. 3,513,403; May 19, 1970

Method of Making Gunn-Effect Devices—L. E. Norton (Labs., Princeton, N.J.) U.S. Pat. 3,518,749; July 7, 1970

Turnoff Method and Circuit for Liquid Crystal Display Element—G. H. Heilmeier (Labs., Princeton, N.J.) U.S. Pat. 3,519,330; July 7, 1970

Threshold Gate Counters—R. O. Winder (Labs., Princeton, N.J.) U.S. Pat. 3,519,-941; July 7, 1970

Radiation-Sensing Matrix Circuit—D. H. Vilkomerson (Labs., Princeton, N.J.) U.S. Pat. 3,519,996; July 7, 1970; Assigned to U.S. Government

INFORMATION SYSTEMS

Magnetic Memory with Noise-Cancellation Sense Wiring—F. D. Cassidy (CSD, Needham, Massachusetts) U.S. Pat. 3,518,640; June 30, 1970

Weighted Time Accounting in Time-Shared Computer—J. E. Croy (CSD, Cherry Hill, N.J.) U.S. Pat. 3,518,633; June 30, 1970

Balanced Mixer Circuits—B. B. Bossard, S. Yuan (CSD, New York) U.S. Pat. 3,513,398; May 19, 1970; Assigned to U.S. Government

COMMERCIAL ELECTRONIC SYSTEMS

Arrangement for Handling Printable Character Bit Codes—R. C. Peyton (CES, Palm Beach, Florida) U.S. Pat. 3,517,165; June 23, 1970

Apparatus for Previewing Slides—W. F. Schacht, W. F. Fisher (CES, Camden, U.S. Pat. 3,514,198; May 26, 1970

Modulation Error Cancelling Apparatus—J. J. O'Toole (CES, Camden, N.J.)

Preset Sensitivity and Amplification Control System—R. R. Brooks (CES, Camden, N.J.) U.S. Pat. 3,518,371; June 30, 1970

Push-Pull Current Source—D. C. Herrmann, J. L. Bazin (CES, Camden, N.J.) U.S. Pat. 3,518,457; June 30, 1970

GRAPHIC SYSTEMS DIVISION

Device for Producing Line Halftone Images Similar to the Images Produced by the Woodcut Type Method of Printing—R. J. Klensch (GSD, Dayton, N.J.) U.S. Pat. 3,517,119; June 23, 1970

Portable Color Television Camera System—A. J. Gravel (GSD, Dayton, N.J.) U.S. Pat. 3,518,360; June 30, 1970

DEFENSE ENGINEERING

Apparatus for Preventing Receiver Recording of Partial Multiplexed Message Transmissions—D. P. Dorsey (ATL, Camden, N.J.) U.S. Pat. 3,519,736; July 7, 1970

Pushbutton Mechanism—H. J. Mackway (ATL, Camden, N.J.) U.S. Pat. 3,519,766; July 7, 1970

Magnetic Core Memory Plane Assembly and Method—R. S. Fow (ATL, Camden, N.J.) U.S. Pat. 3,513,453; May 19, 1970

NATIONAL BROADCASTING COMPANY, INC. RECORD DIVISION

Tape Basket Stripper Apparatus—C. G. Hawkins (Record Div., Indianapolis, Ind.) U.S. Pat. 3,514,024; May 26, 1970

Professional Meetings

Dates and Deadlines

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

Calls for Papers

OCT. 28-30, 1970: **1970 IEEE International Electron Devices Meeting,** Sheraton-Park Hotel, Washington, D.C., IEEE Electron Devices Group. **Deadline info: (abst) 7/1/70 (late news abst) 9/15/70 to:** Edward O. Johnson, Program Chairman, 1970 International Electron Devices Meeting, RCA Corporation, Electronic Components, 415 South Fifth Street, Harrison, New Jersey 07029.

JAN. 19-21, 1971: **1971 Mexico International IEEE Conference on Systems, Networks and Computers,** Oaxtepec, Mor., Mexico, Region 9 and Mexico Section of IEEE. **Deadline info: (three copies of one page, single spaced abst) 8/31/70 to:** Dr. Roberto Canales R., Instituto de Ingenieria, Ciudad Universitaria, Mexico 20, D. F., Mexico.

JAN. 31-FEB. 5, 1970: **Winter Power Meeting,** Statler Hilton Hotel, New York, N.Y., G-P. **Deadline info: (papers) 9/15/70 to:** IEEE Hdqs., Tech. Conf. Svcs., 345 E. 47th St., New York, N.Y. 10017.

APRIL 18-21, 1970: **Off-Shore Technology Conference,** Houston, Texas, TAB Oceanography Coordinating Committee et al. **Deadline info: (abst) 10/1/70 to:** IEEE Hdqs., 345 E. 47th St., New York, N.Y. 10017.

MAY 10-14, 1971: **Symposium on Flow—Its Measurement and Control in Science and Industry,** William Penn Hotel, Pittsburgh, Pa., AIAA, AIP, ASME, ISA, and Nat. Bureau of Standards. **Deadline info: (abst) 9/1/70 (ms) 3/1/71 to:** Program Chairman, Prof Rodger B. Dowdell, College of Engineering, University of Rhode Island, Kingston, R.I. 02881.

MAY 11, 12, 13, 1971: **Engineering for Conservation of Mankind,** Wood Lake Inn, Sacramento, California, IEEE. **Deadline info: (abst 12/1/70 (ms) 3/1/71 to:** Dr. D. H. Gilot, Program Co-Chairman, IEEE Region 6 Conference, Sacramento State College, Dept. of Electrical Engineering, 6000 Jay Street, Sacramento, California 95819 and Dr. R. F. Soohoo, Program Chairman, IEEE Region 6 Conference, University of California at Davis, Dept. of Electrical Engineering, Davis, California 95616.

Meetings

SEPT. 20-25, 1970: **Intersociety Energy Conversion Engineering Conference,** Frontier Hotel, Las Vegas, Nev., G-ED, G-AES, AIAA, ASME, AIChE et al. **Prog info:** A. J. Smith, AFWL (WLAS 3/A), Kirtland AFB, New Mexico 87117.

SEPT. 21-24, 1970: **Int'l Conf. on Engineering in the Ocean Environment,** City Marina Aud., Panama City, Fla., TAB Oceanography Coordinating Committee, et al. **Prog info:** C. B. Koesy, Code P 750, Naval Ship R & D Lab., Panama City, Florida 32401.

SEPT. 21-23, 1970: **The Technology of Pressure Retaining Steel Components,** Vail, Colorado, AIME. **Prog info:** The Metals Engineering Division, The American Society of Mechanical Engineers, United Engineering Center, 345 East 47th Street, New York, New York 10017.

SEPT. 23-24, 1970: **Electron Device Techniques Conference,** United Engrg. Ctr., New York, N.Y., G-ED. **Prog info:** Mayden Gallagher, Hughes Res. Labs., 3011 Malibu Canyon Rd., Malibu, Calif. 90265.

SEPT. 24-26, 1970: **Fall Broadcast Tech. Symposium,** Washington Hilton Hotel, Washington, D.C., G-B. **Prog info:** IEEE, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

SEPT. 27-30, 1970: **Jt. Power Generation Conference,** Pittsburgh Hilton Hotel, Pittsburgh, Penna., G-P, ASME. **Prog info:** W. S. Morgan, Am. Elec. Pwr. Svc. Corp., 2 Bdwy., New York, N.Y. 10008.

SEPT. 29-OCT. 2, 1970: **Conference on Trunk Telecommunications by Guided Waves,** London, England, IEE, IEEE, UKRI Section, IERE. **Prog info:** IEE Office, Savoy Place, London W.C. 2 England.

OCT. 4-9, 1970: **108th SMPTE Technical Conference and Equipment Exhibit,** New York Hilton Hotel, New York, SMPTE. **Prog info:** Herbert Pilzer, Motion Picture Enterprises, Tarrytown, N.Y.

OCT. 5-7, 1970: **1970 Symposium on Feature Extraction and Selection in Pattern Recognition,** Argonne National Laboratory, Argonne, Illinois, IEEE. **Prog info:** Prof. K. S. Fu, School of Electrical Engineering, Purdue University, Lafayette, Indiana 47907 and Mr. A. Hamburgen, IBM Corporation, 3605 Highway 52 North, Rochester, Minnesota 55901.

OCT. 5-7, 1970: **UMR—Mervin J. Kelly Communications Conf.,** Univ. of Missouri, Rolla, Missouri, G-IT, Univ. of Missouri, St. Louis Section. **Prog info:** J. R. Betten, Univ. of Missouri, 123 EE Bldg., Rolla, Missouri 65401.

OCT. 5-8, 1970: **IGA Group Annual Meeting,** LaSalle Hotel, Chicago, Illinois, G-IGA. **Prog info:** A. M. Killin, 3916 Edgewater Dr., Ashtabula, Ohio 44004.

OCT. 6-8, 1970: **1970 IEEE Electromagnetic Compatibility Regional Symposium,** El Tropicano Motor Hotel, San Antonio, Texas, The Central Texas IEEE Section through its Electromagnetic Compatibility Group Chapter with the participation of The IEEE Group on Electromagnetic Compatibility (G-27) and SWIEEECO. **Prog info:** Carl C. Lambert, Program Chairman, The Electro-Mechanics Company, P.O. Box 1546, Austin, Texas 78767.

OCT. 7-9, 1970: **Allerton Conference on Circuit & Systems Theory,** Univ. of Illinois, Monticello, Ill., G-CT, G-AC, Univ. of Illinois. **Prog info:** G. Metze, Univ. of Illinois, Urbana, Illinois 61801.

OCT. 14-16, 1970: **Systems Science & Cybernetics Conference,** Webster Hall Hotel, Pittsburgh, Penna., G-SSC. **Prog info:** R. A. Mathais, Westinghouse R&D, Pittsburgh, Penna. 15235.

OCT. 21-23, 1970: **Ultrasonics Symposium,** Jack Tar Hotel, San Francisco, Calif., G-SU. **Prog info:** W. J. Spencer, Bell Telephone Labs., 555 Union Blvd., Allentown, Pa. 18103.

OCT. 23, 1970: **The End of Communicating: The Impact of Technology,** Boston University's Sherman Union, Boston Chapter, Society of Technical Writers and Publishers. **Prog info:** Mr. Charles Urbon, The MITRE Corporation, P.O. Box 208 (D-140), Bedford, Massachusetts 01730.

OCT. 26-28, 1970: **Electronic & Aerospace Systems Convention,** Sheraton Park Hotel, Washington, D.C., G-AES. **Prog info:** Richard Marsten, NASA Hdqs., Code SC, Washington, D.C. 20546.

OCT. 28-30, 1970: **Switching & Automata Theory Symposium,** Miramar Hotel, Santa Monica, Calif., G-C., Univ. of Calif. **Prog info:** IEEE Office, Technical Activities Board, 345 East 47th Street, New York, N.Y. 10017.

OCT. 29-30, 1970: **Joint Engineering Management Conference,** Drake Hotel, Chicago, Illinois, G-EM, 8 other societies. **Prog info:** AIEE Headquarters, 345 E. 47th St., New York, N.Y. 10017.

Engineering News and Highlights

Edward O. Johnson appointed Manager, Solid State Optoelectronics

William C. Hittinger, Vice President and General Manager, Solid State Division, has appointed Edward O. Johnson as Manager of the newly-formed Solid State Optoelectronics Products activity. In this new position Mr. Johnson will be responsible for directing the development, engineering, production and marketing of all solid state optoelectronic products manufactured by the Solid State Division. These products now include non-coherent and coherent infrared diodes and arrays, photocells, liquid crystal devices and tunnel diodes.

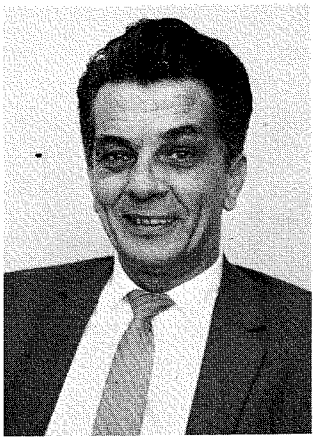
"The newly-formed Solid State Optoelectronics Products activity has been created by consolidating a number of RCA optoelectronic activities to add greater emphasis to the company's role in this field," according to Mr. Hittinger. "In addition, this consolidation will enable RCA to take a more active position in the solid state optoelectronic industry than the company has in the past. RCA has been a pioneer in the development of optoelectronics materials and products for many years," he added.

Prior to this appointment Mr. Johnson was Manager, Engineering, Technical Programs, for RCA Electronic Components since 1963. He received the BSEE from Pratt Institute. He also undertook PhD courses at Princeton University and at the Swiss Federal Institute of Technology. In 1948 he joined RCA Laboratories at Princeton, N. J. and became Manager, Electron Device Research, in 1957. He transferred to the RCA Semiconductor and Materials Division in 1959, as Manager, Advanced Development, and in 1961 was appointed Chief Engineer. He is a fellow of the IEEE, the holder of fifteen patents, and the author of 20 technical papers. A co-recipient of the IEEE Editors' Award, he has also received two RCA Achievement Awards. He is listed in "Who's Who In Engineering".

Mr. Johnson has managed a number of IEEE Solid State Circuits Conferences and is presently technical program chairman for the 1970 IEEE International Electron Devices Meeting. He is also a member of the U. S. Department of Commerce Technical Advisory Board Panel on Electrically Powered Vehicles.

William Ragan is Chief Engineer of Magnetic Products Division

Dr. William A. Ragan has been appointed Chief Engineer of the Magnetic Products Division. Dr. Ragan received the PhD in organic chemistry from the University of Notre Dame; his career for the past 20 years has been one of proven accomplishment with E. I. DuPont de Nemours. At DuPont, Dr. Ragan had technical responsibility for all packaging film research and the development of such products as "Nylon", "Mylar", "Vexar", "Clysar", "Kapton", polyolefin film, and associated structures. Dr. Ragan's experience with the chemistry of films, design and operation of production lines for the movement of film, etc., has a direct relationship to Magnetic Products' type of operation.



P. K. White

Paul White named Chief Engineer, Memory Products Division

Paul K. White recently joined RCA as Chief Engineer of the Memory Products Division in Needham, reporting to Steven P. Marcy, Division Vice President and General Manager. He comes to RCA after 18 years with General Electric. One of his most significant accomplishments within those 18 years was the development of Magnetic Film Memory technology in Phoenix, Arizona. Mr. White started his successful career with General Electric after receiving the BEE from Rensselaer Polytechnic Institute, where he was a member of the honorary societies, HKN and TBP.

Promotions

Electronic Components

P. G. Bedrosian: from Engr., Product Development to Mgr., Standardizing (H. A. Kauffman, Lancaster)

P. D. Strubhar: from Engr. Ldr, Product Dev., to Mgr., Chemical & Physical Lab. (R. H. Zazhariason, Lancaster)

Solid State Division

R. E. Brown: from Ldr., Product Development to Mgr., Engineering Standards (M. Bondy, Somerville)

C. Horsting: from Sr. Engr., Product Development to Engrg. Ldr., Product Development (M. Bondy, Somerville)

Dr. J. C. Miller: Engrg. Ldr., Product Development to Mgr., Design Automation and Advanced Test Technology (B. Jacoby, Somerville)

Computer Systems Division

E. Fulcher from Sr. Mbr., D & D Engr Staff to Ldr., Technical Staff (H. N Morris, West Palm Beach, Fla.)

K. Hoffman from Sr. Mbr., D & D Engr Staff to Ldr., Technical Staff (H. N Morris, West Palm Beach, Fla.)

J. LeGault from Sr. Mbr., D & D Engr Staff to Mgr., Automated Design Ope ations (H. N. Morris, West Palm Beac Fla.)

J. Leise: from Sr. Mbr., D & D Engr Staff to Ldr., Tech. Staff (H. N. Morri West Palm Beach, Fla.)

W. L. Schulte: from Mbr., Engrg. Sta to Sr. Mbr., D & D Engrg. Staff (H. N Morris, West Palm Beach, Fla.)

R. Singleton: from Pr. Mbr., D & Engrg. Staff to Ldr., Tech. Staff (H. N Morris, West Palm Beach, Fla.)

W. D. White: from Mbr., Engrg. Staff t Sr. Mbr., D & D Engrg. Staff (H. N Morris, West Palm Beach, Fla.)

Missile & Surface Radar Division

J. Daglian from Engr. to Ldr. D & D Radiation Equipment (P. Levi, Moores town, New Jersey)

E. B. Darrell: from Ldr. Field Support t Mgr., Equip. D & D (W. Perecinic Moorestown)

J. D. Frattura from Engr. to Ldr. ESP Tactical Systems (C. C. Botkin, Moores town, New Jersey)

H. Geyer: from Ldr. ESP to Mgr TRADEX Site (L. Nelson, Moores town)

J. F. Hawkins: from Sr. Prog. Cont. t Engr. (E. T. Hatcher, Moorestown)

D. D. Keys from Engr. to Ldr. ESP, Tech nical Assurance (G. R. Field, Moores town, New Jersey)

B. Matulis from Engr. to Ldr., T/M Comp., Product Design (W. Perecinic Moorestown, New Jersey)

M. Nowlan from Engr. to Ldr., Enginee ing System Projects (H. Grossman Moorestown, New Jersey)

S. M. Paskow from Ldr. to Mgr., FPS-9 Site (N. Lesso, Moorestown, New Jer sey)

W. T. Patton from Ldr. D & D to Mgr Equip. D&D, Product Design (W. Per cinic, Moorestown, New Jersey)

G. A. Senior from Ldr. D & D to Mg Equip. D & D, Product Design (W Perecinic, Moorestown, New Jersey)

J. M. Sommerville from Ldr. to Mgr Range Operations Programs (J. M. Se igman, Moorestown, New Jersey)

E. Zarnoch from Engr. to Ldr., D & Engineers (G. A. Senior, Moorestown New Jersey)

Commercial Electronic Systems

W. E. Bauer: from Engr. to Ldr., Des. Dev. Engrgs. (R. J. Smith, Camden)

CA Service Company

J. Lobe: from Engr. to Mgr., Marketing District. (G. E. Pinkston, Mktg., Cocoa Beach, Fla.)

G. Commean: from Engr., Systems Service to Ldr., Systems Service Engrgs. (W. R. Hayford, Sanguine Project, Clam Lake, Wisconsin)

Awards

Aerospace Systems Division

Morris Z. Neiman, of Electro-Optics & Controls Engineering has been selected as Engineer of the Month for March for his outstanding work on the Huey Cobra program. Mr. Neiman provided technical direction to a major aircraft subcontractor for the purpose of modifying three aircraft to accept the entire Huey Cobra system.

The Pulse Doppler Radar team of **R. Carter, R. dePierre, D. W. Fogg, J. B. Fuller, N. G. Hamm, J. I. Herzlinger, H. Honda, J. D. Johnson, M. J. Kurina, J. A. Michitson, J. S. Newell, K. T. Konan, J. A. Shay, P. T. Tremblay,** and **G. J. Zerfas** from RF Engineering has been selected for a Team Award for March. On a fixed price contract, the Pulse Doppler Radar system was completed within the contract schedule and authorized funding. The system is a tail-warning radar applicable to SAC and TAC aircraft for detecting missiles and other aircraft to take protective action.

William P. McDonald of Systems Development and Applications, has been selected as Engineer of the Month for April for his work in simulating the effectiveness of the Pulse Doppler Radar in aiding in the protection of tactical and strategic aircraft. The purpose of the simulation was to evaluate the need for a tail-warning radar and determine the performance which this radar must provide to help protect aircraft.

George J. Lamonakis of System Design Support has been selected as the Engineer of the Month for May for his outstanding work in conducting environmental shock and vibration tests on the LCSS Source Detector Adapter. The test program required the design and implementation of modifications of existing test fixtures to accommodate the complex test specimen, to provide adequate stiffening and ballast and to accept an adequate vibration driving technique.

The LLLTV team of **Frank R. Amand, David A. French, R. James Gildea, Jr., Olof C. Johnson, Jr., Edwin W. Ketler, Kenneth M. Knowles, Ronald P. Larson,** and **Richard G. Popvich** from Electro-Optics and Controls Engineering was selected for a Team Award for May. The award recognizes the outstanding Team effort in the development of the low light level television system for the Huey Cobra aircraft. The program required a design using the RCA silicon image tube in place of the SEC tube used in earlier camera system designs. To meet a 4-month delivery schedule the camera design team drew heavily on the TRIM and other similar camera designs.

Astro-Electronics Division

Kevin J. Phillips of the Advanced Development Activity has been selected as the most recent recipient of the Engineering Excellence Award. He was selected for this award as a result of his outstanding work in the analysis of the stability of the TIROS-M Satellite.

Professional activities

Aerospace Systems Division

Barry A. Bendel has been elected to the Executive Committee of the Merrimack Valley subsection of the IEEE. He will serve as membership and attendance chairman for the 1970-71 season.

Astro-Electronics Division

M. H. Mesner has been awarded Knighthood in the Guard of St. Patrick (*summa cum laude*) by the University of Missouri College of Engineering student body.

J. D'Arcy has just completed one year's service as President, Junior's Organization of the Engineer's Club of Philadelphia, Pa.

W. J. Hawkins won the first prize of $20,000 in the *Popular Science* magazine "Anti-Car-Theft Device" competition, sponsored by the Allstate Insurance Co.

Graphic Systems Division

R. M. Carrell has accepted an invitation to assume chairmanship of the Quality Subcommittee of the National Microfilm Association's Computer on Microfilm Standards Committee.

Defense Electronic Products

Joseph G. Mullen has been elected President of the William Penn Chapter of the Association of the United States Army (AUSA) which is a voluntary, non-profit organization composed of individuals devoted to advancing the aims of the U.S. Army and the security of the United States.

RCA Laboratories

G. Kenneth Dye has won a Certificate of Merit for his manuscript, "Casting Up a Projection" in the annual manuscript competition of the National Association of Accountants.

Research and Engineering

Arthur N. Curtiss, Staff Vice President, Administration, received a Certificate of Special Recognition at the recent annual meeting of the Armed Forces Communications and Electronics Association in Washington, D.C. Mr. Curtiss, one of five National Directors of the AFCEA, was honored for his service during the past eight years.

Staff announcements

Operations Staff

Chase Morsey, Jr., Vice President, Marketing has appointed **Joseph W. Curran** in addition to his continuing responsibility as Staff Vice President, Advertising and Sales Promotion, to assume responsibility, in an acting capacity, for the direction of the Corporate Staff Product and Marketing Planning activity; **Stephen Russell** as Staff Vice President, Operations Staff Administration; and **Richard W. Sonnenfeldt,** Staff Vice President, responsible for special projects and studies in the field of communications.

Degrees granted

A. G. F. Dingwall, SSD, Som. ..... MSEE, Brooklyn Polytechnic Inst; 6/70
E. L. Lattanzio, SSD, Som. ..... MSEE, Newark College of Engineering; 6/70
S. D. Smith, AED, Pr. ..... BSEE, Newark College of Engineering; 6/70
A. Cohen, M&SR, Mrstn. ..... BS, Physics Electronics, La Salle; 6/70
A. D. Korbin, M&SR, Mrstn. ..... PhD, University of Pennsylvania; 6/70
T. Murakami, AEGIS, Mrstn. ..... PhD, University of Pennsylvania; 6/70
G. A. Sparks, M&SR, Mrstn. ..... PhD, University of Pennsylvania; 6/70
H. P. Schiefer, EC, Lanc. ..... MS, Physics, Franklin & Marshall; 6/70
E. L. McHugh, AED, Pr. ..... BS, Physics, La Salle; 6/70
J. C. Phillips, CES, Cam. ..... BA, Mathematics, Rutgers; 6/70
G. Beakley, Labs, Pr. ..... PhD, Comm. Theory, Yale; 6/70
C. Catanese, Labs, Pr. ..... PhD, Physics, Yale; 6/70
G. Chandler, Labs, Pr. ..... PhD, Univ. of Illinois; 2/70
J. Davy, Labs, Pr. ..... PhD, Univ. of California; 6/70
L. Goodman, Labs, Pr. ..... PhD.EE, MIT; 6/70
W. Ham, Labs, Pr. ..... PhD.EE, Southern Methodist Univ; 5/70
T. Hitch, Labs, Pr. ..... PhD, Materials Eng, Rensselaer Polytechnic Inst.; 5/70
H. Kawamoto, Labs, Pr. ..... PhD.EE, Univ. of California; 3/70
M. Kovac, Labs, Pr. ..... PhD.EE, Northwestern University; 6/70
A. Levine, Labs, Pr. ..... PhD, Seton Hall University; 5/70
S. Kipp, Labs, Pr. ..... PhD, Chemistry, Univ. of California; 3/70
C. Oh, Labs, Pr. ..... PhD, Organic Chemistry, St. John's University; 6/70
A. Sigai, Labs, Pr. ..... PhD, Rensselaer Polytechnic Inst; 1/70
H. Wasserman, Labs, Pr. ..... PhD, University of Pennsylvania; 12/69
R. A. Dallitis, Globcom, N.Y. ..... BSEE, New York Institute of Technology; 6/70
D. G. Epstein, Globcom, N.Y. ..... MSEE, New York University; 2/70

R. C. Bitting, Staff Vice President, SelectaVision Business Development has announced the organization of SelectaVision Business Development as follows: **H. Ball,** Director, Systems Development; **F. X. Conaty,** Manager, Administration and Controls; **D. I. Brenner,** Administrator, Program Controls; **D. F. Miller,** Director, Marketing; **R. C. Bitting,** Acting Director, Business Planning.

Thomas J. Mc Dermott, Staff Vice President, Special Projects for SelectaVision, has appointed **Anthony D. Thomopoulus** as Manager of SelectaVision Programs. In his new position, Mr. Thomopoulus will negotiate programming contracts, acquire talent, and develop a film library for SelectaVision, RCA's new color television playback system.

Research and Engineering

Edward W. Herold, Director, Technology, has appointed **Harold Sobol** Staff Engineer, Technology.

RCA Laboratories

Kerns H. Powers, Director, Communications Research Laboratory has appointed **Henry Tan,** Head, Cable Systems Research.

Solid State Division

William C. Hittinger, Vice President and General Manager, has appointed **Edward O. Johnson,** Manager, Solid State Optoelectronic Products.

D. Joseph Donahue, Manager, Solid State Department, has announced the organization of the Solid State Department as follows: **Melvin Bondy,** Manager, Technology and Engineering Services; **Robert M. Cohen,** Manager, Quality and Reliability Assurance; **D. Joseph Donahue,** Acting Manager, Marketing Services; **Paul Greenberg,** Manager, Somerville Services; **Robert L. Klem,** Manager, Solid State Signal Marketing; **John P. McCarthy,** Manager, Solid State Power Operations; **Roy H. Pollack,** Manager, Solid State Signal Operations; **Parker T. Valentine,** Manager, Solid State Power Marketing.

Electronic Components

John F. Wilhelm, Manager, Commercial Engineering has appointed **Eleanor M. McElwee** Manager, Solid State Power Devices—Commercial Engineering.

C. Price Smith, Manager, Power & Electro-Optics Products Department has announced the organization of Power & Electro-Optics Products as follows: **William T. Kelley,** Manager, Power & Electro-Optics Services; **Robert T. Rihn,** Administrator, Special Projects; **Ralph E. Simon,** Manager, Electro-Optics Products; **C. Price Smith,** Acting Manager, Power Products.

William T. Kelley, Manager, Power & Electro-Optics Services has announced the organization of Power & Electro-Optics Services as follows: **James W. Kiehl,** Manager, Facilities Planning; **Charles Hanlon,** Administrator, Services; **D. Franklin Herr,** Administrator, Power Products, **Walter W. Houck,** Administrator, Electro-Optics Products; **Douglas Williams,** Administrator, Facilities; **Harry B. Walton,** Administrator, Operations Planning; **Donald G. Kann,** Administrator, Planning.

Ralph E. Simon, Manager, Electro-Optics Products has announced the organization of Electro-Optics Products as follows: **Clarence H. Groah,** Administrator, Electro-Optics Products Administration; **J. Kenneth Johnson,** Manager, Camera & Display Tube Operations; **Ralph E. Simon,** Manager (acting), Advanced Technology.

C. Price Smith, Acting Manager, Power Products has announced the organization of Power Products as follows: **Leonard W. Grove,** Manager, Regular Power & Laser Operations; **Robert E. Reed,** Manager, Power Products Engineering, **Merrald B. Shrader,** Manager, Advanced Development, **Thomas E. Yingst,** Manager, Super Power Operations.

Merrald B. Shrader, Manager, Advanced Development, has announced the organization of Advanced Development, Power Products, as follows: **Wilford P. Bennett,** Engineering Leader, Product Development; **G. Yale Eastman,** Engineering Leader, Product Development; **Robert Roth,** Manager, Development Shop.

Leonard W. Grove, Manager, Regular Power & Laser Operations has announced the organization of Regular Power and Laser Operations as follows: **John T. Mark,** Manager, Regular Power Products Design Engineering; **Herbert W. Sawyer,** Superintendent, Regular Power Products; **William M. Sloyer,** Superintendent, Regular Power Products.

Robert E. Reed, Manager, Power Products Engineering, has announced the organization of Power Products Engineering as follows: **Claude E. Doner,** Engineering Leader, Product Development; **John R. Eshbach,** Manager, Electrical Equipment Construction & Maintenance; **Jerome J. Free,** Engineering Leader, Product Development.

Thomas E. Yingst, Manager, Super Power Operations, has announced the organization of Super Power Operations as follows: **Thomas E. Yingst,** Acting Manager, Super Power Design Engineering; **Thomas E. Yingst,** Acting Administrator, Super Power Products Administration.

Graphic Systems Division

Gerard O. Walter, Chief Engineer, has appointed **Robert S. Eiferd,** Manager, Font Development.

N. Richard Miller, Division Vice President and General Manager, has appointed **David Meredith,** Manager, Programming Development.

David Meredith, Manager, Programmi Development, has appointed **T. Albe Korn,** Manager, Systems.

Astro-Electronics Division

Abraham Schnapf, Manager of Progra Management has appointed **H. L Schwartzberg,** Manager, Improved TIRO Operations System (ITOS) satellite pr gram. Mr. Schwartzberg will be respo sible for the design, development an production of the ITOS weather sate lites.

Abraham Schnapf, Manager of Progra Management has appointed **Robert Mille** Manager, Nimbus Project. Mr. Miller wi have overall responsibility for electron equipment and subsystems being deve oped at AED for the Nimbus exper mental meteorological satellite.

Aerospace Systems Division

John R. McAllister, Division Vice Pres dent and General Manager has appointe **William H. Price, II,** as Manager, Arm Weapons Systems Sales. Mr. Price will b responsible for the marketing of Arm related systems at the Burlington Div sion. He will report to **George A. Earle** Manager, Marketing.

Consumer Electronics

Robert A. Schieber, Division Vice Presi dent, Operations, has appointed **Loren K Kirkwood,** Chief Technical Advisor. I this capacity, Mr. Kirkwood will assis management in the development and ap plication of technical advances in the fiel of Consumer Electronics.

Robert A. Schieber, Division Vice Pres dent, Operations, has appointed **Marvi H. Glauberman,** Chief Engineer, Eng neering Department.

RCA personnel active in IEEE Chapte on Reliability

Several engineers of the Defense Com munications Systems Division are makin significant contributions to the Philade phia Chapter of the IEEE Group on Reliability. Among those playing an ac tive role are **Ed. J. Westcott,** Chapter Vic Chairman; **Sam Canale,** Publicity Com mittee Chairman; **Nick Salatino,** Progra Committee Chairman; **John Davaro,** Ar rangements Committee Chairman; **Ji Goodman,** Advisory Board Chairman an Past Chapter Chairman; and **Bob Killion** Seminar Management Committee Chair man.

New technique for producing metallic film holograms

Development of an experimental tech nique which involves use of a laser a a kind of optical branding iron to im press holograms into thin metal films fo use as fixed, high-capacity computer memories was announced recently by

RCA Laboratories, Princeton, N.J. The new technique eliminates chemical development and the massive, low-vibration tables required in the making of conventional holograms, and may also find application in non-destructive testing and scientific measurement, according to **Dr. William M. Webster,** Vice President, RCA Laboratories, Princeton, N.J.

When the laser light falls on the metal film, it is converted to heat of sufficient intensity to evaporate portions of the film, producing a kind of holographic engraving in from 5 to 20 billionths of a second. With such a short exposure time, the information, or object, being recorded would have to be moving faster than 20 feet per second with respect to the film for the hologram to become distorted.

Furthermore, because no chemical processing or other development is required, the RCA hologram can be viewed immediately after it is exposed without moving it in any way. Thus, the hologram is perfectly positioned for the successive observations required in non-destructive industrial testing of materials and products.

The new technique is also quite adaptable to the storing of large amounts of fixed data in optical memory systems, such as those contemplated for auto license bureaus, insurance companies, and other government and commercial offices that require large amounts of data that are changed relatively infrequently, if at all.

For example, Dr. Webster noted, approximately 300 million bits of permanent information could be stored on a single holographic card 16 by 4¼ inches (the dimensions of a standard magnetic memory card that holds about 2 million bits). He said the RCA holographic approach has many advantages over other large-scale optical storage techniques that require the shining of light through minute holes (0.1 mil in diameter) in thin metal films for reading, and, therefore are quite vulnerable to dust, scratches and other physical distortions that do not affect holograms.

The new RCA technique was developed under the direction of **Dr. Jan A. Rajchman,** Staff Vice President, Information Sciences. The research was done by **Dr. Juan A. Amodei,** of the RCA Solid State Research Laboratory, and **Dr. Reubin S. Mezrich,** of RCA Information Sciences Research.

Computerized testing of jet engine fuel control

Aerospace Systems Division, Burlington, Mass., has obtained a $1.9 million Air Force contract to develop and install a computerized system that performs checks on jet engine fuel controls faster than is possible with conventional, manual techniques. The system, which also offers major advances in checking the accuracy of such parameters as fuel flow, pressure drop, and fluid temperatures, will automatically check out main and afterburner fuel controls for J79 jet engines.

The Automatic Test System/Jet Engine Accessories (ATS/JEA) will be installed at Tinker AFB, Okla., to service fuel controls during engine overhauls. However, the system also could find future use on production lines during engine manufacturing and in maintenance facilities of commercial airlines.

Major equipment components in ATS/JEA include three main fuel control test stands, one afterburner fuel control test stand, and a time-shared process controller to operate the stands in conjunction with the test stand operator.

While the test stands will be controlled by one process control subsystem that is programmed to operate all four stands simultaneously, each operator will appear to have exclusive access to the controller. At no time will any of the operators be aware of demands made by other stands. Each test stand is a self-contained unit with its own hydraulic system and reservoir, transducers, actuators, control panel, digital displays, and teletypewriter.

In the ATS/JEA automatic mode, all stimuli and measurements are controlled by the process controller. The operator performs test stand hook-up and fuel control mechanical adjustments in accordance with simplified printed instructions and/or visual displays. The system then tests the fuel control automatically. Should an adjustment or replacement be necessary the ATS/JEA will identify the required action to the operator by printing out a message.

RCA will also furnished the Air Force with complete operating manuals and will assign field engineers to provide maintenance support for a one year period following ATS/JEA's acceptance.

Earth-controlled color TV system for moon exploration

Astro-Electronics Division of DEP, Princeton, N.J. is developing an earth-controlled space TV system that will beam live, full-color pictures from the Lunar Rover vehicle that Apollo astronauts will drive over the moon's surface. Designated the Ground Command Color Television Assembly (GCTA), several of the systems are being built for NASA by AED under a $1.62 million contract which covers both color TV cameras and remote-control units. The system is slated for use in Apollo 16 and in subsequent lunar exploration missions.

The RCA space color TV camera to be used in the GCTA system employs the revolutionary Silicon Intensifier Tube (SIT). The camera is capable of transmitting pictures under all extremes of lighting on the moon, ranging from the dimness of sunrise to the brilliance of high noon. It is immune to damage from sunlight, even when pointed directly at the sun.

The color TV camera will be cable-connected to its associated control unit which, in turn, will be connected to the RCA-built Lunar Communications Relay Unit (LCRU) mounted on the Rover. (The LCRU, a briefcase-sized system which will permit communications from the moon to stations on earth without the signals being relayed through the LM, is being developed under a separate NASA contract by Defense Communications Systems Division of DEP, Camden, N.J.)

In this mode, the camera either could be operated manually by the astronauts or controlled remotely from earth. Manual switches will permit the astronauts to override all ground command functions and operate the camera without damage to the GCTA system. The switches will be spring returnable so that once released by the astronaut the function will be back under ground command.

If required, the camera can be connected directly to the LCRU, although it will not be ground commandable in that configuration. It also can receive power from the Lunar Module for picture transmission, but again without remote-control capabilities.

Being remotely controlled from earth will offer greater flexibility in TV coverage of the moon since the camera can be employed at any time without depending on the astronauts to operate it. Operators in NASA's Manned Spacecraft Center at Houston will be able, by means of radio remote control, to turn the camera on and off, raise, lower, and turn the camera, adjust the zoom lens focal length, and switch the automatic light control from peak to average. The system will have nearly full-circle panning capabilities and will be designed for an upward tilt to 85 degrees and downward to 45 degrees.

Depending on the Rover's remaining battery life, a ground-commanded camera could telecast the LM lift-off and continue to transmit video from the moon after the astronauts have left.

CSD receives $25 million computer order from Navy

Computer Systems Division has received the largest computer order in its history, a $25 million contract award from the Navy for 14 computerized message distribution systems. Awarded by the General Services Administration, the contract calls for installation of 14 Spectra 70/45's in naval operations centers around the world.

Each communications system also includes two RCA 1600 computers and five 70/7522 video data terminals. The first system will be installed by the end of this year at the office of the Chief of Naval Operations in the Pentagon.

A. R. Harris

R. P. Lamb

Art Harris is new TPA for CSD, Palm Beach

Arthur R. Harris has been appointed Technical Publications Administrator for the Computer Systems Division at Palm Beach Gardens, Florida. In this capacity, Mr. Harris will be responsible for the review and approval of technical papers; for coordinating the technical reporting program; and for promoting the preparation of papers for the *RCA Engineer* and other journals, both internal and external.

Mr. Harris received the BA in Writing from Southern Methodist University of Missouri, and the MBA in Engineering Management from Rollins College, Florida. He was a Senior Technical Editor at Cape Kennedy for twelve years, including seven years with RCA-MTP. He left RCA in 1964 to become Lead Technical Editor with The Boeing Company at Kennedy Space Center, Florida, and at Seattle, Washington. Mr. Harris rejoined RCA at Palm Beach Gardens in June 1970. He is a Senior Member of the Society of Technical Writers and Publishers (STWP).

R. P. Lamb is appointed Ed Rep for MTP

Robert Paul Lamb has been appointed Editorial Representative for RCA Service Company's Missile Test Project. In this capacity, Mr. Lamb is responsible for planning and processing articles for the *RCA Engineer*, and for supporting the activities of **M. G. Gander,** Technical Publications Administrator for the Service Company.

Mr. Lamb, a former Florida weekly newspaper publisher, has also been named Employee Publications and Services Administrator for the Missile Test Project. In addition, Mr. Lamb will serve as editor of the MTP NEWS. He replaces **Walt Mack** who has transferred to Cherry Hill, N.J., where he is a staff writer with News and Information, Computer Systems Division. Mr. Lamb attended Georgia Southwestern College and the University of Georgia under a scholastic scholarship from the Macon newspapers. Following completion of college in December, 1964, he returned to Macon to work for the local newspapers in which he received several citations for outstanding police investigative stories. He left newspaper work in December, 1965, to work full-time at his publicity and promotion company sponsoring entertainment shows. Mr. Lamb closed his public relations organization in August, 1966, to accept a position as editor of corporate publications for the Marriott Corporation. He moved to Florida in August of 1968, and has since served as president of a small corporation which operates apartment units in Tampa and publishes a weekly newspaper in Fort Meade.

New Appointment to *RCA Engineer* staff

W. O. Hadlock, Editor, *RCA Engineer*, has announced the following changes to the *RCA Engineer* editorial staff: **J. C. Phillips,** Associate Editor; **F. J. Strobl,** Consulting Editor; **Miss Diane Juchno,** Editorial Secretary; and **Joan P. Dunn,** Design and Layout Specialist.

Mr. Phillips, who was formerly Assistant Editor, received the Bachelor of Arts degree in Mathematics with honors in June 1970 from Rutgers University. He previously completed two years of evening study at Newark College of Engineering. Before joining the *RCA Engineer* staff in 1967, he was an Editorial Representative at Astro-Electronics Division. In 1962, he joined RCA at the Astro-Electronics Division where he was closely associated with publications for most of the major AED space programs. From 1960 to 1962, he was a technical writer at the Bendix Corporation where he advanced to the position of group leader. From 1956 to 1960, he was on active duty with the U.S. Navy where he was assigned the responsibility for maintenance of all types of submarine electronic equipment. Mr. Phillips is a Member of the IEEE and is active in the Group on Engineering Writing and Speech, as Associate Editor of the *Transactions* and as a member of the Administrative Committee.

Mr. Strobl's primary responsibility is Editor, *TREND* (The Research and Engineering News Digest); however, he is now assisting the *RCA Engineer* staff in planning, editing, and author contacts. Mr. Strobl received the AAS in Electrical Technology from New York City Community College in 1954. In addition to taking further courses in Engineering, Mr. Strobl is pursuing the BS at the evening division of Rugers University. His early experience included two years in the U.S. Army as a Instructor of the NIKE Missile System. From 1958 to 1960, he was a customer engineer for IBM, and from 1960 to 1962, he was a technical writer for the Bendix Corporation where he became a lead writer preparing technical manuals on the B-58 flight control system. Mr. Strobl joined the Astro-Electronics Division of RCA in 1963, where he has served as project writer for the NEW MOONS Program and the Navy Navigation Satellite Program.

Mrs. Dunn will be responsible for providing page-layout and design assistance to the editorial staff. Mrs. Dunn studied fine art for eight years under Frederick Reiniger; she attended Rutgers University for one year, majoring in English; and took courses at Harris School of Business for one year. Currently she is taking fine arts courses at Fleisher Art Institute. In the fall, she plans to continue her education with a course in industrial arts. For the past two years, Mrs. Dunn has worked with the Continuing Engineering Education program RCA Corporate Engineering Services, specializing in the preparation and use of graphics for the video tape media.

Clip out and mail to Editor, *RCA Engineer*, #2-8, Camden

RCA Engineer

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Editorial Representatives

The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

efense and Commercial Systems

Defense Electronic Products

Aerospace Systems Division — D. B. DOBSON* Engineering, Burlington, Mass.

Electromagnetic and Aviation Systems Division — R. J. ELLIS* Engineering, Van Nuys, Calif.
J. McDONOUGH Engineering, West Los Angeles, Calif.

Astro-Electronics Division — I. M. SEIDEMAN* Engineering, Princeton, N.J.
S. WEISBERGER Advanced Development and Research, Princeton, N.J.

Missile & Surface Radar Division — T. G. GREENE* Engineering, Moorestown, N.J.

Defense Communications Systems Division — A. LIGUORI* Engineering, Camden, N.J.

Defense Engineering — M. G. PIETZ* Advanced Technology Laboratories, Camden, N.J.
M. R. SHERMAN Defense Microelectronics, Somerville, N.J.
J. E. FRIEDMAN Advanced Technology Laboratories, Camden, N.J.
J. L. KRAGER Central Engineering, Camden, N.J.

Defense Plans and Systems Development — E. J. PODELL Engineering Information and Communications, Camden, N.J.

Commercial Electronics Systems — D. R. PRATT* Chairman, Editorial Board, Camden, N.J.
N. C. COLBY Mobile Communications Engineering, Meadow Lands, Pa.
C. E. HITTLE Professional Electronic Systems, Burbank, Calif.
R. N. HURST Studio, Recording, & Scientic Equip. Engineering, Camden, N.J.
R. E. WINN Broadcast Transmitter & Antenna Eng., Gibbsboro, N.J.

Industrial and Automation Systems — H. COLESTOCK Engineering, Plymouth, Mich.

nformation Systems

Computer Systems Division — A. HARRIS* Palm Beach Engineering, West Palm Beach, Fla.
W. D. STELLMAN* **(acting TPA)** Engineering, Marlboro, Mass.
E. M. MORTENSON* Instructional Systems Engineering, Palo Alto, Cal.
B. AARONT Service Dept., Cherry Hill, N.J.

Magnetic Products Division — A. G. EVANS Development, Indianapolis, Ind.

Memory Products Division — L. A. WOOD Engineering, Needham, Mass.

Graphic Systems Division — J. GOLD* Engineering, Dayton, N.J.

Research and Engineering

Laboratories — C. W. SALL* Research, Princeton, N.J.

Electronic Components — C. A. MEYER* Chairman, Editorial Board, Harrison, N.J.

Receiving Tube Division — J. KOFF Receiving Tube Operations, Woodbridge, N.J.
R. J. MASON Receiving Tube Operations, Cincinnati, Ohio

Television Picture Tube Division — J. H. LIPSCOMBE Television Picture Tube Operations, Marion, Ind.
E. K. MADENFORD Television Picture Tube Operations, Lancaster, Pa.

Industrial Tube Division — J. M. FORMAN Industrial Tube Operations, Lancaster, Pa.
H. J. WOLKSTEIN Microwave Tube Operations, Harrison, N.J.

Technical Programs — D. H. WAMSLEY Engineering, Harrison, N.J.

Solid State Division — M. B. ALEXANDER Solid State Power Device Engrg., Somerville, N.J.
T. J. REILLY Semiconductor and Conversion Tube Operations, Mountaintop, Pa.
J. D. YOUNG Semiconductor Operations, Findlay, Ohio
I. H. KALISH Solid State Signal Device Engrg., Somerville, N.J.

Consumer Electronics Division — C. HOYT* Chairman, Editorial Board, Indianapolis, Ind.
D. J. CARLSON Advanced Devel., Indianapolis, Ind.
R. C. GRAHAM Procured Products Eng., Indianapolis, Ind.
P. G. McCABE TV Product Eng., Indianapolis, Ind.
J. OSMAN Electromech. Product Eng., Indianapolis, Ind.
L. R. WOLTER TV Product Eng., Indianapolis, Ind.
R. F. SHELTON Resident Eng., Bloomington, Ind.

Services

RCA Service Company — W. W. COOK Consumer Products Service Dept., Cherry Hill, N.J.
M. G. GANDER* Consumer Products Administration, Cherry Hill, N.J.
K. HAYWOOD Tech. Products, Adm. & Tech. Support, Cherry Hill, N.J.
R. P. LAMB Missile Test Project, Cape Kennedy, Fla.

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