OUR COVER

. . . illustrates the new RCA Spectra 70/45 system, which features third-generation computer technology such as monolithic integrated circuits, printed backplane, and advanced concepts in logic and memory. Framing the photo is an enlarged photomicrograph of the Spectra 70/45 monolithic-silicon integrated circuit. The new Spectra 70 series, which also includes Spectra 70/15, 70/25, 70/35, 70/55, and a wide range of peripheral equipment, is compatible with a wide variety of industry-accepted codes and program languages. In the foreground, Dick Yen is at the console of the main processor, while Les Busch is shown with peripheral equipment in the background; both are with EDP Engineering, Camden. (Cover art direction, J. Parvin, Photo, R. Allen.)

ELECTRONIC DATA PROCESSING

A Continuing Challenge

The fact of electronic data processing as it exists today represents the response of engineers to the challenge posed in its initial concept. In the two decades since the start of this branch of engineering, performance-to-cost ratios have shown continuing increase so that today solutions of problems in science, in business, and in management are commonplace — solutions which heretofore were impractical or even impossible.

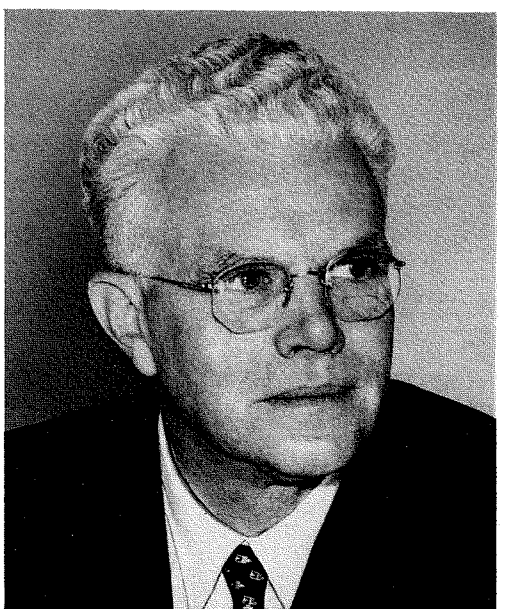
While the improvement in fast memories from storage tubes and sonic delay lines to laminated ferrites with integrated diodes is perhaps the most conspicuous advance, of equal significance are the developments in drums, discs, tapes, and magnetic cards. Logic is more powerful and less costly because of better machine organization, better circuits, and better components. The monolithic integrated circuit and its application mark a breakthrough, the full implications of which can only be guessed at. Software has become more sophisticated and powerful.

Mechanical features of design have become increasingly critical; this trend will continue. In a recent talk before an IEEE group, Dr. Rajchman correctly stated that in many areas the problem of interconnection has become more important than the design of the elements to be interconnected. The demand for higher and higher processing speeds has placed continuously increasing demands on the mechanical designers of peripheral equipment — the video-electronic ingenuity of the optical character reader is matched by the mechanical ingenuity of its transport mechanism.

The challenges which have been met in these developments run throughout the Corporation: the Laboratories, Electronic Components and Devices, and Defense Electronics feel their impact quite as much as does EDP. This issue highlights the Spectra 70, which involves all of the challenges mentioned above. However, in this profession the challenges never stop; the market will continue to demand ever increasing performance-to-cost ratio, higher percentage operating time, and more powerful programs which are easier to write. The challenge of multi-use application, which is already audible, will have to be met by every segment of the data-processing and communicating force. And equal challenges with more stringent environmental requirements come to us from military and space applications.

C. A. Gunther

C. A. Gunther
Division Vice President
Technical Programs



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CONTENTS

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

● To disseminate to RCA engineers technical information of professional value. ● To publish in an appropriate manner important technical developments at RCA, and the role of the engineer. ● To serve as a medium of interchange of technical information between various groups at RCA. ● To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions. ● To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field. ● To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management. ● To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

An index to RCA ENGINEER articles appears annually in the April-May issue.

The increasing number of large aerospace and military research and development programs handled by RCA on an interplant basis has brought out the need for a Directory of company-wide environmental test facilities, such as presented in this paper. Included are details on the specific types and capacities of the equipment complements. The Bibliography notes sources of information for environmental facilities throughout the government and aerospace industry. This Directory can help in the selection and scheduling of environmental test programs.

The Engineer and the Corporation

DIRECTORY OF RCA ENVIRONMENTAL TEST FACILITIES

S. SCHNITZER
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In the highly competitive defense electronics industry, the firm possessing the greatest number and variety of environmental testing facilities has an obvious advantage in bidding for new business. It is noteworthy, therefore, that the engineering offices and plants of RCA collectively provide an impressive aggregation of environmental test equipment. The MINUTEMAN Program Management Office, in planning and directing the environmental testing of ground electronics equipment for the MINUTEMAN ICBM system. has made extensive use of some of these facilities.

It is felt that a list of these environmental test facilities would be of invaluable assistance throughout RCA, not only as a ready reference for design engineers but also in the preparation of proposals for the development of military and aerospace electronic systems and equipment, by enabling planners and estimators to incorporate greater flexibility in their schedules.

Table I presents basic information on most of the environmental test facilities available at the RCA plant in Camden, as well as information on similar facilities at seven other RCA plants. The equipment listed is presented as a help for complying with environmental test requirements of such military and aerospace specifications as MIL-E-4970A *(Environmental Testing, Ground Support Equipment)*; MIL-E-5272C (*Environmental Testing, Aeronautical and Associated Equipment)*; MIL-T-5422E (ASG) *(Testing; Environmental, Aircraft Electronic Equipment)*; and MIL-STD-810A(USAF) *(Military Standard Environmental Test Methods for Aerospace and Ground Equipment)*. In addition to the equipment listed, others are often available (though not noted in detail here) such as "combined environments," sand and dust chambers, rain and sunshine chambers, and screen rooms.

This list does not cover the support services and facilities usually associated with the equipment listed. However, most required items such as oscilloscopes, accelerometers, thermocouples, calibration services, and data reduction facilities are very likely available.

Naturally, where test requirements exceed the capabilities of available RCA facilities, outside laboratories may have to be considered, such as those at the large aerospace concerns and at those government laboratories primarily engaged in aerospace and missile development and testing (see References 1 and 4). Other facilities which should be considered are those offered by concerns which specialize in environmental testing.

The aggregate of RCA environmental test facilities provides capabilities which are more than adequate for most requirements. The environmental testing required on many areospace and military programs may be accomplished within RCA on the same multiplant basis frequently employed in the conduct of other aspects of the work. In the highly competitive electronics industry the objective of timely, economical fulfillment of environmental test requirements necessitates consideration of *all* pertinent RCA facilities.

Final manuscript received June 18, 1965

ACKNOWLEDGEMENT

Appreciation is hereby expressed to the individuals named in Table I for the information each contributed on the environmental facilities in his area.

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3. R. E. Gaumer and V. A. Plaskett, "Environmental Simulation," *Space/Aeronautics Research and Development Technical Handbook*, 1964/1965. (Sept. 1964) p. 187 (Discusses major problems of simulating space environment. Presents table listing NASA's large vacuum chambers.)
4. A. J. Hollings, *Index of Environmental Test Equipment in Government Establishments*, Office of the Director of Defense Research and Engineering, Washington 25, D.C. (revised Aug., 1962).

S. SCHNITZER graduated from the University of Illinois with a BSME in 1935. From 1940 to 1946 he worked at the Boeing Company, Seattle, Washington, where he was a group leader in charge of the development of aircraft hydraulic and pneumatic equipment. From 1946 to 1950 Mr. Schnitzer was in charge of the hydraulics development laboratory at the Pacific Division, Bendix Corporation. In 1950, Mr. Schnitzer joined the U.S. Naval Air Development Center at Johnsville, Pa., where his assignments included the development and testing of aviation armament equipment. Since joining RCA in 1957, Mr. Schnitzer has been in the Mechanical Integration Group for the ARIES aircraft fire control system, and has participated in the design and testing of equipment for the acquisition radar system of the NIKE-ZEUS anti-missile system. He has worked in the Environmental Engineering, Central Engineering, Camden, and since 1962, has been active in the test coordination group of the Minuteman Program Management Office. Mr. Schnitzer has taken graduate courses at Temple University and at the University of Pennsylvania, and is a member of Tau Beta Pi and the Institute of Environmental Sciences.

TABLE I — RCA ENVIRONMENTAL FACILITIES

LOCATION KEY (Individual to contact named in parentheses.)

CSD-1: Environmental Eng. Lab., DEP Comm. Syst. Div., Camden, N.J. (J. N. Breen, Bldg. 13-1)

CSD-2: Acoustics Lab., DEP Comm. Syst. Div., Camden, N.J. (A. Witchey, Bldg. 10-5)

CSD-3: Components and Parts Analysis Group, DEP Comm. Syst. Div., Camden, N.J. (D. M. Way, Bldg. 8-6)

CE: DEP Central Eng., Camden, N.J. (B. H. Rosen, Bldg. 1-6)

ECD-1: Test and Specifications Eng., Electronic Compts. and Devices, Harrison, N.J. (M. DeVito, Bldg. 55)

ECD-2: Environmental Eng., Electronic Compts. and Devices, Harrison, N.J. (J. M. Forman, Bldg. 922)

ECD-3: Reliability Lab., Electronic Compts. and Devices, Harrison, N.J. (J. E. Stoltman, Dept. 916)

MSR: Environmental Test Lab., DEP Missile & Surface Radar Div., Moorestown, N.J. (A. Mastrogiovanni, Bldg. 109-107)

COR: Packaging Testing Lab., Corporate Staff, Camden, N.J. (R. Maska, Bldg. 24-1)

AED: Environmental Test Center, DEP Astro Electronics Div., Princeton, N.J. (F. Yannotti)

ASD-1: DEP Aerospace Systems Div., Burl., Mass. (J. G. Colt)

ASD-2: Environmental Test Lab., DEP Aerospace Syst. Div., Burl., Mass. (S. Steinfeld)

ACOUSTIC CHAMBERS	Internal Dimensions	Volume ft³	Freq. Range c/s	Sound Pressure Level, dB(rms)	Location
A-1 (custom built by RCA)	9″ x 9″ x 6′-0″	3.38	20-10,000	145	CSD-2
A-2 (custom built by RCA)	6′-6″ x 3′-0″ x 1′-6″	29.25	20-10,000	145	CSD-2
A-3 (custom built by RCA)	5′-0″ x 5′-0″ x 6′-0″	150.0	100- 3,000	160	CSD-2

SALT SPRAY CHAMBERS	Internal Dimensions	Temp: Range, °F		Location
		Low	High	
SS-1 Indust. Filt. & Pump 411.3AC	29″ x 18″ x 20″	*	*	ECD-3
SS-2 Indust. Filt. & Pump CAH-3	30″ x 17½″ x 20″	*	*	CSD-3
SS-3 (custom built)	18″ x 3′-0″ x 3′-0″	Amb.	105	MSR
SS-4 Assoc. Test Labs. SS-2-16	20″ x 29″ x 3′-5″	*	*	ECD-3
SS-5 Indust. Filt. & Pump CAH-1	33 x 24 x 48	Amb.	125	CSD-1
SS-6 Indust. Filt. & Pump CAH-1	33 x 24 x 48	Amb.	125	ASD-2

* Meets requirements of MIL-STD-202

SHOCK SYSTEMS	Test Item Wt. Lb.	Table Dimension in.	Drop Ht., In.	Shaped Pulse Capability	Duration, ms	Deceleration g	Location
S- 1 Avco SM-005	5	9 x 9	—	yes	0.2 to 11	3000	CE
S- 2 Barry 16750	20	8 x 8	36	sine wave, square wave, sawtooth	0.5 to 11	1500	ECD-1
S- 3 RCA (custom)	20	15 x 18	(70° swing)	no	0.8	1300	ECD-1
S- 4 Taft-Pierce 722 KK	20	15 x 18	(70° swing)	no	0.8	1300	ECD-1
S- 5 Rad. Freq. Labs. Jan-S-44	24	—	—	half-sine	6 to 12	100	ECD-2
S- 6 Avco SM-005-1	30	9 x 9	—	half-sine	35 0.2 to 11	20 3000	ECD-3
S- 7 Avco SM-005-1	30	9 x 9	—	half-sine	35 0.2 to 11	20 3000	ECD-3
S- 8 Taft-Pierce 3	30	15 x 18	—	half-sine	0.75	1000	ECD-2
S- 9 CEC Hyge-Hy3401	40	4 (dia.)	—	half-sine	6 11 11	40 15 30	ECD-1
S-10 Barry B15-575	100	24 x 24	48	half-sine half-sine sawtooth	30 25 15	11 40 11	ASD-1
S-11 Barry 16805	200	24 x 24	—	half-sine sawtooth square wave	1 to 30 6.5 11	50-1000 110 30	ECD-2
S-12 Barry 150VD Mod.	400	36 x 36	30*	no	6.5 to 32	75	CSD-1
S-13 Barry 150-400 VD	400	36 x 36	30*	half-sine	6.5 to 32	77	ECD-2
S-14 Barry 150-400 VD	400	36 x 36	30*	no	6.5 to 32	75	MSR
S-15 Lab 600-CM-116**	600	40 x 60	20***				COR
S-16 Avco SM-030	1000	36 x 36	26#	sawtooth or tropezoidal square wave	3 15 4 8	300 60 135 60	CSD-1
S-17 Barry 1200 VD	2000	72 x 72	36##	no		105	CSD-1
S-18 CEC Hyge	###	12 x 16	O	half-sine sawtooth or square	2, 6, & 27 6 & 11	300	AED

* Test item = 32″ high
** Inclined inpact package tester
*** Equivalent vertical drop height
\# Test item = 75″ high
Test item = 88″ high
Depends on required acceleration
O Test item is not dropped. Height above table is over 30″.

EXPLOSION CHAMBERS	Internal Dimensions, Ft. & In.	Other Information	Location
E-1 Tenney 3D4	3′-3¼″ dia. x 4′-0″ long	Meets requirements of MIL-E-5272C, Procedures III and IV	CSD-1

TEMPERATURE CHAMBERS	Internal Dimensions	Temp. Range, °F		Location
		Low	High	
T- 1* Statham TC-4A	4″ x 8″ x 5″	—103	617	ECD-1
T- 2 Statham BC-4A	8″ x 10″ x 10″	70	608	ASD-2
T- 3 Tenney TMUF	12″ x 12″ x 12″	—94	302	CSD-3
T- 4 Assoc. Test Labs. ELH-2-LC	12″ x 12″ x 12″	—100	350	ECD-1
T- 5 Statham BC-4B	8″ x 8″ x 34″	—94	662	ASD-2
T- 6 Tenney TMUF-100240	14″ x 14″ x 14″	—105	248	ECD-3
T- 7 Tenney TMUF-120240	14″ x 14″ x 14″	—123	248	ECD-3
T- 8 Assoc. Test Labs LH-4-LC	18″ x 18″ x 18″	—100	1000	ECD-1
T- 9 Am. RSCH. Corp. 5036-100400	3′-0″ x 3′-0″ x 4′-0″	—100	400	ECD-2
T-10 Mantec D102	4′-0″ x 8′-0″ x 3′-0″	—103	572	ECD-1

* Eight low voltage (500 v) terminals available

THERMAL-VACUUM CHAMBERS	Internal Dimensions	Temp. Range, °F		Max. Vacuum mm Hg	Location
		Low	High		
TV-1 Tri metal Works 6A	17″ x 17″ x 17″	—40	572	10^{-5}	CE
TV-2 CVC (custom)	19″ dia. x 2′-6″ high	—70	300	10^{-5}	ECD-1
TV-3 CVC PS-40-A	2′-0″ dia. x 2′-6″ high	—65	160	10^{-6}	CSD-1
*TV-4 Tenney 3D4.5	3′-0″ dia. x 4′-6″ long	—300	300	5×10^{-7}	ASD-1
TV-5 CVC (custom)	4′-0″ dia. x 5′-0″ long	—60	250	10^{-5}	AED
TV-6 High vac. equip. (custom)	5′-6″ dia. x 10′-0″ long	—300	250	10^{-6}	AED
TV-7 Bethlehem (custom)	8′-0″ dia. x 10′-0″ long	—300	300	10^{-6}	AED
TV-8 RCA Service Co. (custom)	24′-0″ dia. x 20′-0″ long	—300	250	5×10^{-6}	AED

* Time to reach 10^{-6} mm Hg and —300°F from +300°F = 8 hrs. time to reach 10^{-6} mm at atmospheric conditions = 5 hrs.

TEMPERATURE HUMIDITY CHAMBERS	Internal Dimensions	Temp. Range, °F		Humidity Range, %		Remarks	Location
		Low	High	Low	High		
TH- 1 Forma Scientific 3190	24″ x 20″ x 30″	0	240	20	95	Humidity range applies between 35° and 185°F	ECD-3
TH- 2 Tenney 12TR100300	24″ x 24″ x 24″	—94	302	0	100		CSD-3
TH- 3 Tenney 8TR-4020	24″ x 24″ x 24″	—40	200	20	95	Humidity range applies between 35° and 185°F	ECD-2
TH- 4 Bowser H-10-R	16″ x 22″ x 41″	35	180	20	95		MSR
TH- 5 Itemco 10H	24″ x 28″ x 23″	35	200	20	95		ASD-2
TH- 6 Tenney TH-16	21″ x 23″ x 43″	32	212	20	95		ECD-3
TH- 7 Tenney TH-10	2′-0″ x 2′-0″ x 3′-0″	35	185	20	95		ASD-1
TH- 8 Tenney TH-16	2′-0″ x 2′-0″ x 3′-0″	35	185	20	95		ASD-1
TH- 9 Bowser H-16-R	1′-2″ x 3′-6″ x 3′-6″	Amb.	185	Amb.	95		CSD-1
TH-10 Forma Scientific (modified)	2′-2″ x 3′-0″ x 2′-3″	10	155	20	98	Programmed for Mil-Std-202, Method 106	ECD-3
TH-11 Assoc. Test Labs ELHH-27-MRLC-3	3′-0″ x 3′-0″ x 3′-0″	0	300	20	100	Two 6″ ports available	ECD-1
TH-12 Tenney 1633	3′-0″ x 3′-0″ x 3′-0″	—20	200	20	95	Humidity range applies between 35° and 185°F	ECD-2
TH-13 Tenney 36TR100	3′-0″ x 3′-0″ x 4′-0″	—100	212	5	98		MSR
TH-14 Amer. Res. Corp. SOH36-100300	3′-0″ x 3′-0″ x 4′-0″	—100	300	20	95	Humidity range applies between 35° and 185°F	ECD-2
TH-15 Bethlehem (custom)	4′-0″ x 4′-0″ x 4′-0″	—100	250	20	95		AED
TH-16 Tenney (special)	14′-0″ x 14′-0″ x 17′-0″	—85	250	20	95	—85° to +250°F in 4 hrs. +250° to —85°F in 6 hours	

TEMPERATURE ALTITUDE CHAMBERS	Internal Dimensions	Temp. Range, °F		Max. Altitude 10^3 ft.	Remarks	Location
		Low	High			
TA- 1 Tenney TMST-100392	14″ x 14″ x 14″	—105	392	150	Limited to 212°F when operating at altitude	ECD-3
TA- 2 Tenney TMST-4.5-100350	18″ x 18″ x 18″	—100	360	100	Nine high voltage terminals (3 kv) and two RF terminals available	ECD-1
TA- 3 Tenney 8S	2′-0″ x 2′-0″ x 2′-0″	Room temp. only		150		ECD-3
TA- 4 Assoc. est. Lab A-4-L	2′-0″ x 2′-0″ x 2′-0″	Ambient		120	Six high voltage (5 kv) terminals available	ECD-1
TA- 5 Tenney 27ST85307	3′-0″ x 3′-0″ x 3′-0″	—94	257	92		CSD-3
TA- 6 Tenney 27ST	3′-0″ x 3′-0″ x 3′-0″	—100	350	125		ASD-1
TA- 7 I.R.C. (special)	3′-0″ x 3′-0″ x 3′-0″	—100	500	100	Four 6″ dia. ports available	ECD-1
TA- 8 Tenney 48ST	3′-0″ x 4′-0″ x 3′-0″	—99	302	125		CSD-1
TA- 9 Tenney 48ST	3′-0″ x 4′-0″ x 3′-0″	—99	302	150		CSD-1
TA-10 Amer. Res. Corp. Alt-36-100750	3′-0″ x 3′-0″ x 4′-0″	—100	750	150		ECD-2

CENTRIFUGES (Accelerators)	Wt. of Test Item, lb.	Max. rpm	Arm Radius	Max. Accel. g	Max. g-lb	Remarks	Location
C-1 Int'l. Equip. Co. Mod. U	**	18,000	2⅝″	20,000			ECD-3
C-2 Int'l. Equip. Co. Mod. EL	**	20,000	4½″	50,000		Refrig. Oper. = —4 to 104°F Vacuum Oper. = Bet. (1—4) x 10^{-3} mm Hg	ECD-3
C-3 Int'l. Equip. Co. Mod. K, Size 2	5	20,000	6″	30,000	—		ECD-1
C-4 Int'l. Equip Co. Mod. K, Size 2	12*	5,500	—	20,000	370	**	CE
C-5 Schaevitz G-50	50		2′-4″	100	2,500	Max. specimen size = 12″ x 12″ x 12″	CSD-1
C-6 Schaevitz B-10D	100		4′-3″	200	15,000	Max. specimen size = 18″ x 18″ x 18″	ECD-2
C-7 Schaevitz B-12D	100	225	5′-3″	100	10,000	Max. specimen size = 18″ x 18″ x 18″	AED

* Includes weight of balanced fixture

** For transistors and other components of comparable size.

HUMIDITY-ALTITUDE-TEMPERATURE CHAMBERS	Internal Dimensions	Temp. Range, °F		Humidity Range, %		Altitude 10^3 ft.	Location
		Low	High	Low	High		
Hat. 1 Tenney 48 str	3′-0″ x 4′-0″ x 4′-0″	—99	185	20	100	70	CSD-1
Hat. 2 Tenney 48 str	3′-0″ x 4′-0″ x 4′-0″	—99	185	20	100	60	CSD-1
Hat. 3 Hieart THV42-85	4′-0″ x 4′-0″ x 4′-0″	—100	250	20	98	80	ASD-2
Hat. 4 Tenney str-73100C	7′-0″ x 9′-0″ x 7′-6″	—99	212	5	98	125	MSR
Hat. 5 Guardite (special)	7′-0″ x 9′-0″ x 7′-6″	—99	199	20	95	80	CSD-1
Hat. 6 Guardite (special)	7′-0″ x 9′-0″ x 7′-6″	—99	199	20	95	80	CSD-1
Hat. 7 Tenney (special)	14′-0″ x 14′-0″ x 14′-0″ (door opening, 8′-6″ x 8′-6″)	—85	185	20	100	75	CSD-1

VIBRATION SYSTEM	Force Output Lb.	Wt. of Moving Element, Lb.	Freq. Range, CPS	Table Stroke Peak to Peak, In.	Table Dim., In.	Type of Excitation	Means of Actuation	Location
V- 1 Ling 6CT	25	5	0-700	0.75	2″ dia.	Sine	Electr.	ECD-1
V- 2 All-American 25H	25	—	10-60	0.125	12 x 15	Sine	Mech.	ECD-1
V- 3 Lab RV-15-30	30	—	5-100	0.375	15 x 15	Sine	Mech.	ECD-3
V- 4 Lab RV-15-30	30	—	5-100	0.375	15 x 15	Sine	Mech.	ECD-3
V- 5 All-American 25H-A	37	—	10-55	0.12	12 x 15	Sine	Mech.	CSD-1
V- 6 Lab RVH-18-50	50	—	5-60	0.125	18 x 18	Sine	Mech.	ECD-3
V- 7 MB C11	50	2.2	5-2000	0.5	2*	Sine	Electr.	CE
V- 8 MB C11-C	50	2.2	5-2000	0.5	2*	Sine or random**	Electr.	ECD-2
V- 9 Ling 227	150	1.75	2-9000	1.0	3.5 dia.	Sine	Electr.	ECD-1
V-10 Lab RVH-30-300	300	—	10-60	0.12	30 x 30	Sine	Mech.	CSD-1
V-11 Lab RVH-30-300	300	—	5-60	0.125	30 x 30	Sine	Mech.	ECD-1
V-12 Lab RVH-30-300	300	—	8-100	0.125	30 x 30	Sine	Mech.	ECD-1
V-13 Lab RVH-30-300	300	—	10-60	0.125	30 x 30	Sine	Mech.	ECD-2
V-14 Lab RVH-30-300	300	—	10-60	0.125	30 x 30	Sine	Mech.	ECD-2
V-15 Lab RVCGA-500	500	—	10-55	0.5	30 x 39	Sine	Mech.	CSD-1
V-16 Lab RVCGA-500-4	500	—	10-60	0.38	36 x 36	Sine	Mech.	ASD-2
V-17 Lab RVH-36	1000	—	10-55	0.06	36 x 36	Sine	Mech.	MSR
V-18 MB C10	1200	17.5	5-3000	1.0	8*	Sine or random**	Electr.	ECD-2
V-19 Ling 58	1250	22.5	5-2000	0.75	15½ x 18	Sine	Electr.	CSD-3
V-20 Unholtz-Dickie 81-CD	1400	20.0	5-3000	1.0	8*	Sine or random	Electr.	ECD-3
V-21 Ling 174/203	1500	20.0	5-3500	1.0	7 x 7#	Sine	Electr.	ASD-1
V-22 Ling 44	1500	8.25	0-500	1.0	9 x 9	Sine	Electr.	ECD-1
V-23 MB C10VB	1750	40	5-6000	1.0	8*	Combined sine & random	Electr.	AED
V-24 Lab RVH-72	2000	—	10-60	0.25	72 x 72	Sine	Mech.	CSD-1
V-25 Lab 2000-SNLV-MCTH-8***	2000	—	4½-7	1.0	60 x 96	"Circular-Synchronous"	Mech.	COR
V-26 MB C25H-E	2100	75	5-2000	0.5	16*	Sine	Electr.	MSR
V-27 MB C25	2500	73	5-500	0.3	19*	Sine	Electr.	CSD-1
V-28 Unholtz-Dickie##	2700	25	60	1.0	8*	Sine	Electr.	ECD-3
V-29 MB C25H	3500	75	5-2000	0.5	16*	Sine	Electr.	ECD-1
V-30 Ling 177A	3500	89	5-3000	1.0	12 x 12	Sine or random**	Electr.	ECD-2
V-31 MB C25H	3500	75	5-2000	0.5	16*	Sine	Electr.	ASD-2
V-32 Ling 177	5000	89	5-2000	0.5	11 x 11#	Combined sine & random	Electr.	CSD-1
V-33 Ling 213	5000	94	5-2000	0.5	11 x 11#	Sine	Electr.	CSD-1
V-34 MB C50	5000	40	5-3000	1.0	12*	Combined sine & random	Electr.	AED
V-35 Ling 300	7000	56	5-3000	1.0	12 x 12	Sine or random**	Electr.	ECD-2
V-36 MB C176	9000	100	5-3000	1.0	16*	Combined sine & random	Electr.	ASD-1
V-37 MB C210E	20,000	345	5-2000	1.0	27*	Combined sine & random	Electr.	AED

* Dia. of bolt circle.

\# Size of bolt pattern.

** MB Model T-388 Random Automatic Control Console available, permitting the attainment of sine, random, or mixed sine and random outputs.

\## Special 60 cps system.

*** Used for package testing.

RCA SPECTRA 70

An Introduction to Basic Design and Philosophy of Operation

The RCA Spectra 70 Series provides an open-ended family of compatible data-processing systems. Spectra 70, with its wide range of system configurations and all-purpose design, meets user requirements in all areas of commercial, scientific, multisystem, control, and communications applications. Through the use of a standard interface, new devices for general or special applications can be added without undergoing major redesign costs. In addition, the standard interface permits the extension of possible system configurations on an extremely favorable, cost-performance basis. This paper presents an overall description of the Spectra 70 systems and their operational features and includes a Bibliography of eleven other papers that treat specific aspects of the Spectra 70 Series.

A. D. BEARD, Chief Engineer

Electronic Data Processing
Camden, N. J.

ARTHUR D. BEARD received his BSEE and MSEE from the Rensselaer Polytechnic Institute and was an instructor there before joining RCA in 1949. He has been involved in the development of analog techniques for electronic navigation systems, and responsible for advanced development work in the fields of interceptor fire control, military television, and air traffic control. In 1958, he was placed in charge of digital development and design activity for such major defense projects as BMEWS. From 1959 to 1962, he was headquartered at the RCA West Coast Missile and Surface Radar Division, Van Nuys, California. In 1962, he was appointed to his present position as Chief Engineer, and has been responsible for engineering activities in connection with the RCA 301 data processing system, the medium-range RCA 501, the large-scale RCA 601, the RCA 3301, and the most recently announced RCA Spectra 70 system.

THE RCA Spectra 70 Series of computers are multilingual data-processing systems capable of accepting and processing a wide variety of industry accepted codes and programming languages. The high-order models feature extensive instruction complements and fast scratch-pad memories for processing power. Internal circuitry consists of the latest developments in the state of the art. As an example, two models use full third-generation circuitry featuring monolithic silicon integrated circuits. Design has been left open-ended to permit the addition of subsequent advanced concepts as they became available.

SYSTEMS STRUCTURE

The RCA Spectra 70 Series consists of a line of fast and powerful processors with the capability for diverse applications. A high through-put rate is ensured by offering a complete range of input-output devices that can be applied throughout the series.

At this writing, four processors are offered in the Spectra 70 Series: Models 70/15, 70/25, 70/45 and 70/55. (The latter two are described in detail in other papers.[1,2]) The common code structure is based on the widely *E*xtended *B*inary *C*ode *D*ecimal *I*nterchange *C*ode (EBCDIC) of eight bits plus parity. The standard memory unit is termed a *byte* (see *Glossary*, below). Memory access ranges from 2 μs down to 0.84 μs. Transfer at these access speeds varies from 1 to 4 bytes, depending upon the model processor used (Table I).

Memory storage capability starts at 4.096 bytes and extends to 524,288 bytes. The user is provided with extensive memory overlap between models; thus, system growth can be directed towards increased memory requirements and/or increased processing power.

In the area of system through-put, simultaneous input-output processing is provided by input-output channels. A selector channel is capable of addressing up to 256 input-output devices, one at a time. The number of selector channels depends upon the processor. In addition, a multiplexor channel capable of simultaneously addressing up to 256 input-output devices is available on Models 70/25, 70/45, and 70/55 processors. The multiplexor provides simul-

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Glossary of Some Computer Terms

Editor's Note: The following terms appear in various papers in this issue, and are defined here together to promote, hopefully, better understanding. Some are new (e.g., byte); some are old, but not always clearly understood (e.g., bit). Credit for these definitions is due H. Spencer, EDP, Camden.

bit field—An arbitrary portion of a computer word which, by its length and position in the word, defines a class of data or instruction.

byte—An arbitrary number of bits which comprise an operational unit of information.

bit—binary digit; an irreducible unit of information.

burst mode—A mode of transferring data to, from, or between processors wherein the data are transferred in bursts rather than in single bits or single characters.

elementary operation—Microprogramming instructions which in combination produce standard computer operations.

execution time—The time required by a processor to execute a given instruction.

current-mode-logic (CML) circuits—A collection of gates consisting principally of emitter-coupled transistors operating in the current-steering mode.

flip-flop—A logic circuit with two stable output states. Receipt of an input invariably changes its output from its present state to the other state.

fetching time—Staticising time.

gate—A logic circuit whose output state depends upon the state of its inputs and thus exactly simulates a formalized rule of logic.

internal control logic—The aggregation of gates in a control assembly which determines the performance of system to be controlled.

logic gate—See *gate*.

logic pair delay—The time required for a processor to perform two (usually related) steps of elementary logic.

laminated-ferrite memory array—A memory array consisting of three thin sheets of ferrite material with orthogonal addressing and sensing conductors imbedded between the sheets. The array is assembled while the ferrite is in its green state, pressed, and fired. A memory location ("core") consists of the volume of ferrite immediately adjacent to a cross point of two orthogonal wires.

monolithic silicon integrated circuit—A circuit consisting of transistors, diodes, and resistors formed by successive diffusion of doped silicon into and deposition of insulating material and conductors onto undoped silicon.

memory tube—A thermionic vacuum tube used in early computers to store many digits of binary information. The Williams' tube (University of Manchester) and the SB-256, or Selectron (RCA Laboratories), are examples.

multiplexor channel—A segment of the input-output circuitry of a processor for the concurrent operation of several peripheral devices by time-multiplexing technique.

optical character reading—A technique for scanning humanly legible characters optically and converting the video signal thus generated into the character's binary code.

parity bit—A redundant binary digit whose presence or absence gives an indication of an error in recording or reading, e.g.; parity bit can be added to (or omitted from) the binary code of a character to assure that the number of bits in every character is even. Thus, an even number of simultaneous errors is required for one to be undetected.

read-only memory (ROM)—A memory for storing fixed, or invariant data. The reading operation is nondestructive of the data.

sense amplifier—An amplifier to detect and amplify the output of a memory.

sense winding—The winding in a memory on which the output signal is generated.

scratch pad memory—A small, very fast memory (relative in the processor's main memory) used to replace registers for the storage of data.

shaded memory—That portion of the main memory of a processor which is reserved for input-output data; thus, it is not available to the programmer.

ultratype camera—An electronic device for composing a document on the face of a cathode-ray display tube. A pair of binary codes selects the character to be displayed from the "font" stored in a monoscope; a second pair of codes selects the coordinates of the location on the display tube where the character is desired. A video scan in the monoscope generates the selected character at the selected location. The entire document is recorded photographically.

taneous operation of devices by time-sharing the channel.

Model 70/15 Processor

The Spectra 70/15 is a small-scale processor for varied applications—as a separate data processor, as satellite support for larger systems, or as a remote communication terminal.

Memory is available in either 4,096 bytes or 8,192 bytes. Memory-cycle time is 2 μs to access 1 byte of information.

Model 70/25 Processor

The Spectra 70/25 is a small-to-medium-size processor that may be used as a free-standing data processor or as a subsystem of a multisystem complex.

High through-put rate is facilitated by fast memory cycle time and a high degree of input-output simultaneity. The 70/25 equipped with selector channels and a multiplexor channel concurrently operates up to eight slow-speed input-output devices in addition to eight high-speed devices.

Basic memory capacity of 16,384 bytes is expandable to 32,768 and 65,536 bytes. Memory-cycle time is 1.5 μs to access 4 bytes of information.

Model 70/45 Processor

The Spectra 70/45 is a medium-scale processor with a high performance capability for business, scientific, communications, and real-time applications.[1,2] A complete and powerful instruction complement with floating-point operation as an option is available.

The 70/45, equipped with a communication multiplexor, addresses up to 256 communications lines in addition to a full range of peripheral equipment.[3,8,10] Thus, the 70/45 is an ideal system-central for a multisystem operation and/or a powerful communication switching system. Up to 259-way simultaneity is possible.

Basic memory capacity of 16,384 bytes is expandable to 32,768, 65,536, 131,072, and 262,144 bytes. Memory-cycle time is 1.44 μs to access 2 bytes of information.

TABLE I — Spectra 70 Characteristics

	70/15	70/25	70/45	70/55
Processing Unit:				
Data Structure (bit width)	8	8	16	32
Scratch Pad	—	Main Memory	Fast Memory	Fast Memory
Control Structure (concept)	Wired Logic	Wired Logic	Elementary Operation	Wired Logic
Circuit Speed (pair delays in ns)	60	60	25	25
Instruction Complement	26	31	144	144
Program States	2	2	4	4
Main Memory Unit:				
Access (bit width, excluding parity)	8	32	16	32
Speed (cycle time in μs)	2.0	1.5	1.44	.84
Capacity (in 8-bit bytes)	4,096	16,384	16,384	65,536
	8,192	32,768	32,768	131,072
	—	65,536	65,536	262,144
	—	—	131,072	524,288
	—	—	262,144	—
Input-Output Unit:				
Multiplexor (max. subchannels)	—	115	256	256
Selector Channel (max. number)	1	8	3	6
Maximum Data Rate:				
Standard, kilobytes	200	267	465	640
High Speed Option, kilobytes	—	667	—	—

Model 70/55 Processor

The Spectra 70/55 is a medium-to-large-scale processor.[1,2] Though capable of the most demanding scientific applications, the 70/55 maintains a high through-put capability with up to 262-way simultaneity, thereby offering a total solution to all data-processing requirements.

Basic memory capacity of 65,536 bytes is expandable to 131,072, 262,144, and 524,288 bytes. Memory-cycle time is 0.84 μs to access 4 bytes of information.

Input-Output Devices

Input-output devices in the Spectra 70 Series are systems-oriented towards the processing task to be performed:

1) Card punches are fully buffered and punch at either 100 or 300 cards per minute.
2) Three models of printers are offered. A medium-speed printer prints up to a rate of 600 lines per minute, and a high-speed printer prints up to a rate of 1,250 lines per minute. A bill-feed printer operates at a speed of 600 lines per minute on continuous forms and a print rate of 800 cards per minute.
3) Card reading up to 1,435 cards per minute is performed photoelectrically.
4) Paper-tape capability of 5, 6, 7, or 8 channels is offered at a reading rate of 200 characters per second and a punching rate of up to 100 characters per second.
5) Three versions of magnetic tape units are available. Data rates are 30, 60, or 120 kilobytes per second. In a numeric mode, tape reading and writing are performed up to 240,000 digits per second.
6) Within the Spectra 70 Series, a complete complement of auxiliary storage devices capable of use on either a random or serial basis is available including a high-speed drum, interchangeable disc-storage units, and a novel mass storage unit.
7) The growing importance of optical character reading[7,10] is recognized in the Spectra 70 Series by the inclusion of the Videoscan Document Reader, which is capable of reading up to 1,300 documents per minute on demand. Videoscan handles stylized numeric characters and selected symbols.

SYSTEMS CHARACTERISTICS

Compatibility

The Spectra 70 Series features program compatibility between individual models. Program compatibility may be upward as in the 70/15 to 70/25, 70/25 to 70/45 and 70/55—or upward and downward as in the 70/45 and 70/55. Program compatibility requires that the ensuing model have at least the configuration of its predecessor and that timings, both internal and external, are not adversely effected.

Advanced programming systems—including input-output control systems, operating systems, generative systems, multiprocessing, COBOL, and FORTRAN IV—are offered within the Spectra 70 Series.

Fifth Computer Added to Spectra 70 Line—The Spectra 70/35

Editor's Note: *The following information was officially released too late to include in the text of the article; it has been appended here by the Editors to complete the description of the Spectra 70 series.*

On September 13, 1965, RCA Electronic Data Processing announced the addition of a fifth computer to the Spectra 70 line—the Spectra 70/35, a medium-scale computer combining third-generation technology (including integrated circuits) and speed in an efficient low-cost data system. The Spectra 70/35 handles a wide range of tasks at almost twice the speed of other general-purpose computers in its price range. Initial deliveries are scheduled to begin in late 1966.

The Spectra 70/35 is fully compatible with the Spectra 70/45 and 70/55 systems, which have identical instruction sets that permit program interchange within the family. The Spectra 70/35 also is designed to be compatible with comparable models of the IBM System 360, while emulators provide compatibility with the RCA 301 and the IBM 1401 computers.

Like its larger counterparts, the Spectra 70/35 standard interface permits the computer to use any of the extensive array of data storage units and input-output equipment in the Spectra 70 line. These include a variety of random access memories and magnetic tape units, video display devices, high speed printers, document readers, and punch card equipment. The computer was designed for on-line communications with a wide range of remote data stations. Up to 196 communications lines can be controlled by the computer. The 70/35 multiplexor channel permits the computer to handle up to 7 low-speed peripheral input-output or 196 communications devices simultaneously, in any combination. Two optional selection channels permit addressing of up to 256 high-speed devices each.

The programming packages or software developed for the larger 70/45 and 70/55 can be used with the new computer interchangeably.

Code Structure

The Spectra 70 Series coding structure is based on the widely used *E*xtended *B*inary *C*oded *D*ecimal *I*nterchange *C*ode (EBCDIC). The series also offers the facilities for generating and using the *A*merican *S*tandard *C*ode for *I*nformation *I*nterchange (ASCII).

To facilitate efficient manipulation of alphanumeric data, a byte consisting of 8 binary digits (bits) is used to represent each character. This allows the Spectra 70 Series to accept most present or future character codes. An 8-bit byte may represent one alphanumeric character, two decimal digits, or the eight bits.

Fixed-length data of 16, 32, or 64 bits may be processed. Variable-length data of up to 256 characters in 8-bit bytes may be processed. For purposes of data description, the terms *character* (1 byte), *halfword* (2 bytes), *word* (4 bytes) and *double word* (8 bytes) are used.

Machine Addressing

The Spectra 70 Series uses a two-part system of memory addressing consisting of a *base address* and a *displacement address*. A standard 12-bit instruction enables the programmer to address up to 4,096 bytes. This part is termed the *displacement*. A base address, stored in a general register, consists of a maximum 32 bits and addresses memory beyond the capacity of the displacement address. Thus, the base address, in effect, subdivides memory into 4,096 bytes—in that the displacement addresses the individual byte within the 4,096-byte module. The memory capacity of the Model 70/15 processor obviates the need for a base address, since the displacement has the necessray addressing range by the addition of a high-order bit to permit addressing of up to 8,192 bytes.

Instruction Format

The Spectra 70 Series uses a variable-instruction format consisting of 2, 4, or 6-byte instructions. Each instruction contains an *operation halfword* (2 bytes), and one or two register and/or memory addresses as required. Each address may be indexed by any of the general-purpose registers in combination with the base-address register.

The smaller processors contain instruction complements which are functional subsets of the larger 70/45 and 70/55 instruction complements. Floating-point operation is standard on the 70/55 and optional on the 70/45. Direct-control and memory-protect are optional features on both the 70/45 and 70/55. There are provisions for expanding the instruction complement to 256 order codes.

Arithmetic Operations

Complete flexibility in handling arithmetic operations is offered in the Spectra 70 Series. Decimal and binary operations are available throughout the series of models. Floating-point operations are avalable on the 70/45 and 70/55 Processors.

Decimal operations are performed on variable or mixed-signed fields in packed format (2 digits per byte). The maximum field size permitted is 31 digits plus sign, and the operation is performed storage to storage.

Binary or fixed-point arithmetic operations use either storage or registers for computation depending on the series model. In the 70/15 and 70/25, a 127-bit field (plus sign) is permissible. In the 70/45 and 70/55 the limit is a 31-bit field (plus sign) and arithmetic is performed in the registers (registers may be coupled to preserve precision).

Both short and long precision, 4 and 8 bytes respectively, are provided for either a speed or precision option. Limits of floating-point values are 2.4×10^{-78} to approximately 7.2×10^{75}.

Interrupt

The Spectra 70 includes a comprehensive set of system interrupts. These interrupts allow the particular Series model to respond to various internal and external conditions affecting systems operation. Processing at the time of the interrupt may be terminated, suppressed, or completed, depending on the cause of the interrupt. Processor interrupts, in general, may be controlled by the program through the use of interrupt masks. Interrupts are divided into the following classifications:

1) *Program Interrupts*—program errors such as overflows and illegal operation codes.
2) *External Interrupts*—servicing remote and operator-controlled devices, such as console intervention and requests from display or analog devices.
3) *Supervisor Call Interrupts*—interrupts caused by the user's program to request various functions in the operating system.
4) *Input-Output Interrupts*—input-output servicing of devices, such as terminations, transfer errors, and inoperable conditions.
5) *Machine Interrupts*—equipment malfunctions such as parity error or power shut-down.

If more than one interrupt occurs simultaneously, the interrupts will be serviced in a fixed order of priority. After servicing of the interrupt condition, linkage will be provided to the pre-interrupt conditions, if desired.

Processor States

Concurrent with the interrupt mechanism, Spectra 70 Systems may have up to four processor states. These processor states facilitate program control of interrupt conditions and normal processing operations. In effect, processor states reflect the particular status of a system at a given time in relation to the functions being performed.

These processor states deal with normal processing, interrupt mechanisms, operating systems, and machine malfunctions. The 70/15 and 70/25 contain two processor states while the 70/45 and 70/55 contain four processor states.

In the 70/45 and 70/55 the combinations of interrupt and processor states are carried to their logical extension in that each state contains its own complete interrupt system. The effect of each state having its own masks, registers, and instruction sets facilitates the servicing of the interrupt mechanism with a minimum of program manipulation.

Input-Output Channels

The control of the transmission of data between the processor and an associated peripheral device is accomplished through channels and the RCA Standard Interface.[3] A channel may be considered as an independent unit controlling data flow to and from the processor, and releasing control to the input or output device. This release allows the processor to function simultaneously with the input-output operation.

Each channel utilizes its own set of commands to perform input-output operations. These commands, referenced as channel commands, controls the device once a start command has been given by the processor. Chaining of channel commands provides a means by which several operations, such as multiple *reads*, may be completed independently of the processor.

The RCA Standard Interface functions as a connector between the channel and a device control. The interface establishes an identical relationship with each input-output device in that any device may be connected to the interface regardless of type, size, or speed. The number of channels and interfaces connected varies with the processor model. Within the Spectra 70 Series there are two types of channels: *selector channels* and *multiplexor channels*.

Selector Channel

The selector channel in the Spectra 70 Series controls the transfer of data to and from a peripheral device. These selector channels operate independently of the processor. A selector channel has from one to four trunks, depending upon the processor model. A controller determines the number of devices that can be connected to a trunk. For example, a tape controller controls as many as 16 tape devices. Channels can operate concurrently resulting in the overlap of

input-output operations. The transfer rate of the selector channel depends upon the speed of the particular processor.

Multiplexor Channel

The multiplexor channel provides a unique method through which varying speed peripheral devices may be attached. Speed variances are accommodated by having available two different transmission modes: *multiplex mode* and *burst mode*.

The multiplex mode is used when low-speed devices are attached to a processor and the channels data track is time-shared by all of the low-speed devices connected to the multiplexor. In this instance, every low-speed device may be operated simultaneously by the multiplexor channel sending and receiving the required data. The devices in the slow-speed range are printers, card readers, card punches, paper-tape reader-punch, and display terminals.

The burst mode must be used when high-speed devices are operated via the multiplexor; however, in the burst mode, only a single input-output device may use the channel at one time. Tape drive, disc, drum, and mass memory equipment are devices which must operate in the burst mode.

The multiplexor channel normally runs multiple devices on a time-sharing basis. A burst mode occurs automatically under certain conditions or is specified by a modification of the input-output command. The burst mode is limited to the Model 70/45 and 70/55 Processors. The multiplexor channel divides the data track into subchannels over which the data will flow. Each subchannel may be individually addressed by the program. The multiplexor channel may contain up to eight input-output trunks from which up to 256 input-output devices may be connected.

Memory Protect

The protection of memory segments from destruction by programming or input devices is provided in the Models 70/45 and 70/55 processors through the memory-protect feature.[4]

Memory-protect feature can, depending upon availability of memory, protect up to 15 memory segments or programs from address interaction. The basic segment consists of 2,048 bytes and is increased in multiples of 2,048 bytes. Memory-protect feature is a processor function and does not require memory allocation nor does it increase instruction timing. This feature greatly enhances the capability or multiprogramming in the Spectra 70 Series.

Direct Control

The optional direct-control feature offered in the Models 70/45 and 70/55 processors provides control and synchronizing information between the processors and/or special external devices. This direct-control feature provides two instructions that implement the transfer of 1 byte of information between the memory and an external device. The direct control also provides six external-signal lines effecting an external interrupt.

COMMUNICATIONS

The design of a communications facility for a family of third generation computers presents many challenges not present with other input-output peripheral devices. Marketing considerations dictate the need for operating with existing and projected remote devices such as video data terminals, data gathering equipments, and remote processors over common-carrier networks to permit the design of efficient and varied information, control, and time-sharing systems. Since the design of the common-carrier equipment and remote terminals cannot be controlled, a flexible and varied interface must be provided to these devices, while maintaining a standard interface with the Spectra 70 Processors.

The Spectra 70 Processors are designed to utilize ASCII as the primary communications code. However, system requirements for operation with many remote devices dictate the need for a multilingual capability to match all devices expected to exchange information with the Spectra 70 Systems. The communication controls are designed to exchange data over the standard interface with an eight-bit plus parity character. Data exchange over the communication lines is made to match the remote device.

Communication controls on the Spectra 70 provide horizontal and vertical parity checking in accordance with the rules governing these checks as dictated by the remote systems that are attached. Features are also included to validate constant-ratio codes, to detect no-data times-outs, and to recognize communication facility malfunctions.

Two types of controls are supplied in the Spectra 70 family. Single-channel controls are provided for high-speed data interchange as required between processors, while a multichannel controller is used when many lines are required.

Single-Channel Controls

Spectra 70 processors can communicate with other RCA processors via communication lines at speeds up to 40,800 baud. All communications are carried out in the native code of the remote processor. Interconnections with Spectra 70 processors can be accomplished in EBCDIC

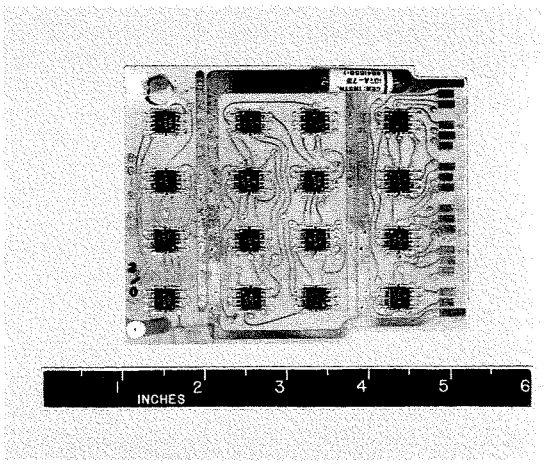


Fig. 1—Logic plug-in containing integrated-circuit packages.

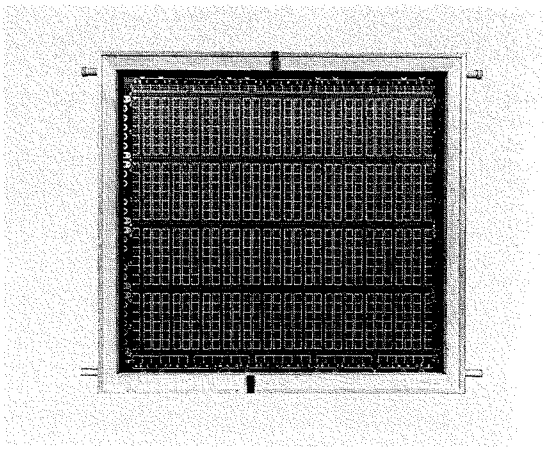
or ASCII codes while interconnections with the RCA 301 or 3301 processors are accomplished in RCA 301 code. Half-duplex operations is utilized on either private line or the message network facilities. Automatic answering and calling features can be provided when utilizing the message network.

Multichannel Controls

Multichannel operation for the Spectra 70 Series is provided by the Model 70/668 Communications Controller-Multichannel and associated line buffers. The 70/668 is provided in three models to service 16, 32, or 48 communication lines. Interconnection with the processor is made via a multiplexor trunk to provide the simultaneous operating capability required.

Each 70/668 can maintain a total communications lines rate of 6,000 bytes per second. Communications lines serviced may be up to 2,400 baud, with a separate feature available permitting operation with the AUTODIN network at 4,800 baud. Additional 70/668's can be connected to the multiplexor channel to provide for additional through-put or for a larger number of lines.

Fig. 2—A multilayered, printed-circuit back panel.



Line buffers operate in conjunction with the 70/668 to provide the multiline capability. Buffers are provided to control each of the major line terminals provided by the common-carriers.

DESIGN PHILOSOPHY

The prime design criteria of the Spectra 70 series was to utilize the latest technical development consistent with equipment schedules. This concept produced an advanced series of computing systems which can be effectively and efficiently used to solve present and future problems. The use of advanced technology is primary lever in achieving higher performance at lower cost.

Logic Circuitry and Packaging

The logic circuitry utilized in the 70/15 and 70/25 computers and peripheral controllers is a diode-coupled *nand* circuit utilizing silicon semiconductors. This basic gate provides for two levels of diode gating to the input of the inverter. The output of the inverter can be tied to other inverter outputs to effect a *phantom or*. This basic gate has a pair delay of 60 ns with a fan-out of 15. Twelve such gates are packaged on a plug-in module card of 4.3 × 7 inches. Forty of these cards can be plugged into a back panel.[2] The back panel provides the interconnections between the plug-in cards. A high percentage of these interconnections are provided by a printed circuit board[5] attached to the back panel. The remaining interconnections are made by discrete wires which utilize wire-wrap. A standard cabinet 48 inches wide by 62 inches high can contain up to 18 rows of these back panels.

Because of the later delivery requirements for the 70/45 and 70/55 computers, it was possible to incorporate monolithic silicon integrated circuits[6,7] for all logical functions. Utilization of these integrated circuits permits high internal operation speeds to be achieved because of the inherent speed of the circuit and by the compact packaging it permits. The gate configuration is an emitter-coupled-current-mode circuit[7] with dual-polarity outputs. Either output has the capability of *phantom or* operation. Worst-case pair delays of 25 ns are achieved with a 30% noise immunity in either direction of the signal swing. Only one power supply voltage is required.

These gates are packaged in 14-lead flatpacks that are of two standard types: a single 8-input gate per package, and a dual 4-input gate per package. Fig. 1 shows a plug-in card containing 16 flatpacks. The size of this card is 3 × 4 inches. It consists of two printed circuit layers interconnected by plated-through holes with a ground plane sandwiched in between.[2,6]

These module cards are plugged into a multilayer printed-circuit back panel[5] 17 × 17 inches in size (Fig. 2). The back panel, or *platter* provides printed-wire interconnections between the plug-ins and maintains a controlled characteristic impedance of 100 ohms. This platter has capacity for 104 plug-in cards plus 26 cable cards used for inter-platter connections. Approximately 95% of all connections within a platter are achieved by the printed circuit wiring. The additional interconnections are achieved by discrete wires wire-wrapped to plug-in receptacles soldered into the back panel.

Scratch Pad Memory

Both the 70/45 and 70/55 computers utilize a high-speed scratch-pad memory[4,11] as an integral part of their data structure. This scratch-pad memory stores 128 words of 32 bits each. The 128 word locations provide for general hardware registers, input-output control registers, and instruction execution registers. Each of the four program states is provided with a unique set of registers, thus saving significant computing time in the servicing of various interrupt conditions. The scratch-pad memory consists of an array of 30/10 ferrite cores utilizing two cores per bit. The memory is operated in a linear-select fashion. It provides full word access at 120 ns with an overall cycle time of 300 ns.

Main Memories

All four computers utilize coincident-current magnetic core memories.[4] These memory speeds range in access time from 2 μs for the 70/15 down to 0.82 μs for the 70/55. The memories range in capacity from 4,096 bytes to 524,288 bytes (Table II). The memories for the 70/15, 70/25, and 70/45 utilize 30/18 cores. The high speed of the 70/55 memory is achieved by utilizing a 20/12 core.

Read-Only Memories

The complexity and speed requirements of the 70/45 computer is well matched to the use of a control concept based on elementary operations. This control concept requires a read-only memory[4] to store elementary instructions. A read-only memory technique is economical when the computer's control structure exceeds a given level of complexity. Since the 70/15 and 70/25 computers execute a subset of the Spectra 70 instructions, it was determined that wired-in control logic techniques were applicable to these computers. On the other hand, the speed requirements of the 70/55 also dictated the use of wired-in logic for its control structure.

The read-only memory for the 70/45 computer consists of basic modules of 1,024 words, each word being 53 bits in length. Four such modules of memory, totaling 4,096 words, can be accommodated by the computer. Only 2,048 are required to implement the 70/45 instruction complement. The remaining modules can be added to provide hardware simulation of other machines. Each module of memory (which has a memory cycle time of 960 ns) is operated in an interleaved fashion—thus providing an effective cycle time of 480 ns.

CONCLUSION

The basic design philosophy of the RCA Spectra 70 Series incorporates the following salient points:

1) The use of new industry standards in character codes and data formats.
2) A family of systems with machine language compatibility.
3) System flexibility and economy by the use of a Standard Interface between all processors and peripheral equipments.
4) A powerful communication capability which interfaces with a variety of existing and proposed communication facilities.
5) A versatility for handling data processing, real-time, and scientific applications from the small user to the very large.
6) Greatly enhanced cost-performance ratios by the utilization of advanced hardware technology.

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5. G. H. Lines, E. A. Szukalski and F. X. Thomson, "Photochemical Laboratory—Processes for Integrated Circuit Multilayer Printed Wiring," RCA ENGINEER, *this issue.*
6. S. E. Basara, "The Impact of Monolithic Integrated Circuits on Computer Design," RCA ENGINEER, *this issue.*
7. M. D'Agostino and H. V. Criscito, "Current-Mode-Logic Integrated Circuit for the Spectra 70/45 and 70/55," RCA ENGINEER, *this issue.*
8. S. Klein and J. L. Miller, "Videoscan—High-Speed Optical Reader for Computer Input" (*Reprint PE-235-8*); RCA ENGINEER *10*-1, June-July 1964.
9. W. R. Lonergan, "Emulation on RCA Spectra 70 Systems," WESCON, San Francisco, Calif., Aug. 24-27, 1965; *Conf. Proceedings.*
10. A. J. Torre, "High-Speed Optical Character Readers," WESCON, San Francisco, Calif., Aug. 24-27, 1965; *Conf. Proceedings.*
11. A. T. Ling, "The Scratchpad Oriented Design of the RCA Spectra 70," Fall Joint Computer Conf., Las Vegas, Nev., Nov. 30-Dec. 1-2, 1965; *Conf. Proceedings.*

PERIPHERAL EQUIPMENT FOR SPECTRA 70

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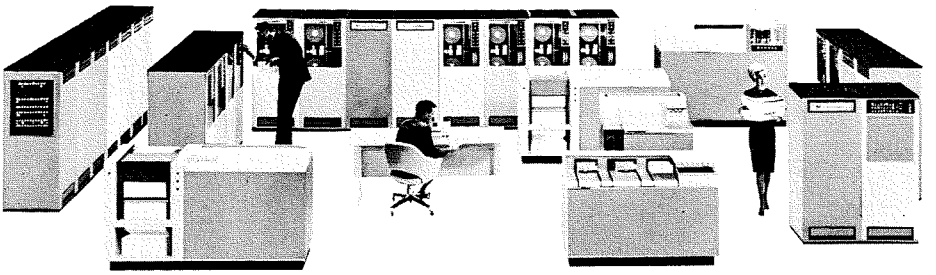

Fig. 1 — A typical Spectra 70 computer system equipment complement.

This paper emphasizes the role of peripheral equipment in the system design of the Spectra 70 series of computers. Computer system compatibility within the RCA computer product line, and with other manufacturer's equipment is reviewed with attention to the role of standards for punched cards, paper tape, magnetic-ink characters, optical readers, magnetic tape compatibility, etc.

SUCCESSFUL suppliers of data processing equipment concern themselves with the complete computer system; RCA is no exception, since efforts of RCA Electronic Data Processing are oriented toward the sale of *complete* computer systems. Such computer systems can be divided, from a hardware point of view, into two classes: 1) the basic processing unit, and 2) peripheral equipment.

From the users point of view, there is more to a complete computer system than processor and peripherals; his concern is greater than the hardware which stands on the floor. He must be supported by and provided with the necessary instructions and tools to effectively and economically use this data-processing equipment. Such tools may encompass programs and programming support as well as service and maintenance. When these added services and fringe requirements are included as actual components of a complete computer system, very few suppliers can claim full coverage; however, RCA is a member of the exclusive minority.

WHAT IS PERIPHERAL?

Identifying all equipment external to the basic processor unit as *peripheral* carries with it a misleading connotation. Granted, the basic processor is the central nervous system of a computer installation; but, the input-output equipment can hardly be classified as "incidental to" or "on the fringe of" the system. An analysis made by any standard—whether it be by weight, volume, number of plug-ins, feet of wire, or dollar volume—reveals that *the peripheral equipments represent by far the overbearing portion of the total computer system.* This fact becomes even more evident when one measures the magnitude of the engineering and design effort provided by RCA in support of input-output equipment. For today's commercial data processing line, three engineering organizations are functioning in widely dispersed geographic locations, all dedicated to contributing to the peripheral equipment product line.

THREE RCA ENGINEERING GROUPS

Video displays and random access card equipments are designed and developed by an engineering organization at Van Nuys, California. The Palm Beach Gardens, Florida, Engineering group concerns itself with providing product line equipment which includes paper-tape reader-punches, card punches, high-speed printers, adaptation of typewriters for interrogation, as well as providing the interface for existing peripheral equipments such as magnetic disc storage devices, drum memories, bill-feed printers, and communication control equipment. The third group functioning in the peripheral design area is located in Camden which designs and develops magnetic storage devices, digital tape stations, optical character-reading equipment, punched-card readers, and communications devices.

When appraised collectively, peripheral equipments and their associated control electronics account for between 75% to 85% of a computer site's total monthly rental. The major portion of peripheral equipment rental comes from storage devices—currently predominant are digital tape stations.

THE SPECTRA 70 FAMILY

RCA took a bold and far-reaching step in 1964 with the announcement of the new Spectra 70 line. At that time, four new processors and 40 peripherals were offered as the initial members of a family of computer systems designed for extended use reaching into the 1970's.

Family Appearance and Function

To achieve an integrated and complete system concept was a major undertaking. A coordinated effort was required among the widely dispersed groups to formalize and maintain a common theme of appearance, function, operability and interchangeability. Without success here, engineering innovation and invention, whether it be in mechanics or electronics, would not have its full effect. Fig. 1 shows a typical systems complement for Spectra 70.

Compatibility

The peripheral equipment designer's main concern is the issue of compatibility. Spectra 70 is program-compatible with the IBM System 360 and in most cases is also data-exchange compatible. The ability to exchange data between competitive systems is a major peripheral equipment design task.

The physical standards such as document size and characteristics, punched-hole size and location, and coding formats are well defined parameters for the punched-card unit record and punched paper tape. As a result, both media are in wide use for the bilateral exchange of data between competitive systems. When established tolerances are reasonably met, industry systems may "talk" to each other successfully

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Fig. 2 — A sample of the standard character set.

and are considered compatible. RCA's equipments are meeting these established standards.

Definition of Standards

When the printed information on a document is used as input, standards are less well defined than for punched cards and punched paper tape. Consequently, only limited data exchange is possible within the industry. The most standardized printed-document format is the *magnetic ink character reading system* (MICR); this method is approved for the exchange of data among American banks and is commonly used on checks (Fig. 2).

By virtue of this standard, documents printed as outputs from one computer may be used as inputs to any other computer system as long as it is equipped with the appropriate input peripheral.

A second exchange media exists for printed documents: this system uses characters printed with regular ink by computer-controlled printers or off-line printing equipment such as typewriters. The inputting of this information is done by *optical character reading* (OCR). Two major factors have restricted the growth of this media; the first being the lack of an industry-standardized type font; the second is the lack of a print-quality standard. Some of the industry's existing and proposed numeric fonts are shown in Fig. 3. The print quality standard is equal in importance for successful reading to the standards for the location and size of a punched hole. In some cases, reentry of data within a system can be achieved without this standardization since the font and print quality may both be controllable; however, the exchange of data between competitive systems must await the adoption of formal standards. Growth and expansion of this media will accompany standardization. In the interim, the excellence of relative systems can only be measured qualitatively by the system's tolerance to printing defects.

Magnetic Recording Compatibility

Compatibility among devices using magnetic recording as the data media exists only partially. To evaluate the significance of this, it is first necessary to establish the need for the exchange of data when it is stored in this form, and secondly to determine the physical practicality of achieving this exchange.

For instance, very large disc files whose discs are three feet in diameter, delicately and dynamically balanced, maintained in a sealed and antiseptic environment, are hardly good candidates to achieve a physical exchange of data. Likewise, magnetic-drum storage files, unless very small, are too bulky and impractical as a means of exchange. Another extreme case is where the magnetic file is huge, storing information in the order of a quarter of a billion characters, as in RCA's Mass Storage Unit or even IBM's Data Cell. It is seldom a requirement to exchange *all* of the information; therefore, in this case, negating the need for compatibility.

On the other hand, digital magnetic tape stations are often called upon to accept data from other systems and are required also to prepare data suitable for direct entry into competitive systems. The problems in doing this are numerous. First, is the fact that magnetic tape standards are not available which completely define all pertinent parameters. This is overcome by designing equipment which is in tune with the maximum number of competitive equipments, resulting in the broadest market coverage. Another problem stems from the fact that information is stored on tape in blocks. To access these blocks, the tape reader must be capable of getting up to its stabilized tape speed in a predetermined time. It must further be able to stop within a prescribed time and position so that a subsequent read may be executed in either the *forward* or the *reverse* direction. These are unique and demanding requirements exclusive to magnetic tape storage.

Designs to meet these *start-stop, forward-reverse* commands within the required interval have taken many forms. The medium- and low-speed Spectra 70 tape stations use a single-capstan drive directly coupled to a very-low-inertia DC motor. A typical *start-stop* command for a tape speed of 75 in/s is shown in Fig. 4. These *start* and *stop* times are adequate to handle data in blocks separated from each other by 0.6 inches and to allow a reading to occur 0.15 inches from the *write* gap for data validation. The duty cycle for these *start-stop's* is determined by the data-block length and, at 75 in/s, can go as high as 80 c/s. Two data track formats are in use today, seven and nine channels. Spectra 70 provides both.

We have so far examined the data exchange compatibility requirements for electromechanical equipments. As the name implies, information which at one time was contained in an electrical signal is converted into a mechanical form, physically carried to a reading mechanism, read and reconverted back to an electrical signal. Data communications require that information be exchanged between two points and possibly between competitive equipments. The problem of compatibility, however, is substantially simplified, since information remains as an electrical signal in the process of carrying the data from point to point. All that remains is for the information coding to be standardized so that the language in use is the same; this feature has been incorporated in Spectra 70 family of equipments.

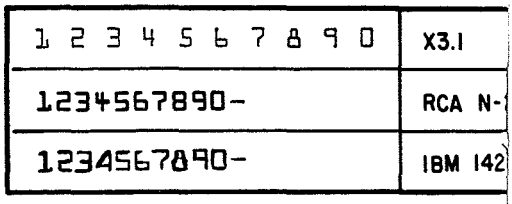


Fig. 3 — Some of industry's existing and proposed numeric fonts.

Standard Interface

The system architects of RCA's new computer family have also gone one step further in providing to the user the ultimate in compatibility. All peripheral equipments have been designed to conform to a *standard interface*. This feature makes all peripherals appear the same to a processor and all processors look the same to a peripheral. By this means, complete freedom of peripheral equipment hook-up is achieved.

For RCA, the issue of compatibility is not a new one, and its importance has long been recognized in many of our businesses. To the design engineer, once it has been specified as a design criteria, it offers a challenge. It is analogous to the solution of the classical problem of radio communications for which RCA is well equipped. Once the wavelength is specified, the most reliable communication is achieved by the combined use of the most powerful and stable transmitter coupled to the most sensitive and noise-tolerant receiver.

RELIABILITY

Only part of an engineer's job is complete when he has designed in the means to communicate data using the various media in today's computer systems. Customer satisfaction and RCA-EDP success are intimately associated with machine reliability. Through records maintained by the field service organization, it is possible to reach some basic conclusions on the reliability of RCA's pre-Spectra 70 equipment.

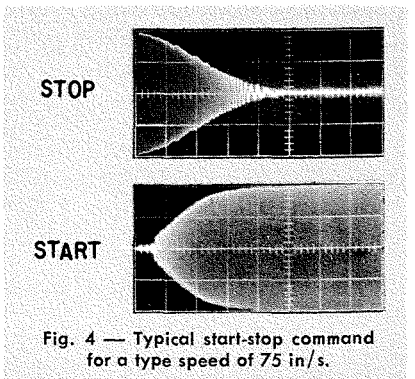


Fig. 4 — Typical start-stop command for a type speed of 75 in/s.

A. J. **TORRE** graduated from the University of Oklahoma in 1943 with a BSEE, and has an MS from Drexel Institute. From 1943 to 1945, he worked on RCA airborne radar design development, transceiver design of an AM altimeter and an aircraft tail warning device. From 1945 to 1950, he worked on advanced black and white TV receiver design, AM and FM home radio design and some components design. From 1950 to 1961, Mr. Torre was Manager of Electrical Engineering Color TV Receiver Design where he made fundamental contributions to the design of the color system and its products. In addition, from 1958, he was Home Instruments Manager of Remote Control Systems Design. Mr. Torre's initial entry into EDP was in January, 1961, as Manager of Optical Character Recognition Development. In this capacity, he directed the development of RCA's first commercial optical character reading machine, the Model 5820. He is presently Manager of Peripheral Product Engineering of EDP, being responsible for the development of advanced high-speed printers, and document handling equipment such as punched card readers and paper handlers. Mr. Torre is a member of Tau Beta Pi, Sigma Tau, Eta Kappa Nu, and Phi Eta Sigma. Mr. Torre is a Senior Member of the IEEE, and is a registered professional engineer in New Jersey. He has 17 U.S. patents issued and one pending.

An analysis was made of the four individual existing systems; i.e. RCA 301, 501, 3301, and 601; another analysis was made for cases where all systems were merged into a single large hypothetical system encompassing all equipments. The performance criteria used was the average MTBF over a 6-month period plus the average time to repair each equipment during the same period. Although these parameters are a meaningful and sound basis to use, they tell only part of the story. For instance, the time and cost of preventive maintenance is not accounted for, nor is the cost of machine time required to reconstruct data lost as a result of an equipment failure. New equipments do not show up as well as older equipments due to the necessary learning period required to minimize the average time to repair.

For ease of analysis, an EDP system may be divided into the following seven classes of equipments:

1) *Processor*
2) *Paper Tape:* reader, reader-punch, punch.
3) *Punched Card:* reader, reader-punch, punch.
4) *Printers:* typewriters, monitor printers, high-speed line printers.
5) *Magnetic Recording Files:* small-disc, large-disc, tape stations.
6) *Switching Equipment*
7) *Special Peripherals*

Within each class there are many variables such as memory size, speed, data rate and capacity, duty cycle, ratio of passive-to-active elements, and mechanical energy expended; nevertheless, several apparent reliability trends are easily observed.

A graphic representation of the range of data for the combined single system case is shown in Fig. 5; in this example, one each of all existing processor types is assumed as part of the system along with one each of all existing peripherals, except tape stations for which six tape decks were assumed.

In general it can be concluded that the processors vary around the mean in accordance with the processor size and complexity. For the peripherals, paper-tape equipment is always better than average, and card equipment poorer. Surprisingly, printing equipment, both fast and slow does not vary much from the mean. Reliability of magnetic recording files is poor for disc type files and covers a wide range for tape stations. No predominant or conclusive trend for reliability versus transfer rate was apparent in the details for each of the various tape station models, except that learning time appears important with respect to reducing the mean time to repair. Switching devices are all better than average with the passive type out-performing the electromechanical type. The superiority of passive switching devices over other peripherals which are usually mechanically oriented is not too surprising or unexpected.

The analysis is useful since it factually presents to the design engineer the most fruitful areas requiring improvement. The reliability profile for Spectra 70 has been specified, and the goals are high.

FUTURE COMPUTER DESIGN TRENDS

We have, so far, concerned ourselves with current peripheral equipment design problems. It is of some interest and value to speculate and observe design trends for the peripheral equipments of tomorrow. Historically, there has been a steady increase in the transfer rate for all peripheral equipments. More recently, however, this design characteristic has been growing at a slower rate than in the past.

To achieve greater reliability, peripheral equipments have steadily migrated away from the purely mechanical toward a greater emphasis on electronic design. An example of this is the single capstan drive for the Spectra 70 model 70/442 tape station. An almost purely electronic approach is used to achieve the precise *start-stop* characteristic, in contrast to the earlier purely mechanical approach of a pinched-roller drive (Fig. 4).

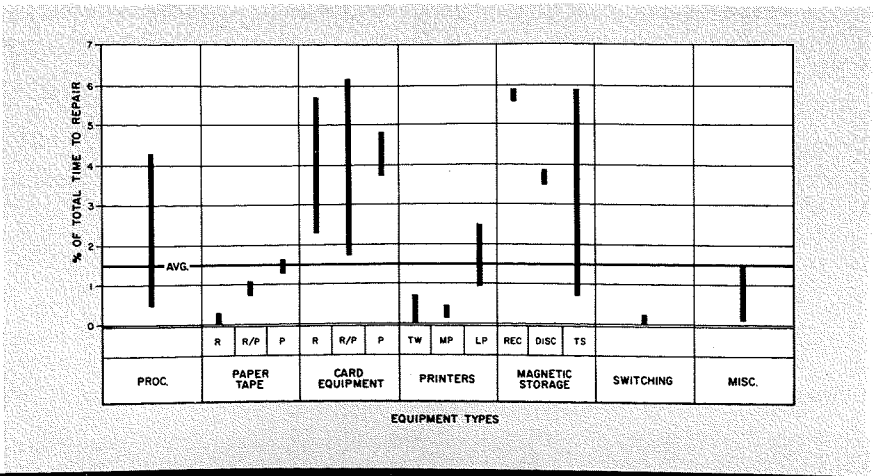
To accommodate efficiently the ever increasing demand for data handling, the access time to interrogate records has been made shorter and shorter. For instance, tape stations have increased their transfer rates from 33 to 120 kilobytes over the last three years. Card readers have been modified to respond within a short interval, and to a feed instructions so that processing of data may be interleaved with other operations. Random access files are becoming predominant; access times range from 8.5 to 385 milliseconds.

Although not a part of RCA's current announcement on Spectra 70, peripheral equipments are available in the industry which respond with a voice-sound output upon interrogation. Equally exotic equipments are in development and being experimentally tested that are capable of reading handwritten information.

CONCLUSION

The Spectra 70 peripheral equipment product line offers a wide range of models exhibiting an integrated styling, and incorporating a maximum of the data processing industry's existing compatibility features. Peripherals constitute the major portion of a system, and their reliability is of utmost importance. Based on past history, card equipment and magnetic recording disc files are the areas requiring the most improvement. Equipments of the "future" will be somewhat faster, will access data more quickly, may read handwriting, and perhaps may even talk back.

Fig. 5 — Representation of the range of data for the combined single-system case.



INTERNAL LOGIC STRUCTURE OF THE SPECTRA 70/45

The RCA Spectra 70/45 is a stored-program, general-purpose digital computer implemented with monolithic silicon integrated circuits. One of its main features is the logic control method. As described herein, the internal logic is controlled by the prestored information in a read-only memory. Each word (53 bits) in the read-only memory is called an elementary operation and is divided into eleven sections to perform different tasks independent to the instructions. A group of elementary operations executed in a particular sequence becomes an instruction. One of the main advantages of using this method is the flexibility of the design. This unique feature enables the Spectra 70/45 to be compatible with the Spectra 70/55 and simulates other existing computers, such as the RCA 301, RCA 501, and IBM 1401, without redesigning the basic processor.

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Logical Design
Electronic Data Processing, Camden, N. J.

THE RCA Spectra 70/45 computer system is designed not only to handle business data processing but also scientific, real-time, and communications applications. This is possible because of the extreme flexibility of the system, which is distinguished by:

1) 1.44-μs main memory—basic memory provides 16,384 nine-bit bytes of storage. (Note that *one* byte of data is equal to *eight* bits in storage and in certain other portions of the machine a ninth parity bit is added.) It can be expanded to a maximum of 262,144 bytes of storage.
2) 300-ns micromagnetic memory—provides 128 four-byte words storage. It contains all general, utility, and address registers.
3) Read-only memory with 480-ns effective cycle time for logic control uses.
4) Simple maintenance panel—provides all man-machine communication facility.
5) Efficient and simple interrupt system.
6) High-speed monolithic-silicon integrated circuitry with a pair delay of 14 ns when driving a typical load.
7) Sophisticated input-output control—provides facilities for 256 input-output devices operating at one time.

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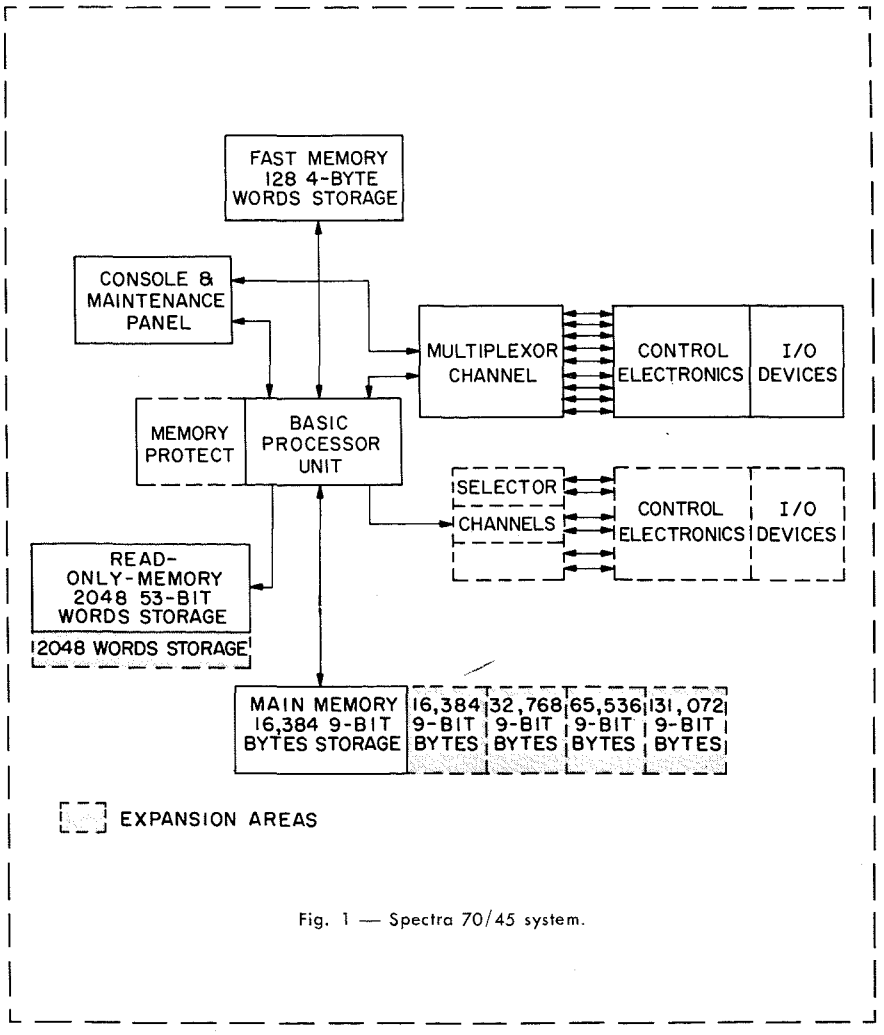
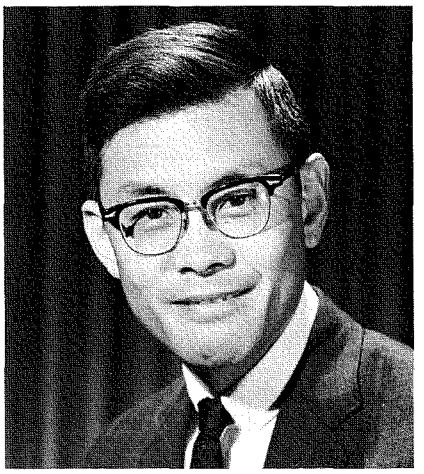


Fig. 1 — Spectra 70/45 system.



R. H. YEN received his BS from Brown University, Providence, R. I. in 1953 and his MS in applied physics from Harvard University in 1954. He joined RCA EDP Engineering and was involved in the design and testing of the 501 computer. This assignment continued until 1959, when he shifted his activity to the group which generated the logic design of the 301. Promoted to leader in 1960, he supervised the testing of the 301 processor and was active in the logic design and testing of some of its control modules. From 1962 to 1964 he supervised the detailed logic design and prototype testing of the 3301 processor and of its high-speed arithmetic unit for scientific applications. Following the completion of this assignment he was assigned the responsibility of the Spectra 70/45 processor logic design and supervision of its logic checkout. The testing of this prototype has proceeded smoothly and rapidly; particularly significant in view of its many innovations. He is a member of the Brown University Engineering Honor Society and of Tau Beta Pi. He was a member of a group nominated from EDP Engineering for the David Sarnoff Outstanding Team Award in 1959 and leader of the group to receive the same nomination in 1963.

8) Emulation of other existing or, perhaps, future computers.

The use of the *read-only-memory* (ROM) can be singled out as the most important implementation feature of the 70/45 System. There are two basic advantages:

1) The control logic is simpler and more uniform than that of the conventional status-level wired logic machines. All the *elementary operations* (EO) are defined independently of the instructions so that internal control logic is a function of the EO's only. Because of the small number of generalized EO types required in the system, a simpler control logic organization is required. This more simplified control logic makes it an easier machine to maintain and trouble-shoot.
2) The flexibility of adding or modifying instructions is another advantage. Changing the content of the ROM is a much easier task than that of altering the circuitry of the existing logic. Moreover, adding EO words within the capacity of the ROM does not represent any additional equipment cost for the system. The size and speed of the ROM are, of course, very important to make the EO concept useful.

BASIC PROCESSOR UNIT

Elementary Operation (EO) Format

Each EO consists of 53 bits, divided into 11 fields. In each segment of the machine, every field has a unique meaning independent of the operation code. The arrangement of the EO bits is as follows, where the X's represent bits and the upper case letters represent fields of which they are mnemonic.

```
XXX XXXX XXXXXXXX XX XXXXXX XXXXXX
 F   V      C     M  S     D
                  XXXXXX XXXXXX XXXXXX XXXXX X
                    T      N      A     E   I
```

1) *F-field (3 bits):* The *F*-field is equivalent to the operation code of an instruction. There are seven basic EO types with variations in most types. These general functions are: *shift, test and branch, set condition code, increment, generate constant, act function and perform,* and *perform.* This field also defines the types of arithmetic operation such as *addition, subtraction, and, or,* etc.
2) *V-field (4 bits):* The *V*-field (variation) assists the *F*-field to further clarify the detail and variation of a given EO function. For instance, in the *shift* EO, *V*-field specifies the type *(algebraic* or *logical)* and direction *(left* or *right)* of shift.
3) *C-field (8 bits):* The *C*-field controls the byte indicator of various registers. Also, it controls the setting, resetting, and triggering of all the control counters.
4) *M-field (2 bits):* The *M*-field indicates whether the operation is to be *reading* or *writing.*
5) *S-field (6 bits):* The *S*-field identifies a hardware register from which data is transmitted. Also, it can specify a register contained in the scratch-pad memory if *M*-field indicates a scratch-pad memory operation.
6) *D-field (6 bits):* The *D*-field identifies the hardware register which is the destination of the transmitted data. Each register has a unique source or destination code assigned to it.
7) *T-field (6 bits):* The *T*-field specifies the condition to be tested by a given EO such that the branch address of the next EO can be determined. Since the ROM requires definite access time, the test is performed in the beginning of each EO in order to have the next EO ready in time for execution.
8) *N-field (6 bits):* The *N*-field specifies the address of the next EO if the result of the test is *false.*
9) *A-field (6 bits):* The *A*-field specifies the address of the next EO if the result of the test is *true.*
10) *E-field (5 bits):* The *E*-field specifies mainly the various exception checks for program interruption. Also, it is used to indicate *unconditional jump, end of instruction, end of staticizing,* etc.
11) *I-field (1 bit):* The *I*-field inhibits input-output servicing from breaking in between the present and the next EO. This enables the processor to continue its correct operation to a convenient stopping point before turning the processor over to an input-output operation.

Read-Only Memory and Its Operation

The overall cycle time of the ROM is 960 ns, consisting of a 360-ns access time and a 600-ns recovery time. In order to improve the effective cycle time to 480 ns, the memory unit is divided into two banks, an *even bank* and an *odd bank.* While one bank is recovering from the previous cycle, the other one can be addressed (Fig. 2).

Each bank of the ROM consists of 53 *E*-cores with each core representing a bit in the EO word. The core has two apertures and a sense-winding attached to the center pole (Fig. 3).

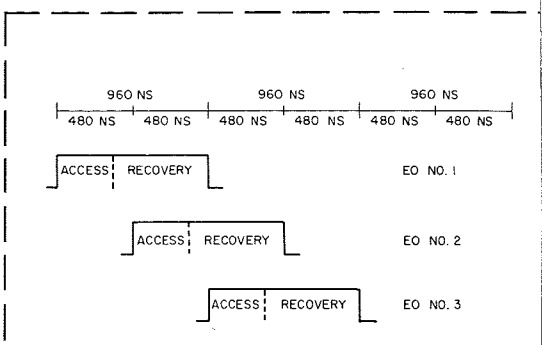


Fig. 2 — Read-only-memory (ROM) cycle time.

Each of the 1,024 wires (representing 1,024 words) is threaded through either the *0* side aperture or the *1* side window of every one of the 53 cores as required. When an EO word is addressed, the wire representing that word receives a current. The sense of a current passing through either window of the *E*-core determines the sense of the voltage on the sense winding. The sense windings feed the flip-flops, which make up the ROM memory register. The wiring of the *E*-cores is shown in Fig. 4.

In Fig. 4, EO word *1* and *3* would have the following meaning

EO word *1:* *0101.....1*
EO word *3:* *1001.....0*

The time relationship between EO fetching and execution is:

	480 ns	*480 ns*	*480 ns*	*480 ns*	etc.
Fetching:	EO1	EO2	EO3	EO4	*etc.*
Execution:		EO1	EO2	EO3	*etc.*

The ROM can be expanded to 4,096 words by adding another even and odd bank set.

Since 4,096 words require 12-bit address and *A*- and *N*-fields have only 6 bits each, each EO can only branch within a 64-word block (leaving the six most significant bits of the address unchanged). In case branching to an address outside of the 64-word block is required, *A*- and *N*-fields are combined to form a 12-bit address.

Fig. 3 — E-core.

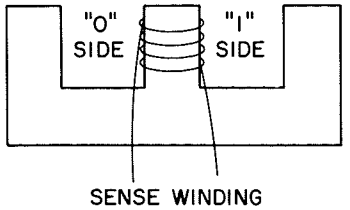
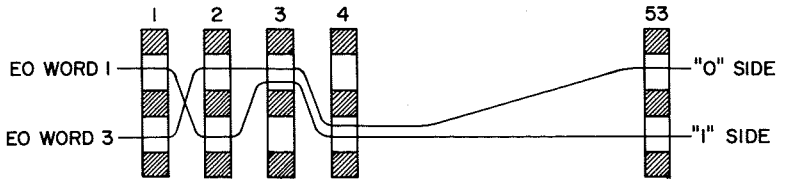


Fig. 4 — Wiring of the elementary operation (EO) words.



Main Memory

The main memory uses magnetic-cores in coincident-current organization. The minimum capacity is 16,384 bytes and maximum 262,144 bytes. There are three other capacities in between for expansion (32,768 bytes, 65,536 bytes, and 131,072 bytes). The memory is 2 bytes in depth with a parity bit associated with every byte. The memory cycle time is 1.44 μs, which is equal to three EO access times. Hence, whenever the main memory cycle is initiated, the three EO's associated with that cycle are tied together by using the *I* bit in the EO format to prevent possible interruption of an operation to provide service to input or ouput devices.

The main memory also has an additional non-program-addressable portion associated with it for input-output use. This portion of memory is called *shaded memory*. The capacity of the shaded memory varies with the main memory:

Main Memory	*Shaded Memory*
bytes	bytes
16,384	1,024
32,768	2,048
65,536	4,096
131,072	4,096
262,144	4,096

Fast Memory (Scratch-Pad)

The fast memory (or scratch-pad memory) consists of 512 eight-bit bytes (every two bytes share a parity bit) arranged in 128 locations of four bytes each. The *read* cycle is 120 ns and the *write* cycle 180 ns. This memory contains all general registers, floating-point registers, various address registers, utility registers. Every location is addressable by program through the load and store scratch pad instructions.

Program Interrupt

The processor is equipped with four program states, with each one having its own set of registers. The use of the different program state is as follows:

Program State No. 1: User's Program
Program State No. 2: Executive Routing
Program State No. 3: Interrupt Analysis
Program State No. 4: Hardware Error Interrupt

All the interrupt conditions will lead the program into States *3* with the exception of power failure and parity error, which force the program to go to State *4*. There are a large number of interrupt conditions designed to detect possible programming errors, such as *address error, date error, divide error, fixed-point-overflow,* etc. Whenever a bit of the interrupt register is set, the interrupt scanning sequence is either initiated immediately or at the end of the current normal processing instruction, depending upon the type of interruption. A special EO routine is used to examine the interrupt condition, as well as the interrupt mask register of the current program state. Once interrupt is permitted, program control is switched from the current state to the State *3* or State *4* depending on the nature of the interrupt. A weight associated with the interrupt condition is generated and stored into the interrupt weight register in the scratch-pad memory. If further interrupt does not occur, the first instruction specified by program counter of the initiating state will be staticized. At the end of the interrupt routine, the program control instruction switches the machine back to its original program state and the interrupt flag register is examined again. If there is further interrupt condition pending, the whole interrupt procedure will be repeated. Otherwise, the original program being interrupted will resume. There is no logic built in to prevent interrupt upon interrupt. This can only be inhibited by masking all interrupts off by program. Therefore, multi-level interrupt is completely controlled by software.

The interrupt feature is also useful for program debugging. A program debugging option can be set and removed by program. During the use of this facility, the completion of every processing instruction causes interrupt to take place. Consequently, the main program will be detoured to a subroutine as previously described. Through the instructions in the subroutine, the computer can perform all necessary housekeeping tasks for an effective program debugging.

Character Code

The 70/45, like all members of the Spectra 70 family, is designed to handle either the *Extended Binary-Coded-Decimal Interchange Code* (EBCDIC) or the *American Standard Code for Information Interchange* (ASCII) extended to eight-bits. The selection of the code is done by setting a program switch. Only the instructions operating on packed data and producing signed or zoned results are code sensitive and others are code independent. Input-output devices involving code translation such as card reader, card punch and printer are also code dependent.

Privileged Instructions

There are thirteen instructions classified as *privileged instructions.* Every program state can be set to the privilege mode by program. The privileged instructions will cause interrupt whenever they are attempted in the non-privileged mode. When this happens, the instruction function is suppressed. The privileged instructions are:

set storage key
insert storage key
write direct
read direct
diagnose
start device
test device
halt device
check channel
program control
load scratch pad
store scratch pad
idle

Memory Protect

The content of the main memory can be protected from destruction during the execution of a program. The main memory is divided into blocks of 2,048 bytes with a four-bit storage key associated with each block. Whenever the main memory is addressed for writing, the storage key is compared with the protection key. The detection of a mismatch causes a program interruption. The storage keys are stored in a small micromagnetic memory with the capacity of 128 four-bit words. The characteristics and speed of this memory are the same as that of the scratch-pad memory. The memory protection is not included in the basic machine. It can, however, be obtained as an option.

Maintenance Panel and Console

The 70/45 processor provides a maintenance panel located on the side of the power supply rack and a free-standing console. The maintenance panel is strictly for hardware trouble shooting and routine maintenance uses. It contains over 150 lights and switches for direct access and display of all key signals in the machine. Wired in logic allows immediate access to all three memories. The operator is provided with a simplified console which, in conjunction with the console typewriter and an executive routine in main memory, allows efficient man-machine communication.

INPUT-OUTPUT CONTROL

Every input-output device is connected to the basic processor via an input-output channel. Each channel communicates with the main memory and the input-output device with a minimum interruption to the normal program mode. The nonbuffered device interrupts the normal mode whenever a single data is ready to be transferred to or from the main memory. The buffered device can accumulate the required number of bytes of data appropriate to the particular input-output device before program intervention is signaled to the basic. These input-output channels make the simultaneous operation possible. Each channel keeps track of the address and count that describe the data in the main memory. Every input-output device is connected to a channel via the RCA

standard input-output interface. The interface provides the same signal format and sequence to all input-output devices.

There are two types of input-output channels, *selector* and *multiplexor*. The selector has higher priority than the multiplexor for servicing. The scanning of all channels takes place continuously in a sequential fashion. The scanning process halts temporarily when a channel is being serviced. Scanning always returns back to the channel of higher priority after servicing of another channel is complete. Servicing time is different for the multiplexor and selector.

Multiplexor Channel

The multiplexor channel has the bottom priority for servicing among all the channels. It provides up to nine input-output trunks, and the ninth one is reserved exclusively for the console typewriter and cannot be used for any other device. Through the remaining eight trunks, a total of 256 devices may be connected to the multiplexor channel, and it is possible to have them all operating at the same time. Each one of the 256 devices requires three 32-bit word registers located in the shaded memory. Therefore, the number of devices which may be connected to the multiplexor channel is a function of the capacity of the main memory and the data rate of the device.

Capacity of Main Memory bytes	*Number of Devices*
16,384	64
32,768	128
65,536	256
131,072	256
262,144	256

The multiplexor channel can handle data transfer at the maximum rate of 62,000 bytes per second.

Selector Channel

The 70/45 processor can have as many as three selector channels connected to it. Up to two input-output trunks may be connected to each of the selector channels. It is possible to have 256 devices connected to each selector channel, however, unlike the multiplexor channel, only one may be operating at a given time. Since multiplexor has bottom priority, all the three selector channels are scanned for servicing ahead of multiplexor channel. Each selector channel has four 32-bit word registers assigned to it in the scratch-pad memory. The maximum data transfer rate for the selector channels is 465,000 bytes per second.

Mode of Operation

In the multiplexor channel, data can be transferred between the main memory and an input-output device in three modes: *multiplex*, *burst*, and *catch-up*. In the multiplex mode, the multiplexor channel is shared by all nine input-output trunks as described previously. The burst mode is selected during the initiation of a device by program. The selection of burst mode locks the multiplexor channel to one of the nine trunks. When this occurs, the multiplexor channel can neither initiate any new input-output devices nor service any input-output trunks other than the one requesting the burst mode. This situation exists until that particular trunk completes its operation. Therefore, it is important for the program to make certain that the multiplexor channel is completely free before the request of burst mode is issued. The catch-up mode is selected by hardware. Any device having backlog data in its buffer may request for service continuously, which causes the multiplexor channel to be locked into it temporarily. During this time, all the input-output trunks with lower priority will not be serviced at all. In either burst or catch-up mode, the selector channel still has higher priority in servicing.

COMPUTER INSTRUCTIONS

The computer operates under the direction of 144 wired-in instructions. These may be classified into seven general categories:

1) logical operations	32
2) branching	9
3) fixed point arithmetic	35
4) floating point arithmetic	44
5) decimal arithmetic	9
6) privileged operations	13
7) miscellaneous	2
Total:	144 instructions

Instruction formats contain two, four, or six bytes, depending upon the number of the main-memory address required for the operation. The five basic instruction formats are shown in Fig. 5. The operation code is contained in the first byte. The four-bit R, B, and X fields denote one of the sixteen general registers in the scratch-pad memory. The 12-bit D is the displacement field. The effective address is the sum of the two 18-bit integers from general registers identified by fields B and X and the 12-bit D contained in the instruction. Zeroes in the B and X fields imply that a zero quantity must be used in forming the effective address regardless of the content of general register *0*. Since RX format uses both X and B fields, it is the only format that permits double indexing. The format of an instruction is indicated by the first two bits of the operation code.

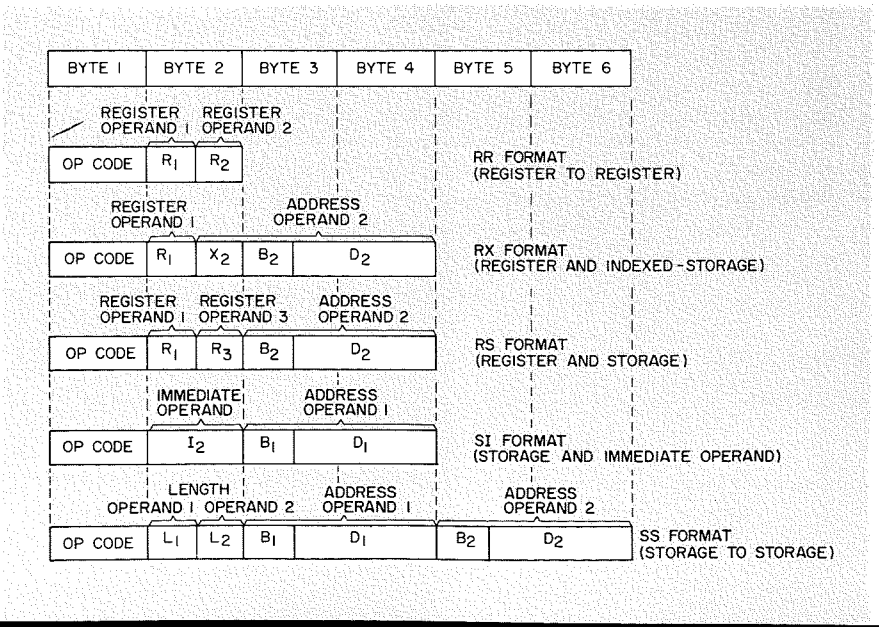
The typical instruction execution times (in microseconds) are as follows:

fixed-point addition-subtraction	5.28
branch and link	4.8
branch on condition	3.84
branch on count	4.8
fixed point compare	4.8
logical compare	4.8
fixed point multiply	65.52
fixed point divide	90.81
load	2.88
move	5.04
decimal add (8 bytes)	35.67
decimal multiply (8 bytes)	330.48
decimal divide (8 bytes)	678.17
shift left logical (15 bits shifted)	15.12
shift left algebraic (15 bits shifted)	17.28
shift right logical (15 bits shifted)	16.08
shift right algebraic (15 bits shifted)	15.36
store character	6.24
load and test	5.28
move numerics (8 bytes)	27.66
move zones (8 bytes)	27.66

CONCLUSION

The RCA 70/45 is strictly a third generation computer. The integrated circuitry, the printed-wiring packaging technique, and the ROM logic control concept make this system highly efficient as both data processor and a scientific machine. The flexibility of the system makes it possible to adapt 70/45 to the specific needs of a wide range of applications.

Fig. 5 — Instruction formats.



MEMORIES FOR SPECTRA 70/45 AND 70/55

Read-Only, Scratch-Pad, and Main

An important design problem in the memories of the Spectra 70/45 and 70/55 computers was that of achieving an efficient interface between the integrated-circuit logic of the processor and the memory drive circuitry. As a result, current-mode-logic (CML) integrated circuits are used throughout the memory logic, as are the same packaging concepts (e.g., multilayer printed back panels, or platters) found in the main processors. Described herein are the 70/45 and 70/55 main memories and scratch-pad memories, and the 70/45 read-only memory.

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SINCE the advent of electronic digital data processing systems, computer memories have held a unique position; they have been the sole analog unit in a world of digital devices. As such, they have been the recipient of concentrated activity on the part of research and development personnel. Such research led to rapid advances in the field of high-speed memories from the early acoustic delay line and electrostatic storage tube to the present transistorized core memories. Storage capacity, speed, physical size, cost and reliability all have been changed in large degrees.

An interesting outcome of this progress is the recent trend of the increasing reliance placed on memories in computer design. High-speed memories have been steadily increasing in all performance characteristics so that they now perform many functions previously done by the processing unit. Peripheral units have employed small, moderate-speed memories as a means of buffering between themselves and the central computer.

The RCA 3301 introduced the use of small very-high-speed scratch-pad memories which replaced more circuit functions of the computer. Now, RCA Spectra 70/45 computer has added a fourth variety of memory to computer design—the *read-only memory* (ROM).

The Spectra 70 series of computers has seven memory systems that serve as storage media in the four different basic processing units. The requirements of the four systems vary in size, speed and function, although all must meet standard commercial environmental conditions, and all must conform to the basic Spectra 70 common packaging requirements. Table I shows the basic characteristics of the memory systems for each of the Spectra 70 processors.

Study of Table I (which does not include any of the buffer memories) indicates the wide assortment of sizes, speeds, and functions of the storage devices. The memory systems of the two larger computers in the Spectra 70 line, the Spectra 70/45 and 70/55, are the subject of this paper.

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GENERAL DESIGN REQUIREMENTS

The Spectra 70/45 and 70/55 memory system designs require a compatibility with the electronic and mechanical aspects of their processor units. The 70/45 and 70/55 computers have an integrated-circuit current-mode-logic (CML) gate as their basic logic device. This presented a design problem, since means had to be found by which this current-steering, low-level, integrated-circuit logic could interface with high-power memory drive circuitry in an efficient manner. It was necessary to prevent the noise generated by the memory drive circuits from exceeding the noise immunity levels dictated by the requirements of the integrated-circuit logic.

It was decided to use the same type of CML integrated circuits throughout the logic design of the memories as used in the logic of the Spectra 70/45 and 70/55 processors. To allow a continuity in design and styling, packaging concepts generated for the processors were carried into the memory systems. Only standard racks, frames, circuit boards, and multilayer printed back panels were used in packaging the memories.

70/45 READ-ONLY MEMORY

The read-only memory (ROM) serves a function in the 70/45 system previously performed by logic circuitry; it stores the elementary operations that establish the instruction complement of the computer. It does this so that instruction complements can be expanded or contracted with relative ease, allowing customizing of order codes for specific customer needs. The ROM allows also a new function, *emulation* (previously not feasible), to be performed by the computer. By this process, the order codes of other computers can be translated and transformed into the order code of one desired computer, thereby allowing the one system to operate on programs written for the others. Each emulator requires a ROM of its own; thus, the emulator storage media must be easily replaceable.

Storage in the ROM is accomplished by directing a word-wire through one side or the other of an *E*-shaped core. The *E* core is a soft ferrite material and acts as a linear transformer; the magnetic path is closed around the wire by mounting a second *E* core face-to-face with the first. The mating surfaces of the legs of the *E* cores are ground to a high finish. The two cores are held together by compression to minimize the effects of air gaps. Current passed through a wire in the logical *1* opening will cause a downward field in the center leg (Fig. 1), while the same current is

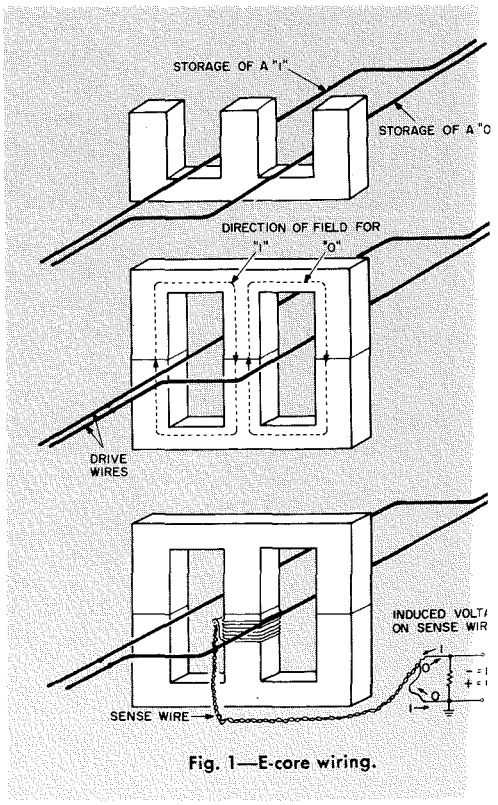

Fig. 1—E-core wiring.

driven through the *0* opening to cause an equal upward field. The change in field direction caused by a current pulse on the drive wire induces a signal on the bobbin-mounted sense wire; this signal is negative for a stored *1* and positive for a stored *0*. The *E*-core pair, therefore, constitutes one bit position containing as many words as there are wires passing through its openings. The basic 70/45 ROM bank consists of two stacks, each containing 1,024 words of 53 bits each; therefore, each stack has 53 *E*-core pairs with 1,024 wires routed through their openings. (See Fig. 2 for ROM stack wiring.)

ROM STACK WIRING

The Spectra 70 ROM drive system is word-organized and, therefore, requires a minimum of one switch per word line; selection of the proper word line is accomplished by diodes arranged in a crossbar switch-driver matrix. To allow selection of one of the 1,024 access lines necessitates 32 drivers, 32 switches, and 1,024 diodes (Fig. 3).

When the 50-mA current pulse passes through the core, a sense signal of approximately 1 volt appears at the output of the terminated multiturn sense winding. This signal is large enough to drive a standard logic gate directly; thus, no sense amplifiers are necessary. A strobe pulse interrogates the 53 sense gates and sends the data to a register located in the processor.

BARRY I. KESSLER graduated from Pratt Institute of Technology with a BEE in 1956, following service as a radio operator in the USAF. Upon completion of the RCA Specialized Training Program in 1956, he joined the Bizmac engineering group, Electronic Products Division. Here he was assigned to the design and development of a transistorized transfluxor memory system under a sub-contract from RCA Waltham. Since that time, he has been associated with the designs of RCA-EDP's core memories, from the 501 through the 3301. He was appointed Leader of the Memory Design group in 1961 and is currently responsible for the design and development of the Spectra 70/45 and 70/55 memory systems.

Odd addresses are stored in one stack and even addresses are stored in the other. The elementary operations are stored so that the two stacks are operated on alternate cycles. The odd-even cycles are overlapped so as to allow an effective data rate of 480 ns; data is available at the processor 360 ns after a given command (Fig. 4).

The ROM banks are added to the system in two-stack groups; each bank contains its own address register, timing generator, drive circuits, and sense gates. The data register is shared by all banks (Fig. 5).

The concept used for obtaining fixed storage in the 70/45 solves many of the problems inherently associated with

TABLE I—Basic Characteristics of Spectra 70 Memories

Processor	Classification	One-Bank Storage Capacity, bytes	Cycle Time, μs	Access Time, μs	bytes in 1 cycle	Expansion Range, banks	Max. Storage Capacity, 10^3 bits
70/15	Main Memory	4,096	2.00	0.75	1	1, 2	74
70/25	Main Memory	16,384	1.50	0.75	4	1, 2, 4	590
70/45	Main Memory	69,632	1.44	0.60	2	¼, ½, 1, 2, 4	2,396
70/45	Scratch-Pad Memory	512	0.48	0.12	4	1	4.34
70/45	Read Only Memory	2,048 words	0.48	0.36	53 bits	1, 2, 3, 4	868
70/55	Main Memory	135,168	0.84	0.44*	4	½, 1, 2, 4	4,359
70/55	Scratch Pad Memory	512	0.30	0.12	4	1	4.34

* Includes processor selection.

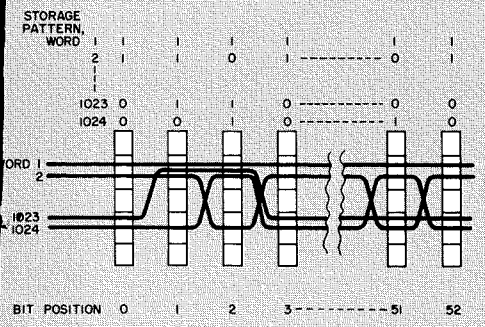

Fig. 2—ROM (read-only memory) stack wiring.

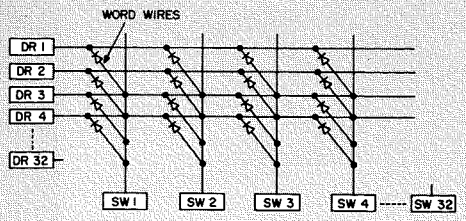

Fig. 3—ROM; selection of one of the 1,024 access lines.

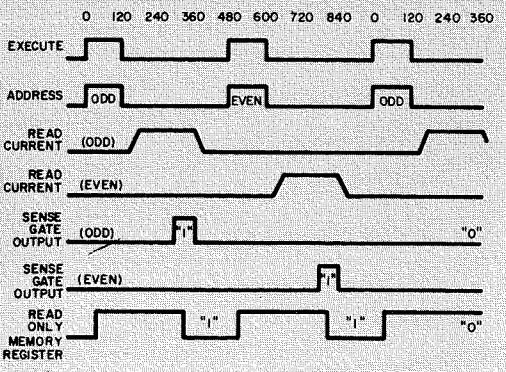

Fig. 4—ROM timing.

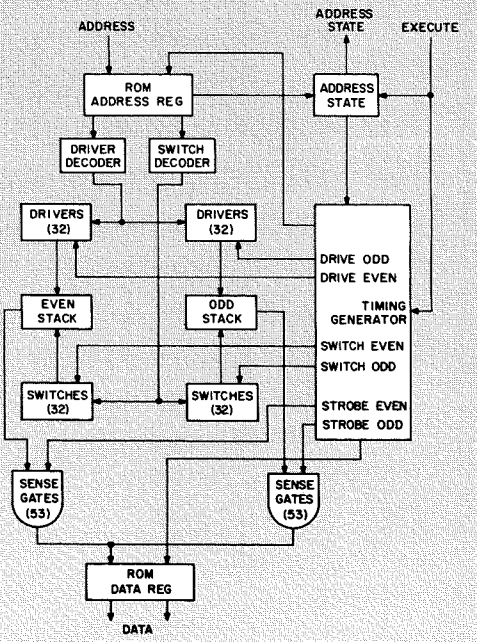

Fig. 5—ROM functions.

such a device. However, it should be noted that this is the *first* venture into read-only memories on a large scale. Certainly, as needs for this type of device grow, better solutions will become necessary. Essentially, it is a new field in computer design, and one that will grow in importance in future systems.

70/45 AND 70/55 SCRATCH-PAD MEMORIES

Requirements for Spectra 70/45 and 70/55 fast (scratch-pad) memories indicated that the same design could serve the needs of both computers. The scratch-pad memory allows the computer to perform very fast register operations economically and with a high degree of simultaneity; the machine status is stored during interrupt procedures and data transfers are buffered at extremely high rates.

The Spectra 70 scratch pad uses cores of 30-mil outside diameter and 10-mil inside diameter in a partially switched mode; the stack is a 128-word linear-select, two-core-per-bit array. Each word contains four 8-bit bytes plus two parity bits, or a total of 34 bits. The memory has a 300-ns cycle time with a 120-ns access time.

Two-Core-Per-Bit Operation

Two-core-per-bit operation is achieved by energizing one of a pair of digit drivers and then comparing the flux state of one core against another during a subsequent read-out. For example, in Fig. 6 assume both core *A* and core *B* at state *R*. To store information, one *digit* pulse will be present in coincidence with and additive to the *write* pulse. When digit *B* is applied, core *B* will partially switch to state *B*, and core *A* (seeing only the *write* pulse) and will partially switch to state *A*, as shown. Since these are stable remanent points for the cores, their flux content will remain unchanged until a *read* pulse of energy greater than that of the combined *write* and *digit* pulses is applied. The voltage induced in the sense winding as the cores return to state *R* will be greater as a result of the switching action of core *B* than that of core *A*. Therefore, the comparative output of *B-A* will be positive. If a positive output is defined as a logical *1*, then energizing digit driver *B* will store a *1*. Energizing digit driver *A* in coincidence with the *write* pulse will cause core *A* to be in state *B*, and core *B* to be in state *A*. A *read* pulse will cause the output of *B-A* to be negative and will therefore constitute a *0*.

Scratch-Pad-Memory Drive System

The organization of the drive system is based upon linear selection of a particular word, using very-high-speed, high-conductance diodes as the word-line switch. Separate wires are used for *read* and *write* so as to allow one transistor switch to serve both functions (Fig. 7). This minimizes the drive circuitry and permits drive pulses of only one polarity to be used, thereby simplifying the design. One of sixteen transistor switches is selected by the address decoder and turned on along with one of eight *read-write* driver pairs. The selected *read* and *write* drivers are pulsed upon receipt of commands from the timing generator, thereby steering current from the source through the appropriate drive line and ultimately to the selected switch. Following the application of a *read* and *write* drive current, the switch is turned off and the discharge circuit rapidly brings the busses back to their initial voltage. The drive system must be capable of supplying a *write* pulse of 200 mA with a 25-ns rise time and 100-ns base-width, and a *read* current of 400 mA with a 30-ns rise time and 140-ns base-width into a load of 68 cores and the associated parameters of the drive matrix. The switch must be ready to accept the *read* current pulse within 35 ns of the *execute* command and must discharge the bus back to its quiescent value within 30 ns following switch turn-off.

Sense Amplifier

The sense amplifier amplifies the core outputs, discriminating between a *1* and a *0*, and converting the signal into digital form acceptable to the processor. Amplification is by a single-stage difference-amplifier and a single-stage, single-ended amplifier with amplitude-limiting features. The amplifier stages must reject common-mode noise of 500 mV while amplifying a difference signal of 30 mV. The amplifier must not be blocked by input signals up to 5 volts. Discrimination is accomplished by use of a tunnel-diode threshold circuit in conjunction with a time-sampling pulse. The tunnel-diode discriminator triggers the output stage which converts a *1* signal into a digital pulse. The entire circuit must recover from the *digit* transient within 90 ns.

Regeneration System

The bit wires serve a dual function by accommodating the sense signals and serving as the means of writing, or regenerating information (Fig. 8). There are two digit drivers required per bit position—one for storing a *1* and the second for storing a *0*. Selection is governed by the contents of the data register at the time that the *digit* signal is generated (Fig. 9). The digit driver supplies a 70-mA pulse with a 12-ns rise time into a load of 128 cores and the associated parameters of the digit-sense matrix. The system is packaged entirely on plug-in cards inserted directly into a standard platter configuration. The stack cards, containing the core matrix and selection diodes, and the circuit cards occupy about two-thirds of a platter.

GENERAL DESIGN OF MAIN MEMORIES

The Spectra 70/45 and the 70/55 main memories were designed to have a high degree of similarity. The intent was to use similar concepts in memory organization, circuitry, components and packaging; they differ insofar as the system requirements differ. Both memories are coincident-current systems utilizing one ferrite core per bit in a full switching mode, although the cores themselves are different. Both memories utilize the same basic drive-system concepts, although some of the components are different. Both memories use the same amplifying and regeneration circuitry, even though the gain of the systems vary. The packaging of the memories is similar, although the 70/55 requires a greater number of basic memory subsystems than does the 70/45.

Word Selection

Word selection is accomplished by the coincidence of two half-amplitude current pulses (*X* and *Y*) at one, and only one, core in each bit plane. The *X* or the *Y* current alone does not provide enough energy to overcome the flux threshold of the core; however, the total of the two currents suffices to switch the core from one remanent state to the other. A third current in the *Z* dimension (*inhibit* current) controls the contents to be stored in the selected core by cancelling one of the selection currents. Detection of data stored in the cores is accomplished by sensing the status of a fourth wire (*sense* wire). Voltages are induced on the sense wire by flux changes in the cores.

Reading and Writing

Reading is accomplished by the simultaneous generation of *X* and *Y* currents which coincide at one core in each bit plane (Fig. 11), causing a flux reversal in only those selected cores that were in a *1* state. The flux change, in turn, induces a voltage on the sense wire and presents a signal to the sense amplifier. At the end of a *read* cycle, all selected cores are in a *0* state. Writing is accomplished by the generation of opposite-polarity current pulses along the selected *X* and *Y* lines. When it is required to store a *0*, the *Z* current is generated in that bit plane to oppose either the *X* or

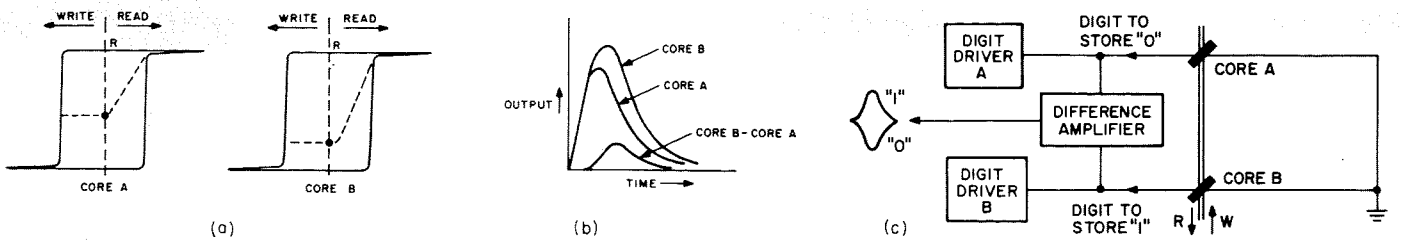

Fig. 6—Scratch-pad-memory two-core-per-bit operation.

(a) FLUX STATES OF TWO CORES
(b) OUTPUTS OF TWO CORES
(c) BASIC READ/WRITE OPERATIONS

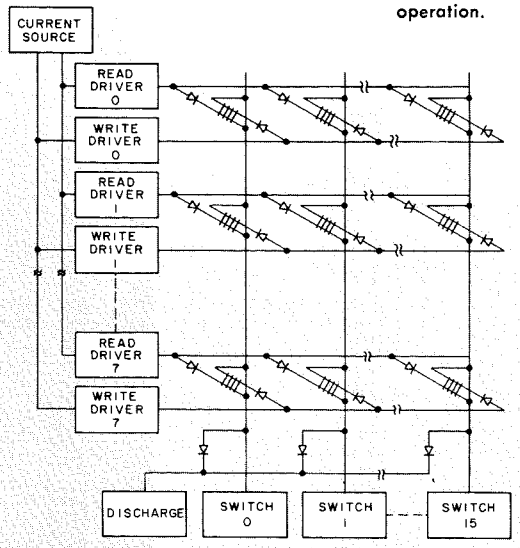

Fig. 7—Scratch-pad-memory drive system.

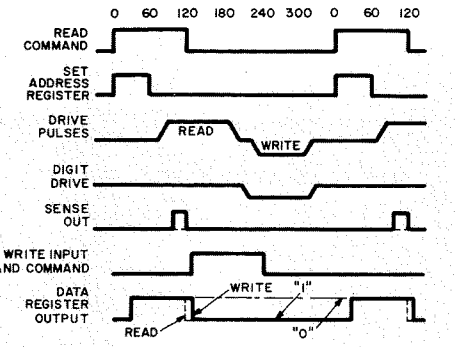

Fig. 9—Scratch-pad-memory timing diagrams.

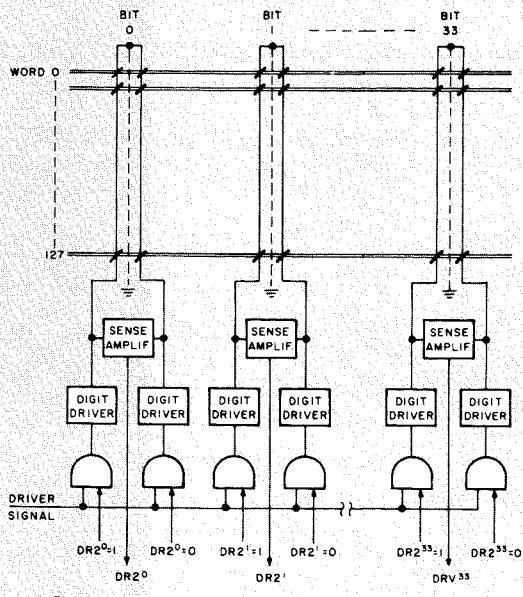

Fig. 8—Scratch-pad-memory regeneration system.

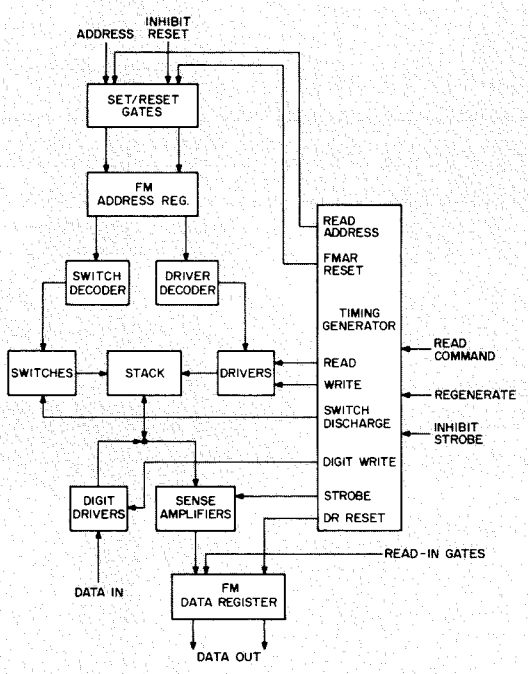

Fig. 10—Scratch-pad-memory functions.

the *Y* current and thereby inhibit a flux change. To store a *1*, no inhibit current is generated, allowing the core to change state. Therefore, a memory cycle consists of a *read* portion (in which sensing of data is accomplished) and a *write* portion (in which that data or new data is stored).

THE 70/45 MAIN MEMORY

The 70/45 main-memory basic bank is made up of two memory stacks. Each stack contains 18 bit planes (2 bytes each with parity) of 16,384 (128 × 128) cores, or a total of 32,768 bytes. In addition, the two stacks of the first bank each contain an additional 2,048 (128 × 8 × 2) bytes that are non-program-addressable and are used internally by the processor. Therefore, the first bank of memory contains a total of 69,632 bytes, while subsequent banks contains 65,536 bytes. The system accommodates memory capacities ranging from a quarter-bank system using a partial stack (17,408 bytes), and a half-bank system using only one stack (34,816 bytes), to a four-bank system using eight stacks (266.240 bytes).

Platter Arrangement

A memory bank is made up of four platters of three basic types. The first platter type mounts one memory stack and all the selection and drive circuitry associated with that stack. The second platter type contains the sense circuitry, address and data registers, data bus, and timing generator associated with that bank. The

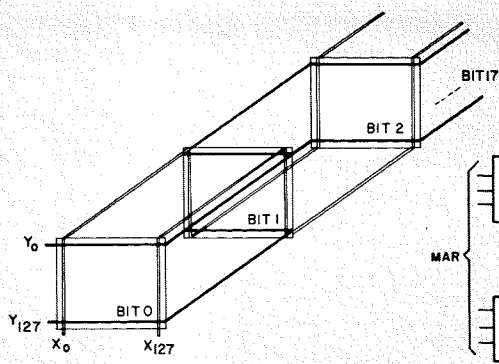

Fig. 11—Main memory: interconnection of driver lines.

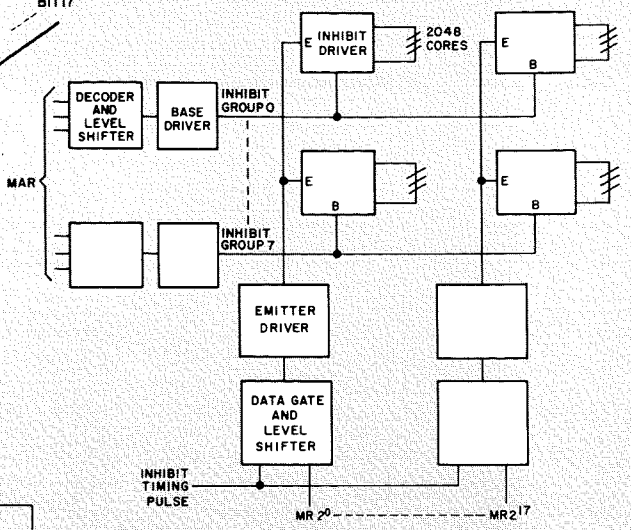

Fig. 14—70/45 main-memory inhibit system.

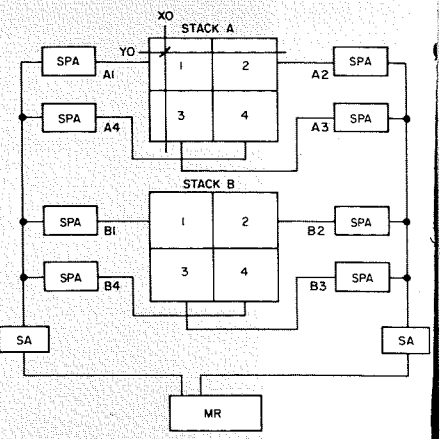

Fig. 15—70/45 sense-line–sense-preamplifier interconnections.

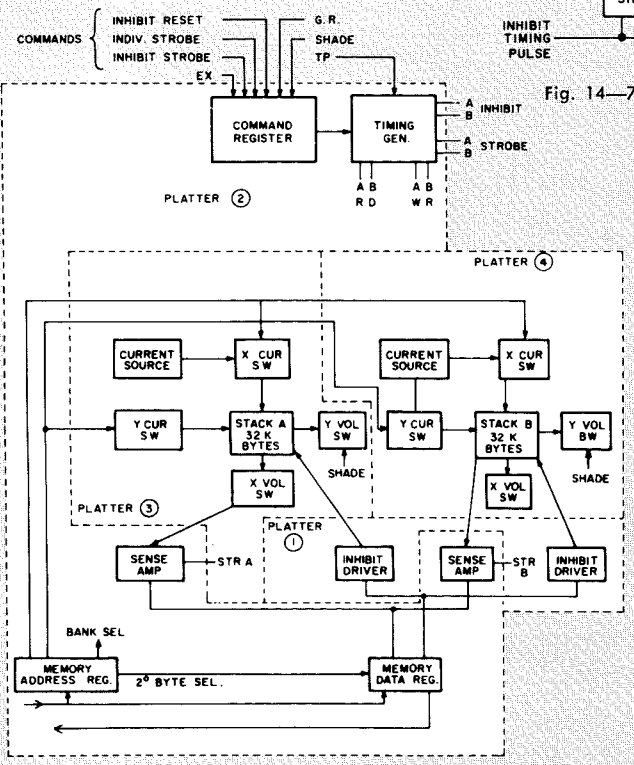

Fig. 12—70/45 platter division.

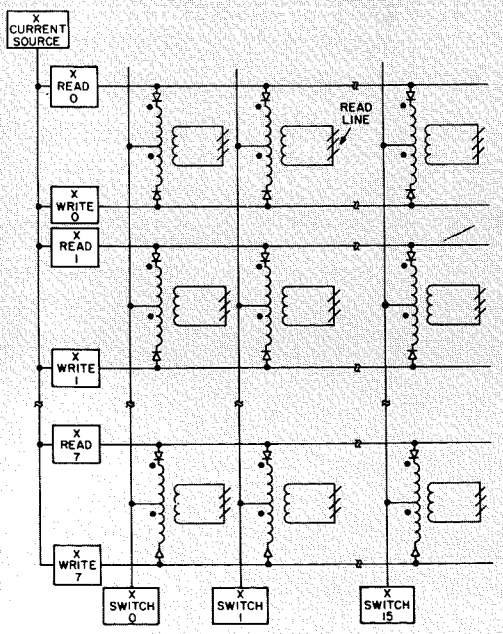

Fig. 13—70/45 main-memory drive system.

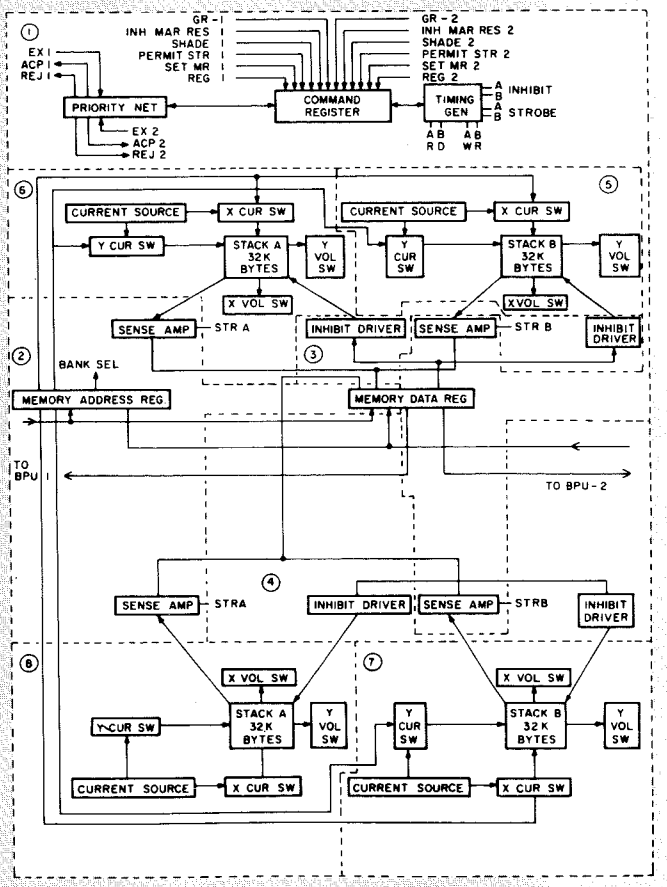

Fig. 16—70/55 platter divisions.

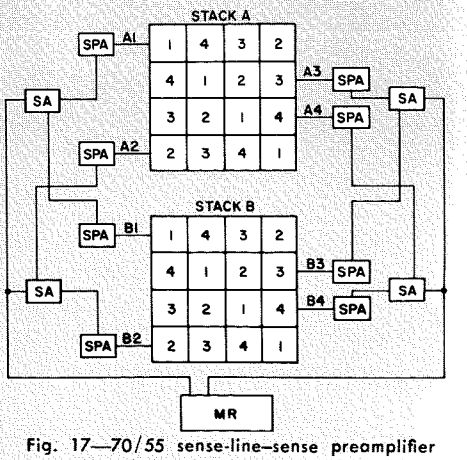

Fig. 17—70/55 sense-line–sense preamplifier interconnections.

third type of platter contains the inhibit drivers and pertinent regeneration circuitry associated with that bank. Therefore, one bank utilizes two stack platters, one sensing platter, and one regeneration platter. A half-bank system utilizes only one stack platter with a sensing platter and a regeneration platter. Expansion beyond one bank is accomplished by additional groups of four platters for each bank (Fig. 12). Selection of an *X* (or *Y*) word line is accomplished by the use of a transformer-diode matrix coupled to a driver-switch arrangement (Fig. 13). The drive system supplies a 350-mA *read-write* pulse with a 100-ns rise-time and a base-width of 500 ns into a maximum load of 2,448 cores and the associated stack parameters. The inhibit line on each bit-plane is divided into eight portions (2,048 cores per section). Inhibit-driver selection is determined by the state of those bits of the address register controlling the eight segments of the bank. The decoded selection pulse is gated with the memory register so that only those inhibit drivers of the selected group associated with the storage of a *0* will conduct current (Fig. 14).

Sensing Amplifiers

Each bit-plane of a stack contains four separate sense windings; a sensing preamplifier stage terminates each of these windings. The sense preamplifier is a highly stable difference amplifier with minimum distortion, affording a high degree of common-mode rejection while permitting some voltage gain of the difference signal. Four preamplifiers operate in parallel to drive one sense amplifier. The sense amplifier further amplifies the difference signal, while providing a greater degree of common-mode rejection. The output of the amplifier drives a hybrid tunnel-diode transistor discriminator that switches when its input signal at strobe time exceeds that of a minimum *1*. Activation of the discriminator sets the memory register. At times other than strobe time, the tunnel diode is heavily biased off by the strobe driver so that no output can occur.

Referring to Fig. 15, the sense preamplifiers (SPA) associated with a particular sense amplifier (SA) are chosen so that the half-select *delta noise* (δ_n) attributable to a sense winding occurs only at one of the four parallel inputs. This provides for a maximum signal-to-noise ratio under adverse data and tolerance conditions. For example, in Fig. 15, if *XO-YO* is driven, delta noise will occur in *A1* ($2\delta_n$), *A2* (δ_n), and *A3* (δ_n). Therefore, in the Fig. 15 example, the left-hand SA sees the core output and $2\delta_n$, while the right-hand SA sees $2\delta_n$.

The sense and inhibit windings in a bit-plane are strung so that they share only 512 cores; this provides for minimum recovery time of the sensing system.

70/55 MAIN MEMORY

The 70/55 main memory is constructed from a basic bank of core storage made up of four memory stacks. Two stacks contain 16-bit planes of 16,384 (128 × 128) cores and two stacks contain 17-bit planes of the same size. One 16-bit stack and one 17-bit stack are used together to form 16,384 memory words (one word equals 4 bytes plus one parity bit) or a total of 65,536 bytes. As in the 70/45, the first bank of memory contains an additional 4,096 non-program-addressable bytes. These are incorporated into the first pair of stacks. Therefore, the first bank of 70/55 memory contains a total of 135,168 bytes while subsequent banks contain 131,072 bytes. The system is designed to accommodate memory capacities ranging from a half bank of two stacks (69,632 bytes) to four banks of 16 stacks (528,384 bytes).

The 70/55 memory can be shared by two processors. Through the use of internal priority logic, the memory receives commands from the two processors and then selects the proper one to service first. It then notifies the processors of its decision, allowing the unserviced processor the prerogative of either waiting for service or performing some other function.

Memory Bank Arrangement

A 70/55 memory bank is made up of eight platters of the same basic types used in the 70/45. There are four stack-platters which are identical to the 70/45. There are two sense platters, containing circuitry similar to the 70/45, with the added priority logic, and there are two regeneration platters. In the half-bank system, one regeneration and two stack platters are removed, leaving a total of five platters (Fig. 16).

Drive System

The drive system is similar to that of the 70/45. The major difference arises because the 70/55 system must deliver a *read-write* pulse of 450 mA with a 50-ns rise time. The voltage induced on the drive line by this current pulse exceeds most transistor limitations; so, a 2:1 transformer ratio is used. Therefore the driver must supply 900 mA (neglecting losses) at 50 ns to the transformer matrix.

Inhibit Systems

The inhibit system is again quite similar to the 70/45 with differences occurring because of the increased power and speed requirements. The effects of these differences are only in component values.

Each 70/55 bit plane contains eight separate inhibit and four separate sense windings. However, because of the faster rise times, the orientation of the sense windings are quite different. The sense line contains 4,096 cores arranged in mats of 1,024 cores. The mats are interconnected so as to allow reduction of delta noise beyond that of the 70/45. The interconnectors are shown in Fig. 17. This type of sense winding configuration allows the sense and inhibit windings in a bit plane to share only 256 cores, providing for a speed-up in recovery of the sense system beyond that of the 70/45.

70/45 AND 70/55 PERFORMANCES

The major differences in performance between the 70/45 and the 70/55 main memories are attributable to the core itself. The 70/45 core has a 30-mil outside diameter, 18-mil inside diameter, and 7.5-mil thickness. The core has a typical switching time of 370 ns. The 70/55 core has a 20-mil outside diameter, 12-mil inside diameter, and is 4.5-mil thickness. This core has a typical switching time of 180 ns. It can therefore be seen that further advances in coincident-current core memory speeds are highly dependent upon the advent of even smaller cores with faster switching times.

It has long been realized that cores cannot continue to become smaller and smaller with no limit. At every decrease in the core aperture, stringing of planes becomes increasingly difficult. It is for this reason that batch-fabricated arrays of individual storage cells have received so much attention.[2,3]

The list of proposed solutions to the batch fabrication problem is long. Starting with ferrite apertured plates to present-day proposals of thin films, laminated ferrites, plated wires, and many more, attempts have been made to consistently fabricate high-quality multibit devices that would replace cores. The need for such a device will continue to grow more acute as further advances are made outside the storage area.

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PACKAGING DESIGN OF SPECTRA 70/45 AND 70/55

Development of highly advanced packaging techniques involving integrated circuits and printed backplane wiring was essential for the more-powerful members of the Spectra 70 family—the Spectra 70/45 and 70/55. The success of these developments has brought into the RCA computer product line many new and advanced concepts for high-performance-computer circuit implementation that feature economy in manufacture and high operating reliability. Described herein are basic design considerations such as crosstalk, multilayer boards, integrated circuit packages, and connectors and contacts. An important design accomplishment—the printed backplane, or platter—is described, in which it was necessary to make major advancements in every phase of printed board design and fabrication. This backplane provides over 90% of the wiring in printed form, as well as the controlled impedance and shielding required. The resulting basic Spectra 70/45 and 70/55 package includes the logic, memory, printed backplane, interconnections, maintenance panel, power supply, and console.

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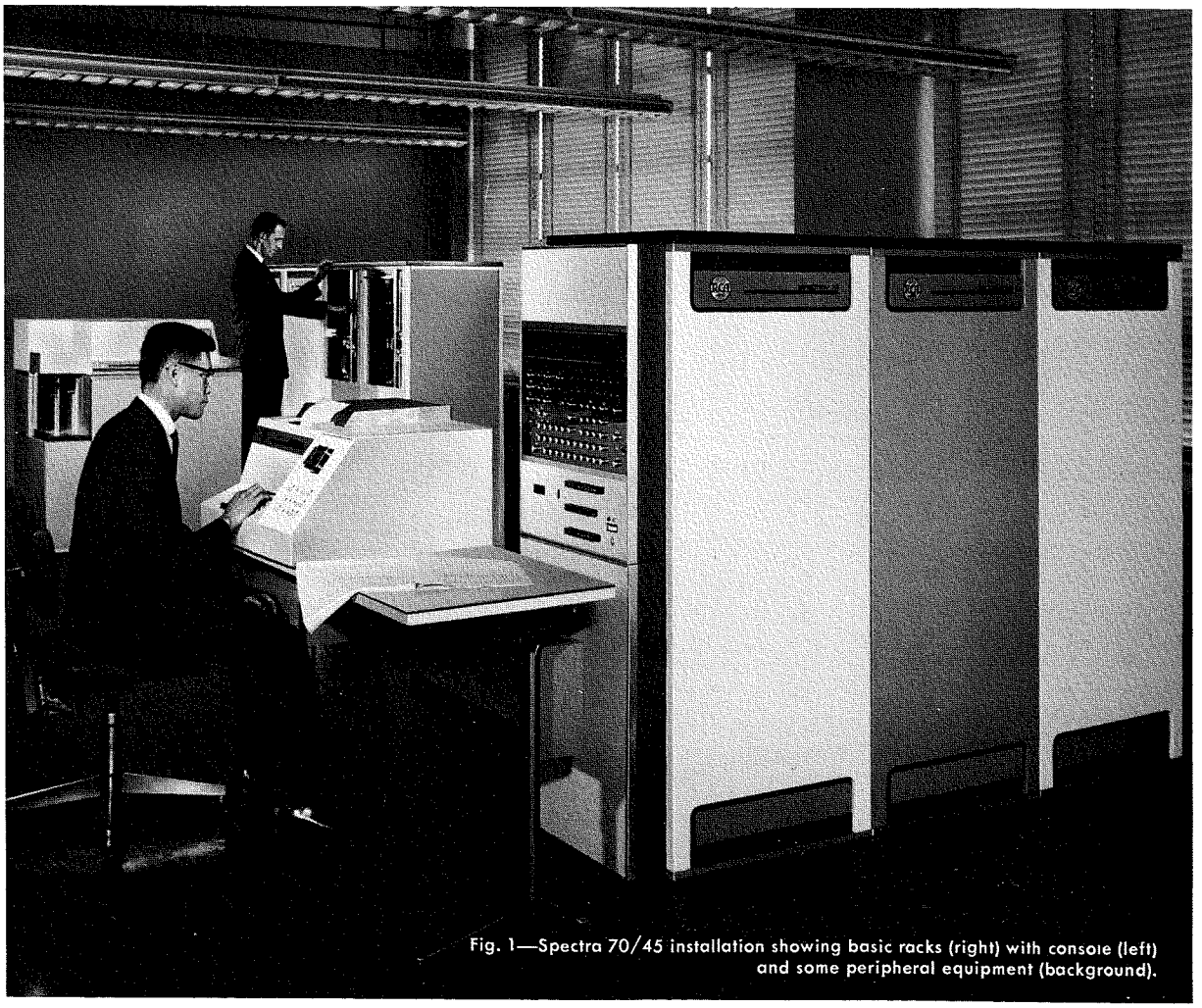


Fig. 1—Spectra 70/45 installation showing basic racks (right) with console (left) and some peripheral equipment (background).

THE Spectra 70 family consists of four basic systems: the 70/15, 70/25, 70/45 and 70/55; each system provides a range of performance and speed capabilities; the 70/45 and 70/55 computer systems are the large systems which provide higher speed and performance. All equipments in the Spectra 70 family have the same external appearance. The similar styling, integrated color schemes, and standardization of rack sizes have combined to produce a very distinctive and functional appearance.

The 70/45 and 70/55 systems are similar in packaging concept, differing only in relative size. Mechanically, the assembly used to house these systems is a standard EDP cabinet rack 22 inches deep, 48 inches wide, and 62 inches high (Fig. 1). Expansion is accomplished by the addition of a half rack of 22 x 24 x 62 inches or matching full-size racks.

The Spectra 70/45 and 70/55 employ advanced packaging techniques using integrated circuits and printed backplanes (Figs. 2-4). The internal structure of the standard rack accommodates 18 printed backplanes or platter assemblies. Six platters are mounted in a central fixed frame assembly, and three are mounted on each of four swinging frames. The platters are multilayer boards which provide the printed backplane wiring, the electrical shielding, and the controlled impedance characteristics required to meet the system requirements. Interconnection between the platters is accomplished by means of cable assemblies. Each of the platters has the capability of accepting 104 logic plug-in units and 26 cable assemblies. The platters used in the various memory applications will have the memory stacks and assemblies mounted directly on the platter. The plug-in cards are approximately 3 x 4 inches. These are mounted on ½-inch centers in four vertical rows consisting of 30 plug-ins per row. A horizontal row of five connectors is provided at top and bottom of each platter. Each platter contains 600 to 1,200 gates. (The design and production of the platter assembly is discussed in detail in another paper.[1])

EARLY DESIGN CONSIDERATIONS

Early in the Spectra 70 packaging design, various techniques and approaches were chosen. At the start of the design phase of the Spectra 70/45 and 70/55 systems, a study program was initiated to evaluate information developed on other high-speed computer system projects,[2,3] as well as results of the RCA 3301 design program. From these studies it was apparent that the previous computer families could not meet the new requirements of higher speeds and greater complexity if conventional types of packaging were employed. Conventional packaging includes the approach of using plug-ins, rack wiring, and cabling. Problems associated with this type of packaging can be grouped into two major areas: *1)* the costs associated with the manufacture, test, and maintenance work caused by the tremendous wire build-up and *2)* the electrical problems of crosstalk and the long signal paths.[4] The RCA 3301 design required some changes and rewiring because of these effects.

NEW SYSTEM DESIGN CONSIDERATIONS

The system operating speed requirements for the new Spectra 70 family of high-speed computers is approximately twice that of the 3301 system; circuits must function at pair delays of 20 to 25 ns. At these speeds and with the short rise times of approximately 5 ns, *the time required to propagate the signal from one point to another becomes a significant part of the delays of the system.* Thus, the need for higher density packaging is evident. With the higher density comes the problems of increased crosstalk and the previously discussed costs associated with high-density wiring.

Crosstalk Requirements and Multilayer Boards

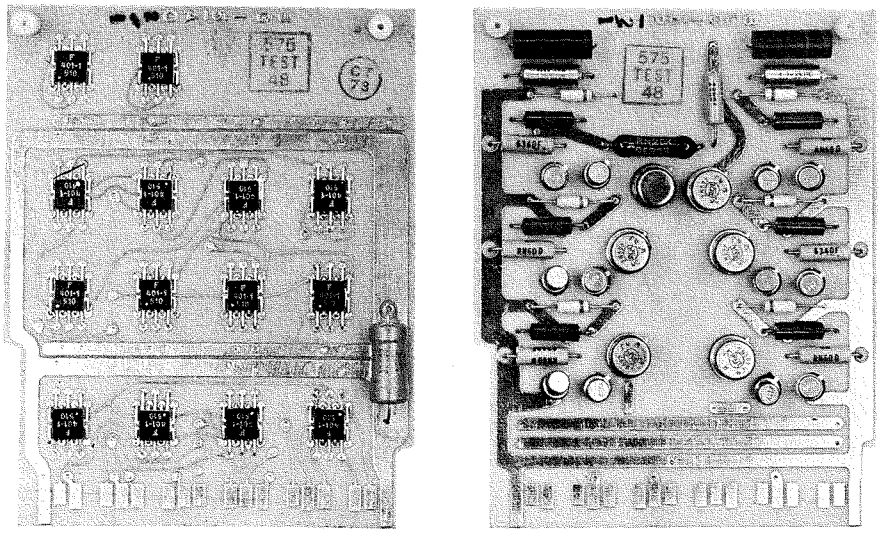
To reduce the crosstalk to an acceptable minimum value, all wiring must be very closely associated with a ground plane, present a uniform and stable impedance, be capable of high-density packaging, be repairable, and be reasonably economical. To meet these requirements, the multilayer board[1] was selected as the backplane. The characteristic impedance needed to meet the circuit requirements was specified as 100 ohms ± 10%. With this as a requirement, several studies were initiated in parallel; these included a vendor survey to obtain printed-board sources, a study to obtain the best layout of the printed board which would achieve high density of wiring and logic, a study to develop a low-cost connector, and a study to develop an integrated packaging approach which would combine plug-in, printed multilayer board, and the interplatter wiring.

The feasibility studies indicated that the objectives of the product-design specification could be met. They also showed that a number of new methods, techniques, and procedures would have to be developed and that the package design must be an integrated design which took into account the basic requirements of the circuit, logic, and memory design. In addition to satisfying these items, the packaging had to meet requirements of high reliability, manufacturability, field serviceablity, and low cost. To insure meeting these requirements, each new concept and technique had to be developed to the point where it could be incorporated into the design only if conventional assembly techniques could be employed. The time cycle from design to production was very short.

Integrated Circuit Packages

One of the basic building blocks of the system is the plug-in circuit board and its components. The 70/45 and 70/55 systems employ integrated circuits for the basic logic functions[5] and in all other possible functions for which integrated circuits that meet the performance and design objectives can be obtained. The plug-in is designed to accept 16 ICP (integrated circuit package) units; each ICP contains two gates. The 1/16-inch-thick plug-in card measures approximately 3 x 4 inches (Fig. 2).

Fig. 2—An ICP board and a discrete component board.



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The same size board is used for discrete components.

Two types of boards are used; one is double-sided with plated-through holes for crossovers, and the other is the multilayer board which has a ground plane as an internal layer. The design of these boards required a considerable upgrading in fabrication standards because line-widths were reduced and spacing tolerances were tighter. Close liaison was required to keep the costs of these boards in line with conventional boards. The high density and the associated wiring limitations were major factors. The ICP handling was another major problem; requirements were that integrated circuit boards had to be inserted as conventional components and wave-soldered on the board. The conventional 14-lead flat package was chosen as the best of the available packages. The lead configurations and the ribbon type of lead do not make this package easy to insert into the printed board.

A three-part design project was started: *1)* the development of a method to handle the ICP units as conventional components, *2)* obtaining a package which had pins on one side, and *3)* development of an interim carrier to be used until the final packaging configuration could be developed. This last approach would be of primary use for replacement operations during the prototype and initial production stages.

The first part of this program was completed successfully and a semi-automatic insertion tool was developed (Fig. 3) which cuts the leads, shapes them, and inserts four ICP's at one time into the plug-in board. The design of this unit is such that during these operations, *no stresses* are placed on the junction of the lead and the end seal. Tests on this operation and the solderability of units with dip or wave soldering have indicated no problems. Extensive tests are continuing on larger quantities of the units.

Progress on the second phase (ICP with pins) necessarily depends on the ability of ICP designers to solve the major problems in changing their package configuration. At this writing, work is in progress and this alternate package should be available reasonably soon.

The third phase, work on an interim package, is proceeding satisfactorily toward a package that will meet the requirements.

Connectors and Contacts

Entrance to and exit from the plug-in are provided by printed fingers on the plug-in board. These are gold plated with a nickel undercoat to insure reliable contact. There are 32 logic pins available with three ground and two voltage

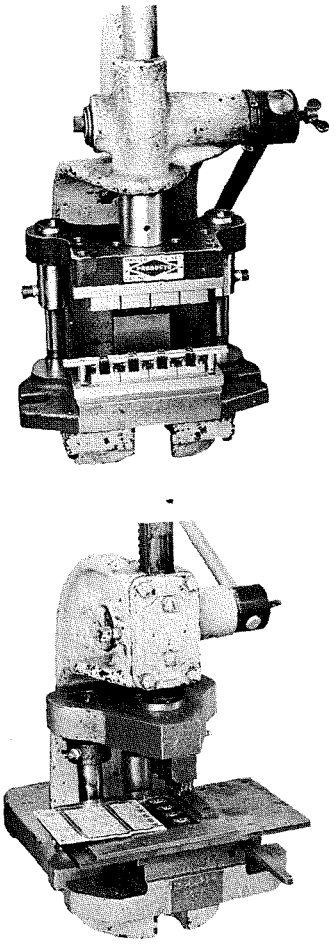

Fig. 3—Insertion machinery for ICP packages.

contacts. Additional contact spaces are provided for the memory and cable boards for voltages and grounding.

Extensive testing has proven the reliability of this plated-finger approach when mated with a low-cost, highly reliable miniature connector developed for this project. The connector contains a maximum of 48 contacts located on a grid employing 0.125-inch centers. The arrangement of the contacts within this grid permits access to the pins by means of the printed wiring on the platter. This function permits the maximum utilization of printed wiring. Polarization is provided as well as limited guiding by means of plastic ears molded as an integral part of the connector body. The contacts are of phosphor bronze material and are of 0.020 x 0.030 inch in cross section. The high-reliability mating between contact spring and the plug-in board is effected by a gold ball welded to the contact. The gold ball provides a low-cost contact, since the quantity of gold plating is greatly reduced while maintaining the gold-to-gold interface between the mating faces. The specified contact forces of 2 to 4 ounces as well as the life test requirements for 500 insertions and withdrawals have been met. Results of the tests have proven the validity of the design and the proper functioning of the gold ball and printed board interface. Reliable contact has been maintained after the life test. The back end of the contact provides proper lead-in for access into the platter and provides for three wirewrap connections using the modified wrap and #26 wire. This, of course, provides for considerably more discrete wiring than is needed for the final systems, but that is essential for flexibility in the prototype phase.

The connectors are assembled in the platter and electrical connection achieved by soldering. Two soldering approaches have been used successfully: the use of solder preforms, and wave soldering. The wave soldering method will very probably be employed for all production units.

PRINTED BACKPLANE OR PLATTER DESIGN

The printed backplane or the platter design is the heart of this package (Fig. 4); it also is a major design accomplishment. The initial design goals set up for the backplane wiring was that a minimum of 90% of the wiring be printed and that the backplane provide electrical shielding and present a controlled impedance. All of this was to be accomplished as economically as possible. To meet the electrical and system requirements, a multilayer board approach was selected and a tentative specification drawn up. This provided the data needed to define the geometry of the board.[6] The conventional microstrip approach was used, and the board parameters which finally evolved were that all signal lines were to be on the top and bottom surface, orthagonal wiring was to be followed, printed lines must have an impedance of 100 ohms ± 10%, and ground and voltage planes were to be used. The physical requirements of the printed lines are 10 ± 2 mils, signal-to-signal spacing of 25 mils, and signal-to-pad spacing of 6 mils minimum. This pattern established the 0.125-inch grid as the basic layout. Pad size for the 40-mil holes for the connector contact were specified as 60 mils.

A typical multilayer board used in the Spectra 70 backplane is approximately 0.1 inch thick by 17 inches long, and 17 inches wide, and contains five printed layers. The three internal layers provide the ground plane and the voltages. The two external layers contain the signal wiring and the inter-layer connections. No signal wires are hidden, and are, therefore, accessible for changes and any needed repair. The two external layers provide approximately 7,500 inches of printed wiring for the signal

routing. Plated-through holes are employed to make the connections between signal layers, connections to the voltage layers, and the connections to the logic and cable connectors. Approximately 8,500 of the available 15,000 holes are used on a platter. Power is brought into the platter by means of a series of plated-through holes along the periphery of the platter. Mounting holes are also provided.

With these requirements, conventional or even premium printed-board manufacturing and design techniques could not be employed. *It became necessary to make major advancements in each and every phase associated with previous EDP printed-board design and fabrication.* The artwork, drilling, etching, and the multilayer techniques had to be improved. Various processes employing both 1- and 2-ounce copper, along with gold and tin lead plating resist, have been used. The gold process has been quite successful. Because of costs and soldering problems, an alternate approach (tin-lead) has been investigated and appears to be quite satisfactory. Final evaluation of this type of board is now in process, with every indication being that this is the best approach for production boards.

Several programs were established to provide this needed capability within RCA. The magnitude of the effort can be best demonstrated by referring to another paper[1] which describes the Multilayer Board Facility and the requirements for the associated artwork. Within EDP, a major program was started to develop a design-automation capability which would computerize the information and prepare it in the best possible format for automated processing.[7] This is a long-term project and to date has been quite successful. The full capability will not be available for some time, but the interim programs and design checks have contributed very significantly to the design effort.

A series of test and evaluation phases were required to measure and prove out the capabilities for production of these boards. In addition to the requirements of the line width and spacing, the multilayer board was further complicated because of the size needed to keep the interconnections at a minimum. Several studies, resulting in functional boards, were made. These studies demonstrated that a board size of approximately 17 x 17 inches was feasible if the manufacturing capabilities and artwork preparation were improved. This size of board met the requirements for high-density packaging with a maximum of printed wiring and a minimum of interconnection. The final configuration of the platter was limited to this size; and based on our layouts to date, the platter will provide more than 90% of the wiring in printed form.

INTERCONNECTIONS OF PLATTERS

Interconnections between platters are accomplished by cables and cable harnesses. The electrical and logic requirements have not permitted the optimum layouts required for the incorporation of flat cables within the present engineering design schedules; however, work continues toward the use of this approach. Access to the platters is provided by a series of connectors mounted on the platters, with the cable connectors located to enhance the printing wiring capabilities. Production of these cables and the associated harnesses is accomplished as an operation external to the main assembly. The racks and platters can be assembled, and the cables then routed and placed into the proper locations. In effect, there is no wiring required at the rack level of assembly. This permits parallel assembly operations and will reduce the overall production assembly cycles.

CONCLUSION

The packaging design of the Spectra 70/45 and 70/55 systems has incorporated many advanced concepts which were mandatory to meet the performance specifications. The basic approach has been to provide a packaging scheme which combined the circuit, logic, and memory components into a very dense package. The package provides the required electrical shielding needed to meet the noise and crosstalk limitations. Laboratory and simulation tests and evaluations to date indicate that these new concepts accomplish the goals. The prototype units are now in various stages of testing, and final evaluation is in process.

J. J. O'DONNELL received his BSEE from Villanova University in 1949. From 1949 to 1955 he worked as Project Engineer for the Naval Air Development Center in Johnsville, Pa., and for the Sperry Gyroscope Company. In 1955 he joined RCA in the Components Evaluation Laboratory of Standards Engineering. In 1960 he moved to EDP where he has had various engineering responsibilities for the 301, 601, 3301, and Spectra 70 Computers. He is presently Manager of the Packaging, Power Supply, and Standards Activity.

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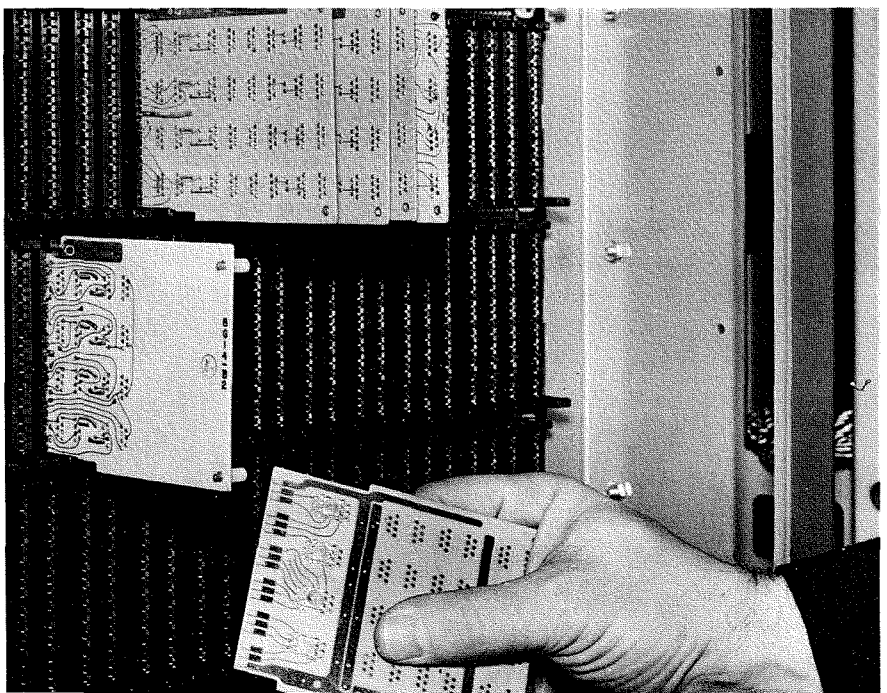
Fig. 4—Platter with connectors and plug-in card.



CURRENT-MODE-LOGIC INTEGRATED CIRCUIT FOR THE SPECTRA 70/45 AND 70/55

In the design and fabrication of a high-speed integrated-circuit digital-logic gate for the Spectra 70/45 and 70/55 computers, first a circuit configuration was chosen that efficiently minimized the deleterious effects of parasitic components on the performance of monolithic-silicon integrated circuits. Second, the configuration was designed to meet the requirements imposed by the circuit's operating environment. The current-mode-logic (CML)—also called emitter-coupled-logic—gate configuration was selected as most adaptable to high speed monolithic-silicon integrated-circuit technology. In addition to the circuit design, this paper presents some of the AC and DC circuit considerations and some effects on performance of the thermal characteristics of the integrated circuit packages.

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THE integrated-circuit logic gate (Figs. 1, 2, 3) for the RCA Spectra 70/45 and 70/55 computers was designed to have a pair delay of 17 ns with a 100-pF load, and to have the ability to drive terminated transmission lines. To achieve this speed, a nonsaturating current-steered mode of operation was adopted, for two basic reasons: First, because the transistors used in the gate are operated in the linear region, no time is wasted in discharging stored base charge, thereby significantly decreasing the response time of the devices. Second, the emitter-coupled configuration minimizes the effect of parasitic capacitances associated with integrated circuits which would slow down switching speeds.

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Fig. 2 shows the basic *current-mode-logic* (CML) gate configuration. (This configuration is also called *emitter-coupled-logic*, ECL, and sometimes *emitter-coupled-current-steered-logic*, ECCSL.) For a high input defined as a *1*, the gate performs an *or-nor* logic function. The *or* output is taken from *Q4* and the *nor* output from *Q3*. The emitter-follower stages driven by the current switch give the gate a low output-impedance. This low output-impedance facilitates a large fan-out capability, provides the proper level shift to guarantee nonsaturating operation, and isolates the collectors of the switch from stray capacitances. The nominal swing of a gate of this type is from −0.74 to −1.62 volts. Fig. 2 shows that any parasitic capacitance associated with R_{o1} or R_{o2} is quickly charged and discharged via the low impedances looking into the emitters of *Q3* and *Q4*. Likewise, any parasitic capacitance present at the common emitter point of *Q1* and *Q2* is quickly charged or discharged. The capacitance at the collectors of *Q1* and *Q2* is chiefly the sum of the parasitic collector-substrate capacitance, the collector-base capacitances of the input transistors or *Q2*, and the capacitance seen looking into the bases of the emitter-follower drivers. These capacitances must be charged through R_{c1} or R_{c2}. These resistors however can be chosen to be low enough in value to minimize any slow-down effects on the collector response.

DC CONSIDERATIONS

In designing high-speed gates to drive terminated transmission lines, several important considerations become apparent. These are current gain (β), base-emitter voltage (V_{be}), and logic swing, as will now be described.

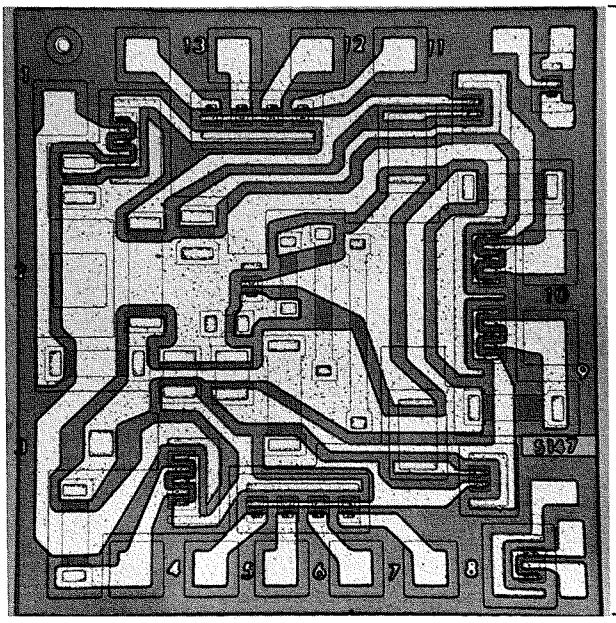

Fig. 1—Integrated-circuit chip of Spectra 70/45, 70/55 type CML gate.

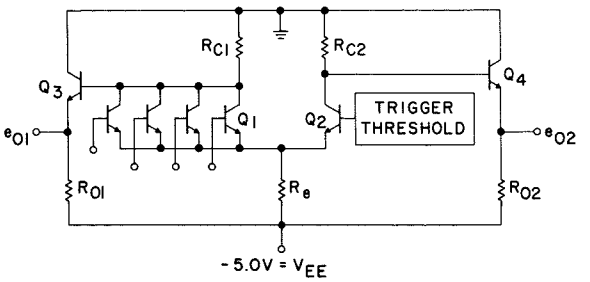

Fig. 2—Spectra 70/45, 70/55 CML logic gate configuration.

Current Gain (β)

With the gate configuration shown in Fig. 2 designed to dissipate approximately 40 mW, a large fan-out (approximately 25) can be accommodated without too severe a current-gain requirement on output emitter-follower transistors *Q3* and *Q4*. For example, the load current to fan-out of 25 at room temperature with a nominal value of $\beta = 50$ on all the gate transistors is less than 2 mA. However, with a 100-ohm terminating resistor (tied, say, to the lowest logic level voltage, −1.62 volts) approximately five times that current is required. This additional drive requirement reflects itself as a droop in the upper logic level because of the $I_b R_c$ drop in the base of the output emitter followers. Detailed data on beta behavior with current, temperature, and production variations must therefore be known.

Base-Emitter Voltage (V_{be})

Because the output logic levels are directly a function of V_{be}, the heavy load current requirement of the terminated output causes still more droop of the upper logic level. Therefore, very detailed information on V_{be} spreads versus current and temperature must also be known.

Eqs. 1, 2, 3, and 4 relate β and V_{be} to the high output logic level state for unloaded and loaded conditions:

$$e^H_{nor\text{-}unloaded} = \frac{-\beta_3 V_{be3} + V_{ee}\left(\frac{R_{c1}}{R_{o1}}\right)}{\beta_3 + \left(\frac{R_{c1}}{R_{o1}}\right)} \quad (1)$$

$$e^H_{nor\text{-}loaded} = \frac{-I_{load}R_{c1} - \beta_3 V_{be3} + V_{ee}\left(\frac{R_{c1}}{R_{o1}}\right)}{\beta_3 + \left(\frac{R_{c1}}{R_{o1}}\right)} \quad (2)$$

$$e^H_{or\text{-}unloaded} = \frac{-\beta_4 V_{be4} + V_{ee}\left(\frac{R_{c2}}{R_{o2}}\right)}{\beta_4 + \left(\frac{R_{c2}}{R_{o2}}\right)} \quad (3)$$

$$e^H_{or\text{-}loaded} = \frac{-I_{load}R_{o2} - \beta_4 V_{be4} - V_{ee}\left(\frac{R_{c2}}{R_{o2}}\right)}{\beta_4 + \left(\frac{R_{c2}}{R_{o2}}\right)} \quad (4)$$

The emitter follower resistors can be approximated the first time around by calculating the current required to discharge the output load capacitance in a specified time:

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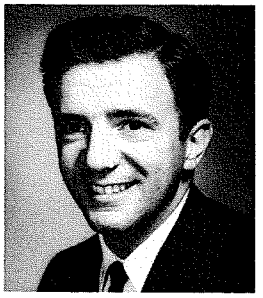
M. D'AGOSTINO received his BSEE from Villanova University in 1960 and his MSEE from Drexel Institute of Technology in 1963. At RCA, Mr. D'Agostino has worked on the Micropac memory, ferrite cores, and memory planes, and has designed the temperature control and sensing circuitry for memories. Mr. D'Agostino was also responsible for the design of the selection circuitry used on a thin-metal-sheet multiaperture-element memory. Recently, Mr. D'Agostino contributed to the evaluation of integrated component characteristics; he is now responsible for the circuit design, analysis, and evaluation of high-speed monolithic logic circuits. He has investigated future logic circuits which make most advantageous use of advanced integrated techniques. He has evaluated also the effects on circuit performance of the thermal characteristics of integrated circuit packages. Mr. D'Agostino is a Member of the IEEE and Eta Kappa Nu.



M. D'Agostino

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$$I_{emitter} = C_{load}\frac{dv}{dt} \quad (5)$$

Therefore, for a given allowable droop in the output level under full load over a specified temperature range, the collector resistors of the gate can be chosen precisely, using Eqs. 1, 2, 3, and 4 with the β and V_{be} data.

Logic Swing

The logic swing of this type of gate is:

$$e_{swing} = I_G R_C \quad (6)$$

where I_G is gate current exclusive of emitter follower current. As mentioned earlier, the normal logic swing of a gate of this configuration is 0.88 volt. For a logic swing greater than 0.88 volt, the gate transistor may be driven sufficiently into saturation at elevated temperatures so as to adversely affect the switching speed. Once the logic swing is chosen, the common emitter resistor can be found from: (7)

$$e^L_{nor} = \frac{-(V_{in} - V_{be1} - V_{ee})\,\alpha_1\beta_3\left(\frac{R_{c1}}{R_e}\right)V_{ee}\left(\frac{R_{c1}}{R_{o1}}\right) - \beta_3 V_{be2}}{\beta_3\left(\frac{R_{c1}}{R_{o1}}\right)}$$

where V_{in} is the nominal high state of the gate, e^L_{nor} is the nominal low state of the gate.

AC RESPONSE

Up to this point, we have considered, chiefly, the logic levels of the gate under DC loading conditions. To a large degree, these load conditions define the component values of our circuit. We have, however, mentioned the AC response of the circuit in the selection of the emitter-follower resistors. Now let us look, in more detail, at the AC response of the emitter-coupled logic gate.

Basically, the response of the gate can be divided into three parts: 1) input base response, 2) collector response, and 3) emitter-follower response.

Base Response

Since the input impedance of the gate is high, the rise time at the base of the input transistor is strongly a function of r_b and c_b, the input capacitance of the transistor. This input capacitance of the gate is a function of the base-collector and base-emitter capacitors which in turn are a function of the input voltage. This relationship is shown by:

$$C_{be}(V_{je}) = \frac{C_{oe}}{\left[1 + \left(\frac{V_{je}}{V_{ct}}\right)\right]^{r_e}} \quad (8)$$

$$C_{bc}(V_{jc}) = \frac{C_{oc}}{\left[1 + \left(\frac{V_{jc}}{V_{ct}}\right)\right]^{r_c}} \quad (9)$$

where: C_{oe}, C_{oc} = zero-bias capacitance of the junction, V_{je}, V_{jc} = junction potentials, V_{ct} = contact potential, and r_e, r_c = a function of the type of base-emitter and base-collector junctions, i.e., graded or abrupt.

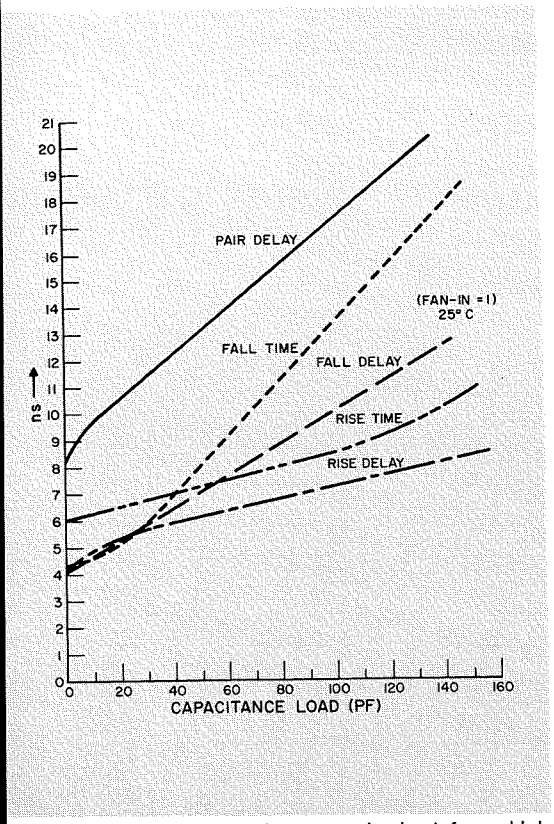

Fig. 3—Speed vs. capacity load for a high-speed CML gate.

The average input capacitance can be calculated on the basis of the rate of charge with respect to input voltages:

$$\overline{C_b} = \frac{\Delta Q_b}{\Delta V_b} = \frac{1}{\Delta V_b}\left[\int_0^{\Delta V_{be}} C_{be}(V_{je})\, d(V_{je}) + \int_0^{V_{bc}} C_{bc}(V_{jc})\, d(V_{jc})\right] \quad (10)$$

Inserting the relationships for the base, emitter, and collector voltages for both the *1* and *0* conditions, Eq. 10 reduces to:

$$\overline{C_b} = 1.46\, C_{oe} + 1.51\, C_{oo} \quad (11)$$

And, the base delay can be expressed as:

$$T_D{}^b = 0.7\, r_b\, (1.46\, C_{oe} + 1.51\, C_{oo}) \quad (12)$$

Collector Response

The collector capacitance C_L consists of three parts: *1)* the collector-base capacitance of the input gate transistors, C_{c1}, those with a *1* applied; C_{cm}, those with a *0* applied; *2)* the collector-substrate capacitance, C_{s1}; and *3)* the emitter-follower capacitance, C_f. This is expressed as:

$$C_L = f(\overline{C}_{c1} + \overline{C}_{cm} + \overline{C}_{s1} + \overline{C}_f) \quad (13)$$

Using a technique similar to that used to arrive at C_b yields: $C_{c1} = 1.62\ C_{oc}$; $C_{cm} = 0.75\ C_{oc}$; $C_f = 0.88\ C_{oc}$; and $C_{s1} = f\ (A, V_1)$. Therefore, the collector delay can be expressed as:

$$T_D{}^c = 0.7\, R_{cl}\, (3.25\, C_{oc} + \overline{C}_{s1}) \quad (14)$$

Emitter Follower Response

At the output, the emitter time constant for a positive going signal can be seen

$$T_e = C_o\left(\frac{r_b + R_{cL}}{\beta}\right) \quad (15)$$

to be where C_o is the total output capacitance. However, for a negative-going signal and $C_o >> C_b$ or C_L, the time constant for the emitter follower is chiefly a function of the RC time constant of the load capacitance C_o and the emitter-follower resistors. This relationship is due to the fact that a sharp negative going edge applied to the base of the emitter follower whose emitter is capacitively loaded tends to cutoff. Therefore:

$$\Delta T = C\frac{\Delta V}{I}$$

$$T'_e = \frac{C_o\, e_l\, R_o}{(V_{ref} - V_{ee})} \quad (16)$$

where e_l is the magnitude of the logic swing.

Thus, with the knowledge of the transistor equivalent circuit, the gate resistor and parasitic values and the nature of the load, the propagation delay for the gate can be determined by simply adding Eqs. 12 and 14 to the average of Eqs. 15 and 16. Fig. 3 shows the speed performance of a typical gate at various load conditions.

LAYOUT CONSIDERATIONS

Since the circuits described in this paper are the first digital integrated circuits to draw relatively large current (22 mA) many layout practices used in the past are inadequate. This consideration is especially true of the Spectra 70/45, 70/55 circuit, which contains two high-power gates along with a tracking reference voltage source. Fig. *1* showed the actual circuit layout. Some of its features are:

1) heavy ground metalization, i.e., low resistance;
2) wide resistors with large contacts, and thus good tolerances;

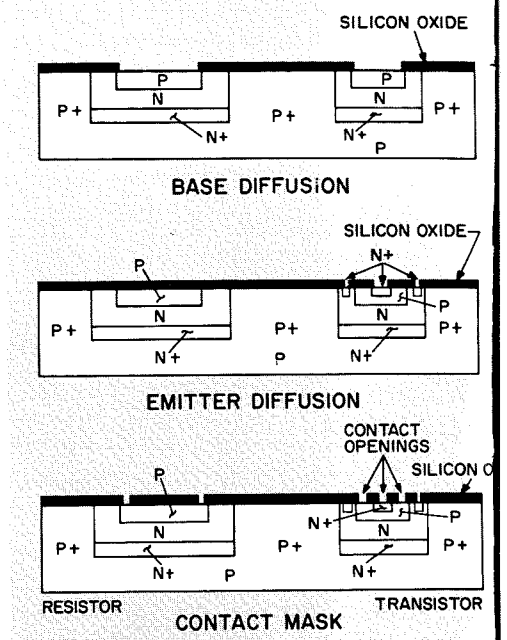

Fig. 4—Successive diffusion steps: a) base diffusion, b) emitter diffusion, and c) contact mask.

3) small geometry input transistors;
4) no current paths through high-resistivity collector regions;
5) short and wide output metalization wires.

Notice, also, that the output transistors are of a large multistripe geometry. This geometry with its associated small V_{be} drop helps prevent output droop under heavy DC load conditions.

Another consideration which was carefully observed in the above-mentioned layout is the use and location of tunnels. Tunnels are low resistance paths of semiconductor material, usually an emitter diffusion, which are used to avoid metalization crossovers on the monolithic chip. The resistance of these tunnels is characteristically 3 ohms. Therefore, their effects can well be minimized by placing them in low-current paths. However, the tunnels do represent a large capacitance to substrate. Care must be taken to avoid having them placed in the circuit where slow down effects can be encountered. In the layout of Fig. 1, three tunnels are used.

EFFECT OF PACKAGE THERMAL CHARACTERISTICS

Because of the relatively high power-dissipation of the circuits presented above, the thermal characteristics of the

circuit package becomes an integral part of the analysis of the speed and logic level behavior of the circuits.

If the circuit-chip temperature rises excessively, slow-down due to saturation is encountered. For this reason, it is desirable to house high power circuits in low-thermal-resistance packages. However, there are other important reasons why this is desirable. First, the failure rate of a circuit increases exponentially as the junction operating temperature increases. Therefore, for the highest reliability, the coolest circuit is desired. Also, as the thermal resistance of the integrated circuit package approaches zero, its effect on circuit operating performance diminishes thus removing one more design variable. This consideration becomes especially important when a high-power circuit is being supplied to a user from more than one vendor.

By far, the majority of high-speed circuits fabricated at RCA to date have been housed in fourteen-lead flat packages. The heat radiating surface is a ceramic material whose largest radiating surface is 0.25 × 0.25 inch. The integrated-circuit chip is mounted on this ceramic slab by means of a metal glazing process. Some heat is also conducted away through the metal leads which are bonded to the chip. The average thermal resistance of this package is approximately 100°C per watt.

FABRICATION

Diffused isolation junctions are required for electrical separations of the diffused elements included in a single block. Although these junctions will effectively block the passage of DC currents, they also add to the parasitic capacitances in the circuit. This will affect high-frequency performance adversely. The number of size of isolation areas can be held to a minimum and the total stray capacitance thereby substantially reduced by the careful selection and application of the elements within the circuit configuration used.

The fabrication of the integrated circuit requires techniques that are essentially extensions of procedures currently used in making other silicon planar epitaxial devices. The basic steps are outlined in the following paragraphs.

The silicon wafer used for this type circuit has an n-n^+-p structure. The first step in the fabrication process after the n^+ and n layers are grown is to form isolated nn^+ regions in the pellet. These regions are made by growing a silicon oxide over the entire wafer surface. The oxide on the n surface is preferentially removed, by means of conventional photoresist techniques, to expose areas into which p-type dopants (boron) are deposited on the wafer and is diffused through the nn^+ layers. These areas isolate the individual elements of the integrated circuit from each other and form back-to-back p-n diodes which will be reverse biased thereby electrically isolating the different n regions. A second photoresist and etch operation removes the oxide above the pads into which the resistor and transistor bases are formed simultaneously by diffusing a p dopant into the designated isolation areas. These regions, shown in Fig. 4a, are diffused with boron to a sheet resistance of 175 ohms per square.

The value of sheet resistance required to establish the desired resistor values is determined by two factors: the depth of the diffused junctions, (x_j) and the concentration of impurities (C_s) at the surface of area in question. Because the resistor and transistor base are diffused simultaneously, x_j and C_s must be selected with regard to the performance of both the transistor and the resistor. The variation in sheet resistance as a function of temperature is shown in Fig. 5. This value of sheet resistance is consistent with the requirement for satisfactory transistor action; for adequate performance, the sheet resistance is fixed at 175 ohms per square. This restriction imposes a practical limit of approximately 20,000 ohms; above this value it becomes economically impracticable because of the large areas associated with resistors of this size.

After the resistor and the transistor base have been diffused, the oxide is photoetched from the areas into which the emitter and collector n^+ contacts are to be diffused. An n-type source (phosphorus) is used to form the transistor emitters and the low-resistance contact areas for the transistor collectors (which must be contacted at the surface of the pellet in monolithic integrated circuits). Fig. 4b indicates the diffusion step. A final oxide is then grown over the whole wafer. The oxide is then selectively removed by photoresist techniques at the contact points for the various components as shown in Fig. 4c. Aluminum is then evaporated over the entire wafer. During evaporation, the wafer is kept at a temperature which is sufficiently high to cause the aluminum to microalloy with the exposed silicon contact areas. The aluminum is then selectively etched so that the remaining metal forms the proper connections for the circuit.

CONCLUSIONS

High-speed operation of integrated-circuit digital-logic gates can be attained even in the presence of parasitic components. Contributing to this achievement are factors such as:

1) *DC Considerations* — Selection of circuit configurations to minimize the effects of parasitics
2) *AC Response* — Selection of transistor geometrics to optimize performance under particular load considerations
3) *Circuit Layout* — Consideration of the integrated chip layout for high-current units.
4) *Package Thermal Characteristics* — Consideration of the thermal characteristics of the integrated circuit package in over-all gate performance.

Once these factors have been included in the design analysis and satisfied, the required circuit parameters can be translated into a circuit layout and fabricated by techniques similar to those used in making silicon planar epitaxial devices.

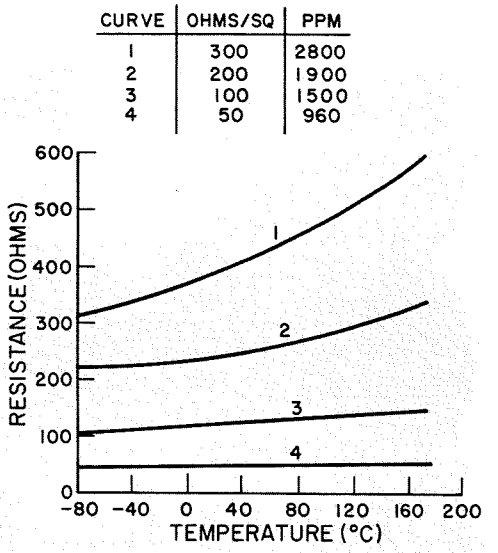

Fig. 5—Diffused resistors (resistance as a function of temperature for various resistivities).

BIBLIOGRAPHY

Much of the background of RCA work on digital monolithic-silicon integrated circuits, and details on their design, fabrication, and packaging will be found in the following collection of papers:

1. *RCA Integrated Circuits (Reprint Booklet, PE-216, P-217, P-218* or *PE-214)* A collection of 15 technical papers by RCA scientists and engineers. Reprinted from the RCA ENGINEER, Vol. 10, No. 3, Oct.-Nov. 1964.

THE IMPACT OF MONOLITHIC INTEGRATED CIRCUITS ON COMPUTER DESIGN

A Case Study of Spectra 70/45 and 70/55

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The larger two systems of RCA's new Spectra 70 family, Models 70/45 and 70/55, use monolithic silicon integrated circuits for the basic logic. This paper describes the effect that monolithic silicon integrated circuits have on the design of these third-generation computers. The relationships between circuit concept, packaging and device restrictions, interconnections, and system application are discussed, along with the reasons leading to the choice of the specific monolithic silicon integrated circuit found in the Spectra 70/45 and 70/55.

THE ENIAC, a computer which utilized radar-type circuits and vacuum tubes, evolved approximately two decades ago. Such early vacuum-tube data processors were physically large, high-power-consuming machines. Then, the advent of economical, high-speed switching transistors in the early 1960's was responsible for the appearance of a second generation of digital computers. Transistorization allowed more circuits per main frame, while system physical size was still greatly reduced. However, even with this physical reduction, 20% to 40% of the machine cycle time was lost because of propagation delay in the backplane wiring and other interconnections. It becomes obvious that further reductions in machine size would be necessary for higher-speed operation. Such a reduction has been made possible by microelectronics techniques, through which a decrease in size of the basic switching circuit can be achieved. Thus, a new third generation of computers are evolving, exemplified by the RCA Spectra 70 series, in which the larger systems—the Spectra 70/45 and 70/55—have capitalized on the potential of the monolithic silicon integrated circuit.

CIRCUIT COST

The motivating element in the emergence of the new generation computer is the availability of monolithic integrated circuits at prices competitive with hybrid circuits, and physically smaller by an order of magnitude. The use of monolithic integrated circuits results in an overall miniaturization of the basic processing unit and the high-speed memory. The total electronic complement of a digital data processing system profits by the miniaturization promised by monolithic integrated circuits and results in more throughput per customer dollar. Thus, the move toward integrated circuits in the Spectra 70/45 and 70/55 results in lower cost and smaller size.

Higher speed is an advantage brought about by this overall miniaturization; the lower cost is brought about by the mass production techniques of batch processing. Although the low cost is the most important advantage, other design features such as small size, low weight, and high reliability are of primary importance in certain selected applications.

The general use of integrated circuits in all types of electronic equipment will be brought about primarily by its low cost, which is the basic advantage of the monolithic integrated circuit over the discrete circuit or ceramic-base multichip modules. An integrated-circuit machine must be less expensive to produce and assemble in order to be considered as serious competition for other types of machines in a commercial market.

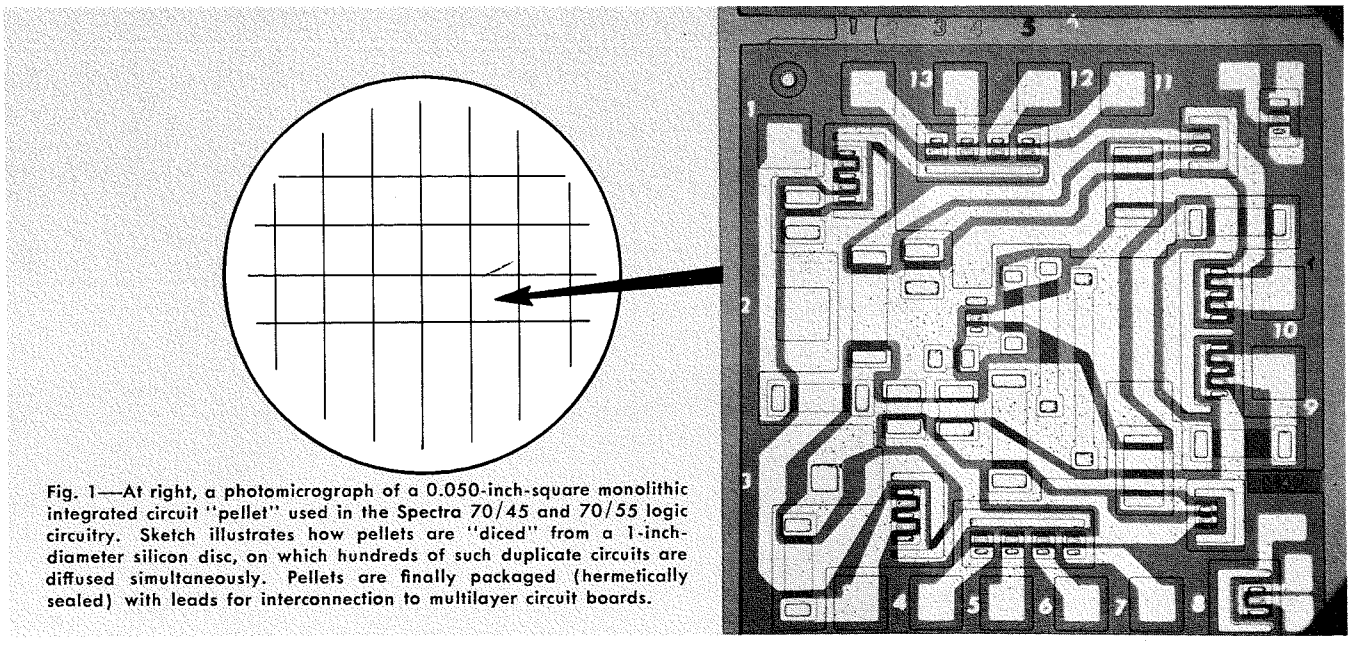


Fig. 1—At right, a photomicrograph of a 0.050-inch-square monolithic integrated circuit "pellet" used in the Spectra 70/45 and 70/55 logic circuitry. Sketch illustrates how pellets are "diced" from a 1-inch-diameter silicon disc, on which hundreds of such duplicate circuits are diffused simultaneously. Pellets are finally packaged (hermetically sealed) with leads for interconnection to multilayer circuit boards.

FACTORS IN LOW COSTS

Low costs of integrated circuits result from the manufacturing processes by which such circuits are produced. Up to 500 duplicate integrated circuits, each consisting of many active and passive circuit functions, can be diffused on a single wafer 1 inch in diameter. Twenty such wafers can be diffused in an oven simultaneously. Operational circuits are made by a series of steps of epitaxy, masking, etching, diffusion, oxidation, and metallization.

Up to this point, no major labor cost has been incurred. The 1-inch-diameter wafers are then diced, and each resulting 0.050-inch-square pellet (containing the complete circuit) is attached to an insulated base, or *header*. Leads are attached from a pad on the substrate to the lead frame by means of thermocompression bonds, and package lids are then assembled. This is followed by hermetic sealing and centrifuge conditioning, which is performed to screen out "leakers" and "bad bonds." Finally, electrical tests are performed to determine which devices meet specification.

The cost per circuit can be computed by determining the process cost of the various steps. Beginning with a 1-inch-diameter, silicon epitaxial wafer, it can be taken through isolation diffusion, N+ diffusion (buried layer), base-and-resistor diffusion, emitter diffusion, oxidation and metallization—and there is only the material cost, setup cost, plus several days of actual processing and overhead (amortization of capital facilities). With good production yields, this initial pellet cost can be only pennies per circuit (neglecting the overhead cost).

The final assembly of the pellets into operational packages and subsequent electrical tests play an important part in yield and final circuit cost. These items are incurred primarily on a per package basis, since the cost is a function of the labor performed on a package. When more than one circuit can be implemented on each pellet, the cost per circuit is reduced. A final cost of $2.00 per package is reasonable in the near future—thus, there is good promise of lower costs than could be achieved with equivalent multichip or discrete-circuit techniques.

CIRCUIT DESIGN

When a circuit designer is first introduced to integrated circuits, it becomes obvious that his basic skills are still required but that he will have to redirect his thinking. He will find that (at the present state of the art) inductors are nonexistent, that capacitors pose production difficulties and their use should be avoided. Resistors, 10,000 ohms or less, can be produced to a +20% absolute tolerance and a tolerance ratio of 4%. Transistors and diodes are readily achievable and are preferred over all other components, since they utilize less area and possess parameters that are more easily controlled.

The major adjustment for the circuit designer is a philosophical one. In the past, he was accustomed to passive components of high precision and low cost. His aim was to minimize the use of expensive active components. With integrated circuits, he must concentrate on the extensive use of active devices and minimize the use of passive components. Table I lists the properties of resistors available in integrated circuits.

The choice of a circuit to be used in a computer is always a difficult one and is influenced strongly by the requirements of the system.

Initially, the circuit configuration depends largely on the switching speed required. This in turn is derived from the speed requirements of a machine, which is eventually determined by the market place and customer requirements. Once the machine speed, memory speed, and logic design philosophy are decided upon, the circuit speed is derived from the number of logic decisions to be made in a given machine cycle.

The Spectra 70/45 circuit requirements were stated very simply as follows:

logic pair delay: 24 ns, includes worst-case temperature, voltage, and life
fan-in: 8
fan-out: 6
power: 100 mW
noise immunity: 25% of signal swing

Several manufacturers were asked to develop a circuit to the above requirements, with the choice of configuration left to them. The circuit configurations of Fig. 2 were investigated: *a*) *complementary transistor logic* (CTL), *b*) *diode transistor logic* (DTL), and *c*) *current mode logic* (CML).

STANLEY E. BASARA graduated from St. Joseph's College, Philadelphia, Pennsylvania with a BS in Electronic-Physics in 1956 and joined RCA the same year. He attended University of Pennsylvania Moore School of Electrical Engineering in pursuit of his MSEE. Mr. Basara spent several months with RCA-EDP as a co-op in the original Bizmac section. He worked with the circuit design group for the 501 computer, and was project engineer of circuit design for the MUX/ARQ-2 and the 301 computer. In 1961, Mr. Basara became Group Leader and has occupied that position until the present, wherein his assignment is the supervision of circuit design for the Spectra 70/45 and 70/55. He is a member of the IEEE.

The DTL circuit (Fig. 2b) consumed too much power and could not meet the speed requirements of 24 ns without a selective gold doping process. In this design, the transistor must be gold-doped to provide low storage. The level-setting diode in the base must be non-gold-doped to provide cancellation charge for the charge storage in the transistor. Several attempts were made at providing discharge paths for the load current (Fig. 3). This illustrates the extensive use of active devices to solve difficult circuit problems.

The CTL circuit (Fig. 2a) came much closer to providing the necessary speed requirements, but was rejected on the basis of poor noise immunity. The CTL circuit also lacked the proper logic function and could not provide the *phantom or* operation at the output terminal.

The CML circuit was finally chosen for the Spectra 70/45 and 70/55. Its practical configuration is shown in Fig. 4. This was successfully produced in a monolithic form by the RCA Special Electronic Components and Devices Division in Somerville.

CML CIRCUIT OPERATION

The CML operates in the following manner (referring to Fig. 4). Resistors R_1 and R_2 and transistor Q_6 provide a bias voltage of approximately −1.2 volts at the base input of the bias transistor Q_5. Transistors Q_1 through Q_4 act as inputs to the gate. Transistors Q_7 and Q_8 provide inverted and noninverted outputs respectively. With the gate inputs biased at −1.6 volts, the base-emitter junctions of transistors $Q_1 - Q_4$ are nonconducting, being forward-biased by approximately 0.4 volt, while 0.6 volts minimum is required for conduction. Current flows through R_{c4} and

TABLE I—Integrated-Circuit Resistor Properties

Specific resistivity	2.5Ω to 300Ω per square
Range of resistance	15Ω to 30,000Ω
Tolerance	10% to 20%
Temperature coefficient	500 to 2,000 parts per million per °C

V_{be} of Q_7 establishing an inverted (with respect to the input) *nor* output voltage of −0.8 volts. Transistor Q_5 is forward-biased and conducts approximately 6 mA collector current, establishing a voltage of −0.8 volts at the junction of R_{c3} and the collector of Q_5. The *or* output level is set by V_{be} of Q_8 and the ratio of R_{c5}/R_e and results in a non-inverted output of −1.6 volts.

When one input rises to −0.8 volt, the *nor* output is at −1.6 volts, and the *or* output is at −0.8 volt. Thus the Boolean expression shown in Fig. 5 is derived.

The characteristics of this circuit are outlined in Table II as well as the characteristics of several other digital logic circuits used in other RCA computers.

Since none of the transistors operate in the saturated mode, the unloaded switching speed of the circuit is limited by the frequency response of the input and output transistors and by the internal parasitic capacitances. It is important in the fabrication of the circuit of Fig. 4 to maintain low output capacitance of the input transistors, low parasitic capacitance of resistors R_{c4}, R_{c5}, R_c, R_{o1}, R_{o2}, and low intrinsic resistance of the output transistors. An unloaded stage delay of 3 ns has been calculated for this circuit using typical integrated circuit parameters. At present, a typical pair delay of 18.0 ns has been established when driving 100-pf output capacitance, including six input loads. Several other important characteristics were responsible for the choice of this circuit:

1) it provided the capability of a *phantom·or* operation at the output,
2) it provided an inverted output,
3) it requires only one power supply,
4) it provides a constant current drain to the power supply during the switching operation,
5) it would occupy less area on an integrated circuit wafer than an equivalent RTL or DTL,
6) the circuit has an excellent signal-to-noise immunity ratio,
7) the circuit has a high-input impedance and is suitable for "transmission line" operation, an essential item in a high-speed computer.

The inverted output resulted in a saving of 20% of the total devices required in a basic processor. The CML circuit exhibits good DC and AC temperature stability. Logical *1* level has a positive temperature coefficient of 1.4 mV/°C while *0* level has a positive temperature coefficient of 0.8 mV/°C. The circuit speed is specified up to 60°C but the circuit has the ability to operate well into the range of 100°C with a speed degradation of 2 to 10 ns. Finally, this

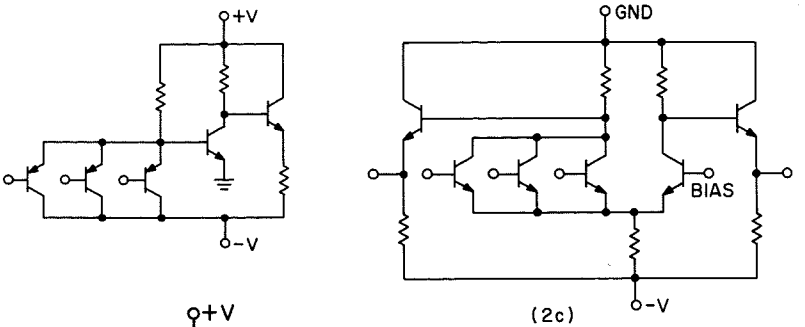


Fig. 2—Various types of logic circuits: 2a, complementary mode logic; 2b, diode transistor logic; and 2c, current mode logic.

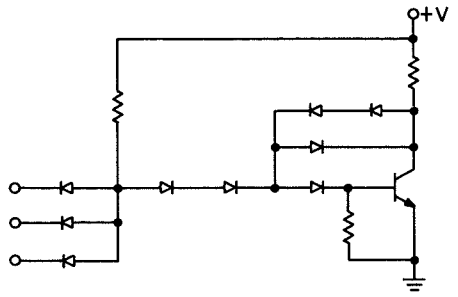


Fig. 3—Diode transistor logic circuit—with additional components for machine use.

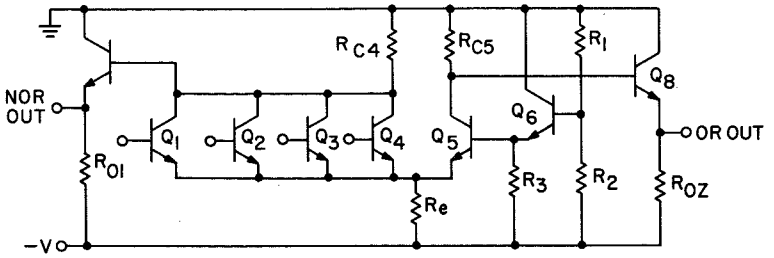
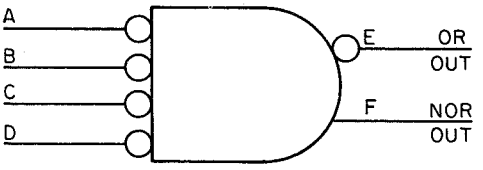


Fig. 4—Detailed schematic of current mode logic circuit.



$$F = \overline{E} = \overline{A} \circ \overline{B} \circ \overline{C} \circ \overline{D}$$

Fig. 5—Boolean expression for CML circuit.

TABLE II—Comparison of Circuit Parameters

	70/45	70/25	3301	601	301	501
Pair delay, ns	24	50	52	92	232	1,000
Fan-in	8*	10	10	10	10	2
Fan-out	8-16**	13	8	5	5	5
Noise immunity, %	±30	+3 −48	+12 −18	±20	±15	±10
Temp. range, °C	10-60	15-55	15-55	15-55	15-55	15-55
Signal swing, volt	−1.6 to −0.8	0 to +5	−5 to 0	−5 to 0	0 to +6.5	0 to +6.5
Configuration	CML	DTL	DTL	DTL	DTL	RTL***
Power, mW	125	70	143	125	227	378

* This is limited by the package configuration of the integrated circuit; a fan-in of up to 20 can be provided with some degradation in circuit speed.
** This is determined by the mode of interconnection. A non-terminated line can drive up to 16 loads. This can be increased by diffusing higher input transistors of higher β.
*** Resistor transistor logic.

type circuit can be designed to provide an interchangeable family of circuits capable of a range of speeds both higher and lower than 24 ns. The circuit speed can be increased by reducing transistor geometries and internal parasitic capacitance.

Several disadvantages exist however. A circuit having a voltage swing less than 1.0 volt imposes design difficulties with associated circuits in a computer. For example, the high-current circuits of the high-speed memory require a stage of amplification. Other circuits having the same problem are lamp drivers, one-shots, line drivers, line receiver, etc. A second disadvantage is the total power consumption of the device. Originally specified at 100 mW per circuit, it became necessary to increase the power to 125 mW to provide a safe margin for worst-case pair delay.

PACKAGING OF INTEGRATED CIRCUITS

The effect of the integrated circuit is much more pronounced when considering the mechanical packaging required. The major influencing factor is the small size of the circuit package itself. Each diced pellet (0.050 inch square) contains a dual, four-input circuit. The pellet is housed in a ¼-inch-square, 14-lead flat package. Sixteen flat packs are placed on a 37-pin, 3 x 4 inch printed circuit card. These are soldered in place to pads 0.060 inch in diameter. Lines as narrow as 0.010 inch are used to interconnect flat packs on two-layer and three-layer cards. Interconnections from layer to layer are provided by plated-through holes. Up to 130 cards can be placed on a 17 x 17 inch multilayer printed-circuit backpanel. This backpanel provides a printed-wire interconnection scheme designed to yield an impedance of 100 ± 10 ohms which is supplemented, where necessary, with 100-ohm discrete wire over a ground plane. Connection from one back panel to another is made through a 48-pin printed-circuit board and connector using conventional wiring designed to yield 100 ohms characteristic impedance. Thus, the full interconnection medium presents a controlled 100-ohm transmission line to the logic circuitry.

The first problem encountered was the method of attaching the flat pack to the circuit card and of bringing signal leads to the circuit. For ease of manufacturing, the configuration shown in Fig. 6 was chosen. The staggered pad cluster allows signal leads to be brought through the integrated-circuit package area when necessary.

The power distribution configuration was chosen to provide a minimum inductance system without blocking signal paths or using excessive area In this type of configuration, a limiting factor is the inductance of the power pin. As indicated above, lines as thin as 0.010 inch, spaced 0.025 inch from a second lead or 0.010 inch from a pad, are used. The flat package ribbon lead, 0.017 x 0.004 inch, is preformed, cut, inserted onto a plated-through hole, and soldered into place. The connector has 48 pins, spaced on 0.125-inch grid, which mounts on a printed backplane. The backplane provides the bulk of the interconnection wiring from card to card; its development is described in another article.[1]

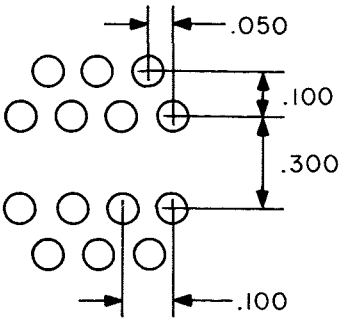


Fig. 6—Method of connecting integrated circuit package (ICP) to circuit card.

Obviously, the integrated circuit has had a major effect in upgrading the mechanical packaging of the computer, both in the area of engineering and manufacturing skills.

CIRCUIT INTERCONNECTION

The high speed and resultant fast rise and fall times, combined with the voltage swing of 0.85 volt, required the development of a controlled impedance transmission line interconnection system. Previous designs with the lower-speed circuits could safely ignore precautions that were necessary for this system. To predict total circuit delay, it is imperative that inductance and capacitance of interconnecting wires be controlled to known levels. Any unexpected ringing, signal-level discontinuity, or signal overshoot would result in a perturbation of the wavefront with a resultant effect upon the circuit delay. Neglecting the internal losses of the circuit itself, the speed is primarily limited by the output capacitive load. Long runs can be allowed only if the line is terminated in its characteristic impedance, since an unterminated line would result in a reflected wave. The design approach for the Spectra 70/45 and 70/55 was to replace conventional discrete wiring by printed-circuit techniques. The backplane is designed to simulate a 100-ohm line. Long lines are terminated in a 100-ohm resistor block. Line length is limited by the DC loss of the line and by crosstalk. In using this "transmission line" technique with the terminating resistor, it becomes important that the input impedance of circuits connected in midline be as high as possible in order to minimize reflections. With all impedances known, it becomes possible to predict the amount of reflection caused by logic gate loads tapped off the main wiring path. Therefore, it is possible to formulate a set of wiring rules to determine spacing requirements for loads on the line in order to keep reflections to a safe level. The DC input impedance to the CML circuit is on the order of 6,000 ohms. The AC impedance simulates a 5-pF capacitor in shunt with the line.

NOISE CONSIDERATIONS

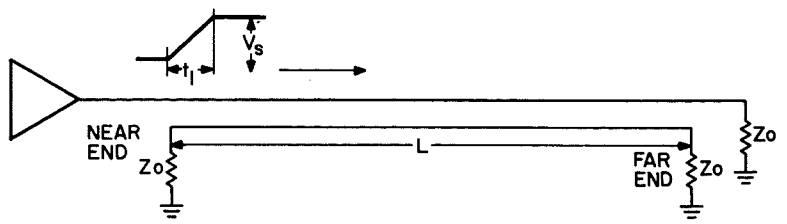
Much has been said and written about noise in a machine the physical size of a commercial data processor. The printed-circuit transmission line medium adapts itself readily to predicting and controlling noise without the necessity of burdensome wiring rules. With this approach, each machine will be very similar to all others because of the uniform printed-wire connections.

Noise can be subdivided into three major categories: *crosstalk*, *reflection*, and *power distribution*. The Spectra 70 machines are designed with the assumption that only 70% of each noise source may be present at the same point at any one time. Each noise source is defined as the worst possible noise generated within the wiring rule allowed.

Crosstalk

Crosstalk noise is the noise picked up on a sense line when the adjacent line is being switched (consider Fig. 7). Two transmission lines run in parallel for length l. The switching line has a ramp voltage as shown. The sense line is a segment of a long serial net and is represented with both ends terminated by Z_o.

The mutual inductance of the two parallel lines is L_m per unit length and the mutual capacitance is C_m per unit length. Consider one segment of the sense line: When the signal passes through the corresponding segment of switching line y, a voltage of the magnitude $L_m(di/dt)$ and a current of the magnitude $C_m(dv/dt)$ are induced on the sense line. The induced voltage and current signal propagates in both directions along the sense line. That portion of the noise pickup traveling in the opposite direction from the switching line signal is called the backwave pickup. That portion of the noise



V_s = DRIVE SIGNAL AT SENDING END OF DRIVE LINE

V_{cm} = PICKUP SIGNAL Cm dv/dt

V_{lm} = PICKUP SIGNAL Lm di/dt

C_m = MUTUAL CAPACITANCE

L_m = MUTUAL INDUCTANCE

Fig. 7—Example of noise due to crosstalk.

pickup traveling in the same direction with the switching line signal is called the *forward-wave pickup*. The noise pickup at the near end is in phase with the switching signal and its amplitude is independent of line length, when the propagation time on the sense line is greater than the rise time of the switching signal. The noise pickup at the far end may be in phase or 180° out of phase with the driving signal. This is dependent upon C_m, L_m, and is a direct function of line length. Typical noise pickups at the near end and far end are shown in Fig. 8.

Reflection

A pulse V_{sig} is propagated toward D having a rise time of 2 ns and an amplitude V_s of 0.85 volt. At point B, the pulse sees Z_o, the line impedance, in parallel with Z_{in}, the input impedance of the CML gate. A reflected voltage of pV_s is set up, where p, the reflection coefficient is given by the following transmission line formula,

$$P = \frac{Z_L - Z_o}{Z_L + Z_o}$$

where Z_L = load impedance (Z_o in parallel with Z_{in}) and Z_o = line impedance. The waveform at the source A, assuming that the source has an output impedance of Z_o, is shown in Fig. 10.

The amplitude of the reflection is a function of the impedance of the tap-off point, which includes the input impedance to the circuit. In the case of the CML gate C_{in} = 5.0 pF. Hence, reflected noise is calculated using the graph shown in Fig. 11. In addition to the C_{in} of the circuit, it is also important to know the capacitance of each element leading away from the tap-off point. Fig. 12 shows a typical connection with the contributing capacitive elements. In the practical case, the rise time of the driving pulse averages 6.0 ns and loads are usually spaced closer than 12 inches. The result is that reflections occur during the rise time, slowing the rise time and increasing the stage delay. There are two types of interconnection nets used in the 70/45 and 70/55 systems. These are classified as *terminated* (serial) and *unterminated* (radial) nets. The radial case is shown in Fig. 13. The drive pulse sees the full capacitive load at the output.

Included in the output load is line capacitance C_L = 75 pF and the input

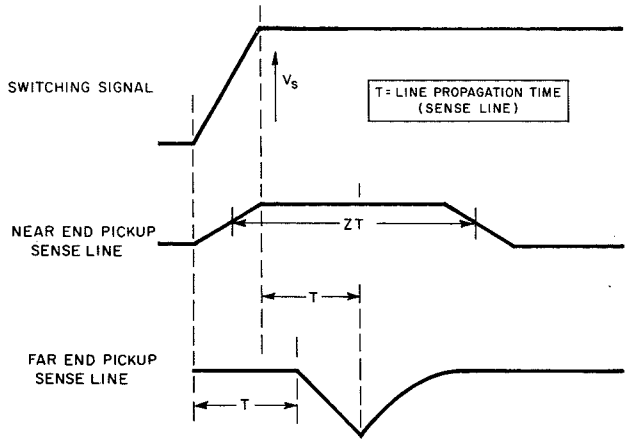


Fig. 8—Typical noise pickup on line of Fig. 7.

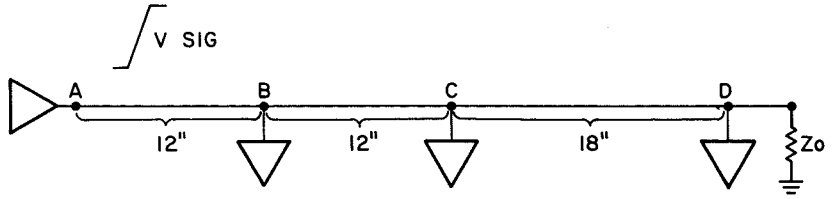
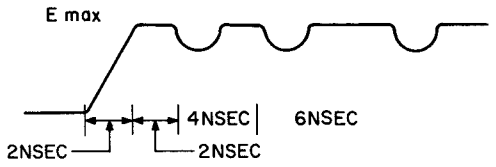


Fig. 9—Example of noise due to reflection.



WAVEFORM AT A DUE TO REFLECTIONS AT JOINTS B, C, AND D

Fig. 10—Waveform at source (A in Fig. 9) due to reflections at B, C, and D.

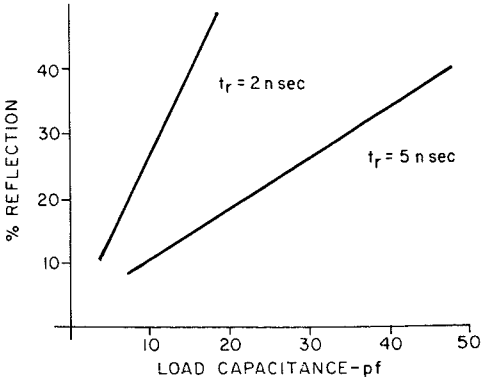


Fig. 11—Amplitude of reflected noise.

capacitance to each circuit $C_{in} = 6 \times 5.0 = 30$ pF. The configuration shown above was used to qualify the speed of the integrated circuit. The maximum length of wire used to connect a source to its farthest load, not requiring the use of a terminating resistor, is 8 inches. This is limited by the signal reflection from the open line which causes overshoot and ringing. The undershoot of the ringing must be kept below the level of noise immunity of the circuit, otherwise false pulses will occur at the output of a load. In the terminated net, the length of line is limited only by the DC loss of the line and by the noise generated in the computer environment. Delay curves are established for each configuration that allow a logic designer to calculate the speed of crucial timing chains.

Power Dissipation

Thus far we have discussed noise due to crosstalk and reflection. In order to exercise full control over noise, power distribution must be considered. The power distribution system must provide a low impedance path for power to all components of the system. This is accomplished by means of flat bus interleaved with ground layers. The AC response of the power distribution system is augmented by local decoupling to provide the transient power required by each unit. Here again is seen the advantage of the current-mode circuitry, viz., no transient power is required during switching, with the load current moving from one leg to the other. Therefore, the load on the power supply remains relatively constant. In summary, it is possible to predict noise by a careful analysis and thus successfully design a basic processing unit.

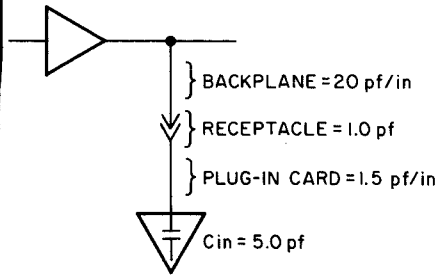


Fig. 12—Contributing elements of circuit input capacitance (C_{in}).

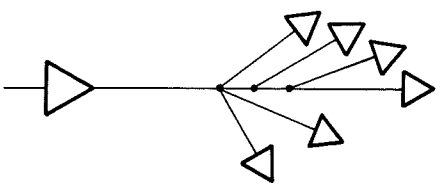


Fig. 13—Radial interconnection network.

SYSTEM INTERCONNECTION

One of the problems in any machine design is the interconnection compatibility between the basic processing unit and the input-output area. The first element in the problem is the ability to drive long lines. Special precautions must be taken to insure that a minimum of interaction occurs between input-output signals and the normal logic signals. The second element concerns the expanded memory concept which places added strain on the capabilities of a logic circuit. The control and data signal lines threaded between the basic processing unit and the high-speed memory must withstand signal degradation and be unaffected by noise. In addition to maintaining a high input impedance on the circuit, the capacitance of connectors and wiring must be considered.

CONCLUSION

Integrated circuits have provided an economical means to reliable, microminiature, ultra-fast circuitry. These speeds exact their toll in packaging design. Because of the reduction in size and increase in speed, more care must be exercised in order to ensure reliable use of the circuit. Consider the graph shown in Fig. 14 which indicates the plot of pair delay of RCA computer circuits versus year of introduction. Future machines will result in further reduction in pair delay. Designers indicate that this will be accomplished by allowing more logic functions to be performed at the integrated circuit level. Two important items must be considered before such an approach is considered acceptable: Increasing the number of logic functions in a single integrated circuit directly increases the number of variations which the integrated circuit manufacturer must control and produce, thus cutting into volume and the "batch process" concept. Secondly, it implies that more pins per package must be available, which complicates the present difficulty in interconnection.

The true impact of the third-generation machines will not be apparent until full advantage is taken of the small size of the integrated circuit. It is obvious that reducing the machine size will result in a reduction of useless signal propagation time. The large number of long interconnecting wiring runs will become unnecessary due to reduced volumetric requirements of the logical elements. Each reduction in machine size will result in a lower power circuit, and a smaller machine; the limit in size reduction being determined by the state of technology and the ingenuity of people responsible for its application.

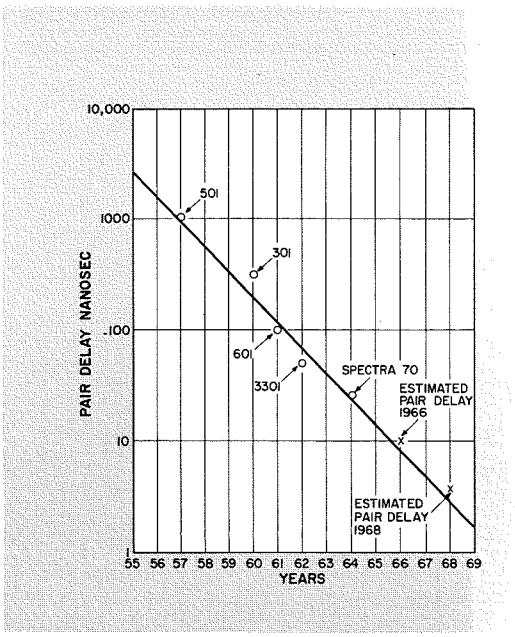


Fig. 14—Pair delay of RCA computer circuits versus year of introduction.

This reduction in machine cycle time will not occur immediately. An educational boot-strap must take place primarily in the enginering areas to achieve maximum utilization of volume. A concurrent development in the manufacturing areas is a necessity to develop fabrication techniques commensurate with the enginering advances.

ACKNOWLEDGEMENT

The author wishes to thank the members of the EDP Circuit Design Group, Applied Research, Electronic Components and Devices, and Defense Microelectronics who contributed during the various design phases of the integrated circuit for Spectra 70/45 and 70/55.

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PHOTOCHEMICAL LABORATORY

Processes for Integrated-Circuit Multilayer Printed Wiring

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and
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The RCA Photochemical Laboratory in Camden combines precision photomechanic artwork generating techniques with chemical methods in the fabrication of multilayer printed-wiring boards. Typical 18x18-inch multilayer interconnection boards such as those used in the new RCA Spectra 70 computers provide thousands of connections. This paper describes the Lab and discusses the equipment used to develop techniques and processes that enable Camden Plant manufacturing activities to produce printed wiring boards that satisfy modern integrated-circuit applications. The capability of this facility is not limited to printed-wiring networks, but can be used for all applications requiring precise graphic delineations.

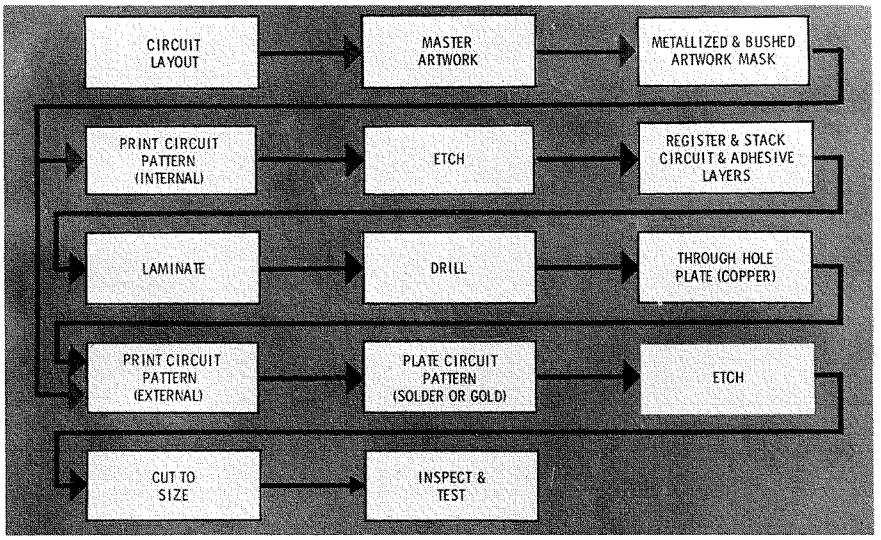

Fig. 1—A simplified flow diagram of the multilayer printed-wiring sequence for the plated-through hole concept, from circuit layout to the completed multilayer board.

IN military and space electronics, the emphasis on miniaturization and high-density packaging has highlighted the need for interconnection techniques to accommodate the increased wiring density. With integrated circuits beginning to play a predominant role in both military and commercial systems,[1-3] and with circuit complexity and speed also increasing, the need for an improved interconnection techniques capability is compounded.

Printed wiring plays a primary role in solving the interconnection problem, but with the increased wiring density, the limits of single- and double-sided printed wiring are quickly exceeded. Thus, the technique of stacking and laminating printed-wiring boards to form multilayers has been developed to meet the high-density interconnection requirement.

FORMATION OF THE RCA FACILITY

As it became apparent that the trend toward increased sophistication in interconnection technology would continue, it was decided to develop an in-house capability. Many of our current designs require a degree of critical process control that could not be obtained with any confidence from outside sources. Thus, a new laboratory facility was started in

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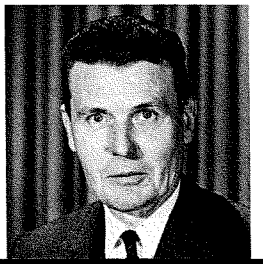
G. H. LINES received the BSME from the University of Vermont in 1950. Following graduation, Mr. Lines worked as an Industrial Engineer supervising the design and improvement of bottle handling equipment. He was subsequently employed by E. I. DuPont Company as a liaison engineer at New York Shipbuilding. He joined RCA in 1953 as a member of Mechanical Standards, responsible for standardization of mechanical components and wiring devices. In 1960 Mr. Lines was placed in charge of the Equipment Packaging Standards group responsible for development of packaging techniques utilizing electronic modules ranging from miniature modules to electronic enclosures. He was promoted to his present responsibility in 1961 for all phases of consultation and development of control specifications in the areas of printed circuit standards, modular packages, and microcircuit device selection and applications. He is additionally responsible for the operation of the Laboratory described in this paper. Mr. Lines is the RCA representative in the Institute of Printed Circuits.

FRANCIS X. THOMSON received his BS from Providence College in 1936 and his MS in Chemistry from Rhode Island State University in 1938. Additional graduate work in Chemistry was performed at Columbia and Princeton Universities from 1939 to 1942. From 1938 to 1942 he was an associate professor in the Chemistry Department at Seton Hall University. Mr. Thomson was engaged in analytical and physical chemical research and development at Hoffman-LaRoche, Inc. and Merck and Company from 1942 to 1945. He joined RCA in 1945 as an engineer in the Chemical and Physical Laboratories in Camden, N.J. Since that time he has been engaged in materials problems with responsibilities in the areas of corrosion, protective coatings, printed wiring materials and methods, chemical analysis and metallurgy. His present position is Engineering Group Leader of the Material Analysis and Metallic Materials Section of Central Engineering. He is a member of the American Chemical Society and the Society for Applied Spectroscopy.

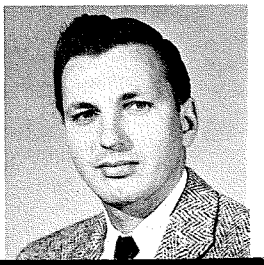
E. A. SZUKALSKI graduated from Drexel Institute of Technology in 1957 with a BSEE and in 1961 with an MSEE. In 1957, Mr. Szukalski joined RCA's Modular Components Engineering Group where he was active in the design of control systems. During this period, he also performed research and development on circuit packaging techniques. He also assumed technical responsibility for the performance testing of the printed circuit modules utilized on the BMEWS program. In 1961, Mr. Szukalski became a Project Engineer engaged in the design and development of advanced packaging techniques for industrial and military applications. In 1962, he became Leader, Design and Development, Design Standards, Central Engineering and is responsible for the design and development of advanced electronic packaging techniques, equipment enclosure designs, interconnection designs, and the establishment of associated Company Design Standards. Mr. Szukalski is the RCA DEP representative to EIA Committee on Printed and Modular Components (P9.3) and to Aerospace Industry Association (AIA) Microelectronic Panel (MEP). Mr. Szukalski was the originator and first chairman of the Institute of Printed Circuits (IPC) Multilayer Printed Wiring Board Committee. He is a member of IEEE and the Franklin Institute.

G. H. Lines

F. X. Thomson



E. A. Szukalski



early 1964 to develop the necessary methods and controls required by the Camden Plant to produce fine-line and multilayer printed wiring in support of not only military but also commercial programs (such as the Spectra 70 computer).

The new laboratory is involved in two types of operations; namely, *photomechanic techniques* or artwork generation, and *chemical methods* or manufacturing techniques. Although this lab has a range of capability much beyond that of printed wiring, this paper will use the multilayer printed-wiring application as a base for describing this capability. Some of the other applications for these facilities will also be highlighted during the description of the key components.

MULTILAYER PRINTED-WIRING PROCESSES

The many process steps in the production of multilayer and fine-line printed wiring require very accurate control. Methods commonly used in production of conventional single- and double-sided printed wiring are often inadequate. The trend toward larger boards such as those used in the Spectra 70 also complicates the already critical tolerance requirements.

The generation of artwork is the first process step in printed wiring; it is also the most critical, since variations here are propagated or expanded throughout the remaining process steps. Basically, the end product can be no better than the artwork from which it is produced. To minimize variations due to temperature and humidity, master artwork is generally produced on glass rather than on the so-called stable films. To provide an image which is resistant to damage during use and handling a metallized mask is produced on glass from the master artwork. This metallized mask also has a bushing accurately placed in the glass to assure accurate pattern registration. In the multilayer board fabrication process, the necessary artwork masks are first used to produce the internal layers. This series of process steps is similar to the techniques used to produce single-sided boards; in many instances, internal layers of multilayer boards consist of a number of thin single-sided laminates.

The etched internal layers and two clad-laminates (which later become the external layers) are then registered and stacked with interleaving layers of adhesive. This layup is then laminated under controlled temperature and pressure to form a homogeneous laminated board. The next series of process steps is similar to techniques used to produce double-sided boards and it is in this area where the majority of variations occur to the basic process steps (see Fig. 1). Required holes are drilled in the laminated board under controlled drilling conditions; properly drilled holes are critical in this step to assure good interlayer connections. Epoxy smear and rough hole walls are two of the most common defects caused by improper drilling. The holes are metallized and then electroplated with copper; during electroplating of the through-hole, an equivalent thickness of copper is deposited also on the external layers.

Artwork is used again to print the desired pattern on the external layers. An overplating, usually gold or solder, is then applied on the previously produced pattern. The selected overplate serves the dual function of an etchant resist and as a surface aid to later processing, such as soldering. The board is then etched, cut to size, inspected and tested. Multilayer printed wiring processes involve two types of operations, those involving photomechanic techniques or artwork generation and those involving chemical techniques. A few of the more significant items of equipment associated with each of these areas are described in the following paragraphs in order to illustrate the flexibility and capability of this laboratory.

PHOTOMECHANIC TECHNIQUES EQUIPMENT

This area of the laboratory includes an automatic generator, a highly accurate photo-reduction camera, a large area contact printer, and photographic development and processing facilities. Since artwork is the first process and probably the most critical step in the production of multilayered printed wiring, the importance of precision in this work is obvious. The following items of equipment demonstrate this capability.

ARTWORK GENERATOR

The Artwork Generator was built to RCA specifications by the Gerber Scientific Instrument Corp.; specifications were developed after a concentrated study by cognizant personnel from DEP Central Engineering, Corporate Staff, EDP, RCA Laboratories and DEP Manufacturing. The Artwork Generator (Fig. 2) is an automatically operated system capable of generating large, precision, two-dimensional patterns, such as printed-wiring and integrated-circuit artworks, precision measurement devices, machine tool tape verification or other precision graphic displays requiring lines and/or point plotting over a large or small plotting area.

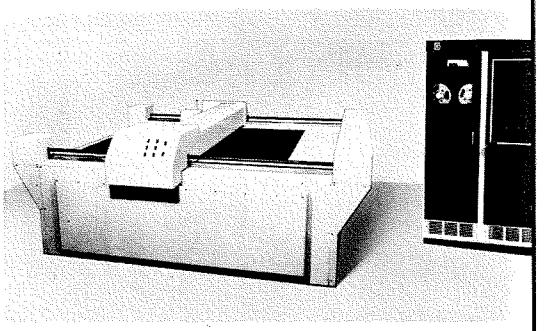
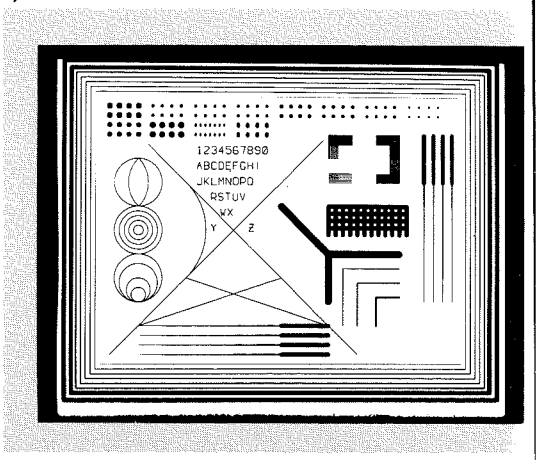


Fig. 2—The Artwork Generator is considered the backbone and probably the most important and most versatile piece of equipment in the Photochemical Laboratory.

Fig. 3—A typical pattern that can be generated by the Artwork Generator.



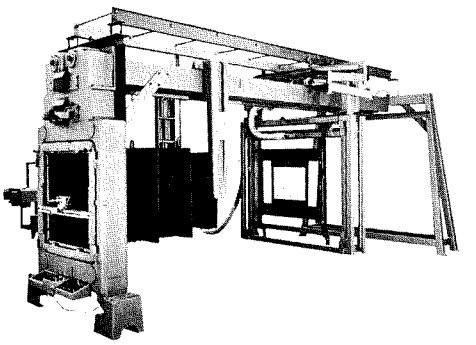
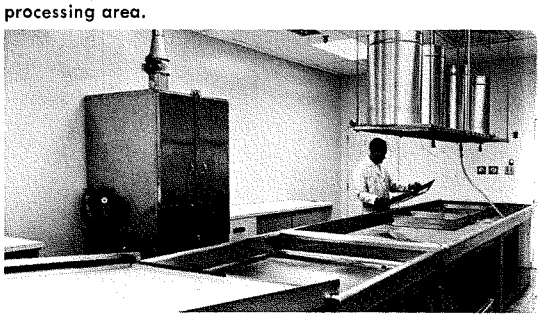


Fig. 4—The photo reduction camera gives 4:1 reduction within tolerances of 0.00025 inch or better.

Fig. 5—Photo-emulsion processing: all material preparation, including mixing, is accomplished in an adjoining room and pumped into the processing area.



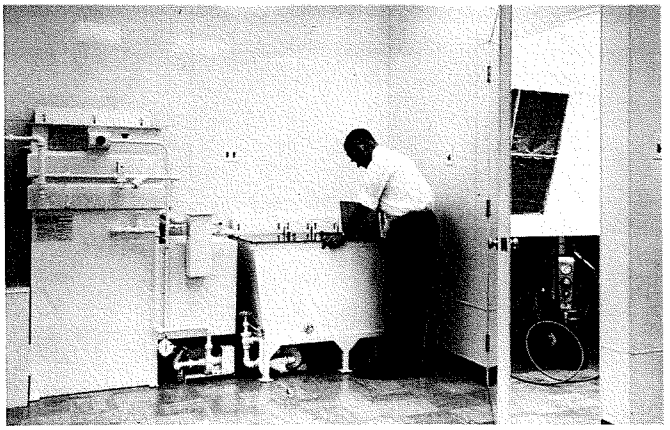


Fig. 6—The vapor degreaser, developing tanks and spray booth.

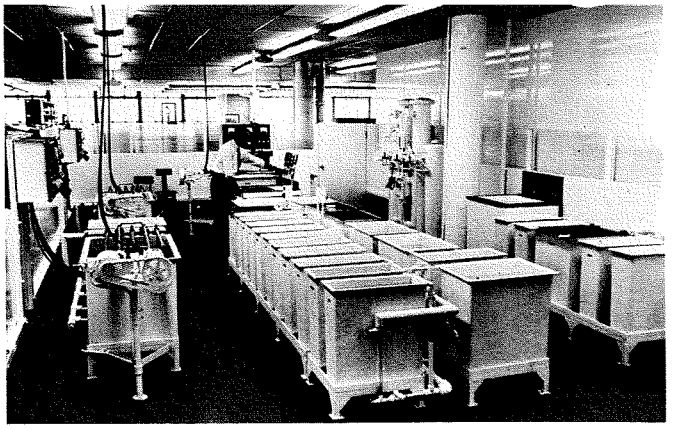


Fig. 8—The plating room includes tanks containing cleaning and metallizing solutions; see center and right. Acid copper and pyrophosphate copper plating tanks are at left. An engineer stands in front of a gold-plating tank used for a variety of materials such as nickel and solder.

PLOTTING PATTERNS

Patterns similar to those produced by manual coordinatographs, engine ruling, engraving, photographic step-and-repeat and other methods can be produced on this equipment to extreme accuracies. The heavy duty and precise plotting table is equipped with a variety of tool heads to allow for the generation of patterns consisting of straight and/or curved lines by photo printing, scribing, inking or routing to accuracies of ±.001 inch (repeatability, 0.0005 inch) over the entire plotting area.

The plotting area for a typical pattern (Fig. 3) is 48 x 60 inches and includes a vacuum hold-down capability. The input may be manual, or from paper or magnetic tape and is programmable in both incremental and absolute modes. Specific tape format and tape code details provide inputs to this equipment. The control console includes a 1,024-bit memory and operating controls for mode selection, feed rate, scaling, imaging, datum offset and others. The system is entirely digital in all logic and drive techniques, using digital differential analyzer techniques to drive the *X* and *Y* coordinate carriages on precision ball screws.

PHOTOREDUCTION CAMERAS

A second key component in the photomechanic techniques area is the photoreduction camera shown in Fig. 4. Advanced specifications were prepared jointly with DEP Applied Research and the camera built by Robertson Photo Mechanix, Inc.; it provides a precision capability second to none in the country for the larger image sizes required. The copy board is equipped to hold up to 50 x 60 inch film copy or up to 30 x 40 inch glass plate copy. Lenses are presently available to encompass a range of magnification from 2 times to 1/10 the copy size. A final image size of up to 20 x 24 inches can be provided. With respect to accuracy, the camera is capable of making reductions while maintaining a geometric distortion anywhere in the image plane to tolerances ranging from 0.001-inch true position to less than 0.0001 inch depending upon the reduction ratio. For example, using the minimum reduction ratio of 2:1 and a large 30 x 30 inch copy to a 15 x 15 inch photographic image, the maximum distortion is 0.001 inch. We have also reduced a 20 x 20 inch copy to a 5 x 5 inch photographic image (a 4:1 reduction ratio) to tolerances of better than 0.00025 inch. These geometric distortions compare to 0.003 inch, which is the best obtainable from any known outside sources.

The photographic image produced has a limiting resolution in excess of 20 line-space pairs per millimeter, producing sharp, usable 0.001-inch lines and spaces.

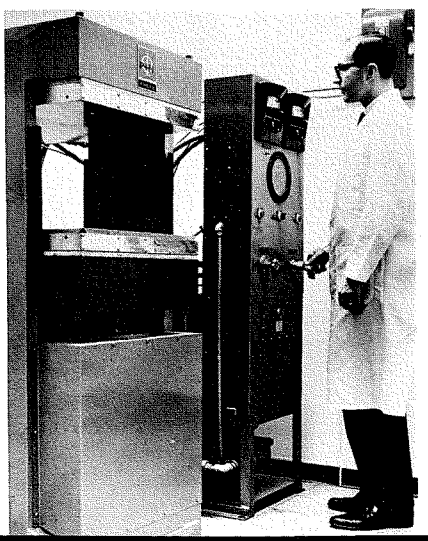
PHOTOEMULSION PROCESSING

In association with the camera and artwork generator equipments, facilities are programmed for optimum photoemulsion processing. This area, as well as all other areas in the photomechanic techniques section, is individually environmentally controlled. All work areas are clean rooms; temperature is controlled to 70° ± 1°F; humidity to 45 ±5%; and filtration for particle sizes equal to or greater than 8 micrometers is provided. Also, variable intensity safe lights are integral with all sections of the laboratory.

[*Ed. Note:* micrometer, the new standard term for micron, is 10^{-6} meters.]

In the photoemulsion processing area, methods are provided for handling photographic film and glass plates up to 30 x 40 inches (Fig. 5). The equipment includes stainless steel trays and sinks with water controlled to temperatures of 70° ± 2°F; a water filtered wash ring which provides a complete water change every 12 minutes; a wet viewing table; and a fired-on drying cabinet.

Fig. 7—Laminating press provides pressures up to 1,000 lbf/in² and handles boards up to 22 x 22 inches.



CHEMICAL TECHNIQUES EQUIPMENT

The manufacturing techniques development is primarily accomplished in the chemical methods area where investigations into the many process steps in the production of multilayer printed wiring are conducted. Investigations are directed toward selecting and exploring equipment and critical techniques for producing high-density printed wiring. This area of the laboratory includes photoresist application and development, laminating, plating, and etching.

PHOTORESIST APPLICATION AND DEVELOPMENT

One of the very critical processes in the fabrication of fine-line circuitry is the application of photosensitive resist materials for plating and etching. The processing of photosensitive resists is a multistage affair requiring rigid control.

Thin, uniform coatings of resist are applied to boards which have been previously chemically and mechanically cleaned. To obtain the required thin, uniform coatings on boards with or without holes, a mechanized spray gun is used. After the pattern is exposed to the sensitized surface, the pattern is developed in the developing tanks or vapor degreaser (Fig. 6).

LAMINATING PRESS

The press used to produce boards by laminating the etched epoxy glass lami-

nates and epoxy glass B-stage prepreg as the interlayer adhesive is shown in Fig. 7. Pressures up to 1,000 lbf/in^2 can be obtained by this press and boards up to 22 x 22 inches may be laminated.

In the manufacture of multilayers, a sheet of woven fiberglass impregnated with semicured epoxy, and known as B-stage prepreg, is used as an adhesive between layers of fully cured circuit layers. The prepreg is preheated for a short period and then cured under simultaneous applications of heat and pressure.

PLATING TANKS

Acid and pyrophosphate copper plating tanks are mechanically designed to agitate printed boards in the plating baths in a parallel or perpendicular direction to the anodes. A gold plating equipment is also included in the facility (Fig. 8).

After boards are drilled by methods which will provide clean, smooth holes, the holes are metallized for subsequent electroplating by the use of an electroless copper deposition system. The boards are then electroplated with copper until the desired plating thickness is obtained on the hole walls. Throwing power of the plating system is important so that satisfactory plating thicknesses on hole walls are obtained. The surface condition of the plated surface is important in later operations such as photoresist and etching.

HORIZONTAL SPRAY TYPE ETCHER

It was determined that fine-line etching can be more satisfactorily accomplished by a spray type etcher; after evaluation of the various spray etchers available, the etcher (Fig. 9) manufactured by Centre Circuits, Inc., was selected.

This horizontal spray type etcher was built to RCA specifications so that it will be an exact duplicate (except for reduced size and production capability) of the etchers being procured by the Camden Manufacturing Plant. This selection of equipments enables transfer of development data to the production area with a minimum of "debugging" and follow-up. Studies to determine effects of pattern configuration, type of resist and thickness of copper on etching have been conducted.

MULTILAYER BOARD

Significant features of the multilayer board (Fig. 10) are: its size, approximately 18 x 18 inches; 200 lineal feet of conductors per surface with controlled widths of 10 $\pm$ 2 mils; approximately 10,000 plated-through holes; and controlled dielectric thicknesses required for transmission line characteristics. These boards are presently being produced by RCA using methods and techniques developed by this Laboratory.

CONCLUSION

The rapidly increasing need for more condensed interconnection methods to keep pace with the microelectronics art requires continued development effort directed toward new techniques and processes that will make possible consistent production of finer lines, spaces and interlayer connections. This photochemical laboratory is a very necessary facility for this purpose and has already produced results in meeting the rigid requirements of the Spectra 70/45 and 70/55 backplane wiring panels.

The tolerances required for the preparation of artwork for integrated circuits and large backplane boards are such that use of conventional methods are no longer applicable in many designs. The problem of generating precision artwork has been recognized as being a fundamental requirement and major breakthroughs have been made by obtaining and utilizing the specialized artwork generator and camera equipment.

The many process steps and close tolerances required for production of multilayer printed wiring also dictate methods other than those used to produce conventional single- and double-sided boards. This problem has been attacked by determining variables involved and methods for controlling these variables. The facilities and the specialized skills, such as chemists and metallurgists, available in DEP Central Engineering, Camden, are the major contributing factors to the total effectiveness of this Laboratory.

It should be emphasized again that these facilities are not restricted to printed-wiring applications. Other applications which benefit from the use of accurate large-area patterns or from controlled chemical processes are equally within the scope of operational capability. In essence, the capability of this laboratory exists, but many applications to which it can be usefully directed are still to be defined.

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3. J. J. O'Donnell, "Packaging Design of Spectra 70/45 and 70/55 Computer System," RCA ENGINEER, *this issue.*

Fig. 9—This horizontal spray etcher was selected for the lab after evaluation of various types and manufacturers.

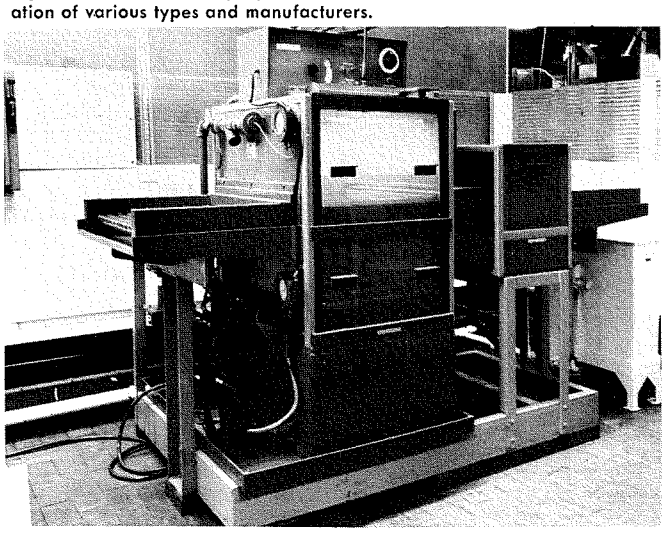
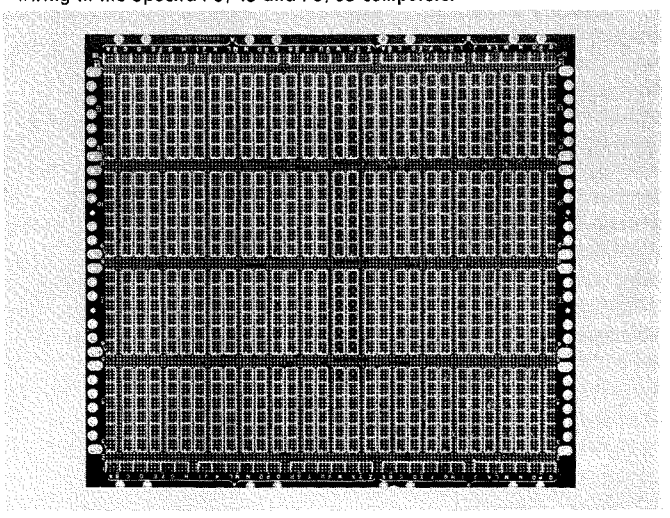


Fig. 10—The large area multilayer platter used to replace backplane wiring in the Spectra 70/45 and 70/55 computers.



ADVANCED COMPUTER TECHNOLOGY IN RCA

A Review

This paper reviews the history and present trends in advanced-development work on computers at RCA. Emphasis is given the Vanguard program, which was conducted by RCA to explore the trends that advanced computers would follow. Also discussed are significant future trends for computer circuits, memories, and packaging. This review illustrates the role that the Computer Advanced Product Research activity in Camden plays in RCA computer research and development. That role includes high-speed digital theory, logic design, circuit development, memory development, and advanced fabrication. The work regularly ranges from theoretical analysis through practical, economical equipment solutions that are tested in feasibility models.

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TEN years ago RCA's first digital data processing system was delivered to the U.S. Army Ordnance Tank and Automotive Center (OTAC) in Detroit, Michigan. This BIZMAC system was the largest data processing installation ever constructed up to that time, and constituted a major effort for RCA, taking more than three years to develop and design. Even with its 32,000 tubes and 600,000 other circuit components, the system finally achieved a "good operating time" of over 96%. In spite of its very good performance, this system was replaced after 6 years by a more compact system, also manufactured by RCA, lower in initial cost as well as in maintenance and service costs. As this paper will describe, the rapid advancements in computer technology have produced new generations of electronic data processing equipment every 5 to 8 years since—a pace that is still continuing.

EARLY DEVELOPMENTS

Actually, advanced computer activities in RCA date back to 1939, when work at RCA Laboratories was undertaken to fill the demand for the more rapid and accurate antiaircraft gun control devices necessitated by faster aircraft. Most of this work, however, was based on analog methods, devices, which yielded a practical solution to a pressing problem. It was recognized then that electronic digital devices might be capable of providing the same functions more precisely, but the large number of vacuum tubes required to carry out the task made the digital approach unappealing.

Shortly after World War II, John von Neumann of the Institute of Advanced Study at Princeton University proposed the construction of a universal digital computing machine, based on the use of a stored program. Many of the basic concepts then expressed by von Neumann are still valid and are used in today's digital electronic computers.

The importance of von Neumann's concept—namely, the storage of data and instructions in a memory from which they can be extracted upon demand by the computer—was recognized by the RCA Laboratories. A research program was initiated to develop a device to provide the storage. One of the first devices conceived was the Selectron, a vacuum storage tube with 256 individual randomly addressable storage locations. The actual storage was achieved by secondary emission at 256 separate locations in the Selectron.

Later work at RCA Laboratories led to the search for more reliable, less delicate and lower cost memory devices. Research programs carried out by the RCA Laboratories on magnetic memories and circuits have added materially to the advancement of this art. Most notable among these was the development of the magnetic ferrite core, which for the past ten years has been, and still is, the basic storage element for most of the digital memory systems in the industry. Other RCA research groups have made significant contributions to the formulation and understanding of computer theory and system concepts.

In 1951, digital data processing activity gathered momentum in the RCA organization and a Data Processing Engineering section was formed at Camden. Some of their most notable early accomplishments were:

1) The first variable word length data processing system; also the first commercial system to use magnetic cores.
2) RCA 501, the first commercially available, fully transistorized computer.
3) First high speed punched-card reader (400 cards per minute).
4) First on-line sales recorder.
5) The Ultratype Camera and Electrofax Printer, the first electronic high speed printing system.

In 1959, the need for a separate advanced EDP activity was recognized. A group of engineers was assigned to explore some of the more advanced techniques, analyze new approaches, and construct feasibility models, with the goal of providing a sound basis for product design of future equipment. This engineering team is now a part of the Applied Research activity in Camden.

THE ROLE OF ADVANCED DEVELOPMENT

A few words are in order to explain the unique and sometimes difficult position which is held by an advanced development group serving product design groups. The advanced development group must form a bridge between research and product design. The techniques developed by the research activity must be tempered with the ingredients that will transform a new technological concept into a practical device, thus meeting the necessary requirements of a competitive industry. The group must be open-minded toward new techniques, but it must also be aware of the problems faced by the product design groups; and it must understand their down-to-earth concern about manufacturing cost, tooling required, reliability, maintenance, etc.

At the start of a project, Applied Research usually faces the problem of selecting one of a number of possible approaches to accomplishing a specific technical objective. Limitations in manpower and budget usually prevent the pursuit of more than one path. The selected path must lead to a signficant improvement over the previously used technique. The chosen approach must also permit fabrication at low cost, to be competitive. The resultant device must be reliable, maintenance and service must be reasonable, and most important of all, it must be ready when the product design groups need it. If any of these goals cannot be met at the end of the project, time and money have been wasted. In addition, it is important that an advanced development group properly evaluate the progress made by competition while the device is being perfected. A device which meets all original engineering and cost aspects,

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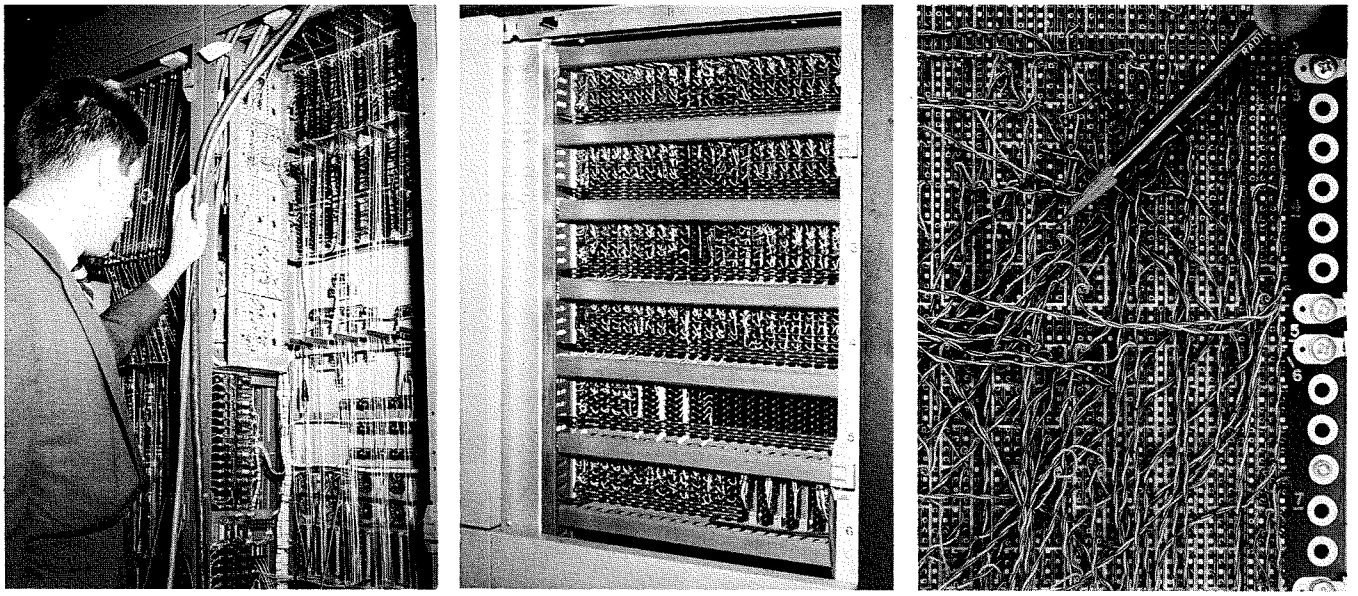

Fig. 1—RCA computer wiring improvements: (left) Bizmac wiring; (center) RCA 501 wiring; (right) Spectra 70/45 printed microstrip lines (pencil point); also shown are twisted pair lines.

but cannot compete with the new competitive device is a failure.

Over the past few years, Applied Research personnel have worked intensively on all phases of research and development of high speed digital techniques, including logic design, circuit development, memory development, and advanced fabrication techniques. This work has encompassed theoretical analysis and evaluation of practical, economical solutions which have been tested in feasibility models. Some of these projects will be described below.

PROJECT VANGUARD—A DEPTH STUDY OF ADVANCED COMPUTER TECHNIQUES

During the early computer days, all electronics for the system were housed in racks similar to those used long before by the communication industry Pulse rise times were a fraction of a microsecond and clock frequency was in the low megacycle range. The impedance of the vacuum tube circuits was many thousands of ohms. Signal propagation delay due to the length of interconnecting wires was no problem at this time. To reduce the capacity of the signal lines and the cross-talk between conductors, the wires were carefully spaced by mounting them on miniature "telephone" poles (Fig. 1a). Transistor circuits used in the RCA 301 and 501 had lower impedances and tests indicated that signal wires could be bundled together without undesirable effects of reflections or cross-talk (Fig. 1b). Unfortunately, increasing the speed of later systems and decreasing the size of the circuit modules again made the problem of interconnection more difficult.

The RCA 601, the Communication Data Processor, and the RCA 3301 had to use transmission lines in the form of twisted pairs and coaxial cables to overcome these undesired effects. Also, the delays through the signal conductors and the reflections of unterminated lines began to present a problem. It was realized that with still higher speed, the signal interconnection paths would become a major problem that should be studied. The problem of interconnections also became important to memory systems. During the design of the RCA 601 memory, it was apparent that the ringing in the memory stack structure following the application of a drive pulse was a major source of noise, which reduced operating margins and limited the speed of operation. To study in depth these problems of future computer systems, Project VANGUARD was initiated.

At the start of the VANGUARD program, reasonable objectives for the system had to be established. It was anticipated that the advanced development phase, and the following product design and manufacturing cycle would take approximately 5 years. Therefore, the performance goals for the memory and circuit speeds had to be set high enough to meet requirements 5 years in the future. The questions which had to be answered were:

What should be the delay per logic level?
What should be the memory cycle time?
What should be the cycle time of a scratch-pad memory?

Starting with the memory system, theoretical analyses and experiments conducted at Princeton and Camden showed that small ferrite elements with apertures in the range of 5 to 10 mils might permit the construction of a memory with a cycle time of the order of a few hundred nanoseconds. The shortest cycle time of existing computer memory systems was then in the range between 2 and 3 μs. Thus, the goal for the basic VANGUARD memory block was established at 1,024 words, 100 bits, operating at a cycle time of 350 ns—a speed increase of approximately eight over existing equipment.

Experiments performed by other organizations indicated that a small array thin-film memory could be operated at

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cycle times below 500 ns. Therefore, it was also desirable to investigate this device. On a rather arbitrary basis, a goal was set for a scratch-pad memory of 64 words, 20 bits, operating at a cycle time of 150 ns.

Another decision that had to be made was the proper ratio of circuit speed to memory speed. The historical approach was to specify speeds based on prevailing technological trends, trying to adhere to a ratio of between 30:1 and 50:1. This approach is only meaningful when the new system is to be *n* times faster or slower than an existing system. When the resultant system concept enters the design phase, tradeoffs occur due to economic considerations, reliability, reproducibility and physical arrangement. The result is a relaxation of certain goals despite the ability to meet them adequately at a certain price.

What, then, is a better approach to determining this ratio? The method used for establishing the goals for VANGUARD circuits was based on the fact that a minimum of ten logical decisions (pair delays) is required to do a meaningful job, such as causing a change in machine state. Thus, it had to be possible for a signal to propagate through ten decision levels during the fastest memory cycle. Since 150 ns was set as the goal for the thin-film-memory scratch-pad, the pair delay had to be a maximum of 15 ns. This in turn meant that the decision rate per logic level had to be no more than 7.5 ns. In addition, the components of that rate not only included the inherent circuit delay, but the additional delay caused by loading at the input-output circuit terminals, the delays due to transmission line propagation, the additive effect of loading on the transmission line, and allowance for such factors as skew. After allowing 2.5 ns for these additional delays, the goal for inherent delay was set at 5 ns or less per logic level.

During the first year of the VANGUARD project, some basic decisions were made related to techniques for circuit design, packaging and memory design. A test device named pre-VANGUARD was constructed. This vehicle partially fulfilled the purpose of proving the initial capabilities of the circuits, their components and the selected packaging techniques. The pre-VANGUARD consisted of two sections:

1) An exerciser composed of 570 transistors and 1,870 diodes packaged in 722 pluggable modules. The propagation time of the two-level logic elements was 5 to 7 ns.
2) A memory system based on two-core-per-bit operation consisting of 16 words of 12 bits, and operating at a 200-ns cycle time. The ferrite elements were 0.08 x 0.08 x 0.01 inch thick. The aperture was 5 mils in diameter.

Conclusions reached at this point indicated that a two-level logic circuit was useful for the implementation of a reasonably wide variety of complex logical structures to be found in a typical computer. Adding, in this case, the passive diode *and* function to a single-level *or* element provided cost, volume and signal delay advantages. It also appeared that the occasional need to devote an entire module to invert a signal was not too frequent. A further decrease in the number of inverters could have been facilitated if a radial fanout of greater than three could have been achieved.

Major attention was focused on interconnection and packaging techniques. Open wire proved completely inadequate to handle pulses with 1.5-ns to 2-ns rise times and coaxial cables, even of the microminiature type, proved bulky and too costly for future product design. Solutions to these problems led to the development of printed microstrip lines. In addition, a unique power distribution system was tested, as was the usefulness of printed microstrips for backboard wiring. Parallel effort also resulted in improved techniques in circuits and packaging (Fig. 2). We were aware, however, that a simple bread board could not simulate the logical complexity of a large-scale design and solve such probems as the noise and crosstalk that might result.

What followed was a five-fold effort that encompassed all areas. The first effort was the development of a micromagnetic memory system. A test unit organized as 1,024 words of 100 bits was constructed along with the associated electronics. The memory stack was fabricated by RCA Memory Products at Needham. The achieved cycle time was 400 ns. Two cores, each 0.03 inch OD and 0.01 inch ID, were used for each bit. The system was a word-addressed organization with diode decoding and transformer drive. The results of this effort included the following:

1) The fastest memory of this size developed to that date.
2) A practical ferrite core memory system with an order of magnitude increase in speed over existing systems.
3) A deeper understanding of the behavior of memories operating at high speeds.
4) Application as a scratch-pad memory in RCA 3301 and later in the Spectra series.
5) Development of plated wiring through the cores.
6) The use of small apertured cores, making low drive currents practical and permitting high packaging density.

The second achievement was a micromagnetic memory exerciser unit (Fig. 3) consisting of approximately 1,560 gates. This unit was designed to test the memory in every sequence and pattern that would "stress" its operation. The basic gate chosen was the DAFO circuit (diode *and*, emitter-follower *or;* Fig. 4). Although this circuit's speed was only equal to the pre-VANGUARD circuit, it was superior to the former circuit because of improved fan-in and fan-out capabilities, improved transmission line operation and reduced power dissipation.

The third achievement was a thin-film memory of 64 words (20 bits each) constructed with a cycle time of 125 ns. The accomplishments of significance here were not only one of the fastest thin-film memories of this size ever built, but also the development of high-speed sense amplifiers capable of reading small signals in the presence of noise, and the development of a drive matrix that could change the word address at an 8-Mc/s rate.

The fourth accomplishment was an exerciser for the thin-film memory system, and the fifth was a test vehicle, HISCAT, for exercising a tunnel diode-transistor hybrid circuit to demonstrate high-speed carry propagation. Of additional interest here was the fact that in the design of the HISCAT control, the functions were visualized in terms of an *automaton*, or sequential state machine. The results implied not only some savings in hardware, but more important, a simple control scheme based on asynchronous methods. Further studies are presently in progress for the implementation of control for large scale processors. Logic in all five of the subsystems utilized the DAFO gate, and demonstrated the feasibility of the interrelated circuits, memory and packaging techniques. Among the achievements collectively resulting from their performance were the following:

1) Reliable operation at fairly high noise levels.
2) Reduced amplitude of spurious signals.
3) Development of rules for interconnecting switching circuits with transmission lines and minimization of the effects of reflection.
4) A 5:1 power dissipation reduction over the pre-VANGUARD circuit.
5) Circuit packaging reduction over pre-VANGUARD.
6) Techniques for using the emitter-follower advantageously in high speed circuits, with protection against unwanted oscillations.
7) Carry propagation of less than 0.5 ns per stage.
8) Successful marriage of tunnel diodes and transistors in a transistor environment.
9) Construction of multilayer printed circuit boards and precise microstrip transmission lines.
10) Proven feasibility of partially integrated construction of circuits.
11) Extensive use of deposited passive components of narrow tolerance on a ceramic substrate for high speed digital circuits and memories.

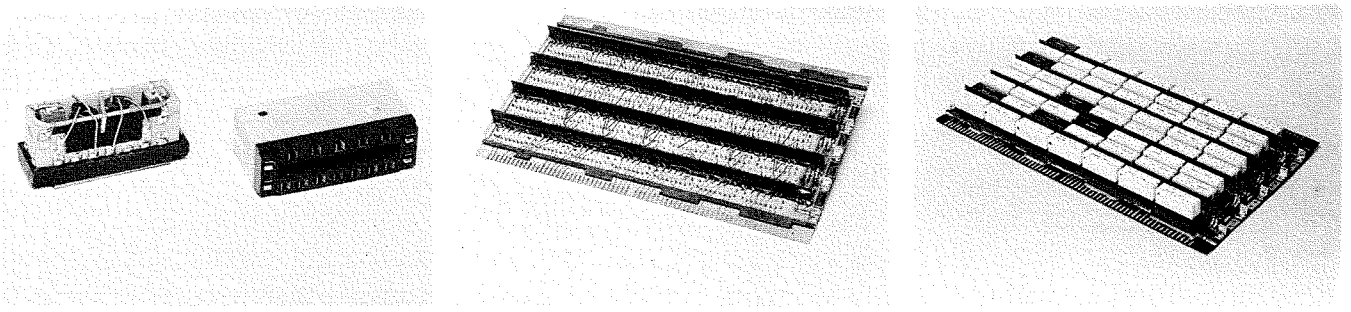


Fig. 2—Vanguard packaging: (left) circuit module, (center) mother board with microstrip lines and power distribution, and (right) mother board with circuit modules in place.

ADVANCED PACKAGING TECHNIQUES

The need for greater speed in digital equipment has led to development of logic devices and storage elements operating in the low-nanosecond region. High speed switching devices and microminiaturized components provide the basic ingredients for this operation. However, these two factors alone will not yield the expected equipment performance. Additional factors, of minor importance in the past, become crucial in the design of ultrahigh speed equipment. Some of these factors are signal propagation delay, placement of modules, wiring density, crosstalk, reflection and other transmission line characteristics. The solution of these problems requires the unified efforts and close cooperation of logic, circuit, memory and packaging engineers.

The need for solutions to the above problems was emphasized when the design of Spectra 70 began. A major part of the Applied Research 1964 efforts was devoted to the study of interconnection and packaging problems associated with switching circuits operating in the low-nanosecond range. The work encompassed theoretical analyses, laboratory tests, and practical considerations of the fabrication aspects of microstrip lines and multilayer boards.

The final phase of this project was the issuance of an *Engineering Guide*[7], which provides detailed guidance to digital equipment designers in the area of:

1) Printed circuit interconnections
2) Transmission line reflections
3) Crosstalk between microstrip transmission lines

The techniques contained in the *Guide* are applied to the design and fabrication of the Spectra 70 series.

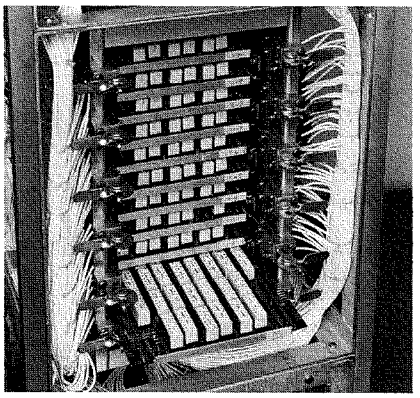
MONOLITHIC FERRITES FOR MEMORIES

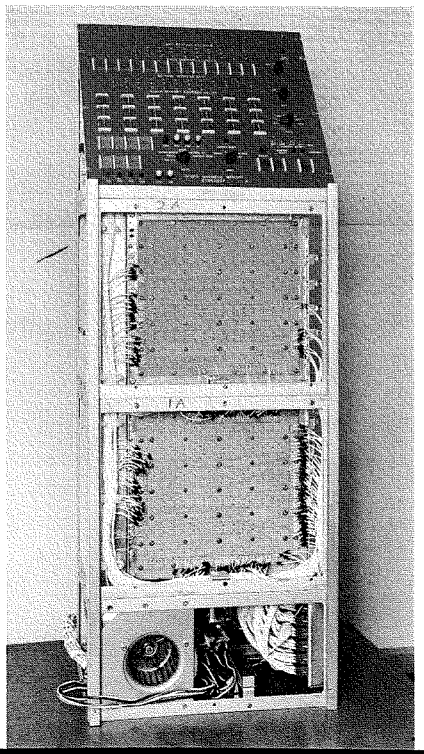
As the type and range of computer applications are increased, greater demands are being placed on the memory, resulting in greater storage requirements. This results in a proportional increase in the cost of the memory.

In the past, the ferrite core has been the major storage device for implementing random access computer memories. Its ability to remain the leading device has arisen from the fact that industry has been able to make improvements in speed, along with cost reductions. Greater packing densities also have been achieved. The major barrier to a continued cost reduction trend with core memories is their inability to lend themselves to fully automated stack assembly techniques, as well as limitations in packing density.

The result of early research at the RCA Laboratories at Princeton and the efforts of the Memory Products fabrication activity at Needham, Massachusetts, have led Applied Research to the development of a memory system having as a basic element a laminated ferrite material capable of batch fabrication. This team has succeeded in producing a thin wafer of magnetic material with embedded conductors by using a doctor-blading technique.

Fig. 3—Micromagnetic memory exerciser. The printed 75-ohm microstrip lines are visible in the front view (bottom photo). The closeup (top photo) shows circuit boards with modules.





This laminated material has properties very similar to those of ferrite cores, except that the packing density is an order of magnitude greater. The basic elements can be easily produced and fabrication techniques provide good uniformity from batch to batch. The drive requirements and sense outputs for these arrays, as well as their ease of fabrication, place them in a favorable cost position with respect to other types of memories.

The basic doctor-blading technique for fabricating ferrite sheets consists of the following steps:

1) Ferrite slurry preparation.
2) Doctor-blading of ferrite sheets.
3) Conductor fabrication.
4) Laminating and sintering of memory arrays.

The monolithic ferrite plates have been made in a number of different sizes. The smallest samples tested were 8 x 8 and the largest were 256 x 64. After experimenting with many different size arrays, an array of 64 x 64 was selected as the most reasonable size, considering the present state of doctor-blading technology and interconnecting problems.

From tests made with individual plates and small assemblies of such plates, enough knowledge has been accumulated to permit reasonable projections of the characteristics of memory systems built from these plates. The monolithic ferrite characteristics of interest are as follows:

Drive Requirements:

Read current	300 to 400 mA
Write current	120 to 150 mA
Digit current	25 to 45 mA

Per-Intersection Characteristics:

Delay	0.03 ns
Back voltage (400-mA *read* and 40-ns rise time)	0.141 mV
Resistance	0.04 ohm
Attenuation (10-ns pulse)	0007 dB
Typical output	20 mV

Although these characteristics are indispensable as a guide to estimating the capability of the laminated ferrite as a *storage element*, they do not give much

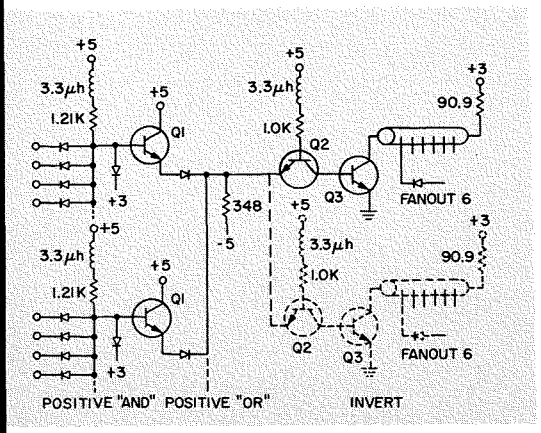


Fig. 4—DAFO circuit.

information about the characteristics of a *memory system*. In particular, there is nothing in that tabulation to indicate how system noises will degrade the performance of a computer system.

A prototype memory of 1,024 words by 64 bits was designed and built using the characteristics just given. At the time of writing this paper, tests on this stack are still in progress. These tests will answer in a definite way the questions of maximum bit capacity per basic memory block, cycle time and overall system performance. Calculations and tests to date indicate that for a basic memory block of 2,048 words (128 bits each), a cycle time of 500 ns can be achieved.

This configuration could also be operated as an 8,192-word, 32-bit system with only a minor increase in cycle time. The increase in cycle time is due to the necessity to gate out the proper 32-bit group of the selected 128-bit word.

A monolithic ferrite scratch pad of 128 words, 32 bits also was constructed and operated at a cycle time of 120 ns.

OTHER ACTIVITIES

In addition to the projects described and the follow-on studies, this story of Applied Research's effort in the data processing field could not be complete without mentioning some of the other developments and studies. Many of these are conducted jointly with other groups in RCA, including RCA Laboratories at Princeton, Defense Microelectronics, and the Electronic Components and Devices division at Somerville, N.J., and Needham, Mass.

There is continued research in the area of high speed circuits utilizing monolithic integrated circuits as well as tunnel diodes, transistors, and their hybrids. Other developments encompass low power and wide temperature circuits for military applications. In addition, the application of large array monolithic integrated circuits and batch fabrication technology is pursuit. Interconnection and intraconnection techniques are being developed to achieve higher packing density and higher operating speed for commercial as well as for military applications.

The efforts in storage systems also include thin films, plated wires, cryogenic devices, and grooved ferrite plates. Besides the regular *read-write* modes, nondestructive-readout and read-only memory techniques are being developed.

The logic design efforts include analysis and minimization of operations, data processing structures, and control systems. In the area of automated design, a study is being conducted to determine optimum circuit modular allocation and thus arrive at simplified wiring and effective grouping. There is also a continuing effort to develop general-purpose computer programs useful to circuit designers. This includes a matrix solver, programs for solving sets of linear equations, map programs which generate the steady-state or transient response of a circuit described in terms of the circuit configuration, and a graph-plotting program.

Software activity includes projects for increasing programming productivity, and the design of a general purpose compiler-assembler. The goal of the first study is a system for decreasing the debug-correction-rerun cycle. The second effort will provide a single program that will translate from any of a number of compiler languages into the machine language of a given computer. To achieve major increases in processing speed, new machine organizations, and interlaced hardware and software are being analyzed.

TRENDS

Circuits

In 1960, the history of electronic computers was too short, especially as far as transistor circuits and random access ferrite core memories were concerned, to permit an accurate prediction of future trends. Today, only 5 years later, we are in a much better position to forecast the future.

Table I summarizes the evolution of characteristics occuring in the major RCA data processing systems announced during the past 10 years. The decrease in logic circuit delay and memory cycle time, as well as the increase in memory size is clearly visible.

Logic pair delays and timing slot widths of all RCA machines are plotted against time of announcement in Figs. 5 and 6. In the circuit area, there appears to be a ten-fold speed increase every 5 years. The BIZMAC computer is ahead and far outside of this trend line because the circuits used were based on long established vacuum tube technology from which we departed in order to achieve greater economy. Thus, speed was traded for equipment size and cost. It took three years to recover this loss in speed.

The VANGUARD circuit leads the trend line by approximately 4 years. However, the VANGUARD circuit, per se, will not be introduced in the future product lines due to the advent of monolithic technology, which had not matured at the time of the VANGUARD project. Nevertheless, the knowledge gained by operating with these high-speed units is of great value to the development of new circuit, memory and packaging concepts.

Recent advancements made in the solid-state industry clearly point out that major speed improvements can be expected in the future with monolithic circuits by such techniques as smaller elements, isolation techniques, beam lead structure, etc. It is predicted that logic pair delays of 5 ns can be expected in equipment by 1968 with 1 ns being reached by 1972. Because the conductor length between logic circuits is becoming a major delay factor, high-speed operation will be greatly aided by the use of will require large array monolithic circuits produced by batch fabrication techniques. Large monolithic arrays with short interconnecting conductors as an integrated part of the assembly appears to be the correct direction in which to proceed. If these circuit trends continue, a 0.1-ns logic pair delay might be achieved in the late 1970's.

TABLE I—Ten-Year Evolution in RCA Computers

Computer	Date Announced	Circuit Speed (Pair Delay), ns	Clock Pulse Width, μs	Memory		
				Speed, μs	Size Range, 10^3 words	Bits per word
BIZMAC	Nov. 1955	250	1	20	4-8	7
501	Feb. 1958	1,000	2	15	16-262	7
301	Feb. 1960	230	0.65	7	10-40	7
CDP	Feb. 1960	120	0.250	1.5	8-32	56
601	Feb. 1960	90	0.250	1.5	8-32	56
3301	Feb. 1963	50	0.214	1.5	40-160	7
Spectra 70/15	Dec. 1964	60	0.300	2.0	4-8	8
Spectra 70/25	Dec. 1964	60	0.080	1.5	16-65	8
Spectra 70/45	Dec. 1964	24	0.060	1.44	16-262	8
Spectra 70/55	Dec. 1964	24	0.060	0.84	65-524	8
As a point of reference, the VANGUARD *feasibility model was:*						
VANGUARD	July 1964	7	0.025	0.40	1	100

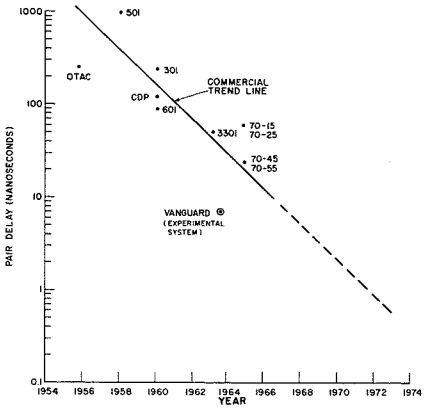


Fig. 5—Logic pair delay decrease in RCA computers.

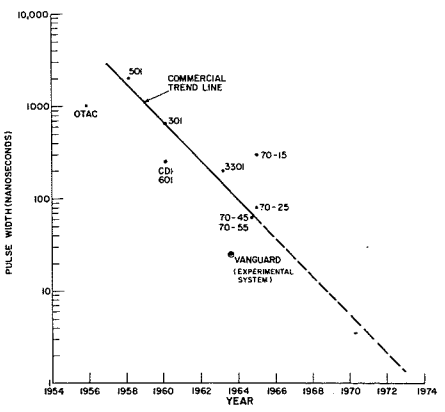


Fig. 6—Pulse width improvements in RCA computers.

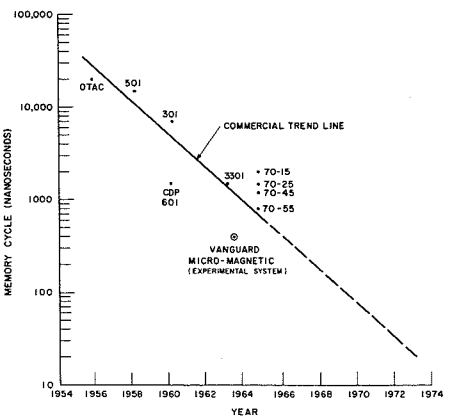


Fig. 7—Memory cycle time decrease in RCA computers.

Memories

Fig. 7 shows that reduction in memory cycle time over the past 10 years have occurred at approximately the same rate as speed increases in logic circuits. No technological change has taken place between the first RCA system and subsequent systems—ferrite cores were used in all systems. Therefore, it is no surprise to find the BIZMAC memory system close to the trend line. Note that both the RCA 601 and the VANGUARD memory systems were ahead and clearly lead the trend line by several years. It is expected that future memory development will continue to follow the slope of this trend line. Tied in with the increase in speed and size is a required reduction in the cost of the memory systems.

In a small digital computing system, the memory represents only approximately 25% of the cost of the processor. However, in larger and faster systems, the cost of the computer memory ranges from 50% to 75% of the total processor cost. Since the trend is continuing toward larger storage capacities, only those techniques will succeed that provide increased speed at a reduced cost per bit. New and ingenious approaches to stack fabrication and memory operation will provide higher operating speed and lower costs per memory bit. The 2.5-D memory system (a technique originally developed for mass storage memories) and laminated ferrite memories are two of the avenues now apparent. Integrated driver and sense amplifiers will drastically reduce the cost of the electronic section of the memory. Thus, to continue along the trend line, future memory systems will have to employ storage elements with faster switching capabilities. Thin magnetic films and plated wires are two of the prime candidates.

Scratch-pad memories have been utilized by RCA beginning with the RCA 3301. Scratch-pads permit an increase in computer performance and help to more fully utilize the logic circuit capabilities. With increased system sophistication, their use will continue, with an increase in storage capacity. Indications are that ultra-high-speed scratch-pad memories will be constructed in the years to come, from large array monolithic flip-flops operating at cycle times in the low-nanosecond range.

Packaging

Batch fabrication of both the circuit and memory systems is the key to future reductions in size and cost of computers, as well as to increased operating speeds. A start has been made, but new technologies are expected to appear within the next few years.

Before these new techniques become reality, however, monolithic integrated circuit are likely to go through a revolution in complexity, greater than that indicated by their development from transistors. Integrated circuits of 50 components are here and are being incorporated in present designs. Monolithic integrated circuits with 1,000 components are being evaluated in laboratories. However, the task of inter-connecting 150 gates on a single slice of silicon is far more difficult than any inter-connection problem faced in the past. Nevertheless, the fabrication of complete systems on one silicon slice appears feasible and eventually will become a reality.

CONCLUSION

The trend of computer technology is such that the boundary lines between logic, electronic hardware, and packaging are rapidly disappearing. The classic "discrete component" has given way to the integrated circuit, which in turn has led to large monolithic arrays with interconnecting conductors. Batch fabrication is now evolving in all areas of computer hardware. This necessitates a merging of *device*, *circuit* and *logic* concepts. In addition, design automation is playing an increasingly larger role as a tool for research, engineering and manufacturing. To reduce the time between concept and delivery logic, circuit and memory engineers, packaging experts and fabrication groups will have to unite in their common tasks. Together and aided by existing electronic computers, they will be able to develop and design the computers of the future.

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REFLECTIONS IN HIGH-SPEED DIGITAL CIRCUITS

Some aspects of transmission line reflection theory as they apply to digital computer design criteria and compromises are discussed. A method is suggested for determining whether a given interconnection between two points may be treated as a transmission line with distributed parameters or, in the more conventional manner, as a lumped element. The relationships between reflection amplitude, characteristic impedance, number of loads, spacing of loads and signal transition times are presented.

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ONE consequence of the trend toward higher operating speeds in digital computers has been the increased attention given to reflections on transmission lines. To faithfully distribute signals with faster transition times, the transmission system must have controlled impedances which are terminated to minimize waveform degradation and reflections. This presents a difficult problem because transmission lines are generally loaded with circuits whose input characteristics are capacitive and frequently nonlinear. Thus, a perfect termination for this kind of a transmission line is impossible. The alternative is to design the signal distribution system so that the maximum generated reflection pulse does not exceed the noise immunity level of the associated circuitry. It is important that the system designer have the ability to make good estimates of the magnitude of the reflections so that he can ascertain that the combined effects of reflection and other noise producing sources do not exceed the overall system noise specifications.

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RELEVANT TRANSMISSION LINE THEORY

When a pulse propagates along a transmission line that is not terminated in its characteristic impedance, a pulse of amplitude no greater than the original will be reflected toward the point of original incidence. Of special interest in high-speed digital processors is the question of when is it necessary to treat the interconnection path as a transmission line and when it may be treated simply as a lumped element. Although the exact criterion is a function of various parameters, a useful criterion can be evolved using the following development: In Fig. 1a, T_d is the time required for the signal to propagate the length of line. If T_1, the rise time of the input signal V_{in}, is less than 2 T_d, the waveform at the sending end of the line will be as shown in Fig. 1b. The reflection signal, due to the capacitor termination, will arrive at the sending end after the input signal has completed its transition. Those signal interconnecting lines for which $T_1 < 2\,T_d$ will be defined as *long lines* and will be treated as transmission lines. Notice that since the input signal completes its transition before the reflection pulse appears, the signal can be processed before the reflection pulse appears. In this case, the reflection pulse is treated as noise, and the system must be designed to operate properly in the presence of this noise pulse if the maximum speed capability of the system is to be achieved.

The transfer of the new information at the sending end could be delayed by timing or clocking until the reflection pulse has decayed, but this would mean a delay of $(2\,T_d + 3/2\,Z_0C_t)$ seconds beyond the time normally allotted the rise time T_1. For 1 foot of 100-ohm line having a propagation factor of 0.5 and terminated in 100 ohms in shunt with 20 pF, this would mean an additional delay of approximately 7 ns. This 7 ns corresponds to the delay of typical high-speed logic circuits and, in several cases, is much longer. Therefore, the high-speed advantage of these circuits would be greatly lessened if the reflection problem was attacked by timing or clocking.

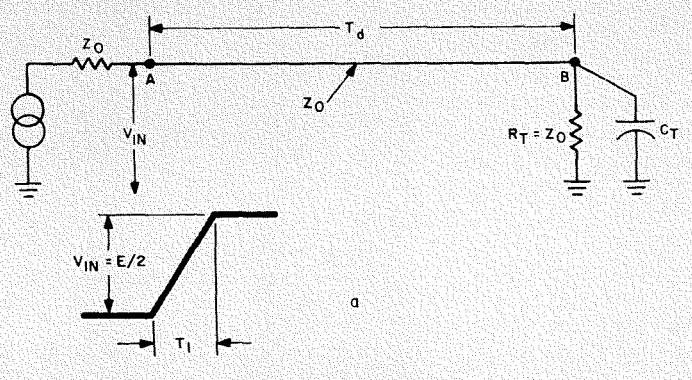
For the case where T_1 is greater than 2 T_d, the rise time of the input signal is degraded by the reflection signal as demonstrated in Fig. 1c. Those signal lines with the property that the initial signal rise time is degraded by the effect of the loaded line are defined as short lines and will be treated as lumped elements (capacitance in this case). Evaluation of this capacitance will be discussed later.

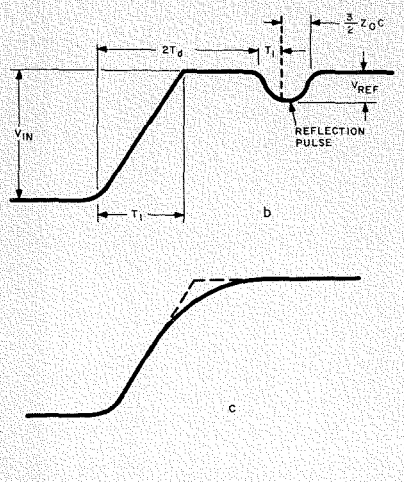
As will be demonstrated shortly, a transmission line loaded with randomly spaced loads can exhibit the properties of both long and short lines. In these cases, the short and long line theories can be applied separately and the results superposed to ascertain the overall effect.

LONG-LINE ANALYSIS

Although there are rigorous methods using computer programs[2] for analyzing the reflections and delays on a transmis-

Fig. 1—(a) Transmission line terminated with capacitor and resistor; (b) Signal at point A for a long line ($T_1 < 2T_d$); (c) Signal at point A for a short line ($T_1 > 2T_d$).





sion line loaded with capacitors, these problems can be analyzed by the novel application of distributed-line theory to a transmission line loaded with lumped capacitance. This technique is an approximation method which yields reasonably accurate results for heavily loaded lines. Heavily loaded lines, for the most part, represent the limiting criteria insofar as reflections are concerned. Requiring only a few minutes of the designer's time, this method provides him with further insight and understanding into the nature of the reflection phenomena.

The technique for estimating reflection is based on the fact that a transmission line uniformly loaded with logic circuits whose loading characteristics are capacitive can be represented by a distributed line with a reduced characteristic impedance. The method of analysis is as follows: Consider Fig. 2, which shows a 74-ohm line connected at both ends to 100-ohm lines. Assume that each 100-ohm line pair has a propagation time T_d and that the 74-ohm line pair has a propagation time T_2. If a pulse with rise time T_1 is applied as shown in Fig. 2, the waveform at A will be as shown in Fig. 3. Thus, using the standard definition for the reflection coefficient[3]:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = -0.15 \qquad (1)$$

Thus, the 74-ohm line will produce a 15% reflection.

Consider next a section of the 100-ohm line alone. Assume that the signal propagation velocity is approximately 0.5 ft/ns. The distributed inductance and capacitance per unit length of line can be derived from the following two expressions:

$$v_p = \frac{1}{(L_0 C_0)^{1/2}} \qquad (2)$$

$$Z_0 = \left(\frac{L_0}{C_0}\right)^{1/2} \qquad (3)$$

where v_p = actual velocity of propagation, L_0 = distributed inductance per unit length, C_0 = distributed capacitance per unit length, and Z_0 = characteristic impedance. Substituting in Eqs. 2 and 3, the distributed parameters for this particular 100-ohm line are $C_0 = 20.3$ pF/ft, and $L_0 = 0.203\mu$H/ft.

Now assume that the 74-ohm line segment B-C of Fig. 2 is replaced by a 100-ohm line segment uniformly loaded with 17 pF/ft of capacitance. The distributed inductance remains the same,

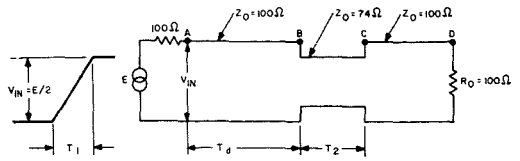


Fig. 2 — Simulated distributed line.

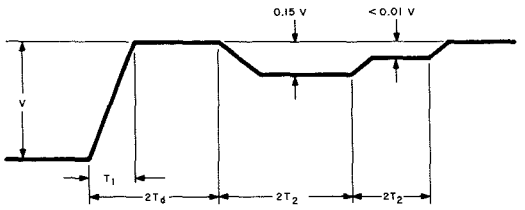


Fig. 3 — Waveform along section A-B of line in Fig. 2.

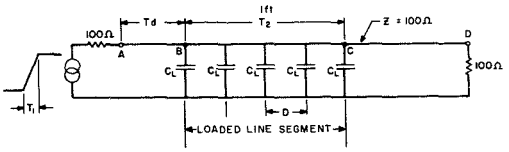


Fig. 4 — Simulated distributed line.

but the distributed capacitance increases to 20.3 + 17.5 = 37.8 pF/ft. Applying Eqs. 2 and 3, the impedance of this segment is reduced to 75 ohms and the propagation time is increased from 2 to 2.72 ns. In addition, the waveform seen at point A of Fig. 2 would be identical for either the 74-ohm line or the uniformly loaded 100-ohm line. In both cases, the reflection would be 15%. The width of the reflection pulse would be twice the electrical length of line segment B-C, or 5.44 ns.

In a physical sense, the input characteristics of transistor input circuits, either integrated or nonintegrated, can be represented by a capacitor. Similarly, the input characteristics of integrated and nonintegrated DTL (digital transistor logic) circuits can be represented by passive circuits comprised of resistors and capacitors. (A method for determining the input characteristic of these various devices is given in Ref. 1.) Thus, if discrete capacitors are used to load the original 100-ohm line segment, as shown in Fig. 4, this segment can be treated as a distributed line whose characteristic impedance is a function of the spacing between capacitors. The closer the capacitor spacing, the lower the characteristic impedance.

The reflection coefficient of the loaded line segment in Fig. 4 can be determined as follows, wherein Z_0 = characteristic impedance of unloaded line, C_0 = capacitance per unit length of unloaded line, L_0 = inductance per unit length of unloaded line, v_0 = velocity of light in free space, $v_p = kv_0$ = velocity of signal in unloaded line, C_L = capacitance per unit load, n = number of unit loads per unit length, D = physical spacing between loads, $C_T = C_0 + nC_L$ = total capacitance of loaded line per unit length, and Γ = ratio of reflected to incident voltage, $E_{ref}/E_{incident}$.

The impedance of line segment B-C is:

$$Z_{L_{BC}} = \left(\frac{L_0}{C_T}\right)^{1/2} \qquad (4)$$

Now, the ratio of the reflected voltage to the incident voltage was defined in Eq. 1, and substituting Eqs. 2, 3, and 4 into Eq. 1:

$$\Gamma = \frac{1 - \left(1 + \frac{nC_L}{C_0}\right)^{1/2}}{1 + \left(1 + \frac{nC_L}{C_0}\right)^{1/2}} \qquad (5)$$

Eq. 5 gives the reflection coefficient in terms of the distributed capacitance of the unloaded line and the added capacitance (per length) as a result of shunt loads. Note in Eq. 5 that the total added capacitance per unit length appears as the product of n and C_L. Thus, the number of loads and the capacitance of the unit load C_L can be inversely altered without changing the magnitude of the reflected voltage. Since, in general, the capacitance of the load is fixed by other considerations, n will determine the reflection for a given C_0, or more generally a given Z_0. Recognizing that n is the inverse of D, the physical spacing between loads, a more useful form of Eq. 5 is:

$$\Gamma = \frac{1 - \left(1 + \frac{C_L}{DC_0}\right)^{1/2}}{1 + \left(1 + \frac{C_L}{DC_0}\right)^{1/2}} \qquad (6)$$

For a given transmission line, Eq. 6 relates the reflection to the load capacitance and the spacing between the loads. For a specified load and a predetermined maximum tolerable reflection, the spacing between equally spaced loads can be determined. It is important to remember that Eq. 6 is most accurate for

a large number of loads while for a smaller number of loads it predicts larger reflections than those observed. However, the system must be able to perform properly in the presence of the maximum reflections; thus it is in this area that accuracy is required.

Some indication of the functional relationship between reflection and the spacing can be seen in Fig. 5, a plot of Γ versus D for $C_o = C_L$. Here, D and the distributed parameters are expressed in the same units.

As an illustration of how Eq. 6 is used, assume that a 100-ohm line with velocity propagation factor = 0.5 and $C_o = 20.3$ pF is loaded with circuits whose input characteristics can be represented by a 5-pF capacitor. If the reflection coefficient is not to exceed 15%, the closest spacing is:

$$0.15 = \frac{1 - \left(1 + \frac{5}{D20.3}\right)^{1/2}}{1 + \left(1 + \frac{5}{D20.3}\right)^{1/2}}$$

$$D = 3.56 \text{ inches}$$

SHORT LINE

As discussed in Fig. 1, the short line is determined by the condition $T_1 \geq 2\,T_d$. This definition applies to the idealized trapezoidal waveform. In most applications, however, the input waveform will not have a linear rise time but an exponential one. As such, its waveform has a decreasing slope during the transition period. Thus defining the end of the transition is ambiguous because of the exponential tail. In addition, most logic circuits have a noise immunity region at either end of the signal swing with the result that the circuit switches before the transition time is completed. Experimentally, it has been found that if T_1 is taken as the time required for the source voltage to rise to about 85% of its ultimate value, the relation $T_1 > 2\,T_d$ can still be used to define the short line.

For those interconnecting lines to which the short line criterion applies, rise times, delays and waveforms are calculated directly by conventional lumped component techniques. In this case the transmission line is represented by an equivalent lumped capacitance as determined by Eqs. 2 and 3. This equivalent capacitance is added to the actual capacitance present to determine the total capacitance to be used in the conventional analysis.

TABLE I—Calculated and Measured Values of Percent Reflections

Capacitance per Load, pF	Spacing, inches	Measured Γ for n Loads, %						Calculated* Γ, %
		$n=2$	$n=3$	$n=4$	$n=6$	$n=11$	$n=12$	
5	1.5	—	16.0	—	19.0	—	26.0	26.8
	3.0	—	15.0	—	17.5	18.5	—	17.3
	4.5	12.0	—	12.4	13.4	—	—	12.9
	6.0	10.5	—	10.5	10.5	—	—	10.1
10	1.5	—	29.0	—	33.0	—	37.5	38.0
	3.0	—	22.0	—	26.0	26.0	—	26.8
	4.5	16.6	—	18.4	20.3	—	—	20.8
	6.0	17.5	—	17.5	17.5	—	—	17.3
15	1.5	—	38.5	—	41.5	—	43.5	45.0
	3.0	—	27.5	—	32.0	32.0	—	33.2
	4.5	25.8	—	27.0	29.0	—	—	26.8
	6.0	21.5	—	22.5	22.5	—	—	22.6

Note: Rise time = 1 ns.
*T calculated from Eq. 6.

SINGLE LOADS OR WIDELY SPACED LOADS

For those cases where the line is loaded with a single load or with widely spaced loads, the reflection amplitude and the time delay can be calculated by applying Thevenin's theorem. Referring to Fig. 6a, if an input signal $V_{in} = 2\,E$ is connected as shown, a signal of amplitude E volts will propagate along the line section A-B. The term T_d is the time required for the signal to propagate the length of the line. If $SW1$ is open, thus open-circuiting the line, the amplitude of the incident signal will jump to $2E$ volts which can be considered the equivalent Thevenin open circuit voltage.

The Thevenin impedance is obtained by short circuiting the input voltage and determining the impedance looking into terminal B towards the generator. This impedance is the characteristic impedance.

Thus, the Thevenin equivalent may be represented as shown in the dotted block in Fig. 6b. If $R_g = Z_0$ there are no multiple reflections at the generator end of the line, and the equivalent circuits of Fig. 6b will give a complete and accurate description of the reflection along the line as well as of the waveform at the load. If $R_g \neq Z_0$, then multiple reflections will exist, and the equivalent circuits shown in Fig. 6b apply only in the interval equal to $2\,T_d$ seconds.

A new Thevenin voltage is determined for succeeding $2\,T_d$ intervals based on the reflected voltage from the generator end of the line. This reflected voltage is determined by the same method; that is, by applying Thevenin's theorem to the generator end of the line. For short lines ($T_1 >> 2\,T_d$) the equivalent circuits of Fig. 6b still apply provided the capacitance of the line is added to C_L.

Using the above approach, the reflection voltage is given as follows:

For $0 < t < T_1$: (7)

$$V_{ref}(t) = \frac{-EZ_0C_L}{2\,T_1}\left(1 - \exp\left[-2t/Z_0C_L\right]\right)$$

For $T_1 < t < \infty$: (8)

$$V_{ref} = \frac{EZ_0C_L}{2\,T_1}\left(\exp\left[2t/Z_0C\right]\right)\left(1 - \exp\left[2T_1/Z_0C_L\right]\right)$$

The maximum reflection voltage is given by $\overline{V}_{ref} = \Gamma_p E$, where: (9)

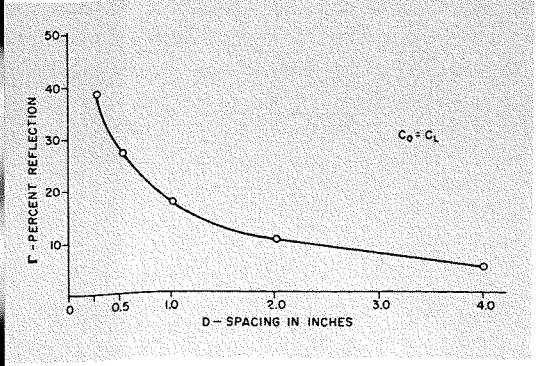
$$\Gamma_p = \frac{-Z_0C_L}{2\,T_1}\left(1 - \exp\left[-2T_1/Z_0C_L\right]\right)$$

It should be noted that when the reflection is due to a lumped capacitance or a nonlinear element or both, *the reflection coefficient must be redefined.* The time delay from A to B as measured at the 50% point is $(T_d + Z_0C_L/2)$.

REFLECTIONS DUE TO SHUNT RESISTIVE COMPONENTS

Because some logic circuits such as DTL gates have nonlinear input characteristics and significant DC input components, it is extremely difficult to define the input impedance in terms suitable for use in the standard reflection formula. Defining R_{in} of the gate as the ratio of the voltage change to the current change is inaccurate since the total current variation usually occurs in some interval of the voltage swing. This assumes that the voltage swing reflects noise immunity properties which is generally the case. However, since the

Fig. 5—Percent reflection vs. spacing for $C_o = C_L$. (a) Transmission line; (b) Thevenin equivalents when $R_g = Z_o$.



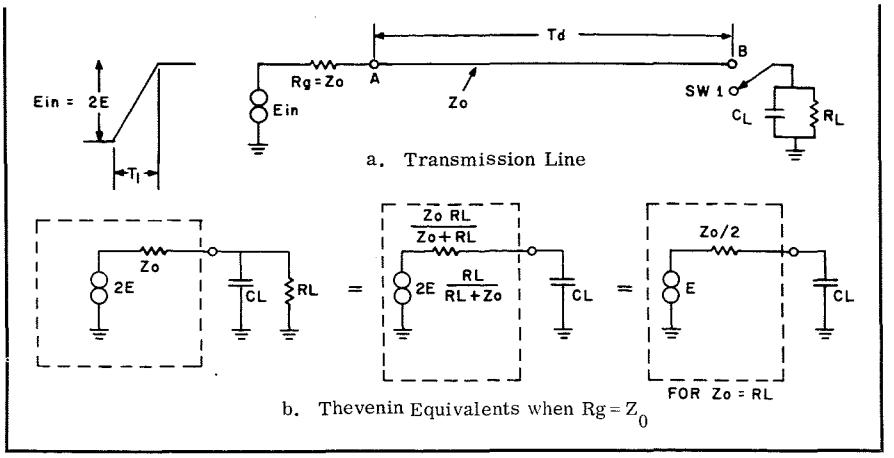


Fig. 6—Thevenin equivalent circuits of transmissions lines.

reflection on a line is proportional to the shunt load current, it is possible to define the reflection coefficient directly in terms of the input current level change which can be easily measured.

Fig. 7 shows a section of transmission line in which an incident current I_{in} is applied. The line is loaded at point P_1 by Z_L through which current I_L flows.

Summing up the currents at node P_1 and using the definition $\Gamma_p = V_{ref}/V_{in}$:

$$\Gamma_p = -\frac{1}{2}\frac{I_L}{I_{in}} \qquad (10)$$

Thus, the reflection coefficient is now expressed in terms of the load current and the incident current, both readily determined parameters for DTL-type loads. Although Eq. 10 was derived for resistive loads, its application can be extended to capacitive loads by replacing I_L by $C(dv_{max}/dt)$.

EXPERIMENTAL RESULTS

Table I shows the comparison between the predicted reflections and the measured reflections for loads of various capacitances and spacings. The table is incomplete simply because all combinations were not measured. As indicated earlier, the accuracy between the calculated and measured reflections for the higher numbered loads is within a few percent. As the number of loads decreases (for the closely spaced loads) the predicted value exceeds the observed value. For slower rise times, the accuracy of Eq. 6 will maintain itself for the higher numbered loads whereas the difference between the predicted and observed reflections will increase with the fewer numbered loads. This follows from the fact that a lumped line more closely approximates a distributed line as the number of sections increases.

CONCLUSION: SOME DESIGN CONSIDERATIONS

In general, the designer will initially endeavor to first specify the characteristics of the transmission line. This happens because the signal transmission system, being an integral part of the packaging, has many physical, mechanical and cost considerations in addition to its electrical properties. Certain types of lines, like coaxial lines, will be eliminated from general use because of their cost and poor package density. Once a line has been chosen consistent with cost and packaging considerations the natural tendency will be to select as high an impedance as is practical in order to reduce the current requirement of the driver circuitry. However, unless the dynamic and static input current requirements of the logic circuitry is exceedingly low, the reflections will be excessive. Excessive reflections in this case means reflection voltages in excess of the predetermined noise immunity of the circuitry.

Even if the designer takes corrective steps by lowering the line impedance or increasing the noise immunity of the circuit (which generally increases the delay) it must still satisfy the requirements of the logic designer whose fan out and fan in requirements directly affect the reflections. Then, still to be considered is the inherent conflict of increased package density versus higher reflections since squeezing a fixed number of loads close together increases the reflection as indicated in Fig. 5. Increased package density usually results in closer spacing between the signal transmission line increasing cross talk between the signal lines. This affects the noise immunity.

Thus, the packing denseness required, the electrical and mechanical properties of the signal transmission system, the noise immunity, the current-speed capability and input impedance of the logic circuitry, the logical fan in and fan out required and the spacing of the loads all affect and are affected by the reflections (and other noise producing sources). Therefore, these various system parameters should be evolved concurrently with the various disciplines cooperating.

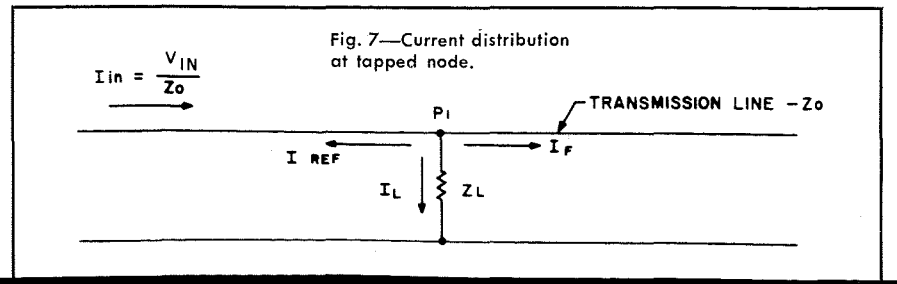


Fig. 7—Current distribution at tapped node.

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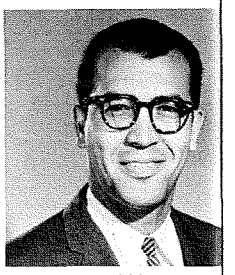
A. Feller



J. J. DiGiacomo

J. J. DiGIACOMO received his BSEE from Villanova University (1958) and his MSEE from the Drexel Institute of Technology (1963). In 1958 he joined the Airborne Communications Section as a design and development engineer on the AN/ARC-62 program. Subsequent assignments included work in system integration engineering and in the field of digital data communication. Mr. DiGiacomo has been associated with the Computer Advanced Product Research group of Applied Research since 1963. His contributions since then have been: 1) a study of the logical implementation and transient analysis of oxide semiconductor circuitry, 2) evaluation and analysis of microelectronic circuitry for the RCA Spectra 70 Computer, and 3) a study of transmission line reflections in nanosecond digital equipment. He is now engaged in a program to militarize the Spectra 70 Circuits. Mr. DiGiacomo is a Member of the IEEE.

A. FELLER joined the RCA Broadcast Television Design Group in 1951; in that year, he received a BSEE from the University of Pennsylvania and an MSEE in 1957. In BCD he worked on low- and high-power amplifiers, active and passive filters, phase equalizers, and color television. In 1959, he joined the EDP Advanced Development Group to work on high-speed digital logic circuits using the tunnel diode transistor combination. Several patents emerged from this project. Mr. Feller also contributed significantly to the high-speed circuits and the high-frequency techniques for the proposed Vanguard Computers. Recently, he made a detailed study of the crosstalk and reflection phenomena on transmission lines, developing simplified analytical expressions for predicting reflections and delays on loaded transmission lines. In addition, he developed techniques for simulating the input of integrated circuits. He has been awarded one patent and has submitted another patent disclosure on high-speed circuitry.

AUTOMATA THEORY

An Aid to Computer Design

The growth of automata theory has been stimulated more by the development of computers than by any other outside agent. This paper surveys its contribution to computer technology, with special attention given to the finite-state sequential machine, which in three examples, is shown as a planning aid in logic design and programming. Moreover, it is suggested that applied automata theory holds promise to surmount difficulties of complexities of logic and function, to enforce consistency during design, and to help diagnose ills in debugging.

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EVIDENCE grows that the computer world considers automata theory less an intellectual madness and more and more a sensible, stimulating, and even productive way of thought. The International Federation for Information Processing (IFIP), in its Congress in May 1965, titled a general session *Automata Theory and Simulation of Thought Processes*, and a special session *Automata Theory and Switching Theory*. In one of the general session papers, V. M. Glushkov, of the Ukrainian Academy of Sciences in Kiev, attested to the fact that interest in the field is more than academic:

> "The recent success of automata theory . . . makes it possible to regard it as a foundation for the development of formal design methods of electronic digital computers, resulting in some cases in considerable economy of equipment and in a substantial reduction in time and cost of designing."

Final manuscript received July 14, 1965.

Perhaps the most important single agent in bringing forth automata theory has been the development and programming of the great artificial automaton—the modern computing machine. Though automata theory does not concern itself primarily with computing machines, it stands to profit from the experimentation that high-speed machines make possible. It seems only fair to investigate how automata theory can repay its debt to these machines.

THE ROOTS OF AUTOMATA THEORY

Automata theory as an academic field has emerged from the hedgerows of mathematics, biology, psychology, philosophy and human ingenuity over the past 30 years. It is still so young and vigorous that anyone who lays a clear boundary around it and neatly categorizes the interior is certain to be wrong in the next man's opinion and in the next day's work. The same is true of classifications of automata themselves.

In broad terms, there is a mathematical branch of the theory that looks like modern algebra and mathematical logic. Its theoretical tool is the Turing machine, with which problems of the

SOME BACKGROUND

What is an Automaton?

Contrary to popular opinion, an automaton is not a robot, although a robot may be considered a form of automaton. Automata theorists are universally vague when asked to define the object of their attention because they do not want to be unduly exclusive; therefore, in words which are vague but seek for generality, an automaton is a black box with input "wires" and output "wires." The various input wires may be stimulated, each in a number of ways, to take on a number of distinct input patterns. The set of all such patterns is the input alphabet. The output wires subsequently each respond in a number of ways to produce a number of distinct output patterns, called an output alphabet. It is characteristic of the automaton that its output depends not only upon present inputs, but upon a history of inputs. An automata can be considered as a transformer of information. For the analysis, synthesis or manipulation of automata, techniques of mathematics are required, for they are both precise and abstract.

To achieve discrete automaton behavior, which is the kind of behavior most applicable to digital computers, the automaton is considered to go through a number of distinct internal states. This kind of automaton is called a finite-state sequential machine. Any fixed, physical finite-state sequential machine will have a finite number of inputs, outputs, and internal states. Any such physical automaton must incorporate memory and logic in the computer sense.

There are a number of conventional descriptions for the automaton. In austere terms the automaton consists of the following:

1) Input alphabet: $X = \{x\}$
2) Output alphabet: $Z = \{z\}$
3) Set of internal states: $S = \{s\}$
4) Characterizing output function: $f(x_t, s_t) = z_t$
5) Characterizing next-state function: $g(x_t, s_t) = s_{t+1}$

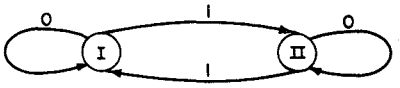
The last two items indicate that the output at a particular time and the next state depend upon the present internal state and the present input.

Automata can be expressed by state-transition diagrams or by transition tables. A state-transition diagram consists of nodes representing the states and directed lines representing transitions. An output is sometimes indicated by a circle within the node. Convenient information, such as conditions of transitions, coding of states, and output response can be put on such graphs.

Although state-transition diagrams provide a quick grasp of allowed transition sequences, they are not immediately as suited to transcription into machine coding as are transition tables (tabulations of transition functions). The state set of the machine can be read from the stub and the input alphabet from the column headings. Entries show the output or next internal state. Since inputs and outputs of physical automata are rarely confined to a single wire, the transition tables are almost always more than two columns wide.

The Simplest Automaton

The simplest automaton, which has one input, one output and one memory cell, is the triggerable flip-flop. It has two internal states: set and reset; an input alphabet of two: trigger and no-trigger; and an output alphabet of two: high and low. Presence of a trigger is represented by a 1 and absence thereof by a 0. The flip-flop automaton is shown below as a state-transition diagram and as a transition table. In this particular instance ouptut is from state I, which may be interpreted as set or reset, depending upon the application. Action of the flip-flop can be traced by following the arrows in the state-transition diagram or by consulting the transition table.



STATE–TRANSITION DIAGRAM

INPUT ALPHABET: $X = \{0, 1\}$
OUTPUT ALPHABET: $Z = \{\text{LOW, HIGH}\}$
STATE SET: $S = \{I, II\}$

PRESENT STATE, S_t / INPUT X_t	NEXT STATE		OUTPUT	
	1	0	0	1
I	II	I	HIGH	LOW
II	I	II	LOW	HIGH

TRANSITION TABLE

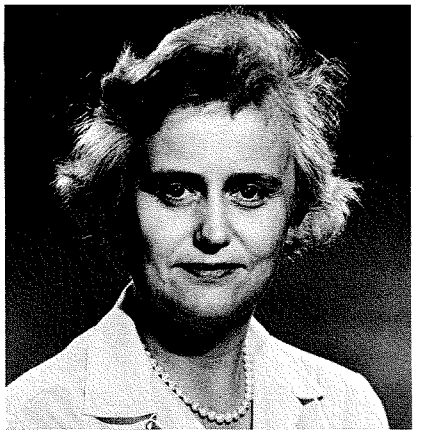
constructibility of algorithms under computer-like restrictions are decided. It deals with what are necessary and sufficient characteristics for automaton activity like self-reproduction and dynamic immortality. The mathematical theorists have enunciated numerous theorems, some of which are elaborately proved.

Another branch devotes itself to simulating human behavior by mechanical and electrical means. The goal here is to have a machine with its speed and memory, as well as its immunity from ordinary fatigue and human distraction, outstrip the human being it imitates in tasks previously considered to be exclusively human. Work on optical and aural recognition, heuristic programming, self-organizing systems, automatic theorem proving, language translation, and game playing are found here.

Finally there is a branch which might be called structural, and which has the most obvious appeal and importance for the computer designer. Structural automata theory deals with the automaton as a specification of black box behavior; moreover it deals with what within the black box is necessary for specified behavior. This internal description takes the form of designating a number of states, the outputs from certain states, and the conditions of transition from state to state. Restricting automata to those having fixed, finite sizes and discrete internal states at distinct points in time, the theory of finite-state sequential machines has become a major subtheory with great promise for analysis and synthesis of digital machines. Work in this area is characterized by transition tables and matrices, by state transition graphs, and by computations which explore the potentialities of the machine under consideration.

FROM THEORY INTO PRACTICE

For several years, practical application of finite-state sequential machine theory has been pursued as applied research. One objective, that of formalizing the procedure for translating verbal specifications into automata, has depended upon observations from analysis and synthesis of a number of different machines in different ways. Such work meets with difficulties when faced with the inexactitudes of English language specifications and with documentation never intended for such complete and demanding scrutiny. Nevertheless, automata—initially from verbal specifications—have resulted in two very different kinds of realizations: *logic design* and *programming*.



ANN S. MERRIAM received her BA in Mathematics from Goucher College, Baltimore, in 1945 and her MA in Physics from Bryn Mawr College in 1959. She has taught mathematics at the school and college level, and, in 1956, held a General Electric Fellowship for Mathematics Teachers. Currently she is a candidate for the MSE from the Moore School of Electrical Engineering of the University of Pennsylvania. Miss Merriam came to RCA as an engineer in 1959. Since then she has worked on threshold logic, systems use of content-addressed memories, logic design of the Vanguard Test Machine, logic design of an exerciser for testing high-speed carry circuits, and automata theory applied to design of control in digital computers. She is a member of IEEE and an associate member of Sigma Xi.

Specifying HiScat Logic Design

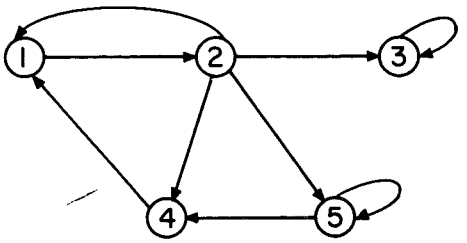
A practical test for the use of automata theory as a basis for logic design came in the building of the High-Speed Carry Tester (HiScat), a 600-gate machine for exercising a 10-bit parallel adder with tunnel-diode carry circuits. HiScat was instructed to *1)* prepare

. . . . . Matrix Calculations . . . . . .

A state-transition diagram can be translated into a skelton transition matrix. In constructing the matrix, if there is a transition from state i to state j, a 1 is placed in row i, column j. This procedure is followed for all transitions in the diagram. All other entries in the matrix are zero. If the skelton matrix is squared by ordinary matrix multiplication, the resulting matrix indicates connectons of states by double transitions, i.e., the states that can be reached in two transitions. In this case, further multiplication leads to M^4 beyond which there is no matrix change in raising it to higher powers. The fact that there is always a limited number of distinct matrices resulting from such multiplications agrees with the observation that in a finite-state machine there is only a certain number of transitions to be made before the entire activity of the machine has been explored.

Tracing the paths of the state diagram below will convince the reader that, with one exception, any state can be reached from any other state in four transitions or less. Use of these matrices to indicate the exact number of required transitions for a path from one state to another is demonstrated by following the entry in row 4, column 2 through the four matrices. The indication is that a path can be established from state 4 to state 2 in two, four, five, or more transitions, but it cannot be established in one or three transitions. This can be verified by tracing through the state diagram. The state diagram shows state 3 to be a dead end; once transition into it is made, there is no transition out. This fact is reflected in row 3 which remains unchanged throughout all multiplications of the matrix.

The elements of a transition matrix need not be confined to showing presence or absence of transition, but can be a logical expression of the conditions of transitions. Multiplication of the matrix by itself forms new elements which are the logical sums of logical products, and each element represents the conditions of moving from one state to another with one more transition than the original matrix, allowed. For five-state automata, manipulations and interpretation of transition matrices represent an elaborate approach, but for analyzing automata of large numbers of states and many transitions, state diagrams become confusing and machine processing of matrices becomes more attractive.



S_i \ S_j	1	2	3	4	5
1	0	1	0	0	0
2	1	0	1	1	1
3	0	0	1	0	0
4	1	0	0	0	0
5	0	0	0	1	1

TRANSITION $S_i \rightarrow S_j$ = M

$$M^2 = \begin{bmatrix} 1&0&1&1&1 \\ 1&1&1&1&1 \\ 0&0&1&0&0 \\ 0&1&0&0&0 \\ 1&0&0&1&1 \end{bmatrix} \quad M^3 = \begin{bmatrix} 1&1&1&1&1 \\ 1&1&1&1&1 \\ 0&0&1&0&0 \\ 1&0&1&1&1 \\ 1&1&0&1&1 \end{bmatrix} \quad M^4 = \begin{bmatrix} 1&1&1&1&1 \\ 1&1&1&1&1 \\ 0&0&1&0&0 \\ 1&1&1&1&1 \\ 1&1&1&1&1 \end{bmatrix}$$

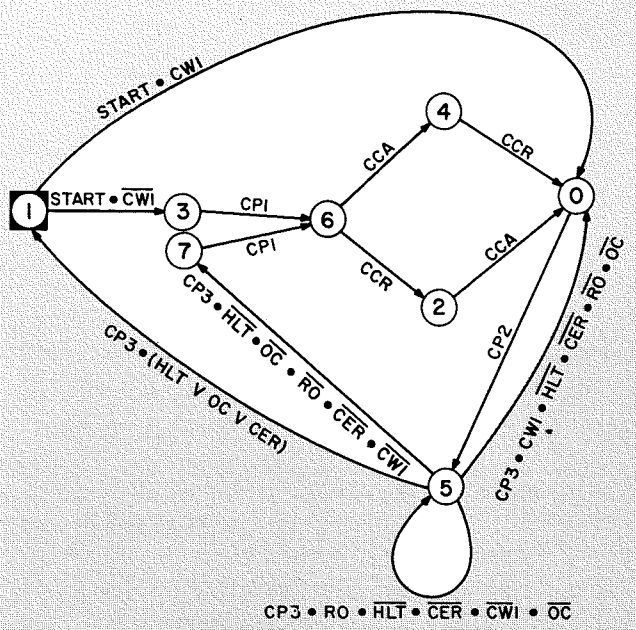


Fig. 1—State transition diagram for HiScat.

CONTROL PANEL COMMANDS

start
stop (HLT)
cycle without increment (CWI)
one cycle (OC)
ripple only (RO)

RETURN SIGNALS

carry complete A reg (CCA)
carry complete R reg (CCR)
comparison error (CER)

COMMAND PULSES AND STATES FROM WHICH GENERATED

CP1-3	CP2-0	CP3-5

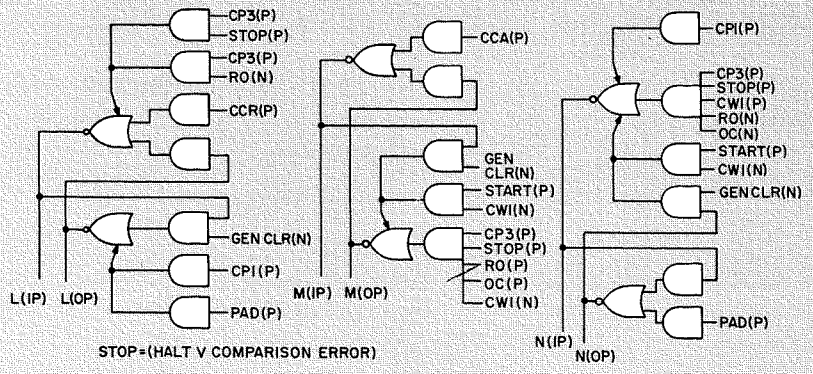


Fig. 2—Control state flip-flops for HiScat.

two operands, *2)* add them by two independent means, *3)* compare them, and *4)* stop only if halted by command of the operator, by one-cycle option or by a discrepancy in the results of the addition; otherwise it was to continue producing new operands and adding them. Variations of this normal cycle were to be at the disposal of the operator. He could either call for HiScat to repeat the same addition with the same operands, or he could have the operands increased, *mod* 2^{10}, to provide different additions, and therefore different lengths of carry ripple through orders of the adder. For specific study of the carry chain, it was provided that the adder be primed and a carry rippled down it at regular intervals. Finally the HiScat was to stop in a reset of control, not of data, so that whatever the cause of the stop, it could be started again by depressing the *start* button on the control panel. With such a verbal specification settled upon, a finite-state sequential machine was constructed. Its inputs corresponded to operator commands and machine return signals, and its outputs corresponded to command pulses. An automaton of seven or eight internal states was adequate to achieve the required behavior. Since each state of the machine corresponded to a configuration of flip-flops, three sufficed; there was not great need for economy here, since the addition of one flip-flop would have provided for double the number of states. Since three command pulses had to be formed, three states produced outputs; the other states were intermediate. Conditions of transition from one state to the next were written logically as the sum of products for later manipulation to fit the particular hardware.

Use of a State Diagram

For a machine the size of HiScat, a state diagram form of the automaton (Fig. 1) proved most useful for both design and debugging. Three flip-flops, L, M, and N, read in this order, correspond to the state numbers in octal at the nodes of the diagram. Thus, for example, transition from state 6 to state 2, upon receipt of the *carry complete in the R-register* return signal (*CCR*), was accomplished by resetting flip-flop L. Immediately, the advantage of successions of state in unit-distance sequences can be seen as a means to avoiding ambiguities or race conditions. Logic designers will further observe that the combinational logic placed on the inputs of the state configuration flip-flops is a function of coding of the states. In such a small

TABLE I—Next State and Output Tables for a Binary Adder.

		Next State for 0, 1 Input		Output for 0, 1 Input	
Present State		0	1	0	1
Start State	1	4	3	—	—
	2	6	5	—	—
	3	1	1	0	1
	4	2	1	1	0
	5	2	1	1	0
	6	2	2	0	1

TABLE II—Formats for Automaton Instructions in RCA 301 Assembly System Code

States Without Output—Format #1		
SN	Compare Transfer on 1 Transfer on 0	Opn'd 1 bit, 0 **Next SN, X** **STP, Next SN**
States With Output—Format #2		
SN	Compare Transfer on 1 Transfer on 0	Opn'd 2 bit, 0 **SN 1, X** **STP, SN 0**
SN 1	Write Write Transfer	**V, Print Loc.** **SV, Switch** **STP, Next SN**
SN 0	Write Write Transfer	**V, Print Loc.** **SV, Switch** **STP, Next SN**

SN=State Name
V=Value of the output
SV=Switch value
X and STP are dummy operands

machine as HiScat, no particular effort was made to achieve the most efficient coding as long as the gate fan-in and fan-out limitations were respected. For more complex control situations, state coding to minimize the combinational logic associated with state configuration flip-flops should be investigated.

The actual logic making up the control flip-flops for HiScat is shown in Fig. 2. Since this logic was implemented with standardized modules, its particular form reflects an economical configuration for particular hardware. The same can be said for the gates producing command pulses in Fig. 3.

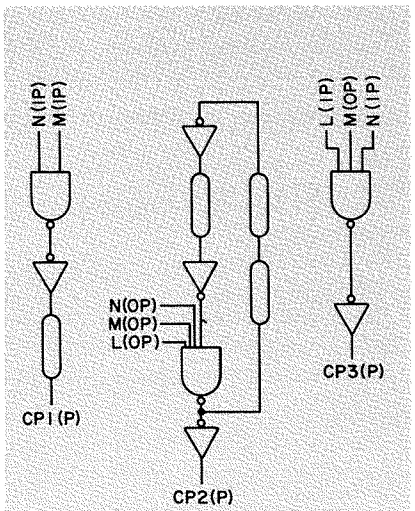


Fig. 3—Command pulse generator for HiScat.

When HiScat went into debugging, the state diagram was a useful supplement to the set of logic diagrams. If the machine failed to run, routine practice was first to read the state of the machine. If HiScat stalled in state 4, failure of the *carry complete in the R register* signal got attention; if it quit in state 0, failure to provide command pulse 2 was probed, to mention two examples. The control automaton itself, along with the tunnel diode circuits, proved to be a very reliable performer, and therefore a trustworthy guide in diagnosing troubles.

The oscilloscope traces in Fig. 4 were taken while HiScat was running continuously through the full cycle of states, as indicated by the vertical zones. The state can be read from the flip-flop traces in the top photograph. A high trace indicates a reset condition of the flip-flop; hence in state 0, all traces are high. In the synchronized photographs below, the production of command pulses (*CP*'s) can be checked against the presence of the state required to produce them. Shown also are the internal return signals, *CAA* and *CCR*, that cause the machine to change state.

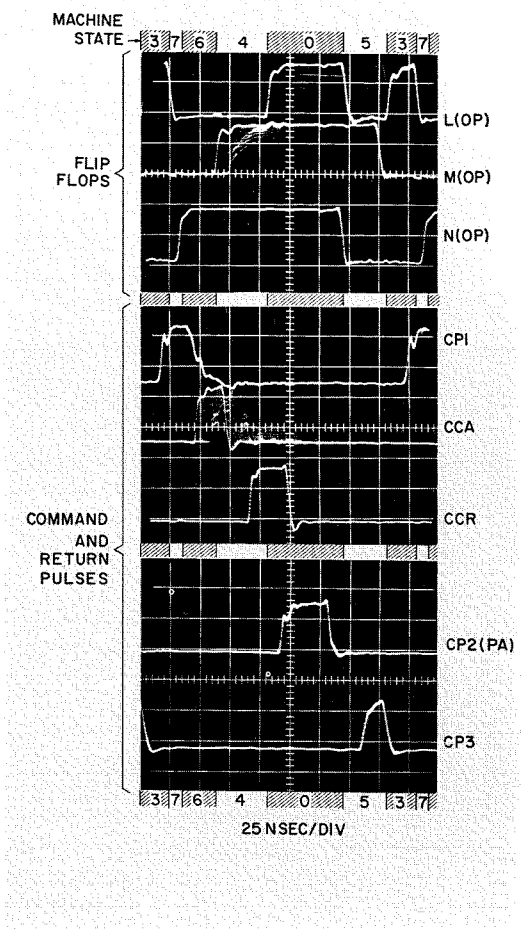


Fig. 4—Scope traces of HiScat control automaton at work.

From Automaton To Computer Program

Just as a machine can be designed and built to behave as an automaton, so a program may be constructed to show the same kind of behavior. Several small programs have been written for execution on the RCA 301 by building a theoretical automaton and then writing a program image of it. A verbal description, from which a binary adder automaton may be constructed, is as follows: The bit in the lowest order of the first operand is the first input, and the bit from the lowest order of the second operand is the second input. At the time of the second input the proper sum bit will appear as an output. While producing the output, the automaton is reset to accept bits of the next higher order and to produce an output in the next order. This cycle will continue until the automaton is prevented from receiving the inputs necessary for internal transition.

An automaton of six states will be adequate, and is described completely in a transition table (Table I). Transistion table descriptions of automata are the most convenient forms of expression for conversion into programs. The automaton starts in state 2. If *1* and *1* are added, the automaton moves to state 5 upon receipt of the first *1* and to state 1 upon receipt of the second *1*. State 1 is the initial state for adding in the next order. While in state 5, however, it has put out a *0* upon receipt of the second *1*. Addition in subsequent orders can be continued by tracing states and outputs in the table. In practical programming, a halt can be called by supplying an illicit character (anything other than *1* or *0*) to the input. It is to be noted that there are two states without outputs and four with outputs. The distinction leads to two formats for sets of instructions.

For use on the RCA 301, coded with the 301 assembly system, the format shown in Table II is appropriate. For each state without output, the coder mentally fills in the items shown in boldface type in format No. 1 from entries in the transition table, and writes the instructions down as specific lines of coding on the 301 automatic assembly program sheet.

When the state has an output, which for a program is likely to be the transfer of a symbol to a print area, the format, as can be seen in format No. 2, is larger because for each input there is a different response in both transition and output. Thus, for programming purposes, the state has been subdivided, here into two parts. The instruction set of the RCA 301 is not ideal for writing this kind of program. Further, what results is not efficient in time or numbers of instructions, but its writing is entirely mechanical.

The automaton for converting binary to hexadecimal notation has an input alphabet of two symbols and an output alphabet of sixteen symbols. It has fourteen states. The time to construct the program was only as long as it took to write down 100 instructions from the format in assembly system code. Although there were many transfers, no flow chart was needed to establish and enforce order. The transition table served in its stead. Obviously, if a coder can write a program so mechanically, a machine can write a larger one—faster and more accurately.

Implementing an Executive Automation

Automata theory also has served programming at a different level. Use of an automaton in implementing an executive system for programs was reported in November 1964 by R. E. Heistand of IBM, Rockville, Md. The 473L system is an Air Force command and control system employing a Librascope L3055 as central processor with numerous remote consoles and data links. "Real-world" tasks imposed on it were to vary from quick question-and-answer exchange with console operators to long loadings or transmissions of files. In order that each real-world terminal have the appearance of being connected to an alert computer which would give service to the terminal in a reasonable length of time, a scheme of priorities and interrupts had to be set up and presided over by an executive control program.

If the sequence of Mr. Heistand's account can be taken as an indication of the sequence of thinking in developing the system, it is interesting to note the steps. First came the verbal specification of how the system should work, then the construction of what he calls the "hypothetical system." This consisted of a "synchronizing section," which prepared inputs for its other section, the automaton. This automaton is a finite-state machine with an input alphabet of three (indicating what kind of input awaits service), an output alphabet of five (indicating what action is to be taken by the central processor (and an internal state set of five (indicating what kind of action the processor is engaged upon). Ultimately, the hypothetical system is the basis for a more versatile system with more sophisticated interrupts. Like its predecessor, it is an automaton embedded in a synchronizing section, which calls it to work and feeds it inputs. The final automaton has 57 internal states, of which 30 produce outputs. It has an input alphabet of 12 and an output alphabet of 17.

Concluding the report, Mr. Heistand is enthusiastic about using automata for two chief reasons: *1)* more complexity can be handled and *2)* debugging is expedited. He writes:

> "Casting the executive function of a command and control system within the framework of a finite-state automaton was quite natural. Many of the complexities that originally seemed insurmountable were easier to handle and unrecognized problems became uncovered during the design phase. The factorization forced onto the constituent parts of the system was an advantage during the debugging phase."

PROMISE FOR COMPUTER DESIGN

These examples from logic design and programming show that some of the concrete potentialities of automata theory are being realized and tested. In the course of this realization, many questions, such as how to achieve appropriate state coding, have been opened to further investigation, but all the early promise of the theory is still present.

The problem of complexity that makes a single human mind too small for logic-systems knowledge sufficient in comprehensiveness and detail for design of large-scale, high-speed computers can be overcome by the organized approach offered by automata theory. The present solution of a committee of human minds, no matter how compatible they seem, becomes a less-good solution as machines grow bigger and more complicated. Unity of organization and internal consistency have a way of falling apart, despite excellent team spirit and intention. There is always the nightmare of building a machine so big and so complicated that no member of the design team can find the inconsistency that prevents the entire machine from being "up" at one time.

CONCLUSION

The very formalism of automaton description is a first step toward putting a computer design within the scope of another computer. It will be this other computer which will remember little logic oversights, that come out later as bugs, and will check the consistency of the latest design innovation while the designers are thinking up the next one to try.

There is another promising aspect of use of the finite-state automaton. As a form of expression, it stands between logic design and programming. Once an automaton has been constructed, it can either be translated into logic design or a program, both of which will manipulate data in the same way. If a design sequence were: *1)* construction of automaton, *2)* translation of automaton to program and *3)* translation of automaton to logic—then the logic could be cheaply simulated by program for a very thorough and fast logic review.

It would seem then, that Prof. Glushkov's remarks about regarding automata theory as a fundamental design aid, with payoff in time and efficiency, are more than dust from the ivory tower.

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DESIGN AND FABRICATION OF A MONOLITHIC-FERRITE INTEGRATED MEMORY

The developmental memory described herein utilizes integrated arrays of magnetic storage elements instead of the presently common approach of wired ferrite cores. Such an integrated memory promises lower memory-system costs for future computers, and the advantage of having the magnetic storage element operate at the power levels of the integrated-circuit logic of the new generation of data processors. In this product-development extension of the continuing research on monolithic (or laminated) ferrite memories[1-3] of the RCA Laboratories, the ECD Memory Products Department in Needham, Mass. has designed an integrated memory stack of 1,024 words of 64 bits, with a built-in word-selection matrix. Words and word lengths can be varied considerably. Described is the preparation and properties of monolithic ferrite arrays and the construction of memory modules. Active product-development continues to improve wafer performance, expand range of operation, and establish techniques for large scale manufacture.

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IN memory systems using wired ferrite cores for information storage elements together with discrete semiconductor circuit devices, the core arrays represent 20% to 60% of the total system cost. With the advent of integrated semiconductor devices appropriate for memory systems use, core arrays will constitute an even greater percentage of cost. As a result, much attention has been given to the development of low-cost integrated arrays of magnetic storage elements. An additional, and by no means minor, objective is to make the magnetic storage elements capable of operation at the power-levels of present-day integrated circuits.

Final manuscript received August 2, 1965.

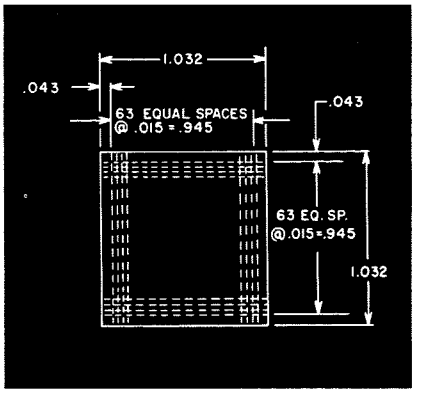

Fig. 1—Ferrite wafer (fired size).

This paper describes the preparation and properties of monolithic arrays of ferrite storage elements, and the techniques developed for their assembly into memory systems. It discusses the monolithic ferrite wafer and its fabrication, the construction of a module composed of two wafers with word addressing diodes, and the assembly of these modules into a 1,024-word, 64-bit-per-word memory having a built-in word-selection matrix. Although a specific stack size is described, the number of words and their lengths can be varied considerably as need dictates.

The monolithic ferrite memory concept described herein evolved from a continuing research effort[1-3] conducted at the RCA Laboratories, Princeton, N. J., and a 2½-year development effort at Memory Products Department, Needham Heights, Massachusetts. The Materials Development Group at Somerville, New Jersey, developed the chips of diodes used in the selection matrix to be described.

FERRITE WAFER

The ferrite wafer is constructed of two groups of conductors sandwiched between very thin sheets of ferrite to form

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ADOLF J. ERIKSON, Leader of Technical Staff, received his BBA in Engineering and Management from Northeastern University in 1950, and currently studying for his MBA. Prior to joining RCA Memory Products Department in 1959, he worked as Mechanical Engineer for the Corps of Engineers and Supervisory Mechanical Engineer for the Quartermaster Corps. Mr. Erikson joined the Memory Products Operation in 1959. His work here has included the design and development of automatic ferrite core and transfluxor handlers, dynamic plane-tester jigs, molded memory plane frames, and more recently, micromagnetic and monolithic memory assembly techniques. Mr. Erikson is a member of RESA and is a registered professional engineer.

P. D. LAWRENCE, Senior Member of Technical Staff, Device Development Section, received an AB degree majoring in Physics from Bowdoin College in June 1961. At that time he joined the RCA Memory Products Operation. His duties have been concentrated on evaluation of ferrite cores and laminates, and development of stack electrical organization for high-speed and very high-speed memory operation.

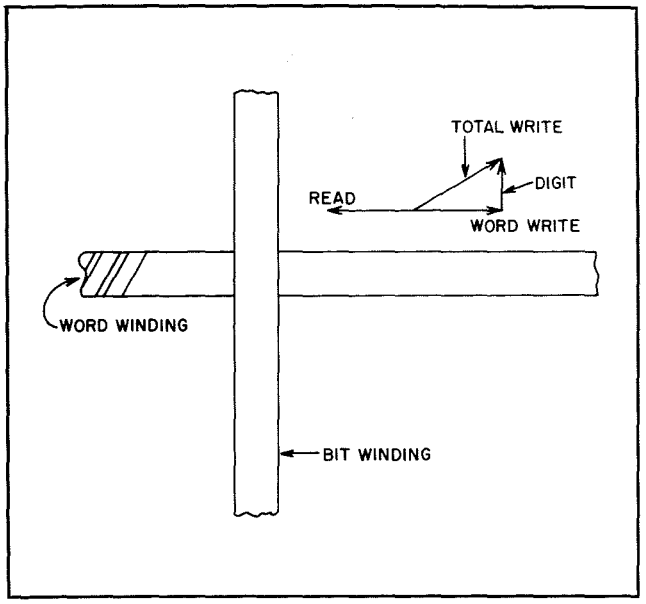


Fig. 2—Nature of magnetic switching at crossover point.

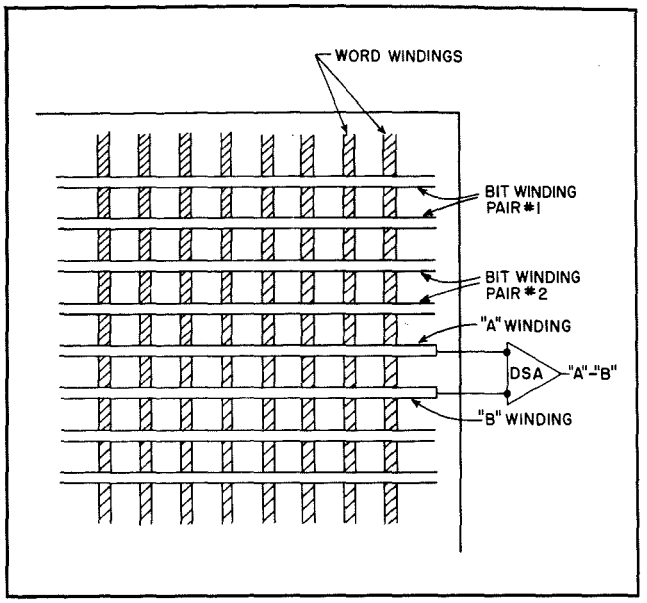


Fig. 3—Laminate winding arrangement for two-crossover per bit storage.

closed-flux-path storage elements. The wafer is just over 1 inch square and less than 6 mils thick. Each group of conductors consists of 64 straight, parallel metallic lines in a planar array, with a center-to-center separation of 15 mils. As shown in Fig. 1, the conductors of one group are placed at right angles to those of the other, with a vertical separation of less than 1 mil.

The ferrite sheets are prepared by a technique known as *doctor blading*. This method consists of passing a metal blade over a mixture of ferrite powder, plastic, and plasticizer dispersed in solvent. When the solvent evaporates, the mixture forms a sheet in which the ferrite particles are bound together by the plastic matrix. Because density of this sheet is related to the extent of dispersion of the ferrite powder in the slurry, the binder system plays a very important role in stabilizing the dispersion. By means of the doctor-blading technique, unsintered ferrite sheets of approximately 50% theoretical density and of thicknesses ranging from 0.1 to 20 mils are readily formed.

In the actual process, the ferrite (Fe-Mg-Mn-Zn composition) is mixed with the plastic binder, plasticizer, and solvent in a ball-mill. The resulting slurry is poured onto a glass substrate, on which the pattern of 64 palladium conductor lines has previously been silk-screened. The conductor lines are 6 to 7 mils wide, 1 mil thick, and 1.2 inches long. The doctor blade is drawn over the slurry to form a sheet of the appropriate thickness. After having dried, the ferrite sheet, with the 64-line pattern now embedded in it, is peeled from the glass substrate. At this point, the resistance of each conductor line is measured as a quality control check on the palladium paste batches.

Four ferrite sheets are then stacked and laminated at high pressure and temperature to form a monolithic body. The firing of these ferrite bodies is divided into two cycles: a binder burn-off stage, and a sinter or densification stage. After sintering, the ends of the palladium conductors are exposed for electrical connection by means of an air abrasive unit that erodes away the ferrite above the conductors. After this operation, electrical resistance of the embedded palladium conductors is 2.5 ohms.

MEMORY BACKGROUND AND WAFER PROPERTIES

Random-access magnetic memories store binary-coded information in groups of digits called *words*. A word has enough binary digits (*bits*) to represent one or more characters, such as alphanumeric characters. A memory is so wired that a specific addressing pulse will simultaneously activate all bits of a selected word to permit insertion (*write*) or retrieval (*read*) of information.

In a linear-select memory, a single winding is used to address all of the bits of a single word. The number of bits of information each word may store is, of course, determined by the number of storage, elements on each word wire. Information is stored in an addressed word by application of appropriate pluses to bit windings, each of which crosses each word winding once at a storage element. Coincidence of these bit-windings pulses (digits) with a word *write* pulse causes magnetic flux to switch to states such that when next that same word is addressed with a *read* pulse, voltage signals representing the stored information appear on the bit lines.

Integrated ferrite wafers have been developed for linear-select operation. Each wafer has 64 word windings and 64 bit windings. Each bit is composed of the crossover points of one word winding with two adjacent bit windings; thus, a wafer has 32 bits per word. Connecting bit lines of several wafers in series produces a memory having some multiple of 64 words. Similarly, word lengths in multiples of 32 bits are formed by the addition of wafers on the other axis.

The vector diagram of Fig. 2 illustrates the nature of the magnetic flux switching that takes place at one crossover point upon the application of *word* and *digit* pulses. So long as pulses are applied to the word winding only, there is no flux change around the bit windings and no signal is coupled magnetically from word windings to bit windings. Fig. 2 also shows the addition of word-*write* and digit driving fields. The respective components are drawn parallel to the driving currents, thus normal to the planes of their respective driving fields. With coincidence of word and digit currents, flux is switched to the plane to which the vector sum is normal. Upon application of word *read* pulse, which is opposite in polarity to the word *write* pulse, all of the flux is switched to planes to which the word winding is normal, with a direction consistent with

the vector marked *read*. The elimination of that component of flux which had linked the bit winding causes a magnetically coupled signal to appear on the bit winding. Analysis shows that the polarity of this signal depends only upon the polarity of the digit current. For the situation shown, the upper end of the bit winding has a positive voltage with respect to the lower end at readout.

Fig. 3 shows the two-crossover-per-bit storage technique. Each pair of bit windings has its own set of digit drivers, as well as a sense amplifier. For those bits of the addressed word which are to store *1*'s, a positive digit current is applied to winding *A*. When that same word is next addressed with a word *read* pulse (opposite in polarity to a word *write* pulse) the *A* lines of bits storing *1*'s and the *B* lines of bits storing *0*'s have negative output voltages, whereas the *B* lines of bits storing *1*'s and the *A* lines of bits storing *0*'s have positive output voltages. Hence, if the difference-sense amplifiers yield *A* minus *B*, the *1* output signals from the amplifiers are negative, and the *0* outputs are positive. Note that the total signal output of the sense amplifier is proportional to the sum of the absolute values of signals magnetically coupled at the contributing crossover points. Capacitance-coupled noise is cancelled. Table I shows representative output values and drive currents for typical wafers.

The bits of each wafer are tested after the winding ends are bared. As shown in Fig. 4, the wafer is placed in a jig with its winding ends in contact with two heads. Each head has 64 metal fingers spaced on 15-mil centers, so that a connection is provided for one end of each word winding and one end of each bit winding. Silver paste is spread along the remaining two edges of the wafer to insure proper grounding of every winding.

TABLE I—Driving Current Pulse Characteristics

Read			*Write*		*Digit*		Output	Read Driving Voltage
I_{read} mA	Time Delay t_d (at 50% points) ns	Rise-Fall Time $t_r - t_f$ ns	I_{write} mA	t_d (50%) ns	I_{digit} mA	t_d (50%) ns	mV	mV/bit
400	110	45	100	120	30	200	45	250
400	80	30	120	100	45	200	60	300
400	60	30	150	30	40	100	30	320

The fingers, in turn, are wired to connectors, which permit easy coupling of digit drivers and sense amplifiers to one bit pair at a time, while the word windings are scanned with reed-switch connections. The pulse sequence shown in Fig. 5 is applied to each bit, and detrimentally disturbed output values of the bit are viewed on an oscilloscope. The drive pulses are shown in column 1 of Table I. The minimum acceptable disturbed signal under these drive conditions is 25 mV.

DESIGN TRADE-OFFS

The successful development of any new and complex electronic device entails recognizing and solving design and processing problems. One of the most challenging problems of the integrated ferrite memory project involved establishing the best combination of wafer dimensions and performance.

At a start of the project, samples were made with a balanced thickness; that is, the sheet within which the word windings were embedded had the same thickness as the sheet within which the bit windings were embedded. Tests showed, however, that this resulted in incomplete readout. A *1* preceded by a *0* had a much lower value than a *1* preceded by another *1*. The reason for this incomplete readout was that with less magnetic material on the side of the word winding away from the bit winding than on the side toward the bit winding, the *read* current was unable to eliminate the flux switched by the digits. Adding material on the side away from the bit windings strengthened the signals, but also increased the drive voltage requirement because of the increased amount of flux switched about the word windings during a *read-write* cycle.

The final trade-off involved total sample thickness, winding width, distance of bit windings from word winding, and distance between word windings. The properties affected were output signal, drive voltage, switching speed, noise, and mechanical design compatibility. Only the 15-mil spacing between word-winding centers remained unchanged to be compatible with the diode-to-diode spacing used in the word-selection matrix.

MODULE

As stated earlier, the windings in the wafer are spaced 15 mils apart. On the digit sense axis, individual connection to each winding is required because every winding must be controlled separately when a word of information is written into the memory, as well as sensed separately when a word is read out. However, only one word winding is ever selected at any one time.

Fig. 6 shows a module made up of two wafers, along with associated diodes and bussing for word selection. The module is used as a building block for larger

Fig. 4—Test jig for monolithic ferrite wafers.

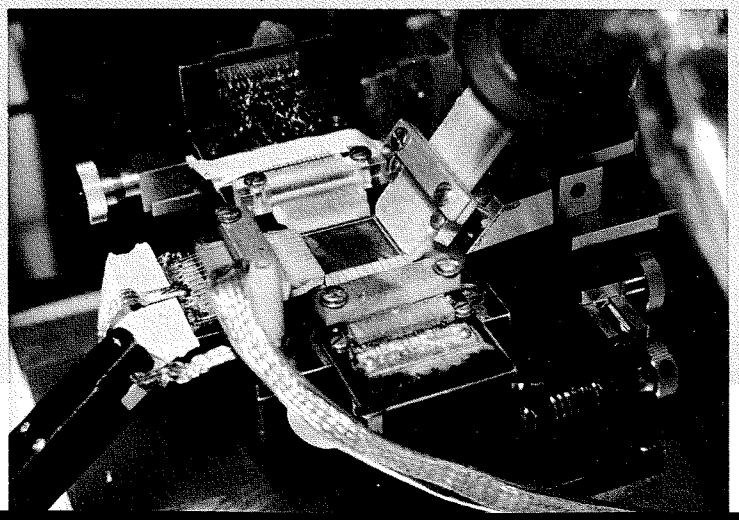
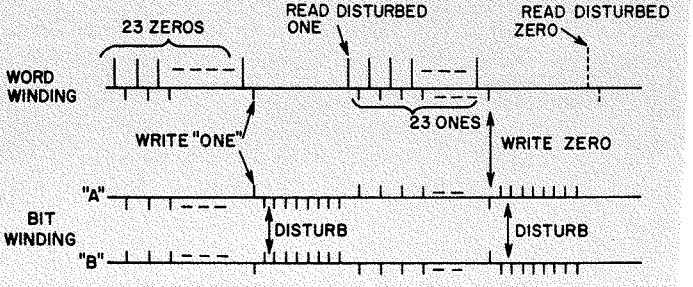


Fig. 5—Test pulse sequence.



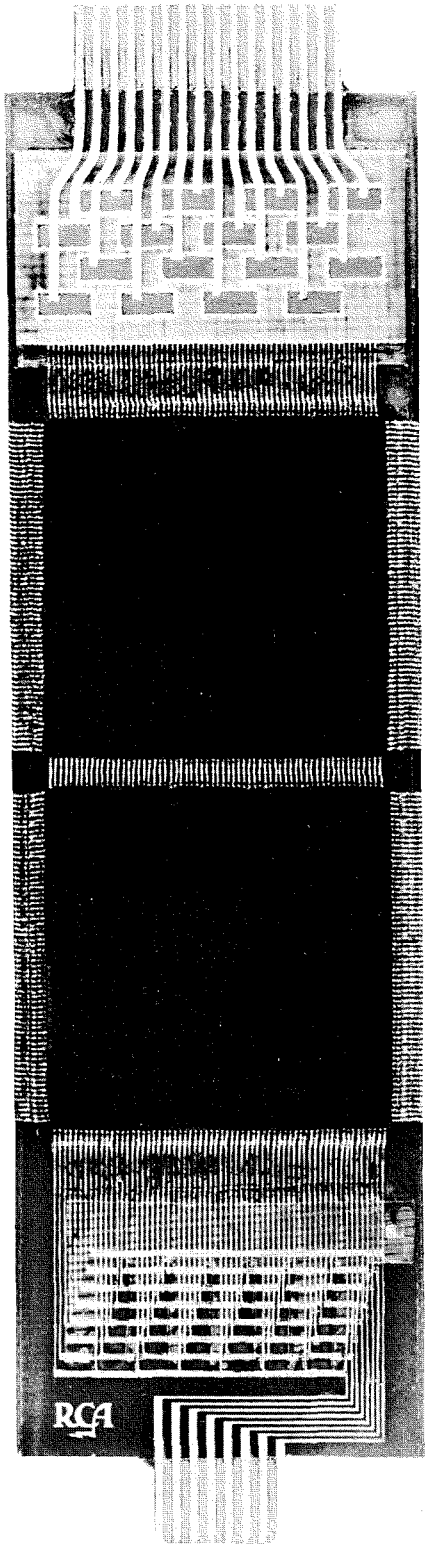


Fig. 6—Two-wafer module.

TABLE II—Diode Characteristics

(Static Values at 25°C)

Forward voltage V_F at $I_F = 400$ mA	2 V max.
Reverse current I_R at $V_R = 30$ V	3 mA max.
Breakdown voltage BV_R at $I_R = 200$ mA	60 V min.
Reverse recovery time t_{rr}	15 ns
Junction capacitance C_j at $V_R = 0$ V	6 pF max.

arrays. Diode characteristics appear in Table II.

Fig. 7 is a schematic of a module. For convenience, a 16-word array is shown, while the modules actually have 64-word arrays. *The explanation below assumes that there are 64 words.*

One end of each word winding is connected to the anode of one diode and the cathode of another. The cathodes of diodes whose anodes are connected to word windings are common in 8 groups of 8 diodes each. The anodes of the diodes whose cathodes are connected to word windings are grouped identically. This arrangement reduces the number of connections required on this end of the word windings from 64 to 16. The other ends of the word windings are connected directly together in eight groups of eight words each. Each group has one word from each of the diode groups, and the number of connections to this end of the module is reduced from 64 to 8.

The diode chips, shown in Fig. 8, have two rows of four diodes each, spaced on 30-mil centers; thus, 8 adjacent word windings can be connected to the diodes of one chip of each type with straight, parallel conductors.

A positive- and a negative-voltage switch are connected to each group of words on the end without diodes, and a driver-to-ground is connected to each of the 16 groups of diodes. For readout of a particular word, the positive voltage switch for the group to which that word belongs is activated, and the grounding driver for the group of common-cathode diodes to which that word is connected is closed. Conversely, a word *write* pulse is applied by the activation of the appropriate negative switch and of the driver connected to the correct group of common-anode diodes. Fig. 7 shows that each word may be separately selected by the appropriate choice of driver and switch.

The word-selection technique described above is not new; it has been used for years. The new feature is that the diodes, busses, and magnetic elements are mounted on the same board to reduce the contact density required for access from the outside.

The diode selection matrix can be expanded to arrays of more than 64 words, by connecting corresponding points of different modules together. For example, a 1,024-word matrix would have 32 groups of 32 words each.

Because connectors spaced on 15-mil centers are not available, fan out is required for bit line connection to the outside. However, a new, low-cost technique has been developed for mass interconnection of wafers. Wafers are interconnected to form modules such as that shown in Fig. 6 by means of tabs soldered directly to the winding ends. These tabs are originally made up in the form of combs etched from one-ounce copper sheet. After etching, the combs are plated with an electroless tin coating to facilitate soldering. As shown in Fig. 9a, the combs have 64 teeth spaced on 15-mil centers. After the teeth of the comb are soldered to the wafer winding ends and the assembly soldered to a printed-circuit pattern on the module substrate, the solid end is sheared off to leave the precisely spaced tabs for connection to the bit windings of other modules.

The diode array is assembled as a separate unit, as shown in Figure 10, and cemented onto the module. Diode connection is also accomplished by means of projecting tabs soldered to previously mounted combs. Connection to the switch busses at the lower end of the module is also accomplished with combs (Fig. 9b) etched from 1-ounce beryllium copper. These combs are raised above the module surface at appropriate crossover points.

The module substrate is constructed from 1/16-inch G-10 laminated glass epoxy board. The diode assembly consists of base board having a printed circuit pattern, and a spacer board of G-10 material, with the common connections etched thereon (Fig. 10).

MODULE TESTING

For testing, the module board is mounted in the fixture shown in Fig. 11. This unit is designed to pick up 64 sense and digit connections simultaneously. Because the sense digit connections are on 15-mil centers, the design of the contact head must be very precise. For accurate contact placement, fine movement of the contact heads is provided by the micromanipulators shown. The contacts are constructed from 7-mil beryllium-copper wire, prebent and guided to retain the 15-mil spacing.

Word drive connections are made by use of printed-circuit plugs having contacts placed on 50-mil centers.

STACK

As shown in Fig. 12, the finished stack (consisting of 1,024 words of 64 bits) is formed from two planes of 512 words. The overall dimensions for the unit, including sense-digit connector boards with terminating resistors, are 14 by 4½ inches, with ½-inch spacing between the planes. The sense-digit connections are fanned out from the 15-mil centers to suitable plug connections on 50-mil centers. The module boards are cemented onto a backboard and interconnections between the modules are made by soldering. Bussing between planes is pro-

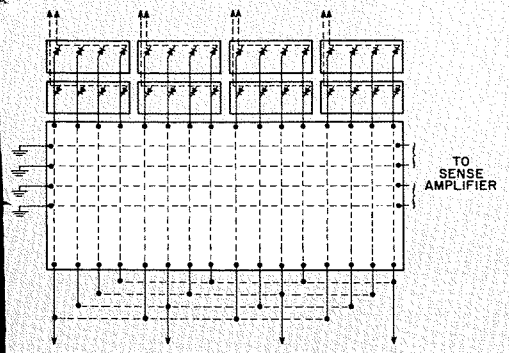


Fig. 7—Schematic of 16-word-array module.

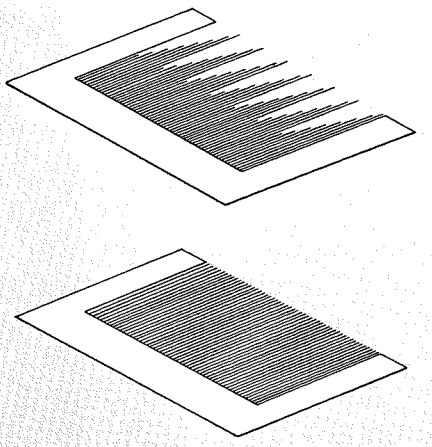


Fig. 9—Connection tab "combs" for (top sketch) wafer winding ends and (below) switch busses.

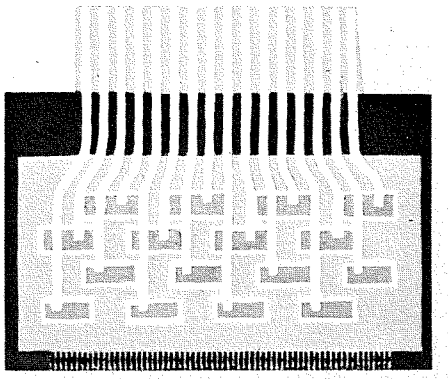


Fig. 10—Diode assembly.

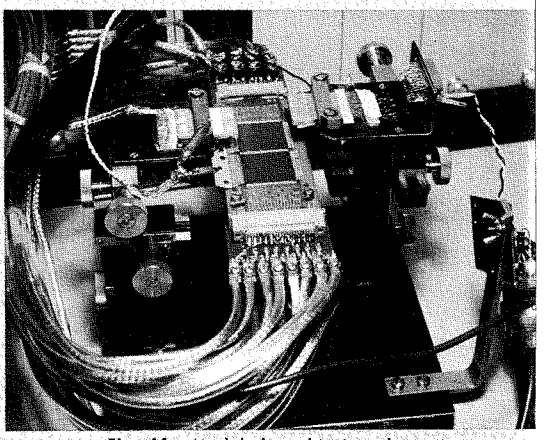


Fig. 11—Module board test equipment.

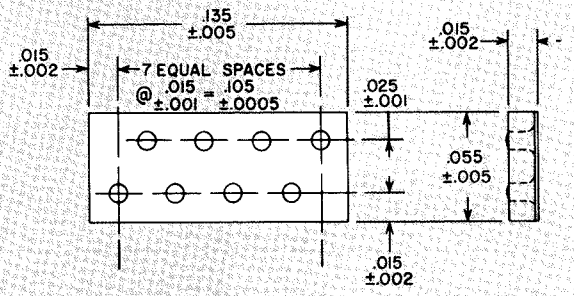


Fig. 8—Diode chip arrangement.

vided by No. 30 wire soldered between corresponding bit windings of the two planes.

This stack has undergone partial preliminary evaluation at DEP Applied Research in Camden, N. J. The results indicate that a 600-ns *read-write* cycle time is realizable in the 1,024-word array. Signal outputs were typically greater than 10 mV, and noise was very low during the turn-on of the *read* current.

FUTURE

Active applied-research and product-development programs are now underway for improving wafer performance, expanding the range of operation, and establishing techniques suitable to large-scale manufacture. The following specific items are receiving greatest emphasis:

1) *Reduction of winding resistance.* Signal attenuation along the sense winding can prevent operation of large arrays.
2) *Reduction of the required driving currents for compatibility with integrated-circuit drivers.* Actually, this is but one step in expanding operational range, but drive reduction is stressed because of the important cost advantage of using memory systems in conjunction with integrated circuits.
3) *Fabrication of wafers from temperature-stable ferrites.* RCA is an industry leader in the development of temperature-stable ferrite cores; use of these materials in integrated wafers is a natural capability to pursue.
4) *Continued development of a nondestructive read-out capability.* To date, output signals of 6 to 8 mV have been attained for standard 64-by-64 platelets with nondestructive *read* drive.
5) *Cost reduction.* A program is in progress to take full advantage of the low-cost potential of integrated structure as wafers move into large-scale production.

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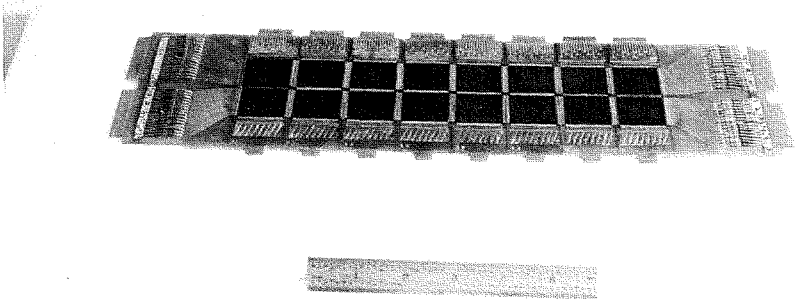
3. R. A. Shahbender, (RCA Labs, Pr.) "Research on a Combined MOS-Circuit Monolithic-Ferrite Integrated Memory," RCA ENGINEER, *this issue.*

Fig. 12—Completed 8-module stack.



RESEARCH ON A COMBINED MOS-CIRCUIT, MONOLITHIC-FERRITE INTEGRATED MEMORY

The continuing RCA Laboratories research program on integrated memories has led to the approach described in this paper, wherein a monolithic-ferrite (also called a laminated-ferrite) stack is integrated with integrated MOS circuitry. Many advantages will accrue from such a batch-fabrication of large-capacity memory stacks. The particular laboratory approach described herein involves a stack of 10^7-bit capacity, cycle-time of a few microseconds, and a cost of less than 1 cent per bit.

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THE *non*integrated, individually manufactured and tested, hand-wired ferrite core is the most widely used storage element in today's digital computer. This universality in the use of cores is a result of the favorable economic and technical performance characteristics accomplished by combining core stacks with *non*integrated electronics to build random-access memories.[1]

For the past decade, the cost of electronic circuitry has been relatively high. This has favored the use of cores in a coincident-current mode of operation to minimize the amount of electronic circuitry.

But today, integrated circuitry, with its promise of low cost, places a greater emphasis on realizing memory stacks compatible with integrated circuits—rather than those that minimize the number of circuits. Further, if truly economic large-capacity memories are to be built in a few years time, then batch-fabricated magnetic stacks compatible with integrated circuits must be realized. This leads to the concept of *integrated memories*. Specifically, the integrated memory discussed in this paper consists of a monolithic ferrite (laminated ferrite) stack integrated with integrated MOS circuitry. The expected memory characteristics are a capacity in excess of 10^7 bits operating at a cycle time of a few microseconds at a cost of *less than* 1¢ per bit.

For a coincident-current memory, the capacity of a module—i.e., a unit stack and its associated driving and sensing electronics—decreases with decreased cycle time. This is shown graphically in Fig. 1 for RCA computer memories.[2]

The decreased cycle time is accomplished by using smaller cores (strung with four wires) with an increased coercive force. The number of words per stack and the number of bits per word is decreased to maintain adequate output signal-to-noise ratios and limit the back voltage to be overcome by the current drivers.[2] Increasing the cycle time permits a limited increase in memory capacity, say up to 5×10^9 bit, beyond which the electronic circuitry must be duplicated.

For a word-organized system, higher operating speeds are possible, as indicated by the data for RCA memories[3] shown in Fig. 1. Use of smaller cores (strung with only two wires) of higher coercive force may lead to additional increase in speed.

Diode word selection is normally used to reduce the cost of the driving electronics. The stack noise introduced by diode selection places an upper limit on the size of the selection matrix. Increasing the cycle time permits the operation of larger selection matrices. The bits per word is limited by back voltage.

For a relatively long cycle time, a coincident-current core memory is more economic than a word-organized system. The cost of the diodes required for word selection normally offsets the savings realized from using cores strung with only two wires (coincident current memories use cores strung with four wires).

Monolithic ferrite memory arrays operated in a word-organized mode via integrated diode selection[4,5] matrices are expected to lead to lower cost systems—i.e., lower than equivalent coincident current memories. The expected performance characteristics of these systems[6] are also shown in Fig. 1.

The recently announced mass core memories[7] utilize two wire core arrays to realize capacities of 2×10^7 bits operating at a cycle time of 10 μs (Fig. 1). These memories combine a coincident-current *write* with a word-organized *read* to realize the large capacity with a minimum of electronics. The bit cost of such a system is considerably lower than an equivalent coincident-current memory. For this type of operation, the magnetic element need exhibit threshold and squareness properties somewhat less stringent than required for coincident-current operation. Thus, it may be possible to operate monolithic ferrite arrays in a similar fashion. The advantages to be gained are, obviously, reduced cost and potentially shorter cycle time.

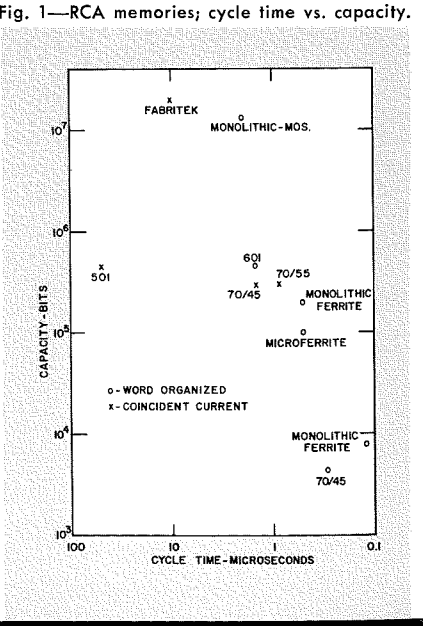
The key to realizing large-capacity magnetic memories is the integration of integrated circuits with magnetic memory stacks. The key to this integration is the realization of batch-fabricated magnetic-memory elements with operating and mechanical characteristics that are well matched to the integrated circuits.

Low cost operation of the magnetic element with relatively high sense outputs are a prerequisite for the successful use of integrated circuits. High packing density to simplify interconnections is also an advantage if low cost is to be achieved. A highly promising approach, under investigation at the RCA Laboratories, is based on the use of monolithic

FERRITE-STACK MEMORY ARRAYS

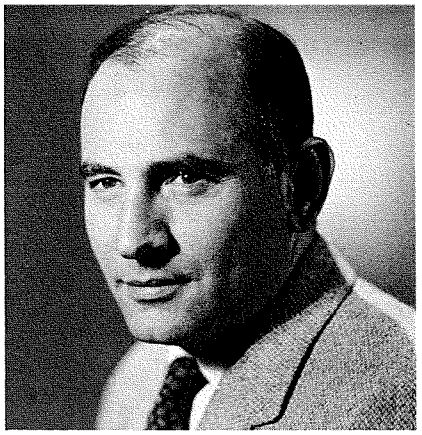
Experimental memory arrays with 256 x 64 crossovers, 256 x 100 crossovers, and 512 x 200 crossovers (kilobit arrays) are being fabricated and assembled into stacks. For the fabricated arrays, the crossover spacing is nom-

Fig. 1—RCA memories; cycle time vs. capacity.



Final manuscript received July 24, 1965.

[EDITOR'S NOTE: Related work on a monolithic ferrite integrated memory now in the preliminary stages of product design and fabrication at EC&D, Needham Heights, Mass. is described in another paper[6] by Cosgrove, et. al. That approach, which does *not* involve integration of MOS circuitry with the laminated-ferrite memory element, is an outgrowth of earlier RCA Laboratories research on integrated memories.]



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ferrite memory arrays with integrated MOS transistor circuitry.
inally 10 mils. Fig. 2 is a photograph of an assembled stack consisting of four 256 x 64 arrays spaced on 50-mil centers[8] (density of 2×10^5 bits/in^3).

Fabrication of kilobit arrays is accomplished by modification of the doctor-blading and laminating technology[5] used for producing smaller-sized planes. Sintering of the kilobit arrays is critical if uniformity and reproducibility in mechanical dimensions and conductor spacing is to be achieved. Fig. 3 is a plot of the cummulative error in conductor placement (defined as the difference between the measured placement of a conductor from a reference point and the desired placement of the conductor) for both edges of a typical kilobit sample plane.

Interconnection techniques compatible with cummulative error equivalent to that shown in Fig. 3 are under investigation.[8] Improvements in the mechanical characteristics of the memory planes will simplify the interconnection problem.

A magnesium-manganese-zinc ferrite[8] specifically developed for low power operation is used in the fabrication of kilobit arrays. The ferrite characteristics are:

H_c = coercive field = 0.4 Oe
B_r = remanent flux density = 1200 G
S_w = switching coefficient = 0.3 Oe·μs
squareness = 0.9
T_c = curie temperature = 110°C
ρ = DC resistivity = 1.1×10^8 ohm-cm at 20°C

Fabricated kilobit arrays have been hand-wired and tested in a word-organized, one-crossover-per-bit mode.

Two alternative digiting techniques—*bipolar* or *unipolar*—may be used to enter information in a word-organized system. For bipolar digiting, the binary numbers are entered by the coincidence of a write pulse applied to the word winding and a digit pulse, say positive for *1* and negative for *0*, applied to the digit-sense winding. The sense signals are bipolar and nominally of equal amplitude. For unipolar digiting, a digit pulse is applied to enter a *1* and no digit pulse to enter a *0*. The sense signals in this case are unipolar and of different amplitude.

For the tested kilobit arrays, bipolar digiting led to considerably better sense-signal discrimination. For a sample plane with 256 x 100 crossovers in which a total of 234 randomly selected bits were tested, a histogram of the disturbed sense signals is shown in Fig. 4. The test operating conditions were:

Current	*Amplitude*	*Duration at 50% points*
read I_R	48 mA	0.5 μs
write I_W	20 mA	0.4 μs
digit I_D	±5 mA	0.7 μs

The *read*-current risetime is approximately 0.4 μs. The peak back voltage is 28.0 mV/bit. Similar data has also been obtained for a number of other sample planes.[8]

INTEGRATED MOS MEMORY CIRCUITS — DEVICE DESCRIPTION

The MOS transistor, also called *insulated-gate-field-effect transistor* (IGFET) consists of two highly doped semiconductor contact areas separated by a narrow semiconductor channel. The channel region is insulated by silicon dioxide from a metal contact on its surface. The contact forms one plate of a capacitor that controls the current flow between the highly doped contact areas. The control electrode is designated the gate and the highly doped contact areas are the source and drain electrodes. The MOS transistors can operate with positive and/or negative gate bias and can be fabricated for conduction with zero bias (depletion mode) or for conduction to begin after exceeding a designable threshold (enhancement type).

The structure of an *n*-channel enhancement-type MOS transistor (induced channel) is shown in Fig. 5. An enhancement mode transistor can be made bidirectional such that source and drain can be interchanged without changing the characteristics of the device. Thus the source-drain current can be reversed by the application of a drain voltage of opposite polarity, as shown in the characteristics of Fig. 6. The current capability of the MOS transistor is a function of the length, width, and doping of the channel region, as discussed in the literature.[9] The device has been designed to meet a wide variety of applications.

MOS WORD CURRENT SWITCH

To supply the word *read-write* currents to the monolithic ferrite memory, an MOS transistor switch is used to route the word currents to the selected memory location. In this application, the MOS transistor is operated as a low-impedance bidirectional switch utilizing the electrical characteristics displayed in the first and third quadrants of Fig. 6. A strip of MOS transistor word switches, each connected to a word conductor, are supplied from a common word-current source, since only a single word is addressed at a given time. Word current in the memory is obtained by pulsing the gate of the MOS transistor connected to the desired word line (Fig. 7).

Arrays of 64 MOS-transistor switches (Fig. 8) with spacings compatible with the monolithic ferrite memory conductors, have been experimentally fabricated with a common source contact bus. To minimize the power expended in driving the word bus, the rise and fall times of the bus *read-write* pulses are slowed to the extent permitted by cycle time. The fast response time of the MOS transistor to a change in gate bias is utilized

Fig. 2—Assembled stack of four 256 x 64 arrays spaced on 50-mil centers, for a density of 200,000 bits/in.^{3}

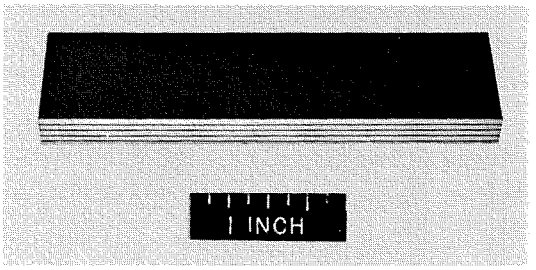
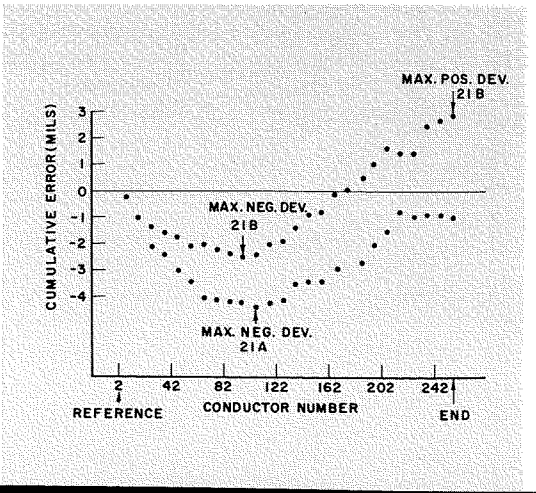


Fig. 3—Maximum deviations from standard vs conductor location, sample 21.



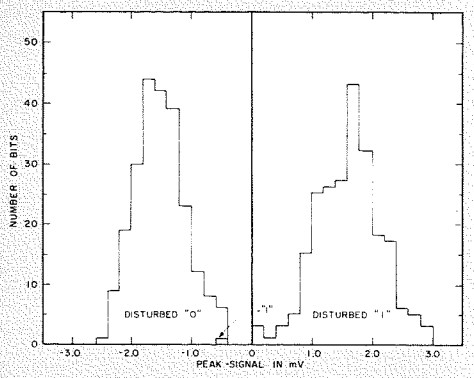


Fig. 4—Histogram of outputs, sample JK3.

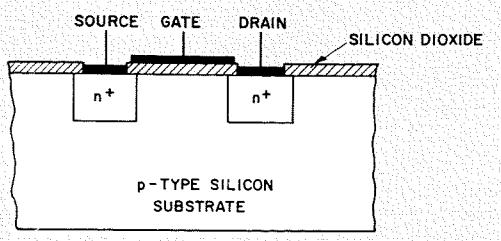


Fig. 5—Geometry of induced channel MOS transistors.

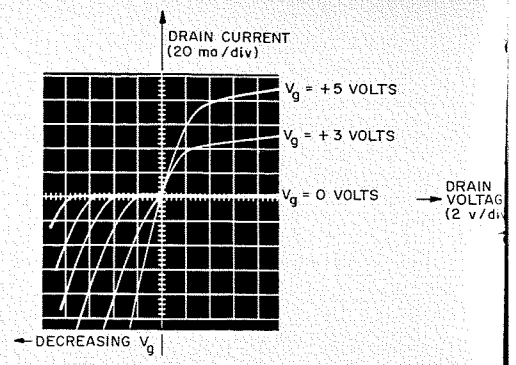


Fig. 6—Characteristics of enhancement type MOS transist

to obtain faster rise and fall times of the actual memory word currents. The same unidirectional *turn-on* signal is supplied to the gate electrode of the selected word transistor switch for both the read and write operations. For operation as a bidirectional switch, a substrate bias is required to provide isolation for the output drains of unselected switches. This bias must exceed the back voltage along the selected memory word plus the voltage across the switch. This bias reduces the effective device g_m and the source junction capacitance.

Experimental MOS transistor word switches with substrate bias of −10 volts exhibit the following characteristics: $I_D = +50$ mA, −80 mA for $V_{SD} = \pm 4$ V, $V_G = 4$ V, gate capacity = 20 pF.

WORD ADDRESS DECODER

Control of the gates of the word switches may be accomplished by use of a matrix or a tree decoder. Integrated-circuit topology and interconnections to the MOS transistor word switches are simplified by use of a tree decoder. A quaternary tree decoder of MOS transistors are such that the fanout of four required for the quaternary system is practical and results in a significant reduction of semiconductor elements compared to a binary system without an increase in control connections. A comparison of the binary and quaternary trees for a 1,024-output system is given in Table I.

Because of the essentially capacitive high impedance gate input of the MOS transistors, high-current transistors are not required for the decoding tree. Small, low-current transistors are applicable as low-impedance switches.

Experimental logic level MOS transistors have the following characteristics: $I_D = 3$ mA for $V_{SD} = 3$ V, $V_G = +5$ V, gate capacity = 5 pF.

Binary-to-quaternary conversion has been accomplished by use of integrated four-output experimental MOS transistors connected to the four control connections of each level of the tree. A two-level, sixteen-output MOS transistor quaternary tree decoder is shown in Fig. 9.

DIGIT DRIVER

The digit driver is operated as a constant current device rather than as a low impedance switch, i.e., it is operated beyond the knees of the curves in the first quadrant of Fig. 6. Because of the reduced current requirements, the digit-driver MOS transistors are scaled down versions of the word switches. (Bipolar digit currents are supplied by use of two digit drivers, each connected to supply a unidirectional current for reasons of circuit simplicity.)

Experimental constant-current digit-driver MOS transistors have the following characteristics: $I_D = 12$ mA for $V_{SD} = +5$ V, $V_G = +4$ V, gate capacity = 12 pF.

SENSE AMPLIFIERS

An important component in a word-organized memory is the sense amplifiers. For the integrated monolithic ferrite memory, it is expected that a considerable number of integrated sense amplifiers will be required.

The MOS as well as bipolar transistors may be used for constructing integrated sense amplifiers. Both types of circuits are being investigated. For the memory the gain and bandwidth required for the amplifier are 500 and 5 Mc/s, respectively.

These characteristics are relatively easy to achieve with integrated bipolar transistor circuits. However, input offset voltages, of the same order as the sense signal, are encountered in tested bipolar transistor circuits thus requiring the use of trimmers or AC coupling networks. Both types of solutions are being investigated.

For the MOS amplifers, equivalent thermal-input noise places a lower limit on the sense signal amplitude that may be reliably detected. Noise measurements on experimental transistors indicate an equivalent noise voltage[10] of 21 μV for a bandwidth extending from 10 c/s to 11 Mc/s. For a sense signal of 0.28 mV into a single-ended amplifier, the error rate is 10^{-10}. Using nonintegrated transistors, a ten-stage, DC-coupled amplifier was constructed and is presently undergoing testing.

SYSTEMS CONSIDERATIONS

The expected speed-capacity characteristic of an integrated-monolithic-ferrite, MOS-circuits memory may be estimated. The cycle time of word organized core systems is in the range of three to five times the switching speed of the core. Thus for the integrated memory the cycle time is expected to be in the range of 1.5 to 3 μs, faster cycle time being associated with a more liberal use of semiconductors.

The permissible word length is primarily determined by the voltage breakdown characteristics of the MOS word switches, and the back voltage per bit. Experimentally, words of 200 bits have been successfully operated in conjunction with MOS circuitry.

The word-selection system utilizes an MOS switch per word, with one end of each word conductor permanently grounded. This is expected to result in extremely low stack noise. The number of words energized from a common current generator is limited by the stack noise. Preliminary estimates indicate that this limit is of the order of 10^4 words.

Attenuation of the sense signal in propagating along the sense-digit winding necessitates the use of sense preamplifiers. The experimental attenuation data shown in Fig. 10 indicates that for bipolar sense signals with a duration greater than 100 ns, preamplifiers may be required for each block of 10^4 words.

From the above considerations it is expected that an integrated-monolithic-ferrite, MOS-circuits memory with a capacity of 65,536 words of 200 bits each, and operating at a cycle time of a few microseconds, *can be constructed.* Paralleling of memory blocks may be used to attain capacities in excess of 10^7 bits.

COMPETING TECHNOLOGIES

A number of competing systems have been proposed for realizing large-capacity magnetic memories. In general, these systems depend on the use of batch-fab-

ricated magnetic elements with or without integrated semiconductor circuits. Prime among these competing systems are plated wire memories.[11] These offer the advantage of nondestructive read which may result in a reduction in sense amplifier electronics. The word drive current required for a plated-wire memory is at least an order of magnitude greater than that of the monolithic ferrite. This necessarily complicates the word drive electronics, and for large capacity (i.e., long words) rules out the use of integrated drivers.

Cryoelectric memories[1], under intensive investigation at the RCA Laboratories, are expected to be the ultimate solution for realizing large-capacity random-access memories. In these memories, *both* the storage cell and the accessing circuitry are batch fabricated as integrated structures—resulting in great economics. A minimum of peripheral electronics is needed to operate the system. The expected memory performance characteristics are a capacity of 10^9 bits at a cycle time of a few microseconds. The expected memory cost is somewhat independent of memory capacity,[12] for capacities in excess of 10^7 bits, thus resulting in a drastically decreasing bit cost for increased memory capacity.

An all-integrated semiconductor memory is technically feasible. However, preliminary cost estimates indicate that a batch-fabricated magnetic storage element is one to two orders of magnitude lower in cost than an integrated semiconductor storage element. Thus, the realization of all-integrated semiconductor random access memories of large capacity is economically not feasible. High-speed scratch pad memories and associative memories are however considerably more attractive for realization with integrated semiconductor circuitry.

TABLE I — Comparison of Binary and Quaternary Trees

Tree	*Number of Semiconductor elements*	*Number of Control connections*	*Number of Levels*	*Number of Outputs*
Binary	2,046	2 x 10 = 20	10	2^{10} = 1,024
Quaternary	1,364	4 x 5 = 20	5	4^5 = 1,024

CONCLUSIONS

The need for high-speed, economic, large-capacity random-access memories is becoming increasingly acute. Various electromechanical storage devices are under development to fill this need in terms of capacity—but not in terms of speed. Further, these electromechanical systems pose considerable difficulty for the user in that they provide random access to relatively large blocks of information rather than to individual words.

The attainment of a magnetic memory with the characteristics described in this paper would be of tremendous value to the data-processing field. Technical feasibility of the described memory system is being established at the RCA Laboratories.

ACKNOWLEDGEMENT

The work on the monolithic ferrite structure and integrated MOS memory is being done in the Computer Research Laboratory under the direction of Dr. Jan A. Rajchman. The author wishes to express his appreciation to Dr. W. A. Bosenberg, Dr. J. Robbi, and J. W. Tuska for their contributions to this project.

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Fig. 8—Photomicrograph of 64 output MOS word switch (44 units shown).

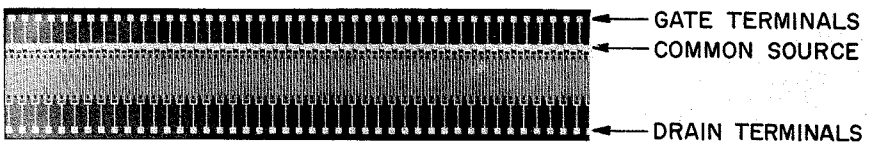


Fig. 7—Integrated MOS transistor word switch.

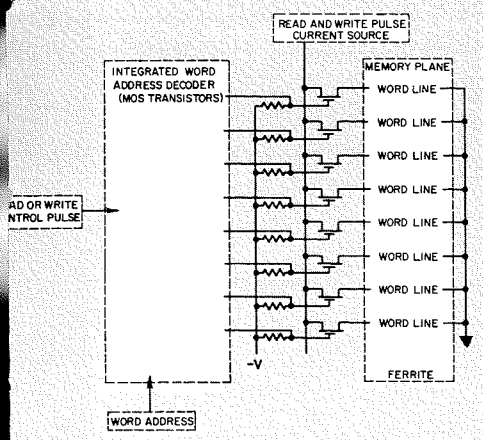


Fig. 9—Integrated MOS transistor quaternary decoder tree (2-level, 16-output shown).

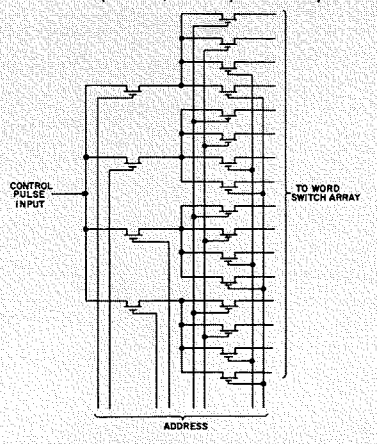
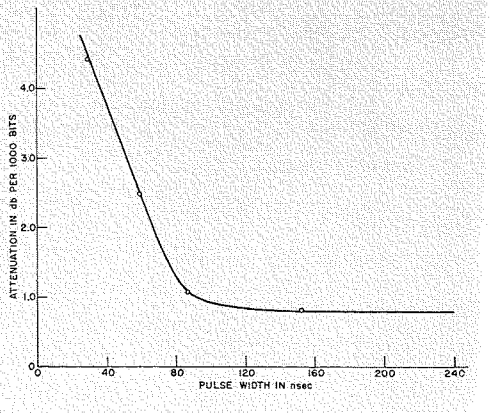


Fig. 10—Attenuation vs pulse width.



DIVCON

Digital-to-Video Conversion System

R. J. CLARK
Defense Systems Group
RCA Victor Company Ltd.
Montreal, Canada

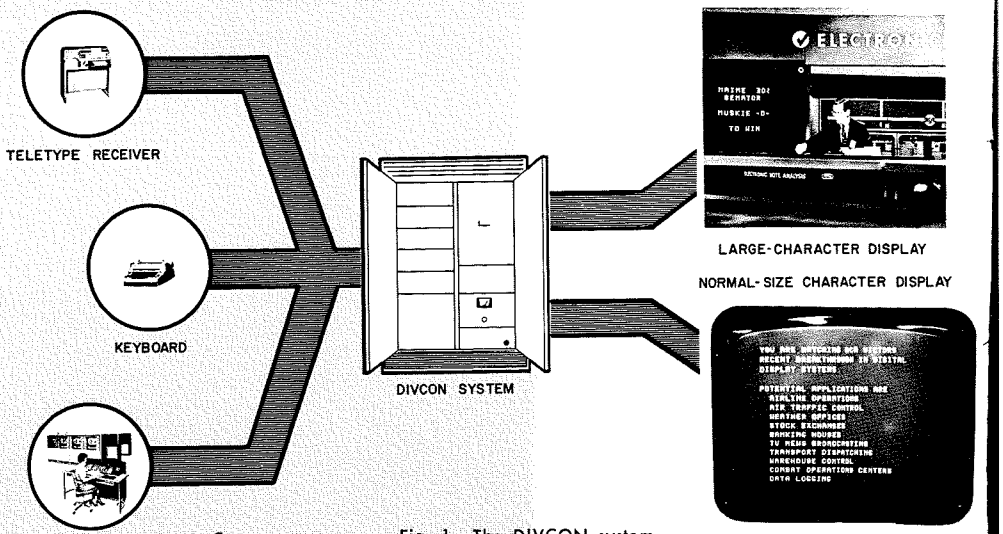


Fig. 1—The DIVCON system accepts data from a variety of sources (teletype, computer, magnetic tape, etc.), stores the data and converts it to a signal form suitable for display on raster scan television equipment.

This digital-to-video conversion (DIVCON) system enables the outputs of data-processing equipment, teletype machines, or keyboards to be readily presented in alphanumeric form by television. The system is extremely economical and flexible, uses low-cost, readily-available TV equipment and simple video transmission techniques.

THE DIVCON System receives data from the various sources and stores it in memory. The contents of the memory are read out to digital video generator units in accordance with a display format. In the digital video generator units, the digital data are converted to standard television video on multiple output channels with up to 2,000 character positions per display screen (for 525-line (interfaced) TV equipment). An internal, fast-random-access core memory can accept write-in speeds of up to 500,000 characters per second, or can accept simultaneous multiple inputs from, for example, data processors, ticker circuits, or keyboards. Writing into the system is simplified by well-presented operating instructions.

It is possible to gain direct access to the location of any character in any channel; thus, single characters can be changed as necessary. This is accomplished with the aid of a cursor which indicates character location. Cursor controls such as line feed, carriage return, advance and backspace are provided to position the cursor on the display screens. Attention can be drawn to single character symbols—or to groups of symbols—by flashing, by underlining, or by the use of color. A special feature is the production of moving character displays for ticker readouts; up to 30 ticker inputs can be monitored on each display channel. It is also possible to position character symbols anywhere on the display screen, a useful feature for map plotting and other large-screen applications.

Final manuscript received April 26, 1965.

GENERAL DESCRIPTION

A DIVCON System consists of:

1) display control logic (DCL) comprising the memory subsystem and the input-output programmer subsystem;
2) display timing logic, comprising the timing and control subsystem;
3) input interface logic, comprising an interface subsystem for each associated input device; and
4) output digital-to-video conversion logic, comprising a digital-video-generator (DVG) subsystem for each pair of output channels.

The display control logic is programmed to store information from the various interface subsystems, and to read the contents of the memory to a series of digital-video-generator subsystems, which translate the digital data into TV video in synchronism with the TV scanning periods.

Operating the system from a keyboard or processor requires a minimum of instruction, and is carried out as follows:

1) The system is alerted by means of a *start of message* code, followed by a channel identification number.
2) The user types the message into the selected channel.
3) An *end of message* code closes the memory to noise or erroneous messages.

The system responds to all control functions normally found on an electric typewriter, such as line feed, return, space, shift and backspace, while facilities are incorporated for such useful operating aids as: *erase character* (blank), *erase to end of line*, *erase to end of channel*, *underline data*, *flash data*, and *blank data*.

The instructions for writing data into the DIVCON System are the same for all input devices; code conversion logic is provided to enable the system to work with data processing centers using different machine languages. The input logic accepts seven-bit parallel characters and a strobe signal from the data source. Each seven-bit character is checked for an odd number of *1*'s, and a parity error signal is generated if an even number of *1*'s is present.

Data are stored in the random-access core memory in eight-bit code; the first six bits describe up to 64 character symbols, the seventh provides additional symbols and/or display control functions such as *underline*, *flasher*, etc., and the eighth bit is the parity bit. The size of the memory depends on the number of output video channels required, and

on the number of character symbols required for each channel. For example, a system with ten channels, each capable of displaying sixteen lines with 48 characters in each line, uses a (4,096 x 16) core memory.

A multichannel system provides a separate video output signal for each channel; these signals can be fed to any number of monitors over any distance. The system is readily adaptable to any raster-type scanning system because DIVCON timing signals are derived from a series of digital counters, synchronized to the TV horizontal and vertical drive pulses.

SYSTEM ORGANIZATION

The DIVCON System (Fig. 2) is composed of subsystems, the number of which depends on the number of associated input devices and output channels. Systems with two to four channels can be housed in a single-bay rack assembly (22 x 22 x 72 inches), while systems with 10 to 24 channels require a triple-bay rack assembly (66 x 22 x 72 inches).

Input-Output Programmer Subsystem

The center of operation is the input-output programmer subsystem, which writes incoming data into the memory from the various interface subsystems, generates a cursor bit for the various keyboard inputs, checks parity for the write and read operations, and reads the contents of the memory to the digital-video-generator subsystems.

The interface and digital-video-generator subsystems are serviced by the input-output programmer on a priority basis, top priority usually being given to the *read* operation. If a parity error is detected during a *write* operation, the memory contents remain unchanged and a parity error signal is generated; if a parity error is detected during a *read* operation, the data are rejected before reaching the digital video generator.

Interface Subsystems

The interface subsystems are basically the same for all sources of data, since they can handle data input rates ranging from zero to 100,000 codes per second. Each interface subsystem has an internal shift register which is set or shifted to the memory address (location designation) of an intended character change; these registers make it possible for the input-output-programmer system to service many associated equipments on a time-shared basis. Each interface subsystem normally receives seven-bit parallel codes from the data source, together with a strobe (or sample data) pulse which indicates that the subsystem is to sample the input data bus and load the data register. In the data register, the code is subjected to a series of logical tests, the first of which is the check for an odd number of *1*'s. If an even number of *1*'s is present, a *repeat* signal is sent back to the data source. The code is then identified. If it represents *start of message, end of message, line feed, carriage return,* etc., the appropriate display control function is generated. If the code corresponds to a valid character, a *write* flag is set, the programmer circuit sees the flag and writes the data word into the memory during the next available *write* time. After the write-in cycle, a demand signal is generated and the internal address register is shifted by one, ready for the next code entry. The *demand* signal indicates to the data source that the DIVCON System is ready to accept the next code.

Memory Subsystem

The memory subsystem is a standard core-storage unit consisting of a core assembly and the circuits required to operate it in the coincident-current mode. It has one register for information words and one for address words; all data written into or read from memory by the input-output programmer subsystem pass through the information register, while the address register holds the location designation sent by the input-output programmer subsystem for each *write* or *read* operation. Program control inputs (*read* or *write* commands) from the input-output programmer subsystem initiate each memory cycle.

Timing-and-Control Subsystem

The timing-and-control subsystem, which synchronizes the DIVCON logic with the television scan periods, consists basically of an X-position counter and a Y-position counter. The X-position counter counts up to 512 dots (64 character positions of 8 dots each) across the TV monitor screen at speeds up to 10 Mc/s. It is driven by a clock which is synchronized with the TV horizontal drive pulse and begins counting at the beginning of a scan line. The Y-position counter counts up to 262 scan lines per display field and begins counting at the leading edge of the TV vertical drive pulse. This subsystem also contains *nand-nor* logic which reduces the X-Y counter signals to line-buffer drive signals for the digital-video-generator subsystems, timing signals for the input-output programmer subsystem, and character-generating signals for the digital video generators.

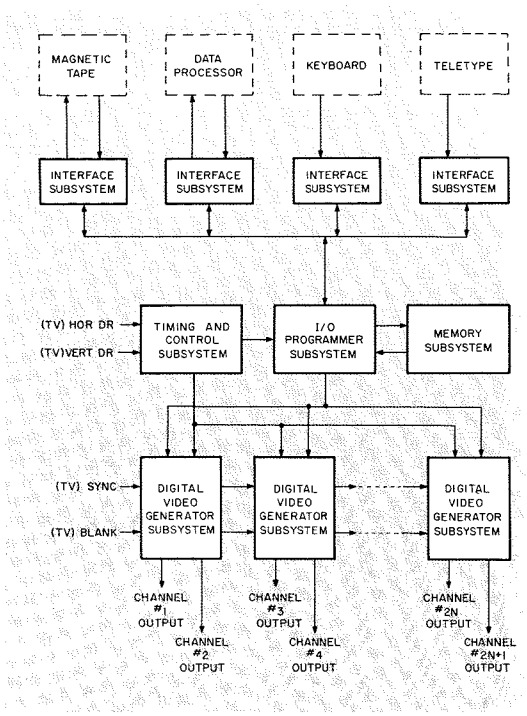


Fig. 2—DIVCON system block diagram.

Digital-Video-Generator Subsystem

Each digital-video-generator subsystem consists of a line buffer and digital-to-video translation logic. Characters are generated on the display screen a full row at a time; the first scan line in the row draws in the tops of all the characters, and the remaining portions are drawn in as the scan-line moves down the monitor screen. Data from the memory subsystem are written one line at a

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time into the line buffer for each channel and, when the buffer is full, it is nondestructively read, character by character, to the associated digital-to-video translating logic; the line buffer is read completely during each of the television scan lines. Data are written into, and read from, the buffer locations in response to coincident control signals from the timer-and-control subsystem.

The digital-to-video translating logic receives information from the line buffer in eight-bit parallel code, one character at a time. Each code is held in a register and is sampled by a decoder which identifies the character code. The resulting *identifier* signal from the decoder feeds through a fan-out (diode) matrix to a series of *nand* gates, where it is *nand*ed with *Y-segment* generating signals. The resulting *identifier—Y-segment* signals are fed through a second fan-out (diode) matrix to a second series of *nand* gates, where they are *nand*ed with *X-segment* generating signals to give digital video in accordance with the simple expression:

$$(identifier) \cdot (Y\text{-}segment) \cdot (X\text{-}segment) = (digital\ video)$$

In the video-amplifier stage, the digital video is mixed with TV blanking and sync signals to give composite video output.

Timing

The input-output-programmer operation is tied to the TV scanning periods by the timer-and-control subsystem; odd-channel digital-video-generator subsystems are serviced by the input-output programmer during even-channel display periods and vice versa, while the interface subsystems are serviced during periods when none of the digital-video-generator subsystems require data from the memory. If the DIVCON system is connected directly (memory-to-memory) to a high-speed input device (up to 500,000 codes per second), the input-output programmer gives top priority to the write-in operation.

The timer-and-control subsystem also ties the operation of the digital-video-generator subsystems to the TV scanning periods. Character codes are read from the line buffer to the translating logic in synchronism with the TV raster scan rate, and the *X-Y* character-generating signals are derived from counters synchronized to the TV horizontal and vertical drive pulses.

The operation of the interface subsystem is asynchronous. The data input cycle is started by a strobe (on sample data) pulse from the data source, following which the data code is put into a register and subjected to a series of logical tests. If a parity error is discovered, a signal is generated within 2 μs of the strobe leading edge. If the code corresponds to a display control function, that function is performed within 10 μs of the strobe leading edge. A valid character code causes a priority flag to be set for the input-output programmer. On completion of a write-in cycle, a demand signal is sent back to the data source.

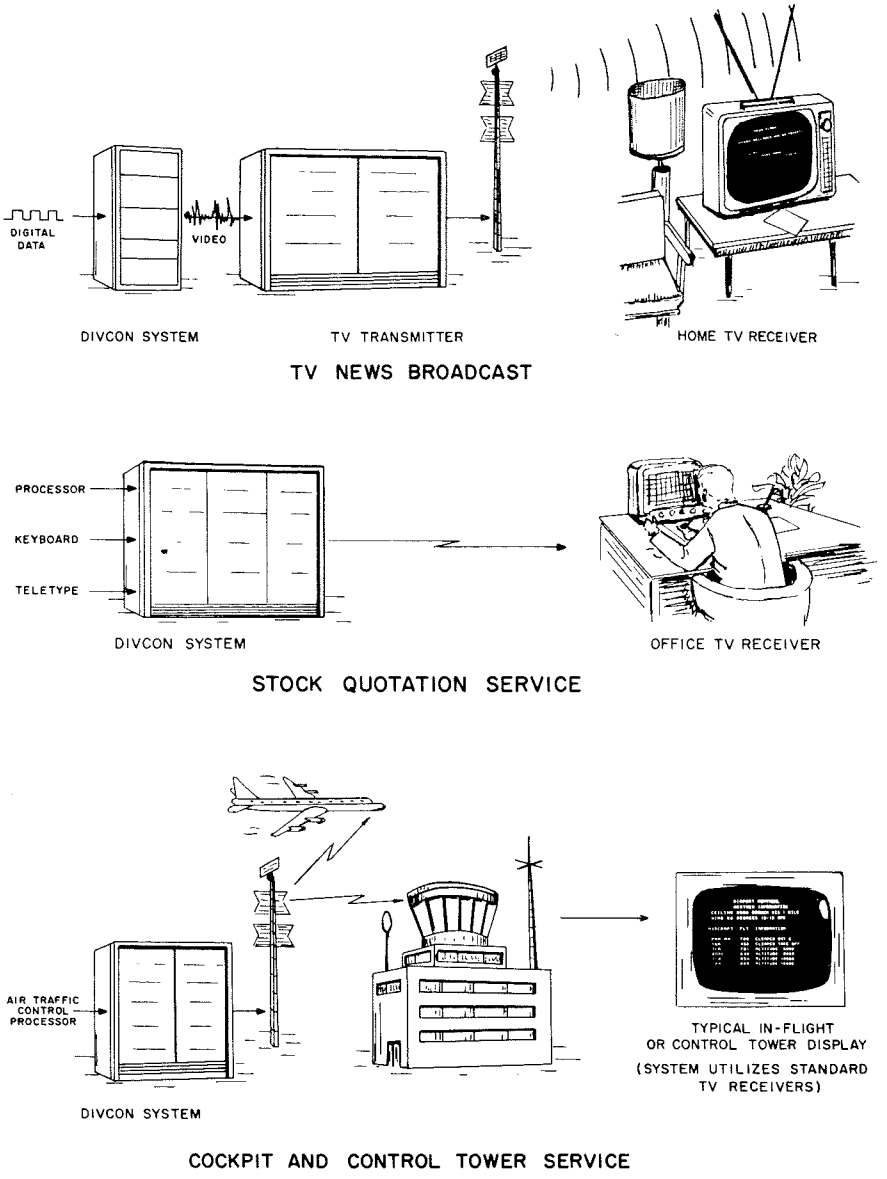

Fig. 3—Typical DIVCON applications.

HARDWARE

Solid-state circuitry is used throughout the DIVCON system. At present, printed-circuit board modules are employed; future systems will incorporate integrated circuits. The basic logic element is a two-input *nand* gate. Approximately 80% of the system is built of two basic board types; this simplifies fault-finding and minimizes the number of spare boards held for maintenance purposes. All logic circuits are worst-case design, using silicon components wherever possible.

APPLICATIONS

The flexibility of the DIVCON concept permits the building of systems for a very wide range of data display applications, some of which are shown in Fig. 3. They include:

1) instantaneous, direct superimposition of news flashes, latest scores, etc., on TV programs;
2) instantaneous displays of stockmarket quotations from local or world-wide sources;
3) passenger-information announcements at airports;
4) flight-path control and weather information in aircraft;
5) racetracks;
6) warehouse control;
7) data retrieval for, auto parts depots, banking and insurance houses, medical offices, and law offices.

COMPUTER ANALYSIS OF SATELLITE THERMAL BEHAVIOR

The computation and prediction of spacecraft thermal behavior is necessary to assure successful equipment operation. Mission parameters governing spacecraft thermal characteristics, such as those described in this paper, are evaluated by digital-computer analysis. Various AED digital-computer programs, their results and some possible future additions are described herein.

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To insure the success of a space mission, a number of complex design problems must be resolved before construction of the vehicle begins. One such problem, vital in spacecraft design, is the accurate prediction of temperatures to which the spacecraft components will be subjected during flight. For example, standard spacecraft batteries require a temperature range from 10°C to 30°C. Deviations beyond this range for extended periods of time will cause failure of the battery system. Spacecraft vidicons require a thermal environment from 5°C to 25°C. Other components, such as precision clocks and infrared detectors, have equally stringent thermal constraints.

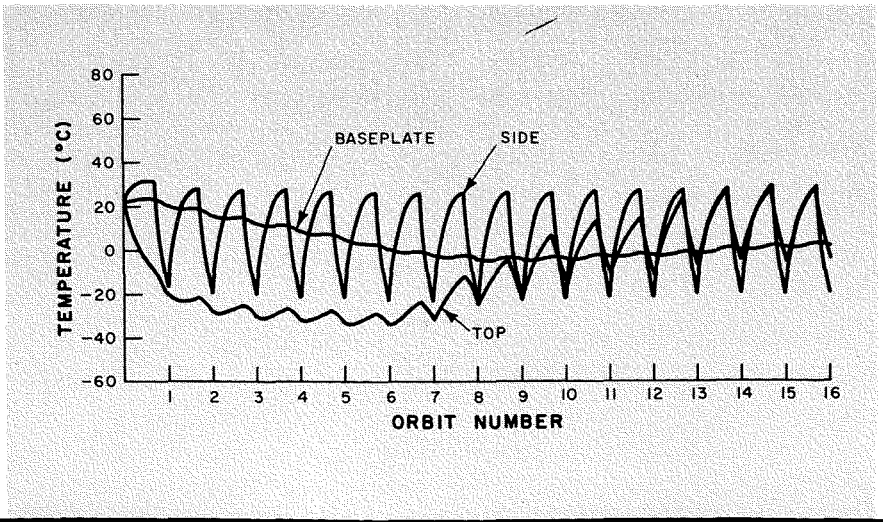
The widely varying thermal requirements of components, and the integration of these components in a small spacecraft (of perhaps 3-foot diameter), make for severe, total-system, thermal constraints. In larger, manned spacecraft, the need for accurate thermal analysis is sharpened by man's dependence on components for survival and need for a bearable thermal environment.

The basic factors which govern the thermal characteristics of a spacecraft in flight are the complex mission and design parameters. The mission parameters include the spacecraft position in space, its altitude, and its operational mission plan. The design parameters include the geometric layout of the spacecraft and its major mechanical components, the thermal properties of the spacecraft, and the heat dissipation of the spacecraft electronic systems. Since 1959, a continuous effort has been made at the Astro-Electronics Division to develop and use digital-computer thermal analysis programs to support various AED space projects. Throughout this period, the various thermal analysis space programs have been constantly refined and improved as a result of experience with the current space programs, actual spacecraft flight observations, increased complexity of the spacecraft, experimental observations, and general progress in the science of space thermal analysis.

Achieving proper thermal design can involve many types of tradeoff, including: change in solar orientation; change in vehicle shape; modification of duty cycle; addition of heaters and/or cooling louvers; change of coating materials; and change of internal geometry of spacecraft. Unfortunately, the majority of these degrees of design freedom are used for tradeoff in optimizing other conditions — weight, size, and vehicle stability. Often, in actual practice the only unique degree of freedom in thermal design is the type of coating.

Final manuscript received July 20, 1965.

Fig. 1—Computer-generated thermal output of TIROS wheel satellite during altitude maneuvering.



GENERAL CONSIDERATIONS

The temperature of any system or subsystem in flight, although complicated by the factors previously mentioned, can be determined by the solution of a set of simultaneous differential equations. However, the solution of such equations is further complicated because heat transfer occurs simultaneously by radiation and conduction.

Because the design of a spacecraft will vary depending upon its ultimate mission, the overall requirements for temperature calculations will change from spacecraft to spacecraft. To provide the flexibility needed to meet the different spacecraft requirements, and to achieve greater accuracy in temperature calculations, the spacecraft system is divided into a number of separate areas (bodies), each of which can be assumed to be isothermal. For example, Fig. 1 shows the computer-generated output of a preliminary system thermal analysis of the top, sides, and baseplate of the TIROS wheel (designed and built by the Astro-Electronics Division of RCA for NASA under contract NAS5-3173) during the initial attitude-maneuvering phase. The purpose of this particular study was to determine if the temperatures encountered during this phase would cause any decrease in power-supply capability.

The following differential equation is used to determine the rate of change of temperature of a specific body (T_i) in a system of n bodies. (In all expressions used in this article, subscript i shall indicate a particular body, and subscript j shall indicate each other body, in turn, affecting the thermal behavior of body i.) (1)

$$\frac{dT_i}{dt} = \frac{1}{W_i C_i}\left[A_i(t) + B_i(t) + C_i(t) + D_i(t) - \sigma \sum_{j=1}^{n} R_{ij}\,(T_i - T_j) - \sum_{j=1}^{n} K_{ij}\,(T_i - T_j) - \varepsilon_i A_{ij}\,\sigma T_i^4\right]$$

where K_{ij} is the conductive coupling between bodies i and j; R_{ij} is the radiative coupling between bodies i and j; ε_i is the emissivity of body i; $A_i(t)$ is the reflected thermal input, from a central body such as the Earth or Moon, that is absorbed by body i; $B_i(t)$ is the direct solar input that is absorbed by body i; $C_i(t)$ is the infrared energy,

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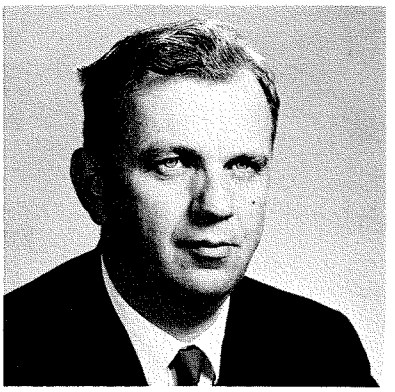

from a central planetary body, that is absorbed by body i; $D_i(t)$ is the internal heat generated by body i; W_i is the weight of body i; C_i is the specific heat of body i; and σ is the Stefan-Boltzmann constant.

To solve Eq. 1 requires:

1) Calculation of absorptivity and emissivity from spectrometry data;
2) Calculation of albedo (ρ) and planetary radiation (μ) as functions of flight parameters;
3) Calculation of the solar radiation absorbed by each body as a function of position, attitude, design geometry, and surface property characteristic;
4) Calculation of the percentage of energy radiated from body i to body j (configuration factors) as a function of spacecraft geometry;
5) Calculation of radiative coupling factors as a function of configuration factors, emissivity, and surface area; and
6) Calculation of temperatures (T_i) by solution of Eq. 1.

DIGITAL COMPUTER PROGRAMS

The AED digital computer programs for spacecraft thermal analysis (Fig. 2) are those required to solve the calculations listed above.

The computational effort required for thermal analysis will vary for different space projects in terms of the required degree of accuracy as well as the complexity of the actual spacecraft design. To meet these various requirements many of these programs have optional uses or features. A brief description of the major programs follows.

Solar Absorptivity and Emissivity Program

Both the solar absorptivity (α) and the emissivity (ε) of materials are determined by spectrometer testing. The spectrometry data is used in the absorptivity and emissivity program to compute the percent of total solar energy absorbed, and the total emittance of a body at given temperatures. This program can be used in either the alpha or the epsilon mode with certain common processing:

1) Standard samples are read in for fixed wavelengths together with the standard tables of solar irradiation [$\omega(\lambda)$].
2) The observed readings are read in as a function of wavelength.
3) The absorptivity or emissivity of the fixed wavelengths for the particular sample [$\alpha(\lambda)$ and $\varepsilon(\lambda)$] is computed by simple algebraic relationships between the table of standard readings and the observed readings of the general form:

$$F(\lambda) = 1.0 - \left[\frac{Sample\ (\lambda)}{Standard\ (\lambda)}\right]^n \cdot \sigma\ Standard\ (\lambda) \qquad (2)$$

The observed data at the fixed wavelengths is found by interpolation.

4) The final required output is found by:

Absorption:

$$\alpha(s) = \int_{\lambda}^{\lambda_n} \frac{\alpha(\lambda)\ \omega(\lambda)\ d\lambda}{\int_{\lambda}^{\lambda} \omega(\lambda)\ d\lambda} \qquad (3)$$

Emittance: At temperature T, the total emittance, $\varepsilon(t)$, is the average emissivity at all wavelengths at temperature T.

Output available from the program consists of $\alpha(s)$ $\varepsilon(t)$ as well as plots of $\alpha(\lambda)$ $\varepsilon(\lambda)$ as a function of wavelength.

Albedo and Infrared Program

A significant amount of heat is absorbed by the external surface of a spacecraft that is relatively close to a central planetary body such as the Moon or the Earth. This heat is the result of solar energy reflected by the planetary body (albedo) and heat emitted by the planetary body (infrared radiation) due to its own temperature. The albedo program is used to compute this reflected heat as a function of flight parameters and planetary characteristics. Two optional uses of the program exist: *1)* for satellite programs, the albedo and infrared radiation is computed for a complete orbit as a function of classical orbital parameters such as height at perigee, height at apogee, and radius of the planet; and *2)* for space probes and landing vehicles, the albedo and infrared radiation is computed at one point of a flyby course, or descent pattern, using a single set of position coordinates. The following is a brief outline

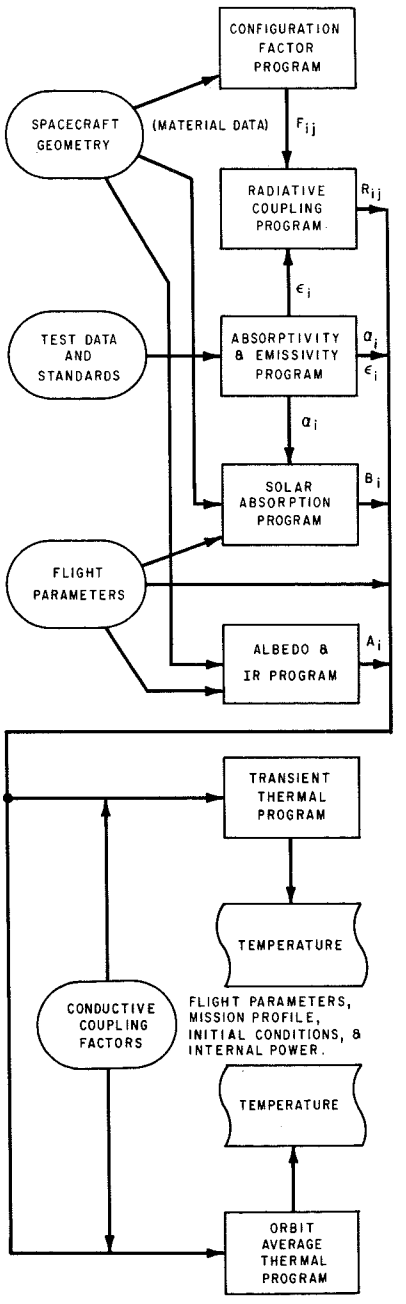

Fig. 2—Organization and data flow for thermal-analysis programs.

of the computational steps involved in the first case:

1) The eccentricity and period of the orbit are computed;
2) The percent of time in the Sun and the true anomalies of the entrance and exit into shadow are computed;
3) The satellite position and attitude vectors at time t are computed;
4) The possibility of a thermal interchange between the satellite surface and the planetary body is determined;
5) The Sun vector is computed if a thermal interchange is possible;
6) The portion of the planetary body visible to the satellite is divided into a network, and the normal and the area are calculated for each point;
7) The configuration factor (F_i), between each point and the surface i, is computed; and
8) The albedo (ρ_i) and infrared radiation (μ_i) are computed.

This program is accurate for most spacecraft which are either cylindrically shaped or which flow smoothly without any protruding surfaces. Certain spacecraft, however, have protruding surfaces, such as radar antennas, which effectively shield the external surface from the planetary body. A revised version of the albedo program is currently being developed which will automatically make allowances for interference of surface view by computing configuration factors. Input data to this version of the program will also include surface array effects.

Solar Absorption Program

One of the principal sources of thermal inputs to a spacecraft is solar energy. This program computes the total solar power absorbed by each surface of a system of planar convex polygons both directly and indirectly. A brief outline of the calculations and computer operations is as follows:

1) The vertices (P_{ij}'s), of every surface are read, and the area (A_i) and unit vector ($\overline{n}_i$) computed;
2) A unit Sun vector is determined either by direct read-in or by rotation of an initial Sun vector;
3) The solar absorptivity (α) of each surface, the solar constant, and the minimum power density are read in;
4) The directly illuminated portion of each surface (A_i*) is computed;
5) The direct solar irradiation of each surface is computed;
6) The direct solar power absorbed by each surface is computed;
7) The direct solar power reflected from each surface is computed;
8) A unit vector ($\overline{S}$) in the direction of the reflected power (R_i) from each surface and other surfaces is examined for reception of this reflected power;
9) The image of A_i* is projected into the plane of each other surface (A_k) under the parallel projection defined by $\overline{S}_i$ and A_{ik}, and the area common to A_k and the resultant image of A_i* is calculated;
10) Each A_{ik}* is processed for shadow with other bodies and A_{ik}, and the area not shadowed is computed;
11) After all surfaces and subsurfaces have been processed, the following total quantities per surface are computed and printed:
    a) total direct solar energy received;
    b) total direct solar energy absorbed;
    c) total direct solar energy reflected;
    d) total indirect solar energy received;
    e) total indirect solar energy reflected; and
    f) power density.

Configuration Factor Program

This program is used to compute the radiative configuration factor between various bodies within a spacecraft, making necessary allowance for intervention of other surfaces. The following is a brief outline of the computation procedure:

1) Geometric data, in terms of vertices for each surface, together with control data provide the input for this program.
2) The surface areas (A_i) and the unit vector normal to each surface ($\overline{n}_i$) are computed.
3) Pairs of surfaces A_i and A_k are tested for possible thermal interchange;
4) All possible intervening surfaces between pairs of A_i and A_k defined by those other surfaces intersecting the dihedral wedge (produced by the intersection of the planes of A_i and A_k) are determined.
5) The configuration factor F_{ij} is determined for each pair of surfaces for which interchange is possible by the method of contour integration. During this process, each element of area (dA) is tested for all possible interventions, and the configuration factors of the individual surface are computed, providing for partial interventions.
6) The following information is then printed out for each pair of surfaces (i and j):
    a) a statement if interchange is not possible;
    b) list of all intervening surfaces;
    c) area of surface i;
    d) area of surface j;
    e) configuration factor from surface i to j; and
    f) configuration factor from surface j to i.

Radiative Coupling-Factor Program

The function of this program is to compute the radiative coupling factors (R_{ij}) between bodies i and j of spacecraft. Input data to the program consists of a symmetric matrix of configuration factors (F_{ij}) and the emissivity (ε_i) of each surface. This can be expressed in the form of a matrix with ε_i on the diagonal, and all nondiagonal elements equal to zero. In this form, the R-matrix, which contains all of the radiative coupling factors (R_{ij}), is computed by

$$R = \varepsilon[I - F + F\varepsilon]^{-1} F\varepsilon \qquad (4)$$

TEMPERATURE PROGRAMS

Depending upon the mission requirements, in terms of flight parameters and accuracy, one of the following standard programs is used for the actual determination of temperature.

Transient Thermal Program

This program is a flexible and accurate method for determining temperatures by the actual numerical integration of Eq. 1. With

$$A_i(t) = \Gamma\rho_i(t)\alpha_i A_{i11} \qquad (5)$$

where $\Gamma = 1$ if the spacecraft is in the Sun, or $\Gamma = 0$ if the spacecraft is in the shadow of the central planetary body, $\rho_i(t)$ is the effect of albedo on body i, α_i is the absorptivity of body i, and A_{i11} is the area of body i receiving albedo.

$$B_i(t) = \Gamma C(\alpha_i - N_i)\, A_{i12} \cos\theta_i(t) \qquad (6)$$

where C is the solar constant, N_i is the solar-cell efficiency of exterior bodies if applicable, A_{i12} is the projected area of body i receiving albedo, and $\theta_i(t)$ is the angle between body i and the vector.

$$C_i(t) = \mu_i(t)\,\varepsilon_i A_{i13} \qquad (7)$$

where $\mu_i(t)$ is the effect of infrared radiation from the planetary body on body i, ε_i is the emissivity of body i, and A_{i13} is the area of body i receiving infrared radiation from the planetary body.

$$D_i(t) = \textit{the internal heat generated by body } i. \qquad (8)$$

To provide this program with greater flexibility in the solution of common thermal-design problems, the following optional features are provided.

1) Different integration steps can be used for the calculation of daytime and nighttime thermal behavior, and integration is automatically carried exactly to the start and end of daytime flight.
2) Representation of $\mu_i(t)$, $p_i(t)$, $Q_j(t)$, and $\theta_i(t)$. These variables can be submitted in any of the following forms: *a)* as a tabulated function of time throughout the entire simulation; *b)* as a repetitive tabulated function (of time through an orbit) which is automatically repeated for successive orbits; or *c)* as a time-independent quantity.
3) Computation may be terminated under either of the following conditions: *a)* a preset time is reached; or *b)* steady-state condition (that condition when all temperatures at the end of one sunlit portion of one orbit equal the temperatures at the end of the sunlit portion of the following orbit to a prescribed tolerance) is reached.
4) A graphical output of temperature versus time is available either for the entire time or for the time of the steady-state orbit.

Although the control logic and data representation is designed to provide a high degree of flexibility for orbital thermodynamics, Eqs. 1, 5, 6, 7, and 8 are themselves completely general. Therefore, by the selection of proper options and control parameters, this program is successful in simulating the thermal behavior of an interplanetary probe.

Average Temperature Program

Over a period of time during which flight parameters are relatively constant or repetitive, average temperatures can be computed by the following iterative program. Input data consists of:

1) An initial estimate of the temperature (T_{ik}) of body i;
2) The maximum error (δ) allowable in the final temperature;
3) The equivalent heat flux (I_s), that represents the external environmental flux absorbed;
4) K_{ij}, R_{ij}, and σ as defined in Eq. 1; and
5) The radiative coupling (R_{is}) between body i and surface s.

To compute the average temperature, matrix A is represented by A_{ij}, and an element of the matrix is represented by a_{ij}. The matrix A_{ij} is generated by:

$$a_{ij} = -\left[R_{ij} + \frac{K_{ij}}{\sigma(T_i^2 + T_j^2)(T_i + T_j)}\right] \qquad i \neq j \tag{9}$$

$$A_{ii} = \sum_j a_{ij} + \sum_s R_{is} \qquad i = j \tag{10}$$

Then the following matrix operations are performed:

$$B_{ij} = A_{ij}^{-1} \tag{11}$$

$$C_{is} = B_{ij}R_{js} \tag{12}$$

$$D_i = B_{ij}Q_j \tag{13}$$

$$E_i = D_i + C_{is}T_s \tag{14}$$

The next approximation of temperature ($T_{i,k+1}$) is computed by

$$T_{i,k+1} = \left[\frac{E_i}{\sigma}\right]^{\frac{1}{4}} \tag{15}$$

Eqs. 9 through 15 are repeated with the improved values of T_i until all temperatures agree with previously computed temperatures to a specified tolerance, or until a specified number of iterations have been made. The primary output resulting from these computations consists of the final temperatures T_i.

TABLE I—Milestones in the Development of Computer Programs for Spacecraft Thermal Analysis

Date	Program	Accomplishment
1959	Prototype thermal analysis, limited to 3 bodies (top, bottom, and sides)	*Checked out.*
1960	Prototype albedo, limited to Earth orbits	*Written and checked out.*
	TIROS I temperatures	*Predicted, and substantiated by flight data.*
1961	Prototype average orbit temperature, neglecting conduction	*Written, and used to predict temperatures on* TIROS II.
1962	Prototype configuration factor	*Written.*
	Generalized transient thermal	*Written and checked out.*
1963	Operational configuration	*Written and checked out.*
	Solar absorption	*Written and checked out.*
	Prototype absorptivity and emissivity	*Written and checked out.*
	Operational average orbit temperature	*Written and checked out.*
	Radiative coupling, considering specular reflection	*Written and checked out.*
1964	Transient thermal analysis	*Modified to: 1) increase capability from 75 bodies to 140; 2) provide graphical output; and 3) provide more flexible representation of flight parameters.*
	Operational albedo programs for closed spacecraft	*Completed.*
	Radiative coupling factor program for considering diffuse reflection	*Developed.*
	Operational absorptivity and emissivity	*Checked out.*
	Albedo, for spacecraft with protruding surfaces	*Started.*
	Prediction of temperatures on Ranger VII	*Maximum deviation of 3°C between computer-predicted and telemetered temperatures during the entire lunar flight.*

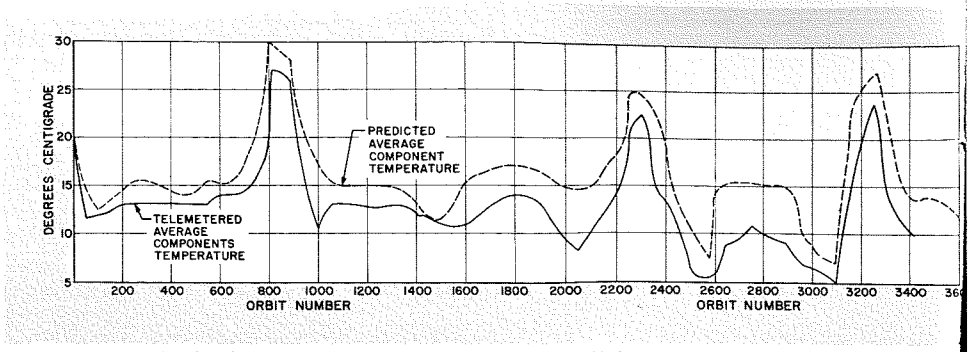

Fig. 3—Comparison of computer-predicted and flight temperatures for TIROS II.

HISTORICAL DEVELOPMENT OF THE PROGRAMS

As stated previously, the development of the AED library of programs for spacecraft thermal-analysis has been a continuous effort since 1959. Generally, this growth pattern has consisted of the analysis and programming of a preliminary or prototype model to meet the specific needs of a project, followed by reanalysis and rework based upon study of the computer results, and comparison to the observed spacecraft thermal behavior. Table I presents a chronological review of this development.

The AED library of programs for spacecraft thermal analysis is not restricted to a particular type of spacecraft. The programs have contributed significantly to AED's engineering on such spacecraft as TIROS, RELAY, NIMBUS, LUNAR ORBITER, RANGER, SERT and LEM. The validity of the mathematical models and computer programs has been shown by postflight comparisons of computer-predicted temperature profiles with observed flight data from the TIROS, RELAY, and RANGER flights; RANGER VII, for example, had a maximum deviation of 3°C throughout the entire lunar flight.

Fig. 3 shows a comparison of computer prediction of temperatures on the TIROS II vehicle with actual telemetry average component temperature. As can be expected, maximum temperatures were achieved during periods of 100% Sun time, when solar and albedo temperatures are at a maximum.

For many bodies or nodes, manual calculation of temperatures is clearly not feasible due to the complexity of Eq. 1 and to the complexity in determining albedo, infrared, and solar energy. A comparison of response time was made for calculation of temperatures via the orbit average method for a ten-body system by manual versus computer methods. Response time for the manual effort was one week; for the computer effort, one day.

CONCLUSION

The computer system outlined in this paper has proved useful in AED thermal design. Additions to this system are being considered. These include: modification for radioisotope generator systems; inclusion of ablation effects; and computer program integration of this thermal system with the AED computer program for power-supply simulation.

ACKNOWLEDGEMENT

These computer programs were the product of a joint effort, by the computations group and by the thermal design group. Significant contributors were: L. Ciabattoni, L. R. Miller, and R. A. Velosky, of the computations group; and W. Bernard, R. R. Laessig, D. Glovach, H. Burgos, and J. R. Owens, Leader, of the thermal design group.

AN/TRC-97/97A

Microwave Multichannel Equipment for Troposcatter, Diffraction, or Line-of-Sight Tactical Communications

AN/TRC-97/97A is the forerunner of a new generation of wideband microwave tactical communications equipment that capitalizes on recent advances in solid-state electronics. It provides full duplex multichannel voice, data, and teletype communications in a 4,400-to-5,000-Mc/s band using line-of-sight, diffraction, or tropospheric-scatter media. A complete communication system, including dual space diversity receivers, exciters, 1-kW power amplifier, multiplex, and monitoring equipment, is housed in an S-308 shelter designed to be transported by the standard M-37 3/4-ton field truck or by helicopter or conventional aircraft. The equipment is especially designed for quick-reaction tactical use, in which tropospheric scatter communications can be established in less than one hour after arriving at the sites. AN/TRC-97/97A is the most modern wideband military communications equipment in existence today. The transmitter is all solid-state, except for the exciter traveling-wave tube and the 1-kW klystron. The receiver is 100% solid state. Achievements in system design, wideband varactor techniques, broadband UHF high-power amplifiers, threshold extender design, and tunnel-diode microwave amplifiers have opened the tactical communications market to this class of equipment. Intensive development effort was devoted to flexibility for anticipated future requirements. As a result, only minor modifications are required to increase channel capacity and operate in different frequency bands.

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THE increasing need for fluid movement of tactical units requires ready mobility and very rapid installation of multichannel communication facilities. Broadband radio systems have supplemented wire circuits extensively since World War II for this need; however, much was left to be desired. Equipment was generally bulky, cumbersome, consumed excessive fuel, and was difficult to operate in the field. The systems usually required a multiplicity of large vehicles for transportation and thus, while transportable, were hardly suitable for many of today's military tactical operations. But, as solid-state research made available the tunnel diode, varactor, high-power high-frequency transistors, and microwave ferrites, a whole new approach towards equipment design became feasible. This was recognized by the U.S. Marine Corps, and in the summer of 1963 BuShips authorized the RCA Communications Systems Division to develop a new tactical wideband communication system which was to eliminate the problems mentioned above by an optimum integration of the latest state-of-the-art devices and system techniques. The AN/TRC-97 (Fig. 1) is the result of this program.

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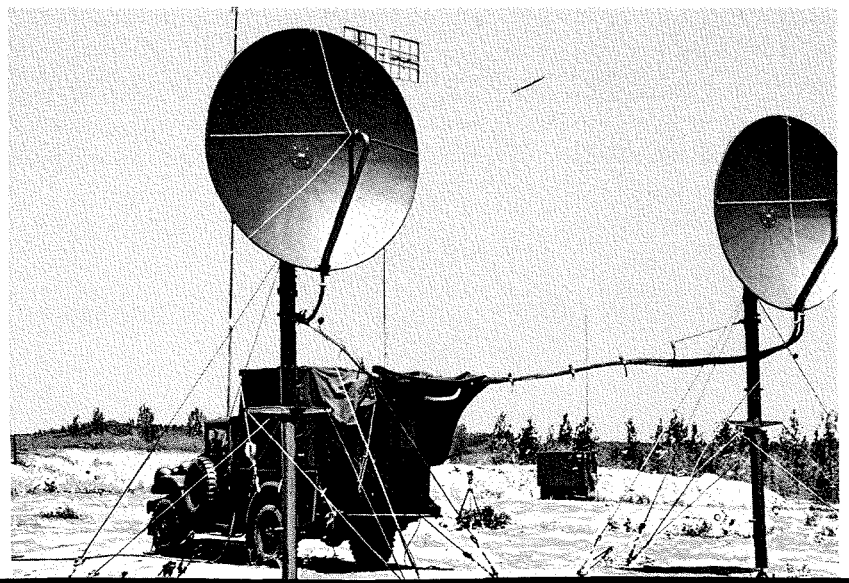


Fig. 1—AN/TRC-97/97A. Two men can assemble and erect the parabolic antennas on-site.

The AN/TRC-97A is a higher channel version of the basic Marine Corps AN/TRC-97, which is being produced for the U.S. Air Force. This equipment contains both twin and inverted sideband multiplex capability for maximum field flexibility.

The development of a system of this type is necessarily quite extensive and a number of new and very interesting circuit designs resulted. Some of these are a very-wideband varactor multiplier chain (13% bandwidth), a phase-locked threshold extender, and tunnel diode RF amplifiers.

SYSTEM DESCRIPTION

The AN/TRC-97 consists of the following major units:

1) 1-kW power amplifier
2) dual receivers
3) exciter
4) multiplex
5) antenna system
6) shelter and trailer assemblies

Fig. 2 depicts the interrelationship of these units, and Figs. 3a and 3b are block diagrams of the radio equipment. The multiplex modulation plan is shown in Fig. 4. The system characteristics are shown in Table I.

In a multichannel communications system, the final criterion of acceptability is the noise performance of the individual voice channels. Such noise arises from many sources—such as radio-equipment front-end thermal noise, intermodulation noise resulting from

TABLE I—System Characteristics

Common to both AN/TRC-97 and -97/A	
Freq. Band	4400-5000 Mc/s
Teletype Chan.	16 in any voice chan.
RF Chan.	1200
Mod.	FM (pre-emph.)
Diversity	Dual space/maximal ratio combiner
Orderwire Resp.	300 c/s to 3 kc/s
RF/IF Bandwidth	1.5 to 20 Mc/s (optional)
Noise Figure	5 dB nom
Output Pwr.	1-W exciter; 1,000 w with P.A.
Freq. Stab.	5 parts in 10^6, long term
Temp.	−40°C to +65°C
Pwr. Req.	208-V, 3-phase, 7-kw, 400 c/s
Shelter Type	S-308
Trailer Type	M-101

	AN/TRC-97	AN/TRC-97A
Voice Chan.	12	24
Mpx. Type	FDM twin SB	FDM-twin & inverted SB
Antennas	2-8 ft. par.	2-8 ft. parab. or 2 horns
Baseband Resp.	12-60 kc/s	12-108 kc/s
Peak Freq. Dev.	±325 kc/s	±375
FM Thresh.	−105 dBm	−102 dBm
Shelter Wt.	1655 lb	1875 lb
Generator	diesel	gas turb.

1-W exciter; 1,000 W

phase nonlinearity, residual circuit noise level, incidental FM modulation, and echo distortion in the antenna system. Increasing the system deviation will improve noise performance if the thermal noise predominates; however, eventually this will cause intermodulation noise to increase unless the bandwidth is made much greater to achieve a constant delay characteristic. This is generally unacceptable in tropospheric scatter systems, however, because a wide bandwidth raises the threshold, which results directly in a lower propagation reliability. In conjunction with the above considerations, additional system restraints were imposed by the very important desirability of being compatible with CCITT and DCA recommendations which specify standards for system engineering such as levels, impedances, modulation rate, frequency and distortion tolerances. The AN/TRC-97 was designed to be compatible with these international standards to assure compatibility with existing and future major systems.

The following sections summarize significant system parameters related to the criteria just discussed.

SYSTEM PERFORMANCE

Fig. 7 shows the overall performance of the AN/TRC-97. All noise sources are included and the curve is based upon dual diversity reception with median received carrier levels. The performance is summarized in Table II for specified conditions. Performance vs. distance is shown in Fig. 5.

FM Deviation

The frequency-division-multiplexed signal during the busy hour can be satisfactorily represented by a uniform spectrum signal (white noise) which, at a point of zero relative level, has a level of $(-1 + 4 \log N)$, where N is the number of traffic channels. With a 0-dBmo test tone yielding a deviation of 50 kc/s-RMS per channel and a peak factor of 13 dB, the resulting system peak deviation is 325 kc/s for 12-voice-channel loading and 375 kc/s for 24 channels.

Noise Improvement Factor

The FM noise improvement factor in the top channel is given (for the non-pre-emphasis situation) by:

$$10 \log\left(\frac{F_d}{F_m}\right)^2 \frac{B}{2b}$$

Where F_d = peak channel deviation, f_m = center frequency of the top voice channel, B = predetection bandwidth, b = voice channel bandwidth.

Pre-emphasis and de-emphasis are used in the AN/TRC-97 to achieve uniform channel performance. Approximately 3 dB of emphasis is applied at the highest baseband frequency and the resulting noise improvement factor is 28 dB.

TABLE II—System Performance

	8-ft Antennas	15-ft Antennas
Median Path Loss, dB	−213	−213
Antenna Gain (2), dB	74.7	84
Feeder Loss, dB	−0.5	−0.5
Median Net Loss, dB	−138.8	−129.5
Median Received Carrier (Ant. Term.), dBW	−108.8	−99.5
Equivalent Noise Input (*ENI*), dBW	−135.9	−135.9
Threshold *CNR*, dB	2	2
FM Threshold, dBW	−133.9	−133.9
Fade Margin (one receiver), dB	26.1	35.4
Predetection *C/N* (one receiver), dB	27.1	36.4
Dual Diversity gain, dB	3	3
NIF, dB	28	28
NPR, dB	50	50
Median *S/N*, dB	55.5	64.5

Performance conditions: path length = 115 miles; traffic channels = 12; transmitter power = 1 kW; modulation index = 5.4.

System Threshold

The noise threshold of FM systems is proportional to the predetection bandwidth which is frequently set by the passband of the IF system. After the signal level reaches the conventional FM threshold, which occurs at about 10 dB above the noise threshold in a conventional receiver, the signal-to-noise ratio deteriorates rapidly for small changes in the input RF signal. The AN/TRC-97, however, uses a phase-locked threshold extender which keeps the output signal-to-noise ratio a linear function of the input-carrier-to-noise ratio and to within 2 dB of the noise threshold. This 8-dB improvement in the usable threshold can be considered as an equivalent noise bandwidth of 234 kc/s for the system.

The threshold extender is basically a phase-locked loop which forces a voltage controlled oscillator (VCO) to follow the carrier excursions, effectively reducing the modulation index to a narrow band signal. The baseband information is recovered by demodulating the excursions of the VCO.

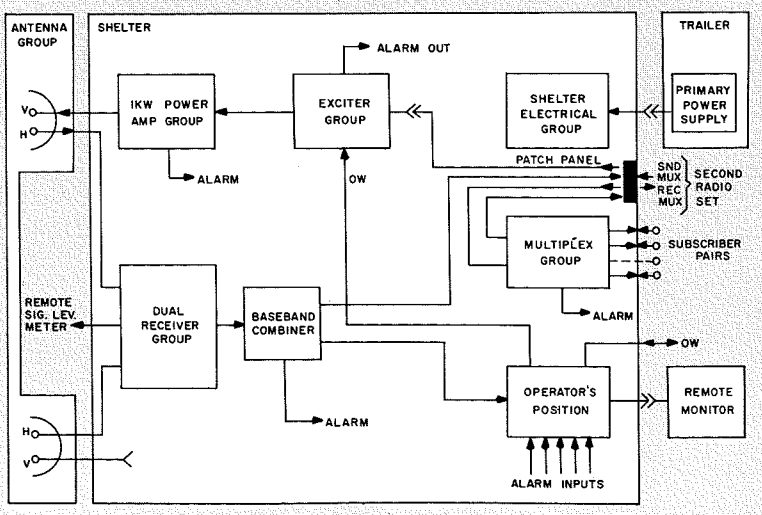
Noise Power Ratio

The noise power ratio (*NPR*) is a measure of the noise due to intermodulation plus the intrinsic circuit noise. The measurement is made at a high received carrier level to ensure that front-end thermal noise does not mask the contribution of these sources. Fig. 6 plots the overall system *NPR* obtained by illuminating the baseband with noise in accordance with CCITT recommendations.

TRANSMITTER

Fig. 3a is a functional block diagram of the transmitter. The baseband amplifier portion of the transmitter consists of the amplifier itself plus input circuitry to accommodate the composite traffic signal from the multiplex or, for a through repeater station, the received baseband signal. Terminations are built in to accommodate the standard spiral-4, 135-ohm cable for the latter type operation. Provisions for accommodating the local order-wire facility, as well as pilot-tone generation, are included. The output of the baseband amplifier serves as the modulating signal for a 70-Mc/s frequency modulated oscillator (FMO). The FMO has actually been designed for 300-channel operation with excellent linearity, in order that any future increase in traffic capacity could be obtained without redesign. An AFC system has been incorporated into the FMO in order that the excellent stability achieved by the synthesizer will not be degraded. The output of the FMO is applied to an amplifier whose output is compatible with DCA and CCITT recommendations, thus enabling hetero-

Fig. 2—System group diagram.



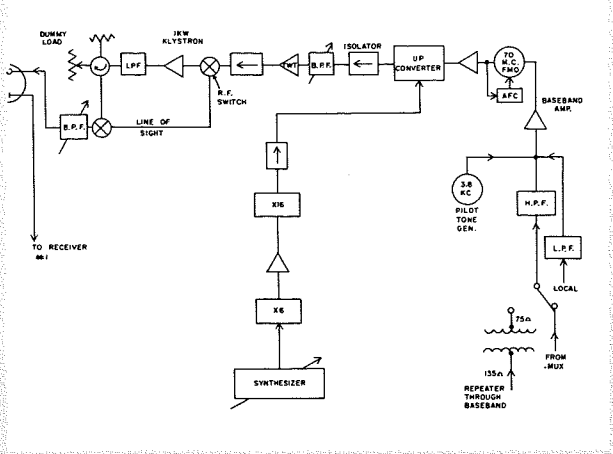


Fig. 3a—Transmitter.

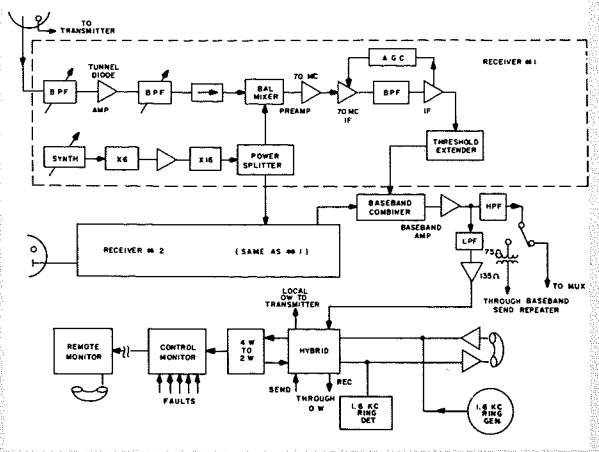


Fig. 3b—Receiver.

dyne repeating with existing communication systems. The signal is then mixed in an upconverter with the RF output of a broad band varactor multiplier chain which translates the frequency synthesizer signals to the microwave region. The upper sideband from this conversion is selected by means of a tuneable bandpass filter and applied to a travelling-wave-tube (TWT) amplifier. The output of the TWT is either applied to a klystron to provide a 1-kW level for tropospheric scatter, or is sent directly to the output bandpass filter for line-of-sight operation at a 1-watt level.

With the exception of the TWT and the 1-kW klystron, the entire transmitter uses solid-state devices. An important operating feature is the ease with which tuning changes can be accomplished. The synthesizer, two bandpass filters, and the klystron are the only elements which need be touched and these are calibrated directly in RF channel numbers. A change in operating frequency can be made in less than 2 minutes.

RECEIVER

Fig. 3b is a simplified functional diagram of the dual-diversity receiver. The receiving system is 100% solid state. The input signals from the antenna pass through a 4-pole microwave filter for RF selectivity and are then amplified in a tunnel-diode amplifier which has a maximum noise figure of 4.4 dB. Since the tunnel-diode amplifier is inherently a broadband device, a second tuneable bandpass filter is used to insure that amplification of thermal noise at an image frequency by the tunnel diode amplifier does not degrade system performance.

The microwave signal is heterodyned in a balanced mixer with a local oscillator signal which is generated in the same manner as that used in the exciter except for the addition of a power splitter used to accommodate receiver No. 2. The varactor chain shown in Fig. 3b has been simplified for clarity; actually, it consists of several lower-order multipliers in cascade. The output of the balanced mixer is sent to the 70-Mc/s IF amplifier whose active stages are broadbanded; selectivity is provided by a passive bandpass filter which can be readily changed to accommodate increased traffic requirements. A phase-locked threshold extender demodulates the signal to the original baseband spectrum. This signal and the one from receiver No. 2 are combined in a maximal ratio baseband combiner. The combiner provides an output-signal-to-noise ratio 3 dB better than that from either receiver alone when the signal-to-noise ratios from each receiver are equal. For unequal signal-to-noise ratios, the combiner provides an output which is never worse than the better of the two signal-to-noise ratios. The baseband system of the receiver is similar to that of the transmitter, except that it operates inversely; it also contains the hybrid circuitry required to perform local order-wire communications and ringing.

A control monitor is provided to display faults in a central location and to transmit order-wire communications and faults to a 17-pound remote-monitor package. The remote monitor is connected to the main shelter by standard field wire, and is operable at distances up to ½ mile from the shelter.

TABLE III—
Multiplex Transmission Parameters

Voice Multiplexer:	
VF Input	+10, 0, −4, −16 dBm
VF Output	−20 to +7 dBm adjustable
HF Line Input/Output	−15 to −30 dBm adjustable
VF Line Impedances	600 ohms ±10% balanced or unbalanced
HF Line Impedances	75, 135 ohms ±10% balanced or unbalanced
Allocation	12 channels, 12 to 60 kc/s 24 channels, 12 to 108 kc/s
Terminations	2 wire or 4 wire
Signaling	In-band (2,600 c/s)
Voice Channel Characteristics (back to back):	
Frequency Resp.	±1 db, 350 to 3450 c/s
Envelope Delay	950-2650 c/s (500 μs) 750-3100 c/s (1,000 μs)
Idle Noise	15 dBa
Loaded Noise	23 dBa
Load Handling	100% data loading at −10 dBmo per channel
Teletype Multiplexer:	
Channel Center Freq.	425-2,975 c/s in 170-c/s increments
Frequency Deviation	42.5 c/s from each center frequency
Total Signal Dist.	Less than 5%
Data Rates	60, 75, and 100 words/min
Impedances	600 ohms ±10%
Input Level	−50 to +6 dBm per channel
Frequency Stab.	±4 c/s

Fig. 4—Multiplex modulation plan for the twin sideband AN/GCC-5 multiplex used in the 12-channel AN/TRC-97.

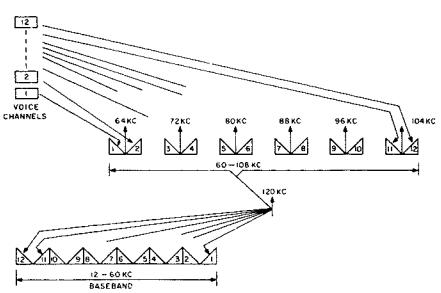
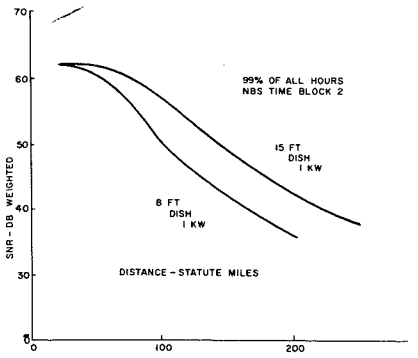
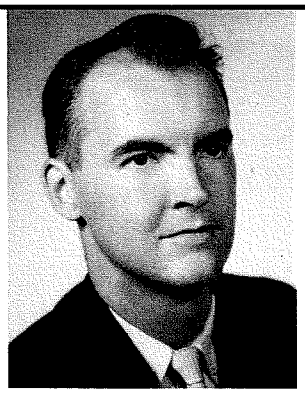
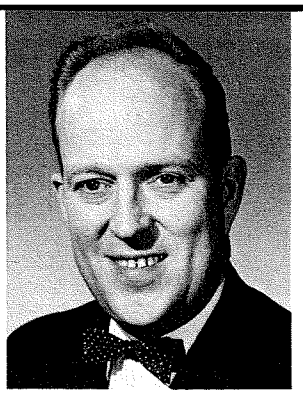


Fig. 5—System median signal-to-noise ratio vs. distance.





W. J. Connor



E. J. Sass

W. J. CONNOR received the BSEE from Worcester Polytechnic Institute in 1952. He joined RCA the same year, and has since worked on military communications (cable and radio). In 1958, he was named Engineering Leader on the AN/GRC-50 Radio Relay program and later was in charge of a group determining system criteria for wideband communications on the 480-L program. He became an Engineering Manager in 1961, responsible for MINUTEMAN communications transmission equipment, and application of advanced techniques to tropospheric scatter systems. He is presently Manager of radio relay and tropospheric scatter equipment. He has published several papers on communications, and is a Member of the IEEE, of the IEEE Group on Communication Systems, and of the Armed Forces Communications and Electronics Association.

EARL J. SASS received his BSEE in 1945 from the University of Nebraska; and his MSEE in 1954 from the University of Pennsylvania. He joined RCA in 1945, and worked on RF and IF coils and transformers and the first RCA printed circuit television tuner. He transferred to the Home Instruments Division in 1951, and was responsible for product design of picture and sound IF amplifiers for RCA's first commercial color television receivers. In 1957, he supervised much of the design of commercial color television receivers and remote control receivers. He transferred to CSD in 1961, where he was responsible for the design 1) of the ground receiving equipment for the DYNA-SOAR Project and 2) a part of the GRC and 744 project. In 1963 he was responsible for the design and development of the AN/TRC-97 exciter, receiver, and shelter. At present, he is Group Leader in charge of the development and design of a tactical frequency division multiplexer. Mr. Sass holds U.S. Patents and is a member of Sigma Tau and Pi Mu Epsilon.

MULTIPLEXER

The AN/GCC-5 multiplexer provides two functions: 1) the stacking of 12 telephone-quality voice channels in the spectrum from 12 to 60 kc/s by frequency-division multiplexing, and 2) the stacking of 16 teletype channels in a spectrum suitable for transmission through one of the voice channels by frequency multiplexing.

The voice multiplexer consists of a 12-channel multiplex bank, a 12-channel demultiplex bank, a group modulator-demodulator (to convert the channel bank frequencies to the desired line frequencies), a channel terminals, a signaling converter, a carrier generator, a test set, and the power supply and alarm circuits. The teletype multiplexer consists of a 16-channel *transmit* keyer group and a sixteen channel *receive* converter group. The voice-frequency teletype terminal is included to provide compatibility with the TH-5/TG Telegraph Terminal.

The stacking plan of the voice multiplexer consists of modulating each of 12 voice channels into 4-kc/s increments in the frequency spectrum between 60 and 108 kc/s, and then translating to the 12-to-60-kc/s spectrum (used for transmission through the radio link).

The teletype multiplexer makes use of standard 16-channel stacking across the voice spectrum at 170-c/s increments. Frequency-shift keying is used wherein the carrier is shifted ±42.5 c/s depending of whether the transmission is a *mark* or *space*. The composite 16-channel teletype signal is inserted into a single voice channel for transmission through the voice multiplexer and then over the radio link. The multiplex modulation plan is shown in Fig. 4 and the transmission characteristics of the multiplex are listed in Table III.

ANTENNA SYSTEM

The basic antenna system (Table IV and Fig. 1) has two 8-foot parabolic reflectors with polarized waveguide feeders, flexible waveguide transmission line, mast and supporting structures. A 15-foot antenna is also available for use on longer paths.

The reflector consists of aluminum skin with radial supporting ribs and a formed aluminum tube providing support and stiffness at the outer circumference. The feedhorn and waveguide are constructed of aluminum alloy to reduce weight. The antennas are assembled and attached to mast on the ground, and the system is then erected by means of a winch and cable. The entire set-up, including antenna alignment can be accomplished in approximately 40 minutes. For tactical operations in heavily wooded areas, a wider-beamwidth and lower-gain horn antenna mounted on a 50-foot tower is provided.

MECHANICAL DESIGN

The basic radio terminal is completely housed in an S-308 tactical shelter, having inside dimensions of 72 inches in length, 70.5 inches in width, and 66.5 inches in height.

Fig. 8 shows the S-308 shelter layout and some of the functional units. This equipment configuration represents the optimum arrangement consistent with ease of operation, adequate amount of personnel space, sufficient maintenance space, simplicity of cooling and heating, proper weight distribution, and a minimum number of interconnections. The operator's position within the shelter contains controls and indicators to provide equipment status information. Desk space and a communications handset are provided.

Through the use of lightweight structural members throughout the shelter, rack, and drawers, the shelter with all the radio equipment weighs less than

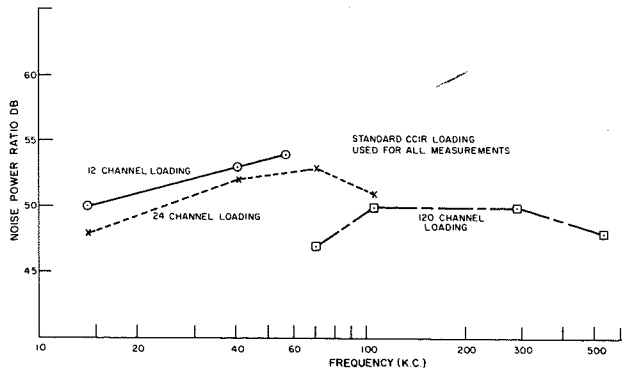


Fig. 6—System noise power ratio. The AN/TRC-97/97A is a wideband system optimized for 12-24 channel operation. The 120-channel measurements were made on a modified AN/TRC-97. The modulator was initially adjusted for 12-channel operation and not changed thereafter.

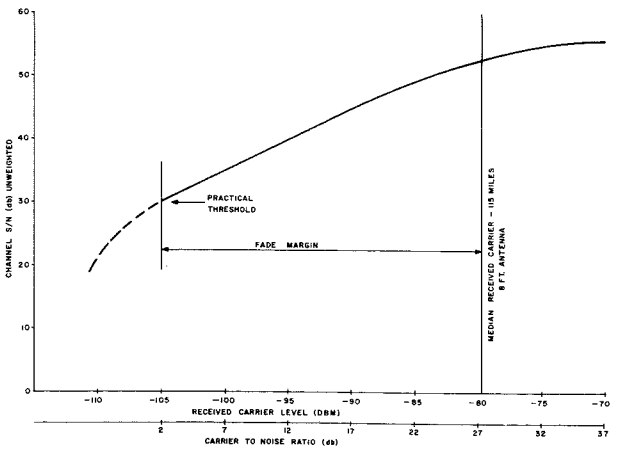


Fig. 7—Overall performance.

TABLE IV—Antenna Characteristics

	8′ Dish	15′ Dish	Horn
Gain, dB	38	44	21
Beamwidth	2°	1°	18°
Tower Height, ft	15	15	50
Segments	4	8	—
Feeder	RG95	RG95	RG95
Feeder Length, ft	30	30	65
Feeder Loss, dB	0.9	0.9	1.9
Azimuth Adj.	±30°	±30°	100°
Elevation Adj.	+10°, −5°	+10°, −5°	±10°
Coupling Loss	0.6 dB for 1° Scatter Angle	2 dB for 1° Scatter Angle	—
Net Gain (1 Ant.), dB	36.5	41.1	19.1

1,700 pounds. It is designed to be transported by the standard M-37 ¾ ton truck, or by any helicopter or conventional aircraft of suitable capacity. The antenna system and primary power source are carried in a standard M-101 ¾ ton trailer.

The equipment racks used in the shelter are of an open frame construction utilizing aluminum alloy as basic structure material. The panel opening is 19 inches by 66.5 inches high, and accepts standard 19-inch-wide panels of varying height. The depth of the racks is 22 inches, except for the power amplifier rack, which is 24 inches deep. The rack is rigidly mounted (shock or vibration isolators are not used) to structural members in the floor of the shelter and to the roof and rear wall of the shelter also. Shock protection for the electronic equipment is provided by the elasticity of the structure itself. The drawers, which are of open-frame construction, are mounted to the racks by pins in the back edges of the front panels and by slide rails. This system prevents bouncing of the chassis during vibration and shock conditions, and transfers the chassis loads directly into the vertical frame.

An important feature of the receiver and exciter equipment is the modular box construction used. Each box represents a complete functional entity which can be interconnected by coaxial cable. The boxes are fastened to the drawers by captivated screw fasteners for easy replacement. Drawer wiring and front panel components are mounted forward of the box section. In the rear of each drawer, retractable flexible cabling simplifies maintenance. Each module box is shielded and bypassed to meet the RFI requirements of MIL-I-16910A on a box basis.

COOLING AND HEATING

Cooling is achieved by circulating ambient air through the equipment and shelter. Air drawn through an inlet is ducted to the klystron tube and out through a duct between the power amplifier rack and the front of the shelter. The heat generated by the equipment is dissipated directly to the outside. For cold weather operation, the heat generated by the power amplifier is used to heat the shelter.

The receivers, multiplexer, and transmitter are grouped together to form a rack complex, and the inlet to this complex is through an intake filter at the bottom of the exciter rack. Dual blowers draw air at a rate of 350 ft³/min through the intake filter to cool the equipment in transmitter and receiver racks. The air is exhausted through a duct at the top of the racks to the rear opening in the shelter.

The power amplifier is cooled by drawing air at a rate of 300 ft³/min through an intake filter located near the bottom of the power amplifier rack on the curb side of the shelter. The heat generated by the power amplifier is exhausted out a grille located in a duct between the power amplifier rack and the front of the shelter and, subsequently, out of a louvered opening in the rear door.

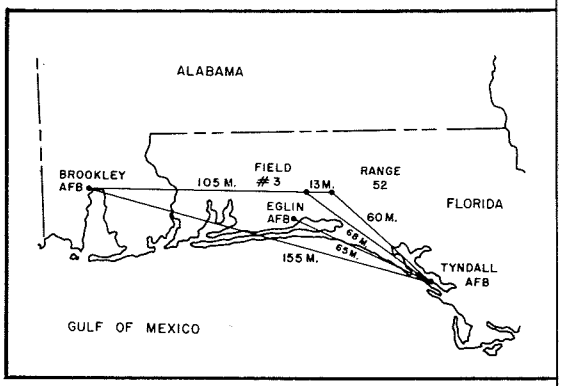


Fig. 9—Operational site locations, Indian River III exercise.

FIELD OPERATION

The first four prototypes of the AN/TRC-97 equipment were used in the Indian River III Exercise conducted at the Air Warfare Center in Eglin, Florida, during late 1964.

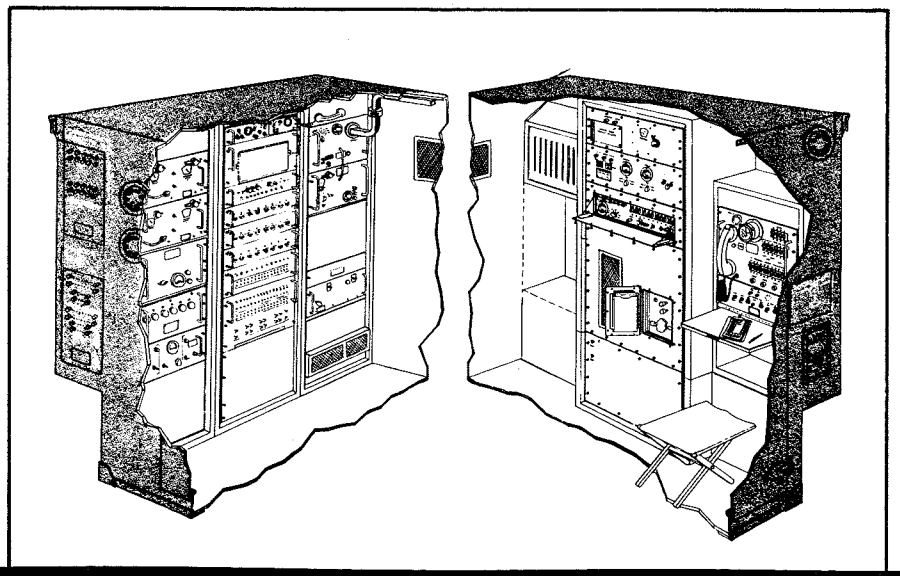
Communication links were established between a mobile Direct Air Support Center and the Combat Reporting Center, as well as regular line-of-sight and tropospheric scatter communication between fixed sites. The fixed site locations are shown in Fig. 9.

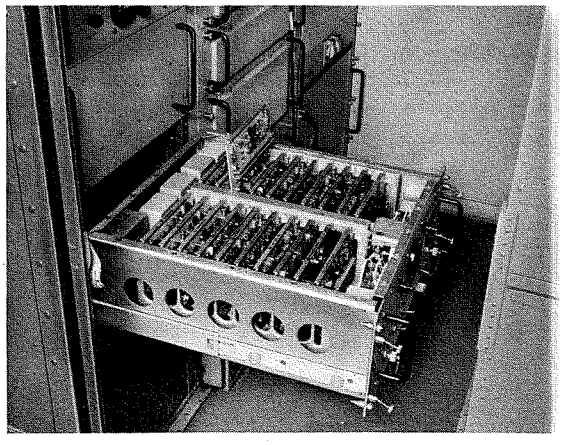
Measured results were excellent and the quick-reaction capability was demonstrated.

ACKNOWLEDGMENTS

Space precludes individual acknowledgments of those who made substantial contributions to this program. The efforts of those in Engineering and the PMO whose specific efforts and effective teamwork made this equipment possible are gratefully acknowledged.

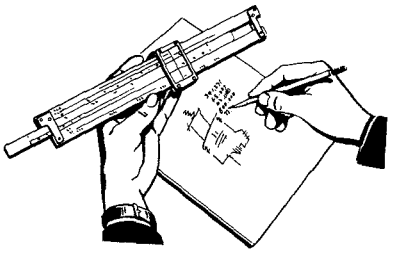
Fig. 8—Sketch of shelter layout: left side, diversity receiver, multiplex group, and transmitter; right side, plenum chamber, power amplifier, operator's position. Photo shows baseband combiner drawer in receiver rack, illustrating packaging.





Engineering and Research NOTES

BRIEF TECHNICAL PAPERS OF CURRENT INTEREST



"Space Etch"—Making Printed Wiring by Etching Spaces Instead of Conductors

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Final manuscript received June 14, 1965

Printed wiring boards with uniform-width spaces rather than uniform-width conductors offer many inherent advantages over conventional printed wiring. Emphasis is on etching of spaces rather than etching of conductors, hence the name *space-etch*. Space-etch considers the pattern as a conductor area broken into smaller areas by spaces of uniform width; conventional printed wiring considers the wiring pattern as copper conductors of varying lengths and widths.

Conventional printed-wiring artwork is prepared as a positive. But in space-etch, master pattern artwork is prepared as a negative of the conductive pattern, so that the spaces are represented by the black tape or ink ordinarily used to represent conductors. This negative space-etch approach then becomes a positive during photographic processing that converts the pattern to a silk screen or film negative. In some processes, starting with such a space-etch negative rather eliminates a step which formerly was used to reverse the pattern.

For design layout of component parts, conventional techniques can be used. In manufacturing operations, processing of space-etched printed boards is identical to conventionally patterned boards.

For breadboard work, the space-etch artwork is simply an engineering sketch in black India ink on paper (Fig. 1). Dots locate the holes for component leads. Lines are drawn to represent the spaces which will separate conductive areas. This dot-and-line sketch is then used directly as a *negative* with the KPR process to produce a printed board, reducing the time between component part layout and finished board, and eliminating the costs of additional drafting and photography. Fig. 2 shows a typical breadboard fabricated directly from an engineering sketch. For best results, the engineering sketch is made so that the inked side of the paper will touch the KPR either by drawing the pattern as it appears when looking *through* the board or by tracing the pattern on both sides of the sketch paper. (Sketches of the "double-traced" variety, viewed from the wiring side of the board, are the type used in this *Note*, for ready comparison of the patterns.)

For greater precision or better appearance, as in production units, scaled master pattern artwork can be made as usual. However, squaring the pattern (Fig. 3) permits use of drafting machines (for the newer types of artwork generators) insuring sufficient precision to satisfy almost any presently known requirements.

Normally, space-etch is best used for small-size printed boards, where maximum conductive area gives good soldering results (by avoiding too-small component lead termination areas that inhibit solder flow and fillet formation). In addition, too-small conductive areas detach readily from the board during soldering, particularly with a hand iron.

The inherent increased capacitance effects between adjacent circuit paths must be considered. On a space-etched single-sided board, capacitance between adjacent areas is approximately 1.5 pF per linear inch of border, compared to 1.0 pF per linear inch for conventionally etched boards.

The major factor in coupling capacitance between two adjacent printed conductors on a single-sided board is the *length of the border*—not the spacing or width of conductors. Therefore, keeping critical conductor paths short is essential in determining the coupling capacitance in a given circuit—true in *either* space-etched or conventional printed wiring.

The larger copper areas of space-etch act as heat reservoirs during initial soldering (and equally in and damaging heat can reach thermally sensitive devices (transistors, diodes, etc.) unless appropriate care is taken. Quick removal or insertion of the component before the joint resolidifies is important to protect thermally sensitive devices.

Larger size boards do not adapt readily to the space-etch technique. Weight of the board increases disproportionately because of the large amount of copper (and solder) per unit area. Large unbroken areas of copper are more likely to blister during soldering. This probability decreases, however, if the large areas are broken up into smaller ones.

Space-etch opens up many avenues of application. One is reduction of a complete circuit pattern to digital bits that can be readily placed on suitable recording media. The circuit wiring pattern normally is arranged such that component part lead mounting holes fall on the intersections of a basic grid. With space-etch, the spaces can also be correlated with the basic grid by specifying *that the space is to be made up of modular incremental horizontal or vertical segments, each of them one grid unit in length and coinciding with the grid lines.* For example, the lower left corner of the pattern in Fig. 2 can be represented numerically by this approach, and the entire circuit pattern can then be converted to digital information. It can then be utilized, for example, as a tape controlled layout of master pattern artwork, or as a punched paper tape in lieu of a production drawing of the circuit pattern.

The space-etch approach is a simple one, yet has numerous inherent advantages for design, drafting, and fabrication that can reduce time and costs. To realize these advantages requires changes in the engineer's design concept thinking—changes that may well open new avenues of application for space-etch.

Fig. 1—Space-etch artwork for breadboard, simply an ink-on-paper engineering sketch.

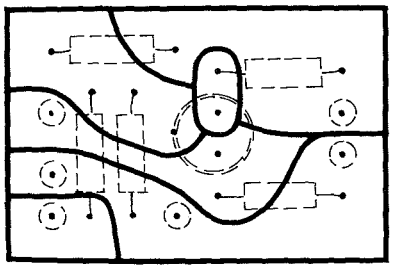


Fig. 2—Typical breadboard fabricated directly from engineering sketch.

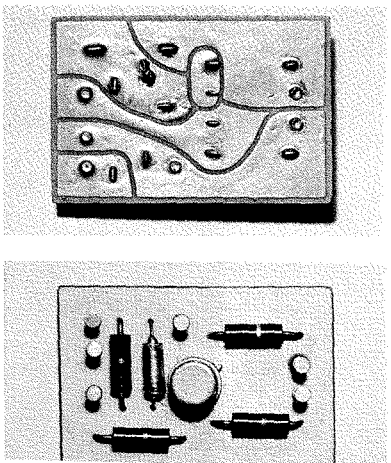
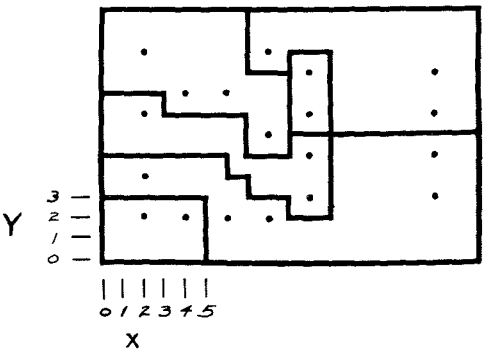


Fig. 3—Spaces and holes are laid out on an X-Y grid to allow digitalized circuit pattern.



Low-Cost, Line-Operated Circuits Using RCA 2N3583, 4, 5, Transistors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Final manuscript received July 8, 1965

The new RCA 2N3583 family represents a significant advance in transistor design—an advance designers can quickly translate into efficient, low-cost circuits. Three types in all (2N3583, 4, and 5), these n-p-n triple-diffused-silicon, high voltage transistors in TO-66 packages have sustaining voltage ratings up to 400 volts and collector current ratings of three amperes. Gain is controlled at one ampere and frequency response is typically above 15 Mc/s. The RCA 2N3583 family is tested to insure freedom from forward and reverse second breakdown within broad thermal ratings.

The characteristics of these devices make them ideally suited for use in line-operated AC-DC audio amplifiers, auto ignition systems, magnetic- and electrostatic-deflection amplifiers, inverters, converters, and ultra-sonic and sonar amplifiers. Circuits already designed and built include a 45-watt, class-B push-pull audio amplifier, and a 150-watt, 50-kc/s inverter. The inverter circuit is shown in Fig. 1. Figs. 2 and 3 show a 5-watt audio amplifier circuit and a horizontal deflection circuit.

Circuits designed around the 2N3583 family are both efficient and inexpensive. The high-voltage characteristic of these transistors not only insures low internal power losses, but also permits the power supply section to be cost-reduced in two ways. First, because the line voltage can be rectified and filtered to provide the supply voltage, the usually bulky and expensive power transformer can be eliminated. Second, inductors and capacitors required for filtering are less expensive (and more easily available) in the popular line-voltage values.

Most of the circuits listed above required some type of nonlinear switching of the transistor. Nonlinear switching results in high energy dissipation and, hence, for most transistors, danger of second breakdown or localized thermal runaway. However, the forte of the 2N3583 family is that it is production tested for forward-, reverse-, and zero-bias second breakdown to insure safe and reliable circuit operation. The data sheet for this family shows several second-breakdown curves for the typical device. These curves help define the safe operating region to guide the engineer in his circuit design.

Breakthroughs in both design and assembly techniques were required to produce an inexpensive device having maximum current-handling capability at high voltage. A new concept in metallizing achieves a five-fold refinement in semiconductor-chip geometry with no additional complexity in assembly. This concept makes possible a device having almost 0.50 inch of emitter periphery compressed into an area of only 0.01 square inch. Assembly costs are kept low by the use of a new technique in which all six interconnections of the semiconductor chip, connector, and package are brazed simultaneously in a continuous-feed furnace.

The RCA 2N3583 family employs other significant design improvements as well. For example, the semiconductor chip is directly mounted to a copper heat sink that not only improves thermal conductivity but increases the transistor's ability to handle large peak power pulses safely. In addition, the device is equipped with large, rugged emitter and base connector clips, which can withstand high mechanical and thermal shock loads without failure. Because of the excellent metallurgical stability of the braze joint between the semiconductor chip and the connectors, the RCA 2N3583 family also exhibits excellent mechanical strength after long-term, high-temperature stress.

Fig. 1—150-watt, 50-kc/s inverter. T_1 core = two Allen Bradley "C" cores (U2625C133A). T_2 core = Allen Bradley toroid (T0620H101A).

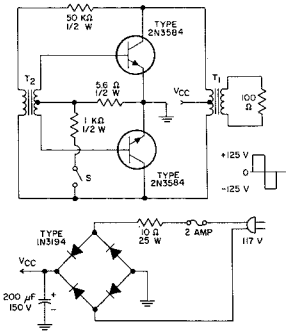


Fig. 3—Horizontal deflection circuit.

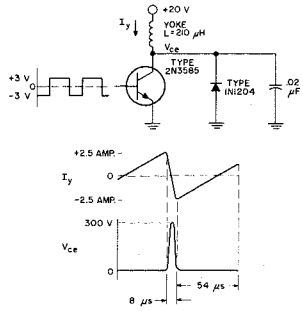
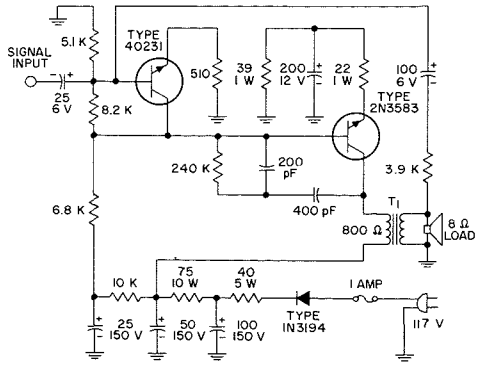


Fig. 2—5-watt audio amplifier. T_1 = C. P. Electronics part #x-9600. Total harmonic distortion is 1.5% at 5 watts output and 400 c/s. Input impedance is 300 ohms. Hum and noise down 65 dB from 4 watts. Note: All resistances in ohms; all capacitances in μF except where shown otherwise.



Electrical Remote-Controlled Gas-Leak Valve

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Final manuscript received August 26, 1965

A small, light-weight gas-leak valve has been developed primarily for use with gas dosing systems for laser tubes. Such applications require the introduction of minute quantities of noble gases under conditions of extreme cleanliness. Conventional valves for this use are generally equipped with differential screws or gears to obtain the necessary degree of leak.

This leak valve is in the form of a cylindrical container with a built-in leak seal member. This seal is electrically controlled.

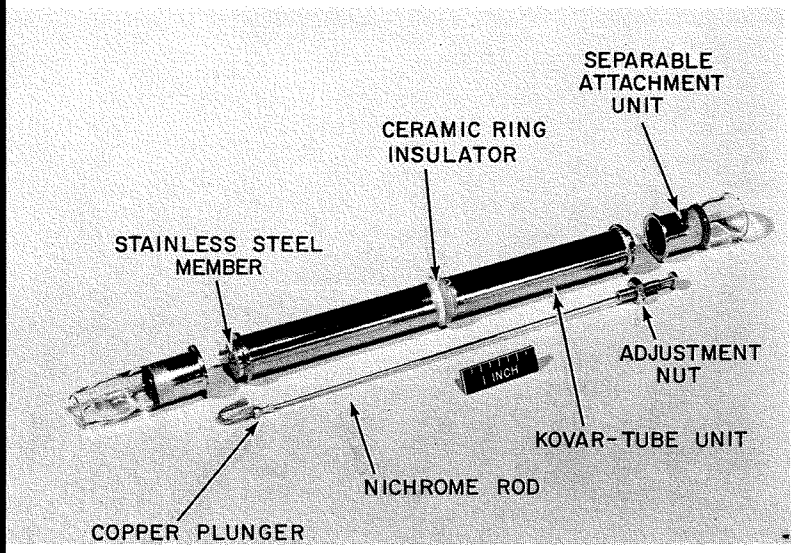
The leak-valve container can be pressurized with any gas to pressures of several atmospheres. However, it is well suited for direct attachment to commercial gas bottles for higher pressures.

The cylindrical container (Fig. 1) consists of two Kovar tubes separated by a ceramic ring insulator. A stainless-steel member is attached to one end of the container. A hole is drilled in the center of this stainless-steel member to form a sharp cylindrical valve seat. A similar arrangement is made on the other end of the container. Here the stainless-steel member represents a support wall and is perforated with one hole in the center.

A conical copper plunger attached to one end of a 40-mil nichrome rod fits into the seat mentioned previously. The other end of the rod is threaded and equipped with a nut. Stretching the rod between the wall and the seat by tightening the nut causes the copper plunger to move. The sharp edge stainless-steel valve seat penetrates into the copper so that a bakeable gas-tight seal is obtained. In this condition the container can be pressurized for use as a separate gas source (Fig. 2).

In operation, an electrical current is allowed to pass between the two Kovar sections so that the nichrome rod heats up by I^2R heating. This causes the rod to expand, thus opening the valve; upon removal of the electrical current the valve closes. The amount of leak is determined by the wire length and its temperature. In a particular design it took 1.7 watts to open the valve to pressures of 10^{-7} mm-Hg. The valve requires 3.5 watts to be fully open if the rod is 13 cm long. The rod attains a temperature of about 180°C. Such a valve has controlled vacuum systems at levels of 10^{-7} mm-Hg. to 760 mm-Hg. In one test, a valve was cycled 3,000 times between pressures of 10^{-7} mm-Hg to 10^{-4} mm-Hg. No sign of wear or failure was detected.

If the gas leak-valve-container is used as a separate gas source, it can be attached, for example, to tubulations of gas laser devices.



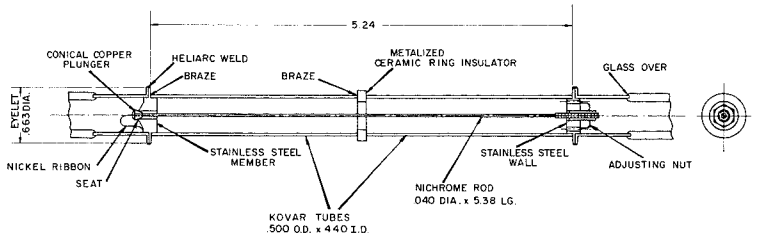


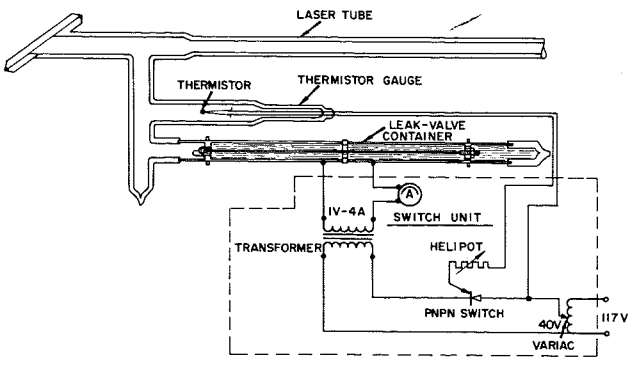
Fig. 1—Electrically remote-controlled gas-leak valve.

Since the gas pressure decreases with time in an operating laser tube due to clean-up, such a gas source will lengthen the life of a laser tube considerably. This has successfully been demonstrated by the use of a newly developed switch unit.

Fig. 2 also shows a simple circuit for automatic dosing of gas. Both the leak-valve-container and a thermistor gauge is sealed onto the tubulation of the laser device. Sensed by the thermistors, a three-terminal power transistor regulates the valve via a transformer. The thermistors sense pressures reliably from 760 mm-Hg to 10^{-5} mm-Hg. The regulator unit circuit is designed to use the transistor as a switch. If the pressure decreases below a fixed level the "switch" closes. The power-unit delivers power to the valve which doses the gas. It brings the pressure above the fixed level and the "switch" opens. This dosing operation lasts for about one minute. The power consumed is brought to a minimum when the valve is disengaged.

Besides the laser, a number of other similar devices and systems require minute quantities of pure gas for their operation. For such applications, the advantages of this valve are simplicity, low cost, ruggedness, and no strain on vacuum systems. A primary feature is the fact that the valve is automatically and remotely operated so that it can be used inside of bell jars and other enclosures.

Fig. 2—Valve and associated switch unit for automatic feeding of gas to a laser tube.



Asynchronously Multiplexed Binary Channel Capacity

R. C. Sommer, *Systems Laboratory, Communications Systems Div., DEP, New York, N. Y.*

Final manuscript received Sept. 1, 1965

This *Note* represents an extension of an earlier paper by White[1] which treats the theortical rate at which information can be transmitted over a binary channel by means of asynchronously multiplexed signals. When the number of signals becomes infinite, a simple equation for information rate is derived. For this limiting case, it is shown that the information rate maximizes to ln2 bits per pulse width.

Consider a binary channel which is occupied by $M = 1,2, \ldots$ asynchronously multiplexed signals. Each transmitted signal consists of standard-width rectangular pulses, and communication is accomplished by sensing the presence or absence of a pulse at the receiver. Let the duty factor per signal (fraction of time that each signal has a pulse in progress) be called δ. Then, following the procedure outlined by White[1], one obtains the theoretical total rate of information (R bits per pulse width) received by M receivers, which can be expressed as:

$$R = -M(1-\delta)\log_2(1-\delta) + M\left[(1-\delta) - (1-\delta)^M\right]\log_2\left[(1-\delta) - (1-\delta)^M\right] - M\left[1-(1-\delta)^M\right]\log_2\left[1-(1-\delta)^M\right] \quad (1)$$

This result is illustrated in Fig. 1 for $M = 2^r$; $r = 0,1 \cdots,7$, where it is seen that there exists an optimum value of δ which maximizes R for any choice of M. The maximum value of R achieved is the channel capacity. Optimum values of δ were found numerically from Eq. 1 for several values of M, and the resulting values of capacity were used to produce Fig. 2, where it is seen that the capacity decreases from approximately 0.768 to 0.693 bits per pulse width as M increases from two.

The optimum values of δ obtained above were used to calculate optimum values of $P_o = 1 - (1-\delta)^M$, where P_o is the probability that the channel is in the *on* state (at least one pulse in progress).

Fig. 1—Information rate vs. duty factor.

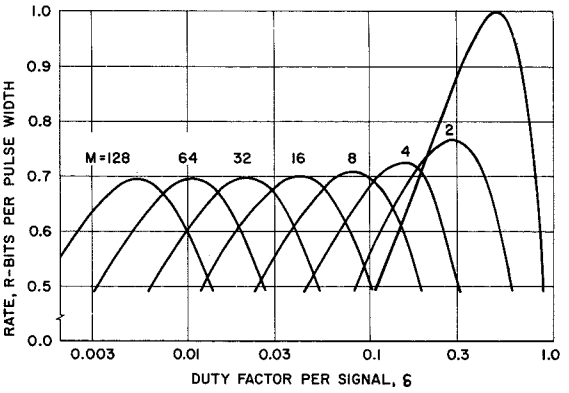
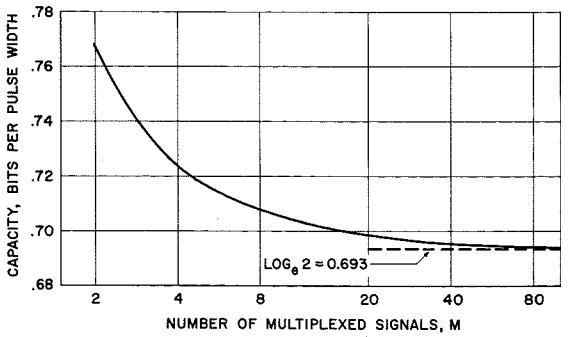


Fig. 2—Channel capacity vs. number of multiplexed signals.



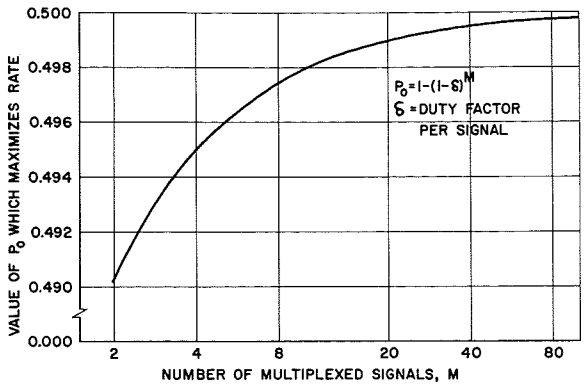


Fig. 3—Optimum P_0 vs. number of multiplexed signals.

The result is illustrated in Fig. 3, where it is seen that the optimum value of P_o is quite insensitive to the choice of M, since it increases from approximately 0.491 to 0.500 as M increases from two.

It is of interest to determine the limit of R when M becomes infinite. For this purposes, it is convenient to define $x = 1 - P_o = (1 - \delta)^M$, where x is the probability that the channel is in the *off* state, and to let $\alpha = 1/M$. Then, Eq. 1 can be recast into the form:

$$R = -x^\alpha \ln x + \frac{1}{\alpha}\left[(x^\alpha - x)\ln(x^\alpha - x) - (1-x)\ln(1-x)\right] \quad (2)$$

As M approaches infinity, α approaches zero, and the bracketed term in Eq. 2 also approaches zero. Thus,

$$\lim_{\alpha \to o}\left[\frac{(x^\alpha - x)\ln(x^\alpha - x) - (1-x)\ln(1-x)}{\alpha}\right]$$
$$= \lim_{\alpha \to o}\left\{\frac{d}{d\alpha}\left[(x^\alpha - x)\ln(x^\alpha - x)\right]\right\} = \ln x + \ln x \ln(1-x),$$

So that, when the information is measured in natural units:

$$\lim_{\alpha \to o}\left[R\right] = \ln x \ln(1-x) \quad (3)$$

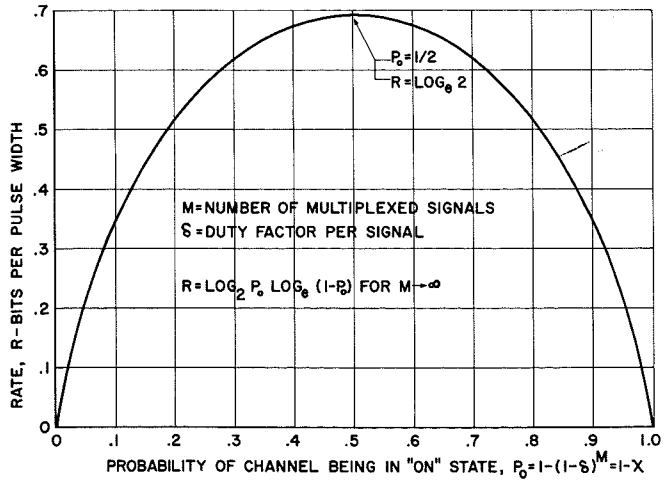
In general,

$$\lim_{\alpha \to o}\left[R\right] = \log_b x \ln(1-x) = \ln x \log_b(1-x), \quad (4)$$

where, for example, $b = 2$ if the information is measured in bits. If x is varied in Eq. 4, it is easily verified that the maximum value of rate (capacity) is ln2 bits per pulse width at $x = \frac{1}{2}$. The result given by Eq. 4 is illustrated in Fig. 4 as a function of $P_o = 1 - x$. It has been numerically verified that Eq. 4, which becomes exact only when M becomes infinite, can be used to estimate R with sufficient accuracy for practical purposes with any M greater than about ten.

1. W. D. White, "Theoretical Aspects of Asynchronous Multiplexing," *Proc. IRE*, Vol. 38, p. 270, March, 1950.

Fig. 4—Information rate vs. P_0.



Expanding the Capabilities of Instrumental Analysis with Computer Techniques

R. T. Smith, J. G. White, and J. R. Woolston
Research Services Lab., RCA Laboratories, Princeton, N. J.

Final manuscript received August 23,1965

Most instrumental analytical techniques require extensive mathematical calculations that have traditionally been done manually. For the RCA 601 at RCA Laboratories, Princeton, several programs have been written to do such computations.

Mass Spectrography: The mass spectrograph produces a photographic plate that shows the kind and amount of impurities present in a sample by the position and optical density of the recorded lines. These lines are scanned with a densitometer to provide the input data for the computer. The computer then examines the data for inconsistencies, generates a calibration curve for the individual photographic emulsion, corrects the data for background fog, applies several additional corrections (e.g., mass effect and isotopic abundance), computes the concentrations (if detectable) and detection limits for every stable element in the periodic table and prepares a complete report addressed directly to the customer who requested the analysis. Typical analysis time has been shortened from five hours to one-half hour, and the services of a secretary to type the report have been obviated. It has also been possible to delve deeper into factors limiting quantitative accuracy because the large volumes of data obtained are now manageable.

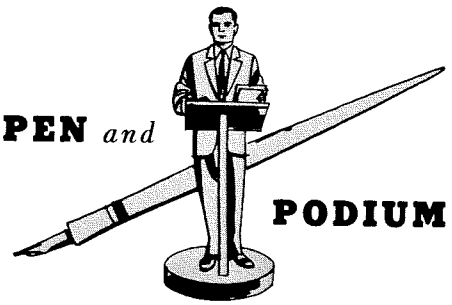
X-Ray Crystallography: Single-crystal x-ray diffraction is used to determine the basic structure of a new material; that is, the positions and spacings of the atoms in the unit cell of the crystal. In x-ray crystallography of organic laser crystals, ferroelectrics, and magnetic materials, the routine stages of a research problem involve very extensive computations of two types: *1)* the scattering distribution throughout the crystal is represented as a three-dimensional fourier series, the magnitudes of the coefficients being derived from the experimental x-ray intensity data. In a typical case, 2,000 items of data may be added in at each 15,000 points in the crystal unit cell. These computations are now carried out in about 5 minutes of computer time. *2)* The structure factors, simply related to the x-ray intensities, may be calculated rapidly from a postulated model of the crystal structure. Input data to the computer are the X, Y, and Z coordinates of each crystallographically independent atom and the scattering factors (variation of scattering power with scattering angle) for each kind of atom present.

A crystal structure determination usually proceeds by alternate use of fourier and structure factor computations with interpretative work in between. The computer has freed the crystallographer from routine calculations that took from one to five months per structure determination. It has enabled him to concentrate on the interpretative phases, no longer delayed by lengthy computations.

X-Ray Powder Diffraction: The x-ray powder diffraction technique is routinely used to identify the crystalline forms present in a solid sample. Crystalline materials, even in finely divided or powder form, reflect x-rays at certain discrete angles characteristic of the spacing between planes of atoms in the crystal lattice. A diffraction pattern is recorded as concentric arcs on photographic film. In interpreting the data taken from these films, lengthy calculations must be made to relate the observed pattern to its associated crystal lattice. Interplanar spacings, or D values, are derived from the photographic record and are used to construct tables of differences of these values. The most frequently occurring differences usually bear simple relationships to the lattice parameters of the crystalline unit cell. The computer tests validity of original data and rejects certain bad data due to human errors made in reading the original films. It then searches the table of differences it has constructed and suggests the unit cell (and hence the material) that could give rise to the recorded pattern. Finally, if desired, systematic and random errors in the data are automatically corrected and a least-squares fit is applied to yield accurate lattice parameter values.

The computer does its calculation in a little more than a minute and saves two man-days of analysis and calculation on a desk calculator. It also eliminates errors induced by human fatigue, rejects errors made in measuring the films, and corrects errors introduced by the x-ray equipment.

For further information on these techniques, contact the authors.



A SUBJECT-AUTHOR INDEX TO RECENT RCA PAPERS

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SUBJECT INDEX

Titles of papers are permuted where necessary to bring significant keyword(s) to the left for easier scanning. Authors' division appears parenthetically after his name.

AMPLIFICATION

Emitter-Coupled Amplifier—Applicability to a Family of Analog Integrated Circuits—R. Tipping (DEP-DME, Som.) *MSEE Thesis*, Univ. of Penna., May 1965

Hybrid-Coupled VHF Transistor Amplifier—A. Newton, R. M. Kurzrok, R. M. Mehlman (DEP-CSD, Camden) *Solid State Design*, Vol. 6, No. 8, Aug. 1965

BIOMEDICAL ELECTRONICS

Evolution of Medical and Biological Engineering, Some Thoughts on the—L. E. Flory (Labs, Pr.) 6th Intern'l. Conf. on Medical Electronics and Biological Eng., Tokyo, Japan, Aug. 22-27, 1965

Perspectives in Medical Electronics and Biological Engineering—V. K. Zworykin (Labs, Pr.) 6th Intern'l. Conf. on Medical Electronics and Biological Eng., Tokyo, Japan, Aug. 22-27, 1965

CHECKOUT; MAINTENANCE

Simplifying the Use of Automatic Test Equipment with a Compiler—R. C. Miller (DEP-ASD, Burl.) IEEE Automatic Support Systems Symp., St. Louis, Mo., June 7-9, 1965; *Conf. Proceedings*

COMMUNICATIONS, DIGITAL

Microelectronic Airborne Data Link—E. J. Mozzi (DEP-CSD, Camden) Engineering Lecture, RCA, Camden, N. J., Sept. 8, 1965. *Also:* 1965 IEEE Conf. on Military Electronics, Sept. 22, 1965, Washington, D.C.; *Conf. Proceedings*

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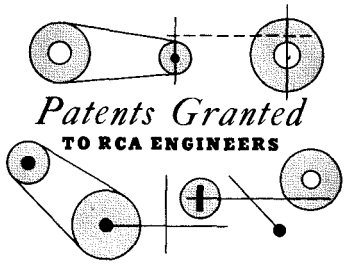
Kiss, Z. J. lasers
Krausbauer, L. solid-state materials—optical properties
Kudman, I. solid-state materials—electronic properties
Lanyon, H. P. D. solid-state materials—optical properties
Larrabee, R. D. solid-state materials—electronic properties
Larrabee, R. D. instruments; lab techniques
Liu, S. G. solid-state materials—optical properties
Mark, P. solid-state materials—electronic properties
Mark, P. solid-state materials—electronic properties
McClure, D. S. solid-state materials—optical properties
Miiller, H. S. solid-state devices
Miller, A. lasers
Miller, R. E. solid-state materials—electronic properties
Moore, A. R. solid-state materials—electronic properties
Moore, A. R. solid-state materials—electronic properties
Nelson, H. lasers
Nievergelt, J. computer programming
Nitsche, R. solid-state materials—optical properties
Rajchman, J. A. computer storage
Revesz, A. G. solid-state materials—physical-chemical structure
Rothwarf, A. superconductivity; cryoelectrics
Sabisky, E. S. radiation effects
Shallcross, F. V. solid-state materials—optical properties
Shewchun, J. solid-state materials—electronic properties
Smith, R. W. solid-state materials—electronic properties
Smith, R. W. solid-state materials—electronic properties
Steele, M. C. plasma
Steigmeier, E. F. solid-state materials—electronic properties
Vural, B. plasma
Vural, B. electromagnetic theory; phenomena
Vural, B. electromagnetic theory; phenomena
Walters, W. L. solid-state materials—optical properties
Warfield, G. solid-state devices
Warfield, G. solid-state devices
White, J. G. solid-state materials—physical-chemical structure
Wild, P. solid-state materials—optical properties
Williams, R. solid-state materials—electronic properties
Williams, R. M. solid-state materials—electronic properties
Williams, R. M. solid-state materials—electronic properties
Woodard, D. W. instruments; lab techniques
Zworykin, V. K. biomedical electronics



AS REPORTED BY RCA DOMESTIC PATENTS, PRINCETON

RCA LABORATORIES

High Speed Amplifying Modulation-Demodulation Logic—W. O. Eckhardt (Labs, Pr.) *U. S. Pat. 3,189,839*, June 15, 1965 (assigned to U. S. Gov't.)

Cryoelectric Circuits—R. W. Ahrons (Labs, Pr.) *U.S. Pat. 3,191,063*, June 22, 1965 (assigned to U.S. Gov't.)

Method of Making Targets for Pickup Tubes—S. A. Ochs (Labs, Pr.) *U.S. Pat. 3,195,199*, July 20, 1965

Electrostatic Printing Apparatus—C. J. Young (Labs, Pr.) *U.S. Pat. 3,195,430*, July 20, 1965

Method of Making Semiconductor Devices—W. M. Webster, Jr. (Labs, Pr.) *U.S. Pat. 3,196,058*, July 20, 1965

Color Television Camera System—A. V. Bedford (Labs, Pr.) *U.S. Pat. 3,196,205*, July 20, 1965

Means for Observing a Workpiece in Electron Beam Machining Apparatus—A. B. El-Kareh (Labs, Pr.) *U.S. Pat. 3,196,246*, July 20, 1965

Beam Penetration Color Cathode Ray Tube—W. H. Barkow (Labs, Pr.) *U.S. Pat. 3,196,305*, July 20, 1965

Electron Gun with Positioner for Emissive Surface of Cathode—A. D. Cope (Labs, Pr.) *U.S. Pat. 3,197,665*, July 27, 1965

Circuits—B. J. Lechner (Labs, Pr.) *U.S. Pat. 3,197,744*, July 27, 1965

Color Television Indexing System for Reducing Color Distortion—R. E. Flory (Labs, Pr.) *U.S. Pat. 3,198,879*, Aug. 3, 1965

F.M. Stereophonic Radio Signal Receivers Having Combined Predetection De-emphasis and Filtering Circuit—A. L. Limberg (Labs, Pr.) *U.S. Pat. 3,198,885*, Aug. 3, 1965

Means for Controlling an Electron Beam—R. B. Lochinger (Labs, Pr.) *U.S. Pat. 3,199,039*, Aug. 3, 1965

Solid State Electrical Devices Utilizing Phonon Propagation—R. Braunstein (Labs, Pr.) *U.S. Pat. 3,200,259*, Aug. 10, 1965

Spherical Grids and Methods of Making Same—H. B. Law (Labs, Pr.) *U.S. Pat. 3,200,469*, Aug. 17, 1965

Flexible Logic Circuit—M. E. Szekely (Labs, Pr.) *U.S. Pat. 3,201,574*, Aug. 17, 1965

Memory Systems Using Tunnel Diodes—J. C. Miller (Labs, Pr.) *U.S. Pat. 3,201,595*, Aug. 17, 1965

Storage-Diode Pulse Generator Employing Tuning Transmission Line for Altering Shape of Output Pulses—J. J. Amodei (Labs, Pr.) *U.S. Pat. 3,201,612*, Aug. 17, 1965

Electrical Circuit—J. J. Amodei (Labs, Pr.) *U.S. Pat. 3,201,613*, Aug. 17, 1965

Redundant Logic Networks—K. K. Maitra (Labs, Pr.) *U.S. Pat. 3,201,701*, Aug. 17, 1965

Apparatus, Without Moving Parts, for Moving a Storage Area Along a Storage Medium—J. Pearl (Labs, Pr.) *U.S. Pat. 3,201,765*, Aug. 17, 1965

Image Pickup System—S. V. Forgue (Labs, Pr.) *U.S. Pat. 3,202,759*, Aug. 24, 1965

Electron Beam Tube with Less than Thirty Mills Spacing Between the Target Electrode and Photo-cathode Electrode—P. K. Weimer (Labs, Pr.) *U.S. Pat. 3,202,853*, Aug. 24, 1965

Pickup Tube Target Having an Additive Therein for Reduced Resistivity—S. A. Ochs (Labs, Pr.) *U.S. Pat. 3,202,854*, Aug. 24, 1965

Glass-to-Metal Seal—J. E. Benbenek (Labs, Pr.) *U.S. Pat. 3,203,715*, Aug. 31, 1965

Color Television Indexing Control Utilizing Intensity and Velocity Modulation Techniques—E. O. Keizer (Labs, Pr.) *U.S. Pat. 3,204,024*, Aug. 31, 1965

Acoustic Apparatus for Encoding Sound—H. F. Olson, H. Belar (Labs, Pr.) *U.S. Pat. 3,204,030*, Aug. 31, 1965

Storage-type Electroluminscent Image Amplifier—J. Murr, Jr., H. O. Hook (Labs, Pr.) *U.S. Pat. 3,204,106*, Aug. 31, 1965

Four-terminal Solid State Superconductive Device with Control Current Flowing Transverse to Controlled Output Current—R. H. Parmenter (Labs, Pr.) *U.S. Pat. 3,204,115*, Aug. 31, 1965

Solid State Superconductor Switching Device Wherein Extraction of Normal Carriers Controls Superconductivity of Said Device—R. H. Parmenter (Labs, Pr.) *U.S. Pat. 3,204,116*, Aug. 31, 1965

Penetration Color Screen, Color Tube, and Color Television Receiver—D. H. Pritchard (Labs, Pr.) *U.S. Pat. 3,204,143*, Aug. 31, 1965

ELECTRONIC DATA PROCESSING

Pulse Amplifier—R. J. C. Chueh (EDP, Camden) *U.S. Pat. 3,193,704*, July 6, 1965 (assigned to U.S. Gov't.)

High Voltage Transformer and Rectifier Tube with Direct Connection There-between—F. E. Brooks (EDP, Camden) C.C. Iden (H.I.) *U.S. Pat. 3,201,730*, Aug. 17, 1965

DEFENSE ELECTRONIC PRODUCTS

Passive Radar Tracking Apparatus—D. K. Barton, W. J. Rose (DEP-MSR, Mrstn.) *U.S. Pat. 3,196,433*, July 20, 1965 (assigned to U.S. Gov't.)

Wide Angle Phase Shifter or Modulator—L. E. Potter (DEP-CSD, Camden) *U.S. Pat. 3,196,368*, July 20, 1965

Semiconductor Modulators—B. M. Rabinovici, R. F. V. Stalemark (DEP-CSD, N.Y.) *U.S. Pat. 3,196,370*, July 20, 1965

Clipping System—J. T. Heizer (DEP-App. Res., Camden) *U.S. Pat. 3,196,289*, July 20, 1965 (assigned to U.S. Gov't.)

Fluid Applicator Apparatus—G. K. Zin (DEP-App. Res., Camden) *U.S. Pat. 3,196,832*, July 27, 1965

AGC Parametric Amplifier with Constant Output Signal Level—W. Y. Pan (DEP-CSD, N.Y.) *U.S. Pat. 3,197,708*, July 27, 1965

Reading Machine—H. E. Haynes (DEP-MSR, Mrstn.) H. J. Woll (DEP-ASD, Burl.) *U.S. Pat. 3,197,735*, July 27, 1965

Search Apparatus—A. S. Rettig (DEP-CSD, Camden) D. Z. Cohen (BCD, Camden) *U.S. Pat. 3,197,742*, July 27, 1965

Signal Detection, Thresholding and Switching System—A. I. Mintzer, A. J. Lisicky (DEP-MSR, Mrstn.) *U.S. Pat. 3,197,771*, July 27, 1965 (assigned to U.S. Gov't)

High Speed Binary Adder-Subtractor with Carry Ripple—W. A. Helbig, R. J. Woldrich (DEP-ASD, Van Nuys) *U.S. Pat. 3,198,939*, Aug. 3, 1965

Color Television Image Reproduction—H. C. Goodrich (DEP-MSR, Mrstn.) *U.S. Pat. RE25,833*, Aug. 10, 1965

Memory—A. I. Pressman (DEP-AED, Pr.) *U.S. Pat. 3,201,598*, Aug. 17, 1965

Multivibrator Employing Voltage Controlled Variable Capacitance Element in a Coupling Network—R. H. Norwalt (DEP-ASD, Van Nuys) *U.S. Pat. 3,201,602*, Aug. 17, 1965

Transformer-Rectifier Combination — G. E. Skorup (DEP-MSR, Mrstn.) *U.S. Pat. 3,201,652*, Aug. 17, 1965

Frequency Doubler Employing Two Push-pull Pulsed Internal Field Effect Devices—M. E. Ames, Jr. (DEP-CSD, Camden) *U.S. Pat. 3,202,840*, Aug. 24, 1965

Coherent Frequency Converter for Testing Microwave Devices with Audio Spectrum Analyzer—R. F. Koontz, Jr. (DEP-MSR, Mrstn.) *U.S. Pat. 3,202,931*, Aug. 24, 1965 (assigned to U.S. Gov't.)

Document Handling System—F. W. Pfleger (DEP-MSR, Mrstn.) *U.S. Pat. 3,203,693*, Aug. 31, 1965

ELECTRONIC COMPONENTS AND DEVICES

Method of Fabricating Electron Tubes Having Photocathodes—A. H. Sommer (ECD, Pr.) *U.S. Pat. 3,195,972*, July 20, 1965

Method of Manufacturing Pickup Tubes—R. L. Van Asselt, W. M. Kramer (ECD, Lanc.) *U.S. Pat. 3,196,515*, July 27, 1965

Electron Tube Having a Novel Electrode Support Arrangement—J. W. Gaylord, J. B. Pyle (ECD, Lanc.) *U.S. Pat. 3,197,666*, July 27, 1965

Enclosure for Semiconductor Devices—N. C. Turner (ECD, Som.) *U.S. Pat. 3,199,003*, Aug. 3, 1965

Method for Making a Semiconductor Device—J. H. Scott, Jr., J. Olmstead (ECD, Som.) *U.S. Pat. 3,200,019*, Aug. 10, 1965

Apparatus for Producing Electronic Tube Stems—R. W. Handmann (ECD, Hr.) *U.S. Pat. 3,201,216*, Aug. 17, 1965

Tubular Glass Sealing Apparatus—J. Lysåk (ECD, Hr.) *U.S. Pat. 3,201,217*, Aug. 17, 1965

Electron Tube Stem Having Break-Away Leads—W. K. Batzle (ECD, Hr.) *U.S. Pat. 3,201,509*, Aug. 17, 1965

High Voltage Electron Discharge Tube—W. R. Weyant (ECD, Hr.) *U.S. Pat. 3,201,636, Aug. 17, 1965*

Mesh Electrode Support Structure—B. Antoniades (ECD, Lanc.) *U.S. Pat. 3,202,857*, Aug. 24, 1965

Electrode Support Means—R. G. Spangler (ECD, Lanc.) *U.S. Pat. 3,202,861*, Aug. 24, 1965

HOME INSTRUMENTS DIVISION

Wire Marking Apparatus—H. D. Williams (H. I., Bloomington) *U.S. Pat. 3,195,499*, July 20, 1965

Deflection Circuit with Barkhausen Oscillation Preventive Means—C. S. Liu (H. I., Indpls.) *U.S. Pat. 3,196,309*, July 20, 1965

Combined Mounting-Bracket and Heat-Sink—J. H. Bruestle (H. I., Pr.) *U.S. Pat. 3,200,296*, Aug. 10, 1965

Mount for Deflection Yoke and Convergence Exciter—J. M. Ammerman (H. I., Indpls.) *U.S. Pat. 3,201,629*, Aug. 17, 1965

Augmented B-boost Voltage Supply—J. Stark, Jr. (H. I., Indpls.) *U.S. Pat. 3,201,642*, Aug. 17, 1965

Shield—W. M. Nuss (H. I., Cherry Hill) *U.S. Pat. 3,201,653*, Aug. 17, 1965

High Voltage Transformer and Rectifier Tube with Direct Connection Therebetween—C. C. Iden (H. I.) F. E. Brooks (EDP, Camden) *U.S. Pat. 3,201,730*, Aug. 17, 1965

Rotary Bi-directional Stepper Mechanism—E. J. Sperber (H. I., Indpls.) *U.S. Pat. 3,202,002*, Aug. 24, 1965

Regulated High Voltage Supplies for Color Television Tube—J. Stark, Jr. (H. I., Indpls.) *U.S. Pat. 3,202,865*, Aug. 24, 1965

BROADCAST AND COMMUNICATIONS PRODUCTS DIV.

Impedance Matching Source to Line for Pulse Frequencies without Attenuating Zero Frequency—G. H. Wells (BCD, Camden) *U.S. Pat. 3,197,719*, July 27, 1965

Search Apparatus—D. Z. Cohen (BCD, Camden) A. S. Rettig (DEP-CSD, Camden) *U.S. Pat. 3,197,742*, July 27, 1965

Perforated Record Member Sensing Apparatus—J. P. Hammel (BCD, L. A.) *U.S. Pat. 3,200,240*, Aug. 10, 1965

DATES *and* DEADLINES

PROFESSIONAL MEETINGS AND CALLS FOR PAPERS

Meetings

Oct. 31-Nov. 5, 1965: 98TH TECH. CONF. & EQUIPMENT EXHIBIT, Soc. of Motion Picture & Television Engrs. (SMPTE); Queen Elizabeth Hotel, Montreal, Quebec, Canada. *Prog. Info.:* R. S. Rekert, Natl. Film Board of Canada, c/o SMPTE, 9 E. 41st St., New York 17, N.Y.

Nov. 1-3, 1965: 4TH INDUSTRY WIDE CONF. ON INDUSTRIAL STATIC POWER CONVERSION, IEEE; Benjamin Franklin Hotel, Philadelphia, Pa. *Prog. Info.:* E. A. Harty, North Electric Co., Box 3556, Columbus, Ohio.

Nov. 2-4, 1965: IEEE INTL. SPACE ELECTRONICS SYMP., IEEE, G-SET; Fontainbleu Hotel, Miami Beach, Fla. *Prog. Info.:* Thos. Broskie, NASA, Cape Kennedy Complex, Cocoa Beach, Fla.

Nov. 3-5, 1965: NEREM NORTHEAST ELECTRONIC RESEARCH AND ENGINEERING MTG., (NEREM), Region 1; Sheridan Boston & Civic Auditorium, Boston, Mass. *Prog. Info.:* NEREM, IEEE Boston Office, 313 Washington St., Newton 58, Mass.

Nov. 10-12, 1965: 18TH ANN. CONF. ON ENG. IN MEDICINE & BIOLOGY, IEEE, G-BME-ISA; Univ. of Pa. & Sheraton Hotel, Phila., Pa. *Prog. Info.:* Dr. H. Schwan, Moore School of EE, Univ. of Pa., Phila., Pa.

Nov. 16-19, 1965: 11TH ANN. CONF. ON MAGNETISM & MAG. MATERIALS, IEEE, G-MAG, AIP; Hilton Hotel, San Francisco, Calif. *Prog. Info.:* J. T. Elder, The 3 M Co., 400 McKnight Rd., St. Paul 19, Minn.

Nov. 18-19, 1965: MAECON (MID-AMERICAN ELEC. CONF.) IEEE, Kansas City Sect.; Continental Hotel, Kansas City, Mo. *Prog. Info.:* W. Wiley, Bonzer, Inc., 11111 W. 59th Ter., Shawnee, Kansas.

Nov. 22-23, 1965: INTL. CONF. ON UHF TELEVISION, IEEE, IERE, IEE; London, England. *Prog. Info.:* UHF Television Conf., Jt. Secretariat, 8-9 Bedford Sq., London, W.C. 1, England.

Nov. 30-Dec. 1-2, 1965: FALL JOINT COMPUTER CONF., IEEE-ACM, AFIPS; Convention Center, Las Vegas, Nev. *Prog. Info.:* S. Shohara, Hughes Aircraft Co., Fullerton, Calif.

Dec. 1-3, 1965: 1965 ULTRASONICS SYMP., IEEE, G-SU; Hotel Kenmore, Boston, Mass. *Prog. Info.:* D. L. Arenberg, Arenberg Ultrasonic Lab., 94 Green St., Jamaica Plain 30, Mass.

Dec. 2-3, 1965: 16TH VEHICULAR COMMUNICATION CONF., IEEE, G-VC; Sheraton Park Hotel, Wash., D.C. *Prog. Info.:* W. F. Biggerstaff, USFS Elec. Ctr., ARC, Beltsville, Md.

Jan. 25-27, 1966: 12TH ANN. SYMP. ON RELIABILITY, IEEE, G-R, ASQC, et. al.; Sheraton Palace Hotel, San Francisco, Calif. *Prog. Info.:* A. R. Park, Genl. Precision Inc., 1370 Encintas Rd., San Marcos, Calif.

Jan. 31-Feb. 2, 1966: INTL. SYMP. ON INFORMATION THEORY, IEEE, G-IT; UCLA, Los Angeles, Calif. *Prog. Info.:* A. V. Balakrishnan, Dept. of Eng., Univ. of Calif., Los Angeles, Calif.

Feb. 2-4, 1966: 7TH WESTERN CONV. ON AEROSPACE & ELECTRONIC SYSTEMS, IEEE, G-AES, L.A. Dist.; Los Angeles, Calif. *Prog. Info.:* IEEE Headquarters, Box A, Lenox Hill Station, New York, N.Y.

Feb. 9-11, 1966: 1966 INTL. SOLID-STATE CIRCUITS CONF., 13TH ANN. MTG., IEEE, Univ. of Pa.; Univ. of Pa. Campus and Sheraton Hotel, Phila., Pa. *Prog. Info.:* K. Fischer, U. S. Army Electronics Command, ATTN: AMSEL-KL-I, Fort Monmouth, N. J.

Calls for Papers

Mar. 2-4, 1966: SCINTILLATION & SEMICONDUCTOR COUNTER SYMP., IEEE, G-NS; Shoreham Hotel, Wash., D.C. **Deadline:** Abstracts, **11/30/65.** *TO:* W. A. Higinbotham, Brookhaven Natl. Labs., Upton, L.I., N.Y.

March 21-24, 1966: IEEE INTL. CONVENTION; IEEE, All Groups, TAB Comms.; Coliseum and New York Hilton Hotel, N.Y., N.Y. **Deadline:** Abstracts, **10/15/65;** Manuscripts, **1/14/66.** *FOR INFO.:* IEEE Headquarters, Box A, Lenox Hill Station, N.Y., N.Y. *(Late abstracts may be acceptable.)*

April 18-19, 1966: 1ST NATL. ISA SYMP. ON MAINTENANCE, ISA; Wilmington, Delaware. **Deadline:** Abstracts, **1/1/66.** *TO:* H. S. Wilson, Div. Dir., Moore Products Co., 2011 Concord Pike, Wilmington, Delaware.

April 18-21, 1966: 1966 SPRING URSI-IEEE MTG., IEEE-URSI; Natl. Academy of Sciences, Wash., D.C. **Deadline:** Abstracts, **1/1/66.** *FOR INFO.:* IEEE Headquarters, Box A, Lenox Hill Station, N.Y., N.Y.

April 20-22, 1966: 1966 INTL. NONLINEAR MAGNETICS CONF. (INTERMAG), IEEE, G-Mag VDE; Stuttgart, Germany. **Deadline:** Abstracts, **12/7/65;** Manuscripts, **4/1/66.** *TO:* Dr. E. W. Pugh, IBM Corp., 1000 Westchester Ave., White Plains, N.Y.

April 26-28, 1966: SPRING JOINT COMPUTER CONF., IEEE, AFIPS, ACM; Boston Civic Ctr., Boston, Mass. **For Deadline Info.:** IEEE Headquarters, Box A, Lenox Hill Station, N.Y., N.Y.

April 26-28, 1966: 1966 REGION SIX ANN. CONF., IEEE; Tucson, Ariz., Pioneer Intl. Hotel. **Deadline:** Abstracts **12/1/65.** *TO:* Dr. L. O. Huelsman, Tech. Papers Chairman, 1966 IEEE Region Six Ann. Conf., c/o Department of EE, Univ. of Ariz., Tucson, Ariz.

May 2-4, 1966: 1966 AIAA COMMUNICATIONS SATELLITE SYSTEMS CONF., AIAA, IEEE; Wash., D.C. **Deadline:** Abstracts, **11/30/65;** Manuscripts, **3/21/66.** *TO:* N. Feldman, Electronics Dept., The RAND Corp., 1700 Main St., Santa Monica, Calif.

May 4-6, 1966: 1966 ELECTRONIC COMPONENTS CONF., EIA, IEEE; Marriott Twin Bridges Motor Hotel, Wash., D.C. **Deadline:** Abstracts, **10/8/65;** Manuscripts, **1/30/65.** *TO:* R. A. Gerhold, Chairman, Tech. Program Committee, U. S. Army Electronics Command, (AMSEL-KL-I), Fort Monmouth, N. J.

May 2-4, 1966: 12TH NATL. ISA AEROSPACE INSTRUMENTATION SYMP., ISA; Marriott Motor Hotel, Phila., Pa. **Deadline:** Abstracts, **1/1/66.** *FOR INFO.:* B. S. Hines, ISA Headquarters, 530 William Penn Place, Pittsburgh, Pa.

Be sure deadlines are met—consult your Technical Publications Administrator or your Editorial Representative for the lead time necessary to obtain RCA approvals (and government approvals, if applicable). Remember, abstracts and manuscripts must be so approved BEFORE sending them to the meeting committee.

May 10-12, 1966: 15TH NATL. TELEMETERING CONF., IEEE, AIAA-ISA; Prudential Center, Boston, Mass. **Deadline:** Abstracts, **1/15/66.** *TO:* J. Kelley, Program Chairman, NASA-Electronics Res. Center, 575 Technology Sq., Cambridge, Mass.

May 11-13, 1966: 12TH NATL. ISA ANALYSIS INSTRUMENTATION SYMP., ISA; The Shamrock Hilton, Houton, Texas. **Deadline:** Abstracts, **1/15/66.** *TO:* G. I. Doering, Program Dir., Industrial Nucleonics Corp., 1205 Chesapeake Ave., Columbus, Ohio.

May 16-18, 1966: NAECON (NATL. AEROSPACE ELEC. CONF.), IEEE, G-ANE-AIAA, Dayton Section; Dayton, Ohio. **Deadline:** Abstracts, **approx. 12/15/65.** *FOR INFO.:* IEEE Dayton Office, 1414 E. 3rd St., Dayton 3, Ohio.

May 16-18, 1966: 1966 NATL. SYMP. ON MICROWAVE THEORY & TECH., IEEE, G-MTT, Palo Alto, Calif. **Deadline:** Abstracts, **approx. 11/15/65.** *FOR INFO.:* IEEE Headquarters, Box A, Lenox Hill Station, N.Y., N.Y.

June 15-17, 1966: 2ND IEEE INTL. COMMUNICATIONS CONF., IEEE, G-Com Tech., et. al. **Deadline:** Abstracts, **3/1/66.** *FOR INFO.:* IEEE Headquarters, Box A, Lenox Hill Station, N.Y., N.Y.

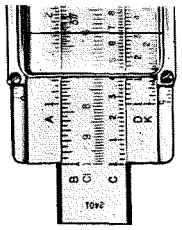
June 20-25, 1966: 3RD CONGRESS OF THE INTL. FEDERATION OF AUTOMATIC CONTROL (IFAC); London, England. **Deadline:** Abstracts, **12/1/65.** *TO:* Prof. G. Weiss, Polytechnic Inst. of Brooklyn, 333 Jay St., Brooklyn 1, N.Y.

June 21-23, 1966: CONF. ON PRECISION ELECTROMAGNETIC MEASUREMENTS, IEEE, G-IM NBS; NBS Standards Lab., Boulder, Colorado. **For Deadline Info.:** Dr. Kiyo Tomiyasu, Genl. Elec. Co., Schenectady, N.Y.

August 17-19, 1966: 7TH ANN. JOINT AUTOMATIC CONTROL CONF., (JACC); ISA, AIAA, AIChE, ASME, IEEE; Univ. of Wash., Seattle, Wash. **Deadline:** Abstracts, **4/15/66.** *FOR INFO.:* B. S. Hines, Meetings Assistant, ISA Headquarters, 530 Wm. Penn Place, Pittsburgh, Pa.

Oct. 24-27, 1966: 21ST ANN. ISA CONF. AND EXHIBIT; N.Y. Statler Hilton Coliseum, N.Y., N.Y. **Deadline: 7/15/66.** *TO:* Conf. Program Coordinator, c/o ISA Headquarters, 530 William Penn Place, Pittsburgh, Pa.

Nov. 14-16, 1966: 19TH ANN. CONF. ON ENG. IN MEDICINE AND BIOLOGY, ISA, IEEE; Sheraton-Palace Hotel, San Francisco, Calif. **Deadline:** Abstracts, **7/15/66.** *TO:* Dr. Victor Bolie, Genl. Chairman, Autonetics, 3370 Miraloma Ave., Anaheim, Calif.

Engineering  **NEWS** *and* **HIGHLIGHTS**

NEW RCA TOP MANAGEMENT ALIGNMENT TO BE EFFECTIVE JANUARY 1, 1966

The Board of Directors of RCA, at its regular monthly meeting on Sept. 3, 1965, approved a new top management alignment that will become effective on January 1, 1966.

Dr. Elmer W. Engstrom, President of RCA since December 1961, will become Chief Executive Officer of RCA and Chairman of the Executive Committee; the former position has been held by Chairman of the Board **David Sarnoff** since 1947, while the latter responsibility has been held by **Frank M. Folsom** since 1957 (who continues as a Director of the Company).

Robert W. Sarnoff, Chairman of the Board and Chief Executive Officer of the National Broadcasting Company, will become the new President of RCA to replace Dr. Engstrom. Mr. Sarnoff, who is 47 years old, has served NBC for the past 18 years. He will report to Dr. Engstrom and will assume the responsibilities of Chief Administrative Officer at RCA.

At a meeting of the NBC Board of Directors, **Robert E. Kintner,** President of NBC since 1958, was elected Chairman of the Board and Chief Executive Officer of NBC, effective January 1, 1966. Mr. Kintner will also continue as President of NBC.

General Sarnoff, who has served RCA since it was founded in 1919, becoming its President in 1930 and Chairman of the Board and Chief Executive Officer in 1947, said the new executive alignment was designed to insure continuity of the management, policies, and programs that have brought RCA in 1965 to the highest sales and profit peaks in the Company's 46-year history.

"Elmer Engstrom has worked closely with me for more than 35 years in advancing the interests of RCA," General Sarnoff added. "I am pleased that the Board's action today gives appropriate recognition to his outstanding accomplishments, and that it will permit us to continue our association in the years ahead and to continue building on the momentum that underlies RCA's operations today."

Robert Sarnoff has become intimately familiar with the operations of RCA as a member of the RCA Board of Directors since 1957, as a member of the RCA Executive Council since 1958, and as Chairman of the RCA Executive Planning Committee since April, 1964.

SEELEN NAMED DIVISION V-P, ECD TV PICTURE TUBE DIV.

Promotion of **Harry R. Seelen** to Division Vice President and General Manager, ECD Television Picture Tube Division, has been announced by **John B. Farese,** Division Vice President, RCA Electronic Components and Devices. In July, M. Seelen was appointed General Manager of the Division, succeeding Mr. Farese when the latter was promoted to his present post.

Mr. Seelen joined RCA in 1930 as a tube design engineer at the Harrison, N.J. plant. He received a BS in Physics from Providence College. He is a *Fellow* of the IEEE and a Registered Professional Engineer in New Jersey. In 1955, Mr. Seelen received the *RCA Victor Award of Merit.*

SCHADE RECEIVES SMPTE 1965 "JOURNAL AWARD"

Otto H. Schade, Sr., Electronic Components and Devices, Harrison, N. J., has been named as the 1965 recipient of the *Journal Award* of the Society of Motion Picture and Television Engineers (SMPTE).

The Journal Award Certificate is presented annually to the author of the most outstanding paper originally published in the *Journal of the SMPTE* during the preceding calendar year, in this case, Mr. Schade's paper "An Evaluation of Photographic Image Quality and Resolving Power" which appeared in the February 1964 issue, Vol. 73, No. 2.

Mr. Schade's outstanding engineering career at RCA began in 1931. In 1951 he was awarded the first David Sarnoff Gold Medal Award of the SMPTE. In 1960, he received the Progress Medal Award of the SMPTE for his outstanding technical contributions in the engineering phases of the motion picture and television industries. In June 1963 he was invested with the honorary degree of doctor of Engineering by Rensselaer Polytechnic Institute. Mr. Schade, holder of 80 patents, has received numerous other honors during his career.

NEUHAUSER AND ULMER NAMED SMPTE FELLOWS

Two RCA men are among the 18 members of the Society of Motion Picture and Television Engineers (SMPTE) just named *Fellows* of the Society. This honor has been bestowed, in recognition of their outstanding contributions to the industry and to the Society, on **Robert G. Neuhauser** of Electronic Components and Devices, Lancaster, Pa. and **Alfred R. Ulmer,** RCA Service Company, Redstone Arsenal, Ala.

GRISWOLD WINS IEEE-BTR OUTSTANDING PAPER AWARD

David M. Griswold of the ECD Commercial Semiconductor and Receiving Tube Division, Somerville, N. J., is the winner of the award for the outstanding paper presented at the IEEE Spring Conference on Broadcast and Television Receivers, entitled "Characteristics and Applications of RCA Insulated-Gate Field-Effect Transistors." Mr. Griswold received $100 and a plaque at the National Electronic Conference in Chicago on Oct. 26, 1965.

DR. GEORGE H. BROWN AND ROBERT E. KINTNER ELECTED DIRECTORS OF RCA

Election of **Dr. George H. Brown** and **Robert E. Kintner** to the Board of Directors of RCA was announced on October 1, 1965 by RCA Board Chairman **David Sarnoff.** Dr. Brown is RCA Executive Vice President, Research and Engineering. Mr. Kintner has been President of the National Broadcasting Company since July 1958.

LICENSED ENGINEERS

A. E. Berzon, DEP-CSD, Camden, PE-10988E, Pa.
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J. J. Feierbacher, EDP, W. Palm Beach, Fla., PE-7932, Fla.
F. A. Helvy, ECD, Lanc., PE-11131-E, Pa.
E. G. Miller, ECD, Lanc., PE-11001E, Pa.
D. Rosenthal, DEP-CSD, Camden, PE-13994, N. J.

DR. KOZANOWSKI RECEIVES SMPTE 1965 "KALMUS GOLD MEDAL"

Dr. Henry N. Kozanowski, Manager, Television Advanced Development, Broadcast and Communications Products Division, Camden, N. J., has been named recipient of the *1965 Herbert T. Kalmus Gold Medal Award* of the Society of Motion Picture and Television Engineers (SMPTE). The medal will be presented during the Society's 98th Semiannual Technical Conference, October 31 - November 5, 1965 at the Queen Elizabeth Hotel, Montreal, Canada.

This award, established in 1955, recognizes outstanding achievement in color motion-pictures for theater or television. Dr. Kozanowski is a Fellow of SMPTE, and in 1963 was recipient of the SMPTE *David Sarnoff Gold Medal Award* in recognition of his accomplishments to improve the quality and practical operation of TV studio and film camera equipment.

Some of the advanced developments in color TV for color film credited to Dr. Kozanowski include: 3-vidicon color TV equipment for 16 and 35mm color film; completely stabilized 3-vidicon color TV film reproduction equipment; demonstration of live pickup separate luminance 4-tube color camera; completely transistorized separate luminance channel 4-vidicon color film chain using modular construction and including transistorized colorplexer and color bar generator; and many others.

SCHROEDER RECEIVES SMPTE 1965 "SARNOFF GOLD MEDAL"

Alfred Christian Schroeder, member of the Technical Staff, RCA Laboratories, Princeton, New Jersey, will receive the *1965 David Sarnoff Gold Medal Award* of the Society of Motion Picture and Television Engineers (SMPTE) in recognition of meritorious achievement in television engineering. The Award will be presented to Mr. Schroeder at ceremonies to be held during the SMPTE 98th Semiannual Technical Conference in Montreal, October 31 to November 5, 1965.

The Award is being conferred upon Mr. Schroeder for his many contributions to the fundamental concepts and decisions which have gone into the development and refinement of color picture tubes and of the NTSC color systems. His efforts have earned him over 60 patents, 30 of which were for developments in color television. Mr. Schroeder has been honored with five successive *RCA Laboratories Achievement Awards,* all in recognition of his work in the color TV field.

DR. WEIMER RECEIVES IEEE LIEBMANN AWARD

Dr. Paul K. Weimer, RCA Laboratories, Princeton, N. J., has been selected by the IEEE as recipient of the *1966 Morris N. Liebmann Award* with the following citation: *"For invention, development, and applications of the thin film transistor."* The award consists of $1,500.00 and a certificate. Presentation of the award was made at the National Electronics Conference in Chicago, Illinois, on October 27, 1965. Dr. Weimer has authored and co-authored a number of papers on TFT development and application in RCA ENGINEER, *RCA Review, Proceedings of the IEEE,* and other journals.

—C. W. Sall

DR. MAMELAK RECEIVES ASA COMMENDATION FOR COMPUTER STANDARDS

Dr. J. S. Mamelak, DEP Applied Research, has received a commendation from the American Standards Association for his outstanding work as an active technical member of Subcommittee X3.5. The following is a direct quote from the letter of commendation:

"The need for a standard vocabulary in information processing has been widely recognized for many years. The application of your technical competence and outstanding skill in the field of automatic data processing has made the preparation of these superb standards in information processing possible. Your continued efforts to prepare additional standards at the national and international level are vital to the dynamic development and expansion in the field of automatic data processing. On behalf of the ASA, the Sectional Committee X3, and the Subcommittee X3.5, congratulations on an excellent piece of work."

His contributions included preparation of term definitions, and revieving and processing drafts of proposed national and international standards in the computer and information processing fields.

—M. G. Pietz

RCA IS FIRST TO OPERATE INTERNATIONAL COMMERCIAL TELEGRAPH SERVICE VIA EARLY BIRD SATELLITE

RCA Communications, Inc., in July placed in operation the nation's first international commercial telegraph service via the EARLY BIRD satellite. The service was inaugurated with the transmission of the first regular paid telegrams between the United States and Germany.

RCA Communications, Inc. will use channels in the EARLY BIRD for its data, facsimile, and telex service as well as for the message telegraph service. In the near future, RCA also plans to provide bandwidths capable of high-speed overseas computer-to-computer communications via the satellite.

MSR ADMINISTRATIVE CHANGES AFFECT ENGINEERING AND PROGRAM MANAGEMENT

Administrative realignments to provide greater efficiency and more effective use of resources have been effected at the DEP Missile and Surface Radar Division, Moorestown, N.J.

1) A major portion of the Program Operations staff has been transferred into the Project Operations Staff in the Engineering Department, and *the Engineering Department will be known in the future as Technical Operations,* under Chief Engineer **Russell A. Newell.**

2) Division Program Managers have been named to the General Manager's staff to give greater executive management attention to the major areas of MSR's business operations. The Division Program Managers act in the role of Deputy General Managers for their assigned areas of business. They have the responsibility to give direction, develop policy and insure that proper action is carried out on current programs and in the acquisition of new programs. The Division Program Managers are: **Edward D. Carfolite,** Tactical Programs; **William H. Congdon,** Strategic and Defensive Programs; **William V. Goodwin,** Naval Air Defense Programs; **Andrew L. Hammerschmidt,** Program Operations; and **Edward W. Petrillo,** Range and Re-entry Programs.

Who Should Own and Operate Communications Satellite Ground Stations?

. . . RCA says International Carriers, and applies to FCC for authority to do so —and asks FCC to deny COMSAT exclusive ownership

RCA Communications, Inc., today formally asked the Federal Communications Commission for authority to acquire ownership and operating interest in the communications satellite ground station at Andover, Me., and those to be built at Brewster Flat, Wash., and Paumalu, Hawaii. In its application, RCA Communications, Inc. said international carriers should be permitted to participate in the ownership and operation of earth stations in proportion to their present and future traffic requirements.

At the same time, RCA Communications filed an accompanying petition asking the FCC to deny a request by the Communications Satellite Corporation (COMSAT) for the exclusive right to own and operate the three initial satellite earth stations.

Thompson H. Mitchell, President of RCA Communications, Inc. said participation by the international carriers in owning and operating these stations would be in the public interest because:

1) it would take full advantage of the reservoir of experience, expertise and know-how possessed by the international carriers and developed over long years of public service.
2) it would encourage RCA Communications, Inc. and other interested carriers to make maximum use of satellite facilities in which they had a capital investment.
3) it would enhance the ability of RCA Communications, Inc. to discharge its statutory obligation of providing rapid, efficient, nationwide and worldwide wire and radio communication service with adequate facilities at reasonable charges.

Mr. Mitchell said "the public interest, convenience and necessity" require participation by international message carriers in owning and operating the ground stations.

In the petition, Mr. Mitchell and COMSAT's request for exclusive ownership and operation of the three ground stations is "inconsistent with the public interest, convenience and necessity." The denial petition said exclusive ownership and operation by COMSAT would subject the authorized communications carriers to substantially higher operating costs in providing communications service. Mr. Mitchell said in the petition that "unless COMSAT's ambitions in satellite communications are properly contained within the framework of the Communications Satellite Act, COMSAT could dominate and control all satellite communications and eventually all international communications."

. . . PROMOTIONS . . .

to Engineering Leader & Manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parentheses.

Electronic Data Processing

F. Symes: from Sr. Mbr., D&D Eng. Staff to *Ldr., Tech. Staff* (J. R. Hammond, West Palm Beach, Fla.)

DEP Communications Systems Division

A. H. Kettler: from Staff Engr. to *Mgr., Program 422* (J. M. Osborne, Program Management, Camden)

W. T. Newkirk: from Sr. Programming Planner to *Ldr., Programming Planning, 422* (A. M. Fleishman, Systems Program Dev., Camden)

D. Shore: from Chief Systems Eng., (SEER) to *Chief Engr., Engineering Department, CSD* (J. M. Hertzberg, Div. Vice Pres., CSD, Camden)

DEP Applied Research

E. J. Schmitt: from Class AA Engr. to *Ldr., Dev. & Design Engrs.* (J. A. Brustman, Mgr., Advanced Product Res., Camden)

H. S. Zieper: from Class A Engr. to *Ldr., Dev. and Design Engrs.* (J. A. Brustman, Mgr., Advanced Product Res., Camden)

DEP Defense Microelectronics

R. C. Heuner: from Mbr. Tech. Staff to *Ldr., Tech. Staff* (Mgr., Integrated Electronics Eng., Som.)

DEP West Coast Division

R. Ellis: from Admin., Value Eng. & Procedures to *Mgr., Pub. Engrs.* (G. Fairhurst, Van Nuys, Calif.)

DEP Aerospace Systems Division

P. Frawley: from Sr. Proj. Mbr., Tech. Staff to *Ldr., Tech. Staff* (C. E. O'Toole, LEM Program, Burl.)

R. K. Gorman: from Sr. Proj. Mbr. to *Ldr., Tech. Staff* (D. J. Cushing, Systems Support Eng., Burl.)

E. Tahan: from Sr. Proj. Mbr., Tech. Staff to *Ldr., Tech. Staff* (M. E. Siegal, Radar Eng., Burl.)

Electronic Components and Devices

W. H. Hackman: from Assoc. Engr., Product Dev. to *Mgr., Production Eng.-Conversion Tube* (Mgr., Camera Tube Operation, Lanc.)

L. Iannuzzelli: from Assoc. Engr., Prod. Dev. to *Admin., Adv. & Sales Promotion* (E. B. May, Comm. Eng., Harrison)

W. O. Watts: from Mgr., Engr. Standards to *Mgr., Mfg. Standards* (G. W. Farmer, Rec. Tube Prod. Engr., Harrison)

RCA Service Company

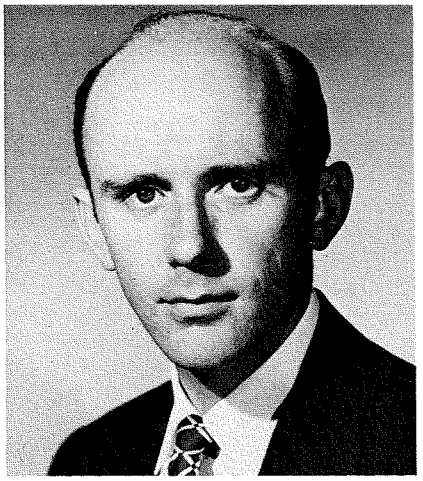
C. P. Brooks: from Engr. to *Ldr., Engrs.* (K. F. Wenz, Pulse Radar-Missile Test Project, Cocoa Beach, Fla.)

K. A. Jacobson: Installation & Modification Engr. to *Mgr., Computer Site Operations* (J. James, Reliability Facility, Cherry Hill)

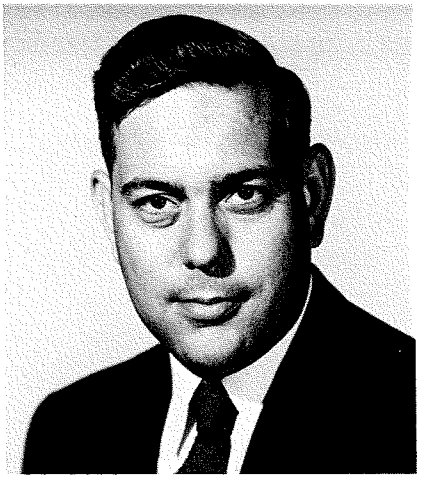
E. J. Rainwater: Engr. to *Ldr., Engrs.* (E. Sears, NASA Base Communication, Cocoa Beach, Fla.)

N. L. Sawyer: from Assoc. Engr. Shipboard to *Mgr., Communication & Telemetry* (L. F. Dodson, Signature Data Acquisition—Missile Test Project, Cocoa Beach, Fla.)

H. A. Wiedmer: from Installation & Modification Engr. to *Mgr., C&M Eng.* (N. J. Rauch, White Alice Project, Anchorage, Alaska)



R. Aires



D. Shore

AIRES NAMED CHIEF ENGINEER OF DEP WEST COAST DIVISION; MOORE HEADS DEFENSE MICROELECTRONICS

The formation of a West Coast Division of RCA Defense Electronic Products incorporates in one management structure the functions of the RCA facilities at Van Nuys and West Los Angeles, Calif. **Arthur L. Malcarney,** Group Executive Vice President, appointed **S. N. Lev** (formerly Division Vice President, Defense Manufacturing and Program Management for DEP) as Division Vice President and General Manager of the new West Coast Division.

Ramon H. Aires has been named as Chief Engineer of the DEP West Coast Division. Mr. Aires was formerly Manager of the DEP Defense Microelectronics activity in Somerville. He is succeeded in this position by **Elvet E. Moore,** who was Manager of Integrated Circuit Techniques for Defense Microelectronics. (*Both were authors in the integrated-circuit issue of the* RCA ENGINEER, *Vol. 10, No. 3, Oct.-Nov. 1964*).

Mr. Aires came to RCA in 1954 from Philco Corporation, Philadelphia, Pa., where he participated in advanced television department. His past assignments at RCA have included management of design groups for advanced antennas and servomechanisms for fire-control radar, and electrical design manager of the RCA activity which built the first TIROS weather satellite. Mr. Aires holds a BSEE from Cornell University and an MSEE from the University of Pennsylvania. A member of the IEEE, Mr. Aires has several patents for television and servomechanism circuits.

WCD headquarters are at the Van Nuys facility (previously part of the DEP Aerospace Systems Division, which still has headquarters in Burlington, Mass.) The Van Nuys facility specializes in data processing and display devices, and is building 110A computers for checkout and launching of SATURN rockets, computerized message switching systems for United Air Lines, electronic countermeasure devices, and other computer and display devices.

The West Los Angeles plant has been the headquarters of RCA's Aviation Equipment Department. Among the avionics equipment manufactured at the facility are the RCA AVQ-10, AVQ-20 and AVQ-55 weather radars, the AVQ-70 and AVQ-75 Distance Measuring Equipment (DME), the AVQ-60 Air Traffic Control Transponder, and other airborne equipment.

Mr. Lev announced that **Charles A. Wolf** will continue as Manager, Operations, for the Van Nuys facility as will **Joseph R. Shirley** as Manager, Aviation Equipment Department. **John D. Woodward** also continues as Manager, Commercial Aviation Marketing.

SHORE APPOINTED CHIEF ENGINNEER OF DEP COMMUNICATIONS SYSTEM DIVISION; MILLER NAMED TO RUN SEER

Appointment of **David Shore** as Chief Engineer, Engineering Department of the DEP Communications Systems Division, was announced on August 25, 1965, by **Joseph M. Hertzberg,** Division Vice President and General Manager. Mr. Shore succeeds **O. B. Cunningham,** who has been appointed Manager, Technical Planning of the DEP Defense Engineering activity. Mr. Shore was formerly Chief Systems Engineer of the Systems Engineering, Evaluation, and Research (SEER) activity of Defense Engineering, located at Moorestown, N.J. This activity directs company-wide efforts on many major government systems.

Sidney G. Miller succeeds Mr. Shore as Manager, SEER. He was formerly Manager of SEER's Operations Analysis.

In 1954, Mr. Shore joined RCA as a staff engineer in the Missile and Surface Radar Division, Moorestown, N.J., after serving as the Assistant Chief of the Weapon Systems Planning Office at the Air Force's Wright Air Development Center. At RCA, he has had responsibilities including overall systems design of the Ballistic Missile Early Warning Systems (BMEWS), Associate Directorship of Advanced Military Systems, and Manager of the SAINT satellite project. A graduate of the University of Michigan, Mr. Shore holds a BS in Aeronautical Engineering from that institution, and an MS in Physics from Ohio State University.

Mr. Cunningham joined RCA in 1935 and was active in communications and navigation equipment design. Among his supervisory positions were Manager, Aviation Communications Engineering and Chief Engineer of the Surface Communications Division, from which the Communications Systems Division was evolved. He holds a BSME from the University of Kentucky, and is a senior member of the IEEE.

RCA RADARS FOR GEMINI

RCA-built radars scored two firsts during the GEMINI 4 mission: *1*) skin tracking (vehicle surface reflection) the GEMINI capsule and *2*) providing detailed radar observations of the reentry and breakup of the booster. In all, 14 fixed tracking stations supported GEMINI 4 with 16 RCA-built radars. Another RCA tracking radar mounted on a ship also was used. DEP-MSR, Moorestown, N.J., produced the radars.

APPLICATIONS OPEN FOR 1966-1967 SARNOFF FELLOWSHIPS

Applications for the *1966-1967 David Sarnoff Fellowship* program for RCA employees are now open, according to **Dr. Douglas H. Ewing,** Chairman of the RCA Education Committee. These Fellowships are awarded each year to at least ten outstanding employees selected to work toward post-graduate degrees at approved universities.

Six *Fellowships* are awarded in Science and Engineering, three in Business Administration and one in Dramatic Arts or Journalism. The latter *Fellowship* is for award to an employee of NBC, while the other nine are open to all employees of RCA and subsidiaries. Each *Fellowship* is for one academic year, but application may be made for renewal for one additional year. Employees awarded these *Fellowships* are given leaves of absence without pay for the duration of the award.

The stipend granted to a recipient of a *David Sarnoff Fellowship* is $2,500 to $4,000, depending on marital status, in addition to RCA payment of full tuition and allowance toward purchase of textbooks. An undesignated gift of $1,000 also is made to the university where the recipient studies.

Recipients are selected by the RCA Education Committee on the basis of academic aptitude, promise of professional achievement and character and must qualify for graduate study in a graduate school acceptable to the RCA Education Committee. Preference will be given to Science and Engineering applicants who have indicated, by successful completion of courses at graduate level, their ability to proceed on a doctoral program. In the case of Business Administration and Dramatic Arts or Journalism applicants, the end degree need not necessarily be the doctorate. The head of the employee's division or subsidiary will nominate outstanding candidates to the RCA Education Committee.

Employees interested in applying for these prized awards for the 1966-67 academic year may obtain application forms from their divisional Personnel office. **The application must be complete and returned to their Personnel office by December 1, 1965.** Awards will be announced in February, 1966.

DEGREES GRANTED

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R. Tipping, DEP-DME ..... MS, University of Pennsylvania
J. T. Nessmith, Jr., DEP-MSR ..... Ph.D., University of Pennsylvania
H. M. Finn, DEP-MSR ..... Ph.D., University of Pennsylvania
F. Ginters, DEP-MSR ..... MSEE, University of Pennsylvania
W. H. Hodge, DEP-MSR ..... MS, Mathematics, Temple University
R. H. Fitzmaurice, R&E ..... BS, Business Admin., Drexel Institute of Technology

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