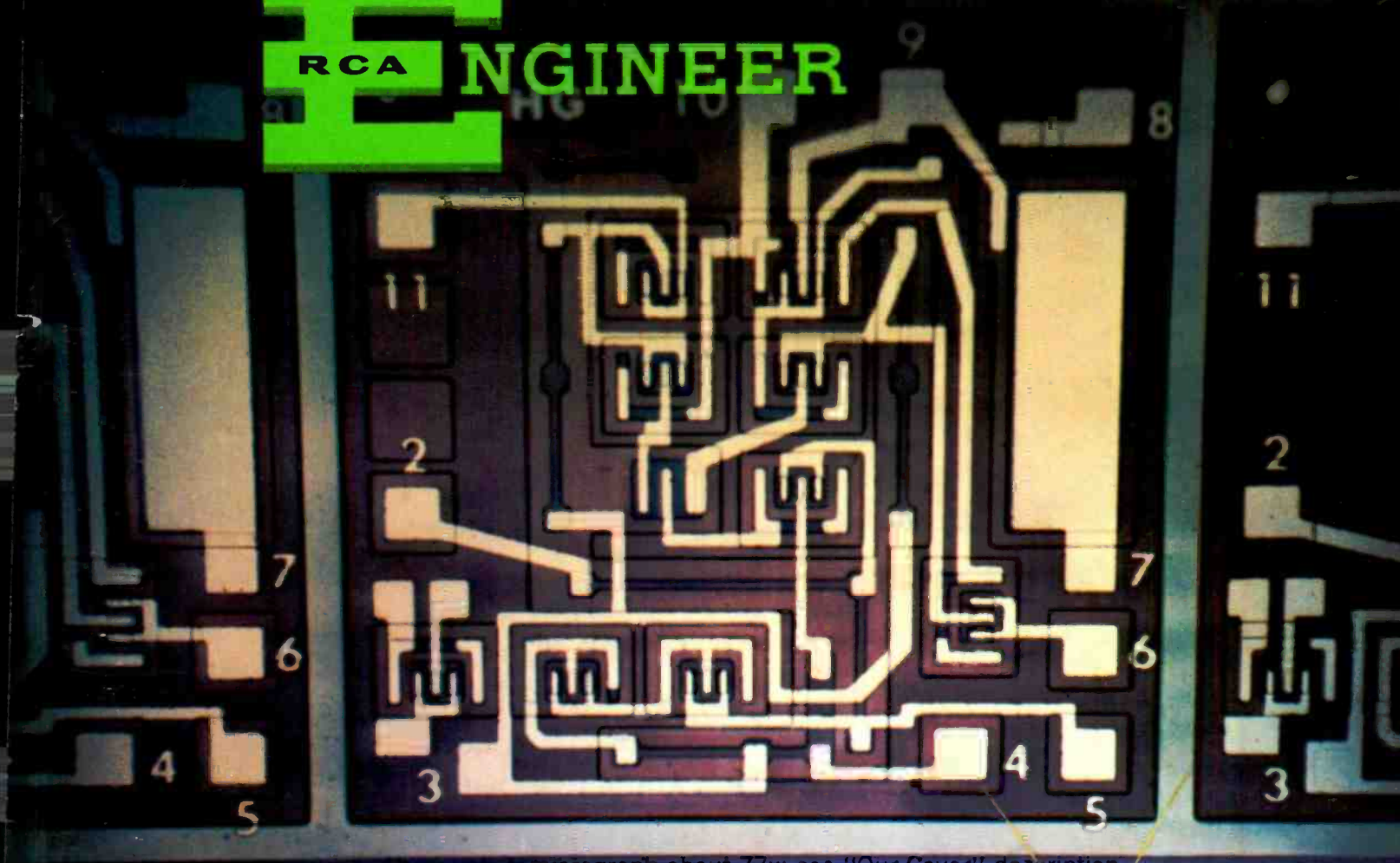
RCA ENGINEER



Cover: photomicrograph about 77x; see "Our Cover" description

Vol. 10 — No. 3
OCT. — NOV. 1964

OUR COVER

. . . a grouping of EC&D's new monolithic silicon integrated circuits contained in the RCA flat package that measures ¼ x ¼ inch (less leads); a colorful praying mantis standing among the packages provides an interesting size contrast. The center square of the upper background is a photomicrograph (about 77x enlargement) of an amplifier circuit, representing 20 discrete, interconnected components. The circuit is duplicated many times on a silicon disk, a portion of which is shown; the disk is then diced into pellets, 62 x 62 mils, each containing the complete circuit, and sealed within the flat packages. Three unsealed packages appear in the foreground; barely visible in their center is the tiny silicon pellet. The flexible leads on each end of the flat packages are for connection to other circuits. (Cover art direction, Jack Parvin. Photography, Radman Allen.)

Integrated Electronics and RCA

The RCA ENGINEER is again fulfilling one of its most important functions by presenting a group of papers relating to a new phase of technology which, without doubt, will have a significant impact on our corporate business future and on our professional engineering future. Last fall, steps were taken to initiate an integrated-electronics program which would make the best use of the technical talents residing in RCA Laboratories, EC&D, and DEP. The primary responsibility for implementing the program resides with the Special Electronic Components Division of EC&D at Somerville. The new DEP activity, Defense Microelectronics, in residence at Somerville, is formulating the specific circuit designs to be fabricated for DEP in the initial phase of this long-term program.

Many presentations have been made in the past six months to acquaint engineers in all divisions of RCA with the projected program, with the accomplishments to date, and with the immense potential of the integrated-circuit approach which will result in a higher degree of automation in the making of basic circuits, in interwiring of equipment, and even in engineering design. Now we have this excellent group of technical papers designed to inform an even greater circle of participants. This work by our own RCA authors, coordinated by the staff of the RCA ENGINEER and the Editorial Representatives, illustrates in the best manner what I had in mind when I referred on this page a little over a year ago to "*a continuous and articulate dialogue between the growing number of specialists within our discipline.*"

George H Brown

Dr. George H. Brown
Vice President
Research and Engineering
Radio Corporation of America

RCA ENGINEER

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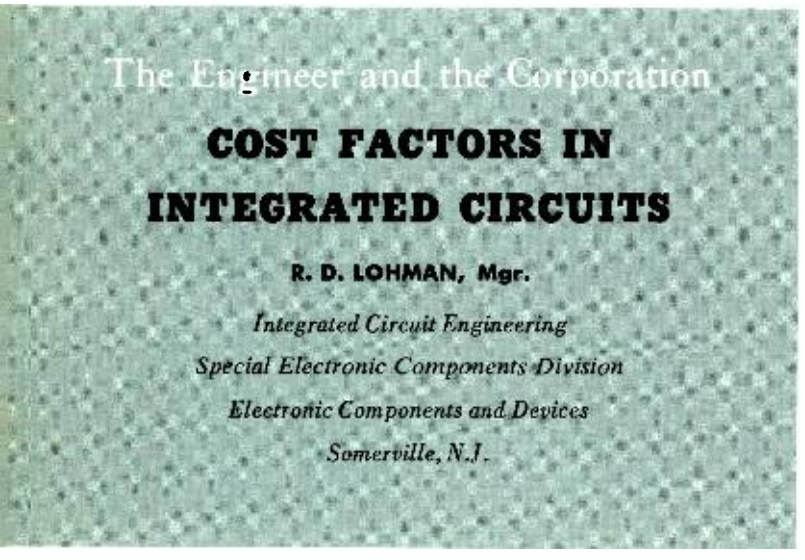
CONTENTS

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

● To disseminate to RCA engineers technical information of professional value. ● To publish in an appropriate manner important technical developments at RCA, and the role of the engineer. ● To serve as a medium of interchange of technical information between various groups at RCA. ● To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions. ● To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field. ● To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management. ● To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

An index to RCA ENGINEER articles appears annually in the April-May issue.

Editor's Note: Engineers are sometimes thought of — erroneously — as putting their technological ideas above everything, including practical cost considerations. We submit that design engineers do display cost consciousness, and in fact possess unusual ability to seize upon and pass along the benefits of cost reductions to the users of their circuits, equipments, and systems. This paper introduces our "integrated circuits" issue by showing how design engineers — as both circuit producers and users — hold an important key to achieving attractive costs.



COST FACTORS IN INTEGRATED CIRCUITS

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Integrated Circuit Engineering

Special Electronic Components Division

Electronic Components and Devices

Somerville, N.J.

THE most important advantage of integrated circuits is their potentially low cost. Although other design features such as small size, low weight, and high reliability are of primary importance in certain selected applications, the general use of integrated circuits in all types of electronic equipment will be brought about primarily because of cost reduction.

As is the case with most new technological developments, the low cost of integrated circuits must be inferred from some general concepts before it can be proved by experience. This paper explores the cost centers for monolithic silicon integrated circuits and how these differ with respect to a discrete component such as a transistor, and, most importantly, discusses the role of the circuit and equipment design engineer in determining these costs.

Integrated circuit costs can be divided roughly into three major categories: 1) *development cost*, the cost of bringing an integrated circuit from the point of broad concept to the point where it can be mass produced; 2) *fabrication cost*, that incurred in actually producing the integrated circuit in a factory; and 3) *overhead costs*, those associated with marketing, distributing, and selling the integrated circuit. As will be seen, the engineers who design and use integrated circuits have a strong effect on the magnitude of *all three* of these costs.

ENGINEERING DEVELOPMENT COSTS

Before examining the engineering development cost of an integrated circuit, it is necessary to define carefully what is meant by a *new circuit*. The technology to develop and fabricate integrated circuits involves a number of complicated processing steps. A particular process imposes, within broad categories, limitations on the components to be used in a given circuit. Within these broad categories the specific components and their interconnections for a particular circuit are determined by the masks used during fabrication. Thus, for each fabrication process, there is a limited set of possible components which the circuit designer has at his disposal. By making the process more complicated, additional components or a larger set of components are available; however, when the circuit function can be accomplished by using those components available from the simpler process, the resulting circuit will be economically more attractive.

To develop a new process is a time-consuming and expensive enterprise. On the other hand, the development of a new circuit within an established, well-controlled process can be achieved in a relatively short time and at a correspondingly lower cost. If the equipment design engineer can use an available off-the-shelf circuit, he reduces the development cost for his application to very nearly zero.

When the design engineer devises a circuit for a specific application and when this circuit can be fabricated within an existing process by only mask changes, then the development cost will lie between $2,000 and $10,000. In many cases, this cost is worth incurring because it may reduce subsequent production expense or additional overhead cost later on. Obviously, the liquidation of the development cost on a per-unit basis depends on the number of circuits actually used; this number should be as high as possible in order to minimize the development cost per unit.

DEVELOPMENT AND FABRICATION TRADE-OFFS

Many of the decisions made at the development stage affect not only total design and development costs but also later production costs. Most of the well-known economic rules used successfully by engineers designing circuits with discrete components do not minimize costs when applied to monolithic silicon integrated circuits. In general, minimum integrated circuit cost is achieved when the greatest number of usable circuits is obtained per silicon wafer. The number of usable circuits is the number of gross circuits times the yield. Thus, any attempt to minimize cost usually starts with reduction of circuit size to the smallest possible area to increase the gross circuits per wafer. Because transistors generally occupy less space than any other component, they are more economical to incorporate in the circuit than either resistors or capacitors.

Once a minimum-size design has been obtained, the tolerances placed on the components in order to produce a working circuit must be examined. At this point, various trade-offs can usually be made which depart from the absolute minimum size but result in wider tolerances on the components and thereby result in a higher yield. Although a sophisticated approach to this problem has yet to be developed, the optimum seems to lean generally toward active devices rather than passive ones, and greater numbers of devices rather than tight-tolerance devices. It is apparent that the very closest communication and cooperation between the user and the maker of integrated circuits is an absolute necessity.

PRODUCTION COSTS

The costs of producing monolithic silicon integrated circuits are quite analogous to those incurred in the manufacture of silicon planar transistors. Both are produced by similar batch processing techniques and, to a certain extent, most of the rules which lead to low transistor costs also result in lower monolithic silicon integrated circuit costs.

Many projections predict that integrated circuit production costs will approach those of a single silicon planar transistor. This reasoning, when applied to a transistor the same size as an integrated circuit chip, is logical when an equal production yield is assumed. Except for some additional processing steps involved in attaining isolation, it would be difficult to distin-

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guish between a fairly large silicon planar transistor and a monolithic silicon, completely integrated circuit (after both had been processed through the metallizing stage but prior to mounting, bonding, and encapsulation). It is even reasonable to assume that the yield at this point could be the same. Cost additions accrue at subsequent steps, however; and such costs must be very carefully weighed lest a superficial comparison lead to serious errors in judgment.

The transistor can be assembled with 1/5 the number of bonds, and its package will have 1/4 to 1/5 the number of hermetically sealed leads. Even so, the differential can still be kept very small in comparison with fixed overhead costs provided the final acceptance test yield can be kept high.

MARKETING COSTS

A major difference arises between transistors and integrated circuits in the area of test yield. In marketing transistors, it is common to sell the production from a given product line under many different type numbers. Each type corresponds to a specification, and supposedly this specification is tailored to some particular application. When there are enough applications, the producer may sell a very large percentage of his output even though only a small portion may meet the requirements of any given application.

It is difficult to see an analogous situation developing for integrated circuits. While it is true that some selection may be made because of restricted environmental conditions for various applications, the idea of generally selecting integrated circuits to satisfy a large number of application categories does not appear feasible. Therefore, the yield for a given application must be high, and neither the electronic device manufacturer nor the user can depend on the statistics previously used to reduce transistor costs.

Once again, it is apparent that the communication channels between producer and user of integrated circuits must be much closer than those which have been established in the past for discrete components. When the user is fully cognizant of the conditions which must be met for high integrated circuit yield and if the design of the circuit is accomplished with these requirements in mind, there is every reason to believe that monolithic silicon integrated circuit costs can be reduced substantially below those incurred with discrete components.

CLOSE TECHNICAL COUPLING VITAL FOR CIRCUIT DESIGNER AND USER

The discussion to this point has emphasized the need for increased communication between the user and the producer of integrated circuits in order to reduce development and production costs. It is inevitable that additional costs will be incurred to achieve the improved communication vitally needed.

Integrated circuits cannot be marketed and sold in the same manner as discrete components; instead, the integrated circuit user must be much more cognizant of the technical details of his vendors' processes than ever before. Additionally, the user must provide the producer with more information than has previously been the custom.

Those integrated circuit producers and users who first learn the value of *closer technical coupling* will possess economic and design advantages over their respective competition which may well prove to be decisive in the future.

Fortunately, RCA is particularly well suited to adapt to the concept of close technical coupling between engineering groups; the RCA integrated circuit program is oriented well toward attaining this end. The combined role played by the design engineers, who are both circuit users and producers, is the key to success in attaining these goals.

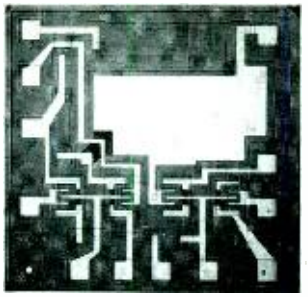

Fig. 1—An integrated circuit containing transistors, resistors, and capacitors. The 50-picofarad capacitor consumes an area equivalent to that used for 8 transistors.

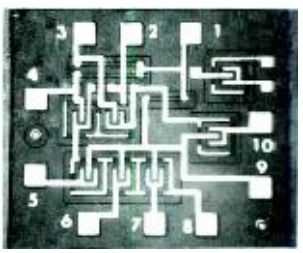

Fig. 2. — Typical integrated-circuit logic gate. Note the relatively large number of transistors.

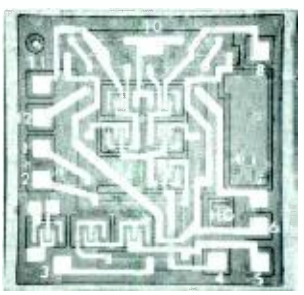

Fig. 3 — A more complex integrated circuit which can be connected to perform several analog functions.

ROBERT D. LOHMAN received the B.S. degree in Electrical Engineering from Norwich University in 1949 and the M.S. degree in Electrical Engineering from North Carolina State College in 1951. In June of 1951 he joined the RCA Laboratories as a member of the technical staff. From 1951 to 1956, he was engaged in research in the areas of basic semiconductor noise phenomena, transistor circuit development, color television display systems, and information theory. In 1956 he joined the RCA Semiconductor and Materials Division as an applications engineer. In 1957 he became Manager of applications for computer devices. In 1960, he was promoted to Engineering Manager, Computer Products. He assumed his present position, Manager Integrated Circuit Engineering, in January, 1964. Mr. Lohman has been issued thirteen U. S. Patents and has published twelve papers in the field of Semiconductor applications.

RCA'S INTEGRATED CIRCUIT PROGRAM

Reviewed herein is RCA's coordinated program for developing, designing and applying integrated circuits. The philosophy and relationship between circuit conception, device fabrication, and system application require close collaboration of many RCA research and engineering activities. Applications necessarily involve all major product areas such as data processing, defense electronics, consumer products, commercial and industrial electronics, space electronics, and special electronic components. Each area of interest is reviewed.

H. KIHN
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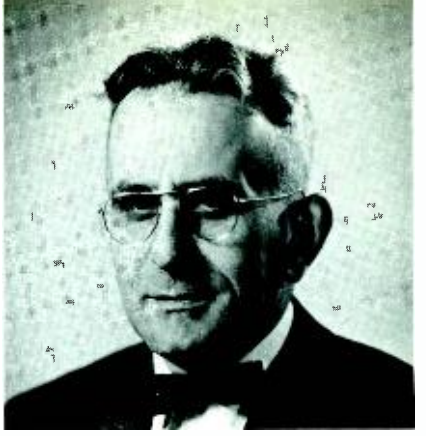

HARRY KIHN received his BSEE from the Cooper Union Institute of Technology in 1934, and his MS from the University of Pennsylvania in 1952. Mr. Kihn joined RCA in 1939 as a research engineer associated with television receiver and circuitry development. During World War II, as a member of the technical staff of RCA Laboratories at Princeton, he performed research relating to radar for automatic bombing and altimeters. With the advent of color television development in the post-war period, he played a prominent part in the development of receiver circuitry. Subsequently he was engaged in further radar research and directed research in pulse code and digital communication and computer systems. Since early 1960, he has been a Staff Engineer on the RCA Research and Engineering Staff, in charge of coordinating RCA technical activities in data processing, semiconductor devices, and other fields, including both defense and commercial applications. Mr. Kihn is the Corporate Staff coordinator of the Integrated Circuit program. He is a Fellow of the IEEE, and is a Member of Sigma Xi.

THE great involvement of RCA in all aspects of electronic systems, components, and materials insures its great interest in revolutionary developments in circuitry. Thus, during the past decade, when the trend toward microminiaturization began to exert pressure on the electronics industry, RCA pioneered in a number of areas.

In the early beginnings of the "microminiaturization era," analog rather than digital circuitry was visualized as the most important for immediate conversion, since the data processing industry with its extensive use of digital circuitry was only a fraction of its present size. The nature of the end use of microminiature devices therefore determined the emphasis on modular assemblies of close-tolerance elements of resistance, capacitance, inductance, active devices, and frequency control components. It is well to remember that even today when silicon-based bipolar active and passive circuitry seems to dominate the digital circuitry field, it has major limitations in application to high-frequency, high-gain tuned circuits and circuitry involving large values of capacity and inductance.

However, because of the phenomenal growth of digital circuit applications in the data processing, the defense, and the space electronics industry, and the development of digital circuits involving only transistors, diodes, and resistors, the silicon-based approach to circuit integration has come into prominence. These three circuit elements are most easily implemented by the techniques of diffusion, photolithographic masking, oxide formation, and etching which are characteristic of the silicon transistor technology that has developed very rapidly during the past several years.

The integrated circuit industry has been characterized by several competing technologies, by major new research developments, and by rapid technological obsolescence. To a considerable degree, this will continue into the future. The great investment of the semiconductor industry in silicon transistors has recently shifted the cost-vs.-performance balance in the direction of silicon-based integrated circuitry. Thin-film, ceramic-based, and hybrid circuitry will continue to be used where they have unique advantages in close tolerances, in higher-power and wide-temperature-range requirements in digital, but mainly in analog, integrated circuitry.

Final manuscript received September 8, 1964.

In a previous paper[1] surveying developments in integrated electronics at RCA, a wide spectrum of circuit techniques was described, as well as integrated memories and integrated ferroelectric and optoelectronic circuits and displays. These are still of interest at RCA, but this paper will confine itself to the present major RCA effort in silicon-based and thin-film integrated circuitry.

INTEGRATED CIRCUIT PHILOSOPHY

The development of circuits particularly suited to silicon-based device technology brings into focus several important tenets of integrated-circuit pholosophy:

There is an intimate relationship between *circuit conception and device fabrication*, requiring the close collaboration of the materials, device and circuit engineers.

The considerable *cost of making even small changes* in the circuit design, is quite *unlike* the situation which exists in discrete circuitry as presently used This cost depends on:

1) Whether the circuit requires modification of the masks only (such as is involved in a variation in the number, magnitude and interconnections of a *given* set of active and passive elements),
2) Whether they involve a change in processing (inclusion of new active elements such as p-n-p/n-p-n transistors, charge storage diodes, radically different doping density, or changes from saturated to unsaturated mode operation, etc.)

or

3) Combinations of *1* and *2*. Changes involving *2* are more costly than *1* and require a longer development cycle.

New systems considerations and circuit concepts should be sought because of the ease of fabrication of active components such as transistors and diodes and the limitations of diffused resistors and capacitors as far as temperature, tolerances, and magnitudes attainable are concerned. This is the reverse of discrete-component circuits where passive components are generally of high precision and relatively inexpensive, while active devices are costly. Historically, existing circuit concepts and designs have been developed with the latter environment in mind, hence the need for a *new* point of view.

Digital circuits are generally repetitive and concerned with only two levels of voltage or current and do not require accurate control of transitional regions as do analog circuits (transconductance linearity for example). *Digital circuits are therefore more readily integrated than analog, in competition with discrete circuits.*

For these reasons, *digital integrated circuits are more competitive in cost compared to discrete cricuits than are analog circuits,* particularly since the latter are generally more specialized and are used in smaller quantities which results in higher cost. For widespread use of analog circuits in *consumer* products, however, the volume can be large enough to result in low cost, too.

In the case of monolithic silicon integrated circuits, because of possible area defects in the silicon wafer it is advantageous to have each circuit occupy a minimum of area to improve the yield. This also reduces the cost per circuit, since the wafer processing cost is largely independent of the number of circuits.

There is, of course, a lower limit below which it is impractical to go because of power dissipation, difficulty of bonding, and the limitations of the resolution of masking.

To provide a minimum of propagation delay it is advantageous to operate transistors in a nonsaturated mode. (This consideration largely determined the approach to high-speed gate requirements of electronic data processing designers.)

Fig. 1 shows one of many industry surveys of present and future markets for integrated circuits. Although there are some differences of opinion as to specific figures in the various categories of defense, consumer, and industrial applications and the specific technology which will be used (silicon-based, thin film, or hybrid circuits which include modular circuits), the trend is unmistakable and has been largely accepted by the industry. This conclusion has been fortified by the great strides in engineering and production which have occurred in the semiconductor industry in the past five years.

RCA has therefore committed itself to extensive corporate effort and to considerable investment in integrated circuitry, both because of the crucial nature of these devices in the systems and equipment built by our manufacturing divisions and to provide the component division with product for sale in the decades to come.

APPLICATIONS BY RCA ACTIVITIES

Fig. 2 shows the various RCA product activities which are now or will ultimately be users of integrated circuits. These are discussed in the following paragraphs.

Defense Electronics

It was inevitable that the first application of integrated circuits be to defense equipment because of the inherent requirements of high reliability, small size and light weight. Those requirements had, in fact, prompted defense agencies to initiate many of the important industry programs in integrated circuits. *It is axiomatic in the present defense procurement that integrated circuitry be an essential part of many programs in military electronics.* It is for this reason that engineers of Defense Electronic Products are actively participating in the planning, design, and application of integrated circuits at Somerville in the Defense Microelectronics group[2] under R. H. Aires, Mgr., which serves all DEP as a staff function. This DME group is working closely with the Integrated Circuits Dept. (R. D. Lohman, Mgr.) of RCA Electronic Components and Devices[3] which designs and fabricates the circuits. As mentioned previously *the intimate interrelation between concept and process, between circuit and device, requires the close working together of circuit and system engineers and fabricators of semiconductors.* This joint effort has proved successful indeed and has advanced our timetables for production of monolithic silicon integrated circuits by several months.

Electronic Components

Components such as tubes and transistors have long been a mainstay in RCA's corporate income. Since monolithic silicon integrated circuits can in turn supplant many discrete transistors, in digital applications, RCA Electronic Components and Devices organized the Integrated Circuits Department, with R. D. Lohman as Manager, as part of the Special Electronic Components Division headed by L. R. Day, to insure its primacy in future active components. Large investments (both corporate and divisional) in capital, engineering and manufacturing are being made to insure that RCA is *second to none* in the integrated circuit business.

While the demands of the internal RCA requirements will saturate the output of the EC&D integrated circuit facility for about a year, it is expected that EC&D will ultimately pursue its traditional course of marketing these circuits through the same channels as their tube and transistor product line. Although the present trend is toward custom circuits, this is not far different from the transistor industry's present practice. In the latter case, however, *selections* from a given fabrications can provide large volume of specialized product. This has not yet been attained in integrated circuits and there is some opinion that it can never be attained, with the consequent result of low specification-yield and high prices. It will require some ingenuity to devise a means of defining "functional performance" specifications (propagation delay, voltage swing, etc.) for integrated circuits which can then be segregated into various classes and sold on the open market.

The integrated circuit line of EC&D will ultimately include emitter coupled current steered circuits, (ECCSL), diode transistor logic (DTL) circuits, T²L (transistor, transistor logic), analog circuits, MOS circuits, multiple transistors and diodes, and circuits combining silicon-based active and thin-film passive elements for greater precision in tolerance. All of these circuits have either been developed or are under active investigation.

An important by-product of the precision masking and multiple processing developed in the integrated circuit program is the revolutionary "overlay" power (2N3375) transistor which is actually hundreds of transistors in parallel interconnected by integrated-circuit techniques. This is the leading power transistor in the industry in its power class and is being built into many communication, defense, and space electronic equipments both at RCA and in the industry at large.

Data Processing

Data processing and computer technology are probably the most natural ap-

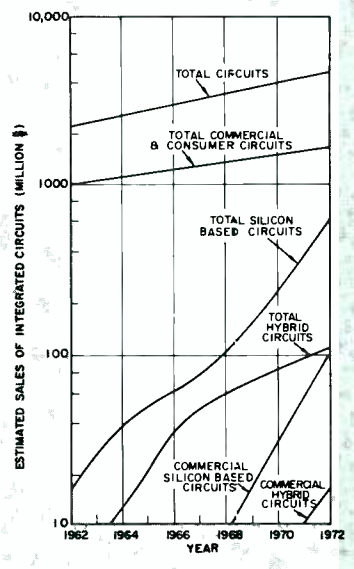

Fig. 1 — One of various industry surveys showing the present and future market for integrated circuits.

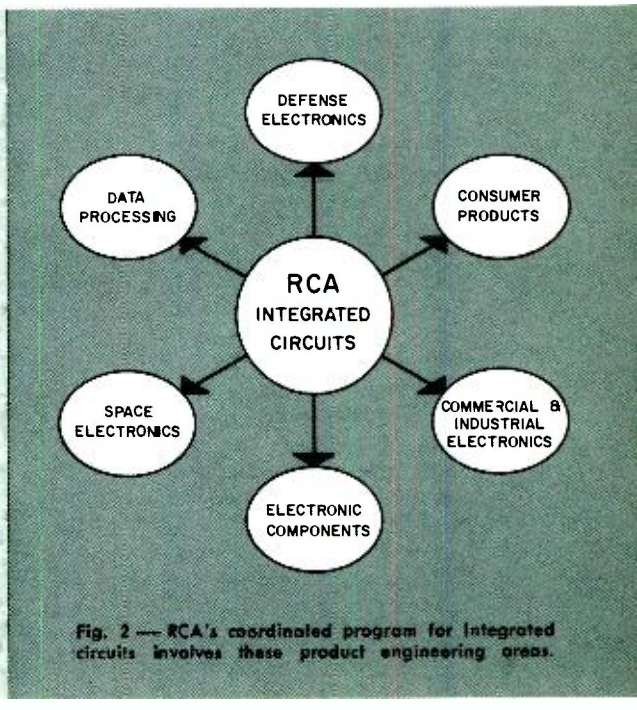

Fig. 2 — RCA's coordinated program for integrated circuits involves these product engineering areas.

plications of silicon based integrated circuitry known. They require large numbers of nearly identical binary *digital* circuits, of relatively low voltage and power. The environment except for a few military computers, is not extreme, and the trend to printed circuit wiring and high packing densities provides maximum advantage to integrated circuits. The research efforts to organize the computer in redundant "logic blocks" rather than individual or dual gates should encourage the integration of larger grouping of circuitry with consequent increase in reliability and, hope fully, a reduction of cost. In addition to the above digital applications, the development of circuitry for balanced sense-amplifiers, memory drivers, and selection matrices can bring the integrated circuit computer closer to realization. Both theoretical and experimental approaches to these objectives are being investigated at the RCA Laboratories and in product divisions.

Because a typical data processor may use 5,000 to 10.000 digital gates, it becomes evident that this application can become a major customer of the RCA integrated circuits. The recent trends to incorporate integrated circuits in our future data-processing product lines pose major challenges to design engineers. The circuit requirements involved extremely low pair-delay and large fan-out working into a rather large capacitative load, with relatively low-power consumption, for a cost per gate *not to exceed* the equivalent discrete component circuit cost. Since almost all of the industry integrated circuits to date had been directed toward military applications, with performance rather than price the major concern, these requirements must be attained with an order of magnitude reduction in price. From a technical viewpoint this has been largely accomplished. Since the fabrication technology is similar to that used in the manufacture of high frequency silicon transistors, the cost projections should be comparable for the two types of devices when large volume production has been attained. Considering the projected sales of RCA computers in the next several years, this volume requirement should readily be met with the resultant attainment of the cost goal.

The important areas of *data communication* and *data switching* in which RCA has a great stake are very similar to data processing in the potential use of digital circuitry. Because these systems can be large and complex (AUTODIN, and RCA Communications, Inc., switching systems) the use of integrated circuitry could materially reduce the size and power consumption of such systems as well as simplify their maintenance.

Space Electronics

RCA's space program can benefit greatly from a wide spectrum of integrated circuits both digital and analog.

Although the past utilization of integrated circuits in the space program has not been extensive, largely through concern about the reliability of early developmental circuits, the maturing of technology and the availability of large samples of integrated circuits to establish mean-time-before-failure data will encourage their use. Applications in counters, synchronous clocks, audio and video and differential amplifiers, computer circuitry and control gates are possible with presently available circuits. New complementary *n-p-n/p-n-p* unipolar transistor gates can provide switching at micropower levels for long journeys in space.

Communication satellites are particularly amenable to the use of integrated circuits because of the need of high packing density, low weight, and extreme reliability for long periods of time. As a matter of fact, all of the circuitry except for the output power stages will be available in integrated circuit form by the time the program is fully implemented.

Silicon-based integrated circuits are considered to be basically no different in a particle radiation environment than silicon planar transistors except that their large isolation junctions may be more prone to leakage. Because of the smaller size, however, it should be possible to provide adequate shielding under severe radiation environment without too great a weight penalty. Thin-film transistor integrated circuitry may be an answer to this environment when development is completed because of their polycrystalline nature and non-dependence on doping levels for their passive elements. Two of the several programs planning to use integrated circuits are the APOLLO camera systems and the TIROS wheel satellite.

Consumer Products

The major limitations to the extensive use of integrated circuits in the consumer market are their high cost compared to presently used discrete components, the majority of which are used in analog circuits. Except for specialized applications as in hearing aids and to some extent in the more expensive personal radios there is little present interest in paying the higher price.

Fig. 3 represents an industry survey of silicon-based network range-of-costs versus several types of circuit card or chassis assembly techniques including consumer discrete circuit costs, as a function of time. The comparison is not exact because the circuits are somewhat differently organized, furthermore, the lower bound of network costs has recently been reduced (dashed lines), below that shown in the solid line of Fig. 3. The reduction in defense spending and the length of the design and manufacturing cycle of electronic equipment has produced a temporary overcapacity in the industry which has considerably affected the price structure. It is apparent that integrated circuit costs have a long way to go to compete with the assembly and component rationalization developed during several decades in the consumer product industry. Even if the slope of the lower bound of network cost were to be doubled, the cost crossover would occur in 1967.

It is interesting to note, however, that a major factor in the cost of the integrated circuit is in the package, the latter having been developed for a military environment. With the attainment of low cost encapsulation, the cost of consumer oriented integrated circuits

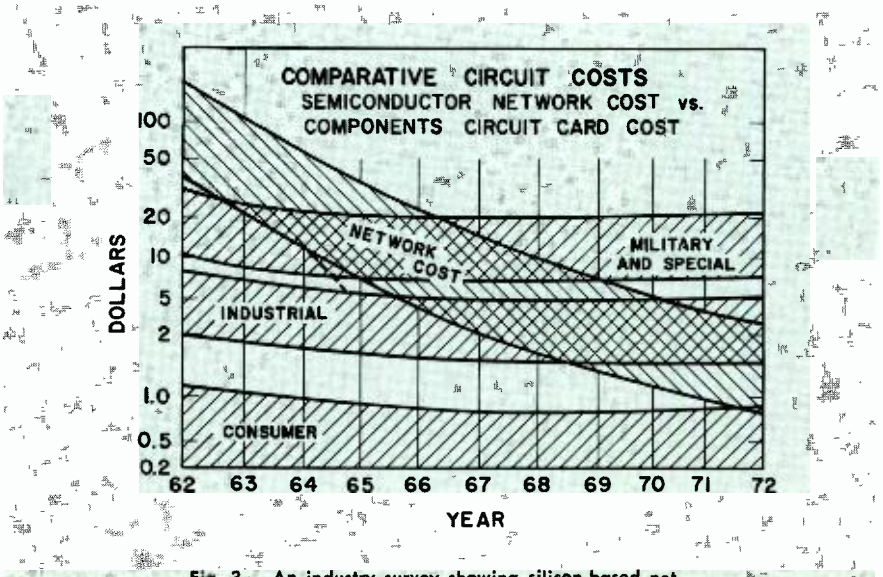

Fig. 3 — An industry survey showing silicon-based network range of costs versus component circuit card costs.

could easily become competitive to *low-power* discrete component assemblies if the number of circuits used were sufficiently high. This large volume requirement is easily met in the radio, television hi-fi product line—hence the importance to our Home Instruments Division of developments which portend cost reductions.

Because of the large number of different circuit functions characteristic of most consumer products, hybridization will probably precede complete circuit integration. Thin film active and passive circuits may provide the means of attaining high-Q tuned circuitry which is impractical to date as part of a silicon based circuit. It could easily happen that digital circuit applications will be captured by the silicon based devices, and consumer product circuits would be a hybrid of thin film (active and passive) circuits on ceramic substrates, some silicon based integrated circuits, and discrete components where it was advantageous to do so. The latter may be power transistors for output stages or television deflection applications. These may in time give way to integrated power amplifiers, since such units have already been built in Somerville but are yet too costly for consumer product use.

Because of the potential importance of integrated circuitry to our consumer business, development in several technologies are being actively pursued. As in digital use, new concepts of circuit organization in amplifiers, detectors, and other circuit functions consistent with the increasing availability of inexpensive multiple active elements of complementary nature are being studied. The consumer products of the future will probably not alter their present appearance, which, as in television receivers, is dictated by the kinescope, but their manufacture will certainly be greatly influenced by the new technology of integrated circuits.

Commercial and Industrial Electronics

These applications largely borrow their technology from the areas described above but have the advantage that cost considerations are not so dominant as in the mass market items. Many of these products have yet to be transistorized or have only recently done so. Additionally, there are often other elements in the system which control the size, weight, and overall cost of the system. Nevertheless integrated circuits will ultimately contribute to improve cost-performance in such equipments as television cameras, mobile and personal radios, the low-power circuitry of transmitters, and multiplex circuitry in communication systems and airborne radar. The emphasis on hermetic encapsulation and circuit reliability of these circuits enhances their use in severe industrial environment, such as the steel and chemical industries, as well as in remote, relatively inaccessible stations of microwave relay systems.

AN INTRODUCTION TO TECHNICAL ASPECTS OF INTEGRATED CIRCUITS

As an introduction to more-detailed papers on integrated circuit devices and technology, the following paragraphs discuss several active elements involved in the RCA integrated circuit program and present simplified representation of a typical integrated device. Also, an understanding of the complex semiconductor processing and the special facilities required to convert a single-crystal silicon wafer into several hundred identical high-performance circuits emphasizes why the integrated-circuit engineering "skill center" is located at the EC&D Somerville plant rather than in the locations involving end use of the circuits.

Fig. 4 shows the three types of transistors useful for integrated circuits presently under development at RCA: the standard planar bipolar transistor, the thin-film transistor (TFT) and the metal-oxide semiconductor transistor (MOS).

Fig. 4a illustrates the standard planar bipolar transistor whose technology is the basis of the present major effort in the RCA program—that of monolithic silicon integrated circuits. It consists of a p-type single-crystal silicon chip into which had been diffused n-type doping in a geometrical pattern by sequential steps of oxidation of the silicon surface to form SiO_2 (an insulator), masking, and etching to expose the desired areas. These exposed areas are then treated with the p or n dopants and heated to cause diffusion of the dopant into the body of the wafer in the concentration desired. The surface is then metalized by evaporation (aluminum) and the desired interconnection pattern developed by etching away the undesired areas. The steps are many and require accurate registration of many masks, and precise timing and temperature cycles. The remarkable record of high performance and large variety of types and high reliability of product at a low cost is convincing proof that this can indeed be done on a production basis. Transistors of this type have been made to amplify at 1,000 Mc, they possess *steep* collector current characteristics so are ideal for switching and digital applications, and have low impedance input and output characteristics useful in wide frequency bandwidth and fast rise time circuitry. They have a major limitation in their poor cross modulation characteristic for radio frequency amplification, an important analog circuit application.

Both the MOS (Fig. 4b) and the TFT (Fig. 4c) were developed at the RCA Laboratories. These are field-effect transistors, as contrasted to the bipolar transistor of Fig. 4a. In the bipolar, a small current in the base-emitter space controls a large current in the collector emitter space; but, in the field-effect transistors, the current between the source and drain is controlled by the potential between the gate and the source by effectively *constricting the cross section* of the path between the source and drain. The field-effect transistor is analogous to a vacuum tube in its operation, wherein the source, gate, and drain correspond to cathode, grid, and plate respectively. Like the vacuum tube it has very high input impedance, moderate transconductance and high output impedance and operates with basically zero gate current. This feature plus its excellent cross modulation characteristics makes for useful analog integrated circuitry. The switching characteristics and gain-bandwidth of field effect transistors are not as good as bipolar tran-

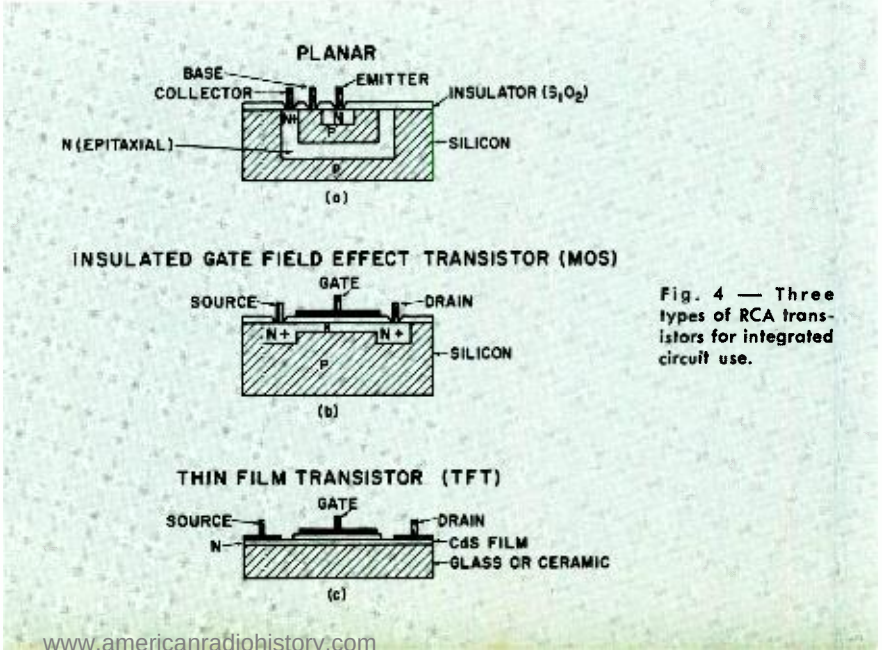

Fig. 4 — Three types of RCA transistors for integrated circuit use.

sistors of equivalent geometric dimensions, but their simpler structure plus ease of mass fabrication provides advantages in many applications including complex integrated circuits. A symmetrical field effect transistor is uniformly *bidirectional* which is advantageous in computer and switching applications where interrogation and response waveforms are carried on a common line.

As far as construction of the devices is concerned, the MOS starts with *p*-type single-crystal silicon on the surface of which a doped oxide is formed. This accomplishes both insulation of the gate and a negative "inversion" layer for a channel. The *n*+ regions are high-conductivity heavily doped regions to provide low resistance between the *n* channel and the metallized source and drain electrodes. A metallized area on the SiO_2 insulation forms the gate which produces constriction of the channel cross section when a negative voltage is applied (reduced current) and expansion of the channel (high current) with reduced negative or a small positive voltage. A complementary version can be made by the use of an *n* substrate and a *p* channel. A combination of a complementary pair in series can perform a digital switching function requiring a few microwatts input. Because the semiconductor effect occurs in a film about 1,000 angstroms from the surface, surface charge effects and similar phenomena which influence the transconductance have kept these devices from large scale commercial applications to date. These problems are now largely under control at Somerville and MOS transistors should become available for both analog and integrated digital circuitry applications in the near future.

The basic differences between the MOS and the TFT is that the TFT uses glass or ceramic substrate (or other smooth insulating material) and a polycrystalline film of a semiconductor such as cadmium sulfide. The behavior in a circuit of a TFT is the same as the MOS, but since it does not require a single crystal semiconductor substrate, it gives promise of being fabricated at the same time as other thin film passive devices in large area depositions. One can envision a complete chassis fabricated by evaporative means including resistors, capacitors, interconnections, thin-film transistors, and diodes. A 30-stage shift register has already been constructed at the RCA Laboratories. Problems of hermetic encapsulation for large area depositions are still to be solved.

In addition to effort on the TFT, thin-film passive elements are under active development both in Somerville and in the DEP-CSD Systems Laboratory in New York City. These include binary alloy film resistors, high-dielectric-constant film capacitors, high-*Q* inductors and interconnections and experimental bipolar film transistors—all of which are important elements in a complete integrated circuit program.

Fig. 5 shows the structure and layout of a portion of a silicon-based integrated circuit, illustrating an *n-p-n* transistor connected to a *p-n* diode, a diffused resistor, and a capacitor.

SUMMARY

RCA has embarked on an extensive effort in digital and analog silicon-based and thin-film circuitry. *The ultimate applications cut across all lines of RCA's corporate interests* with the immediate needs of defense and space electronics and data processing preempting the present production capacity. Device developments and applications for the consumer, commercial, and industrial markets are under active investigation and will become increasingly important as the integrated circuit costs approach those of the equivalent discrete component circuitry.

An integrated-circuit "skill center" has been organized and is located at Somerville with participating engineering from the major RCA product divisions. Spearheading this effort, RCA Electronic Components and Devices has greatly expanded their Integrated Circuit Department, with multimillion-dollar investment in new facilities, backed by a major engineering staff of their own. To insure the success of the program, the finest engineering and production facilities including new, state-of-the-art laminar flow white rooms have been built and will be in full operation by the end of the year.

To evaluate the status of integrated circuit effort it is important to remember that the industry is an explosive one. Technologies which seemed difficult to accomplish and of a long time scale to implement in production, have within a year or less produced a usable yield of products. Price predictions have proved conservative and in large volume use, such as in data processing, price may within one year be less than the equivalent discrete component assembly.

New techniques of circuit isolation already developed promise to remove the major limitation of silicon-based circuits —the parasitic elements inherent in the fabrication process which limit the performance of the devices. The combination of silicon-based circuitry and thin-film passive elements incorporating high resistivity and higher-dielectric-constant lower-loss films, promise to attain truly precise circuits involving large resistances and high capacitance not presently available. New modes of complementary circuit operation portend micropower dissipation so important for space and battery-operated equipment in general.

Many problems still remain to be solved both in the economic and technology categories; the high cost of making circuit changes and the improvement of processes to increase the yields for example. Combined effort at all stages is vitally important between: 1) the research scientist concerned with concepts and material, 2) the engineers developing and fabricating the devices, and 3) the systems and design engineers implementing integrated circuits in actual equipment. *Only through such combined effort can RCA assume a leadership position in integrated circuits.*

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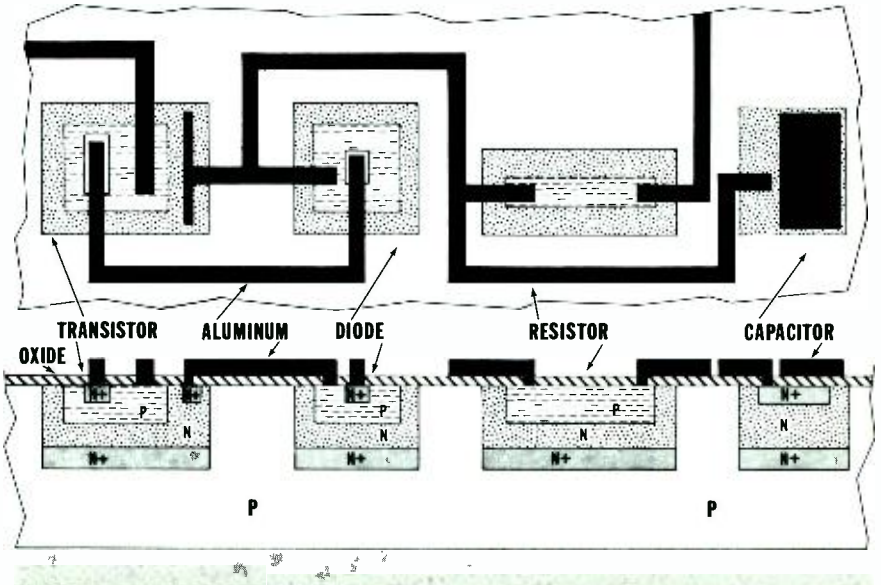
Fig. 5 — A silicon-based integrated circuit.



THE EC&D INTEGRATED CIRCUIT ORGANIZATION AND ITS OBJECTIVES

Probably no other new product development has received greater attention in RCA in 1964 than integrated circuits. Furthermore, few product developments can match integrated circuits in their impact across all the major divisions of the Corporation. Thus, it is particularly important that personnel in all RCA product divisions know where this program stands and what it means to them. This article explains the major steps taken during the past year to develop RCA's capabilities in integrated circuits and describes the organization of the Integrated Circuit Department of RCA Electronic Components and Devices.

L. R. DAY, General Manager

Special Electronic Components Division, EC&D, Harrison, N. J.

THE RCA component activities first became involved in the design of monolithic silicon integrated circuits at the beginning of 1963, with the organization at Somerville of a small technical task force — sponsored jointly by RCA Research and Engineering, the former Semiconductor and Materials Division, and the Chief Engineer's office of the Defense Electronic Products — and headed by R. D. Lohman. Good technical progress was made by this pilot group in their first six months and on July 1, 1963, responsibility for integrated circuits was assigned to the new Special Electronic Components Division.

One of the first questions to be resolved on the heels of the initial technical success was the kind and magnitude of effort to be applied during 1964.

A study of potential requirements indicated that the demands for integrated circuits *within RCA alone* in 1964 would far exceed any production capability that might be established during the year in Somerville. Accordingly, a decision was made to concentrate the development of integrated circuits, at least during this initial phase, on devices that would stand the best chance of satisfying as many of the needs of other RCA activities as possible. It was also recognized that very close coupling would be required between the integrated-circuit design and fabrication engineers and the equipment design engineers. Thus, the first objective of the Integrated Circuit Department for 1964 became the establishment of the closest possible interface with the user divisions of the Corporation.

The second objective of the Integrated Circuit Department in 1964 was to expand considerably upon the technical competence established by the engineering task group in early 1963. This objective has been met in a very full sense under the direction of R. D. Lohman, Manager, Engineering, Integrated Circuit Department. An engineering department consisting of approximately 100 people has been established, and a multimillion dollar investment has been made to provide this group with the finest facilities available in industry.

Key members of Mr. Lohman's activity are I. H. Kalish, Manager, Integrated Circuit Design; B. V. Vonderschmitt, Manager, Integrated Circuit Applications; and F. M. Yates, Project Administrator.

In its very first year of existence, the engineering organization of the Integrated Circuit Department has proven its technical competence in actual design competition with the leaders of the integrated-circuit industry.

The third objective for the Integrated Circuit Department in 1964 was to establish an organization and facility at Somerville for the production of integrated circuits. This objective has been fulfilled and, in August, 1964, a vertical-laminar-flow facility, unique in the industry and designed to provide the ultimate in a super-clean manufacturing environment, was completed and staffed by an initial complement of personnel. R. A. Wissolik is Manager, Integrated Circuits Products Manufacturing, and has reporting to him L. P. Fox, Manager, Production Engineering; H. I. Eberly, Manager, Manufacturing; R. R. Giordano, Manager, Production and Material Control; and P. Greenberg, Manager, Quality and Reliability Assurance.

Responsibility for coordinating the market-development and product-planning functions of the Integrated Circuit Department rests with D. W. Chace, Manager, Integrated Circuit Product Administration. Assisting Mr. Chace in this function are D. R. Deakins, Manager, Market Development; H. F. Scott, Manager, Product Coordination & Control; and V. J. DeFillipo, Administrator, Special Account Sales.

One of the important strengths of the Integrated Circuit Department is the support that this new activity has been given by other EC&D organizations having a wealth of experience in related semiconductor technologies. These related technologies include the materials, process, and device know-how and the photomask-making capability of EC&D's Technical Programs organization, and the packaging skills of the Commercial Receiving Tube and Semiconductor Division. Services provided by these organizations are an important part of the total capability represented at Somerville.

As mentioned at the outset of this article, RCA has already invested several millions of dollars advancing its integrated-circuit effort to its present position, and is well aware of the need for additional investment to push this new technology to the point where it can hopefully become an established profit-producing arm of the Corporation. It should be obvious that investments of this type can be undertaken only when they can be supported by adequate profits generated by other product lines.

The management of the Integrated Circuit Department recognizes its debt to these other product lines and its responsibility to achieve the greatest possible mileage from RCA's investment. Our ultimate goal is to project RCA into a position of profitable leadership in this new field. Progress in 1964 has established a base for such achievement.

An SECD integrated circuit planning session: (l to r) H. Lewis, Administrator, Financial Planning; R. H. Wissolik, Mgr. Manufacturing Integrated Circuit Products; R. D. Lohman, Mgr., Integrated Circuits Engineering; L. R. Day, Gen. Mgr., Special Electronic Components Division; and D. W. Chace, Mgr. Administration. *For a biography of the author, see his article on "Direct Energy Conversion . . . A Management Viewpoint," RCA ENGINEER, Vol. 9—No. 3, Oct.-Nov. 1963.*

Final manuscript received August 10, 1964

INTEGRATED CIRCUIT CAPABILITY AT SOMERVILLE—GOALS AND PROGRESS

Within the past year, a major corporate effort has been expended to develop a capability for the design and fabrication of monolithic silicon integrated circuits at the Somerville location of the Electronic Components and Devices organization. This paper reviews the goals of this effort and indicates the progress made to date.

I. H. KALISH, Mgr.
Integrated Circuit Design
Special Electronic Components Division
Electronic Components and Devices
Somerville, N. J.

In monolithic silicon integrated circuits, *capability* means the ability to deliver to equipment manufacturers semiconductor network arrays that function properly in the customer's circuits, are packaged in an enclosure satisfactory to the customer, and are priced competitively. Such capability must be based on competence in three areas—materials, components, and packages. The materials needed for such integrated circuits are epitaxial silicon wafers. The components required include resistors, transistors, diodes, and capacitors. The package configurations vary from axial (TO-5) configurations to 14-lead flat packages.

The processing of integrated circuits can be divided into three general areas: 1) obtaining isolation between components, 2) fabricating the components, and 3) interconnections and packaging.

ISOLATION

In multichip microcircuits, electrical isolation is accomplished by physical separation of individual discrete components. But when circuits are made in monolithic form, alternative means must be used. Fig. 1 illustrates the junction method of achieving electrical isolation. The transistors shown are electrically blocked from each other by two back-to-back diodes. Present technology can achieve DC isolation in excess of 10 megohms with this method. Such values are more than adequate for applications at frequencies up to a few hundred kilocycles. At higher frequencies, however, the junction capacitances associated with the diodes begin to degrade circuit performance in most applications.

An alternative approach toward achieving isolation is illustrated in Fig. 2. This technique (now under development) isolates individual silicon chips in a glass matrix. The advantages of wafer processing are thus maintained without corresponding penalties in terms of high-frequency isolation.

FABRICATION

The quality of circuit that can be integrated depends directly on the quality of the components that can be fabricated.

The initial goal at Somerville was to develop a process that could generate usable diodes, transistors, resistors, and capacitors simultaneously. Table I summarizes the characteristics of components generated by the first Somerville processing. These components were designed for use in low-voltage, high-current digital applications. Their availability made possible the fabrication of digital gates having pair delays of 15 nsec under worst-case conditions.

The capacitance capabilities of this initial process can best be described in terms of a capacitance-per-unit-area coefficient. This value was approximately 0.3 pf/square mil. Thus, although capacitors having values of several hundred picofarads could be generated, the area required would be comparable to the rest of the circuit. Fig. 3 shows the disproportionate area required by the capacitor in a circuit having a single 50-pf capacitor and other components.

With the capability described in Table I as a base, development work during the past year has concentrated on improving

Fig. 1 — Structure and equivalent circuit of transistor pair isolated by diodes.

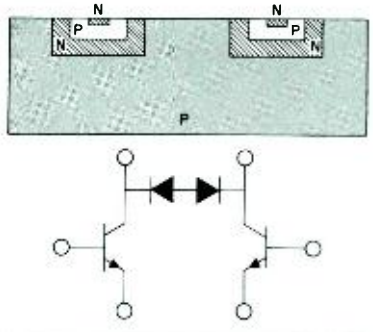


Fig. 2 — Isolated transistor pair made by use of glassing techniques.

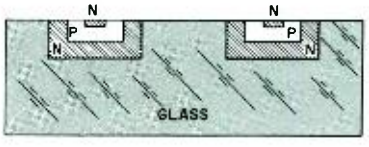
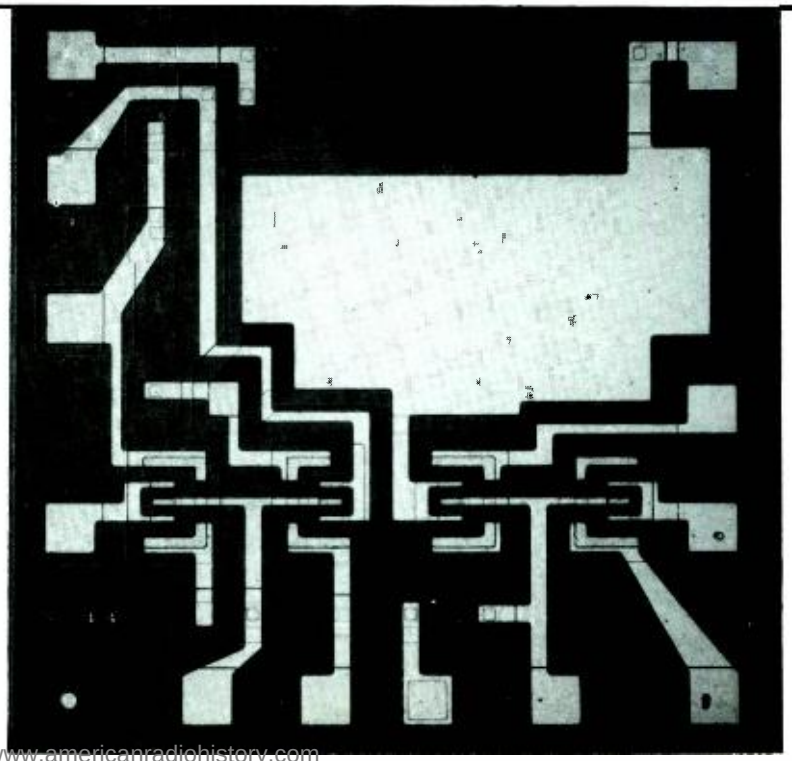


Fig. 3 — Integrated circuit including a 50-pf capacitor.



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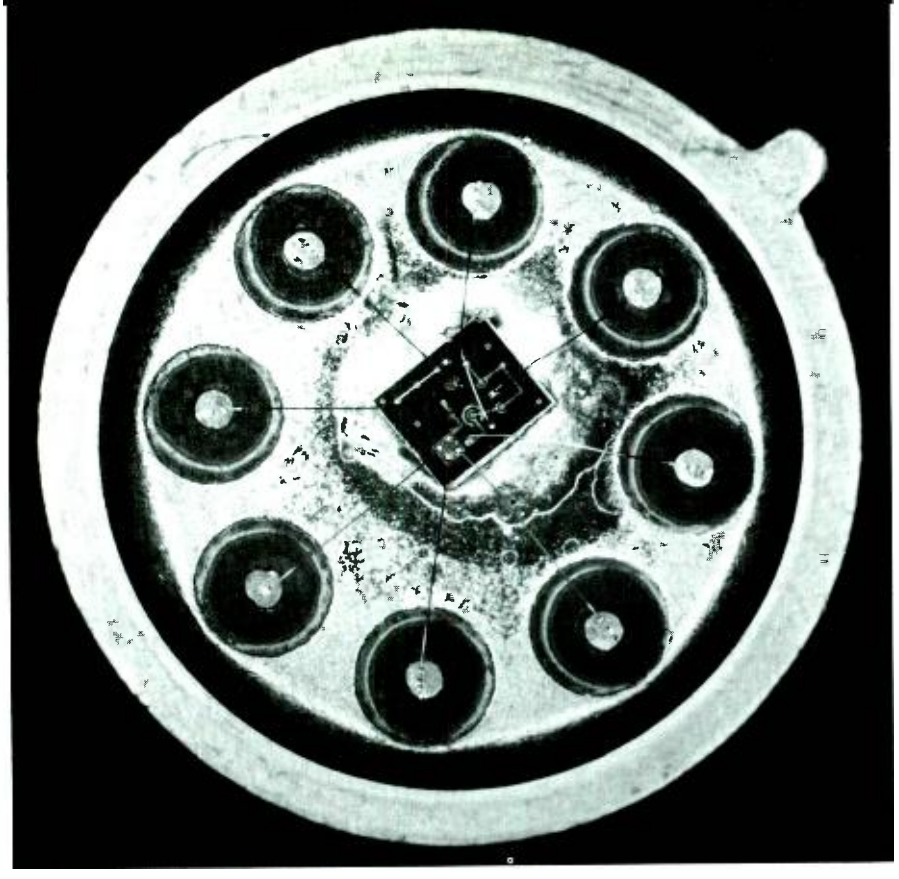

Fig. 4 — Integrated circuit on 8-lead TO-5 stem.

ISRAEL KALISH received the BSEE from the Cooper Union School of Engineering in 1953 and the M.S. degree in Electrical Engineering from Columbia University in 1956. He joined RCA in 1953 as a semiconductor-device engineer. He was promoted to Manager of Germanium Product Design in 1961, and assumed his present position as Manager of Integrated-Circuit Design in January 1963. Since 1954, Mr. Kalish has been an Adjunct Instructor in Physics and Electrical Engineering at the Cooper Union School of Engineering.

all items of electrical performance. Breakdown voltages have been improved by use of advanced epitaxial techniques that permit higher resistivities without compromising saturation voltages. Capacitances have been reduced and high-frequency performance enhanced by improved photolithographic techniques. The quality of resistors has been upgraded by the use of compatible thin-film techniques. Where applications justify the extra processing required, the thin-film approach can provide temperature coefficients below 100 parts per million. In addition, the development and refinement of gold-doping techniques have reduced transistor storage times below 5 nsec and thus have made the fabrication of high-speed saturating circuits possible.

A major increase in the integrated-circuit capability has been the development of processing to permit simultaneous fabrication of p-n-p and n-p-n transistors. Because transistors are relatively inexpensive components in integrated circuits (i.e., they use little area per device), such complementary circuits can be used to give equipment designers the additional flexibility of using transistors for direct coupling, as active loads, and as current sources in applications that would not be economically feasible in discrete form.

PACKAGING

The requirements for an integrated-circuit package are that it be hermetically sealed, reliable, and inexpensive. The first package that was used for RCA monolithic silicon integrated circuits is shown in Fig. 4. Except for the number of leads, this package is similar to the TO-5 package used for encapsulating transistors. Although this design was easy to fabricate, equipment considerations caused the industry to demand a coplanar package. Experience and familiarity with "solid-ceramic" techniques permitted the design and fabrication of the ten- and fourteen-lead solid-ceramic packages shown in Fig. 5. The availability of this type of package has permitted the use of a reliable sealing process, welding, to deliver reliable circuits in convenient form factors.

SUMMARY

The development of a successful integrated circuit depends upon strong support in the areas of materials, processing, and packaging. The location of the integrated-circuit activity within the semiconductor arm of Electronic Components and Devices has permitted the use of its established transistor capability as the foundation for RCA's integrated-circuit efforts and as a continuing reinforcement of the new integrated-circuit capability.

TABLE I—Characteristics of Components Generated by First Processing

Diodes:
Forward Drop, 0.8 volts at 10 ma
Capacitance, 2 pf at 0 volts
Series Resistance, 5 ohms
Breakdown Voltage, 25 volts
Transistors (n-p-n):
Current Gain, 40 at 10 ma
Saturation Voltage, 0.4 volts at 10 ma
Gain-Bandwidth Product, 400 Mc
Collector-Emitter Breakdown, 12 volts
Emitter-Base Breakdown, 6 volts
Storage Time, 30 nsec
Resistors:
Range, 100-10,000 ohms
Temperature Coefficient, 2,500 ppm
Isolation, 15 volts
Tolerances: absolute, ±20%; *ratios*, ±3%

Fig. 5 — Welded 0.25" x 0.25" integrated-circuit packages.

THE DEP MICROELECTRONICS ACTIVITY ...Applying Integrated Circuits to Military and Space Equipment

Described herein is the rapid growth and use of integrated circuits in defense electronics; and the formation at RCA of a DEP Microelectronics Group to concentrate on the application of integrated circuits in new and sophisticated military and space systems. Industry trends, manufacturing costs and system economies are discussed.

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Defense Microelectronics
DEP, Somerville, N. J.

To engineers concerned with military and space equipment, the term *microelectronics* has meant any device-and-circuit technology that allows whole electronic functions to be performed by a very small module or device package. Until recently, implementation of microelectronic circuitry in actual equipment was generally restricted to modules constructed from miniature, but *discrete* circuit components. Familiar types have included approaches such as cordwood, minimodules, micromodules, etc.; a common characteristic of these was that each active and passive element making up the circuit function was a very small but still discrete and separable device.

But now, equipment designers can capitalize on the advantages of truly *integrated* circuits—i.e., monolithic circuit packages wherein active and passive elements are inseparable from each other. Currently leading this new technology in practical application are the monolithic silicon integrated circuits. Their rapid penetration into microelectronic technology is due to the similarity of their fabrication techniques to those of silicon planar transistors. As a result, the transition from standard transistorized circuits to monolithic silicon integrated circuits is occurring at a much faster rate than did the transition from tubes to transistors. It should be emphasized that *significantly different application design rules for monolithic silicon integrated circuits require the development of new circuit design techniques to make optimum use of integrated circuits.*

The continuing development of other approaches to integrated circuits—such as those based on thin-film active (TFT) and passive techniques, and the insulated gate metal-oxide semiconductor devices (the MOS) is following rapidly the current practical possibilities of the monolithic-silicon integrated circuits.

In *all* these approaches, RCA has made and continues to make significant contributions to microelectronic technology. The RCA Laboratories at Princeton pioneered in research on the TFT and the MOS. Within DEP, the Applied Research activity established integrated-circuit device research and development programs in both monolithic silicon and thin-film configurations several years ago. In addition, the DEP Communications System Division's Laboratory in New York has been conducting research on thin-film passive components for several years. During this same period, RCA developed an outstanding capability in epitaxial growth and silicon-planar-transistor techniques which are keys to the successful, practical production of monolithic silicon integrated circuits. In short, RCA has both the technological and facility resources necessary for a leading position in integrated circuitry.

THE RAPID GROWTH AND USE OF INTEGRATED CIRCUITS

Fig. 1 shows the rapid technological growth of integrated circuits. At the beginning of 1963, there were approximately 30 types of integrated circuits available as off-the-shelf devices from the entire industry; at the close of 1963, some 130 different types of circuits could be purchased. Significantly, the bulk of production circuits were limited to use in low-speed digital applications. During 1964 a similar number of analog and high-speed digital circuits have become available.

Fig. 2 gives an indication of utilization, showing the actual shipments of integrated circuits reported for 1963. Of the total 515,000 circuits delivered, approximately 50% were purchased in the last quarter of 1963. Of equal interest to both users and producers of integrated circuits is a projection of sales based upon anticipated microelectronic equipment programs; Fig. 3 shows an extrapolation of sales of integrated circuits for the next 10 years, based upon overall industry surveys. The usefullness of such a curve depends upon the completeness of the survey data and intelligent factoring; Fig. 3 is considered to be a *conservative estimate* based on present accelerated plans to use integrated circuits in a large number of military and space electronic systems. (It

Final manuscript received July 15, 1964.

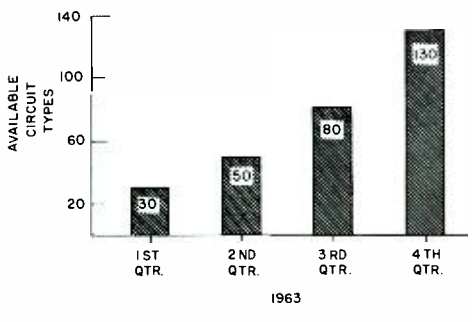


Fig. 1—Number of different types of microcircuits available in 1963.

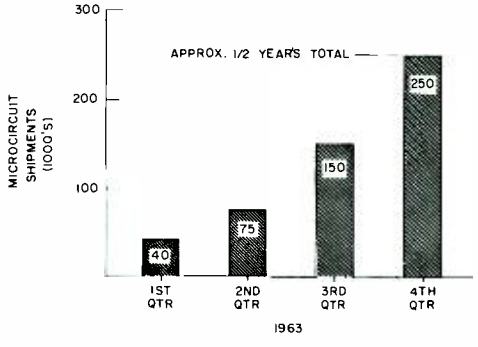


Fig. 2—Over one-half million microcircuits were shipped during 1963 by the electronics industry (EIA data).

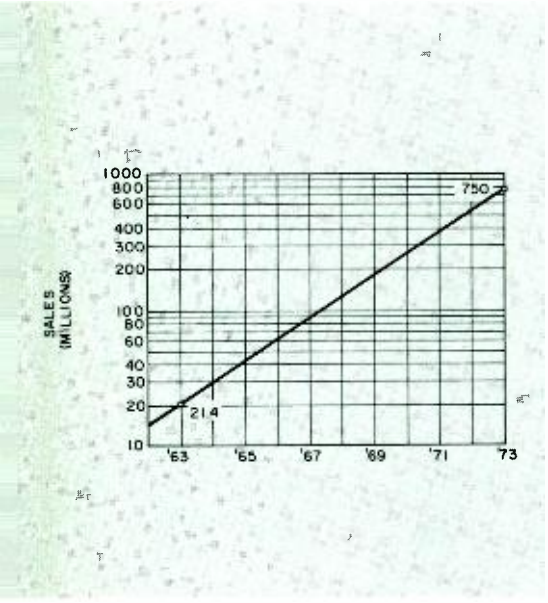


Fig. 3 — Projected microcircuit sales for the years of 1963 through 1973; data from P. E. Haggerty, "The Economic Impact of Integrated Circuitry," IEEE *Spectrum*, June 1964.

RAMON H. AIRES recieved the BEE degree from Cornell University in 1950. He received the MSEE from the University of Pennsylvania in 1959. He joined RCA in 1954, following employment in the Advanced Development Television Laboratory of the Philco Corporation where he was responsible for the development of precision feedback deflection and high-voltage circuits for use in color television display systems. Shortly after joining RCA, he was promoted to Leader and then Manager of a group working on servomechanisms for stabilization and control of Antennas for Airborne Fire Control Radar Systems. In 1958 he became Manager of the electrical design group that built the first TIROS Weather Satellite. From 1959 to 1963 he served on the staff of Chief Defense Engineer and was responsible for administration and control of company sponsored Independent Research and Development Programs. In 1963 he became Manager of Defense Microelectronics. Mr. Aires holds several patents in circuitry and feedback control techniques. He is a member of the IEEE and Eta Kappa Nu.

also appears that the use of integrated circuits in non-military electronics is getting under way much sooner than expected.

THE DEFENSE MICROELECTRONICS ACTIVITY

As indicated previously, RCA's activities in microelectronics began many years ago; early in 1963, it was recognized that radically new circuit design techniques would be required to implement integrated circuits; thus, a central group of microelectronic specialists was formed to provide guidance to the numerous design and systems application groups within DEP. In 1963, an experimental program was conducted by a small group from Applied Research who worked closely with the EC&D integrated circuit group at Somerville, N. J., to develop the first monolithic silicon integrated circuit specifically designed for use in DEP.

Based upon the noteworthy success of this approach, the decision was made to formally establish a group within DEP that would work closely with the integrated circuit design and fabrication group of the EC&D Special Electronic Component Division (SECD) and spearhead subsequent integrated circuit developments for DEP. Accordingly, in October of 1963, the Defense Microelectronics (DME) activity (Fig. 4) was established reporting directly to Dr. H. J. Watters, Chief Defense Engineer.

In the short time since its inception, DME and SECD have successfully developed a family of monolithic high-speed digital logic functions and a series of analog amplifiers covering frequency ranges from DC to 100 Mc.

In addition to its integrated circuit research and development responsibilities, DME provides engineering services to a wide range of RCA activities concerned with the establishment of advanced integrated design capabilities. DME also provides technical support in the preparation of proposals requiring integrated circuit devices, conducts formal training programs, provides facilities for representatives of the DEP Divisions to work at the DME facility, and performs specific tasks as a subcontractor for groups who have equipment and study contracts throughout DEP.

A continuous program of evaluation is being conducted by DME on competitive integrated circuits; the results are made available to cognizant activities. To assure rapid dissemination of significant data, a *Microelectronic Bulletin* is sent at frequent intervals to interested managers, leaders, and engineers within RCA; such data serves both as a source of current technology and as a training document.

THE NEW INTEGRATED CIRCUIT DESIGN TECHNIQUES

To achieve an optimized integrated circuit function requires design techniques drastically different from those utilized in the past; in particular, the fabrication of passive components, (resistors and capacitors), is more difficult than the preparation of transistors and diodes. As a result, transistors replace resistors and capacitors wherever possible. Primarily, the technical basis for this departure from standard techniques hinges upon the importance of surface area considerations in monolithic silicon integrated circuit fabrication and circuit yield; circuit yield is inversely proportional to the area of silicon required. The area required for a single 100-kilolm diffused resistor or a 150-pf capacitor is approximately the same as that required for ten transistors.

In addition, component tolerances assume a new and critical role in the design of monolithic silicon integrated circuits. Although silicon diffused resistors normally have a tolerance of about 20% for absolute values, resistor ratios can be maintained to within about 4%. Therefore, circuits are designed so that

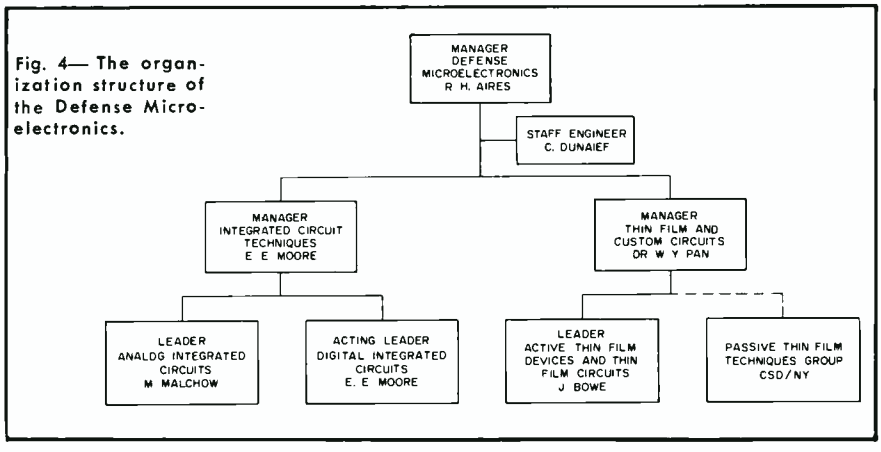


Fig. 4— The organization structure of the Defense Microelectronics.

critical parameters depend on resistor ratios rather than absolute resistor values. Monolithic silicon integrated circuit performance can be appreciably enhanced by basing the design on matched transistor characteristics. Since all components are produced simultaneously with the same diffusion processes. and are so close together, the tracking of the characteristics can readily be achieved with existing techniques.

Thus, the apparent advantages of diffused monolithic circuits can be fully realized only when unique characteristics of diffused components are known and used correctly. A basic problem encountered in design is the coupling or parasitic effect between the diffused components and/or the silicon substrate. Such coupling action may result either from a back-biased diode or a parasitic transistor. To achieve more effective isolation of the diffused components, appreciable effort is being exerted to reduce undesirable coupling effects. Another primary problem is the implementation of required inductance in monolithic form; no satisfactory replacement for an inductor has been found. In spite of such limitations, monolithic silicon integrated circuits frequently perform better than their discrete-component equivalents in many applications.

ANALOG CIRCUIT DESIGN

Because the implementation of analog functions is critical to the success of communication and radar systems, DME places great emphasis on integrated analog-circuit design; in fact, the choice of emitter-coupled current-steering logic (ECCSL) for the first RCA monolithic silicon integrated circuits was based partially on its applicability to analog circuits as well as a large number of high-speed digital functions. DME has developed a basic integrated differential amplifier which can be utilized with minor modifications in internal connections for a number of analog circuit functions. As a result, fabrication of a variety of circuits can be realistically and economically accomplished, even in small quantities.

Analysis of typical circuit functions of DEP systems indicates that between 15 and 35% of the integrable circuit functions are analog circuits. Fig. 5 indicates distribution, by frequency, of analog requirements for a typical large weapon control system; it can be seen that approximately 75% of the circuits are in the frequency spectrum below 10 Mc. Most of these circuits can be constructed in monolithic silicon form with present techniques.

Higher frequency circuits and circuits requiring tighter component tolerances than those accomplished with diffusion processes, use hybrid combinations. One form of hybrid circuit consists of thin-film passive components evaporated on silicon substrates into which the active elements have been diffused. This technique has three primary advantages. Thin-film resistors and capacitors can be designed to use less area than their diffused counterparts; improved isolation characteristics can be achieved which alleviate the coupling effects experienced with monolithic circuits, and better tolerances can be obtained.

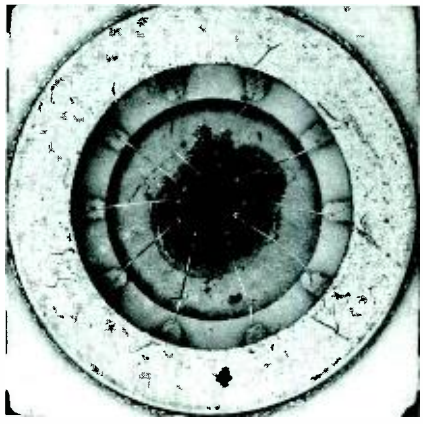
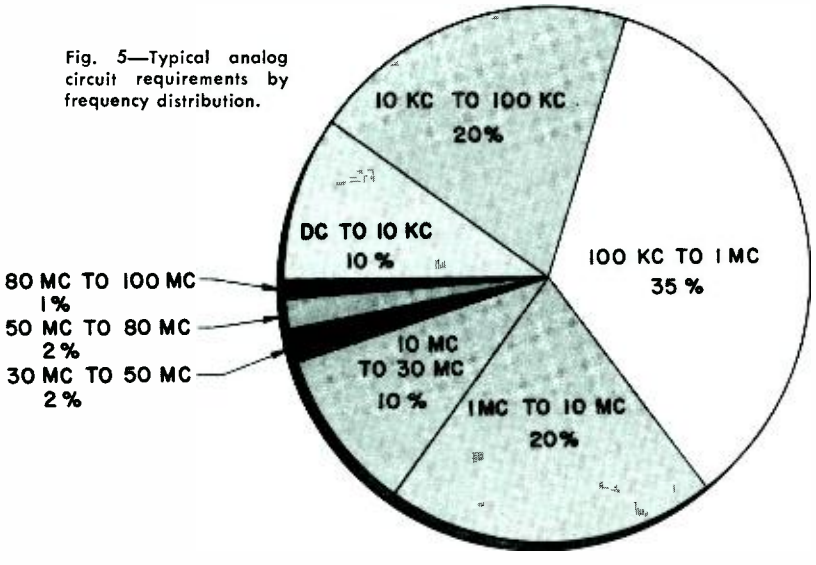


Fig. 6—Dramatized here is the fact that the tiny square silicon chip (center) containing all the circuitry requires only a small fraction of the total area or volume needed for making practical connections to outside circuits.

Fig. 7—The flat package has advantages in packaging aver the conventional transistor case.

Fig. 5—Typical analog circuit requirements by frequency distribution.



THIN-FILM INTEGRATED CIRCUITS

While major applications emphasis has been on the monolithic silicon approach to integrated circuits, there are certain limitations to this technology, which are alleviated through use of thin-film techniques; some of these characteristics have been briefly outlined above.

Future applications of thin film techniques will most probably be based on the improved isolation characteristics, simplified interconnections, and closer component tolerances. Thin film component performance is generally very close to that of equivalent discrete components. As a result, circuit designers with a minimum amount of experience with integrated circuits will find it easier to apply thin-film circuits than mono-

lithic silicon circuits. A major obstacle to be overcome, prior to the widespread utilization of thin-film circuitry, is the fabrication of active thin-film devices. Most thin-film circuits now commercially available are hybrids—they utilize either chips containing diffused active devices bonded to the insulating substrate or thin-film passive components evaporated on a silicon substrate containing diffused active components.

DME has been working in conjunction with RCA Laboratories on several military contracts involving research on thin-film active devices (the TFT). Appreciable progress has been made but a number of critical performance characteristics must be further improved before wide application of *all-thin-film* circuits will be possible.

MICROELECTRONIC PACKAGING TECHNIQUES

Although the design and fabrication of integrated circuits is already quite sophisticated, significant improvements can still be made in the packaging of integrated circuits. Fig. 6 shows that greater packaging efficiency can still be obtained; only a small percentage of the area available within the package is required for the silicon chip containing the circuit. The major physical limitation in the design of the package is the requirement to supply sufficient external connections for the circuit. The obvious answer, demanding serious consideration, is to maximize intra-connections *within the package* so that external lead requirements are minimized. When connection requirements are satisfied, several times the electronic functional capability can be packaged within the volume currently used for one function.

As a result of severe reliability requirements and the lack of high-volume production of flat packages during 1963, proven containers such as the TO-5 transistor case were used in early designs. Although the TO-5 type case has a proven record of reliability, effective hermeticity, shielding characteristics, and low cost, the flat package has many advantages from a packaging standpoint (Fig. 7). Much effort is being expended in the development of a highly reliable yet low cost flat package for monolithic silicon integrated circuits. Numerous design approaches are being considered by RCA in the development of flat packages for integrated circuits. It will undoubtedly always be possible to purchase a variety of flat-pack designs, but economic factors will direct most users toward a standard configuration.

INTEGRATED CIRCUIT PRICING

As the quantity of integrated circuits increases, cost decreases in almost direct proportion. Progress has been so rapid that it appears conservative to predict that, for many applications, the cost of integrated circuits in 1965 will be the same or less than that of equivalent military standard components; as recently as 1963, such a cost prediction could not be made confidently.

Fig. 8 indicates an average circuit-function price representative of many circuit types and manufacturers; significance of such data to an individual user would depend upon the nature of his requirement. For example, in digital applications requiring the highly repetitive use of a small number of digital functional devices, the average price would be lower than that of the projected curve. Further, with appropriate logic design using multiple circuit functions on a single chip or within a single package, the price per function would be further decreased.

SUMMARY

Industry's capacity to produce integrated circuits during the first quarter of 1964 was estimated to be in excess of 250,000 deliverable devices per month. Considering that only a few equipments containing integrated circuits have reached the production phase, and that most users are purchasing circuits for developmental purposes, it can be seen that an over-capacity situation has developed throughout the industry. One of the results of this condition is the appreciable price cutting that started early this year. The net effect has been the enticement of new integrated circuit users through the primary incentive of low cost. As these new developments mature, the number of circuits required will increase, resulting in still further cost savings. The well established regenerative cycle will rapidly lead toward integrated-circuit prices that are lower than those of discrete-component circuits providing the same functions.

Thus, we are rapidly coming to the time when we will no longer ask "can we afford integrated circuits"? In a competitive bid for new programs, *it will be necessary to use integrated circuits to become the successful bidder.*

Finally, in winning defense and space contract awards, a unique capability for developing integrated circuits and applying them into equipment in a practical and economic manner is vital to DEP. In almost all advance systems, the implementation of special integrated circuits is a critical factor in proposal evaluation. In conjunction with all divisions of DEP and in cooperation with SECD, the goal of the Defense Microelectronics activity is to help develop the technological skills and special integrated circuits required for a leading position in new microelectronic equipment programs.

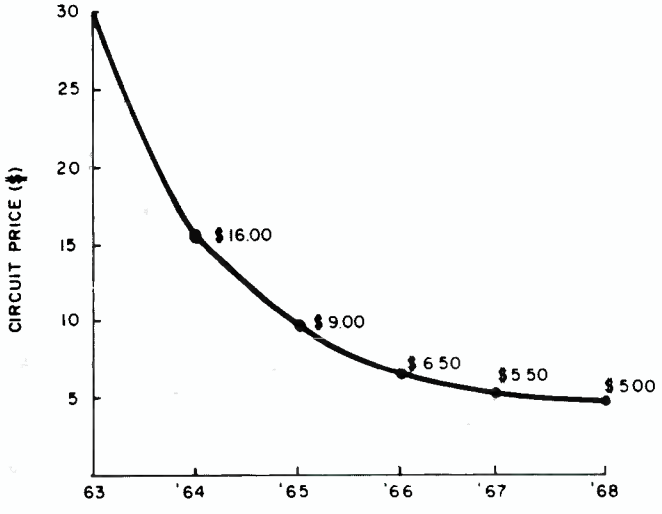
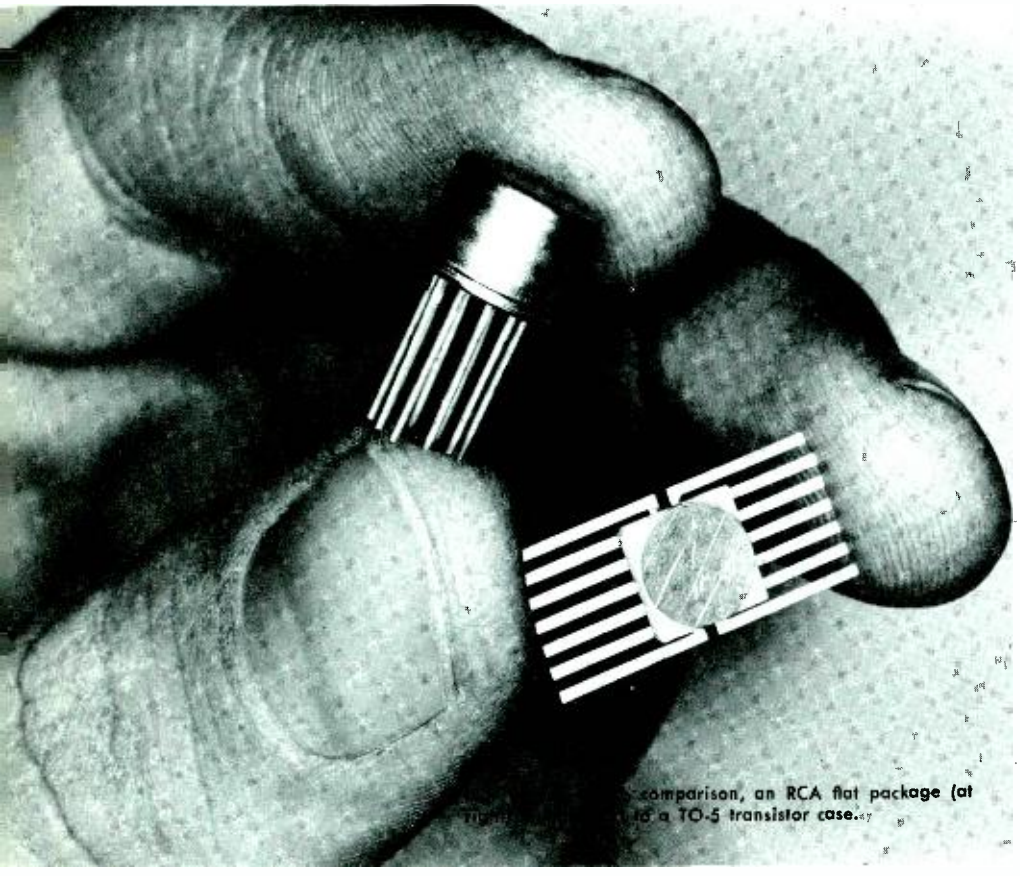


Fig. 8—An extrapolation of average integrated circuit prices vs. time.



comparison, an RCA flat package (at ... to a TO-5 transistor case.

E. E. MOORE received his B.S. in E.E. from Purdue University in 1952 and his M.S. in Systems Engineering and Operations Research from the University of Penna. in 1958. His 12 years of experience at RCA in electronic circuits and systems development includes: circuit and logic design for the BIZMAC tape sorter, part of RCA's first digital data processing and computing system; development of an airborne closed loop transistorized television system; study of information requirements of the Pilot under Pilot Vision Program for the B-52 bomber; study of digital communications system employing various information rates, and study of means of improving radar systems by the use of analog recording of the video signals on magnetic drums. In 1960, Mr. Moore was promoted to Mgr., Signal Processing Group, Applied Research, where he was responsible for advanced communication systems, application of neural logic to pattern recognition, and development and application of integrated circuits. In 1963, Mr. Moore was made Mgr. of Integrated Circuit Techniques in the newly formed Defense Microelectronics activity in Somerville. Mr. Moore is a member of the IEEE, Tau Beta Pi and Eta Kappa Nu.

EMITTER-COUPLED MONOLITHIC SILICON INTEGRATED CIRCUITS FOR HIGH-SPEED COMPUTERS—A STATUS REPORT

Emitter-coupled monolithic circuits are described specifically and some of the related fabrication areas associated with monolithic circuits are considered. In addition, experimental data on emitter-coupled logic circuits are presented to point up the relative effects of monolithic parasitic elements and of system wiring capacitance on the circuit speed attainable.

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Integrated Circuit Techniques
Defense Microelectronics
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DURING 1962 and 1963, many semiconductor manufacturers introduced digital integrated circuitry for use in medium- and low-speed computers. Schematically, these circuits essentially duplicate the discrete circuits familiar to the computer field—one such popular circuit used by RCA is the DTL (diode transistor logic). The penetration of circuits such as the DTL into military developmental systems has proceeded rapidly. As a result, prices have tumbled until today equipment manufacturers can purchase large quantities of integrated circuits at or below the cost of similar discrete circuits that use conventional components. Fortunately for equipment manufacturers, the integrated-circuit makers are already cooperating in creating industry standards for producing interchangeable circuits; such arrangements will lead to even greater cost reductions and penetrations into military and commercial systems in the years to come.

All manufacturers of integrated DTL circuits have encountered some technical difficulties in achieving circuit performance comparable to that provided by discrete components. Such obstacles are due primarily to the fact that monolithic circuit components have parasitic elements associated with them, and hence circuit speed is reduced; component tolerances are also generally poorer, thus degrading performance.

LIMITATIONS IMPOSED BY MONOLITHIC INTEGRATED CIRCUIT DESIGN

In this paper, a *monolithic* circuit will be considered as one fabricated entirely out of silicon, with all transistors, diodes, resistors, and capacitors diffused in the same wafer of single crystal silicon. To

Final manuscript received July 21, 1964

design and fabricate such a circuit, requires that certain factors concerning the circuit components be carefully considered; when such factors are accounted for, the "final" or production circuit will perform better and have a greater fabrication yield. Some of those considerations are described herein.

Area Versus Yield

Generally, circuit yields are inversely proportional to the area of silicon used for each circuit; this relationship is based on the assumption that very few silicon wafers are completely free of imperfections or physical defects. Hence, the smaller the size of the silicon die required by a given circuit, the greater the probability that the die will be free of defects; thus, the possible total number of circuits per wafer will be also greater.

The absolute tolerance on resistors is a function of the area used to fabricate the resistor. For example, since a 2-mil-wide resistor is less sensitive to dimensional inaccuracies than a 0.5-mil-wide resistor, the former can be made more accurately. Of course, since the areas vary as the squares of the width, more area is occupied by the 2.0-mil-wide resistor for a given amount of resistance, and yield will be poorer. Herein lies a design tradeoff peculiar to monolithic circuits. The area required by one 10,000-ohm, 20%-tolerance resistor is roughly equal to *that of two transistors*; hence, circuit designers should favor the use of transistors and employ only a few low-resistance resistors to keep surface areas required for a circuit to a minimum.

Resistor ratios can be held accurately (±3%) when the resistors are roughly the same resistance, the same geometry, and have the same diffusion profile; otherwise, their ratios are not likely to agree much better than their variations from absolute values (i.e., ±10 to 20%).

The area required by a nondiffused 15-pf coupling capacitor is roughly equal to that required by two transistors. Obviously, the use of larger capacitors will seriously decrease the yield of a given circuit per unit of area.

Stray Capacitance and Frequency Response

The capacitance to ground of a diffused coupling capacitor is roughly one quarter that of the coupling capacitor. Hence, frequency response will be seriously hampered by the use of large coupling capacitors. Capacitance to ground of a diffused resistor is distributed in nature and proportional to the active surface area and to the operating voltages; thus, low-value resistors are desirable when high circuit speed is desired.

A transistor in a monolithic silicon chip is isolated from neighboring devices by back-biased diodes, and the collector contact is available only from the top of the wafer. This results in a shunt capacitance to the substrate and in additional series collector resistance. The chief effect of these factors is a degradation in frequency response.

Resistors using base diffusions will exhibit temperature coefficients from 1,500 to 2,000 ppm/°C, whereas resistors using emitter diffusion will exhibit 100 to 300 ppm/°C coefficients. This represents a wide latitude set primarily by the desired transistor parameters sought.

Transistor parameters within a given circuit have a high probability of a closer match than do comparable nonselected discrete units; 90% of adjacent transistor pairs will have V_{be} match closer than 5 mv out of 700 and current gains within 30% of each other. All such factors should be carefully examined during the development, design, and breadboard phases.

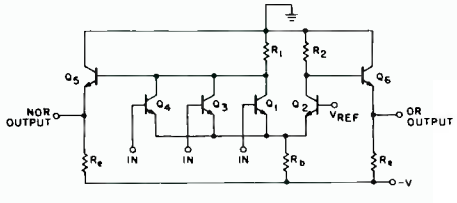


Fig. 2—Diagram of basic emitter-coupled logic gate.

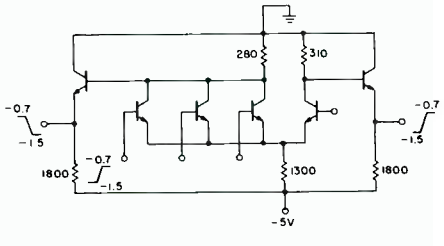


Fig. 3—Same circuit as Fig. 2 with typical circuit values assigned.

Fig. 4—Photomicrograph of a TA-5005 developmental emitter-coupled monolithic logic gate.

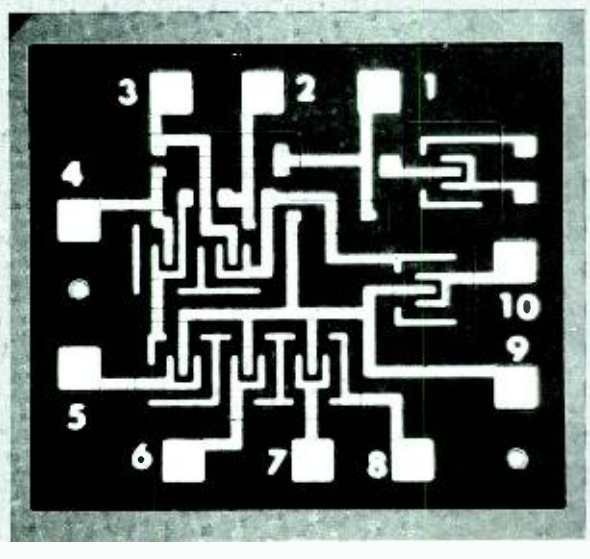
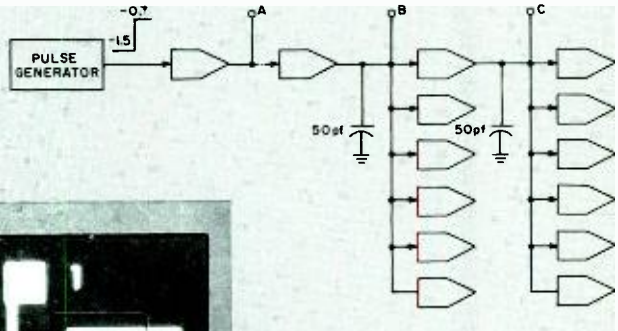


Fig. 5—Test setup for making pair delay measurements.



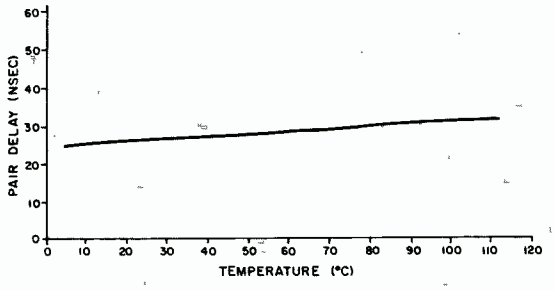


Fig. 6—Curve showing pair delay versus temperature for the TA-5005.

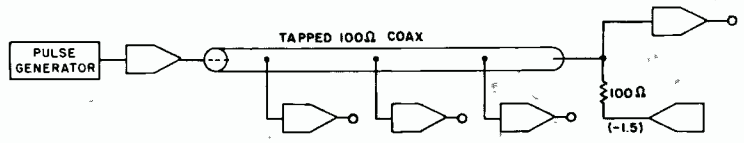


Fig. 7—An additional configuration tested in which a temperature regulating bias is used.

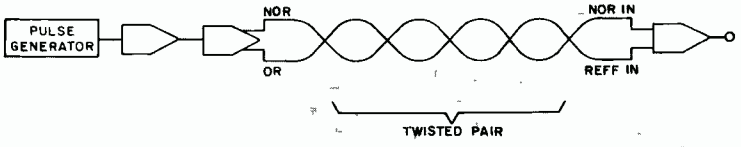


Fig. 8—Sketch of a differential drive scheme.

MONOLITHIC DESIGN APPLIED TO EMITTER-COUPLED CIRCUITS

Fig. 2 shows the basic emitter-coupled logic gate; the heart of this circuit is the differential amplifier using transistors Q_1 and Q_2 and resistors R_{C1}, R_{C2}, and R_b. A fixed reference voltage is connected to the base of Q_2, and signal levels applied to the input of Q_1 (or Q_3 or Q_4) are adjusted to swing symmetrically above and below the reference by 0.4 volts. By so doing, the current flowing in R_b switches between Q_1 and Q_2. Complementary outputs appearing across R_{C1} and R_{C2} are provided through emitter followers Q_5 and Q_6.

The same circuit can be designed using various resistor values depending upon the desired signal level, the circuit speed, and allowable power dissipation; a typical set of values is given in Fig. 3. These values provide a high speed gate of 40-mw power dissipation with a 0.8-volt swing. Output levels are adjusted to permit cascading of logic stages without any additional level setting. When the gate is operated over a wide temperature range, the reference voltage should be provided from a temperature tracking supply in order to compensate for shifts in the output levels.

In monolithic form, all parasitic capacitances are located at relatively low-impedance points. The collector resistances are low, requiring small area and a low resultant capacitance to ground. The parasitics across the 1,300-ohm resistor are shunted by the emitter impedance of the reference transistor; likewise, the parasitics across the 1,800-ohm emitter resistors are also shunted by low-impedance paths. No coupling capacitors are used; thus, overall circuit area and stray capacitances are reduced; only transistors and resistor (no diodes) are used, minimizing the number of process steps. The $B+$ current is essentially constant due to the differential nature of the circuit; hence, large $B+$ bypass capacitors, difficult to provide in integrated form, are not required. The output levels are a function of the resistance ratio of R_C and R_b and not on their absolute resistance values.

In summary, the emitter-coupled logic circuit, thus designed, accounts for the problems associated with monolithic components. The following describes the test results obtained on RCA's integrated emitter coupled current steered logic circuits (ECCSL).

PERFORMANCE DATA ON RCA DEVELOPMENTAL ECCL GATES

Fig. 4 shows one of the first developmental emitter-coupled monolithic logic gates (TA-5005) developed by RCA; components on the wafer are identical to those of Fig. 3.

Using the test setup shown in Fig. 5, pair delay measurements for the TA-5005 gate were made (see Fig. 6).

Fig. 7 shows an additional configuration tested to determine the feasibility of driving a 100-ohm coaxial line terminated with a 100-ohm resistor. By connecting the low-voltage terminal end of the terminating resistor to the OR output of another TA-5005 circuit (see Fig. 7), a temperature regulating bias potential is established on the 100-ohm resistor which tracks the most negative signal excursion. With a single receiver gate connected at the end of the terminated cable, the pair delay measured at 25°C was 12 nsec (neglecting cable delay). The pair delay increased somewhat when additional gates were tapped onto the coax.

Fig. 8 shows a differential drive scheme for use on long lines; no termination is used at the receiving end. The push-pull signals received are connected to the normal input plus the reference input. Due to the differential input circuit at the remote gate, common-mode noise rejection is excellent; Fig. 9 shows the pair delay (minus line delay) versus temperature curve. Input and output waveforms of the driver and receiver were very clean.

The data presented revealed that the pair delay of the circuit under heavy capacitive loading can be improved from 24 nsec to 12 nsec through the use of the Fig. 8 push-pull drive scheme. Further examination shows that most of the system pair-delay can be attributed to the fact that the output emitter-follower tends to cut off during the downward signal excursion. Under such a condition, the fall time experienced in the test setup of Fig. 5 is dictated by the capacitance load and the 1,800-ohm emitter resistors. However, when using the Fig. 8 differential scheme, there is always one signal at the receiving gate which is a low-impedance, positive-going signal to switch the gate.

Further tests were run to determine the effect on pair delay of the emitter follower being cut off. Fig. 10 shows external emitter resistor R_e added to reduce the fall time significantly under capacitive loading conditions. By connecting R_e to — 1.6 volts (the most negative signal level), the DC current in the output transistor is only increased during positive signal swings.

A performance curve under a fan-out of six plus an additional capacitance of 50 pf was taken as a function of R_e; the results show that with 100 ohms in the emitter circuit, pair delay decreases from 24 to 15 nsec (Fig. 11). Further reduction in pair delay can be accom-

plished by reducing the values of the collector and emitter resistors associated with the differential pair. However, most of the pair delay under capacitance loading conditions (even with 100-ohm emitter resistors) is caused by the emitter follower.

Based on the above considerations, the TA-5038 gate circuit shown in Fig. 12 was developed; this is a 100-mw gate circuit, which is described in another paper.[1] The monolithic circuit incorporates a built-in fixed reference voltage and an effective 100-ohm emitter follower resistor connected to — 1.6 volts. Test results indicate that the circuit exhibits a pair delay of 16 nsec under the conditions indicated in Fig. 5.

A LOOK AHEAD

The experimental results show that monolithic emitter-coupled logic gates, unloaded, exhibit pair delays in the order of 12 nsec; this pair delay is doubled under fan-out of 6 and 50-pf loading conditions, and most of this increase is due to the emitter follower cutting off, *not* the parasitic elements in the monolithic circuit.

It is evident from our data that until computer wiring procedures are modified to reduce stray capacitances, *the limiting factor on circuit speed will be the computer system, not the parasitics within integrated circuits.*

Pressures to reduce the cost per circuit and to increase the speed of the computer are being applied by commercial computer manufacturers; such pressure will force a revolution in the manufacture of integrated circuits. Integrated circuit manufacturers will propose multiple gates per wafer interconnected in some prescribed manner by evaporated metallization; such multiple gates will be sold as functional subsystems prewired according to a specification. This will make possible the ultimate in low cost per circuit and will make possible even faster machines since intercircuit capacitances (within the subsystem) will be an absolute minimum. To accomplish this, logic designers must think beyond the design of individual gates interconnected by the back plane; more important, they must think in terms of *how many logic functions can be performed by some particular cluster of gates interconnected by the component manufacturer and sold as a functional subsystem.*

Only when this happens will the price per circuit drop drastically below the cost of discrete component circuits and then only will the circuit speeds now available from monolithic circuits produce correspondingly faster computer systems.

ACKNOWLEDGMENT

The author wishes to give credit to Michael D'Agostino and Stanley Neimiec for the evaluation and circuit development work cited in this paper, which made possible the conclusions reached.

REFERENCE

1. G. Cohen, "Integrated Circuit Design of a Monolithic Silicon NAND-NOR Gate," TA-5038," RCA ENGINEER, this issue.

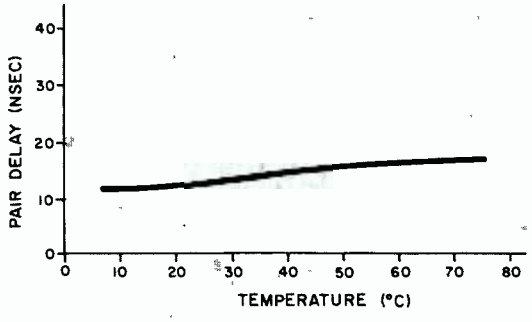


Fig. 9—Curve of pair delay versus temperature.

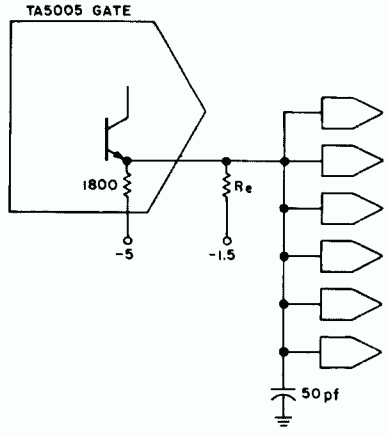


Fig. 10—External emitter resjstor, R_e is added to reduce fall time.

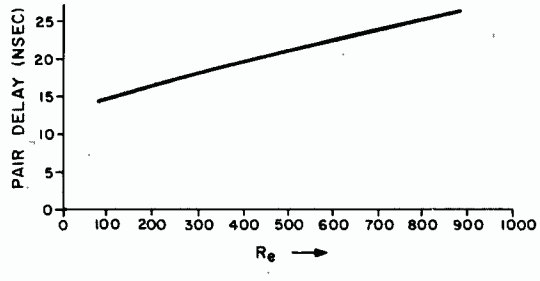


Fig. 11—Curve shawing a decrease in pair delay from 24 to 15 nsec with 100 ohms in the emitter circuit.

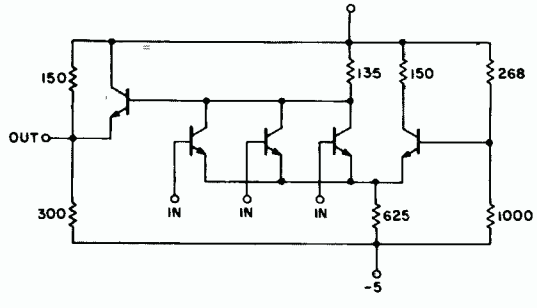


Fig. 12—Diagram of the TA-5038 gate circuit develaped.

DESIGN OF A MONOLITHIC SILICON INTEGRATED CIRCUIT NAND-NOR GATE, TA-5038

A circuit designer experienced with semiconductor devices has a good general background for the design of integrated circuits in monolithic form. For best integrated-circuit performance, however, many special factors must be observed. This paper briefly describes the evaluation of monolithic silicon integrated-circuit design to acquaint circuit designers with the essentials of this new and important technology.

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Somerville, N. J.

THE objective specification for the circuit described herein called for a *nand-nor* gate having a maximum logic input voltage of −5 volts and power-supply voltage up to −10 volts. The gate was to be capable of performing the desired function at temperatures from 10 to 60°C with a power dissipation of less than 100 mw. The logic specification for the *nand-nor* gate required levels of logic $1 = -0.75 \pm 0.10$ volt and logic $0 = -1.55 \pm 0.10$ volt. Fan-in of 7, *nor* fan-out of 6, maximum input capacitance of 5 pf, and maximum propagation delay of 18 nsec were specified. Fig. 1 shows the testing schematics for propagation delay and DC logic levels; Fig. 2 defines some of the terms used. In addition, the circuit was to be designed with a built-in bias driver and to have provision for expandability.

LOGIC FUNCTION

The logic form chosen (Fig. 3) is frequently referred to as emitter-coupled logic (*ECL*). In this developmental circuit (RCA Dev. No. TA-5038), resistor R_1 is a constant-current sink which requires a current of approximately 6.6 ma (that is, $[5.2 - 1.12] \div 620$). The reference potential E_{ref} is obtained by appropriate selection of R_2 and R_3. The bias point is selected to fall midway between the logic levels.

The signals at the inputs to transistors T_3 and T_4 are controlled so that the entire current demanded by R_1 is supplied from these two transistors. If the base of T_3 is more than 0.2 volt above E_{ref}, then T_3 is forward-biased more than T_4, and all current demanded by R_1 emanates from T_3. As a result, the output voltage at point 10 is at a low level.

If the current flows through T_4, then T_3 does not supply current to its collector and the drop across R_4 is eliminated. In this case, point 10 is at a high level.

The output voltage at point 9 is less than that at point 10 by the value of the base-to-emitter voltage V_{be}. That is, when there is a zero voltage at point 10, the voltage at point 9 is equal to V_{be} or about −0.75 volt. If the voltage at point 10 is at a high level, or at −0.8 volt, the output at point 9 is $(0.8 + V_{be})$ or −1.55 volts. The gate thus has two logic levels. These levels are defined by the specification and are determined by the V_{be} of a conventional silicon transistor. Switches of this configuration can be used to form *nand* and *nor* functions by the addition of inputs in parallel with the input con-

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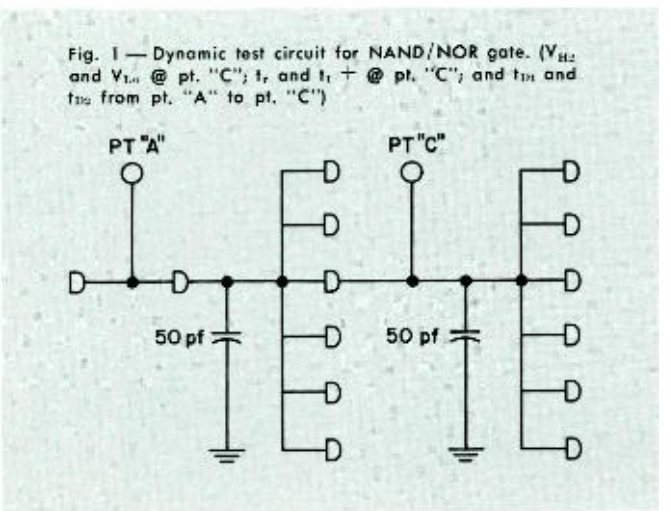

Fig. 1 — Dynamic test circuit for NAND/NOR gate. (V_{H2} and V_{L1} @ pt. "C"; t_r and t_f + @ pt. "C"; and t_{D1} and t_{D2} from pt. "A" to pt. "C")

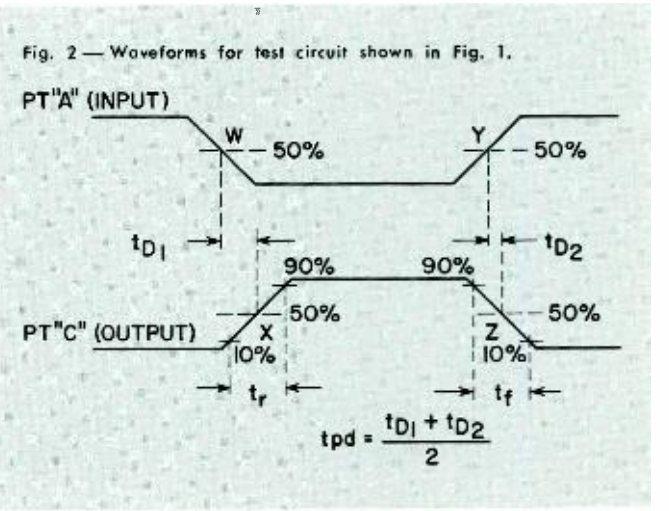

Fig. 2 — Waveforms for test circuit shown in Fig. 1.

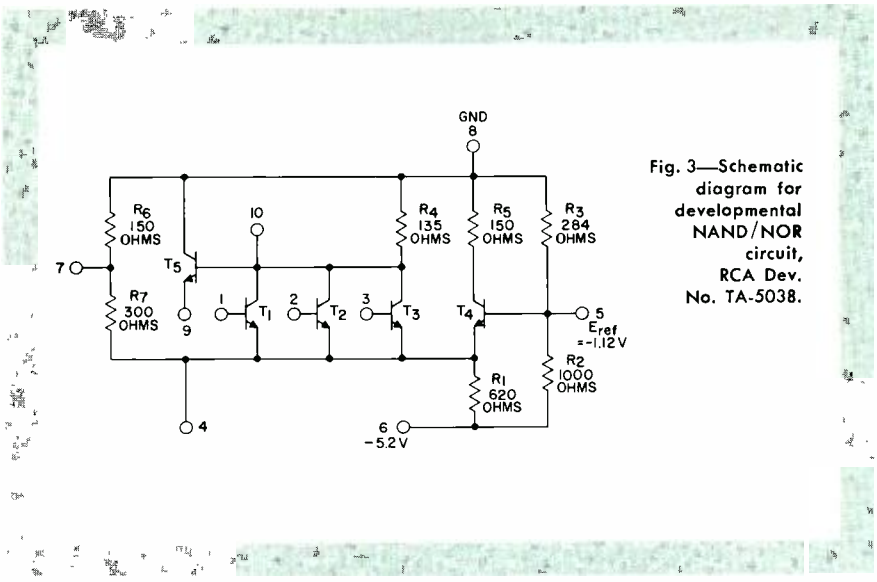

Fig. 3—Schematic diagram for developmental NAND/NOR circuit, RCA Dev. No. TA-5038.

trol transistor T_3. Thus transistors T_1 and T_2 provide two additional inputs to a three-input gate. The developmental circuit described, RCA Dev. No. TA-5038, is a positive *nor* gate or a negative *nand* gate.

DESIGN CONSIDERATIONS

Transistors used in monolithic structures differ from their conventional discrete counterparts in a variety of ways, the two most important differences being much larger output capacitances and larger collector series resistances.

The need for electrically isolating one component from another is satisfied in integrated circuits by imbedding the components in a substrate material and providing a rectifying junction (Fig. 4). The substrate is biased with the most negative potential available to reverse-bias the isolation junction and prevent the signal at the collector from entering the substrate. The result is a depletion region between the collector and the substrate, and an associated parasitic capacitance which produces large output capacitance.

The second difference in an integrated-circuit transistor results from the necessity for making contact to the collectors from the top surface instead of the bottom, as in conventional transistors. This technique increases the effective length of the collector-current path. A first-order increase in collector series resistance results from the use of a lateral current path rather than the longitudinal current path normally obtained in discrete devices (Fig. 4). Introduction of an $n+$ region under the active collector region reduces the series resistance. This effect is inherent in monolithic design and is independent of the circuit being integrated.

However, the collector series resistance is further increased by a second-order effect which is a function of the circuit layout and results from the need for connector crossovers. As shown in the photograph of the TA-5038 in Fig. 5, the collectors of T_1, T_2, and T_3 (represented by numerals 1, 2, and 3) are located at different distances from terminal 10 and therefore are at different potentials from terminal 10 because of the resistance introduced by the common collector connection, or "stripe." The total resistance of the collector stripe in this circuit is 36 ohms (12 ohms associated with each transistor). Of the several possible ways of decreasing this resistance, the simplest is to add a parallel stripe next to the existing collector stripe, thus effectively doubling the line width. In this manner, the total resistance can be reduced by a factor of 4 to 5. However, this modification increases the isolation capacitance as a result of the increased area. The two factors must be weighed carefully to determine the advisability of reducing one at the expense of increasing the other, because circuit performance could be adversely affected by an undesirable choice.

The performance of any circuit is a function of the tolerance of the resistors available. In emitter-coupled-logic circuits, as in many other cases, the absolute value is less important than the ratio of resistor values. The parameters of importance are the absolute value of E_{ref} and the bias points of the transistor collectors. Thus, the potentials of concern can be accurately regulated by close control of the resistor ratios. Fig. 6 shows the tolerance that may be expected with different resistor line widths when there is a constant absolute variation in line width. It follows, therefore, that minimum resistor ratios can be attained only when resistors of identical line width are used. This technique is practical only where the resistor values are of the same order of magnitude. Geometrical considerations would otherwise require areas in excess of that required for good design practice. As an example, if two resistors of 300 ohms and 6,000 ohms were designed to be 1 mil wide, the length ratio would be 10:1. However, a practical minimum length is 10 mils. Therefore, the 6,000-ohm resistor would have to be 200 mils long, too long for a practical design.

PERFORMANCE CHARACTERISTICS

More than 1,000 monolithic gate circuits of the TA-5038 design (shown in Fig. 4) were fabricated and analyzed for performance. These circuits were designed to operate from DC to 5 Mc over the full temperature range −55 to 125°C required by military environmental specifications.

The data given below were accumulated from raw product with only shorts and opens removed. Results were obtained from 271 units having a composite electrical test yield, based on the objective specification, of 45%.

TRANSIENT RESPONSE

The gate described has excellent switching characteristics over the specified temperature range for a fan-out of six, as measured in the circuit of Fig. 1. The rise and fall times of the output pulse showed normal distributions and averaged 14 and 22 nsec, respectively. The rise and fall times were below 18 and 25 nsec in 97% and 85% of the circuits, respectively.

The total *on* delay, Td_1, is measured between the 50% points of the leading edges of the input and output pulses (points w and x on waveforms in Fig. 2). The total *off* delay, Td_2, is measured between the 50% points of the lagging edges of these pulses (y and z in Fig. 2). The average value of these two quantities $[(Td_1 + Td_2) \div 2]$ is defined as average propagation delay.

A median propagation delay of 17.0 nsec was determined for the TA-5038. Values as low as 14 nsec were observed; 68% of the circuits had values below 18 nsec.

Total *on* and *off* delays ranged from 13 to 23 nsec, with median values of 18 and 16 nsec, respectively. All of these statistics were measured with a fan-out of six and a capacitive load of 50 pf.

The variation of propagation delay as a function of temperature is shown in Fig. 7. The curve shows a reduction in speed of approximately 2:1 as the temperature increases from 27 to 125°C.

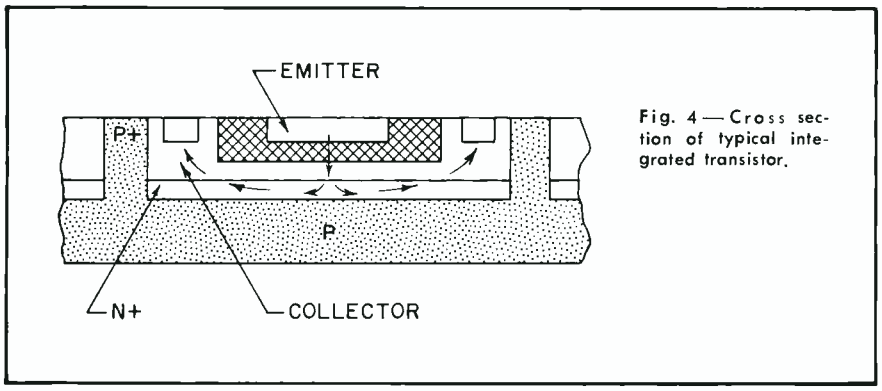

Fig. 4 — Cross section of typical integrated transistor.

The distribution of the high-voltage logic level closely follows a normal distribution, with a median value of 1.62 volts. Of the fabricated circuits, 63% were within the specified limits.

A comparable distribution for the low-voltage logic level showed similar results, with a median value of 0.82 volt. There were 64% of the circuits within the specified limits.

CONCLUSIONS

The results described indicate that integrated-circuit technology is capable of generating low-voltage digital circuits. As better parts and improved techniques are developed, the over-all capability will be enhanced. However, the basic rules of monolithic design will remain valid. A working knowledge of these principles and an appreciation of the required compromises will enable the circuit designer to design useful and reliable integrated circuits.

ACKNOWLEDGMENT

The author wishes to thank H. Criscito, R. Grant, and A. Storz for their efforts in fabricating the devices; M. D'Agostino for his labors in accumulating the electrical data; and R. Kroll for his assistance in tabulating the data.

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GENE COHEN received his BSME from the College of the City of New York in 1951. He has taken graduate courses in EE at CCNY, and courses in solid-state physics at Northeastern University. He was employed by Sylvania Electric Products, Inc., from 1955 to 1958 as a development engineer working on p-n-p and n-p-n silicon and germanium transistors. From 1958 to 1959, he was responsible for the development of a commercial line of high-current silicon rectifiers at the Chatham Division of Tung-Sol Electric Corporation. He joined the RCA Semiconductor and Materials Division in 1960, and was instrumental in developing a line of both germanium and silicon multiple packaged computer diodes. These devices were the forerunners of the DMC and Integrated-Circuit Programs at RCA. He is presently group leader in integrated-circuit design and is responsible for bipolar integration projects. Mr. Cohen is a registered Professional Engineer in New York State. He is a member of the IEEE and the Group on Electron Devices. He has served as a member of JEDEC Semiconductor Committees on Small Signal Diodes (JS-1) and Mechanical Standardization and Packaging (JS-10).

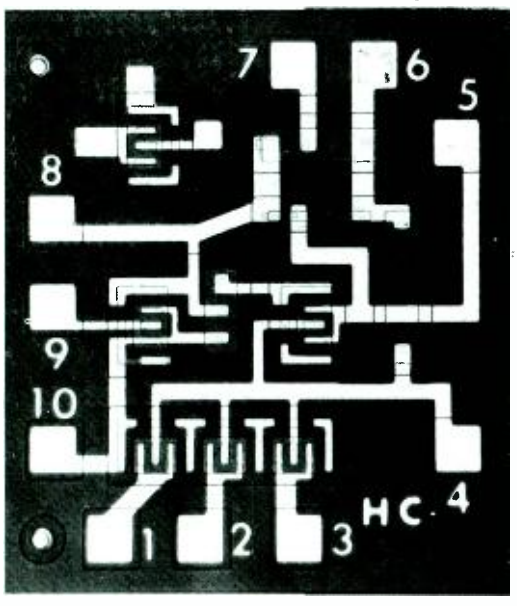
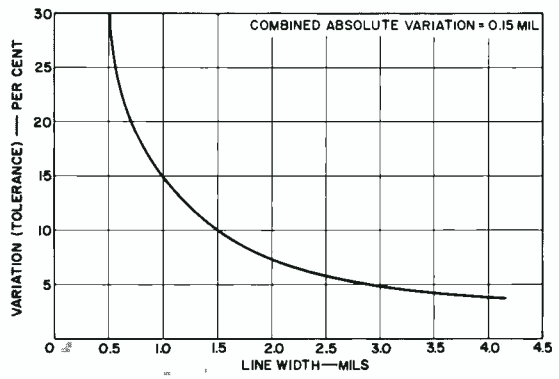


Fig. 5 — Photomicrograph of Dev. No. TA-5038.

Fig. 6 — Resistor tolerance as a function of line width.



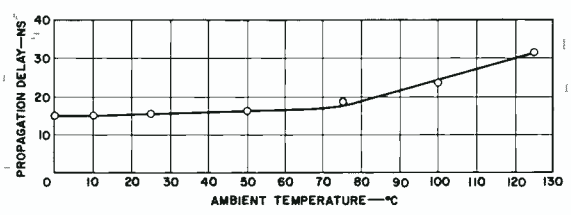


Fig. 7 — Propagation delay as a function of temperature.

DIGITAL INTEGRATED CIRCUITS FOR SATELLITES

Reduction of size and weight, and the promise of higher reliability are obvious advantages of integrated circuits for satellite systems; with increasing frequency, such circuits will replace standard components in the design of satellite systems. Immediate space satellite use is found in digital circuits because of the relative ease of design and fabrication and the small number of basic building blocks required for most logic systems. The use of integrated circuits is reviewed herein for space applications in relation to AED experience with a clock that was designed for a company-sponsored program on integrated circuits. Circuit considerations, reliability, packaging, environmental tests, and costs are included.

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THE application of integrated digital circuits is particularly fruitful in such systems as the TIROS spacecraft in which 70% of the transistors are contained in the digital circuits. Future spacecraft for more sophisticated missions promise to contain even more digital circuitry, suggesting that designers of these future satellite systems will need integrated-circuit application know-how equal to their knowledge of transistor applications.

Because of the decreased size of integrated circuits, the greater use of redundant equipment will improve mission reliability and performance. For example, sufficient weight and space could be saved to permit an additional camera to be used on a TIROS satellite, thus improving coverage or extending the useful life of the satellite.

A satellite digital clock subsystem was used to investigate both the impact of integrated circuitry on satellite systems and on mechanical packaging problems inherent in this new technique. The digital clock subsystem is typical of the logic circuits currently employed in satellites such as the TIROS series, and thus serves as a practical model for projecting the application of integrated circuits to a total spacecraft system.

A comparison of the two clocks (conventional and integrated) demonstrates the dramatic decrease obtained in size and weight; the difference in size is illustrated below and in Fig. 1.

	Conventional Clock	Integrated-Circuit Clock
Size, in³	83	11
Weight, lbs	3.5	0.5
No. of Logic Elements	45	66
Assembly Method	Soldered	Welded
Power, watts	0.7	1.0

Since certain types of low-power integrated circuits were not available during the early design phase of the integrated circuit clock, a slight increase in power consumption resulted. This situation is not inherent in the use of integrated circuits; on the contrary, the variety of integrated circuits now available will allow power reductions that correspond to the physical reduction.

CLOCK OPERATION

The clock subsystem (Fig. 2) provides remote programming of the satellite when the spacecraft is out of range of the ground station; the clock provides a programmable delay time T_o of up to 4.096 seconds, followed by a fixed sequence of operations such as a series of pictures or a satellite magnetic attitude control program. The integrated-circuit clock is composed of four major logic blocks:

1) *data former*, which develops shift and transfer pulses from the ground transmitted data;
2) *sequencer*, which generates signals that control the various working modes of the clock;
3) *buffer shift register*, which temporarily stores data that is later transferred to the Programmer Register; and
4) *programmer register*, which provides the actual delay time T_o and the preset program.

The heart of the clock system is a 16-bit (stage) binary counter contained in the programmer register. To select a delay time T_o from ground programming, the binary counter is preset to the complement of one-half of the delay time T_o desired. For example, when a 1,000-second delay is desired, the binary number 1,548 (the complement of the binary number 500) is stored in the first 11 bits of the counter; after 1,000 seconds, the eleventh stage overflows at the count of 2,048 and the program sequence is initiated. Bits 12 to 16 are also loaded from the ground to provide the desired program sequence combinations.

The buffer shift register temporarily stores the ground-programmed binary word which contains the T_o delay complement and the program sequence word. As the bits are stored in the buffer register, they are simultaneously routed to the corresponding bits of the programmer. This register was not necessary in the conventional-circuit clock where separate control of the bases of the flip-flop transistors permitted both shift and count with the same flip-flop. If more flexible integrated circuits had been available, a shift-register-counter could have been designed for the programmer in the integrated-circuit clock, and the buffer shift register could have been eliminated. This difference in the

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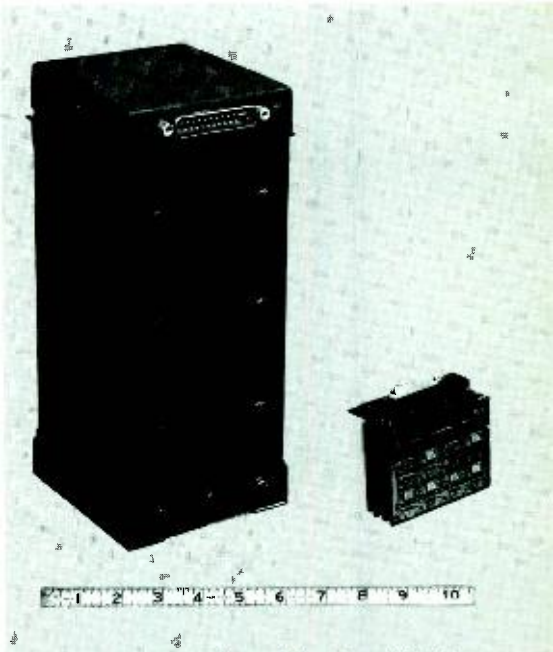

Fig. 1—A comparison of the sizes of the two digital clocks. (the integrated-circuit clock is on the right.)

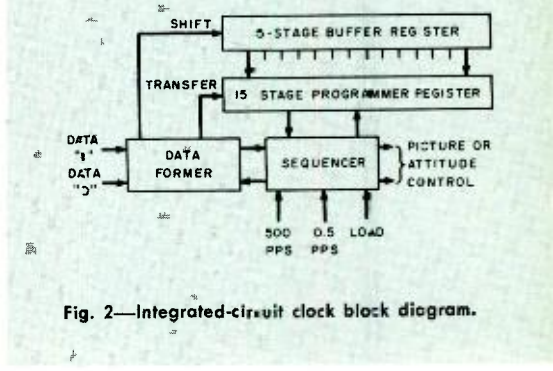

Fig. 2—Integrated-circuit clock block diagram.

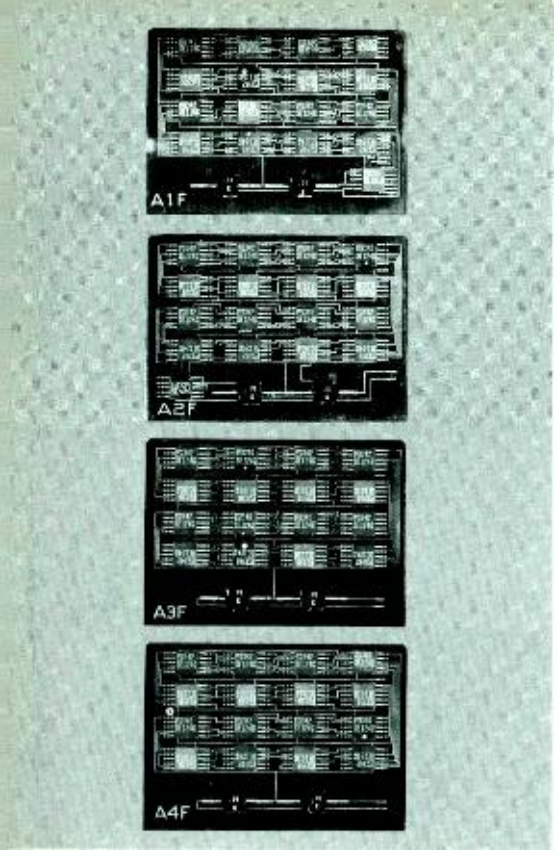

Fig. 3—The four digital clock printed-circuit boards, with the flat packs packaged in a planar array.

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A. I. ARONSON graduated from Syracuse University in 1951 with a BEE degree. He joined RCA in 1951 and worked on the design of low-frequency amplifiers, magnetic recording circuits, video synchronizing generators, medical electronics, and on analog-to-digital convertors, with special emphasis on the application of transistors. Mr. Aronson also taught courses at Camden and Moorestown in low-frequency transistor circuits. He has published many technical papers and holds six patents in the field of transistor applications. Mr. Aronson transferred to the Astro-Electronics Division in 1958 and became engaged in the design and development of satellite command systems. He had a major role in the development of the spacecraft command systems for SCORE, the TIROS I and II satellites, and Stratascope II. Mr. Aronson assumed his present position in 1961. His duties include the design and development of satellite command systems, data handling systems and related components for a wide variety of spacecraft. Mr. Aronson is a member of the IEEE.

C. STALOFF is currently leading the AED Integrated Circuit AR&D program. Mr. Staloff was graduated from Stevens Institute of Technology in 1956 with a ME degree with highest honors; he also has a MSEE degree from the same institute. Mr. Staloff joined RCA in 1961 having come from ITT Laboratories where he was associated with a wide scope of activities ranging from the design of Sonar System simulation and navigation equipment to the design and development of generalized solid state equipment. At RCA, Mr. Staloff has been associated largely with the OGO project, TIROS, and classified satellite programs. Mr. Staloff is a member of Tau Beta Pi, IEE, and Sigma Xi.

P. J. TRUSCELLO received a BSME degree from Drexel Institute of Technology in 1962. After graduation, Mr. Truscello joined the tactical radio group of RCA's Communications Systems Division where he participated in the mechanical development of combat transceivers. In 1963, Mr. Truscello joined the Astro-Electronics Division and was assigned to the Electro-Mechanical Packaging Group. He has worked on RANGER, RELAY, TIROS and several classified projects.

two clocks accounts for more circuits being used in the integrated-clock circuit; however, the increased circuitry is not considered a serious limitation since performance is significantly more reliable than that of the conventional clock.

RELIABILITY

In any space application, reliability is of paramount importance. Fortunately, early life test data from several manufacturers and government agencies[1] indicates that typical integrated-circuit flip-flops (containing as many as 12 transistors and several diodes) are as reliable as a *single* high-quality Mil-Spec transistors.

Another important factor is the improved reliability of interconnections inherent in integrated circuits. The conventional components to be hand-welded or solder-connected in conventional circuitry are often supplied by many different manufacturers; thus, it is difficult to control the many variables affecting interconnection reliability.

By contrast, the integrated circuit interconnections are fewer and are formed simultaneously by evaporation so that a more uniformly controlled product results. Such interconnections are tested by the manufacturer *before* the circuits are integrated into the final system, providing an additional controlled check on connection integrity. A comparison of failure rates[2] is given above for both clocks; the latest accepted component failure rates are indicated.

Conventional Clock

Part	Failure Rate (%/1,000 hrs)	No. of Parts	Total
Trans.	.02	45	0.9
Diodes	.01	206	2.06
Resist.	.001	237	0.237
Capac.	.001	64	0.064

Total Failure Rate = 3.261%/1,000 hrs

Integrated-Circuit Clock

66 integrated circuits @ .02%/1,000 hrs
= 1.32%/1,000 hrs

For a mission life of 8,640 hours (one year) the probability of survival P_s may be computed by: $P_s = exp(-t/m)$. Where: P_s is probability of survival; t is time (8,640 hours); and m is mean-time-to-failure (the reciprocal of the percent of failures per thousand hours).

The probability of survival is 86.5% for the integrated-circuit clock and 76% for the conventional clock. This comparison probably favors the conventional clock since no degradation or failure was assigned to the interconnections of the welded cordwood modules while the interconnection reliability is contained in the failure rates used for the integrated circuits. Failure rates for the integrated clock correspond to 125°C ambient temperature operation; however, satellite temperatures seldom exceed 50°C and generally average 25°C so that additional life over that predicted would appear possible.

MECHANICAL PACKAGING

The packaging phase of the clock offered an excellent opportunity to evaluate various methods of assembling integrated circuits into a practical unit that could survive the rigorous environmental tests commonly employed on spacecraft components.

The actual assembly method selected was a simple straightforward technique providing ease of assembly, test, and debugging. The clock was fabricated on four double-sided, Kovar printed circuit-boards (Fig. 3); two boards held 17 circuits each, and the remaining two held 16 circuits each. The boards measured 2.0 × 2.8 × 0.031 inches. A mother board provides means for interconnecting the four boards to the satellite system cable.

The low-power consumption of the unit permits conductor runs, 0.010-inch wide, and welding pads 0.020 inch wide. Consequently, a drawing scale of 12 to 1 allowed the draftsmen to use standard ⅛-inch tape for conductor runs and ¼-inch tape for welding pads on all printed-circuit-wiring layouts. The circuitry was divided so that the four similar boards used a standard wiring layout drawn and reproduced, full size, on chronoflex sheets; nonstandard conductor runs were then added to complete the layouts. Reproducing the standard layout instead of redrawing it for each nonstandard conductor run saved considerable drafting time.

The integrated circuits were welded to the printed boards by parallel-gap welding (Figs. 4 and 5). In this application, welding is superior to dip soldering

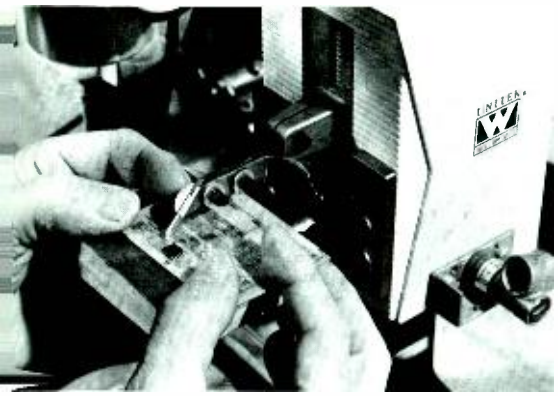
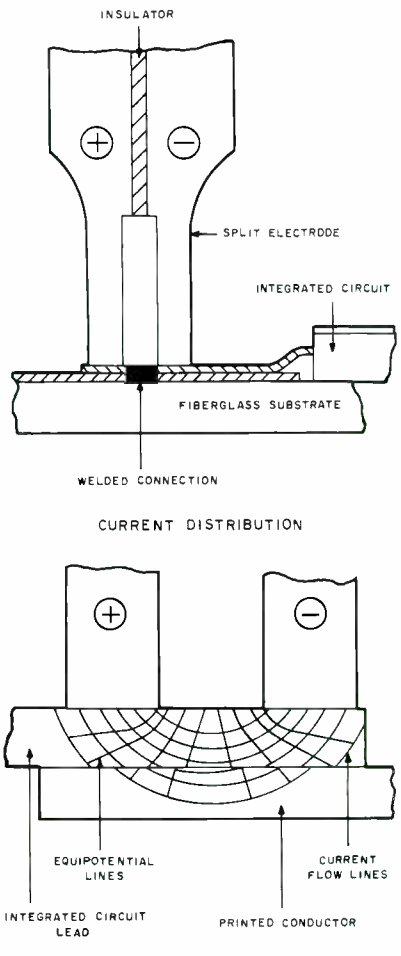


Fig. 4—The parallel-gap resistance-welding equipment in use.

Fig. 5—Parallel-gap welding and the current distribution it produces during welding of the integrated circuit.



since less heat is generated, thus permitting denser packaging. In the welding process, the absence of fluxes produces joints which are easier to clean; stronger joints also result because welding variables are more easily controlled.

ENVIRONMENTAL CONSIDERATIONS

Clock circuit environmental tests are summarized above; the clock operated successfully without failure before, during, and after these tests.

Random Vibration

	Thrust Axis	Each Lateral Axis
Bandwidth, cps	20-2,000	20-2,000
Duration, min	2	2
Level, g(rms)	35	25

Thermal Vacuum

Pressure: 5×10^{-5} mm-Hg
Initial temperature: +60° C, for 12 hours
2nd temperature: +25° C., for 12 hours
3rd temperature: −15° C, for 12 hours
Final temperature: +25° C, until stabilized

No problems arose during mechanical environmental tests even though no conformal coating was used on the integrated circuit clock. This is important because considerable effort, time, and expense is devoted to potting and conformal coating of spacecraft hardware to insure survival during launch. Since some problems were encountered with humidity, some form of moisture protection is still required for the boards.

COST

While too little manufacturing experience is available to accurately estimate the cost for fabrication and assembly of the integrated-circuit clock, a conservative prediction is that the manufacturing costs will at least be equal for the two types of clocks. The cost saving expected must come from a projected integrated circuit cost in the next two years where module prices of less than $10 are quoted; this price compares with an average of $50 for the conventional modules indicating a decided cost advantage using integrated circuits. Some additional cost savings will result from less need for sophisticated conformal coating and potting processes of the type employed at AED for the past few years.

INTEGRATED CIRCUITS APPLIED TO A COMPLETE SATELLITE SYSTEM

Upon completion of the integrated-circuit clock, a study was undertaken to evaluate the application of integrated circuits to the digital portion of a complete satellite system. The system chosen for this study was the TIROS-Wheel spacecraft which contained a significant portion of its semiconductors in the command and control equipment. This equipment consisted of the following components:

decoder, which demodulates the digital data, checks the data for errors, and decodes the words into appropriate channels;

command programmer, which is similar to the programmer discussed earlier in the paper except that it performs a more varied program and sequence; and

command distribution unit, which converts the digital commands into stored commands and which also contains command and redundancy switching.

The decoder and the command programmer are duplicated to provide redundancy. Since the command distribution unit required relays, power switches, and other large components, there would have been little to gain by using integrated circuits in this unit; however, the other two units did provide a good application comparison between integrated circuits and conventional circuits. Listed below is a summary of the important comparisons resulting from this study:

	Conventional Cordwood Circuits	Integrated Circuits
Power, watts	3.0	0.3
Volume, in³	588	197
Weight, lbs	17.4	5.7
Module Count	330	300

In two important areas—*power* and *module count*—a significant improvement was noted compared with corresponding areas in the study discussed earlier in the paper. The lower power resulted from the use of low-power integrated circuits which were not available during the development of the integrated-circuit clock; the favorable module count resulted because the limitation imposed by the use of a shift-count function was relatively less important when the whole system (where much control logic is used) is considered. On the other hand, the weight and volume comparisons were not as favorable because more interface circuits using conventional components were required.

CONCLUSIONS

From a size, weight, reliability, and cost standpoint the integrated circuit clock has shown dramatic advantages over the conventional clock. The conclusion from this improvement is inescapable: future spacecraft electronics will rely heavily on the use of this new technique. The impact will be so great that we expect the conversion from transistors to integrated circuits to be faster than that of tubes to transistors. Systems design in progress today at AED is already being planned around integrated circuits for tomorrow's spacecraft.

ACKNOWLEDGEMENTS

Acknowledgement is made to co-workers B. L. Matonick and S. Teitelbaum who contributed much to the work reported herein.

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P-N-P/N-P-N COMPLEMENTARY MONOLITHIC SILICON INTEGRATED CIRCUITS

The use of complementary and symmetrical p-n-p and n-p-n transistors in integrated circuits provides distinct advantages in many types of applications. For example, such circuits can be used to improve the speed-power relationship in digital circuits and to replace the transformer in push-pull amplifier circuits. This paper briefly describes the advantages of the complementary structure in typical applications, and discusses the related fabrication processes.

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EUGENE C. CONSER received his BSEE from Penn State in 1961 and is presently studying for his MSEE at Newark College of Engineering; in 1961, he joined Westinghouse Electric Corporation, Semiconductor Division where he designed and developed epitaxial growth systems and was responsible for the first production epitaxial growth furnaces at that site. In 1963 Mr. Conser joined the Integrated Circuits Department of RCA's Semiconductor and Materials Division; he designed NPN Integrated Circuits and is currently working on fabrication techniques for bi-polar complementary PNP-NPN integrated circuits. Mr. Conser is a member of IEEE, of Sigma Tau, and of Eta Kappa Nu.

BECAUSE of the extremely small size of integrated circuits, standard-size or even miniature-type coils, transformers, and capacitors cannot be used without a major sacrifice in circuit size and reliability. To eliminate the need for coils and large capacitors, designers have resorted to such compromises as the use of RC instead of RLC tuning, and direct instead of capacitor coupling. To replace the coupling transformer in source applications, they are now designing complementary integrated circuits using symmetrical *p-n-p* and *n-p-n* transistors. For example, a complementary *n-p-n/p-n-p* integrated circuit eliminates the need for the conventional coupling transformer in a push-pull amplifier circuit.

The use of complementary transistors also offers advantages in the design of other analog circuits. In conventional amplifier stages, for example, it is common practice to use one transistor in the grounded-emitter configuration to amplify the input signal and a second transistor as an emitter follower for phase inversion (to provide an output signal which has the same phase as the input signal). When transistors of the same type are used in both stages, the circuit amplification is proportional to the beta (common-emitter current transfer ratio) of the individual transistor type. When complementary *p-n-p* and *n-p-n* transistors are used (*n-p-n* for the amplifier and *p-n-p* for the inverter), however, gain becomes proportional to the product of the betas of the two transistors. Consequently, greater gain can be realized with fewer transistors.

In digital circuits, complementary *p-n-p/n-p-n* structures can be used to provide higher speeds with lower power dissipations, and also to increase the range of operating temperatures.

Although the complementary structure offers many advantages as compared with single-type transistor circuits, fabrication of complementary circuits is more complicated. Depending on the complexity of the structure, at least one and usually many extra fabrication steps are required.

In the two general types of complementary structures presently being used, the *p-n-p* and *n-p-n* transistors are either partially isolated by a single diode between their collectors (Fig. 1), or completely isolated by means of back-to-back diodes (Fig. 2a) or by dielectric material (Fig. 2b). The completely isolated structure can be used in any type of complementary circuit; the use of the partially isolated structure is somewhat restricted by the requirements that the single diode be reverse-biased and that the collectors of all *p-n-p* units be common.

Although the fabrication processes used for complementary circuits are similar to those used for other integrated circuits (described by Saunders in another paper[1]), additional photoresist and diffusion steps are required. Fig. 3 shows both a conventional *n-p-n* integrated-circuit wafer and a complementary *p-n-p/n-p-n* structure, and lists the major processing steps in the fabrication of each type. In effect, the complementary structure requires an additional photoresist and diffusion step for the deposition of the *p*-type collector, and duplication of the photoresist and diffusion steps for the deposition of bases and emitters.

Because of the additional fabrication steps required for complementary integrated circuits, extra care must be used during processing to maintain reasonable yields. With the continuing improvements in fabrication techniques, however, it is felt that in the near future complementary circuits will be no more difficult to make than the now-standard *n-p-n* devices.

Final manuscript received August 21, 1964

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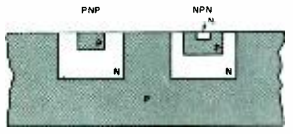

Fig. 1—Partially isolated complementary structure. Transistors are separated by a single diode.

Fig. 2—Completely isolated complementary structures in which transistors are separated by back-to-back diodes (a), or by dielectric material (b).

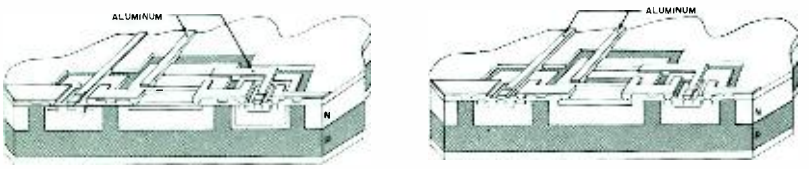

Fig. 3—Conventional n-p-n integrated-circuit wafer (a) and complementary p-n-p/n-p-n structure (b). At right is a comparison of steps involved in fabrication of each. (Assume appropriate photo-resist steps, which are omitted here for simplification.

N-P-N	P-N-P/N-P-N
1. Oxidation	1. Oxidation
2. Isolation deposition	2. Isolation deposition
	3. P Collector deposition
3. Isolation Drive-in	4. Isolation and P Collector Drive-in
4. P Base Deposition	5. P Base Deposition
	6. N Base Deposition
5. Base Drive-in	7. P and N Base Drive-in
6. N Emitter Deposition	8. P Emitter Deposition
	9. N Emitter Deposition
7. Emitter Drive-in	10. Emitter Drive-in
8. Contacts	11. Contacts
9. Al Evaporation	12. Al Evaporation
10. Interconnections	13. Interconnections

COMPUTER ANALYSIS OF AN INTEGRATED CIRCUIT AMPLIFIER

Integrated circuit design causes a new and costly time lag to exist from conception to device; as a result, the designer must avail himself of new tools to insure an accurate and correct design on the first try. This paper describes a mathematical approach, utilizing a computer, for predicting the behavior of an active linear circuit after it has been integrated. The simple but powerful computer analysis technique described herein is based upon the nodal equations of a complete amplifier. It provides a unified approach to linear circuit analysis, in place of the conventional piece-meal approach requiring three separate equivalent circuits (one each for low, midband, and high frequencies). Further, this technique is applicable to any system which can be described by a set of linear simultaneous complex equations.

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A three stage differential amplifier using 2N918 transistors was selected to demonstrate the feasibility of an analysis method for an integrated-circuit amplifier employing computer techniques. The procedure followed was to write first the circuit equations for, and to calculate the frequency response of three stages of the discrete circuit of Fig. 1.

An integrated version of this same circuit was then simulated by including parasitic capacitances and resistances characteristic of such circuits. The equations for the latter case were next written, the values of all parasitic components set close to zero, and the response again calculated. The two responses were found to be in excellent agreement. Satisfied that the equations for the circuit including the parasitic components did in fact degenerate to the discrete case, the response was calculated with the parasitics taking on actual values (obtained from RCA, Somerville). The high-frequency 3-db point was found to drop from 20 Mc for the discrete case to approximately 10 Mc for the simulated integrated circuit. This calculated 50% reduction in bandwidth agreed very well with the change in bandwidth observed in the laboratory between a general purpose integrated amplifier, and its discrete equivalent.

DISCRETE CIRCUIT ANALYSIS

A single stage of the amplifier circuit under examination is shown in Fig. 1. Using the transistor y parameter equivalent circuit of Fig. 2, the single-stage equivalent circuit of Fig. 3 was constructed; corresponding nodes of Figs. 1 and 3 are labeled. The overall three-stage equivalent circuit is shown in Fig. 4.

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A nodal approach was the most logical method of analyzing the configuration of Fig. 4, and was enhanced by the fact that the complex y parameters of the 2N918 were available over the frequency range of interest. These parameters, published for only the common emitter configuration, were converted where necessary to the common collector and common base parameters as follows:

The seven simultaneous complex nodal equations describing circuit operation were next written as shown in Fig. 5a and the coefficients then arranged in the matrix form shown in Fig. 5b.

As a final step, the computer was programmed to pick up the transistor y parameters and solve for the complex elements of the matrix at each frequency, as well as to invert the matrix for the complex node voltages. The amplifier gain was made numerically identical to the voltage of the output node e_o by taking the input voltage e_i equal to unity. Further, the computer was instructed to take 20 $\log_{10} |e_o|$ thereby giving the gain directly in db. A plot of this computer-calculated response is shown in Fig. 8.

SIMULATED INTEGRATED CIRCUIT ANALYSIS

As a first approximation toward simulating integrated circuit behavior of the discrete circuit of Figs. 1 and 3, the collector parasitics of Fig. 6 were introduced into the collector circuit of each transistor.

A new overall three-stage equivalent circuit was then drawn and an analysis identical to the one just described, performed. This circuit is shown in Fig. 7a and its thirteen nodal equations in Fig. 7b; a new FORTRAN computer program was then written to solve the resulting 13 x 13 matrix. To insure that this new equivalent circuit and computer program truly represented a more generalized description of the original circuit of Fig. 4 and did in fact degenerate to that case, all the collector parasitics were initially given values close to zero; to actually set them equal to zero would have caused difficulties in the computer program. The resulting computer-calculated response differed from that of the discrete case in only the third significant digit.

Satisfied that this equivalent circuit and computer program were valid, the parasitics were then given the values indicated in Figs. 6 and 7, and the response again calculated; the results are shown plotted in Fig. 8. As can be seen, the 3-db point dropped from 20 Mc for the discrete case to approximately 10 Mc for the simulated integrated case. These results confirmed previous observations in the laboratory.

ALAN G. ATWOOD received his BSEE from Northeastern University in 1957, and his MSEE in 1960 from the Massachusetts Institute of Technology where he was employed as a Research Assistant in the Instrumentation Laboratory. From 1960 to 1961 Mr. Atwood worked for the Systems Division of Beckman Instruments, Inc., Fullerton, California as an Associate Systems Engineer. Since joining RCA in 1962, Mr. Atwood has engaged in laboratory development of advanced switching techniques; he developed the system design equations and feedback relationships of a hybrid closed loop low-level magnetic multiplexing system, and has more recently been active in the computer analyses of multistage amplifier circuits. He has coauthored numerous RCA reports on this work. Mr. Atwood is presently engaged in a program investigating mathematical techniques for fault isolation. He is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, and IEEE.

LAURENCE C. DREW received his BSEE in June 1960 from Tufts University. Prior to that time, Mr. Drew spent three years as an electronic technician for the U.S. Army during which time he taught electronics to Army personnel who later operated and maintained Nike systems. While attending college, Mr. Drew was a research assistant engaged in designing and testing instrumentation for physiological studies of the brain. Mr. Drew joined RCA in 1962 as a Member of the Technical Staff; he has worked in the field of high-speed pulse circuitry and wideband video amplifiers. Presently, he is a task engineer on a company-sponsored AR&D program to develop integrated analog circuits; this effort commenced in July of 1963. Mr. Drew has disclosed two inventions in the field of high-speed pulse circuitry and one in integrated circuit technology. Mr. Drew is a member of the IEEE.

A. G. Atwood

L. C. Drew

ADDITIONAL APPLICATIONS

Fig. 9 shows a five stage high-gain broadband amplifier to which this technique was applied to obtain its frequency response. The computer solution of the 21 simultaneous complex nodal equations describing the circuit is plotted in Fig. 10, along with the laboratory measured response. Note how well the two curves agree, especially in the immediate region of high frequency roll-off. A greater appreciation for the correlation between the two curves is had when it is realized that strictly *typical* values of transistor *y* parameters were used in the mathematical solution.

Although frequency has been the only parameter thus far varied, it seems equally certain that tabulated values of non-linear elements such as integrated resistors and capacitors could as easily be handled. For example, tabulated values of expected variations in R_b, Fig. 1, from unit to unit, or as a function of temperature could be individually introduced into the circuit equations, in the same manner that the various transistor *y* parameter values were handled above, and the matrix solution of node voltages then obtained with each different value; sets of parametric curves could thus be generated for evaluation.

Further, since it is very little work to write the circuit equations, it becomes mathematically simple to handle distributed circuit components as described by networks of discrete components. The discrete representation of an integrated resistor Fig. 11 is a typical example; the values of the various capacitors and resistors are set by a specific value of reverse junction voltage.

Despite the fact that many additional nodes would thereby be introduced into the overall circuit, the size of the matrix to be solved is not necessarily increased. This is true because we are not specifically interested in the voltages at these new "conceptual" nodes. A criterion for

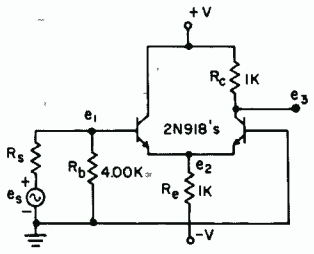


Fig. 1 — Single - stage differential amplifier.

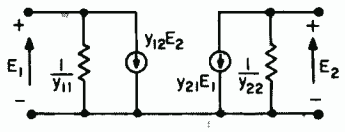


Fig. 2 — Transistar y equivalent circuit.

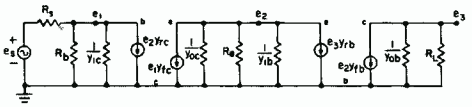
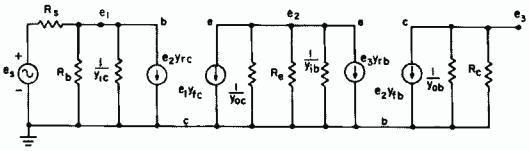
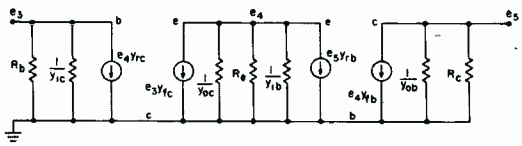
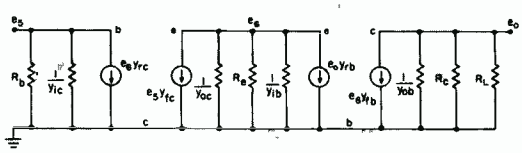


Fig. 3 — Single-stage equivalent circuit.

Fig. 4 — Three-stage equivalent circuit, discrete case.







e_1	e_2	e_3	e_4	e_5	e_6	e_0	
$A_{1,1}$	$A_{1,2}$	0	0	0	0	0	$A_{1,8}$
$A_{2,1}$	$A_{2,2}$	$A_{2,3}$	0	0	0	0	0
0	$A_{3,2}$	$A_{3,3}$	$A_{3,4}$	0	0	0	0
0	0	$A_{4,3}$	$A_{4,4}$	$A_{4,5}$	0	0	0
0	0	0	$A_{5,4}$	$A_{5,5}$	$A_{5,6}$	0	0
0	0	0	0	$A_{6,5}$	$A_{6,6}$	$A_{6,7}$	0
0	0	0	0	0	$A_{7,6}$	$A_{7,7}$	0

Fig. 5b—Coefficients of equations of Fig. 5a arranged in 7 x 7 matrix form.

Fig. 5a—Seven simultaneous complex nodal equations describing circuit operation.

$$e_1\overbrace{\left[\frac{1}{R_a}+\frac{1}{R_b}+y_{ic}\right]}^{A_{1,1}}+e_2\overbrace{\left[y_{rc}\right]}^{A_{1,2}}=e_s\overbrace{\left[\frac{1}{R_a}\right]}^{A_{1,8}}$$

$$e_1\overbrace{\left[y_{fc}\right]}^{A_{2,1}}+e_2\overbrace{\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]}^{A_{2,2}}+e_3\overbrace{\left[y_{rb}\right]}^{A_{2,3}}=0$$

$$e_2\overbrace{\left[y_{fb}\right]}^{A_{3,2}}+e_3\overbrace{\left[y_{ob}+y_{ic}+\frac{1}{R_c}+\frac{1}{R_b}\right]}^{A_{3,3}}+e_4\overbrace{\left[y_{rc}\right]}^{A_{3,4}}=0$$

$$e_3\overbrace{\left[y_{fc}\right]}^{A_{4,3}}+e_4\overbrace{\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]}^{A_{4,4}}+e_5\overbrace{\left[y_{rb}\right]}^{A_{4,5}}=0$$

$$e_4\overbrace{\left[y_{fb}\right]}^{A_{5,4}}+e_5\overbrace{\left[y_{ob}+y_{ic}+\frac{1}{R_c}+\frac{1}{R_b}\right]}^{A_{5,5}}+e_6\overbrace{\left[y_{rc}\right]}^{A_{5,6}}=0$$

$$e_5\overbrace{\left[y_{fc}\right]}^{A_{6,5}}+e_6\overbrace{\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]}^{A_{6,6}}+e_0\overbrace{\left[y_{rb}\right]}^{A_{6,7}}=0$$

$$e_6\overbrace{\left[y_{fb}\right]}^{A_{7,6}}+e_0\overbrace{\left[y_{ob}+\frac{1}{R_c}+\frac{1}{R_L}\right]}^{A_{7,7}}=0$$

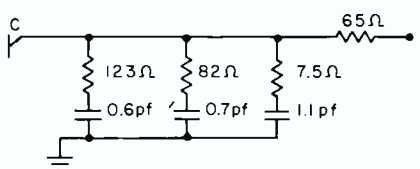
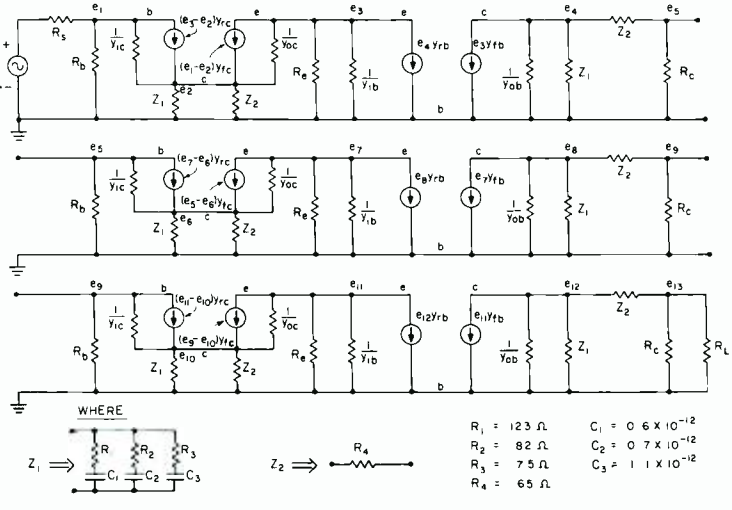


Fig. 6 — Collector parasitics.

Fig. 7a — Simulated integrated circuit, three-stage equivalent.



$$e_1\left[\frac{1}{R_s}+\frac{1}{R_b}+y_{ic}\right]-e_2\left[y_{ic}+y_{rc}\right]+e_3y_{rc}=e_s\left[\frac{1}{R_s}\right] \quad (1)$$

$$e_1\left[y_{ic}+y_{fc}\right]-e_2\left[y_{ic}+y_{rc}+y_{fc}+y_{oc}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]+e_3\left[y_{rc}+y_{oc}\right]=0 \quad (2)$$

$$e_1\left[y_{fc}\right]-e_2\left[y_{fc}+y_{oc}\right]+e_3\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]+e_4\left[y_{rb}\right]=0 \quad (3)$$

$$e_3\left[y_{fb}\right]+e_4\left[y_{ob}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]-e_5\left[\frac{1}{Z_2}\right]=0 \quad (4)$$

$$e_4\left[\frac{1}{Z_2}\right]-e_5\left[\frac{1}{Z_2}+\frac{1}{R_e}+\frac{1}{R_b}+y_{ic}\right]+e_6\left[y_{ic}+y_{rc}\right]-e_7\left[y_{rc}\right]=0 \quad (5)$$

$$e_5\left[y_{ic}+y_{fc}\right]-e_6\left[y_{ic}+y_{rc}+y_{fc}+y_{oc}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]+e_7\left[y_{rc}+y_{oc}\right]=0 \quad (6)$$

$$e_5\left[y_{fc}\right]-e_6\left[y_{fc}+y_{oc}\right]+e_7\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]+e_8\left[y_{rb}\right]=0 \quad (7)$$

$$e_7\left[y_{fb}\right]+e_8\left[y_{ob}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]-e_9\left[\frac{1}{Z_2}\right]=0 \quad (8)$$

$$e_8\left[\frac{1}{Z_2}\right]-e_9\left[\frac{1}{Z_2}+\frac{1}{R_c}+\frac{1}{R_b}+y_{ic}\right]+e_{10}\left[y_{ic}+y_{rc}\right]-e_{11}\left[y_{rc}\right]=0 \quad (9)$$

$$e_9\left[y_{ic}+y_{fc}\right]-e_{10}\left[y_{ic}+y_{rc}+y_{fc}+y_{oc}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]+e_{11}\left[y_{rc}+y_{oc}\right]=0 \quad (10)$$

$$e_9\left[y_{fc}\right]-e_{10}\left[y_{fc}+y_{oc}\right]+e_{11}\left[y_{oc}+y_{ib}+\frac{1}{R_e}\right]+e_{12}\left[y_{rb}\right]=0 \quad (11)$$

$$e_{11}\left[y_{fb}\right]+e_{12}\left[y_{ob}+\frac{1}{Z_1}+\frac{1}{Z_2}\right]-e_{13}\left[\frac{1}{Z_2}\right]=0 \quad (12)$$

$$e_{12}\left[\frac{1}{Z_2}\right]-e_{13}\left[\frac{1}{Z_2}+\frac{1}{R_c}+\frac{1}{R_L}\right]=0 \quad (13)$$

Fig. 7b — Thirteen nodal equations for circuit of Fig. 7a.

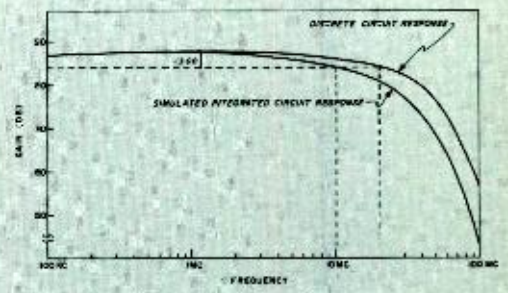


Fig. 8 — Computer-calculated frequency responses.

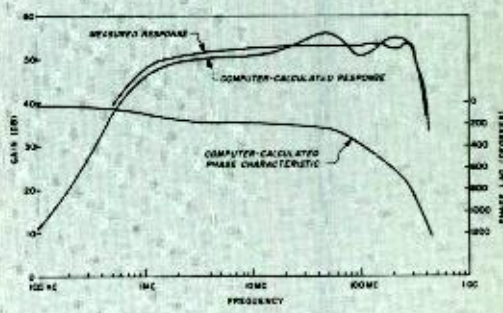


Fig. 10 — Amplifier frequency response.

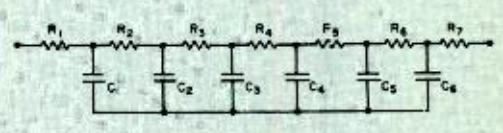
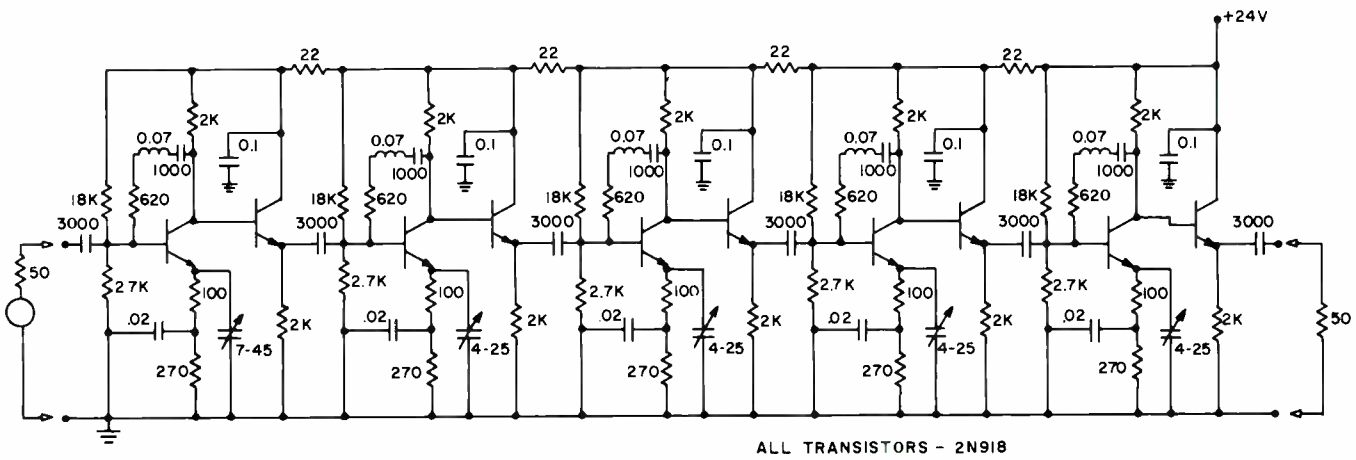


Fig. 11 — Integrated resistor equivalent cricuit.

determining the number of voltages to be solved in a discrete circuit is to take the total number of separate circuit nodes at the transistor terminals, exclusive of the transistor terminals tied to ground, plus one for the output node if that is a separate terminal.

Although the computer analysis described here is relatively simple, the idea of using a computer as a ready made design tool may be fairly new to some engineers. It is felt by the authors that this simple example significantly demonstrates the value of this technique in helping integrate circuit designers to achieve the best possible circuit before attempting the costly and timely manufacture thereof.

Fig. 9 — Broadband amplifier schematic.



INTEGRATION OF THIN-FILM PASSIVE COMPONENTS WITH MONOLITHIC SILICON INTEGRATED CIRCUITS

The integration of thin-film passive components with monolithic silicon active devices represents a logical step in the continuing improvement of integrated circuits. This important advance, coupled with RCA's broad experience in diffusion techniques, promises to make the integrated circuit a more profitable item to produce as well as a more efficient and reliable circuit element. This paper describes some of the recent developments combining diffused and thin-film techniques, and discusses their significance in terms of the capability, reliability, and manufacture of integrated circuits.

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In simplest terms, the combination of diffusion and thin-film techniques in the production of integrated circuits involves the evaporation of film resistors and capacitors on the top surface of a silicon dioxide insulating layer, and the connection of these elements by means of metallized conductors to planar semiconductor devices which lie below the oxide surface. This integration of thin-film and diffusion techniques offers several advantages, including improved electrical performance and smaller pellet size.

The improvement in electrical performance is partially explained by the fact that the characteristics of a thin-film passive component are better than those of its diffused counterpart. Temperature coefficients, for example, are at least an order of magnitude smaller. The absolute value of the components can be more easily controlled, generally to within ±5% for thin-film resistors and ±10% for thin-film capacitors. As a result, circuits requiring precise values of resistors and capacitors can be more easily fabricated, and, in addition, variations of power dissipation from circuit to circuit can be minimized. Performance is also improved because thin-film components do not possess the detrimental characteristics inherent in diffused passive components, such as parasitic capacitances, leakage currents, and distributed capacitances which vary with bias.

In addition to improved performance, the pellet area required per circuit is reduced. The physical space required for resistors is greatly decreased because higher values of sheet resistance can be obtained (1,000 ohms/square for thin-film resistors, as opposed to 175 ohms/square for resistors diffused with typical base concentrations). Similarly, the physical dimensions of capacitors are decreased because materials having higher dielectric constants can be employed (25 to 50 for thin-film capacitors as opposed to 3.8 for silicon dioxide dielectric capacitors). Therefore, a larger number of circuits can be fabricated on a given semiconductor wafer with lower unit cost. In addition, the reduction of physical dimensions of the circuit minimizes the effect of distortions inherent in the photolithographic and mask-making processes.

Other advantages also result from the use of thin films. Circuits which require very high resistance or capacitance values, and which are difficult if not impossible to fabricate in monolithic form, can easily be produced with thin-film techniques. Furthermore, feedback between the various stages in a circuit can be reduced.

Up to and including the metallizing step, the processing of integrated circuits using thin-film components is similar to that used for conventional monolithic silicon integrated circuits, as described by Saunders in another paper.[1] This paper describes the additional steps required in the processing of integrated circuits when thin-film techniques are used.

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Fig. 1—Section of wafer showing photoresist mask.

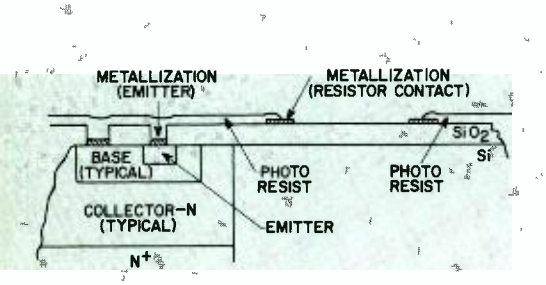


Fig. 2—Special fixture to hold targets in evaporator; four disks are silicon wafers; cylindrical device is film thickness monitor.

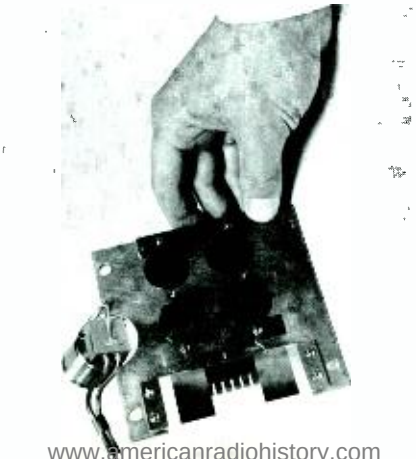
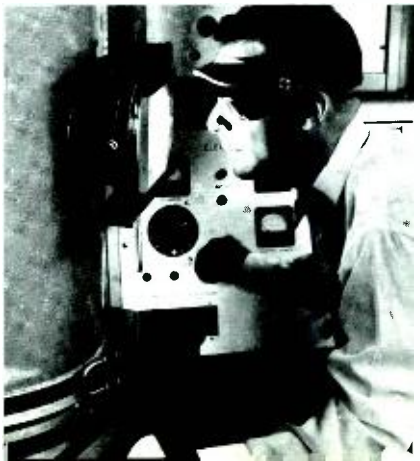


Fig. 3—F. P. Chiovarou operating electron-beam evaporator used in production of thin-film capacitors.



THIN-FILM RESISTORS

In general, the thin-film resistors used with monolithic integrated circuits are similar to those developed for evaporation on glass chips in the earlier digital microcircuit program.[2] However, the substrate material has been changed. In integrated circuits, silicon dioxide which has been thermally grown on a single-crystal silicon wafer is used instead of flame-polished borosilicate glass. The pad metallization in integrated circuits is aluminum instead of gold, and a new alloy for evaporating resistors has been developed.

One of the characteristics of the bulk properties of all metals is a positive temperature coefficient of resistance. In thin enough layers, however, nearly all metals exhibit a negative temperature coefficient. In other words, at some thickness the temperature coefficient of most metals changes from negative to positive and, therefore, exhibits a "zero" temperature coefficient. This thickness differs for each metal.

By careful selection of a metal or combination of metals, near-zero temperature coefficients can be obtained for any

desired value of sheet resistance. For example, the nichrome alloy used in earlier thin-film resistor fabrications (80% Ni, 20% Cr) has a temperature coefficient of less than 100 parts/million/°C in the range from 100 to 200 ohms/square. An improved alloy has recently been developed at Somerville to provide similar temperature coefficients at sheet resistivities an order of magnitude higher. Over the temperature range from −55 to 125°C, the temperature coefficient is better than 100 parts/million/°C. Stability tests at 125°C, with operating loads of 200 watts/in^2, show less than 1 % change in 1,000 hours.

The technique for fabricating thin-film resistors is essentially the same as that described previously.[2] After the active semiconductor devices of the integrated circuit are completed, contact holes are etched in the silicon dioxide insulating layer and aluminum metallizing material is evaporated over the entire surface. Photoresist is applied and exposed, and the aluminum is etched out to leave metal areas which form contacts, bonding pads, conductors, and resistor pads. Photosensitive material is then applied to the surface, aligned with a mask which registers the resistor areas, and exposed and developed (Fig. 1).

For deposition of the resistive film, the integrated-circuit wafer is placed in a special fixture, shown in Fig. 2, which is constructed to insure uniform heating of the substrates. Included in this fixture are two monitors which allow control of thickness for both the resistor and a silicon monoxide film which is evaporated on top of the resistive film. This SiO insulating film serves to stabilize the resistor.

After this double evaporation, the resistor and its "overcoat" adhere tightly to the silicon oxide surface but can easily be removed from the wafer in areas where deposition on the photoresist film has taken place. This technique is the reverse of the conventional etching process, in that the photoresist material is used to create geometric patterns by preventing films from reaching and adhering to the wafer surface.

THIN-FILM CAPACITORS

If thin-film capacitors are required in the same circuit with thin-film resistors, the capacitors are usually prepared in two additional steps. In the first step, a dielectric material is deposited on selected open metallized areas which serve as the bottom electrode; in the second step, an additional metallization deposits the top electrode of the capacitor. As in the case of the resistors, monitors are used to control the film thickness; after each evaporation, photoresist is applied and used as a mask during the etching of the required patterns.

The type of dielectric material used for a capacitor is determined by many requirements, including capacitor size, breakdown voltage, and dissipation factor. Depending upon the material selected, the evaporation may be performed by either conventional source heating techniques or, if higher melting point refractory materials are used, by an electron-beam heating source (Fig. 3).

Even though the voltages used in integrated circuits are generally low, the dielectric strength of an insulator is an important criterion because materials which can withstand high electric fields can be used in thinner films to provide increased capacitance per unit area. Perhaps the most important determining factor is dielectric constant, followed by temperature coefficient, Q, and frequency response. Suitable materials generally fall into two classes: those having low dielectric constant (below 20) and those having high dielectric constant (between 100 and 1,000).

As in the case of resistive materials, the characteristics of dielectrics in bulk differ from the characteristics of their thin-film counterparts. The method of evaporation (including background pressure, rate of evaporation, and temperature of substrate) contributes greatly to the structure of the film and hence to its electrical properties. The Materials and Processes Laboratory at Somerville has contributed extensively to this study and evaluation.

Some of the materials which have been used in the fabrication of capacitors include silicon monoxide, magnesium fluoride, barium titanate, and lanthanum titanate. The first two are conventionally evaporated, while the latter two require electron-beam heating. Aside from the actual evaporation technique, the processes are identical. Further work in the materials area, as well as additional effort in deposition technique, is continuing.

When both thin-film resistors and capacitors are required on the same circuit, the capacitors are formed first, and then the resistors. In this sequence, the bottom capacitor electrode is set up first (at the device metallization stage), then the capacitor dielectric is evaporated, and then the top electrode metallization which forms the interconnections and the resistor pads takes place. Finally, the resistor film and SiO insulating film are evaporated to complete the device. A total of four additional steps (two photoresist and two evaporation) are required to add thin-film resistors and capacitors to conventional monolithic silicon integrated circuits.

RESULTS

The results of these new fabrication techniques can be shown by some recent examples. An amplifier fabricated with diffused resistors required two chips, each larger than 0.050 by 0.053 inch. The same circuit fabricated with thin-film resistors was made on a single chip 0.049 by 0.065 inch. Similarly, when two IF amplifiers were fabricated with the same space allotted for the capacitor, the circuit using a silicon dioxide capacitor had a capacitance of 15 pf, while the circuit using a thin-film capacitor had, in the same area and with the same breakdown voltage, a capacitance of 45 pf. This thin-film unit used a SiO dielectric; greater capacitance values are anticipated from higher-dielectric materials still in development.

Electrical analysis of circuits fabricated with thin-film components has confirmed the predicted improvement of performance characteristics discussed earlier. These thin-film components offer the advantages of higher frequency response, faster switching speeds, and lower and more uniform power dissipation, all in addition to the benefits of reduced size and more pellets available per wafer.

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ALBERT H. MEDWIN received the BSEE degree from the College of the City of New York in 1949. After several years designing oscilloscopes, signal generators, and vacuum-tube voltmeters, he joined the Monroe Division of Litton Industries, where he worked on the design and construction of special-purpose digital computers. In 1959 he joined RCA in the Micromodule Activity at Somerville. His assignments included the design of the Microrac computer modules and the development of new packaging and interconnection techniques for the Project Lightning tunnel-diode computer. In 1961, he transferred to Somerville's Computer Department, where he developed the DMC (Digital Micro Circuit) approach to integration. As a group leader in Integrated Circuit Design, he is currently responsible for the development of advanced isolation, component fabrication, and interconnection techniques for MOS and bipolar integrated circuits. He holds several patents, and is a member of Eta Kappa Nu, IEEE, and the American Vacuum Society.

LAYOUT OF MONOLITHIC SILICON INTEGRATED CIRCUITS

The layout of a silicon planar monolithic integrated circuit is essentially a solid-state schematic of the corresponding discrete-component circuit. This solid-state schematic, which is drawn out on a single silicon pellet, generally employs one or more transistors, diodes, resistors, and capacitors. Prior to determining the topography of the circuit, the designer must design and lay out each individual component required for the specific application so that it will function at the desired voltage, current, gain, frequency response, and ambient temperature. The respective components are then physically located on the silicon surface in such a fashion that they can be interconnected as required, and suitable photolithographic masks are prepared. The prime objective of the layout and mask design is to reduce material and labor costs by minimizing the pellet area used for each circuit.

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THE first consideration in the layout of a monolithic silicon integrated circuit is to determine the number of isolation regions required. Separate isolation regions are needed for each monolithic transistor (and diode) which uses a different collector-voltage level, for all the resistors, and usually for each capacitor.

As shown in Fig. 1, the isolation diffusion process forms back-to-back *p-n* diodes which are reverse-biased in the integrated circuit to electrically isolate the different *n* regions. The diode formed during the isolation of a monolithic transistor has a parasitic depletion-layer capacitance which is in parallel with the collector-to-base junction and which has a deleterious effect on the frequency response of the circuit. This capacitance can be reduced by minimizing that part of the isolation area of the transistor which is parallel to the wafer surface or curving to the surface, and by connecting the *p* substrate to the most negative voltage supply in the circuit. The latter step increases the depletion-layer width to a maximum and, all other factors being equal, results in the smallest isolation capacitance.

In the case of a diffused resistor, a parasitic *p-n* diode is formed between the resistor *p* region and its *n* isolated region, as shown in Fig. 2. The resistor and its parasitic distributed capacitance then act as an RC filter, with the associated frequency limitations. A technique similar to that described for transistors is used to minimize this capacitance. When the minimum practical area has been selected for the resistors, based on tolerance requirements, provision is made for applying the most positive supply voltage to the *n* isolated region to widen the depletion region of the diode. This method also insures that the resistor *p* and isolated *n* regions are reverse-biased for all circuit conditions; for this reason, it is generally good practice to locate all resistors in one isolated region (exceptions to this practice are not uncommon, however, for certain circuits).

The *n* region of a silicon dioxide capacitor is also connected to the positive-voltage side of the circuit to minimize the parasitic shunt capacitance of the capacitor-substrate junction.

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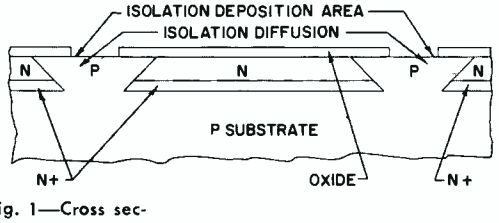


Fig. 1—Cross section of isolation diffusion process.

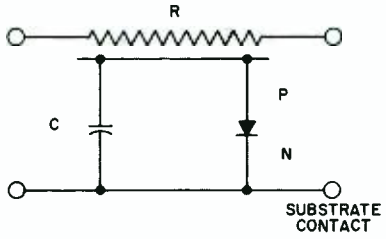


Fig. 2—Equivalent circuit of a diffused resistor.

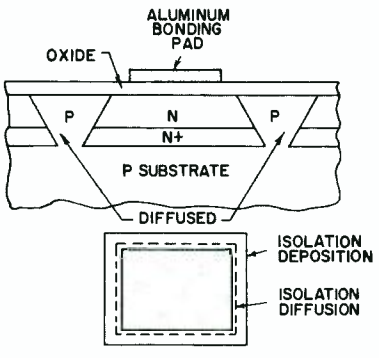
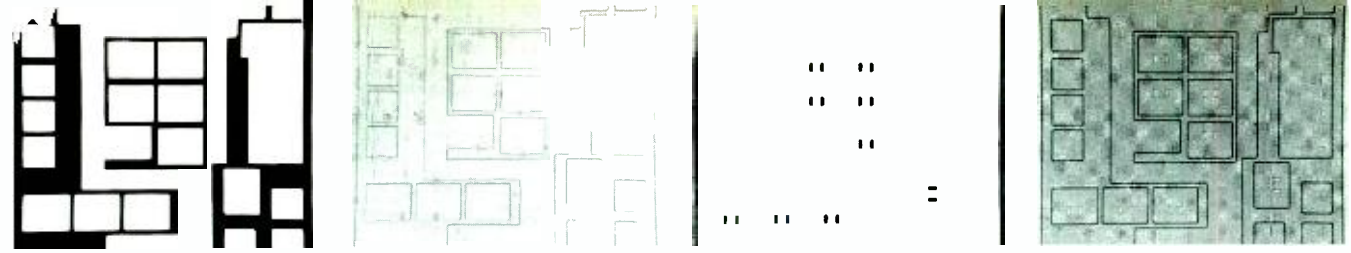


Fig. 3—Location of metal bonding pad.

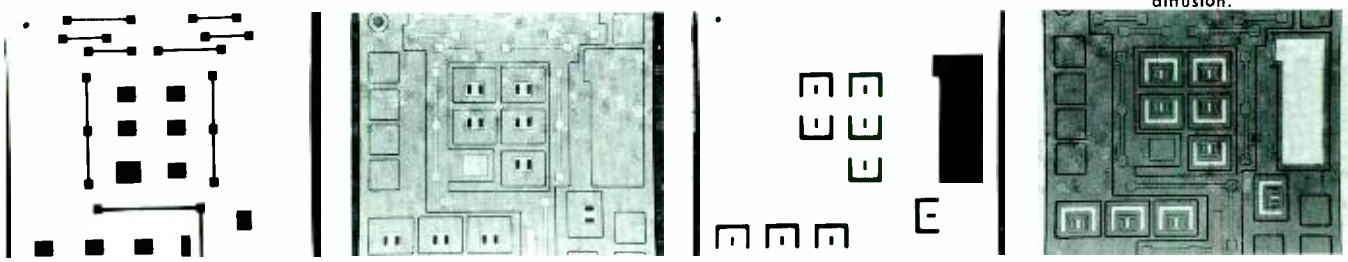
MASK LAYOUT

The design of the individual components for an integrated circuit establishes many dimensional and processing factors, such as the isolation diffusion allowance for each component, the exact nature and position of the transistor electrodes, the diffused-resistor and oxide-capacitor geometries, the diode configuration, the contact areas of each component, and a number of other clearances and allowances. The objective of the mask layout phase is to combine all these factors into the minimum practical pellet area, allowing enough room for all of the isolation regions, aluminum interconnecting stripes between components, and bonding pads around the periphery of the pellet. The design should avoid the use of metallization crossovers, such as additional bonding between metal breaks, or low-resistance diffusion crossovers because such crossovers involve additional labor and material costs and result in some sacrifice of reliability. It is sometimes an advantage

HAIG GOSHGARIAN received the B.S.E.E. from Pratt Institute in 1951 and the M.S. in E.E. from Newark College of Engineering in 1958. During 1951-52, he did guidance systems design work for Fairchild Guided Missiles Division and Arma Corporation. From 1952-54, he was employed at the Signal Corps Engineering Lab., Ft. Monmouth, N. J. He joined RCA's Electron Tube Division in 1954 as a transistor design engineer. In 1956 he transferred to Production Engineering. During 1957-58, he was instrumental in establishing operations in the RCA Semiconductor and Materials Division, Somerville plant. He became an Engineering Leader in production engineering in 1959 and in 1962 became Manager, High-Speed Products. He transferred to the Integrated Circuit Department late in 1963 as a Senior Engineer and has been actively engaged in the design of analog monolithic silicon integrated circuits.



(a) Isolation mask. (b) Pellet after isolation. (c) Base p+ mask. (d) Pellet after base p+ contact diffusion.



(e) Base and resistor mask. (f) Pellet after base diffusion. (g) n+ mask. (h) Pellet after n+ diffusion.

Fig. 4—Typical photolithographic masks and resulting topography of silicon pellet; see (a) through (h) above.

to insert additional resistors and a transistor on the pellet which will not be functional in the circuit; these components can be probed at various stages of fabrication to gather information on process variables and establish control.

In some cases, several integrated circuits may be required which use similar combinations of components. The pellet layout for such circuits can often be designed to include all the components in such a fashion that any one of the several circuit configurations can be selected by use of an appropriate metallization. This approach has some merit in that several circuits may be available from one basic design, with resultant savings in engineering and inventory costs. However, care must be used to assure that this advantage is not outweighed by the resultant engineering compromises that may be required, the greater complexity, and the increased pellet size.

There are, of course, any number of ways of physically laying out the masks. One method is to make scaled (200:1 or larger) top-view drawings of the individual monolithic components, showing all oxide etch lines (isolation, $p+$ base, and resistor, $n+$ and contacts). These individual scaled component models are affixed to a large quadrille (10 × 10 to the inch) sheet in a physical layout corresponding to their locations in the circuit schematic (for lack of a better starting point). A transparent sheet (preferably mylar or similar dimensionally stable material) is then placed over the component layout, and an interconnect pattern is drawn to completion. The object of this initial step is to determine what potential layout problems exist for the given circuit in terms of crossovers and pellet size. The designer can then attack these problems by rearranging the components as necessary until a satisfactory layout is achieved.

Because the layout of the mask is governed principally by the metal interconnection configuration, the problem reduces to a topographical one. The fewer components in a circuit, of course, the simpler the layout phase becomes and the larger the number of satisfactory configurations that can be obtained. In complex circuits, several trials may be required to ferret out the one or two possible layouts. During these trials, minor design changes may be made to obtain a more acceptable layout. For example, some of the circuit resistors may be lengthened for crossover purposes. Occasionally, low-resistance diffusion crossovers must be added to the circuit; however, care must be taken not to add such crossovers in series with supply voltages lest they cause voltage-level shifts in the circuit.

When an acceptable configuration has been determined, the layout is then refined to its final form. The isolation deposition area should be no narrower than one mil in any area. Metallization stripes should be 1 to 1.5 mils wide in connections between components to assure continuity, and spacing between stripes should be no less than one mil. (For very short connections of 3 to 4 mils, it is sometimes permissible to reduce metal width and spacing to 0.5 mil.)

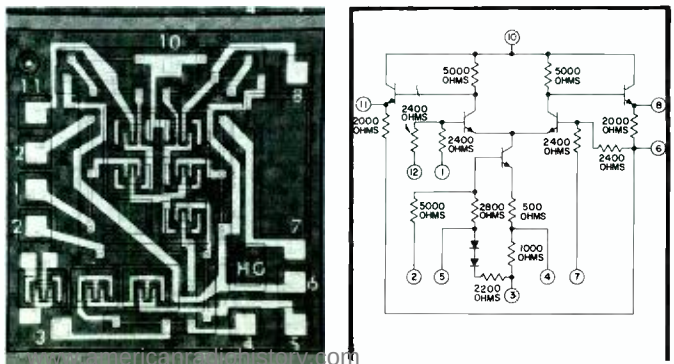
Metal bonding pads (3 × 3 mils minimum) are provided at the periphery of the pellet to provide a large target area for ease of bonding. The bonding pads are located over isolated areas, as shown in Fig. 3, to guard against circuit shorts. If the bonding results in oxide breakage, the connections are still isolated from the substrate, and the circuit can still function.

After the designer completes his final layout, separate detailed drawings are prepared for each mask (i.e., isolation, $p+$ base, base and resistor, $n+$, contacts and metallization). Typical masks are shown in Fig. 4, together with the topography of a pellet as it proceeds through the various processes up to, but not including, contacts and metallization. In the mask fabrication procedure, it is essential to check and overlay masters in detail to assure that all masks align and to make necessary corrections.

The wafer shown in Fig. 4 can be used for many circuit configurations by use of different sets of contact and metallization masks. Fig. 5 shows an audio-amplifier circuit, Dev. No. TA-5034; certain components on the pellet are not used in this particular circuit. The same wafer (with different contacts and interconnections) is used for an IF amplifier, Dev. No. TA-5035 and for an RF amplifier, Dev. No. TA-5037 (Fig. 6).

Fig. 5—Layout for audio-amplifier integrated circuit (Dev. No. TA-5034) (a), and corresponding schematic diagram, (b). This differential amplifier provides phase inversion and low-impedance drive for class B output stages. It is DC coupled to output stages; feedback connections are provided; a constant-current transistor bias network provides temperature compensation.

Fig. 6—Differential RF amplifier (Dev. No. TA-5037) to be used with tuned circuits for applications through 100 Mc. A constant-parent feed to the emitter-coupled pair is designed for DC stability and can be used for AGC and mixing.



FABRICATION PROCESSES FOR MONOLITHIC SILICON INTEGRATED CIRCUITS

The manufacture of monolithic silicon integrated circuits involves numerous processes which depend upon each other and which must be precisely controlled: 1) slice preparation, 2) epitaxial growth, 3) diffusion and oxidation, 4) photoengraving, 5) evaporation, and 6) pellet processing (including mounting, wiring, and encapsulation). This paper discusses these processes as they are related to monolithic silicon circuits in which all components with the exception of interconnections are formed in the silicon itself..

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A block diagram of the major processing steps for monolithic silicon integrated circuits is shown in Fig. 1. This diagram does not include the many handling, cleaning, and miscellaneous process steps which, for yield considerations, are just as important as those shown.

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Processing of integrated circuits is normally performed from only one side of the wafer. Although this approach introduces minor problems such as increased collector series resistance, these problems can be by-passed or alleviated by special techniques. Fig. 2 shows a cross-section of a typical integrated-circuit pellet. Although this figure does not show all possible component structures, it illustrates the general cross-section topology upon which components can be built.

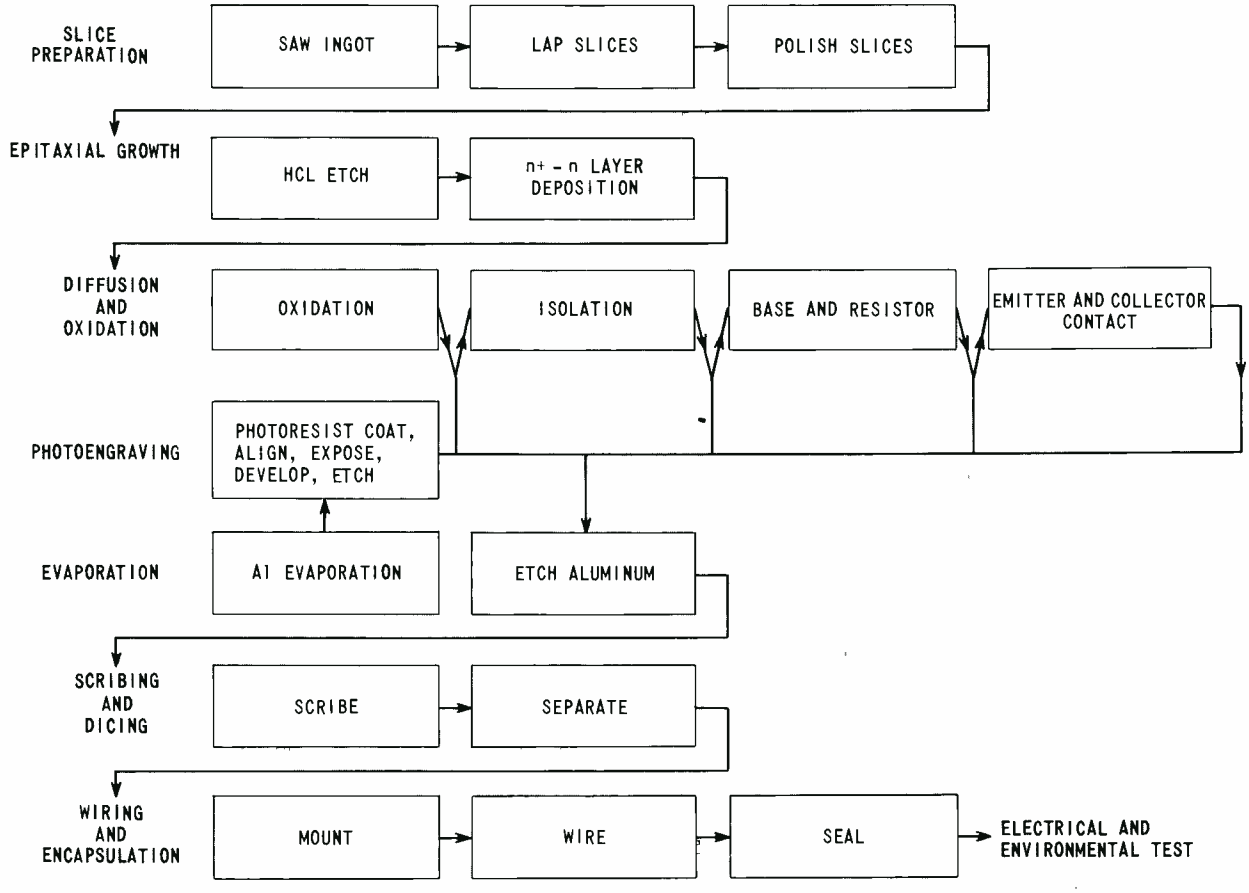
SLICE PREPARATION AND EPITAXIAL GROWTH

Epitaxial growth[1,2] of silicon has become a standard operation in the production of integrated circuits because it provides low collector resistance, low collector-to-base capacitance, and high collector-to-base breakdown. In addition, it facilitates isolation operations. The chemistry of the process involves the reduction of $SiCl_4$ by hydrogen over a hot silicon substrate, as shown by the following reaction:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl$$

The reversibility of this reaction is used in the cleaning of the silicon slices prior to epitaxial deposition. This cleaning, which occurs in the reactor, removes controlled amounts of silicon from the slice surface and helps to maintain high-quality epitaxial material.

Fig. 1 — Major processing steps for integrated-circuit fabrication.



The epitaxial material used for integrated circuits generally consists of an $n+$ layer (heavily doped) on a p substate, followed by an n layer (lightly doped) over the $n+$ layer. Because the $n+$-p diode is later used in the isolation of components, it must have low leakage and a breakdown voltage high enough for the circuit requirements. The HCl precleaning step helps to obtain low-leakage junctions of epitaxial layers and substrates.

The best temperature range for epitaxial growth of silicon is 1,150 to 1,250°C. Although lower-temperature growth can be obtained by means of special techniques, epitaxial growth at temperatures too far below the preferred range generally results in polycrystalline growth or numerous defects such as stacking faults and nonuniformity in thickness and doping level.

The epitaxial reaction is carried out in a quartz tube of a size dependent upon the size of the power supply. The RF inductive heating of a susceptor upon which the slices are placed is the preferred method of heating. This method allows the chamber walls to remain at a low enough temperature so that silicon is deposited only on the susceptor and the silicon slices.

Silicon tetrachloride is generally used as a silicon source because of its purity and ease of handling (other sources such as $SiHCl_3$ and SiI_4 have also been used). Doping can be accomplished by use of liquid sources or by metering of doped gases. With either of these methods, good control can be obtained and alternate layers of p and n or $n+$-n can be grown within certain doping-level restrictions.

After the epitaxial growth process, the material, as mentioned previously, generally has n and $n+$ layers on a p substrate. To a large extent, the n layer into which the base of the transistors is diffused determines the breakdown voltage of the collector-to-base junction. The $n+$ region determines the amount of collector series resistance. Because some outdiffusion of the $n+$ region takes place during the epitaxial growth and also during the subsequent diffusion operations, the dopant used for the $n+$ region should be a donor having a low diffusion coefficient. In addition, if the n and $n+$ regions are to be isolated by p diffusion, the substrate resistivity must not be too high or the original junction will move down into the substrate too fast for the isolation diffusion to reach it in a reasonable time.

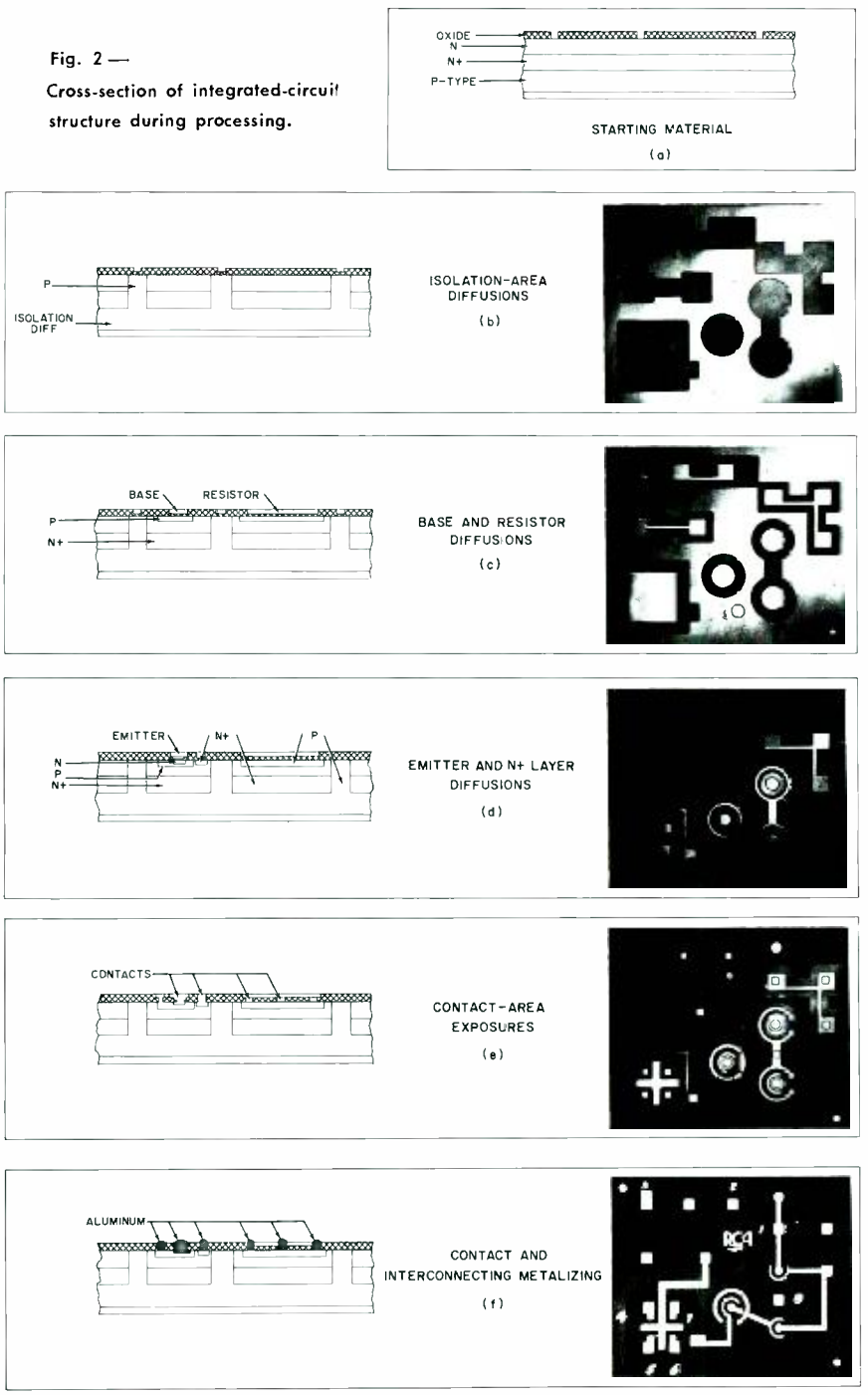
DIFFUSION AND OXIDATION

Although the diffusions discussed in this paper are related to epitaxial material, integrated-circuit diffusion is in no way restricted to this material for isolation techniques or for device fabrication. For most applications, however, the use of epitaxial material into which the isolation regions and subsequent diffused areas can be formed results in inherently superior devices than those produced by methods which use triple diffusion or *box isolation diffusion*. (In this technique, isolation regions are obtained by diffusing from both sides of the slice).

The actual mechanics of diffusion can be carried out in many ways. The general basic process used in semiconductor technology is a batch-type operation which uses quartz tubes, resistance furnaces, and quartz fixtures. Fig. 3 shows a bank of furnaces used for integrated-circuit diffusion. For epitaxial planar transistors, it is desirable that oxidation take place in the same tube and, in most cases, at the same time as the diffusion. For epitaxial planar integrated circuits using n-p-n transistors, the diffusions take place in the following sequence: 1) wall isolation (p-type), 2) base diffusion (p-type), 3) emitter diffusion (n-type).

Prior to the p-type wall-isolation diffusion, an initial oxidation is performed to place 7,000 to 10,000 angstroms of SiO_2 on the surface. This step is performed in a steam or wet-oxygen atmosphere and actually becomes a diffusion-rate-limited reaction after the first several thousand angstroms of SiO_2 are grown. The SiO_2 layer acts as a selective barrier to the diffusion of the impurities so that localized areas can be

Fig. 2 — Cross-section of integrated-circuit structure during processing.



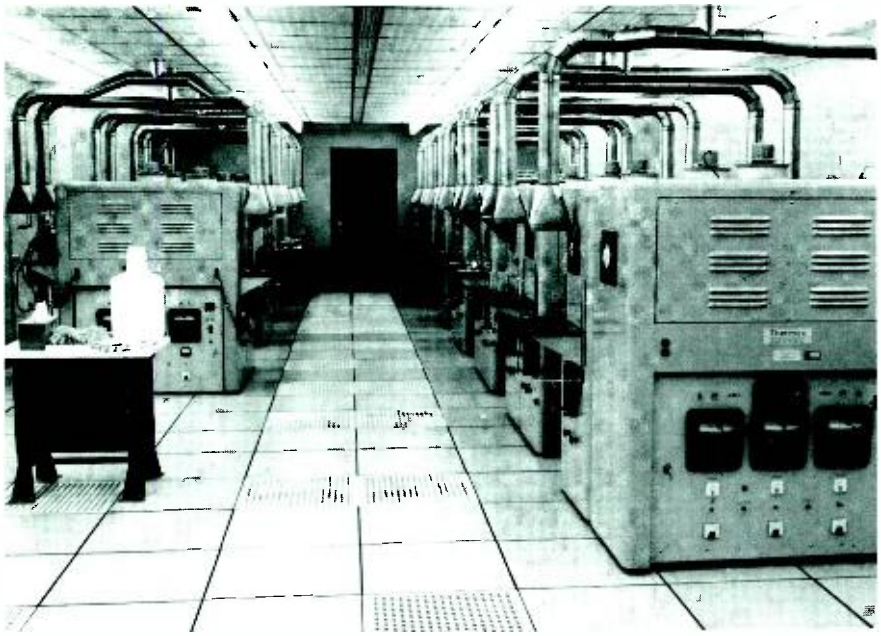


Fig. 3 — Diffusian furnaces far integrated circuits.

doped with *p*- or *n*-type impurities. These localized areas form the resistors, transistors, diodes, and capacitors for the circuit. The sheet resistivities ρ_s, junction depth x_j, and impurity dopants shown in Table I are typical for integrated-circuit components when *n-p-n* transistors are called for in the circuit.

The control possible on the values shown in Table I is approximately ±10% (for higher resistivities, it may be closer to ±20%). In as many cases as possible, more than one component is prepared with one diffusion even though the resistivities obtained are not optimum for one or both of the components. This compromise is used to reduce the number of operations and to improve over-all control. Control of the sheet resistivity and junction depth obtained in an early diffusion becomes a much more difficult task if two or three more diffusions within the same temperature range are subsequently performed.

A diffusion technique commonly called open-tube diffusion is used. This method uses a flow of gas through an unsealed tube either to carry the doping material or for oxidation purposes. Three different types of impurity sources can be used: solids such as B_2O_3 or P_2O_5, liquids such as BBr_3 or $POCl_3$, and gases such as B_2H_6 or PH_3. The advantage of liquid sources is that the partial pressure of the liquid can be varied to provide changes in doping concentration. The advantage of gaseous sources is that the total dopant mole ratio in the carrier gas can be varied. It is usually mandatory either that an oxidizing atmosphere flow through the furnace during the diffusion or that a thin oxide layer be present on the silicon wafers to prevent surface pitting.

The diffusion is generally carried out in a two-step operation when sources such as BBr_3 and $POCl_3$ are used. In the first step, a deposit is made on the surface of the slice and a highly doped thin surface layer is obtained. This operation is followed by a "drive-in" step in which the junction depth and sheet resistivity are controlled to some extent by the quantity of surface oxidation allowed. For purposes of calculation, this drive-in step is generally considered to produce a Gaussian distribution; however, outdiffusion and surface depletion of the dopant may reduce the surface concentration below that which is expected. This effect can lead to surface inversion of *p*-type material, along with other changes in device characteristics.

PHOTOCHEMISTRY

The process of photoengraving for integrated circuits consists of exposing to ultraviolet radiation a light-sensitive chemical which is spread in a thin layer over the oxidized surface of the silicon slice. The exposure is made through a mask prepared by photographic techniques.[5] After the photochemical is polymerized by the ultraviolet light, the nonpolymerized regions can be washed away, and the SiO_2 which is exposed can then be selectively etched out with hydrofluoric acid. The film left on the slice must be resistant to the acid etch so that sharp definition can be obtained without undercutting.

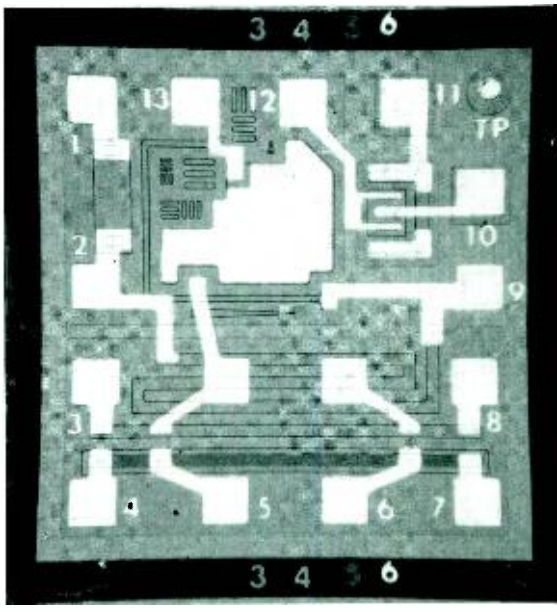
The resolution that can be obtained in the process depends upon the total size of the individual circuits to be exposed, the optics of the mask-making equipment, the photochemical used, and the processing of the exposed masks and coated wafers. The practical limits of this process for most circuits are presently in the range from 0.1 to 0.2 mils, with the bulk of the components using larger dimensions. As the limits of the process are approached, the reproducibility is affected and component values can vary to a large degree.

Pinhole etch resistance is much more important in the processing of integrated circuits than in transistor processing because of the larger percentage of critical area in which pinholing can cause device failures. In the manufacture of planar transistors, the main concern is pinholing at the junction interface; in the manufacture of integrated circuits, the junction interfaces, the major portion of the isolated regions, and the bulk of the area under the aluminization interconnects are critical.

An additional problem involved with integrated circuits is the requirement of etching through different thicknesses of oxide in some of the photoengraving steps, particularly the contact-opening step. Although this problem can be eliminated by stripping the oxide and regrowing, this step involves an added high-temperature process which should be avoided if possible.

Fig. 4 shows a test pattern which contains different components normally used in integrated-circuit design. This test pattern is designed primarily to test electrical parameters, but can also be

Fig. 4 — Test pattern far integrated-circuit resolution and electrical parameters.



used to determine the dependence of some electrical parameters on the photoresist integrity. Included in the pattern is a resolution-capability chart with which the photoengraving resolution can be measured down to 0.1-mil spacings. In addition, the test pattern can provide an approximation of oxide pinholes if they exceed a critical quantity.

EVAPORATION

In integrated-circuit processing, evaporated surface layers have been used to obtain surface diffusion sources, ohmic contacts, interconnects, passive components, and oxide isolation layers. The following discussion on evaporation is primarily concerned with the evaporation of metals for ohmic contacts and interconnects.

Aluminum has proved to be an excellent material for interconnecting monolithic silicon integrated circuits. Aluminum makes good ohmic contact to *p*-type material, as well as to heavily doped *n*-type material. Aluminum adheres well to both Si and SiO_2, and has high enough conductivity to act as an interconnector even in fairly thin layers.

The silicon wafer may be either hot or cold during the aluminum evaporation. Depending upon the temperature of the wafer at the time of evaporation, a further heat treatment may be required to ensure good ohmic contact between the evaporated metal and the silicon. Evaporation should be performed at vacuums in the range of 10^{-6} torr, although good aluminization has been obtained in poorer vacuums. Strict attention must be paid to slice cleanliness before evaporation, and all possible precautions should be taken to eliminate oil contamination when oil diffusion pumps are used in the evaporators.

One disadvantage of aluminum as a contact and interconnect material is that it is not completely compatible with the best wiring material, gold. Ultrasonic and thermocompression bonding of aluminum wiring are being developed to circumvent this problem.

WIRING AND ENCAPSULATION

After the integrated circuit slice is metallized for interconnects and contacts, it is diced into individual circuit pellets and mounted onto a package header. Two kinds of headers have been used, the TO type (generally TO-5 headers with 8 to 12 pins) and the flat package. Although each of these packages had advantages, the flat package allows for a higher packing density. Mounting is performed either in furnaces or in specially designed die-mounting machines. Gold-alloy preforms are used for furnace mounting, and may or may not be used for mounting with die-bonding machines. For mounting to ceramic, it is possible to use low-melting glasses for bonding when the substrate does not have to be directly grounded to a metallized pad.

After die mounting, the integrated-circuit interconnect pads are connected to the package leads, usually with either gold or aluminum wiring. More advanced techniques have been evaluated which eliminate such wiring by making use of a printed-circuit-board effect. With gold wiring, the most convenient method is a combination of the nail-head or ball-bonding technique and the wedge-bonding technique. This process makes use of a movable capillary through which the gold wire is threaded. After one wiring operation is completed, a small gas flame burns off the gold wire and forms a ball which can be thermally compression welded to an aluminum pad on the die. Any number of wedge-type welds can be completed before the wire is burned off again to form a new ball. This procedure is very convenient because gold welds easily to aluminum; however, the brittle compound $AuAl_2$ may form in circuits exposed to high-temperature storage or service. Because aluminum-to-aluminum thermocompression bonding is not as reliable as gold-to-aluminum bonding, ultrasonic bonding of aluminum wire has been developed. This technique has produced good bonds to interconnect pads, to gold-plated package posts, and to aluminized package posts.

Sealing of integrated circuits should be hermetic. Although the planar process yields relatively stable devices, some degradation can take place with time in unfavorable atmospheres. This condition is particularly true with aluminum interconnects, which can open up with time under conditions of extreme moisture.

SUMMARY

This paper demonstrates the complexity and interdependence of the processes required in the manufacture of monolithic silicon integrated circuits. From the initial step of slice preparation, through diffusion and oxidation, to the final processing of the finished pellet, the production of high-yield integrated circuits encompasses and combines the fields of optics, chemistry, metallurgy, physics, and electronics. These varying disciplines have been blended by RCA into an efficient and promising integrated-circuit capability.

M. S. SAUNDERS received the B.S. in Metallurgical Engineering from Lehigh U. in 1949, and the M.S. in Metallurgical Engineering from the University of Michigan in 1952. From 1949 to 1951 he worked for Curtiss Wright Corp. He joined Westinghouse Electric Corporation, Aviation Gas Turbine Division, in 1952, where he worked on turbine blade materials and special metallurgical applications and alloys; he was a supervisor in a group which set up one of the first commercial nuclear fuel plate fabrication facilities. In 1959, he transferred to the Semiconductor Division of Westinghouse and performed work on new materials and infrared sensing devices. He became supervisor of a group developing high-power controlled rectifiers and later supervised a group designing and developing integrated circuits. He came to RCA in 1964 as an Engineering Leader, and has been engaged in process evaluation and control in the manufacturing of silicon integrated circuits.

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TABLE I—Typical Sheet Resistivities (ρ_s) and Junction Depths (x_j) for Integrated-Circuit Components (with n-p-n Transistors).

Component	ρ_s (ohms/square)	x_j (microns)	Impurity
Isolation wall	3-10	7-50	boron
Bases and resistors	120-250	1.8-5	boron
Diodes, capacitors	20-250	1.8-4	boron
Emitters, capacitors, collector contacts	3-6	1-3	phosphorus
Floating collectors	100-500	4	arsenic or antimony

RELIABILITY PROGRAM FOR MONOLITHIC SILICON INTEGRATED CIRCUITS

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THE significant advances in the use of monolithic silicon integrated circuits during the past year have resulted from several contributing factors, not the least of which is their promise of very high reliability. Although much of this reliability is inherent in the materials and processes used in the fabrication of these circuits, an extensive testing program has been developed to determine and improve circuit reliability. This program includes automatic testing of every unit for static electrical characteristics; sample testing, both in-process and final, for special mechanical, electrical, and environmental features; and detailed analysis of test "rejects" to determine and eliminate failures.

STATIC ELECTRICAL TESTS

The automatic static test set (Fig. 1) incorporates many features which facilitate and expedite the testing of production quantities of integrated circuits. (This test set was designed and manufactured by Non-Linear Systems, Inc., Delmar, Calif., according to the specifications of the Integrated-Circuits Applications Laboratory.) It can measure the DC characteristics of complex digital and analog integrated circuits or integrated components with high speed (nine *go, no-go* indications per second) and accuracy (±0.01%), or can provide one recorded reading per second for engineering design evaluation. Because of its unique design, ease of operation, and flexibility, a variety of circuits and DC parameters can be tested.

Programming of the test set is accomplished by means of plug boards which can be easily removed and changed to accommodate the type of circuit being tested. In effect, the entire unit is self-checking; the accuracy of the digital voltmeter can be checked with a standard cell, and the power supplies can in turn be checked by means of the voltmeter. Trouble-shooting time and maintenance are greatly reduced by the use of plug-in cards.

The test specifications for each type of integrated circuit are written by the applications engineer and the device engineer after careful evaluation of the capability of the manufacturing process and permissible worst-case tolerances. This testing specification includes tolerances of the measurable components and voltage-output levels under different input conditions. A typical circuit such as the TA-5038 (see G. Cohen's paper in this issue) is tested under 19 different sets of conditions. These tests include checks for logic level, logic level with external load, input and output currents, and individual components such as resistors.

As shown in Fig. 2, an interconnecting mechanism connects the power supplies, the external resistors, and the digital voltmeter to the proper leads of the integrated circuit. As testing progresses, these connections are changed automatically according to the specifications for each test. The required circuit paths are selected by means of the program patch panel, which has two main units, the receiver and the plug panel. The plug panel, a perforated board containing small phone jacks and interconnecting buss wires, serves as a small memory unit which can store a maximum of 30 different test commands for each type of integrated circuit. The operator merely inserts a new plug board for each circuit to be tested.

The readings on the digital voltmeter are stored in binary-coded decimal form. As a result, the information can easily be converted to give print commands to an automatic data-processing punch-card machine. The data cards classify the test results to show whether the readings are within limits, on the low side, or on the high side. When the only indication required is whether the reading is within limits *(go)* or out of limits *(no-go)*, the comparator compares the voltmeter readings to preset high and low limits stored on the comparator limit patch panel; then, a green or red light shows results on the indicator panel.

IN-PROCESS TESTING

Because all components of monolithic silicon integrated circuits are produced on a single silicon chip, in-process checking is greatly simplified. Faults in any of the various components of the circuit can often be located by a single microscopic examination. Inspection stations are set up at all critical points in the processing cycle, including diffusion, photoetching, and dicing. A typical product failure detected during tests is shown in Fig. 3.

ENVIRONMENTAL TESTS

A rigid series of environmental tests has been designed to accelerate the effects of failure mechanisms in integrated circuits so that weaknesses in materials or processes can be located and eliminated. Table I describes this environmental testing program. A sample of 15 circuits is selected from each production lot; three are subjected to each of the first five sub-groups of tests.

Several additional tests are being undertaken to determine the capability of integrated circuits under extraordinary environments. Tests are scheduled at the Industrial Reactor Laboratories (at which RCA is a participating partner) to ascertain the radiation resistance of integrated circuits. Plans are also in process for a thermal vacuum test to determine the capability of silicon circuits in outer space.

LIFE TESTS

A major facility has been completed which permits the simultaneous life testing of 900 integrated circuits. One of the three environmental chambers is shown in Fig. 4; each one accommodates 300 circuits; one operated at a different temperature condition, one at

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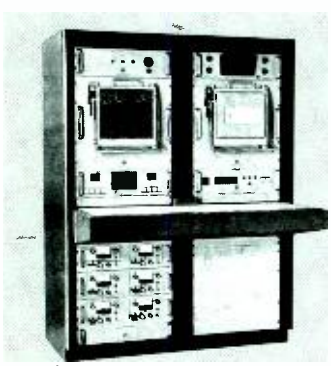


Fig. 1—Automatic static test set used for production testing of integrated circuits.

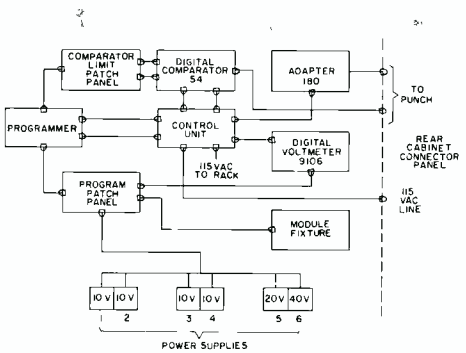


Fig. 2—Block diagram of automatic static test set.

Theodore S. Spitz

Joseph T. Molnar

THEODORE S. SPITZ received the B.S. degree and the M.S. degree in Electrical Engineering from the New York University in 1955 and 1956 respectively. He joined RCA in 1960 in the Microelectronics Department as a project engineer responsible for the design of automatic test equipment. In 1961 he was appointed Engineering Group Leader of the Micromodule Reliability and Test Engineering section; at present he is an application engineer in the Integrated Circuits Department and is responsible for reliability engineering. Mr. Spitz is a member of IEEE and of the Professional Group on Electronic Devices and Reliability and a member of Eta Kappa Nu and Tau Beta Pi.

JOSEPH T. MOLNAR received the Diploma of Electrical Engineering from the Politechnical University of Budapest in Hungary in 1956. He was employed at the Quality Control Company in Budapest where he was responsible for test engineering of communication equipment. He also worked in the electrical laboratory of the Technical University of Vienna and obtained an Austrian State Recognition of his Engineering Proficiency. In 1957 he came to the United States and worked for Ballantine Labs., Inc. where he was engaged in electronic instrumentation designs. In 1959, he joined the RCA Semiconductor and Materials Division and designed numerous engineering test sets for transistors and other semiconductors. At present, he is responsible for the development of efficient measuring methods and test sets for integrated circuits.

TABLE I—Environmental Testing Program

Test	Mil Spec	Method	Conditions	Special Conditions
Sub Group I				
Solderability	202	208	—	none
Temperature Cycling	202	107	B	Maximum high temperature +175°C (instead of 125°C)
Thermal Shock	705	1056	B	Temperature range +125°C to −65°C (instead of +100°C to 0°C)
Moisture Resistance	202	106	—	Omit the vibration tests and dryouts. Substitute lead fatigue test; one arc for each lead, with an 8.0 ±5 oz. weight applied.
Sub Group II				
Shock	750	2016	—	Acceleration 3,000 g's. Five blows in each of six planes
Vibration	750	2046	—	none
	750	2056	—	none
Constant Acceleration	750	2006	—	Acceleration 40,000 g's.
Sub Group III				
Terminal Strength	750	2036	A	2 lbs for 3 seconds.
			E	2 lbs for 3 leads.
			F	2 lbs for 3 seconds.
Sub Group IV				
Salt Atmosphere	750	1041	—	none
Sub Group V				
Storage Lifetest	750	1031	—	1,000 hours—standard production electrical tests.
Sub Group VI				
Operating Lifetest	750	1026	—	Test lot is divided into three groups, one tested at 125°C, one at −65°C, and one temperature-cycled between 125°C and 65°C on a 6-hour cycle.

125°C, one at −65°C, and one cycling between these two extremes. When tests have determined the environment which accelerates failure mechanisms by the greatest degree, all three chambers will be so converted.

All circuits are life-tested under conditions of power and full load. Test methods are designed to simulate actual electrical operation as nearly as possible. Present capacity for life-testing makes it possible to amass data at a rate of 650,000 circuit-hours per month.

STEP-STRESS TESTING

Step-stress tests are used for integrated circuits both to predict reliability levels at normal stresses and to uncover possible failure mechanisms. In such tests, a group of circuits is tested (generally to destruction) at a series of progressively increasing temperatures. Typically, the temperature is raised in 25°C steps, and the devices are kept at each temperature for 24 hours. After each such cycle, the devices are allowed to stabilize at room temperature, and electrical parameters are tested. Failures are analyzed to determine the failure mechanism. Testing continues until all circuits fail.

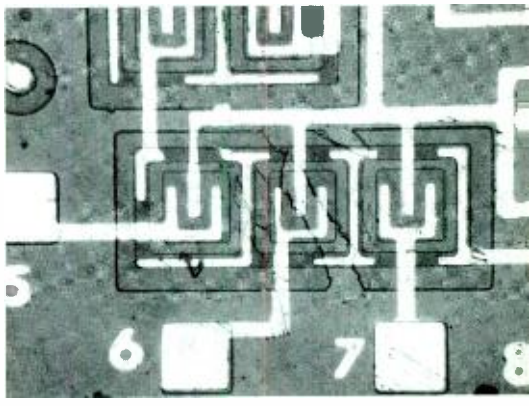
Much information about integrated circuits can be obtained from curves plotted to show failures as a function of applied stress (temperature). If there are no sharp discontinuities, the curve can be interpolated down to normal stress levels for an indication of normal-stress reliability. A sharp discontinuity indicates that a new failure mechanism is introduced.

FAILURE ANALYSIS

The most important factor in improving product reliability is an effective program of failure analysis to locate, analyze, and eliminate the causes of failure mechanisms. This type of analysis (which is performed on rejects from all tests) is a joint effort of many people and activities. The test reject is first returned to the Applications Engineer, who performs a thorough electrical analysis to pinpoint the exact component or connection which caused the failure. The circuit (with all recorded data) is then forwarded to the Device Design Engineer, who determines the exact mechanism in the semiconductor material, metallizing, or bond which caused the failure. Fig. 5 shows the microscopic probing mechanism which is used for this examination. After the cause of failure has been analyzed, corrective measures are determined and corresponding corrective action is incorporated in the production processes.

In addition to electronic and microscopic test equipment, both microphotography and X-ray photography are used extensively.

Fig. 3—A section of a photomicrograph showing a typical product failure detected through in-process testing.



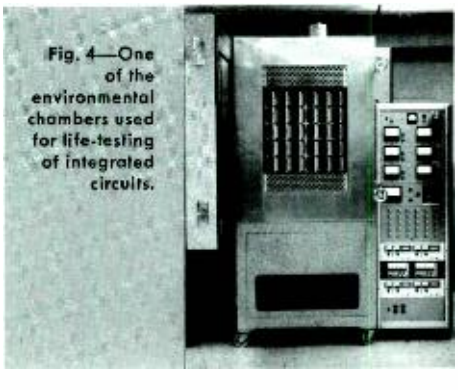


Fig. 4—One of the environmental chambers used for life-testing of integrated circuits.

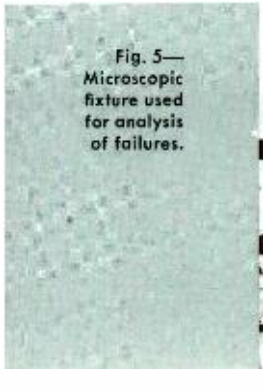


Fig. 5—Microscopic fixture used for analysis of failures.

PACKAGING OF MONOLITHIC SILICON INTEGRATED CIRCUITS

As in the case of conventional semiconductor devices, the package protects the final integrated circuit against mechanical damage and preserves desired ambient atmosphere. In addition, packaging provides electrical and physical isolation, corrosion resistance, and desired thermal conductivity and, to a large extent, determines mechanical interchangeability. This paper discusses a recent study of package design for monolithic silicon integrated circuits and describes the final configuration selected. The final package has an inherent reliability due to its design and construction unmatched by any other known package in the semiconductor field.

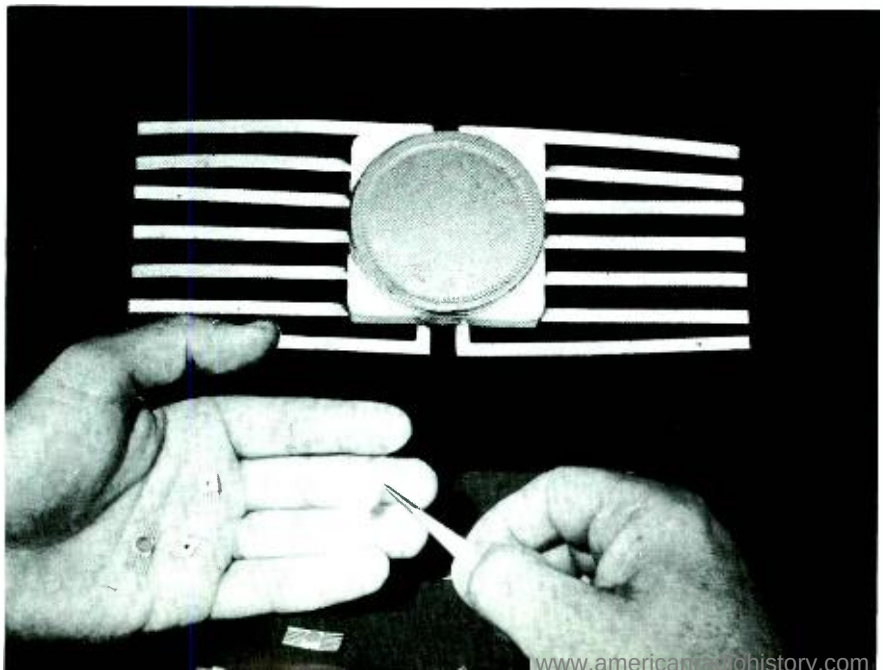
A. MORENA and H. KRAUTTER
Package Development
Special Electronic Components Division
Electronic Components and Devices, Somerville, New Jersey

At the outset of the study program, it was recognized that the package design for integrated circuits was required to meet a number of unique and demanding specifications. Some of the more important factors considered included: the size and shape of the package; electrical connection from the hermetic chamber to the external leads; materials meeting specified physical and electrical characteristics; type of seal (frit, solder, braze, or weld); thermal conductivity of the package; ease of manufacture in conjunction with present and future cost; versatility of design; and reliability of the package.

Market research and engineering evaluation indicated that no single available product possessed all the desired requirements. As a result, the Package Development activity began a program to design a suitable package. The ¼-by-¼-inch RCA package shown in Fig. 1 embodies as nearly as possible both the technical and economic requirements for an integrated-circuit package.

Final manuscript received August 21, 1964

Fig. 1—RCA's flat-package (inset) for integrated circuits; size is ¼-by-¼ inch.



SELECTION OF SUITABLE MATERIALS

The purpose of the first phase of the packaging program was to investigate suitable materials and techniques and to determine the feasibility and economics of producing hermetic enclosures. Materials such as plastic, glass, steatite, forsterite, and alumina were investigated. (Although the term *alumina* refers to 100% aluminum oxide, this paper uses this term to represent any ceramic possessing at least 90% alumina by weight.)

Plastics were quickly ruled out because of many serious technical deficiencies. Glass was not considered because of several reasons. First, a welded seal was desired for the package and glass, as a material, does not lend itself to this type of sealing treatment. In addition, glass when compared to many ceramics does not have the physical strength nor the thermal conductivity properties required. Accordingly, a detailed study of steatite, forsterite, and alumina was begun to determine the most suitable material.

The investigation revealed that forsterite and steatite possessed similar properties except at high frequencies, where forsterite was electrically superior. On the other hand, alumina was clearly superior in thermal conductivity and physical strength, and possessed significantly superior electrical characteristics even at elevated temperatures. In addition, aluminas also have excellent abrasive and thermal shock resistance. The over-all superiority of alumina coupled with recent advances in metallizing techniques make alumina ceramics the most logical choice.

The next phase of the investigation was to evaluate various metallizing pastes. The resultant investigation revealed that a paste primarily of molybdenum produced the most favorable over-all results.

The metals considered for use as leads, flanges, and caps were nickel, copper, and kovar (an alloy of iron containing 54% iron, 28% nickel, and 18% copper.) Although nickel and copper offer better thermal conductivity properties than kovar, they also posses expansion coefficients which do not closely match alumina ceramics. Kovar provides a better expansion match and better lead flexing strengths after annealing (Fig. 2).

FABRICATION TECHNIQUES

The unique process developed by RCA for construction of the packages makes use of accurately controlled organic bonded sheets of ceramic powder. Because the ceramic sheets are thermoplastic, they may be heated to form a composite structure. The metallized ceramic assembly, after sintering, produces a hermetic monolithic structure.

The initial effort was devoted to the development of casting and heating cycles and finding suitable compositions for the alumina. The alumina composition which gave the best results was found to contain 94% aluminum oxide by weight.

As received from the vendor, the particle size of the ceramic raw material is controlled to maintain proper mesh size. After weighing and blending, the ceramic mix is ball-milled to insure homogeneity and to decrease particle-size further.

A careful check is kept on the viscosity of the ceramic slip so that fabricating techniques will give reproducible results. The slip viscosity is measured

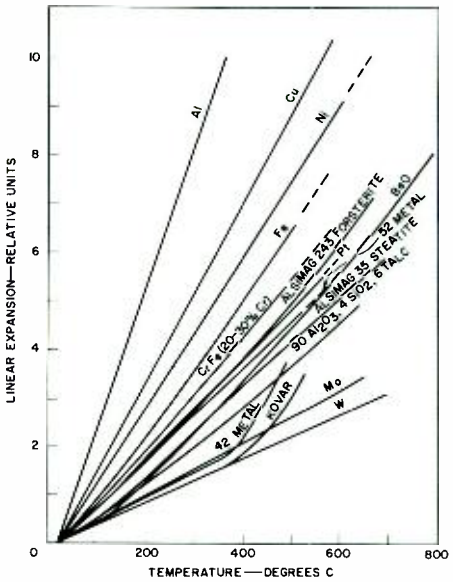


Fig. 2—Linear expansion as a function of temperature for several different materials.

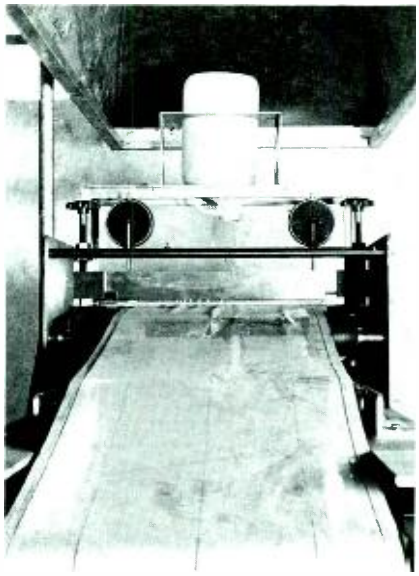


Fig. 3—"Doctor blade" technique used in the formation of precisely controlled thermoplastic sheets.

by means of a Brookfield Viscosimeter.

The slip is cast in sheets of the desired thickness by use of the *doctor blade* technique. As shown in Fig. 3, a blade set a specified distance above the casting bed is drawn over the material to be cast. The thickness of the deposited film is controlled by the blade height above the casting plate. The film is then removed from the casting plate and processed.

The metallizing material, is applied by standard screening techniques. The viscosity of the metal paste is maintained at a specified level to produce the best screening results. The first of three sheets is metallized with pads on both sides, one side for the kovar leads, the other side for mounting the integrated circuit. The second sheet is metallized on one side only to provide the metallized circuitry. The third and top sheet is metallized for the ring mounting required for the final weld seal.

These three properly metallized sheets are then formed into a unit having a thickness of approximately 0.048 inch. The assembly is made with precise temperature and time controls. The resultant assembly is fired in a reducing atmosphere to provide optimum physical and electrical characteristics for this material. The physical shrinkage of the ceramic is about 15%. The final ceramic package measures 0.250-inch square, with an over-all height of 0.048 inch (less lead and cap), a well depth of 0.030 inch, and a mounting-pad diameter of 0.130 inch.

After the nickle plating operation, the metallized ceramics are fabricated into shell assemblies by brazing on the kovar ring and lead preforms in carbon brazing jigs (see Fig. 4). The assembly is then sent through a conveyor-belt brazing furnace in a reducing atmosphere. The package is visually and hermetically checked prior to electroplating. After plating, the packages are again tested for hermeticity on a Veeco MS-9 Leak Detector. The shell packages are then ready for device mounting, bonding and sealing.

MOUNTING AND SEALING OF INTEGRATED CIRCUITS

In the integrated-circuit pellet, a gold preform is used to solder down the chip with standard mounting techniques. Bonding is presently accomplished by means of standard thermocompression bonding techniques.

One of the most important problems in integrated-circuit packaging is hermetic sealing of the final unit. Because of the size of the flat package, usual techniques of sealing semiconductors devices could not be used. A number of other methods were considered, including soldering, brazing, glass sealing, diffusion welding, epoxy sealing and resistance series welding.

It soon became apparent that the first three methods of sealing could cause problems as a result of the heat required to seal the unit; therefore, these methods were abandoned. The fourth method, diffusion welding, is a technique that has been used by the radio-tube industry for many years in large power tubes and is finding new applications every day in the metal-joining field. This technique of gold diffusion welding produced good results, but was abandoned because of the time (in the order of hours) required to obtain a hermetic seal. Epoxy sealing may prove useful in time to come, but at present little experimental data is available on the ability of epoxy to provide a lasting hermetic seal.

Resistance-series welding proved to be the most advantageous of all methods tried. This method is well known to the metal-joining industry and with some modifications was adopted for sealing of the RCA package. Fig. 5 shows a simplified diagram of a series welding set-up.

The primary advantage of resistance-series welding is its speed. Because of the short weld time required, and also because heat loss in the weldments must be minimized to prevent warping of the weld ring, each overlapping weld is made quickly. In this technique pulses of current such as can be obtained from ½-cycle AC control or an energy-storage type of control are used. The latter control was selected because it is independent of line-voltage variations.

Fig. 4—Brazing jig used to join metal parts to the metallized ceramic pieces, and some of the brazed packages.

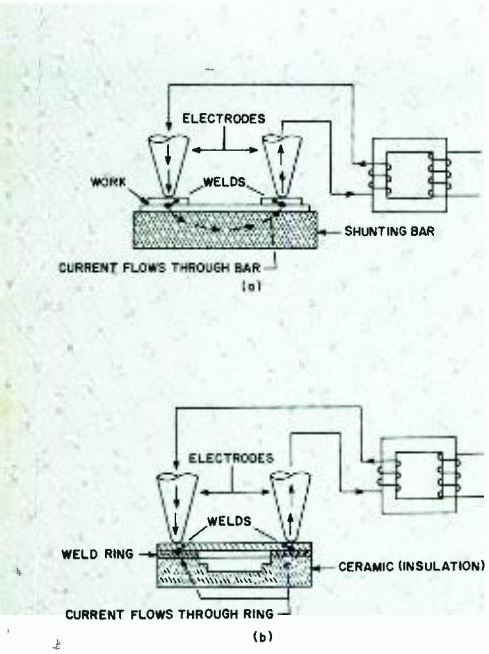


Fig. 5—(a) Representation of current flow through metal bar during series welding and (b) welding setup for actual welding of ring to ceramic.

HENRY J. KRAUTTER received his BSEE from Lafayette College in 1950 and his MSEE from Newark College of Engineering in 1953. In 1950, he joined Westinghouse as a welding engineer in their trainee program where he worked on various types of automatic machinery used in the production of electron tubes and lamps. He then joined the Air Reduction Co. in 1954 where he was responsible for the design of production equipment used in the manufacture of the Titan missile. In 1958, Mr. Krautter joined the Package Development group at RCA, Semiconductor and Materials Division as a packaging engineer. In this capacity, he designed and developed packaging for a wide variety of semiconductor devices, and was awarded two RCA Achievement Awards for his work on tunnel diode packages. Presently, he is engaged in the development and production of the RCA's flat packages used for integrated circuits. Mr. Krautter holds 9 patents, and is a member of the IEEE and the American Welding Society.

ALFRED MORENA received his B.S. degree from the University of Illinois in 1951, and his M.S. degree from Rutgers University in 1960, both in Ceramic Engineering. In 1951, he joined RCA as a glass technologist where he was primarily involved in liaison work between laboratory and production activities. From 1952 to 1956, he was employed by the Mucon Corporation, Newark, and was responsible for the development of ceramic capacitors and transducer compositions. Mr. Morena then joined Electro Ceramics, New Haven and implemented and directed all phases of development and manufacture for subminiature ceramic capacitors. In 1960, he joined Metal and Thermet Corporation, Rahway, where he worked on high purity raw materials used in ceramic dielectrics. Mr. Morena rejoined RCA in 1962 as a ceramic engineer at Somerville and worked on the development of multi-layer ceramic capacitors for micromodules. Mr. Morena is now engaged in semiconductor package development, primarily for integrated cricuits. He is a member of the American Ceramic Society, Institute of Ceramic Engineers, New Jersey Ceramic Society and the National Ceramic Fraternity Keramos.

The heating action of the capacitor discharge current in making the weld is very important. The most desirable welding current will heat the metal quickly but with only the quantity of heat needed to fuse the desired volume of material in each weldment. A capacitor-discharge energy-storage system provides this desired type of current wave, as shown clearly in Fig. 6. The capacitor discharge current rises quickly to a maximum value to point *A*, where fusion of the metal begins; from *A* to *B* the weld is made, and at *B* cooling begins.

A major factor which had to be considered in this method of sealing is electrode polarity. In this welding of polarity-sensitive materials, a simple reversal of the direction of weld current can reduce the strength of the weld as much as 50%. The problem of improper polarity is not overly critical in standard types of spot welding, but for series welds in which two weld nuggets are produced for every pulse of current, this condition cannot be corrected by reversing polarity. The polarity effect was overcome by use of a different electrode material and by adjusting the pressure on one of the electrodes to achieve a proper heat balance.

Fig. 7 shows the package and the current-flow direction when the hermetic seal is being made. In pilot production, this technique has proved to be 97% effective in the production of hermetic seals.

CONCLUSIONS

The RCA package satisfies the basic packaging requirements of protection, physical and electrical characteristics, and form factor. In addition, it offers the versatility of form and construction which permits changes in lead dimension, size, shape, and type of mounting without major changes to the manufacturing set-up. Although this additional versatility is desirable, the single most important feature of this package is the unique construction which permits electrical continuity from inside the hermetic chamber to the external lead without "through-hole" connections. Such through-hole connection, which is an integral part of all other packages, represents the major cause for leakage in the hermetic seal. The RCA package has an inherent reliability as a result of its design and construction which cannot be offered by any other package in the semiconductor field.

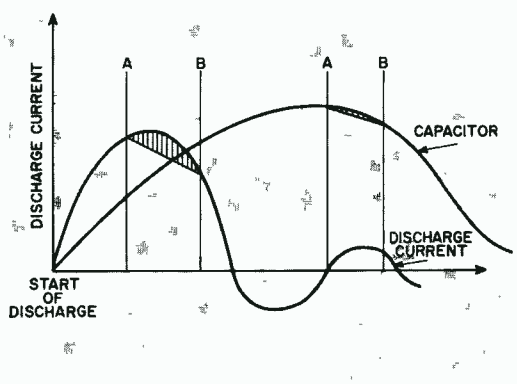


Fig. 6—Pattern of capacitor discharge current.

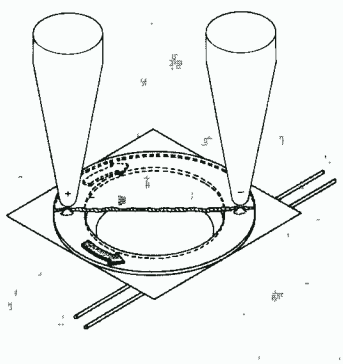


Fig. 7—Isometric view of package and current flow during welding.

LAMINATED FERRITE MEMORIES

The batch fabrication technology and operating characteristics described herein for a laminated ferrite memory with integrated windings results from research on high-speed digital memory systems. A 100-nsec cycle time has been obtained, and the batch fabrication technology promises a drastic cost reduction. The nature of the laminated structure makes practical a further cost reduction from the use of integrated semiconductor driving circuitry. Limitations[1] on memory capacity of an economic nature may be removed, and memories with capacities in excess of 10^7 bits operating at cycle times of a few microseconds may become practical—an order of magnitude increase in capacity over present nonintegrated core-transistor memories. The general philosophy for the high-speed-memory research program in the RCA Laboratories Computer Research Laboratory is: 1) use of the well established ferrite technology; 2) miniaturization of the size of the storage element while maintaining closed magnetic flux paths, and 3) use of printed circuit techniques to facilitate fabrication and assembly. This philosophy resulted in the development of the "Microaperture High Speed Ferrites"[2], the "Microferrite Arrays"[3] commercially available from the RCA Electronic Components and Devices Memory Operations in Needham, Mass., and is culminating in the laminated ferrite memory described here. A brief description of the former memories is included to demonstrate the wide scope of characteristics that may be attained with microsized ferrite storage elements.

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BEFORE describing the laminated ferrite memory, a brief discussion of preceding RCA microsized ferrite storage elements will demonstrate their wide scope of characteristics.

BACKGROUND

The "Microaperture High Speed Ferrites" consist of miniature ferrite wafers. Four apertures with a diameter of 1 mil each and a center-to-center spacing of 2 mils are drilled in the center of each sintered wafer (Fig. 1). This element is equivalent to a core with an inside diameter of 4 mils.

Drilling is accomplished by a finely focused, high-energy, pulsed electron beam. Four separate windings, each linking an aperture in the pattern shown in Fig. 1, are fabricated by photoetching techniques to give a wired element. The elements are assembled in a mosaic and the individual windings are interconnected by mass fabrication techniques to give a wired memory plane. Fig. 2 is a photograph of an assembled 4 x 4 mosaic. A 16 x 12 mosaic was also assembled and operated at 100-nsec cycle time.

The "Microferrite Arrays" utilize ferrite toroids with an inside diameter of 10 mils, an outside diameter of 50 mils, and a height of 10 mils. The toroids are metallized with a pattern on both surfaces and through the apertures by vacuum evaporation. The metallized toroids are inserted into plastic channel strips with preprinted tabs. The tabs interconnect the far surface of one core to the near surfaces of the adjacent cores, resulting in a printed winding linking all the cores in a strip (Fig. 3). The strips are mounted on a board and an additional winding, for operation in a word-organized mode, is hand-threaded through corresponding cores in adjacent strips. Fig. 4 is a photograph of a microferrite plane containing 32 x 60 cores available commercially from the ECD Needham Memory Products Department. A stack of 1,024 words, with 200 cores per word, assembled at the Needham Memory Operation, is presently undergoing tests at DEP Applied Research in Camden. A cycle time of 300 nsec, with maximum drive currents at 350 mamp, and sense outputs of ±50 mv (two cores per bit operation), are anticipated.[4]

Competitive approaches for achieving high-speed operation and/or large bit capacities include magnetic thin films,[5] aperture ferrite plate,[6] the FLEA permalloy sheet,[7] and the waffle iron memory.[8] *It is believed that the laminated ferrite memory described in the remainder of this paper, offers considerable advantages in operating characteristics and anticipated bit costs over these other approaches.*

Final manuscript received April 22, 1964.
Editor's Note: This paper received the coveted *"Best Paper Award"* at the AFIPS 1963 Fall Joint Computer Conference, Las Vegas, Nevada.

Fig. 1a—Geometry of a microaperture ferrite element.

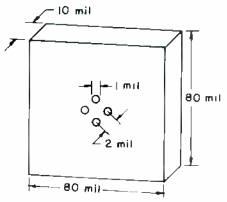


Fig. 1b—Winding pattern for microaperture element.

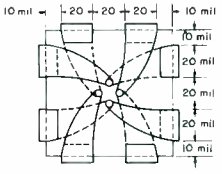
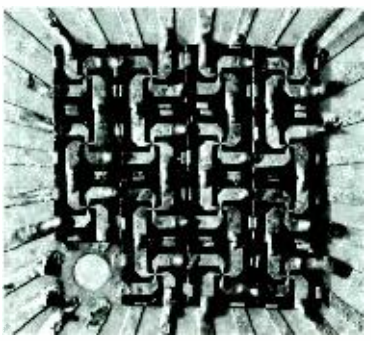


Fig. 2—A 4 x 4 mosaic of microaperture wafers.



ORTHOGONAL ARRAY STRUCTURE

The laminate technology permits a great flexibility of geometries of the windings. The simple orthogonal winding structure shown in Fig. 5 is particularly suited for high speed. In this structure, two orthogonal sets of conductors, an X-directed set and a Y-directed set, are embedded in a sheet of square loop ferrite. Each cross-over point, between an X and a Y conductor, is a storage location. For high speed, the array is operated using impulse switching in a mode that is word-organized with two cross-overs per bit—analogous to the mode of conventional arrays (word-organized, two cores per bit[9]). The *word* current (read-write) is applied to an X winding, and the Y windings are used for both *digit* and *sense*.

The experimental arrays fabricated to date have a capacity of 256 cross-overs (128 bits, equivalent to 16 words of 8 bits each). The overall thickness of the ferrite laminate is approximately 5 mils and the conductor spacing, for both the X and Y conductors, is 10 mils. The conductor cross-sectional dimensions are approximately 2.5 x 0.7 mils.

FABRICATION TECHNOLOGY

The basic operations involved in the fabrication of a laminated memory array are: *doctor blading, laminating and sintering*, and *conductor screening*.

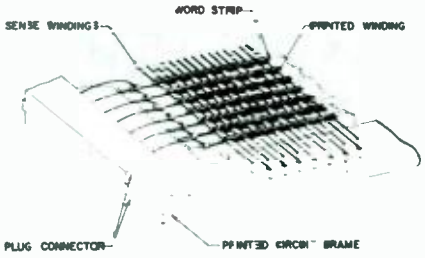


Fig. 3—Microferrite array.

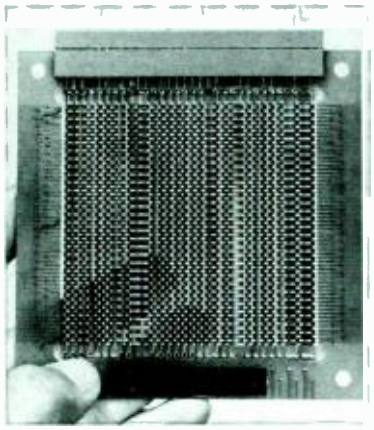


Fig. 4—Assembled 32 x 64 microferrite array.

Fig. 6—Doctor bladed ferrite.

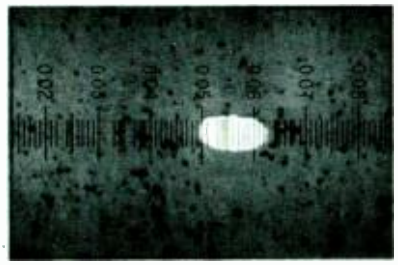
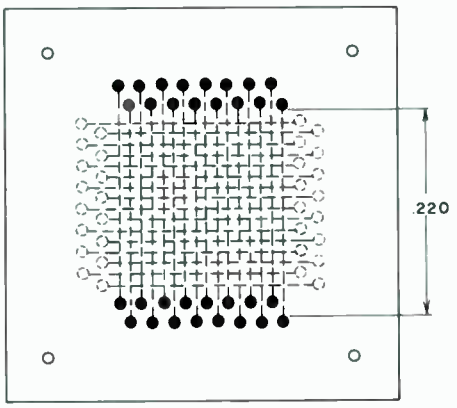


Fig. 8—A 3 x 0.7 mil conductor section.



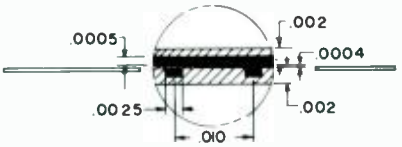


Fig. 5—Laminated array structure.

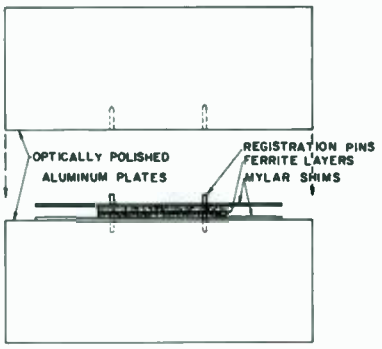


Fig. 7—Laminating jig.

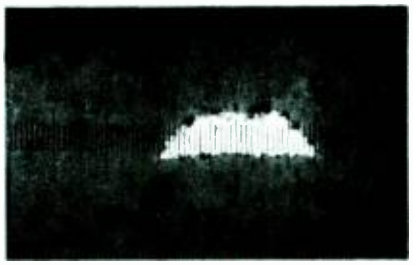


Fig. 9—A 3.0 x 0.8 mil conductor section.

Doctor Bladed Ferrites

The doctor-blading (DB) technique for fabricating sheets of ferrites consists of preparing a slurry of the desired ferrite powder and appropriate organic binders. The slurry is spread in an even layer on a glass substrate by the sweeping action of a blade, called a *doctor blade*, held at a constant distance above the glass surface as shown in Fig. 6. The sheet is air-dried and peeled off the glass surface.

The magnetic characteristics (coercive force, saturation, flux density, squareness ratio, and switching coefficient) attained in DB toroids is the same as the toroids of the same composition prepared by conventional dry pressing techniques.

Laminated Ferrites

Monolithic structures with embedded conductors are fabricated by laminating together the required number of sheets. This is accomplished by pressing green sheets together at moderate pressures and temperatures which are not too critical. A simple hydraulic press with heated platens is adequate for this purpose. The ferrite sheets are sandwiched between two aluminum blocks as shown schematically in Fig. 7, and placed between the heated platens of the press. Pressure is applied for a few minutes after the block temperature, as monitored by a thermocouple, has stabilized. The laminated sheets are next sintered in a controlled temperature furnace.

Conductor Screening

The technique developed for forming conductors as an integral part of a "green" ferrite sheet is similar to the familiar silk-screening process. A photoformed metal mask is laid on a glass substrate, and a paste consisting of the required metal powder and a binder is squeegeed through the mask onto the glass substrate. The mask is then removed leaving the required conductor pattern on the glass surface. Ferrite is doctor-bladed on the glass substrate over the conductor pattern. When peeled off the glass, the ferrite sheet contains the conductors intimately embedded in it and flush with its surface. Similar ferrite sheets with conductors, or spacer sheets without conductors, are then laminated, as described above. On firing, the conductors sinter along with the ferrite.

Conductor dimensions as small as 1.3 x 0.5 mils in cross section (Fig. 8), with a resistance of 2 ohms per inch, have been obtained. For most of the arrays tested, the conductor cross section is 2.5 x 0.7 mils (Fig. 9), and their resistance is 3 ohms per inch.

ORTHOGONAL ARRAY FABRICATION

A number of experimental arrays, 16 x 16, were made. The orthogonal array structure (Fig. 5) is fabricated by laminating three sheets of doctor-bladed ferrite in the order shown in Fig. 10. The top and bottom sheets, with a green thickness of approximately 2.5 mils, contain conductors spaced 13 mils apart. The center sheet is 0.5 mils thick and contains no conductors. Holes of 16-mil diameter are gang-punched in each sheet in the patterns shown in Fig. 10. The rows of holes are used for access to the embedded conductors. The corner holes are used for registry during assembly and match the pin locations in the laminating jig of Fig. 7. After sintering, the ferrite laminate shrinks to the dimensions shown in Fig. 5 (overall thickness approximately 5 mils, conductor spacing 10 mils).

Interconnections to the embedded conductors are provided via the plastic film with etched conductors (Fig. 11). The conductors, spaced on 10-mil centers, overhang the plastic film and are positioned over the access holes. They are then manually soldered in place. Fig. 12 shows a 16 x 16 array mounted on a printed-circuit board ready for testing. Fig. 13 is a magnified x-ray photograph of an array. Fig. 14 is a partial cross section showing some of the embedded conductors which shows the monolithic nature of the ferrite without any trace of the lamination.

OPERATING MODE

The memory is word-organized, and two crossovers per bit are used. In this mode, all bits of a selected word are subjected to the same read-write current pulses. The best digit drive techniques[2] found consist of applying a unipolar digit pulse to either one or the other of the two crossovers of a bit in time coincidence with the write pulse. In other words, if the two crossovers of a bit are labeled A and B, crossover A is digited with, say, a positive pulse to write a binary *1* and crossover B is digited with a positive pulse, also, to write a binary *0*.

Sensing is differential, in that the output sense voltage obtained during the read is the difference between the two voltages induced along the digit sense windings linking the two crossovers of a bit. Different polarities of voltage correspond to the two binary states.

Because of the orthogonal disposition of word and digit conductors, word read-write currents switch flux along a selected word conductor that does not link the digit conductor. A digit pulse applied to a digit conductor in time coincidence with a write pulse switches a component of flux mutual to both the word and digit conductors at the corresponding crossover point. The application of a read pulse switches this mutual flux and induces a sense voltage in the digit winding. The polarity of the induced sense voltage is determined by the polarity of the applied digit current.

Operation of a bit may be visualized with the aid of the vector diagrams shown in Fig. 15. The flux switched by the word write current in the vicinity of a crossover point may be represented by the vector ϕ_w. The magnitude of this vector is proportional to the flux contributing to the bit operation. The direction of this vector is normal to the plane of the flux iself, and using the right-hand-rule convention, is in the direction of the current establishing the flux. The application of a digit current in time coincidence with the write pulse causes the vector ϕ_w to tilt to ϕ_t in the direction of the digit current, i.e., to have a component in the digit direction, as shown in Fig. 15.

Application of the word read current reverses the flux vector ϕ_t to the position ϕ_r, resulting in a sense output. Increasing the amplitude of the digit current relative to the write current increases the tilt angle and correspondingly the sense output. The amplitude of the digit current is limited by its disturbing effect on the stored information.

EXPERIMENTAL DATA

Ferrite Composition

The composition selected for the high speed laminated array is the same as that in use for the previously developed high speed ferrite memories.[2,3] The switching coefficient for this material is 0.3 oersteds-microseconds, the coercive force is 1.0 oersted, the Curie temperature is 250°C, and the squareness ratio is 0.9.

With different materials other operational characteristics could be obtained. For example, power requirements can be very low using a switchable ferrite with low coercity, e.g. half an oersted. Also, recently developed wide temperature range material could be used.[9]

Array Operation

Three basic pulse programs are used to evaluate the performance of an array. These are:[2]

1) Alternate *1-0* read-write.
2) Alternate *1-0* read-write with disturbs.
3) Mixed *1*'s and *0*'s read-write with disturbs.

These programs are provided by a set of transistor drivers (described in detail in Ref. 2) triggered by commercially available 10-Mc logic building blocks. The read-write and digit pulses are of adjustable amplitude, 30 nsec wide at the base with a maximum repetition rate of 10 Mc. The operating current levels and sense outputs are:

Read Current = 370 mamp
Write Current = 220 mamp
Digit Current = 21 mamp
Undisturbed Sense Output = ±9 mv
Back Voltage (including IR drop) per crossover = 340 mv

The sense outputs observed with test programs 2 and 3 are ±6 mv and ±5 mv, respectively. Test program 3 is sufficiently stringent that a memory array yielding the acceptable outputs of ±5

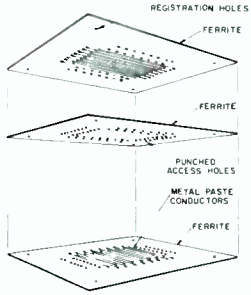


Fig. 10—Laminate details.

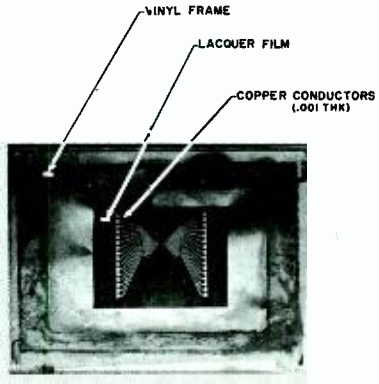


Fig. 11—Interconnecting conductors.

Fig. 12—A 16 x 16 array mounted for test.

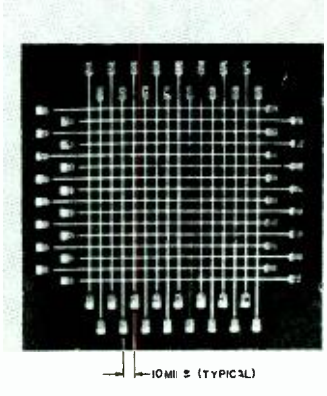


Fig. 13—Magnified X-ray of array.

mv will perform satisfactorily in a computer under random conditions.

Uniformity of Fabricated Arrays

The uniformity of the electrical and magnetic characteristics of laminated arrays is obviously of importance in determining the feasibility of the fabrication process. The measured electrical resistance of 32 (2 x 16) embedded conductors in a recently fabricated sample have a total variation of 0.2 ohms (15 conductors have a resistance of 0.7 ohms, 11 conductors have a resistance of 0.8 ohms, and the remaining 6 conductors have a resistance of 0.9 ohms). Fig. 16 shows the superimposed sense output signals obtained from the same bit position in eight successive words. Approximately 80% of the 128 bits in the array have acceptable outputs above a certain arbitrary minimum while the remaining bits could possibly be used, but would present undue system difficulties. The nonuniformity in output is attributable entirely to a nonuniform conductor cross section, and reasonable care in the fabrication of the conductors should provide the required uniformity.

Propagation Characteristics of Sense-Digit Line

The experimentally determined characteristics of the sense-digit lines in a laminated array are:

$Z_o = 200$ ohms
$\alpha_{ac} = 5.7 \times 10^{-3}$ db/bit
$\alpha_{dc} = 1.2 \times 10^{-3}$ db/bit
$\tau_d = 3.3 \times 10^{-11}$ sec/bit

This data is obtained by propagating a pulse along a line consisting of the series connection of 16 sense-digit conductors in an array. The total embedded conductor length is 3.32 inches. This is equivalent to 332 bits spaced 10 mils apart. The 16-word conductors in the array are grounded as shown schematically in Fig. 17. The characteristic impedance of the line is experimentally determined from the condition of minimum reflection. The delay per bit τ_d is computed from the total delay between the peak of the output pulse and that of the input pulse (Fig. 18) divided by 332, the number of equivalent bits on the line. The pulse attenuation is due to two factors: the attenuation α_{dc} due to the series DC resistance of the line (measured value of 10 ohms), and α_{ac} that due to the losses in the ferrite reflected as an equivalent AC line resistance. As can be seen in the data above, the AC losses exceed the DC losses.

ACCOMPLISHMENTS AND FUTURE DEVELOPMENTS

The fabrication techniques described have been modified to permit the fabrication of monolithic sheets with embedded conductors measuring 2.8 x 0.8 x 0.005 inches containing 16,384 crossovers (organized as 256 x 64). Fig. 19 is a magnified x-ray photograph of such a laminate, and Fig. 20 shows the laminate mounted on a printed-circuit board with all windings interconnected to multipin connectors. Test data obtained with these large arrays is in agreement with that obtained with 16 x 16 samples. A 1,024-word stack is presently under construction using four of the 256 x 64 arrays.

Such techniques for fabrication are obviously applicable to the preparation of a large class of ferrite devices and systems with integrated windings. The memory arrays fabricated and tested have not been especially optimized. For example, higher bit packing densities can be achieved quite readily. Fig. 21 is an x-ray photograph of an array with 5-mil conductor spacing. The advantages to be gained from this tighter packing is a reduction in back voltages, in propagation delays, and in signal attenuation. A further decrease in bit spacing, down to a few mils is possible with the small cross sectional conductor dimensions shown in Fig. 8. The reduction in conductor cross section will result in a reduction in drive current requirements without a deterioration in sense output. For memories of short word lengths, say 20 to 30 bits, a thicker ferrite laminate may be used to advantage to give higher sense outputs with correspondingly higher back voltages.

Conversely, long words are readily realized by reducing the laminate thickness. This reduces both the sense output and signal attenuation.

For relatively slow speed operation, say a 1-μsec cycle time, the required drive currents are under 50 mamp as has been experimentally verified. The sense output is approximately 1 mv. The low drive currents and the relatively high sense outputs are well matched to the capabilities of integrated electronic circuitry. Word drivers, triggered by address decoding trees, can be fabricated and assembled as integrated arrays. Similarly, integrated sense amplifiers may be built to detect the binary signals. The physical structure, and physical dimensions of laminated array are also well suited for interconnection to arrays of integrated semiconducting elements. Combining laminated arrays

Fig. 14—Micrograph of partial cross section of array (1 division = .435 mil).

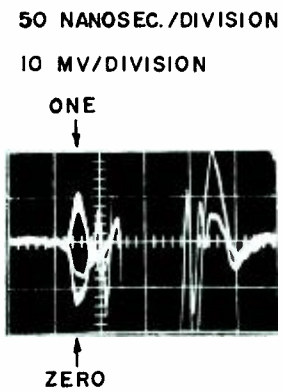


Fig. 16—Superimposed sense outputs from corresponding bit of eight words.

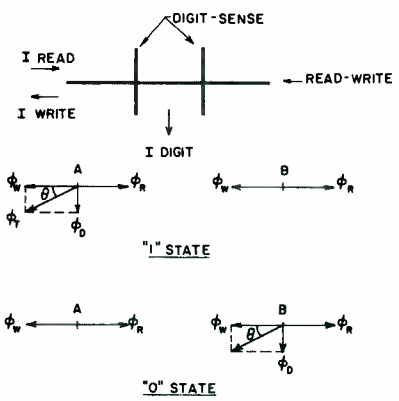


Fig. 15—Flux vector diagram.

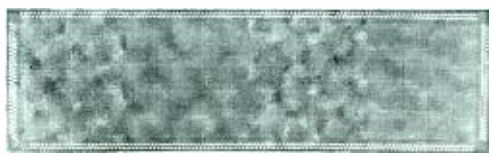


Fig. 19—Magnified X-ray of 256 x 64 array.

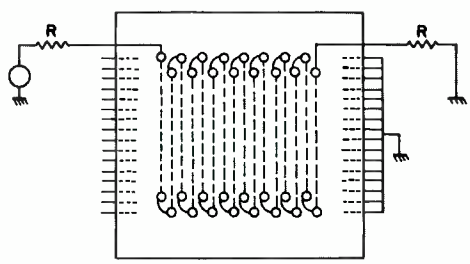


Fig. 17—Long bit sense digit line.

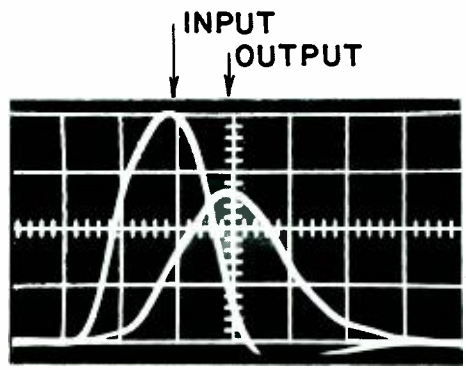


Fig. 18—Pulse propagation characteristics.

with integrated electronic circuitry promises to result in a substantial cost per bit reduction over the present state of the art. This in itself will make economical random access ferrite memories with capacities in excess of 10^7 bits. The expected cycle time of these memories will be predominantly determined by the characteristics of the integrated semiconducting circuits and may conceivably be less than 0.5 μsec.

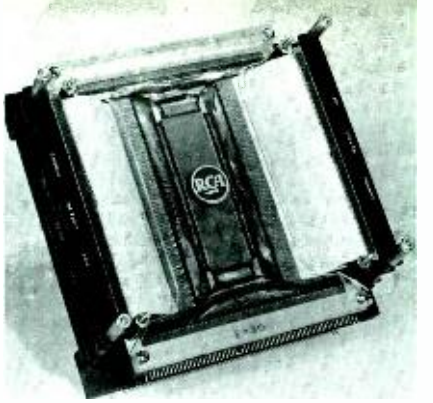


Fig. 20—Fully connected 16,384 cross-over memory plane.

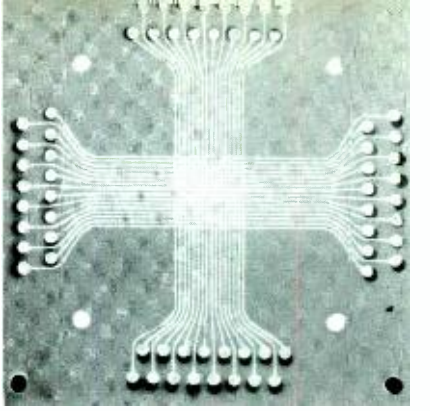


Fig. 21—A 5-mil-spacing X-ray.

CONCLUSIONS

The results presented in this paper show conclusively that the techniques described are well-suited for the low-cost fabrication of memory arrays of micro size at exceptionally high packing densities. The physical and electrical characteristics of these arrays may be tailored to meet all important aspects of digital random access memories, including high speed (100-nsec cycle), large capacities (in excess of 10^7 bits), nondestructive read-out, wide temperature range operation, etc. The drive requirements and sense output for these arrays as well as their ease of fabrication place them in a favorable position with respect to other integrated magnetic arrays, e.g., FLEA memories, twistor memories, thin magnetic film memories, or the waffle iron memory.

ACKNOWLEDGMENTS

The authors wish to express their appreciation to their many colleagues at RCA Laboratories and the Product Divisions of the Corporation who were involved in this program.

Dr. Bernard Schwartz, RCA Laboratories, suggested the basic ceramic techniques used for the fabrication of these memory arrays. The authors wish to express their appreciation to him for his help during the early phases of the work.

The authors wish to express their thanks also to R. Noack and A. Monsen, RCA Laboratories, who fabricated and wired many of the sample arrays.

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Left to right: Authors Chandler Wentworth, Dr. Rabah Shahbender, Dr. Jan Rajchman, Dr. Kam Li, and Stuart Hotchkiss examine an experimental unit of laminated ferrite memory.

THIN-FILM MICROELECTRONICS —A REVIEW

Reviewed herein is the present status of thin-film microelectronics relative to silicon-diffusion processes; the role of both passive and active components is considered. Advantages, characteristics, and technical problems in applying thin-film integrated circuits are discussed and summarized in tabular form; some of the several promising fabrication approaches for thin-film integrated circuits are also described. It is possible that the best technical features of the two technologies (silicon and thin-film) will produce a single integrated circuit.

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THE technology of microelectronics involves two basically different processes: the *silicon-diffusion* process and the *thin-film* process. It is the former, the silicon-diffusion, that has made a major breakthrough in recent years, and has reached the stage of development and production; monolithic silicon blocks perform satisfactorily in most digital applications, and in many analog applications. It appears reasonably certain that increasing numbers of electronic components will be manufactured this way in the future.

Analogous to the fact that a wonder drug does not cure all diseases, the monolithic silicon block has limitations for certain applications, such as parasitic effects, relatively poor component tolerances, and instabilities. Thin-film passive elements, on the other hand, excel in these areas. The potential advantages of thin-film integrated circuits are summarized in Table I; however, many possibilities are yet to be determined through research efforts. Thus, thin-film integrated circuits ideally supplement the monolithic silicon blocks for integration into equipment having stringent circuit requirements. As components, thin-film integrated circuits are not likely to compete with monolithic silicon blocks on a volume basis.

Thin-film circuits represent a rather small portion of the total defense equipment circuitry; however, the thin-film circuits represent an important minority to equipment manufacturers such as RCA's Defense Electronics Products, since the resultant improvement in overall equipment performance may be sufficient to make the difference between winning or losing defense contracts. Therefore, to these manufacturers, thin-film technology may be just as important as silicon diffusion.

THIN-FILM PASSIVE COMPONENTS

In microelectronics, passive components include resistors, capacitors, inductors, and conductors for intra- and interconnections. In addition to their precision in holding tolerance, their stability, and their relative economy, the merit of passive components is judged on the basis of parameter values per unit area; eg., the resistivity or dielectric constant per unit of required substrate surface area; the surface areas occupied are closely related to the cost of an integrated circuit, since this factor may determine the complexity of functions or circuits that can be accommodated in fixed restricted space.

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Thin Film Resistors

Conventional thin-film resistors are made from Nichrome and Cermet; Table II shows their essential characteristics compared with diffused silicon resistors. Thin-film resistors can be held to closer tolerances, exhibit greater stability and demonstrate an absence of distributed capacitance. These characteristics ensure that thin-film resistors will behave like conventional resistors even at high frequencies.

Resistor composition and deposition processes employing binary alloy systems and containing metals *A* and *B* (Fig. 1), have been developed for improving resistivity; the resultant resistivity is substantially greater than that of either metal alone. Maximum resistivity takes place for many systems when the atomic percentage is approximately 50:50.

The resistance of a thin-film resistor varies inversely with film thickness; for a given system, however, there is only one film thickness that exhibits zero temperature coefficient. Fig. 2 shows the manner in which the temperature coefficient of a thin-film resistor relates to the film thickness, where thickness t corresponds to zero temperature coefficient; for most resistor systems, t is in the order of 1,000 angstroms.

TABLE I
Potential Advantages of Thin-Film Integrated Circuits

A. In Performance
  1. Higher Reliability
  2. Higher Switching Speeds
  3. VHF, UHF and Microwave
  4. Greater Nuclear Radiation Resistance
B. In Manufacturing
  1. Large Array Integration
  2. Low Cost Integration
  3. Lower Capital Investment
C. In Engineering
  1. Closer Tolerances
  2. More Stable
  3. Same Basic Circuit Techniques

TABLE II — Resistor Characteristics

Parameters	Diffused Silicon		Thin Film	
	Diffused *p*	*n*	Nichrome	Cermet
Resistivity, Ohms/Sq.	100-300	2.5	40-400	100-1000
Resistance, Ohms/mil²	50-150	1.25	20-200	50-500
Temp. Coeff., ppm/°C	+1500 +2800	+100	+100	−55
Power Dissipation mw/mil²	3	3	2	1
Value Tolerance	± 20%	—	± 8%	± 8%
Distributed Capacitance pf/mil²	0.2	0.6	nil	nil

Thin Film Capacitors

Silicon monoxide, with a dielectric constant of approximately 5. has been used for years as the dielectric materials of thin-film capacitors. Table III compares the pertinent characteristics of thin-film and diffused-silicon capacitors. Thin-film capacitors are not voltage sensitive and offer high-quality Q factors; the exceedingly low leakage current and zero shunt capacitance make the thin-film capacitors suitable components for high-speed and high-frequency operation.

To increase capacitance values per unit area. dielectric materials other than SiO must be developed. One such material is a pyrochlore structure that yields a moderately-high dielectric constant, low temperature coefficient, and an intrinsically high Q. At zero temperature coefficient, a dielectric constant approximately one order of magnitude higher than that of SiO has been observed (Fig. 3). These outstanding qualities hold up well at very-high frequencies.

Conductors and Inductors

Intra- and interconnections of integrated circuits usually consist of thin metal films, prepared by vacuum deposition. The ability of the film to adhere to the substrate and the electrical conductivity of the film are two of the most important characteristics. Electrical conductivity increases (conductor resistance decreases) when the films are made thicker; such behavior occurs not only at low frequencies but more significantly and in greater proportion at high frequencies. Furthermore, geometry changes. when coupled with the use of multiple films, may decrease the skin effect and substantially improve the conductivity at very high frequencies; however. there are restraints which must be observed in order to assure that the thin films are compatible with other components of an integrated circuit.

The relatively low conductivity of the thin-film conductor limits the circuit Q even at VHF frequencies. At lower frequencies, thin-film inductors render no practical advantages. Substantial research and development effort has been exerted by industry to simulate inductors by means of active RC networks; such simulated inductors are now beginning to give way to thin film circuits.

THIN-FILM ACTIVE DEVICES

The major impediment to progress in thin-film technology has been the lack of thin-film active devices; therefore, the development of outstanding active devices was of the highest priority. Although still in the early research stage, both bipolar and field-effect thin-film transistors[1,2] have been evaporated on insulating substrates. Such transistors can become diodes by changing either the electrode connections or the deposition processes.

Field-Effect Thin-Film Transistors

The RCA Laboratories first announced the field-effect thin-film transistor,[1,2] known as the TFT, in 1961. Recent evaporated units have been life tested over thousands of hours, and following this testing, many of them exhibit transistor action with only slightly degraded characteristics.

The TFT can be adequately represented by the circuit of Fig. 4; note

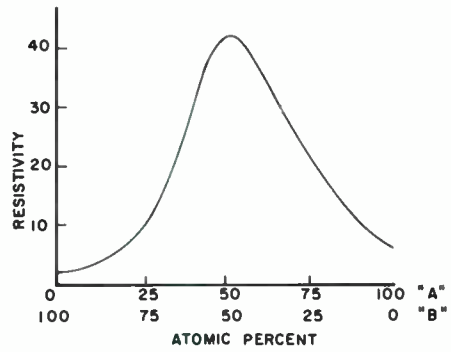

Fig. 1 — Resistivity of a binary alloy system, metals A and B.

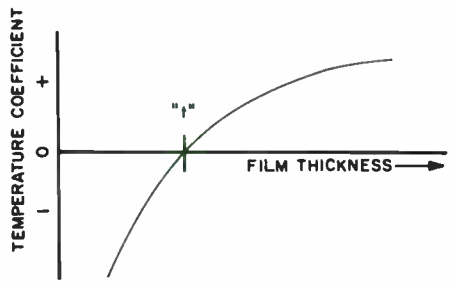

Fig. 2 — Temperature coefficient of thin film resistors as a function of film thickness.

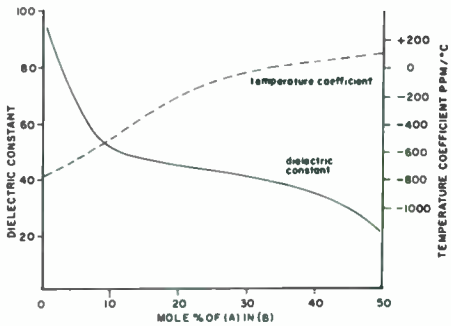

Fig. 3 — Dielectric constant and temperature coefficient of a new dielectric system as a function of composition.

TABLE III — Capacitor Characteristics

Parameters	Diffused Silicon		Thin Films	
	Max.	Min.	Max.	Min.
Capacity, pf/mil²	0.1	0.25	0.01	2.5
Dissipation Factor	0.7%	100%	0.2%	2.5%
Voltage Sensitivity	$V^{-1/2}$	$V^{-1/2}$	0	0
Polar	Yes	Yes	No	No
Shunt Capacitance	18%	25%	0	0
Leakage Current at 5 Volts	10^{-9}	10^{-9}	10^{-15}	10^{-11}

TABLE IV — Application Considerations of TFT's

Potential Advantages		*Present Disadvantages*
1. Large array integration	6. High nuclear radiation resistance	1. Low g_m/C_{fb}
2. Both p and n types on the same substrate	7. Low cross-modulation products	2. Low f_{max}
3. Low-cost integration	8. Low harmonic distortion	3. Poor life and stability at present
4. High input impedance	9. Low-power integrated circuits	
5. High Reliability	10. Packageless integrated circuits or arrays	

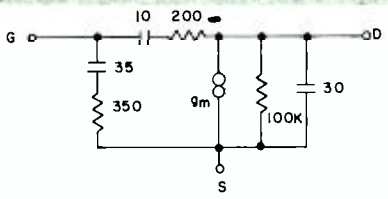

Fig. 4 — TFT equivalent circuit and parameters:

	TFT	MOS	2N918
V_{d-s}, volts	3	15	5
I_d, ma	2	2	2
Supply power, mw	6	30	10
g_m, umhos	2,000	2,000	80,000
C_{rb}, pf	10	0.1	1.5
R_{in} (low freq.)	infinite	infinite	2,000 ohms
C_{in} (low freq.)	40	2.5	5
R_{out} (low freq.) pf	100	40	100
Power gain (low freq.)	high	high	45 db
μ	high	medium	high
f_{max}, Mc	20	200	1,000

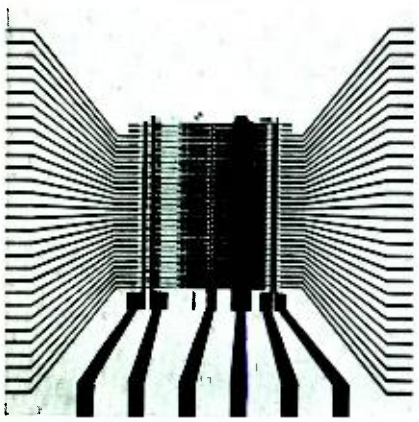

Fig. 5 — A 30-stage scanner with evaporated fan-out connections (Weimer).

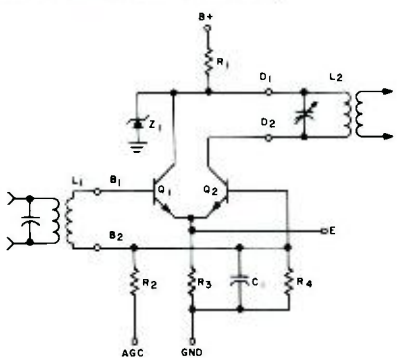

Fig. 6 — Frequency converter stage, 120 Mc to 12 Mc.

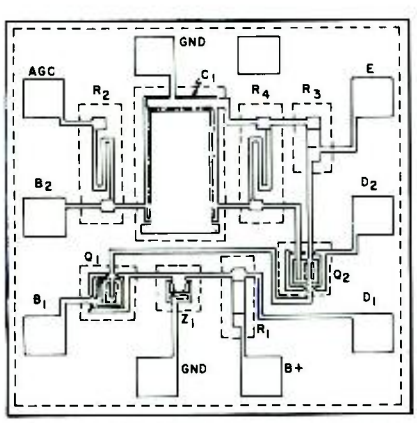

Fig. 7 — Integrated pattern, 120-Mc to 12-Mc frequency-converter stage.

the accompanying comparison of the TFT with the MOS and 2N918 transistors in pertinent parameters of operation.[3] Fig. 4 illustrates the advantages of the TFT for large-array integration. The TFT possesses high input and output impedances and power gain at low drain-to-source voltages. In its present geometry and construction, the TFT has been operated at frequencies up to 75 Mc; for the benefit of equipment designers, pertinent considerations of TFT applications are listed in Table IV.

Bipolar Thin-Film Transistors

Some work in industry has been directed toward laying down thin films of intrinsic monocrystalline silicon on a nonconducting sapphire substrate. This technique may, for instance, involve the hydrogen reduction of silicon tetrachloride at high temperatures. However, it is too early to predict the role of the bipolar thin-film transistor in future microelectronics.

When the day comes that an adequate variety of active devices can be formed by thin-film depositions, then the thin-film technology will be in an excellent position to exploit certain exclusive advantages in competing with silicon-diffused integrated circuits.

THIN-FILM INTEGRATED CIRCUITS

Unlike the diffused-silicon process, thin-film integrated circuits can be fabricated by several approaches; each approach seems promising at this time. Principally, there are four types of thin-film integrated circuits currently under development.

Monolithic Thin Film Integrated Circuits

In this process for preparing thin film integrated circuits, all transistors, diodes, resistors, and capacitors are evaporated on an insulating substrate. For instance, workers at RCA Laboratories fabricated a 30-stage scan generator[4] on a single substrate by a single fabrication process; the integrated pattern with evaporative fan-out connections is shown in Fig. 5. Each stage consists of two TFT's, one diode, two resistors, and one capacitor; accordingly, there are 180 elements in this integrated scan generator which has been in successful operation for several months.

The TFT's are facing stability and reproducibility problems today, but the yield of monolithic integrated circuits of any kind is still low. In looking ahead, when the yield of monolithic integrated circuits approaches that of other solid-state devices, such as the 2N700 transistor, large-array integration would lead to a low integration cost.

Thin-Film Passive Components on Silicon Substrate

All transistors and diodes are diffused, and all passive components are in the form of thin films evaporated on the silicon substrate to complete the electrical circuit. This technique minimizes the effect of parasitics, thus extending the switching speed or frequency of operation.

Extreme care must be exercised in fabricating integrated circuits of this type. At high temperatures, for instance, the nichrome resistor material reacts with the silicon oxide passivation layer to form glass. When this chemical action takes place, the resistors become open circuited. To combat this difficulty, materials including the tin oxide have been developed, which, it was believed, would not react readily with silicon oxide. Tin oxide films, grown by the spray atomizer process and using antimony dopant, have a resistivity of about 100 ohms/sq. Ohmic contacts have been reported using nickel as an intermediate metal between such metal electrodes as aluminum and tin oxide.

As an illustration of the efforts of other companies in the field, the frequency converter stage shown in Fig. 6 is reported to work at an input frequency of 120 Mc, and an output frequency of 12 Mc, with a significant power gain.[5] Transistors Q_1 and Q_2 and diode Z_1 were diffused in the silicon substrate shown in Fig. 7, whereas all resistors, capacitors, intraconnections, and interconnection posts were evaporated on the same substrate; the complete converter stage is mounted in a TO-5 type case. In this integrated circuit, the power gain obtained at this high operating frequency is attributable to the thin-film passive components.

Transistor Chips and Thin-Film Passive Components on Insulating Substrates

To eliminate all parasitic effects, chips of transistors and diodes are bonded on an insulating substrate; again, all passive components are thin films. This hybrid combination extends the operating frequency into the VHF and UHF regions. To illustrate this high-frequency capability, RCA Defense Microelectronics (DME) proposed a high-gain, linear hybrid amplifier operating in the VHF region from 200 to 300 Mc; Figure 8 shows a two-stage, 200-Mc amplifier. Each stage has a power gain of 15 db, which has been determined to be the best compromise for stability, noise figure, and curve shift with AGC. Fig. 8 shows the topological layout of the 200-Mc amplifier in which the chips are standard 2N918 transistors.

Thin-film capacitors cause circuit problems at higher frequencies because of dielectric losses, thin-film contact losses, and contact non-linearity. It is known that the usual SiO-Al-SiO capacitors, so effective at lower frequencies, become exceedingly lossy at high frequencies. One of the few satisfactory materials at VHF and UHF is the pyrochlore structure developed by the New York Systems Laboratory of the RCA-DEP Communications System Division.

Hybrid modules have been described using substrates of 95% alumina, 0.455-inch square and 0.006-inch high. Epitaxial transistors on separate chips and multiple diodes on other chips are used, together with silk-screened interconnection patterns and resistors of Pd-Ag mixed with glass. Such techniques are similar to RCA micromodule techniques. The substrates are encapsulated in a plastic both to protect the components and reduce corrosion.

Silicon-Diffused Active Devices Embedded in an Insulating Substrate

To meet the military requirements of performance, high reliability, low cost, and resistance to adverse environmental conditions, a marriage between silicon-diffused active devices and thin-film passive components appear to be a laudible choice for satisfying circuit functions having stringent electrical characteristics. The glass embedding technique developed by the Advanced Development Section of Special Electronic Components and Devices Division at Somerville, N.J., makes this marriage possible.[6] At this writing, only diodes of certain kinds have been successfully formed into small cylinders of diffused silicon that are totally embedded in the glass and totally isolated from each other. From the standpoint of military requirements, this type of integrated circuit has many advantages:

1) Total electrical isolation of active devices,
2) Improved active device performance, because the glass substrate is an effective getter for silicon surface impurities,
3) Availability of active device contacts on thin-film surfaces, thus eliminating connection wires,
4) Compatibility with high-quality thin-film passive components, thus improving performance characteristics,
5) No hermetic package necessary.

Two diode matrices have been developed by the New York Systems Laboratory, one for use in a slow-speed 15-kc, switch-board, and the other for use in a transceiver operating at 5 Mc. The two diode matrices are shown schematically in Figs. 9a and 9b, respectively. The 15-kc matrix uses eight diodes to form a complete crosspoint, while the 5-Mc matrix uses only four different types of diodes for switching.

To illustrate the integration process, the thin-film resistor pattern and interconnections of the low-speed crosspoint are shown in Fig. 10; both sides of the glass substrate are visible[7]. The middle row of four diodes is utilized as a common connection post. The two horizontal strips on the Fig. 10 left-hand diagram represent four equal resistors, each 1.5 kilohms. Since the diode functions are entirely sealed within the glass, no further hermetic package is necessary; the substrate has been boiled in salt water for a period of 72 hours, with no degradation. Measurements indicate that both the 15-kc crosspoint and the 5-Mc diode switch exhibit crosstalk isolation approaching 90 db and insertion loss of less than 2 db. Monolithic diffused-silicon integrated circuits cannot now offer these characteristics.

CONCLUSIONS

In comparing the two processes of microelectronics on grounds of reliability, ability to withstand severe environments, and electrical capabilities, thin-film passive elements lead the competition. Thin-films have demonstrated the following advantages: 1) reliability through a longer history of use, 2) ability to withstand heat and nuclear environments which render the silicon circuits unstable, and 3) usable at power levels and at frequencies presently impossible with silicon circuits.

On the other hand, scientists and engineers of the silicon technology have been stimulated and are making vast strides in many areas. At the same time, it is conceivable that the two technologies may well be merged in time, so that the best attributes of both will be joined in one integrated circuit.

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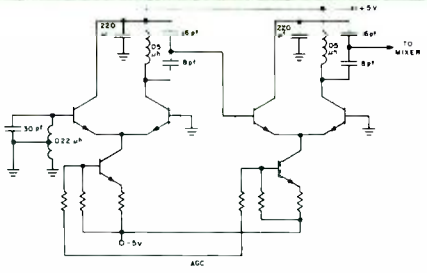

Fig. 8a — 200 Mc amplifier having a gain of 30 db.

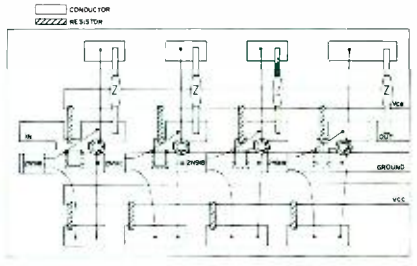

Fig. 8b — Topological layout of 200-Mc amplifier of Fig. 8a.

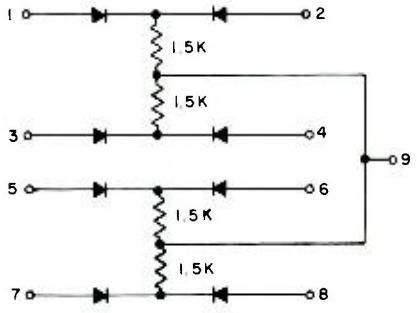

Fig. 9a — Diode matrix (90-db crosstalk, 2-bd insertion loss): a 15-kc cross point for o switchboard.

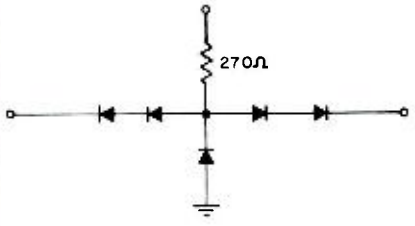

Fig. 9b — Diode matrix (90-db crosstalk, 2-db insertion loss): a 5-Mc diode switch circuit.

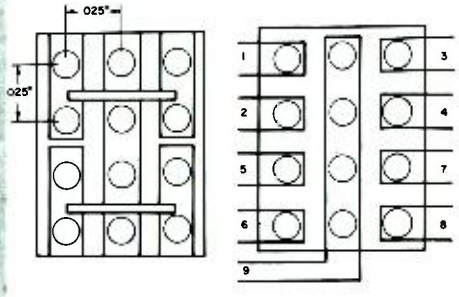

Fig. 10 — Integration pattern of the 15-kc cross point for switchboord.

A COMPLETELY INTEGRATED THIN-FILM SCAN GENERATOR FOR CROSSED-ARRAY IMAGE PANELS

A 30-stage completely integrated thin-film scan generator incorporating 60 thin-film transistors, 30 diodes, 60 resistors, and 30 capacitors has been designed. The novel circuit, whose operating characteristics resemble those of a shift register, is deposited by evaporation using movable metal masks controlled from outside the vacuum system. In one unit, 28 consecutive stages were operated for nearly 700 hours. Laboratory models of the scan generator drive the address strips in experimental solid-state image sensor panels.

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PRESENT-DAY image-scanning systems utilize electron-beam scanning in both the camera and display equipment. Image-sensing and display panels which use two scan generators to provide sequential pulses to an array of *X-Y* address strips have been proposed many years ago.[1] The picture elements in the panel are addressed in sequence by the proper coincidence of voltage pulses applied to the strips. To achieve adequate resolution for many applications, the number of vertical and horizontal strips should be very large, of the order of 500.

Fig. 1 illustrates a solid-state image panel.[2] For feasibility of manufacture, it may be preferable to fabricate the scan generators and the address strips as a single integrated thin-film circuit deposited upon a common insulating substrate. The insulated-gate thin-film transistor (TFT)[3-7] is particularly suitable as the active element in such application. A transparent substrate such as glass provides added convenience of design for devices having an optical input or output. Although an image-sensing panel may be less than 1 inch square, a large display panel could be several feet on a side.

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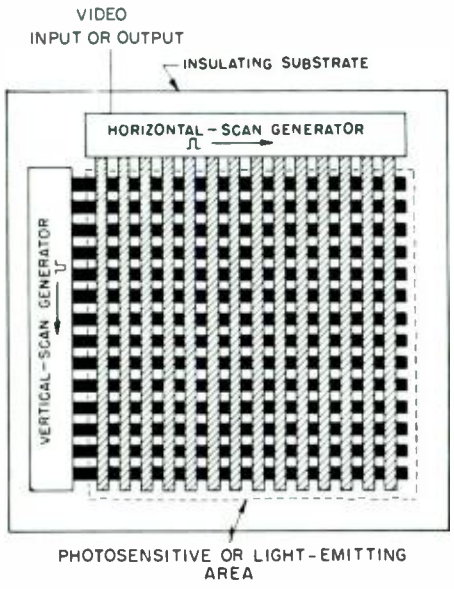
Fig. 1—Schematic diagram of a sald-state image panel. The central partian af the panel represents either a light-sensitive ar a light-emitting array.



CIRCUIT DESIGN

A novel scan-generator circuit[2] based upon the TFT, which is suitable for driving the address strips in a panel, is shown in Fig. 2. The generator is clock-driven at an elemental rate, and can provide scanning pulses of either polarity to the strips. Its operation is similar to that of a shift register in its ability to transfer any binary input. However, the circuit is simpler than a conventional shift register in that only two TFT's, two load resistors, a diode and a capacitor are required for each output connection. Although the scanning speed is accurately controlled by the clock generator, the range of permissible scanning speeds in a particular unit is determined by the load resistor capacitor time constant and by the loss of stored charge through the TFT in its off condition. For slow speed operation the TFT's must have low drain current at zero gate bias.

Fig. 3 shows an experimental model of a completely integrated 30-stage thin-film scan generator embodying the circuit described. The output strips spaced 0.0125 inch apart are connected directly to 30 photosensitive elements deposited upon the same 1-inch-square glass substrate. The TFT's and diodes use polycrystalline cadmium sulfide with overlying coplanar electrodes. Fig. 4 shows an enlarged view of a portion of the TFT and diode area. Three enhancement-type TFT's are formed for each stage, with one of the three having the gate tied to the drain to serve as a field-effect diode.[6] The load resistors are Nichrome strips, and the capacitors consist of aluminum electrodes separated by silicon monoxide.

FABRICATION AND PERFORMANCE

An evaporation jig and eight photoetched masks are used in fabricating the circuit. Fabrication of TFT circuits is discussed in more detail in another paper.[7] Following the initial deposition of the cadmium sulfide, the entire scan-

Fig. 2—Simplified shift-register circuit suitable for driving the address strips af a salid-stage image panel. Insulated-gate field-effect transistars are used as the active element.

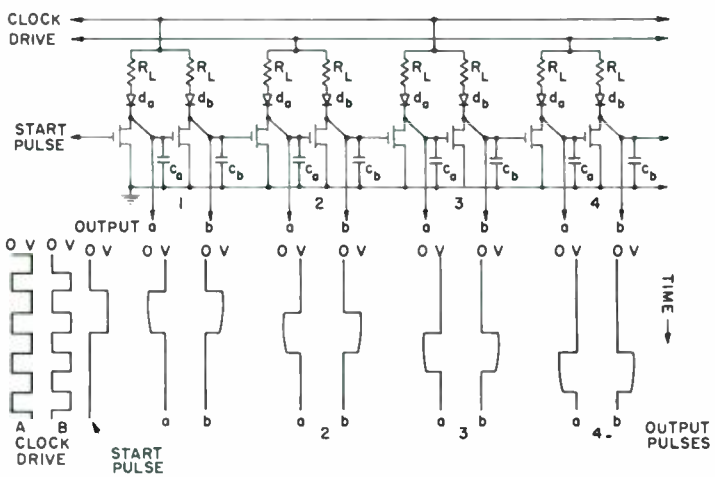
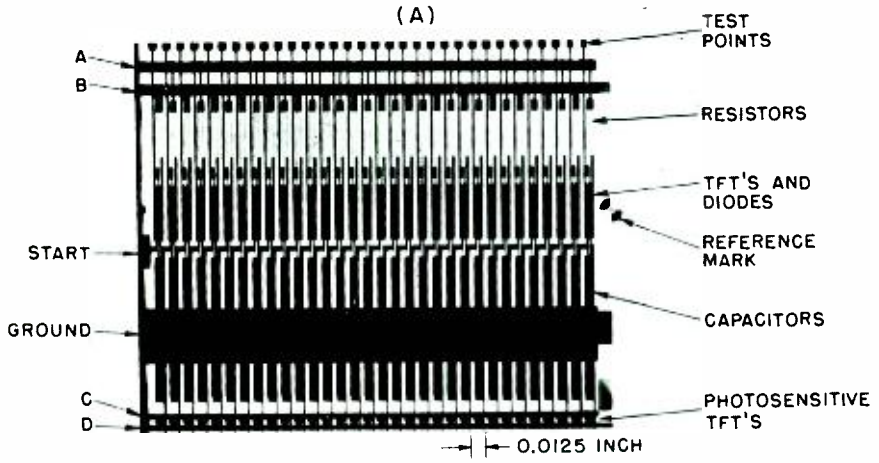


Fig. 3—Photograph of a completely integrated 30-element thin-film scan generator based upon the circuit of Fig. 2.



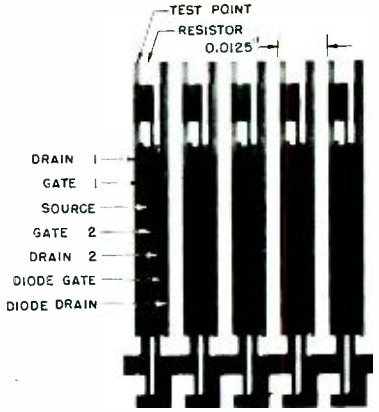


Fig. 4—An enlarged view of a portion of the thin-film scan generator showing the TFT's and field effect diodes for five stages.

ner is deposited in seven steps during one evacuation of the system.

For operation of the image scanner only five leads are required: two for the clock drives, and one each for the start pulse, the ground lead and the video output. Tests were made, however, using 60 evaporated fan-out leads connected to the drain of each TFT, as shown in Fig. 5. The ends of these leads were attached to a printed circuit board which was plugged into the test equipment. Fig. 6 shows the drain characteristics of all 60 TFT's displayed on a transistor curve tracer. Good uniformity is observed from one unit to the next. The characteristics of the odd-numbered units are tipped up because of an alternate shunt path through the load resistors to ground. There is no difference in the performance of the odd and even numbered units.

The fan-out connections permit the voltage pulse appearing at each output terminal of the scanner to be displayed by an oscilloscope. Fig. 7 shows the resultant waveform at each of the thirty output terminals when a *start* pulse is applied to the input terminal of the first stage. The uniformity in timing and pulse heights is apparent. Fig. 8 shows similar waveforms at alternate output stages for another unit which had been operated for 150 hours. In driven operation, an external *start* pulse is applied to stage 1, while in cyclic operation the output of stage 30 is used to trigger stage 1. Three scan generators have been connected together to operate in cyclic fashion as a 90-stage ring counter. Scan generators have operated at clock frequencies ranging from 2 to 200 kc. Both higher and lower frequencies can be obtained with modified circuit parameters.

Many experimental scan generators were built in the laboratory having all 30 stages initially operable. Without encapsulation the generators usually became inoperative in a few hours. By covering the entire unit with an evacuated enclosure, the stability was greatly improved and several units were operated continuously for many hundreds of hours.

CONCLUSION

Laboratory models of the 30-stage scan generator are currently being used in research on image-sensor panels. The 30 output terminals of the generator can supply scanning pulses to a set of individual photocells or to an experimental evaporated array deposited upon a separate glass blank. Improved resolution in the image sensor will require scan generators having many more output stages which are spaced much closer together. A 200-stage generator with output strips spaced 0.0021 inches apart has been designed. A wire grill having 480 wires per inch will serve as the principal evaporation mask.[7] A future paper will describe the work on image sensors in greater detail.

Fig. 5—View of the 30-element thin-film scan generator showing the evaporated fan-out connections used for test purposes.

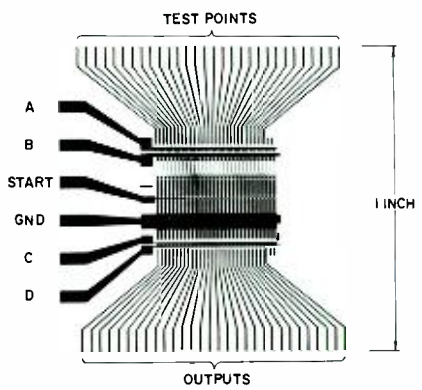


Fig. 6—Drain characteristics of the 60 TFT's incorporated into the 30-element thin-film scan generator.

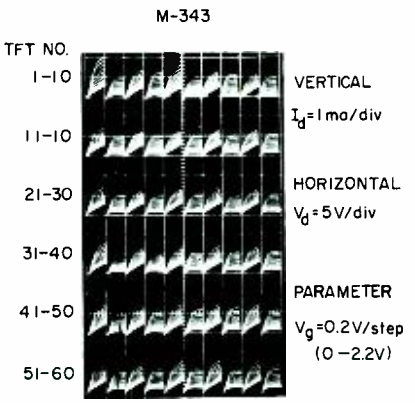
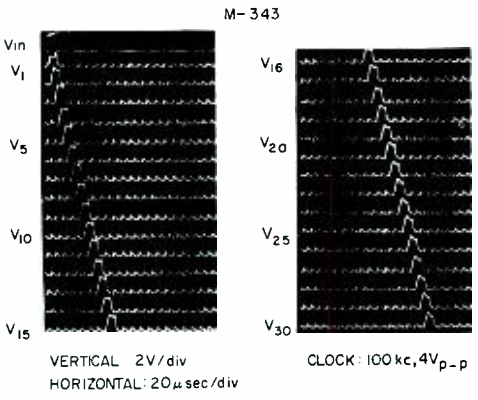


Fig. 7—Pulse waveforms observed at each of the 30 output strips of the thin-film scan generator. A start pulse is applied to the input of stage 1.



ACKNOWLEDGEMENTS

The writers wish to thank H. Johnson. J. T. Wallmark, and A. Waxman for helpful discussion. Many valuable contributions were made by H. P. Lambert in the construction of the thin-film scan generator. W. S. Homa, V. L. Frantz. and R. G. Pugliesi have contributed in the fabrication and testing of experimental TFT's.

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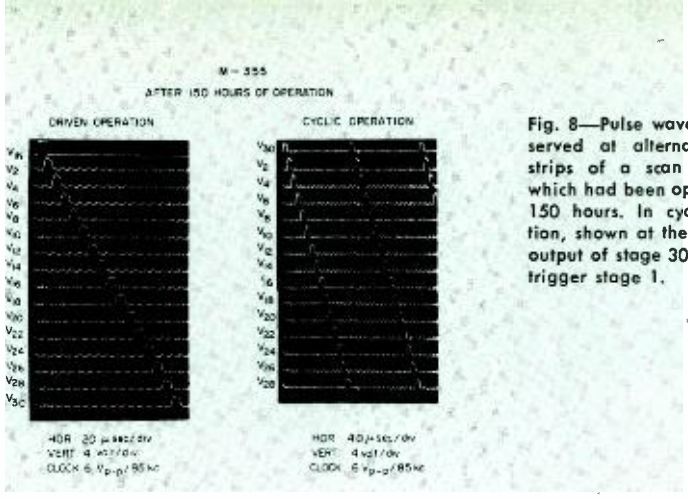

Fig. 8—Pulse waveforms observed at alternate output strips of a scan generator which had been operated for 150 hours. In cyclic operation, shown at the right, the output of stage 30 is used to trigger stage 1.

DR. PAUL K. WEIMER received his B.S. degree from Manchester College in 1936, his M.A. degree in physics from the University of Kansas in 1938, and his Ph.D. degree in physics from Ohio State University in 1942. From 1937 to 1939, he taught physics and mathematics at Tabor College, Hillsboro, Kansas. Since 1942 Dr. Weimer has been engaged in research at RCA Laboratories Division at Princeton, N. J. where he is a Fellow, Technical Staff. At RCA Laboratories he has participated in the basic development of various types of television pickup and display tubes, and more recently of the insulated-gate thin-film transistor. From 1959 to 1960, Dr. Weimer was granted an RCA fellowship for study abroad, which was spent as a research associate at the Laboratoire de Physique, Ecole Normale Superieure, Paris, France, working in the field of semiconductors. He was recipient of a Television Broadcasters' Award in 1946, the IRE Vladimir K. Zworykin Television Prize in 1959, an Outstanding Paper Award Plaque at the 1963 International Solid State Circuits Conference, and the RCA David Sarnoff Outstanding Achievement Award in Science in 1963. Dr. Weimer is a Fellow of the Institute of Radio Engineers, and a member of the American Physical Society.

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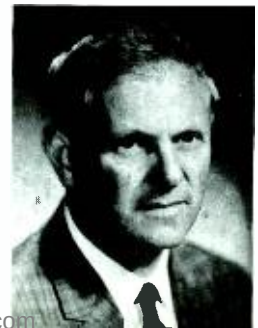
Dr. P. K. Weimer

H. Borkan

Dr. G. Sadasiv

L. Meray-Horvath



Dr. F. V. Shallcross

ENTIRELY THIN-FILM INTEGRATED CIRCUITS FOR SPACE APPLICATIONS

J. J. BOWE, Ldr.

Active Thin-Film Devices and Thin-Film Circuits
Defense Microelectronics
DEP, Somerville, N. J.

THIN-FILM techniques, used in integrated circuits for over 15 years, have been a fruitful area in miniaturization. But until recently, a major limitation on thin-film circuits has been the lack of an active thin-film device which could be incorporated into the thin-film circuit. Vacuum tubes and, later, transistors were added to the thin-film circuit to perform the function of the active device. In recent years a thin-film transistor (TFT) was invented by Dr. P. K. Weimer[1,2] at the RCA Laboratories. This TFT was the first of the long-awaited thin-film active devices which may be incorporated into integrated circuits.

Why should the active devices for integrated circuits be fabricated at the same time as the passive components? In the past (and continuing in hybrid integrated circuits) the active components, usually chip transistors (and diodes), are added to circuits of evaporated passive components. This process is an expensive, potentially unreliable procedure which impedes achieving two of the foremost goals of integrated electronics—*reliability* and *low cost*. The batch process of diffusion has avoided these problems for monolithic silicon integrated circuitry. The invention of the TFT has now made possible batch processing by evaporation of entirely thin-film circuits, including active and passive components. These circuits will cost less and will be more reliable than the hybrid type. Additionally, they are more resistant to radiation by orders of magnitude than the diffused silicon circuits.

The requirements for a satisfactory circuit for space applications include fabrication feasibility, reliability, small size, low-power usage, and insensitivity to radiation—*precisely the characteristics of thin-film circuits*. The small size is apparent from the dimensions of a typical amplifier circuit: 100 mils square. Low-power usage is a corollary of the small size. Since power of the order of milliwatts is all that can be dissipated in such a small volume without causing undue heating, low-power circuits are almost mandatory. The reliability of thin-film passive components has been time-tested and proven.

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THIN-FILM PASSIVE COMPONENTS

The advantages of evaporated passive components over their solid silicon diffused counterparts are well known. Fabrication of evaporated resistors is possible over a wider range of values because the range of resistivities achievable in thin-film structures is wider than is possible with diffused resistors. This feature permits practical fabrication of megohm film resistors in contrast to the limited values of, say, 50 kilohms, for diffused resistors. The capacitance associated with resistors also is much lower with the film resistor. Evaporated capacitors can be fabricated with a value of capacitance per unit area which is larger by a factor of two or three than the value which can be achieved with the capacitance associated with a diffused junction. When one additionally considers the very practical stacked film capacitor, the advantage becomes ten to one. The problems of leakage and crosstalk, of maintaining proper bias (or keeping junctions backbiased) and of keeping interelectrode capacitances small are much reduced or eliminated entirely.

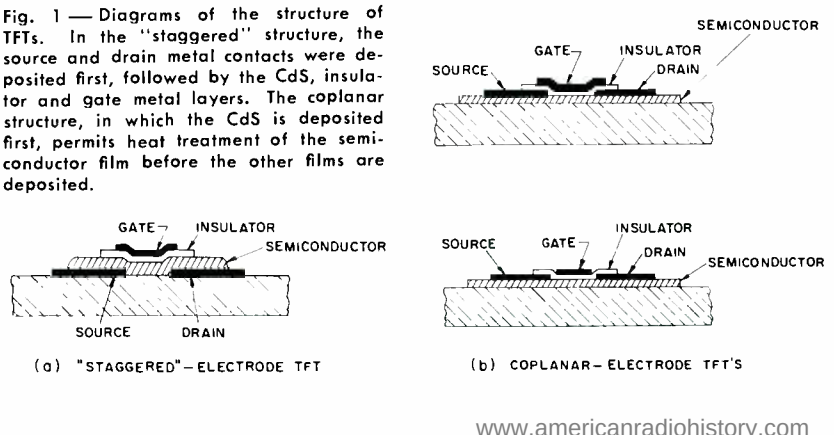


Fig. 1 — Diagrams of the structure of TFTs. In the "staggered" structure, the source and drain metal contacts were deposited first, followed by the CdS, insulator and gate metal layers. The coplanar structure, in which the CdS is deposited first, permits heat treatment of the semiconductor film before the other films are deposited.

THIN-FILM ACTIVE DEVICES

Various hybrid models previously have been devised to incorporate active semiconductor components onto, or into, a substrate with evaporated thin-film *passive* components. But, with the advent of the cadmium sulfide TFT, the necessity for awkward, expensive hybridization has been removed. It is now possible to evaporate entire circuits in place. Solid-state triodes, prepared by evaporation of all parts, will play the same significant role in thin-film integrated circuity that diffused transistors play in the diffused monolithic silicon integrated circuitry.

The Integrated Electronics group of Applied Research, DEP Camden, has conducted a program of research and development to exploit the evaporated cadmium sulfide TFT in integrated circuits, a program now being continued at DEP Defense Microelectronics, a new group recently established in Somerville, N. J. Recent advances in technology have made it possible to evaporate CdS unipolar (or, more precisely, *insulated-gate field-effect*) transistors and their associated passive circuit components. All the materials deposited are wide-gap semiconductors, insulators, or metals deposited on glass, ceramic, or other suitable substrate.

A typical structure for the device consists of an evaporated film of cadmium sulfide (the semiconductor) deposited over source and drain metal contacts evaporated on a suitable substrate. The evaporation of an insulating film and of a metal gate complete the transistor (Fig. 1); the triode has then the structure of a field-effect transistor. The analysis of the TFT follows that of Shockley[3,4] for the general field-effect transistor.

The TFT has a volt-ampere characteristic similar to that of a vacuum-tube pentode, has a high input impedance (gate-to-source), and a high output impedance (drain-to-source). A typical set of characteristics is shown in Fig. 2.

The evaporated TFT exhibits excellent electrical characteristics. Typical values of small-signal characteristics are:

Transconductance, g_m: 5,000 to 10,000 μmhos
Output resistance, R_o: 10 kilohms
Input resistance, R_i: 10 megohms
Gate capacitance, C_g: 35 picofarads
Gain, μ: > 30

The TFT, with evaporated cadmium sulfide as the semiconductor, has been fabricated and investigated in a variety of device geometries, circuit topologies, and configurations. The two main categories of TFT's are the earlier *staggered* geometry and the more recent *coplanar* type[5] (Fig. 1).

The staggered type is fabricated by laying down metallic (gold) source and

drain contacts on a glass substrate, evaporating cadmium sulfide, followed by an insulating layer (SiO or CaF_2) and then a metallic gate contact. The coplanar type is fabricated by evaporation, the cadmium sulfide first on the substrate, then the source-drain, insulator, and gate. The coplanar structure permits processing of the evaporated cadmium sulfide semiconductor layer alone, without the metallic or insulator films.

EXAMPLE OF A COMPLETE THIN-FILM CIRCUIT—ANALOG AMPLIFIER

The TFT has been incorporated into a variety of thin-film circuits. Among the functions are *and* gates, *or* gates, flip-flops, pulse amplifiers and audio amplifiers. The pulse amplifiers exhibited rise times of less than 1 μsec; the audio amplifiers showed gains of 20 and bandwidths of 40 kc. Circuit diagrams for some of the configurations are shown in Fig. 3.

As a typical example of an entirely thin-film integrated circuit, consider an analog amplifier circuit (Fig. 4). Topological design of the circuit is shown in Fig. 5. This circuit was designed around a TFT with the following characteristics at a 4.5-volt, 2-mamp operating point (subscript *gs*, gate-to-source; *gd*, gate-to-drain):

Transconductance, g_m: $\geq$ 2,000 μmhos
Output resistance, R_o: 25 kilohms
Capacitances, C_{gs}, C_{gd}: $\geq$ 20 picofarads
Resistances, R_{gs}, R_{gd}: $\geq$ 5 megohms

A Kovar 7056 glass, 0.1 × 0.1 × 0.04 inch, is used for the substrate. The cadmium sulfide film is deposited as the first layer through a stainless steel mask onto the substrate mounted on an aluminum plate. The substrate holder contains a nichrome-wire-wound heating coil and a thermocouple terminal to monitor the substrate temperature, which is held at 165°C. A control glass 1 square centimeter in area is also attached to the holder for optically monitoring the thickness of the film. The cadmium sulfide is evaporated out of an alumina-coated molybdenum crucible at a throw distance of 3.5 inches from the substrate. The evaporation rate is approximately 25 angstroms per second at a vacuum pressure of 5×10^{-5} torr. As soon as the deposition of the cadmium sulfide has been completed and an optical film thickness of six quarter-wavelengths of green light has been achieved, the vacuum is broken, and the sample is then placed in an oven for baking. The sample is processed further with the deposition of aluminum source and drain film contacts. This deposition is achieved by the evaporation of aluminum from a tungsten source. The gap is formed by a thin (0.3-mil-diameter) etched tungsten wire. In order to avoid possible contact difficulties due to oxidation of the aluminum film, gold tabs are deposited prior to the aluminum evaporation. Silicon monoxide evaporated from a molybdenum boat (or calcium fluoride from an alumina-coated molybdenum crucible) is used to produce an insulating film about 700 angstroms thick. Aluminum is again evaporated from a tungsten boat to deposit a gate film 1,000 angstroms thick. During all these evaporations, the pressure is held at 5×10^{-5} torr or lower. Resistors of nichrome are evaporated, and stacked aluminum and SiO layers are deposited to form capacitors.

All masking patterns are photoetched into one mask, which is manipulated over the substrate. This method permits achieving the very tight positional tolerances required for such thin-film circuits.

A photograph of the completed TFT circuit is shown in Fig. 6. This is mounted on a 12-lead TO-5 header (Fig. 7), capped and sealed. The size of the substrate was chosen to fit the TO-5 header. TO-5 headers with 12 leads are commercially available. Thermocompression-bonded or ultrasonic-bonded connections of 1-mil gold wire are made to evaporated tabs and to the header pins.

The expression for gate capacitance is:

$$C_g = \frac{KWL}{t}$$

Where: K is the dielectric constant, W is the width of the gate, L is the length of the gate, and t is the thickness of the dielectric film (the gate insulation). For TFT's under consideration, typical values are $K = 11.6$, $W = 200$ microns, $L = 7$ microns, and $t = 750$ angstroms, yielding a theoretical value of C_g as approximately 20 picofarads; measured values of C_g are of this order.

The expression for transconductance g_m is:

$$g_m = \frac{KW\mu_d V_d}{tL}$$

Assuming $\mu_d \sim 10$ cm²/volt-sec and taking $V_d = 5$ volts, values of $g_m \sim$ 3,000 μmho are obtained. Measured values of g_m in TFT's of acceptable quality range from 3,000 to 12,000 μmho. From these equations, it is seen that the expression for the gain-bandwidth product is:

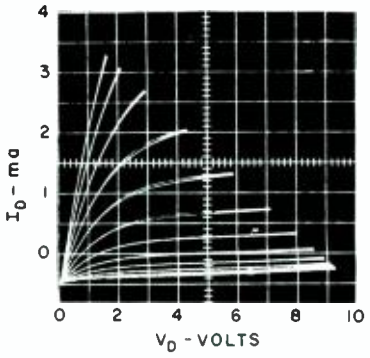
$$GB = \frac{g_m}{2\pi C_g} = \frac{\mu_d V_d}{2\pi L}$$

The amplifier circuit has been designed and constructed so that there is a choice of source and drain resistors. Depending on the choice, the circuit can be used as a high-gain audio amplifier or a low-gain video amplifier. For operation as an audio amplifier, terminals *1-2-3-5-8* (Fig. 4) are used, while for operation as a video amplifier, terminals *1-2-4-5-7* are used. This arrangement yields circuits with the following characteristics:

	Gain	Bandwidth
Audio amplifier:	14	150 cycles to 500 kc
Video amplifier:	2	150 cycles to 5 Mc

Fig. 8 shows input and output characteristics of the amplifier.

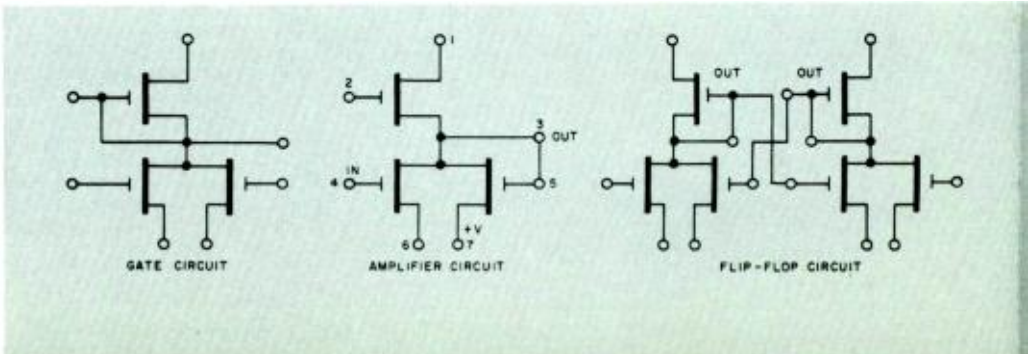
The characteristics above assume the amplifier is driving a high-impedance load and is driven from a low-impedance source. By choosing other combinations of load and source resistance, the gain and bandwidth can be tailored to meet other requirements. The performance of the amplifier, of course, is improved as the characteristics of the TFT are improved above the values stated above.



V_G: 0 TO +6 VOLTS IN 0.5 VOLT STEPS

Fig. 2 — A typical set of TFT volt-ampere output characteristics.

Fig. 3—Circuits formed by DC connecting pins and gates, showing the versatility of a simple three-triode structure used as a gating circuit, an amplifier circuit and a flip-flop.



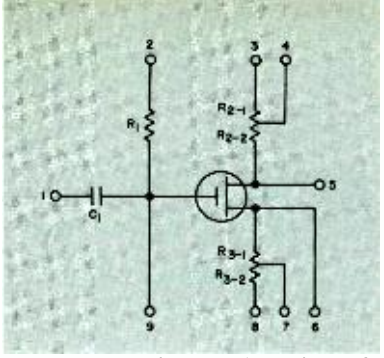


Fig. 4 — Integrated amplifier circuit. Note the range of values of resistance (100 ohms to 1 megohm) and the large value of capacitance (1000 pf) achievable with thin films, which cannot be accomplished with silicon integrated circuitry.

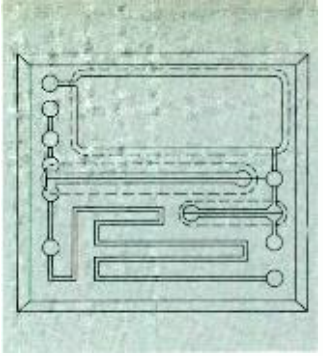


Fig. 5 — Topological layout of integrated amplifier. The large area at the upper right is the capacitor (stacked four times). The meandering lines are resistors. The central area enclosed by the dashed lines in the TFT, and the smaller dashed area is the 1-megohm resistor.

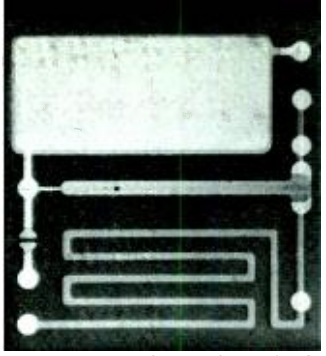


Fig. 6 — Thin-film amplifier circuit. Entire substrate is 1/100 sq. in., of the same order as a silicon integrated circuit. Meandering line (resistor) is 2.5 mils wide. Square substrate is 0.1-in. on a side. The white rectangle is a capacitor, 36 mils x 80 mils.

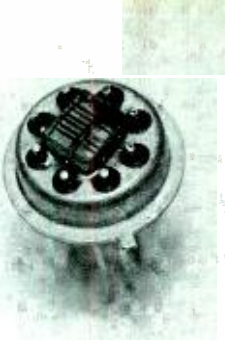


Fig. 7 — Integrated thin-film circuit on TO-5 header. The small size of the substrate (0.1-in. on a side) permits the circuit to be packaged in a TO-5 can.

SMALL RADIATION EFFECTS ON THIN-FILM TRANSISTORS

Of significance for space applications is the fact that the TFT operates with a polycrystalline cadmium-sulfide film. It is known that passive thin-film components are less affected by radiation by orders of magnitude over the diffused silicon type of integrated circuit in which the resistors and capacitances are junction-dependent. For example, junctions deteriorate under 10^{12} to 10^{14} integrated neutron flux densities, for example. Single-crystal silicon transistors suffer likewise. Since polycrystalline structure initially contains many lattice vacancies and other structural defects, it is deteriorated less than the single-crystal structures by the introduction of such structural disorders by radiation.

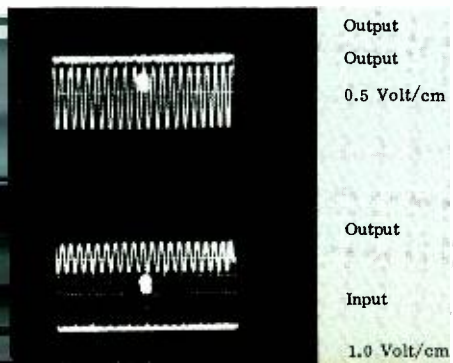
Recent tests at the RCA Laboratories, Princeton, show that thin-film circuits can withstand integrated flux densities of 10^{15} neutrons, and there are indications that an order of magnitude higher can be achieved.

FUTURE OF THE THIN-FILM TRANSISTOR

Much work remains to be done on the TFT but its significance is clear at this stage.

One of the obstacles to large-scale fabrication is that of achieving a space of 0.3-mil or less in an evaporation mask. Two techniques to accomplish this spacing are used at present. In one technique, a wire of appropriate diameter—a 0.3-mil etched tungsten wire, for example—is used as a mask. In another technique, a mask is displaced the appropriate distance and a second evaporation of the metal source or drain is made. Photoresist techniques are very desirable here, but there are problems of contamination of the cadmium sulfide transistor and of obtaining an etch good enough to etch the photo mask, but not the underlying cadmium sulfide. One can think of evaporating, say, for example, an SiO layer which could be etched, but there remains the problem of etching the oxide mask without disturbing the underlying semiconductor, a situation which is not a problem in silicon circuits. Work of this nature is being pursued at Defense Microelectronics, Somerville, N. J. Thin-film transistors of other materials are also being investigated. Good units have been fabricated at the RCA Laboratories from cadmium-selenide,[6] for example. Work is progressing on silicon TFT's.

Fig. 8 — Input and output characteristics of the thin-film amplifier, showing the effectiveness of the circuit in the range from a few cycles per second to megacycles per second.



CONCLUSIONS

The invention of the TFT is of great significance to integrated circuits. The feasibility of fabrication of miniature evaporated circuits, incorporating cadmium sulfide TFT's has been demonstrated. Such circuits exhibit the characteristics required of space hardware: they are small and reliable, have low-power requirements, and are versatile in that wide ranges of values of passive components are achievable with close tolerance.

Problems, however, remain with the TFT. Chief among these is the problem of life. Present times to failure can be improved; programs to this end are under way. Work to move the TFT to its final goals must continue. The TFT is the reliable, inexpensive active component in integrated circuits for future space vehicles.

ACKNOWLEDGMENT

The author acknowledges his indebtedness to Dr. P. K. Weimer and his colleagues, to Dr. W. Laznovsky, and to G. J. Dusheck and E. L. Snyder.

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J. J. BOWE received the AB degree in mathematics in 1947 and the MA degree in applied mathematics from Brown University in 1949. After a year of teaching physics at the University of Bridgeport, Mr. Bowe joined the Air Force Cambridge Research Center where he became chief of the Devices Research Unit, directing research on negative resistance diodes, transistor techniques, and microelectronics. In 1959 Mr. Bowe organized and headed the R&D Department (Microelectronics) at Sperry Semiconductor. In 1962 Mr. Bowe joined RCA in the DEP Applied Research activity in Camden as Engineering Leader in integrated circuits, directing work on cadmium-sulfide thin-film transistor circuits and solid silicon circuitry. In 1963 he was transferred to the newly established Defense Microelectronics activity in Somerville, N. J., to work in the thin-film laboratory. Mr. Bowe has published several papers on solid-state devices and was a contributor to Electronics Encyclopedia. He is a member of the APS, IEEE, and is listed in "American Men of Science."

MOS INTEGRATED LOGIC NETWORKS

Most digital data-processing systems utilize only a few basic circuit building blocks to achieve a required system function. It is natural, therefore, that digital systems readily should lend themselves to highly ordered, repetitive, fabrication techniques. Realization of such mechanized fabrication within the framework of the new integrated-circuit technology is the goal of the "Integrated-Logic-Network" (ILN) concept.

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A. KARL RAPP received his BSEE from Drexel Institute of Technology in 1954 and his MA degree in Applied Physics from Harvard University in 1955. He was employed by the Philco Corporation as a cooperative student engineer in intervals during the period 1950-1954. In 1955 he joined the research Division of Philco Corporation where he worked in the field of solid-state circuits. Concentrating primarily on digital circuits, he investigated high-speed logic and memory techniques utilizing semiconductor and magnetic devices. In 1963, Mr. Rapp joined the Electronic Research Laboratory of RCA Laboratories. He is currently investigating integrated digital circuits utilizing field-effect transistors. He is a member of IEEE, Phi Kappa Phi, Eta Kappa Nu, and Tau Beta Pi.

THE ILN thesis is that data-processing systems can advantageously be fabricated as arrays of many identical elements with superimposed connections. The resulting advantages over systems employing conventional components include:

1.) *increased reliability*—because fewer mechanical (welded or soldered) connections are needed.
2.) *reduced size*—because of the reduced number of sub-system packages and their interconnections.
3.) *lower cost*—because of fabrication simplicity and batch interconnections.
4.) *reduced power dissipation*—due to a unique complementary circuit made possible by the MOS transistor.

The MOS transistor is eminently suited to serve as the basic element of ILN arrays. Not only can it be fabricated in large arrays with high yields, but it can serve as the sole component of digital circuits—filling the role of both active and passive components. Circuit wiring connections can be made by techniques which are completely compatible with the diffusion and evaporation procedures used for the transistor's fabrication.

Details of the fabrication procedure and properties of the MOS transistor are given in other papers[1]; however, it may be helpful to review briefly the device properties and terminology pertinent to integrated circuits.

An MOS transistor (Fig. 1) fundamentally comprises a semiconductor *channel* and a *gate* electrode which controls the channel conductance. The channel is defined by diffusing two highly doped n-type regions into a p-type silicon wafer. (Alternatively, p-type regions can be diffused into an n-type substrate, thus producing the complementary-polarity transistor.) The channel, the narrow surface layer between the two highly doped regions, then is insulated by thermally grown silicon dioxide. Finally, the gate electrode and contacts to the doped regions are vacuum-deposited.

In operation, a potential applied between one of the doped regions (the *source*) and the gate electrode creates an electric field which either increases or decreases the number of mobile charge carriers in the channel, depending on the field polarity. In this way, the gate-to-source voltage can be used to control the resistance between the source and *drain* (the other doped region).

According to application, two different types of MOS transistors can be defined. If the channel is doped slightly n-type, source-drain conduction exists with zero gate-source voltage. Negative

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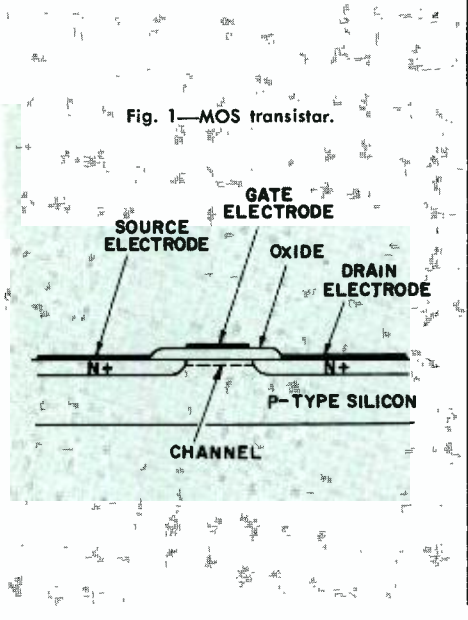
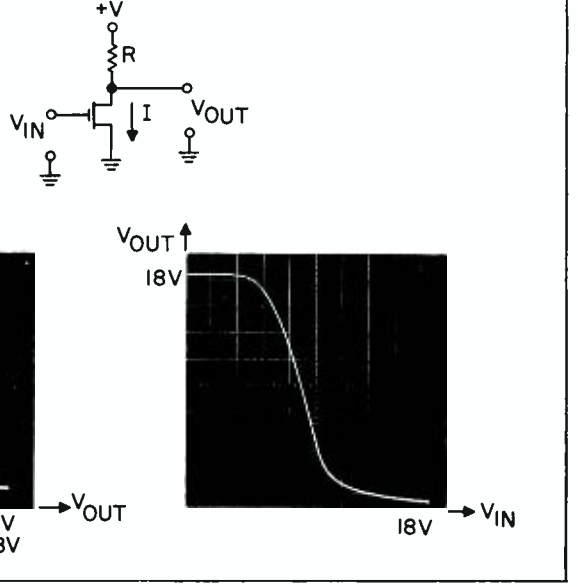
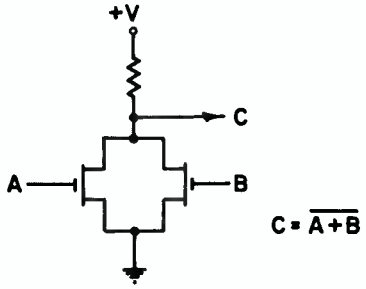


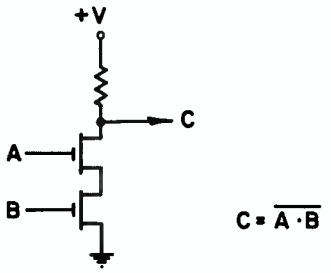
Fig. 1—MOS transistar.

Fig. 2—Basic inverter stage.





(a) NOR GATE



(b) NAND GATE

Fig. 3—Basic gates.

voltage on the gate then depletes the channel of electrons, reducing its conductance. Positive voltage enriches the channel charge, thereby increasing the conductance. This type of behavior characterizes a *depletion* transistor. If, on the other hand, the channel is intrinsic or slightly p-type, then no drain-source conduction can occur until the gate is driven positive. This *enhancement* (or induced-channel) transistor is the more useful type for constructing logic circuits.

LOGIC CIRCUITS

A basic MOS-transistor switch (or logical inverter) is illustrated in Fig. 2. The transistor is designed to have a delayed-conduction threshold of several volts; i.e., several volts must be applied between gate and source electrodes before any appreciable drain current can flow. This threshold and the load resistor R are chosen to provide an output signal swing which brackets the input swing, to permit the direct coupling of logic stages.

The *nor* and *nand* functions can readily be implemented, as Fig. 3 illustrates. Assemblies of these basic circuits then can form other logic functions, such as the shift-register stage of Fig. 4.

INTEGRATION

Integrated arrays of transistors are conveniently fabricated by forming the transistors in continuous ladder-like patterns, as illustrated in Fig. 5. Because the transistors are completely symmetrical, each small diffused region can serve as either source or drain. The number of wired circuit connections is reduced because of the series connections inherent in this ladder-type of structure. To isolate two sections of a ladder, it is necessary only to ground a source-drain or gate electrode between them.

Fig. 6 shows an integrated circuit fabricated from this type of ladder array—a 16-transistor logic block. Fig. 7 illustrates a transistor array with the superimposed connections required to produce groups of these logic blocks.

Although such circuit *intra*connections (connections between elements on the same semiconductor wafer) can readily be evaporated onto an array, means also must be available for *inter*connecting wafers to one another and to other non-integrated parts of a system. A successful method (Fig. 8) uses a temporary bridge as a base for evaporating a ribbon lead. Dissolution of the bridge then leaves the ribbon free to flex and follow thermal expansions and contractions. Utilizing this bridging technique, the logic block of Fig. 6 has been packaged in a ceramic container (Fig. 9); the necessary load resistors were fabricated as part of the ceramic package.

The integration of larger, more complex circuits introduces the requirement for intraconnection crossovers. Such crossovers can conveniently be provided by using two layers of wiring, separated by a layer of insulation. The first layer consists of "fingers" extending from each source-drain region and gate (Fig. 10a). Strips of insulation then are evaporated, covering all but the tips of the fingers (Fig. 10b). Finally, the second layer of wiring is evaporated onto the insulation, extending onto the finger tips where contact is to be made (Fig. 10c). A photograph of an array of MOS transistors intraconnected by this technique is illustrated in Fig. 11.

INTEGRATED DIVIDE-BY-N COUNTER

An example which demonstrates the design of a rather complex integrated system employing evaporated crossovers is the *divide-by-N* counter developed for use in a communication equipment. (Because the requirements of the com-

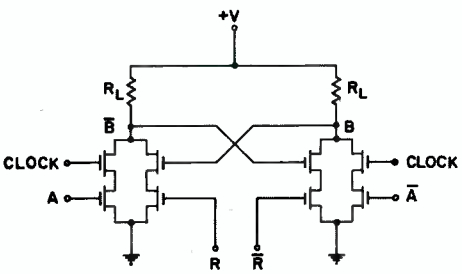


Fig. 4—Shift-register stage.

Fig. 5—Transistor array.

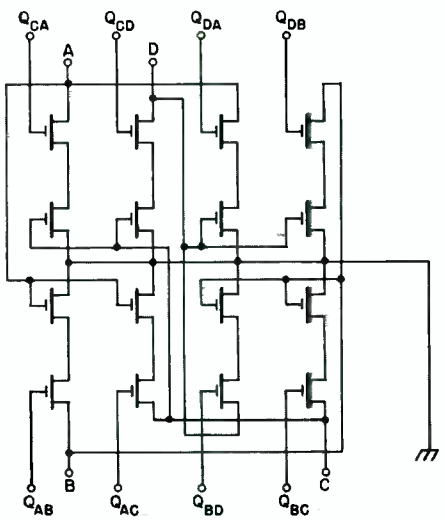


Fig. 6—Integrated 16-transistor logic block.

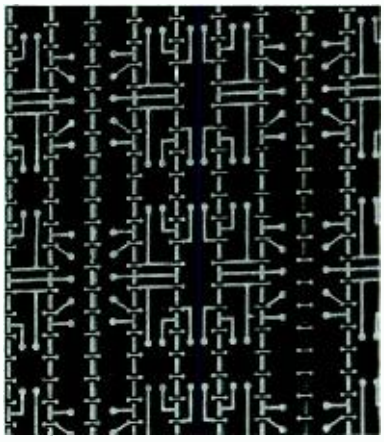


Fig. 7—Transistor array with superimposed connections to produce groups of logic blocks of Fig. 6.

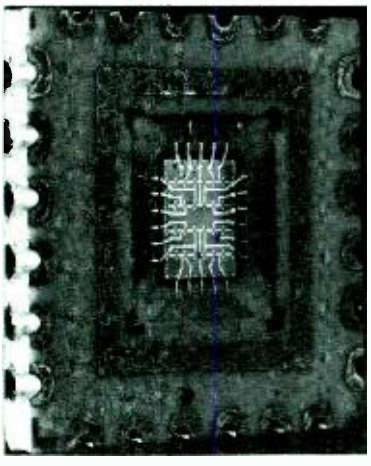
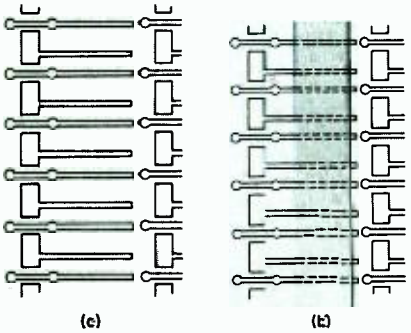


Fig. 9—Ceramic packaging of Fig. 6 logic block using Fig. 8 bridging technique



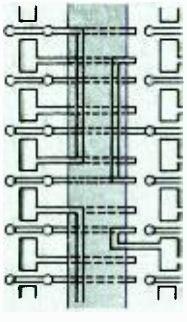


Fig. 10—Circuit intraconnections.

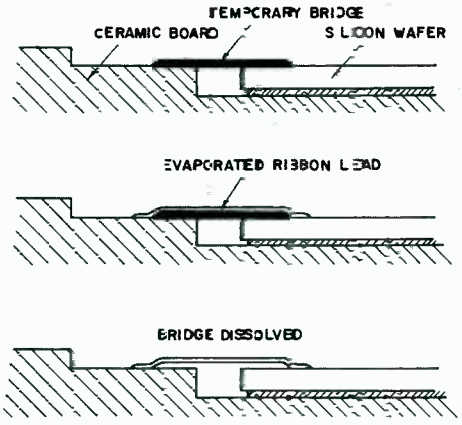


Fig. 8—Bridge technique.

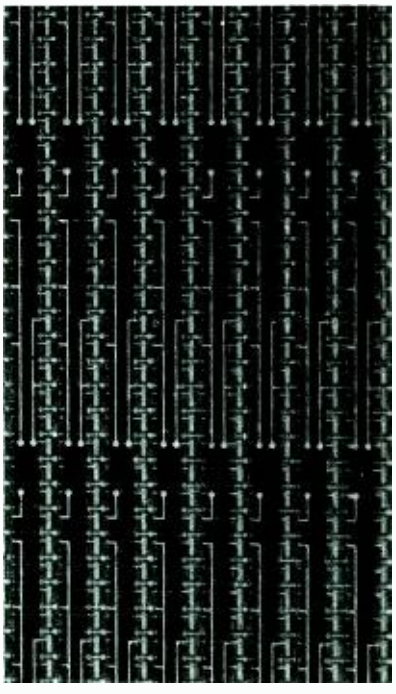
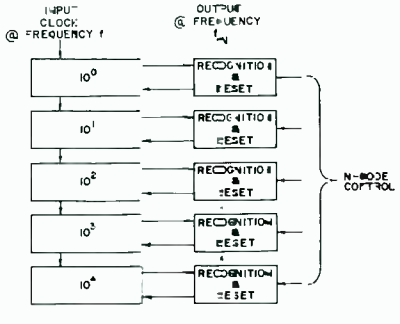


Fig. 11—Photomicrograph of an MOS array intraconnected by Fig. 10 technique.

Fig. 12—Divide-by-N counter.



munication system were changed during the development, the counter never was completely fabricated.)

A *divide-by-N* counter is a vital system component of digital frequency synthesizers, equipments used for the generation of a large range of precisely controlled frequencies. To perform its function, the counter must have exactly N distinct states through which it cycles automatically and repetitively. The value of N is selectable; typically, N ranges over tens of thousands of values, each corresponding to one output frequency of the synthesizer. A divide-by-N counter thus is similar in complexity to the arithmetic unit of a small digital computer.

The counter was designed to have five identical decimal decks (Fig. 12), each representing one digit of the divide ratio N. Each deck contained 134 MOS transistors and 50 load elements. It was planned that each deck be fabricated on three wafers, two wafers to contain the transistors and one, the load elements. Fig. 13 illustrates the topological design for one of these transistor wafers. To obtain additional crossover flexibility for this design, the gates on alternate columns of transistors were staggered and the fingers extended out both sides of each column. The fingers of successive columns thus interleave. Only fingers actually used for connections are indicated in the diagram.

NONLINEAR LOAD ELEMENTS

Although the load resistors have been indicated in the preceding circuit diagrams as conventional, linear resistors, it was planned that the *divide-by-N* counter utilize depletion-type MOS transistors for loads. By connecting the gate terminal of each load transistor to its source, a nonlinear, but still passive, load element is obtained. (Fig. 14)

Several advantages accrue from the use of this type of load element. First, the same technology used to fabricate the active elements also can be used for the load elements. The resulting simplification in fabrication processes aids uniformity and thus increases yields. Second, the circuit stability and switching speed are increased.

FUTURE TRENDS IN INTEGRATED LOGIC NETWORKS

Complementary MOS-transistor circuits are unquestionably the most exciting, most promising development anticipated for ILN's. The complementary circuit configuration results in an active load element. an element whose resistance changes advantageously as the stage switches. The basic complementary inverter stage and the effective load line

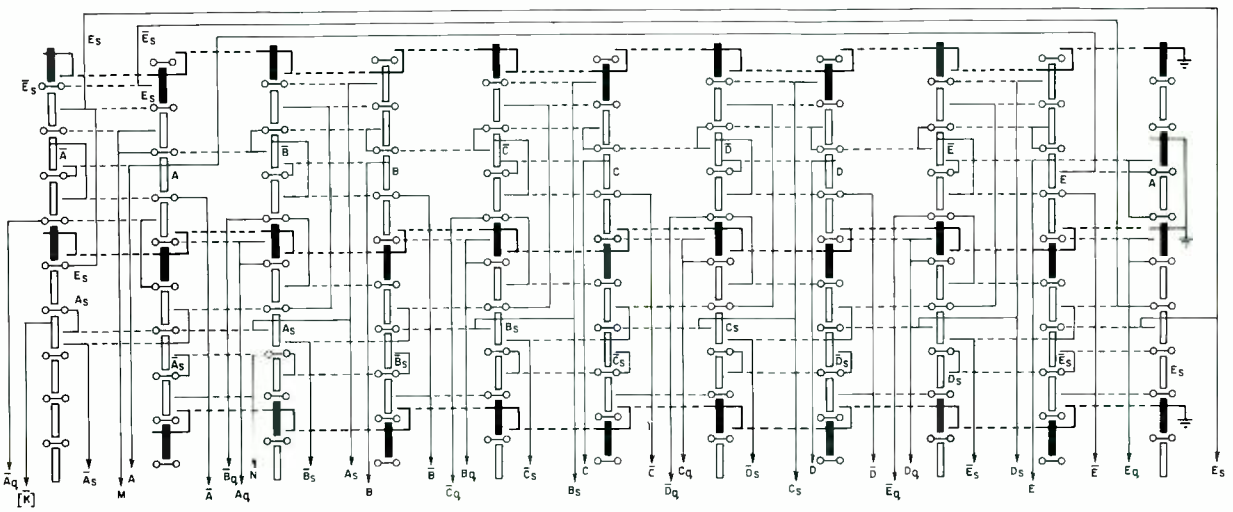


Fig. 13—Transistor wafer topology for *divide-by-N* counter. (Slave flip-flop denoted by subscript *s*, rather than lower-case letters; that is, $A_s \equiv a$, $B_s \equiv b$, etc.)

produced by the complementary-transistor load are shown in Fig. 15. The complementary circuit provides the remarkable advantage of dissipating essentially zero power in either the *on* or *off* state, even while controlling subsequent stages. Appreciable dissipation occurs only during a switching transient. In addition, even greater circuit stability and switching speed is obtained than is produced by the inactive, depletion-transistor load. Analysis has indicated that a complementary MOS switch is about 2.5 times as fast as a switch with a resistor load, for typical load-currents and logic gains. A depletion-transistor load, for comparison, produces about 1.5 times the speed of a resistor load.

In general, the trend is toward the fabrication of flexible, general-purpose transistor arrays, upon which a wiring pattern later can be evaporated for a specific application. Alternatively, it may prove desirable to utilize expendable intraconnection planes which later can be disposed of without sacrificing the basic array. Still greater flexibility might be achieved by controlling the function of various portions of arrays by non-electrical, external controls, e.g., light beams.

Flexible or not, MOS integrated logic nets should endow digital systems of the future with significantly improved reliability and economy—of dollars, watts, and cubic inches.

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Fig. 14—Load elements.

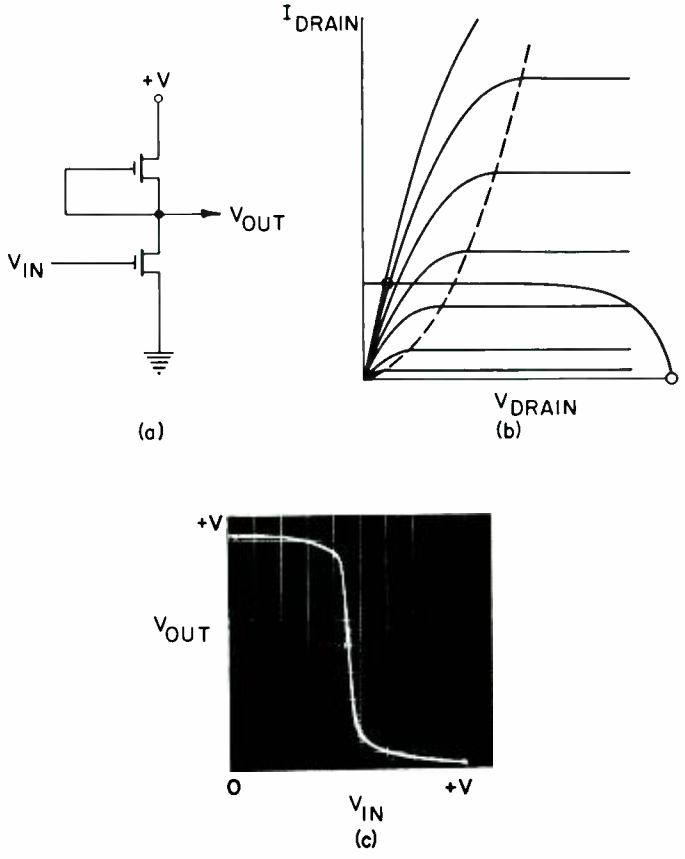
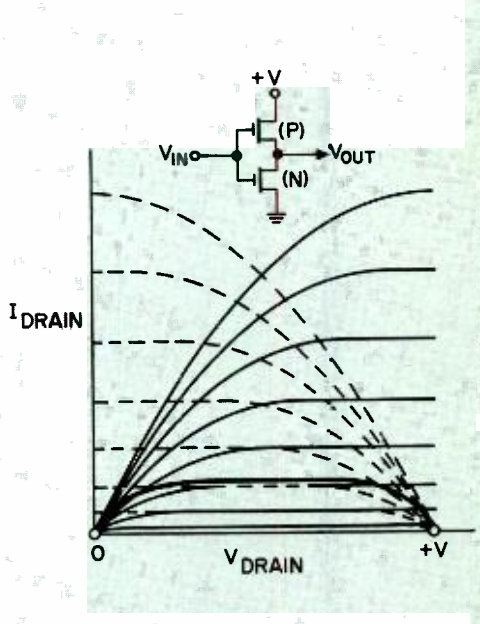


Fig. 15—Complementary gate.



PHOTOCOMPOSITION MACHINE FOR THE CHINESE LANGUAGE

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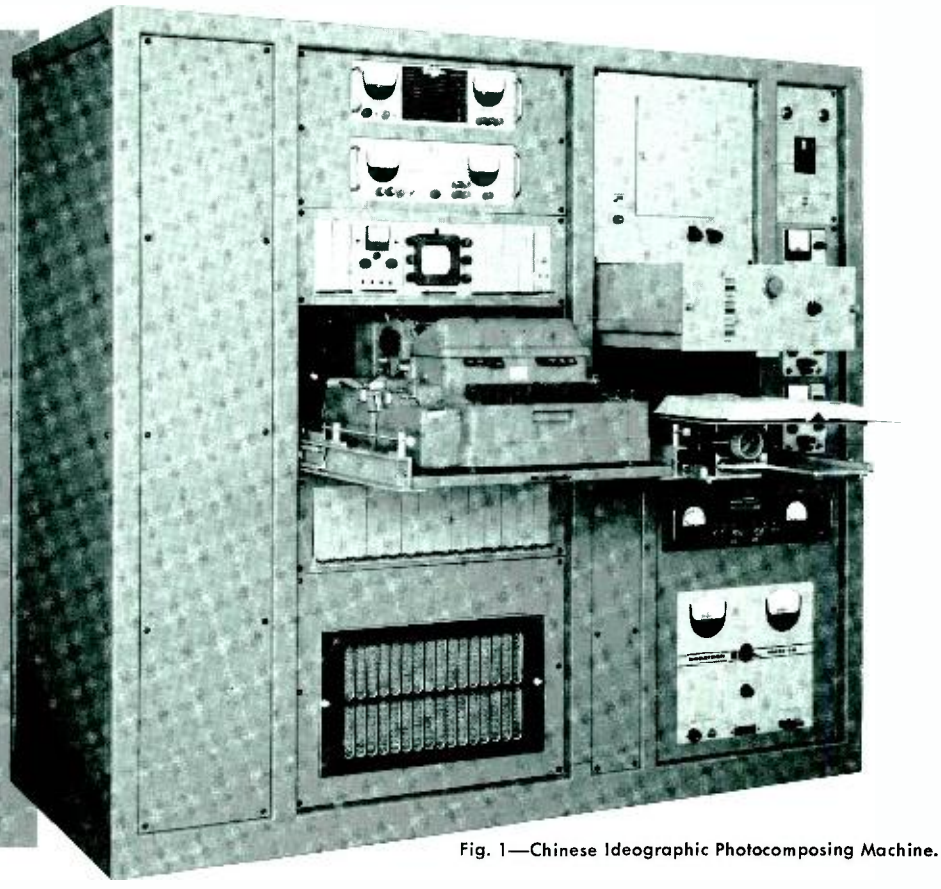


Fig. 1—Chinese Ideographic Photocomposing Machine.

The Ideographic Composing Machine (ICM) shown in Fig. 1 provides a means of rapidly composing high-quality Chinese ideographic characters in page format to be used as printing copy. Conventional techniques for printing Chinese are presently limited to manually selecting characters from large storage bins and assembling the selected characters in page format to produce printing plates. This technique is cumbersome and slow when considering the large selection of characters and the duplication of these characters in multiple font sizes. To circumvent this hand operation, the ICM was designed to photocompose Chinese characters directly from a keyboard input at rates comparable to those achieved from a conventional English typewriter, but without excessive operator training.

CHINESE characters, in general quite complex in structure. are difficult to construct directly. Observing an individual writing Chinese reveals that only a small number of basic brush strokes are assembled to form an ideographic character. However, within the area occupied by the character, a given stroke can appear almost anywhere with wide variety in its dimensions and location (Fig. 2). This complex structure precludes composition of Chinese characters by conventional mechanical keyboard techniques. Thus, successful composition of the Chinese language can be achieved only by maintaining a storage bank of complete Chinese characters which can be selected as needed by an operator. The ICM (Fig. 1) stores complete ideographic characters on photographic masks.

Final manuscript received June 24, 1964

CHINESE LANGUAGE CHARACTERISTICS

Study of the Chinese language has revealed that it does have an "alphabet" in the sense that all Chinese characters are written by selecting strokes from a relatively small number (21) of basic strokes. In addition, these characters are written in a definite sequence of strokes, providing building blocks to form the entire character. Studies also have shown that the Chinese, regardless of their speaking dialect or geographic location, seldom deviate from this set sequence of strokes in writing characters. The design of the ICM, therefore, takes advantage of the existence of strokes and their unique sequence in character formation to provide a system for composing Chinese ideographs from a keyboard. The ICM can be operated by anyone who can write Chinese by "typing" strokes in the same sequence used in writing.

Fig. 3 shows the sequence followed in composing a Chinese character from a number of strokes. The operator begins operation by depressing the stroke keys on the input-writer keyboard. When the input from the keyboard is sufficient to define a specific character, logic circuitry within the ICM recognizes the desired character, addresses the photographic mask, and optically and electronically positions the character for photography and composition. The input-writer keyboard of the ICM is shown in Fig. 4. It contains keys for 21 basic strokes, 11 punctuation marks, and 20 entities. The entities are a number of groups of strokes that occur very frequently in the spelling of characters, somewhat similar to English syllables such as *-ing*, *-tion*, or *-ous*.

SYSTEM DESCRIPTION

A simplified block diagram of the ICM is shown in Fig 5. A Chinese character is spelled out on the keyboard in the normal stroking sequence of the Chinese language. A given character may be composed of as many as 20 strokes. Each stroked key generates a 5-bit digital character code giving a maximum of 100 bits per character code. The code is fed to shift registers and then to a coincidence detector. A magnetic drum with 115 tracks and provisions for storing up to 10,000 character codes is continuously read back at a rate of 10 revolutions per second. Each character code on the

drum is sequentially fed to the coincidence detector. At the coincidence detector, a comparison is made between the code generated from the keyboard and each code from the drum. When coincidence occurs between a keyboard stroked character and a character stored on the drum, a signal is generated. In addition, the drum generates a clock track coincident with the character stations on the drum. This clock track is fed to a synchronous counter. When coincidence is indicated, the count in the counter is gated into a storage register. The position of the character on the mask is then identified through suitable digital-to-digital converters.

The equipment has the capability of handling 10,000 characters. These characters are located on three separate masks in the optical system. Each mask is divided into groups of 16 characters (Fig. 6). Each group of 16 characters is illuminated when a lamp placed behind it is energized. The code from the digital-to-digital converter energizes the lamp that will illuminate the block containing the desired character. After passing through a beam splitter and the lens system, the block of 16 characters is imaged at the input to the optical tunnel. At the output of the tunnel, a vidicon faceplate is illuminated with these 16 characters. The digital-to-digital converter also controls the vertical and horizontal deflection of the vidicon in such a way that the vidicon scans only one of the 16 characters. This character is the one stroked on the keyboard.

After the character signal from the vidicon is suitably shaped, it is directed to the display kinescope for operator inspection. The operator may accept or reject the display character. When the operator accepts the display character, he depresses the *photograph* key on the keyboard. This action feeds the vidicon output to the exposure kinescope and exposes the film. As soon as the film is exposed, the film magazine is moved into position to permit composition of the next character, and the entire machine is reset to accept a new keyboard operation.

LOGIC DESCRIPTION

The logic modules accumulate the information generated at the keyboard; when this information is sufficient to define an operation or a character, the logic modules initiate the operation or locate the character. A block diagram of the logic is shown in Fig. 7. The input to the logic module is an 8-bit code at the keyboard level. After shifting to the logic level and gating by using one of the bits, the 7-bit code is presented to the next logic stage. This code is in a form compatible with the logic speed.

Fig. 2—Variation of size and location of same basic strokes in a Chinese ideograph.

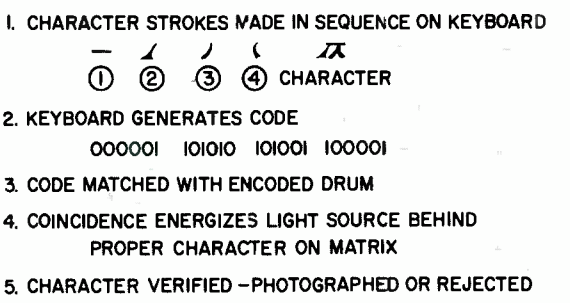


Fig. 3—Ideograph construction by ICM.

Two bits of the 7-bit code are used to define the code as a stroke, a punctuation mark, an entity or an operation for processing as follows:

1) A stroke code enters the encoder directly.
2) A punctuation code enters the encoder as a stroke and then operates on the storage register to uniquely define the punctuation mark.
3) An entity is diverted to the phrase-to-stroke converter, where the stroke sequence that forms the entity is generated and transmitted to the encoder.
4) An operation code is channeled to the appropriate initiating and control circuitry.

The encoder sequences the five bits presented to the shift register where they are stored for comparison with the information on the drum memory.

The timing and index tracks of the drum memory advance and reset an asynchronous counter so that the output of the counter uniquely defines the position of the drum at all times. When the information on the drum is identical to the information in the shift register, the coincidence detector generates a signal which gates the counter reading into a storage register. The contents of the storage register automatically locate that position on the character mask, defined by the input information.

Peripheral logic circuitry is provided within the module to perform a number of operations. As soon as a particular stroke sequence is unique to a character on the matrix, the keyboard will lock and the character will be displayed to the operator for verification. If a stroke sequence is not unique to a single character, an ambiguity exists and the characters concerned will be displayed to the operator for his verification and selection. When an operation is to be performed, the keyboard will lock during the transient period. The insert code will cause unblanking of the insertion vidicon. The erase code will cause a complete reset of the system.

SPECIAL OPERATION FEATURES

Following are descriptions of a number of special operational features of the ICM.

Input

Input may be from keyboard or punched tape at the rate of 600 strokes per minute. Character compostion is possible at the rate of 60 to 100 characters per minute. In addition, the keyboard is

Fig. 4—ICM keyboard.

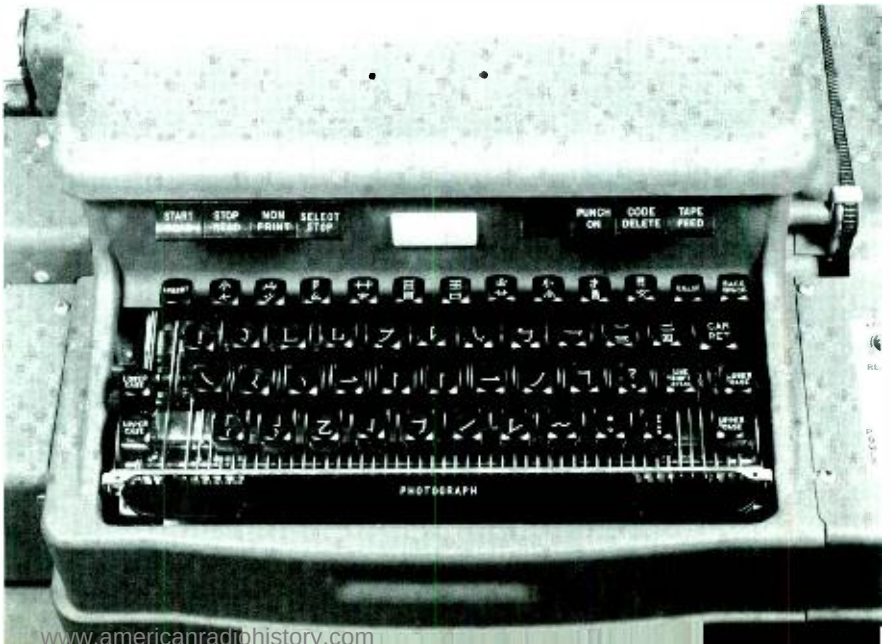
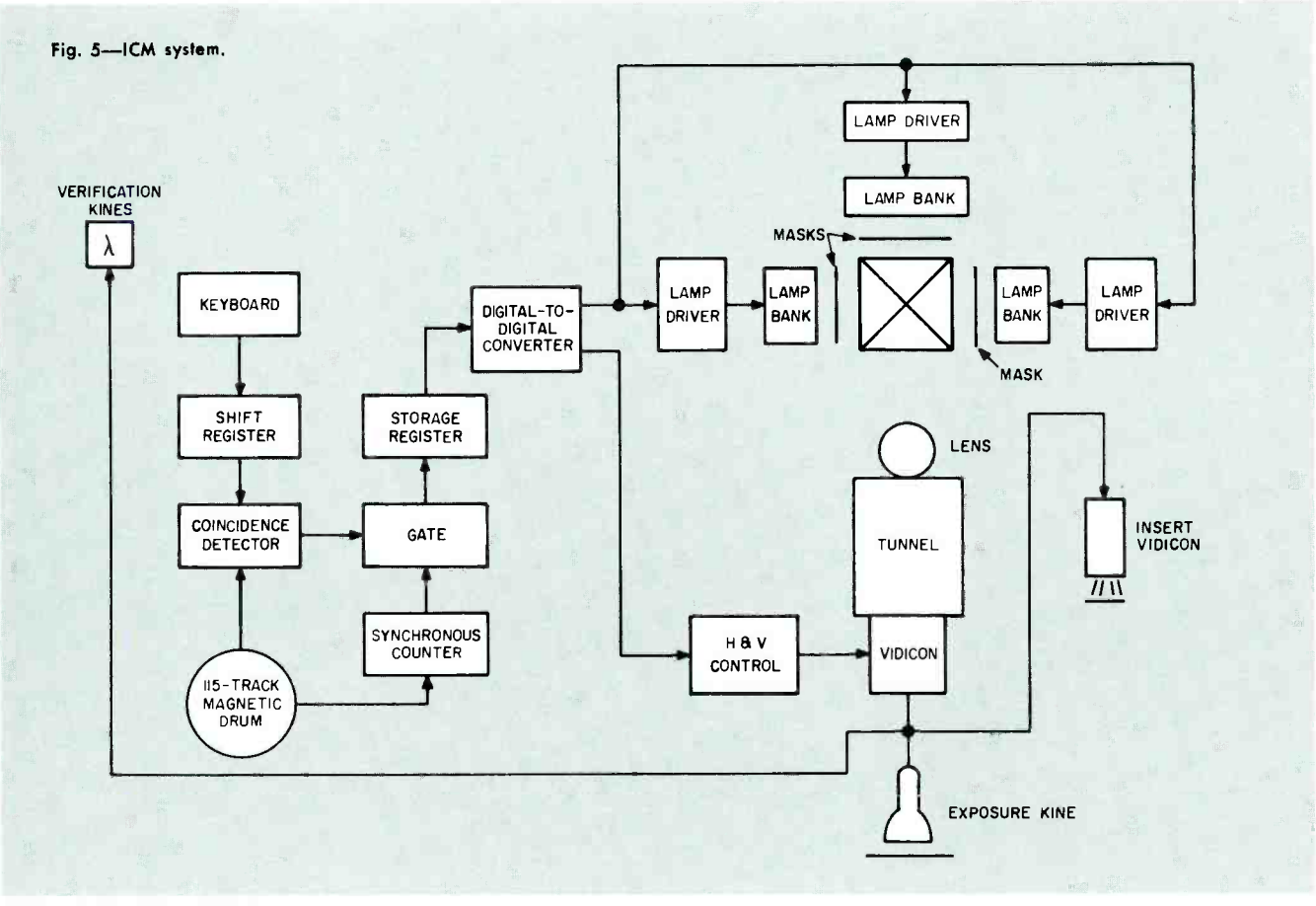


Fig. 5—ICM system.



equipped with a paper tape punch and reader.

Output

The output of the machine is an exposed film on 5-inch-wide page format. Composition of characters may be in vertical columns from right to left or horizontal rows from left to right. Any one of four type fonts, 12-, 18-, 24-, and 30-point size, may be selected by the operator.

Ideograph Display

If in stroking a complex character an operator strokes the code for a shorter character, the machine will recognize this shorter character and display it immediately on the verification kinescope. The operator will continue stroking until he has completed the stroking sequence for the desired character. The machine will continue to display the shorter character until the stroking sequence identifies the desired character. When this happens, the machine will replace the shorter character with the desired character and display it for verification. When the *photograph* bar is pressed, only the last character displayed will be photographed.

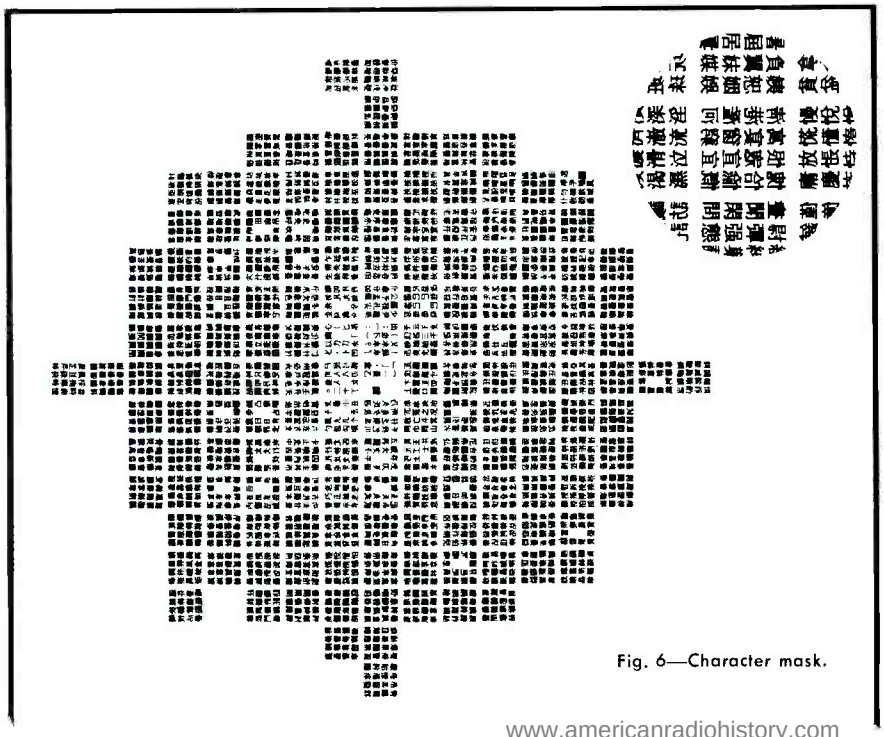


Fig. 6—Character mask.

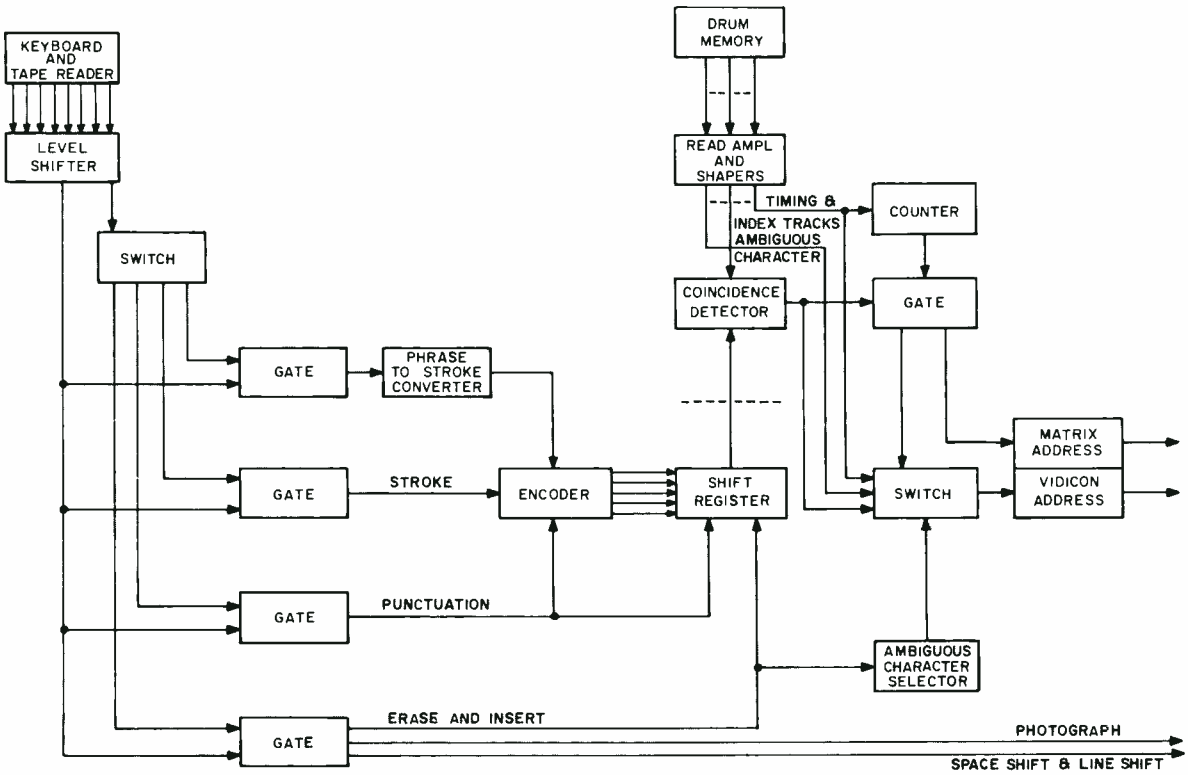
Minimum Spelling

As a time saving device, the ICM is designed to operate on a minimum stroke basis. When the operator reaches a point in the stroking sequence where the strokes accumulated represent a unique character, this unique character is immediately displayed and the keyboard is locked to indicate recognition. This feature will prevent superfluous stroking when a character has already been identified with only partial stroking.

Ambiguous Characters

As indicated previously, the majority of the Chinese characters may be uniquely identified by their strokes and stroking sequence. However, there is a special situation where a given stroking sequence leads to two or more different characters. Fig. 8 shows some samples of these cases. A study of the language has shown, fortunately, that there are relatively few cases that have the same sequence of strokes but look different in

Fig. 7—ICM logic diagram.



the final composition. In a vocabulary of 2,500 Chinese characters, it was found that there are precisely 20 pairs and 4 triads of such characters. These characters are identified as ambiguous characters and require special treatment. If the operator has stroked a sequence that describes an ambiguous character, then a maximum of three characters will be displayed simultaneously on the verification kinescope for operator inspection. The operator will then select the desired character by stroking special keys on the keyboard, at which time the ambiguous characters are removed from the verification kinescope and replaced by the desired character only. The operator may then press the *photograph* bar to complete the composition of the desired character.

Additional Character Insert

A special character insertion capability is also provided. If a desired character is not present in the machine vocabulary, the operator may place his copy, or a document containing the desired character, on a character insertion tray. When the *insert* key on the keyboard is depressed, the insertion vidicon (shown in Fig. 5) is activated and will scan the document. The operator must position the document until the desired character is displayed on the verification kinescope. A zoom lens is then adjusted until this character fills the raster on the verification kinescope. This adjustment assures the proper magnification of the inserted character to match the rest of the internally generated characters. When the magnification adjustment is completed, the inserted character is photographed by pressing the *photograph* key on the keyboard.

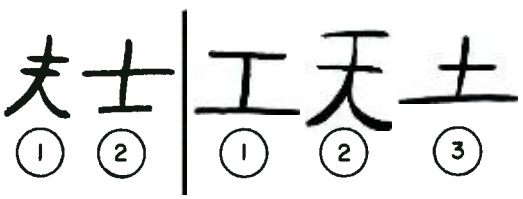


Fig. 8—Characters generated by identical stroke sequences.

ACKNOWLEDGEMENTS

A project of this magnitude naturally necessitates a large team effort. The author wishes to acknowledge the effort of all the members of the team, particularly the two lead engineers G. T. Burton and W. Heagerty and the Optics Group in Applied Research who contributed significantly to the success of this program.

This work was supported by the U.S. Army Natick Research Laboratories.

FRED E. SHASHOUA received his BSEE in 1952 from Faraday House College in England, and his MSEE from Newark College of Engineering in 1954. He worked at Weston Electrical Instrument Corp. in the design and development of a variety of instruments and transformers. In 1956, Mr. Shashoua joined RCA as a design and development engineer of high-speed precision servomechanisms for the Quadruplex Video Tape Recorder; he has specialized also in the area of analog and digital magnetic tape recording systems, including transistorized servos for high-temperature operation. In 1959, Mr. Shashoua was promoted to Leader, Recording Systems Development Group; under his direction, audio-to-video signal converters, multichannel tape loops, and helical and slant-track video recorders for single and multi-channel applications were developed. In 1961, Mr. Shashoua became Leader, Electro-Physical Techniques Group, responsible for investigating such techniques as Transparent Electrofax recording, Photoconductive Thermoplastic recording, magneto-optical recording using Faraday and Kerr principles, and for the design of the Chinese Ideographic Composing Machine. In 1963 Mr. Shashoua was promoted to Manager, Electro-Optics and Thermoelectrics group. He is a member of IEEE and a graduate of IEE (England); he has five patents pending in the field of magnetic recording and electro-optics.

TRANSISTORIZED PORTABLE "VICTROLAS"

During the past few years, transistorization has become very desirable in portable phonograph amplifiers to obtain the well-known advantages of lighter weight, better reliability, instant warm-up, and cooler operation. At the same time, new product designs demand better performance, both in power output and in frequency response. In engineering the models described herein, the feasibility of low-cost portable transistor phonographs having better performance at somewhat lower cost than previous tube-amplifier models has been proven. These models are now in quantity production.

J. A. TOURTELLOT
RCA Victor Home Instruments Division
Indianapolis, Indiana

In low-cost phonographs using single-stage tube amplifiers, high-output pickups are required; such pickups are quite stiff mechanically, require a high stylus force, and thus track marginally. These low-cost amplifiers ordinarily use "transformerless" power supplies with the attendant design problems of minimizing hum and shock hazards.

With transistor amplifiers, DC-coupled multistage circuits provide ample power gain, use pickups with higher compliance and smoother frequency response, and greatly improve tracking. The higher efficiency of the output stage and the elimination of the heater-power requirement result in a cooler amplifier —and make possible the use of a secondary winding on the phonograph motor for the power supply. Thus, the transformer is isolated to eliminate the shock hazard and straightforward ground connections may be made to minimize hum problems.

RELATIVE COSTS

Obviously, the degree of improvement that can be made over the present tube phonographs depends mainly on relative costs. In this product area, selling prices are extremely competitive, so that product cost is a paramount problem. The transistor amplifier portable phonographs described herein provide greater power output than previous tube models, use better pickups, and provide somewhat better overall fidelity at lower costs when averaged over the line and compared with previous products selling for the same list price.

Since these phonographs are AC-line operated, and output circuit efficiency is not a limitation, single-ended class A output transistors were chosen. This choice results in simple low-cost circuits, since this same "economy" transistor is used in very large quantity as a power-output transistor for automobile radios.

POWER OUTPUT VS. GAIN

Since the new transistor amplifiers are rated at substantially greater power than the tube amplifiers being replaced, the final selection was made from the RCA 2N301 family of transistors. The effective power output is then limited by available system gain, power supply output, and proper heat dissipation for thermal stability rather than by the transistor ratings. Transistor ratings are high enough so that no conditions of short circuit or overloading can cause transistor failure.

The power gain available in a single-stage tube amplifier is about 47 to 50 db. Using high-output crystal pickups, the power output per channel that can be developed from an average recording level is approximately ½ watt. A power gain of approximately 70 db is required for the higher cost deluxe portables that use high-compliance ceramic pickups and develop about 1.6-watt output per channel.

The transistor amplifiers for use with crystal pickups were designed to provide 58-to-60-db power gains and power outputs of 1 watt per channel. The pickup compliance is two to three times greater than of the single-tube amplifiers. For use with the higher-compliance ceramic pickups, an amplifier having a power gain of approximately 75 db and a power output of 1.8 watts per channel at less than 5% total distortion is provided.

TWO-STAGE TRANSISTOR AMPLIFIER DESIGN

To obtain minimum cost when using crystal pickups, a two-stage amplifier was designed with a high-gain planar silicon n-p-n transistor directly feeding the p-n-p germanium output stage. While the performance with average transistors was better than the single-stage tube amplifier, the performance with low-β transistors was found to be inadequate. Also, the available system

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J. A. TOURTELLOT studied at Columbia University and graduated in 1937 with an AB degree in Physics. From 1937 to 1939 he was engaged in his own private business and joined RCA in 1940. From 1940 to 1945, he was engaged in UHF, electromechanical modulators and "butterfly" circuits work for military applications. From 1945 to 1953 he was with the Philco Corporation, and upon his return to RCA in 1954 joined the Radio & "Victrola" Record Changer Design group. Since then he has been engaged in development and design work on the automobile "Victrola", stereo phonograph pickups and amplifiers, the "Studiomatic" record changer, and tape recorders for the RCA Victor Home Instruments Division.

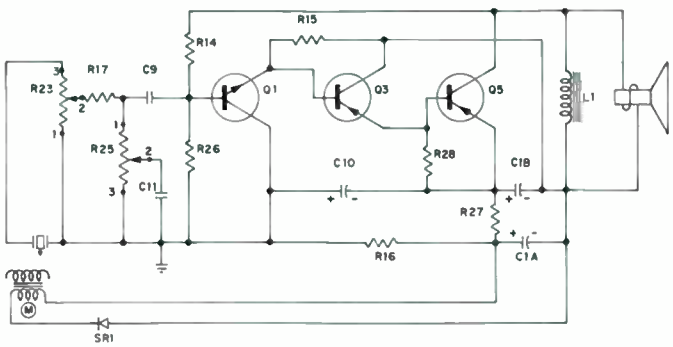


Fig. 1—The 1-watt monaural transistorized amplifier.

gain did not allow the desired increase in pickup compliance, and variation in system gain with limit-β transistors was approximately 12 db.

Accordingly, an additional stage (a p-n-p germanium transistor) was added to the amplifier between the silicon transistor and the output stage. The added gain available allows the use of considerable negative feedback, which stabilizes the DC operating point of the output stage and minimizes the variations in system gain as a function of transistor β's.

The amplifier for use with the ceramic pickup also uses a p-n-p germanium transistor driver, connected as an emitter follower, to drive the p-n-p germanium transistor output stage. The DC coupling eliminates the added costs of coupling capacitors and resistors; thus, the input impedance of the driver was made as high as possible, to maximize the gain of the first stage.

Temperature instability, however, is the product of the instabilities of the two stages. Since the instability of the first stage is of opposite sign, complementary stabilization results when a grounded emitter p-n-p unit is DC-coupled to the second stage; so, initially, the circuit was set up this way; two problems became evident:

1) *The change in collector current of the first stage with temperature tended to overcompensate the other two stages.* While the proper choice of operating points for the various stages and the proper use of feedback might allow the use of this circuit, it appeared almost impossible to maintain properly the operating point of the output stage and achieve adequate temperature stability.
2) When using crystal and ceramic pickups, the generator impedance is equivalent to that of a 1,000-pf *capacitor in series with a low-impedance generator.* Since the input impedance of the grounded-emitter transistor amplifier is very low, a severe drop in low-frequency response occurs unless a large series resistor is used in the input circuit, or unless the input impedance is made to look capacitive by means of feedback. The high-frequency hiss voltage developed in an input resistor is large, and the signal-to-noise ratio is poor. When the gain control is placed between stages, some improvement can be made; but, this connection makes DC coupling impractical and therefore increases cost. If capacitive feedback is used, the addition of the necessary volume control upsets the feedback loop, and high-frequency oscillation resulting from phase shift is a severe problem.

The p-n-p input stage was then connected as an emitter follower input stage; this method alleviated the signal-to-noise problem, with an improvement of nearly 20 db, providing a performance equivalent in this respect to tube amplifiers. However, the DC-coupled arrangement was more unstable with temperature; stability to approximately 50° C was obtained, but this did not allow for high ambient temperature operation.

The final amplifier designs use an n-p-n silicon planar input stage, connected as an emitter follower, with DC coupling throughout the amplifier to provide complementary stabilization. Because of the very low leakage current of the input stage, very high values of resistance can be used in the bias network; this method increases the input impedance and improves low-frequency response.

THREE MODELS OF AMPLIFIERS

Three model amplifiers have been designed: 1-watt monaural, 2-watt stereo, and 3.6-watt deluxe stereo. The problems of temperature stability, interchangeability of Betas, and balance between channels in stereo amplifiers are inter-related to such a degree that a discussion of the circuit development must include all these factors.

1-Watt Monaural

The 1-watt monaural units uses a p-n-p silicon transistor equivalent to 2N2484 with a range of DC β of approximately 5:1 in the first stage; a 2N406 driver, and 40022 output stage with a β range of approximately 5:1; the circuit is shown in Fig. 1. The feedback from the output collector through R14 to the input stage helps to maintain the proper DC operating point for the output stage; DC input to the amplifier varies approximately 23% with the minimum and maximum combinations of all resistor values and transistor β's. Power output variations are less than 2 db.

The power supply for the 1-watt monaural unit uses a half-wave, RC filter arrangement; the filter resistor is in the positive side of the power supply and provides DC feedback to improve temperature stability; a separate RC filter feeds the positive supply to the input stage. The RC values are chosen to cancel out some of the power-supply ripple voltages appearing at the output of the amplifier. The stereo models use full-wave rectification, but otherwise are the same.

2-Watt Stereo

The 2-watt stereo (total for 2 channels) circuit is shown in Fig. 2; it uses essentially the same transistor lineup, with two exceptions. Due to the common power supply, and common-emitter resistor in the output stage, channel

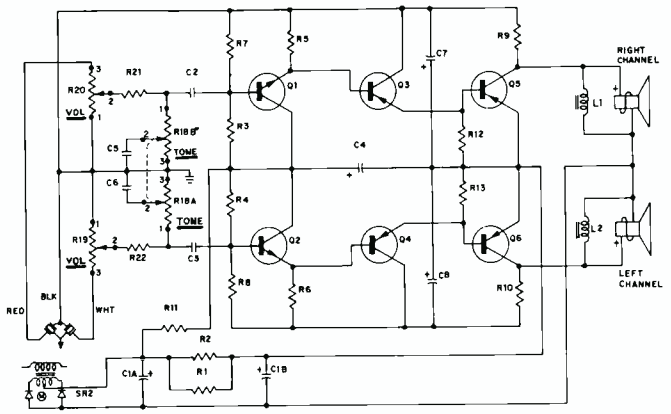


Fig. 2—The 2-watt stereo (2-channel) transistorized amplifier.

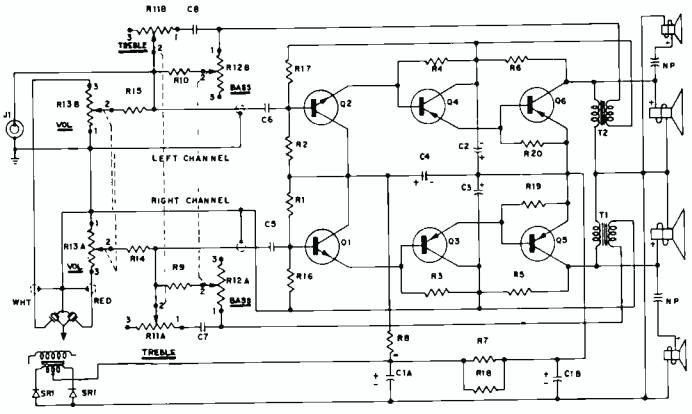


Fig. 3—The 3.6-watt stereo transistorized amplifier.

Fig. 4—Top view of the 2-watt stereo amplifier with turntable cut away to show printed circuitry.

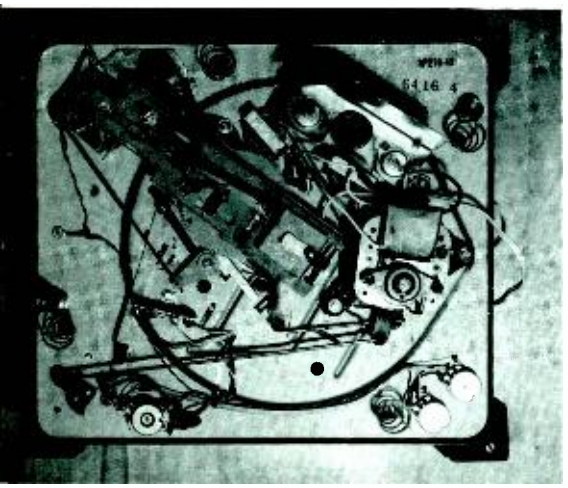


Fig. 5—Bottom view of 2-watt transistorized portable Victrola showing motorboard and mounting of components.

unbalance is acceptable only when DC β's of the output transistors are "matched" within range of approximately 1.5:1. The input stage transistors also have an important bearing on operating point; these units are "matched" in β groups of 2:1 spread. Selection of driver units is not required, nor is it necessary to select high or low β groups. The DC feedback is again provided by R7 and R8 to assist in maintaining the proper operating point. The DC input to the amplifiers varies approximately 23% with all combinations of resistor tolerances and transistors. Power output varies less than 2 db.

3.6-Watt Stereo

The 3.6-watt (total for two channels) stereo uses the same input and output transistors and the same degree of matching; the driver transistors are RCA 2N408's (Fig. 3). The DC power input and audio power output variations are the same as that of the 2-watt unit.

The 3.6-watt amplifier uses a high-resistance volume control, with two knobs frictionally coupled to allow channel balancing. Volume control adjustments vary feedback to provide variations in the low-frequency response which approximate the desired frequency-response-vs.-loudness curves from maximum volume down to −30 db. In addition, high-frequency tone control is provided by variable resistors used in series with the feedback capacitors; low-frequency control is provided by shunt variable resistors which reduce the low-frequency response by altering the feedback.

GENERAL AMPLIFIER DESIGN CONSIDERATIONS

Grounding and Hum Elimination

The audio ground connections in the stereo models are made to one channel only, at a point where the ripple voltage is approximately the same as that at the input stage base; in this way, hum voltage across the speakers remains nearly constant as the volume control is shifted. Separate grounds for each channel could be used, but would increase cost.

Many other filter and grounding arrangements were evaluated, but were found to be more costly because they require greater total filter capacity.

Transistor Operation Vs. Temperature

The efficiency of the output transistor feeding the speaker is approximately 47% at room temperature, and drops to approximately 43% at 55°C. The use of a choke to feed DC to the transistor, and the use of a speaker impedance which properly loads the transistor considerably improve the circuit efficiency over that usually experienced with small, low-cost output transformers.

The transistors and other components of all three amplifiers will operate satisfactorily up to a temperature of approximately 75°C. In the complete instruments, amplifier temperatures are approximately 52°C when the instruments are operated in a 25°C ambient temperature. Thus, operation will be satisfactory up to an ambient of almost 120°F. Operation in higher ambients will not produce thermal runaway, but may damage phonograph records or crystal pickups.

Volume and Tone Controls

Volume controls used in the 1- and 2-watt amplifiers are high-resistance units. Some series resistance inserted between the volume control and amplifiers improves somewhat the impedance matching. At the amplifier end of these resistors, shunt capacitors and series variable resistors provide the usual treble attenuation used as a tone control.

Volume and tone controls are mounted on the motorboard; all interconnecting cables and wiring are integral with the record changer assembly except the cable to the loudspeakers. The use of the mounting screws for the printed board as circuit terminals, plug-in connectors on all cables and plug-in speaker terminals facilitate assembly on the same production line as the record changer and allows processing for minimum testing. Figs. 4 and 5 show top and bottom views of the amplifier and controls mounted in the record changer; the model shown is the 2-watt amplifier with the turntable cut away.

COST FACTORS

There are several important factors in the cost of a portable phonograph. Cost of supporting chassis, interconnecting cables, hand wiring required, and labor of assembling all the components into the cabinet are all appreciable. The normal attrition due to handling in the factory of record changers, amplifiers, cables, and cabinets, usually dictates a rather thorough and costly final instrument test, even though individual components have been completely tested before assembly.

To minimize costs, these amplifiers have been designed to be built on printed circuit boards. The need of a separate supporting chassis has been eliminated by mounting the printed board under the turntable on the record-changer motorboard, allowing the output chokes and filter capacitor to extend through the motorboard. The motorboard serves both as a heat sink and mounting for the output transistors; in the higher powered units an added aluminum bracket and fan on the motor help maintain proper transistor temperatures.

CONCLUSION

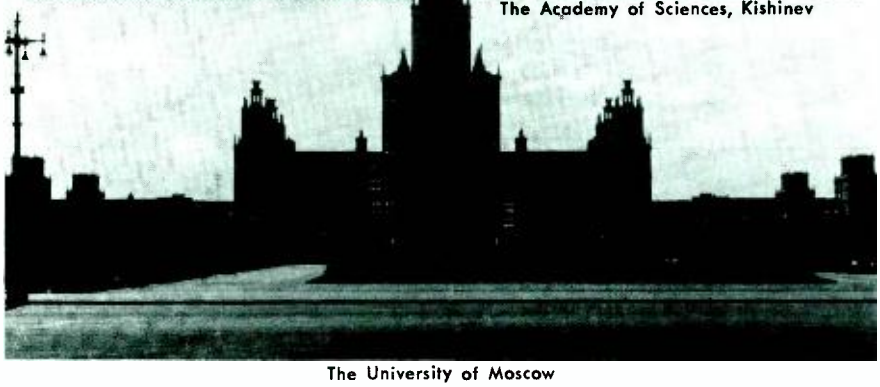
The feasibility of low-cost portable transistor phonographs having better performance at somewhat lower cost than previous models using tube amplifiers has been proven. These models are now in quantity production.

ACKNOWLEDGEMENT

The author wishes to express appreciation to R. P. Peterson for his electrical design work and to P. E. O'Connell and his group for mechanical design work, during this development.

REPORT ON A VISIT TO THE SOVIET UNION

The Academy of Sciences, Kishinev



The University of Moscow

The Academy of Sciences of the U.S.S.R. extended to the author an invitation to participate in the Third All Soviet Conference on Compound Semiconductors held in Kishinev in late 1963. This paper presents some impressions gathered at the meeting and during visits to several Soviet laboratories.

Dr. J. I. PANKOVE

RCA Laboratories, Princeton, N.J.

We all have heard of many depressing aspects of life behind the Iron Curtain: seriously limited freedoms, crowded housing, low standard of living, and the like. Most of this is obvious to the inquiring visitor, but strangely enough, it does not seem so obvious to most Russians. They have only one standard of comparison: life of a few years ago. They have long lived through such repressions as the "dark days" of Stalin's era and the Nazi occupation, and have endured such low economic standards that to those who have not experienced a better way of life—this includes almost all the Soviet citizens—they have, by comparison, a feeling of freedom and prosperity. *We must appreciate this inside perspective if we are to understand the dedicated patriotism of the Russian people in spite of their enduring an ambiance that we could not tolerate.* However, this report is concerned with impressions about science in the Soviet Union and I wish to stress its positive aspects.

The overall impression is almost incredible, but seeing is believing. The Soviet Union has placed a tremendous effort on education that is now paying off in terms of available skilled manpower. This fact shows up in the rate of growth of the various laboratories visited. Not only is scientific manpower abundant, but also the supply and availability of equipment is fantastic. Even if the average performance is mediocre, the existing facilities provide a favorable breeding ground for major scientific advances. This is the picture today and we must bear in mind that the rate of growth is—*by our standards*—tremendous. Another factor that may be favorable to rapid progress is the nature of the organization. The work in various laboratories can be coordinated to minimize the duplication of effort. There is no problem of company secrecy to impede such coordination. Consequently, there is flexibility not only to give adequate support to worthwhile projects, but also to deploy available manpower over a broad range of problems.

We are often not aware of their accomplishments for the simple reason that very few of us can read Russian. Translation suffers so much delay that most people do not bother surveying the Russian literature. By the way, this is a delicate point in our international relations in scientific circles because, through ignorance, we frequently fail to give proper credit to pertinent Soviet work in our references. But in contrast to their sometimes flagrant statements of data without any reference to American sources, I believe that our omissions are not intentional.

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ARRIVAL TO MEETING

As soon as we stepped off the plane at the Kishinev airport, it became quite clear that most of us were not simply tourists. A welcoming committee from the Kishinev Academy of Sciences was on hand to greet the conferees. Cordiality, hospitable words, and handshakes were only a prelude to the marathon that followed. Throughout the day-long conferences, during the laboratory visits and even beyond, from the moment one stepped out of his bedroom for breakfast until the lights were turned off in all the public rooms at midnight, the Soviet scientists were persistently anxious to discuss their work, describe their life and, mostly, find out about life in the USA. The thaw in the Cold War was hailed with hopes for further rapprochement. Never have I experienced such prolonged and massive demonstration of interest and cordiality. The ability to communicate in Russian was, of course, a very favorable factor in our contacts.

Why was the conference held in Kishinev? Kishinev, with a population of 236,000 is the capital of the Moldavian Republic. At first glance, one has the impression of a sprawling village. The major industries of Kishinev are viticulture and textiles. But Kishinev is also a rapidly growing cultural center. It is the seat of the Academy of Sciences of the Moldavian Republic. About three years ago, the Academy of Sciences set up an institute for the study of semiconductor physics. This group, plus previously existing supporting activities in the fields of chemistry and electrochemistry, now number over 100 people. In spite of its short existence, this group has already published several papers. It was to welcome this new group to the scientific community of the Soviet Union that the Soviet Academy of Sciences organized this conference in Kishinev, thus not only acknowledging its existence, but also bringing inspiration and assistance to the new organization.

About 300 people attended the conference. Eleven nations were represented. Three representatives came from the U.S.A.: Professor H. Y. Fan (Purdue), Dr. Sangster (Texas Instrument), and the author. Ehrenreich (Harvard), Petritz (T.I.) and Whelan (B.T.L.) had also been invited, but were unable to attend. Two came from Great Britain: Hilsum and Putley (SERL); one from West Germany: H. Weiss (Siemens). From France, the husband-and-wife-team, Drs. Rodot. Two came from China, others from Hungary, Czechoslovakia, Rumania, Lithuania, etc. Of course, a great number of local scientists attended. All but four papers were given in Russian. The British and French papers were given with a pause after each phrase to allow simultaneous translation. A pretty teacher of English tried her best as a translator at the side of one of the Chinese delegates, Miss Lin

Lan Ying, from Peking, (formerly from Sylvania, Bayside) for Miss Ying knew no Russian; it was amusing that in this instance, English should be the bond between Russian and Chinese!

The meeting was held in the auditorium of the University Club. A raised stage bordered with a garden-full of cut flowers and potted greenery was framed with heavy drapes topped by a red banner carrying a long slogan in Moldavian. In back of the stage, a bust of Lenin stood illuminated by a beam of purple light. When the meeting began, a curtain masked the bust. There were two enormous Leitz epidiascopes and other projectors as needed. Two stenographers were partially hidden in a corner of the stage. A back room was loaded with tape recording equipment. Two rooms with small round tables were available for private conferences.

The schedule of the meeting was rather flexible and not too well observed. Some speakers showed up later than their turn. No one was cut off successfully. They plowed through their speeches while the chairman signaled, passed notes, and begged them to terminate. The conference was concerned with a fantastic variety of compound semiconductors, but few device papers were given.

SOME LABORATORY FACILITIES

In addition to attending the conference, I visited several laboratories. My dominant impression was amazement at the fantastic rate of growth of the trained personnel and the abundance of equipment. In Kiev, for example, the semiconductor group grew from 70 to 300 in the space of two years. The Institute for semiconductors in Kishinev started two years ago. The x-ray department there has grown from 1 man to a team of 24; new quarters will be ready in two months with 600 square yards available for x-ray alone to replace the present 24 square yards. There are eight machines for x-ray diffraction and one with a Geiger counter; three interference microscopes; many spectrometers; sensitive instruments stand on shelves up to the ceiling; there are many spectrometers; equipment for paramagnetic resonance and spin resonance; an electron microscope, and some equipment still in crates. Sometimes the new and the old form a strange contrast: for example, an electric calculator on the desk and an abacus on the wall. The buildings seem to age rapidly. A new building, about 5 years old, looks as if it were 30 years old. Little attention is given to maintenance: For instance, in the so-called new buildings there are raised floor boards creating a danger of tripping while carrying equipment. The inside of the buildings look gray, but most of the walls are hidden by huge piles of equipment.

New projects often originate from individual researchers. Thus, there is sometimes an overlap between research in various laboratories. But, by and large, the research is coordinated by the Academy of Sciences. Various groups specialize in limited areas. But, they expand this activity very rapidly, especially in depth. Although, in general, there is no competition between the various laboratories, since they all work for the same "management," there is sometimes competition between individuals or between small groups, motivated by the desire to publish first. As an example of coordination by the Academy of Sciences let us cite the foliowing case: About two years ago, the Academy of Sciences decided that there ought to be a deep study of heavily doped semiconductors. Specialists with appropriate backgrounds were requested to participate in this program. This involved several laboratories. Thus, Bagaiev's group in Moscow was assigned to study heavily doped germanium and Dubrovski in Leningrad was assigned to study heavily doped silicon. Representatives of the two groups often visit each other. (To get an idea of the effort placed in this project, Dubrovski's group numbers about 20 people.)

I was asked to give a seminar at the Lebedev Institute of Moscow, The Institute for Semiconductors of Kiev and the Physico-Technical Institute of Leningrad. It was remarkable how quickly a large audience could be assembled on short notice (less than one hour). My conducting both the presentation and the discussion in Russian was much appreciated. Although almost every Russian scientist reads technical English, not many can follow spoken English. The subject of the seminars was, like my paper at Kishinev, on electroluminescence in GaAs.

At Moscow University, I had a tour of the semiconductor laboratories. The most impressive aspect of this laboratory, in contrast to other laboratories in the U.S.S.R. is the neat arrangement of the equipment in all the rooms and the fact that the laboratory is well illuminated.

SEMICONDUCTOR LABORATORY OF THE ACADEMY OF SCIENCES OF MOLDAVIAN REPUBLIC—KISHINEV

This organized tour was arranged for the foreign conferees including those from satellite countries. The greatest specialty of this laboratory is the x-ray study of the structure of various semiconducting compounds but, the oldest and most substantial group in the laboratory is the Analytical Laboratory. It is the oldest group because the main industry of Kishinev is wine-making and the chemical and biochemical laboratory was an important original asset. As semiconductors became a more fashionable field of research, the Analytical Laboratory turned in this direction. Their major analytical tool for semiconductors is polarography. I am still greatly impressed by the wealth of scientific equipment gathered in this very new laboratory.

KIEV INSTITUTE FOR SEMICONDUCTORS

The Semiconductor Group was created in 1961 using a nucleus of 70 people from the Academy of Sciences of Kiev. They moved into their brand new building in 1962. Although the building is spacious, the windows large, and some offices freshly painted in pastel colors, I would have guessed that the age of the building was more like ten years. Now the staff of the Semiconductor Laboratory numbers 300 people, a third of whom are scientists.

SOME ASPECTS OF EDUCATION IN THE USSR

Now, a few words about what really is the *most impressive fundamental aspect of science* in the Soviet Union—the large number of scientific personnel and their high rate of growth. The growth rate is high in terms of the economic needs of the country and in terms of the manpower shortage (which in other economies could mean that education is not essential to get a job). This rate of growth is striking when one visits laboratories: one sees expansion of laboratories in equipment as well as in personnel and in space. Many of the research

DR. JACQUES I. PANKOVE obtained his BS in 1944, and his MS in 1948 from the University of California, both in EE. In 1948 he joined the RCA Laboratories; In 1956, he was the recipient of a "David Sarnoff Fellowship" to study at the University of Paris, France. His doctoral research topic there was the study of infrared radiation from surface processes in germanium. Since his return to RCA Laboratories, he has worked on superconductivity, where he has evolved several new device concepts and has done research on silicon carbide. He has investigated the optical properties of degenerate germanium and the electrical properties of tunnel diodes in germanium. Currently, he is concerned with interjection luminescence and the laser action in gallium arsenide and other compounds. Dr. Pankove has published over 20 papers and has over 30 issued patents. He is a member of the APS, IEEE, the Electrochemical Society, and Sigma Xi.

people are in their late twenties or early thirties. Last year there were about 100.000 scientific graduates in the U.S.S.R. compared to about 30.000 in the U.S.A. Part of the large availability of manpower results from the equality of women on the job. Most women are employed, and there are *many* female scientists. (Nearly half of the audience at the Kishinev meeting was female.

Not only the number of people available for a scientific career is high, but also the interest in sciences runs high—stimulated by high literacy, capitalization on space achievements, and perhaps the love of chess which helps develop a logical mind (bellhops in hotels spend their waiting moments in one small room playing chess).

Formal education starts at the age of 7. Prior to that time, children are taken care of either by grandparents or by nursery schools or kindergartens. Usually, when starting school the child already knows how to read and count; (but not to write, because teachers prefer to instruct this skill their own way). English is introduced at the age of 11, (at the rate of one hour a day). In big cities, there are schools where all subjects are taught in one foreign language. *In Moscow alone, there are several schools that teach everything in English from the first grade on.* These schools, like all the others, are free of charge. They are so much in demand that admission is on a priority basis. (It helps to have pull). At the college level, language instruction becomes more concentrated: four teachers are used to treat different aspects of the language, vocabulary, phonetics, grammar, literature. This explains why many young scientists who have never been beyond the iron curtain are fluent and accentless in English. *They all read American scientific literature* (even those who cannot speak English).

The American scientific literature is received with about one to two months delay. It takes two months to get copies reproduced by photo-offset (a widespread practice for the most-read journals). Translation takes another four months.

The students enter the university between the ages of 17 and 35, but mostly at 19. Physics students spend five and a half years as undergraduates in the department. For the first three years, they study general Physics. On the fourth year they begin the study of Semiconductors. On the fifth year, at the university of Moscow, they study the effect of radiation on semiconductors and also the theory of semiconductors. During the second half of the fifth year, they begin experimental research which lasts a whole year. At this point, they get the Bachelor's degree. Then they can pursue further experimental work in a research lab and receive, after three years, a diploma (this is equivalent to our Master's degree). After this, if they wish to work for a Doctorate, they acquire the title of "Aspirant." Oftentimes, the Aspirant is assisted by those preparing for the diploma; thus, the coverage of his thesis gains in breadth as well as depth.

The course on semiconductor devices at Moscow University (in the fourth year) includes a laboratory period during which the students get an intimate acquaintance with the phenomena involved in device operation. The laboratory consists of compact test stations all wired up. The test stations are as follows:

- Photoconductivity and its spectral dependence.
- Volt-ampere characteristic of a rectifier as a function of temperature.
- Carrier diffusion length by the Valdes method.
- Transistor characteristics (which demonstrates carrier transport).
- The Haynes-Shockley experiment.
- Characteristics of the tunnel diode.

The test procedure and the samples are furnished. The student makes all the required measurements, reports the calculations and makes conclusions about the performance of the devices or the significance of the phenomena. Six hours are allowed for each experiment.

REMUNERATION AND GENERAL LIVING

The pay scale of scientists is among the highest in the Soviet Union. A 30-year-old researcher gets about 200 rubles per month (1 ruble = $1.10). (A store clerk gets about 50.) A laboratory director in his fifties gets the fabulous sum of 500. Since the major expenditure is on food and clothing (and even store clerks look well-fed and adequately dressed) such salaries, often doubled by the spouse's income, allow many luxuries, like a car or a country house (built on government-owned property). Sometimes the income is handsomely supplemented by extra fees for translation or abstracting scientific papers and books. There is no income tax for incomes lower than 60 rubles per month; above 100 rubles per month, the income tax is 13% and does not increase with higher income.

Paid vacations last at least a month and often, depending on the nature of work, are six weeks long. Usually people spend their vacation traveling, (within the iron curtain) visiting relatives, or staying at resorts. There are inexpensive two-week train excursions from Leningrad. The train takes the vacationers to the Black Sea, remains there for a week as their hotel, and then brings people back to Leningrad. Although there is no visa requirement to visit other Iron Curtain countries, it is still very difficult to go beyond the curtain. Such travel can be done only on business. In this case, a round-trip to the U.S.A. costs only $500. This figure implies that the Moscow-Paris or Moscow-London part of the trip via Aeroflot is government-subsidized.

When scientists go to meetings in other cities (this is called "Komandirovka"), their travel and hotel expenses are refunded against a receipt. For food, a flat allowance of 3 rubles per day is made.

Regarding housing, scientists get first priority in new apartments—"They need more quiet space for homework." The official minimum living area is 10 square yards per person. The rent runs about $3.00 per month for the average apartment.

The regard that the Soviet government has for its scientists is illustrated by extending privileges into the religious domain: although most churches have been closed or torn down, one particular church in Leningrad destined to be replaced by a subway station was kept "operational" as long as lived the famous scientist Pavlov, a very religious man who regularly frequented this church.

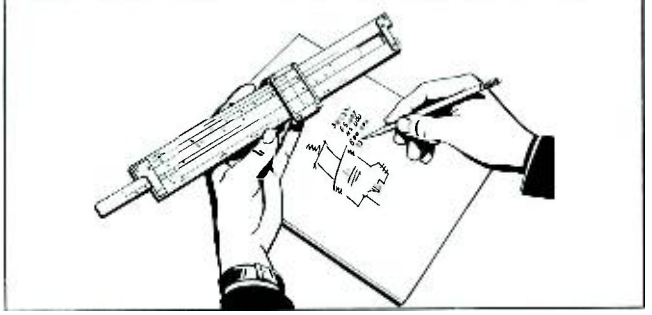
CONCLUSION

In spite of the many shortcomings of a centralized, bureaucratic economy, the Soviet system has the flexibility of placing emphasis wherever they wish. Thus, they have chosen to push education and the sciences. In education, their success is obvious in the high literacy and the quantity of books and other publications available at very low cost; in the sciences, their space exploits, and the rapid rate of growth of various scientific disciplines. In semiconductors, the quality of work, with few exceptions, has been mediocre in the last decade, but the perspective is changing. With their large facilities in personnel and equipment, it won't be long before excellent original work will begin appearing in the Soviet scientific literature. This expansion into the sciences may not continue when other aspects of the economy receive full attention, but *if it continues, it will be our turn to follow their technical literature.*

Our future requires that we upgrade the quality of our grammar schools and that we subsidize the tuition and subsistence of capable college students. Also, the time probably has come for our youngsters to learn the Russian language.

Engineering and Research NOTES

BRIEF TECHNICAL PAPERS OF CURRENT INTEREST



Effect of Unpublished Characteristics and Mounting Variables on Accelerometer Performance

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Final manuscript received March 20, 1964.

The need to clear vibration data of the influence of variables introduced by various mounting techniques, as well as those variables introduced by unpublished accelerometer characteristics, was considered to be of sufficient importance that a study of these problems was conducted.

Many of the unpublished accelerometer characteristics, which the instrumentation engineer is usually cognizant of, are inherent functions of design. Among the more well known are mounting torque and acoustic sensitivity, dependence of the accelerometer capacitance on temperature, and dynamic linearity. There are several other potential problem areas which are not so easily recognized:

1) *Polarity*—this can be disastrous if it is not alike for all accelerometers.
2) *Sensitivity to base distortion (surface strain)*—this is of particular importance in a cemented mounting where full-surface bonding forces the accelerometer base to follow ripples in the test object surface. These ripples are coupled through the base of the accelerometer into the transducing element and can result in an output error regardless of the actual vibration level; however, these ripples are more evident in the 5-to-30-cps region with miniature, compression-mode accelerometers.
3) *Pyroelectric effect*—high sensitivity to the rate-of-change of temperature: sudden drafts from a door, transients in room illumination, etc.—these temperature transients, if sufficiently fast, can cause very high D-C level shifts in some models. These shifts can cause saturation of associated impedance-matching amplifiers or, at the very least, confuse data interpretation efforts if data reduction involves filters and integration.
4) *Magnetic effect*—sudden changes in a magnetic field such as turning on the shaker field, or passing the accelerometer through a stationary field, have produced outputs equivalent to 2 g's (peak).

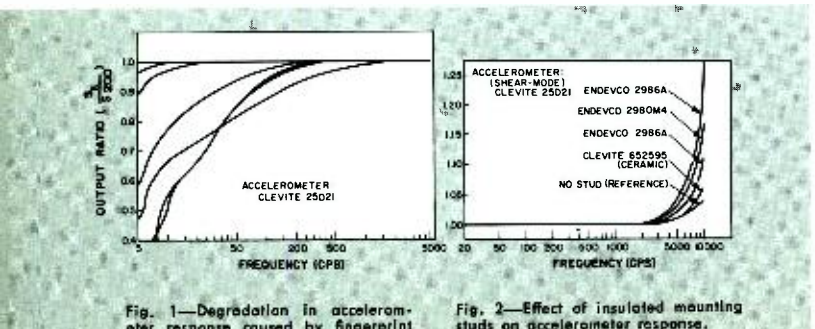

Fig. 1—Degradation in accelerometer response caused by fingerprint deposits.

Fig. 2—Effect of insulated mounting studs on accelerometer response.

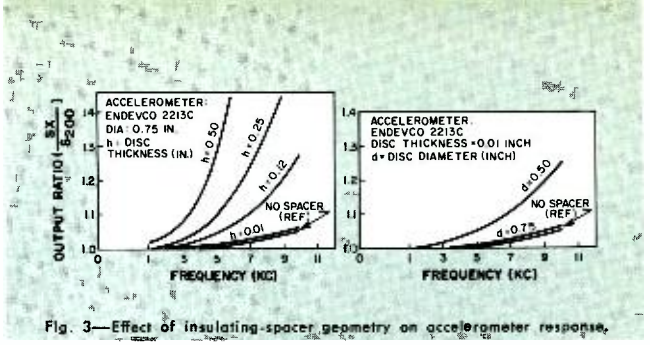

Fig. 3—Effect of insulating-spacer geometry on accelerometer response.

Another group of variables is introduced into vibration data by the simple fact that in order to use an accelerometer, one has to mount it. One important variable is torque effect in accelerometers which are otherwise not case sensitive. Frequency response from these accelerometers can be improved by a light oil-film at the interface. This oil-film causes the torque effect to be less pronounced (an improvement of 20% was achieved at 10 kc). This finding is particularly valuable in shock testing. The effects of improper handling are also important and are illustrated in Fig. 1. Each curve represents the degradation of response at low frequencies caused by varying degrees of fingerprint deposits.

Effects of the geometry and material of adapter blocks were investigated; these blocks are used to mount the accelerometer to odd-shaped surfaces or to combine three accelerometers into a tri-axial system. For a while, Fiberglas (G-11) was used as the adapter block material since it provided the most practical combination of mechanical coupling and ground-loop isolation. However, after an insulated-wafer technique was developed, this material was replaced by aluminum. In all cases, the sweep frequency during the investigations was extended to 10 kc (as opposed to a normal 2-kc maximum during most vibration tests) because waveforms obtained during actual tests often show a large harmonic content; the interaction of Fourier components with the resonances caused by poor mounting can lead to gross waveform distortion by selective amplification or attenuation.

For applications where threaded holes can be tolerated, commercial insulated studs were investigated. A comparison of the effect of studs of this type was made, and some of the results are shown in the curves of Fig. 2. Vacuum and magnetic mounting techniques were also considered for general mounting applications, and vacuum mounting was ruled out as impractical. Magnetic techniques were investigated using a General Radio magnetic clamp Model 1560-P-35, but, because of a limited useful frequency and acceleration range and because most structures are non-magnetic, this technique was found to be of limited value.

Cementing the accelerometer in place with an insulating material in between was determined to be the most practical method for the majority of applications at AED (for example, mountings on cameras, solar cells, etc.). Considerable effort was spent in the investigation of insulating-spacer various materials to be used with this method. The best material for this purpose was determined to be melamine-impregnated Fiberglas (G-11); effects of spacer geometry are illustrated in Fig. 3. On the basis of these curves the material was reduced in physical size until only a thin layer of cement was retained. The insulating properties of the cement were adequate but any uncontrolled pressure during the mounting operation could ground the accelerometer before the cement had a chance to harden. This problem was then resolved by using a layer of paper impregnated with the cement; mechanical coupling in this case was excellent, and the difference between this method and the direct stud-mount was not measurable.

Of the various cements tried, Eastman 910 was found to be the most suitable. The cementing method of mounting did present new problems in the enforcement of specified cementing routines. The bonding quality cannot be judged accurately by hand pressure:

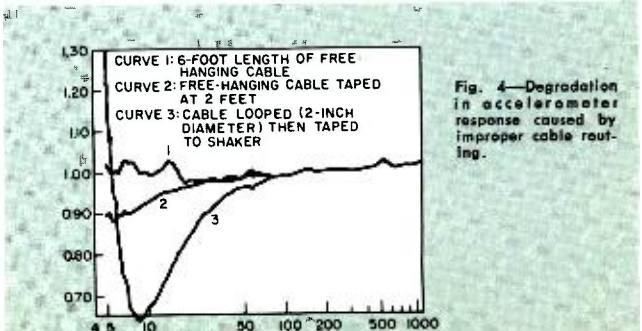

Fig. 4—Degradation in accelerometer response caused by improper cable routing.

seemingly sturdy assemblies often showed resonances which could be traced to a nonuniform bonding and formation of air pockets. There are, however, numerous applications where cementing is the only practical method that can be used.

Pressure-sensitive tapes and films (so-called transfer types—without backing were investigated because of the relative ease with which an accelerometer could be mounted and removed. After the dependence of this type of bond on application pressure (sponge factor), temperature, cold flow, shear strength, and other factors was established, the advantages of this type of mounting seemed doubtful. The need for close and continuous surveillance ruled the tapes and films out as general mounting methods.

Cable routing can be important at low frequencies with some models of accelerometers. An example of this is shown in Fig. 4. The effect of cable routing was found to be less on shear-mode accelerometers than on the other types tested. A rule of thumb for cable routing is to let the cable assume its own natural position, as long as its weight does not become excessive. It was found also that substantial noise levels (some as high as 3 or 4 g's) were being created by applications of sudden stress along the cable. Consequently, the previously popular technique of taping the cable every 6 inches had to be released in order to provide a certain amount of slack.

As a result of this investigation, much valuable knowledge has been gained concerning the application and handling of accelerometers. It was shown that an engineer must take into account much more than the published characteristics of an accelerometer if he is to derive meaningful data from its use. In addition, it was demonstrated that the user can cause serious degradation in accelerometer response by unknowingly adding variables of his own.

Acknowledgement: This *Note* has been condensed from a paper presented at the 33rd Symposium on Shock and Vibration held recently in Washington, D. C.

Microwave Amplification in Superconductors

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Final manuscript received June 30, 1964

Recent experiments[1] show that superconducting films exhibit a nonlinear inductance at frequencies extending well into the millimeter-wave range. Frequency conversion was observed in tin films cooled below their critical temperature. Now amplification and oscillation have also been demonstrated. A superconducting "paramp" has been operated at 6 Gc with 11 db of net gain; parametric oscillations at about the same frequency were also effected.

The superconducting film and the varactor differ markedly in many respects; hence, their circuit needs also differ. A study of the characteristics of superconducting films and parametric device requirements resulted in the concept of the *modified dielectric resonator*. This consists of a very low-loss, high-permittivity, dielectric cavity modified at one of its boundaries by a superconducting film. The unit is placed in a waveguide where power is coupled to it with a movable short-circuit. The resonant frequency of the cavity is a function of its dimensions, the permittivity of the dielectric and the impedance of the film.

Since the inductance of a film depends only on the magnitude of the current through it and not on its direction, doubly degenerate operation is possible, i.e., signal, pump, and idler frequencies may be made very close to one another. While non-degenerate operation is advantageous from some points of view, the simplicity of the doubly-degenerate mode justified its use in the first laboratory attempt at amplification. Pump and signal are introduced in the same guide and monitored with the same equipment. Only one resonant circuit is required. These simplifying features are especially welcome in a device that must operate at liquid helium temperature.

Fig. 1 is a photograph of the output and input spectra of the amplifier. The right-hand trace shows pump and signal inputs. The left-hand trace is device output and illustrates a larger signal, a

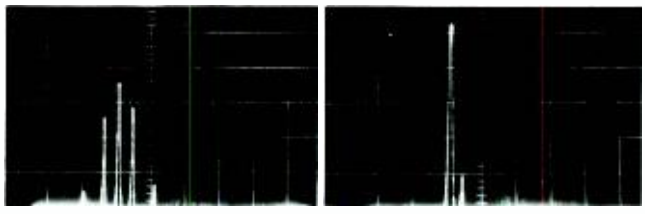


Fig. 1—Output (l.) and input (r.) spectra of the superconducting paramp.

reduced pump and three new frequencies. The frequency immediately to the left of the pump is the idler. The two smaller pips result from higher order terms in the film's inductance-current characteristic. With the signal input turned off and the pump parameters properly adjusted, parametric oscillations were observed. These occurred in pairs, symmetrically spaced about the pump frequency, as expected.

While it may be premature to speculate on the eventual role of the superconducting "paramp", it should be noted that the device, in principle, offers an outstanding set of features not to be found in the varactor or any other device. First, the frequency limit of superconducting films may extend into the sub-millimeter wave range. Second, it is expected that the noise performance of the device can match that of the maser. Furthermore, superconductors can be pumped with considerable lower power and at a lower frequency than either the varactor or the maser. Finally, since one can fabricate large-area films (as compared with lumped varactors), wide-band truly-distributed traveling-wave parametric amplification may become possible.

1. A. S. Clorfeine, Applied Phys. Lett. 4, No. 7, 131 (1964).

The Reed Switch as a Laboratory Tool

M. B. Knight, *Electronic Components and Devices, Harrison, N. J.*

Final manuscript received March 17, 1964.

In addition to the growing number of commercial uses for the magnetic reed switch, this versatile component is an inexpensive and time-saving tool for every day lab work. This *Note* calls attention to some practical uses of the reed switch which suggest its usefulness in the engineer's "bag of tricks." For example, the reed switch has low capacitance to ground and can be operated in a "hot" breadboard circuit by simple manipulation of a permanent magnet a few inches from the switch. Many more uses of permanent-magnet and electromagnet operation are easily visualized if one is familiar with the basic operating characteristics of the reed switch.

Basics of the Magnetic Reed Switch: As shown in Fig. 1, the reed switch consists of two thin reeds of magnetic material in a glass enclosure which provides both mechanical support for the reeds and hermetic sealing to protect the contacts. The reeds overlap and are spaced a small distance apart so that a magnetizing force applied along the axis of the reeds causes the free ends to be attracted to each other. Because the resulting displacement of the flexible reeds decreases the reluctance of the air gap, the flux density in the gap increases further, and, when the magnetizing force reaches a sufficient value, the reeds snap together. They remain in contact until the magnetizing force is reduced to a considerably lower value, whereupon they snap apart. Although the user may need no more than this simple explanation, the details of magnetic and mechanical theory used to describe the quantitative behavior of the reed switch is worthy of earnest analysis.[1,2]

This simple switch package is quite rugged, notwithstanding the usual handling and soldering precautions for glass-to-metal seals. Even though a laboratory worker may not mind breaking a few for the sake of the experiment, however, he should be wary of exceeding the contact ratings. In particular, excessive peak currents or voltages caused by switching in capacitive or inductive circuits can cause the contacts to stick.

A reed switch may be conveniently actuated with a permanent magnet or by current in a solenoid coil surrounding the switch envelope. A magneto motive force of the order of 50 ampere-turns is sufficient for most miniature types. The contacts are generally capable of switching ⅛ ampere or withstanding 300 volts or more.

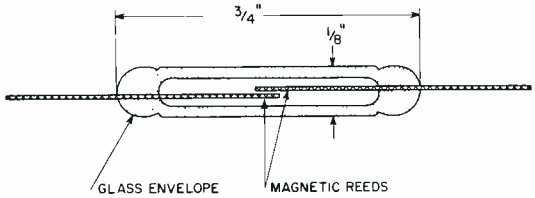


Fig. 1—Cross section of typical miniature reed switch.

The special utility of reed switches for experimental work is due to exceptional characteristics in those areas in which mechanical-contact switches are superior to their electronic counterparts. For example, in terms of fundamental switching ability, the resistance of a typical reed switch changes from less than 0.2 ohm when closed to more than 25,000 megohms when open. Furthermore, both contacts are free from "ground" and the small size of the reed switch minimizes capacitance effects. The direct capacitance between open contacts of an unshielded switch is less than 0.2 picofarad, and it is less than 0.1 picofarad when the actuating coil is used as a shield. Capacitance from each contact to a centrally located coil is less than 0.6 picofarad, and this value can be reduced for one contact by moving the coil toward the other end of the capsule (with some increase in ampere-turns required for closure). Capacitance can be further reduced by use of a permanent magnet for actuation.

The operating speed of reed switches is fast when compared with that of conventional relays. Closure time is less than one millisecond (including contact bounce) and drop-out time is less than 0.1 millisecond. Although operation up to several hundred closures per second is possible, high-speed operation is not always practical because the reeds continue to vibrate after opening. A period of more than one-tenth second should be allowed for decay of this vibration if the next closure time is to be essentially independent of the previous operation.

Experimental Applications: Experimental uses for reed switches may be suggested by description of some laboratory situations recently encountered by the writer. For example, there was an uncertainty whether the addition of a series grid resistance would affect the performance of a television circuit. The sensitivity of such a test is improved if numerous observations can be made in rapid sequence. The circuit of Fig. 2 fulfilled the requirements. The switch was operated by a strong bar magnet from a distance of about 2½ inches, and, therefore, eliminated the hand-capacitance effects and electric shocks associated with bridging components by hand. The switch even provided audible "clicks" to correlate with tests.

Another situation called for a more sophisticated application of the reed switch. When a small capacitance was added from grid to ground in a television circuit, the transient effect on horizontal synchronization was difficult to observe. By means of the circuit shown in Fig. 3, the transient was repeated with each field and the picture disturbance could be observed continuously while circuit adjustments were being made. The switch was operated from the 60-cycle heater voltage by use of a 1,000-turn coil with a series resistor to limit the coil current to a suitable value. A permanent magnet supplied a steady bias to the magnetic field so that the switch would operate at a 60-cycle rate. Without bias, the switch would close on both polarities of the magnetic field and operate at twice the frequency of the AC current. If the AC current is set at a suitable value, the permanent magnet can be positioned to yield no switch closure, repetitive closure, or full closure.

The same principles can be applied to many other applications. For example, a transient can be repeated in synchronism with an oscilloscope sweep either by use of the sweep voltage to operate the switch or by synchronization of the sweep to the switch signals. Moreover, it should be convenient in many cases to synchronize the initiation of a single transient with a camera shutter.

The utility of reed switches in mechanical apparatus should not be overlooked. Permanent magnets and reed switches could be used in many applications that now employ cams and sensitive snap-action switches. The absence of mechanical contact between the actuator (magnet) and switch not only permits such expediencies as the use of adhesive tape to affix components but opens the way to unique reed switch applications. An example which has come to the writer's attention is the control of fluid level or flow rate by use of a small permanent magnet floating within a glass tube to actuate a reed switch outside the tube.

The reed-switch package is well suited for experimental work. The leads are fairly long, easily trimmed to a desired length, quite flexible, and readily soldered. As a result, the capsule can be handled in much the same manner as a resistor or capacitor. Furthermore, the cost is low enough that it can be considered expendable to the same degree as many other small components.

1. O. M. Hovgaard and G. E. Perreault, "Development of Reed Switches and Relays," *Bell System Technical Journal*, Vol. 34, p. 309, March 1955.
2. R. L. Peek, Jr., "Magnetization and Pull Characteristics of Mating Magnetic Reeds," *Bell System Technical Journal*, Vol. 40, p. 523, March 1961.

Fig. 2—Application of reed switch to determine influence of series grid resistor.

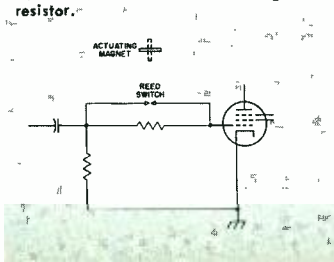
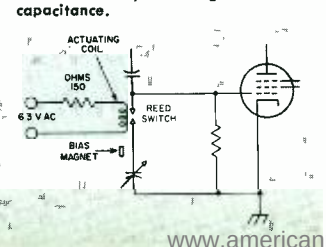


Fig. 3—Application of reed switch to induce 60-cycle repetitive transient caused by added grid-cathode capacitance.



A High-Quality Phonograph Pickup Arm for Professional Use

Dr. J. G. Woodward, *RCA Laboratories Princeton, N. J.*

Final Manuscript received August 17, 1964

Marked improvements in stereophonic pickups have been made in the past few years. In particular, increased compliance (reduced stiffness of the stylus mechanism) has permitted the vertical tracking force to be reduced to about two grams, with a consequent reduction in record wear. Unfortunately, the development of the pickup arms has lagged to the point where we cannot always realize the advantages of the improved pickups. A study of pickup arms, undertaken at the request of the Broadcast and Communications Products Division, has yielded a new pickup arm that eliminates most of the drawbacks of existing arms.

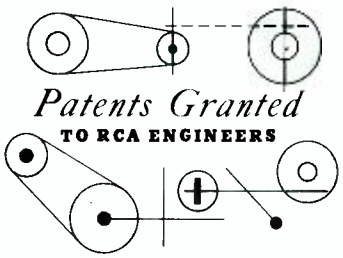
The pickup arm, shown in the photograph below, is for professional use with a magnetic pickup similar in characteristics to that now used in RCA's professional-quality equipment. The pickup arm could be mounted in our current-production 12-inch turntable by merely enlarging an existing hole in the motor board.

Several of the arm's improved characteristics required mechanical innovation or re-tailoring of conventional approaches. For example, even for slightly warped records, the low stylus pressure has made it difficult to maintain proper stylus contact with the groove walls. This contact was improved by making the arm of lightweight aluminum tubing to reduce its inertia and by use of instrument-type jewel bearings to reduce bearing friction. In addition, the tracking capability was improved by a system of counterweights that eliminates all tendency of the free arm to swing in any direction when the turntable is tilted.

For minimum distortion, the axis of the pickup should always be tangent to the groove, but this is impossible because the arm swings about a fixed pivot, which changes the angle between the groove and the pickup axis as the pickup moves from the edge toward the center of the record. The average distortion throughout the record was minimized by proper choice of pivot point and arm shape. Unfortunately, this necessary choice of geometry leads to a *skating force*, i.e., there is a component of the frictional drag on the stylus that pulls the pickup toward the center of the record and unbalances the stereo channels. No simple spring will balance out this skating force, but a novel system of springs and levers was devised that we believe could provide the first satisfactory compensation of the skating force over the entire playing surface.

There are several other improvements in the new arm. The major resonances have been moved to below the lowest frequency in the recorded material. In addition, the pickup can be lifted from and lowered onto the record by means of a lever conveniently located on the mounting base of the arm.

Fig. 1 — Improved professional phonograph pickup arm.



AS REPORTED BY RCA DOMESTIC PATENTS, PRINCETON

BROADCAST AND COMMUNICATIONS PRODUCTS DIV.

3,109,620—Transistor Clamp, November 5, 1963; G. M. Buivid (Patent assigned to U.S. Government)

3,145,321—Beam Current Stabilization in a Cathode Ray Tube, August 18, 1964; K. Sadashige

3,147,387—Electrical Circuit Having Voltage Divider Effecting Priming and Gates Effecting Sequence, September 1, 1964; M. Silverberg

ELECTRONIC COMPONENTS AND DEVICES

3,137,551—Ultra High Vacuum Device, June 16, 1964; J. T. Mark (Assigned to U.S. Government)

3,144,611—Reflex Amplifier Circuit with Reduction of Minimum Volume Control Play-Through Effect, August 11, 1964; H. M. Kleinman and L. Plus

3,145,318—Cathode Grid Assembly for Electron Gun, August 18, 1964; R. C. Paull

3,146,515—Method of Making an Electron Tube, September 1, 1964; F. R. Ragland, Jr.

3,147,053—Method of Sealing Vacuum Tubes, September 1, 1964; G. N. Phelps

3,150,965—Method of Producing Gallium, September 29, 1964; A. Mayer

3,151,004—Semiconductor Devices, September 29, 1964; R. Glicksman and E. T. Casterline

3,151,377—Method of Manufacturing Electron Tube, October 6, 1964; D. D. List

3,151,381—Electron Tube Assembly Apparatus, October 6, 1964; R. H. Hedel

3,151,388 — Assembly Device, October 6, 1964; K. A. Wroblewski

3,151,635—Apparatus for and Method of Cutting and Forming Wire Sections, October 6, 1964; H. Levine

3,151,636—Manufacture of Vacuum Tube Grids, October 6, 1964; R. Mahr and C. W. Lindsley

3,151,637—Apparatus for Producing RCA Heaters for Plural Purpose Vacuum Tubes, October 6, 1964; H. Levine

3,151,819—Detection Apparatus, October 6, 1964; J. L. Hodgdon

DEFENSE ELECTRONIC PRODUCTS

3,143,588—Range Measuring System, August 4, 1964; P. J. Donald and W. E. Martin

3,143,660—Stabilized Negative Resistance Diode Circuit, August 4, 1964; M. M. Kaufman and F. N. Weigel

3,143,662—Tunnel Diode Amplifier Employing Alternating Current Bias, August 4, 1964; J. J. Hill and M. M. Kaufman

3,141,073—High Speed Rotary Switch with Contact Cleaning Means, July 14, 1964; A. C. Stocker, F. Wendzel, W. Rolke and K. G. Kaufman (assigned to U.S. Government)

3,150,976—Electrostatic Printing, September 29, 1964; S. W. Johnson

3,152,217—Heat Dissipating Shield for Electronic Components, October 6, 1964; A. V. Balchaitis

HOME INSTRUMENTS DIVISION

3,143,686—Flyback Transformer and Transistorized Deflection Circuit, August 4, 1964; R. A. Daniel

3,144,598—Bi-directional Motor Control Circuit, August 11, 1964; J. F. Merritt

3,147,056 — Protective Interlock Structure, September 1, 1964; H. Mendelson

3,147,630—Tuning Control Mechanism, September 8, 1964; E. J. Sperber and N. G. Kelln

3,148,331—Tunnel Diode Converter Utilizing Two Tunnel Diodes, September 8, 1964; D. J. Carlson

3,148,332—Signal Translating System with Isolation of Input Terminals from Output Terminals, September 8, 1964; G. E. Theriault

ELECTRONIC DATA PROCESSING

3,147,054—Test Pointer Extender for Circuit Boards, September 1, 1964; R. A. Alexander, H. H. Olson

3,151,311—Magnetic Core Control Circuit for Actuating Solenoid Devices Utilizing a Single Sense Amplifier, September 29, 1964; G. Spector and J. V. Fayer

RCA LABORATORIES

3,146,205—Lithium-Manganese Ferromagetic Ferrite Core, August 25, 1964; I. J. Hegyi

3,130,342 — Photoelectric Cell, April 21, 1964; G. A. Morton (issued to U.S. Government)

3,148,342—Stereophonic Signal Transmission System, September 8, 1964; F. R. Holt

3,149,995—Magnetic Recording Element and Method of Preparation Thereof, September 22, 1964; H. Bauer

3,150,995 — Magnetic Recording Element Having Diisocyanate-Based Elastomer Binder and Method for Preparing Same, September 29, 1964; H. Bauer

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DATES *and* DEADLINES

PROFESSIONAL MEETINGS AND CALLS FOR PAPERS

Meetings

Nov. 4-6, 1964: NEREM (NORTHEAST ELEC. RES. AND ENG. MTG.), Region 1, IEEE; Commonwealth Armory and Somerset Hotel, Boston, Mass. *Prog. Info.:* Dr. James E. Storer, Boston Section IEEE, 313 Wash. St., Newton 58, Mass.

Nov. 16-18, 1964: 17TH ANN. CONF. ON ENG. IN MEDICINE AND BIOLOGY, IEEE-ISA (G-BME); Cleveland-Sheraton Hotel, Cleveland, Ohio. *Prog. Info.:* Dr. Peter Frommer, Cincinnati Genl. Hospital, Cincinnati 29, Ohio.

Nov. 16-18, 1964: SPACE SIMULATION TESTING CONF., AIAA, G-AS; Pasadena, Calif. *Prog. Info.:* IEEE Headquarters, Box A, Lenox Hill Station, New York, N. Y.

Nov. 16-19, 1964: 10TH CONF. ON MAGNETISM AND MAGNETIC MATLS., IEEE, AIP, et al. Raddison Hotel, Minneapolis, Minn. *Prog. Info.:* J. D. Goodenough, Lincoln Labs., Lexington 73, Mass.

Nov. 23-24, 1964: 1964 MAECON, Kansas City Section, IEEE; Kansas City, Mo. *Prog. Info.:* Robert E. Barnes, Wilcox Electric Co., Inc., 14th and Chestnut Sts., Kansas City 27, Mo.

Nov. 23-24, 1964: SYMP. ON THE DEFINITION AND MEASUREMENT OF SHORT TERM FREQUENCY STABILITY, IEEE; Goddard Space Flight Center, Greenbelt, Md. *Prog. Info.:* C. Boyle, Code 207, Goddard Space Flight Center, Greenbelt, Md.

Dec. 3-4, 1964: 15TH ANN. VEHICULAR COMM. SYMP., G-VC, IEEE; Cleveland-Sheraton, Cleveland, Ohio. *Prog. Info.:* R. E. Bloor, Ohio Bell Tel. Co., 700 Prospect Ave., Cleveland, Ohio.

Dec. 21-23, 1964: AMERICAN PHYSICAL SOC.; Berkeley, Calif. *Prog. Info.:* W. Whaling, Regional Secy, Calif. Inst. of Tech., 1201 E. Calif. St., Pasadena, Calif.

Dec. 26-31, 1964: SYMP. ON GENL. SYSTEMS KNOWLEDGE, G-CT, IEEE; AAAS Mtg., Montreal, Canada. *Prog. Info.:* Omar Wing, Dept. of EE, Columbia Univ., New York, N.Y.

Calls for Papers

Jan. 5-8, 1965: SOLID-STATE PHYSICS; Inst. of Physics and Physical Soc.; U. of Bristol. **Deadline:** Abstracts, **11/20/64.** *TO:* D. A. Greenwood, H. H. Wills Physics Lab., Royal Fort, Bristol 8: Administration Assistant, IPPS, 47 Belgrave Sq., London, S.W. 1, England.

Feb. 17-19, 1965: INTL. SOLID STATE CIRCUITS CONF., IEEE, G-CT, Univ. of Pa.; Univ. of Pa. and Sheraton Hotel, Phila., Pa. **Deadline:** Abstracts, **10/26/64.** *TO:* G. B. Herzog, RCA Labs., Princeton, N.J.

March 10-12, 1965: PARTICLE ACCELERATOR CONF., G-Nuclear Science; Wash., D.C. **For Deadline Info.:** R. S. Livingston, Oak Ridge Natl. Lab., PO Box X, Oak Ridge, Tenn.

Apr. 13-15, 1965: NATL. TELEMETERING CONF., IEEE, AIAA-ISA; Shamrock Hilton, Houston, Texas. **Deadline:** Abstracts, approx. **12/1/64.** *TO:* R. W. Towle, Philco Corp., Western Dev. Labs., 3825 Fabian Way, Palo Alto, Calif.

Apr. 14-15, 1965: 1965 ELECTRONICS AND INSTRUMENTATION CONF. AND EXHIBIT, IEEE and ISA, Cinc. Sect.; Cincinnati Gardens, Cincinnati, Ohio. **For Deadline Info.:** IEEE Headquarters, Box A, Lenox Hill Station, New York, N.Y.

Apr. 21-23, 1965: SOUTHWESTERN IEEE CONF. AND ELEC. SHOW (SWIEEECO), Region 5, IEEE; Dallas Memorial Auditorium, Dallas, Texas. **Deadline:** Abstracts, approx. **1/1/65.** *FOR INFO.:* E. F. Sutherland, Genl. Radio Co., 2501-A Mockingbird Lane, Dallas, Texas.

Apr. 21-23, 1965: 1965 INTL. NONLINEAR MAGNETICS CONF. (INTERMAG), IEEE; Sheraton Park Hotel, Wash., D.C. **For Deadline Info.:** E. W. Pugh, IBM Components Div., Poughkeepsie, N.Y.

May 4-6, 1965: 5TH ANN. PACKAGING INDUSTRY CONF., IEEE; Milwaukee Inn, Milwaukee, Wisc. **For Deadline Info.:** IEEE, Box A, Lenox Hill Station, New York, N.Y.

May 5-7, 1964: 1965 MICROWAVE THEORY AND TECHNIQUES SYMP., G-MTT, IEEE; Jack Tar Harrison Hotel, Clearwater, Fla. **Deadline:** Abstracts, **11/15/64.** *TO:* J. E. Pippin, Sperry Microwave Elec. Co., Box 1828, Clearwater, Fla.

May 5-7, 1965: ELECTRONIC COMPONENTS CONF. (ECC), IEEE-EIA; Marriott Motor Hotel, Wash., D.C. **Deadline:** Abstracts, approx. **12/1/64.** *FOR INFO.:* IEEE Headquarters, Box A, Lenox Hill Station, New York, N.Y.

May 10-12, 1965: NAECON (NATL. AEROSPACE ELECTRONICS CONF.), G-ANE, AIAA, Dayton, Section, IEEE; Dayton, Ohio. **Deadline:** Abstracts, approx. **2/1/65.** *FOR INFO.:* IEEE Dayton Office, 1414 E. 3rd St., Dayton 2, Ohio.

May 13-14, 1965: SYMP. ON SIGNAL TRANSMISSION AND PROCESSING, G-CT, IEEE; **For Deadline Info.:** IEEE Headquarters, Box A, Lenox Hill Station, New York, N.Y.

May 19-21, 1965: POWER INDUSTRY COMPUTER APP. CONF. (PICA), G-P and Fla. Westcoast Section; Jack Tar Hotel, Clearwater, Fla. **For Deadline Info.:** L. F. Kennedy, Genl. Elec. Co., 1 River Rd., Schenectady, N.Y.

June 7-9, 1965: INTL. SYMP. ON GLOBAL COMMUNICATIONS (GLOBECOM VII), G-ComTech, Denver Boulder Sect.; Univ. of Colo. and NBS Labs., Boulder, Colo. **For Deadline Info.:** R. C. Kirby, NBS, Boulder, Colo.

June 21-25, 1965: SAN DIEGO SYMP. FOR BIOMEDICAL ENG., IEEE, US Naval Hosp.; San Diego, Calif. **For Deadline Info.:** Dean L. Franklin, Scripps Clinic and Res. Found., La Jolla, Calif.

June 22-25, 1965: JOINT AUTOMATIC CONTROL CONF., IEEE-ASME, AIChE, ISA; Rensselaer Polytech Inst., Troy, N.Y. **Deadline:** Abstracts, **11/15/64.** *TO:* Prof. James W. Moore, Univ. of Va., Charlottesville, Va.

Aug. 23-27, 1965: 6TH INTL. CONF. ON MEDICAL ELEC. AND BIOLOGICAL ENG., (IFMEBE) Tokyo, Japan. **Deadline:** Abstracts, approx. **4/30/65.** *FOR INFO.:* Dr. L. E. Flory, RCA Labs., Princeton, N.J.

Aug. 24-27, 1965: WESCON, IEEE, WEMA; Cow Palace, San Francisco, Calif. **Deadline:** Abstracts, approx. **4/15/65.** *FOR INFO.:* IEEE L. A. Office, 3600 Wilshire Blvd., Los Angeles, Calif.

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Tape Playback Amplifier, Low Noise Transistorized—J. J. Davidson (Record Div., Indpls.) *Journal of the Audio Engineering Society*, Oct. 1963

ATOMIC THEORY; PHENOMENA

Kramers-Gaunt Formula, High-Intensity Correction to the—W. Zernick (Labs, Pr.) Conf. on Quantum Electrodynamics of High Intensity Photon Beams, Durham, N. Carolina, Aug. 26-27, 1964

Secondary Breakdown: Two Modes and One Mechanism—R. Rosenweig, D. R. Carley (ECD, Som.) IEEE Solid-State Device Research Conf., Boulder, Colo., July 1-3, 1964

Two-Photon Ionization of Atomic Hydrogen—W. Zernik (Labs, Pr.) *Physical Review*, July 6, 1964

CHECKOUT; MAINTENANCE

Accuracy in Automatic Test Equipment—M. C. Kidd (DEP-ASD, Burl.) *IEEE Transactions on Aerospace*, Vol. 2, No. 3, July 1964

Maintenance Time Specification—B. L. Retterer, G. H. Griswold (Svc. Co., Cherry Hill) 10th Nat'l. Symp. on Reliability & Quality Control, Jan. 7-9, 1964

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Integrated Amplifier Analysis—L. C. Drew, A. G. Atwood (DEP-ASD, Burl.) *Electronic Industries*, July 1964

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Effective Industrial Packages Rest on Step-by-Step Development—T. W. Kisor (ECD, Som.) *Package Engineering*, July 1964

Films for Packaging, Problems in Using—H. W. Hittie (Record Div., Indpls.) *Management Bulletin*, No. 25, 1963

Rack Panel Mounting, Cost Reduction—RCA TR-22 Tape Equipment—R. L. Holtzheimer (BCD, Cam.) Nat'l. Electronic Packaging and Production Conf., N. Y., Hilton Hotel, June 9, 1964

COMMUNICATIONS, DIGITAL

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System Reliability: Redundant Network—G. D. Weinstock (DEP-CSD, N.Y.) *Electro-Technology*, Aug. 1964

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Vehicular Communications Transmitter, 150-Mc, 15-Watt, Using RCA Transistors and Varactor Diodes—H. C. Lee, S. J. Matyckas, R. Minton (ECD, Cam.) *Electronic Industries*, Aug. 1964

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Demodulator, A Solid-State Ultra-Linear Wideband FM—R. Glasgal (DEP-CSD, N.Y.) *Audio*, Vol. 48, No. 5, May 1964

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COMPUTER APPLICATIONS

Display Systems, Computer in—W. Helbig (DEP-ASD, Van Nuys) Society for Information Display, San Fernando Valley Group, July 1, 1964

Identification and Information Retrieval—F. H. Fowler, Jr. (DEP-CSD, Cam.) *Computers and Data Processing*, June 1964

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Microcore—Backward Diode Shift Register—G. R. Briggs (Labs, Pr.) *Proceedings of the 1964 Intermag Conference*, Wash., D.C., April 6, 7, 8, 1964

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P-N Junctions as Radiation Sources—M. F. Lamorte, R. B. Leibert (ECD, Som.) *Electronics*, July 13, 1964

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PLASMA

Post-Pinch Oscillations in Impact-Ionization-Produced Plasma—M. Glicksman (Labs, Pr.) Symp. on Plasma Effects in Solids, 1964 Int'l. Conf. on the Physics of Semiconductors, Paris, France, July 12-24, 1964; *Proc. of Conf.*

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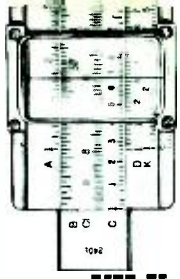
AUTHOR INDEX

Subject listed opposite each author's name indicates where complete citation to his paper may be found in the subject index. Where an author has more than one paper, his name is repeated for each.

Engineering NEWS *and* HIGHLIGHTS



TV Cameras Similiar to Ranger VII Used on Experimental Nimbus Satellite; Advanced Versions To Be Used On Future Five "Wheel" Tiros Operational Weather Satellites

Television cameras similar to those of Ranger VII were included on the NIMBUS satellite, designed to photograph weather conditions for the nation's meteorologists. The experimental NIMBUS carried two different TV systems one of which has cameras similar to those aboard RANGER VII. The camera systems for both spacecraft were designed and built at RCA in a program headquartered at the DEP Astro-Electronics Division Princeton.

(*For technical descriptions, see* article by B. Miller "RANGER TV Subsystem," which was mailed as an insert with RCA ENGINEER, *10*-2, August-Sept. 1964 and the article by M. Mesner, published in that issue. *For background see* article by Callais, et al, "NIMBUS—An Advanced Meteorological Satellite" in RCA ENGINEER, *9*-1, June-July 1963.)

Modified versions of the advanced NIMBUS cameras will be used later on the five new WHEEL TIROS satellites which have been selected as the Weather Bureau's first *operational* space system to be orbited in late 1965. The WHEEL TIROS satellites are being designed and built for NASA by the Astro-Electronics Division.

NIMBUS was a research spacecraft designed to test new TV camera systems in conjunction with an earth-oriented control system designed to keep the satellite's cameras always pointing toward the earth. In a near-polar orbit, this permitted photographs of weather conditions over the entire globe at least once each day.

In addition to the AVCS and APT camera systems, RCA has provided the special tape recording and multiplexing equipment for NIMBUS's high-resolution infrared sensing system, the huge solar cell paddles and batteries for the power system, with associated regulating equipment, and the clock (command) receiver. The two paddles, each 8 feet tall and 2.75 feet wide, are among the largest ever designed for a spacecraft. Together they carry approximately 11,000 solar cells.

DR. McCOY HONORED

Dr. Donald S. McCoy, RCA Laboratories, Princeton, New Jersey, has been selected by the U.S. Junior Chamber of Commerce to be included in its 1964 annual publication of *Outstanding Young Men of the Nation.* The selection was made by the national review board primarily on the basis of Dr. McCoy's participation in the David Sarnoff Industry-Science teaching program. Dr. McCoy is a member of Sigma Xi, Tau Beta Pi, and is the 1964-1965 chairman of the Princeton section of the IEEE.

V. E. TROUANT HONORED FOR DISTINGUISHED 43-YEAR CAREER

On Sept. 21, 1964, **V. E. Trouant,** formerly Chief Engineer of the Broadcast and Communications Products Division, and most recently Chief Technical Administrator of that Division, was honored by a group of his professional associates at a testimonial dinner in Camden, on the occasion of his retirement from RCA. Mr. Trouant's career has been outstanding both as an engineer and in the management of RCA's Broadcast engineering activities. In addition, he has been a member of the RCA ENGINEER Advisory Board, and certainly one of its most valued consultants.

Mr. Trouant received his BSEE from the University of Maine in 1921. With Westinghouse Electric, he specialized in automotive ignition systems and later transferred to radio transmitter engineering. Coming to RCA in 1933, Mr. Trouant designed one of the early 50-kilowatt broadcast transmitters. He continued as a supervising engineer until his 1945 appointment as Manager of the Communication and Radio Frequency Section. In 1951, he was appointed Chief Design Engineer for Standard Products, and subsequently became Chief Engineer of the Broadcast Division.

DEP-ASD, VAN NUYS, GETS $27 MILLION CONTRACT FOR 19 COMPUTER SYSTEMS FOR SATURN CHECKOUT AND LAUNCH

DEP Aerospace Systems Division, Van Nuys, recently received a $27 million contract from NASA to build 19 ground computer systems to be used for the checkout and launch of the SATURN 1B and SATURN V launch vehicles.

The systems, to be built at Van Nuys, Calif., for NASA's Marshall Space Flight Center, Huntsville, Alabama, include the RCA 110A computer, conventional input-output equipment, digital and analog stimulus and measuring equipment, and high-speed data communications equipment. The new contract brings to 26 the number of 110A systems procured by NASA for the Saturn program. (*For background, see* "High-Speed Computer-Controlled Checkout System for SATURN," by W. M. McCord, RCA ENGINEER, *8*-6, April-May 1963.

DR. ROBINSON NAMED TO HEAD NEW BRANCH OF DEP-MSR ENGINEERING DEPARTMENT

Appointment of **Dr. Arthur S. Robinson** as Manager of the Systems and Advanced Technology group, DEP Missile and Surface Radar Division, Moorestown, N.J., was announced recently by **R. A. Newell,** Chief Engineer of the Division.

As head of this newly created branch of the Engineering Department, Dr. Robinson will give technical direction to all systems engineering and advanced technology programs in the Division. He also will have technical responsibility for new business activities, both in developing new program concepts and in expanding the potential of eixsting systems.

Dr. Robinson joined RCA in April of this year, with a distinguished background in management and high-level research and engineering. As a staff engineer, to **Dr. H. J. Watters,** Chief Defense Engineer of DEP, he participated in systems and applied research activities in DEP's four operating divisions.

R. G. NEUHAUSER RECEIVES SMPTE GOLD MEDAL AWARD FOR 1964

Robert G. Neuhauser, Leader, Image Orthicon Advanced Development ECD, Lancaster, Pa. has won the *1964 David Sarnoff Gold Medal Award* of the Society of Motion Picture and Television Engineers (SMPTE). The award recognizes meritorious achievement in television engineering, citing that Mr. Neuhauser's contributions to improvements in camera-tube design and techniques of operation "have constituted one of the outstanding elements of progress in the television art of the last few years." Formal presentation of the medal was made during the Society's semiannual Technical Conference Sept. 27-Oct. 2 at the Commodore Hotel in New York.

Specifically cited is Mr. Neuhauser's leadership in the use of the vidicon tube as a replacement for the iconoscope in film reproduction in the development of cold-seal and electrostatically focused vidicons, and in the development of precision image-orthicon camera tubes for color television. He has published a number of technical papers in the *Journal of the SMPTE* and elsewhere. Two of his SMPTE papers have won honorable-mention awards from the Society. Mr. Neuhauser is a member of SMPTE, of the AAAS, and of the Society for Social Responsibility in Science, and has been recommended by RCA for the "outstanding young electrical engineer" award of Eta Kappa Nu, honorary electrical engineering society. Mr. Neuhauser's most recent RCA ENGINEER paper appeared in the last issue, *10*-2, August-September 1964 entitled "Developments in Electron Optics Produce Two New Lines of Vidicon Tubes."

LABS OFFER NEW PROGRAM OF 1-YEAR POST-DOCTORAL AND VISITING-PROFESSOR APPOINTMENTS

Inauguration of a novel program of temporary post-doctoral research appointments by RCA Laboratories to be carried out at Princeton, N. J. has been announced by **Dr. James Hillier,** Vice President, RCA Laboratories.

The program will offer one-year staff appointments, renewable for a second year, in areas of research where significant work can be done during the time of appointment. It is designed for both university professors on sabbatical leave, and outstanding new PhD graduates who are interested in post-doctoral experience in industrial research. Appointees will be given the title of "Visiting Members of the Technical Staff." According to **Dr. D. A. Ross,** who maintains graduate-level liaison with universities, and who will be director of the new program, selection of appointees will be on the basis of interest in a current RCA research program in which significant results can be anticipated in one or two years. No more than five appointees will be named in any year. Visiting staff members will receive the same remuneration and company-paid benefits as permanent staff members during the term of their appointment.

. . . PROMOTIONS . . .

to Engineering Leader & Manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parenthesis.

Electronic Data Processing

J. P. Beltz: from Engr. Class A to *Leader, Design & Dev. Engineers* (J. L. Miller) Optical Character Reading Machines.

J. Haney: from Sr. Mbr., Dev. & Design Engrg. Staff to *Leader, Technical Staff.*

Aerospace Systems Division—DEP

Henry Brodie: from Sr. Project Mbr. to *Leader, Technical Staff* (R. Gildea) Data Processing Engineering, Burlington.

C. D. Brudos: from Sr. Mbr. D&D Engr. Staff to *Leader, D&D Engr. Staff* (F. Worth) Van Nuys.

R. F. Powell: from Sr. Mbr. Technical Staff to *Leader, Technical Staff* (R. D. Crawford) Reliability & Standards Eng., Burlington.

Astro-Electronics Division—DEP

M. Berry: from Engr. to *Leader, Engineers* (M. Mesner, Mgr., TV Cameras) Princeton.

E. Burnett: from Sr. Engr. to *Leader, Engineers* (S. Gubin, Mgr. Electronic Systems Eng.) Princeton.

Electronic Components & Devices

L. P. Fox: from Eng. Ldr., Prod. Dev. to *Mgr., Product Eng.* (R. Wissolik) Somerville.

H. N. Hillegass: from Engr., Prod. Dev. to *Eng. Leader, Prod. Dev.* (Mgr., Application Eng. Lab.) Lancaster.

V. C. Kneizys: from Jr. Engr., Mfg. to *Mgr. Quality Control* (Mgr., Plant Quality Control) Lancaster.

J. W. Young: from Gen. Foreman, Mfg. to *Mgr., Mfg. Standards* (R. J. Hall, Mgr., Findlay Plant) Findlay, Ohio.

Broadcast and Communications Products Div.

K. Sadashige: from Engr., Design & Dev., to *Leader, Design and Development Engineers* (A. C. Luther) Tape Equip., Projector & Scientific Instr. Eng., Camden.

RCA Service Company

R. V. Lisle: from Assoc. Engr. to *Mgr., Calibration Services* (H. Laessle) Southwestern Area Field Eng. Operations.

B. H. Morefield: from Field Engr. to *Mgr., Radar Shipboard* (D. L. Ely) Marine Instrumentation.

R. B. Pickett: from Field Engr. to *Leader, Engineers* (K. J. Starzinger) Eleuthera Instrumentation Station.

STAFF ANNOUNCEMENTS

RCA: Effective Sept. 4, 1964, **Dr. D. H. Ewing** was appointed Staff Vice President. Dr. Ewing will continue to serve as Chairman of the RCA Education Committee and will be available for services to the divisions and subsidiaries as assigned. Dr. Ewing will continue to report to **Dr. E. W. Engstrom,** President, RCA.

Electronic Components and Devices: Effective Sept. 1, 1964, **W. H. Painter,** Division Vice President and General Manager, Commercial Receiving Tube and Semiconductor Division, appointed **F. R. Buchanan,** Manager, Memory Products Operations Department.

Effective Sept. 1, 1964, **R. M. Cohen,** Manager, Engineering, Commercial Receiving Tube and Semiconductor Operations Department, announced his organization as follows: **W. E. Babcock,** Manager, Special Products Development; **M. Bondy,** Manager, Receiving Tube Design; **J. W. Englund,** Manager, Entertainment Applications; **P. L. Farina,** Administrator, Special Engineering Projects; **H. V. Kettering,** Manager, Semiconductor Design; **R. R. Painter,** Manager, Computer and Communications Applications; **R. N. Peterson,** Manager, Nuvistor Development; and **L. R. Shardlow,** Manager, Engineering Services Laboratories.

Research and Engineering: Effective Sept. 8, 1964, the Operations Research function was transferred to the Vice President, Research and Engineering. **F. Edelman** continues as Director, Operations Research, and will report to **Dr. G. H. Brown,** Vice President, Research and Engineering.

Effective September 15, 1964, **F. S. Misterly,** Staff Vice President, Patent Operations announced the organization of Patent Operations as follows: **G. H. Bruestle,** Manager, Domestic Patents—Electronic Components and Devices; **P. G. Cooper,** Director, Foreign Patents; **E. J. Norton,** Manager, Domestic Patents—Engineering; **J. V. Regan,** Manager, Domestic Patents—Electronic Data Processing; **A. Russinoff,** Patent Counsel, Interferences and Litigation; **E. M. Whitacre,** Manager, Domstic Patents—Home Instruments; and **M. S. Winters,** Manager, Patent Plans and Services.

ECD Industrial Tube and Semiconductor Division: **H. K. Jenny,** Manager, Microwave Engineering, Microwave Tube Operations Dept., announces effective August 1, 1964, the organization of Microwave Engineering as follows: **W. F. Beltz,** Manager, Microwave Engineering Services; **W. J. Dodds,** Manager, Solid State Device Engineering; **M. Nowogrodzki,** Manager, Microwave Engineering Programs; **F. Sterzer,** Manager, Microwave Applied Research, **F. E. Vaccaro,** Manager, Traveling-Ware Tube and Pencil Tube Engineering; and **H. M. Wolkstein,** Manager, Advanced Product Development.

MEASUREMENT AGREEMENT IN DEP

Product Assurance is concerned with achieving the best value in delivered products and services in terms of reliability, maintainability, quality, and overall effectiveness for customer use. There are a number of disciplines associated with providing meaningful value; those dealing with measurement are fundamental to all the others. Because of this, the DEP Product Assurance Quality Council has established the *Calibration and Measurements Standards Committee* to coordinate the uniform and consistent implementation of measurement disciplines throughout DEP.

The Committee's functions include: 1) Providing a place for discussing and resolving the problems of achievement of measurement agreement within DEP, 2) Coordinating the implementation of uniform and compatible calibration systems and thereby facilitating the interchange of workload and equipment among the four DEP Divisions; 3) Providing maximum meaningful value to the customer and DEP through calibration systems that are in agreement in administrative, operational, and technical factors, and which can operate within the minor differences of disciplines enforced by the various contracting agencies.

The DEP Calibration and Measurements Standards Committee meets quarterly with its divisional representatives to discuss and improve the operation of calibration systems. The areas considered include the attainment of agreement in records, equipment handling, calibration techniques, and standards as well as agreement in technical results. Task groups study uniform records and other documentation, methods of establishing calibration periods, and technical measurement agreement.

Detailed information on the committee and its activities may be obtained from **H. S. Ingraham, Jr.,** *Camden, Bldg. 1-6-1, PC-5601.*

LICENSED ENGINEERS

B. R. Czorny, EC&D, Somerville, PE-13518, N.J.

C. G. Dietsch, RCA Communications, N.Y., PE-14233, N.Y.

F. H. Erdman, Labs, Pr., PE-872, Wash., D.C.

G. R. Field, M&SR, Moores., PE-13595, N.J.

R. S. Fow, EDP, Camden, PE-004391E, Pa.

L. B. Hall, EC&D, Marion, PE-7084, Indiana

A. P. Hummer, EC&D, Marion, PE-17848, Ill.

W. Y. Pan, Dr., DEP-CSD, N.Y., PE-13594, N.J.

G. Polrivchak, EC&D, Somerville, PE-8119E, Pa.

E. W. Richter, DEP-ASD, Burl., PE-16238, Mass.

J. L. Seibert, NBC-NY, PE-4732EE, Calif. (correction 10-1)

B. D. Smith, DEP-ASD, Burl., PE-19349, Mass.

S. M. Solomon, DEP-CSD, N.Y., PE-38663, N.Y., PE-13053, N.J.

H. E. Thierfelder, DEP-AED, Princeton, PE-2440-E, Pa.

DEGREES GRANTED

R. E. Hartwell, DEP-ASD ..... MS, University of Pennsylvania
R. J. Konrad, ECD ..... MS, Purdue University
R. E. Winn, BCD ..... MSEE, University of Pennsylvania

SEMICONDUCTOR APPLICATIONS SEMINARS PRESENTED BY ECD ENGINEERS IN LOS ANGELES AND PALO ALTO

In August, a group of 600 were given a preview of new semiconductor applications at an RCA Solid-State Device Applications Seminar conducted by EC&D engineers in Los Angeles, Calif. At a similar earlier seminar in Palo Alto, Calif., a group of 200 were involved. The seminars are a continuing program sponsored by RCA distributors for computer, communications, industrial and military equipment design engineers representing original equipment manufacturers. An important aspect of these seminars is that EC&D engineers and managers who are directly concerned with development, design, and manufacture of these devices present the detailed technical information in the form of papers, and are available for questions and discussions on the spot. **E. O. Johnson,** Manager, Engineering, Technical Programs, EC&D, presided at both seminars. The one at Los Angeles included the following ten papers by EC&D engineers:

"Power Transistors for Audio-Frequency Applications"—**H. M. Kleinman**
"Transistor Circuit Design for 450 Mc and Above"—**P. E. Kolk**
"Design of Large-Signal VHF Transistor Power Amplifiers"—**R. Minton**
"Current Considerations for Silicon-Controlled Rectifier Circuits"—**D. E. Burke**
"High-Speed Power-Switching Applications"—**R. L. Wilson**
"Design of Microwave Power Sources Using Varactors"—**A. H. Solomon**
"The MOS Field-Effect Transistor"—**D. M. Griswold**
"Wide-Operating-Range Computer Switching Transistors"—**A. J. Bosso**
"Wide-Temperature Cores"—**H. P. Lemaire**
"High-Speed Magnetic Memory Systems and Their Applications"—**B. P. Kane**

The Palo Alto seminar included the first eight of the above ten papers. Mr. Johnson has stated that the philosophy behind these seminars is as follows: "With the rapid introduction of new and radically different semiconductor and high-speed magnetic memory devices . . . stronger relations are necessary between the component design engineer and the equipment design engineer. . . . The communications link between these two engineering areas must be shortened to take maximum advantage of the advances being made in solid state technology. These seminars represent a major step in shortening that link."

HIGH INTEREST IN COLOR SHOWN IN 34% RISE IN ORDERS FOR RCA TV BROADCAST EQUIPMENT IN FIRST HALF 1964

A high degree of customer interest in color television was reflected in a 34% increase in orders for RCA TV broadcast equipment for the first half of 1964 as compared with the same period a year ago. The rise in business was distributed generally over the full line of TV studio and transmitting apparatus and included new station plants and modernization of existing facilities. Noteworthy in the half-year record was the high degree of customer interest and increased sales activity in color TV equipment, particularly in the new "live" and film color cameras which RCA introduced to the trade earlier this year. (See RCA ENGINEER, Vol. 10, No. 2, Aug.-Sept. 1964.)

The broadcasting industry's continuing prosperity and the improved depreciation allowance on new items of capital equipment purchased by TV stations were major factors in the higher level of sales for the first half. Also credited is the Division's new line of broadcast equipment, demonstrated at the 1964 National Association of Broadcasters convention, which have stimulated the market beyond normal expectations.

The "new look" equipment line is the result of a major investment in product engineering, begun three years ago when solid state components suitable for broadcast gear first became available. The line includes cameras, TV tape recorders, and other items that are entirely solid state in design. This has had a marked impact on the equipment size, reliability and ease of operation and maintenance.

RCA ENGINEER BINDERS AVAILABLE

Wire-rod-type, brown, simulated-leather binders are available for binding back issues of the RCA ENGINEER. The binders are 9¼ x 12 x 3¼, and will hold about 10 issues each. (Six binders will house all issues since Vol. 1, No. 1). RCA ENGINEER copies (or similar size magazines) are held in place by wire rods (supplied) that run along the center fold of the magazine and snap in place (no need to punch holes or otherwise mutilate the issue). These binders may be ordered directly for two-week delivery as follows: Order by stock number and description *exactly as below;* make check or money order payable *directly to the vendor,* and specify method of shipment:

Binder, rod type, No. 1534, price $3.66 each.
ORDER FROM: *Mr. Shaeffer, A. Pomerantz & Co. 1525 Chestnut St., Philadelphia, Pa.*

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To enable RCA to maintain timely, accurate indexes (see *Pen & Podium,* this issue) to its technical papers all RCA engineers and scientists should notify *their Technical Publications Administrator* whenever one of their technical papers is published or presented before a technical society. The TPA should be given the exact name, volume number, and the date of the publication, and/or the exact name of the professional society meeting and the date the paper was presented. Furnishing such information will enable the RCA ENGINEER and the *RCA Review* to make their technical paper indexes more accurate and complete.

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The second quarter of 1964 has seen an exceptional increase in orders for the new RCA 3301 data system, as well as the RCA 3488 mass memory unit. Many of these orders were obtained in direct competition with the most recent computer systems announced by other manufacturers. That overall increase in sales and leases of RCA data processing equipment this year will surpass the substantial sales gain recorded in 1963. At the present time, there are more the 740 RCA computer systems either on order or in operation.

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