RCA ENGINEER *Staff*

W. O. Hadlock ..... Editor
E. R. Jennings ..... Assistant Editor
Mrs. C. S. Marchionni ..... Editorial Secretary
J. L. Parvin ..... Art Director
J. O. Gaynor ..... Photography

Engineering Editors

C. A. Meyer, Mgr., Commercial Engineering Technical Services, Electronic Components and Devices
T. T. Patterson, Mgr., Technical Publications, Electronic Data Processing Engineering
C. W. Sall, Technical Publications Administrator, RCA Laboratories
L. A. Thomas, Mgr., Publications Services Astro-Electronics Division
F. D. Whitmore, Technical Publications Administrator, Defense Electronic Products

Editorial Advisory Board

E. I. Anderson, Mgr., Operations, RCA Victor Home Instruments Division
A. D. Beard, Chief Engineer Electronic Data Processing
J. J. Brant, Director, Personnel
C. C. Foster, Mgr., RCA REVIEW
M. G. Gander, Mgr., Consumer Product Administration, RCA Service Co.
Dr. A. M. Glover, Division Vice President Technical Programs, Electronic Components and Devices
C. A. Gunther, Division Vice President, Technical Programs, DEP and EDP
E. C. Hughes, Administrator, Technical Committee Liaison, Electronic Components and Devices
W. C. Morrison, Assistant to the Chief Defense Engineer, Defense Electronic Products
D. S. Rau, Vice President Engineering, RCA Communications, Inc.
H. E. Roys, Chief Engineer, RCA Victor Record Division
D. F. Schmit, Staff Vice President, Product Engineering
C. M. Sinnett, Director, Product Engineering Professional Development
V. E. Trouant, Chief Engineer, Broadcast and Communications Products Division
Dr. H. J. Watters, Chief Defense Engineer, Defense Electronic Products
J. L. Wilson, Director, Engineering National Broadcasting Co., Inc.

OUR COVER

. . . a feasibility tunnel diode subsystem consisting of 40 gates. This subsystem was developed and fabricated as a part of an ultra-high-speed research and development contract which was initiated in mid-1957 as a joint effort of the Semiconductor and Materials Division in Somerville, the RCA Laboratories in Princeton, and RCA Electronic Data Processing in Camden. Eldon Cornish, Research and Development Engineer, Computer Advanced Development Activity, is shown explaining the operation of one of the basic circuits, a 350-megacycle OR gate. (See paper by Cooperman, this issue.)

Computer R&D at RCA

Electronic data processing—for the past decade these have been words of magical significance; words of promise in the reduction of highly repetitive tasks and increased operating efficiency, both most important in today's turbulent situation when we, as a nation, are literally in competition on a world-wide basis.

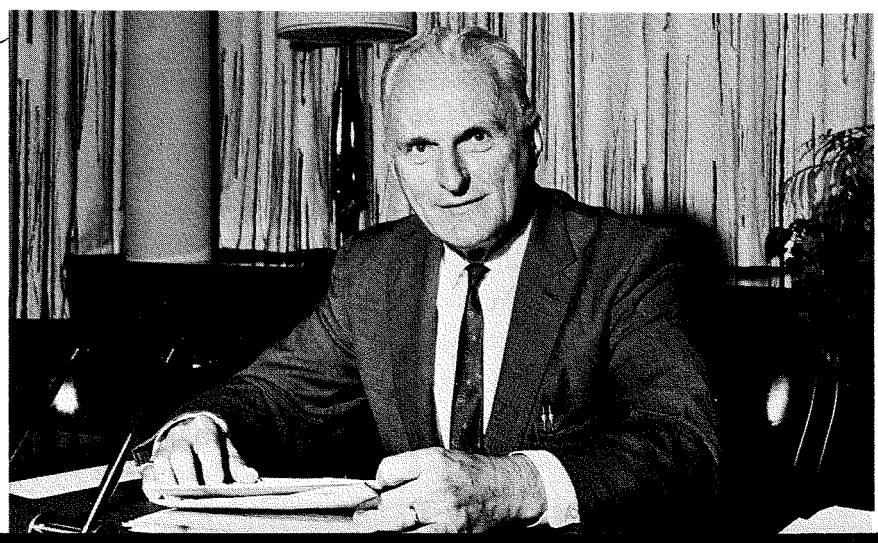
Thirty-three years ago, as RCA entered the equipment manufacturing field, the EDP concept was at most just an idea in some scientist's mind. I remember very clearly the counsel my uncle gave me as I considered leaving the established environment of the General Electric Company. He stated, "Why leave GE with its diversified interests to join a new venture specializing in radio sets and phonographs?" It was a difficult question to answer in the face of facts but even then it was clear that radio was on the threshold of a whole new unpredictable future.

With all our fine progress today, it can again be said that we still stand virtually on the threshold of new electronic wonders. This issue emphasizes *R&D*—the advanced research, development, and design so vital to RCA's dynamic electronic data processing business.

It is a great business with which to be associated, and to engineers and scientists who have imagination and a desire to live to their fullest potential, many hints and suggestions are contained in these pages.

Arnold K. Weber

Arnold K. Weber
Division Vice President and General Manager
Electronic Data Processing
Radio Corporation of America



RCA ENGINEER

VOL. 9, NO. 2
AUG.-SEPT. 1963

CONTENTS

A TECHNICAL JOURNAL PUBLISHED BY **RADIO CORPORATION OF AMERICA,** PRODUCT ENGINEERING 2-8, CAMDEN, N. J.

● To disseminate to RCA engineers technical information of professional value. ● To publish in an appropriate manner important technical developments at RCA, and the role of the engineer. ● To serve as a medium of interchange of technical information between various groups at RCA. ● To create a community of engineering interest within the company by stressing the interrelated nature of all technical contributions. ● To help publicize engineering achievements in a manner that will promote the interests and reputation of RCA in the engineering field. ● To provide a convenient means by which the RCA engineer may review his professional work before associates and engineering management. ● To announce outstanding and unusual achievements of RCA engineers in a manner most likely to enhance their prestige and professional status.

An index to RCA ENGINEER articles appears annually in the April-May issue.

Copyright 1963
Radio Corporation of America
All Rights Reserved
PRINTED IN U.S.A.

The Engineer and the Corporation

PATENTS, RCA, AND YOU

O. V. MITCHELL, Director
Domestic Patents
Research and Engineering
Princeton, N. J.

IN RELATIVELY recent years a mistaken idea has developed among some of our engineering personnel to the effect that RCA is no longer interested in patents. *This emphatically is not the case.* We do want valid patents on good ideas; such patents constitute a valuable asset to RCA.

This paper covers the essential factors involved in obtaining patents—with special emphasis on how important it is for the individual engineer or scientist to *correctly* and *promptly* document the invention so that our rights to it can be legally upheld, should they be contested.

Before such useful patents can be obtained, it is necessary that the RCA engineer or scientist first recognize the need for an invention and then generate inventions of such high caliber that our competitors would need to avail themselves of this advancement in the art to remain competitive with RCA products. It is then essential that RCA engineers *promptly* submit their patent disclosure of the invention to the RCA Patent Department, for this is *the* formal technique by which the Patent Department is advised that an invention has been made. Patent Department personnel also visit the various operating divisions to search out inventions and see that the usual patent approval procedures are followed in connection with the manufacture and sale of a product. But in most respects, *we must rely upon the individual engineer* to acquaint us with the fact that he has made an invention that is, or could be, of significance in the present or future manufacture of an RCA product.

PATENTABILITY

Disclosures submitted to the Patent Department are reviewed very carefully to determine the extent of patentable novelty as determined by the prior art in the particular field. With the assistance of the appropriate RCA personnel, the possible present or future commercial value of the invention is determined. Certain inventions or patentable ideas may be very clever; however, for cost or other practical reasons, the idea may not be applicable in a commercial product. Thus, a patent on such an invention would be of little value to the company, and it would not be to the best interests of RCA to file a patent application on such an idea. By the same token, an idea subject to considerable commercial use may not represent a novel invention or may have been patented previously or described in a publication. In such cases, RCA would be foolish to file a patent application. Even if a patent could be obtained, it might later be held invalid for lack of patentable novelty.

After much careful screening, about 20 to 25 percent of the submitted invention disclosures result in patent applications; a few are published as *Technical Notes* as a means of obtaining a modicum of protection, and the remainder are placed in the inactive files.

To determine whether a disclosed invention might be used commercially requires some degree of study and understanding. To keep the percentage of evaluation errors to a minimum, the most reliable engineering information and recommendations are obtained. To know whether an invention actually exists in the disclosure is likewise difficult even after a search of the prior art. An accurate conclusion of whether an *invention* is present brings to mind a statement of the Supreme Court of the United States:

> "Invention cannot be defined. It is that impalpable something which you must have to get a patent. Experienced patent lawyers, the Patent Office and the courts understand what it means, only they never agree."

WHAT IS A PATENT?

Virtually every engineer and scientist has heard of patents, but it is not at all unusual to find that they do not actually know what a patent is. A patent is an agreement between the U.S. Government and the patentee; the Government extends to the patentee the right to preclude others from using his invention for a period of 17 years in exchange for his (the patentee's) making available to the public his advancement in the science or art to which the invention pertains. The patent is, therefore, a means of encouraging dissemination of valuable information of a scientific nature in exchange for valuable rights to the inventor. Accordingly, there is consideration flowing in both directions, otherwise the "contract," i.e., the patent, would be invalid.

The inventor who produces a valuable invention should avail himself of the patent statutes. In so doing, he must include in the original patent application (so that it will appear in the resulting patent) a complete and detailed description of his invention—preferably with information so exact that anyone skilled in the art may produce the device by the information contained in the application. If the Commissioner of Patents and his corps of Patent Examiners find that a new invention is properly described in an application, and that the scope of the claims are commensurate with the known prior art, he will issue a patent to the applicant provided he is the proper first inventor of that subject matter.

INTERFERENCE PROCEEDINGS

The matter of issuing the patent to the proper first inventor sounds easy, but determining his identity may not be so easy. It is not unusual for two companies, for example RCA and a competitor, to file patent applications at about the same time on the same or similar inventions.

Contrary to popular belief, the Patent Office *does not* issue the patent to the person who first filed his patent application. When two or more applicants prosecute patent applications on the same invention, the Patent Office places the patent applications in what is called an *interference*. Interference proceedings are necessary to determine the proper first inventor in accordance with patent interference law. At first blush, it might appear that this type of coincidence does not frequently occur; but, in the fields of interest to RCA, 8 to 10 percent of our patent applications ultimately get involved in interference proceedings. This, incidentally, is about *ten times* the national average, indicating clearly that we are in a highly competitive business and that our competition is as eager to obtain patents in our fields of interest as we are.

Interference proceedings are highly complex, and in no other country is there anything even remotely comparable. For many years, proposals have been made to amend, modify, and simplify the U.S. interference practice, but to date no actual changes in the direction of simplification have been made.

PRELIMINARY STATEMENTS — IMPORTANCE OF DATES

Once an interference is declared, the initial document presented thereafter by each applicant is a preliminary statement; the applicant, under oath, states the following dates or approximate dates:

1) when the invention was conceived,
2) disclosed to others,
3) when the first drawings were made,
4) reduce invention to writing,
5) commenced active diligence toward building, perfecting or actually reducing to practice his invention, and
6) the date on which he actually reduced the invention to practice.

He should include also any other dates that would assist in a determination of a proper priority award between the various applicants involved in the interference.

Not until after this statement has been filed is the applicant or his attorney aware of any of the details of the opposing party's application other than the name of the applicant and his attorney. Not even his filing date is known.

After the preliminary statements have been filed and found by the Patent Office to comply with the requirements, a motion period is set and each party to the interference is advised of his opponent's filing date. Each party may then obtain a copy of the opposing party's patent application. During the motion period, the parties submit well founded motions; these may be for the purpose of dissolving the interference or, conversely, for enlarging the issue, or for modifying the issue, or for substituting one application for another. These interlocutory proceedinge are very important and frequently provide a legal basis for subsequent actions that may or may not be taken during the testimony and "trial" or during any appeals.

TESTIMONY ON INTERFERENCE

When an interference still exists after the motion period, a testimony period is set by the Patent Office. During specified time intervals, the junior party (i.e., the last to file) presents his testimony-in-chief. Next, the senior party (i.e., the first to file) presents his testimony-in-chief. Lastly, the junior party is permitted to present rebuttal testimony.

There is no intent in this paper to get involved in the legal technicalities of the testimony proceedings; suffice it to say that the witnesses are under oath, they are subjected to direct examination, and frequently are subjected to exacting cross examination by opposing counsel. This part of the proceedings may involve an appreciable amount of time on the part of the attorney and the witnesses.

The most important thing with respect to the testimony part of the proceedings is that the testimony elicited from the inventor and his corroborating witness (if it is to be of real unimpeachable evidentiary value) is based upon his prior written records; of all these, *the inventor's notebook is the most significant*. The notebook kept by the engineer, therefore, becomes a *most valuable* document in a priority contest with respect to the oral testimony, and in the weight and value given by the Patent Office and appellate courts to such testimony in interference proceedings.

THE ENGINEER'S NOTEBOOK

The RCA engineer is familiar with the fact that a standard RCA notebook is available to him, generally through his local library. He is also aware of the fact that he is urged to enter his technical activities in the notebook promptly, to sign it, to date it, and to have it properly witnessed.

The engineer is not so aware of the reasons for keeping such records, and how RCA benefits when notebooks are kept in a timely and orderly manner.

Diligent and prompt recording of data in a notebook may assure that RCA is awarded a decision; otherwise, failure to have the book properly witnessed can result in an adverse decision in an interference priority contest. Such awareness by RCA engineers may avoid having a competitor obtain a patent on an idea which was first conceived by RCA and which should be the property of RCA.

If we are not, in fact, the proper first inventor, then of course we should not have an award of priority. But, if RCA *is* the proper first inventor, it is very regrettable if our proofs are inadequate to satisfy the very exacting requirements of patent interference law because of lack of attention to the keeping of the notebook—thus causing us to lose the priority contest in an interference that we otherwise should win.

THE GREAT IMPORTANCE OF DATED RECORDS AND WITNESSES

Many hypothetical situations could be given to emphasize the idiosyncrasies and exactness of interference law. Some basic situations are illustrated in Figs. 1 through 5 and discussed in detail in their captions. The legal principles discussed in Figs. 1 through 5 gain further emphasis from the following actual cases—two of which resulted in the loss of awards of priority, and accordingly the loss of patents, which otherwise could have been the property of RCA. The other two involved unnecessary complications.

No Witness

During the research and development of color television in 1949 and 1950, many inventions were made by RCA employees. Knowing the value of a promptly prepared and witnessed document, one employee wrote a patent

OLIN V. MITCHELL was born in Ohio and was graduated with the BSEE from Carnegie Institute of Technology in 1929. He received his LLB from Washington College of Law, Washington, D.C., in 1935. Mr. Mitchell began his patent career with the U.S. Patent Office, where he was a Patent Examiner from June 1929 to April 1937. He joined the RCA Patent Department in 1937 as a Patent Attorney and was assigned to the New York office. In the fall of 1947 he was transferred to Princeton. During World War II he was on part-time leave from RCA to the Office of Scientific Research and Development. In November 1957 he was named Director, RCA Patent Operations, after serving as Manager, Patent Operations, Home Instruments. He is now Director, Domestic Patents, Patents and Licensing, RCA Research and Engineering (corporate staff). A recipient of the Bureau of Ordnance "Exceptional Service" award in 1945, Mr. Mitchell is a Registered Patent Attorney and is a member of the Bar of the District of Columbia, the Circuit Court of Appeals for the District of Columbia, and the Court of Customs and Patent Appeals. He also is a member of the American Patent Law Association, the Philadelphia Patent Law Association, the Patent Lawyers Club of Washington, D.C., Eta Kappa Nu and Sigma Nu Phi.

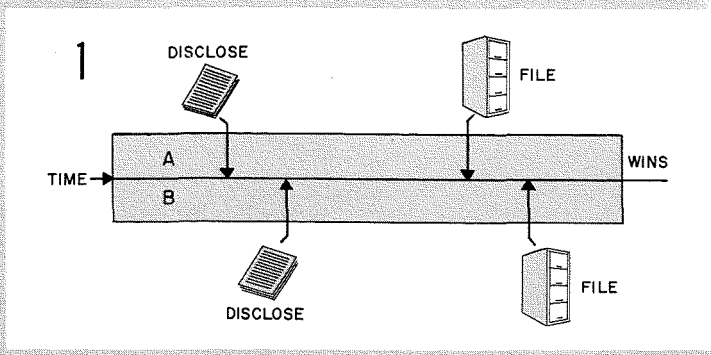


Fig. 1—Applicant A conceived and disclosed to others an invention prior to Applicant B. Furthermore, A also filed a patent application prior to B. In this simple situation, A will win the priority award and will be granted the patent. The controlling factor with only these circumstances involved is the filing date. If the acts by each applicant were only those of conception and filing, the actual conception date is not of significance, and the final decision rests on the filing date. Accordingly, had B filed prior to A, B would have won.

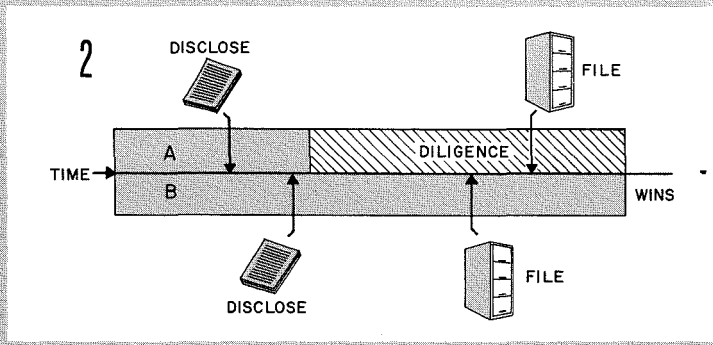


Fig. 2—Here the ingredient of "diligence" is added. Applicant A conceived and disclosed to others prior to B. However, B filed prior to A. Assume also that A commenced diligently to perfect his invention, and that this diligence continued unbroken to the date of filing the application (and beyond), but that no actual "reduction to practice" resulted. Even with this proven diligence by A, and even though B conceived last and exercised no diligence, B will win the interference because he was first to file. Because the proven diligence by A started after the proven conception by B, and because there was no actual reduction to practice by A prior to B's filing date, A's diligence is of little value in winning the priority contest.

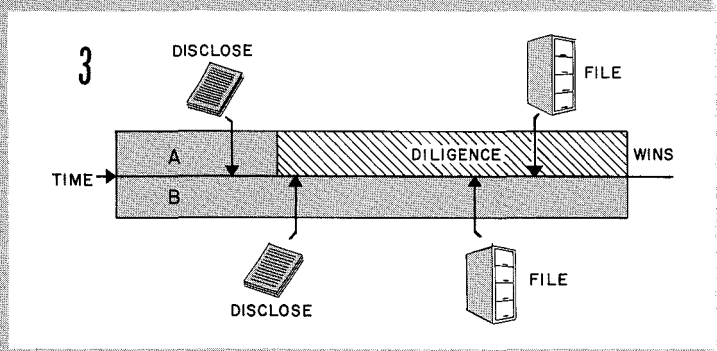


Fig. 3—Compare with Fig. 2—the only difference is the time when A's proven diligence commenced. If A can prove that this diligence began just *prior* to B's proven conception date, and if A's diligence is continuous to his filing date, then even though A was last to file, A will win the interference, and, accordingly, obtain the patent.

The significant point here is that the date on which A can prove he commenced diligently to perfect his invention is very critical. If A can advance (by possibly only a few days) the date on which diligence began by having available his notebook record properly witnessed and dated for corroboration, he may effect a profound difference on the final outcome—the difference between winning and losing. Ironically, the importance of notebook records is seldom realized when the entries are made, because proof of diligence frequently is not required until many years later—for example, when an interference is involved. Many of our important pending interferences (for which testimony is now being taken or has just been concluded) concerns events of 12, 15, or more years ago. To the courts, written signature and date of the witness carry more weight as evidence than oral testimony based solely on recollection after many years.

Accordingly, in Fig. 3, for A's diligence to be of value in winning an interference, the diligence must be proven to have commenced prior to B's proven conception date, and A's diligence must have continued without interruption either to an actual reduction to practice of the device (with appropriate witnessing) or to the filing of a patent application.

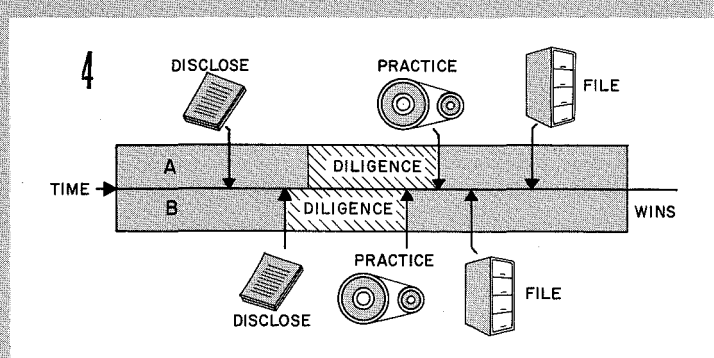


Fig. 4—In this example wherein actual reduction to practice occurred, A conceived and disclosed to others before B. Also, assume that B started immediately and diligently to build the device, worked continuously and did reduce it to practice (with appropriate witnessing), and then filed a patent application. Further assume that A commenced diligence after proven conception by B, that he required approximately the same time, and reduced to practice his invention (with appropriate witnessing) subsequent to B's reduction to practice and prior to B's filing date. Under these circumstances, B will win the interference—even though second to conceive—because he immediately exercised diligence and was the first to reduce to practice the invention common to both litigants.

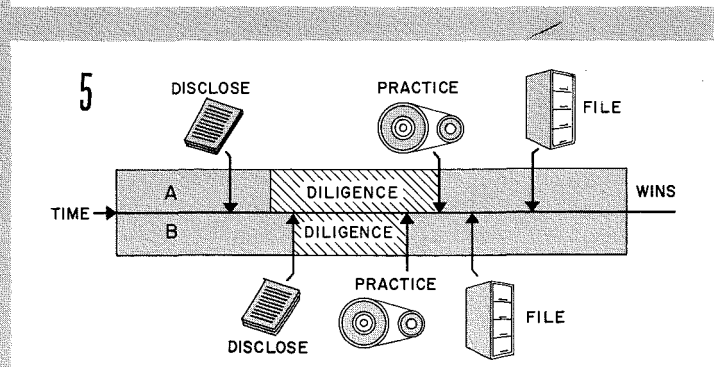


Fig. 5—Here, the circumstances of Fig. 4 are altered by making one seemingly minor change—that of having a notebook with such entries and witnessing that A's diligence can be proven to have commenced just *prior* to B's conception date. This "minor" change in A's proofs might involve only an advance of a few days, but it can reverse the outcome—A will win instead of B. Again, a demonstration of the necessity of keeping timely and accurate notebooks—properly signed, dated, and witnessed.

disclosure and had the document witnessed and dated by a research associate. Many years later, when an interference with the patent application of a competitor required the witness for corroboration purposes, not only had the witness in the intervening years retired and moved to Florida, he had also expired. No witness! In the absence of the witness and the corroboration, the proofs were inadequate. Don't select a witness who is soon scheduled for retirement.

Delayed Dating

In another instance, a capable young engineer wrote a description of an invention on a single sheet of paper, signed and dated it, and handed it to a senior development engineer for witnessing. The senior engineer read the description, commented on the merits of the invention and instructed the young engineer to rewrite the description and make it more detailed and elaborate in order that other people not so experienced in the field might better understand it. The senior engineer *did not sign or date* the original single-page description.

By the time the young engineer got around to rewriting his description and expanding it into three pages, nearly a month had expired (according to the recollection of the young engineer). The later-written three-page document was witnessed and dated by the senior engineer. A patent application was filed on the invention.

Years later, we got involved in an interference with an application on the same invention assigned to a competitor. The opposing party in the interference was able to prove a conception date just prior to the date on which the senior engineer had signed and dated the three-page description. The first description, signed and dated by the young inventor, was fully adequate as far as completeness of description of the invention was concerned. The senior engineer, when called as a corroborating witness, could not, however, fix with positive assurance the date on which the description was first seen, because he had not signed and dated the first description. In the absence of positive and concrete documentary proof of conception ahead of the date proven by the opposing party, we lost the interference.

This demonstrates the necessity of having witnessed, *dated* documents. A delay of a seemingly short time in reducing the invention to writing, signing and dating it, and in having it promptly witnessed and dated can cost us valuable inventions. In the absence of any requirement to prove conception, failure to witness the first-written description would have been immaterial. Under the circumstances of an interference, however, and in recognition of the exacting requirement of patent interference law, this oversight was crucial.

A "Remote" Witness

In still another instance, one of our inventors, at the time the invention was made, had working for him a foreign exchange student from Pretoria, Union of South Africa. The inventor wrote, signed, and dated a description of his invention and had the description witnessed by the foreign exchange student who understood it, signed his name, and dated it—all very properly.

Years later, the patent application filed on the invention became involved in an interference, and we were required to prove our best dates. By this time, the witness had returned to South Africa, and we attempted to elicit information from the witness by a technique known as *letters rogatory*, i.e., the questions being presented in written form, and the answers being supplied by the witness also in written form and under oath. The U.S. Patent Office had no objections to this procedure, but our opposing counsel jumped up and down and in effect said *"No!* We want the right to cross examine this witness, and furthermore, how do we know what the penalty is for making a false statement before a notary public in South Africa?" To make a long story short, we were compelled, at great expense, to bring the man from South Africa to Princeton to act as a corroborating witness in the interference. Try to select as your witness a person who will be readily available.

Can the Witness Read What is Written?

Recently, in the RCA Laboratories, a humorous incident occurred that was discovered as a result of a review of a notebook. A certain employee, a capable and respected research scientist, had recently come to the United States. Being of German origin, he found it much more convenient to think and write in the German language, and accordingly his notebook entries were made in what appeared to be very legible German script. The pages of the notebook were properly signed and dated by the employee. Furthermore, each page was signed by a witness and dated. There was, however, one catch which no doubt would be uncovered by opposing counsel, and which would no doubt detract from the evidentiary value of his testimony as a corroborating witness—the witness could not read German! If you are capable of making your notebook entries in Sanskrit, the Patent Department has no objection *provided* the witness can read and understand the Sanskritic language.

SOME CHARACTERISTICS OF A VALID WITNESS

Properly witnessed documents have much value in connection with proof of conception or proof of diligence in an interference. It is necessary for the witness to have read and understood the document and to have signed and dated it on the day he read it. It is not necessary for the witness to agree with the theory, or that the stated effect, for example, will result. He may be of the belief that the invention is based on an improper or incorrect scientific theory; this is beside the point. If he *understands* what the inventor has written, it is sufficient.

To prove conception of an invention, the inventor *must* have disclosed the completed invention to another person. Preferably, this should be done *by* a written document, signed and dated both by the inventor and by the witness. The extent to which an invention should be described in the written document (or disclosed to others) should be such that if the inventor is hit by the proverbial truck, the witness (with the information supplied by the inventor) would be able to build the device without the addition of any further inventive ingenuity. The conception of an invention not disclosed to another in such manner as to preclude the loss of the invention should the inventor die is not a properly "witnessed" conception, and from an interference standpoint, conception of the invention does not technically exist.

Witnessing Reduction to Practice

With respect to an *actual* reduction to practice of an invention, a corroborating witness is also required. The work of the lone inventor and the records he produces in private, even though complete in all technical detail, are of no value in proving a reduction to practice unless that reduction to practice was witnessed by a corroborator; this witness must *of his own knowledge* know that the

invention was incorporated in the equipment demonstrated. This is true even though the records and test results that the inventor produced could only have been produced by building the equipment. It is one of the quirks of patent interference law, and it is very strictly observed.

Accordingly, when you build a device which is an actual reduction to practice of your invention, make certain that the device is operated in the presence of one or more witnesses, and that the witnesses *know of their own knowledge* that the invention is incorporated in the equipment. For the witness to be told by the inventor that a certain circuit as represented is physically contained within the equipment is not sufficient. The witnesses must actually see the parts or pieces of the equipment which constitute the inventive contribution and must see it successfully operated in the manner and environment intended.

An Ideal Witness

If the equipment representing the actual reduction to practice was assembled or built by an engineering associate, an assistant, or a technician under the direction of the inventor, this situation is wonderful. He is not the inventor; he is a witness; he can corroborate both conception and the actual reduction to practice; he knows of his own knowledge the invention is in the equipment constituting the reduction to practice because he put it there. Notebook records kept by him are very valuable and may be offered in evidence as documentary proof of the events and when they occurred. He is not a joint inventor unless, in fact, he contributed some inseparable part of the particular invention, in which case he could *not* be a corroborating witness. *Joint inventors cannot corroborate for each other.* The law on corroboration may seem harsh, but it is for the purpose of preventing perjury. The law favors a witness who has too little to gain and too much to lose. One court said: "There has to be one rule for all, and rather than do away with the rule, it would be better that the research scientist share his laboratory with another, a system that some companies now impose."

WHAT AND WHAT NOT TO PUT IN NOTEBOOKS

A few examples are given here of notebook entries that have resulted in unnecessary complications. Needless to say, be truthful; but don't be too modest.

A Gross Understatement

In one instance, an RCA engineer entered in a notebook that a "semblance of an image" was produced. Actually the inventor was a perfectionist, and most people would have considered that a good image was produced. The court, however, was of the opinion that had the picture been "good" the inventor would have said so, and having called it a "semblance of an image" left with the judge the impression that the image was rather hazy. If the results are good, do not be bashful.

When Recording Problems — State Solutions

In another instance, one of our engineers, in working with diversity receivers many years ago, entered in his notebook that the signal was full of "mushes and beats." This was true, but both the inventor and his corroborator remember that within 15 minutes after the entry was made in the notebook, one of the oscillators was rephased and the signal was completely clarified, and the equipment worked perfectly. *The only catch is that no entry to this effect was made in the notebook.*

The oral testimony was given years later, and the judge was more inclined to believe the notebook and was disinclined to believe that everything was in the desired proper operating condition minutes later. It was difficult for the judge to imagine that had success been in fact attained a record would not have been made in the notebook, particularly when coupled with the fact that the inventor went out of his way to record a *lack* of success. Accordingly, if you must make derogatory statements because they are true, do not overlook the prompt entry of statements of success when such has been attained (with witnesses!).

Keep Records With the Project

In still another incident of years ago, one of our engineers invented a code converter. He had worked on the device sufficiently to prove the commercial practicality of his invention. He had kept very meticulous and timely records, signed and dated by him, and duly witnessed by corroborators who fully understood the invention. The invention was of such significance that work on the invention was transferred (but the records were not) to the communications terminal facilities where it would ultimately be used. The invention was a success and was used commercially. A patent application was filed, and as luck would have it, a competitor likewise filed a patent application on the same invention. We got involved in a patent interference. When it came time to present our proofs, we then discovered that the original records unfortunately had been destroyed. Attempts were made through oral testimony to win the award of priority (which we should have had), but the Patent Office was not convinced. The *absence* of the records prevented our getting an award of priority. A competitor got the patent.

IN SUMMARY: RCA's BATTING AVERAGE IS OVER .500

Although these examples might lead one to believe that for one or another reason we lose all of our interferences; this is not the case. Happily, we have shown a record of 60 wins (vs. 40 losses) in the last 100 interferences terminated in which there was an award of priority to one of the parties involved.

It might be appropriate to end with an example in which an award of priority was lost by an opposing party. In this particular case, we were in interference on the subject matter of the atomic battery. Our opponent, in presenting his testimony, had the inventor testify that he took a device to the attendant at an irradiation source, had the attendant irradiate the device by a radioactive isotope, and then returned to his laboratory to find that he had made an atomic battery. When the attendant was called as a corroborating witness, he testified that the inventor had brought to him an article to be irradiated, and that the article was wrapped in black paper to exclude light so as to avoid any erroneous scientific results due to actinic radiation. He further testified that he exposed the article, while wrapped in the black paper, to bombardment from the isotope.

His testimony, however, was of little value for the simple reason that the attendant, *of his own knowledge*, did not know what was in the black paper but instead was informed by the inventor as to the contents. His testimony as a corroborator was held to be insufficient, and as a result, our opponent lost the award of priority. *Today, we have the patent on the atomic battery.*

AUTOMATIC TEXT PROCESSING

A number of character-recognition devices are under development which hopefully will transcribe hard-copy text material to a form useable by a computer. Increasing attention is now being given to the problem of what the computer can do with this tremendous data base. The goals of such computer processing of natural-language text include automatic retrieval of data, automatic indexing, automatic formatting of data for subsequent logical and manipulative processing, and so on. A number of possible techniques might be suggested to achieve these goals: fast scanning techniques for searching text for occurrences of words in particular combinations; word counting techniques which will extract word lists in order to approximate an indexing function; word association techniques to group words which have some semantic relationship; grammatical analysis techniques which will make explicit the functions of the words in sentences so that levels of information and word relationships can be determined. This paper discusses each of these techniques.

W. D. CLIMENSON
Data Systems Center
Bethesda, Md.

WILLIAM D. CLIMENSON received his BSEE magna cum laude from Duke University in 1953 and his MSEE from the University of Pennsylvania in 1958. He joined RCA in 1957 and worked on Project ACSI-MATIC concentrating on natural language information to be handled by the computer. He set up automatic syntax analysis programs, and has done basic language control research into linguistics and computer-language problems. As Leader, Language Analysis and Documentation Handling Group in the Data Systems Center, Mr. Climenson has ancillary responsibilities for document handling and medical data-processing programs. He is a member of ACM and Vice-Chairman of its Special Interest Group on Information Retrieval. He is the author of several papers in his field.

OVER THE PAST ten years, considerable attention has been given to the challenging task of reading printed text by machine. A number of specialized devices geared to a well-controlled reading environment are already in operation to process bank checks, credit-card purchases, and public-utility accounts. Progress is being made in the development of devices to read typewritten or printed text, and even handwritten material.

Certainly one of the goals of this development is the ability to automatically transcribe data available in reports, books, and periodicals to a form which can be accepted by a computer. The question which one must immediately raise is: *What can the computer do with these new sources of data?* Some of the goals are:

automatic language translation
automatic retrieval of the stored texts
automatic abstracting of texts
automatic extracting of text portions in a form suitable for manipulating and correlating data
cryptoanalysis

But such ambitious goals can only be met with equally sophisticated and advanced computer processing techniques. It is curious that when such tasks are suggested as appropriate to computers, one usually hears either of two extreme reactions: "impossible" or "obviously feasible." It is hoped that the reader will be left with the impression that the current state of the art is somewhere between these extremes; that the computer can be productive as an assistant in the tasks normally expected of a text processing function.

COMPUTERS AND FORMATS

Before some promising computer techniques for dealing with raw text are discussed, it would be useful to consider the problem as one of formatting. If we view the capabilities of the computer in a deterministic sense, we must use terms such as *record* and *item descriptions*, *parameters*, and *bounds* when we describe a task to be performed; i.e., we expect data to obey certain format rules. Otherwise we could not predict the outcome of computer operations. Thus, a major task in data processing is defining and adjusting formats so that data can be recorded and processed (or rejected) in a consistent fashion. In short, natural languages such as English are quite *un*natural to the computer and must be manipulated to conform with the machine characteristics if any productive work is to be done.

Thus we are faced with somewhat of a paradox: we want to process unformatted data directly with a machine which can only accept formatted data. The answer must lie in a sort of bootstrapping operation, starting with a minimum of format information which is available in natural language orthography:

a limited character set.
a limited punctuation set (including word, sentence, paragraph, and document delimiters).
a large, but finite, number of legal combinations of symbols.

While we take comfort in the fact that the combinatorial possibilities are finite, the central problem is to recognize an organization in the seemingly chaotic nature of natural language. Can we state what is *legal* in the language? If so, is the set of rules for forming utterances (which we call a grammar) of a character and size which the limited capacity of a computer can handle?

TEXT ANALYSIS

We might start by matching the simpler characteristics of the language with the elementary functions which a computer can perform, build on the insight that such an analysis provides, and recognize and test possible operational applications as we proceed.

First, we can certainly compare letter sequences, count matches (or mismatches), and order the results. We could do this at the word or word sequence levels, and suggest, for example, that words which occur a sufficient number of times can be interpreted as descriptive of a document's content. We can tack on to this process a list of reference words which permits us 1) to discard common "function" words (such as *in, the, for*), and 2) upgrade the importance of some words which we know to be indicative of content regardless of the number of times they occur.

At first glance this notion, as simple as it is, seems to provide striking results. Authors obviously select words in a nonrandom fashion, and word-frequency distributions tend to exhibit clustering around significant words. But, on the other hand, good writing style sometimes demands the use of synonyms, and a given word spelling can have two or more unrelated meanings. This will degrade the value of word-frequency lists. We could overcome this difficulty to some degree by storing synonym and homograph word lists, and "respelling" texts so that synonyms become indistinguishable and homographs are assigned subscripts prior to the application of counting techniques.

This basic word-look-up, word-counting approach (with many variations) has been tried for three applications

which require a document description or characterization:

automatic indexing, where a list of words ordered by their significance is used.

automatic abstracting, where sentences which best satisfy some statistical criterion are extracted from the document.

direct text searching for information, where sentences containing selected key words are extracted and examined.

None of these applications has been very successful; to the author's knowledge, these techniques have never been advanced to an operational stage. There are two basic reasons for this: English orthography simply does not contain sufficient information which can be used directly for such intellectual tasks as indexing and abstracting, and the "respelling" of words in text which was suggested above requires a satisfactory solution for a more difficult problem, that of semantics.

THE SEMANTIC PROBLEM

An appreciation of the rich reservoir of concepts which English allows us to communicate can be gained by playing a game with *Roget's Thesaurus:* pick two words at random from the thesaurus index. The object of the game is to get from one word to the other, using the cross references available in the thesaurus categories, with as few intermediate words as possible. For example, we can trace a path from *pacify* to *punish* as follows:

pacify	723.4
harmonize	23.8
adjust	27.7
compensate	30.4
repay	807.9
retaliate	718.2
punish	972.5

Any two adjacent words could be considered as synonyms, but a different aspect is selected to determine the next synonym in the chain. This suggests that if we could isolate these aspects of meaning as a list of elementary concepts such as *movement, size, relation* and the like, we could synthesize any complex concept we need, and more important, we could state explicitly how two concepts are related. In principle, this sounds like a good way to work on the problem of nailing down the definitions of words, and therefore suggests an approach to a vocabulary format for computer processing of text.

Unfortunately, we can see that the solution is still as far away as before when we realize that there would be more than one way to synthesize a concept; i.e., the rules for synthesizing concepts constitute a sort of language grammar which has all the characteristics of the natural language we are trying to control. This is the problem which has been plaguing investigators concerned with automatic language translation (and the entire field of linguistic analysis, for that matter).

With such a pessimistic introduction, the reader may begin to wonder if we know anything at all about the language we use for communicating so effectively. We do, in fact know quite a bit about natural language, particularly its structure. By *know*, we mean that we have been able to state formal rules for constructing sentences, for example. Secondly, more sophisticated mathematical notions, when applied as carefully as they are defined, have been shown to be useful. The remainder of this paper will be concerned with these linguistic and statistical techniques.

AUTOMATIC SYNTAX ANALYSIS AND ITS APPLICATIONS

A description of sentence structure is fundamental to any linguistic approach to text processing. If it were possible to determine the relationships of words in sentences, we could systematically develop the necessary processes needed to analyze sequences of sentences, paragraphs, and documents. This philosophy has motivated an investigation into natural-language structure by the Language Analysis Group at the DEP Data Systems Center in Bethesda, Md. Considerable progress has been made in automatic "parsing" or "diagramming" of English sentences. An RCA 501 program has been written which accepts declarative sentences, marks the limits of phrases and clauses, and displays the results.

An example of the printed output for two sample sentences is given in Fig. 1. The sentence is read vertically, one word per line, with indention to indicate nesting of phrases and clauses. The symbols on the extreme right show the limits of phrases (called first-order strings): *N*, noun phrases; *V*, verb phrases; *A*, adjuncts (prepositional or adverbial phrases). The prefixed numbers indicate a phrase count. For example, in the second sentence the sixth adjunct is "*by a quick and decisive victory*," which contains the eighth noun phrase "*a quick and decisive victory*." Similarly, the symbols in the center column indicate the limits of clauses or degenerate clauses (called second-order strings). Three types of second-order strings are recognized: *MN*, main string in independent clause; *NL*, nounlike (entire strings which behave as nouns in a larger string); *IG*, ignorable (strings which do not play a vital syntactic role in the larger string). In addition, suffix symbols are used to indicate the beginning of a second-order string subject *(S)*, the limits of the verb *(V)*, and the end of the object *(O)*.

The steps needed to perform this analysis are shown in Fig. 2 and described below:

1) After initial screening, the words in the sentence are replaced by the syntactic class(es) of the word. These correspond in a rough way to the conventional parts-of-speech.
2) Words assigned to more than one

Fig. 1—Example of printed output for two sample sentences (1 and 2).

SENTENCE 1

```
    WHILE                1 1G
    THE                  1 1GS          1 N
    MONSOON                             1 N

       WHICH                    2 1G
       HAD                      2 1GV   1 V
       JUST                                     1 A
       STARTED                  2 1GO   1 V

,
    TURNED               1 1GV          2 V
    #KOREA'S                            2 N
    DIRT                                2 N
    AND

       GRAVEL                           3 N
       ROADS                            3 N
       INTO                             2 A
          BOGS           1 1GO          2 A   4 N

,
THE              1 MNS                  5 N
ENEMY                                   5 N

MANAGED          1 MNV                  3 V
TO
FERRY            1 MNV                  3 V

HIS                                     6 N
ARMOR                                   6 N
ACROSS                                  3 A
THE                                                7 N
#HAN                                    3 A   7 N
AND
       ADVANCE                          8 N
       INTO                             4 A
          THE                                      9 N
          OUTSKIRTS                     4 A   9 N
       OF                               5 A
          #SUWON   1 MNO                5 A  10 N
```

SENTENCE 2

```
   IN                    1 1G
   DRAWING                          1 V
   UP
      THEIR                         1 N
      TIMETABLE          1 1GO      1 N

,
THE              1 MNS                  2 N
COMMUNISTS                              2 N
APPARENTLY                              1 A

ASSUMED          1 MNV                  2 V

   THAT                  1 NL
   THE                   1 NLS          3 N
   INITIAL
   ADVANTAGE                        3 N
   OF                               2 A
   A                                       4 N
   STRONG
   SURPRISE
   ATTACK                           2 A   4 N
   IN                               3 A
   GREAT                                   5 N
   FORCE                            3 A   5 N
   AGAINST                          4 A
   THE                                     6 N
   #REPUBLIC                        4 A   6 N
   OF                               5 A
   #KOREA                           5 A   7 N
   WOULD                 1 NLV      3 V   PASSIVE
   BE
   FOLLOWED              1 NLV      3 V
   BY                               6 A
   A                                       8 N
   QUICK
   AND
   DECISIVE
   VICTORY                          6 A   8 N
   FOR                              7 A
   THE                                     9 N
   FORCES                           7 A   9 N
   OF                               8 A
   COMMUNISM     1 MNO  1 NLO       8 A  10 N
```

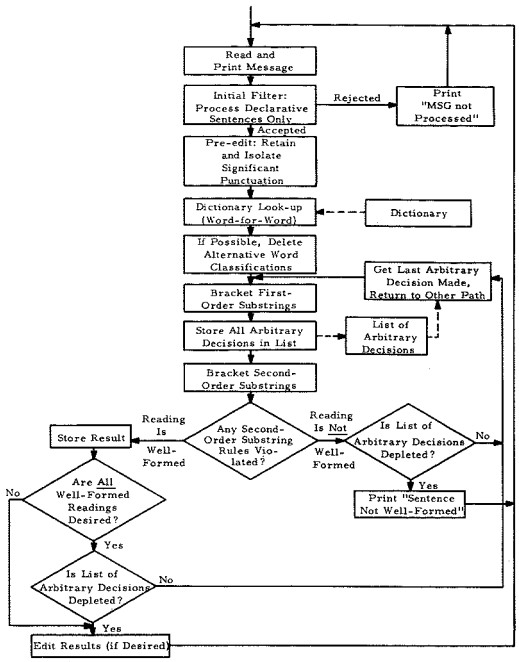


Fig. 2—Basic program steps in syntax analysis.

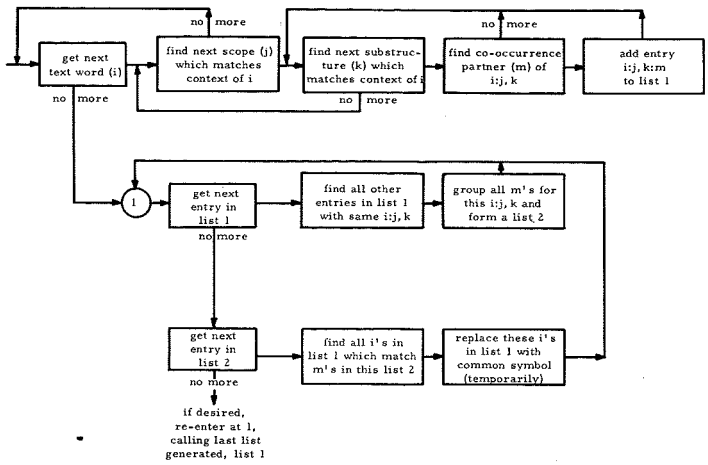


Fig. 4—Generation of a document thesaurus.

class (such as *surprise*, which can be a noun or verb) are examined to see if their specific function in this particular context can be resolved.

3) The first-order strings (phrases) are bracketed. This is done by a pass through the sentence for each of the three phrase types, searching for allowable word sequences.
4) On a final pass through the sentence, second-order strings are isolated. During this pass, the program searches for allowable sequences of first-order strings (rather than of individual words) to form clauses.
5) Because some multiclass words could still remain unresolved after step 2, the search for first-order strings may include some arbitrary decisions. Rather than stop the analysis at these points and seek to resolve the difficulty, the program chooses one logical path and notes in passing that the decision may be wrong. Thus when the second-order analysis is complete, so-called "well-formedness" criteria may not have been met (e.g. a clause may lack a needed noun phrase). If this happens, the analysis returns to the point where the last arbitrary decision was made and follows a new path.

The program, while imperfect, can provide a "good" reading in about 80 percent of the sentences expected in normal written discourse, and it seems feasible to expect that the program could be refined to an operational status. If this is so, how can the results of such an analysis be used? A number of interesting possibilities are suggested in the following paragraphs.

Sentence Condensation

First, we can hypothesize that there is a correlation between the position of a word or phrase in a sentence and its significance to the document. To test this hypothesis, a sentence-condensation program was written for the RCA 501 which uses the syntactic information available in sentences as the sole criterion for reducing the length of the document. Machine implementation of a limited set of rules applied to this data produced a reduction to about 35 percent of original document length. An example of such a condensation is shown in Fig. 3, which was produced from a section of a book on the history of the Korean War. This type of intermediate use of automatic syntax analysis shows promise, but needs to be investigated further.

Thesaurus Generation

A second application of automatic syntax analysis is in the development of a specialized thesaurus. The principal difficulty with a semantic analysis even in a limited subject field is that the meaning

THE ATTACKING COMMUNIST DIVISIONS MOVED SWIFTLY ACROSS THE 38TH PARALLEL TOWARD SEOUL, FIFTY MILES TO THE SOUTH, AN BY 28 JUNE 1950, THREE DAYS AFTER THE BEGINNING OF THE NORTH KOREAN INVASION, THE CAPITAL HAD FALLEN INTO ENEMY HANDS. THE ELEMENT OF TACTICALSURPRISE AND THE NORTH KOREANS' OVERWELMING SUPERIORITY IN WEAPONS CURSHED ORGANIZED ROK RESISTANCE IN THE VICINITY OF THE PARALLEL. NORTH KOREAN TANK COLUMNS GROUND FORWARD UNSCATHED AGAINST THE INEFFECTIVE REPUBLIC OF KOREA FORCES WHICH LACKED TANKS AND ADEQUATE ANTITANK WEAPONS. THE WILD EXODUS OF REFUGEES FROM SEOUL SWELLED THE POPULATION OF THE TWON OF SUWON, WHICH LAY A FEW MILES BELOW THE CAPITAL. INDIVDUAL ROK SOLDIERS DISPLAYED A WILL TO FIGHT, BUT COMMUNICATIONS WERE IN A STATE OF CHAOS, AND AMMUNITION OF EVERY KIND WAS RUNNING LOW. ON 27 JUNE THE SEAT OF THE SOUTH KOREAN GOVERNMENT WAS TEMPORARILY MOVED FROM SEOUL TO TAEJON BELOW THE HAN AND KUM RIVERS. ALTHOUGH U.S. BOMBERS ATTACKED P'YONGYANG AND TARGETS NEARER THE FRONT, ENEMY PLANES FREELY STRAFED THE SUWON AIRSTRIP WHICH WAS NEAR THE HEADQUARTERS OF BRIG. GEN. JOHN H. CHURCH, THE COMMANDER OF ADCOM. WHILE THE MONSOON, WHICH HAD JUST STARTED, TURNED KOREA'S DIRT AND GRAVEL ROADS INTO BOGS, THE ENEMY MANAGED TO FERRY HIS ARMOR ACROSS THE HAN AND ADVANCE INTO THE OUTSKIRTS OF SUWON. RUSSIAN T34 TANKS, RUSSIAN VEHICLES, RUSSIAN COMBAT PLANES, AND RUSSIAN AUTOMATIC WEAPONS WERE USED AGAINST THE PEOPLE OF SOUTH KOREA. THOUSANDS OF NORTH KOREAN SOLDIERS WITH YEARS OF SERVICE IN THE OTHER COMMUNIST ARMIES PROVIDED THE HARD CORE OF THE INVADING TROOPS. THERE CAN BE NO DOUBT THAT SOVIET ADVISERS PLAYED AN OVERWELMING PART IN PLANNING THE OPERATION. IN DRAWING UP THEIR TIMETABLE, THE COMMUNISTS APPARENTLY ASSUMED THAT THE INITIAL ADVANTAGE OF A STRONG SURPRISE ATTACK IN GREAT FORCE AGAINST THE REPUBLIC OF KOREA WOULD BE FOLLOWED BY A QUICK AND DECISIVE VICTORY FOR THE FORCES OF COMMUNISM.

Fig. 3a—Original text to be processed.

Fig. 3b—Text condensation.

ATTACKING DIVISIONS MOVED ACROSS 38TH PARALLEL TOWARD SEOUL; THREE DAYS AFTER NORTH KOREAN INVASION BEGINNING, CAPITAL HAD FALLEN INTO HANDS. SURPRISE ELEMENT, OVERWHELMING SUPERIORITY CRUSHED ROK RESISTANCE IN PARALLEL VICINITY. NORTH KOREAN GROUND FORWARD AGAINST KOREA FORCES REPUBLIC WHICH LACKED TANKS, ADEQUATE WEAPONS. REFUGEES WILD EXODUS SWELLED SUWON TOWN POPULATION. INDIVIDUAL ROK SOLDIERS DISPLAYED WILL; COMMUNICATIONS WERE IN CHAOS STATE; EVERY KIND AMMUNITION WAS RUNNING LOW. SOUTH KOREAN GOVERNMENT SEAT MOVED FROM SEOUL TO TAEJON. PLANES STRAFED SUWON AIRSTRIP. ENEMY MANAGED TO FERRY ARMOR. RUSSIAN PLANES; AUTOMATIC WEAPONS USED AGAINST SOUTH KOREA PEOPLE. THOUSANDS OF NORTH KOREAN SOLDIERS WITH SERVICE YEARS PROVIDED TROOPS HARD CORE. COMMUNISTS ASSUMED THAT ATTACK INITIAL ADVANTAGE IN FORCE AGAINST KOREA REPUBLIC FOLLOWED BY VICTORY FOR COMMUNISM FORCES.

of a word depends on the *context* in which it is used. While context is a very elusive concept, a structural analysis at the sentence level can be used as an elementary approach to its formal definition.

The particular approach suggested here avoids the pitfalls of setting up a single thesaurus for the entire language; instead it is hoped that small, document-oriented thesauri can be constructed and that some of these may be eventually joined into larger organizations of vocabulary. If this is possible, the "respelling" of words in a text which was mentioned earlier could become quite useful.

Assuming that a syntax analysis has been performed on a text, we could proceed as follows (see Fig. 4).

1) Search the text for all occurrences of a given word. For each occurrence note the structure (context) in which it is used. This must be done with knowledge that these structures are described at various levels of precision. Those levels of structure which can be defined formally we will call "substructures;" the higher, less defined portions of text we will call "scopes."
2) Attempt to match word occurrences in the same type of structure, starting at the most precisely defined level.
3) Where a match is discovered within some limits of scope and substructure, find for each word its "co-occurrence partner" among the other units of the substructure (e.g. the co-occurrence partner of the head of a noun phrase might be the object of a succeeding preposition). List these co-occurrence partners together.
4) Replace all occurrences of all the words on such lists by a single, common symbol (word).
5) Reenter the process, this time using the text in its "normalized" form, and repeat the procedure until some criterion is satisfied.

While this procedure has not been mechanized, manual simulation has shown that some significant semantic implications can be drawn from the results. Note that there was no mention of word meaning in the above; the procedure makes use of the author's structuring of his ideas to determine when and where words can be considered synonyms *in this text.*

Paragraph Analysis

Paragraph Analysis, a third application of automatic syntax analysis, is really an extension of it. That is, we would like to be able to state "well-formedness" rules for units of text larger than the sentence. Because the variety of ways to form sentences into paragraphs is greater than that of putting words in sentences, we could expect a paragraph "grammar" to be less precise.

A paragraph, in this analysis, is similar to the orthographically marked paragraph in text in that both are concerned with unity of topic. But there is one important difference: Paragraph analysis considers a set of paragraph markings as its *output*, not its input. Therefore we are free to use as complex a paragraph structure as necessary to explicitly mark the relationships between sentences (just as we marked the relationships between words in syntax analysis).

The relationship we are concerned with is one of dependency, which is manifested in two ways:

If some one element of a paragraph structure is deleted, other elements which depend on it must also be deleted.

When certain dependencies are established, it is possible to treat whole groups of sentences as a single element in subsequent analysis.

Some simple examples of sentence dependency rules are given below (these can operate only after a syntax analysis on the text has been performed):

1) A sentence (clause) containing a noun phrase with *this* at the left depends on the first preceding clause which contains a noun phrase with the same word at its head (usually the right most word in the noun phrase).
2) A clause introduced by a word in a certain class of conjunctions such as *although*, depends on the preceding clause.
3) A clause containing *its* plus noun phrase depends on the next following clause which has the same noun phrase head.

In addition to rules such as these, paragraph analysis makes use of rules to organize the discovered dependencies, and partition the document into paragraphs. These take the form of topological and linguistic well-formedness criteria.

The availability of structural data above the sentence level makes feasible a number of useful tasks in processing textual material. A few possibilities are listed below.

The notion of sentence condensation can be extended to permit deletion of entire clauses or sentences in order to systematically reduce the size of a document.

The resultant paragraph structure can be examined to determine the minimum text unit which can be considered informationally independent, therefore indexable.

The previously mentioned method of generating a thesaurus could be enhanced since the paragraph structure adds precision to the notion of context.

Transformations

An important aspect of structural linguistics is the recognition and explicit marking of equivalent or similar structures. Considerable work in this area at the sentence level has been done under the name "transformational analysis." This analysis provides the means for reducing the number of structures possible in the language in a systematic fashion. Thus transforming or rewriting a sentence is to the language's structure as respelling of a text (from a thesaurus) is to its vocabulary.

If both of these could be realized at the level of context required, we would be within reach of our formatting goal. Context is again mentioned here because care must be exercised not only in determining the types of transformations to be applied to the entire language, but where and when to apply them in the local environment of the text. For example, we can specify a passive-voice to active-voice transformation:

His buddy carried John.
$\rightarrow$*John was carried by his buddy.*

But if we met the latter sequence out of context, we would not know the transformation to use to answer the question: Who does the *his* refer to?

This type of processing and a description of it are very important for two basic reasons. First, it is as fundamental as syntax analysis in any attempt to describe language. Secondly, all of the applications in linguistic analysis mentioned previously could be more manageable if a previous (or a concurrent) transformational analysis was performed.

Statistical Analysis

As mentioned previously, statistical techniques applied directly to natural language texts cannot promise more than rudimentary results. But it should be obvious that if something close to a "well-controlled" sample can be found, statistical techniques will offer much in the analysis of documents.

The purpose of the following discussion is not how the needed control of data might be achieved (perhaps manually or with the use of the suggested linguistic techniques); rather we will assume that a sufficient degree of text normalization has been obtained.

Counting

In addition to the counting techniques

suggested earlier, mention should be made of a method for "normalizing" word counts by using the ratio of their *relative* frequency in the document to their relative frequency in the file. This notion would attempt to characterize a document by determining how it differs from the remainder of the file. Thus, words which were equally common (or rare) in the file and in the document would be ignored. Words which occurred more in one document than would be expected (as predicted by the file statistics) would be selected as significant.

Correlation

Correlation techniques are pertinent to text processing in three ways:

The retrieval of data which is only implicitly stored in the file.

The amplification of requests for data.

The characterization of the file as a whole.

In each of these we are getting farther away from the text itself and working, in most cases, with document descriptor lists.

Basically, we are interested in determining numeric values for word (or descriptor) relationships. For example, starting with a group of selected words and their occurrences in file documents we can generate a word-document matrix, with each cell containing $N_{i,j}$, the number of occurrences of word i in document j. Using conventional correlation techniques we can develop correlation coefficients for each word-pair. Similarly we could obtain a measure of correlation between two index terms using the number of documents indexed by both terms, and the number of documents indexed by each term (without regard for the other). Other parameters have been used as well.

The value of correlating terms can be seen if reference is again made to the semantic problem and context. That is, we can legitimately ask questions about the relationships of terms within the context of the file or group of data we are working with (and not the entire universe of concepts). For example, the effectiveness of a document-retrieval system can be enhanced considerably if in addition to retrieving documents, the system retrieves information *about the file* to help the requestor formulate his query. Specifically, the original terms in a request can be correlated with all other terms used in the file to determine which new ones (the requestor neglected to use) ought to be appended to the request. These new terms might be checked against the file for additional correlations.

Secondly, correlation techniques are important in measuring the dynamic elements of the data to be processed. New trends and aspects of a particular subject area can be detected. One method of extending correlation techniques in the area of file characterization is discussed below.

Factor Analysis

It is often quite difficult to analyze a matrix of correlation coefficients because of the complex relationships which one must examine in order to determine, say, the overlap of two pairs of elements. The problem of interpreting correlation matrices has been tackled by psychologists who have developed a technique called "factor analysis" to assist in the task of finding common elements in the variables of a testing situation. The technique has been carried over to the document-retrieval field. In this application, factor analysis has been used to extract "factors" from a descriptor correlation matrix. A factor consists of a list of related descriptors each with a numeric weight (or loading), which are extracted by a matrix reduction process.

The various factors extracted from the matrix (lists of terms) can be interpreted and assigned names. They should (and do) show the gross classes of data in a document file and relationships of the terms used in document descriptions. Dynamic document classification might be possible using this technique.

SUMMARY

It is hoped that techniques borrowed from psychology, graph theory, linguistics and so on will develop into useable tools in text analysis. Some progress has been made already. Because of the tremendous increase in technical and administrative documentation and the anticipated availability of reading machines more progress *must* be made.

There are two basic reasons why research in automatic text processing has produced disappointing results thus far:

1) The potential customer wants to see operational results in a relatively short time. This has directed the researcher's attention to *ad hoc* and obvious techniques which seem to promise some payoff quickly.
2) The researcher himself is either impatient to see useable results, or at the other extreme, is pursuing relevant tasks but at a leisurely academic pace, far removed from the realities of the problem at hand.

As a result of these two factors, we have seen a number of simple techniques worked and reworked by different people at considerable cost with little success. It seems that an approach closer to that which we might call "goal-oriented linguistic-theoretic" is needed. This requires considerable discipline and patience from both the investigator and his sponsor, but could be more successful in the long run.

One could point to numerous examples of research in text processing supported on this basis. Three projects being carried on at the DEP Data Systems Center might be mentioned:

1) *Fact Correlation Study*, performed for the Rome Air Development Center, which supplied to the Air Force an applied research plan in text processing.
2) *Advanced Recognition Techniques Study*, performed for the U. S. Army Electronics Materiel Agency, which is concerned with the use of contextual clues in improving the performance of character readers.
3) *Fact Correlation, Phase IIa*, for Rome Air Development Center, which is concerned with a benchmark program in concept correlation; specifically, the problem of automatic reassembly of paragraphs into the documents from which they were extracted.

BIBLIOGRAPHY

A paper of this type normally demands a rather complete bibliography. In lieu of this, a list of basic references is included whose topics and internal references should lead to the desired information.

1. *Current Research and Development in Scientific Documentation*, Office of Science Information Service, National Science Foundation, numbered bulletins published semi-annually.
2. *Foreign Developments in Machine Translation*, Joint Publications Research Service, Office of Technical Services, U. S. Department of Commerce, numbered translated reports.
3. "Machine Indexing, Progress and Problems", *Proceedings of the Third Institute on Information Storage and Retrieval*, The American University, February 1961.
4. *Mechanical Translation*, Massachusetts Institute of Technology, published quarterly.
5. *Organization of Information for Storage and Retrospective Search*, Preprints of papers for the International Conference on Scientific Information, Area V., National Academy of Sciences, November 1958.
6. *Transformations and Discourse Analysis Projects*, Department of Linguistics, University of Pennsylvania, numbered reports.
7. S. R. Snodey, "Information Retrieval Systems and Technology—A Literature Survey", *IEEE Transactions on EWS*, (in press; to appear in Fall 1963); A comprehensive bibliography of world literature on information retrieval for the period 1957-61.

THE LOGIC OF UNIVERSAL CHARACTER RECOGNITION

Many computer research laboratories are developing logic for recognizing alphabetic and numeric characters printed in many different fonts (type faces). The most promising schemes are based upon the detection of geometric features that tend to be invariant under changes in fonts and imperfections in printing. Features can be combined by parallel or sequential processing. Choosing between these two methods is a controversial problem, but there is some evidence that sequential processing and its generalizations have the greatest potential.

DR. IVAN H. SUBLETTE
RCA Laboratories
Princeton, N. J.

ELECTRONIC COMPUTERS are assuming an increasing share of the data-processing tasks that burden our society. Although it is questionable that these machines are thinking, there is no doubt that some people are being forced to think more consciously and more precisely than they ever have before. Each new application of a computer has been possible only because somebody has specified down to the last detail the operations to be performed in a given task. Most persons who have helped prepare a new computer installation would agree that it is easy to underestimate the difficulty of stating *precisely* just what human beings do in performing apparently routine duties.

Character recognition is a problem in automation that has been forced upon us by the computers themselves. Input information for a computer appearing in the form of printed or handwritten characters on a document must be translated into computer language. Since the employment of keyboard operators for this purpose is expensive, there is now a demand for machines which can recognize alphabetic and numeric characters. Because recognizing characters requires little in the way of human intelligence, designing a reading machine may appear to be a simple problem. Those persons who have attempted to do so would not agree.

The basic difficulty seems to be that the rules used by human beings in recognizing visual patterns are not known, even approximately. We learn to multiply numbers by memorizing an explicit set of rules, but we learn to recognize visual patterns merely by being presented with examples. Our lack of understanding of the human recognition processes need not lead to pessimism, however. For the time being, we will be satisfied with machines for reading printed characters; the recognition of human faces and fingerprints can wait. Also, the best way of building a reading machine may not be to copy the brain.

Important progress has already been made in the reading-machine field. Machines which read a single, specially-designed font (type face) are now commercially available. RCA Electronic Data Processing has announced a machine (the RCA *Videoscan*) that reads the ten numerals and five other symbols printed in one font. Since many existing data-processing systems can control the font being used, machines of this kind will dominate the field for the next several years.

This paper is concerned with multi-font, or *universal* reading machines. Many government and industrial laboratories are working on this problem. Some projects are aimed at the reading of printed characters; others seek methods for reading cursive script; still others are attempting to uncover general principles of visual pattern recognition with the expectation that universal reading machines may be a by-product of their work.

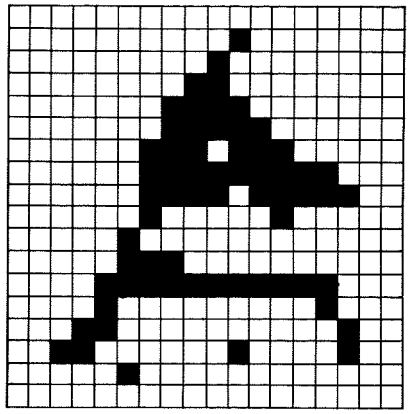


Fig. 1—Digital form of a distorted *A*.

The character-recognition research program at RCA Laboratories is aimed at developing the logical principles of machines for reading printed characters in many fonts. It is hoped that our work will lead eventually to a machine capable of reading copy produced by almost any typewriter. Such a machine would be useful in a data-processing systems which must process input documents filled out by typewriters in many different locations.

PRELIMINARY PROCESSING OF CHARACTER IMAGES

Character recognition is primarily a problem in data-processing rather than in optics or television. Therefore little will be said here about the methods employed in converting the optical image of a character into a video signal suitable for processing by recognition circuitry. Typically, a flying-spot scanner or a vidicon is used for this purpose.

Most character-recognition systems require that a character image be converted into a digital form at an early stage. The scanning system usually divides the character field into a matrix of cells, and the video signal is quantized so that each cell is either black or white. Fig. 1 shows the digital form of a distorted *A*. The advantage of using a digital, rather than an analog, representation of characters lies in the ease with which binary (yes-no) signals can be manipulated by electronic circuits. The early conversion to a digital representation can be criticized on the grounds that important grey-scale information may be destroyed in the quantizing process, particularly for smudged or weakly-printed characters. This difficulty is overcome in the RCA Videoscan by using a variable quantizing threshold that is automatically adjusted to compensate for changes in the average contrast in a character image. In speculating on future trends in character-recognition systems, it should be remembered that video-processing decisions are not necessarily irreversible. For example, a reading machine having difficulty in recognizing a character may scan it again with a different quantizing threshold.

RECOGNITION BY FEATURE DETECTION

The most obvious way of recognizing characters would be to compare an unknown character with a set of templates stored in a fixed memory. Each template would represent a different member of the alphabet and might resemble the pattern shown in Fig. 1 (except that it would represent a typical undistorted character). An unknown character would be compared with all of the templates, a comparison perhaps consisting of counting the number of cells in which the unknown and the template agreed (both white or both black). The

unknown character would be identified with the template yielding the largest count.

It is generally agreed that template-matching is not suitable for a universal reading machine. The main weakness of template matching is the necessity of positioning the unknown character accurately with respect to a template. Another weakness is the tendency to be intolerant of variations in stroke width. Finally, template-matching clearly cannot be expanded to handle the recognition of hand printing or any kind of characters which vary randomly in size or shape.

Almost all of the current proposals for universal reading machines rely instead upon the use of *feature detection.* Many different tests are applied to an unknown character, the purpose of each test being to detect the presence of some feature that helps distinguish one character from another. The success of feature detection depends upon the existence of features that are invariant with respect to changes in the style of the characters. There is no doubt that such features exist. For example, in most fonts the capital letter H can be described in part by the features *concave on top, concave on bottom,* and *vertical strokes on left and right.*

The method of feature detection also depends upon the existence of features that tend to be invariant when the printing is imperfect. It is less easy to show that features of this type exist. If the letter H, for example, is smudged near the top, the upper concavity may be changed into an enclosed white region. Now the H is described by the features *enclosed region on top, concave on bottom, vertical strokes on left and right.* With the possible exception of the right-hand vertical stroke, this sounds suspiciously like the description of the capital letter R. Does the R have a vertical stroke on the right? It might, depending on how much smearing there is on the right and exactly how the vertical stroke detector in the machine operates. Probably, a machine should detect features in addition to those already mentioned before making a final decision between the H and the R.

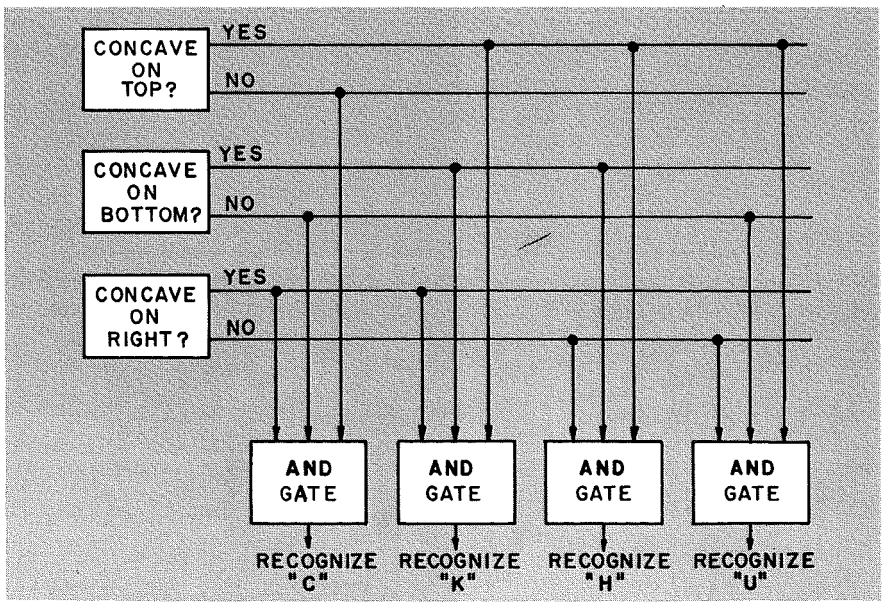
Because of the large number of possible variations due to font changes and printing imperfections, a universal machine must have many kinds of feature tests in its repertoire. In some recent experiments at RCA Laboratories on a system for recognizing a 29-character alphabet, about sixty features of the type discussed above were used. Universal machines of the future may use feature tests numbered in the hundreds.

It would not be entirely flippant to remark that the more features used in recognition, the better. It should be remembered, however, that a figure of merit for a reading machine must include a measure of cost as well as a measure of recognition accuracy. If it were assumed that the cost of a machine is proportional to the number of features it can detect, it would be reasonable to state that

$$\textit{figure of merit} = \frac{1}{(\textit{error rate}) \times (\textit{number of features})}$$

But it is doubtful that there need be a close relation between the number of features detected by a machine and its cost. This important point will be discussed further.

Fig. 2—Parallel processing of feature data.



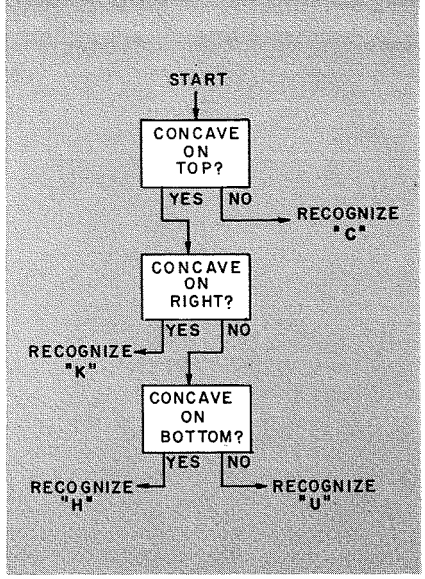


Fig. 3—Sequential processing of feature data.

PARALLEL OR SEQUENTIAL PROCESSING?

Selfridge and Neisser[1] have pointed out that there are two fundamentally different methods of character recognition: *parallel processing* and *sequential processing.* Parallel processing is basically a two-stage process. In the first stage, all possible feature-detecting operations are performed, usually simultaneously. In the second stage, the results of the feature tests are combined simultaneously in a decision-making network that identifies the unknown character. Fig. 2 shows parallel processing being used in a simple system for distinguishing between the four characters U, C, H, and K.

Sequential processing is a multistage process in which only one feature is detected at a time. The result of the previous feature test is used to determine which feature test is to be applied next. As this process continues, the number of possible identities of the unknown character diminishes until (hopefully) only one possibility is left. Usually, not all possible features are used in identifying any single character. Fig. 3 shows sequential processing being used to solve the simple problem introduced previously.

It is an open question whether parallel or sequential processing is best for character recognition. Selfridge and Neisser have argued in favor of parallel processing, but we have found a sequential method to be the most promising in our work at RCA Laboratories. Without claiming to have settled this question, we will present here the reasons for choosing sequential processing and some results that have been obtained with it.

But first a word should be said for the parallel side of the argument. Parallel processing is usually faster because the features are detected and combined simultaneously. Parallel processing also tends to be less costly when the total

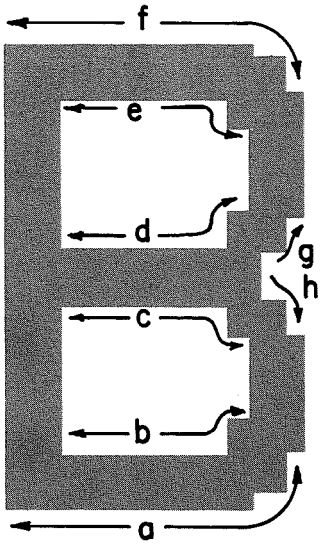


Fig. 4—Edge labels assigned to the digital form of the letter *B*.

number of features is small. Therefore, controlled-font readers, such as the RCA Videoscan, ordinarily process feature data in parallel.

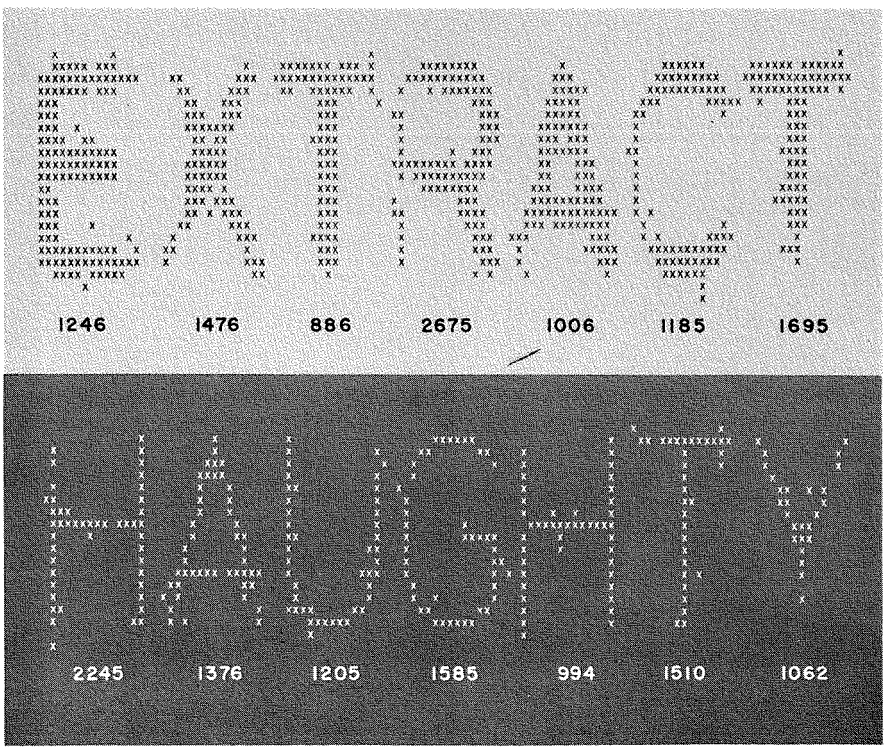
It has been argued that the parallel method is in general superior because it is inherently less error-prone. Since the parallel method evaluates the results from all of the feature detectors, and the sequential method jumps to a conclusion after detecting a smaller number of features, it has been alleged that the sequential system must make more mistakes. But a sequential system always can be made equal to or better than any given parallel system by increasing the complexity of its decision procedure. It is evident, then, that sequential and parallel processing must be compared on the basis of cost, as well as error rate.

For a universal machine which must detect many features, sequential processing may be superior because it does not waste effort in detecting irrelevant features. The number of features used in identifying any particular unknown character frequently will be small compared to the total number of features used in recognizing all characters. For example, a large battery of tests may be required for distinguishing *O* from *Q*, *K* from *X*, *V* from *U*, and so on. But these tests are not needed except when these cases come up, so why perform them blindly every time?

A simple analogy to sequential processing in character recognition is the game of "Twenty Questions", in which the aim is to identify an unknown object by asking twenty or fewer questions answered by either "yes" or "no". The player uses the answer to his previous question to determine what question to ask next. A list of questions about all possible objects would be endless, but the number of questions asked in identifying any particular object is frequently less than twenty.

This analogy suggests that sequential processing always can be shown to be the most efficient procedure by choosing a sufficiently difficult problem in recognition. Arguing for sequential, rather than parallel, processing is equivalent to arguing that universal character recognition is a complex, rather than a simple, problem.

Fig. 5—Words correctly recognized by a computer program simulating machine *M*. The numbers beneath each character denote the number of instruction executions required for recognition.



GENERALIZATIONS OF SEQUENTIAL PROCESSING

There would be no advantage in omitting the detection of irrelevant features if it were necessary to provide separate arrays of electronic components for each feature detector. Some way must be found by which group of feature detectors can use a major portion of a machine in common. In our research on character recognition at RCA Laboratories we have accomplished this by using a machine organized much like a general-purpose digital computer.

Consider a character-reading machine comprised of a large instruction memory, a small data memory, and a processing unit. The instruction memory contains a list of primitive instructions which are executed one at a time in the processing unit. The data memory contains the digital form of the character pattern. This machine hereafter will be referred to as M. Feature detectors are realized in M by programs (lists of instructions) stored in the instruction memory. Since all programs use the same processing unit, increasing the number of feature detectors implies an increase only in the size of the instruction memory. Since memory elements are among the cheapest of computer components, the cost of M grows slowly as the number of features is increased.

Increasing the number of features in the repertoire of M need not even cause a proportional increase in the size of the instruction memory. The feature-detecting programs can be arranged in a hierarchy so that a low-level program (a subroutine) can be used as a part of two or more higher-level programs. Then it is possible to create new feature detectors in the higher-level programs by using old subroutines in new ways.

The efficient use of multipurpose subroutines in M depends upon being able to assign different names, or labels, to separate parts of patterns. As shown in Fig. 4, an unknown character (in this case a *B*) is stored as a set of edge trajectories, each of which is assigned an alphabetic label. Suppose that in recognizing a *B*, it is desired to detect the two features *large enclosed region on top* and *large enclosed region on bottom*. A single subroutine designed to measure the size of enclosed regions can be used to detect both features, first by

assigning it to work with the edge pair (d, e) and then with the edge pair (b, c). Suppose it is desired to detect the three features *bottom horizontal stroke, middle horizontal stroke,* and *top horizontal stroke.* For the *B*, these three features can be detected by one subroutine assigned in succession to the edge pairs (a, b), (c, d), and (e, f).

In a sequential machine, it is possible to go beyond the idea of multipurpose subroutines and to construct subroutines of fixed size that can operate on arbitrarily complex patterns. When a character is broken into several pieces, it is desirable to begin the recognition procedure by detecting the features of the largest object in the pattern, since this ordinarily will reduce the number of subsequent alternatives. Therefore, the program of M includes a subroutine for finding the largest object in a group of disconnected objects. This subroutine carries out the following procedure:

1) Find one object X that has not been assigned the tag "used." If such an object is found, proceed to step 2. If no such object is found, the procedure is terminated, and the label of the largest object can be found in memory location L.
2) Assign the tag "used" to object X.
3) Compare the size of object X to the size of the largest object that has been found since the beginning of this procedure. If and only if object X is the largest, store its label in location L. Return to step 1.

An important characteristic of this subroutine is that it contains no reference to the number of objects in the pattern. If the memory required to store the pattern itself is ignored, the size of the machine required to carry out this procedure is independent of the complexity of the pattern. Of course, more time will be required to find the largest object when the number of objects is increased.

Since starting with the largest object does not eliminate entirely the difficulty of writing short programs for recognizing broken characters, subroutines for joining disconnected objects have been included in the program of M. One such subroutine executes the following procedure: find a pair of disconnected objects separated by a distance less than a certain fixed amount and join them together. The size of this subroutine is independent of the number of pair of objects in the pattern. Also, the use of joining subroutines tends to make the size of the entire recognition program of M independent of the number of pieces into which a character is broken. The reader is referred to Minsky's[2] survey of research in artificial intelligence for a more extensive discussion of programs for operating on arbitrarily complex patterns.

EXPERIMENTAL RESULTS

Research on the character-reading machine M is being performed by simulating it on an existing large-scale computer. Computer simulation yields the desired experimental results without incurring the large expense of actually constructing reading machines. The present version of M contains an instruction memory of 4,096 words (36 bits per word) and a data memory of 1,024 words (6 bits per word). The instruction repertoire of M is designed so that the instruction memory can be a fixed (read-only) memory. The present version of the program of M is capable of recognizing 29 different alphabet and numeric characters. This program occupies about 3,000 words of the instruction memory.

Fig. 5 shows the digital forms of distorted words that M has recognized correctly. In these patterns, which have been formed by a computer output printer, an *X* represents a black element. With the level of distortion shown here, M recognizes about 85 percent of all characters correctly.

The characters shown in Fig. 5 are synthetic samples generated by a computer program that simulates common distortions in printing. Synthetic samples are more convenient than real samples because the frequency of deteriorated characters in actual samples of printing tends to be low—perhaps only one out of 1,000 characters would be distorted severely enough to be interesting to us. Since the program for simulating M requires about one second to recognize a character, too much computing time would be required to obtain significant results from real characters. With synthetic characters, the frequency of interesting cases can be increased to at least 10 percent. We have described elsewhere[3] the method used to generate synthetic samples of distorted characters.

Since sequential processing is inherently slower than parallel processing, a special effort has been made to obtain usefully-high reading rates. For each character recognized by M, the number of instructions executed is recorded. The average number of instruction executions required to recognize a character is less than 2,000. Therefore a reading rate of 100 characters/sec could be obtained with an instruction execution time of 5 μsec. This rate is high enough to be useful, and prospects are good for obtaining much faster instruction execution times.

CONCLUSIONS

With our present knowledge of data-processing principles, sequential processing is the most natural way of solving complex problems in character recognition. By making a current operation depend upon the result of a previously-completed operation, elaborate hierarchies of processing rules can be executed with a minimum of equipment. For simple problems which can be divided into independent parts, parallel processing tends to be faster and cheaper.

ACKNOWLEDGMENTS

Juri Tults, a colleague of the author, has contributed significantly to the character recognition project at RCA Laboratories. The author is grateful to Saul Amarel for general encouragement and for helpful suggestions concerning this paper.

BIBLIOGRAPHY

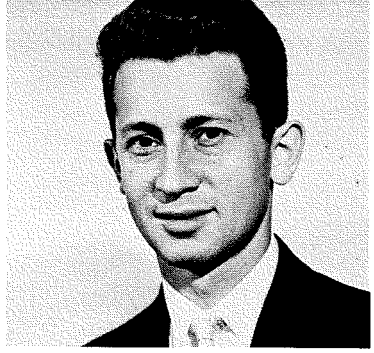
1. Oliver Selfridge and Ulric Neisser, "Pattern Recognition by Machine", *Scientific American,* vol. 203, pp. 60-68, August 1960.
2. M. L. Minsky, "Steps Toward Artificial Intelligence," *Proceedings of the IRE,* vol. 49, pp. 8-30, January 1961.
3. I. H. Sublette and J. Tults, "Character Recognition by Digital Feature Detection", *RCA Review,* vol. 23, pp. 60-79, March 1962.

DR. IVAN H. SUBLETTE received a BSEE from Purdue University in 1949 and MS and PhD degrees from the University of Pennsylvania in 1951 and 1957, respectively. Dr. Sublette joined an advanced development group at the Camden plant of RCA in 1949. After working for two years on the application of television techniques to radar systems, he entered the digital computing field. He worked on diode switching circuits, coincident-current magnetic memories, magnetic logic, and contributed to the logic design for the first electronic digital computer developed by RCA. Later he developed techniques for processing radar data in digital computers and worked on computer systems engineering for the BMEWS program. In 1959, he transferred to the RCA Laboratories, where he is now conducting research on character recognition.

300-Mc TUNNEL-DIODE LOGIC CIRCUITS

A complete set of tunnel-diode logic circuits has been developed. Average delay per logic level is 0.5 nsec. Average DC power dissipation per gate is 100 mw. To achieve this performance, new techniques were employed: 1) nonlinear biasing using the tunnel resistor, a new tunneling device; 2) trimming, a technique of current bias adjustment to offset initial tolerances; 3) transmission-line terminating without sacrificing signal amplitude. Using these circuits, a 40-gate model was constructed that can shift and count at 300 Mc, and that has operated for 200 hours with very good reliability. The short delay per logic level, high repetition rate, and low average power dissipation make these logic gates a powerful set of building blocks for high-speed digital computers. (The 40-gate model is shown on the front cover.)

M. COOPERMAN
Advanced Development Engineering
Electronic Data Processing
Camden, N. J.



MICHAEL COOPERMAN received the BEE degree from the City College of New York in June 1955. From 1955 to January 1961, he was with the Advanced Development Section of the RCA Home Instruments Division, Cherry Hill, N. J. His work has centered around the application of ferromagnetic and ferroelectric devices to television circuits and, more recently, the development of tunnel-diode circuitry and parametric amplifiers for operation at gigacycle frequencies. He is presently with EDP, Pennsauken, N. J., where he is engaged in development of tunnel-diode logic circuits for digital computers. Mr. Cooperman is a member of the IEEE, Tau Beta Pi, and Eta Kappa Nu.

FOR SEVERAL YEARS, RCA has been developing tunnel-diode logic circuits for high-speed digital computers. A set of circuits was developed by the middle of 1961 which was then used to build a feasibility model of approximately 300 gates. The reliable operation of that model proved the feasibility and practicality of using tunnel-diode logic circuits in high-speed digital computers.[1,2]

The experience obtained with that model suggested numerous ways in which those logic circuits could be improved to provide better performance and reliability. A program was undertaken which resulted in the new and improved set of logic circuits described herein. These new circuits, as compared to those in the 300-gate model, have reduced delays, reduced power dissipation, and increased reliability, repetition rates, fan-in, and fan-out. To demonstrate the improved circuits, a 40-gate model was constructed that can shift and count at 300 Mc.

This paper describes the operation and performance of these circuits, intended for the reader interested in a general understanding of their operation and capabilities. (Additional design considerations, circuit diagrams, layouts, and waveforms, are available in the literature.[5])

Tunnel-diode logic circuits can be designed to operate in either the monostable or bistable mode.[3] Stages operating monostably are used in all of the three gates described in this paper. These are the *or* gate, *and* gate, and bistable circuits. The bistable circuit is the only one using a stage operating in the bistable mode.

BASIC MONOSTABLE STAGE

The basic monostable stage, a tunnel diode in series with an inductance and a tunnel resistor, is shown in Fig. 1. The tunnel resistor is a new device formed by plating a resistive path across a tunnel-diode junction. The two are then mounted in one glass package to form one device. Plating and mounting in one package is used to keep the stray inductance between the two elements to a minimum. Otherwise, the tunnel diode may oscillate, thus preventing the two elements from acting as one device. The characteristics of a tunnel resistor and the elements from which it is formed are shown in Fig. 2. The characteristic of a tunnel rectifier is shown in Fig. 3.

To facilitate describing the operation of this circuit, the tunnel-resistor biasing characteristic is superimposed on the characteristic of the tunnel diode in Fig. 4. The more popular term for *biasing characteristic* is *load line;* however, since this circuit will have other loads, *biasing characteristic* is preferred.

When an input is applied to the stage of Fig. 1, the biasing characteristic shifts to a position indicated by curve b in Fig. 4. This causes switching along the trajectory indicated by the dotted lines. The switching cycle is divided into a number of regions as indicated in Fig. 4. The tunnel resistor provides a desirable biasing characteristic, as it is relatively flat when the tunnel diode switches over the peak; it then drops sharply to permit monostable operation. Since the voltage required to obtain this biasing characteristic is only 250 mv, the power dissipation is relatively low (Table I).

TUNNEL-DIODE OR GATE

To perform a logical *or* function, a circuit must produce an output when any one of its inputs is activated. This is easily accomplished by providing more than one input to the basic monostable stage of Fig. 1. A current into any one of the inputs causes the tunnel diode to fire and thus accomplish an *or*.

A complete circuit diagram of a tunnel-diode *or* gate is shown in Fig. 5. It consists of two monostable stages cascaded to provide the required current amplification. (TD_1, TDR_1, R_1, and L_1 are elements of the first stage, while TD_2, TDR_2, R_2, and L_2 are elements of the second stage.) Because of the requirements of increased fan-in, fan-out and speed, new techniques had to be employed in this circuit. Two of the most important circuit techniques now utilized in the *or* gate and the other gates are *trimming* and *transmission line terminating*. Trimming is done with R_1 and R_2; transmission line termination is accomplished by a network consisting of TR_1 and TR_2.

Trimming

To increase both fan-out and operation speed, TD_1 and TD_2 (Fig. 5) required being biased closer to their peaks; however, worst-case tolerance conditions do not permit this. To cancel some of these tolerance variations, a current source of several milliamperes is added to each stage. In Fig. 5, the current sources for the first and second stages are provided by R_1 and R_2 connected to +3 volts. The resistance of R_1 and R_2 can be increased by trimming (mechanically removing some of the conductive material). After the gate is assembled, R_1 and R_2 are trimmed in accordance with a specified procedure to bias each stage to the desired amount below its tunnel-diode peak. In addition to its essential functions, trimming also provides the desirable characteristic of making the electrical performance more uniform. This results in an additional increase of speed in the entire system.

Terminating Network

The purpose of the terminating network is to eliminate reflections between gates. The operation of this network may be understood by referring to Fig. 6, which shows an output stage of an *or* gate driving the input stage of an *and* gate via a transmission line. When TD_2 fires, it supplies a current to TD_1 via TR_6, TR_1, and TR_2. Because TR_1 is biased, during this time it absorbs no current. When TD_1 fires, V_6 increases to about 500 mv. Assuming temporarily that TR_1 is not in the circuit, the increase in V_6 *prevents* the flow of I_{in}, which is reflected back to TR_6. Depending on the length of the transmission line and the pulse width produced by TD_2, this current may once again be reflected. By this time, the current pulse is traveling towards the input stage and if that stage had recovered from its firing cycle, this reflection could cause undesired firing of TD_1. With TR_1 in the circuit, current I_{in} is absorbed by TR_1 when TD_1 fires. Thus the flow of I_{in} is practically not interrupted, and consequently no significant reflection is generated. The characteristics of TR_1, TR_1, and TR_2 are chosen such that the transmission line will be approximately terminated at all times.

TABLE 1—Gate Properties and Performance

OR GATE:	
Fan-in	5
Fan-out	6
Delay (Total delay of the gate from input to output, measured at 300-mv points.)	0.27 nsec min; 0.6 nsec max
Repetition rate (Maximum repetition rate at which pulses may be applied.)	300 Mc
DC Power Dissipation	57 mw
AND GATE:	
Fan-in	6 (5 pulse and 1 level*)
Fan-out	3
Delay (Total delay of the gate from input to output, measured at 300-mv points.)	0.65 nsec; 1.00 nsec max
Repetition rate (Maximum repetition rate at which pulses may be applied.)	300 Mc
T_1: (Waiting time between application of a pulse and application of a level to an *and*-gate when switching is desired.)	0.13 nsec
T_2: (Same as T_1 except switching not desired.)	1.00 nsec
T_3: (Waiting time between application of a pulse and removal of a level from an *and*-gate when switching is desired.)	0.62 nsec
T_4: (Same as T_3, except switching not desired.)	0.13 nsec
DC Power Dissipation	137 mw
BISTABLE CIRCUIT:	
Fan-in set	4
Fan-in reset	4
Fan-out	3 + Console
Set Delay	0.13 nsec min; 0.65 nsec max
Reset Delay	0.23 nsec min; 1.1 nsec max
Set-Reset Wait (Waiting time between application of a reset pulse to a bistable gate.)	1.6 nsec
Reset-Set Wait (Waiting time between application of a reset pulse and the application of a set pulse to a bistable gate.)	2.0 nsec
Repetition Rate (Maximum repetition rate at which pulses may be applied.)	150 Mc
DC Power Dissipation	74 mw

*Performs an *and* operation between the level and any one or more of the five pulse inputs.

TUNNEL-DIODE AND GATE

A schematic diagram of the *and* gate is shown in Fig. 7. To understand the operation of this gate, it is divided into three stages: pulse buffer stage, *and* stage, and output stage. All of these operate in a monostable mode and are biased with tunnel resistors, as in the *or* gate.

A pulse input, after being reshaped by the pulse buffer stage, is applied to TD_2 of the *and* stage. Because TD_2 is returned to a positive potential, under quiescent conditions TR_4 and TR_5 are conducting currents the amplitudes of which are determined by the magnitude of R_3 and R_4, respectively. If either the pulse or the level is low, the *and* stage is inhibited from firing because of the conduction of either TR_4 or TR_5. The presence of a level cuts off TR_5, while an output from the pulse buffer stage cuts off TR_4. This causes the entire current from TDR_2 to flow into and fire TD_2.

This type of *and* gate has the advantage of not requiring tight control between the amplitude of its pulse and level inputs. The only requirement is that the inputs (V_6 and V_L) be less than 100 mv when they are low and greater than 470 mv when they are high.

Output Stage

The output stage is coupled to the *and* stage via the reverse direction of TR_6, the characteristic of which is shown in Fig. 3. Coupling in this manner is necessary in order that the quiescent voltage difference (approximately 250 mv) between the *and* stage and output stage be absorbed with negligible DC leakage current between the two stages.

The purpose of R_5 is to provide the proper biasing characteristic for the *and* stage and efficient coupling between the *and* and output stages.

Pulse Buffer Stage

This stage serves several important functions: 1) It converts the pulse input impedance of the *and* gate to that of the other gates. This prevents the *and* gate from imposing severe requirements upon the preceding gate, alleviating a reduction in fan-out of all gates. 2) It makes the pulse input impedance of the *and* gate compatible with the termination network used in the *or* gate. 3) The output of the buffer stage is relatively

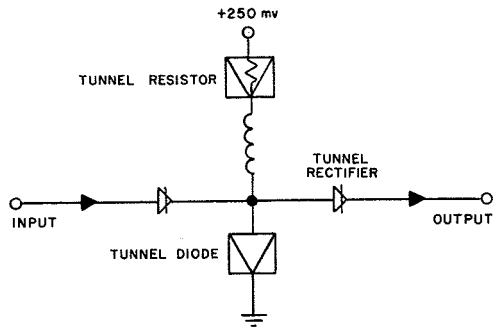


Fig. 1—Basic monostable stage.

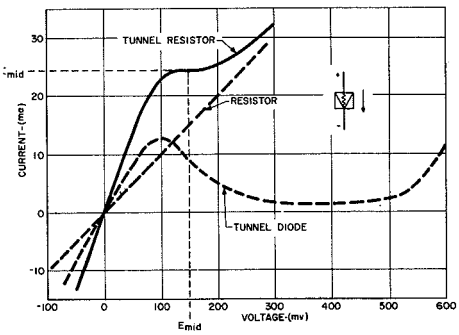


Fig. 2—Tunnel-resistor characteristic.

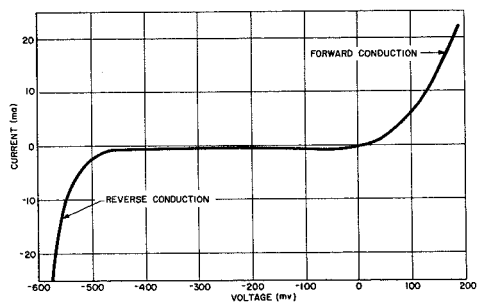


Fig. 3—Tunnel-rectifier characteristic.

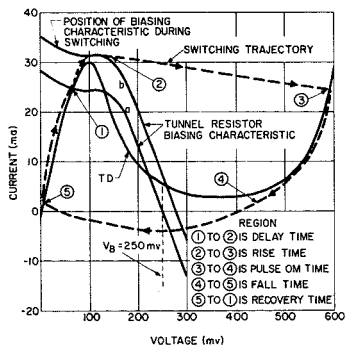


Fig. 4—Monostable stage, tunnel-resistor biasing.

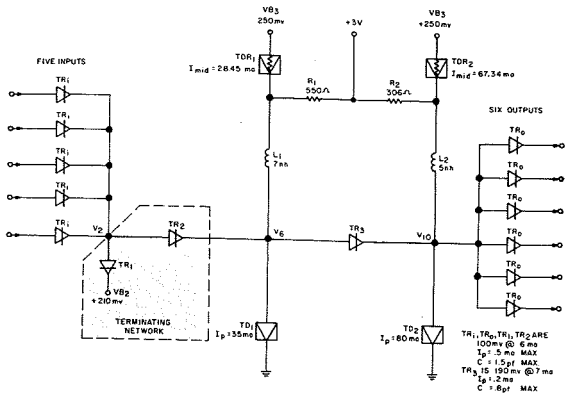


Fig. 5—Tunnel diode or gate.

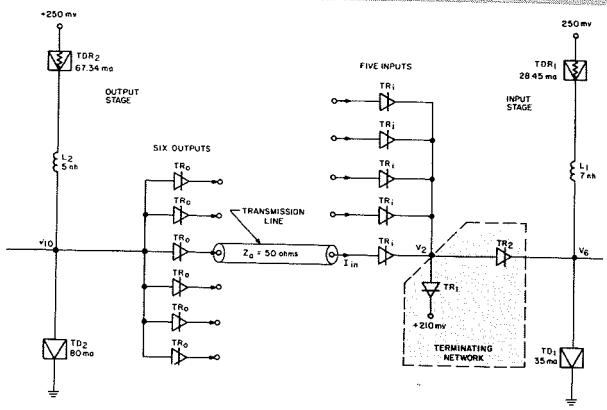


Fig. 6—Interconnection of gates.

insensitive to input pulse width variations. Thus, under all conditions of input, the buffer stage generates a narrow pulse of constant width. This reduces the waiting period for applying a level after the application of a pulse.

In this gate, trimming is employed whenever possible; R_1, R_2, and R_6 are the trimming resistors for the buffer, *and*, and output stages, respectively.

TUNNEL-DIODE BISTABLE CIRCUIT

The bistable circuit consists of a set amplifier, inverter driver, inverter, and bistable unit (Fig. 8).

The bistable unit stores a *0* when it is in the low state and a *1* when it is in the high state. The other units are monostable, and when activated, their function is to set or reset the bistable unit.

The bistable unit (Fig. 9) consists of TD_4, V_{B4}, and V_{B6} and R_4. Bistable action is obtained in conjunction with the *and*-gate loading (Fig. 10). After the curve of TD_4 is inverted and returned to 550 mv, its characteristic shifts from the first into the fourth quadrant. The current biasing characteristic of R_4, in conjunction with that of the *and*-gate input characteristic, results in a bistable load line, as indicated.

Setting

The set amplifier is a monostable stage identical to the first stage of an *or* gate. When activated by a set pulse, the set amplifier supplies an amplified current pulse to the bistable unit which is switched to the high state along with the indicated trajectory of Fig. 10.

Resetting

The inverter driver (TD_2 and TDR_2) operates like a monostable stage, while the inverter (TD_3 and TDR_3), is an inverted monostable stage.

When a reset input is applied, TD_2 switches to the high state. This causes the current I_2 in TD_2 and TDR_2 to decrease. A decrease in I_2 acts as a negative current input to TD_3, triggering the inverter to produce a negative pulse. The negative pulse causes reverse conduction in TR_6 which diverts some of the current from TD_4. (An approximate characteristic for TR_6 is shown in Fig. 3.) A current flow out of TD_4 causes the load line of Fig. 10 to move down such that the intersection at point B disappears. This causes the bistable unit to switch to the low state along the indicated trajectory.

In the bistable circuit, R_1 and R_2 trim the set amplifier and inverter driver, respectively; R_3 boosts V_2 and V_6 to values required for proper operation.

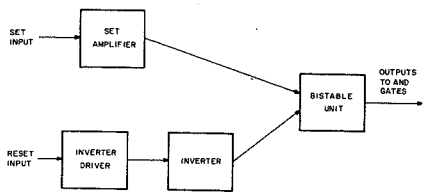


Fig. 8—Bistable circuit.

DESIGN CONSIDERATIONS

The three circuits were designed so that after having been trimmed to overcome some of the initial tolerance variation, they could operate under worst-case conditions of component and power-supply variations. This design resulted in certain rules to be adhered to by the logic designer using these circuits. Using these circuits and restrictions, a number of trial logic designs were made for general and special purpose computers. These designs indicated that the rules could be adhered to with very little or no sacrifice in system performance.

The choice of circuit parameters was based on DC worst-case analysis, and dynamic simulation on the RCA 301.

CIRCUIT INTERCONNECTIONS

All interconnections are made with 50-ohm miniature coaxial transmission lines for monostable circuits and 31.5-ohm lines for bistable to *and*-gate connections. The choice of 50-ohm lines for monostable circuits was based on obtaining optimum coupling efficiency between gates. The choice of 31.5-ohm lines for bistable circuit coupling was based on a compromise between speed of level build up and reliability.

PERFORMANCE

Table I summarizes circuit properties and performance.

Fig. 11 shows a disassembled wafer and a typical assembled wafer. The

Fig. 7—Tunnel diode *and* gate.

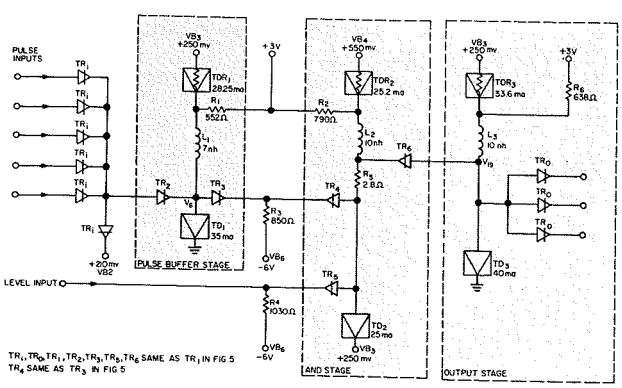
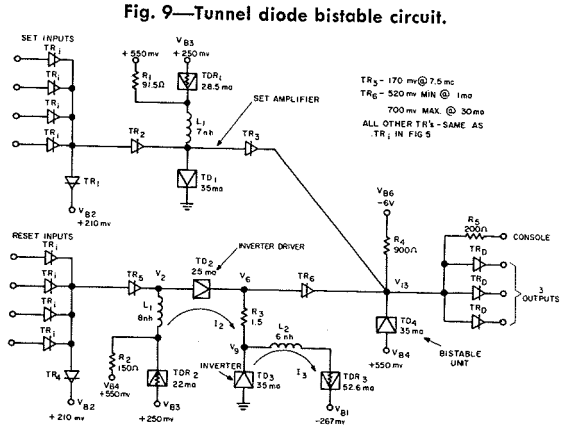


Fig. 9—Tunnel diode bistable circuit.



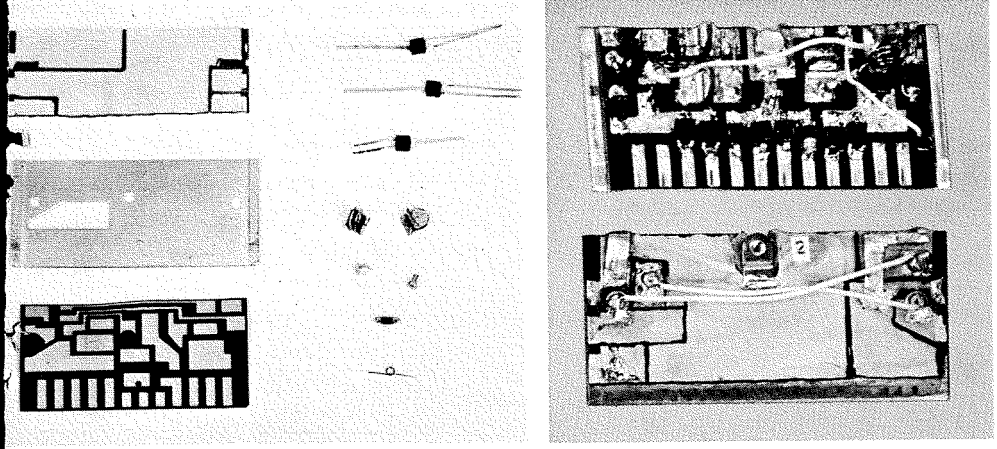


Fig. 11—Disassembled wafer, and an assembled bistable wafer (front and rear). Wafers are about 1½" long.

wafer has 12 signal connections and 6 power-supply connections. The signal connections are on top of the wafer; power is supplied to the back of the wafer. Each power supply connection is shunted by a high-dielectric pad which serves as a capacitance to absorb transients due to circuit switching. In the circuit layout, care was taken whenever possible to keep stray inductances and capacitances to a minimum. In several cases, the tunnel diode had to be mounted in a flat position in order to reduce the stray inductance to a tolerable value. This was especially true with the output of the *or* gate.

Circuits of this kind were constructed and trimmed in accordance with a trimming procedure established for each circuit. The circuits were then tested for electrical performance, which indicated reliable operation and good agreement with theoretical and computed results.

Typical output waveforms from these circuits are shown in Figs. 12, 13, and 14.

Using 40 of these gates, a 5-bit shift-register–counter was constructed and has been operated reliably at 300 Mc. The *shift mode* utilizes two bistable circuits per bit of storage and two *and* gates to transfer information from one stage to the next. In the *count mode*, the same two bistable circuits and two *and* gates are used per bit, resulting in five triggerable flip-flops, which are connected serially to function as a counter.

Fig. 10—Bistable switching.

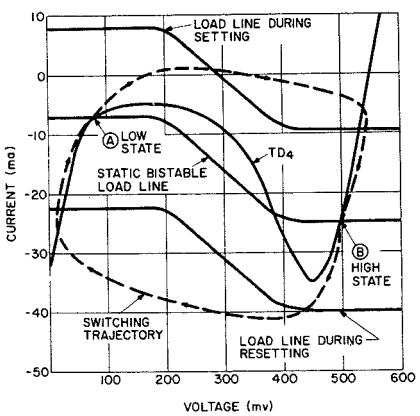


Fig. 15a shows the output of one of the bistables in ring shifting for various bit patterns. Fig. 15b shows the states of the first through the fifth bits when counting is performed.

CONCLUSION

Theoretical analysis and experiments have shown that the tunnel-diode logic circuits presented here are logically complete and suitable for the construction of large-scale, high-speed digital computers. The 40-gate model constructed with these circuits demonstrated the most commonly performed logic operations in digital computers. Among these were shifting and counting at a 300-Mc rate with an average delay per logic level of 0.5 nsec. Logic designers have made trial designs for general-purpose and special-purpose computers using these circuits, which were found to be effective and versatile logic building blocks.

ACKNOWLEDGEMENTS

The work described here is the product of a joint effort by the Logic Circuit Group of the EDP Advanced Development Section. Credit is due the following individuals for their part in this work: R. H. Bergman, for coordinating this project and for his ideas which lead to this circuit approach; E. C. Cornish, for circuit analysis and laboratory development of the individual circuits and the 40-gate subsystem; C. R. Pendred and D. Durr for dynamic simulation of the circuits on the RCA 301 Computer; I. Abeyta and H. Ur for laboratory circuit development; and W. J. Lipinski for DC tolerance analysis.

Some of the basic ideas which lead to circuit trimming were contributed by S. T. Jolly. The mechanical engineering of the wafers and assembly was done by M. E. Ecker. The power distribution system was designed by H. V. Rangachar.

The author also wishes to express his gratitude to the colleagues at Pennsauken, Somerville, and Princeton for their support and cooperation. Particular thanks are due to R. K. Lockhart and J. N. Marshall for their support.

Fig. 12—*Or* gate output voltage waveform: vert., about 300 mv above baset of waveform; horiz., about 3 nsec peak to peak. (Reference grid lost during photography.)

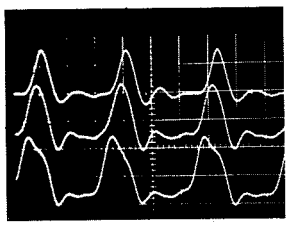


Fig. 13—*And* gate voltage waveforms. Top to bottom: output stage, *and* stage, buffer stage. Vert.: 200 mv/div.; horiz., 1 nsec/div.

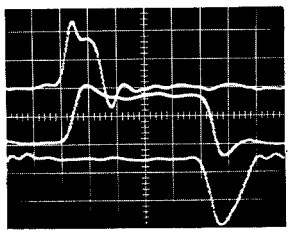


Fig. 14—Bistable circuit voltage waveforms: top to bottom, set amplifier, bistable output and inverter. Vert., 200 ma/div.; horiz., 1 nsec/div.

BIBLIOGRAPHY

1. R. H. Bergman, M. Cooperman, H. Ur, "High-Speed Logic Circuits Using Tunnel Diodes," *RCA Review*, June 1962, Vol. XXIII, No. 2. *Also see* their paper "High-Speed Tunnel-Diode Logic Circuits," RCA ENGINEER, April-May 1962.
2. R. H. Bergman, "Tunnel Diode Logic Circuits," *Trans. IRE-PGEC*, Vol. EC-9, p. 430, December 1960.
3. H. S. Sommers, "Tunnel Diodes as High Frequency Devices," *Proc. IRE*, Vol. 47, p. 1201, July 1959.
4. M. H. Lewin, "Negative-Resistance Elements as Digital Computer Components," *Proc. Eastern Joint Computer Conf.*, No. 16, p. 15, December 1959.
5. M. Cooperman, "300-Mc Tunnel Diode Logic Circuits," *Proc. Pacific Computer Conference*, March 14-15, 1963.

Fig. 15a—Ring shifting at 300 Mc: vert., 300 mv/div.; horiz., 10 nsec/div.

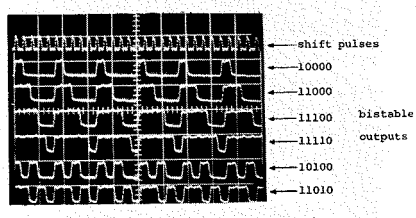
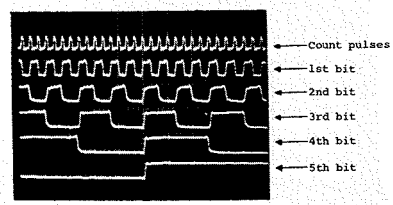


Fig. 15b—Counting at 300 Mc: vert., 300 mv/div.; horiz., 10 nsec/div.



THE NEW RCA 3301
. . . An Advanced, User-Oriented Family of Medium-Priced Computer Systems

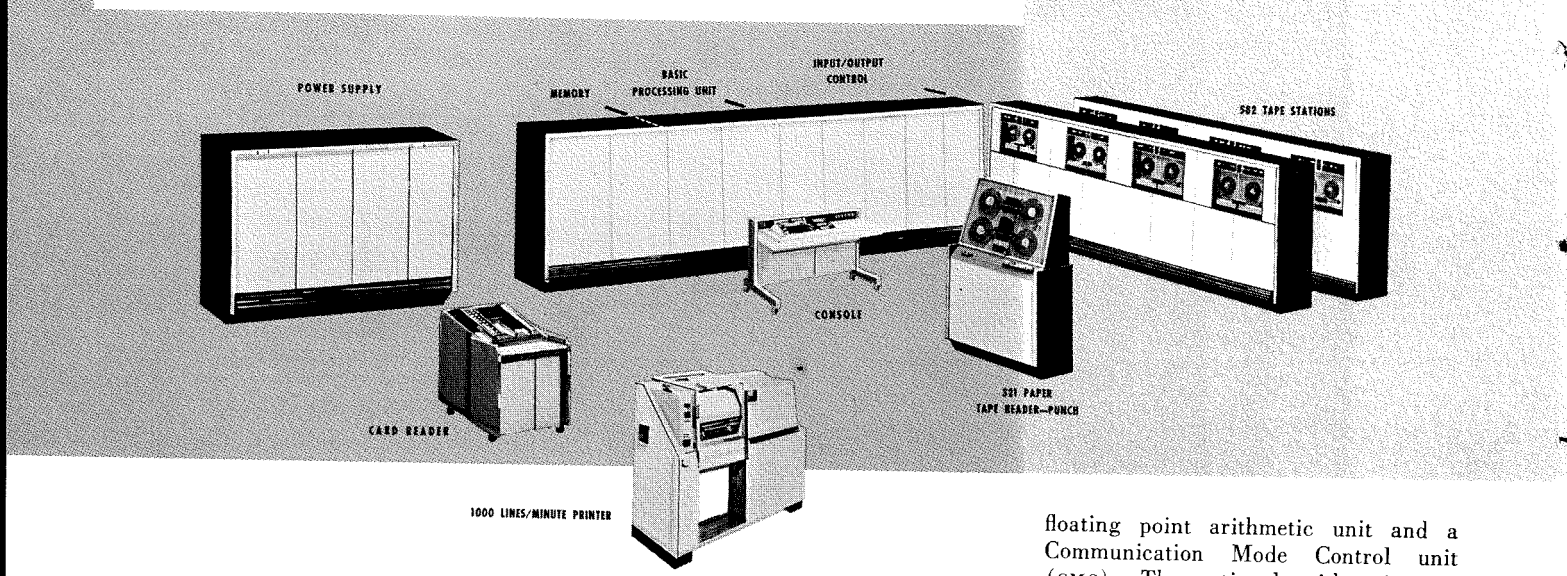


Fig. 1—The prototype complement of the RCA 3301 computer system.

Introduction of the new RCA 3301 Data Processing System (Fig. 1) culminates an intensive engineering effort to produce a distinctly advanced, user-oriented system. The RCA 3301 represents a logical extension of the RCA 501 and RCA 301 with particular emphasis on enhanced performance, greater reliability, and adaptability to both real and non-real-time environments. The RCA 3301 is a two-address, bit-parallel, character serial processor. Through the judicious design of both the command structure and the optional features, the RCA 3301 is effective and efficient in an especially wide range of applications—a goal for a medium-priced system against which all major engineering decisions were measured.

T. A. FRANKS, Ldr.
Design and Development Engineering
Electronic Data Processing, Camden, N.J.

THE "RCA 3301 System" actually refers to an extensive family of systems, because of flexibility incorporated into the basic processing unit. The many possible system configurations allow 1) efficient tailoring of the initial equipment complement to suit existing requirements, and 2) convenient capability to expand and/or reorient an installed RCA 3301 system to meet changing needs.

BASIC SYSTEM AND OPTIONAL FEATURES

Fig. 2 illustrates both the basic RCA 3301 elements and its optional features. These basic elements are:

1) *micromagnetic memory*—replaces most of the hardware registers normally required in the basic processor and operates at an independent read or write cycle time of 250 nsec;
2) *program control and central bus*—contains the main communication artery and the addressing control logic;
3) *logical processing unit*—includes the instruction execution controls and the logical, arithmetic, and comparison processing functions;
4) *main memory*—provision for storing 40,000 seven-bit characters with a complete read-write cycle time of 1.75 μsec;
5) *console and operator's typewriter*—for all operator-system communications; and
6) *input-output control unit*—includes interfaces for connecting various peripheral-device control modules capable of being operated in either of two independent simultaneous modes.

Enhancements to the processing functions of the RCA 3301 include a fixed-floating point arithmetic unit and a Communication Mode Control unit (CMC). The optional arithmetic unit allows higher-speed execution of wired-in *add*, *subtract*, *multiply*, and *divide* instructions with either 8-character fixed-point operands or 10-character floating-point operands. The CMC unit provides the connecting link between the basic processor and low-speed real-time data links. Up to 160 such data links can be handled in an independent "CMC mode" so that normal data processing is unaffected.

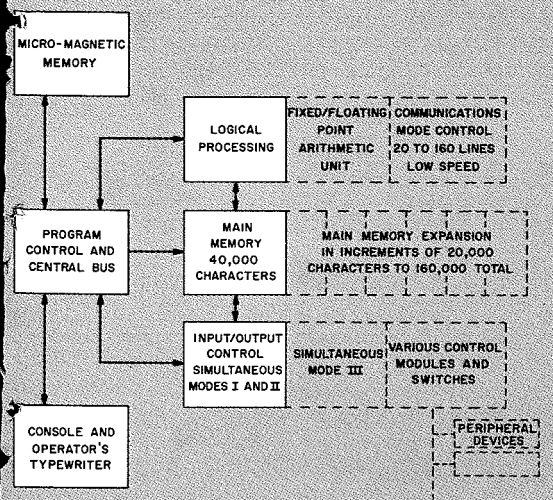
As another option, additional modules of main memory may be added in increments of 20,000 characters up to a total maximum of 160,000 characters.

The remaining optional elements consist of various control modules to link peripheral devices and the processor's input-output control. Another mode of simultaneity is available for on-line operation of up to three functions concurrently—in addition to the normal processing and CMC functions. Typical performances characteristics of these devices are included in Fig. 2.

The characteristics of the RCA 3301 System are compatible with the existing RCA 301 System;[1,2] however, the RCA 3301 provides a faster and larger main memory, higher-speed circuitry, enhanced input-output capabilities including program interrupt, and a more powerful command structure. The internal representation of data is identical with the RCA 301, and the RCA 301 instruction repertoire is a subset of the RCA 3301 instruction repertoire.

In the RCA 3301, the major hardware features include:

1) a compact 200-character micro-



PERIPHERAL DEVICES INCLUDE:

1. Magnetic Tape Stations: alphanumeric character rate options: 33, 66, and 120 kc
2. Random Access Disk Files: total capacity: 528 x 10^6 alphanumeric characters min-max access: 70-120 msec transfer rate: 32 x 10^3 character/sec
3. EAM Cards: reading: 1,500 cards/min punching: 300 cards/min
4. Paper Tape: reading: 1,000 characters/sec punching: 100 characters/sec
5. Line Printers: asynchronous mode (64 printable symbols): 800 lines/min synchronous mode (47 printable symbols): 1,000 lines/min
6. Computer to Computer Exchange Channels
7. High Speed Communications Channels
8. Interrogating Typewriters
9. Custom Real Time Interfaces
10. Real Time Clock
11. Communication Mode Control: capacity: 20, 40, 60, 80, 120, 140, 160 lines data rate: 10,000 characters/sec maximum total

Fig. 2—RCA 3301 system functions and peripheral devices.

T. A. FRANKS graduated from Rensselear Polytechnic Institute with a BEE in 1956 and received the MS from Stanford University on a fellowship program in 1957. Since joining RCA in 1956, he has taken part in the development of solid state memory circuitry; was a project engineer on several computer programs; worked on logic design of checkout equipment, and system organization of advanced computers; and was a project engineer on a BMEWS computer installation. Since joining EDP in 1962 he has been the Project Leader coordinating engineering of the RCA 3301 System. Mr. Franks is a registered Professional Engineer-in-Training in New York State, and a member of the IEEE, Tau Beta Pi, Sigma Xi and Eta Kappa Nu.

magnetic memory, used in lieu of flip-flop registers;

2) a program-interrupt feature, permitting efficient use of input-output and error-recovery capabilities;
3) a high-speed main memory, organized in 70-bit words, and available in a basic size of 40,000 characters with optional modules to raise total capacity to 160,000 characters;
4) a flexible input-output bus interface for adding various combinations of control modules; and
5) an advanced circuit and packaging design concept that balances operating speeds and design margins against ease of manufacture.

Basic Processor and Micromagnetic Memory

Fig. 3 shows the basic processing unit and illustrates how the micromagnetic memory has replaced many of the hardware registers normally required in a processor. The extremely fast cycle time is effectively employed for the same tasks normally assigned to flip-flop registers. This memory is significantly less expensive and more compact than the total number of registers it replaces. Thus, it is one of the *major state-of-the art advances* incorporated in the RCA 3301.

The micromagnetic memory consists of 200 seven-bit characters (six bits of information and parity) arranged in 50 locations of four characters each. To achieve the extreme performance required, this memory system used the concept of the RCA microferrite array.[3,1] It is a word-oriented, two-core-per-bit, linear-select configuration with three wires threaded through each core. Two are used for the driving system (one for read, one for write) and one printed wire is used for the digit-sense circuits. The independent read or write cycle time is 250 nsec. This permits reading one micromagnetic memory location into the micromagnetic memory register, or writing from the micromagnetic memory register to one micromagnetic memory location within one time-pulse period. The micromagnetic memory is functionally used for address registers, control registers, various indicators, and as temporary storage during instruction execution and progam-interrupt sequences. All of the contents are addressable by specific instructions.

The equality detection between the micromagnetic register and the main-memory address register is required to determine the termination of address-controlled instructions and input-output service sequences. Fig. 4 illustrates the use (and timing) of the micromagnetic memory during a typical instruction-fetch cycle.

Multilevel Program Interrupt

Another unique feature of the RCA 3301 is the multilevel program interrupt system. This facilitates real-time programming, servicing of multiple input-output devices, error-recovery procedures, program debugging techniques, and compatibility routines for execution of other RCA computer programs.

The three levels of program priority, in order of their priority, are: 1) *real-time interrupt*, 2) *general interrupt*, and 3) *normal processing*. Thus (1) cannot be interrupted, (2) can be only by (1), etc. There are 18 conditions which will cause an interrupt process to take place, of which 5 are designated as real-time and 13 as general interrupt conditions. The mechanization of the interrupt process involves:

1) interrupt sequence (all hardware);
2) interrupt routine (software using hardware indicators and instructions);
3) return after interrupt (an instruction); and
4) program control of interrupt (an instruction);

Step 1, the *interrupt sequence*, is initiated when a bit of the interrupt register is set, the appropriate inhibit-interrupt interlock indicator is clear, and the execution of the current normal processing instruction is completed. The interrupt sequence automatically stores the appropriate registers in standard micromagnetic-memory locations, one set for a general interrupt, another set for a real-time interrupt. The associated inhibit-interrupt indicator is set, i.e. general or real-time. The automatic interrupt sequence then obtains the *jump* address from another standard location in the micromagnetic memory and transfers control to the interrupt routine.

In Step 2, the *interrupt routine* determines which condition(s) of the 18 caused interrupt. As a result of a programmed scanning operation, this routine branches to the appropriate program. Further instructions test the various status conditions for proper recovery. After the interrupt condition has been dealt with, the software interrupt routine scans the interrupt register

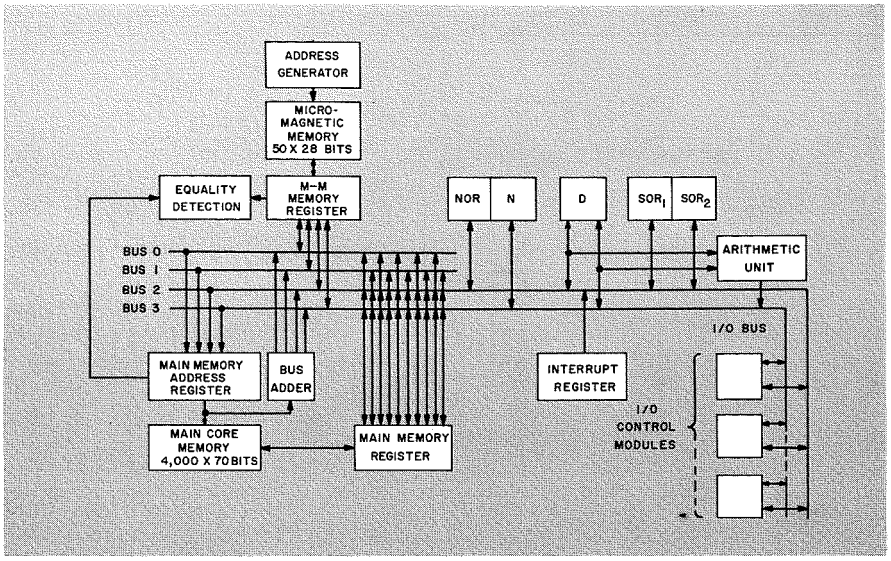


Fig. 3—Basic processing unit.

again to determine if another bit is set. If so, that condition is dealt with. This cycle is repeated until all conditions have been accommodated. Then the interrupt routine exits by means of a *return-after-interrupt* instruction.

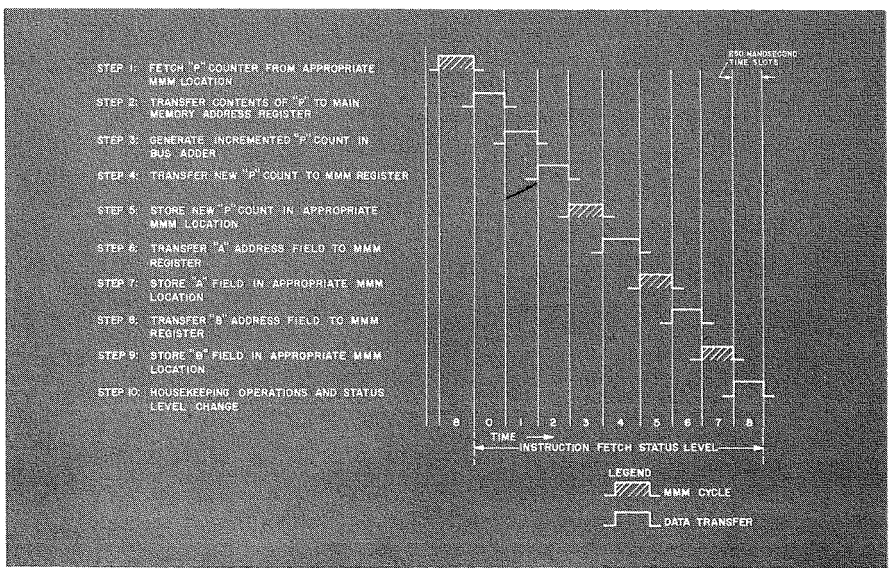
Step 3, *return-after-interrupt* instruction, automatically restores all the register and flip-flop settings that were stored in the micromagnetic memory by the most recent interrupt sequence and clears the appropriate inhibit-interrupt indicators. Then the instruction addressed by the instruction-counter register is fetched and normal processing continues.

Step 4, *program control of interrupt* by the programmer is affected by another instruction which allows the selective setting or clearing of the two inhibit-interrupt indicators.

Main Memory

The RCA 3301 random-access main memory is a magnetic-core design available in a basic size or 40,000 alphanumeric (7-bit) characters, with optional 20,000-character modules available for increased capacity (up to a total of 160,000 characters). Each location is individually addressable and can store one character. The main memory cycle is designed for 1.75 μsec and is subdivided by the basic processing unit into seven 250- nsec slots. The machine cycle, however, can be either 1.75 or 2.25 μsec, depending on the amount of control and data manipulation required during a given cycle. The 2.25-μsec cycle consists of nine 250-nsec time pulses, and is required for operations such as instruction fetch or input-output service (Fig. 4).

Fig. 4—Simplified micromagnetic memory example.



The multiplicity of connections shown between the main memory register and the central bus in Fig. 3 are a logic network. This allows the ten character positions of the memory to be interchanged with the four character positions of the bus, thus, providing the selective character-oriented operation of this system. Address incrementing (or decrementing) is performed by the bus adder in order to properly sequence instructions and operands located in the main memory.

Input-Output Devices

A broad range of input-output devices are available for any given RCA 3301. The basic processing unit incorporates the essential control logic necessary for generalized operation of peripheral devices and, by means of an extension to the central bus (Fig. 3), a standardized interface for connection of control modules. Thus, enhancements can be conveniently added to an operating system by simple field modifications. The schematic configuration of the control-module connections are shown in Fig. 5. The system design provides for accommodating up to six input-output control-module racks.

Circuitry and Packaging

The circuit and packaging concepts were selected to allow maximum performance with ease of manufacture and maintenance. The basic high-speed logic circuit is a multi-input diode gate followed by a transistor inverter. A zener diode provides proper voltage offset and charge storage characteristics between the input-diode gate and transistor base (Fig. 6). This circuit accounts for 94% of all the active elements in the basic processing unit. The other 6% are special circuits required for line drivers, line receivers, delay lines, oscillators, etc.

To minimize signal-wire lengths, a compact method of packaging circuits on plug-in module assemblies was chosen. Twenty-four basic plug-in types similar to that shown in Fig. 7 were selected for use in packaging the processor logic. These plug-ins employ vertical submodules to provide additional room for components. Appropriate test points are included. Additional ground contacts are used on the top and bottom edges of the plug-in to minimize ground impedances and increase circuit noise-immunity margins. All external signal wiring is wire-wrapped to further ensure reliability of connections. Fig. 8 shows a typical configuration of plug-ins mounted in the basic-processing and main-memory racks.

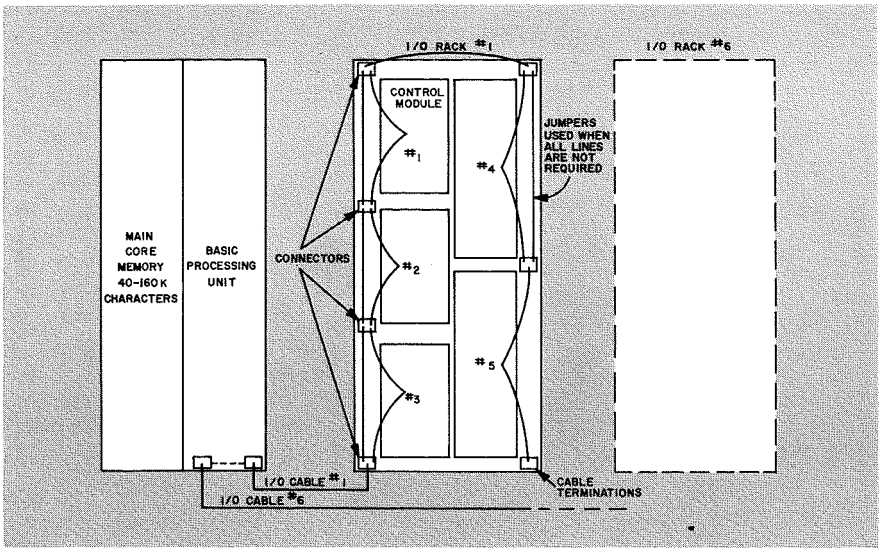


Fig. 5—Control module connections.

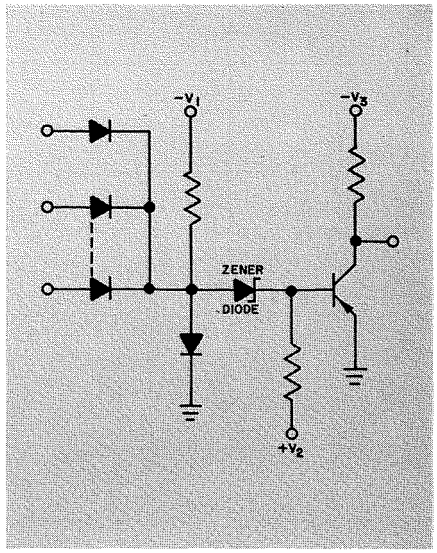


Fig. 6—RCA 3301 basic high-speed logic gate.

PROGRAMMING FEATURES

The RCA 3301 operates by character-oriented, two-address instructions. The instruction format consists of ten characters interpreted as follows:

OP	*N*	*A*	*B*
X	X	XXXX	XXXX

The first character, *OP*, specifies the basic operation to be performed. The second, *N*, indicates a count, a specific symbol, or a device identification number depending on the operation character. The next four specify the first address (*A* address field); the remaining four specify the second address (*B* address).

Indirect addressing is indicated by a bit in the least-significant character of the address. After instruction fetch, if this bit is present in either (or both) the *A* or *B* address field, the processor will automatically replace the contents of the *A* or *B* locations in the micromagnetic memory with the contents of the main-memory location addressed by the previous value of the *A* or *B* field. This process will repeat for as many levels of indirect addressing as necessary until this bit is zero.

Similarly, indexing of either (or both) the *A* or *B* address fields is indicated by two bits of the second least significant address character. There are three address fields, each with an associated increment field and all are located in the micromagnetic memory. Indexing always precedes indirect addressing. Identification of indirect addressing and indexing are indicated by the original instruction, but the effect of indirect addressing occurs on the address formed after indexing.

For descriptive purposes, the instruction repertoire may be classified into four general categories: 1) input-output, 2) data handling, 3) arithmetic, and 4) decision and control. (Typical execution times are shown in Table I.)

Input-output instructions link the processor with the peripheral devices (through the control modules) to position and/or search tapes and disk files, bring data from an input medium into the processor, or send data from the processor to an output medium. Five basic functions are provided that can be executed in any one of the two (or optionally three) simultaneous modes (plus one special instruction for specifying operation of the communications mode control). These functional varieties are: 1) input-output control, 2) read, 3) read reverse (magnetic tape only). 4) write, 5) erase (magnetic

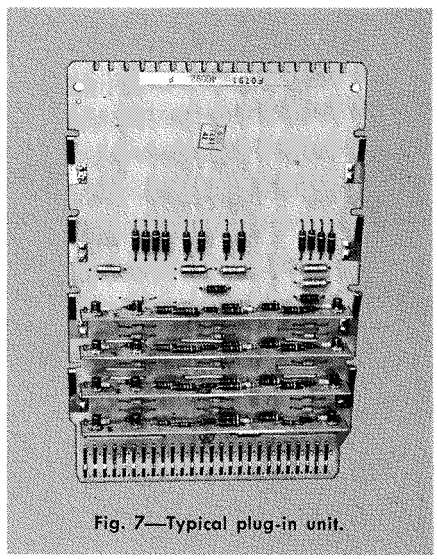


Fig. 7—Typical plug-in unit.

Fig. 8—Basic processing and main-memory racks.

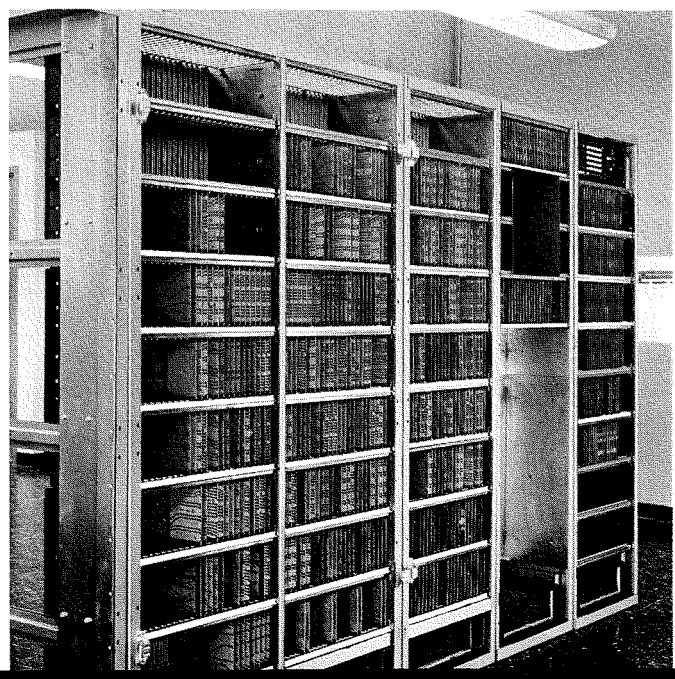


TABLE I—Typical Instruction Execution Times

Instruction	*Time, μsec*
DATA HANDLING:	
translate by table (6-character field)	33.75
transfer data left (6-character field)	23.25
ARITHMETIC:	
data add (6-character operands)	
no end-around carry condition	37.25
with end-round-carry condition	61.75
logical or (6-character operands)	33.75
DECISION AND CONTROL:	
Unconditioned Transfer of Control	2.25
Repeat	5.75
Set (or store) *register*	5.75

Notes: Indirect addressing adds 3.5 μsec for each level of modification. Indexing adds 2.25 μsec for each address modified.

tape only), and 6) communication mode control (one instruction only). Operations such as tape rewind, track select (disk file) and paper advance are initiated by the processor (via an input-output control instruction), but once underway, are completely independent in execution.

The data-handling instructions are nonarithmetic operations for manipulation of data stored in the main memory. The instructions included in this group permit control of data fields by symbol, address, or count. Instructions for edited manipulation of varied fields are also included in this group.

The arithmetic instructions include: 1) four decimal operations, *add, subtract, multiply,* or *divide*; 2) three operations used to alter the bit configuration of an operand through the use of logical commands; and 3) three operations for arithmetically manipulating four character fields in accordance with the rules of addressing. The decimal instructions operate in accordance with standard arithmetic rules and are designed to handle operands of mutually equal lengths. Three instructions, *logical or, logical and,* and *exclusive or* constitute what may be considered as a separate arithmetic category. They can alter the bit configuration of an operand by the employment of a second operand to "mask out," or insert 1 bits. The three address-oriented instructions allow operations of *address add, address subtract,* and *address compare* on four-character operands consistent with the progression rules of memory addresses.

The decision and control instructions influence the sequence of operation. Four instructions enable the programmer access to registers of machine indicators directly and one instruction provides conditional control; that is, it chooses a path according to selected conditions. Another instruction either halts or causes a program interrupt in the processor's operation. A *repeat* command enables the execution of loops a designated number of times. The *compare* instruction enables the programmer to determine the relative magnitude of two operands of equal length. The last two instructions in this group enable program control and restoration of machine conditions after interrupt sequences, as described in a previous section.

In addition to this command structure, the overall system efficiency is further improved by:

1) built-in and programmed accuracy controls;
2) automatic storage of the contents of various working program-control locations in the micromagnetic memory;
3) character addressability providing completely variable data organization; and
4) machine code covering the full range of numerics, alphabetics, and special symbols.

The accuracy-control philosophy of the RCA 3301 System includes not only error detection, but also error recovery. When an error occurs and is detected by wired-in parity and invalid-code checking circuits, program control is transferred (by the interrupt feature) to an executive error-recovery routine. Appropriate actions can be taken at this time. Transient processor malfunctions, as well as input-output-equipment errors, can be handled by these techniques.

Facilities for automatically storing various program-control address fields are included in the basic processing unit. These are called STA, STP, and STPr.

STA automatically occurs at the conclusion of selected instructions. In STA, the final contents of the *A* field located in micro-magnetic memory are automatically stored in standard main memory locations. This permits the subsequent use of the final *A* field contents and is a convenient programming technique to eliminate memory searching time.

STP occurs whenever program control is to be transferred out of immediate sequence; STP automatically stores the contents of the instruction-counter field in another set of standard main-memory locations at the conclusion of those instructions that would cause transfers of control. The stored address is the address of the instruction that would have been executed if the transfer of control had not taken place.

STPr similarly automatically stores in standard main-memory locations the instruction address immediately following the repeat instruction, and is used for looping control reference during a repeat sequence.

CONCLUSION

This paper has described the most significant engineering features incorporated in the RCA 3301 Data Processing System. Obviously, many design details and novel techniques have been either presented very generally or not at all due to space limitations. Readers interested in further information should consult the EDP Marketing Department, Cherry Hill, New Jersey.

ACKNOWLEDGEMENTS

The author acknowledges the intensive efforts expended by the entire RCA 3301 engineering design team on this project. These efforts extended from establishing the initial system concepts, during 1962, to final manufacturing release during 1963. As of the time of publication of this paper, the prototype system will have been in hot tests for two months, and complete operational capability is anticipated during October 1963. The successful conclusion of this project within the original performance, schedule, and cost goals represents a significant achievement for the design team. In particular, the author wishes to acknowledge the efforts of: G. R. Gaschnig, W. F. Glass, B. I. Kessler, J. E. Linnell, J. J. O'Donnell, P. H. Reynolds, G. D. Smoliar, G. J. Waas, and R. H. Yen.

BIBLIOGRAPHY

1. H. Kleinberg, "The RCA 301: Flexibility at Low Cost—An Engineering Challenge," RCA Engineer, Vol. 6, No. 4, Dec. 1960-Jan. 1961.
2. A. Turecki, "The RCA 301 Scientific Computer," RCA Engineer, Vol. 8, No. 6, April-May 1963.
3. Dr. H. Lemaire, "New Techniques for Ferrite Nanosecond Memories," RCA Engineer, Vol. 8, No. 2, Aug.-Sept. 1962.
4. D. F. Joseph, "The NS1—A New 400-nsec Microferrite Memory System," RCA Engineer, Vol. 8, No. 6, April-May 1963.

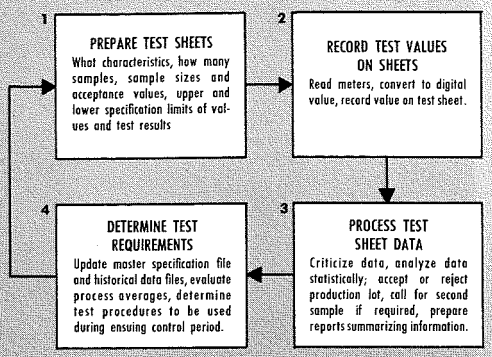


Fig. 1—Quality Department acceptance sampling procedure.

Fig. 2—John Gates (author, seated) and Bob Conroy at the STAR.

JOHN R. GATES received his BSEE from the University of Nebraska in 1942. He has been with RCA in various capacities since 1942. His first 13 years were with the Electron Tube Division, where he has been Mgr., Mechanical Equipment Design; and Mgr., Advanced Equipment Development. In 1947, he received his MS from Stevens Institute of Technology. He was awarded a Sloan Fellowship in 1955 to study at MIT, and received an SM in Industrial Management in 1956. In 1956, he assisted in forming the Automation Systems Development group for the Electron Tube Division, and was Mgr., Automation Projects Administration; and Mgr., Technical Systems. A major endeavor since 1957 has been in developing data-handling systems for product quality data. Mr. Gates is a Member of the IEEE and the Institute of Management Sciences.

QUALITY-CONTROL TEST-DATA SYSTEM USES THE RCA 501

Computers available at RCA Electronic Components and Devices in Harrison, N. J. (both RCA 501 and 301) are being applied to many business and product-control problems. One especially successful application is described herein: the automation of a quality-control acceptance sampling procedure that is vital to the profitable mass production of receiving tubes.

J. R. GATES, Mgr.
Technical Data Systems
Electronic Components and Devices
Harrison, N. J.

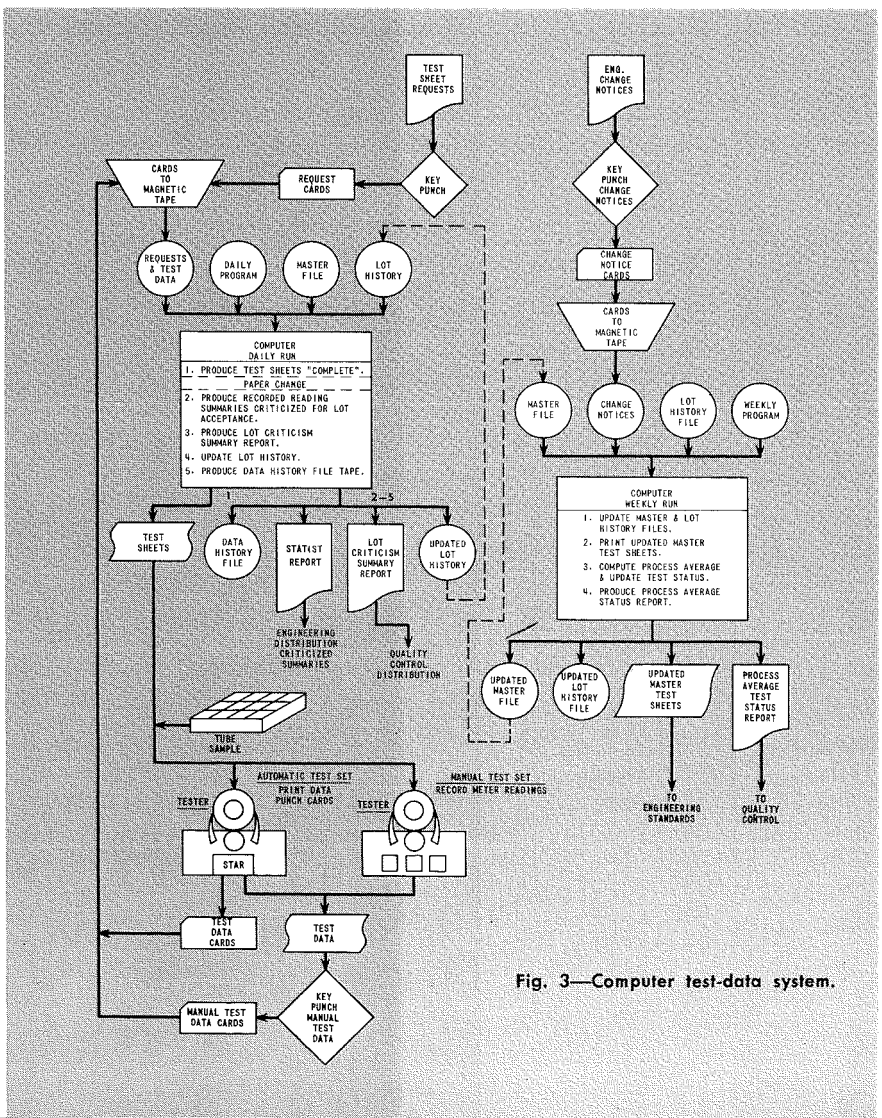


Fig. 3—Computer test-data system.

A SMOOTH-RUNNING computerized quality-test data system at the Harrison, N. J. receiving-tube plant has successfully automated the Quality Department acceptance sampling procedure. The computers (RCA 501 and RCA 301 are both involved) analyze and make *reject* or *ship* decisions on the total plant output in one-half hour of running time each night. The many advantages of this data-handling system include such key features as minimized cost increase or handling-time increase with increased production volumes and much improved quality insurance when competition forces expense-cutting campaigns.

The actual project to develop this Quality Acceptance system got a serious start in 1957 and reached the computer in 1961 after progressing from the original manual system, through a punched-card phase, and on to the computerized system of today. The many hands involved in its development consisted of a project team, some RCA Corporate Staff "systems expert" assistance, local-management backing, and some extremely cooperative user personnel.

QUALITY-CONTROL TESTING

The basic system, or job, which was automated is illustrated in Fig. 1. As can be seen, it is a closed-loop arrangement with certain aspects of the first operation depending on the analysis of results of past final operations. The object is to test a sample lot of tubes to a given flex-

ible specification. The test-recording document is prepared, specifying the sample size, tests to be performed, allowable number of rejects and similar items. These specifications are tightened or relaxed, based on the results of past test histories. The tests are then performed and results are recorded on the test sheet. The data are processed for correctness of sample size, conformance to limits, number of rejects, statistical quantities, need for a second sample, and the like. A decision can then be made as to whether the lot represented by the sample can be passed on and shipped or must be rejected. In addition, reports can be prepared summarizing the total product *pass* or *reject* picture and engineering and quality-control information. These test results are then evaluated with other past history, the process averages are determined and testing specifications are relaxed or tightened, if necessary, and made ready to be used with the next sample to be tested. Hence, the loop is closed.

INITIAL MANUAL IMPLEMENTATION

For many years, a fully manual system quality-data system was used—a tedious series of manually interpreted and updated printed specifications, many test-equipment setups, human interpretation and recording of meter readings, clerks and desk calculators for data reduction, and result judging and reporting. Because volume often changed with changing production levels, the clerks and testers either worked more or less hours, or their number was varied. The many drawbacks to such a system are obvious. The manpower problem can be a serious one. Human fatigue is a real gremlin, especially in the case of test operators or clerks who work with columns of poorly written figures for hours at a time.

The manual system was relatively slow; consequently, often only the most critical tests were analyzed and the remaining data were not used unless trouble occurred. At such times, the required data could be extracted and treated manually by an engineer investigating the problem.

History data of tests could not be readily extracted and processed when desired. The main source for this type of data was files full of raw data (test readings) which were neither easy to survey nor cheap to use.

AUTOMATION BY PUNCHED CARDS

In 1958, a decision was made by Receiving Tube Engineering to purchase an automatic test set referred to as STAR (for *S*pecialized *T*ube *A*nalyzing *Re*corder). STAR, shown in Fig. 2, is a plugboard preprogrammed test set which tests manually inserted tubes according to the plugboard program of tests, test conditions, and acceptance limits. The tests are sequenced and grouped as desired, test conditions are varied as required from test to test, results of each are compared to limits, and *pass* or *fail* notations are made.

This programming feature permitted test-set changeovers to be made in a matter of seconds. The really big "plus" of this equipment, however, is its readout. Test results are recorded in two ways—typed on a test sheet, and punched into cards.

Such a piece of equipment can do much to speed up testing and eliminate setup and data-recording errors. It can also be many times more effective if it is integrated into a complete test-data processing system which plans for and makes the best use of men and machines.

To develop this improved system, Receiving Tube management set up a project team consisting of representatives from Engineering, Quality Control, and Data Processing. Several months of study by the team were necessary to insure a good understanding of the manual system in use at that time. As expected, some of the accepted procedures were found not documented, and some documented ones were not the ones in use. It was probably fortunate that STAR was not an "off-the-shelf" item because, as the team developed a data-processing system, they were also able to influence the development of some needed features in the test equipment. Some of these features were size of printed output document to be handled, method of decimal-point notation, and provisions for entering data description into the punched-card output.

The team came to realize that the computational job required in this work was a large one for two main reasons—volume and complexity. More than 40,000 test readings were being collected each week, and the mathematics required varied from test to test and from tube type to tube type. These factors indicated that a *complete* computational system using existing tab equipment with an electronic calculator would not be too practical. Such a system could be set up, but it seemed questionable whether it could be kept operating properly.

The punched-card system which finally evolved was used for more than a year and put much order into a complicated data system. Punch-card test-specifications files were built so that test sheets, ready for the recording of results, could be produced by machine and would contain information to which collected data could be compared for pass or reject decisions. The system was flexible enough to accept data collected either by STAR or from a test operator at a manual test set. The manually collected data was keypunched and then merged with the card output from STAR.

It was not practical to do all of the calculations, for reasons previously stated, but some which were common to all tests and tube types were handled. Average, range, and a total defect count were performed on all tests, and a summary report was prepared on the available electric accounting machine. The more difficult or peculiar-to-test-or-tube computations and decisions had to be left to manual means. The punched-card system did include a more accessible data-history file. The card file as set up was in a form for easier mechanical processing, but keeping the data tied back to a changing specifications file was quite a chore for this generation of automatic data-processing equipment.

APPLYING THE RCA 501

The punched-card system indicated the possibilities of a completely automated test-data system. Up-to-the-minute specification files, the automatic tightening or relaxing of decision criteria based on product history, fast error-free computation, unemotional decision making by machine, and the neat, orderly presentation of output information were some of the more obvious advantages over former manual methods. What was needed was a computer capable of handling the full data-reduction and analysis load from this test area.

One of the systems analysts was, at that time, engaged in a study of several small-scale computers which might be used for engineering problem-solving. He investigated the idea of renting one of these small computers for process-average calculations on the Quality Project, and then using any remaining time for engineering problems. His findings indicated that the most promising of the small card-oriented computers would have required almost 40 hours each week for the one application, leaving little time for anything else.

Early in 1959, the Electron Tube Division made the decision to place on order an RCA 501. Top-grade programming talent was then added to the project team so that the punched-card program could be picked up by the computer using the best computer techniques. The team then had the opportunity and task of completing the job which had started as a

major effort with STAR, and had become difficult because of its bulk-data-processing aspects in the punched-card phase. Fig. 3 shows the computerized system, including STAR as an important cog in the test area. This system went into operation in January 1961.

Fully as important as the main jobs of calculations and comparisons for decision making is the file-maintenance portion of the system. Accurate, up-to-date files must be maintained or the output information will not be reliable. In an engineering atmosphere where specifications change is normal, an error-free, rapid file-updating procedure is demanded if test data are to be judged against the proper criteria. As Fig. 3 shows, the main input for file maintenance is engineering Change Notices. These notices are the means by which the master specification file, a magnetic tape, is kept current. Specifications for a new tube type are entered in the file in essentially the same way.

In this system, file-updating is done once each week. This frequency has been satisfactory, but is definitely no computer limitation. Changes are entered and documented in only a few minutes of computer time. Each file-updating computer run produces printed copy in the form of new master specifications sheets for those specifications which were changed, as well as a new master file on magnetic tape. The printed pages can be distributed to those locations where specifications books are kept.

The power of the computer was well demonstrated recently. Several general changes were to be made to 100 different tube types. Instead of entering separate handwritten change notices for each change, a short computer program was written to seek out the places for change in the master file, and create a computer-written change notice. For about $40.00, the program was written, tested, and run. It created 2,800 change notices on tape, which never had to come out of computer language. These changes were then applied in the next regular file maintenance run. The manual method would have required many months to accomplish this task, and reference books would have remained out of date for some time.

Another part of the weekly file-maintenance computer run is used to calculate the latest process averages, including the most recently entered data. As explained earlier for the basic system, the computer considers the history of past test lots (10 lots are presently used), and adjusts the testing specifications for future testing. As can be seen, the computer is now taking a big decision-making load from the human. Some very comforting thoughts about this are:

1. *The computer will not get tired and make errors.*
2. *The computer will not leave any of this work undone when volume is great, because its appetite is tremendous.*

The daily quality-test computer run also has two main tasks: it must produce test sheets for the recording of tomorrow's test results; and it must analyze and make decisions on tests recorded today. In the printing of test sheets, it actually refers to the master magnetic tape specifications and lot-history files, and produces a custom test document which identifies the lot to be tested, tests to be made, test limits, sample size, number of allowable rejects, calculations to be made, and many other parameters.

This particular task was one of the first "sticklers" which confronted the team at the start of the project. If all products were tested alike, or even if there were several patterns, the test-recording document might possibly be preprinted and a standard computational procedure set up. The power of the computer is a great advantage in this respect. In about thirty seconds, the computer refers to its magnetic tape memory and produces a 2- to 5-page test sheet.

The computations and analysis part of this run is handled in a somewhat unique manner. Because the RCA 501 has a relatively large internal memory (more than 65,000 characters), a matrix scheme can be used rather than many computer passes which would do the rather involved job in a run-after-run fashion. All test data for one tube type are brought into memory at one time, together with specifications from the master file and lot histories from the lot-history tape. These three pieces of information create a matrix which is held in memory until all calculations and decisions have been made on the one tube type. The tremendous advantage of an automatic audit should be noted at this point. The computer will not accept any less data than the specifications require. Any deviation will cause rejection of the data. All calculations and decisions are then worked on at the microsecond internal speeds of the computer. No referrals outside the machine are necessary until the answers are ready for printing. With all data so conveniently arranged for processing, the "comparison-to-limits" feature of STAR was abandoned in favor of the computer operation. Each and every test reading is now looked at by the computer and compared to limits.

As Fig. 3 indicates, the information output from this part of the run consists of a detailed Statistical Analysis for the engineer and quality or manufacturing man, and an abbreviated Lot Decision (Quality Acceptance) Report. The latter report gives the number of lots passed or failed, and if failed, gives the reason why. A shipping clerk can ship from it, or a quality-control manager can see where his efforts should be concentrated.

Another important advantage of the computer in this work is the history-storage feature and the possibilities for retrieval and analysis. A magnetic-tape data-history file is added to by each day's run, and a ten-lot history tape is maintained. The use of these reservoirs of information has really only started, but the ease of access and possibilities of fast analyses are apparent. Data for certain selected periods or product are periodically fed into a computer-plotting program to develop X-Y plots and histograms. Other requests have caused simple special programs to be written to develop averages or ranges for given periods. There are endless possibilities in this area.

THE FUTURE LOOKS BRIGHT

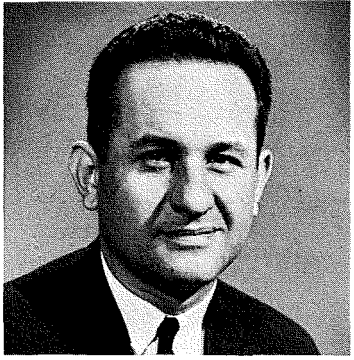
There are tremendous possibilities for these techniques in almost any business situation. A shrinking product line can be helped to remain competitive, or an expanding business can be assisted in maintaining control. RCA Electronic Components and Devices faces both of these conditions.

Receiving Tube engineers are already at work adding to and revising the computerized test-data system to increase its power. They are visualizing a statistically powerful system based on the use of variables data which would eliminate most of the *go, no-go* testing presently in use. Savings possibilities in testing and associated processing might easily be as much as a million dollars a year. Other product lines on the verge of large expansion programs are also considering the computer as a tool to help maintain product control.

The computer has arrived, and its power has been demonstrated. Future benefits will be a function of ingenuity in developing its application.

ACKNOWLEDGMENTS

The author gratefully acknowledges the assistance and encouragement of the following people in this project: W. E. Bahls, R. A. Jacobus, S. A. Cochrane, P. J. Musso, M. A. Cofone, H. W. Kirk, R. E. Conroy, B. W. Wheeler, and A. C. Grover, Jr.



RALPH E. MONTIJO, JR. received his BSEE from the University of Arizona in 1952. In 1952, he joined RCA's Specialized Training Program. He was then assigned to the Computing Systems Engineering Section where he participated in the development and design of the BIZMAC. In 1956, he was promoted to engineering management; and in 1957 directed the West Coast Engineering Laboratory of RCA's Electronic Data Processing Division. In 1957-61, he directed systems engineering and development effort on: data systems for airborne vehicle flight testing, random access memories, magnetic tape stations, operations research, and input-output studies. He also made major contributions to the USAF's DATACOM network. In 1961, he was promoted to his present position of Manager, Systems Engineering for Electronic Data Processing. Mr. Montijo has authored several technical papers, and is a member of the IEEE, the ACM, and the AMA.

EDGE . . .
Electronic Data Gathering Equipment

EDGE provides a low-cost, reliable method for remote input of data to computers that is competitive with manual input. The high-volume information supplied directly to the computer enables business decisions on more timely information. This extension of the input-output capability of computers foretells a day when systems like EDGE, coupled with volatile displays (not unlike present military control centers), may be a major tool for decision making.

R. E. MONTIJO, Jr. Mgr.
Systems Engineering
Electronic Data Processing, Camden, N.J.

ALONG WITH the rapid assumption by the computer of its rightful place in our operating systems has come the recognition of its limitations. And, its primary limitation in the area of input-output has been magnified as the internal computing speed and magnetic-tape data rate have risen. Inherent in this problem is the physical separation between the locations where data is generated and subsequently used, and the location of the processing element.

The EDGE (Electronic Data Gathering Equipment) system was developed to implement the tasks of collecting, code converting, and reducing the disparity between present and desired input-output data rates for typical computers.

Simplicity, flexibility, and reliability are fundamental to meet stringent cost-performance requirements for a system such as EDGE. The functions which EDGE automates are far less sophisticated than those performed by the computer. In the kind of locations where EDGE might be installed (for example, a factory work area), EDGE must compete with proven manual methods that are well accepted by local personnel. And because it is intended that EDGE be utilized by such local personnel (not computer personnel), installation and operation must be simple and inexpensive; performance must be consistent and reliable; and the integrity of data handled by the system must be above suspicion.

A two-year program of study, analysis, evaluation, and optimization of customer requirements was performed upon several hundred combinations of available techniques. As a result, EDGE provides the means for reading input documents, accepting data directly from humans, converting the data to a machine-usable code, transmitting it to a distant central point, and recording it for subsequent processing.

When EDGE is combined with other elements of RCA data-communications and data-processing equipment, the entire data gathering, processing, and output cycle may be performed *on-line*; the term *on-line* is used here to describe the processes of both data gathering and computation. (Source-data recording by EDGE is always performed "on-line" in the sense that EDGE input devices are directly linked to the EDGE central recording equipment.) The term *off-line* EDGE (as used here) refers to the setup wherein the EDGE central recording equipment produces a punched paper tape for subsequent use as a computer input. The term *on-line* EDGE refers to a direct link between EDGE and the computer, without intermediate punched paper tape recording. In the EDGE system itself, intermediate storage devices are eliminated, since data is transmitted from its input point(s) through a passive network of telephone lines and line switching devices to the EDGE central recorder. Storage elements are thus only the input media and the ouput store.

The balance of capability between the system components was chosen to provide a simple telephone-subscriber type of interface between remote input devices and the central equipment that was amenable to commonly used telephone-system signalling and installation practices. This interface also enhanced the desired ability to operate over long lines with least future modification.

ELEMENTS OF THE SYSTEM

The EDGE System (Fig. 1) is comprised of three basic types of equipment: remote input devices, passive line or circuit switching devices, and the central recording equipment with its time generation function. Input stations are used to enter data from remote points over two-wire telephone in-plant lines, which are switched by line concentrators into a smaller number of two-wire trunks that are terminated by the central recording equipment.

Input Station

The input station (Fig. 3) is used in great quantity in a given EDGE system application. Physically, it includes two enclosures: a reader unit, and a subset. There are two basic types of reader units used: The general-purpose input station uses a data-input reader (Fig. 2). The alphanumeric input station (Fig. 4) is a more specialized unit and utilizes an alphanumerical reader unit. Both of these devices are designed to sit on a countertop or wall-mounted shelf.

In addition to data read from input documents and manually set data levers, the input station adds certain fixed data and control symbols to each transaction. The subset accepts data from either type of reader unit, translates transaction message characters to the EDGE transmission code, and transmits these characters in a character-serial, bit-serial stream over standard telephone lines using a 2,000-cps phase-modulated tone.

Line Concentrator

The Line Concentrator acts as a switching intermediary to distribute the intermittent demand for service from a large number of input stations to a smaller number of two-wire trunks connected to the central recorders. The line concentrator is mechanized with standard telephone-type, combinational relay logic. Its circuits and components are similar to that used in private-automatic-telephone-exchange (PABX) units. The line concentrator (Fig. 5) accepts up to 25 input lines, which can be switched to four trunks.

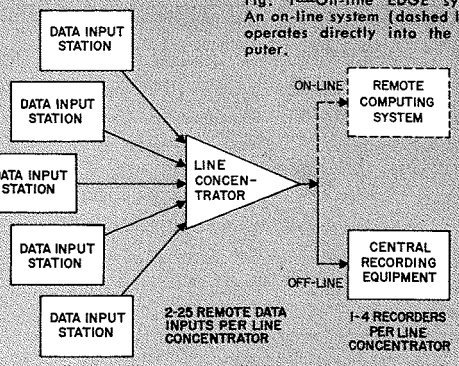


Fig. 1—Off-line EDGE system. An on-line system (dashed lines) operates directly into the computer.

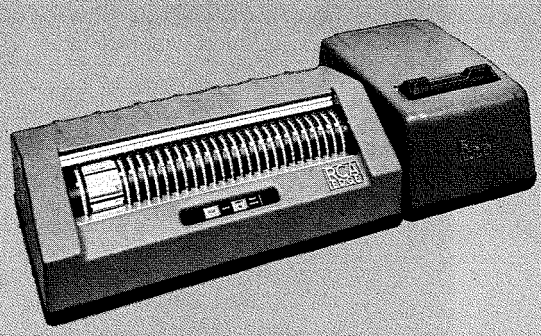


Fig. 4 — The alphanumeric reader unit is used to originate transactions requiring manually settable fields of alphanumeric data. Up to 25 digits of alphanumeric data may be entered into a transaction by this device. Data is entered by operation of its 25 wheel-type switches. This unit is used primarily in the origination of remote inquiry transactions, and to create records with a long alphanumeric data field for which no prepunched cards are available at a location.

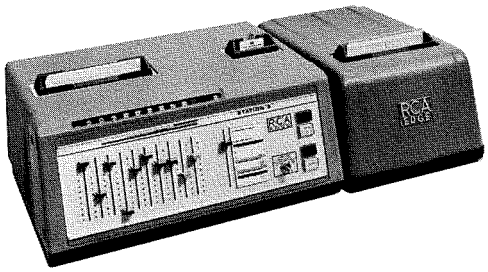


Fig. 2—The data reader unit accepts data from an EDGE token that contains up to 12 alphanumeric characters of punched data, an 80-column Hollerith-coded punched card, and up to 11 manually-set numeric characters from 10 multiposition sliding switches. All manually-selected characters are visually displayed. A single manually-set transaction-selector sliding switch is provided for identification of 11 transaction types. Transactions which are comprised of Token Data only; Token Data and Variable data; or Token data, Variable Data, and Hollerith card data can be originated. A key-operated supervisory switch restricts the use of certain pre-designated transactions.

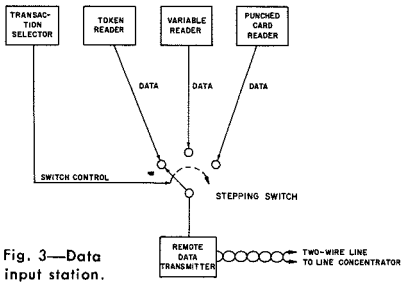
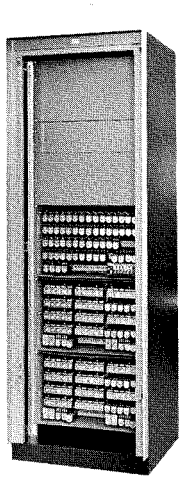


Fig. 3—Data input station.



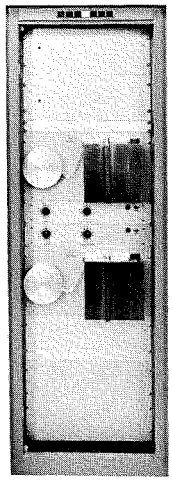


Fig. 5—A Model 6244 line concentrator with the door and cover panels removed. Model 6242 provides two output-trunk connections to two receivers, while Model 6244 provides four output-trunk connections to four receivers.

Fig. 6—A two-receiver-punch central recorder assembly. The receivers contain parity checking circuitry and transmission sequence control logic to insure proper reception. Two receivers and recorders with a single power supply are contained in each central recorder rack.

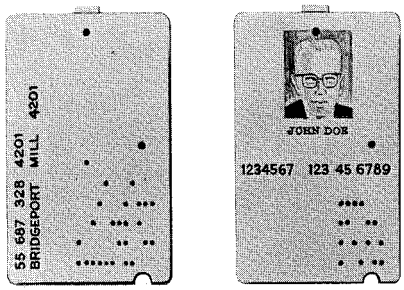


Fig. 7—The EDGE token provides space for punching up to twelve alphanumeric, seven-bit characters in binary-coded-decimal format. The seventh bit allows parity checking of each character read from the token. The EDGE token is credit-card sized (2⅛" or 3⅜"), and is compatible with standard automatic credit-card embossing and punching equipment.

Table I—The EDGE Transmission Code.

CHARACTER MEANING	PUNCHED CARD CODE EQUIVALENT	EDGE CODE
The code is arranged with the least significant bit designated 2^0 and the most significant data bit designated 2^5. Parity in the EDGE code is defined as even.		
Space		000000
1	1	000001
2	2	000010
3	3	000011
4	4	000100
5	5	000101
6	6	000110
7	7	000111
8	8	001000
9	9	001001
&	12	010000
A	12-1	010001
B	12-2	010010
C	12-3	010011
D	12-4	010100
E	12-5	010101
F	12-6	010110
G	12-7	010111
H	12-8	011000
I	12-9	011001
—	11	100000
J	11-1	100001
K	11-2	100010
L	11-3	100011
M	11-4	100100
N	11-5	100101
O	11-6	100110
P	11-7	100111
Q	11-8	101000
R	11-9	101001
O (Zero)	0	110000
/	0-1	110001
S	0-2	110010
T	0-3	110011
U	0-4	110100
V	0-5	110101
W	0-6	110110
X	0-7	110111
Y	0-8	111001
Z	0-9	111001
Start Message (SM)	not used	111110
End Message (EM)	not used	111010
Item Separator (ISS)	not used	111101
Delete Message (DM)	not used	101110

Table II—Bit Sequence for One Frame.

Bit Period	1	2	3	4	5	6	7	8	9
Bit Name	Start	2^0	2^1	2^2	2^3	2^4	2^5	2^6	Stop
Bit	1	*	*	*	*	*	*	*	0

* Character bits, 1 or 0

Table III—EDGE Format Symbols.

<	Start message symbol (SM)
•	Item separator symbol (ISS)
>	End message symbol (EM)
■	Delete message symbol (DM)
T_c	Transaction code
I_b	Unit identifier character
T	Token reader character
V	Variable character
C	Chard character
H_{10}	Ten hour character
H_1	Hour character
$H_{.1}$	Tenth hour character
$H_{.01}$	Hundredth hour character
W	Day of Week Character

Table IV—The Transmitted Message Formats.

These formats apply to both an off-line and an on-line system. In an on-line system, the transmitted format is stored in memory where it is combined with the time and day code field output of the time scanner, on-line by computer program. The off-line receiver-punch adds the time and day code field at the central recorder equipment.

TITLE	FORMAT
T-6	$\lceil T \mid \mid \mid \mid C\ D_1\ D_2\ D_3 \bullet T_1 — T_6 \rceil$
T-12	$\lceil T \mid \mid \mid \mid C\ D_1\ D_2\ D_3 \bullet T_1 — T_{12} \rceil$
V	$\lceil T \mid \mid \mid \mid C\ D_1\ D_2\ D_3 \bullet T_1 — T_{12} \bullet V_1 — V_{10} \rceil$
C-X	$\lceil T \mid \mid \mid \mid C\ D_1\ D_2\ D_3 \bullet T_1 — T_{12} \bullet V_1 — V_{10} \bullet C_1 — C_X \rceil$
C-Y	$\lceil T \mid \mid \mid \mid C\ D_1\ D_2\ D_3 \bullet T_1 — T_{12} \bullet V_1 — V_{10} \bullet C_1 — C_Y \rceil$

Central Recorder

The modular central recorder used with off-line EDGE consists of receivers and punched-paper-tape recorders (Fig. 6). A time equipment unit is associated with the central recorder to automatically supply time-of-day and day-code data to each receiver-punch. Dual time emitter units provide extra reliability and unambiguous read-outs during time changes without the need for a blanking period.

Central Receiver Terminal

When an EDGE system is used on-line (i.e., linked directly with a computer), the central recorder is replaced by a central receiver terminal designed to operate with an RCA 301 system that is equipped with a communications-mode-control (CMC) unit. The central receiver terminals replace the receiver-punch units in the on-line configuration.

In the on-line configuration, the time equipment unit is replaced by the time scanner on-line dual (TSOL) channels, which are sampled by the CMC in the same manner as it scans all 80 receiver trunks.

In all other respects, the equipment and operation of the basic EDGE is the same for on-line as for off-line operation.

THE TRANSMISSION SYSTEM

The code used in transmission is called the EDGE *transmission code* (Table I) a 7-bit, Hollerith-derived, alphanumeric code. Data read from the punched card and manual levers are code-converted prior to transmission. EDGE tokens are punched in EDGE transmission code and, therefore, bypass the code-conversion process. Although EDGE transmission code is always utilized between the subset and receiver, the output of the receiver may be converted to variations of the basic code.

The transmission of data in the bit-serial form requires parallel-to-serial conversion at the subset and serial-to-parallel conversion at the receiver using shift registers. Serial transmission requires bit synchronization and character framing to properly extract discrete characters from the bit stream.

A frame contains 9 bits. The first bit of the frame is designated the *start* bit and is always a *1*. The succeeding seven bits are six *data* bits and one *parity* bit. The ninth bit is designated the *stop* bit and is always a *0*. The presence of a *1* in the *start* bit position of every frame provides the means by which the serial-to-parallel shift register in the receiver determines the beginning of each frame. Loss of this bit will cause loss of synchronization, failure to satisfy the parity check, and will generally be detected within three frames (or characters).

Table II illustrates the bit sequence for a frame, the relationship between the *data, parity, start,* and *stop* bits.

Transmission of data from an input station utilizes the 2-kc carrier frequency-generated within the subset from the 4-kc timing source. The 2-kc carrier exists in two forms: a *1* phase, and a *0* phase, which are 180° out of phase. When a marking element is present at the subset output, the *1* phase carrier is transmitted. When a spacing element is present, the *0* phase carrier is transmitted. At the central receiver, a phase detector monitors the 2-kc input signal and generates a pulse for each change of phase of the carrier. This pulse triggers a binary circuit, the outputs of which are read into a shift register each bit time, thus recontracting the transmitted character in binary form.

ORGANIZATION OF DATA

EDGE uses a semivariable data-field and message-length concept to reduce the number of unwanted space characters that would otherwise be required. This feature, together with the concept of masked setup, clearing and system switching time enables EDGE to achieve an effective transmission efficiency equal to or greater than might be achieved with a fixed-message-length format operating at double the EDGE transmission rate of 27.7 characters/sec.

The scanning order for the reader-unit components and their corresponding data fields is fixed in this sequence at the time of factory assembly: *station identification, token, variable* and *card.* The *token-only* transaction for attendance recording creates the shortest transaction message used and accounts for the greatest number of messages per unit time during clock-in and clock-out periods. Hence, with the token data field occurring first in the scanning sequence, the stepper may be caused to short-scan by homing immediately after the last character of the employee number within the token field is read. Two typical tokens are shown in Fig. 7.

While the volume of *token-variable* transactions is signficantly less than *token-only* transactions, homing of the stepper immediately after scanning of the last character of the variable data field also eliminates unwanted space characters.

A *token-variable card* format repeats the field length requirements of the token-variable format and adds the *card* field. The card field may contain a maximum of 80 characters. Movement of a single taper tab in the reader unit stepper determines the number of columns which are read from a card.

Several different symbols are used in describing the message formats which can be used when transmitting data in the EDGE system (Table III). The format of the transmitted message depends upon the transaction that is selected. Each position of the transaction selector switch is wired to effect reading and transmission of the desired format. Whether or not data must be entered into the card reader, token reader, and/or variable data reader is a function of format and interlock selection.

Data fields within a message may or may not contain data. When data is not required from a particular field for a particular transaction, all character positions of the corresponding data field will contain space characters if the field is scanned. The formats are listed in Table IV.

In an off-line EDGE system, all data are punched on paper tape in the order received. Upon arrival of the *end message* symbol, the receiver completes its various checks on the message. If the message checks satisfactorily, the *end message* symbol is replaced by an *item separator,* wherein the time and day-code field of five data characters is scanned from the time equipment unit and appended to the portion of the message received. An end message symbol is then inserted.

Should the receiver detect a parity or sequence error in an incoming message, the punching of all subsequent characters is inhibited and a *delete message* symbol is punched on tape in place of the character found to be in error. The output from the paper tape recorder is a 7-bit code punched in 1-inch paper tape.

The EDGE token (Fig. 7) is a rugged, multipurpose, machine-readable input medium for use with the input station. This token has many applications, including employee identification, tool crib check-out, standard operation data, and machine utilization data.

ACCURACY AND CHECKING FEATURES

EDGE provides four basic types of accuracy checking: 1) input-station interlocks to assure that messages are properly set-up before transmission; 2) parity check of token characters read from token, and parity-bit generation for variable and card field characters; 3) parity and symbol sequence checks of the transmission to protect against transmission errors; and 4) recording checks to assure accurate recording on paper tape.

Input station checks include:

1) A *punched card insertion check*

which rejects the card if it is inserted incorrectly.

2) A *token insertion check* which rejects token if inserted badly.
3) A *card-attendance exclusive interlock* which prevents transmission of an attendance message when a card is inserted in the card reader and token-insertion transmission-initiation is used.
4) A *ready interlock* which prevents transmission of any selected transaction message until all required inputs are properly satisfied.
5) A *supervisory key-switch* which provides for the restriction of certain transactions.
6) An *automatic reset* which provides automatic return of all input documents and reset of all manually-set levers after a message transmission has been received and verified.

Transmission checks include:

1) Automatic retransmission of messages for transmission errors.
2) Automatic shutdown and alarm of faulty input stations and/or receivers when error incidence is excessive. When an input station fails to transmit a message correctly after 15 to 35 seconds of automatic retransmission, it alarms and retains all documents and settings until manually and deliberately cleared by the operator.

Recording checks include:

1) *low paper indicator* illuminates an alarm at the central recorder.
2) *end of paper alarm* disables the receiver and causes message to be diverted to other receivers.

The coordination method used between the input station and the receiver is closed loop. No transmissions are initiated without issuance of a *request to transmit level* from the input station, and subsequent receipt of *permission to transmit* from the receiver. No message transmission is assumed to be correct without receipt of *verification* by the input station. If *verification* is not received, automatic retransmission is repeated until a 15-to-35-second hold-down time delay expires at the input station. A similar arrangement enables the receiver hold-down to expire if satisfactory transmission is not achieved in 35 seconds. In both cases, hold-down expiration results in an *out-of-service* alarm.

FUNCTIONAL REDUNDANCY

In a typical EDGE installation, all system components contribute to the overall capability of the system. The elements of the system are designed and interconnected in a manner to prevent the failure of any component or major system element from causing a catastrophic loss of all system capacity. Automatic alternate path routing within the network results in partial degradation rather than total failure of the system when a major malfunction occurs. This desirable characteristic has been implemented in the following manner:

Input Station: Because of the multiplicity of stations, loss of a station results only in loss of the time required for an employee to walk to the next nearest input station. Use of separate two-wire communication lines between each input station and the line concentrator minimizes the danger of catastrophic loss of a subsystem because of sympathetic faults that are characteristic of commonly used way-station type operation or wire failures.

Line Concentrator: Alternate path capability through two of four trunks is provided by the internal relay logic of this unit. In addition, telephone switching circuitry of this nature has been perfected to a very high degree of reliability by many years of field operation.

Central Recorder: The multiplicity of receiver-punch combinations and the automatic re-routing by trunk that is characteristic of line concentrator prevents total failure of the central equipment. Thus, failure of any receiver, punch, or power supply results in only partial degradation of system capacity.

Time data for the central recorder is provided from dual time emitter units. Hence, loss of one of the time units results only in small loss in system handling performance.

APPLICATION

In designing an EDGE System for a particular customer application, several factors must be considered in optimizing the equipment complement. These factors include:

1) Volume of messages by type per unit time.
2) Geographic distribution of remote units to reduce long walking distances for operators.
3) Need for two-way transmission.
4) Types of transactions to be originated and set-up times.
5) Ratio of input stations to line concentrator to receivers necessary to satisfy traffic requirements.
6) Allowable attendance recording queues.
7) Physical separation between units in observance of maximum loop resistance.

An EDGE System in combination with communications control computers and other system elements forms a completely integrated data-communication and processing system.

While the detailed procedure for optimizing an EDGE System complement is beyond the scope of this paper, there are several considerations and performance characteristics of general interest:

Traffic Analysis: Each customer's operation must be analyzed to determine the number of transaction types per unit time which the system must handle. Traffic loadings must be determined in terms of messages and characters per unit time for the areas served.

Geographic Layout: Layout and location of the EDGE devices within a plant is generally performed on the basis of employee population density and the average walking distance for employees to and from an input station in their area. One input station is generally assigned to employees located within a radius of 75 feet. Within this rule, the minimum number of input stations for an area is limited by the input station set-up, clearing, and transmission time. A data input station can clock up to 30 employees per minute. A receiver, however, handles 85 employee attendance transactions per second. Therefore, the maximum number of input stations which are connected to a line concentrator is either limited by the receiver message rate and the number of trunks on the concentrator or by the 25 input lines to a concentrator. For low-volume applications, two or more line concentrators may be connected in tandem, thereby increasing the ratio of input stations per receiver. Input-station-to-line-concentrator telephone-line lengths are limited to a total loop resistance of 900 ohms. This resistance represents a distance of 2 to 6 miles depending on wire gauge. The line-concentrator-to-receiver telephone lines may have a loop resistance of 2,400 ohms.

Installation: A major advantage of the EDGE system is its use of standard two-wire telephone lines between all units. Such lines may be installed by private contractors, plant maintenance personnel, or by the local telephone company. Telephone company lines are usually installed at a cost of approximately $5 per drop and rented for $1 to $2 per quarter mile per month. This arrangement minimizes capital investment. Once the telephone lines are installed, removal and relocation of a unit is accomplished with the same ease as moving the telephone instrument.

ACKNOWLEDGMENT

The many contributions to the planning, development, and design of the EDGE System by Messrs. C. J. Pritchard, J. P. Reid, R. R. Helus, W. Saeger, R. P. Graeber and B. P. Silverman are gratefully acknowledged.

APPLICATIONS OF COMPUTERS TO SYSTEM STUDIES

M. S. CORRINGTON
Applied Research, DEP, Camden, N.J.

WHENEVER A mathematician starts to develop a new branch of mathematics, it is necessary to pay the tooling costs to provide the special functions required to solve the equations. For example, the integral

$$\int_0^x \sin t\, dt = 1 - \cos x \qquad (1)$$

is easily evaluated using elementary functions. If the problem is changed slightly to

$$\int_0^x \frac{\sin t}{t}\, dt = \mathrm{Si}\, x \qquad (2)$$

a more advanced function, the sine integral, is needed. When the argument of the trigonometric function becomes nonlinear, as in

$$\int_0^{\pi} \cos\,(x \cos\theta)\, d\theta = \pi J_0\,(x) \qquad (3)$$

the zero-order Bessel function is required. These functions are "tooled up" in the sense that someone has provided the effort required to study them in detail and to compute good tables.

NONLINEAR ANALYSIS

In the solution of nonlinear problems, one quickly runs out of these special functions and tables; closed-form expressions are no longer available. At this point, mathematicians tend to go in two different directions. One type will spend his time deriving long orthogonal-function or series expansions to cut down on the computational effort required to find the numerical value of the function. The second type of mathematician *will develop computer programs to solve the equation directly*, using crude mathematical methods repeated often at high speed to converge on the answer. It is no longer necessary for him to spend his time doing the drudgery and tedious algebra required to grind out the series or other approximations. He is then free to spend his time developing new concepts and improving the theory.

An example will make this clear. If an engineer is required to solve a nonlinear ordinary differential equation, and if he is not an expert on this subject, his best bet will be to look for the answer in a table of solutions.[1,2] (Reference 1 contains 1,600 different solutions and Reference 2 contains 2,315 solutions.) If the answer is not in one of these two books, the average engineer might as well give up.

Even if the solution is found in a handbook, it may be in terms of some special function that has never been adequately tabulated. One could spend many years studying all of these solutions and still not be very successful at solving nonlinear system problems.

COMPUTERS REDUCE TOOLING COSTS

The modern high-speed digital computer changes all of this. A single general-purpose program can tabulate the solution to any differential equation in the two books, to a prescribed accuracy, in a few seconds. It can solve systems of equations so complex that most mathematicians would quickly give up in frustration using conventional methods. The differential equations can be linear or nonlinear, simultaneous, or higher degree, and the computer can solve them all with the same program. There is no need for new functions or a different special technique for each new problem. The mathematician or engineer can spend his time developing new concepts or interpreting the results; the computer will fill in the details. This means that mathematical tooling costs can be substantially reduced, since the general computer subroutine needs to be written only once. It then goes into the "library" and can be used by relatively unskilled labor from then on.

COSTS AND SPEEDS OF COMPUTATION

The speed and cost reduction that can be achieved with modern computers is illustrated by the approximate values in Table I. The exact figures will vary somewhat depending upon what peripheral equipment is needed, the details of the arithmetic and logic used, and the skill of the programmer.

It is thus clear that an amount of arithmetic that would take an entire lifetime for a man using a pencil and paper can now be done in a few minutes. One can now solve problems easily that were impossible a few years ago.

AUTOMATION OF CIRCUIT THEORY

A second example of interest to electronics engineers is in the field of linear lumped-constant circuit theory. It is possible to feed a schematic into a computer and come out with the steady-state or transient response of the network. This can be done by reading in a list of the components as a single-column matrix and a second two-dimensional matrix of $+1$'s, -1's, and 0's to connect them together. The computer can then use Kirchhoff's laws and matrix inversion to reduce the transfer function to a ratio of two polynomials. Standard subroutines can then be used to find the frequency response, phase response, time delay, or envelope delay of the network.

If the transient response to a given driving force is required, the computer can find the roots of the denominator, expand the transfer ratio in partial fractions, find the inverse Laplace transforms, and tabulate the transient as a function of time. The entire process will be completed in a few seconds on a modern computer. If the engineer were to do this on a desk calculator, it would take at least two or three days of tedious work to complete the calculations and to make sure that no errors had been made.

Such a program can be used to study tolerances on components, to find the effects of temperature changes, or to compare the performance of alternative designs. It probably would be possible to store all of the reliability data in the computer memory and to come out with the failure rate to be expected.

SIMULATION OF COMPLEX SYSTEMS

Often it is easier, less expensive, and quicker to simulate a complete system on a computer and to perform the experiments to find the best design than it is to do the work in the laboratory. Ad-

TABLE I—Comparative Costs of Computation

Computer	*Approximate Cost per Hour*	*Relative Speed*	*Computer Time Required*	*Cost of Lifetime of work = 100,000 hr.*
Man	$ 7.00	1	50 years	$700,000
Desk Calculator .	7.50	10	5 years	75,000
IBM 650	40.00	2000	50 hours	2,000
IBM 709	300.00	0.2×10^6	30 min.	150
IBM 7090	400.00	1.6×10^6	4 min.	27
RCA 601	300.00?	2.0×10^6	3 min.	15
CDC 3600	475.00	3.2×10^6	2 min.	16

vanced systems can be simulated which would be very expensive to build, or where experimentation is not feasible. The computer can change one thing at a time and one can be sure that it is the only thing changed. If the optimum design can be defined in terms that the computer can recognize, feedback can be used to search out the best design.

Such simulation of equipment does not teach one how to build a new device. It shows what the new device would do if it were built, and helps one to decide whether he would like it if he had it. It is useful in deciding whether one understands a system well enough to construct a good mathematical model. Some typical systems computer-synthesized at RCA are:

1) *Stereo phonograph record*—to calculate distortion and intermodulation due to finite stylus size.
2) *Video amplifiers*—to study transients.
3) *TV deflection yokes* — to eliminate "snivets" which are unwanted lines in the picture.
4) *Analog-digital convertor* — to determine output error rate.
5) *FM tape recorder*—to find distortion due to band limiting, aperture effect, and comparison of different demodulators.
6) *Temperature variations of satellite*—to find effect of alternate sunshine and darkness as it orbits the earth.
7) *Dipole immersed in plasma*—to find the change of impedance when the antenna is put in a tensor medium.
8) *Retina of the eye*—to show the variation of the response with time after stimulation with a light pattern.
9 *Adaptive learning machines*—to find the best way to adapt a filter to a sorting operation.
10) *Noise in systems*—solved with Monte Carlo methods.
11) *Neural networks*—to find the best nonlinear operations for a given data-processing system.

AUTOMATION OF DESIGN AND PRODUCTION

It is sometimes possible to automate an entire design and production installation. For illustrative purposes, suppose one had a business making a line of transformers or electric motors. The steps might be as follows:

1) The salesman who is talking to a customer calls the plant giving the customer's specifications and the number of items desired.
2) The computer starts with the specifications and designs the transformer or motor, using a design program, stored on tape. It may modify the design if the price of steel and copper changes or if special size or weight is important.
3) The program prints out the list of components required, makes any special drawings needed, checks the inventory of parts and materials and updates the inventory, prepares the orders on the factory where needed, punches out the tape for the computer-controlled machine tools and wiring machines, computes the price to quote to the customer, checks the factory production schedule to determine the delivery date, prints out the shipping label, determines the best shipping method, and makes out the order acknowledgment and invoice.

All of this takes only a few seconds on a fast computer—a combination of scientific computing, data processing, and accounting.

MONTE CARLO APPLICATIONS

There are many processes where one cannot write a complete deterministic sequence of formulas that transforms the input data into the desired result. The source may be a random process, such as noise in a communication network, or randomly arriving people waiting for service, the queueing process.

Band-limited stochastic processes can be simulated on the computer by generating a sequence of random numbers having the required statistics, and by using regularly-spaced samples of signal plus noise to represent the process. The samples are processed in the computer in the same way they would be if they were sent through the communication system. At the output the computer can use statistical subroutines to determine means, variance, autocorrelation functions, etc., to answer questions.

This is really an "experimental" method for studying random processes. It can be made as accurate as desired by taking long enough runs of random numbers, or by using special techniques to reduce the variance of the output.

MATCHING THE DISPLAY TO THE HUMAN SENSES

The human eye has a remarkable ability to detect a very tiny signal immersed in noise if the display is suitable. If one had a large wall covered with black and white spots, the eye could quickly spot a tiny red one, even though the signal-to-noise ratio might be very small. If a drawing consisted of a sequence of parallel lines, the eye could quickly see one that was slightly crooked.

The human mind is not suited to thinking in terms of mathematical transforms, unless one has had extensive experience with a given type of transform. It is hard to obtain this experience without a computer or special laboratory equipment. There is reason to believe that a computer could be used to process the data so that the display would be especially suited to the human senses. For example, the Hilbert transform of speech sounds will produce an orbit on an oscilloscope that is distinctive for each sound. A pattern of each desired sound could be sketched on the end of the oscilloscope tube and a deaf person could practice each sound until he mastered it, even though he could not hear. Electroencephalograms could be processed before the doctor studied them to make it easier to decide whether there were any abnormalities in the brain functions. Underwater sounds could be modified by the computer to make a display especially suited to detecting unfriendly submarines. The ability to recognize certain patterns could be increased considerably by carefully matching the data to the special abilities of the human senses.

SUMMARY

If man is included in the computer loop, the combination can accomplish many things neither one can do alone. Man uses multipurpose parallel data processing and the computer usually does serial processing. It is not a question of whether computers are better than men for a given job, but how men and machines can work together as the machine takes over the drudgery and leaves the man free to create new concepts and techniques.

BIBLIOGRAPHY

1. E. Kamke, *Differentialgleichungen Lösungsmethoden und Lösungen*, vol. 1, 3rd ed., Chelsea Publishing Company, New York, N. Y., 1959.
2. George M. Murphy, *Ordinary Differential Equations and Their Solutions*, D. van Nostrand Company, Inc., Princeton, N. J., 1960.
3. Martin Greenberger, (Editor), *Management and the Computer of the Future*, John Wiley & Sons, Inc., New York, N. Y., 1962.

MURLAN S. CORRINGTON received a BSEE in 1934 from the South Dakota School of Mines and Technology, and the MS in 1936 from Ohio State University. From 1935 to 1937 he was a graduate assistant in the Physics Department of Ohio State University, and in 1937 he joined the Rochester Institute of Technology where he taught mathematics and mechanics. In 1942 he joined the RCA Television Division. In April 1952 he became a Manager of the Advanced Development group and was responsible for audio, acoustics, receiving antennas, radiation measurements, and theoretical work. In February 1959 he transferred to DEP Applied Research, where he is now an Engineering Leader. Mr. Corrington is a Fellow of the Acoustical Society of America, a Fellow of the IEEE, and a member of the Society for Industrial and Applied Mathematics. He has been active on many national and local IEEE committees and has helped write many industry-wide standards. He has published some 50 technical articles and is the author of textbooks on applied mathematics and machine shop practice. He holds 8 patents.

ACCD PROGRAMMING SKILL CENTER

H. J. PLATT, Ldr.
Real Time Engineering
Aerospace Systems Division
DEP, Burlington, Mass.

DEP Aerospace Communications and Control Division (ACCD) engineering provides a complete system programming capability in the new Programming Skill Center (PSC) at Burlington, Mass. A wide range of available personal skills and experiences are being applied to a broad technical spectrum of programming tasks. The PSC has demonstrated its capability in producing systems analysis, systems synthesis, design, programming, and production of operational programs of varying size and complexity for digital and analog equipment.

In terms of major functions, the group is comprised of systems analysis and design personnel, programmers, and various types of support personnel. The PSC group has been operating as a functional entity since 1960; however, many of the present subgroups have been in existence for a much longer period. Capabilities and experience of the engineers are varied and include work with the following computers:

1) RCA 301, 501, and 601
2) ACCD-developed computers STREAC (which stands for "streak"), the Aerospace Micromodule (AM) 3100, and AM 3200 series
3) IBM 650, 704, 705, 709, 7090, 1401
4) Remington Rand UNIVAC Solid State 80, UNIVAC II, 1103, 1107
5) Burroughs Datatron 25 and E-102

Equipment available to PSC engineers includes the Burroughs E-102, and an IBM 7090 and 1401. In addition to these computers, there also exists a breadboard model of an airborne computer called STREAC and a 200-amplifier electronic differential analyzer installation. An IBM 7090-1401 combination used in connection with the BMEWS Site III effort was shipped to England in 1962, and has been replaced by another IBM 7090-1401 combination.

The ACCD Programming Skill Center is organized around two groups: the analog-computer facility reporting to I. Akerblom, Manager of Engineering Services, and the Programming activity or digital-computer facility under R. A. J. Gildea, Manager of Programming.

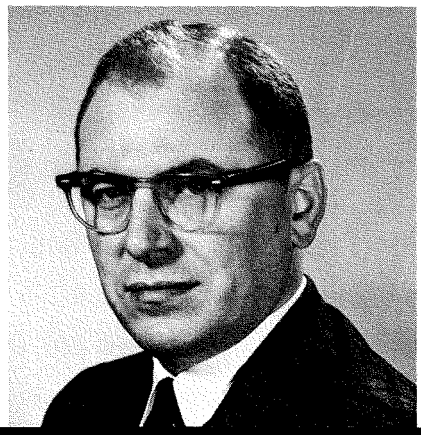
REAL-TIME PROGRAMS

In systems programming, past and present efforts embrace a wide range of activities from prime contracts in programming to support activities for other sections of ACCD and DEP. The Programming Skill Center specializes in handling real-time programs; such applications are characterized by timing constraints in which the problem dictates the manner of solution. This contrasts with the use of an arbitrary mathematical technique to determine how the program evolves. Capsule descriptions are given herein of real-time programs in which this Skill Center has been involved.

Checkout Data Processor (DP) for BMEWS Sites I and II

This special purpose digital computer inserts real-time simulated radar target data (i.e., missiles and satellites) into the BMEWS central data processor. This operation occurs while the processor is operating on-line and to evaluate the ability of the BMEWS equipment to perform correctly.

HERBERT J. PLATT received his BSEE from Pratt Institute in 1950 and his SM degree from Massachusetts Institute of Technology in 1952. At M.I.T., he was first a research assistant and then a staff member; Mr. Platt was a member of the Digital Computer Laboratory and then the Lincoln Laboratory. He participated in the design, analysis, and testing of electrostatic storage tubes for digital computer memories, the design and analysis of circuits for the AN/FSQ-7 XD-1 computer of the SAGE System, and in the analysis and cure of interface problems between the XD-1 computer and other peripheral devices. Mr. Platt joined RCA in 1955. He has studied applications of digital computers to real-time problems. His recent responsibilities have been as a Leader in acceptance testing of the BMEWS Site III Missile Impact Program and in carrying out the design, analysis, and implementation of digital computer programs for guidance and control of a missile.



The Missile Impact Predictor (MIP) Program for BMEWS SITE III

The prime effort was to produce an operational program for a BMEWS modified IBM 7090 which would receive and process real-time radar data reports and determine by means of several discrimination criteria whether any of the objects sighted are threatening missiles. Using list processing and control program techniques the MIP operational system is comprised of approximately one-hundred programs tied together in functional blocks and controlled by a rather elaborate executive control system.

Automatic Programmed Checkout Equipment (APCHE)

Automatic Programmed Checkout Equipment (APCHE) involved the design of card decks used to check out subsystems of the ATLAS missile during tests. The programmer examines the subsystem and determines the items to be tested and a plan to carry out the test. The programmer then specifies the test deck by the preparation of card-punching instructions on so-called card-time diagrams. These card-time diagrams were then translated to cards used as inputs to a digital computer forming the actual test deck. (See APCHE *Compiler* below.)

The special ability of APCHE is to maintain a real-time testing facility. The APCHE test deck causes a stimulus to be applied to the subsystem component being tested and APCHE measures the response, whether it be voltage, current, time, etc.; response is compared to prescribed limits. In this way, the programmed test deck is used to check circuit gains, valve opening and closure time, various calibrations, pitch and roll program sequencing time, etc.

Special Purpose Programming

The Program Skill Center personnel is presently programming a special-purpose airborne computer used to guide and control a missile in a classified application.

SCIENTIFIC AND ENGINEERING PROBLEMS

The Programming Skill Center has authored many scientific and engineering programs in association with the

engineering groups at ACCD. Some of the representative efforts described herein will afford an idea of the range of problems encountered.

Digital Differential Analyzer (DDA) Simulation

The STREAC computer, a breadboard model of a computer for airborne applications, was programmed to simulate a DDA solving navigation problems. A descendant of this computer, the AM3100, has been programmed to carry out a comprehensive self-check of its operation.

Study Programs

Error studies of the derivation of position of an ICBM under observation by two cooperating airborne observers using triangulation techniques.

Radar cross-section study involving the effects of scintillation. This problem involved solving two sets of twelve first-order differential equations relating the angular rates and the direction cosines of body axes of a radar target with respect to earth axes.

Study of the cumulative probability of detecting a moving radar target. Such factors as scan rate, beam angle, range, target cross section, and target velocity are taken into account and varied in order to determine the combination giving the highest probability of detection.

Satellite Rendezvous Program

This program involved a space vehicle flight simulation which determines the maneuvering of a vehicle attempting to rendezvous with a passive orbiting target. The problem statement included approximately 200 equations.

Power Spectral Density Program

This program is used for obtaining the power spectral density of a time series or for obtaining the spectra, co-spectrum, and quadrature spectrum, of two simultaneous time series.

Inertial Navigation Error Program

This program calculates the error vector due to several error sources in an inertial navigation system. Typical error sources are accelerometer bias and scale factor, and gyro drift. The program calculates the *position covariance matrix* due to control errors, and the corresponding *velocity covariance matrices*. The program also calculates the principal axes and orientation of error ellipsoids.

APCHE Compiler

This program involved the analysis and conversion of engineering data in the form of graphs, tables, and card-time diagrams to a binary Remington Rand card deck for use as input data to the RCA-built APCHE. A special card deck was also produced which served as a self-test for the checking equipment.

UTILITY PROGRAMS

Utility type programs handled at the Programming Skill Center provide a set of programming aids and tools used time and again by various programmers. Once implemented, such programs free the programmer to address the execution of the problem at hand. Utility systems have been created for the BMEWS Site III IBM 7090 computers and the Burroughs Datatron 205, both of which have been at ACCD Burlington.

Originally, utility or service routines performed small common housekeeping tasks of the computer installation, such as duplicating and verifying tapes. The scope of service routines has now expanded to include powerful program testing aids, program selection, storing and maintenance procedures, and generalized common production-type runs, such as sorts and merges.

Assembly and compiler routines are specialties of the utility programmers in the Skill Center. Digital computers operate on the basis of combinations of binary digits; it is a great source of difficulty to use these bits to program the machine. The assembler and compiler rountine enables the programmer to use another "language" to arrive at the program.

Generally, mnemonic names have been given to the instructions. However, instruction, in most cases, must refer to an address; sometimes, the address is referred to many times. Rather than use a specific bit combination, the assembly program allows the use of symbols for addresses. The assembly program will take as its input a program written with mnemonic and symbolic notation and produce as its main output a program expressing the binary digit combinations of the machine. The assembly program is also sophisticated enough to perform certain error checks and call to the attention of the programmer gross errors which will prevent the program from operating.

The use of symbols has been extended to the creations of new "languages" for the programmer. These languages may be oriented for classes of problems such as *c*ommon *b*usiness *o*riented *l*anguage (COBOL) or *a*lgetraic *o*riented *l*anguages (ALGOL). These languages contain macro-instructions requiring several machine instructions to accomplish. Compiler programs accept these languages and produce the proper sequence of machine instructions.

SIMULATION

Simulation or mathematical modeling represents a large class of problems handled by the Programming Skill Center. In this area both analog and digital techniques are used where each is of the best advantage.

The analog facility installed in 1955 has been used on many problems. One large-scale simulation included a three-dimensional model of a fighter-bomber intercept problem with a model cockpit and a visual surround. Simulation equipment fed radar and other signals to the instruments in the cockpit and the entire system responded to the pilot's actions. This type of simulation is in real time and requires the fast response of the analog equipment.

Another simulation, presently being implemented is concerned with a missile application involving an orbital rendezvous. This program will take into account the physical situation, the response of the missile, the detailed action of the guidance and control system, and will produce the required signals used in the guidance and control system at the proper simulated time. This simulation will be used as an engineering tool to study the design of the entire missile system being simulated.

In this way parametric studies can be made for large scale systems or those which are not analytic in nature in order to arrive at the optimum parameters for a system subjected to a given range of input and output conditions.

MISCELLANEOUS PROGRAMS

The Programming Skill Center engineers are engaged in many diverse programs too numerous to detail; however a few typical examples are as follows: 1) the management sciences involving analysis of management dynamic control functions through the use of feedback control theory and the analysis of PERT networks for no-links and loop conditions; 2) data reduction programs; 3) human factor studies using a computer as a teaching machines; 4) participation in numerous proposals from the analysis of data processing and computing requirements to the computations involved in determining parameters so necessary for the framework of many proposals; and 5) competitive evaluation studies between various computers for the performance of particular classes of functions.

CONCLUSION

The Programming Skill Center at Burlington provides capability for the implementation of many computer-oriented projects and problems. Services can include the comprehensive analysis and programming of such problems. Members of the Skill Center can contribute at the various levels—from the defining of a problem, through the programming, coding, system integration, and system checkout.

PROGRAMMING INFORMATION SYSTEMS

Information processing is being mechanized to help men to make better decisions. Voluminous information is sifted, analyzed, condensed to manageable proportions, and presented in a variety of ways. Men are able to draw conclusions and to take decisive action on the basis of accurate and timely information. The implementation of such information systems is discussed and the relationship of a program to its environment is explored.

Dr. BURNETT H. SAMS, Ldr.
Programming Systems
Data Systems Center, Bethesda, Maryland

DEVELOPMENT OF AN information system (Fig. 1) is an evolutionary process—their nature is not clearly understood, and there is no theory of information systems to bridge the scattered theoretical and experimental results. The requirements for an information system usually develop in step with the system design. It is perhaps a mistake to speak of *the* system; actually, each application provides a series of systems as requirements, technology, and understanding of the problem mature. The design of information systems is based upon the meager experience to date, analysis of design models, and analogies with data processing. These facts of engineering life presage that a system design will undergo repeated modification before a fully operational system is achieved. While in principal an information system could be realized in hardware, the relative economics of modifying programs as opposed to revamping hardware suggest basing information systems upon computers and computer programs.

This paper concentrates on the *implementation* of such information systems. Published literature[3,4] discusses the design of an information *system* itself. Within RCA, for example (at the Data Systems Center), the ACSI-MATIC Program, under contract with the Department of the Army, Office of the Assistant Chief of Staff for Intelligence is developing a major information system to support certain headquarters operations of the U. S. Army.[5,7,9,11]

COMPUTER SYSTEMS

During the next decade, information systems based on different types of computer systems will evolve.

The first type will be a direct outgrowth of the present general-purpose, stored-program, digital computer. Such a computer system will involve a high-speed random-access memory of 32,000 to 64,000 words and a magnetic-disk or magnetic-card secondary memory of 100 million to 500 million characters.

The principal criterion for overall system performance is the time to acquire information from the secondary memory; thus the secondary memory must permit multiple accesses, and the computer system will need programable input-output units capable of operating in a simultaneous manner.[10] This simultaneous information-transfer capability will be coordinated with internal processing by a program-interrupt subsystem. Internal operations will be geared to the manipulation of strings of bits, and a variety of operations on addresses and index registers will be provided. Users and operators of the information system will be viewed as additional input-output devices linked to the central processor by two-way consoles.[7]

A second type of computer system of interest during the next decade will feature a multiple-processor organization. Each processor may be a somewhat reduced version of the central processor described above, with the work load of the system distributed among the several processors. When inter-memory transfer times are short compared with other input-output transfer times, the processors may specialize in certain aspects of computations or in handling certain files or displays. Otherwise, when interprocessor communication is costly, each processor must control self-contained subsystems with little need for intersystem communication. For example, a system might consist of several independent but coordinated processing, retrieval, and display subsystems.

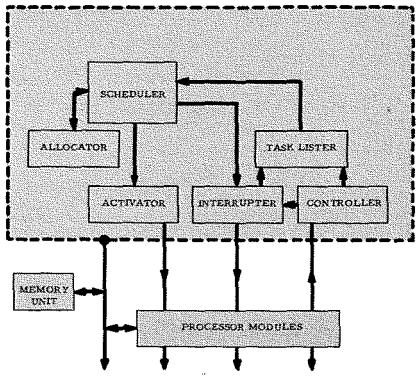
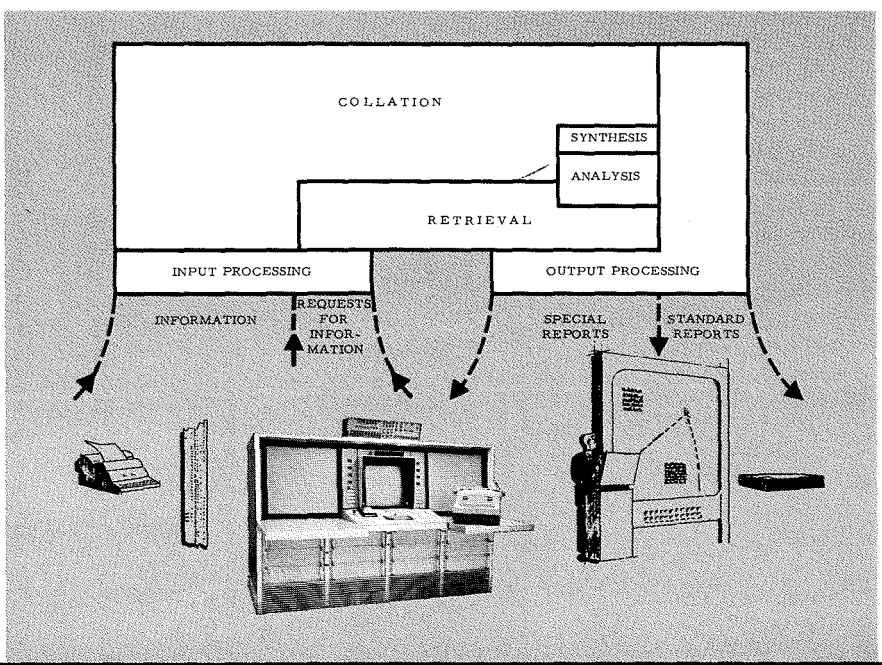


Fig. 2—Representative programming system. The processor modules include computation modules, input-output modules, operator consoles, and analyst consoles. Typical memory units are thin films, core, drum, disc, magnetic cards, and magnetic tape.

COMPUTER PROGRAMS

A computer program is a sequence of instructions to be executed by a computer in performing a stated function. The capability of reusing instruction sequences without regenerating them accounts for much of the power of computers. A program is called upon to perform its function in a stated environment; it is started, receives inputs, produces outputs, and comes to an end. When the function of one program is to receive inputs from a second program, the first program is called a subprogram of the second. A collection of programs organized by the program-subprogram relation is called a program structure.

Fig. 1—Functions of an information system. Inset photo: the prototype analyst console (PAC), which is used on line with an RCA 301 at the Data Systems Center.



The program structure for an information system will be developed as the joint effort of several teams of programmers. Planning must be performed as a continuing function pertaining to the scheduling and coordination of the various tasks.[5] The planning must account for successive stages of program design corresponding refinements of system requirements.

PROGRAMMING

Programming is the intellectual process of creating a program design and the technical process of implementing the design to achieve an operating program. The programmer is always striving to obtain an artful union of a problem and a computer. Programming involves several phases, beginning with system analysis and problem definition, and ranging through the final coding, testing, and—finally—an operational system.

System analysis is the first phase of programming. It organizes the problem in *programming terms*, by comparing computer capabilities and the operational environment to:

1) determine significant and relevant features,
2) reduce the number of design options,
3) determine the portions of the system to automate,
4) arrive at a gross organization of file structure,
5) select appropriate programming techniques.

Problem definition is the next phase of programming; the functions of system inputs and outputs are specified. At this stage, the procedures to be followed by the system in carrying out its functions are expressed in terms arising out of the problem; later, these problem-oriented procedures will be expressed in terms of the programming environment. *The problem definition is the system design outline.* As the design is elaborated and implemented, the system will undergo redefinition.

Program analysis determines a processing flow for the system. Both the flow of data and the flow of programs must be considered. The two extremes of processing flow are *single-input* processing and *batch* processing. Single-input processing occurs when one input is presented to the computer, and programs are brought into the computer to process that single input until the processing cycle is complete. Batch processing occurs when a program is brought into the computer and a number of inputs are processed by the given program, then, a second program is brought into the computer and the inputs are all processed by the second program. This pattern is continued until all inputs have been processed by all programs.

This brief characterization of single-input and batch processing illustrates one aspect of the duality of data and program: i.e., in the one case, many programs are operating on each of a series of inputs, in the other many inputs are operated upon by each of a series of programs. A large program does not generally fall into either of these extreme cases but involves a mixture of the two strategies in performing its various functions. The analysis of the flow of data and programs determines the system's processing capacity.

Early computer designers and programmers recognized the stored-program digital computer's capability of operating upon program as well as data; this was exploited in the sense that a program could modify its own instruction sequence to perform the successive iterations of a computation. With the advent of index registers and indirect addressing, less is gained by such program modification. In fact, allowing programs to modify themselves can be a disadvantage. It is desirable to reuse a program in more than one place in the program structure; it is also desirable to change the location of a program in memory during the course of a computation. These kinds of program design are complicated (or impossible) when programs perform self-modifications. Furthermore, there is the always-present danger that a program will modify another program by mistake, setting up the conditions for an error in some other part of the system. These situations can be alleviated, if not eliminated, by forbidding programs to modify themselves and by building computers which prohibit changes to selected areas of memory and which provide for multiple stages of address modification through indexing and indirect addressing.[6] The capability of a stored-program digital computer to operate on program as well as data is still significant; however, its importance lies in the direction of an executive program (see below) managing a large number of programs and modifying program codes with the parameters of a particular execution.

After determining the processing flow, the problem-oriented procedures are analyzed to arrive at computer algorithms. The program analysis must optimize a set of performance parameters; such parameters include the size of the program, the time required to execute the program, and the time required to construct and test the program.

Coding develops computer algorithms into a program represented as a sequence of statements in a programming language. Much variety is possible in the choice of a programming language: some languages facilitate numerical calculation and manipulation of numerical arrays, others contain effective data-describing features, another may facilitate the allocation and control of program structures, and other languages may provide additional features valuable for specific applications. It is desirable to incorporate several programming languages in the operating system so that programs may be written in the most suitable languages.

DR. BURNETT H. SAMS graduated Magna Cum Laude from the University of Washington in 1951 with a BS in Physics. He received his MS in Mathematics from the University of Illinois in 1953, followed by the Ph.D. in 1958. In 1957 Dr. Sams was a Research Associate at the University of Illinois and in 1958 was a research associate at MIT. He joined RCA-AED in 1959, where he conceived the ACSI-MATIC programming system and designed the first allocatable code assembly program. Dr. Sams later joined the Data Systems Center as Leader, Programming Systems Group, to direct the design and implementation of the ACSI-MATIC programming system. Dr. Sams is a member of the American Mathematical Society, The Association for Computing Machinery, The American Association for the Advancement of Science, Phi Beta Kappa, Sigma Xi, Phi Kappa Phi, Pi Mu Epsilon, and Zeta Mu Tau.

Debugging uncovers and corrects logical faults and typographical errors in a program code. A number of computer programs may assist the programmer to isolate a bug, set up test situations, or correct programs.

Integration is the continued testing of a program with other programs and other aspects of its intended environment. Integration continues with larger and larger program complexes until all subsystems and finally the entire system have been successfully integrated.

Operational testing is the final stage of program testing. The system is placed into limited, controlled operation to observe its performance under actual operating conditions.

Program operation is the final phase of programming with the program placed in full operation. This is a follow-up period in which some remaining bugs may be corrected and the program modified or extended to satisfy changed requirements.

These phases of the programming process should not be viewed as separate

activities, but as overlapping shifts of emphasis as programming progresses from broadly specified requirements to an operational system. The phasing of a system development, on the other hand, might proceed along quite different lines; parts of a system may be placed into operation before system analysis is completed on other parts.

PROGRAM MANAGEMENT

Computer programs of great size and complexity have been developed to automate information systems. The design, construction, debugging, maintenance, and operation of these programs are tasks of major proportions. Some aspects of these tasks have become systematized to the point that computers have acquired the derived function of assisting programmers in performing these tasks. The programs developed to automate an information system have themselves become the material handled by a *programming system*. The purpose of an information system is to perform stated functions; programs for carrying out these functions are called *production programs*. Auxiliary or *utility programs* facilitate working with production programs. A *programming system* is an integrated set of utility programs.[1,8,12]

The phrase "computer programs of great size and complexity" was introduced to describe the following situation: Many programs are involved. The succession of programs to perform a given computation is determined by the course of the computation on the information being processed. A program may compute the identification, as well as the inputs, of a successor program; thus program organization is a function of the information processed. The memory requirements of the programs are so severe that only a few pieces of the programs can coexist in the computer's memory. As the computation proceeds, some program pieces are replaced by others. The portion of computer memory needed by each program in order to maintain a given processing efficiency is a function of the program organization and the information processed.

The proportion of input-output transmission devoted to program as opposed to data is higher than one encounters in the standard data-processing applications. In the absence of statistics on the operation of information systems, such a comparison is at best an informed guess; however, the ratio of program transmission to total input-output transmission depends upon the designs of the program and hardware systems. Representative ratios of program transmission with state-of-the-art equipments might have orders of magnitude 0.1 for information systems and 0.001 for other data-processing applications, e.g., payroll. The processing capacity of an information system is relatively insensitive to small changes in the size of main memory while the ratio of program transmission is greatly affected by changes in memory size. On the other hand the processing capacity of an information system is roughly proportional to the random-accessing rate of secondary memory; this rate has little effect on the ratio of program transmission. Thus, the management of program flow is an important consideration in designing an information system.

The designers must provide effective means for revising the system. As the system evolves or as user requirements change, the system will undergo a series of revisions. It is most economical to effect a revision as the collective modification of individual programs. When a program is modified, it is necessary to effect the modification with a minimum of disturbance to the system and to other programs. It is mandatory that programs be individually compiled. Programs are placed in an automated file from which they are called into use by an executive program. In order to make meaningful modifications to a single program, there must be conventions for distinguishing between 1) those matters which are internal to a program (treated as private affairs of that program) and 2) matters external to a program, perhaps common to a set of programs or the entire system. These latter must be handled in prescribed ways. There must be standard ways for having the executive program call programs into use. As processing becomes involved, the executive program becomes more deeply enmeshed in the processing, and programs must adhere to more and more conventions. Some of the work of following conventions may be passed off onto the programming language or absorbed within its translator.

A programming language, translator, program file, and executive program are obvious components of a programming system. In addition there must be programs to maintain files recorded in variants of some standard format or any of a number of specialized formats. These file maintenance programs must provide for both the copying of files from one medium to another and the revising or merging of files. The executive program must provide facilities to:

1) prepare the computer system for each program execution,
2) provide for the inputs and outputs of each program,
3) recover from system errors,
4) provide diagnostic information during execution,
5) handle program-subprogram relationships.

EXECUTIVE PROGRAM

The executive program interprets and carries out requests for performance of utility programs; it coordinates the use of the various programs, schedules their execution, and enables recovery from system failures.

The executive program must maintain a record of the facilities assigned to each program. These records enable the saving and restoration of memory to take place automatically as one program is interrupted to allow another to proceed. A call on the executive program will effect a transfer of control to a utility program; a subsequent call will correspondingly return control to the calling program. When the next program is ready in the main memory for execution, a direct transfer of control suffices; however, if the next program is not ready there are then two cases: 1) a previously used program which in whole or in part has been removed to secondary storage must have its parts returned to main memory, or 2) a new program must have its parameters replaced by values as it is moved into its assigned facilities. There are utility programs to select production programs from a program file, to load programs into memory, and to effect data and control transfers.

Ordinarily, the execution of programs is scheduled in the order that requests are received by the executive program. However, a program cannot be executed unless all programs which must precede it have been completed, all programs of higher priority are underway, and all program parts are in place ready for the execution. The order of execution cannot be exactly predicted when the programming system is a multiprogramming system.[2] As noted above, computer systems permit data transmission to be conducted simultaneously with program execution. Accordingly, data for one or more programs may be flowing into the main memory while computation is proceeding with another program and while perhaps another program is waiting for an operator to mount a magnetic tape or respond to a request for information.

The monitoring function of an executive program provides for logging program executions, manual interventions, production of outputs, and other significant events. As an aid to program debugging and integration, monitoring may include the logging of all calls upon a program and the performing of selected debugging functions. Monitoring options are selected by requests to the

executive program; and may include the dynamic insertion or removal of program interruption points to enable monitoring at points other than those originally selected. Due to the size of the programs under consideration, it is not appropriate to allow the action of each computer instruction to be monitored.

PROGRAM STRUCTURE

There is an initial requirement for an executive program to interpret transfers between programs to insure that the program transferred to is in memory. In general, successive programs will have considerable overlap of common code, data, and working areas. The definition of *program* must therefore encompass portions of independently developed programs. Furthermore, it is often desirable to allow work areas to be assigned to programs as requirements arise during execution.

An example will suggest the richness of program structure applicable to information systems. An information system exists to perform stated tasks. Corresponding to each task is a body of computer code called a *process*. A task is performed by executing the corresponding process. In general, a process is too large a body of code to be developed or executed as a single unit. Programming analysis is conducted to structure the task as a complex of simpler functions. A *block* is a body of code which can be placed in the memory of the computer system and executed to perform a given function. A closely related set of blocks which are developed as a unit is a *program*. A process is developed as an integrated collection of programs; a given program may belong to more than one process.

A program execution occupies an interval in space-time. The spatial entities are memory sequences, input files, output files, such entities borrowed at execution time from programs already in use, and other programs which this program might call into use. Each entity may be further partitioned to take advantage of hardware configurations. For instance, a memory sequence may be partitioned to take advantage of noncontiguous memory locations; likewise, a magnetic-tape file may be partitioned into reels by physical necessity or to permit faster accessing.

Time, due to multiprogramming, has a multivalued nature. At any given moment of computer-time, calculation or data transmission is proceeding in one or more program blocks. As the execution progresses from block to block, some spatial entities drop out of use and others come into use. Computer time is thus punctuated by control signals to form a series of time intervals. The control signals may either announce the completion of an activity (e.g., computation, data transmission) or request the initiation of an activity (e.g., error analysis, monitoring, data transmission, operator communication, processing). The control signals are recognized by a marriage of hardware and software (Fig. 2) to interrupt the processing of some blocks, resume the processing of other blocks, or to initiate the processing of additional blocks.

ALLOCATION

There has been no intended implication as to how or when spatial entities are assigned to hardware facilities. The above remarks apply equally to applications having all assignments made by the programmer or compiler, and applications having some or all assignments postponed to the time of loading or the time at which assignments are required by the computation. Storage allocation effort may be distributed between the programmer and a programming system by using a programming language capable of expressing the space-time requirements of programs. The task of storage allocation may be divided into work done by the programmer while planning and coding, work done by a translator or operator system prior to the start of a "machine run," and work done during a machine run (either performed by the computation or performed by the executive program).

The term *dynamic storage allocation* applies to those cases in which: 1) the code presented to the computer at run time is not directly executable by the computer but requires a number of parameters to be set, 2) it is not necessarily known which parts of the code will coexist in high speed memory at each step of the computation, and 3) it is not known where in memory a given part of the code will be held when it is used (executed as instructions or referenced as data).

Dynamic storage allocation implies that the computation is interrupted from time to time to assign code to storage elements, to set allocation parameters, to save code which may be used later but occupies space allocated now to a different use, to load new code, and to restore previously saved old code. The allocation of storage for a code depends upon the state of the machine at the moment the code is loaded. The state of the machine includes such factors as available high speed memory, relative priorities or programs now occupying space, and the disposition of peripheral devices. Dynamic storage allocation does not preclude or eliminate planning; rather, the option of postponing part of allocation until computation time is added to planning. The objective of these considerations is to minimize a total programming cost involving the interrelated factors of planning, coding, debugging, computer storage, computation time, and operational requirements.

CONCLUSION

Many problems arise in developing information systems. Some are organizational problems requiring the introduction of programming and operating conventions to facilitate interprogram compatibility, to increase debugging efficiency, and to reduce the operational procedures to a manageable number. Other basic programming problems require general solutions applicable to all parts of the system or solutions applicable to a program as a whole. The programming must allow the piecing together of parts produced by different people or at different times. Furthermore, the parts must be capable of individual modification for both initial development and subsequent change as system requirements evolve.

A programming system provides a context in which these problems can be expressed, a framework for representing solutions, and a favorable environment for developing and operating programs.

BIBLIOGRAPHY

1. T. E. Cheatham, Jr., G. O. Collins, Jr., and G. F. Leonard, "CL-1, An Environment for a Compiler," *Communications of the Association for Computing Machinery 4*, January 1961, pp. 23-28.
2. E. F. Codd, "Multiprogram Scheduling," *Communications of the Association for Computing Machinery 3*, June-July 1960, pp. 347-50; 413-18.
3. R. A. Colilla and B. H. Sams, "Information Structures for Processing and Retrieving," *Communications of the Association for Computing Machinery 5*, January 1962, pp. 11-16.
4. H. Gurk and J. Minker, "The Design and Simulation of an Information Processing System," *Journal of the Association for Computing Machinery 8*, April 1961, pp. 260-70.
5. T. A. Holdiman, "Management Techniques for Real Time Computer Programming," *Journal of the Association for Computing Machinery 9*, July 1962, pp. 387-404.
6. K. Kozarsky and A. T. Ling, "The RCA 601: Speed and Flexibility in a Large-Scale System," RCA ENGINEER 7, Aug.-Sept. 1961, pp. 42-45.
7. P. B. Lazovick, A. W. Reickord and J. C. Trost, "A Versatile Man-Computer Communication Console for Information Processing Systems," RCA ENGINEER, Vol. 7, No. 5, Feb.-March 1962, pp. 50-53.
8. G. H. Mealy, "Programming Systems, Whither?" *Communications of the Association for Computing Machinery 5*, July 1962, pp. 374-75.
9. L. Miller, J. Minker, W. G. Reed and W. E. Shindle, "A Multi-Level File Structure for Information Processing," *Proceedings of the Western Joint Computer Conference*, 1960, pp. 53-60.
10. J. Minker, "Implementation of Large Information Retrieval Problems", Gordon Research Conference, New Hampton School, New Hampton, N. H., July 1961, 9 pp.
11. B. H. Sams, "Dynamic Storage Allocation for an Information Retrieval System," *Communications of the Association for Computing Machinery 4*, Oct. 1961, pp. 431-35.
12. B. H. Sams, "Some Observations on the Development of Large Programs," First Congress on the Information Sciences, Hot Springs, Va., Nov. 1962, 28 pp.

RENSEC: LOGICAL DESIGN FOR A RESIDUE-NUMBER-SYSTEM DIGITAL COMPUTER

RENSEC is a design for a digital computer that makes use of a unique coding scheme—the residue number system. The most attractive feature of RENSEC is elimination of the carry circuitry generally found in computers using binary arithmetic. The computer can perform basic arithmetic operations, data transfers, and comparisons necessary for computation. Arithmetic operations are performed with wired-in instructions (magnetic-core planes) in less than 3 μsec—except for division which, along with input-output conversion, is done with stored subroutines. General-purpose computation presents problems in overflow for which techniques have been developed that involve programming RENSEC to evaluate computed quantities; however, if every quantity must be so evaluated, computation speed is lost. Thus, the RENSEC approach may be most attractive for applications where the range of variables is reasonably well controlled.

$N = K \cdot 3 + R$	R	R *mod 3*	R *mod 4*
0	0 0	0	0
1	0 1	1	1
2	0 2	2	2
3	1 0	0	3
4	1 1	1	0
5	1 2	2	1
6	2 0	0	2
7	2 1	1	3
8	..	2	0
9	..	0	1
10	..	1	2
11	..	2	3
12	..	0	0
		etc.	

Fig. 1—Left portion: calculation of residue code for R *mod 3* from Equations 1 and 2. Right column: residue code for R *mod 4*.

MOD 3 ARITHMETIC TABLE

x \ y	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

SUM

x \ y	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

PRODUCT

x \ y	0	1	2
0	0	2	1
1	1	0	2
2	2	1	0

DIFFERENCE (x−y)

Fig. 2—Tables illustrating the addition, subtraction and multiplication rules for moduli 3 and 4.

E. C. DAY* and R. A. BAUGH*
Missile and Surface Radar Division
DEP, Moorestown, N. J.

FROM THE least-positive residues of several relatively prime number bases, a code can be formed representing uniquely all numerical values falling within the limits determined by the number bases used. This numerical code is referred to as the *residue number system* (RNS).[1] To explain the development of the residue code, consider the equation:

$$N = KM + R \qquad (1)$$

Where: N, K, M, and R are integers, and $M > 0$. If N is a decimal value and M is the number base, then K is a multiplying constant and R is a remainder. For instance, if 14 (decimal) is expressed in terms of base 3, then Equation 1 states that $14 = (4 \times 3) + 2$. Equation 1 may also be expressed in a congruence relationship:

$$N = R \; Mod \; M. \qquad (2)$$

Equation 2 states that N is congruent to R *modulo* M. The multiplying constant K of Equation 1 is eliminated. Equations 1 and 2 are illustrated in Fig. 1 where N represents decimal values and $M = 3$. Also shown in Fig. 1 are the residue codes for R *mod 3* and R *mod 4*.

The multiplying constant K in Equation 1 represents the carries required to represent the numerical value N *modulo* M. The residue code is derived by using the congruence relationship in Equation 2 and retaining the least positive residue with respect to several moduli. By *least positive residue* it is meant that $0 \leq R < M$.

There is an isomorphic relationship between the residue code and the number N when $0 \leq N < M$ (where M is the product of the moduli) provided the moduli are relatively prime. Using *moduli 3* and *4*, the residue code has a range of decimal values 0 through 11. If the moduli are not relatively prime, the range is reduced to the product of the relatively prime factors. For example, using *moduli 4* and *6*, the range is equal to 4×3, because 2 is common factor in each modulus.

ARITHMETIC OPERATIONS

Tables illustrating the rules for addition, subtraction, and multiplication using *moduli 3* and *4* are given in Fig. 2. Rules for these operations are identical with those for the decimal number system, except that all carries have been eliminated between the different moduli. To illustrate the arithmetic operations using the residue code for *moduli 3* and *4*, consider the following examples.

Addition:

	mod 3	*mod 4*
$x = 2$	2	2
$y = 3$	0	3
sum $= 5$	2	1

This example illustrates that the arithmetic operations are performed independently on residues of each modulus. When 3 and 2 are added *modulo 4*, the result is 1 with no carry. The residue code for the *sum* (2, 1) is equivalent to the decimal value 5.

* The authors performed this work while assigned to the DEP Aerospace Communications and Controls Division.

Subtraction:

	mod 3	*mod 4*
$x = 10$	1	2
$y = 7$	1	3
difference $= 3$	0	3

Note that in subtracting 3 from 2, *modulo 4*, the result is -1. The addition of a multiple of 4 corrects this to the least positive residue, which is 3.

Subtraction can also be performed by complementing the subtrahend and adding the two operands. The complement may be obtained in the residue number system by subtracting the residue code from zero. In other words, each residue is complemented independently with respect to its own modulus. This method of subtraction is illustrated below using the operands in the previous example.

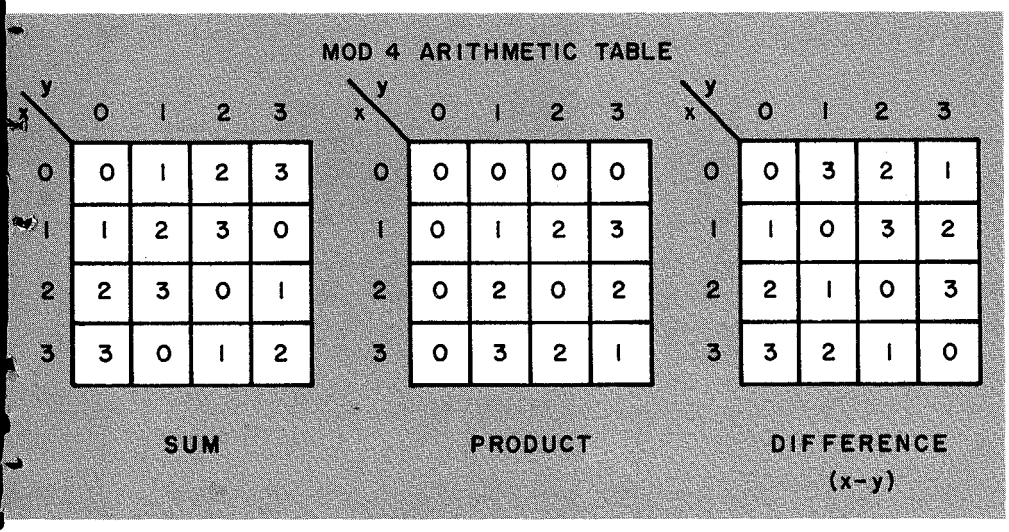
Subtraction:

	mod 3	*mod 4*
$x = 10$	1	2
$y = +(-7)$	+2	+1
difference $= 3$	0	3

veloped for sequentially accomplishing division. This algorithm accomplishes division similar to the methods used in conventional binary computers by successively subtracting and comparing the numerator and denominator.

Since carries do not exist in addition, subtraction, and multiplication, these operations may be easily implemented with the use of magnetic core planes. Fig. 3 illustrates the wiring diagram for a magnetic core plane to accomplish *mod 4* additions. A sensing wire is placed through all cores having a common sum. Thus, four sense wires are required to obtain all the *mod 4* residues 0, 1, 2, and 3.

The operations of multiplication and subtraction may be accomplished in a similar manner by properly wiring a magnetic core plane as defined by the arithmetic tables in Fig. 2.



The residue code (2, 1) is the complement of [1, 3 (+7)] since (0-1) *mod 3* $= 2$ and (0-3) *mod 4* $= 1$.

Multiplication:

	mod 3	*mod 4*
$x = 2$	2	2
$y = 3$	0	3
Product $= 6$	0	2

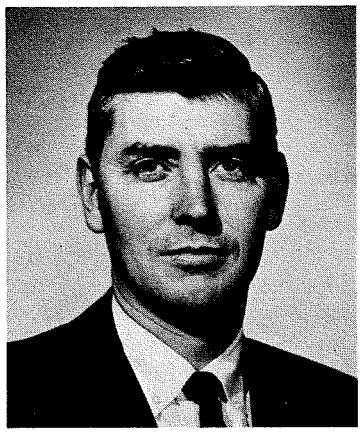
By examining the *mod 4* multiplication table, one finds that 3 times 2 gives a product of 2; likewise, from the *mod 3* table, 0 times 2 gives 0. Therefore, the residue code (0, 2) represents the decimal product of 3 times 2, or 6. This example illustrates the elimination of carries between moduli, since each residue of the product is determined from the two residues of the corresponding modulus.

Fig. 2 does not contain tables for division because this operation cannot be accomplished in a straightforward manner[2]; however, an algorithm has been de-

COMPUTER DESIGN AND ORGANIZATION

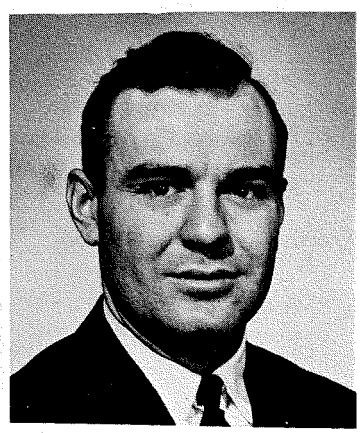
The number range of the residue code depends upon two factors—the size and quantity of moduli. The major consideration when determining size of the moduli is the requirement that each residue must be stored in the computer memory in binary code. Thus, the moduli are selected so they are relatively prime and near a power of 2. Whether the moduli are near 16, 32, 64, or 128 depends upon the techniques used in implementing the arithmetic operations and the desired range.

The quantity of moduli is of particular importance because more hardware is required for an arithmetic unit using three moduli near 64 than one using four moduli near 32. The moduli selected for use in RENSEC (29, 31, and 32) provide a range of $\pm 14{,}384$. The computer word length of 17 bits include 5 bits for each



ELMER C. DAY received an AB from Western Kentucky State College in 1953 and a MS in Applied Mathematics from Harvard University in 1955. For the next five years he worked for the U.S.A.F. on several research projects including a random access card memory, 3-D displays, and an automated Air Force base supply accounting system. Since joining RCA in 1960, he has participated in several study programs for the development of automatic test equipment. Mr. Day is presently assigned to the Information Data Processing Group of BMEWS Systems Engineering at Moorestown Missile and Surface Radar Division. He is a member of the Association for Computing Machinery and the IEEE Professional Group for Electronic Computers.

RICHARD A. BAUGH received a BSEE from Virginia Military Institute in 1955 and his MSEE from Drexel Institute of Technology in 1962. Prior to joining RCA in 1958, Mr. Baugh served as a communications and radar officer with the U.S.A.F. Since joining RCA, he has participated in design and systems engineering on projects in the fields of digital communications, system support, and digital computation. His recent work has been concerned with the development of system support concepts and the application of the residue number system to computer technology. During this period, he has completed studies to determine the requirements and use of digital computers for automatic testing in underwater and advanced space vehicles. In addition, he has participated in studies which led to the development of practical sign determination and conversion techniques for the residue number system. Mr. Baugh is currently assigned to Information Processing Systems, BMEWS Program, M&SR, as a systems engineer.



residue and two bits for sign and parity.

Fig. 4 illustrates the organization of RENSEC, which consists of the following subsystems: memory, arithmetic unit, input-output, and control.

The computer uses synchronous logic and accomplishes each instruction in approximately 10 μsec. The computer operates from an internally stored program using single-address instructions. The operation time of 10 μsec per instruction includes 5 μsec for instruction access, 2 μsec for obtaining the operand from memory, and 3 μsec for executing the operation. Each instruction includes 9 bits for memory address and 6 bits for the operation code. The instruction repertoire consists of 27 commands including the arithmetic operations of addition, subtraction, and multiplication; the conventional transfer of data commands; conditional transfer of control; and some special commands that are peculiar to RENSEC for using the residue code. Stored subroutines are used for division and input-output conversion.

The program is written in octal code and punched into paper tape using a Flexowriter. The Flexowriter tape reader is used to transfer the program to the input buffer where the parity bit is added to the word. The computer is programmed to transfer the instruction words from the input buffer to the proper storage locations.

Program data are punched into paper tape in decimal code and input to the computer using the Flexowriter reader. A stored subroutine is used to convert the program data from binary-coded decimal to binary-coded residue. Similarly, for data output, a stored subroutine is used for conversion from binary-coded residue to binary-coded decimal.

The arithmetic operation of division is accomplished with a stored subroutine that contains 97 instructions. The time required for division is approximately 2 msec. The operation of division could be wired-in as a program instruction and the operation time reduced to approximately 200 μsec.

MEMORY

Since the problems solved on the computer will be used primarily to demonstrate the computational speeds and techniques of the residue number system, the capacity of the computer memory can be relatively small. A magnetic-core memory is used that has a capacity of 256 words of 17 bits each which includes five bits for each of the three residues plus two bits for sign and parity. In addition to the 256-word core memory, the computer has four flip-flop registers that are used for temporary storage of data words for the arithmetic unit.

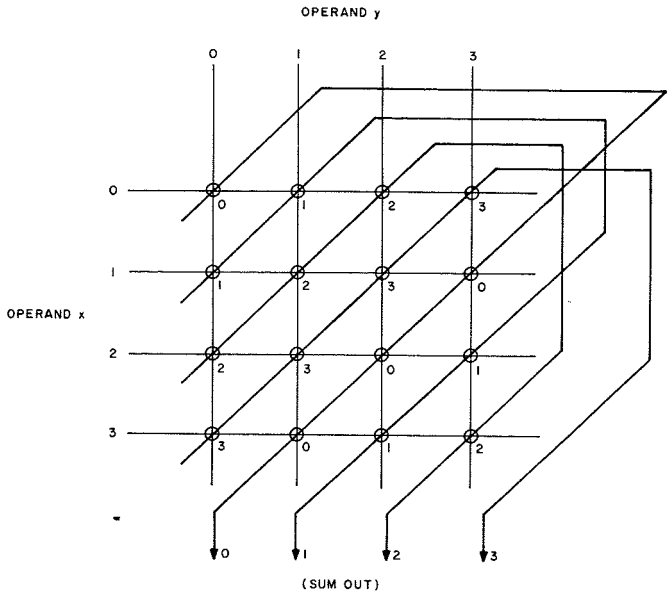


Fig. 3—Wiring diagram of the magnetic core plane to perform modulo 4 additions.

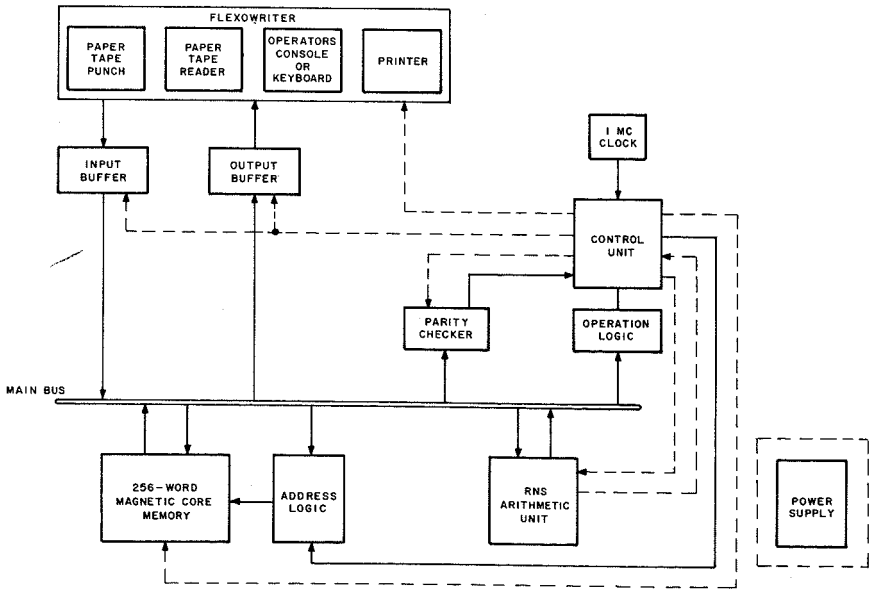
ARITHMETIC UNIT

The arithmetic unit shown in Fig. 5 performs the operations of addition, subtraction, multiplication, and sign determination. The arithmetic unit consists of four registers, three magnetic-core translators, and control gates to route the operands to the appropriate locations within the arithmetic unit. The four registers are identified in Fig. 5 as A_1, A_2, A_3, and A_4. Each of these registers consists of three smaller registers (X, Y, and Z) used to store the three residues representing the operands. For example, register A_1 consists of registers X_1, Y_1 and Z_1, where the X register normally contains the residue *modulo 29*, the Y register contains the residue *modulo 31* and the Z register contains the residue *modulo 32*.

The two operands for an arithmetic operation are stored in registers A_1 and A_2. The results of the arithmetic operation are obtained in register A_3. The A_4 register is used only for temporary storage.

The arithmetic unit performs the computations in parallel. The residue in register X_1 is added, subtracted, or multiplied by the quantity in register X_2 using the M_1 translator. Simultaneously,

Fig. 4—The Residue Number System (RNS) computer block diagram; solid lines indicate data flow, and broken lines shown control signal.



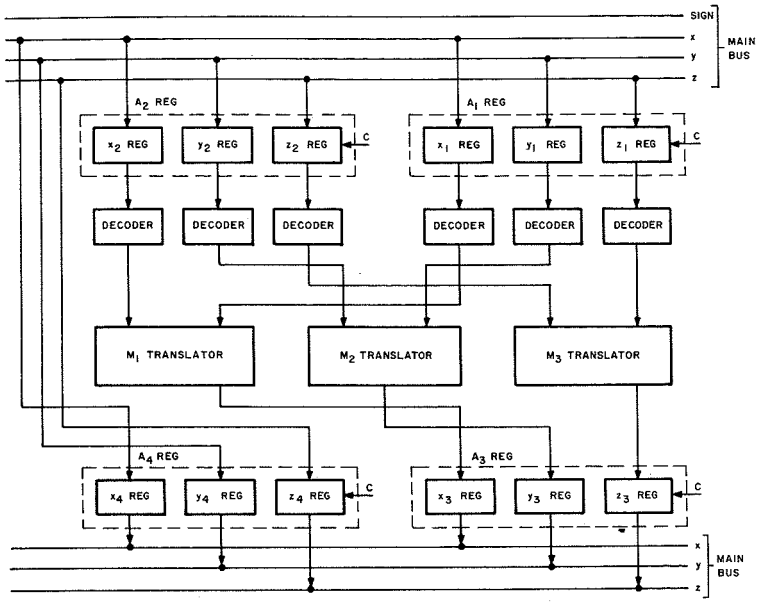


Fig. 5—The RNS arithmetic unit.

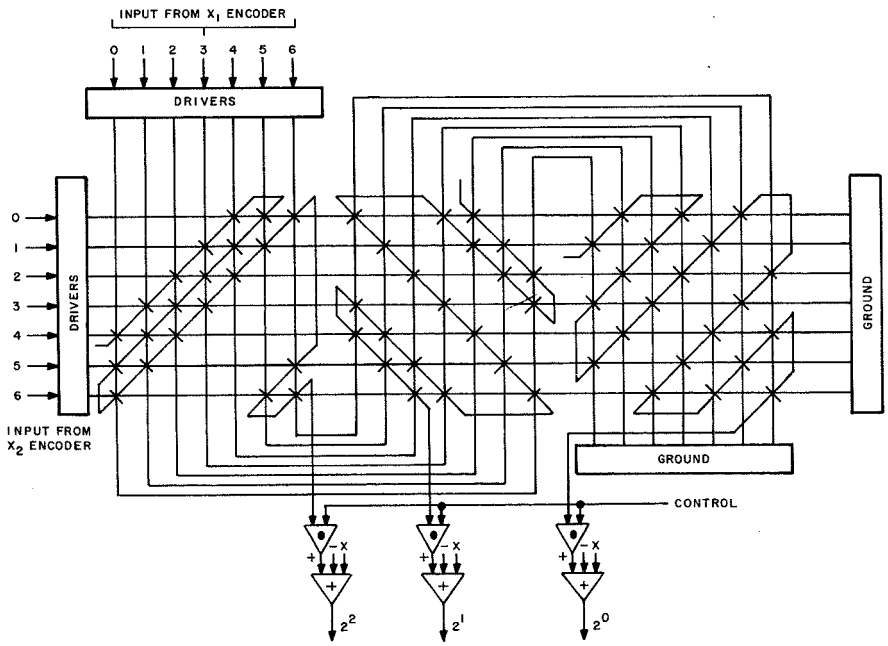
the quantities in registers Y_1 and Y_2 are operated on by M_2 translator; and Z_1 and Z_2 are operated on by the M_3 translator. The arithmetic operations are accomplished with the use of magnetic cores as a switching operation in each of the translators, M_1, M_2, and M_3. Fig. 6 illustrates the wiring diagram for the sensing wires through the magnetic cores to accomplish addition *modulo* 7. For example, if two residues $X_1 = 4$, and $X_2 = 2$ are added *modulo* 7, a sum of 6 or 110 (binary coded residue) is obtained by sensing the position of coincidence. Similar sensing wires are placed through the magnetic cores of each translator M_1, M_2, and M_3 to provide the sum, product and difference.

From the previous discussion it becomes apparent that the RNS arithmetic unit is similar to three small memories operating in parallel. The major difference between a conventional magnetic-core memory and the RNS arithmetic unit is the manner in which the sensing wires are placed through each magnetic core plane.

INPUT-OUTPUT

The input-output facilities of RENSEC have two modes of operation, the transfer of computer instructions and the transfer of program data. The computer instructions are input in octal code and automatically converted to binary code for storage in the computer memory. The program data are input-output in decimal code with stored subroutines for conversion between decimal and residue codes. The subroutine for decimal to RNS conversion contains 15 program instructions and requires approximately 663 μsec for a conversion operation. The subroutines for conversion from RNS to decimal contains 25 program instructions and requires approximately 2.4 msec per conversion. These operations could be wired-in and accomplished at much higher speeds. For example, in RENSEC, the input conversion would require 50 μsec, and the output conversion 280 μsec.

Fig. 6—Modulo 7 translator for addition.



CONTROL

The control unit for RENSEC is similar to those used in conventional digital computers, except the duration of control signals is shortened. The control signals in binary computers become a long sequence for operations such as multiplication and division because many steps are required to obtain the results. By comparison, most of the operations for RENSEC can be accomplished in two machine cycles.

CONCLUSIONS

This paper has described a digital computer (RENSEC) that utilizes the residue number system (RNS) for digital computation. The computer is designed to accomplish the basic arithmetic operations, data transfers, and comparisons necessary for computations. These operations are accomplished as wired-in instructions with the exception of division and input-output conversion which are accomplished with stored subroutines.

The residue number system may be attractive for computers used in applications where the range of variables is well controlled. General purpose computation presents problems in overflow. Techniques have been developed for detecting overflow which require programming the computer to evaluate the computed quantities; however, if every computed quantity must be evaluated for overflow, the speed of computation is lost.

BIBLIOGRAPHY

1. Aiken, H., and Semon, W., *Advanced Digital Logic*, WADC-TR-59-472, July 1959.
2. Garner, H. L., "The Residue Number System," *Proc. of the Western Joint Computer Conf.*, March 3-5, 1959.
3. Cheney, P. W., "A Digital Correlator Based on the Residue Number System," *IRE Transactions on Electronic Computers*, March 1961.

COMPUTER MONITORING AND CONTROL OF COMMUNICATION NETWORKS

The long-haul communications network is the backbone of military communications. It provides the coordination necessary for global military operations and logistic support. For maximum network effectiveness, a central monitoring and control function is necessary. System studies described in this paper have shown that automatic data processing is applicable to network monitoring and control, and provides rapid and efficient network reaction to natural and man-made disturbances.

D. I. CAPLAN, Mgr.
Switching Systems Engineering
Communications Systems Division, DEP, Camden, N. J.

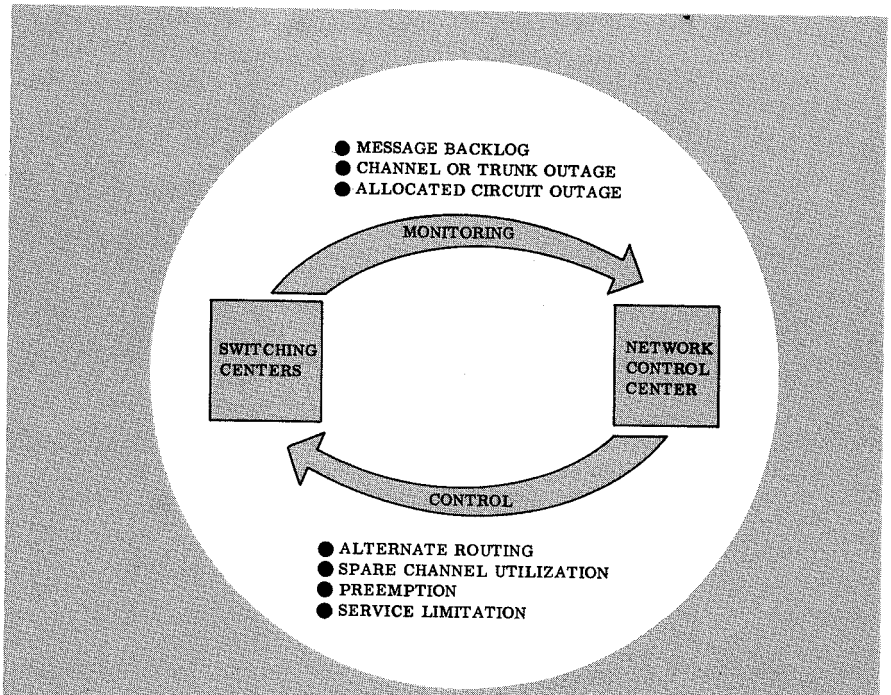


Fig. 1—Feedback concept network monitoring and control.

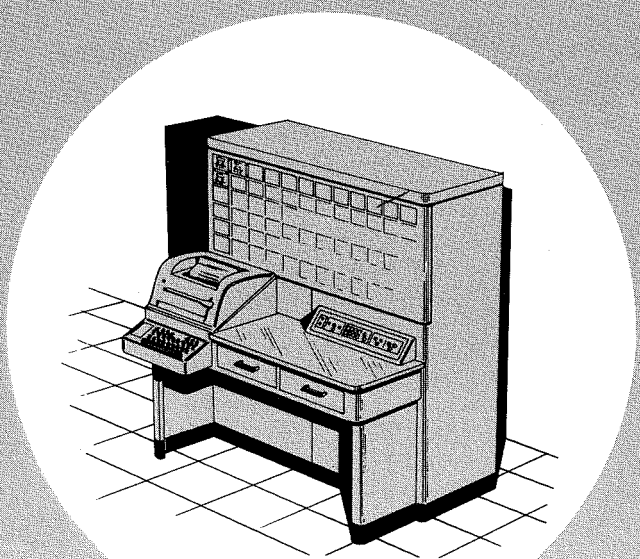


Fig. 2—Typical station status message composer.

THE BASIC ELEMENTS of the long-haul communication network are the switching centers, the trunks connecting them, and the subscribers. Three types of service are provided to the user of the long-haul network:

1) *Direct.* A direct connection is made on demand between two subscribers, and broken down when the call is completed.
2) *Store and Forward.* A message is transferred through the network. It is stored at each switching center, and then passed along to the next center until it reaches its destination.
3) *Allocated Service.* Allocated service is a direct subscriber-to-subscriber connection which remains in effect full time. This "hot-line" service differs from direct service in that the connection is not broken down at the end of a call.

The long-haul network must provide service in the face of many operational difficulties. These difficulties include wide variations in the traffic load and "outages" of equipment due to acts of nature or enemy action. The hot-line service must be restored immediately when any of the hot-line channels are affected by outages. To complicate the situation, peak traffic loads will usually occur at the very time outages are caused by enemy action or severe storms.

There are basically four actions which can be taken to alleviate operating difficulties:

1) *Alternate Routes.* Backed up store-and-forward traffic can be sent via other routes. Direct calls can also be handled over routes other than the preferred route.
2) *Spare Channels.* Spare channels can be put into service, either to replace down channels or to add transmission capacity.
3) *Preemption.* Circuits or facilities can be reassigned from low priority users to high priority users.
4) *Service Limitations.* Maximum message length or call time can be specified, service can be denied to certain classes of subscribers, or other limitations can be placed on the subscribers.

The actions listed above can be taken on a local or global level. Local action will be taken at an individual switching center, while regional or global action will require cooperative performance at a number of switching centers. Obviously the effectiveness of regional or global measures depends on coordination of the switching centers, which must be achieved through central control.

Based on analysis of the problems involved, a system study of the control center functions and possible implementation has been performed. Automatic data processing was found to be applicable both at the switching centers and at the control center. The results of the system study, described in this paper, are applicable to many long-haul systems, and provide an insight into the network control complex of the future.

NETWORK MONITORING AND CONTROL CONCEPT

To provide effective network reaction to varying traffic loads and equipment outages, a closed-loop network monitoring and control system is necessary. As shown in Fig. 1, the status of the network is monitored at the switching centers and transferred back to the network control center. Network operation is analyzed at the control center and control actions are initiated there. These control actions are carried out through command messages sent to the switching centers.

Like any closed-loop system, the monitoring and control system can be made ineffective by delay or by inaccuracy caused by data errors. To reduce these two problems to a minimum, automatic data processing should be used at the switching centers for composition of the status messages and at the control center for network status analysis and display.

Communication between the switching centers and the network control center can be accomplished in several ways. *First,* allocated channels could be provided between the switching centers and the network control centers. *Second,* direct or store-and-forward communications can be initiated either periodically on a preassigned schedule or when required. In order to achieve effective use of communication facilities, a common practice is to use store-and-forward messages for both monitoring and control information, with direct calls used only under emergency conditions. In the case of status messages which are usually long and which contain routine information for the most part, a preassigned schedule of reports is used. Generally, an hourly report is frequent enough for satisfactory reaction time. Emergency reports can be entered at any time.

STATUS MESSAGE COMPOSITION

The simplest approach to station status monitoring is manual. The technical controller at the station records the message backlogs, channel outages, and other pertinent data. He then composes a teletype status message which he sends to the network control center.

From the network control center viewpoint, the manually prepared status messages are a special problem. Because of human error, mistakes in format are common. Messages having incorrect formats will be rejected at an automated network control center, and manual intervention and correction will be required. An automated status message composed at the switching center is therefore desirable.

Data ordering is another problem in manually prepared status messages. Each event at the station, such as a channel outage or restoration, has a time of occurrence which must form a part of the status messages. These events are usually recorded by the station personnel in order of occurrence. However, the status message format will normally require grouping by channel or trunk, so the events must be sorted into a prescribed sequence before they are transmitted. This opertaion is time consuming and subject to error when performed manually.

The *Status Message Composer* concept (Figs. 2, 3) was developed to provide automatic status-message generation from manual inputs. The display and entry panel at the top of the Status Message Composer provides the means for manual entry of trunk or channel outages. Each of the small display and entry modules corresponds to a single trunk or channel. The color of the display module indicates the last inserted status, and serves as a station status display.

The operator types variable data, such as reason for outage, into the keyboard on the left of the Status Message Composer. The panel on the right of the keyboard indicates to the operator what information is required, and provides overall controls such as unit power.

As shown in Fig. 3, the operator-entered information is stored in a core memory. The time of data entry is read into the core memory automatically from a real-time clock. The location of the stored information is predetermined, so that all information about a particular trunk or channel always goes into the same group of words in the memory. Therefore, the status data are always stored in the proper sequence, and will be properly grouped when read out of the memory.

The initial setup of the core memory is performed by reading in a punched paper tape which designates the core locations to be used for each trunk, channel, etc. The paper tape also designates the display and entry module corresponding to each trunk or channel. Changes in station trunks or channels can be accommodated by simply changing the paper tape and relabeling one or more display and entry modules.

A status report can be generated either periodically under clock control or at any time under manual control. The report is generated by a memory read-out which transfers all stored status data to both the paper tape punch and the page printer. The punched paper tape is entered into the communications network for store-and-forward transmission to the network control center. The copy produced by the page printer becomes the station operating log.

NETWORK CONTROL CENTER FUNCTIONS

The functions performed at the network control center can be handled manually or automatically. (The next section describes an automatic implementation of the network control center.)

The network control center operation is shown in the information flow diagram of Fig. 4. Status messages from the switching centers are received at the network control center and recorded, either manually or automatically. The information in the incoming messages is checked for errors, using whatever redundancy is available in the messages (i.e. parity bits or format). The status data are then recorded in the control center file.

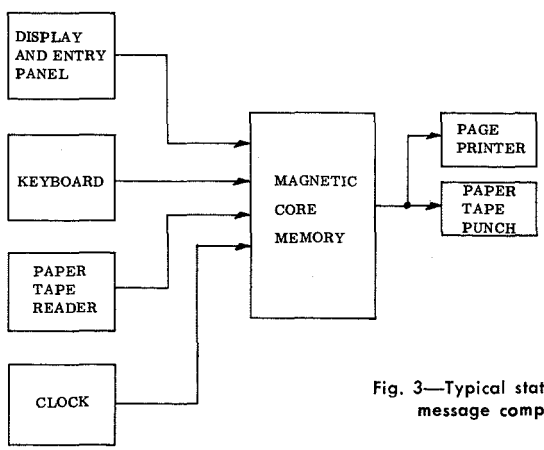


Fig. 3—Typical station status message composer.

The status information is summarized for display to the network controller. It is important that the degree of summarization be optimized: Too much detail will swamp the controller; too little will limit his understanding of network status. Also, new information must be flagged in some way to attract the controller's attention and indicate the need for action on his part. The controller will acknowledge recognition of the new information by resetting the flag.

Using the data provided by the display, the controller is able to solve most network problems. On occasion, however, he may need additional detailed data. Any information in the control center files will be on-call, as required. To get additional data, the controller will initiate a query, designating the desired data. This operation is shown in Fig. 4 as the *query-reply* loop.

AUTOMATED NETWORK CONTROL CENTER

To provide the network control center functions automatically, the system concept shown in Fig. 5 has been developed. A general-purpose digital computer is proposed, together with special equipment and displays, to provide status message processing, storage, and display. The Information Processor suggested for this application is an RCA 304 computer with a record file for bulk storage.

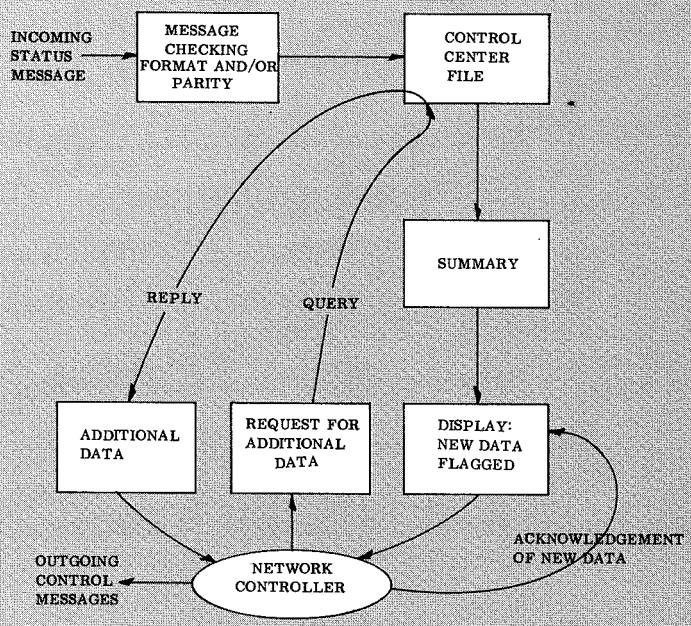


Fig. 4—Network control center information flow diagram.

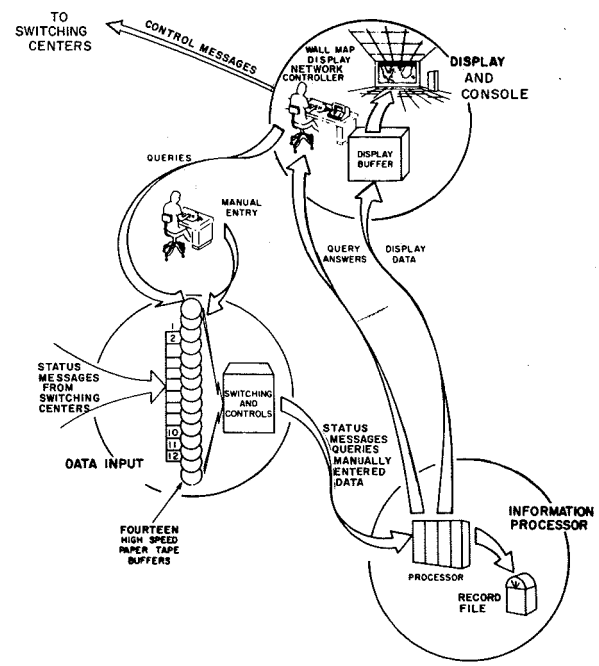


Fig. 5—Data flow in automated network control center.

Temporary storage for all incoming channels is provided by paper tape. Data can be handled on all channels simultaneously at 100 words per minute. When a complete message has been recorded on tape in one channel, it is read into the Information Processor at 1000 words per minute. The Information Processor checks the incoming messages for correct format. Messages with format errors are rejected and printed out. Control center personnel correct the format errors and reenter the corrected status messages at the manual entry keyboard.

In addition to checking the incoming status messages, the Information Processor maintains a complete file of network status. It continually provides an updated summary of network status, in suitable code and format, for transfer via the display buffer to the wall map display. New display data are indicated to the controller by flashing lights, which the controller can reset when he desires.

Both trunk equipment status and traffic backlog would be provided in a single geographic-type display (Fig. 6). These two factors are closely related and form the basis for intelligent system control decision. Above the geographic display would be a tabular display of the status of lines allocated to high priority users.

If the controller wants data other than that shown by the display, he will enter a query to the Information Processor. The Processor prepares the reply data and transfers it back to the controller. By entering a query, the controller can get any data recorded in the Processor files.

An artist's concept of the proposed network control room is shown in Fig. 6. The wall map displays the status of all switching centers, traffic backlogs, and trunks in the network. The tabular display at the top of the map shows the status of allocated channels.

The controller's console is simple and functional. It contains a page printer and

keyboard for query entry and reply and a second keyboard for composition of control messages. A small panel is provided for display illumination controls, and for indicators showing status of equipment in the next room. Although one man can operate the console, working space for an observer is provided.

A possible layout of the automated control center is shown in the artist's concept of Fig. 7. The equipment room is located next to the network control room. The separating wall has been removed for clarity. At the wall to the right is an RCA 304 Information Processor, with record file and paper tape inputs located in front. The smaller cabinets contain the paper tape punches and readers for terminating the incoming channels. Two teletype operator positions are provided; one for manual entry and the other for channel coordination with the incoming and outgoing channels. The large racks in the rear house the display buffers and other special equipment.

DATA PROCESSING IN THE AUTOMATED CONTROL CENTER

The Information Processor in the Automated Network Control Center must perform four data processing functions:

1) *Incoming Message Check.* The processor will check the format of incoming messages and reject those having format errors. The messages in error will be printed out, together with an indication of the detected error.
2) *Station File Maintenance.* A file of the current status and recent history of each station (switching center) will be kept in the processor memory. As the station status reports come in, the status information will be posted to the station file.
3) *Display Data Output.* The processor will automatically provide updated status in a form suitable for the control center display.
4) *Process Queries.* The processor will accept queries from the keyboard at the controller's console. The data requested will be retrieved from the station file and output to the page printer at the controller's console.

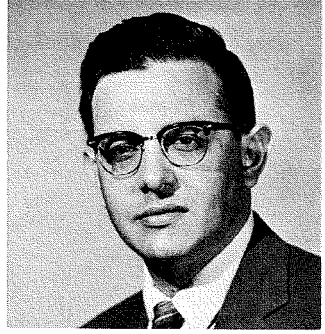
Each of these tasks must be done on a real time basis, to avoid system delays which would reduce effectiveness. The operating speed of the processor complex should be designed to keep up with the peak work load, and to catch up after periods of scheduled maintenance.

The data processing operations in the proposed control center system are based on the use of a Data Record File for storage of station status. The RCA Data Record File, Model 361, stores information on both sides of 128 magnetic coated records, with 18,000 characters stored on a side. The status of each station is stored on one side of a record in the Data Record File. Included in the stored data are the status of every trunk terminating at the station, broken down into traffic backlog, status of the trunk, status of the channels in the trunk, and status of the users having allocated channels in the trunk.

As previously described, the incoming status reports are initially stored on paper tape, and then read into the Processor as complete messages. As soon as the Processor recognizes the station identity referred to in a particular tape, it selects the record containing the status of that station and reads the complete station file into the core memory. When the station file is in the core memory and the status message has been read in, the Processor performs the updating operation. After the entire station status has been updated, it is rewritten in the record file as a unit.

As the Processor updates the station file, it abstracts the data that must be displayed. These data are translated into the proper code and format for driving the display, and transferred to the display buffer.

Query processing is done on a station basis. Each query is analyzed by the processor to determine the stations involved. The station file records are then scanned and the appropriate information is extracted and converted to a format suitable for print-out.



DAVID I. CAPLAN graduated from MIT in 1951 with a BS in Mathematics and in 1952 with an MS in Mathematics. He received the MSEE from the University of Pennsylvania in 1957. From 1952 to 1957, Mr. Caplan worked at the Burroughs Corporation, Paoli, Pennsylvania, on digital computers for various military applications. He joined the Navigation Computer Corporation in 1957 as Chief Engineer, responsible for the development of special purpose data processing equipment. In 1958, Mr. Caplan joined the EDP Division of RCA, where he worked on magnetic core memory and transfluxor development. He then transferred to Surface Communications where he was responsible for the digital ground terminal of the AGACS data link system. During the past three years, he has directed work on the design of communications systems such as Unicom, 480L, and the Minuteman Launch Control System.

SUMMARY

A system study of long-haul network control center requirements, functions, and operation has resulted in a network monitoring and control concept which includes data processing at both the switching centers and the control center. Such high speed data processing will substantially increase effectiveness of the present world wide long-haul system by reducing the reaction time to natural and man made disturbances. It, therefore, is a valuable tool in meeting the increased traffic loads and the vulnerability of communication channels to modern weapons.

ACKNOWLEDGEMENT

Many RCA engineers contributed to the network control center concepts described above. The author wishes to particularly acknowledge the efforts of A. Coleman, S. Kaplan, J. Karroll, M. Masonson, D. O'Rourke, and E. Simshouser.

Fig. 6—Typical network control room.

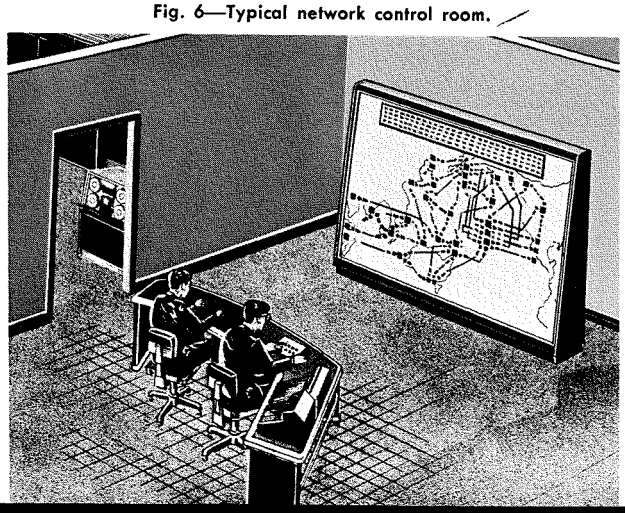
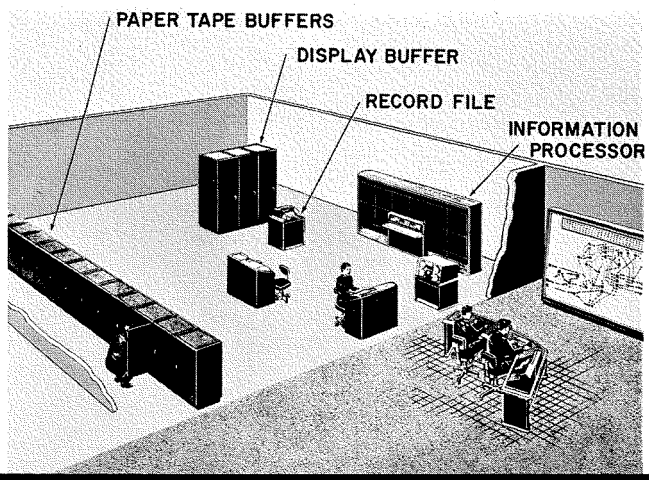


Fig. 7—Typical network control center.



A UNIQUE FAMILY OF HIGH-SPEED DIGITAL CIRCUITS

Two major circuits of a new family of serial data-processing circuits operate at bit rates up to 25 megabauds—a gated retimer and a clock-pulse generator. Others include lamp and relay drivers, a multiplexer, a demultiplexer, and a timing generator. Typical uses for this family are presented to show their versatility for general logic implementation. Proper use of this high-speed circuit family saves both hardware and cost in the implementation of any logic black-box.

W. C. MAVITY and C. D. BRUDOS
Aerospace Systems Division
Van Nuys, Calif.

RECENT NEW uses of serial data-processing techniques include circuits designed to allow 25-Mb (megabaud) data rates with additional capability for 50-Mb rates in special applications. This complete circuit family is thoroughly compatible with other computers. A recirculating memory utilizing zero-temperature-coefficient glass delay lines can be organized into a system of unlimited capacity. Any conventional drum organization can be replaced with a more compact, cheaper system with bit rates up to 50 Mb.

The complete circuit-memory complement can be used in various systems; in addition to conventional serial computers, the family can be organized into real-time processors, input-output buffers, and high-speed arithmetic units to name a few. This paper describes the main circuits in the family, including the *gated retimer* and the *clock-pulse generator*. Logical uses of these circuits are given in typical applications.

THE GATED RETIMER

The gated retimer is a unique arrangement of conventional components and circuits for use as the basic logic element for a data processing system with clock rates up to 25 Mb. The logic element can perform logic functions and always provide complementary outputs. Signal outputs do not require any special care in their interconnection. Circuits are designed to minimize the conventional interdependence of load, input, drive, and clock timing.

The gated retimer (see Fig. 1) is composed of four distinct subcircuits. The *logic array* may be an implementation of any particular logic function or expression constructed from any number of diode or diode-transistor circuits. The *strobe circuit* is a controlled-current pulse generator having a current-pulse output of sufficient magnitude to set a flip-flop. The current gate steers the current pulse to the side of the flip-flop that is to be set (or reset); the output of the logic array is compared with a reference voltage whose value is midway between the signal levels. The flip-flop stores the resultant output of the logic array as well as its complement. The flip-flop includes a filter on each output to delay the output sufficiently to prevent race conditions; this filter is the key to the retimer's successful operation, permitting the flip-flop outputs to be connected to any logic-array input (including its own), with practically no restrictions on wiring.

Fig. 2 shows a typical configuration of the gated retimer. Both the *1* and *0* outputs have a fan-out of four. The input configuration consists of three positive-logic *or* gates which drive a three-input *and* gate (the more-positive signal level is a *1*). The retimer includes four basic interconnected circuits: 1) the *flip-flop and filters*, 2) the *diode gate*, 3) the *current gate*, and 4) the *strobe circuits*, or clock pulse.

Flip-Flop and Filters

The flip-flop stores the logic function as generated by the diode gate in the form of complemented outputs. The flip-flop is composed of two inverter gates cross-connected to form a bistable circuit; the DC stability of this flip-flop is well known.

When a clock pulse occurs, a current pulse is drawn from the base of Q1 or Q2, depending on the setting of the current gate. If the transistor supplying the base current is already on, the current pulse forces the transistor on even harder; but the stability of the circuit is not affected (the flip-flop is not flipped). Thus, the input function causes the flip-flop to stay in the same state.

When the current pulse is gated to the base of Q2, the transistor in the off state, the current is supplied from R5, from the reverse recovery charge in CR4 and CR16, the charge in the base of the back-biased transistor Q2, and then from the base current of Q2 as it is turned on. The current pulse is sufficiently large to turn the transistor on long enough to insure that the flip-flop will change state. The collector of Q2 rises near ground potential; Q1 is turned off, its collector voltage falls toward V1; CR3 is reverse biased, thus insuring that Q2 remains turned on. This entire transition, the flip-flop's change of state, occurs before the end of the current pulse.

Each flip-flop output is fed through a second-order time-constant filter. The filters are composed of R1, C1, Z1 and R2, C2, Z2. These gated-retimer filters eliminate feedback problems, and avoid the usual noise-sensitive capacitor-resistor-diode gating. The filter sufficiently slows the output voltage transitions to allow the flip-flop section to be changed while the gate inputs remain well above (or below) the critical transition level (the voltage at the base of Q4). Thus, any output can be connected to its input or any other input. All circuits in a machine may be clocked simultaneously with no danger of losing information. Allowable noise levels are slightly less than half the amplitude of the signal.

To have the clock pulse end before any output voltage crosses the "critical" level is a criterion of operation; clock pulse maximum width is 12 nsec. The unfiltered output does not begin a transition concurrent with the clock pulse due to inherent circuit delays. Thus, the filter and circuit delays must be greater than 12 nsec (measured at the critical level). The second-order time-constant filter accomplishes this for transitions in both directions. Since the flip-flop cross-coupling is taken directly from Q1 and Q2 collectors before the outputs are filtered, the set time for the flip-flop is not affected by the filter. The flip-flop set time is less than 8 nsec, thereby insuring that the required flip-flop action is completed during the clock pulse. The transient strobe current applied to the flip-flop bases is four times greater than the normal base drive when the clock is quiescent. The overdrive assures that the flip-flop action will be completed during the clock pulse.

Diode Gate

The diode-gate array may assume a number of configurations. Flexibility is insured by having the reference switching voltage midway between the output levels. This allows for nearly maximum noise insensitivity; the circuit deviates from a maximum noise insensitivity of half amplitude by only a V_{be} drop at the input of the current gate. Thus, any

diode combination of *and*'s and *or*'s can be used to implement a desired logic function with an accompanying change in noise sensitivity. Speeds of common collector gates are such that they would also be useful as a method of logic implementation. Therefore, the only limitation on the input combinations would be the respective system requirements.

Current Gate

The fan-out (the number of inputs one output can drive) of the retimer as specified is that chosen for a particular application. It must be noted, however, that the base drive for the flip-flop is independent of the input loading. The flip-flop could be theoretically designed for a wide range of fan-outs. The amount of output current required is dependent upon the gate input current as determined by the input resistors. The gate input resistors are determined solely from transient conditions at the input base of the current gate. A 2N709 is used for high clock rates since its capacitance is the lowest presently available, allowing minimum power dissipation, maximum R10, for any given time constant at the base of the current gate.

Strobe Circuits (Clock Pulse).

The clock-pulse width remains constant no matter what operating frequency is used; hence, the delay required is always constant. The output wave-shape can best be described as a delayed exponential. Since the filter inductance is heavily damped, the waveform is delayed slightly and then appears as an RC time constant. This decreases the frequency-spectrum bandwidth of the output signal considerably, allowing the relatively nonrestrictive wiring rules. Thus, the internal voltage steps and current pulses of less than 5-nsec rise and fall time appear as 20- to 25-nsec rise and fall times at the circuit output. Marginal circuit operation could be assumed after the rise or fall times reach half amplitude. Good design requires waiting until at least 90% rise or fall is achieved. Diode and/or common-collector transistor gating are active gating; except for a possible initial delay, they move with the input waveform. Thus, logic can be performed during transition with minimum series delay, a powerful method for achieving logic implementation in short times.

THE CLOCK PULSE GENERATOR

The *clock pulse generator* is the other main circuit in the family. For successful gated retimer operation, the circuit must be capable of generating a 10-nsec, 2-volt pulse of sufficient current to drive many retimers. The clock must operate within close tolerances because each circuit in any system must be clocked at the same time. The 25-Mb clock pulse generators are uniform within ±1 nsec. Gated retimer modules are clocked by terminated transmission lines of equal length; in this way there is equal delay in each line. Terminated lines insure that proper pulse shape is retained throughout the distribution system. Each clock circuit is capable of driving 17 terminated lines, i.e., 17 gated retimer modules. The present configuration has 4 retimer circuits on each module, hence one clock is used to drive 68 gated retimer circuits. In a special case where 6 retimer circuits are mounted on a module board, one clock can drive up to 102 gated retimer circuits.

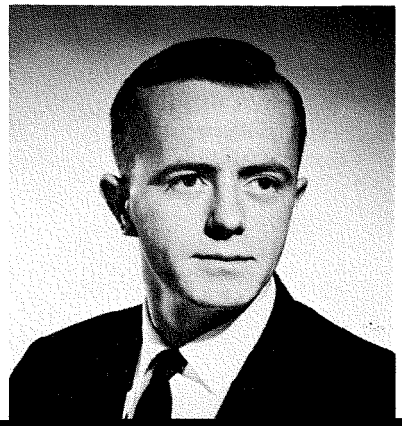
Circuit Operation

Fig. 3 shows a schematic diagram of the clock pulse generator. The timing input to the circuit is a square wave with rise and fall times of less than 10 nsec; switching is between 0 and –4 volts. The 100-ohm resistor provides proper termination for the timing input; a clock pulse output is generated when timing input transitions are 0 to –4 volts-D.C.

In the system for which this circuit was designed, the transmission line terminations are 100-ohm resistors connected to –4.5 volts-DC. Thus the *off* level for the output pulse is –4.5 volts-DC and the *on* level is determined by the total output current which flows into a resistive load equal to (100 ohms÷17) in the case where 17 transmission lines are driven; this load would then be 5.9 ohms. To develop a 2-volt pulse which is used in this system requires a current pulse of (2 volts÷5.9 ohms)=340 ma.

WILLIAM C. MAVITY graduated from the University of Illinois in June 1958, and has completed graduate work toward a Masters Degree at the University of Pennsylvania and the University of California at Los Angeles. Upon graduation he joined RCA as a member of the Engineer Training Program. His permanent assignment was with the Digital Design Unit of the Missile and Surface Radar Divisions. There he designed a universal logic circuit, variations of which now appear in several DSD standard computer modules. He transferred to the Data Systems Division in August 1959. He completed the design, development, and equipment incorporation of a basic logic circuit for a 25 megabaud digital circuit family. He has completed an evaluation of the use of high speed glass delay lines which successfully showed their usefulness as a high speed storage medium. Mr. Mavity is a member of Sigma Tau, IEEE, and is a Junior Member of the Illinois Society of Professional Engineers.

C. D. BRUDOS graduated from South Dakota State College in 1958 with a BSEE. He has completed the unit requirements for the MSEE at U.C.L.A. Prior to joining RCA he was employed as a digital design engineer at Remington Rand Univac and served in the U.S. Army Signal Corps. Mr. Brudos joined the Data Systems Division in 1959. His first assignment was the design and development of a 10-megabaud logic circuit which was incorporated in a high-speed digital equipment as the basic logic circuit. He also designed a high-speed module tester for the 10-megabaud digital circuit family and served as an instructor in a training course on the equipment for the Army. He was responsible for the circuit design and development for the 4101 (MIPIR) Computer and most recently for the 4102 and 4103 Computer. He has also completed the design of the 25-megabaud timing circuits for a 25-megabaud digital circuit family. Mr. Brudos is a member of Eta Kappa Nu, Sigma Tau, Phi Kappa Phi, and the IEEE.



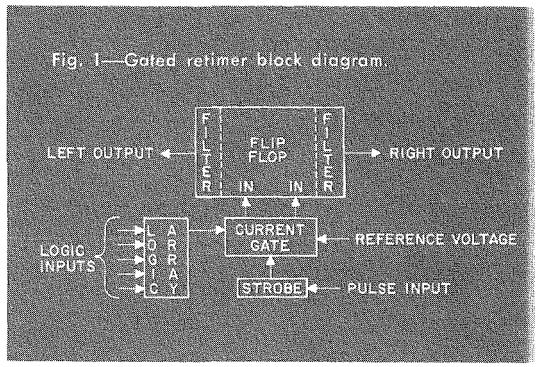


Fig. 1—Gated retimer block diagram.

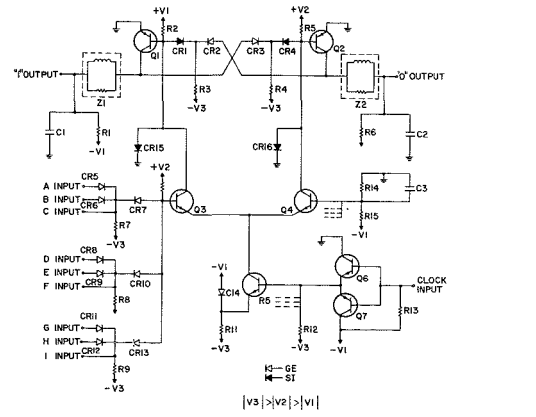


Fig. 2—Gated retimer circuit.

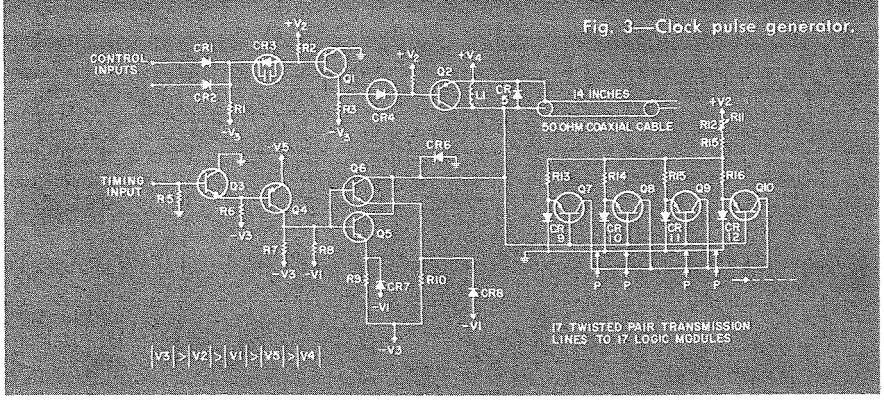


Fig. 3—Clock pulse generator.

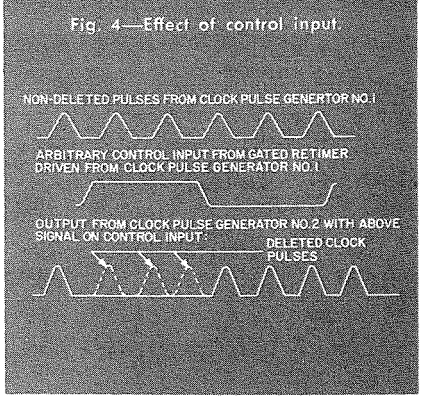


Fig. 4—Effect of control input.

This requires a current pulse from each of the four output transistors (340 ma÷4)=85 ma. This current drain is well within the capability of the transistors, each of which can deliver 100 ma minimum. The current pulse is adjustable by means of variable resistor R11.

The width of the output pulse is determined by the length of the shorted coax and the turn-on time of transistors Q5 and Q6. Using the 2N914 with 14 inches of shorted coax, an output pulse width of 8 nsec (measured at the 50% points) is produced.

The control inputs must be synchronous to prevent half-pulse generation at the output. The control inputs may be driven by a gated retimer that switches immediately following a given clock pulse and deletes the following clock pulses. Either or both control inputs at ground will cause the clock pulse to be deleted; this is shown in Fig. 4.

Clock Pulse Generator Application

Although the clock pulse generator circuit of Fig. 3 was designed to drive 17 transmission lines, the circuit concept could be used to design a higher fanout (number of loads attached to the output) pulse generator. Since the output transistors share the load almost perfectly, more output transistors could be used to obtain more pulse current. This would necessitate more base drive from the previous stage and a lower impedance shorted coaxial cable.

One can use several pulse generators in a synchronous system when the square-wave timing inputs are in synchronism. Variations in delay through the pulse generator circuits are in the neighborhood of ±1 nsec of each other. The primary advantages are:

1) Constant pulse width versus frequency.
2) Frequency range, 0 to 25 Mb.
3) Output transistors are paralleled so that more can be added to provide increased fanout.
4) Amplitude of pulse is adjustable.
5) Output pulse may be deleted by control input.

USES OF THE GATED RETIMER

Following are descriptions of eight typical ways in which the gated retimer circuit family can be utilized. These are by no means exhaustive and are presented to show the versatility of the family. In each of the examples, normal synchronous clock input will always be assumed present and therefore not shown in the logic symbol. However, when a controlled clock is used, it will be shown as an additional input at the side of the logic symbol. The logic symbol is shown in Fig. 5.

Considering time slots to be separated by clock pulses, the *1* output during the time slot (n+1) is the resultant of the logic function $(A+B+C)\cdot(D+E+F)\cdot(G+H+I)$ at time *n*. The *0* output is the complement of the *1* output and represents the function $ABC+DEF+GHI$.

Shift Register (Fig. 6): It is important that only one interconnection is required for each shift register stage. Also, each unused *or* gate must be tied to ground to avoid disabling the *and* gate. If the *1* output becomes fan-out–limited, the shift register may be implemented by taking the *0* output to the next stage, with the understanding that the functional outputs are reversed. This feature allows additional freedom when implementing a logic organization.

High-Speed Storage (Fig. 7): When the gated retimer is used as a storage cell a special clock must be used; it may be turned on or off by a retimer that is driven by the regular clock. A special clock is a regular clock pulse generator whose control inputs are used to suppress clock pulses in some special manner. The special clock, then, can be turned on for one clock pulse; it is used to read in the data setup on the input during the previous regular time slot. The outputs then store the data until the next special clock pulse. When several gated retimers are driven by the same special clock they form a high-speed storage register.

Set-Reset Flip-Flop (Fig. 8): Set pulse is a *1* when it is desired to set the flip-flop. There can be several set pulse inputs, and they are "*or*'d" together at the flip-flop input. The reset pulse must be a *0* (hence, for consistency it is called $\overline{R}$). The reset pulse $\overline{R}$ overrides the set pulses *S*. One reset pulse may be applied to each used *or* gate which, in effect, allows two independent reset pulses to be used.

Binary Differentiator (Fig. 9a, b): The positive differentiator has a *1* output of one time-slot duration, one time slot after the input goes from a *0* to a *1*. It disregards an input transition from *1* to *0*. In a similar manner the negative binary differentiator detects a change of state at the input from a *1* to a *0*, and also has a *1* output of one time slot deviation, in the next time slot.

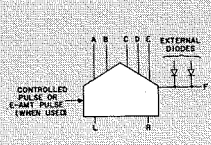


Fig. 5—Gated retimer logic symbol.

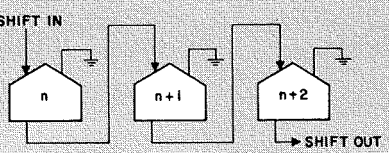


Fig. 6—Gated retimer shift register.

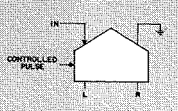


Fig. 7—Storage cell.

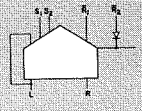


Fig. 8—Set-Reset flip-flop.

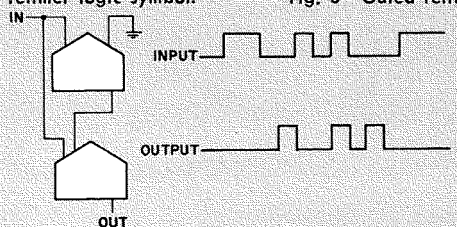


Fig. 9a—Positive binary differentiator.

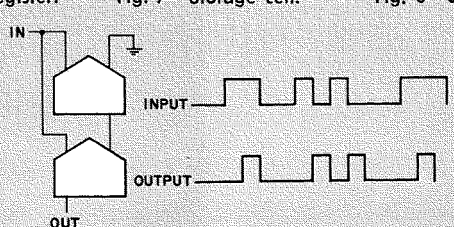


Fig. 9b—Negative binary differentiator.

Modulo-Two Adder (Fig. 10): The modulo-two adder *(exclusive–or)* is especially easy to implement, since complemented outputs are always available.

Serial Full Adder (Fig. 11): Addends are read, least significant bit first. It is important to note that when $\overline{C}$ (the carry) is fed back, it accomplishes the delay required to form the next carry. It is further important to note that the $\overline{X}$'s and $\overline{Y}$'s used to generate the carry must be taken after they are used in the modulo-two adder. When the sum is being made from two circulating registers and if it doesn't replace one of the addends, the time-slot difference can be accomplished by taking the inputs from the next stage of the register. If this is not possible, the output C must be delayed one time-slot by inserting another retimer in series with the C outputs before they go into the S retimer. The R inputs are included to indicate that the carry can be reset when a new sum is started.

Binary Counter (Fig. 12): When the input is a *1*, the counter begins to count; however, after the count has stopped it is necessary to allow $n+1$ (where n is the number of stages) clock pulses while the final carry is being propagated. Provision can be made to reset the counter on demand by utilizing the third *or* gate input.

GENERAL SYSTEMS APPLICATION

The gated retimer's ability to perform several levels of logic and provide complemented outputs fulfills the requirements imposed by serial machines. The usefulness of the gated retimer, however, is not limited to serial data processors. There are many applications in conjunction with parallel machines. Many special-purpose computer sections can be especially adapted to retimer implementation. Input-output peripheral equipment and arithmetic units are two examples. The circuit is also applicable as a general-purpose logic element. Fig. 7 shows the use of the gated retimer as a storage cell which can be expanded to form a storage register. This basic configuration can be modified to facilitate high-speed serial-to-parallel (or reverse) conversion and as such is readily transformed into an input-output register. Since the controlled clock is available, the only change necessary is to incorporate shifting logic into the storage register. These logic changes are straightforward and pose no problems to the retimer.

Arithmetic Unit

One special purpose application that shows promise is an adder-multiplier arithmetic unit. This special black-box is easily designed and would be capable of adding serially two 30-bit words in 1.2 μsec and multiplying the same two words in 36 μsec, maximum. Multiply time assumes a worst-case condition of all *1* bits in the multiplier. For each *0* bit in the multiplier, the multiply time is reduced by 1.16 μsec. An average multiply time (half *1*'s, half *0*'s) would be 18.6 μsec. The gated retimer registers used in this arithmetic unit would be available for other uses found in the registers of a conventional parallel arithmetic unit.

A present-generation parallel computer has an add time of ½ μsec and a multiply time of 60 μsec which cannot be reduced by *0* bits in the multiplier. While there is some sacrifice in absolute add time, there is no actual loss in machine time, since the memory-cycle time is usually the speed-limiting item. In a multiplication, however, the multiply time is limiting and any reduction is a machine time saving. On a direct replacement basis both adder-multipliers have approximately equal hardware requirements. If a large parallel computer were designed around the gated retimer considerable hardware savings would result; and above all, the speed of the machine would be greatly increased.

General Logic Element

The gated retimer has many applications as a general logic element. It has a fan-out of four at each of its complemented outputs that could be increased to five or six with minimal modifications. Any number of input arrays are feasible. While the present circuit has two levels of diode logic, there is no reason why more levels cannot be added. Emitter follower amplifiers should be used within the diode logic for current gain. The special clock feature is especially useful in a parallel organization using the gated retimer. With it, timing levels may be set up to give the retimer equal versatility with present *nand-nor* logic. An added advantage is gained through the filters. Wiring constraints when interconnecting gated retimers are greatly reduced over those required when conventional gates are used.

The gated retimer has all active gating, providing minimal series propagation delay; this is in contrast to the pair delay of a conventional gate. Since propagation time for the same amount of logic is less, longer rise and fall time waveforms can be tolerated. The longer times require less bandwidth; hence, more open wire can be used than with sharp step waveforms. Great savings in wiring complexity can be realized. Various tests show that open wire lengths up to three feet long are entirely feasible. Twisted pair appears more than sufficient for longer runs. Coaxial cable need never be used. No special packaging is required; circuits are laid out on conventional printed circuit boards. These advantages alone make the use of gated retimers highly desirable.

25-to-50-Mb Memory Capabilities

The basic memory loop can store 12,000 bits at 25 Mb. Data rates of 50 Mb can also be accommodated by utilizing parallel loops and placing alternate bits in each loop. Each loop operates at 25-Mb rates internally and can be reconstructed back into a single 50-Mb output stream. Circuits are available in this family for proper separation and recombination of the data stream. This capability insures that a memory system will be available for future circuit developments up to 50 Mb.

The 12,000 bits can be considered as a portion of a conventional drum track. Memory loops can be broken and put in series to achieve any multiple number of bits desired. Any length loop can be paralleled, simulating memory drum tracks. This allows a high degree of flexibility at high-speed data rates.

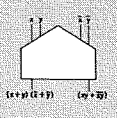


Fig. 10—Modulo-two adder.

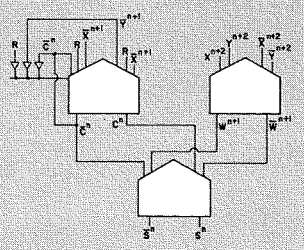


Fig. 11—Serial full adder.

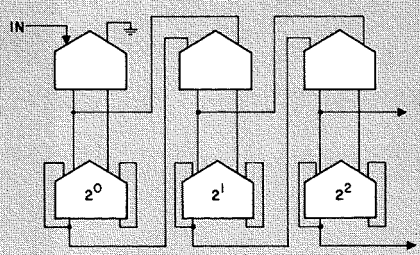


Fig. 12—Binary counter.

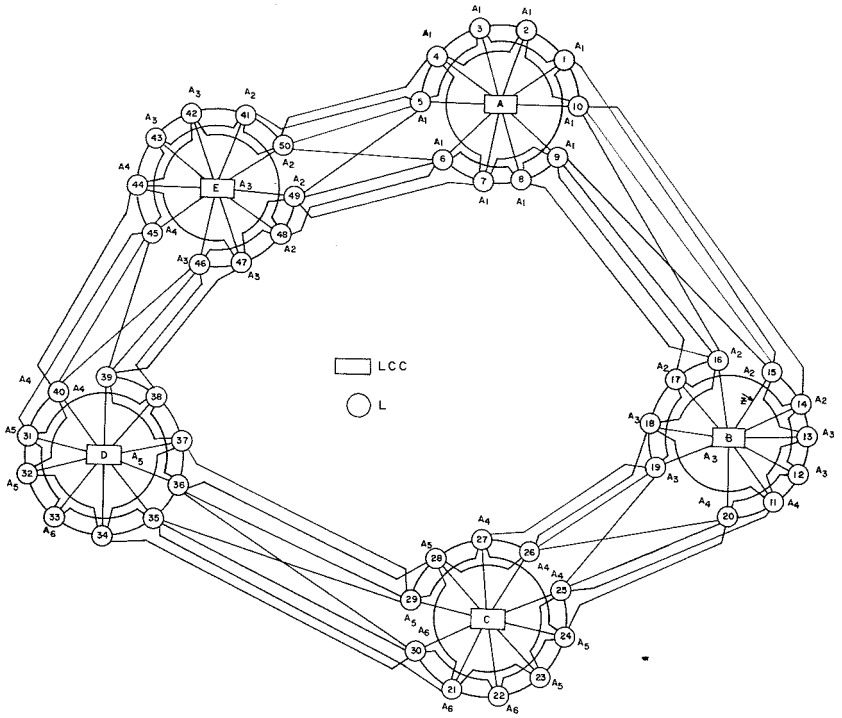


Fig. 1—Idealized MINUTEMAN Squadron sensitive-command network, showing buried-cable interconnection of the 50 unmanned underground launch silos (L's) and the 5 manned launch-control facilities (LCC's). Each line is a 4-wire, 2-way digital data circuit. In practice, actual shape of network paths depends on terrain. Average cable length is 23 miles.

MINUTEMAN DIGITAL-DATA TRANSMISSION SYSTEM TESTS

The high operational reliability required of the communications network for the MINUTEMAN launch-control system made it imperative that extensive testing be performed at various levels of development, prior to installation. Meeting this requirement rests on two types of reliability achievement: one comprises the familiar equipment reliability considerations; the other, emphasized in this paper, relates to the reliable generation, transmission, and demodulation (in the presence of interference) of the digital data signals used for command and status functions.

A. CORTIZAS, Ldr., and J. H. WOLFF, Ldr.
Systems Laboratory, Communications Systems Division
DEP, New York, N.Y.

A. P. CORTIZAS graduated from Polytechnic Institute of Brooklyn with a BEE degree in 1951 and an MEE degree in 1957. From 1951 to 1954 he contributed to the development of high-power UHF negative grid tube and klystron—transmitters at ITT. From 1954 to 1958, he conducted military communications, research and development for Olympic Radio & Television. Mr. Cortizas joined RCA's Surface Communication Laboratory as a Senior Project Member of the Technical Staff in 1958. He contributed to an advanced communication concept known as Radio Relay Central. He has also participated in millimeter and satellite-communications system studies. In 1959 he became a member of the RCA Minuteman Project Management office and is currently Leader, Minuteman Systems Organization. Mr. Cortizas is a member of the IEEE, Eta Kappa Nu, and Tau Beta Pi.

J. H. WOLFF graduated from New York University with a BEE in 1954. From 1951 to 1959 he worked for the American Telephone and Telegraph Company on the engineering of integrated long-line communication facilities at voice, carrier and microwave frequencies. He joined RCA in 1959 and is currently on loan to the Minuteman PMO. During this period he has been engaged in system and transmission engineering of the Minuteman communication network, and was responsible for conducting an R&D program on the hardened buried cable transmission system as well as data transmission. In 1962 he was promoted to Leader, Engineering Systems Projects, DEP, SurfCom. Mr. Woff has authored and delivered several papers on communications, and is a member of the IEEE, and IEEE-PTGCS.

RCA HAS played the prime role in establishing the over-all MINUTEMAN communication-system configuration, generating detailed specifications and conducting related test programs. These activities were carried out under the direction of the Boeing Company, the Ballistic System Division of the Air Force, and Space Technology Laboratories.

In the data-transmission tests described in this paper, RCA investigated the characteristics of the major communications subnetwork of the launch-control system: the *sensitive command network* (SCN), a major subsystem of the MINUTEMAN launch-control system. It is the medium through which remote control of the launching function is accomplished. It also performs auxiliary functions, which complement the primary function of reliable launch command control.

An idealized SCN interconnects a MINUTEMAN Squadron's 50 unmanned underground launch silos (L's) and its 5 manned launch-control centers (LCC's), as shown in Fig. 1. Each LCC can control all 50 L's, and all the L's and LCC's are hardened and dispersed. The redundant buried-cable network that interconnects the L's and LCC's is fitted into a trench pattern that provides redundancy sufficient for survival.

The sensitive commands, which are *launch* and *inhibit-launch* commands, are generated at LCC's and transmitted in the form of binary-coded, digital-data messages over the command network. The modulation is modified diphase, developed by RCA.[1] Fig. 2 illustrates the modified diphase signals transmitted over the cable system. Messages, formed by *mark-space coding* a diphase signal, propagate over the entire network. At each node (LCC or L) the message is checked for validity before being retransmitted to adjacent nodes in the network. The possibility of message interference at any point in the complex is eliminated by assigning to L's and LCC's a set of switching rules which are automatically invoked during periods of message propagation. Of course, at each L, the receipt of such messages effects control of the MINUTEMAN missile. Each L can receive commands on any one of six receiving lines and retransmit these commands simultaneously over six transmitting lines. The LCC has ten *transmit* and ten *receive* lines through which it can propagate messages. The many

paths provided by this redundancy of transmit-receive links, together with the hardness designed into the LCC and L, provide the communications system with a high degree of invulnerability to enemy attack.

During normal peace-time operations, additional communications circuits are required within and beyond the squadron for supervisory, maintenance, command, and coordination functions. In this connection, intra-squadron circuits involve additional diphase, voice, tone, and DC circuits. For reasons of economy in some cases, and for reasons of vulnerability in others, all these services share the same hardened cable plant employed for the sensitive command network. This paper deals only with the performance of the digital transmission circuits which employ the modified diphase techniques.

THE SINGLE THREAD

In evaluating parameters and performance characteristics of the overall SCN it is convenient to first examine its smallest complete entity; a *single-thread network* consisting of one LCC, one L, and the interconnecting transmission link. The principal LCC equipment items pertinent to this network are the *command control console*, the *data processing equipment*, and the *cable terminating equipment*. At the L, the corresponding equipment complement consists of cable-termination equipment, data processor, and a *sequencer and monitor* whose primary function is to program a launch countdown process. (The termination equipment and data processors at both LCC and L are RCA-designed equipments.) The control console and the sequencer, as well as the assembly of the entire weapon system, are under direct Boeing cognizance.

Multipair, 16- and 19-gauge polyethylene-insulated cable interconnects the two terminals. Cable lengths range from 7 up to 40 miles, with an approximate average of 23 miles. For maximum reliability, unloaded and non-repeatered cable is employed on all links.

Operation of the "single thread" is basically as follows: The LCC either initiates command messages or retransmits any received command messages. Retransmission of received messages occurs only when the LCC is not initiating commands, and this only if the received messages pass certain validity checks. Messages are received at the L through the cable-termination equipment, which amplifies and equalizes any distortion incurred in the non-loaded cable. The modified-diphase signal is then demodulated, retimed, decoded, and transmitted both to the sequencer and to the transmit lines via the diphase modulator and the termination equipment. The sequencer receives only that part of the message essential to control of the missile. In addition to the command subnetwork described above, the single thread also contains an L-to-LCC status reporting subnetwork, which provides the LCC with a continuous report of the operating state of the L. Voice circuits needed to coordinate activities in the squadron also employ the single thread cable route.

THE TEST PROGRAM

Early in the development program, RCA initiated plans for a test program, wherein a number of L's and LCC's would be interconnected with the aid of cable simulators (explained in a later paragraph) in patterns typical of those existing in a squadron. These tests were designed to validate both the performance of the switching rules and the data transmission links. Eventually this program was carried out, and tests were successfully conducted with the support of RCA engineering personnel in the network resolution area of The Boeing Company. In the interim, RCA implemented a program of tests to verify the performance, first, of the individual elements in a single thread of the SCN, and subsequently, of the complete integrated single thread system. In the area of data transmission, this program entailed the following major tasks:

a) Data-processor and cable-termination equipment
b) Cable tests (equalization)
c) Cable tests (crosstalk)
d) Cable simulation tests

Data Processor and Cable-Termination-Equipment Tests

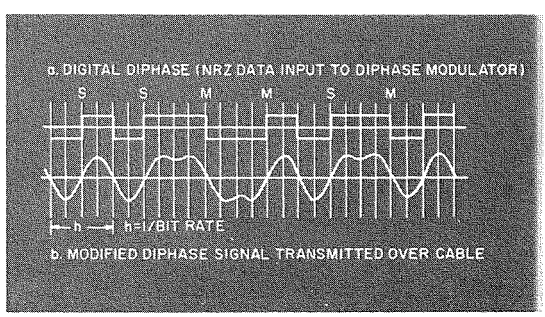
Although feasibility tests had been performed in the modified diphase development program, this equipment had not been tested in an integrated single-thread system. The additional factors introduced which might have affected the system's transmission performance were 1) the inclusion of a line-selection function equivalent to one drawer of logic between the termination equipment and the demodulator, 2) local clock synchronization employed for the retiming of messages for retransmission, 3) the use of cable and cable terminating equipment, 4) drift between transmitter and receiver oscillator frequencies, 5) the message-checking function, 6) the message-retransmission function, 7) the possibility of interaction between data processing equipment and demodulators via common power-supply impedances, 8) power-supply regulation and ripple, and 9) stray coupling effects. All these factors were included in the digital transmission tests which were part of an over-all systems evaluation program.

In this program particularly careful control of tests was maintained in order to determine whether any of the above factors might have individually or collectively contributed to degradation of the basic performance of the diphase modulation system.

In order to evaluate the significance of these test results, statistical theory was employed to establish confidence limits and determine whether deviations obtained were statistically significant or were just attributable to experimental error. This, in turn, required that a large number of readings be obtained rather frequently, to establish the normality of samples by a chi square test; and, having established that samples belonged to a Gaussian distribution, i.e., were normal, confidence limits were then obtained by the so-called *t-test*.[2]

The test program began with a series of control tests in which the physical and electrical environments of the data link were established; e.g., room atmosphere, power supply regulation, ripple, and noise (see Fig. 3). Demodulator threshold (i.e., sensitivity) tests were then performed to establish how far below the nominal operating signal level the demodulators functioned. Tests on ten different circuits in the LCC data processor determined the mean and extreme performance available from these samples. The results indicated that the demodulators would function with signals ranging over approximately a 30-db change in level. In more familiar terms, this would be equivalent to a hypothetical change in cable length of ±15 miles. (Subsequent higher-gain demodulators provide a threshold close to 33 db below nominal level.) Actually, the tolerances in transmission loss in the cable system due to temperature and manufacturing tolerances are within 3 db of its nominal value (equivalent to the loss in 3 miles of cable). The above sensitivity is, therefore, quite ample; and, in fact, other

Fig. 2—Modified diphase waveforms.



system factors associated with maintenance have dictated that a demodulator be switched away from a line long before the dynamic range in signal can occur. Detector thresholds were established both by noiseless bit-error-rate techniques and visual observation of waveforms in the demodulator. Both techniques provided results in close agreement.

Following these tests, and with the set-up shown in Fig. 4, the lowest-, median-, and highest-threshold demodulators were subjected to bit-error-rate tests with additive white noise. The results obtained indicated a spread of 15% in error rate between the lowest and highest threshold demodulator, a difference which, in light of the estimated average signal-to-noise (S/N) ratio of greater than 20 db in the actual installation, proved to be rather insignificant. The mean performance measured is shown in Fig. 5, and compared very well with error rates determined in the modified diphase development program. This test provided the desired correlation between a demodulator on a test bench and one integrated into a system.

Based on 1) the reaction time of complete command message processing, 2) the security of the message establishing a minimum number of bits, and 3) the launch reliability requirements imposed on the system, a transmission performance objective was established prior to equipment design. This objective was to obtain a bit-error rate probability of less than 10^{-4} at a received S/N of 15 db. As Fig. 5 shows, this error rate corresponds to a $S/N \approx 13$ db. Since in the actual installation an average S/N will be greater than 20 db, a considerable safety factor is indicated.

Various other tests followed to establish the effect of input signal variation level at a constant S/N. These tests, which preceded the addition of cable and termination equipment to the system, showed a high degree of insensitivity to demodulator input-signal level. The termination equipment was then added to the system, and tests were resumed using several lengths of 19AWG, polyethylene-insulated cable. An eight-mile length of a representative sample of the type to be used in the operational system was available in the laboratory for these tests. A 25-pair cable was used, and transmission over 8, 16, 24, and 32 miles of this cable was tested by routing the transmitted diphase via 1-, 2-, 3-, and 4-wire pairs, respectively, of an 8-mile length of cable. The objective of this test was to determine the effect of the termination equipment and cable on the basic demodulator error-rate performance.

Equalization Tests

Phase and gain equalization of the cable are provided in the termination equipment so that the diphase signal encounters minimum distortion over the cable links. The equalizer adjustment was determined experimentally as not critical.

The results obtained (Fig. 6) indicated that for 8, 16, and 24 miles of 19AWG cable no significant difference in performance was evident from that of the basic modem above (performance of the basic modem is shown in dashed lines).

Specifications relating cable gauge to cable length indicate that above 24 miles 16AWG cable should be employed. The above test showed, however, 1-db degradation in S/N performance between the 24- and the 32-mile tests. These tests were repeated with both signal and white noise applied at the transmitting end of the cable. The results obtained indicated a performance improvement of approximately 1 db, which was due to the noise-shaping effect of the cable equalizer above 2-kc noise frequencies.

Crosstalk Interference Tests

The objective of these tests was to determine the effect on diphase transmission of the cable crosstalk characteristics. Specifically, the tests were made to 1) determine the effects of diphase signal transmission under various noise and crosstalk interference conditions, 2) determine the types and levels of interference which could be tolerated for successful signal transmission, and 3) obtain sufficient data to allow subsequent comparison with results of similar tests on simulated cable.

Fig. 7 indicates the test arrangement used for the near-end crosstalk measurements. A similar arrangement was used for far-end crosstalk.

The tests were performed on an 8-mile-long 25-pair 19AWG cable section, which was of similar construction to the operational MINUTEMAN cable. The disturbing signals for all these crosstalk tests were applied to those cables that had previously exhibited the worst crosstalk characteristics during signal-frequency crosstalk-coupling-loss tests.

Four channels of disturbing diphase signals, identical to the disturbed diphase signals in message structure and bit delay, were applied to four cable pairs. In addition, other disturbances were applied: tape-recorded voice at zero VU, 2.6-kc signalling at 3 dbm, and an interrupted direct current of 28 volts.

A bit error-rate test was then performed over a 20-hour period. At the end of this time no errors had been recorded. To extend the length of the circuit from 8 miles to the maximum permissible circuit length, a 24-mile cable simulator was inserted ahead of the 8-mile cable pair of the disturbed channel. This arrangement increased the attenuation by an additional 28 db prior to the 8-mile crosstalk coupling exposure of the cable. The disturbed signal level was set for +3 dbm at the secondary of the transmitter repeat coil. This gave a received level of −41 dbm at the primary of the disturbed channel repeat coil.

The four disturbing diphase-channels were increased above the operational levels to +6 dbm, and the 2.6-kc signalling was raised to +8 dbm to obtain maximum interference into the disturbed diphase channel. A bit error-rate test was then run for a 65-hour test period. At the end of this time no errors had occurred.

Near-end and far-end crosstalk tests were then repeated with the receiving

Fig. 3—Checking cable pressure and splices in the communications cable laboratory. Left: D. A. Cornelius, RCA Service Co. engineer; right: coauthor J. H. Wolff.

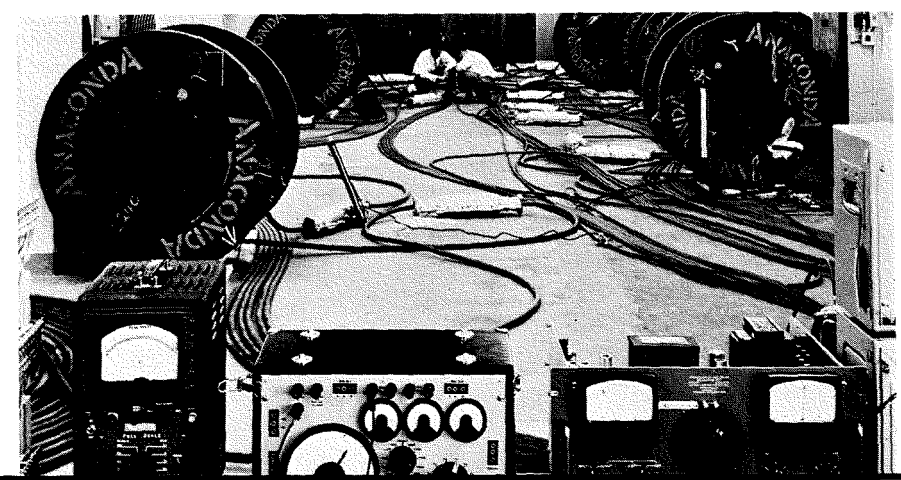
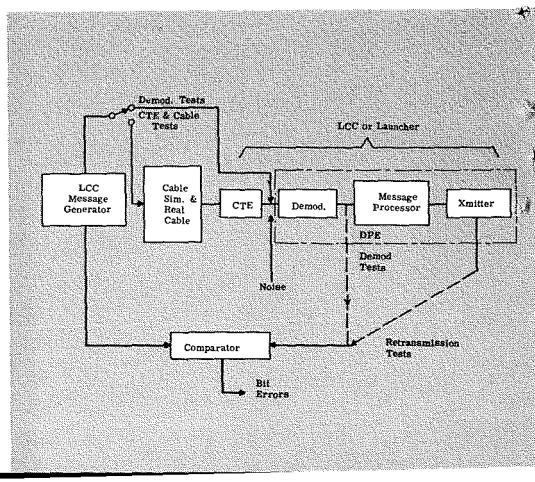


Fig. 4—Single thread test setup.



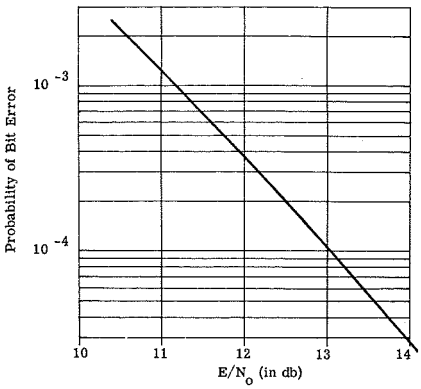


Fig. 5—Bit-error rate measurements in the presence of white noise.

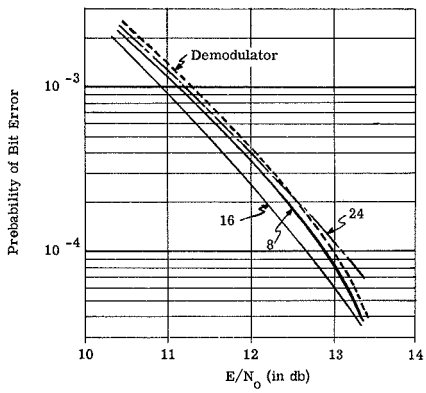


Fig. 6—Bit-error rate measurements in the presence of white noise over equalized cable circuits.

disturbed channel biased with white noise.

Bit-error-rate tests were performed on this disturbed diphase channel under the following conditions: Four disturbing diphase channels transmitting simultaneously; interrupted 2.6-kc signalling; 28-volt DC interrupted; and voice, all transmitting simultaneously. These tests were run for near-end and far-end crosstalk at E/n_o ratios of 10, 12, and 14 db, where E = watt-seconds/bit (average energy/bit); and n_o = watts/cycle (noise power density). To establish reference error rates, tests were also run at these E/n_o ratios with no disturbing signals applied to the cable.

A summation of pertinent data for the near-end crosstalk tests is plotted in Fig. 8. The results for far-end crosstalk showed similar trends. From Fig. 8 it was concluded that for near-end crosstalk, four channels of disturbing diphase degraded the system by 0.25 db (at E/n_o = 10 db) to 0.7 db (at E/n_o = 14 db). Four channels of disturbing diphase plus voice, 2.6-kc and 28-volt DC, degraded the system by 0.5 db (at E/n_o = 10 db) to 1.0 db (at E/n_o = 14 db). For far-end crosstalk the average degradation was less than 0.1 db.

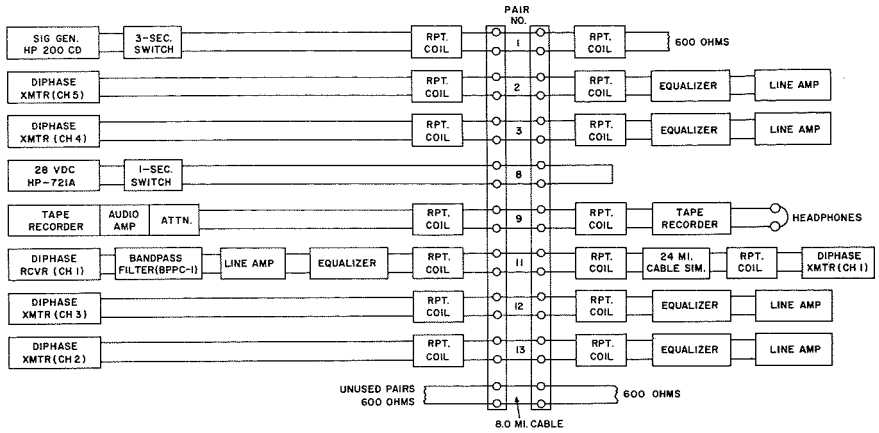


Fig. 7—Near-end—crosstalk test instrumentation.

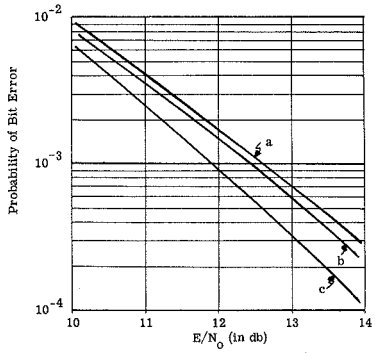
Cable Simulators

A considerable number of cable simulators were required by the various MINUTEMAN test activities, which for practical reasons, had no access to significant lengths of real cable. RCA supported these programs by developing and manufacturing 10- and 20-mile cable simulators for both 16AWG and 19AWG, polyethylene-insulated cable. These simulators duplicated the impedance, attenuation, and delay characteristics of the cable with a high degree of precision, and were intended primarily for use in bit error-rate tests.

Another aspect of this test program was the verification of these simulators. Following measurements of characteristic impedance, attenuation, and delay, the simulators were used in a series of bit error-rate tests employing white noise. By a process of substituting the simulators for the cable in the test setup shown in Fig. 5, the performance of 10-, 20-, and 30-mile cable simulators was compared to that of 8, 16, 24, and 32 miles of real cable. The difference between the performance of 8, 16, and 24 miles of 19AWG cable with 10 and 20 miles of simulated cable were found to correspond to less than an E/n_o = 0.3 db as measured between E/n_o = 10 and 14 db. In the case of 30-mile simulation, obtained by placing 10- and 20-mile simulators in series, the difference was no greater than E/n_o = 0.5 db. These differences, which correspond approximately to the 95% confidence band of the test data, verified the accuracy of the simulator to be adequate for all the test programs involved.

CONCLUSIONS

This paper has described only a few of the many tests which were performed by RCA to verify the predicted performance of the sensitive command network of the MINUTEMAN communication system.



a. Four Channels Disturbing Diphase + Voice, 2.6 kc & 28V dc.
b. Four Channels Disturbing Diphase
c. No Disturbing Signals

Fig. 8—Bit-error-rate measurements in the presence of crosstalk and white-noise interference.

The tests were performed under white-noise conditions to allow comparison with theoretical predictions. Other in-plant and field tests investigated the performance of the system under different noise environments (lightning, power-line induction, crosstalk, impulse, etc.). All the tests performed to date have indicated that under the worst predicted noise conditions the probability of bit errors occurring is far less than required by the system criteria.

ACKNOWLEDGEMENT

The tests described in this article involved a great deal of testing and data analysis and reduction. This is to acknowledge the assistance of the numerous engineers and technicians who participated in this and associated test programs, particularly that of C. G. Arnold, Director of Systems Engineering, MINUTEMAN PMO.

BIBLIOGRAPHY

1. D. Douglas, G. Aaronson and G. Meslener, "A New Digital Communication System Modified Diphase," presented at GLOBECOM V, May 1961.
2. S. Diamond, *Information and Error*, Basic Books, Inc., 1959.

Engineering and Research NOTES

BRIEF TECHNICAL PAPERS OF CURRENT INTEREST

Radar Observations of the Clear Atmosphere Between 10,000 and 30,000 Feet

R. J. WAGNER, JR. AND L. C. CONANT, JR., *Missile and Surface Radar Division, DEP, Moorestown, N. J.*

Theory predicts that a sufficiently high-powered radar should produce detectable echoes from inhomogeneities in the clear atmosphere.[1] If it could be demonstrated in practice that radars are indeed capable of direct observation of atmospheric turbulence and other clear-air phenomena, possibilities of new instrumentation and techniques would be opened in the fields of meteorological research and observation, missile launching, and air traffic control.

Limited experimental verification of the theoretical speculation has been obtained. The experimental program was conducted using a modified AN/FPQ-4 radar, located near Moorestown, N. J. This is a precision monopulse tracking radar, operating at C-band (a frequency of 5,736 Mc was used in the experiments) with a peak transmitter power of 3 Mw, and an antenna gain of 47 db above an isotropic source. The receiver noise figure was 4.5 db, using a parametric amplifier in the first RF stage. Various pulse repetition rates were available, but usually 855 pulses/sec were used during the experiments described here. The pulse length was 1 μsec.

The experiments were carried out at various times during the daylight hours (and at night on one occasion), during the months of March, April, and May of 1962. The atmosphere was considered suitable for experimentation if visual inspection indicated there were no clouds or haze.

Some simultaneous rawinsonde observations were obtained by courtesy of the U. S. Army Signal Research and Development Laboratory, Fort Monmouth, N. J. The site of the balloon releases was about 40 air miles from the radar. The rawinsonde data was used to compute wind shear (from balloon motion) and gradient of refractive index for comparison with the radar results.

Fig. 1 contains plots of normalized backscattered power vs. altitude, and of windshear vs. altitude. The windshear is taken as the magnitude of the vector change in two adjacent wind values. The altitude increments for wind velocity vectors varied from one reading to another, but at 10,000 to 20,000 feet, the increments were about 500 feet. In plotting the windshear profiles, the data points were placed midway in each altitude increment.

Fig. 2 presents the results of tests where the backscattered power is compared to the gradient of refractivity squared. The gradient of refractivity was calculated on the basis of rawinsonde results and the ICAO standard atmosphere with 60% relative humidity.[2]

The initial results obtained here are such as to encourage further experimentation with high-powered radar. The technique should have application to determination of wind fields and rapid analysis of the atmosphere at high altitudes. Future experiments are being planned which will have as an objective the identification of the meteorological processes active in producing the echoes.

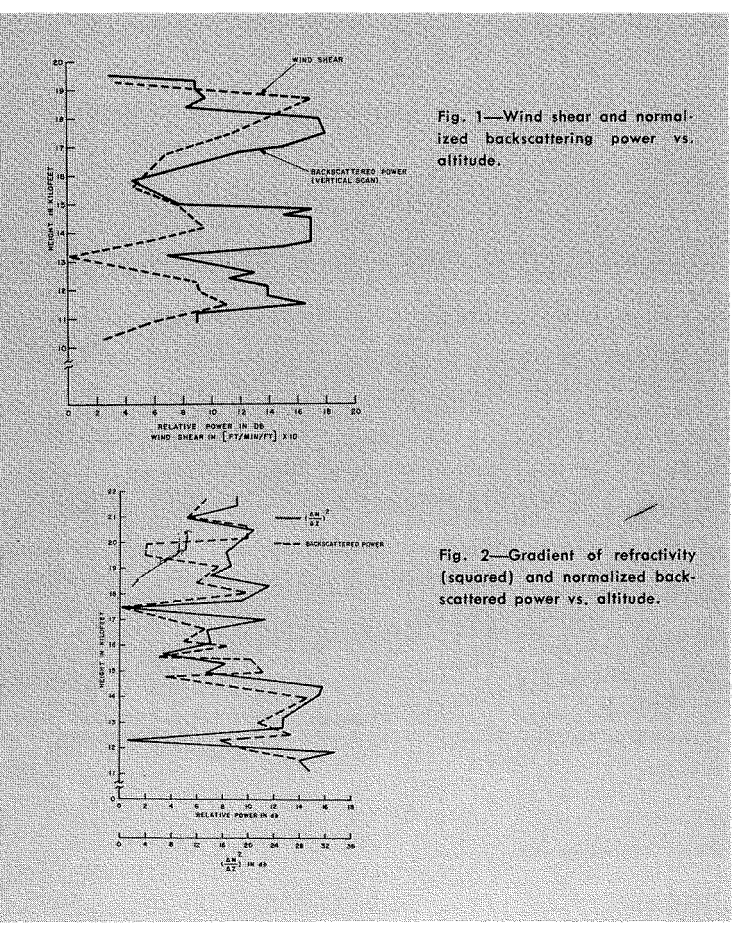


Fig. 1—Wind shear and normalized backscattering power vs. altitude.

Fig. 2—Gradient of refractivity (squared) and normalized backscattered power vs. altitude.

1. H. G. Booker and W. E. Gordon, "A Theory of Radio Scattering in the Troposphere," *Proc. IRE*, Vol. 38, pp. 401-412, April 1960.
2. B. R. Bean, "The Radio Refractive Index of Air," *Proc. IRE*, Vol. 50, No. 3, pp. 260-272, March 1962.

Technical Papers Interest Survey

C. W. FIELDS
Surface Communications Division DEP, Camden, N.J.*

We conducted a survey among the authors of technical papers in the Surface Communications Division on the degree of interest generated by the publication and presentation of papers. The survey covered the period from January 1961 through the first quarter of 1963. There were 90 papers applicable, meeting the criteria of presentation as a talk, or publication in a professional journal, or publication in a general technical magazine. For example, papers were given at the IEEE International Convention, published in the *Journal of the Acoustical Society of America*, and published in *Electronics* magazine.

There were several motivations for the survey: 1) to determine the extent to which technical papers publicize RCA capabilities, 2) to compile marketing leads and data, 3) to gauge the quality of SurfCom papers, and 4) to investigate relative merits of the media of presentation.

This is how we phrased the questionnaire: "Were any requests for information received as a result of presentation or publication of your paper? If so, indicate the number, source and nature of the inquiries."

About 95% of the questionnaires were filled in, albeit with a good deal of button-holing and file-searching; the only blanks resulted from authors having left the company.

The results showed that 70% of the papers elicited requests for reprints or further information and even purchase orders (three). The requests were from the U. S. Government—civil and military; industry; universities; institutes; foreign entities; and the technical press. The foreign requesters represented government, industry and universities in several European countries (including Czechoslovakia, Yugoslavia and Hungary) and Canada, Israel, India, Japan and Australia. The requesters represented a broad spectrum of occupations and functions: engineers, scientists, managers, technical academicians, marketing personnel, librarians, and technical press editors.

The nature of the information was generally requests for reprints,

*As of Sept. 1, 1963, renamed the *Communications Systems Division*.

but there were also queries on RCA products and facilities, where to buy, magazines wanting to give further treatment and invitations for the author to write another paper.

Here are some examples of the more popular papers:

1) "Practical Design Guides for Interference Reduction in Electronic Equipment," by R. F. Ficcki. Presented at the Fourth Annual Symposium of PGRFI, San Francisco, June, 1962 (79 requests).
2) "Chirp Signals for Communications," by M. R. Winkler of SurfCom, Tucson. Given at WESCON, Los Angeles, August, 1962. It elicited some 30 requests for copies of the paper and an Air Force inquiry about the RCA Tucson facility.
3) "Value Engineering" by A. D. Zappacosta. Published in *IRE Transactions on PGPEP and Armed Forces Management* (over 100 requests).
4) "Designing Tunnel-Diode Circuits Using Composite Characteristics," by B. Rabinovici and J. Klapper of SurfCom, New York. Published in *Electronics*, February, 1962. Queries came from Telefunken in Germany; Institute of Science, Rehovoth, Israel; Motorola; etc. (about 20 requests).

The most productive media for exposition of papers, in order of importance are: technical meetings, professional journals, and general technical magazines. (Any paper from SurfCom is placed in all three, where possible.) The most fruitful topic according to our survey was engineering or managerial techniques, e.g., RF shielding and value engineering, with the tunnel diode being the most popular product.

In Surface Communications Division, requests are being handled on a coordinated basis to insure that their potential as marketing leads is exploited, to insure that no proprietary information is released, to assure prompt and tactful response to the queries, to gauge trends as to what the rest of the electronics milieu is interested in, and to control release of information to foreign countries.

We conclude from the survey that the presentation and publication of papers pays off in the promotion of the company image and capabilities, and in the furtherance of the authors' professional reputations.

Acknowledgement: Credit is due Miss Martha Hertzberg, Ass't. Engineering Editor, SurfCom, for much of the research involved.

Generalized Distortion Analysis

by R. NOTO
Communications Systems Division
DEP, Camden, N.J.

Often, a design engineer needs to determine the distortion of an output function $f(t)$ with respect to the desired output function $g(t)$. The purpose of this *Note* is to provide the necessary general equations.

From the analyses described herein, it is concluded that: 1) It is not necessary to find a large number of the harmonic amplitudes in order to determine RMS distortion; definite integrals can be used instead. 2) The reference waveform need not be a sinusoidal function nor need it be periodic. 3) The usual definition for RMS distortion can be extended to nonperiodic and almost-periodic functions.

Distortion of a Periodic Function: The standard definition of RMS harmonic distortion for a periodic function $f(t)$, with respect to the fundamental component $g(t)$, is:

$$D = \frac{\sqrt{E_2^2 + E_3^2 + \ldots + E_n^2 + \cdots}}{E_1} \tag{1}$$

Where: $g(t) = E_1 \sin(\omega t + \psi_1)$ is the desired output waveform; $f(t) = E_o + E_1 \sin(\omega t + \psi_1) + \ldots + E_n \sin(n\omega t + \psi_n) + \cdots$ is the distorted output waveform, and D = RMS distortion.

Distortion with Respect to a Harmonic: Sometimes it may be necessary or desirable to determine distortion with respect to a function which is not the fundamental frequency. An example is the calculation of distortion in the output of an unbalanced full-wave rectifier with respect to the second harmonic of the input sine wave. To find the distortion with respect to a harmonic, Eq. 1 may be modified as follows:

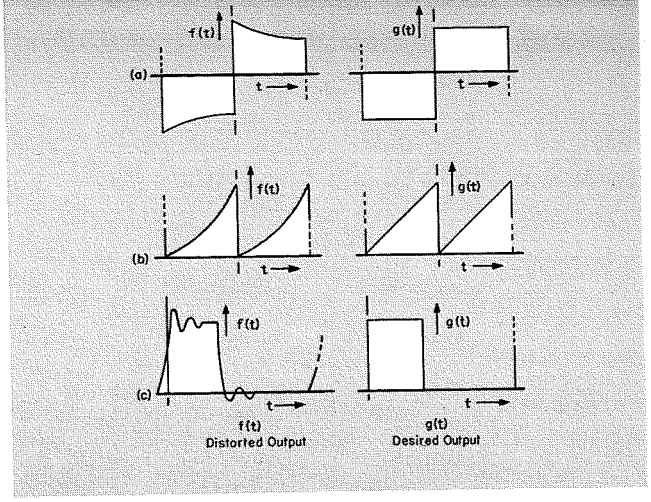


Fig. 1—Examples of distorted and desired outputs.

$$D = \frac{\sqrt{E_1^2 + E_2^2 + \ldots + E_{r-1}^2 + E_{r+1}^2 + \ldots + E_n^2 + \cdots}}{E_r} \tag{2}$$

Where: $g(t) = E_r \sin(r\omega t + \psi_r)$ is the desired output waveform; and $f(t) = E_o + E_1 \sin(\omega t + \psi_1) + E_2 \sin(2\omega t + \psi_2) + \ldots + E_r \sin(r\omega t + \psi_r) + \ldots + E_n \sin(n\omega t + \psi_n) + \ldots$ is the distorted output waveform.

Distortion of a Function $f(t)$ with Respect to a Function $g(t)$: To determine the distortion of $f(t)$ with respect to another function $g(t)$ it is first necessary to find the content (amplitude) of $g(t)$ in $f(t)$ by the following equation:

$$V = \frac{1}{NT}\int_d^{T+d} g(t)\, f(t)\, dt \tag{3a}$$

Where: $g(t)$ = given reference function; $f(t)$ = distorted output function; V = content of $g(t)$ in $f(t)$; T = period of $g(t)$; $d = 0$ or $-T/2$ (usually); and:

$$N = \frac{1}{T}\int_d^{T+d} [g(t)]^2\, dt \tag{3b}$$

The term N is the normalizing factor which makes V, in Eq. 3a equal to unity if $f(t) = g(t)$. Examples of values of N are: rectangular waveform, $N=1$; sine wave, $N = 1/2$; triangular wave, $N = 1/3$.

The difference in the average (or DC.) value of $f(t)$ and $g(t)$ is:

$$V_o = \frac{1}{T}\int_d^{T+d} [f(t) - g(t)]\, dt \tag{3c}$$

The RMS distortion is given by:

$$D = \sqrt{\frac{\frac{1}{T}\int_d^{T+d} [f(t)]^2\, dt - \frac{1}{T}\int_d^{T+d} V_o^2\, dt - \frac{1}{T}\int_d^{T+d} V^2\, [g(t)]^2\, dt}{\frac{1}{T}\int_d^{T+d} V^2\, [g(t)]^2\, dt}} \tag{4a}$$

If T is not infinite, if the difference of the average value of $f(t)$ and $g(t)$ is zero ($V_o = 0$) and usnig Eq. 3b; Eq. 4a reduces to:

$$D = \sqrt{\frac{\int_d^{T+d} [f(t)]^2\, dt}{V^2 NT} - 1} \tag{4b}$$

By inspection of Eq. 1 and 2, distortion is actually the square root of the total power of $f(t)$ minus the power of the reference, $g(t)$, minus the power of the difference of the average values of $f(t)$ and $g(t)$, divided by the square root of the power of the reference, which corresponds to Eq. 4. A proof that Eq. 4 will reduce to Eq. 1 or 2 for an arbitrary complete orthogonal set of functions, such as the Fourier series, of which $g(t)$ is a member, is similar to that used to establish the Fourier series. Substituting the general series

expansion for $f(t)$ as a function of the orthogonal set, squaring and integrating over the period T will reduce Eq. 4 to 1 or 2. Eq. 3 and 4 are general and can be used as a definition of distortion of any function $f(t)$ with respect to any other function $g(t)$. The period, T, can approach infinity in the limit in Eq. 4a in the case of nonperiodic functions, whenever the functions are integrable square. Examples of the type of functions for which distortion may be easily calculated are shown in Fig. 1.

Advantages of Integral Representation: Use of Eq. 3 and 4 for calculation of RMS distortion for periodic functions with respect to a sinusoidal reference rather than Eq. 1 or 2 is easier and more accurate than finding all of the (Ej)'s of Eq. 1 or 2. It is easier because it is only necessary to calculate the content of one member of a complete set of orthogonal functions rather than the content of a large number of members of the infinite set. There is some error introduced in Eq. 1 and 2 if significant higher-order harmonics of the Fourier-series expansion are neglected, whereas the definite integral is exact.

Time Delay of Reference Waveform: If the reference function $g(t)$ does not have the same time delay as the distorted function $f(t)$, or if the delay is not known or given, it is necessary to find the value of τ which will give the greatest maximum content of $g(t)$ in $f(t)$ and to use $g(t+\tau)$ rather than $g(t)$ as the reference waveform. In the case where $g(t)$ is a sinusoidal function, Fourier series may be used and the amplitude of $g(t)$ in $f(t)$ will be:

$$E_r = \sqrt{a_r^2 + b_r^2}$$

And: $E_r\, g\,(t+\tau) = E_r \sin\left(\frac{2r\pi t}{T} + \tau\right)$

Where: a_r and b_r are defined by Fourier series.

Distortion of Almost-Periodic Functions with Respect to a Sinusoidal Reference: Examples of almost-periodic functions are ocean tides and narrowband noise. If the integrals in Eq. 3 and 4 do not exist for an infinite period, no calculation over a finite range can yield an exact answer for distortion of an almost-periodic function. However, if $g(t)$ is a sine wave, the error in Eq. 4, when restricting $f(t)$ to a finite range, will usually decrease as the integration extends over more and more cycles of $g(t)$. Effects of departures from true periodicity of $f(t)$ tend to cancel. The integration range will be controlled by the nature of $f(t)$ with respect to $g(t)$ and the required accuracy. Normally, all of the function $f(t)$, as given, should be used.

Acknowledgement: M. S. Corrington, of DEP Applied Research, Camden, contributed many helpful suggestions for the generalized analysis.

An Improved High-Speed Compare Circuit With Parallel, Instantaneous Operation

by H. WEINSTEIN
RCA Laboratories, Princeton, N. J.

The approach to a *compare* circuit described herein features a *compare* operation that is parallel and instantaneous in nature. It is hoped that the suggested scheme may offer substantial improvement in high-speed data-processing systems.

Consider the following two binary numbers:

$$a_n 2^n + a_{n-1}2^{n-1} + \ldots + a_i 2^i + \ldots + a_1 2' + a_o$$

$$b_n 2^n + b_{n-1}2^{n-1} + \ldots + b_i 2^i + \ldots + b_1 2' + b_o$$

Where: All a and b may assume either one of the two possible values *0* or *1*. Let it be required to construct a system that will find out which one of the two numbers is larger than the other. A conventional way of doing this is by subtracting one number from the other, and since they are fed into known locations, the sign bit will determine which number is larger. In computer language, this procedure involves *two* addition operations (the first one exercised for complementing).

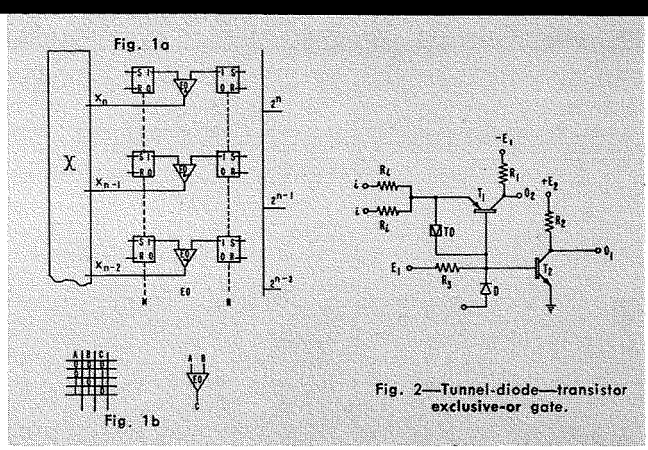


Fig. 2—Tunnel-diode—transistor exclusive-or gate.

Another way of determining which number is larger suggests itself: Select the first *bit* in which the two numbers differ. By *first*, we mean the one obtained when we travel in the direction from the most-significant bit (a_n, b_n) towards the least-significant bit (a_o, b_o). For example:

$$\begin{array}{r} \\ *\\ \\ \end{array} \begin{array}{l} 1\,1\,0\,1\,0\,0\,1\,0 = M \\ \longrightarrow \\ 1\,1\,1\,0\,1\,0\,1\,0 = N \end{array}$$

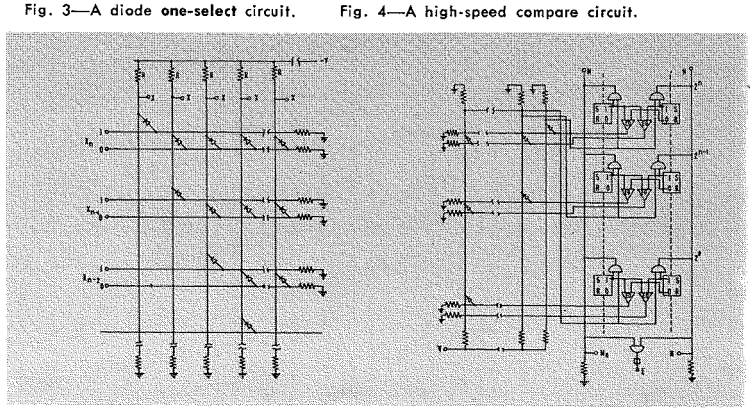
Here, the first bit in which M and N differ is marked by * (associated with 2^5 power). When such a point is reached, we do not need to travel any further down the digit rows, since *we can immediately determine which number is larger by noting which row has the 1 in it, as opposed to the other which has the 0 in it.* To perform this operation simultaneously, consider Fig. 1a. Here, M and N are assumed to be temporarily stored in two registers, whose elements may be, for example, conventional flip-flops. The *1* outputs of the pairs of flip-flops which correspond to equal powers of two are fed into *EO* gates, which are simply *exclusive or* gates (sum modulo two), whose description is given in Fig. 1b. A rapid tunnel-diode–transistor *exclusive or* gate with inputs i_1, i_2 and output *0*, is illustrated in Fig. 2. (This circuit will deliver 100 ma in approximately 15 nsec.) However, the system is not restricted to any particular gate realization. (This gate was developed by J. J. Amodei.) The output of the *EO* gates will thus be enabled (*1*) whenever two corresponding digits differ, and will be disabled (*0*) whenever the corresponding digits are alike. The outputs of the *EO* column are now fed into a system X, which now is required to yield a single pulse, corresponding to the first digit in which the numbers differ (closest to the most significant bit).

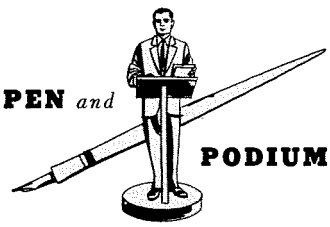
A possible circuit for X is illustrated in Fig. 3. A diode *one select* matrix with *and* operation along the columns, and which assumes all x_i to be available with their complements, always selects the uppermost response.

The combined circuit is shown in Fig. 4. Here, two *EO* gates per bit are associated with registers M and N to yield complementary inputs to the diode *one select* circuit. When a single, unique response is obtained from the diode circuit, it is fed into a corresponding pair of *and* gates. As shown, the only gate that will be enabled is connected to a flip-flop in the set state (i.e., storing the digit *1*.) This, in turn, will enable either output M_o, or output N_o, which are associated with the words M or N respectively. The larger binary number is thus selected. An equality is indicated on terminal E.

Fig. 3—A diode one-select circuit.

Fig. 4—A high-speed compare circuit.





AS REPORTED BY YOUR TECHNICAL PUBLICATIONS ADMINISTRATOR

RCA LABORATORIES

Electronic Room Acoustic Fundamentals—J. E. Volkmann: ASA Meeting in N. Y. C., May 15-18, 1963

Procedures for Efficient Problem Solving by Machine—S. Amarel: Symposium on Computer and Data Processing, Denver, Colorado, June 26-27, 1963

New Advances in Passive Telemetering Implants—V. K. Zworykin, L. E. Flory and F. L. Hatke: National Telemetering Conference, Albuquerque, New Mexico, May 20, 1963

Ferroelectricity in SbSI and Other V-VI-VII Compounds—W. J. Merz and R. Nitsche: Symposium on Ferromagnetism and Ferroelectricity, Leningrad, May 1963

Harmonic Generation Mixing and Detection of Millimeter and Submillimeter Waves Using Parametric or Tunnel Diodes—K. K. N. Chang: 1963 PGMTT National Symposium, Santa Monica, Calif., May 20-22, 1963

The Theoretical Performance of a Diversity Combining System with AGC-Weighted Combining—F. I. Zonis: University of Penna. *Master's Degree Thesis*, May 3, 1963

Review of paper "Flux Reversal in Three-Rung Laddic" by J. A. Baldwin, Jr.—G. R. Briggs: *IEEE Transactions on Electronic Comp.*, May-June 1963

The Growth of Single Crystal Gallium Layers on Germanium Substrates—J. A. Amick: Conference on Single Crystal Films, Blue Bell, Pa., May 13-15, 1963

Ultimate Limits of Microelectronics—J. T. Wallmark: Conference on the Impact of Microelectronics, Armour Research Foundation and *Electronics*, Chicago, June 26-27, 1963

Double-Stream Amplification with Fast-Wave Coupling—B. Vural: 21st Annual Conference on Electron Device Research, University of Utah, June 26-28, 1963

Mechanism of the Flexode: Field-Aided Lithium Precipitation in Germanium—J. Blanc, J. O. Kessler and M. S. Abrahams: IEEE Conference on Solid Devices, East Lansing, Michigan, June 12-14, 1963

Electronic Synthesis of Music—H. F. Olson: Acoustical Society of America, Hotel New Yorker, May 16, 1963

Theory of Serial Codes—J. R. Macy: Thesis: Stevens Institute of Technology—*Doctoral Dissertation*, May 8, 1963

Review of Experimental Evidence Supporting the Shockley Model in Epitaxial Heterojunctions—S. S. Perlman and R. M. Williams: Solid State Device Conference, Michigan State Univ., East Lansing, Mich., June 21, 1963

Gallium Arsenide Materials and Laser Emission—J. I. Pankove: NAECON, Dayton, Ohio, May 13, 1963

Feasibility of Neuristor Laser Computer—W. F. Kosonocky: NAECON Session; Electronics Aspects in Bionics—W. F. Kosonocky, Dayton, Ohio, May 13, 1963

RCA Microelectronic Device Research and Development—T. O. Stanley and R. D. Lohman: DOD-AGED Microelectronic Device Conference, Durham, N. C., May 21, 1963

Three-and Four-Level Solid-State Laser—J. P. Wittke: New York University Lecture, June 17, 1963

The Electron Microscope: A Survey of the Instrument and Its Uses—G. W. Neighbor: New Jersey Chapter of the Society of Photographic Instrumental Engineers, New Brunswick, N.J., May 23. 1963

Theory of the Stimulated Emission of Radiation—H. R. Lewis: New York Univ. Lecture, June 17, 1963

Optical Maser Systems Utilizing the Fluoride Hosts—Z. J. Kiss: New York Univ. Lecture, June 19, 1963

A Coplanar-Electrode Insulated-Gate Thin-Film Transistor—P. K. Weimer, F. V. Shallcross, H. Borkan: Solid State Device Research Conference, East Lansing, Mich., June 12, 1963

Unconditional Stability in Tunnel-Diode Amplifiers—A. S. Clorfeine: *RCA Review*, March 1963

The Crystal Structure of Tetramethylammonium Mercury Tribromide $N(CH_3)_4HgBr_3$—J. G. White: *Acta Crystallographica*, May 1963

Crystal Field Splitting in $CaF_2:Nd^{3+}$—Z. J. Kiss: *Journal of Chemical Physics*, April 1, 1963

Observation of Paramagnetic Resonance Centers in GaAs in Unusually High Concentrations—B. Goldstein and N. Almeleh: *Applied Physics Letters*, April 1, 1963

The Range of Hot Electrons and Holes in Metals—J. J. Quinn: *Applied Physics Letters*, May 1, 1963

Laser-Induced Emission of Electrons Ions and Neutral Atoms from Solid Surfaces—R. E. Honig and J. R. Woolston: *Applied Physics Letters*, April 1, 1963

Redundancy in Unipolar Field-Effect Transistor Circuits—by J. T. Wallmark and A. G. Revesz: *IEEE Transactions on Electronic Computers*, February 1, 1963

High-Speed Arithmetic Employing Tunnel Diodes—H. S. Miller, *RCA Review*, Mar. 1963

An Electron-Beam Machine—A. B. El-Kareh: *RCA Review*, Mar. 1963

High-Field Study of a Hall-Effect Microwave Converter—K. K. N. Chang and R. D.

DATES *and* DEADLINES

PROFESSIONAL MEETINGS AND CALLS FOR PAPERS

Meetings

Sept. 15-19, 1963: 5TH NATL. ELECTRICAL INSULATION CONF., IEEE-NEMA; Conrad Hilton Hotel, Chicago, Ill. *Prog. Info.:* J. Swiss, Westinghouse Elec. Corp. Res. Labs., Pittsburgh 35, Pa.

Sept. 18-19, 1963: 12TH ANN. INDUSTRIAL ELECTRONICS SYMP., IEEE-ISA; Kellogg Center, Michigan State Univ., E. Lansing, Mich. *Prog. Info.:* Henry Patton, Acromag Inc., Detroit, Mich.

Sept. 20-21, 1963: 11TH ANN. CONF. ON COMMUNICATIONS (MICRO-ELECTRONICS), Cedar Rapids Sec.; Roosevelt Hotel, Cedar Rapids, Iowa. *Prog. Info.:* D. E. Loop, Collins Radio Co., Cedar Rapids, Iowa.

Sept. 24-27, 1963: INTL. TELEMETERING CONF., IEEE-ISA-AIAA-IEE; Savoy Place and London Hilton Hotel, London, England. *Prog. Info.:* L. L. Rauch, Univ. of Mich., Dept. of Aero Eng., Ann Arbor, Mich.

Sept. 30-Oct. 2, 1963: CANADIAN ELECTRONICS CONF., Region 7; Automotive Bldg., Exhibition Park, Toronto, Ont. Canada. *Prog. Info.:* Dr. J. L. Yen, Dept. of EE, Univ. of Toronto, Toronto, Ont., Canada.

Oct. 1-3, 1963: 8TH NATL. SYMP. ON SPACE ELECTRONICS, PTG-SET; Fontainebleu Hotel, Miami Beach, Fla. *Prog. Info.:* H. N. Upthegrove, Bell Tel. Labs., Whippany, N.J.

Oct. 4-5, 1963: 13TH ANN. BROADCAST SYMP., PTG-B; Willard Hotel, Washington, D.C. *Prog. Info.:* S. Bergen, 103 Fairchester Dr., Fairfax, Va.

Oct. 7-9, 1963: 9TH NATL. COMMUNICATIONS SYMP., PTG-CS; Hotel Utica, Utica, N.Y. *Prog. Info.:* Dr. J. Ryerson, Dir. of Center, Griffiss Air Force Base, New York. Communications, Rome Air Development

Oct. 8-11, 1963: INTL. CONF. ON ELECTROMAGNETIC RELAYS, ICER, Tohoku Univ., IEEE, IEE, et. al.; Tohoku Univ., Sandai, Japan. *Prog. Info.:* C. F. Camerson, School of Eng., Oklahoma State Univ., Stillwater, Okla.

Oct. 21-23, 1963: E. COAST CONF. ON AEROSPACE AND NAVIGATIONAL ELECTRONICS (ECCANE), PTG-ANE, Baltimore Sec.; Emerson Hotel, Baltimore, Md. *Prog. Info.:* Richard Allen, Martin-Marietta Corp., Baltimore 3, Md.

Oct. 28-30, 1963: NATL. ELECTRONICS CONF., IEEE and others; McCormick Place, Chicago, Ill. *Prog. Info.:* Dr. H. W. Farris, E. E. Dept., Univ. of Mich., Ann Arbor, Mich.

Oct. 29-31, 1963: 10TH ANN. MTG. PTG-NS INTL. SYMP. ON PLASMA PHENOMENA AND MEAS., PTG-NS; El Cortez Hotel, San Diego, Calif. *Prog. Info.:* Robert DeLosh, Bendix Systems Div., Ann Arbor, Mich.

Oct. 31-Nov. 1, 1963: 1963 ELECTRON DEVICES MTG., PTG-ED; Sheraton-Park Hotel, Washington, D.C. *Prog. Info.:* Mason Clark, Hewlett-Packard Assoc., Palo Alto, Calif.

Nov. 4-6, 1963: NEREM (NORTHEAST RES. AND ENG. MTG.), Region 1; Commonwealth Armory, Somerset Hotel, Boston, Mass. *Prog. Info.:* A. O. McCoubrey, c/o Boston Sec., IEEE, 313 Wash. St., Newton, Mass.

Nov. 10-15, 1963: 9TH ANN. CONF. ON MAGNETISM AND MAGNETIC MATLS., PTG-MTT-IEEE-AIP; Chalfonte-Haddon Hall, Atlantic City, N.J. *Prog. Info.:* C. J. Kriessman, Physics, Matls. and Processes Sec., Box 500, Blue Bell, Pa.

Nov. 11-13, 1963: RADIO FALL MTG., IEEE-EIA; Hotel Manager, Rochester, N.Y. *Prog. Info.:* V. M. Graham, EIA Eng. Dept., 11 W. 42nd St., N.Y.

Nov. 12-15, 1963: 9TH ANN. CONF. ON MAGNETISM AND MAGNETIC MATLS., PTG-MTT-IEEE-AIP; Chalfonte-Haddon Hall, Atlantic City, N.J. *Prog. Info.:* W. L. Shevel, Jr., IBM Mag. Res. Dept., Yorktown Heights, N.Y.

Nov. 12-14, 1963: FALL JOINT COMPUTER CONF., AFIPS (IEEE-ACM); Las Vegas Convention Center, Las Vegas, Nev. *Prog. Info.:* Paul Davies, Abacus, Inc., 1718-21 St., Santa Monica, Calif.

Calls for Papers

Feb. 19-21, 1964: INTL. SOLID-STATE CIRCUITS CONF., IEEE-Univ. of Pa.; Sheraton Hotel and Univ. of Pa., Philadelphia, Pa. *DEADLINE:* Abstract, **11/1/63.** to: Howard Parks, Martin Co., R and AT Dept., Mail 683, Baltimore 3, Md.

Feb. 26-28, 1964: NINTH SCINTILLATION AND SEMICONDUCTOR COUNTER SYMP., IEEE; Hotel Shoreham, Washington, D.C. *DEADLINE:* Abstracts, **12/1/63.** to: W. A. Higinbotham, Chairman, Prog. Committee, Brookhaven Natl. Laboratory, Upton, L.I., N.Y.

March 23-26, 1964: IEEE INTL. CONVENTION, All PTG's; Coliseum and N.Y. Hilton, New York, N.Y. *DEADLINE:* Submit by **Oct. 18, 1963,** the following: 1) A statement, in quadruplicate, of why the paper should be presented; 2) 100-wd. abstract, quadruplicate; 3) 500-wd. summary, quadruplicate; 4) Indicate how your paper should be classified: a) *Basic Sciences and Techniques;* b) *Power;* c) *Industry and Industrial Applications;* d) *Communications;* e) *Electronic Systems;* f) *Computers and Data Processing;* g) *Instrumentation;* h) *Materials, Components, and Production Processes;* i) *Bio-Medical Electronics;* j) *Professional Activities.* Send all to: Dr. F. Hamburger, Jr., Chairman, 1964 Tech. Prog. Committee, The Institute of Electrical and Electronics Engineers, Inc., Box A, Lenox Hill Station, New York 21, N. Y.

Apr. 1-2, 1964: 5TH SYMP. ON ENG. ASPECTS OF MAGNETOHYDRODYNAMICS, IEEE-AIAA, MIT; MIT, Cambridge, Mass. *For Deadline Info.:* Dr. G. S. Janes, Avco Everett Res. Labs., Everett 49, Mass.

Apr. 6-9, 1964: INTL. CONF. ON NONLINEAR MAGNETICS (INTERMAG), IEEE; Shoreham Hotel, Washington, D.C. *For Deadline Info.:* W. L. Shevel, Jr., IBM Mag. Res. Dept., MRD 807, Box 218, Yorktown Heights, N.Y.

Apr. 8-10, 1964: ISA MEASUREMENT AND CONTROL INSTRUMENTATION DIVISION SYMP., with District III Exhibit; Hotel Floridian, Tampa, Fla. *DEADLINE:* Abstracts, approx. **12/1/63.** to: J. Barker, Taylor Instrument Companies, P.O. Box 13735, Station K, Atlanta 24, Georgia.

Apr. 19-25, 1964: INTL. CONF. AND EXHIBIT ON AEROSPACE ELECTRO-TECHNOLOGY, IEEE, et. al.; Westward-Ho Hotel, Phoenix, Ariz. *DEADLINE:* Abstracts, **8/19/63,** Manuscripts, **11/1/63.** to: E. E. McLellan, Motorola Inc., 8201 E. McDowell Rd., Scottsdale, Ariz.

Apr. 21-23, 1964: SPRING JOINT COMPUTER CONF., AFIPS (IEEE-ACM); Sheraton-Park Hotel, Wash., D.C. *DEADLINE:* Manuscript, approx. **11/10/63.** to: Jack Roseman, 2313 Coleridge Dr., Silver Spring, Md.

Apr. 22-24, 1964: SOUTHWESTERN IEEE CONF. AND ELEC. SHOW (SWIEEECO); Region 5; Dallas Memorial Auditorium, Dallas, Tex. *DEADLINE:* Abstracts (approx. **10/1/63.** to: Richard A. Arnett, Tex. Instruments, Inc., P.O. Box 35084, Dallas, Texas.

May 4-6, 1964: 10TH NATL. ISA AEROSPACE INSTRUMENTATION SYMP., ISA; Biltmore Hotel, New York City. *DEADLINE:* Abstracts, approx. **1/1/64.** to: J. K. Stotz, Jr., Grumman Aircraft Eng. Corp., Bethpage, Long Island, New York.

May 5-7, 1964: ELECTRONIC COMPONENTS CONF., IEEE-EIA; Marriott Twin Bridges Hotel, Wash., D.C. *DEADLINE:* Abstracts, approx. **10/9/63.** to: John Bohrer, IRC, 401 N. Broad St., Phila. 8, Pa.

May 11-13, 1964: NAECON (NATL. AEROSPACE ELECTRONICS CONF.), PTG-ANE Dayton Sec., AIAA; Biltmore Hotel, Dayton, Ohio. *DEADLINE:* Abstracts, approx. **12/1-15/63.** to: IEEE Dayton Office, 1414 E. 3rd St., Dayton, Ohio.

May 19-21, 1964: INTL. SYMP. ON MICROWAVE THEORY AND TECHNIQUES, PTG-MTT; Intl. Inn, Intl. Airport, Idlewild, N. Y. *DEADLINE:* Abstracts, approx. **1/8/64.** to: Dr. L. Swern, Sperry Gyroscope Co., 3 T 105, Great Neck, N. Y.

May 25-28, 1964: 13TH NATL. TELEMETERING CONF., ISA, AIAA, IEEE; Biltmore Hotel, Los Angeles, Calif. *DEADLINE:* Abstracts, approx. **1/1/64.** to: A. P. Gruer, 7530 Sandia Corp., Box 5800, Albuquerque, New Mexico.

June 1964: 2ND NATL. ISA BIOMEDICAL SCIENCES INSTRUMENTATION SYMP.; New Orleans, Louisiana. *DEADLINE:* Abstracts, approx. **2/1/64.** to: Dr. R. Jonnard, The Prudential Insurance Co. of America, Newark, N. J.

June 19-21, 1964: 5TH ANN. JOINT AUTOMATIC CONTROL CONF., ISA, AIChE, ASME, IEEE; Stanford Univ., Stanford, Calif. *DEADLINE:* Abstracts, approx. **2/1/64.** to: D. A. Rodgers, Consolidated Systems Corp., 1500 Shamrock Ave., Monrovia, Calif.

Aug. 25-28, 1964: WESCON SHOW AND IEEE SUMMER GENL. MTG., Region 6, WEMA, All PTG's; Los Angeles, Calif. *DEADLINE:* Abstracts, approx. **4/15/64.** to: WESCON, 3600 Wilshire Blvd., Los Angeles, Calif.

Sept. 7-11, 1964: INTL. CONF. ON MICROWAVES, CIRCUIT THEORY AND INF. THEORY, IECE of Japan, et. al.; Tokyo, Japan. *For Deadline Info.:* Dr. K. Morita, Oki Elec. Indus. Co., Ltd. 1, 4 Chome, Nishi-Shibaura, Minato-Ku, Tokyo.

Sept. 22-24, 1964: PTG ON ANTENNAS AND PROPAGATION SYMP., PTG-AP; Long Island, N. Y. *DEADLINE:* Abstracts, **3/1/64.** to: H. Jasik, Jasik Labs., 100 Shames Dr., Westbury, N. Y.

Be sure DEADLINES are met — consult your Technical Publications Administrator for lead time needed to obtain required RCA approvals.

Hughes: *Journal of Applied Physics*, Apr. 4, 1963

Measurements of the Density of GaAs—L. R. Weisberg and J. Blanc: *Journal of Applied Physics*, Apr. 4, 1963

The Neuristor Laser Computer—W. F. Kosonocky: RCA Labs., Princeton, N. J.

Photoconductivity Performance in Large Single Crystals of Cadmium Sulfide—A. B. Dreeben and R. H. Bube: *Journal of the Electrochemical Society*, May 1963

Magnetic Memories—Capabilities and Limitations—J. A. Rajchman: *Journal of Applied Physics*, Apr. 1963

Absorption Spectrum of Germanium and Zinc-Blende-Type Materials at Energies Higher than the Fundamental Absorption Edge—M. Cardona and G. Harbeke: *Journal of Applied Physics*, Apr. 4, 1963

Conditions Existing at the Onset of Oscillator Action—R. D. Larrabee: *Journal of Applied Physics*, Apr. 4, 1963

Duo-Emitter Diode—K. G. Hernqvist and J. R. Fendley, Jr.: *Journal of Applied Physics*, Apr. 4, 1963

Switching Properties of a Single-Crystal Specimen of Nickel Ferrite—J. C. Miller and R. C. Barker: *Journal of Applied Physics*, Apr. 4, 1963

Proton-Induced Lattice Displacements in Silicon—J. A. Baicker, H. Flicker and J. Vilms: *Applied Physics Letters*, Mar. 1963

Thermoelectric Behavior in N-Type Ge-Si Alloys in the "Overlap" Region—A. Smith: APS Solid State Meeting, Mar. 1963

A Markov Chain Model of Adaptive Signal Detection—J. Sklansky: Bionics Symposium, Dayton, Ohio, Mar. 19-21, 1963

The Behavior of Electrons in Strong Crossed Electric and Magnetic Fields—M. Glicksman and W. Hicinbothem: American Physical Society Meeting, St. Louis, Mo., Mar. 25-28, 1963

Evaporated Metal Contacts to Conducting Cadmium Sulfide Single Crystals—A. M. Goodman: Physical Society Meeting, St. Louis, Mo., Mar. 24-27, 1963

Diffusion Length Measurement in InP—H. Flicker: Physical Society Meeting, St. Louis, Mo., Mar. 24-27, 1963

Magnetic Field Dependence of the Microwave Surface Impedance of Nb_3Sn—M. Cardona, G. Fischer and B. Rosenblum: APS Meeting, St. Louis, Mo., Mar. 25-28, 1963

Thermal Conductivity of InAs and Other III-V Compounds at High Temperatures—E. F. Steigmeier and I. Kudman: American Physical Society, Wash. D. C., Apr. 22, 1963

Recent Band Structure Determinations of Semiconductors from Optical Measurements—G. Harbeke: Semiconductor Meeting of German Physical Society, Bad Pyrmont, Germany, Apr. 1963

Fundamental Reflectivity of PbS, PbTe and PbSe—D. L. Greenaway: Semiconductor Meeting of German Physical Society, Bad Pyrmont, Germany, Apr. 1963

Laser-Induced Emission of Neutrals, Electrons and Ions from Solid Surfaces—R. E. Honig and R. Woolston: Electrochemical Society Meeting, Pittsburgh, Pa., Apr. 15-16, 1963

Polarization Processes in $BaTiO_3$—W. J. Merz: Meeting on "Dielektrika" of German Society for Communications, Aachen, Germany, Apr. 25-26, 1963

Self-Magnetoresistance Effect in Bismuth—T. Hattori and M. C. Steele: Physical Society of Japan Meeting, Apr. 1963

Direct Observation of Self-Pinched Plasma Distributed in Indium Antimonide—M. Toda: Physical Society of Japan Meeting, Apr. 1963

Optical Masers—The State of the Art—R. J. Pressley: Forrestal Electronics Seminar, Mar. 1, 1963

Extraction of High-Density Electron Beams from Synthesized Plasmas—A. L. Eichenbaum and H. Sobol: 23rd Annual Conference on Physical Electronics, MIT, Cambridge, Mass., Mar. 21-23, 1963

The Role of the Engineer in an Electronics Laboratory—H. Borkan: Rutgers University, Student Branch, IRE, Mar. 20, 1963

Surface Decoration and Domains in Very Thin Magnetic Films—M. D. Coutts: New York Society of Electron Microscopy, N. Y., Mar. 21, 1963

Optical Spectra of Divalent Rare Earth Ions in Crystals—D. S. McClure and Z. J. Kiss: Polytechnic Institute of Brooklyn Symposium on Optical Masers, Apr. 16-18, 1963

Thermal Conductivity of InAs and Other III-V Compounds at High Temperatures—E. Steigmeier and I. Kudman: Washington Meeting of the American Physical Society, Apr. 22-25, 1963

Zeeman Tunning Internal Modulation and High Rep-Rate Q Switching of the $CaF_2:Dy^{2+}$ Maser—Polytechnic Institute of Brooklyn Symposium on Optical Masers, Apr. 16-18, 1963

Instrumentation in Nanosecond Technology—B. J. Lechner: Spring Lecture Series of New York City Section of IEEE Western Union Auditorium, N. Y.

NATIONAL BROADCASTING COMPANY

Systems Considerations in Color Equipment Installation—J. L. Wilson: NAB Convention, Chicago, Ill., April 2, 1963

RF Interference Reduction in Television Pickups—J. L. Hathaway: NAB Convention, Chicago, Ill., April 3, 1963

Color Television Camera Matching Techniques—E. P. Bertero: SMPTE Convention, Atlantic City, N. J., April 25, 1963

in the United States—N. Grant: 3rd International Television Symposium, Montreux, Switzerland, April 26, 1963

DEFENSE ELECTRONIC PRODUCTS

The Importance of Company Standards—M. S. Gokhale: United Nations, N. Y.

Magnetic Shielding by Persistent Currents of Vapor-Deposited Niobium Stannide Cylinders—J. P. McEvoy: APS Meeting, Stanford University

MERT, The Manpower Evaluation and Review Technique—P. W. Coben: AIIE Conference, June 10, 1963

Effective Utilization of Resources—C. Fallon: IEI Skill Training Value Eng. Course, April 29-30, May 1, 2, 3, 1963

Value Engineering Presentation (Mathematical Portions)—C. Fallon: USAF School of Systems & Logistics, May 15, 1963

Mathematical Techniques in Value Engineering and Management Decision-Making—C. Fallon: Monsanto Chemical Company Mtg., May 20, 1963

High Resolution Lunar Measurement—W. O. Mehuron: 15th National Aero-space Electronics Conference—NAECON, May 13, 1963

Adaptive Decommutation Ground Station with Computer Control—J. A. Bauer: National Telemetry Conference, May 22, 1963, *NTC Proceedings.*

TRADEX—The Second Generation of Super Power UHF Transmitter—R. Graham, Jr.: National PGMTT Symposium, May 20-22, 1963

Antenna Systems for the Project Relay Communications Satellite—O. M. Woodward: Los Angeles Chapter of the PGMTT & PCAP, April 4, 1963

Fads and Fallacies of Reliability Creation—G. H. Beckhart: ASQC National Convention, May 22, 1963

Radar Tracking of Objects with Low Signal/Noise Using Video Integration—L. J. Clayton: *Thesis*, Master of Science in Electrical Engineering, University of Penna.

RCA Techniques in Electronic Photocomposing—H. E. Haynes: Annual Meeting of TAGA, New York City, June 4, 1963

Flux Logic Elements for Use in Digital Computer memories—M. V. D'Agostino: *MSEE Thesis*, Drexel Inst. of Technology, June, 1963

Analysis of the Effectiveness of a Controlled Environment Facility in the Electronics Industry—M. J. Munkacsy: *MBA Thesis*, Drexel Institute of Tech., June, 1963

Shock Spectrum Analysis of Electronic Equipment—E. Westcott: *MSEE Thesis*, Drexel Inst. of Technology, June, 1963

Micromodule Ejection Made Easy—G. Rezek: *Electronic Equipment Engineering*, June, 1963

Five-Layer Diode Guards Cables—H. R. Montague: *Electronics*, June 21, 1963

What is a Standards Engineer?—M. S. Gokhale: Standards Engineers Society, Steering Committee, Bombay Section, Bombay, India, Apr. 23, 1963

Technical Training—Twin Star of Technical Writing—S. Hersh: *Review of Society of Technical Writers and Publishers*, Jan. 1963

Digital Computers and Integrated Displays for Air Traffic Control—C. Fanwick: Panel Member, Meeting San Fernando Valley Chapter, Association of Computing Machinery, Jan. 16, 1963

PERT—H. R. Headley: AIEE, Apr. 23, 1963

Circuit Considerations and Operational Results of a Permalloy Sheet Memory—M. V. D'Agostino and C. H. Sie: International Conference on Non-Linear Magnetics, Washington, D. C., Apr. 17, 1963

Topological Analysis of Non-Series-Parallel Redundant Networks—G. D. Weinstock: IEEE International Convention, N. Y., Mar. 25, 1963. *Convention Record*

Thermal Analysis and Analog Representation of a Thermoelectric Refrigerator—G. Rezek: IEEE International Convention, N. Y., Mar. 28, 1963. *Convention Record*

Interference Reduction in Cable—R. F. Ficcki: 1963 IEEE International Convention, Mar. 28, 1963, N. Y. *Convention Record*

Technical Future of Satellite and Space Programs—H. M. Gurk: Princeton Adult School Series, Mar. 21, 1963

Thermal Control of Spacecraft—G. D. Gordon: Northern N. J. Section, AAS Meeting, Apr. 2, 1963

Measurement of Magnetic Multiple Singularities by Field Mapping—R. Moskowitz: Faculty and Graduate Students of School of Elec. Engineering, Rutgers Univ., Apr. 4, 1963

Advanced Defense System Simulator—A. Bezgin/E. J. Hartnett: Master of Science *Thesis*, University of Penna.

A Study of an Earth-Moon-Earth Radio Frequency Communications System—J. G. Kammerer: Master *Thesis*, Moore School of Electrical Engineering, Univ. of Penna.

Design of a Satellite Information Processing Program—T. A. Dorsay: Master *Thesis*, Moore School of Electrical Engineering, University of Penna.

Application of Monte Carlo Technique to Determine Statistical Performance of Radar Networks Engaged in Satellite Surveillance—A. E. Franz: Master *Thesis*, Moore School of Electrical Engineering, Univ. of Penna.

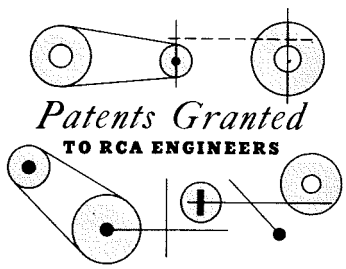
Statistical Analysis of a Pseudo-Random Coded Pulsed Radar Applied to Radar Astronomy—I. Marion: *Ph.D. Dissertation*, Univ. of Penna.

A Study of Certain Aspects of Lunar Ascent and Rendezvous with an Orbiting Vehicle—H. U. Burri: IAS Second Manned Space Flight Meeting, Dallas, Texas, Apr. 1963

Laser Communications—D. J. Parker: Phila. Section of the Optical Society of America, May 2, 1963

Indexing a Random Access File—W. Rodenki: RCA Computer Users Association, Buffalo, N. Y., June 4, 1963

On the Solution of Information Retrieval Problems—Dr. B. Sams: American Federation of Information Processing Societies, Detroit, Mich., May 23, 1963



AS REPORTED BY RCA DOMESTIC PATENTS, PRINCETON

RCA LABORATORIES

3,092,782—Solid State Traveling Wave Parametric Amplifier, June 4, 1963; K. K. N. Chang

3,092,998—Thermometers, June 11, 1963; L. E. Barton

3,093,817—Magnetic Systems, June 11, 1963; J. A. Rajchman and A. W. Lo.

3,094,612—Microwave Adder Circuit, June 18, 1963; F. Sterzer

3,094,634—Radioactive Batteries, June 18, 1963; P. Rappaport

3,095,533—Voltage Control Circuits, June 25, 1963; E. O. Keizer

3,096,219—Semiconductor Devices, July 2, 1963; H. Nelson

3,096,445—Square Wave Generator Comprising Negative Resistance Diode and Mismatched Delay Line Producing Steep Edge Pulses, July 2, 1963; G. B. Herzog

3,096,485—Diode Traveling Wave Parametric Amplifier, July 2, 1963; K. K. N. Chang

3,097,308—Semiconductor Device with Surface Electrode Producing Electrostatic Field and Circuits, July 9, 1963; J. T. Wallmark

3,097,312—Shift Register Including Two Tunnel Diodes per Stage, July 9, 1963; J. C. Miller

3,097,977—Semiconductor Devices, July 16, 1963; J. A. Amick and G. W. Cullen

3,098,170—Power Supply Circuit for Television Receivers, July 16, 1963; R. N. Rhodes

***3,093,788—Radioactive Power Supply System**, June 11, 1963; E. G. Linder
(*Assigned to U.S. Government)

DEFENSE ELECTRONIC PRODUCTS

3,091,876—Display Devices, June 4, 1963; D. A. Cole

3,092,694—Loudspeaker, June 4, 1963; S. Walczak

3,092,830—Decoder and Coder Circuit, June 4, 1963; D. P. Clock and G. A. Lucchi

3,097,349—Information Processing Apparatus, July 9, 1963; F. L. Putzrath and T. B. Martin

ELECTRONIC DATA PROCESSING

3,092,254—Control Apparatus, June 4, 1963; U. Germen

HOME INSTRUMENTS DIVISION

3,092,296—Tape Transport Mechanism, June 4, 1963; D. R. Andrews

3,092,734—Amplitude Limiter for AC Signals Using a Tunnel Diode, June 4, 1963; G. E. Theriault

3,093,334—Magnetic Recording and Reproducing Apparatus, June 11, 1963; D. R. Andrews

3,093,984—Coupling Mechanism, June 18, 1963; D. R. Andrews

3,096,399—Television Receiver Circuits, July 2, 1963; L. P. Thomas, Jr.

BROADCAST AND COMMUNICATIONS DIV.

3,092,345—Braking Mechanisms, June 4, 1963; R. W. Clayton and A. E. Jackson

ELECTRONIC COMPONENTS AND DEVICES

3,094,957—Brazing Jig for Electron Tube Fabrication, June 25, 1963; H. V. Knauf

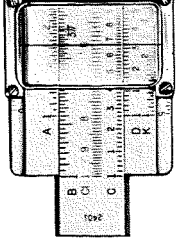
3,096,184—Glass Marking Ink, July 2, 1963; J. L. Gallup

3,096,458—Electroluminescent Device, July 2, 1963; R. C. Demmy

3,097,555—Apparatus for Notching Vacuum Tube Grid Lateral Wire, July 16, 1963; C. W. Lindsley

3,097,621—Brazing Jig for Electron Tube Fabrication, July 16, 1963; G. A. Lalak

Engineering NEWS *and* HIGHLIGHTS



RCA EARNINGS SET ALL-TIME RECORDS FOR FIRST HALF OF 1963

RCA set all-time sales and earnings records in the first half of 1963. The second quarter results provided the ninth consecutive quarter in which RCA's earnings have exceeded the comparable period of the previous year.

For the first half of 1963, profits after taxes rose to a new peak of $29.4 million, an increase of 23 percent over earnings of $24.0 million in the first 6 months of 1962. Sales rose 3 percent to a new first half high of $877.3 million compared with $853.9 million a year earlier. Earnings per share for the 6 months ended June 30, 1963 totaled $1.60, as against $1.32 in the similar 1962 period.

In a joint announcement, **General Sarnoff** and **Dr. Engstrom** said that the steady upward progression of RCA's earnings is expected to continue through 1963 and beyond if the national economy encounters no unforeseen reversals. They stated:

". . . The research and planning begun more than a decade ago for products such as color television are now being translated into rising sales and profits and a leading position in the industry. At the same time, the favorable effects of these developments have been intensified by a profit-oriented management group . . . We believe we have today a stronger management team . . . than at any time in RCA's history.

"No single product or service can account for the continuing improvement . . . From broadcasting to space satellites, from worldwide electronic servicing operations to computer sales and rentals, the impact of progress was registered . . .

"RCA now has more than 550 computer systems currently installed or on order. During the second quarter, we received our largest single domestic order for electronic data processing systems—a lease contract for thirty RCA 301 systems from the U. S. Air Force Logistics Command. Electronic Data Processing is advancing according to plan toward a crossover into profitability during the fourth quarter of 1964.

"In color television, the expansion and intensification of competition has not reversed our position of leadership—a position we fully intend to maintain. It is significant that the month of June, normally a period of seasonal decline, produced 48 percent more RCA color set sales than the previous peak month of September, 1962. With black and white set sales also moving strongly, the Home Instruments Division had its best second quarter and first half in history.

"RCA's growing role in space was underlined by the successful launching of the seventh TIROS weather satellite, by the successful completion of seven months of orbital tests with the RCA-built RELAY communications satellite and by the start of work on RCA's portion of NASA's Project APOLLO—the manned landing on the moon. As a major subcontractor to Grumman Aircraft Engineering Corporation, RCA's share of the APOLLO Project is expected to be in excess of $40 million.

"The National Broadcasting Company . . . in both sales and profits . . . . surpassed its previous records . . . set in 1962.

"The overall performance during this period has reinforced our conviction . . . that RCA now stands on the firmest footing since its founding forty-four years ago."

SIMA WINKLER HONORED FOR SPACE ENGINEERING WORK

Mrs. Sima M. Winkler of the DEP Astro-Electronics Division, Princeton, N. J., has been honored for her work in space vehicle design, weather and communications satellites, and space-connected nuclear and radiation research. A member of AED's Advanced Projects and Operations Analysis group, Mrs. Winkler was among the eight recipients of the first *Salute to Women in Electrical Living Awards,* presented jointly by the New York Chapter of the Electrical Women's Round Table and the New York State Dept. of Commerce Women's Program.

THERIAULT HONORED FOR PAPER

On June 18, 1963 at the Chicago Spring Conference of the PTGBTR (IEEE Professional Technical Group on Broadcast and TV Receivers), **Gerald E. Theriault** of the Home Instruments Advanced Development Laboratory, Princeton, was awarded a scroll and $50.00. The scroll reads *"For the submission of an outstanding paper published in the Transactions on BTR entitled: Cross-modulation and Modulation Distortion of RF Transistors."—D. Carlson*

RCA DIRECT ENERGY CONVERSION FILM AVAILABLE

The Direct Energy Conversion Department of Electronic Components and Devices, Harrison, has produced a 16mm color motion picture depicting RCA's role in the fast-moving field of direct energy conversion. The 20-minute, semitechnical film covers thermionic energy conversion, thermoelectric energy conversion, solar cells, batteries, and superconductors. *(Editor's Note:* The next issue of the RCA ENGINEER, October-November 1963, will feature papers on these fields.)

Prints are available for both internal and external showings. Requests for prints, on a loan-and-return basis, should be directed to **R. F. Kelleher,** Advertising Department, RCA Electronic Components and Devices, Harrison, N. J. (phone extension TH-2371).

SURFCOM HONORED FOR INTERLOC MICROMOD PACKAGING DESIGN

The DEP Surface Communications Division has been honored by the IEEE Professional Group on Product Engineering and Production with a Design Award Citation for the INTERLOC Micromodule Packaging System. This high-density packaging system is a dovetailed strip-socket arrangement permitting individual module replacement without unsoldering. The design features automatic wire-wrapped interconnections in place of the conventional soldered printed circuit techniques. The citation was presented to **John W. Knoll,** Administrator, Microelectronics Engineering and Techniques, Camden, by the IEEE at a luncheon in Boston on May 28, 1963. **Donald Mackey,** Manager of Microelectronics Engineering and Techniques said that the award was won in a competition that included 40 companies.—*J. Gillespie*

DEP REORGANIZES

COMMUNICATIONS SYSTEMS DIVISION AND AEROSPACE SYSTEMS DIVISION CREATED BY COMBINING DSD, ACCD, AND SURFCOM

Effective September 1, 1963, the following changes were announced in Defense Electronic Products:

S. W. Cochran was appointed Division Vice President and General Manager, *Communications Systems Division.* This new division will encompass the activities of the former DEP Surface Communications Division and the communications activities of the former DEP Aerospace Communications and Controls Division. Division headquarters will be in Camden, New Jersey.

I. K. Kessler was appointed Division Vice President and General Manager, *Aerospace Systems Division.* This new division will encompass the activities of the former Data Systems Division (Van Nuys, Calif.) and the remaining activities of the former Aerospace Communications and Controls Division. Division headquarters will be in Burlington, Massachusetts.

Messrs. Cochran and Kessler will report to **W. G. Bain,** Vice President, Defense Electronics Products. The other two DEP product divisions remain as *Astro-Electronics Division* and the *Missile and Surface Radar Division.*

ENGSTROM RECEIVES HONORARY DEGREES

Dr. Elmer W. Engstrom, President of the Radio Corporation of America, recently received honorary degrees from four colleges and universities. On June 9 Dr. Engstrom was the Commencement speaker at Thiel College, Greenville, Pennsylvania, and received the honorary degree of Doctor of Laws. On June 15 Dr. Engstrom also delivered the Commencement address at Drexel Institute of Technology and received the honorary degree of Doctor of Engineering. At the 197th anniversary commencement of Rutgers University, held in Rutgers Stadium on June 5, Dr. Engstrom received the honorary degree of Doctor of Science. Also, at the commencement exercises at Franklin and Marshall College, Lancaster, Pennsylvania, he received the honorary degree of Doctor of Science.

NEW SCIENTIFIC COMPUTER CENTER AT RCA LABS WILL USE RCA 601 AND RCA 301

A new scientific data processing center is being constructed at RCA Laboratories, Princeton, N. J. The new facility, housing an RCA 601 computer in combination with an RCA 301, is scheduled for completion this fall. The center will be used for research in such areas as lasers, plasma physics, solid state theory, character recognition devices, advanced computer memories, and computer programming. It will be used not only by RCA Laboratories scientists but also by scientists and engineers from other RCA divisions for solving complex engineering and production problems. In addition, the center will be a backup facility for two RCA 601 customers—the New Jersey Bell Telephone Company and the New Jersey Public Service Gas and Electric Company.

. . . PROMOTIONS . . .

to Engineering Leader & Manager

As reported by your Personnel Activity during the past two months. Location and new supervisor appear in parenthesis.

RCA Service Company

P. C. Groot: from Engr., BMEWS to *Ldr., Engrs. BMEWS* (E. W. Amundsen, Site Engineering)

A. H. Shepard: from Ldr., Engrs. BMEWS to *Mgr., Facilities Engineering Oper. and Maint.* (A. J. Gustray, Facility and Support)

P. J. Barnette, Jr.: from Engr. to *Mgr., System Integration* (H. Reese, Jr., Nuclear and Scientific Svcs.)

J. E. Stuart: from Engr., to *Ldr., Engrs.* (R. E. Purvis, Engineering and Tech. Svcs.)

RCA Victor Co., Ltd.

J. M. Stewart: from Sr. Member of Scientific Staff to *Lab Director, Electronics* (Dr. J. R. Whitehead, Res. Labs.)

J. Soul: from Ldr., Comm. Eng. to *Supervisor* (V. E. Isaac, Special Products Group)

R. H. Colt: from Ldr., Defense Eng. to *Supervisor* (J. C. Barron, Defense Systems)

C. Tupinier: from Engr., to *Plant Mgr.* (H. E. Clogg, Cowansville, Que.)

D. N. Ross: from Admin., Product and System Mdsg. to *Mgr.* (B. R. Machum, Industrial Products Sales and Service)

J. E. H. Elvidge: from Engr., Comm. Eng. to *Ldr.* (G. F. Baylis, Comm. Eng.)

Electronic Components and Devices

L. A. Murray: from Engr. to *Engineering Ldr.* (A. Rose, Somerville)

C. Turner: from Engineering Ldr. to *Mgr. Applications* (D. Donahue, Somerville)

Data Systems Division, DEP

E. Wendkos: from Prin. Member, Dev. and Des. Eng. Staff to *Ldr., Dev. and Des., Eng. Staff* (A. Davies, Act. Mgr.)

M. Anderberg: from Sr. Member, Dev. and Des., Eng. Staff to *Ldr., Dev. and Des., Eng. Staff* (G. Grondin, Van Nuys)

A. Rosenberg: from Sr. Publications Eng. to *Ldr., Publications Eng.* (S. Hersh, Van Nuys)

Astro-Electronics Division, DEP

L. A. Freedman: from Sr. Eng. to *Ldr. Engrs., Eng.* (J. E. Dilley, Mgr., Special Camera Systems)

M. Hollander: from Ldr., Engrs. to *Mgr., Eng. Reports and Proposals, Publications Services* (L. A. Thomas, Mgr., Publication Svcs.)

L. P. Hunneman: from Engr. to *Ldr., Publication Engrs., Publications Svcs.* (M. Hollander, Mgr., Reports and Proposals)

J. Kiesling: from Engr. to *Ldr., Engrs., Eng.* (R. B. Marsten, Act. Mgr., Systems Eng.)

S. Skarlatos: from Eng. Editorial Assistant to *Mgr., Graphic Arts Production, Publications Svcs.* (L. A. Thomas, Mgr., Publication Svcs.)

K. Greene: from Sr. Eng. to *Ldr., Engrs., Eng.* (V. R. Monshaw, Mgr., Program Reliability)

J. W. Jones: from Sr. Eng. to *Ldr. Eng. Systems Projects* (C. T. Cole, Mgr., Program P417)

G. King: from Sr. Eng. to *Ldr. Eng. Systems Projects* (C. T. Cole, Mgr., Program P417)

E. Miller: from Ldr. Eng. Systems Projects to *Mgr., APOLLO TV Project, Projects* (C. S. Constantino, Mgr., Equipment Projects)

J. E. Mortimer: from Engr. to *Ldr., Engrs., Eng.* (S. H. Fairweather, Mgr., Propulsion Systems)

R. A. Smith: from Engr. to *Ldr., Engrs., Eng.* (V. R. Monshaw, Mgr., Program Reliability)

Aerospace Communications and Controls Division—DEP

F. F. Dupre: from Sr. Eng. Scientist, Tech. Staff to *Mgr., Eng. Planning* (H. J. Woll, Burlington)

RCA Communications, Inc.

J. Goldberg: from Design Engr. to *Group Ldr., Terminal Facilities, Installation Design* (E. M. Gaetano, N.Y.)

Electronic Data Processing

P. Kircher: from Methods Analyst Programmer to *Ldr., Product Support* (R. O. Austin, Palm Beach)

H. Peters: from Sr. EDP Product Support Specialist to *Ldr., Product Support* (R. O. Austin, Palm Beach)

DEGREES GRANTED

E. L. Ressler, BCPD, Camden ..... BS, Physics, LaSalle College
J. H. Pierce, BCPD, Camden ..... BS Drexel Institute of Technology
A. Skele, Rec. Div., Indianapolis ..... MS, Engineering, Purdue University
J. E. Gallo, ACCD, Camden ..... MS, Engineering, University of Pennsylvania
R. F. Trump, SurfCom, Camden ..... MSSE, Rutgers University
P. G. Dearman, SVC. Co., P.A.F.B., Florida .. Assoc., Engrg., Brevard Engineering College
J. W. Gillis, Svc. Co., P.A.F.B., Florida ..... Assoc., Engrg., Brevard Engineering College
F. L. LeMosy, Svc. Co., P.A.F.B., Florida ..... Assoc., Engrg., Brevard Engineering College
D. A. Ritchley, Svc. Co., P.A.F.B., Florida .... Assoc., Engrg., Brevard Engineering College
L. Gibbons, ECD, Somerville ..... MS, Electrical Engineering, Rutgers University
B. Czorney, ECD, Somerville ..... MS, Chem. Engrg., Newark College of Engineering
D. Nichols, ECD, Somerville ..... BS, Metallurgy, Drexel Institute of Technology
C. VandeZande, ECD, Somerville ..... MS, Statistics, Rutgers University
J. Handen, ECD, Somerville ..... MS, Statistics, Rutgers University
R. Krallinger, ECD, Somerville ..... MS, Electrical Engineering, Rutgers University
C. Drake, ECD, Somerville ..... MS, Industrial Engrg., Stevens Institute of Technology
R. Citron, ECD, Somerville ..... MSA, Management, Seton Hall
F. A. Hartshorne, ACCD, Camden ..... MSEE, Drexel Institute of Technology
W. C. Luebkemann, MMSR, Moorestown ..... BSEE, Drexel Institute of Technology
J. A. Arico, ECD, Harrison ..... BSEE, Newark College of Engineering
G. W. Barclay, ECD, Harrison ..... MSEE, Stevens Institute of Technology
F. Kolondra, ECD, Harrison ..... BSEE, Newark College of Engineering
E. L. Lattanzio, ECD, Harrison ..... BSEE, Newark College of Engineering
W. Nething, ECD, Harrison ..... BSME, Fairleigh Dickinson University
R. V. Nikiel, ECD, Harrison ..... MSIE, Stevens Institute of Technology
H. Noterius, ECD, Harrison ..... MS, Stevens Institute of Technology
R. J. Rundstedt, ECD, Harrison ..... MSEE, Stevens Institute of Technology
S. Sarowitz, ECD, Harrison ..... MSME, University of the City of New York
E. J. Triano, ECD, Harrison ..... MSEE, Newark College of Engineering
G. Simmons, ECD, Harrison ..... BSME, Newark College of Engineering
R. Donohue, ECD, Harrison ... MS, Engrg. Management, Newark College of Engineering
R. Askew, ECD, Harrison ..... BSEE, Newark College of Engineering
A. A. Rotow, ECD, Lancaster ..... Ph.D. in EE, University of Pennsylvania
J. F. Heagy, ECD, Lancaster ..... MS, Physics, Franklin & Marshall College
R. L. Stegall, DEP-MSR, Moorestown ..... MSEE, University of Pennsylvania
R. J. Ryan, ECD, Somerville ..... MS in Chemistry, Drexel Institute of Technology
P. K. Baltzer, RCA Labs., Princeton ..... Ph.D. in Physics, Rutgers University
N. J. Imperial, ECD, Somerville ... MBA, Management & Statistics, New York University
F. Romig, ECD, Somerville ..... MS, Applied Statistics, Rutgers University
J. A. Zena, ECD, Somerville ..... MS, Retailing, New York University
E. F. Kopec, ECD, Somerville ..... BS, Management, Rutgers University
C. Srinivason, RCA Labs., Princeton ..... Eng. Sc. D., Columbia University
S. Siskind, AED, Hightstown ..... MA, Physics, Temple University
J. G. Bakos, ACCD, Camden ..... BS, Industrial Management, LaSalle College

NEW RECORD DISTRIBUTION CENTER

The RCA Victor Record Division has started construction in Indianapolis on a Record Distribution Center. When completed next year, the new center will provide more than 300,000 square feet of floor space for the Division's inspection, packing, warehousing, and the world-wide distribution operations.

BCP TO CONSOLIDATE ANTENNA FACILITIES AT ENLARGED GIBBSBORO SITE

The Broadcast and Communications Products Division plans to consolidate its engineering, laboratory, and assembly facilities for broadcast antennas at its 40-acre Gibbsboro, N. J., test area and to erect a new building there to accommodate the enlarged operation. [*Editor's Note:* See H. E. Gihring, "The Broadcast Antenna Facility," RCA ENGINEER, Oct.-Nov. 1962.]

The move is intended to give RCA the most modern facilities in the broadcast equipment industry for the production of radio and TV station antennas. The improved facilities are needed to handle an unprecedented volume of antenna business which has given the Division the largest backlog of orders for antennas in its history. The high level of business is expected to continue indefinitely as existing broadcast stations upgrade their transmission facilities, and new UHF educational and commercial TV stations are built.

The consolidation will bring to the Gibbsboro site the B&CP antenna engineering, laboratory, assembly facilities, and employees now located at Buildings 53 and 57 in Camden. In addition to eliminating travel among the three separate locations, the centralization will provide the most modern materials handling facilities, an important consideration in fabricating antennas up to 140 feet in length and 15 tons in weight.

STAFF ANNOUNCEMENTS

EC&D - Technical Programs: The organization of Technical Programs, reporting to **A. M. Glover,** Division Vice-President, Technical Programs, is: **E. O. Johnson,** Manager, Engineering; **R. L. Kelly,** Administrator, Product Assurance; and **A. M. Glover,** Acting Manager, New Business Development.

EC&D - Industrial Tube and Semiconductor Division: The organization of EC&D-IT&SD, reporting to **C. E. Burnett,** Division Vice President and General Manager, IT&SD, is: **G. W. Duckworth,** Mgr., Marketing Dept.; **D. W. Epstein,** Mgr., Conversion Tube Operations Dept.; **C. H. Lane,** Mgr., Industrial Semiconductor Operations Dept.; **C. F. Nesslage,** Mgr., Financial Controls and Planning; **C. C. Simeral, Jr.,** Mgr., Microwave Tube Operations Dept.; **E. E. Spitzer,** Mgr., Power Tube Operations Dept.; and **S. White,** Mgr., Operations Services.

EC&D - Special Electronic Components Division: The organization of EC&D-SECD, reporting to **L. R. Day,** General Manager, SECD, is: **D. W. Chace,** Mgr., Administration; **L. R. Day,** Acting Mgr., Direct Energy Conversion Dept.; **N. S. Freedman,** Mgr., Special Project Development; and **R. E. Koehler,** Mgr., Microelectronics Dept.

EC&D Television Picture Tube Division: The organization of EC&D-TPTD, reporting to **J. B. Farese,** Division Vice President and General Manager, TPTD, is: **M. J. Carroll,** Mgr., Marketing Dept.; and **H. R. Seelen,** Mgr., Television Picture Tube Operations Dept.

EC&D - Commercial Receiving Tube and Semiconductor Division: The organization of EC&D-CRT&SD, reporting to **W. H. Painter,** Division Vice President and General Manager, CRT&SD, is **F. R. Buchanan,** Mgr., Financial Planning and Controls; **H. A. DeMooy,** Mgr., Receiving Tube Operations Dept.; **N. H. Green,** Mgr., Commercial Semiconductor Operations Dept.; **G. J. Janoff,** Mgr., Marketing Dept.; **K. M. McLaughlin,** Mgr., Memory Products Dept.; and **W. H. Painter,** Acting Mgr., Services.

DEP Missile and Surface Radar Division, Moorestown: The organization of DEP-M&SR, reporting to **J. H. Sidebottom,** Division Vice President and General Manager, is: **W. H. Congdon,** Mgr., Tactical Systems Programs; **F. J. Drakeman,** Plant Mgr., Mooretown Plant; **W. R. Frysztacki,** Mgr., Operations Control; **E. Gerjuoy,** Director, Plasma and Space Applied Physics; **A. L. Hammerschmidt,** Chief Engineer, Engineering Dept.; **C. M. Lewis,** Mgr., Marketing Dept.; **A. Mason,** Mgr., Strategic and Defensive Systems Programs; **C. B. McGinley,** Mgr., Moorestown Personnel; **H. J. Morley,** Purchasing Agent, Purchasing; **E. W. Petrillo,** Mgr., Range Systems Program; **W. L. Richardson,** Mgr., Program Management and Planning; and **M. W. Rogers,** Mgr., Product Assurance.

RCA Victor Ltd., Montreal, Canada: **R. G. Power** has been appointed Manager of the Semiconductor Department; **J. Almond,** who held the position temporarily, will return to a senior position in the Research Laboratories.

RCA Victor Record Division: **A. L. McClay** is now Mgr., Record Operations Dept., reporting to **N. Racusin,** Division Vice President and Operations Mgr. The organization of the Department is: **R. A. Bradel,** Purchasing Agent; **R. A. Lynn,** Administrator, Quality; **R. O. Price,** General Plant Mgr.; **A. A. Pulley,** Adm., Audio Engineering Red Seal Recording; **D. L. Richter,** Mgr., Recording; **H. E. Roys,** Chief Engr., Engineering; and **A. Stevens,** General Plant Engineer.

RCA Laboratories, Princeton: **L. H. Good,** formerly at RCA Somerville, is now on assignment with Project PANGLOSS.

DEP & EDP, Staff of Group Executive Vice President: **C. M. Mooney** has been appointed to the newly established position of Division Vice President, Federal Government Systems Support, reporting to **A. L. Malcarney,** Group Executive Vice President. Mr. Mooney will be the senior representative of RCA in its marketing efforts with the Federal Government in Washington, D.C., and will be available for marketing counsel and guidance to all RCA Divisions doing business with the Federal Government. He will provide administrative and business counsel to the Federal Government Office activities of DEP and EDP. (Profit responsibility for these activities will be retained by DEP and EDP.) The Data Systems Center, Bethesda, Md. formerly part of DEP-DSD, will report directly to Mr. Mooney.

GLICKSMAN NAMED HEAD OF RCA JAPANESE LABORATORY

Dr. Maurice Glicksman, of the Microwave Research Laboratory, has been appointed the new Director of Research of Laboratories RCA, Inc., in Tokyo. Dr. Glicksman is expected to assume his new duties about July 1.

Dr. Glicksman succeeds **Dr. Martin C. Steele,** who has been head of research at the Japanese Laboratory since its inception. Dr. Steele, who is returning to the David Sarnoff Research Center, will assume responsibility for the plasma research being done in the Microwave Research Laboratory. (See article on Tokyo Laboratories by Dr. Steele in June-July 1963 RCA ENGINEER.)

$11.6 MILLION EXPANSION PLANNED FOR LANCASTER TUBE PLANT

Plans were recently announced for an $11.6 million expansion program at the Lancaster, Pa., tube plant to provide an additional 200,000 square feet for color TV picture-tube engineering and conversion-tube manufacturing operations. **D. Y. Smith,** Vice President, RCA Electronic Components and Devices, said the expansion involves the construction of two new building additions, one of which will devote 46,000 square feet to color TV picture-tube engineering. The other 154,000-square-foot addition, to be undertaken first, will enlarge the plant's conversion-tube operations, which include image-orthicon and vidicon camera tubes, image converters, display storage tubes, phototubes, and photomultipliers.

Several hundred additional employees probably eventually will be required as part of the expansion program. The Lancaster plant presently has a work force of approximately 4,000. The first addition will be ready within the next 21 months. Ground breaking plans for the second addition are not yet final, but will not take place before occupancy of the first addition.

The new color-tube engineering building will be attached to the present administration building, and will supplement the 400,000 square feet now assigned to color picture tube operations in Lancaster. Color-tube design, application, chemical and physics engineering will be conducted in this new area.

The new manufacturing and engineering facility will be utilized for conversion tube manufacturing, engineering, and advanced development, as well as for a chemical and physics laboratory and administration offices.

15 CHILDREN OF RCA EMPLOYEES AWARDED RCA NATIONAL MERIT SCHOLARSHIPS

Fifteen high school seniors, 11 boys and 4 girls, have been named winners of the *1963 RCA National Merit Scholarships* for children of RCA employees, as announced recently by **Dr. Douglas H. Ewing,** Vice President and Technical Director, RCA. Each year, in cooperation with the National Merit Scholarship Corporation, RCA sponsors a maximum of 15 four-year college scholarships, carrying stipends up to $1,500 annually, for the children of RCA employees. The *RCA Merit Scholarship Program* is part of RCA's aid-to-education program, established in 1945, and directed by the RCA Education Committee, of which Dr. Ewing is Chairman. (See Dr. Ewing's article "RCA Aid to Education," in RCA ENGINEER, Vol. 8, No. 4, Dec. 1962-Jan. 1963.)

The RCA Merit Scholars for 1963 are:

Robert B. Ehrman, Westfield, N. J., will enroll at Denison University, Granville, Ohio, in political science. His father, George A. Ehrnman, is with RCA International Division, Clark, N. J.

William F. Aikman, Ridley Park, Pa., will enroll at Brown University, Providence, R. I., in political science. His father, John E. Aikman, is with the RCA Service Company, Collingdale TV Branch, Pa.

Mary Grace Birrel, Cocoa Beach, Fla., will enroll at Stetson University, De Land, Fla., in mathematics. Her father, David J. Birrel, is with the RCA Service Company, Cocoa Beach, Fla.

Thomas S. Ferguson, Jr., Oceanside, N. Y., will enroll at Brown University, Providence, R. I. in applied mathematics. His father, Thomas Ferguson, is with the RCA Service Company, Franklin Square TV Branch, N. Y.

John L. Marshall, Portland, Maine, will enroll at Massachusetts Institute of Technology, Cambridge, Mass., majoring in chemical engineering. His father, Robert M. Marshall, is with the RCA Service Company, at Roi-Namur, Marshall Islands.

Justin J. O'Connor, Rockville Centre, N. Y., will enroll at Boston College, Boston, Mass., in English. His father, Justin J. O'Connor (deceased), was with the RCA Electronic Data Processing, New York.

John P. Shipley, Jr., Birmingham, Mich., will enroll at the University of Michigan, Ann Arbor, Mich., in physics. His father, John P. Shipley, is with the Broadcast & Communications Products Division in Michigan.

Susan T. Dworkin, Yonkers, N. Y., will enroll at Swarthmore College, Swarthmore, Pa., in English Literature. Her father, Lawrence J. Dworkin, is with NBC-TV in New York City.

Sylvia R. Babcoke, Kansas City, Kan., will enroll at Ottawa University, Oakland, Kansas, in mathematics. Her father, Carl H. Babcoke, is with the RCA Victor Distributing Corp., in Kansas City, Kan.

Faith P. Dreher, Camden, N. J., will enroll at a college still to be determined in history. Her father, Robert L. Dreher, is with Missile & Surface Radar Division at Moorestown, N. J.

Richard L. Handelsman, Princeton, N. J., will enroll at Princeton University in liberal arts. His father, Dr. Morris Handelsman, is with Advanced Military Systems in Princeton, N. J.

John C. Lewis, Moorestown, N. J., will enter Swarthmore College, Swarthmore, Pa., in political science. His father, C. M. Lewis, is with the Missile & Surface Radar Division at Moorestown, N. J.

John M. Pesando, Lexington, Mass., will enroll at Harvard College, Cambridge, Mass., in engineering. His father, Mario Pesando, is with Defense Electronic Products at Burlington, Mass.

Ernest F. Raeuber, Westmont, N. J., will enroll at Boston College in Latin. His mother, Ellen T. Raeuber, is with Defense Electronic Products at Camden, N. J.

Philip J. Werner, Riverside, N. J., will enroll at Michigan State University in aeronautical engineering. His mother, Lorraine Werner, is with Missile and Surface Radar Division at Moorestown, N. J.

MAJOR NEW IEEE JOURNAL TO SERVE GENERAL TECHNICAL AUDIENCE

The IEEE (Institute of Electrical and Electronics Engineers) recently announced the inauguration of a major new journal to serve its 150,000 members and the scientific community at large.

Effective January 1964, the IEEE will publish two primary monthly periodicals: One will be a totally new journal, *IEEE Spectrum* which will be distributed to all IEEE members (except student members). Its primary editorial mission will be to present technical articles of high professional quality written so as to be meaningful to a wide audience. The subject matter will cover the entire spectrum of electrical and electronics engineering. Special emphasis will be placed on the clarity of the articles—both staff written and contributed by leading authorities in the field—to ensure that members can grasp and keep abreast of important technical developments outside their own particular fields of specialization. *Such a journal has long been needed to serve the complex field of electronics.*

The *IEEE Spectrum* will include review, tutorial, and application papers; occasional theoretical papers of outstanding significance; news of the profession and of the Institute; letters to the editor; abstracts; book reviews and other departments.

The second monthly periodical, *Proceedings of the IEEE,* will be available to members and nonmembers on a subscription basis only. (Previously, this was the only primary journal of the IEEE distributed automatically to all members.) A continuation of the present publication with that title, but expanded to embrace all fields served by the IEEE, the *Proceedings* will be a research-oriented journal for advanced papers of broad and lasting significance. It will provide an avenue for introducing scientific discoveries and new concepts into the electrical and electronics engineering field. Special issues will be published from time to time to lay a foundation for the development of newly emerging fields.

In addition these primary periodicals, the IEEE will continue to publish the various *IEEE Transactions* in each of a number of specialized fields, now totalling 33, that are served by IEEE Professional Technical Groups and Technical Committees. The *IEEE Student Journal* will continue to be published for 27,000 student members. In addition, special publications devoted to convention and conference papers will be published from time to time.

FOUR SURFCOM MEN BEGIN NEW DEP PROGRAM MANAGEMENT COURSE

Four men from the DEP Surface Communications Division have started a year-long Program Management course developed by the DEP Training activity. The course's object is to supplement DEP's normal management development processes in which high level management positions are filled from within RCA.

The four men are **H. J. Hamlin,** Administrator, Technical Projects Coordination, Command and Control Communications Engineering; **Douglass A. Lesser,** Leader, Minuteman Program Management Office; **Daniel A. Tannenbaum,** Manager, Engineer Systems Projects, QRC Program; and **Allan A. Weissburg,** Manager, Program Controls, Minuteman Production Program Management Office. Mr. Weissburg is from Cambridge, Ohio; the other three are from Camden.

Mr. Lesser and Mr. Tannenbaum are now attending a four-week course in executive management at Pennsylvania State University, and Mr. Hamlin and Mr. Weissburg are taking a similar course at Syracuse University. The remainder of the Program Management course includes guest lecturers; in-house management skills seminars; training sessions by the American Management Association, the National Defense Education Institute, and the American Management Institute; and temporary assignments in various RCA operating departments as well as at customer facilities.

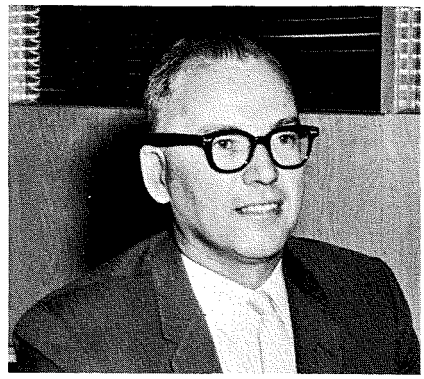
TIROS VII ORBITED—SEVEN OUT OF SEVEN FOR AED

The highly successful NASA weather satellite program was extended on June 19, 1963 with the orbiting of the TIROS VII meteorological satellite. The successful TIROS series holds a record achievement of seven satellites orbited and operationally successful—in seven tries.

Both TIROS VII and its predecessor TIROS VI are expected to operate in conjunction, providing dual and extended weather observations. TIROS VII's launch date was planned for an earlier time, but because of the excellent performance and longevity of TIROS V and VI, the date was deferred. TIROS VI, launched Sept. 18, 1962, has been televising photographs to earth for 9½ months—far exceeding the 90-day mission requirement—and has transmitted over 54,000 photographs, 89 percent of which have been usable for weather information. Over 1,200 of these were used by the MERCURY weather operation for Major Cooper's 22-orbit flight, and for Walter Schirra's flight during October 1962.

TIROS V, launched June 19, 1962, operated for 10½ months and transmitted over 58,200 earth cloud cover photographs of which 80 percent were usable for meteorological purposes. The U. S. Weather Bureau sent 396 storm advisories to nations around the world based on TIROS V's cover pictures providing first warning on half of the world's ten most serious tropical storms during August 1962.

TIROS VII, although similar in appearance ance, differs from its predecessors in experiments carried and overall weight—300 pounds compared to the 275 to 285 pounds of TIROS I through VI. The DEP Astro-Electronics Division was recently awarded a follow-on TIROS contract for seven additional spacecraft by NASA's Goodard Space Flight Center.



W. C. Praeger

W. C. PRAEGER NAMED ED REP FOR DEP-CSD, CAMBRIDGE, OHIO

W. C. Praeger has been named to succeed **P. J. Riley** as RCA ENGINEER Editorial Representative for the Cambridge, Ohio plant of the DEP Communications Systems Division. He will serve on **F. D. Whitmore's** DEP Editorial Board.

William C. Praeger graduated with honor from Clarkson College of Technology in 1947 with a BEE, and is presently engaged in publications coordination for Cambridge Product Engineering in the DEP Communications Systems Division. Bill was previously involved in documentation and publications at SurfCom's MINUTEMAN PMO in Camden, and BMEWS tech-manual program administration at MSR, Mooretown. Prior to that he spent eleven years in publications with the Electronics Division of Westinghouse Electric Corporation in Baltimore. Bill is a member of the IEEE, the Professional Group on Engineering Writing and Speech, the Society for Technical Writers and Publishers, and Tau Beta Pi.

EDITOR'S NOTE: *The regular* Professional Activities *column will appear in the next issue and will bring up to date the news items recently submitted.*

Clip out and Mail to Editor, RCA ENGINEER, #2-8, Camden

RCA ENGINEER

HAVE WE YOUR CORRECT ADDRESS?

If not indicate the change below.

PLEASE INDICATE THE CODE LETTER(S) THAT APPEAR NEXT TO YOUR NAME ON THE ENVELOPE.

Name _____ Code _____

Street or Bldg. _____

City and State or Plant _____

Editorial Representatives

The Editorial Representative in your group is the one you should contact in scheduling technical papers and announcements of your professional activities.

DEFENSE ELECTRONIC PRODUCTS

F. D. WHITMORE *Chairman, Editorial Board, Camden, N. J.*

Editorial Representatives

Aerospace Systems Division

D. B. DOBSON *Systems Support Eng., Burlington, Mass.*

R. B. GLENDON *Technical Administration, Burlington, Mass.*

S. HERSH *Data Systems Eng., Van Nuys, Calif.*

G. LIEBERMAN *Systems Engineering, Camden, N. J.*

Astro-Electronics Division

I. SEIDEMAN *Engineering, Princeton, N. J.*

Missile & Surface Radar Division

I. N. BROWN *Systems Engineering, Moorestown, N. J.*

T. G. GREENE *Engineering Dept., Moorestown, N. J.*

Communications Systems Division

C. W. FIELDS *Engineering, Camden, N. J.*

J. F. GIBBINGS *Systems Labs., Tucson, Ariz.*

R. B. HINES *Engineering Services, Camden, N. J.*

W. C. PRAEGER *Engineering, Cambridge, Ohio*

M. P. ROSENTHAL *Systems Labs., New York, N. Y.*

Defense Engineering

J. J. LAMB *Central Engineering, Camden, N. J.*

G. E. MORRIS *Advanced Military Systems, Princeton, N. J.*

M. G. PIETZ *Applied Research, Camden, N. J.*

FEDERAL GOVERNMENT SYSTEMS SUPPORT

H. J. CARTER *Data Systems Center, Bethesda, Md.*

BROADCAST AND COMMUNICATIONS PRODUCTS DIVISION

D. R. PRATT *Chairman, Editorial Board, Camden, N. J.*

Editorial Representatives

N. C. COLBY *Mobile Communications Engineering, Meadow Lands, Pa.*

H. E. GIHRING *Brdcst. Transmitter & Antenna Eng., Gibbsboro, N. J.*

C. E. HITTLE *Closed Circuit TV & Film Recording Dept., Burbank, Calif.*

D. G. HYMAS *Microwave Engineering, Camden, N. J.*

R. N. HURST *Studio, Recording, & Scientific Equip. Engineering, Camden, N. J.*

D. H. MCCONNELL *Industrial & Automation Products Engineering, Plymouth, Mich.*

ELECTRONIC DATA PROCESSING

T. T. PATTERSON *Technical Publications Administrator, EDP, Camden, N. J.*

R. R. HEMP *Palm Beach Engineering, West Palm Beach, Fla.*

B. SINGER *Data Communications Engineering, Camden, N. J.*

H. H. SPENCER *Computer Advanced Development, Pennsauken, N. J.*

ELECTRONIC COMPONENTS AND DEVICES

J. F. HIRLINGER *Chairman, Editorial Board, Harrison, N. J.*

Editorial Representatives

Commercial Receiving Tube & Semiconductor Division

H. J. CARTER *Semiconductor Operations, Somerville, N. J.*

P. L. FARINA *Receiving Tube Operations, Harrison, N. J.*

J. KOFF *Receiving Tube Operations, Woodbridge, N. J.*

G. R. KORNFELD *Memory Products Dept., Needham and Natick, Mass.*

R. J. MASON *Receiving Tube Operations, Cincinnati, Ohio*

J. D. YOUNG *Semiconductor Operations, Findlay, Ohio*

Television Picture Tube Division

J. D. ASHWORTH *Television Picture Tube Operations, Lancaster, Pa.*

J. H. LIPSCOMBE *Television Picture Tube Operations, Marion, Ind.*

Industrial Tube & Semiconductor Division

H. J. CARTER *Semiconductor Operations, Somerville, N. J.*

R. L. KAUFFMAN *Conversion Tube Operations, Lancaster, Pa.*

M. N. SLATER *Semiconductor and Conversion Tube Operations, Mountaintop, Pa.*

G. G. THOMAS *Power Tube Operations and Operations Svcs., Lancaster, Pa.*

H. J. WOLKSTEIN *Microwave Tube Operations, Harrison, N. J. and Los Angeles, Calif.*

Special Electronic Components Division

P. L. FARINA *Direct Energy Conversion Dept., Harrison, N .J.*

J. SWENTZEL *Microelectronics Dept., Somerville, N. J.*

RCA VICTOR HOME INSTRUMENTS

K. A. CHITTICK *Chairman, Editorial Board, Indianapolis*

Editorial Representatives

J. J. ARMSTRONG *Resident Eng., Bloomington, Ind.*

D. J. CARLSON *Advanced Devel., Princeton, N. J.*

R. C. GRAHAM *Radio "Victrola" Product Eng., Indianapolis, Ind.*

P. G. MCCABE *TV Product Eng., Indianapolis, Ind.*

J. OSMAN *Electromech. Product Eng., Indianapolis, Ind.*

L. R. WOLTER *TV Product Eng., Indianapolis, Ind.*

RCA SERVICE COMPANY

A. L. CHRISTEN *EDP Svc. Dept., Cherry Hill, N. J.*

W. W. COOK *Consumer Products Svc. Dept., Cherry Hill, N. J.*

E. STANKO *Tech. Products Svc. Dept., Cherry Hill, N. J.*

M. W. TILDEN *Govt. Svc. Dept., Cherry Hill, N. J.*

RCA COMMUNICATIONS, INC.

W. C. JACKSON *RCA Communications, Inc., New York, N. Y.*

RCA VICTOR RECORD DIVISION

M. L. WHITEHURST *Record Eng., Indianapolis, Ind.*

NATIONAL BROADCASTING COMPANY, INC.

W. A. HOWARD *Staff Eng., New York, N. Y.*

RCA INTERNATIONAL DIVISION

L. S. BEENY *Clark, N. J.*

RCA VICTOR COMPANY, LTD.

H. J. RUSSELL *Research & Eng., Montreal, Canada*

RCA LABORATORIES

C. W. SALL *Research, Princeton, N. J.*